UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2022-00615
Patent No. 7,619,912

PATENT OWNER PRELIMINARY RESPONSE

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EXHIBIT LIST

Exhibit No.	Document
EX2001	Complaint for Patent Infringement and Summons in *Netlist, Inc., v. Google, Inc.*, Case No. 4:09-cv-05718 ("Google Action"), filed December 4, 2009.
EX2002	Complaint for Patent Infringement and Summons in *Netlist Inc. v. Inphi Corp.*, Case No. 2:09-cv-06900, filed September 22, 2009.
EX2003	Google's Reply In Support of Its Motion to Strike Netlist, Inc.'s New Assertion of Claim 16 (Redacted), Google Action, filed August 27, 2021.
EX2004	Google's Notice of Motion and Motion to Stay (Redacted), Google Action, filed June 3, 2022.
EX2005	Samsung's Answering Brief in Opposition to Netlist's Motion to Dismiss Plaintiff's First Amended Complaint, Case No. 1:21-cv-01453-RGA ("Delaware Action") filed March 2, 2022.
EX2006	Samsung's Reply Brief In Support of Its Motion for Leave To File Second Amended Complaint, Delaware Action, filed February 14, 2022.
EX2007	Declaration of Michael C. Brogioli, Ph.D.
EX2008	Sumit Adhikari, *[Update: Video] Samsung & Google Launch Ad Campaign Highlighting Their Partnership*, Android Headlines (July 5, 2022).
EX2009	David Curry, *Android Statistics (2022)*, Business of Apps (Updated: May 4, 2022).
EX2010	Dieter Bohn, *Sundar Pichai And Rick Osterloh Think The Pixel 6 Is Google's Breakout Phone*, The Verge (October 19, 2021).
EX2011	*A Decade in the Making: How Samsung Foldables Are Defining the Future of Smartphone Innovation*, Samsung Newsroom (December 31, 2021).
EX2012	*Samsung Galaxy Watches to Incorporate Wear OS*, Business Korea Daily News (May 20, 2021).

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Exhibit No.	Document
EX2013	*Samsung And Google Introduce The World's First Chromebook - Samsung Series 5 Samsung Creates Another*, Business Wire (May 11, 2021).
EX2014	*Samsung and Google Sign Global Patent License Agreement*, Samsung Global Newsroom (January 27, 2014).
EX2015	Netlist Inc.'s Amended Disclosure of Asserted Claims and Infringement Contentions, Google Action, as filed August 20, 2021.
EX2016	Inphi's Corrected Request for Reexamination, filed May 7, 2010, Reexamination Control No. 95/001,339.
EX2017	Netlist Inc.'s First Amended Complaint for Patent Infringement, Case No. 09-cv-6900, filed December 23, 2009.
EX2018	Samsung DDR3 SDRAM Memory Product Guide (October 2016).
EX2019	Samsung DDR4 SDRAM Memory Product Guide (May 2018).
EX2020	Inphi Corporation, 2010 Form 10-K (March 4, 2011).
EX2021	*Inphi to Partner With Samsung Semiconductor to Showcase LRDIMM Technology at VMworld 2012*, GlobeNewswire (August 21, 2012).
EX2022	Inphi Corporation, 2015 Form 10-K (February 29, 2016).
EX2023	ORDER Re: Motions for Summary Judgement and Related Applications, in *Netlist Inc. v. Samsung Electronics Co., Ltd.*, Case No. 8:20-cv-00993, filed October 14, 2021.
EX2024	Samsung's Reply In Support of Its Motion for Leave to File Sur-Reply Brief (D.I. 29), Delaware Action, filed April 13, 2022.
EX2025	Redline Comparison of EX1035 (U.S. Patent No. 7,363,422 to Perego) With Related U.S. Patent No. 7,356,639.
EX2026	Joint Claim Construction and Prehearing Statement Under Patent Local Rule 4-3, Google Action, filed June 25, 2010.
EX2027	*Why Samsung Needs To Move Beyond Android – And Google*, ComputerWorld (July 11, 2014).

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Exhibit No.	Document
EX2028	Smart Global Holdings, Inc. 2020 Form 10-K (October 22, 2020).
EX2029	Inphi's Feb. 13, 2012 Comments in Reexamination, Reexamination Control No. 95/001,339.
EX2030	Samsung Electronics Co., Ltd. 2021 Half-year Business Report.
EX2031	Xilinx, Programmable Logic Design Quick Start Handbook, (August 2003).
EX2032	*Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2022-00063, Paper 13 (P.T.A.B. May 5, 2022).
EX2033	*High-Speed Samsung LRDIMMs with Inphi Isolation Memory Buffer*, Principled Technologies (August 2012)
EX2034	Smart Modular Technologies (WWH), Inc., 2010 Form 10-K (November 3, 2010).

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STATEMENT OF MATERIAL FACTS IN DISPUTE

Petitioners did not submit a statement of material facts in this Petition. Accordingly, no response is due pursuant to 37 C.F.R. § 42.23(a), and no facts are admitted.

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I. INTRODUCTION[1]

This Petition represents a gross abuse of the post-grant review process at the USPTO. The '912 patent went through a decade-long reexamination process in which claim 16's validity was repeatedly affirmed by the Office, the Board, and the Federal Circuit. The nominal requestors were Google, Inphi and Smart Modular Technologies ("SM"). Google is one of the largest consumers of the memory modules in the world; and Samsung is the largest supplier of memory modules in the world, including for Google. Inphi (now Rambus) is one of Samsung's largest suppliers of the chips that are used in its memory modules. Google and Inphi were sued for infringement of the '912 patent in 2009.

In 2021, after the Federal Circuit affirmance, the suit against Google reinitiated. Samsung took two steps: it filed a declaratory judgment against the '912 patent and it filed this IPR. Netlist has never communicated with Samsung regarding the '912 patent. In pleadings in the District of Delaware, Samsung openly acknowledged that it was attacking the '912 patent because Google had demanded protection.

The IPR should be denied for three reasons: *First*, because Google is a real-party-in-interest ("RPI") and privy, the Section 315(b) statutory bar applies. *Second*,

[1] All emphases are added unless otherwise noted.

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this petition is an improper serial attack that recapitulates the same arguments considered and rejected by the Office, the Board, and the Federal Circuit for a decade. *Third*, the Petition is riddled with conclusory assertions that fail to make out a *prima facie* case.

II. RESPONSE LENGTH

Petitioner evaded the word limit set by the Board through its use of non-standard spacing. The Board held "[o]ur brief review of the Petitions reveals the presence of gamesmanship by using non-standard cites without spaces in an attempt to circumvent the word count requirement." Paper 6, 3. Based on this behavior, the Board granted Netlist 15,000 words for its response. *Id.*, 2-3. This was not a single isolated instance: Petitioner filed a set of IPRs against Netlist, all of which use the same tactics to evade the Board's word limits.

III. GOOGLE, SAMSUNG AND INPHI (RAMBUS) ARE EMPLOYING A STRATEGY OF SERIALLY ATTACKING THE '912 PATENT VALIDITY IN THE PATENT OFFICE

The '912 patent issued in 2009. It claims techniques that are used in certain rank-multiplied dual in-line memory modules ("DIMMs"). Google is one of the largest users of rank-multiplied memory modules covered by the '912 patent in the world. *See* Section IV.A.2(c). Samsung is the largest supplier of memory modules in the world, and Google is one if its largest customers. *See* Section IV.A.2(c). Inphi (Rambus) supplies the control chips that are used in the rank multiplied memory

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modules that Samsung manufacturers. *See* Section V.B; EX2018, 8-9; EX2033, 2; EX2019, 13. Rank multiplication has become more and more complex over time. The '912 patent anticipated this evolution. Claim 16 is directed at a very specific technique that allows for an individual chip within a rank-multiplied DIMM to be addressed.

Netlist designs and markets its own DIMMs. By 2008, Netlist had developed the critical technologies for load reduction and rank multiplication via its HyperCloud® modules and chipsets. Soon after the introduction of Netlist's pioneering rank-multiplied DIMMs, it became clear that instead of purchasing or partnering with Netlist, entities like Google, Samsung and Inphi (Rambus) were going to make competing products and accept the risk of infringement.

In 2009, Netlist served a complaint alleging infringement of the '912 patent on Google and Inphi in separate proceedings in the Northern District and Central District of California, respectively. EX2001; EX2002; EX2017 (FAC). In 2010, Google, Inphi, and a third entity—SM—sought *inter partes* reexamination of the '912 patent. EX1010, 1366. SM was not accused of infringement by Netlist; but it is a long-time memory development partner with Samsung. EX2028, 25 (characterizing Samsung as a "major supplier"), 8 (Samsung represented 34% of net sales in FY2018); EX2034, 6-7 (SM frequently working with semiconductor suppliers including Samsung "in bidding for customers' design-in opportunities").

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The PTO ordered reexamination and merged the three proceedings. EX1010, 1367. The consolidated proceeding examined every single claim of the '912 patent, including claim 16. In 2010, the lawsuits initiated against Google and Inphi were stayed pending the completion of the merged reexamination.

The reexamination proceeding authorized all parties to make arguments as to all challenged claims until the close of prosecution. EX1010, 1367 n.1. At least Inphi, SM and Google shared a common interest in coordinating on the '912 patentability challenges. EX2003, 6. On April 4, 2011 the Examiner affirmed the validity of claim 16. EX1010, 1402-03, 1405. Later, the Examiner again affirmed the validity of claim 16 despite third-party requesters' objections. *Id.*, 3865-67, 3904, 4442, 4828, 4830, 4702-04, 4723-25.

On appeal to the Board, SM and Google shared counsel and this continued through the Federal Circuit Appeal. EX1010, 6740. The Board affirmed the Examiner's maintenance of claim 16 twice. EX1011, 78-80, 152. The Federal Circuit affirmed the Board. *Google LLC v. Netlist, Inc.*, 810 F. App'x 902 (Fed. Cir. 2020).

The Petition argues that "the prior reexamination concluded before Petitioner had any reason to challenge the validity of claim 16 of the 912 Patent." Pet., 116. Samsung and Netlist did not enter into a Joint Development and License Agreement ("JDLA") under which Samsung obtained certain rights to Netlist's patents until

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November 12, 2015. The reexaminations were filed in 2010. Samsung chose not to participate because its commercial partners in the DIMM space were already challenging the patent, and its presence would do nothing but increase the likelihood of the *inter partes* reexamination estoppel provision (pre-AIA 35 U.S.C. §§ 317(b) and 315(c)) applying to Samsung.

In March 2021, the district court proceeding against Google re-started after more than a decade delay. Samsung claimed that Google (and Google's server assembly subcontractor Lenovo) demanded that Samsung indemnify Google against Netlist's claims. EX1051, ¶¶43-44. Based on this demand, Samsung took two steps: (a) although the case against Google has been pending for more than a decade in the Northern District of California, on October 15, 2021, Samsung brought a declaratory judgment of non-infringement on the '912 patent in the District of Delaware (EX1049, ¶¶114-17); and (b) Samsung filed this IPR.

Netlist has never communicated with Samsung regarding the '912 patent, and has never accused it of infringing the '912 patent. Instead, the basis for Samsung's declaratory judgment suit in the District of Delaware is indemnification requests it received from Google and Google's subcontractor Lenovo. EX1049, ¶11; EX1051 ¶43 (July 6, 2021 indemnification demand from Google), ¶44 (July 19, 2021 indemnification demand from Lenovo). Netlist has never sued or threatened Lenovo with suit; Lenovo is merely Google's server supplier. EX2004, 10. Samsung has

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repeatedly pointed to its indemnification obligations from Google to justify its declaratory judgment action. EX2005, 9-10, 13 (arguing Netlist's assertion of the '912 patent "based on Google's use of standard-compliant memory supplied by Samsung" established standing). Google is the ultimate beneficiary of Samsung's actions: Google is using Samsung's declaratory judgment action and IPR as a basis to stay—for the second time—the case that has been pending against it in the Northern District of California since 2009. EX2004, 6, 15-16 (arguing for stay in light pending resolution of Samsung's declaratory judgment action and this IPR).

IV. THE PETITION IS TIME BARRED BECAUSE GOOGLE IS SEPARATELY A REAL-PARTY-IN-INTEREST AND A PRIVY

A. The Petition Is Barred Under 35 U.S.C. § 315

Patent Owner first served Google with a complaint of infringement of the '912 patent in 2009. Petitioner is an RPI and privy of Google, and therefore the Petition is time-barred under 35 U.S.C. § 315(b).

1. Legal Standards

Section 315(b) bars the institution of IPR if the petition "is filed more than 1 year after the date on which the petitioner, ***real party in interest, or privy of the petitioner*** is served with a complaint alleging infringement of the patent." 35 U.S.C. § 315(b). Petitioner bears the burden of persuasion to demonstrate that its petition is not time-barred. *Worlds Inc. v. Bungie, Inc.*, 903 F.3d 1237, 1241-42 (Fed. Cir.

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2018); *RPX Corp. v. Applications in Internet Time, LLC*, IPR2015-01750, Paper 128, at 7 (P.T.A.B. Oct. 2, 2020) (Precedential).

The Federal Circuit emphasized that the fact that a petitioner may have its own independent interest in challenging a patent does not mean it is the only RPI. To the contrary, the statutory language contemplates that there could be multiple RPIs, and that each must be analyzed separately in applying § 315(b):

> Congress did not speak of there being only one interested party in each case; instead, it chose language that bars petitions where proxies or privies would benefit from an instituted IPR, even where the petitioning party might separately have its own interest in initiating an IPR.

Applications in Internet Time, LLC v. RPX Corp., 897 F.3d 1336, 1347 (Fed. Cir. 2018). Moreover, the Federal Circuit instructed that:

> § 315(b) does not presume the existence of only one real party in interest—it is not an either-or proposition. The point is not to probe [petitioner]'s interest (it does not need any); rather, it is to probe the extent to which [the time-bared party] … has an interest in and will benefit from [petitioner's] actions, and inquire whether [petitioner] can be said to be representing that interest after examining its relationship with [time-barred party].

Id. at 1353.

The Board's precedential decision in *RPX Corp.* describes the inquiry as follows:

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> We approach the inquiry by focusing on the "two related purposes" of the real party in interest ("RPI") requirement set forth in the legislative history, i.e., ***to preclude parties from getting "two bites at the apple"*** by: (1) ensuring that third parties who have sufficiently close relationships with IPR petitioners are bound by the outcome of instituted IPRs in final written decisions under 35 U.S.C. § 315(e), the IPR estoppel provision; and (2) safeguarding patent owners from having to defend their patents against belated administrative attacks by related parties via 35 U.S.C. § 315(b).

RPX, Paper 128, 2.

2. Google is an RPI

In determining whether an un-named entity is an RPI, the *RPX* Panel focused on three factual inquires: (1) Salesforce's interests in, and benefits from, the IPR; (2) whether RPX was representing Salesforce's interest in filing the IPR; and (3) RPX's business model, including its preexisting relationship to Salesforce. *RPX*, Paper 128, 11-25.

(a) Google Has a Direct Interest In, and Benefits From, the IPR

Google has a direct interest in this IPR and will benefit from it.

First, in the Google Action, Patent Owner contends that Google's infringement of the '912 patent has been and continues to be willful based on

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Google's decision to abandon its established commercial relationship with Netlist in favor of producing knock-off products. EX2015, 10-12.

Second, Samsung has represented in legal filings that it does not manufacture or design any DIMMs in the United States. EX2006, 13. Samsung has also not conceded that it sells, offers to sell, or imports into the United States DIMMs used by Google. If these facts are true, it means the legal exposure for the damages associated with Google's infringement is Google's.

Third, because Google was served with a complaint of infringement of the '912 patent more than a decade ago, it is bared from initiating an IPR.

Fourth, having actively participated in the consolidated *inter partes* reexamination that repeatedly examined the validity of claim 16, Google is barred from challenging the same claim in the district court. Pre-AIA 35 U.S.C. §§ 317(b), 315(c).

(b) Samsung is Representing Google's Interest

As the Federal Circuit has made clear, the RPI determination "demands a ***flexible*** approach that takes into account both ***equitable and practical*** considerations, with an eye toward determining whether the non-party is a clear beneficiary that has a preexisting, established relationship with the petitioner." *AIT*, 897 F.3d at 1351. The focus of this inquiry is "whether a non-party 'desires review of the patent' and whether a petition has been filed at a nonparty's 'behest.'" *Id.* It

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matters not that Samsung "might separately have its own interest in initiating an IPR." *Id.* at 1347.

There may be instances in which this inquiry is unclear or contentious. In this case, however, Samsung openly admitted in legal filings in the District of Delaware that it was challenging the '912 patent because of the indemnification requests it received from Google and Google's subcontractor Lenovo:

> [I]n an ongoing patent infringement lawsuit against Google, Netlist recently amended its infringement contentions to allege that Google's servers (which include Samsung's standard-compliant memory modules) infringe the '912 patent. As a direct and proximate result of Netlist's patent enforcement activities with respect to the '912 patent, Samsung has received demands for indemnification, including from Google and Lenovo.

EX1049, ¶11; EX1051, ¶14. But Netlist has never communicated with Samsung/Lenovo regarding the '912 patent and has not filed a lawsuit against them; Lenovo's sole connection is that Google has publicly announced that Lenovo builds servers for it with Samsung DDR4 LRDIMMs. EX2004, 10.

This was not isolated, inartful wording by Samsung. Samsung repeatedly explained that it was challenging the '912 patent at the behest of Google. In its First Amended Complaint, it pleaded:

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- "On July 6, 2021, Google made an indemnification request to SSI in connection with Netlist's assertion in the Google Infringement Action of the '912 patent against Google's use of Samsung's DDR4 LRDIMM and RDIMM memory modules." EX1051, ¶43.
- "On July 19, 2021, Lenovo made an indemnification request to SSI in connection with Netlist's assertion in the Google Infringement Action of claim 16 of the '912 patent against Google's use of Lenovo's 'Octopod' servers, which contain Samsung's DDR4 LRDIMM and RDIMM memory modules." *Id.*, ¶44.
- "As a direct and proximate result of Netlist's patent enforcement activities with respect to the '912 patent, Samsung has received demands for indemnification, including from Google and Lenovo." *Id.*, ¶14.

And in opposing Netlist's motion to dismiss in Delaware as to the '912 patent, Samsung again pointed to Google's demand for assistance:

- "Netlist accused Samsung's customer Google of infringing U.S. Patent No. 7,619,912 (the ''912 patent'), based on Google's use of standard-compliant memory supplied by Samsung." EX2005, 9-10.
- "The Federal Circuit and Courts in this District have found jurisdiction over a manufacturer's declaratory judgment action based on infringement suits against a customer." *Id.*, 13.

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If there was still any question about who benefits from Samsung's actions, Google disposed of that via motion practice in the Northern District of California. Although the Northern District of California case only reinitiated in 2021 after more than a decade of reexamination, Google has filed another motion to stay, based on Samsung's declaratory judgment action and IPR:

- "Because Samsung manufacturers those products, its declaratory judgment action should proceed and this case should be stayed pending resolution." EX2004, 6.
- "Finally, on February 17, 2022, Samsung filed a petition for *inter partes* review ('IPR'), asking the U.S. Patent and Trademark Office ('USPTO') to invalidate claim 16 of the '912 Patent on three separate grounds…. The USPTO will decide whether to institute *inter partes* review by October 21, 2022." *Id.*, 11.

(c) Petitioner's Business Model: Google and Samsung Have an Expansive and Symbiotic Pre-Existing Relationship That Permeates All Aspects of the Their Businesses, Including DIMMs

Google holds a worldwide monopoly in internet search, and together with Microsoft and Amazon holds oligopoly power in cloud computing. As a result, Google is one of the largest users of DIMMs in the world. Samsung is the dominant supplier of DIMMs in a highly competitive market. EX2030, 40. Google and

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Samsung both claim that products imported by Google and accused of infringing the ’912 patent are manufactured by Samsung. EX2006, 13 (Samsung claiming “[n]one of the allegedly infringing Samsung memory modules is designed, developed, or manufactured in the United States”); EX2004, 6 (Google claiming “Samsung memory modules [are] the only products at issue in this litigation”). Indeed, the relationship is so deep that Google and its subcontractor Lenovo sent a request for Samsung to “indemnify” against the claims in the Google lawsuit, (EX1051, ¶¶14, 43-44), and Samsung immediately brought suit against Netlist and then filed this IPR. Notably, Samsung took this step even though neither Google, Lenovo nor Samsung points to the existence of a written indemnification agreement or an actual legal obligation to indemnify. And Samsung took these steps even though Netlist has never accused Samsung of infringing the ’912 patent.

The business dealing between Samsung and Google also extends beyond the memory business. EX2008, 3 (“Samsung and Google have collaborated on numerous occasions in recent years. The latter’s keynotes often feature the Korean firm’s products. New Google features also often debut on Galaxy devices.”). Samsung is the largest manufacturer of Android-based smartphones (EX2009, 4) (Samsung’s share of Android market: 37.1%); and it depends on Google’s continued support for the continued success of its Android phones and operating environment. EX2027, 2 (“Android currently keeps Samsung and Google linked at the hips. Both

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companies heavily depend on the OS ....”). This relationship is symbiotic, as Google’s CEO Sundar Pichai underscored in recent comments that “[t]hey [Samsung] are our most important partner on Android. I think Samsung is a big partner for our devices and services team as well.” EX2010, 4. Samsung and Google have also collaborated on foldable smartphones, wearable technology, and personal computers. *See, e.g.*, EX2011, 5 (“For years, Samsung and Google have been collaborating to make the foldable experience scalable by providing Android developers with the necessary framework and resources.”), EX2012, 1 (“Google announced on May 18 that it would work together with Samsung Electronics in order to create an integrated platform in which its Wear OS and Samsung's Tizen are combined.”), EX2013, 1 (“Samsung Electronics America Inc., a subsidiary of Samsung Electronics Corporation, today announced its stylish Series 5 Chromebook.”).

Samsung also maintains major contracts with Google. For example, in 2014, Samsung and Google entered into a licensing agreement that “furthered their long-term cooperative partnership.” EX2014, 1. As another example, Samsung recently renewed its European Mobile Application Sales Agreement (EMADA), a critical license to Google’s Android OS for the European market. EX2030, 29-30.

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3. Google is a Privy

The Federal Circuit has given guidance on the standard for defining a privy under § 315(b):

> [T]he PTO correctly recognizes that the related concept of privity "is an equitable rule that takes into account the 'practical situation,' and should extend to parties to transactions and other activities relating to the property in question."

AIT, 897 F.3d at 1349 (citing 157 Cong. Rec. S1376 (Mar. 8, 2011) (statement of Sen. Kyl)). The Federal Circuit observed that this concept of privity is consistent with the legislative history as a whole:

> One of his colleagues, Senator Schumer, expressed a similar belief, stating that "[a] 'privy' is a party that has a direct relationship to the petitioner with respect to the allegedly infringing product or service."

Id., at 1350 (citing S5432 (Sept. 8, 2011) (statement of Sen. Schumer)). Although there will be instances in which the question of privity is hotly contested, in this case, Samsung and Google have both admitted it on the record. In Google's motion seeking a stay of Netlist's decade-long lawsuit involving the '912 patent, Google represented that it purchases all relevant products from Samsung. EX2004, 6. In the first section of its brief, "The Samsung Litigation Will Resolve the Issues Disputed in This Case," Google admits that it has a direct relationship with Petitioner

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concerning the products accused of infringing claim 16, therefore establishing privity:

> Netlist does not dispute that the Samsung declaratory judgment action will resolve the question of whether 4-Rank DDR4 RDIMMs and LRDIMMs that Samsung supplies to Google infringe claim 16 of the '912 patent.

Id., 11. Likewise, Samsung has candidly described Google as its "customer" with respect to the products at issue for claim 16 of the '912 patent, once again establishing a direct relationship with respect to the products accused of infringing claim 16:

> Several months later, Netlist accused Samsung's customer Google of infringing … the '912 patent[], based on Google's use of standard-compliant memory products supplied by Samsung.

EX2005, 9-10. Google and Samsung have both pleaded that they are focused on attacking the '912 patent because of the allegedly same product and the same alleged infringing activity. They are privies under *AIT*.

V. THE BOARD SHOULD DENY THE PETITION AS AN IMPROPER SERIAL CHALLENGE

The '912 patent, including claim 16, has been through one of the most thorough reexaminations in recent history. Over a 10-year period, three highly sophisticated and motivated entities operating under a common interest agreement—Google, Inphi, and SM—collectively challenged every single claim in the '912

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patent. Claim 16 was affirmed valid without amendment multiple times by the Office, the Board and the Federal Circuit. In March 2021, the Northern District of California re-activated Netlist's suit against Google. Within a year, Samsung filed this IPR, which transparently uses the argument and analysis in the reexamination as a roadmap.

A. Legal Standards

General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha, IPR2016-01357, Paper 19, at 15-16 (P.T.A.B. Sept. 6, 2017) (precedential) and *In re Vivint, Inc.*, 14 F.4th 1342, 1353 (Fed. Cir. 2021) guide the analysis.

The Federal Circuit has made clear that the fact that one proceeding challenging a patent was a reexamination while the other was an IPR does not alter the standards to be applied in preventing undesirable serial attacks. *Vivint*, 14 F.4th at 1353. *Vivint* involved an IPR challenge to a patent, which was denied not on the merits, but because it was an example of "undesirable, incremental petitioning." *Id.* at 1346. The second challenge was an *ex parte* reexamination. The Federal Circuit held that it was an abuse of agency discretion to allow the *ex parte* reexamination to proceed. *Id.*, 1354. The facts on this Petition are even starker. There has been a decade-long full adjudication before the Office, the Board, and the Federal Circuit on the identical claim Samsung now attacks, at the express behest of Google, one of the nominal parties to the reexamination.

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B. Samsung Has Longstanding Relationships With Google and Inphi, Who Are Estopped From Challenging Claim 16 Before the Office

GP Factor No. 1 is "whether the same petitioner previously filed a petition directed to the same claims of the same patent." *General Plastics*, Paper 19, at 16.

Here, the previous reexamination proceeding expressly involved claim 16 of the '912 patent. Inphi's reexamination request expressly challenged claim 16. EX2016, 141. SM presented argument attacking claim 16. EX1010, 4442-43. SM and Google shared counsel from the time of the first appeal to the PTAB through the Federal Circuit opinion. EX1010, 6740. And claim 16 was the subject of combined briefing from all three challengers on appeal, in which SM and Google shared counsel. *Id*. The Office and Board repeatedly addressed claim 16. *Supra*, III.

In *Valve Corp. v. Elec. Scripting Prods., Inc.*, IPR2019-00062, Paper 11, at 8-15 (P.T.A.B., Apr. 2, 2019) (precedential), the Board determined that the first *GP* factor can properly be applied when a previous challenge was brought by a different, but related party. "When different petitioners challenge the same patent, [the Board] consider[s] any relationship between those petitioners when weighing the *General Plastic* factors." *Id.* The facts of *Valve* are informative. The Board declined to initiate an IPR petition filed by HTC. Valve, the supplier of a component HTC used to assemble the infringing instrumentality, subsequently filed an IPR petition challenging the same patent. One of the primary factors that the Board focused on

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is that HTC used components and technology supplied by Valve in the products that were accused of infringing the challenged patent:

> Indeed, in that lawsuit, Valve represented that "HTC's VIVE devices incorporate certain Valve technologies under a technology license from Valve" and that "Valve employees did provide HTC with technical assistance during the development of the accused VIVE devices."

Id. at 10. The Board also emphasized that "Valve was aware of Patent Owner's infringement allegations at the time HTC filed its petition." *Id*. The same facts apply here.

First, Samsung has admitted in pleadings that it closely followed the '912 patent lawsuits against Google and Inphi when they were initiated over a decade ago. In particular, Samsung told the District of Delaware that jurisdiction existed over its DJ challenge to the '912 patent because it was aware of "Netlist's litigation campaign against the industry, including an assertion of the '912 patent against Inphi." EX2024, 2. Consistent with this argument, Samsung pleaded that it was aware of the following:

- "In addition, Netlist previously asserted the '912 patent in litigation against Inphi Corporation, and in doing so served claim charts that purport to demonstrate infringement based on compliance with certain JEDEC memory standards." EX1051, ¶15.

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- "As noted above, Netlist has also asserted the '912 patent against Inphi, a chip supplier, based on the practice of certain JEDEC memory standards...." *Id.*, ¶45.

The reference to Inphi as a "chip supplier" was not an accident. Inphi is not just any chip supplier; Inphi chips are used in Samsung's DIMMs. At the time of the Netlist lawsuit against Inphi and Inphi's reexamination proceeding, Inphi was a provider of memory buffer chip products, including Inphi's "Isolation Memory Buffer," or "iMB" at issue in Netlist's infringement action against Inphi in 2009. EX2017, ¶8. Inphi supplied the accused iMBs to Samsung for use in Samsung's DDR3 LRDIMMs. EX2033, 2 (August 2012 report: "Using Inphi's iMB technology, high-speed Samsung LRDIMMs can provide twice the memory in a given amount of space."); EX2018, 8-9 (Samsung October 2016 product indicating Inphi provided the RCD and iMBs for certain DDR3 DIMMs). Samsung was an important partner to Inphi between 2010 when the reexamination was ordered and 2015 when Samsung entered into the now-terminated JDLA with Netlist. EX2020, 9 (Samsung accounted for 34% and 36% of Inphi's revenue in 2010 and 2009 respectively); EX2022, 15 (Samsung accounted for 18% and 20% of Inphi's revenue in 2014 and 2013 respectively); EX2019, 13 (Samsung product guide from May 2018 indicating that Inphi (Rambus) provided the RCD for certain DDR4 DIMMs). Likewise, Inphi was important to Samsung. For example, the two partnered in 2012

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to showcase LRDIMM technology for the next generation servers, which incorporated Inphi's accused iMBs. EX2021, 1 ("Inphi will showcase the benefit of a system with 768GB capacity using 32GB Samsung LRDIMMs enabled by Inphi's Isolation Memory Buffer (iMB™) technology to real world applications."); EX2022, 2 (award from Samsung to Inphi), 12 (strategic collaborative discussions between Inphi and other companies, including Samsung).

As for Samsung and Google, the two have an important symbiotic relationship which continues through this day with Samsung claiming to be the key supplier of the DDR4 LRDIMMs and RDIMMs used by Google that are accused of infringing the challenged claim. EX1051, ¶44. Notably, public documents evidence that Inphi chips are used in the DDR4 LRDIMMs that Samsung claims to manufacture and supply to Google, and on which Samsung is seeking a DJ at Google's behest. EX2022, 13. This factor favors denying institution.

C. At the Time of the Reexamination, Samsung Knew of the Prior Art Asserted in the Second Petition

GP Factor No. 2 considers whether the prior art relied on in the later petition "could have been found with reasonable diligence." *General Plastics*, Paper 19, at 20. Here, both Amidi and Ellsberry were cited during prosecution of the '912 patent in the Notice of Allowance, dated September 30, 2009. EX1002, 509 ("The prior art made of record and not relied upon is considered pertinent to applicant's

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disclosure: Amidi ... Ellsberry."). U.S. 7,356,639 to Perego—materially identical to Petitioner's Perego-422 (*see infra*, VII.A.1 below)—was also cited and considered during prosecution. This factor favors denying institution.

D. Samsung Benefited From the Office's and the Board's Prior Analysis and Tailored the Arguments Accordingly

GP Factor No. 3 examines the potential benefit a petitioner may receive from lying in wait as others assail a patent: "[t]he absence of any restrictions on follow-on petitions would allow petitioners the opportunity to strategically stage their prior art and arguments in multiple petitions, using our decisions as a roadmap, until a ground is found that results in the grant of review." *General Plastics*, Paper 19, at 17-18. The '912 reexamination concluded in June 2020 following repeated Office Actions discussing claim 16, two PTAB decisions and the Federal Circuit's summary affirmance of the Board's decision. EX1010, 1402, 3865-67, 3904; EX1011, 78-80, 152; 810 F. App'x at 902. That Samsung studied these decisions and used them to plan the IPR petition is evident from the Petition itself, which recounts the history of the reexamination of claim 16. Pet., 10-11. And it relies on alleged findings in the reexamination to build the Petition. Pet., 10-11, 50; EX1003, ¶¶63-65, 160; *see also, e.g.*, Pet., 49 (citing "Dell2" reference from reexamination, EX1044). For example, during the reexamination, the Board affirmed the examiner's finding that "Requester has not provided a reasonable explanation as to

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why one skilled in the art would transmit a command signal ***to only one DDR memory device at a time when there is a plurality of memory devices in a rank***." EX1011, 79. Apparently unable to make such a showing here either, Petitioner resorts to a claim construction where there is but a single device in every rank. *See* Pet., 31, 43 (modifying Perego-422's Figure 4B by leaving only a single device in each rank); Pet., 71, 76-77 (assuming that Ellsberry disclosed a single device per rank). This is the exact argument that the Board rejected in the reexamination, expressly finding that a "rank" requires a plurality of memory devices. *See* Section VI.C below. This factor favors denying institution.

E. Samsung Did Not Provide Adequate Explanation for the Time Elapsed

GP Factor No. 4 addresses the length of time between when the petitioner learned of the prior art asserted in the second petition and the filing of the second petition. *General Plastics*, Paper 19, at 16. *GP* Factor No. 5 addresses whether the petitioner provides adequate explanation for the time elapsed between the filings of multiple petitions directed to the same claims of the same patent. *Id.*

As noted in Section V.C., Samsung was aware of the prior art it uses because it was cited on the face of the '912 patent, which issued 13 years ago.

As noted above in Section V.B, Samsung was aware of the previous assertion of the '912 patent by Netlist, including against its chip supplier Inphi in 2009. The

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Petition misleadingly claims that "the prior reexamination concluded before Petitioner had any reason to challenge the validity of claim 16 of the 912 Patent." Pet., 116. Samsung and Netlist did not enter into a JDLA under which Samsung obtained certain rights to Netlist's patents until November 12, 2015. The assertion of claim 16 against Inphi occurred in 2009. The requests for reexamination, including against claim 16, were filed in 2010. EX1010, 1366. Netlist terminated the license based on material breach by Samsung on July 15, 2020. EX2023, 18-20. Samsung admitted it was aware of what it described as the assertion of the '912 patent against the "industry," including against its chip supplier Inphi and admitted that it believed Netlist was asserting the '912 patent against industry standards:

- "Netlist's litigation campaign against the industry, including an assertion of the '912 patent against Inphi...." EX2024, 2.
- "In addition, Netlist previously asserted the '912 patent in litigation against Inphi Corporation, and in doing so served claim charts that purport to demonstrate infringement based on compliance with certain JEDEC memory standards." EX1051, ¶15.

Samsung's partner Inphi knew claim 16 was a risk, because it challenged that claim. Samsung has not adequately explained its failure in challenging the '912 patent in 2010, when its chip supplier Inphi did. Samsung was not licensed in 2010.

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Indeed, the most likely explanation was that Samsung withheld its challenge to avoid the estoppel risk that attaches to participants in *inter partes* reexaminations.

This factor favors denying institution. *Valve*, Paper 11, at 13-14 (five-month delay favored denying institution).

F. The Remaining Factors Require Independent Board Analysis

For the two remaining factors, Netlist acknowledges that the Board has the resources to handle one more trial and can likely meet the 1-year deadline. But given the resources that the Board has already invested in the '912 patent (two reviews), it does not make any sense for the Board to devote even more resources to it. These two factors therefore weigh either in favor of denial or are neutral.

VI. PETITIONER FAILS TO ESTABLISH A REASONABLE LIKELIHOOD OF PREVAILING ON CLAIM 16

The Petition is asking the Board to reconsider the same arguments that were rejected in the decade-long reexamination proceedings. To best frame this context, Patent Owner will first describe Petitioner's arguments, explain why it does not make out a *prima facie* case, and then explain why the Petition requires the Board to in effect reverse itself.

A. The '912 Patent

The '912 patent relates to memory module technology, and more specifically, to a concept called rank multiplication. A memory module is a device that contains individual memory devices arranged in "ranks" on a printed circuit board. *Id.* at

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1:26-31; *infra*, VI.C. At the time of the invention, most computer systems supported accessing only one or two ranks, limiting the number of ranks that can be added per memory module. EX1001, 1:20-2:42.

The ’912 patent teaches that one way to upgrade the memory capacity of a memory module is to use on-module logic to present a memory module with, *e.g.*, 2n physical ranks of memory devices, as a module with n (virtual) ranks to the computer system. *Id.*, 6:64-7:19. In this way, “even though the memory module 10 actually has the first number of [physical] ranks of memory devices 30, the memory module 10 simulates a virtual memory module by operating as having the second number of [logical or virtual] ranks of memory devices 30.” *Id.*, 7:9-13. This technique is commonly referred to as “rank multiplication.”

Rank multiplication allows a designer to expand the number of ranks and hence the total memory capacity on a memory module. It also enables them to construct a memory module of a given capacity using lower density memory devices that often cost less. *Id.*, 4:42-58, 22:5-14. For example, for the same 1 GB memory capacity, it could be more cost-effective to use thirty-six 256-Mb DRAMs arranged in 4 ranks than eighteen 512-Mb DRAMs arranged in two ranks. *Id.*, 4:42-58, 4:59-5:5.

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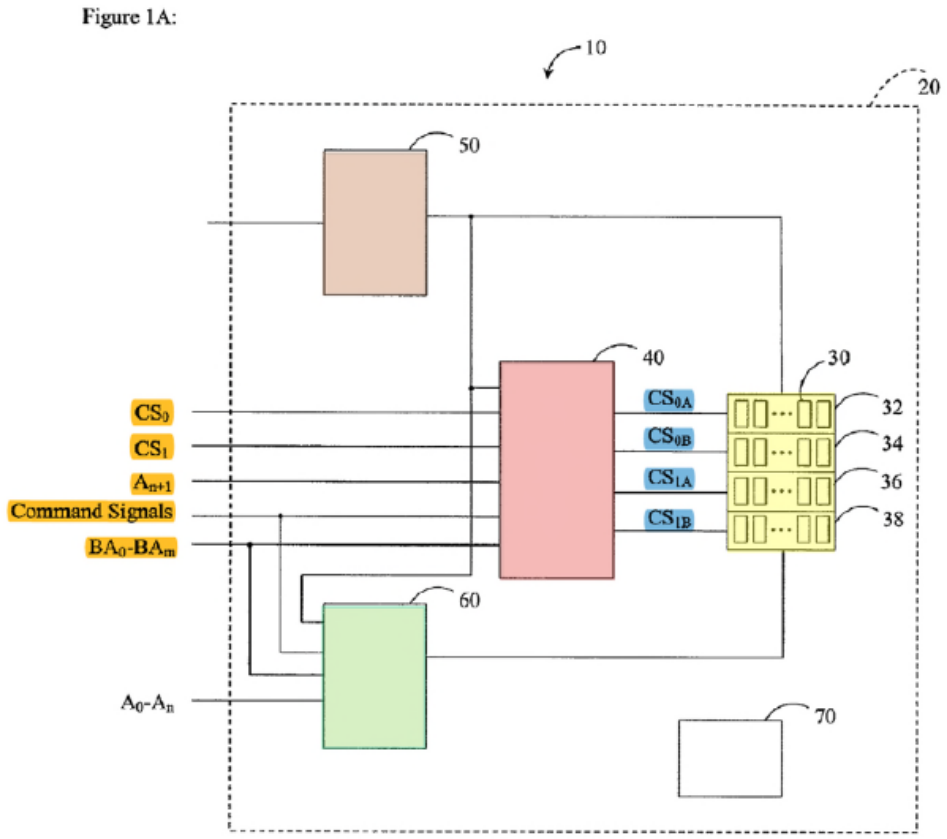
Figure 1A illustrates an example of a memory module with rank multiplication capability. The memory module has a register 60 and a logic element 40.



The logic element receives a set of input control signals from the computer system that include chip-select signals CS_0-CS_1, address signal A_{n+1}, and bank address signals BA_0-BA_m. *Id.*, 7:35-53; Fig. 1A. From the computer system's perspective, it is connected to only two ranks of memory devices, to be selected by CS_0 or CS_1, even though the memory devices are arranged in four physical ranks. *Id.*, 6:55-7:19. In response to the received input control signals, the logic element

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on the memory module generates a set of output control signals, corresponding to the four physical ranks of the memory devices. *Id.*, 6:61-63. The logic element 40 also receives command signals (such as read/write) from the computer system. *Id.*, 6:55-61, 7:46-53. In response to the command signal and the input signals, the logic element transmits the command signal to the memory devices on the selected rank of the memory module. *Id.* In some embodiments, command signals are transmitted to only a single memory device on a multi-device rank at a time. *Id.*, p. 44, 3:9-43.

B. Skill Level of a POSITA

For the purposes of this Preliminary Response only, Patent Owner applies the skill level of a POSITA proposed by Petitioner.

C. Claim Construction

Petitioner seeks to construe the term "rank" as "an independent set of ***one or more memory devices*** on a memory module that act together in response to command signals, including chip select signals, to read or write the full bit-width of the memory module." Pet., 12. The Board should reject Petitioner's construction. First, it contradicts the determination of the Board during reexamination. Second, it contradicts the agreed-upon construction of "rank" in the Google Action. Third, it contradicts the specification and Petitioner's own evidence. The claim construction issue is dispositive of the Petition on the merits because Petitioner only presents an

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analysis under a construction in which "rank" is redrafted to cover "one" "memory device" per rank.

Yet, during the reexamination, the Examiner allowed claim 16 by concluding that Amidi failed to teach "transmit[ting] a command signal to only one DDR memory device at a time ***when there is a plurality of memory devices in a rank***." EX1010, 3865-67, 3904. Simply put, the Examiner properly construed a "rank" as comprising "a plurality of memory devices." The Requesters challenged the Examiner's claim interpretation and argued specifically that claim 16 "requir[ed] only that the command signals are sent to a single rank ***because "one memory device" encompasses a rank of [one] memory***." *Id.*, 4442. The Board nevertheless affirmed the Examiner's decision upholding the patentability of claim 16 because the claim requires a plurality of memory devices in a rank and Amidi does not disclose sending command to a single device within the plurality of devices that constitutes a rank:

> We agree that Amidi teaches using a command signal to read or write to a cell within a DDR memory device. [Citation]. Presumably, because Amidi discusses a particular cell within a bank, Requester 1 contends that the command signals are being transmitted to one DDR memory device at a time as recited. [] Yet, as the Examiner indicates:
>
> > Requester 1 asserts that "[o]ne of ordinary skill in the art would have understood from the '152 publication [of Amidi] that the

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> command signal may be transmitted to the DDR memory devices serially in a sequential fashion" without any reasoned explanation to support the assertion.... The claims require transmission of a command signal to only one DDR memory device at a time. Requester has not provided a reasonable explanation as to why one skilled in the art would transmit a command signal to only one DDR memory device at a time ***when there is a plurality of memory devices in a rank***.

EX1011, 79-80.

The Board's construction is consistent with the stipulated construction for "rank" in the Google Action: "***a group of memory devices*** enabled to receive and transmit data by a common chip-select signal." EX2026, 7. That construction, which again contemplates multiple "memory device***s***" per rank, comports with the intrinsic evidence, which consistently shows that a "rank" of memory devices includes more than one memory device. The figures, for example, consistently show multiple memory devices in each rank. *See id.*, Fig. 1A-B, 2A, 3A (reproduced below, with multi-device ranks highlighted).

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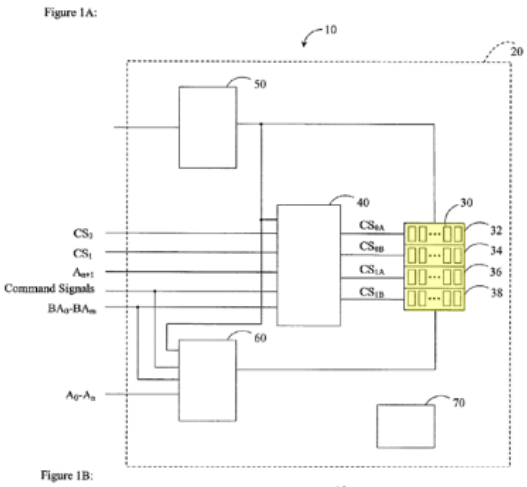

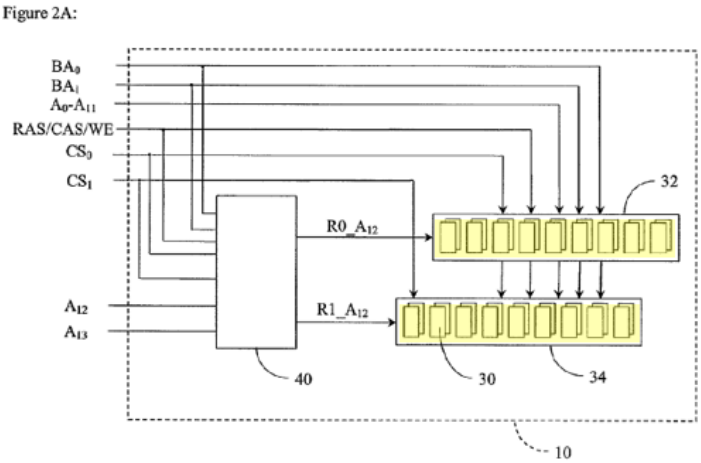

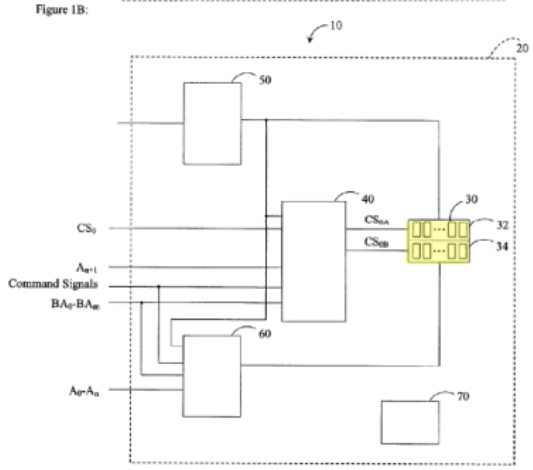

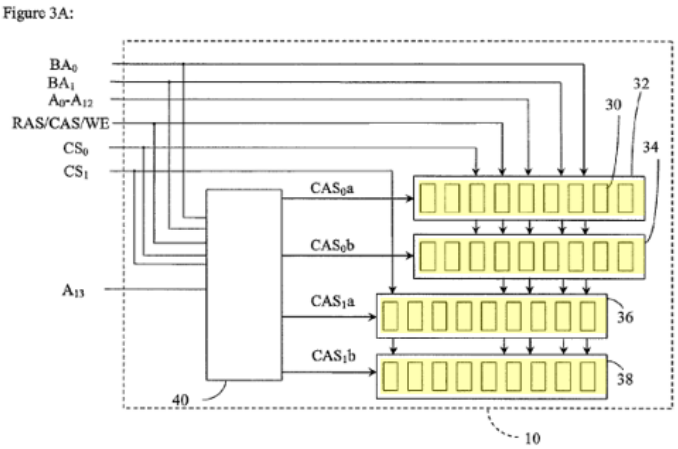

The written description makes repeated and consistent references to ranks composed of multiple memory devices:

- "[I]n certain embodiments, two ranks of memory devices having a memory density are used to simulate ***a single rank of memory devices*** having twice the memory density…." *Id.*, 12:13-25.
- "Thus, in certain embodiments, even though the memory module 10 actually has the first number of ***ranks of memory devices*** 30, the memory

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module 10 simulates a virtual memory module by operating as having the second number of ***ranks of memory devices*** 30." *Id.*, 7:9-13.

- "[I]n certain embodiments, the ***memory devices*** 30 are arranged in four ranks, as schematically illustrated by FIG. 1A. In other embodiments, the ***memory devices*** 30 are arranged in two ranks, as schematically illustrated by FIG. 1B. Other numbers of ***ranks of the memory devices*** 30 are also compatible with embodiments described herein." *Id.*, 6:31-38.

See also, *id.*, 7:55-8:43, 8:64-9:18 (logic tables "for the selection among ***ranks of memory devices*** 30"); *id.*, 10:31-35 ("In certain embodiments, the SPD device 70 comprises data which characterize the memory module 10 as having fewer ***ranks of memory devices*** than the memory module 10 actually has, ….").

The specification also distinguishes embodiments directed to the simulation of a single high-density "memory device" as depicted in Figure 1C from embodiments directed to the simulation of "ranks" of memory devices. *Compare* EX1001, 12:12-15 (discussing emulating a single, high density memory device where "[i]n certain embodiments, ***two memory devices*** having a memory density are used to simulate a ***single memory device*** having twice the memory density") *with* 12:15-21 ("[I]n certain embodiments, two ***ranks of memory devices*** having a memory density are used to simulate ***a single rank of memory devices*** having twice the memory density").

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Petitioner ignores this intrinsic evidence and instead contends that the '912 patent describes a single-device "rank" embodiment. Pet., 13-14. That passage states "[i]n certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of ***Table 1***). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time." EX1001, 8:47-54.

Table 1 is a logic diagram "for the selection among ***ranks of memory devices*** [] using chip-select signals," indicating that the description that follows refers to ranks of multiple memory devices. *Id.*, 7:56-8:10.

Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using chip-select signals.

TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:

1. CS_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

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In state 4 above, the rank corresponding to CS_{1A} is chosen; and within that selected rank, "the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time." 8:47-54; EX2007 (hereinafter "Brogioli"), ¶¶71-73. Read in context, the embodiments described with reference to Table 1 refer to transmitting a command signal to one of the multiple memory devices in the selected rank. *Id.*, ¶73.

A construction of "rank" that requires more than one memory device is also consistent with Petitioner's evidence. *E.g.*, EX1033, 413 ("[T]he word *rank* is now used to denote ***a set of DRAM devices that operate in lockstep*** to respond to a given command in a memory system."). The reference to "operat[ing] in lockstep" makes no sense for a single-device rank, because in such a rank, there would be no other DRAM devices that operate "in lockstep" in response to a command. Brogioli, ¶74. The same reference also notes that "a DRAM memory module can be organized as multiple ranks of DRAM devices on the same memory module, ***with each rank consisting of multiple DRAM devices***." EX1033, 421.

D. The Cited Art

1. Perego-422

Perego-422 discloses a memory system architecture with point-to-point topology which includes a buffered module having a configurable width buffer device. EX1035, Abstract; 5:35-55; 8:10-17, 8:20-26. The buffer device

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communicates to the plurality of memory devices on the buffered module via channels 370, for example, in the case of a normal read operation purportedly to "one or more, or all of memory devices 360." *Id.*, 5:4-6, 6:13-24, 7:65-67; Fig. 3B.

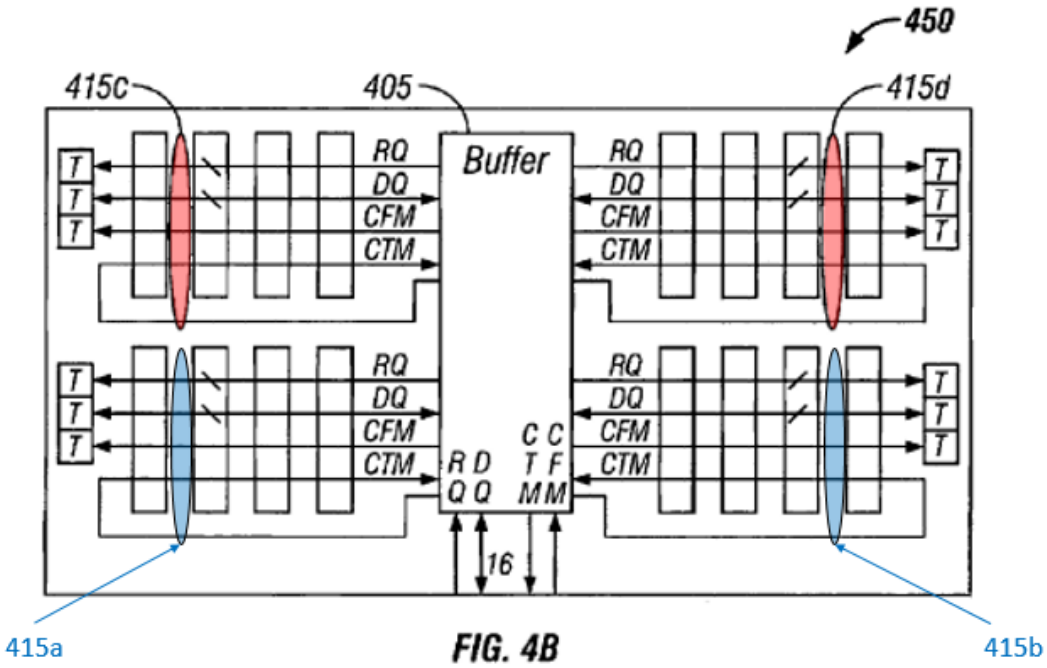

FIG. 4B

Petitioner relies on a modified version of Perego-422's Figure 4B with single-device ranks. *See, e.g.*, Pet. 62. Figure 4B of Perego-422 shows a memory module with multiple memory devices that communicate with the data buffer via channels (415a-415d), which Petitioner maps to the claimed "ranks." *Id.*, 9:26-33, 10:22-36, Fig. 4B (reproduced above); Pet., 61-62; EX1003, ¶124. Perego-422 explains that in one arrangement, the channels depicted in Figure 4B operate in pairs, that is, "channels 415c and 415d are ***routed in parallel*** with channels 415a and 415b"

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(EX1035, 10:23-26), and in another arrangement, "channels 415a and 415b may operate ***simultaneously*** with channels 415c and 415d" (*id.*, 10:32-33).

2. Amidi

Amidi discloses a four-rank "transparent" memory module which emulates a memory module with two ranks in order to "fit[] into a memory socket having two chip select signals routed." EX1036, Abstract, [0011]. Amidi was considered extensively during reexamination, and found not to render obvious claim 16.

In its reexamination request, Inphi argued that Amidi disclosed [16.e] because a POSITA "would have understood from [Amidi] that the command signal may be transmitted to the DDR memory devices serially in a sequential fashion," i.e., one-by-one to each memory device, which the Examiner rejected. EX2016, 141; EX1010, 1402-03. Later, Inphi supplemented this theory by pointing to Amidi's disclosure of "provid[ing] RAS and CAS signals to isolate a particular memory device in an array of memory cells." EX2029, 26-27. The Examiner concluded that Amidi's RAS and CAS signals ("command signals") were not transmitted to only one DDR memory device on the selected rank, as required by the claims. EX1010, 3865-67, 3904. In response to this Office Action, Requester SM challenged this claim interpretation and argued specifically that claim 16 "requir[ed] only that the command signals are sent to a single rank ***because "one memory device" encompasses a rank of [one] memory***," and was thus rendered obvious by Amidi

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(EX1010, 4442). The Examiner entered SM's comments into the record in the next Office Action, but nonetheless maintained its construction of claim 16. *Id.*, 4828, 4830, 4702-04, 4723-25.

The Board later affirmed this finding, emphasizing the Examiner's conclusion that "Requester has not provided a reasonable explanation as to why one skilled in the art would transmit a command signal to ***only one DDR memory device at a time when there is a plurality of memory devices in a rank***." EX1011, 79. That is, the Board agreed that each "rank" is comprised of multiple memory devices, and that it would not be obvious to a POSITA to send a command signal to just one device in the "rank." The Board explained that Figures 6A and 6B of Amidi "show[ed] various command signals [] being transmitted to more than one memory device," as evidenced by the label "Signals to Memory ***Devices***" on those figures. *Id*.

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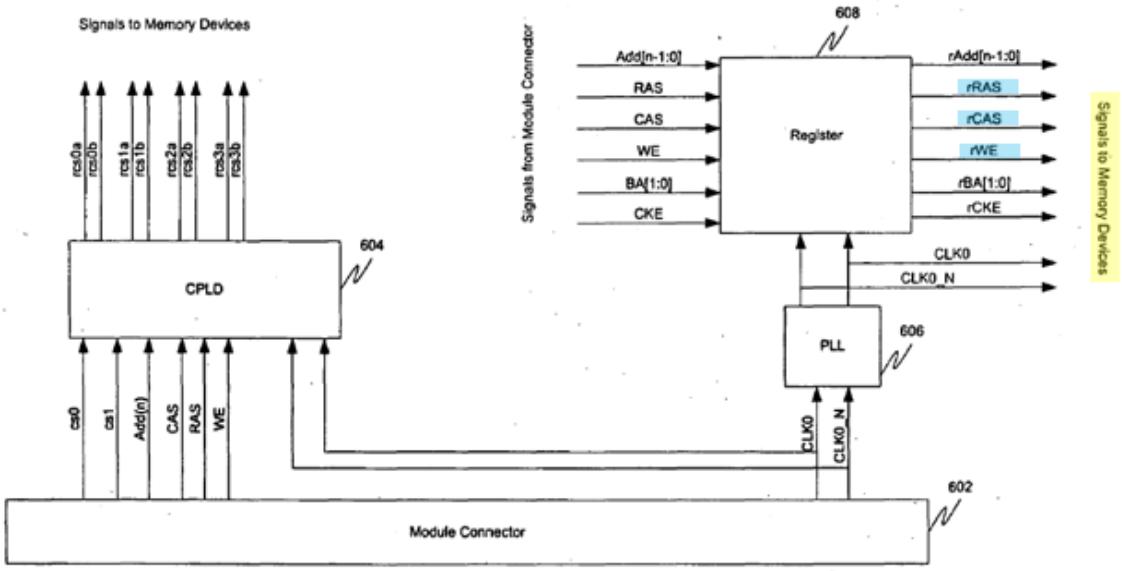

Row Address Decoding
FIG.6A

3. Ellsberry

Ellsberry discloses a memory module architecture, depicted in Figure 2, that "permits transparent bank switching of memory devices." EX1037, [0001]. Control ASIC 204 (red) "receives memory addresses and commands over the DIMM interface 202" from the system memory controller, and switch ASICs 206 and 208 (purple) "receive data information from the DIMM interface 202 via data buses 230 & 232, respectively." *Id.*, [0028]-[0029]. Each switch ASIC is connected to a number of memory banks (e.g., Bank 0-3 below), each with one or more memory devices. *Id.* Switch ASICs 206 and 208 receive respectively data byte group N and data byte group 0, provided "simultaneously" by the DIMM interface 202. *Id.*, [0030], Fig. 2 (depicting at least two data groups); Fig. 5 (depicting nine data

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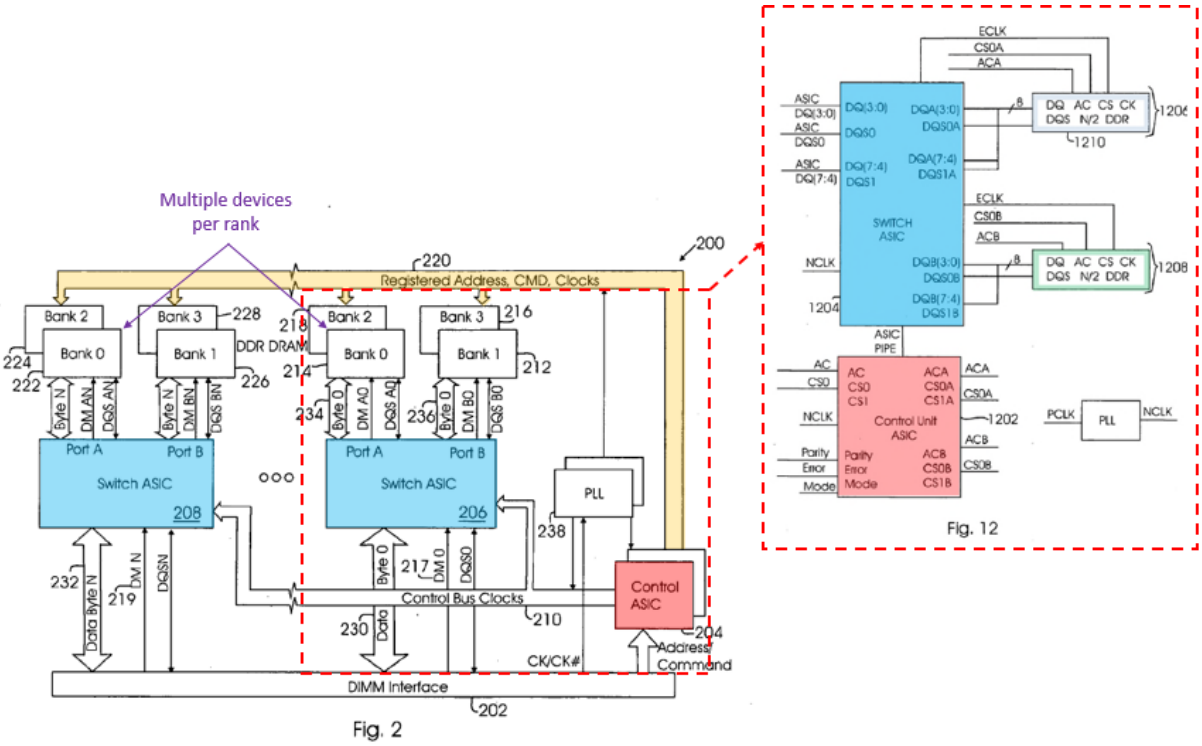
groups). Figures 10-13 illustrate parts of Ellsberry's overall memory module architecture depicted in Figure 2. *See id.*, Figs. 2 and 12 (reproduced below, annotated); EX1038, 50 (Board noting that "Figure 13 shows ***part of a memory module***"), 51, 57, 81; EX2032, 40 n.11; *infra*, VI.F.2.



Control ASIC 204 sends command signals to memory devices in different memory banks via bus 220. *Id.*, [0030]. Each ASIC switch includes two data ports, Port A and Port B, coupled respectively to data busses 234 and 236. Petitioner relies on Ellsberry's teachings that in row/bank addressing mode, control ASIC 204 sends commands to an intended bank, while sending NOP commands to the other bank. Pet., 100-101, 109-110; EX1037, [0042].

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E. Petitioner Has Not Made a *Prima Facie* Case of Obviousness under Grounds 1-2

1. Petitioner Has Not Presented Any Competent Evidence that Grounds 1-2 Disclose [16.b.i]/[16.c.ii]

Claim 16 requires a "plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ***ranks***," and "a second number of DDR memory devices arranged in a second number of ***ranks***," EX1001, p. 44, 3:9-43, where each rank comprises more than one memory device. *See supra*, VI.C. By contrast, both Grounds 1 and 2 rest on hypothetical constructs featuring four channels with one device each, each channel a purported rank. Pet., 28-43. In other words, Petitioner relies on four purported single-device ranks. *Id.*

As a preliminary matter, Petitioner has not even shown that each channel constitutes a rank even under Petitioner's own definition of "rank." This is discussed further in VI.E.2 below. But even if each channel corresponded to a rank, Petitioner's construct admittedly has only single-device ranks.

Petitioner's first example (Ground 1) features four x16 memory devices arranged in what it arbitrarily defines as four ranks ("first number of ranks"). Pet., 30-31 (alleging "Perego teaches an embodiment in which its module includes four memory devices arranged in four ranks, each rank having a single memory device"), 39-41. That is, Petitioner's first example is concededly limited to "ranks" that each contain a single memory device. *See supra*, VI.C.

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Petitioner's second example (Ground 2) features four x16 memory devices arranged in what it arbitrarily defines as four ranks ("first number of ranks") that Petitioner contends can simulate a module with two x16 memory devices arranged in what it arbitrarily defines as two ranks ("second number of ranks"). Pet., 42-43. Here too, Petitioner's relied-upon construct is a module "where each rank has one x16 memory device." Pet. 42; Pet., 43 (modified Fig. 4B). Claim 16, however, requires multi-device ranks. *See supra*, VI.C. As such, Petitioner has not made a *prima facie* case of obviousness.

2. Petitioner Has Not Presented Any Competent Evidence that Grounds 1-2 Disclose [16.e]

Claim 16 requires that "the command signal [be] transmitted to only one DDR memory device at a time." EX1001, p. 44, 3:42-43. Petitioner only asserts that the limitation is met if each rank has a single device. Pet., 61-62; *Id.*, 62-63 ("[W]hen the width of one memory device is equivalent to that of the module, the command received at a specific time is transmitted to only one DDR memory device at a time."). But as explained in VI.C above, each "rank" is understood to have two or more memory devices; and claim 16 requires sending a command to a single device at a time even though there are multiple devices in each rank.

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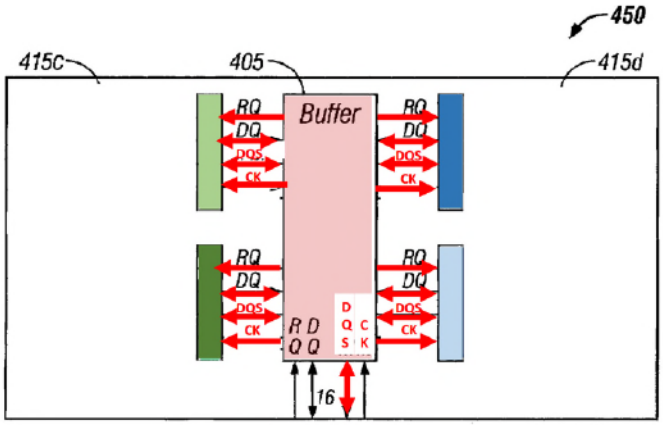

FIG. 4B

Pet. 62 (modified Fig. 4B)

Furthermore, even if a "rank" could encompass one memory device, Petitioner has not provided competent evidence that Perego-422 discloses single-device ranks. Petitioner's mapping assumes that each channel corresponds to a rank. *See* Pet., 61-62. That is not supported by Perego-422's specification. The buffer circuit in Figure 4B communicates with the memory devices via four channels 415a-415d. EX1035, 9:26-33, 10:22-36. These channels may operate in pairs or simultaneously. *Id.*, 10:22-36. In the paired arrangement, "channels 415c and 415d are ***routed in parallel*** with channels 415a and 415b." *Id.*, 10:24-25. In the simultaneous arrangement, "channels 415a and 415b may operate ***simultaneously*** with channels 415c and 415d." *Id.*, 10:32-33.

Petitioner provides no explanation why either arrangement describes single-device ranks, even under Petitioner's construction. Pet., 12, (contending "rank"

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means "an independent set of one or more memory devices on a memory module ***that act together in response to command signals***"). To the contrary, a POSITA would understand that in the paired arrangement, the devices connected to channels 415c/d correspond to one "rank" because they are "routed in parallel," i.e., "act together in response to command signals." Brogioli, ¶¶93-94. Likewise, the devices connected to 415a/b correspond to another "rank." *Id*. A POSITA would also understand that the simultaneous arrangement corresponds to a one-rank module, because all the memory devices connected to channels 415a-d "act together in response to command signals." *Id*. Hence, Petitioner's four-device configuration at best corresponds to a two-rank module, with ***two devices in each rank*** (paired-channel arrangement) or a one-rank module, with ***four devices in the rank*** (simultaneous-channel arrangement). *Id.*, ¶¶93-95. Petitioner does not assert that Perego-422 teaches a POSITA how to transmit a command signal to one memory device at a time when each "rank" includes more than one channel of devices, and thus has failed to make a *prima facie* showing of obviousness.

F. *Ellsberry* Neither Qualifies as Prior Art Nor Renders Obvious Claim 16

1. Ellsberry is Not Prior Art

Ellsberry was filed on June 1, 2005. EX1037. The '912 patent claims priority to a provisional application filed on July 15, 2004 (60/588,244) and U.S. 7,286,436

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("the '436 patent").[2] The Petition's argument that there is no written description requires this instant panel to reject written description findings in the reexamination. *See infra*, VII.A.3.

(a) Legal Standards

Petitioner has the burden to persuade the Board that a reference qualifies as prior art. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

(b) '244 Provisional

The '244 provisional discloses a memory module comprising DRAM devices arranged in a rank and a memory module decoder that is configured to simulate a memory module with a smaller number of ranks (*e.g.*, two logical ranks) than the module actually has (*e.g.*, four physical ranks). EX1005, [0001]-[0002], [0005]-[0008], [0024]-[0025]. The ASIC decoder "decodes two chip-select signals and one control signal (such as an address signal) and converts them into four chip-select signals." *Id.*, [0005]. The decoder receives certain control signals, *e.g.* command signals that "include, but are not limited to, activation read, write, precharge, and refresh." *Id.*, [0019]. In certain four-rank memory module embodiments, "the ASIC uses one additional address signal (A_{n+1}) and at least one control signal. Exemplary

[2] For purposes of the Preliminary Response only, Netlist addresses only the '244 provisional and '436 patent.

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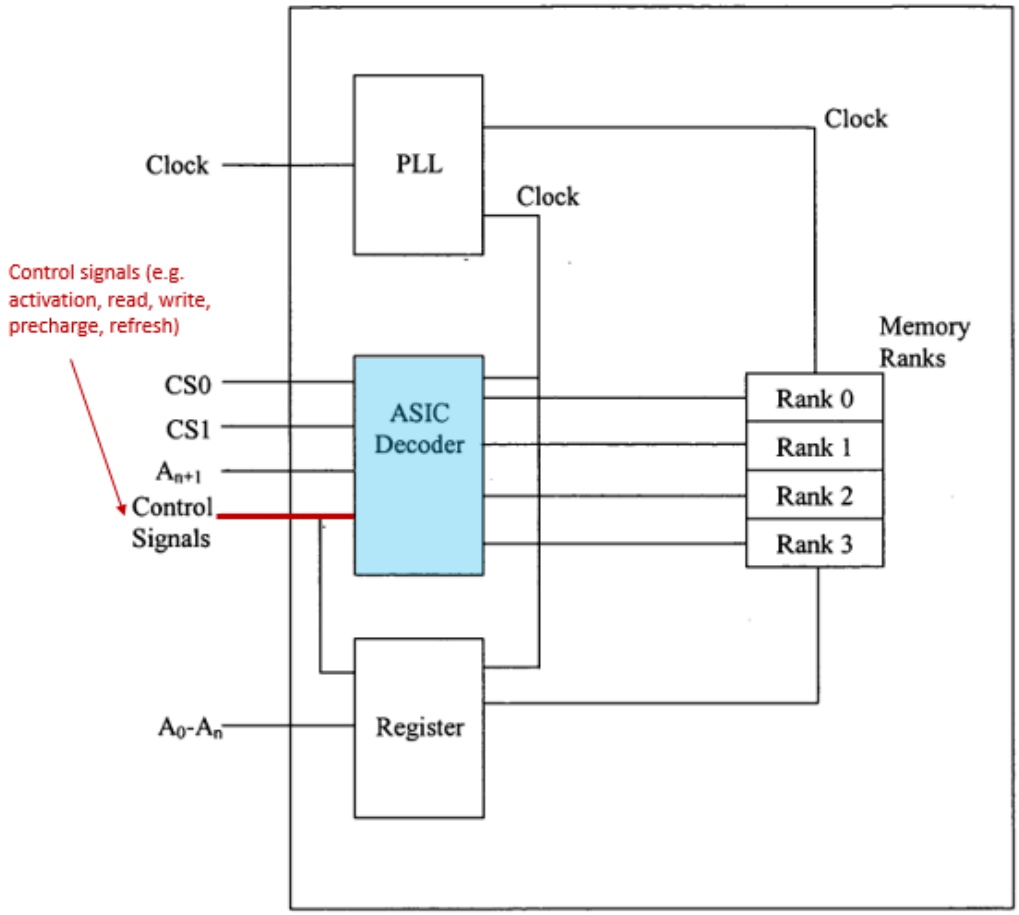
control signals … includ[e], but are not limited to, refresh, precharge, and other operations used for the proper functioning of the memory module." *Id.* [0010], [0025] ("The decoder is configured to receive input signals comprising a first number of chip-select signals and at least one control signal and to convert the input signals into output signals, the output signals comprising a second number of chip-select signals and to pass the output signals to the first number of ranks …."); Figure 1 (reproduced below).



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Petitioner acknowledges that the ’244 provisional discloses a memory module with a “logic element” (ASIC Decoder). Pet., 63. Petitioner’s sole argument—limited to a single sentence in the Petition—is that the ’244 provisional does not disclose a “logic element” that receives “bank address” signals. Pet., 63. But a POSITA would necessarily understand, per the JEDEC DRAM standards of the day, that the “control signals” received by the decoder ASIC (blue) for certain memory operations—such as READ/WRITE—would necessarily include bank address signals. Brogioli, ¶¶40-43.

Indeed, the Petition acknowledges that certain commands such as Bank Activation, Write, and Read necessarily requires bank address signals as part of the command code. Pet., 45-46 (reproduced below, annotations as in Petition); EX1029, 49 n.2 (“Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated on.”).

Table 10 — Command truth table.

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.
NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

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In fact, Petitioner admits "to perform a read or write operation, the JEDEC standard … first requires ***a Bank Activate command with*** the row and ***bank address signals***, followed by ***a read or write command with the corresponding bank address signals***." Pet., 45; *see also* EX1029, 6 (bank addresses are inputted for Active, Read, Write and Precharge commands); *id.*, 49 (truth table for various commands showing the use of bank addresses); EX1030, 7 ("Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.").

1.2 Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, and $\overline{DM}$ signal for x4x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, $\overline{UDM}$, and $\overline{LDM}$ signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (UDM), (LDM)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/$\overline{RDQS}$ is enabled by EMRS command.
BA0 - BA2	Input	**Bank Address Inputs:** BA0 and BA1 for 256 and 512Mb, BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A15	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands.

(EX1029, 6)

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Table 10 — Command truth table.

Function	CKE Previous Cycle	CKE Current Cycle	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1,2
Refresh (REF)	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1,7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.

NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

NOTE 3 Burst reads or writes at BL=4 cannot be terminated or interrupted. See sections "Reads interrupted by a Read" and "Writes interrupted by a Write" in section 2.2.4 for details.

NOTE 4 The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined in section 2.2.7.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See section 2.2.2.4.

NOTE 6 "X" means "H or L (but a defined logic level)".

NOTE 7 Self refresh exit is asynchronous.

EX1029, 49.

According to Petitioner, a POSITA "would have been knowledgeable about the JEDEC DDR (EX1030, EX1031) and DDR2 (EX1029, EX1039) SDRAM standards." Pet., 6. Indeed, Petitioner relies on the JEDEC standard to argue that Perego-422 discloses receiving "bank address signals" by a logic element. Pet., 36-

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37 ("A POSITA would have understood that, for DDR memory devices, the 'address lines' (and 'address information') labeled RQ in Perego … convey both row/column, and bank, addresses, per the JEDEC standard.") (citing EX1029 and EX1032).

Accordingly, under Petitioner's own theory, a POSITA, being knowledgeable about the above-cited sections of JEDEC, would have understood that the '244 provisional disclosed a "logic element" receiving "bank address signals" as such signals were part of the control signals received for read, write, and bank activation. Brogioli, ¶¶41-42. For the same reason, they would understand that the inventors were in possession of the concept that the bank address signals were received by the logic element. *Id.*, ¶43.

To be clear, this is not a factual dispute between experts. The Petition simply applies the wrong standard. Petitioner's expert, Dr. Wolfe, opines that "the '244 provisional does not even mention the words 'bank address' anywhere, confirming that the applicants did not have possession [of the invention]." EX1003, ¶189. That is not the law. The Federal Circuit has made clear that the specification need not recite the claimed invention verbatim. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1352 (Fed. Cir. 2010) ("[T]he description requirement does not demand any particular form of disclosure, … or that the specification recite the claimed invention *in haec verba* ….").

By ignoring the background knowledge of a POSITA, Dr. Wolfe's approach is inconsistent with black-letter law. *Capon v. Eshhar*, 418 F.3d 1349, 1357-58 (Fed. Cir. 2005) ("The 'written description' requirement must be applied in the context of the particular invention and the state of the knowledge [in the art]."); *LizardTech, Inc. v. Earth Res. Mapping, Inc.*, 424 F.3d 1336, 1345 (Fed. Cir. 2005) ("[T]he patent specification is written for a [POSITA], and such a person comes to the patent with the knowledge of what has come before."). In contrast, Dr. Brogioli examines what a POSITA would have known as required by the law.

(c) '436 Patent

The '436 patent discloses increasing the memory capacity or memory density of a memory module by implementing a logic element that performs operations on certain input signals. *E.g.*, EX1009, 3:5-38; 17:30-18:11.[3] Fig. 11A illustrates an embodiment featuring a four-rank memory module with a logic element 640 which receives a first set of address and control signals, including at least bank address signals BNK0 and BNK1, addresses signal A13, and command signals such as RAS/CAS/WE, CS0 and CS1 (chip-select 0 and 1).

[3] The '436 patent incorporates by reference the '595 and '668 provisionals.

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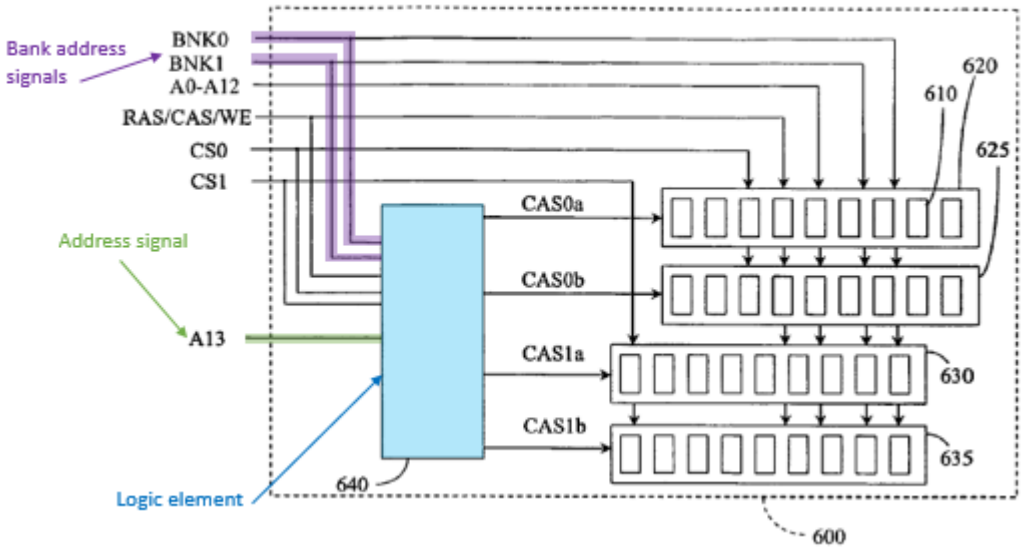
FIGURE 11A



To access a particular physical rank, "the two chip-select signals (CS0, CS1) are used with other address and control signals to gate a set of four CAS signals." EX1009, 17:30-34. In some embodiments the logic element "uses sequential and combinatorial logic to produce four gated chip-select signals (e.g., CS0a, CS0b, CS1a, and CS1b)." *Id.*, 18:6-9; *id.*, 17:41-45.

In the exemplary embodiment in Figure 11A, the logic element (blue) "receives a first set of address and control signals," *e.g.*, as depicted in Figure 11A, bank address signals (BNK0-1, purple), address signal A13, and chip-select signals CS0-CS1, and "translates the first set of address and control signals into a second set of address and control signals … which is transmitted to the first rank 620, the second rank 625, the third rank 630, and the fourth rank 635." *Id.*, 16:57-17:10.

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The ’436 patent also provides that “the logic element 640 comprises a programmable-logic device (PLD) 642 and four ‘OR’ logic elements.” EX1009, 17:41-45. The PLD 642 in turn can “comprise[] an ASIC, an FPGA, a custom-designed semiconductor device, or a CPLD.” *Id.*, 17:46-48; *see also id.*, 16:6-15 (similar disclosure for embodiment depicted in Figures 10A-10B). Specific examples of PLDs include those made by Altera or Xilinx. *Id.*, 17:48-52. In addition to the embodiment in Figures 11A-11B, the ’436 patent also illustrates a similar embodiment in Figures 10A-10B. *Id.*, 14:66-16:56. Petitioner makes three facially incorrect arguments to attack claim 16’s priority claim to the ’436 patent.

(i) <u>Alleged Absence of the “Circuit”</u>

Petitioner argues that the ’436 patent “lack[s] any embodiment including ‘a circuit’ comprising ‘a logic element’ and ‘a register.’” Pet., 64. But the ’436 patent expressly discloses embodiments featuring *registered* DIMMs. *See, e.g.*, EX1009, 7:22-28 (“[M]emory modules 100 compatible with embodiments described herein include, but are not limited to, ... registered DIMMs (RDIMMs)”). In the JEDEC design specification for DDR RDIMMs, the register is shown schematically, for example, for a x72 RDIMM. *See, e.g.*, EX1032, 4.20.4-10 to 4.20.4-16 (example below).

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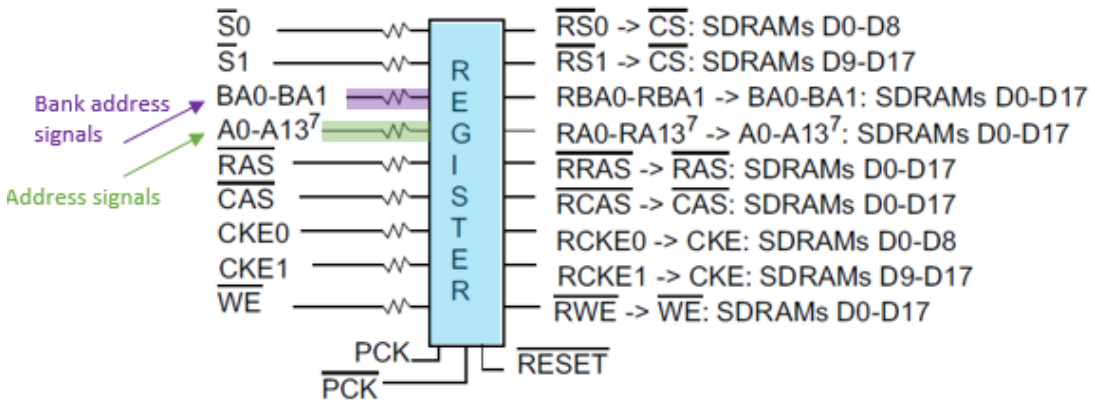
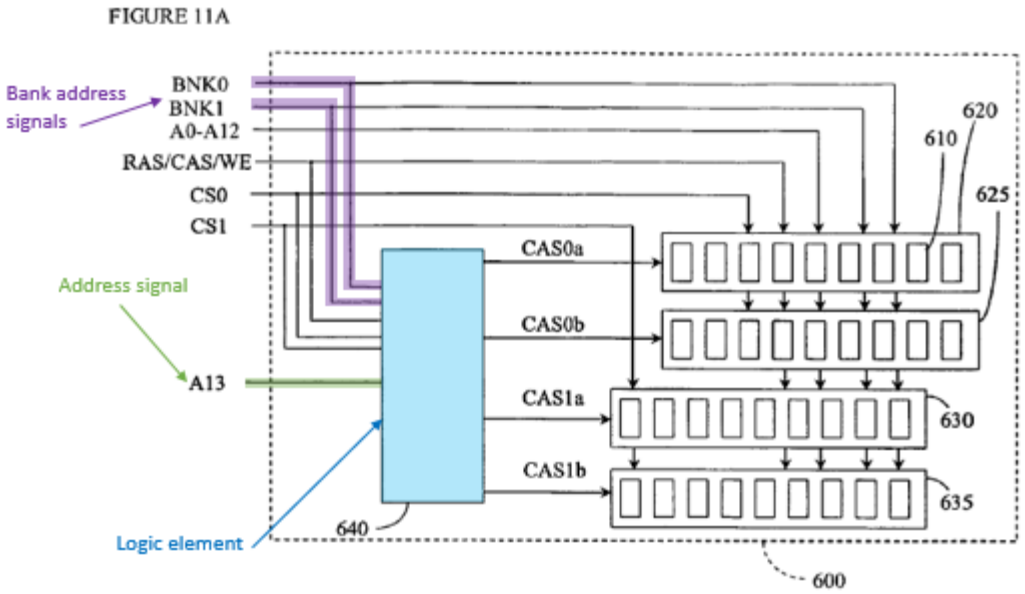


(EX1032, 4.20.4-12)



(EX1009, Fig. 11A)

Several of the signals entering the "REGISTER" function block are also depicted as entering logic element 640 in Figure 11A of the '436 patent, including two bank address signals (BA0-BA1), two chip-select signals S0/S1, the address bit A13 and RAS/CAS/WE, indicating that the "register" and "logic element" are part

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of the same component illustrated in the "REGISTER" function block above. Brogioli, ¶49. Indeed, during reexamination, the Board found that "registers [for an RDIMM] perform some type of logic function or comprise a logic circuit." EX1011, 19. Consistent with the Board's finding, Dr. Brogioli explains that a POSITA "would understand the 'REGISTER' function block in an RDIMM would include both logic elements for data processing and a register for storing data bits because (1) translating the input bits to output registered bits would involve the use of logic elements to process the input bits; and (2) the description of the functional block as a 'register' would indicate to a [POSITA] that the block included register functionality." Brogioli, ¶50.

Moreover, as noted above, the '436 patent discloses exemplary logic elements including ASICs, FPGAs, and CPLDs, (EX1009, 16:12-20, 17:46-52), at least some of which necessarily include registers. Brogioli, ¶51. Indeed, in referring to identical disclosure in the '912 patent during reexamination, the Board observed that "the expansive examples in the '912 patent of a logic element cover custom devices or a device of various discrete electrical components, which includes at least some types of registers." EX1011, 19; *see also id.*, 17 ("The '912 patent states that logic element 40 … can be a PLD, an ... (ASIC), ... (FPGA), or a ... (CPLD)."). As also explained by Dr. Brogioli, Altera and Xilinx PLDs specifically mentioned by the '436 patent (EX1009, 16:16-20, 17:48-50) suitable for memory applications

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included both logic elements and registers. EX2031, 39 (example of Xilinx FPGA featuring registers, reproduced below); Brogioli, ¶51.

XILINX SOLUTIONS

FIGURE 2-4: SPARTAN-3 FEATURES

The Spartan-3 FPGA memory architecture provides the optimal granularity and efficient area utilization.

Shift register SRL16 blocks

- Each CLB LUT works as a 16-bit fast, compact shift register
- Cascade LUTs to build longer shift registers
- Implement pipeline registers and buffers for video or wireless

Furthermore, with respect to the embodiment shown in Figures 10A-10B, the ’436 patent expressly discloses a “logic element 540” that includes a PLD 542 that would “save[] or latch[] the A13 address” during a row access for use as “an extra column address” in the subsequent column access. EX1009, 16:27-45. A POSITA would therefore understand that logic element 540 includes both the logic element and the “register” element for storing extra address bits. Brogioli, ¶52.

Thus, a POSITA would have understood that the ’436 discloses a circuit comprising a logic element and a register.

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(ii) Alleged Absence of Using "Row" and/or "Bank Address" signals

Petitioner argues that the '436 patent "lack[s] any Verilog code showing the use of 'row' and/or 'bank address signals.'" Pet., 64; EX1003, ¶190. First, the test for whether the inventor was in possession of the invention is not whether the inventors had reduced the inventions to actual practice. *Hologic, Inc. v. Smith & Nephew, Inc.*, 884 F.3d 1357, 1361 (Fed. Cir. 2018) (test for sufficiency of disclosure is "whether the disclosure of [earlier] application relied upon reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter" as of that earlier filing date). Second, the claim only requires "the circuit generating a set of output signals in response to the set of input signals" that include row and bank address signals. EX1001, p. 44, 3:28-29. This is clearly disclosed. For example, Figure 11B shows four gated CAS signals outputted in response to the set of input signals that include both row address signal A13 and bank address signals BNK0/1. *See also* EX1009, Fig. 10B (logic element 540 outputting rank-selection signals in response to input signals that include bank address signals and row address signal A13).

Moreover, the '436 patent explains that "[t]o access the additional memory density of the high-density memory module 600, the two chip-select signals (CS0, CS1) ***are used with other address and control signals*** to gate a set of four CAS

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signals." EX1009, 17:31-34. "For example, to access the additional ranks of four-rank 1-GB 128M 8-byte DDR1 DRAM memory module, the CS0 and CS1 signals along with the other address and control signals are used to gate the CAS signal appropriately, as schematically illustrated by FIG. 11A." *Id.*, 17:34-39.

As seen in the annotated Figure 11A above, the logic element (blue) receives both address signal (A13) and bank address signals (BNK0-1), and in response to A13, BNK0-1 as well as command signals CS0, CS1, RAS/CAS/WE, the logic element outputs four gated CAS signals. *Id.*, 17:31-34, 18:6-9, Fig. 11A; EX1029, at 49. A POSITA would therefore understand from Figure 11A that the "other address … signals" used by the '436 patent to "gate a set of four CAS signals" or generate four chip-select signals (EX1009, 17:31-34, 18:6-9) necessarily include the row address A13 and the bank addresses BNK0 and BNK1. Brogioli, ¶57; *see also*, EX1011, 88 (POSITA "would have reasonably concluded that the signals that enter logic element [] have some purpose and affect the output signals"); *infra* VII.A.3.

Moreover, a POSITA would necessarily understand that a bank address signal (e.g. BNK0 or BNK1) would be used, for example, to select the targeted memory bank for a command, per the DDR standards. Brogioli Decl. ¶¶37-42, 58; EX1009, 12:48-52 ("JEDEC standard JESD79D … [is] incorporated in its entirety by reference herein"); EX1029, 6 ("BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied."), 49 ("Bank addresses BA0, BA1,

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BA2 (BA) determine which bank is to be operated upon"). This is consistent with Petitioner's own theory that Perego-422 inherently discloses a logic element that receives a row address and bank address signals per the JEDEC standard. Pet., 36-37; Pet. 44-45 ("[T]o perform a read or write operation, the JEDEC standard … first requires a Bank Activate command with the row and bank address signals, followed by a read or write command with the corresponding bank address signals…. Thus, a POSITA would have understood that the target memory device and its target memory bank ***is selected in accordance with the bank address signals*** of the read or write command and ***the previously received row address and bank address signals*** of the activate command."); *supra*, VI.F.1(b).

Thus, a POSITA would have understood that the '436 discloses a circuit using a row and bank address signal.

(iii) Alleged Non-Enablement of the '436 Invention

Petitioner argues that the '436 patent fails to disclose any solution to the problem of executing a "standard" back-to-back read commands which crosses memory device boundaries ("BBARX"), and thus does not adequately support claim 16. Pet., 65-68. Petitioner contends that material added in the July 1, 2005 application that issued as the '386 patent provides the necessary support. *Id.*, 66.

A BBARX (*i.e.*, across memory device "a" in Rank0 and memory device "b" in Rank1) may result in collisions when "the last data strobe of memory device 'a'

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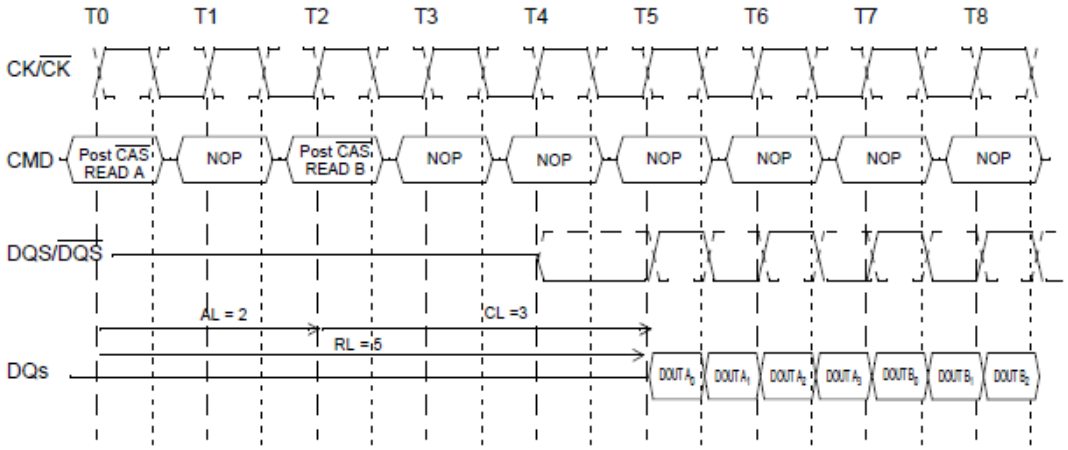
collides with the pre-amble time interval of the data strobe of memory device 'b.'" EX1008, 24:16-30. One solution is to "insert wait time intervals or clock cycles to avoid collisions or interference between [BBARX]." *Id.*, 24:15-17. However, in the context of rank multiplication, the memory controller is unaware of the physical boundaries of the memory devices on a rank. *Id.*, 24:19-30.

As an initial matter, Petitioner's citations do not support its claim that BBARX were "part of the normal operation of memory modules at the time." Pet., 66. Petitioner cites to the "seamless burst read operation" for DDR2 memories (EX1029, Fig. 27), as one such example. *Id.* A "[b]urst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle)." EX1029, 25. As illustrated below, in a seamless burst operation, the memory controller issues two read commands (Read A, Read B) at T0 and T2, separated by a NOP, which is followed by four-bit bursts of data starting at T5. *Id.*, 28. However, the timing issues that arise in the context of successive read bursts are different from a BBARX because there is only a single DQS preamble for the same read operation by the same memory device there is no DQS collision window. Brogioli, ¶62.



The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 27 — Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

Nor do the DDR standards Petitioner cite feature BBARX. Petitioner's Fig. 8 shows successive read commands to different columns *within* the same memory device, as confirmed by the description "Read commands shown must be to ***the same device***." EX1030, 19.

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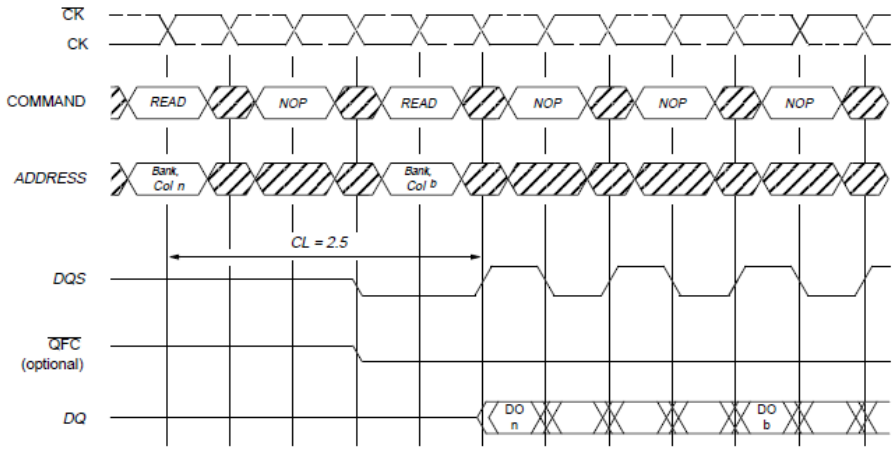

DO n (or b) = Data Out from column n (or column b)
Burst Length = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
3 subsequent elements of Data Out appear in the programmed order following DO n
3 (or 7) subsequent elements of Data Out appear in the programmed order following DO b
Shown with nominal tDQSCK, and tDQSQ
Read commands shown must be to the same device

Figure 8
CONSECUTIVE READ BURSTS – REQUIRED CAS LATENCIES

Moreover, nowhere does Petitioner address the standard for non-enablement, or argue that a POSITA starting with the '436 patent's disclosure would be unable to arrive at a rank-multiplied memory module capable of avoiding collisions during back-to-back read operations. *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 941 (Fed. Cir. 1990) ("It is not fatal if some experimentation is needed, for the patent document is not intended to be a production specification."). For example, a POSITA could readily configure the memory controller in a memory system featuring the '436 module to use appropriate timing sequences to avoid such collisions by inserting a delay between successive read commands, without the need to know the physical boundaries of the memory devices. Brogioli Decl., ¶64. As

Dr. Brogioli explains, a POSITA could also use a serial presence detect (SPD) device to inform the memory controller of the physical boundaries of each memory device, and insert delays where appropriate to avoid BBARX collisions. *Id.* As such, Petitioner has not sustained the high burden of demonstrating that the specification of the '436 patent lacks enabling disclosure for claim 16.

In short, Petitioner has not sustained its burden showing that Ellsberry can qualify as prior art. This is not because of a dispute of fact. This is because Petitioner's expert does not apply the correct legal standard for written description and the Petitioner does not apply the legal standard as to enablement.

2. Ellsberry Does Not Disclose [16.e.]

Petitioner argues that Ellsberry discloses transmitting a command signal to one DDR memory device at a time based on Ellsberry's alleged disclosure of a construct featuring single-device ranks where "an Activate, Write, or Read command signal is transmitted to only the selected memory device" and the other memory device "receives a no-operation (NOP) command." Pet., 109-10. Petitioner relies specifically on Figure 12 of Ellsberry, which Petitioner interprets as disclosing an 8-bit memory module with a single device per rank. *Id.*, 75-76.

As provided above, in the context of the '912 patent, the term "rank," properly construed, excludes single-device "ranks". *See supra*, VI.C; EX1011, 79.

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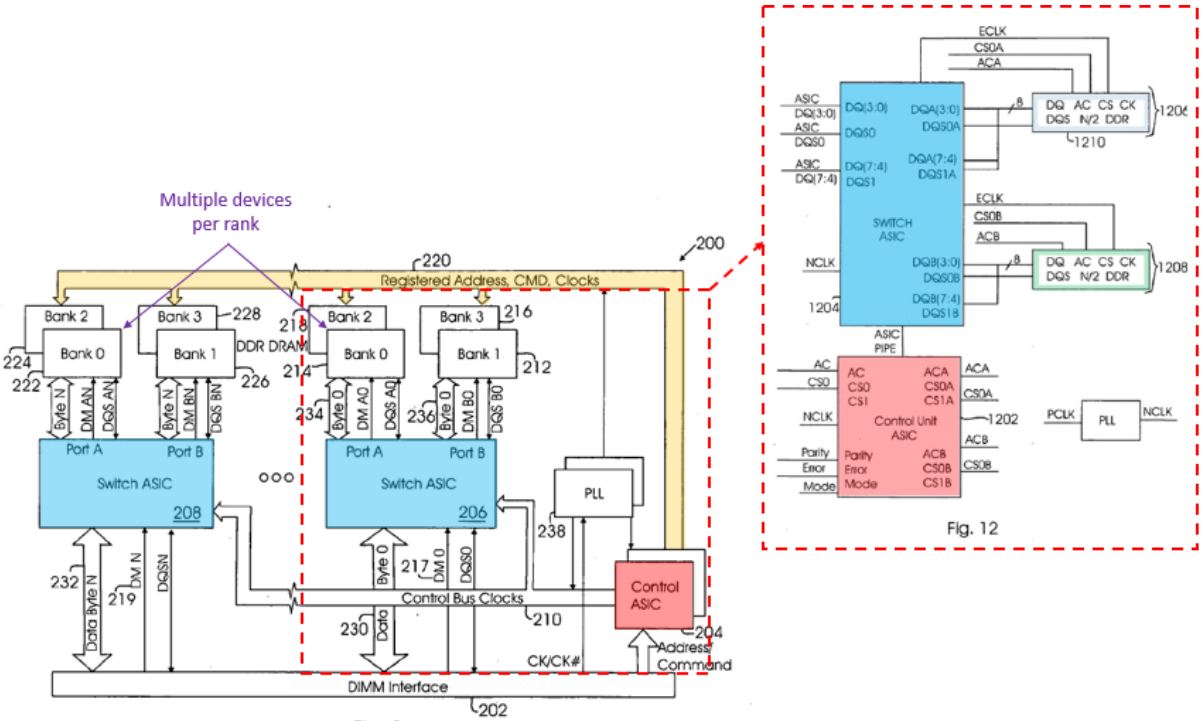
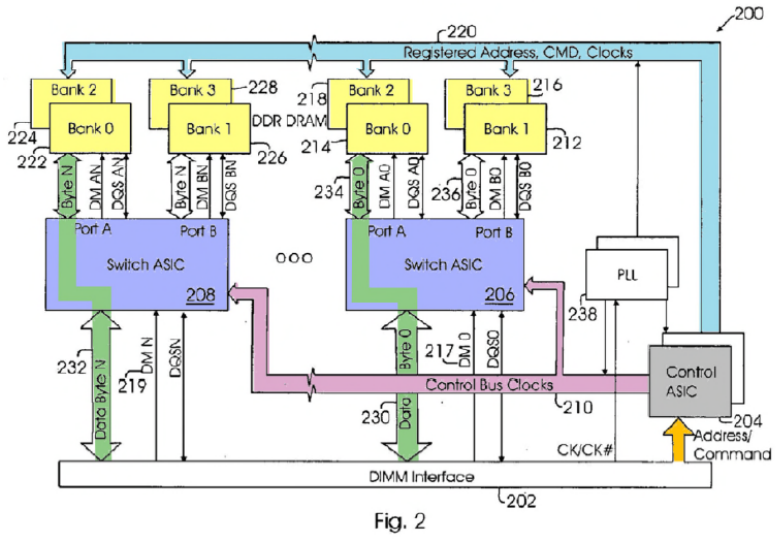
Petitioner's hypothetical single-device construct fails to render claim 16 obvious on this basis alone.

Nor does Ellsberry disclose a memory module with only a single device under Petitioner's improper construction of "rank." A POSITA reading Ellsberry as a whole would understand that Figures 10-13 of Ellsberry shows only components connected to a single switch ASIC, which is only a part of Ellsberry's overall architecture, as the Board previously found. *See, e.g.*, EX1038, 50 (noting "Figure 13 shows ***part of a memory module***"), 51, 57, 81; EX2032, 40 n.11 (agreeing with Samsung that "FIGS. 2, 5, and 13 of Ellsberry correspond to a 'First Embodiment' utilizing four ranks, each composed of nine 8-bit memory devices for a total bit width of 72"); Brogioli, ¶¶100-01.

That is, a POSITA would understand that Figure 12 (or Figure 13) relied on by Petitioner shows the structure for just one switch ASIC. *See* EX1037, Fig. 12; Brogioli, ¶99. Ellsberry's memory modules, however, each have multiple switch ASICs: Figure 2, for example, shows two switch ASICs, each connecting to multiple banks. *See id.*, Fig. 2 (reproduced below).



(EX1037, Fig. 2 as compared to Fig. 12)



(EX1037, Fig. 2 as annotated by Petitioner in IPR2022-00639)

Petitioner argues elsewhere in the Petition that a bank is another name for a rank. *See* Pet., 12 ("[T]he term 'bank' was … used to refer to what is now typically

called a 'rank'"), 74 (contending that "each of Ellsberry's four 'banks' discloses a respective 'rank'"). Thus, for example, in Figure 2, when Bank 1 is selected, there are at least two Bank 1 devices, device 226 connected to switch ASIC 208 and device 212 connected to Switch ASIC 206. EX1037, Fig. 2; Brogioli, ¶102. Device 226 and device 212 receives data bytes N and 0 respectively. EX1037, [0030]; [0031] (control unit 204 "causes the memory bank switch 206 and 208 to activate the correct memory bank").

Petitioner does not explain how Ellsberry could transmit a command to only one memory device at a time when there are multiple devices in a rank. Instead, a POSITA would understand that in Ellsberry, if commands are sent to devices in Bank 1, commands will be transmitted to at least two devices at a time via bus 220.[4] Brogioli, ¶¶100-02.

Similarly, Figure 5 shows multiple bank switches 508 (which is the same as bank switch 206 described in Figure 2), each connected to two memory devices 504 and 512, as is consistent with Figure 12. EX1037, [0050]. Again, Petitioner does not address how commands may be sent to a single device when there are multiple

[4] A command signal is "transmitted" to a targeted memory device only if it initiates an operation for the targeted memory device, consistent with the parties' agreed-upon construction of "command signal" in the Google Action. EX2026, 7 ("command signal" means "a signal that initiates a predetermined type of computer operation, such as read, write, refresh or precharge").

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devices in a rank.

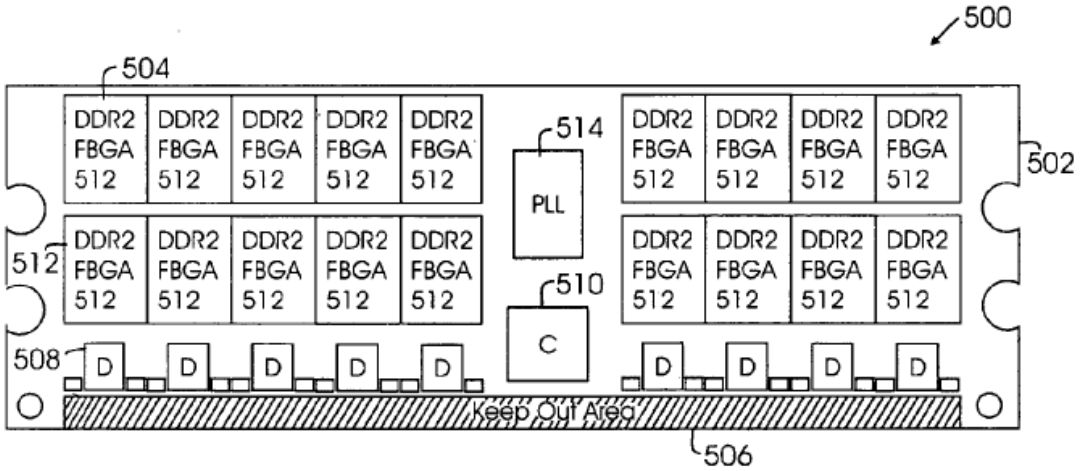

Fig. 5

Petitioner's citations do not support the proposition that Ellsberry discloses a memory module having only a single bank switch ASIC (or what Petitioner calls "a single data buffer"). Pet., 75, 76 (citing EX1037, [0021], [0030], [0035]). [0021] generically states that "FIGS. 10, 11, 12 and 13 illustrate different configurations of memory modules (e.g., DIMMs) that can be built using combinations of the control unit and bank switch according to various embodiments of the invention." *Id.*, [0021]. Indeed, as the Board previously noted, "in reference to Figures 10, 11, 12, and 13, Ellsberry states '[t]hese configurations employ the control unit and bank switch previously described,' ***thus relating these figures to the earlier-described control units and switches*** (including Figures 2, 5, and 6).'" EX1038, 77 (citing EX1037, [0052]).

Moreover, Ellsberry teaches that each switch ASIC in Figure 2 receives from the DIMM interface a range of data bits corresponding to a respective data group. EX1037, [0030]. However, [0030] discusses *multiple* data groups, not a single data group. *Id.* ("***A first data group*** (i.e., Data Group 0) is received by a first memory bank switch 206 while ***a second data group*** (i.e., Data Group N) is received by a second memory bank switch 208."). A POSITA would understand the reference to "N" Data Groups to mean that Ellsberry's overall architecture would include N switch ASICs, corresponding to, for example, a 64-bit (N = 8) or 72-bit (N = 9) memory module. Brogioli, ¶101.

Petitioner is apparently arguing that [0035] suggests starting from a single data group, as does Dr. Wolfe, who opines that "Ellsberry explains that the operation of one data group, as shown in Figs. 12 and 13, 'is expanded when implementing a wider memory bus formed by several data groups composed of a plurality of memory bank switches and the associated memories.'" Pet., 76; EX1003 ¶217 (quoting EX1037, [0035]). But the sentence immediately before the citation makes reference to ***two*** switch ASICs, which Ellsberry states correspond to ***two*** data groups:

> The control unit 204 then handles mapping the logical memory addresses it receives via the DIMM interface 202 to a corresponding bank for a particular memory bank coupled to the ***switches 206 and 208***. This same principal is expanded when implementing a wider

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> memory bus formed by several data groups composed of a plurality of memory bank switches and the associated memories. EX1037, [0035].

See also id., [0030] (noting that "***a first data group*** … is received by ***bank switch 206*** while a ***second data group*** … is received by ***bank switch 208***"). Thus, Ellsberry teaches starting with at least two bank switches, consistent with Figure 2's illustration of Ellsberry's overall architecture. Brogioli, ¶106; EX1037, Fig. 2.

Petitioner argues that it would have been obvious to a POSITA to make a module with only a single data group, "as expressly illustrated in Ellsberry's Figures 10-13," Pet., 76, but as discussed these figures only show a part of the total multi-data group module.[5] Petitioner also states that a POSITA would have understood that such a module "would have been simpler to make and required fewer parts, leaving fewer error sources," citing Dr. Wolfe's declaration which parrots the same without elaboration. *Id.*; EX1003, ¶218. Petitioner's conclusory approach is legally insufficient. *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355 (Fed. Cir. 2016) ("common sense" cannot "substitute for reasoned analysis and evidentiary support, especially when dealing with a limitation missing from the prior art references specified").

[5] Petitioner also incorrectly notes that the '912 patent discloses an embodiment with single-device ranks, which it does not. *See supra*, VI.C.

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Ellsberry discloses multiple switch ASICs, but no means of transmitting a command signal to individual memory devices in the same rank, which Petitioner equates to Ellsberry's "bank." Pet., 74 ("[E]ach of Ellsberry's four 'banks' discloses a respective 'rank'"); *id.*, 12. In fact, Ellsberry expressly states that "command information [is] received from the DIMM interface 202, buffered in a register 302 and ***sent to all memory banks*** (e.g., Bank 0, Bank 1, Bank 2 and Bank 3) over address bus 220." EX1037, [0039]; *see also id.*, [0030]. As shown in Figure 2, the DIMM interface 202 includes a byte-wide data groups (Data Byte 0-N) corresponding to each switch ASIC 206 and 208. *Id.*, Fig. 2, [0030]. Under Petitioner's theory, where a "bank" is interchangeable with "rank," and a "rank" of memory devices "act together in response to command signals," Pet. 12, a POSITA would understand that ***all the devices*** in one of the banks on Ellsberry's multiple-switch module (e.g., Bank1 composed of memory devices 212 and 226) act together in response to command signals. Brogioli, ¶108. This is consistent with Ellsberry's disclosure that interface 202 sends a range of byte-wide data signals corresponding to each switch ASIC 206 and 208 "***simultaneously***," such that "[d]ata may be read from or written to [the] memory devices." EX1037, [0030]. That is, read and write commands are sent simultaneously to multiple devices of the same rank. *Id.* Thus, Petitioner has failed to show that Ellsberry renders obvious to a POSITA transmitting a command signal to one memory device at a time.

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VII. THE BOARD SHOULD EXERCISE ITS DISCRETION TO DECLINE TO INSTITUTE UNDER SECTION 325(d)

The Board should deny institution of the Petition because "the same or substantially the same prior art or arguments previously were presented to the Office." 35 U.S.C. § 325(d). Petitioner's primary reference for Grounds 1 and 2 (Perego-422) is substantially the same as U.S. 7,356,639 to Perego ("Perego-639") that the Office expressly considered during prosecution of the '912 patent. Moreover, Petitioner's arguments for each ground—including Ground 3—are also substantially the same as arguments based on Amidi that the Office and the Board already rejected in the '912 reexamination. Petitioner also does not contend that in ***either*** instance, the Office, the Board, or the Federal Circuit committed material error. Pet., 112-13. Simply put, Petitioner presents no evidence justifying the premise in this IPR: that the ten years of labor invested by countless examiners, ALJs, Federal Circuit judges, lawyers, and clerks was worthless.

A. The *Advanced Bionics* Framework

Under *Advanced Bionics*, the Board first asks "whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office." *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020) (precedential). If either is satisfied,

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Petitioner must demonstrate that the "Office erred in a manner material to the patentability of challenged claims." *Id.*, at 8.

1. Perego-422 Is Materially the Same as Perego-639 Considered By the Office

Netlist listed Perego-639 in an IDS dated June 19, 2009. EX1002, 125. The Examiner expressly considered Perego-639, as indicated by the annotation "ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH" and the lack of any line through Perego-639. Perego-639 is also cited on the face of the '912 patent. EX1001, p. 2.

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Receipt date: 06/19/2009

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	11/862,931
	Filing Date	September 27, 2007
	First Named Inventor	Jayesh R. Bhakta et al.
	Art Unit	2824
(Multiple sheets used when necessary)	Examiner	Alexander Sofocleous
SHEET 3 OF 7	Attorney Docket No.	NETL.018CP1C1

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	59	US 6961281	11-01-2005	Wong et al.	
	60	US 6981089	12-27-2005	Dodd et al.	
	61	US 6982892	01-03-2006	Lee et al.	
	62	US 6982893	01-03-2006	Jakobs	
	63	US 6999686	02-07-2006	Doblar et al.	
	64	US 7007175	02-28-2006	Chang et al.	
	65	US 7007130	02-28-2006	Verbrugge	
	66	US 7120727	10-10-2006	Lee et al.	
	67	US 7124260	10-17-2006	LaBerge et al.	
	68	US 7133972	11-07-2006	Jeddeloh	
	69	US 7133960	11-07-2006	Thompson et al.	
	70	US 7181591	02-20-2007	Tsai	
	71	US 7200021	04-03-2007	Raghuram	
	72	US 7266639	09-04-2007	Raghuram	
	73	US 7281079	10-09-2007	Bains et al.	
	74	US 7289386	10-30-2007	Bhakta et al.	
	75	US 7346750	03-18-2008	Ishikawa	
	76	US 7356639	12-23-2004	Perego et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Foreign Patent Document Country Code-Number-Kind Code Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T[1]
	77	WO 1992/002879	02-20-1992	Du Pont Pixel Systems Limited		
	78	WO 1994/007242	03-31-1994	Atmel Corporation		
	79	WO 1995/034030	12-14-1995	Intel Corporation		
	80	WO 2002/058069	07-25-2002	Honeywell International Inc.		
	81	WO 2003/017283	02-27-2003	Micron Technology, Inc.		
	82	WO 2003/069484	08-21-2003	Micron Technology, Inc.		
	83	WO 2006/055497	05-26-2006	Intel Corporation		

Examiner Signature /Alexander Sofocleous/ Date Considered 09/08/2009

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] - Place a check mark in this area when an English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /AGS/

EX1002, 523 (annotated).

Perego-639 is materially identical to Perego-422 cited in the Petition. *See generally* EX2025 (redline comparing Perego references). Indeed, ***every portion*** of Perego-422 that Petitioner relies on is present in the considered Perego-639 reference. *See id*. (highlighting cited-to Perego-422 disclosure). Because the Office already considered the pertinent parts of Perego-422 when it considered Perego-639,

the Board should deny institution, especially since Petitioner does not assert the Office made a material error. *Nespresso USA, Inc. v. K-Fee System GMBH*, IPR2021-01221, Paper 9, at 13-14 (P.T.A.B. Jan. 18, 2022) (denying institution of IPR where three of five references cited in IPR were not used as a basis for rejection and only "appear[ed] on a relatively long list of documents presented to the Examiner in an IDS," because "[c]lear intrinsic evidence informs, 'All references' submitted in the IDSs were 'considered except where lined through'"); *Boragen, Inc. v. Syngenta Participations AG*, IPR2020-00124, Paper 16, at 21 (P.T.A.B. May 5, 2020) (finding the same references were considered by the Office based on evidence "that the same disclosures that Petitioner cites from Baker were in the related Baker references before the Examiner").

Petitioner's reliance on Amidi in Ground 2 does not materially alter the 325(d) analysis because Amidi was discussed at length during reexamination and as Petitioner admits, "Amidi is used here only as a secondary reference … to the extent one were to conclude that Perego alone does not disclose or render those limitations obvious." Pet., 112. Thus, the Board should decline to institute on Grounds 1 and 2 under 325(d).

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2. Ellsberry Was Considered By the Office

Petitioner acknowledges that Ellsberry was before the Office, but "the Examiner … assumed Ellsberry was not prior art." Pet., 112. As discussed in Section VI.F.1, the Examiner was correct that Ellsberry did not qualify as prior art.

3. Petitioner's Priority Date Arguments Contradict the Board's Explicit Findings

To qualify Ellsberry as prior art, Petitioner primarily argues that the priority applications fail to disclose a "logic element" that receives bank address signals ('244 provisional), or that uses row and/or bank address signals ('436 patent). Pet., 63-64. During reexamination, Inphi similarly argued that claims reciting a "logic element [that] generates a first number of chip-select signals … in response at least in part to clock signals received from the [PLL]" were unsupported by the '912 patent, because a POSITA "would not have known for certain how the signals from PLL 50 were used by logic element 40." EX1011, 88. The Board rejected this argument, concluding that "Figure 1A shows the signals that enter logic element 40, including the clock signal of PLL 50," and thus a POSITA "would have reasonably concluded that ***the signals that enter logic element 40 have some purpose and affect the output signals which are only chip-select signals*** (e.g., CS_{0A}-CS_{1B})." *Id.*, 88-89.

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Here too, both priority documents feature figures depicting a "logic element" receiving a bank address signal ('244 provisional) or a row and bank address signal ('436 patent). EX1005, Fig. 1 ("Control Signals"); EX1009, Fig. 11a; *supra* VI.F.1(b)-VI.F.1(c). In particular, Figure 11A of the '436 patent illustrates that the signals that enter logic element 640 include a row address signal A13, and bank address signals BNK0 and BNK1, demonstrating, as the Board found, that a POSITA would have reasonably concluded that those signals "have some purpose and affect the output signals," i.e., four gated CAS signals or chip-select signals. EX1009, 16:57-17:10, 17:31-34, 18:6-9. Thus, Petitioner's priority arguments should also be rejected under 325(d).

4. Petitioner's Arguments Are Cumulative

Claim 16 recites that "the command signal is transmitted to only one DDR memory device at a time." EX1001, p. 44, 3:42-43. During reexamination, the Examiner implicitly construed [16.e] as requiring the command signal be transmitted to a single memory device in a rank featuring ***more than one memory device***. *Id.*, 3865-67, 3904. The Board affirmed. EX1011, 78-80. Petitioner now asks the Board to reject its previous construction. *See* Pet., 31-43, 75-76.

(a) Grounds 1 and 2 Are Cumulative

Petitioner contends Perego-422's Figure 4B, when modified to include only ranks with a single memory device, renders obvious claim 16. Pet., 31, 43. This

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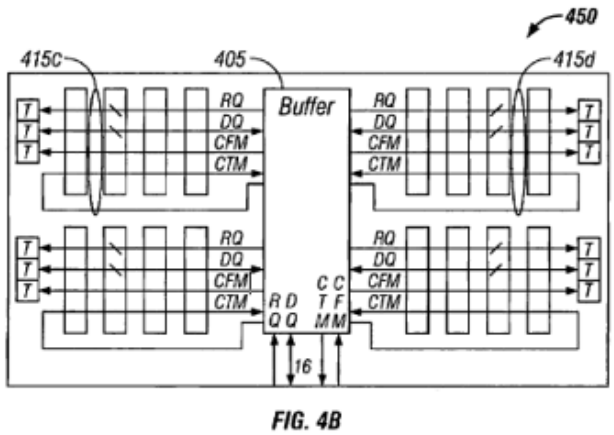
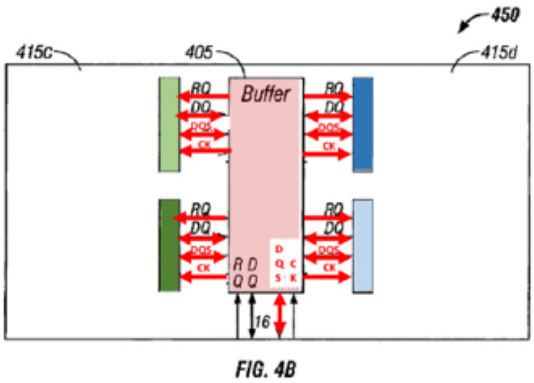
ignores the Examiner's and Board's determinations in reexamination that the claimed "ranks" have more than one memory device per rank. Just as Requesters' argument regarding Amidi failed to address the requirement that a command be transmitted to a single memory device on a "rank," which in the '912 patent features multiple devices (EX1010, 3865-67, 3904; EX1011, 79), so too does Petitioner's Perego-422 theory.



EX1035, Fig. 4B



Pet., 62 (modified Figure 4B)

Petitioner's modified version of Figure 4B is reproduced above on the right. In such a module with single-device "ranks," Petitioner argues that Perego-422 teaches transmitting a command signal to one memory device at a time. Pet. at 61-63 (citing EX1035, 15:31-45). This argument is just a surreptitious attempt to

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convince the Board to abandon its ruling in the reexamination that the '912 patent required "ranks" with multiple devices per rank.

But just as the Requesters failed to do during reexamination, Petitioner does not identify how Perego-422 teaches a POSITA to transmit a command signal to a single memory device in a rank with a *plurality* of memory devices. *See supra*, VI.E.2.

Thus, Petitioner's theory regarding Perego-422 is cumulative of the Requesters' Amidi-based theory in reexamination. That Ground 2 is supplemented by Amidi's rank multiplication teachings is immaterial, because as noted above Amidi was extensively considered during reexamination, and is not relied on for [16.e]. Pet., 61-63, 112.

(b) Ground 3 Is Cumulative

Petitioner next argues that Ellsberry's Figures 12 and 13 when modified to include single-device ranks render obvious claim 16. Pet., 76-77. As above, just as Inphi's theory regarding Amidi failed to address the requirement that a command be transmitted to a single memory device on a rank featuring multiple devices (EX1010, 3865-67, 3904; EX1011, 79), so too does Petitioner's Ellsberry theory. *See supra*, VI.F.2.

Petitioner contends that Ellsberry's Figures 12-13 teach a memory module with a single "data buffer" (switch ASIC 1204) connected to memory banks (which

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Petitioner maps to the claimed "ranks"). Pet., 75-77; EX1003, ¶124. In these single-device rank constructs, Petitioner contends that when control ASIC 204 transmits a command to a specific memory ***bank*** connected to switch ASIC, it necessarily transmits that command to a single memory device at a time (because there is only one memory device in said bank). Pet., 109-110.

But as discussed above in Section VI.F.2, Petitioner is incorrect that "Ellsberry teaches a POSITA that a memory module can include only a single data group having a [single] data buffer." Pet. 76 (citing [0021], [0030], [0035]). In fact, Ellsberry contains only evidence to the contrary. *See, e.g.*, EX1037, [0030] (discussing ***two*** bank switches that receive a respective "first data group … received by a ***first memory bank switch 206***" and "a second data group … received ***by second memory bank switch 208***"); *id.*, [0035] (embodiment with ***two*** "***switches 206 and 208***," each associated with its respective data group); *supra* VI.F.2. Indeed, Ellsberry's Figure 2, of which Figures 12-13 are a part of, depicts ***two*** switch ASICs (each what Petitioner calls a "data buffer"). Figure 5 depicts ***nine*** switch ASICs. EX1037, [0035], [0050]. That means, even if each bank that is connected to a single switch ASIC has only one memory device, there are multiple memory devices in each rank/bank per module.

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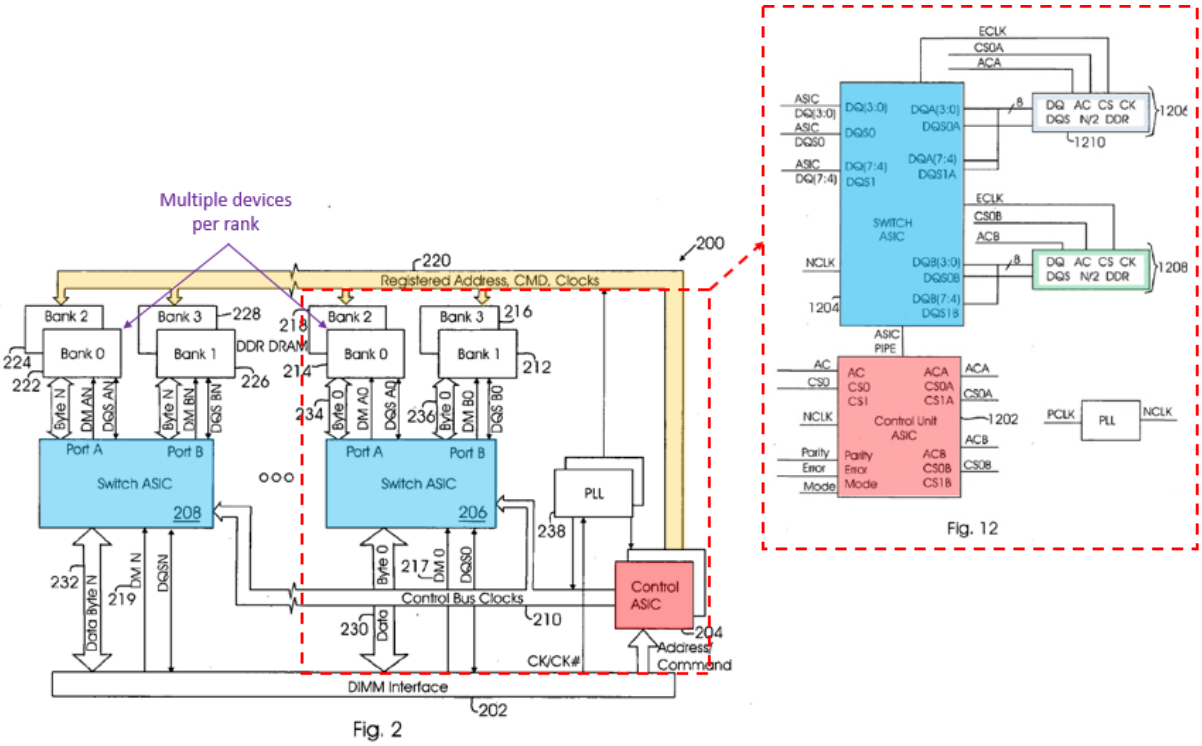

(EX1037, Fig. 2 as compared to Fig. 12)

Petitioner's analysis fails to acknowledge that each of Figures 12-13 represents only a portion of the overall multiple-switch ASIC architecture depicted in Fig. 2, as the Board previously found. *See, e.g.*, EX1038, 50 (noting "Figure 13 shows ***part of a memory module***"), 51, 57, 77, 81; EX2032, 40 n.11; *supra*, VI.F.2. As depicted above in Figure 2, commands are transmitted from control ASIC 204 via bus 220 to the memory banks directly; not to switch ASICs 206 and 208. *Id.*, [0028]-[0029]. The memory devices in the selected bank are accessed. *Id.*, [0031]. Because Ellsberry discloses only multiple-switch ASIC configurations where each rank would have more than one memory device (*see* annotation above), Petitioner's

theory suffers from the same flaw as Requesters, i.e., fails to show how the command signal is transmitted to only one memory device in a rank. *See supra*, VI.F.2.

5. Petitioner Has Not Demonstrated That the Office Materially Erred

The second step of the analysis examines whether the Office had materially erred. *Becton Dickinson,* Paper 8, 17–18.

First, as to Grounds 1 and 2, Petitioner only argues that the Office did not consider Perego-422, but does not assert that the Examiner materially erred in allowing claim 16 of the ’912 patent in light of Perego-639’s teachings. Pet., 112. But that is incorrect because the Office considered related Perego-639 that is materially the same in pertinent parts. *See* VII.A.1 above. *Second*, as to Ground 3, claim 16 is entitled to a priority date at least as of the filing date of the ’244 provisional or the ’436 patent. *See*, *supra* VI.F.1. Thus, the examiner did not err in finding that Ellsberry was not prior art. EX1002, 510.

Third, as to all grounds, Petitioner does not challenge the Examiner’s and the Board’s findings that claim 16 requires transmitting a command signal to only one DDR memory device at a time “when there is a plurality of memory devices in a rank.” *See* EX1011, 79; Pet., 112-13. Instead, Petitioner bases its “new” invalidity arguments on constructs that include only a single device per rank. *See supra*, VII.A.4. Because Petitioner fails to present any argument distinguishing the Board’s

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finding with respect to claim 16 during reexamination, it "would not be an efficient use of Board resources" to institute review in this case. *Unified Patents Inc. v. Berman*, IPR2016-01571, Paper 10, 12 (Dec. 14, 2016) (informative).

VIII. CONCLUSION

Based on the foregoing, the Board should decline to institute an *inter partes* review.

Dated: July 21, 2022

Respectfully submitted,

/Hong Zhong/

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CERTIFICATE OF WORD COUNT

I hereby certify, pursuant to 37 C.F.R. section 42.24, that the foregoing Patent Owner Preliminary Response contains 14,987 words, excluding the words in the table of contents, table of authorities, mandatory notices under section 42.8, this certificate of word count, certificate of service or exhibit list. The word count is based on the word count of the Microsoft Word program used to prepare the Patent Owner Preliminary Response.

/Hong Zhong/
H. Annita Zhong (66,530)

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CERTIFICATE OF SERVICE

I hereby certify, pursuant to 37 C.F.R. section 42.6, that on July 21, 2022, a complete copy of the **PATENT OWNER'S PRELIMINARY RESPONSE and EXHIBITS 2001-2034** were served upon the following, by ELECTRONIC MAIL:

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