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(54) **MEMORY MODULE DECODER**

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Related U.S. Application Data

(63) Continuation of application No. 11/862,931, filed on Sep. 27, 2007, now Pat. No. 7,619,912, which is a continuation of application No. 11/173,175, filed on Jul. 1, 2005, now Pat. No. 7,289,386, and a continuation-in-part of application No. 11/075,395, filed on Mar. 7, 2005, now Pat. No. 7,286,436.

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G11C 5/06	(2006.01)
G11C 7/10	(2006.01)
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CPC ***G11C 8/12*** (2013.01); ***G06F 12/0207*** (2013.01); ***G06F 12/0215*** (2013.01); ***G11C 5/04*** (2013.01); ***G11C 5/066*** (2013.01); ***G11C 7/1048*** (2013.01); ***H05K 1/181*** (2013.01); *G11C 2207/105* (2013.01); *H05K 2201/10159* (2013.01); *H05K 2203/1572* (2013.01); *Y02P 70/611* (2015.11)

(58) **Field of Classification Search**

None

See application file for complete search history.

(56) **References Cited**

To view the complete listing of prior art documents cited during the proceeding for Reexamination Control Number 95/001,758, please refer to the USPTO's public Patent Application Information Retrieval (PAIR) system under the Display References tab.

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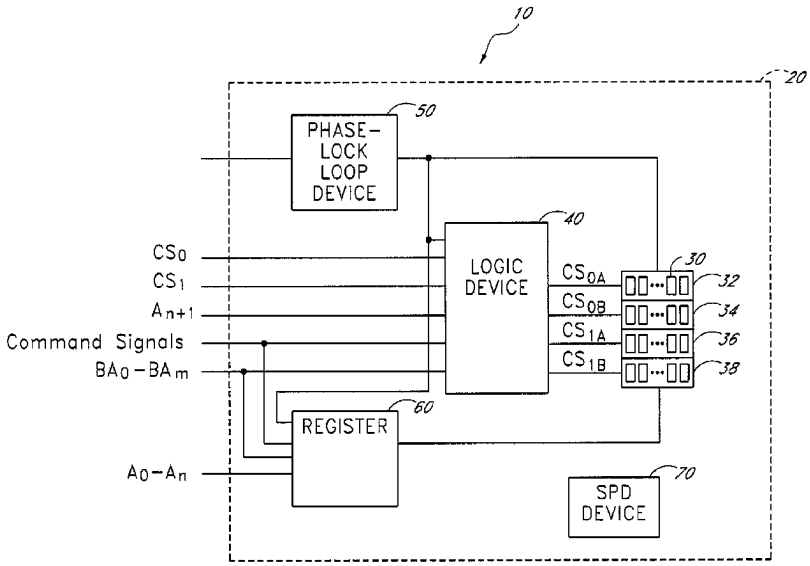
(57) **ABSTRACT**

A circuit is configured to be mounted on a memory module connectable to a computer system so as to be electrically coupled to a plurality of memory devices on the memory module. The plurality of memory devices has a first number of memory devices. The circuit comprises a logic element configurable to receive a set of input signals from the computer system. The circuit further comprising a register and a phase-lock loop circuit, the phase-lock loop circuit configurable to be operatively coupled to the plurality of memory devices, the logic element, and the register. The set of input signals corresponds to a second number of memory devices smaller than the first number of memory devices.



INTER PARTES REEXAMINATION CERTIFICATE

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

Claims **1**, **4**, **13**, **19** and **20** are cancelled.

Claims **2**, **5-12** and **14-18** are determined to be patentable as amended.

Claim **3**, dependent on an amended claim, is determined to be patentable.

2. The circuit of claim **[1]** *12*, wherein the set of input signals comprises a first number of chip-select signals and wherein the set of output signals comprises a second number of chip-select signals greater than the first number of chip-select signals.

5. The circuit of claim **[1]** *12*, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.

6. **[**The circuit of claim **1**,**]** *A circuit configured to be mounted on a memory module so as to be electrically coupled to a first number of double-data-rate (DDR) memory devices arranged in a first number of ranks on the memory module, the memory module configured to be electrically coupled to a memory controller of a computer system so as to receive a set of input signals from the computer system, the set of input signals comprising row/column address signals, bank address signals, and chip-select signals, the set of input signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit comprising:*

a logic element configurable to receive the bank address signals, at least one chip-select signal of the chip-select signals, and at least one row address signal of the row/column address signals from among the set of input signals;

a register; and

a phase-lock loop circuit configurable to be operatively coupled to the first number of DDR memory devices, the logic element, and the register, wherein, in response to signals received from the computer system, the phase-lock loop (PLL) circuit transmits a PLL clock signal to the first number of DDR memory devices, the logic element, and the register,

wherein the circuit is configurable to generate a set of output signals in response to the set of input signals, the set of output signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit is configurable to further respond to the set of input signals from the computer system by generating and transmitting the set of output signals to the first number of DDR memory devices,

wherein the register (i) receives, from among the set of input signals, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the first number of DDR memory devices, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element, wherein the bank address signals of the set of input signals are received by both the logic element and the register,

wherein the logic element generates rank-selecting signals of the output signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal received by the logic element and (iv) the PLL clock signal,

wherein the circuit further responds to an input command signal from the computer system by generating an output command signal comprising a read command signal or a write command signal, wherein the at least one row address signal is a density transition bit, and the logic element stores the density transition bit during an activate command for a selected bank, wherein the density transition bit is stored for subsequent use for the output command signal.

7. The circuit of claim **[1]** *12*, wherein two or more of the phase-lock loop circuit, the register, and the logic element are portions of a single component.

8. The circuit of claim **[1]** *12*, wherein the register comprises a plurality of register circuits.

9. The circuit of claim **[1]** *12*, wherein the plurality of DDR memory devices comprises a plurality of DDR**3** memory devices.

10. The circuit of claim **[1]** *12*, wherein the set of input signals corresponds to a first memory density per rank, and the set of output signals corresponds to a second memory density per rank, the second memory density per rank less than the first memory density per rank.

11. The circuit of claim **[1]** *12*, wherein the circuit is configurable to further respond to the set of input signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output signals to at least one DDR memory device of the selected at least one rank of the first number of ranks.

12. **[**The circuit of claim **1**,**]** *A circuit configured to be mounted on a memory module so as to be electrically coupled to a first number of double-data-rate (DDR) memory devices arranged in a first number of ranks on the memory module, the memory module configured to be electrically coupled to a memory controller of a computer system so as to receive a set of input signals from the computer system, the set of input signals comprising row/column address signals, bank address signals, and chip-select signals, the set of input signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit comprising:*

a logic element configurable to receive the bank address signals, at least one chip-select signal of the chip-select signals, and at least one row address signal of the row/column address signals from among the set of input signals;

a register; and

a phase-lock loop circuit configurable to be operatively coupled to the first number of DDR memory devices,

the logic element, and the register, wherein, in response to signals received from the computer system, the phase-lock loop (PLL) circuit transmits a PLL clock signal to the first number of DDR memory devices, the logic element, and the register,

wherein the circuit is configurable to generate a set of output signals in response to the set of input signals, the set of output signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit is configurable to further respond to the set of input signals from the computer system by generating and transmitting the set of output signals to the first number of DDR memory devices,

wherein the register (i) receives, from among the set of input signals, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the first number of DDR memory devices, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element,

wherein the logic element generates rank-selecting signals of the output signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal received by the logic element and (iv) the PLL clock signal,

wherein the circuit further responds to an input command signal from the computer system by generating an output command signal corresponding to a read command or a write command, wherein the at least one row address signal of the set of the input signals is a density transition bit, and

wherein *the logic element of* the circuit is configurable to store **[**an input signal of the set of the input signals**]** *the density transition bit* during **[**a row access procedure**]** *an activate command for a selected bank, wherein the density transition bit is stored* for subsequent use during the read command or the write command **[**a column access procedure**]**, *wherein the activate command is a row access procedure, wherein the read command or the write command is a column access procedure.*

14. The circuit of claim **[13]** *15*, wherein the set of input signals comprises a number of chip-select signals and wherein the set of output signals comprises more chip-select signals than the number of chip-select signals.

15. **[**The circuit of claim **13,]** *A circuit configured to be mounted on a memory module so as to be electrically coupled to a first number of double-data-rate (DDR) memory devices arranged in a first number of ranks on the memory module, the memory module configured to be electrically coupled to a memory controller of a computer system so as to receive a set of input signals from the computer system, the set of input signals comprising row/column address signals, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit comprising:*

a logic element configurable to receive the bank address signals, the at least one chip-select signal, and at least one row address signal of the row/column address signals from among the set of input signals;

a register; and

a phase-lock loop circuit configurable to be operatively coupled to the first number of DDR memory devices, the logic element, and the register, wherein, in response to signals received from the computer system, the phase-lock loop (PLL) circuit transmits a PLL clock signal to the first number of DDR memory devices, the logic element, and the register,

wherein the circuit is configurable to generate a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit is configurable to transmit the set of output signals to the first number of DDR memory devices,

wherein the register (i) receives, from among the set of input signals, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the first number of DDR memory devices, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element,

wherein the logic element generates rank-selecting signals of the output signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal received by the logic element and (iv) the PLL clock signal,

wherein the circuit further responds to an input command signal from the computer system by generating an output command signal corresponding to a read command or a write command, wherein the at least one row address signal of the set of the input signals is a density transition bit, and

wherein *the logic element of* the circuit is configurable to store **[**an input signal of the set of input signals**]** *the density transition bit* during **[**a row access procedure**]** *an activate command for a selected bank, wherein the density transition bit is stored* for subsequent use during **[**a column access procedure**]** *the read command or the write command, wherein the activate command is a row access procedure, wherein the read command or the write command is a column access procedure.*

16. The circuit of claim **[13]** *15*, wherein the circuit is configurable to select at least one rank of the first number of ranks and to transmit the set of output signals to at least one DDR memory device of the selected at least one rank of the first number of ranks.

17. The circuit of claim **[13]** *15*, wherein two or more of the phase-lock loop circuit, the register, and the logic element are portions of a single component.

18. The circuit of claim **[13]** *15*, wherein the set of input signals corresponds to a first memory density per rank, and the set of output signals corresponds to a second memory density per rank, the second memory density per rank less than the first memory density per rank.

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