Trials@uspto.gov
571.272.7822

Paper No. 36
Filed: March 29, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

DIABLO TECHNOLOGIES INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2014-00882
Patent 7,881,150 B2

Before LINDA M. GAUDETTE, BRYAN F. MOORE, and GEORGIANNA W. BRADEN, *Administrative Patent Judges*.

GAUDETTE, *Administrative Patent Judge*.

DECISION ON REMAND
35 U.S.C. § 144 and 37 C.F.R. § 42.5(a)

I. INTRODUCTION

This Decision addresses the order of the United States Court of Appeals for the Federal Circuit in *Netlist, Inc. v. Diablo Technologies, Inc.*, 701 F. App'x 1001 (Fed. Cir. 2017) ("*Netlist*"), vacating our opinion with respect to U.S. Patent 7,881,150 B2 (Ex. 1001 ("the '150 patent")), and remanding for further proceedings. Having analyzed the entirety of the record anew in light of the court's directive in *Netlist*, we conclude that Petitioner has shown by a preponderance of the evidence that claims 15–17, 22, 24, 26, and 31–33 of the '150 patent are unpatentable.

A. Procedural History

Diablo Technologies, Inc. ("Petitioner") filed a Petition (Paper 5, Corrected Petition ("Pet.")) requesting *inter partes* reviews of claims 15–17, 22, 24, 26, and 31–33 of the '150 patent. On the same day, Diablo also filed a second petition requesting *inter partes* review of the '150 patent in *Diablo Technologies, Inc. v. Netlist, Inc.*, Case IPR2014-01011 ("IPR1011"), and a petition requesting *inter partes* review of U.S. Patent 8,081,536 B1 ("the '536 patent") in *Diablo Technologies, Inc. v. Netlist, Inc.*, Case IPR2014-00883 ("IPR883"). The '536 patent is a continuation of the application that issued as the '150 patent. *See* IPR883, Ex. 1001 (the '536 patent), (63).

In its Petition, Petitioner did not assert that any claim terms required express construction. *See* Pet. 11–15. Netlist, Inc. ("Patent Owner"), however, filed a Preliminary Response to the Petition wherein it proposed constructions for three claim terms, including the term "selectively electrically coupling," recited in challenged independent claims 15 and 31. Paper 9 ("Prelim. Resp."), 13–19.

Petitioners
Ex. 1040, p. 2

In our Institution Decision, we agreed that express construction of the term "selectively electrically coupling" was necessary, but determined Patent Owner had not proposed the broadest reasonable construction of this term. *See* Paper 11 ("Inst. Dec."), 9–11. Accordingly, we applied our own construction of "selectively electrically coupling" in instituting an *inter partes* review of '150 patent claims 15–17, 22, 24, 26, and 31–33. *See generally id.* at 12–33.

Patent Owner subsequently filed a Patent Owner Response (Paper 25 ("PO Resp.")), and Petitioner filed a Reply (Paper 27 ("Reply")). An oral hearing, consolidated with IPR883 and IPR1011, was held on July 28, 2015. Paper 31 (Record of Oral Hearing).

On December 14, 2015, this Board issued a Final Written Decision in the present *inter partes* review, wherein we modified our prior construction of "selectively electrically coupling"; we again declined to adopt Patent Owner's proposed construction of this term. *See* Paper 33 ("Final Decision" or "Final Dec."), 11–13. In our final decision in IPR1011, we also construed the claim term "selectively isolating," which is recited in '150 patent claims 24 and 26[1]; we declined to adopt Patent Owner's proposed construction of this term. *See* IPR1011, Paper 34, 11–13. In our Final Decision in the present *inter partes* review, we applied these constructions of the terms "selectively electrically coupling" and "selectively isolating" in holding unpatentable all challenged claims of the '150 patent as follows:

[1] Claim 26 recites "selectively isolate." For convenience, our discussion below refers to the term "selectively isolating." However, our findings and conclusions also apply to the term "selectively isolate."

Petitioners
Ex. 1040, p. 3

References	Basis	Claims Challenged	Claims Held Unpatentable
Amidi[2] & Klein[3]	§ 103	15–17, 22, 24, 26, and 31–33	15–17, 22, 24, 26, and 31–33
Amidi & Wiggers[4]	§ 103	15–17, 22, 24, 26, and 31–33	15–17, 22, 24, 26, and 31–33

Final Dec. 50. We likewise held unpatentable all challenged claims of the '150 patent in IPR1011. IPR1011, Paper 34. We applied our own construction of the '536 patent claim term "selectively isolating" in holding unpatentable all challenged '536 patent claims in IPR883. IPR883, Paper 33.

Patent Owner filed a Notice of Appeal to the United States Court of Appeals for the Federal Circuit requesting review of our unpatentability determinations. Paper 34. The Federal Circuit consolidated the appeal from our decision in the present *inter partes* review with Patent Owner's concurrently-filed appeals from our decisions in related cases IPR883 and IPR1011. *Netlist*, 701 F. App'x at 1002.

On July 25, 2017, the Federal Circuit issued a decision determining that we erred in our construction of the '150 patent claim term "selectively electrically coupling." *Id.* at 1005. The court further determined that because the construction of "selectively isolating" applied in our analysis of the challenges to the '150 patent claims was based on an erroneous construction of "selectively electrically coupling," we likewise erred in the construction of "selectively isolating" applied in this *inter partes* review and

[2] U.S. Patent Publication 2006/0117152 A1 (Ex. 1008).
[3] U.S. Patent Publication No. 2001/0008006 A1 (Ex. 1009).
[4] U.S. Patent 6,011,710 (Ex. 1010).

Petitioners
Ex. 1040, p. 4

in IPR1011. *Id.* (noting that "[t]he specification uses the terms 'coupling' and 'isolating' in a similar fashion"). The court observed that we had arrived at a different construction of the term "selectively isolating" in IPR883, but found the record was unclear as to which construction of "selectively isolating" we actually had applied in our analysis of the challenges to the '536 patent. *Id.* at 1005–06. The court directed us on remand to construe "selectively isolating" in view of its construction of "selectively electrically coupling," and to reconsider whether the references disclose circuits that are capable of selectively isolating based on our new construction. *See id.* at 1005.

The court's mandate issued on August 31, 2017. Neither party sought to provide additional briefing or requested that we take new evidence upon remand. Here, we determine that no new argument or evidence is necessary because the claim constructions we apply on remand were proposed by Patent Owner (*compare* PO Resp. 13 *and* IPR1011, Paper 26, 50, *with* Section II *infra*) and "the effect thereof has been fully briefed" (Patent Trial and Appeal Board Standard Operating Procedure ("SOP") 9 (Rev. 1)[5], 8). *See Netlist*, 701 F. App'x at 1005 ("Indeed, the parties below raised factual disputes about whether prior art circuits perform selective electrical

[5] SOP 9 addresses the procedure for handling all decisions on cases remanded from the Court of Appeals for the Federal Circuit to the Patent Trial and Appeal Board for further proceedings. SOP 9 currently is available at https://www.uspto.gov/sites/default/files/documents/sop_9_%20procedure_for_decisions_remanded_from_the_federal_circuit.pdf.

Petitioners
Ex. 1040, p. 5

coupling, even under Netlist's construction. . . . But because the Board based its conclusions of obviousness and anticipation on an erroneous construction, the Board must assess these factual issues on remand."). We address the errors identified by the Federal Circuit in view of the record as of December 14, 2015, the date of issuance of the Board's Final Decision. For the reasons that follow, we conclude that Petitioner has shown by a preponderance of the evidence that claims 15–17, 22, 24, 26, and 31–33 of the '150 patent are unpatentable.

B. The '150 Patent

The '150 patent is described in the Final Written Decision. *See* Final Dec. 3–6. A summary description is provided below.

The '150 patent relates to a memory module of a computer system with improved performance and memory capacity. Ex. 1001, 1:30–33. The memory module includes a plurality of memory devices (arranged in ranks), and a circuit electrically coupled to the memory devices. *Id.* at 4:59–63, Fig. 1. The circuit includes a logic element, such as a complex programmable-logic device (CPLD). *Id.* at 6:4–9. In response to a set of input address and command signals from a memory controller, the circuit generates a set of output address and command signals (*id.* at 15:23–31), whereby the circuit selectively isolates the loads of some of the memory devices from the computer system (*id.* at 6:48–50).

Figure 3A, reproduced below, is a schematic diagram of a circuit in accordance with certain embodiments of the invention. *Id.* at 4:14–18.

Petitioners
Ex. 1040, p. 6

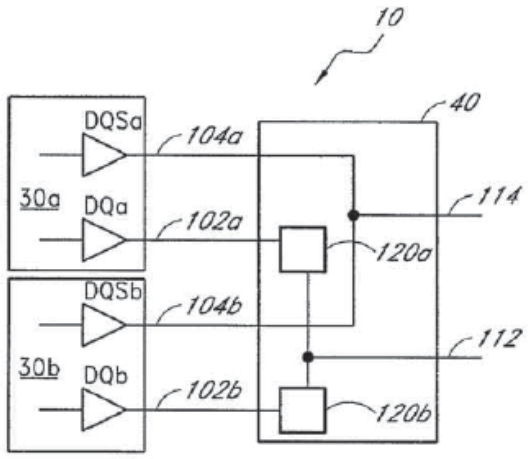


FIG. 3A

As shown in Figure 3A, the logic element of circuit 40 uses switches 120a, 120b to selectively isolate or selectively electrically couple one or both of DQ data signal lines 102a, 102b of memory devices 30a and 30b from common data signal line 112. *Id.* at 3:45–47, 7:2–5, 19–26. By selectively isolating the loads of memory devices that are not being accessed by the memory controller, the capacitive load on the memory controller can be substantially reduced. *Id.* at 7:27–31.

II. CLAIM CONSTRUCTION

"A claim in an unexpired patent that will not expire before a final written decision is issued shall be given its broadest reasonable construction in light of the specification of the patent in which it appears." 37 C.F.R. § 42.100(b). Pursuant to that standard, the claim language should be read in light of the specification, as it would be interpreted by one of ordinary skill in the art. *In re Suitco Surface, Inc.*, 603 F.3d 1255, 1260 (Fed. Cir. 2010). An inventor may provide a meaning for a term that is different from its ordinary meaning by defining the term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480

Petitioners
Ex. 1040, p. 7

(Fed. Cir. 1994). "[W]here multiple patents 'derive from the same parent application and share many common terms, we must interpret the claims consistently across all asserted patents.'" *SightSound Tech., LLC v. Apple Inc.*, 809 F.3d 1307, 1316 (Fed. Cir. 2015) (quoting *NTP, Inc. v. Research in Motion, Ltd.*, 418 F.3d 1282, 1293 (Fed. Cir. 2005)).

In our Final Decision, we construed the terms "selectively electrically coupling," "selectively isolating," and "circuit configured to be mounted on a memory module." *See* Final Dec. 8–15. The Federal Circuit agreed with our construction of "circuit configured to be mounted on a memory module," but determined we erred in our constructions of "selectively electrically coupling" and "selectively isolating." *See Netlist*, 701 F. App'x at 1004–05.

"Selectively electrically coupling" is recited in each of challenged independent claims 15 and 31 as follows:

> A circuit configured to be mounted on a memory module so as to be electrically coupled to a first double-data-rate (DDR) memory device having a first data signal line and a first data strobe line, to a second DDR memory device having a second data signal line and a second data strobe line, and to a common data signal line . . . wherein the circuit is configurable to be responsive to the set of input signals [comprising row address signals, column address signals, bank address signals, and chip-select signals] by *selectively electrically coupling* the first data signal line to the common data signal line and *selectively electrically coupling* the second data signal line to the common data signal line.

Ex. 1001, 42:41–46, 48–50, 58–62, 44:29–34, 36–38, 46–50 (emphasis added). The Federal Circuit determined the broadest reasonable construction of this term is "coupling in response to a selection." *Netlist*,

Petitioners
Ex. 1040, p. 8

701 F. App'x at 1004. As instructed by the court, below we construe the term "selectively isolating" in view of the court's construction of "selectively electrically coupling." *See id.* at 1005–06.

"Selectively isolating" is recited in challenged '150 patent claims 22 and 26 as follows:

> 22. A circuit configured to be mounted on a memory module so as to be electrically coupled to a plurality of . . . [DDR] memory devices arranged in one or more ranks on the memory module . . . wherein the circuit is configurable to be responsive to the set of input signals [comprising row address signals, column address signals, bank address signals and chip-select signals] by *selectively isolating* one or more loads of the DDR memory devices from the computer system.

Ex. 1001, 43:35–38, 40–42, 51–54 (emphasis added).

> 26. The circuit of claim 22, further configurable to *selectively isolate a data signal line* of a DDR memory device of the plurality of DDR memory devices from the computer system.

Id. at 44:8–11 (emphasis added).

As noted above, in the present *inter partes* review, neither Petitioner nor Patent Owner proposed an explicit construction of "selectively isolating." *See* Pet. 8–11; PO Resp. 5–16. In its patent owner response in IPR1011, Patent Owner implicitly construed the term "selectively isolating" as "isolating in response to a selection." *See* IPR1011, Paper 26, 50. As also indicated above, the '536 patent is a continuation of the application that issued as the '150 patent and, therefore, the two patents share the same written description. *See Netlist*, 701 F. App'x at 1003. In IPR883, involving the related '536 patent and claims reciting the term "selectively isolating," Patent Owner explicitly proposed construing this term as "isolating in

Petitioners
Ex. 1040, p. 9

response to a selection." IPR883, Paper 8, 14–15. In support of this construction, Patent Owner cited disclosure in the '536 patent that corresponds to column 6, line 63 through column 8, line 20 of the '150 patent. *See* IPR883, Paper 8, 14–15; *compare* Ex. 1001, 6:63–8:20, *with* IPR883, Ex. 1001, 7:32–8:56. The referenced disclosure describes, with reference to Figures 3A, 3B, that by selectively isolating DQ data signal line 102a of memory device 30a from common DQ data signal line 112, which is coupled to the computer system, circuit 40 "selectively allows" (1) a DQ data signal to be transmitted from the memory controller of the computer system to DQ data signal line 102b of memory device 30b, and (2) a DQ data signal from DQ data signal line 102b of memory device 30b to be transmitted to the memory controller via common DQ data signal line 112 (*see* Ex. 1001, 6:63–7:12). The '150 patent explains that by selectively isolating DQ data signal line 102a and DQS data strobe signal line 104a of memory device 30a (i.e., the memory device that is not being accessed by the computer system) from the common data signal and data strobe signal lines 112, 114 to the memory controller, the load from memory device 30a is isolated from the memory controller, thereby reducing the capacitive load on the memory controller. *Id.* at 6:40–47, 58–62. The '150 patent describes DQ data signal line 102b (i.e., the data signal line to the memory device that is being accessed by the computer system) as "selectively electrically couple[d]" to common DQ signal line 112. *See id.* at 7:19–33.

In construing the claim term "selectively electrically coupling," the Federal Circuit determined that this term "is directed to *how* the circuit performs th[e] function [of activating some memory devices and not others], which is by coupling or decoupling specific data signal lines." *Netlist*, 701

Petitioners
Ex. 1040, p. 10

F. App'x at 1005. Noting that "the claims call out exactly which two data lines must be coupled," the court determined that our construction of "selectively electrically coupling" as "making a selection between at least two components so as to transfer power or signal information from one selected component to at least the other selected component," was unreasonable. *Id.* at 1004–05. The court explained that "the 'selection' is to couple or uncouple the first/second data signal line to the common signal line, not to select among multiple components." *Id.* at 1005.

The above cited disclosure in the '150 patent similarly is directed to how the circuit performs the function of reducing the load to the computer system, which is by isolating the load of specific memory devices from the memory controller, and to how the circuit performs the function of preventing data transmission between a specific memory device and the computer system, which is by isolating specific data signal lines from the common signal line.

In its arguments in support of patentability in IPR1011, Patent Owner asserts that the term "selectively isolating" requires electrical separation. IPR1011, Paper 26, 23. Patent Owner's expert, Dr. Carl Sechen, testified that in a system in which the chip select signal lines and the data bus lines are permanently hard-wired via an electrical conduit to the memory devices, load isolation is not possible without switches on these lines to enable electrical decoupling. Ex. 2002 (Declaration of Dr. Carl Sechen) ¶ 81; *see also* Ex. 1022 (Transcript of Dr. Carl Sechen's deposition), 133:6–14.

We are not persuaded that the broadest reasonable construction of "selectively isolating" requires electrical separation. The '150 patent discloses that:

Petitioners
Ex. 1040, p. 11

> As used herein, the term "load" is a broad term which includes, without limitation, electrical load, such as capacitive load, inductive load, or impedance load. As used herein, *the term "isolation" is a broad term which includes, without limitation, electrical separation* of one or more components from another component or from one another.

Ex. 1001, 5:3–8 (emphasis added). Patent Owner has not identified, nor do we find, any disclosure in the '150 patent that supports a broadest reasonable construction of the claim term "selectively isolating" as requiring electrical separation. To the contrary, use of the term "electrically" throughout the '150 patent to specify how the data signal lines are selectively coupled, suggests that the inventors did not intend to limit how the data signal lines are selectively isolated or the type of loads that are selectively isolated. *See, e.g.*, Ex. 1001, 8:48–52 ("In certain embodiments, the load isolation provided by the circuit 40 advantageously allows the memory module 10 to present a reduced load (*e.g.*, *electrical load*, such as capacitive load, inductive load, or impedance load) to the computer system." (emphasis added)); *id.* at 9:12–14 ("In certain embodiments, load isolation advantageously provides system memory with reduced electrical loading."); *cf.* Ex. 2002 ¶¶ 67–68 ("[T]he claim term 'selectively electrically coupling' is more specific than just a generic 'coupling.'. . . [T]he added word 'electrically' specifies an electrical aspect to 'coupling' to [one of ordinary skill in the art]."). Because we are not persuaded that the claim term "selectively isolating" requires electrical separation, we also decline to construe this term as requiring a switch or other specific component that would enable electrical decoupling. *See Netlist*, 701 F. App'x at 1005 ("To be clear, we do not limit 'selectively electrically coupling' to a switch or

Petitioners
Ex. 1040, p. 12

other specific component. Nor do we hold that 'selectively electrically coupling' necessarily precludes a hard-wired connection.").

Accordingly, consistent with the Federal Circuit's determination that the broadest reasonable construction of "selectively electrically coupling" is "coupling in response to a selection" (*id.* at 1004), we determine the broadest reasonable construction of the claim term "selectively isolating" is "isolating in response to a selection."[6]

III. ANALYSIS

To prevail in its patentability challenges, a petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). In its decision, the Federal Circuit found that we applied erroneous constructions of "selectively electrically coupling" and "selectively isolating" in determining Petitioner had met its burden to prove unpatentability. *See Netlist*, 701 F. App'x at 1004–05. Following the court's directive in its construction of the claim term "selectively electrically coupling" as "coupling in response to a selection," in this decision, we construe "selectively isolating" as "isolating in response to a selection." *See* Section II *supra*. As instructed by the court, we apply these constructions in reconsidering whether Petitioner has met its burden to show that the combination of Amidi and Klein and the combination of Amidi and Wiggers disclose "selectively isolating" and "selectively electrically coupling." *See Netlist*, 701 F. App'x at 1005–06. The court did not identify any other error in our findings and, therefore, we

[6] We apply the same construction of this term in our decisions on remand in IPR883 and IPR1011.

Petitioners
Ex. 1040, p. 13

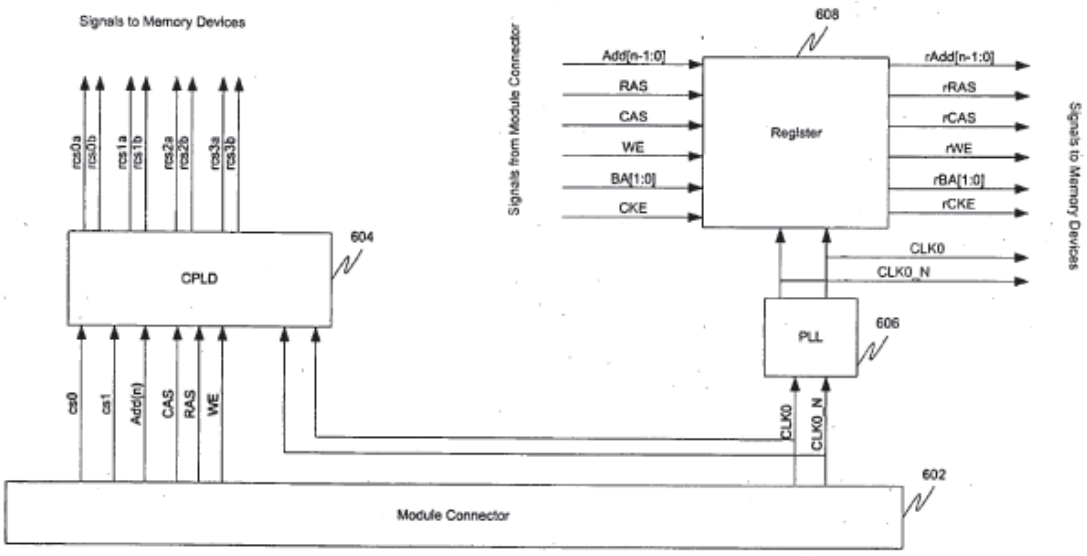
do not revisit our determinations that the combination of Amidi and Klein and the combination of Amidi and Wiggers disclose or suggest all other limitations of challenged claims 15–17, 22, 24, 26, and 31–33, and that one of ordinary skill in the art would have had a reason to combine these references and a reasonable expectation of success in so doing. *See generally*, Final Dec. 23–35, 39–50.

A. The Prior Art

The prior art is described in the Final Decision. *See* Final Dec. 19–23, 35–38. Below we provide summary descriptions.

1. Amidi (Ex. 1008)

Amidi discloses a transparent four rank memory module for use in a standard two rank sub-system. Ex. 1008, Title. As illustrated in Figure 6A, reproduced below, Amidi's memory module includes complex programmable logic device ("CPLD") 604, phase-lock loop ("PLL") 606, and register 608. *Id.* ¶¶ 28, 50.



Row Address Decoding
FIG.6A

Figure 6A is a block diagram schematically illustrating a row address decoding system for a transparent four rank memory module in accordance with an embodiment of Amidi's invention. *Id.* ¶ 21. Module connector 602 sends signals from a memory controller (not shown) to CPLD 604, PLL 606, and register 608. *Id.* ¶¶ 38, 50. The signals sent to CPLD 604 include chip select, row address, and column address signals. *Id.* ¶¶ 41, 50. CPLD 604 includes internal decoding circuitry for determining which rank from the four ranks of memory devices to activate based upon the address and command signals from the memory controller. *See id.* ¶¶ 41, 43, 57, 61. CPLD 604 generates and relays the command signals to activate a rank of memory devices. *Id.* ¶ 62.

2. Klein (Ex. 1009)

Klein discloses a method for reducing data bus capacitance "by decoupling unaccessed memory circuits from a data bus during data transfers to or from other memory circuits." Ex. 1009, Abstract. An embodiment of Klein's method is described in connection with Figure 6, reproduced below.

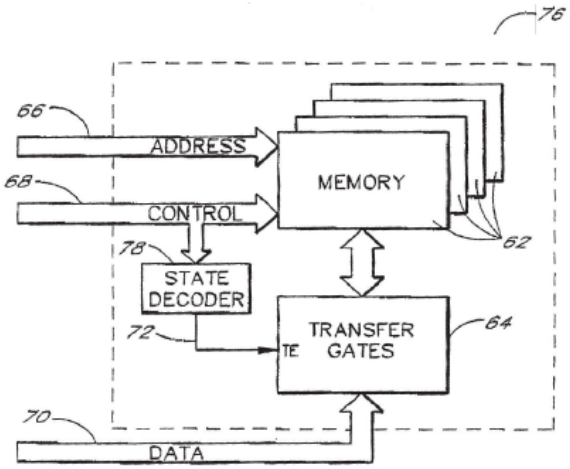


FIG. 6

Petitioners
Ex. 1040, p. 15

Figure 6 is a block diagram illustrating memory module 76. *Id.* ¶¶ 16, 35. Memory module 76 includes memory elements 62, transfer gates 64, and electrical contacts for interfacing with address bus 66, control lines 68, and data bus 70. *Id.* ¶ 35. Memory module 76 further includes state decoder 78 for receiving one or more control signals from the host system. *Id.* "[S]tate decoder 78 decodes the signals on the control lines to determine whether or not a memory access to or from the module is being made, and asserts the gate control signal 72 to open the transfer gates 64 when a memory access is being made." *Id.* Klein discloses that state decoder 78 may be an inverter which has chip select signal 82 as an input. *Id.* ¶ 36. Klein discloses that transfer gates 64 may be constructed as described in Figure 2 (*id.* ¶ 32), which shows a bus switch comprising one or more n-channel MOSFET transistors with commonly connected gates 15, an input portion and an output portion for connection to one or more lines of a bus (*id.* ¶ 25). The transistors are turned on by asserting the gates via an input transfer enable ("TE") signal line. *Id.* ¶ 26. "The switch . . . therefore decouples or isolates the bus segments when the transistors comprising the switch are in the off state, and couples or connects the bus segments when the transistors comprising the switch are in the on state." *Id.*

Klein Figure 4 is reproduced below.

Petitioners
Ex. 1040, p. 16

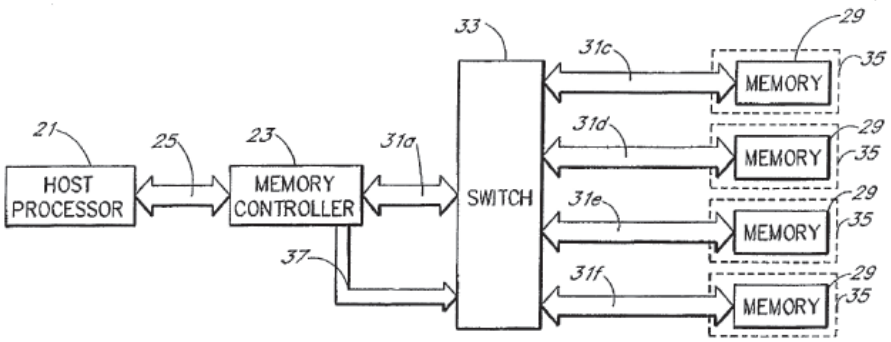


FIG. 4

Figure 4 is a block diagram of a computing system comprising host processor 21 that interfaces with memory controller 23 via bus 25. *Id.* ¶¶ 14, 29. Bus switch 33 splits single input data bus 31a from memory controller 23 into a plurality of output data buses 31c, 31d, 31e, 31f, which are routed to respective memory modules 35 having memory devices 29 mounted thereon. *Id.* ¶ 29. Klein discloses that bus switch 33 comprises a plurality of the Figure 2 switches, each having an input side commonly connected to input data bus 31a, and an output side separately routed to a respective one of output data buses 31c, 31d, 31e, and 3lf. *Id.* ¶ 29. "Therefore, selectively asserting the corresponding four TE [(transfer enable)] signal inputs would selectively couple the input data bus 31*a* to one of the output buses 31*c*, 31*d*, 31*e*, or 31*f*." *Id.* Klein further discloses that

> the memory controller 23 may include a control output 37 which controls the bus switch [33] . . . so as to connect the input data bus 31*a* to one of the output buses 31*c*, 31*d*, 31*e*, and 31*f* while the remaining three output buses remain disconnected from the input bus. . . . [D]uring memory accesses, the memory controller 23 will therefore only need to drive one bus and memory module rather than all of them during each memory access.

Id. ¶ 30.

Petitioners
Ex. 1040, p. 17

Klein discloses that bus switch 33 in the Figure 4 embodiment includes interface circuitry 26, as described in connection with Figure 3, reproduced below. *Id.* ¶ 29.

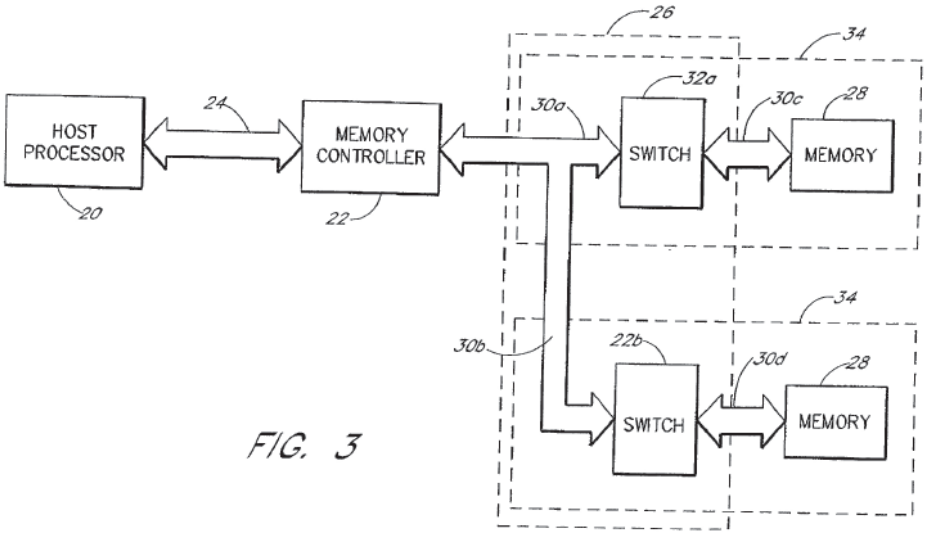


FIG. 3

Figure 3 is a block diagram of a computing system including host processor 20 that interfaces with memory controller 22 which, in turn, connects to circuitry 26 for interfacing with one or more memory elements 28 on memory module 34. *Id.* ¶¶ 13, 27–29. Circuitry 26 includes data bus 30*a*–*d* for transferring data between memory elements 28 and memory controller 22. *Id.*

> [T]he data bus between the memory controller 22 and memory elements 28 may comprise several branches 30*a*, 30*b*, one for each of the separate memory elements 28. Each branch may include a switch 32*a*, 32*b* that . . . may be used to selectively isolate portions or segments 30*c*, 30*d* of the data bus running from the memory controller to the memory circuitry 28.

Id. at 28.

> [B]y turning the switches 32*a* and 32*b* on or off, one or the other memory . . . [device] 28 may be removed from the data bus. For example, when the host processor requires data in the memory . . . [device] 28 connected to bus segment 30*c*, switch

> 32*a* may be switched on, while switch 32*b* may be switched off. Thus, the design of FIG. 3 may reduce the parasitic capacitance that the memory controller needs to charge and discharge during data transfers because a portion of the data bus and the stray capacitance of unaccessed memory circuits are removed.

Id.

3. Wiggers (Ex. 1010)

Wiggers relates to a memory system for minimizing the capacitive load of a memory data bus. Ex. 1010, Abstract. A preferred embodiment of Wiggers's memory system is shown in Figure 3, reproduced below. *Id.* at 4:44–45.

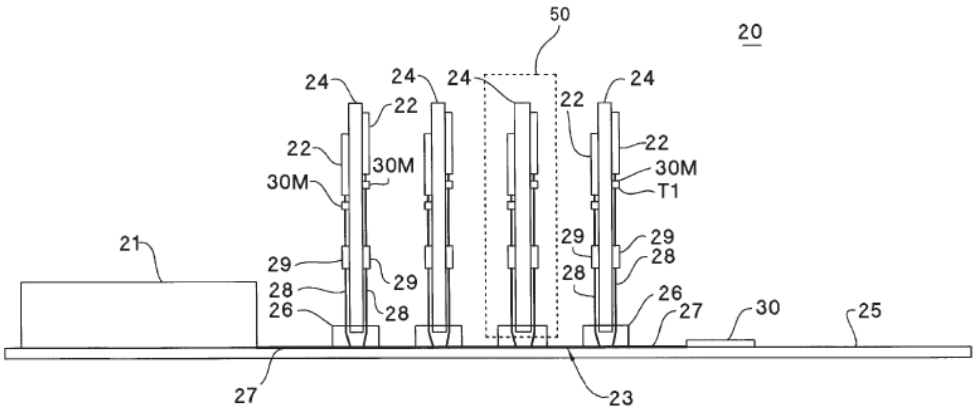


Figure 3

Wiggers Figure 3 is a side view of memory system 20, which includes memory controller 21 electrically connected to data bus 23. *Id.* at 4:13–14, 45–47. Memory controller 21 "selectively accesses numerous memory devices 22 which are arranged either serially, in parallel, or in some combination of the two along the data bus 23." *Id.* at 4:48–50.

> The memory controller can also selectively electrically couple and decouple each of the memory devices from the data bus, either individually or in small groups using a number of switches 29, preferably including field effect transistor (FET)

> type switches. In addition to being electrically connected to the data bus, each of these switches is electrically connected to the controller via a control line (not shown . . .).

Id. at 4:53–60.

B. *Alleged Obviousness of Claims 15–17, 22, 24, 26, and 31–33 in view of Amidi and Klein*

Independent claims 15 and 31 recite:

> wherein the circuit is configurable to be responsive to the set of input signals [comprising row address signals, column address signals, bank address signals and chip-select signals] by *selectively electrically coupling* the first data signal line to the common data signal line and *selectively electrically coupling* the second data signal line to the common data signal line.

Ex. 1001, 42:48–50, 58–62, 44:36–38, 46–50 (emphasis added). Independent claim 22 recites: "wherein the circuit is configurable to be responsive to the set of input signals [comprising row address signals, column address signals, bank address signals and chip-select signals] by *selectively isolating one or more loads* of the DDR memory devices from the computer system." Ex. 1001, 43:40–42, 51–54 (emphasis added). Claim 26 recites: "The circuit of claim 22, further configurable to *selectively isolate a data signal line* of a DDR memory device of the plurality of DDR memory devices from the computer system." *Id.* at 44:8–11 (emphasis added).

Petitioner contends Amidi discloses a memory module comprising four ranks of memory devices, and a circuit including a CPLD. Pet. 25. Petitioner asserts that each stack of DDR memory devices has a data signal line and a data strobe line, and "at least two DDR memory devices are connected to the same (common) memory bus ('common data signal line')."

Petitioners
Ex. 1040, p. 20

Id. at 27 (citing Ex. 1008 ¶¶ 34, 35, Fig. 3). Petitioner contends Amidi's circuit is responsive to input signals, including row address, column address, bank address, and chip-select signals. *See id.* at 30 (citing Ex. 1008 ¶ 50, Fig. 6A). In particular, Petitioner asserts that in response to chip select signals cs0, cs1 and address signal Add(n) from a memory controller, Amidi's CPLD generates signals to activate a selected one of the four ranks of memory devices, while inactivating (selectively isolating) the other three ranks from the data bus, thereby enabling the activated rank to read from or write data to the system bus. *Id.* at 33 (citing Ex. 1008 ¶¶ 43, 44, 62), 35.

Petitioner contends Klein discloses memory module 76 having mounted thereon state decoder 78 and a plurality of DDR memory devices 62. Pet. 34–35 (citing Ex. 1009 ¶ 35, Fig. 6). Petitioner asserts that in response to a set of input signals, e.g., a chip select signal, state decoder 78 generates gate control TE signals 78 (*id.* at 34–35 (citing Ex. 1009 ¶ 36)); the gate control TE signals drive the switches used for coupling and isolation (Ex. 1007 ¶ 87). Petitioner contends that in response to the input signals, switch 33 may "selectively couple[] one of the output data buses 31c, 31d, 31e, 31f ('the first data signal line' and 'second data signal line') to the input data bus 31a ('the common data signal line')." Pet. 34 (citing Ex. 1009 ¶ 29). Similarly, Petitioner contends that in response to input signals, bus switches 32a, 32b disconnect ("selectively isolating") one of two output data buses 30c, 30d ("one or more loads of the DDR memory devices") from input data bus 30a. *Id.* at 36; Reply 16–17. Petitioner asserts that one of ordinary skill in the art would have understood that the chip-select signals generated by Amidi's CPLD may be provided to the transfer gates associated with the memory devices of Klein, and would have applied the

switch control circuitry in Klein to the circuit of Amidi to improve the performance of Amidi's memory chip. Pet. 29, 35 (citing Ex. 1007 ¶¶ 89, 91).

Patent Owner contends Amidi's data lines are never in a decoupled state that would allow them to be subject to acts of "selectively electrically coupling," because the data lines of its four ranks are hard-wired in permanent coupling to the same 72-line data bus. PO Resp. 30. Patent Owner does not raise a similar argument with respect to the claim limitation "selectively isolating," although Dr. Sechen testified that the hard-wiring in Amidi would prevent the signal lines of Amidi from being subject to an act of selectively isolating. Ex. 2002 ¶ 81.

Having considered the parties' respective arguments and evidence cited in support thereof, we find Petitioner has met its burden to show that the combination of Amidi and Klein discloses "selectively electrically coupling" as recited in claims 15 and 31 and "selectively isolating" as recited in claims 22 and 26.

We find that Amidi discloses a circuit that, in response to a signal selecting a rank of memory devices, enables the selected rank to read and write data to a system bus while disabling non-selected ranks from reading and writing data to the system bus. Ex. 1008 ¶¶ 43, 44, 62. Dr. Sechen acknowledged that adding switches on Amidi's chip select signal lines or data bus lines would enable decoupling of the data bus lines from the memory controller to the memory devices. *See* Ex. 2002 ¶ 80; *see also* PO Resp. 15 (noting that the '150 patent discloses selectively actuating a switch to perform an act of "selectively electrically coupling"). Dr. Sechen also testified that Klein's MOSFET switches (i.e., data bus switches) are capable

Petitioners
Ex. 1040, p. 22

of decoupling a memory device from a data bus. *See* Ex. 1022, 49:16–50:18, 88:5–22; *see also* Ex. 1001, 8:34–36 ("Example switches compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches . . . ."), 10:15–16 (Example 1 circuit "comprising six FET switches for providing load isolation to DQ and DQS lines").

We credit Dr. Jagannathan's testimony that one of ordinary skill in the art would have "implement[ed] the bus switch of Klein into the architecture of Amidi" (Ex. 1007 ¶ 91) to "provide[] the benefit of incorporating more functionality in a smaller space, thereby providing more space on the memory module for additional memory devices" (*id.* ¶ 89) and to "provide the benefits of load isolation of data buses and reduction in parasitic capacitance on the data buses" (*id.* ¶ 91). We further credit Dr. Jagannathan's testimony that modifying Amidi in this manner "would have been routine for one of ordinary skill in the art." *Id.* We find Klein discloses that *in response to a* host system's *selection* of memory elements to access, the *switches* associated with the selected (e.g., first and second) memory elements *electrically couple* the respective (e.g., *first and second*) *data signal lines* to the selected memory elements *to the common data signal line* to the system processor. Ex. 1009 ¶¶ 22, 28, 29. We further find Klein discloses that *in response to the selection* of memory elements for access by the host system, *a switch* associated with a non-selected memory element *isolates* that memory element (i.e., *the load*) from the system data bus *by electrically disconnecting the data signal line* to the non-selected memory element *from the common data signal line* to the system processor, thereby reducing parasitic capacitance of the data bus and allowing increases in the

Petitioners
Ex. 1040, p. 23

speed of data transfer. *Id.* ¶ 22.

In sum, we are satisfied that the combination of Amidi and Klein discloses "selectively electrically coupling" under the Federal Circuit's construction of this term as "coupling in response to a selection." We are also satisfied that this combination discloses "selectively isolating" under our construction of this term as "isolating in response to a selection."

C. Alleged Obviousness of Claims 15–17, 22, 24, 26, and 31–33 in view of Amidi and Wiggers

Petitioner's contentions with respect to the teachings of Amidi are discussed in Section III.B, above. *See* Pet. 44–53.

Petitioner contends Wiggers discloses memory module 24 having mounted thereon memory devices 22 and switches 29 (a circuit) that include field effect transistor (FET) type switches (a logic element). Pet. 44 (citing Ex. 1010, 4:47–57, 61–65; Ex. 1007 ¶ 93). Petitioner contends "Wiggers discloses that the memory module receives a set of input signals from the memory controller including address bus connections ('row address signals, column address signals') and switch control line connections ('chip-select signals')." *Id.* at 47–48 (citing Ex. 1010, 4:65–5:6). Petitioner contends "Wiggers discloses that switches 29 ('the circuit') selectively electrically couple . . . individual memory devices ('first data signal line' and 'second data signal line') from the data bus ('common data signal line')." *Id.* at 49 (citing Ex. 1010, 4:53–57). Petitioner also contends "Wiggers discloses that the switches ('the circuit') selectively electrically . . . decouples ('selectively isolating') each of the memory devices ('one or more loads of the DDR memory devices') from the data bus ('computer system')." *Id.* at 50–51 (citing Ex. 1010, 4:53–57); *see also id.* at 51 (citing Ex. 1010, 5:62–66); *id.*

at 55–56 (citing Ex. 1010, 5:52–56). Petitioner contends a person of ordinary skill in the art would have "appl[ied] the switch disclosed in Wiggers to the CPLD in Amidi . . . to reduce the capacitance load of a memory data bus and increase the speed of data propagation." Pet. 56 (citing Ex. 1007 ¶ 96).

Patent Owner advances arguments similar to those made in support of patentability of the challenged claims over the Amidi-Klein combination. *Compare* PO Resp. 47–55, *with id.* at 35–44. Having considered the parties' respective arguments and evidence cited in support thereof, we find Petitioner has met its burden to show that the combination of Amidi and Wiggers discloses "selectively electrically coupling" as recited in claims 15 and 31 and "selectively isolating" as recited in claims 22 and 26.

Our findings with respect to Amidi in Section III.B, above, likewise apply to our analysis of the present challenge. We find that Wiggers, like the '150 patent, discloses the use of FET type switches for electrically coupling and decoupling data signal lines. *Compare* Ex. 1010, 4:53–57, *with* Ex. 1001, 8:34–36. We credit Dr. Jagannathan's testimony that one of ordinary skill in the art would have "appl[ied] the switch taught by Wiggers to the memory module of Amidi because the switch of Wiggers increases the speed of data propagation" (Ex. 1007 ¶ 96). We further credit Dr. Jagannathan's testimony that "implementing the switch of Wiggers into the architecture of Amidi would have been routine for one of ordinary skill in the art" (*id.*).

We find Wiggers discloses that *in response to a selection* of memory devices for communication with a host system, the *switches* associated with the selected (e.g., first and second) memory devices are used to *electrically*

Petitioners
Ex. 1040, p. 25

couple the respective (e.g., *first and second*) *data signal lines* to the selected memory devices *to the common data signal line* to the system processor. *See* Ex. 1010, 4:53–57; 6:5–8. We find Wiggers further discloses that *in response to the selection* of memory devices for communication with the host system, *a switch* associated with a non-selected memory device *isolates* that memory device (i.e., *the load*) from the system data bus *by electrically decoupling the data signal line* to the non-selected memory device *from the common data signal line* to the system processor, such that the capacitive load of the non-selected memory devices no longer contributes to the overall capacitive load on the data bus and data propagation between the memory controller and selected memory devices will become faster. *See id.* at 5:52–6:11.

In sum, we are satisfied that the combination of Amidi and Wiggers discloses "selectively electrically coupling" under the Federal Circuit's construction of this term as "coupling in response to a selection." We are also satisfied that this combination discloses "selectively isolating" under our construction of this term as "isolating in response to a selection."

IV. CONCLUSION

Having reconsidered the parties' respective arguments and evidence cited in support thereof in light of our construction of "selectively isolating" as "isolating in response to a selection," and in light of the court's construction of "selectively electrically coupling" as "coupling in response to a selection," we are persuaded that the combination of Amidi and Klein and the combination of Amidi and Wiggers disclose a circuit "configurable to be responsive to the set of input signals [comprising row address signals,

Petitioners
Ex. 1040, p. 26

column address signals, bank address signals and chip-select signals] by selectively isolating one or more loads of the DDR memory devices from the computer system," as recited in claim 22, and "further configurable to selectively isolate a data signal line of a DDR memory device of the plurality of DDR memory devices from the computer system," as recited in claim 26. We are also persuaded that modifying Amidi to include Klein's switch control circuitry and modifying Amidi to include Wiggers's switch circuitry would have resulted in a circuits "configurable to be responsive to the set of input signals [comprising row address signals, column address signals, bank address signals and chip-select signals] by selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line," as recited in claims 15 and 31. Accordingly, given the Federal Circuit's directive, because we find the asserted prior art discloses or suggests these limitations, we determine that '150 patent claims 15–17, 22, 24, 26, and 31–33 are unpatentable.

V. ORDER

Accordingly, it is

ORDERED that claims 15–17, 22, 24, 26, and 31–33 of U.S. Patent 7,881,150 B2 are unpatentable; and

FURTHER ORDERED that this is a final written decision under 35 U.S.C. § 318(a). Parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

Petitioners
Ex. 1040, p. 27

For PETITIONER:

Fabio E. Marino
Barrington Dyer
McDermott Will & Emery LLP
fmarino@mwe.com
bdyer@mwe.com

For PATENT OWNER:

Mehran Arjomand
David S. Kim
Erol C. Bsol
Jean Nguyen
Jonathan Z. Statman
Morrison & Foester LLP
63516-150-IPR1@mofo.com