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(54) **MEMORY MODULE WITH DATA BUFFERING**

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(56) **References Cited**

U.S. PATENT DOCUMENTS

4,218,740 A 8/1980 Bennett et al.
4,249,253 A 2/1981 Gentili et al.
(Continued)

FOREIGN PATENT DOCUMENTS

EP 1 816 570 A2 8/2007
JP 2009-237492 9/1997
(Continued)

OTHER PUBLICATIONS

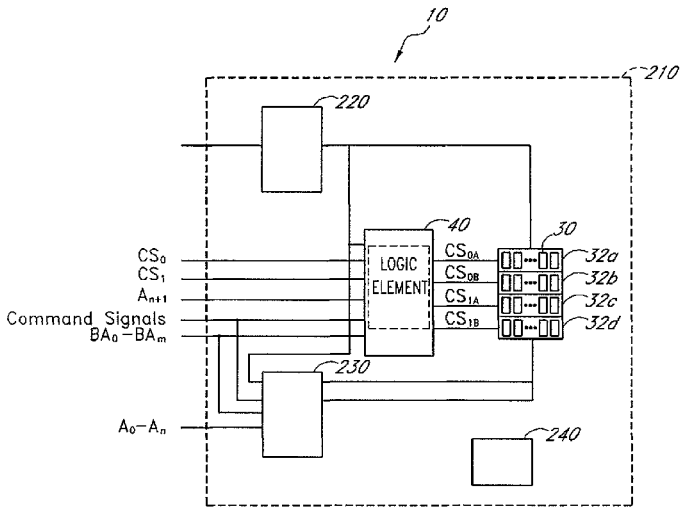
US 6,832,284 B1, 12/2004, Perego et al. (withdrawn)
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(57) **ABSTRACT**

A memory module operable to communicate data with a memory controller via a data bus comprises a plurality of memory integrated circuits including first memory integrated circuits and second memory integrated circuits, a data buffer coupled between the first memory integrated circuits and the data bus, and between the second memory integrated circuits and the data bus, and logic coupled to the data buffer. The logic is configured to respond to a first memory command by providing first control signals to the data buffer to enable communication of at least one first data signal between the first memory integrated circuits and the memory controller through the data buffer, and is further configured to respond to a second memory command by providing second control signals to the data buffer to enable communication of at least one second data signal between the second memory integrated circuit and the memory controller through the data buffer.

33 Claims, 23 Drawing Sheets



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(56) **References Cited**

U.S. PATENT DOCUMENTS

4,368,515	A	1/1983	Nielsen
4,392,212	A	7/1983	Miyasaka et al.
4,571,676	A	2/1986	Mantellina et al.
4,592,011	A	5/1986	Mantellina et al.
4,633,429	A	12/1986	Lewandowski et al.
4,670,748	A	6/1987	Williams
4,706,214	A	11/1987	Kassai
4,739,473	A	4/1988	Ng
4,866,603	A	9/1989	Chiba
4,958,322	A	9/1990	Kosugi et al.
4,961,172	A	10/1990	Shubat et al.
4,961,204	A	10/1990	Tanaka et al.
4,980,850	A	12/1990	Morgan
5,060,188	A	10/1991	Zulian et al.
5,247,643	A	9/1993	Shottan
5,272,664	A	12/1993	Alexander et al.
5,313,624	A	5/1994	Harriman
5,345,412	A	9/1994	Shiratsuchi
5,357,478	A	10/1994	Kikuda et al.
5,388,072	A	2/1995	Matick et al.
5,388,240	A	2/1995	Olderdissen et al.
5,392,252	A	2/1995	Rimpo et al.
5,426,753	A	6/1995	Moon
5,463,590	A	10/1995	Watanabe
5,483,497	A	1/1996	Mochizuki et al.
5,485,589	A	1/1996	Kocis et al.
5,495,435	A	2/1996	Sugahara
5,513,135	A	4/1996	Dell et al.
5,532,954	A	7/1996	Bechtolsheim et al.
5,537,584	A	7/1996	Miyai et al.
5,541,448	A	7/1996	Carpenter
5,559,970	A	9/1996	Sharma
5,572,691	A	11/1996	Koudmani
5,581,498	A	12/1996	Ludwig et al.
5,590,071	A	12/1996	Kolor et al.
5,602,999	A	2/1997	Hyatt
5,617,559	A	4/1997	Le et al.
5,630,096	A	5/1997	Zuravleff
5,638,534	A	6/1997	Mote, Jr.
5,649,159	A	7/1997	Le et al.
5,655,153	A	8/1997	Sandorfi
5,699,542	A	12/1997	Mehta et al.
5,702,984	A	12/1997	Bertin et al.
5,703,826	A	12/1997	Hush et al.
5,717,851	A	2/1998	Yishay et al.
5,724,604	A	3/1998	Moyer
5,745,914	A	4/1998	Connolly et al.
5,729,716	A	5/1998	Lee et al.
5,764,590	A	6/1998	Iwamoto et al.
5,784,705	A	7/1998	Leung
5,802,395	A	9/1998	Connolly et al.
5,802,541	A	9/1998	Reed
5,805,520	A	9/1998	Anglada et al.
5,822,251	A	10/1998	Bruce et al.
5,905,401	A	5/1999	Sher
RE36,229	E	6/1999	Cady
5,909,388	A	6/1999	Mueller
5,926,827	A	7/1999	Dell et al.
5,926,839	A	7/1999	Katayama
5,953,215	A	9/1999	Karabatsos
5,953,280	A	9/1999	Watsui
5,958,025	A	9/1999	Sonobe
5,959,930	A	9/1999	Sakurai
5,963,464	A	10/1999	Dell et al.
5,966,736	A	10/1999	Gittinger et al.
5,973,392	A	10/1999	Senba et al.
5,974,493	A	10/1999	Okumura et al.
6,011,710	A	1/2000	Wiggers
6,018,787	A	1/2000	Ip
6,044,032	A	3/2000	Li
6,061,754	A	5/2000	Cepulis
6,070,217	A	5/2000	Connolly et al.
6,070,227	A	5/2000	Rokicki
6,097,652	A	8/2000	Roh
6,108,745	A	8/2000	Gupta et al.
6,115,278	A	9/2000	Deneroff et al.
6,134,638	A	10/2000	Olarig et al.
6,141,245	A	10/2000	Bertin
6,151,271	A	11/2000	Lee
6,154,418	A	11/2000	Li
6,154,419	A	11/2000	Shakkarwar
6,173,357	B1	1/2001	Ju
6,185,654	B1	2/2001	Van Doren
6,188,641	B1	2/2001	Uchida
6,205,516	B1	3/2001	Usami
6,209,074	B1	3/2001	Dell et al.
6,223,650	B1	5/2001	Johnson
6,226,709	B1	5/2001	Goodwin et al.
6,226,736	B1	5/2001	Niot
6,233,650	B1	5/2001	Johnson et al.
6,247,088	B1	6/2001	Seo et al.
6,260,127	B1	7/2001	Olarig et al.
6,262,938	B1	7/2001	Lee
6,317,352	B1	11/2001	Halbert et al.
6,349,051	B1	2/2002	Klein
6,381,140	B1	4/2002	Liao
6,400,637	B1	6/2002	Akamatsu et al.
6,408,356	B1	6/2002	Dell
6,414,868	B1	7/2002	Wong et al.
6,415,374	B1	7/2002	Faue et al.
6,438,062	B1	8/2002	Karabatsos
6,446,158	B1	9/2002	Karabatsos
6,446,184	B2	9/2002	Dell et al.
6,453,381	B1	9/2002	Yuan et al.
6,470,417	B1	10/2002	Kolor et al.
6,480,439	B2	11/2002	Tokutome et al.
6,487,102	B1	11/2002	Halbert et al.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,502,161 B1 12/2002 Perego et al.
6,518,794 B2 2/2003 Coteus et al.
6,526,473 B1 2/2003 Kim
6,530,007 B2 3/2003 Olarig et al.
6,530,033 B1 3/2003 Raynham et al.
6,546,476 B1 4/2003 Gillingham
6,553,449 B1 4/2003 Dodd et al.
6,553,450 B1 4/2003 Dodd et al.
6,618,320 B2 9/2003 Hasegawa et al.
6,618,791 B1 9/2003 Dodd et al.
6,621,496 B1 9/2003 Ryan
6,625,081 B2 9/2003 Roohparvar et al.
6,625,687 B1 9/2003 Halbert et al.
6,636,446 B2 10/2003 Lee
6,636,935 B1 10/2003 Ware et al.
6,646,949 B1 11/2003 Ellis et al.
6,658,509 B1 12/2003 Boneila et al.
6,674,684 B1 1/2004 Shen
6,681,301 B1 1/2004 Mehta et al.
6,683,372 B1 1/2004 Wong et al.
6,697,888 B1 2/2004 Halbert et al.
6,704,910 B2 3/2004 Hong
6,705,877 B1 3/2004 Li et al.
6,717,855 B2 4/2004 Underwood
6,717,885 B2 4/2004 Lai
6,721,843 B1 4/2004 Estakhri
6,721,860 B2 4/2004 Klein
6,738,880 B2 5/2004 Lai et al.
6,742,098 B1 5/2004 Halbert et al.
6,747,887 B2 6/2004 Halbert et al.
6,754,797 B2 6/2004 Wu et al.
6,785,189 B2 8/2004 Jacobs et al.
6,788,592 B2 9/2004 Nakata et al.
6,807,125 B2 10/2004 Coteus et al.
6,807,650 B2 10/2004 Lamb et al.
6,813,196 B2 11/2004 Park et al.
6,832,303 B2 12/2004 Tanaka
6,834,014 B2 12/2004 Yoo et al.
6,854,042 B1 2/2005 Karabatsos
6,880,094 B2 4/2005 LaBerge
6,889,304 B2 5/2005 Perego et al.
6,912,615 B2 6/2005 Nicolai
6,912,628 B2 6/2005 Wicki et al.
6,925,028 B2 8/2005 Hosokawa et al.
6,944,694 B2 9/2005 Pax
6,948,084 B1 9/2005 Manapat et al.
6,950,366 B1 9/2005 Lapidus et al.
6,954,281 B2 10/2005 Fukuda et al.
6,961,281 B2 11/2005 Wong et al.
6,981,089 B2 12/2005 Dodd et al.
6,982,892 B2 1/2006 Lee et al.
6,982,893 B2 1/2006 Jakobs
6,990,043 B2 1/2006 Kuroda et al.
6,996,686 B2 2/2006 Doblar et al.
7,007,130 B1 2/2006 Holman
7,007,175 B2 2/2006 Chang et al.
7,024,518 B2 4/2006 Halbert et al.
7,046,538 B2 5/2006 Kinsley et al.
7,047,361 B2 5/2006 Chong et al.
7,054,179 B2 5/2006 Cogdill et al.
7,065,626 B2 6/2006 Schumacher et al.
7,072,231 B2 7/2006 Pax
7,073,041 B2 7/2006 Dwyer et al.
7,078,793 B2 7/2006 Ruckerbauer et al.
7,093,066 B2 8/2006 Klein
7,120,727 B2 10/2006 Lee et al.
7,124,260 B2 10/2006 LaBerge et al.
7,127,584 B1 10/2006 Thompson et al.
7,130,308 B2 10/2006 Haddock et al.
7,130,952 B2 10/2006 Nanki et al.
7,133,960 B1 11/2006 Thompson et al.
7,133,972 B2 11/2006 Jeddeloh
7,142,461 B2 11/2006 Janzen
7,149,841 B2 12/2006 LaBerge
7,167,967 B2 1/2007 Bungo et al.
7,181,591 B2 2/2007 Tsai
7,191,302 B2 3/2007 Usami
7,200,021 B2 4/2007 Raghuram
7,225,303 B2 5/2007 Choi
7,227,910 B2 6/2007 Lipka
7,254,036 B2 8/2007 Pauley et al.
7,266,639 B2 9/2007 Raghuram
7,272,709 B2 9/2007 Zitlaw et al.
7,281,079 B2 10/2007 Bains et al.
7,286,436 B2 10/2007 Bhakta et al.
7,289,386 B2 10/2007 Bhakta et al.
7,334,150 B2 2/2008 Ruckerbauer et al.
7,346,750 B2 3/2008 Ishikawa
7,356,639 B2 4/2008 Perego et al.
7,370,238 B2 5/2008 Billick et al.
7,379,361 B2 5/2008 Co et al.
7,437,591 B1 10/2008 Wong
7,461,182 B2 12/2008 Fukushima et al.
7,464,225 B2 12/2008 Tsern
7,471,538 B2 12/2008 Hofstra
7,532,537 B2 5/2009 Solomon et al.
7,619,912 B2 11/2009 Bhakta et al.
7,636,274 B2 12/2009 Solomon et al.
7,864,627 B2 1/2011 Bhakta et al.
7,865,674 B2 1/2011 Gower et al.
7,881,150 B2 2/2011 Solomon et al.
7,916,574 B1 3/2011 Solomon et al.
8,001,434 B1 8/2011 Lee et al.
8,089,795 B2 1/2012 Rajan
8,130,560 B1 3/2012 Rajan
8,189,328 B2 5/2012 Kanapathippillai
8,233,303 B2 7/2012 Best
8,250,295 B2 8/2012 Amidi et al.
8,417,870 B2 4/2013 Lee et al.
8,516,185 B2 8/2013 Lee et al.
8,516,188 B1 8/2013 Solomon et al.
8,756,364 B1 6/2014 Bhakta et al.
8,856,464 B2 10/2014 Karamcheti
9,606,907 B2 3/2017 Lee et al.
2001/0003198 A1 6/2001 Wu
2001/0008006 A1 7/2001 Klein
2001/0050857 A1 12/2001 Keeth et al.
2001/0052057 A1 12/2001 Lai
2002/0048195 A1 4/2002 Klein
2002/0088633 A1 7/2002 Kong et al.
2002/0112119 A1 8/2002 Halbert et al.
2003/0063514 A1 4/2003 Faue
2003/0070052 A1 4/2003 Lai
2003/0090359 A1 5/2003 Ok
2003/0090879 A1 5/2003 Doblar et al.
2003/0191995 A1 10/2003 Abrosimov et al.
2003/0210575 A1 11/2003 Seo et al.
2004/0000708 A1 1/2004 Rapport et al.
2004/0037158 A1 2/2004 Coteus et al.
2004/0098528 A1 5/2004 Janzen
2004/0201968 A1 10/2004 Tafolla
2005/0010737 A1 1/2005 Ware et al.
2005/0036378 A1 2/2005 Kawaguchi et al.
2005/0154820 A1 7/2005 Briggs et al.
2005/0257109 A1 11/2005 Averbuj
2005/0281096 A1 12/2005 Bhakta et al.
2006/0044860 A1 3/2006 Kinsley et al.
2006/0117152 A1 6/2006 Amidi et al.
2006/0126369 A1 6/2006 Raghuram
2006/0129755 A1 6/2006 Raghuram
2006/0179206 A1 8/2006 Brittain et al.
2006/0233012 A1 10/2006 Tomonori et al.
2006/0248969 A1 11/2006 Seo et al.
2006/0259711 A1 11/2006 Oh
2006/0262586 A1 11/2006 Solomon et al.
2006/0267172 A1 11/2006 Nguyen et al.
2006/0277355 A1 12/2006 Ellsberry et al.
2007/0058409 A1 3/2007 Ruckerbauer
2007/0070669 A1 3/2007 Tsern
2007/0293094 A1 12/2007 Aekins
2008/0046631 A1 2/2008 Takaku et al.
2008/0104352 A1 5/2008 Talbot
2008/0162790 A1 7/2008 Im
2009/0103387 A1 4/2009 Shau

(56) **References Cited**

U.S. PATENT DOCUMENTS

2010/0070690	A1	3/2010	Amer et al.
2010/0091540	A1	4/2010	Bhakta et al.
2010/0128507	A1	5/2010	Solomon et al.
2011/0016250	A1	1/2011	Lee et al.
2011/0016269	A1	1/2011	Lee et al.
2011/0090749	A1	4/2011	Bhakta et al.
2011/0125966	A1	5/2011	Amidi et al.

FOREIGN PATENT DOCUMENTS

JP	H10092169	A	9/1997
JP	2010-320270	A	12/1998
JP	10320270	A	12/1998
JP	2000-285674		10/2000
JP	2000311485	A	10/2000
JP	2002-184176		6/2002
JP	2003-007963		1/2003
JP	2008-046989		2/2008
WO	WO 1992/002879		2/1992
WO	WO 1994/007242		3/1994
WO	WO 1995/034030		12/1995
WO	WO 1999/000734		1/1999
WO	WO99/30240		6/1999
WO	WO 2002/058069		7/2002
WO	WO 2002/063804		8/2002
WO	WO 2003/017283		2/2003
WO	WO 2003/069484		8/2003
WO	WO 2006/055497		5/2006

OTHER PUBLICATIONS

Patent Trial and Appeal Board Decision on Request for Rehearing for Reexamination Control No. 95/001,381, mailed Aug. 13, 2014, 7 pages.

Patent Trial and Appeal Board Decision on Appeal for Reexamination Control Nos. 95/000,546 and 95/000,577, mailed Feb. 25, 2015, 25 pages.

Patent Trial and Appeal Board Decision on Request for Rehearing for Reexamination Control Nos. 95/000,546 and 95/000,577, mailed Aug. 27, 2015, 5 pages.

Examiner's Determination after Board Decision on Appeal for Reexamination Control No. 95/001,337, mailed Sep. 11, 2015, 16 pages.

Inter Partes Review Case No. IPR2015-01020, Petition for Inter Partes Review of U.S. Pat. No. 7,881,150, filed on Apr. 7, 2015.

Inter Partes Review Case No. IPR2014-01020, Exhibit 1002 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on Apr. 7, 2015.

Inter Partes Review Case No. IPR2014-01020, Exhibit 1023 to Petition for Inter Partes Review, curriculum vitae of Dr. Srinivasan Jagannathan, filed on Apr. 7, 2015.

Inter Partes Review Case No. IPR2014-01020, Exhibit 1025 to Petition for Inter Partes Review, "operational," *The Pocket Oxford American Dictionary of Current English*, Oxford University Press, 2002, filed on Apr. 7, 2015.

Inter Partes Review Case No. IPR2014-01020, Decision to Institute Inter Partes Review of D U.S. Pat. No. 7,881,150, dated Oct. 8, 2015.

Inter Partes Review Case No. IPR2015-01 021, Petition for Inter Partes Review of U.S. Pat. No. 8,081,536, filed on Apr. 7, 2015.

Inter Partes Review Case No. IPR2014-01 021, Corrected Exhibit 1002 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on Apr. 22, 2015.

Inter Partes Review Case No. IPR2014-01 021, Exhibit 1026 to Petition for Inter Partes Review, curriculum vitae of Dr. Srinivasan Jagannathan, filed on Apr. 7, 2015.

Inter Partes Review Case No. IPR2014-01 021, Decision to Institute Inter Partes Review of U.S. Pat. No. 8,081,536, dated Oct. 8, 2015.

U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc.* v. *Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Corrected Joint Claim Construction and Prehearing Statement Pursuant to Patent L.R. 4-3, including Exhibit A, filed Aug. 27, 2014, 28 pages.

U.S. Court of Appeals for the Federal Circuit, Decision on Appeal for Reexamination U.S. Appl. No. 95/001,381, filed Nov. 13, 2015, 14 pages.

"64 & 72 Pin Zip/Simm Sram Module", JEDEC, Standard No. 21-C, www.jedec.com/download/search/4.sub.--04.sub.--01.pdf, Jun. 1997 pp. 4.4.1-1.

"Bank Striping of Data Across Internal SDRAM Banks," IP.com, IPCOM000013697D, 2000.

"Distributed Memory Mapping," IP.com, IPCOM000014788D, 2000.

"Information Huawei or FPGA-Take Five," Electronic News, 2002, p. 24.

"Method for a high-performance DRAM address mapping mechanism," IP.com, IPCOM000008164D, 2002.

"Method for memory probing on a multiple-DIMM bus," IP.com, IPCOM000019063D, 2003.

"Method for multiple device interface testing using a single device," IP.com, IPCOM000010054D, 2002.

"PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification" JEDEC, Standard No. 21-C, Revision 1.3, Jan. 2002.

"Quad Band Memory (QBMA.TM.): DDR200/266/333 devices producing DDR400/533/667" (the "QBMA Reference"), published by the QBMA Alliance, Platform Conference, San Jose, California, Jan. 23-24, 2002.

Abali, B. "Memory Expansion Technology (MXT): Software Support and Performance," IBM J. Res. & Dev., vol. 45, No. 2, 2001, pp. 287-300.

Arlington, DL Evans. "Enhancement of Memory Card Redundant Bit Usage Via Simplified Fault Alignment Exclusion," IMB Technical Disclosure Bulletin, 1987.

Arroyo et al. "Method of executing Manufacturing ROM Code Without Removing System Roms," IP.com, IPCOM000037214D, 1989.

Ayukawa et al. "An Access-Sequence Control Scheme to Enhance Randon-Acess Performance of Embedded DRAM's," IEEE Journal of Solid-State Circuits, vol. 33, No. 5, p. 800-806, dated May 1998.

Barr, Michael. "Programmable Logic: What's it to Ya?," Embedded Systems Programming, Jun. 1999, pp. 75-84.

Bennayoun et al. "Input/Output Chip Select Doubler," IBM Technical Disclosure Bulletin, vol. 38, No. 04 1995, pp. 237-240.

Blum et al. "Fast Multichip Memory System With Power Select Signal," IMB Technical Disclosure Bulletin, 1979.

Carvalho, Carlos; "The Gap between Processor and Memory Speeds"; ICCA '02.

Cuppu et al. "A Performance Coparison of Contemporary DRAM Architectures," IEEE Proceedings of the 26.sup.th International Symposium on Computer Architectures, May 2-4, 1999, Atlanta, Georgia, pp. 1-12.

Cuppu et al. "Concurrency, Latency, or System Overhead: Which Has the Largest Impact on Uniprocessor DRAM-System Performance?," IEEE, 2001, pp. 62-71.

Cuppu et al. "High-Performance DRAMs in Workstation Environments," IEEE Transactions on Computers, vol. 50, No. 11, 2001, pp. 1133-1153.

Denneau, M. "Logic Processor for Logic Simulation Machine," IBM Technical Disclosure Bulletin, vol. 25, No. 1, 1982.

Fairchild Semiconductor. "DM74LS138 DM74LS139 Decoder/Demultiplexer," Fairchild Semiconductor Corporation, 2000.

Fitzgerald et al. "Chip Select Circuit for Multi-Chip RAM Modules," IP.com, IPCOM000044404D, 1984.

Freedman, Alan. "The Computer Glossary," The Complete Illustrated Dictionary, American Management Association, 2001.

Gray, KS. "Fet Ram Chip Double Density Scheme," IP.com, IPCOM000043942D, 1984.

Grimes et al. "Access Rate/Availability Improvement Logic for Dynamic Memories," IBM Technical Disclosure Bulletin, Oct. 1982.

Gupta et al. "Designing and Implementing a Fast Crossbar Scheduler," IEEE Micro, 1999, pp. 20-28.

Hession et al. "Chip Select Technique for Multi Chip Decoding," IP.com, IPCOM000070404D, 1985.

(56) **References Cited**

OTHER PUBLICATIONS

Hewlett-Packard. "Memory technology evolution: an overview of system memory technologies," technology brief, 7th edition. 2003.
Hoare et al. "An 88-Way Multiprocessor Within an FPGA With Customizable Instructions," Proceedings of the 18th International Parallel and Distributed Processing Symposium, 2004.
Intel Corporation, 66/100 MHz PC SDRAM 64-Bit Non-ECC/Parity 144 Pin Unbuffered SO-DIMM Specification, Revision 1.0, Feb. 1999.
Intel Corporation, PC SDRAM Registered DIMM Design Support Document, Revision 1.2, Oct. 1998.
Intel® 6400/6402 Advanced Memory Buffer Datasheet, published Oct. 2006.
Jacob, Bruce L.; "Synchronous DRAM Architectures, Organizations, and Alternative Technologies". University of Maryland, Dec. 10, 2002.
JEDEC "JEDEC Standard: Double Data Rate (DDR) SDRAM Specification", JESD79C Mar. 2003.
JEDEC Standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published Jan. 2004.
JEDEC Standard No. 21-C, 4.20.5-184 Pin. PC1600/2100 DDR SDRAM Unbuffered DIMM Design Specification, Revision 1.1, Release 11b, Published Apr. 2003.
JEDEC Standard No. 21-C, 4.20-2-168 Pin, PC133 SDRAM Registered Design Specification, Revision 1.4, Release 11a, Feb. 2002.
JEDEC Standard No. 21-C, 4.20-3-144 Pin, PC133 SDRAM Unbuffered SO-DIMM, Reference Design Specification, Revision 1.02, Release 11. Published Oct. 2003.
Jedec Standard, "Definition of the SSTV16859 2.5 V 13-Bit to 26-Bit SSTL.sub.-2 Registered Buffer for Stacked DDR DIMM Applications," JESD82-4B, May 2003.
Jin et al. "Embedded Memory in System-On-Chip Design: Architecture and Prototype Implementation," CCECE, 2003, pp. 141-146.
Jin et al. "Prototype Implementation and Evaluation of a Multibank Embedded Memory Archtecture in Programmable Logic," IEEE, 2003, pp. 13-16.
Kane et al. "Read Only Store Memory Extension," IP.com, IPCOM000082845D, 1975.
Kazusawa et al. "RAS Buffering Technique to Precent Stored Data Destruction in DRAM Standby State," dated Jan. 1, 1996, p. 341-344.
Kellog, Mark; "PC133: SDRAM Main Memory Performance Reaches New Heights"; IBM Microelectronics, 1999.
Keltcher et al.; "The AMD Opteron Processor for Multiprocessor Servers"; IEEE Micro, vol. 23, No. 2, Mar. 2003.
Kirihata et al.; "A 390-mm, 16-Bank, 1-Gb DDR SDRAM with Hybrid Bitline Architecture"; IEEE Journal of Solid-State Circuits, vol. 34, No. 11, Nov. 1999.
Kornaros et al. "A Fully-Programmable Memory Management System Optimizing Queue Handling at Multi Gigabit Rates," DAC, 2003, pp. 54-59.
Lee et al. "A banked-promotion translation lookaside buffer system," Journal of Systems Architecture, vol. 47, 2002, pp. 1065-1078.
Lee et al. "An on-chip cache compression technique to reduce decompression overhead and design complexity." Journal of Systems Architecture, vol. 46, 2000, pp. 1365-1382.
Lin et al. "Designing a Modern Memory Hierarchy with Hardware Prefetching," IEEE Transactions on Computers, vol. 50, No. 11, 2001, pp. 1202-1217.
Luthra et al. "Interface Synthesis Using Memory Mapping for an FPGA Platform," Proceedings of the 21st International Conference on Computer Design, 2003.
Matick et al. "Read-Select Capability for Static Random-Access Memory," IMB Technical Disclosure Bulletin, 1985, pp. 6640-6642.
Matick, RE. "Logic and Decoder Arrangement for Controlling Spill/Wrap Boundaries of a Bit-Addressable Memory Decoder," IMB Technical Disclosure Bulletin, 1984.
Meyers et al. "Use of Partially Good Memory Chips," IP.com, IPCOM000066246D, 1979.
Micron "DDR SDRAM RDIMM, MT36VDDF12872-1GB, MT36VDDF25672-2GB," 2002 Micron Technology, Inc. 20 pages.
Micron "Synchronous DRAM Module MT18LSDT472," 1998, Micron Technology, Inc., 17 pages.
Micron Technical Note,"Decoupling Capacitor Calculations for a DDR Memory Channel," 2004, 3 pages.
Murdocca et al., "Principles of Computer Architecture," Prentice Hall, 2000, pp. 249-251.
Ofek et al. "Partial Two Way Mapping Technique," IMB Technical Disclosure Bulletin, 1969.
Paldan, David. "Programmable Memory Address Decoding for Microprocessor Memory Device," IP.com, IPCOM000005486D, 1983.
PC133 SDRAM Registered DIMM Design Specification, Revision 1.1, Aug. 1999, 62 pages.
Pellinger et al. "Dual Addressable Memory," IP.com, IPCOM000068610D, 1978.
Plotnick et al. "Shuffle Your Chips for Better Performance," PC Week, 1998, p. 90.
Portion of Request for Inter Partes Reexamination of U.S. Pat. No. 7,289,386, corresponding to Reexam U.S. Appl. No. 95/000,577, in 184 pages.
Portion of Request for Inter Partes Reexamination of U.S. Pat. No. 7,619,912, corresponding to Reexam U.S. Appl. No. 95/000,578, in 66 pages.
Portion of Request for Inter Partes Reexamination of U.S. Pat. No. 7,619,912, corresponding to Reexam U.S. Appl. No. 95/000,579, in 32 pages.
Qureshi, "High Utilization and Reliability Memory Bit Steering Method," dated Mar. 1, 1995, p. 615-616.
Schubert et al. "Accelerating system integration by enhancing hardware, firmware, and co-simulation," IBM J. Res. & Dev, vol. 48, No. 3/4, May/Jul. 2004, pp. 569-581.
Skelton, MH. "Program Controlled Paging Scheme for Memory Expansion," IP.com. IPCOM000050954D, 1982.
Siegel et al. "IBM's S/390 G5 Microprocessor Design," IEEE Micro, 1999, pp. 12-23.
Stelzer, KC. "Planar Memory Boundary Registers with Remap Feature," IMB Technical Disclosure Bulletin, 1993.
Smith, BA. "Chip Select Decoder Circuit," IP.com, IPCOM000063400D, 1985.
Sunaga et al. "An Enable Signal Circuit for Multiple Small Banks," IP.com, IPCOM000015887D, 2002.
Sunaga et al. "Continuou RAS Access Method in Multiple-bank DRAM Chip," IP.com, IPCOM000123375D, 1998.
Takai et al. "250 Mbyte/s Synchronous DRAM Using a 3-Stage-Pipelined Architecture," IEEE Journal of Solid-State Circuits, vol. 29, No. 4, p. 426-431, dated Apr. 1994.
Texas Instruments, "TM2SR72EPN 2097152 by 72-Bit, TM4SRT2EPN 4194304 by 72-Bit, Synchronous Dynamic RAM Modules," 1997, 15 pages.
Toal et al. "A 32-Bit SoPC Implementation of a P5." Proceedings of the Eighth IEEE International Symposium on Computers and Communications, 2003, pp. 1530-1346.
Tudruj, Marek. "Dynamically reconfigurable heterogenous multiprocessor systems with transputer-controlled communication," Journal of Systems Architecture, vol. 43, 1997, pp. 27-32.
U.S. District Court Central District of California, Case No. CV09 06900, *Netlist, Inc.* vs. *Inphi Corporation*, Complaint for Patent Infringement, filed Sep. 22, 2009 in 10 pages.
U.S. District Court Central District of California, Case No. CV09 06900, *Netlist, Inc.* vs. *INPHI Corporation*, Defendant Inphi Corporation's Answer to Plaintiff's Complaint for Patent Infringement, filed Nov. 12, 2009 in 6 pages.
U.S. District Court Central District of California, Case No. CV09 06900, *Netlist, Inc.* vs. *INPHI Corporation*, Defendant Inphi Corporation's Answer to Plaintiff's First Amended complaint for Patent Infringement, filed Feb. 11, 2010 in 9 pages.
U.S. District Court Central District of California, Case No. CV09 06900, *Netlist, Inc.* vs. *INPHI Corporation*, Defendant Inphi Corporation's Notice of Motion and Motion for Stay Pending Reex-

(56) **References Cited**

OTHER PUBLICATIONS

aminations and Interference Proceeding Regarding the Patents-In-Suit; Memorandum of Points and Authorities in Support Thereof, filed Apr. 21, 2010 in 28 pages.
U.S. District Court Central District of California, Case No. CV09 06900, *Netlist, Inc.* vs. *INPHI Corporation*, Plaintiff Netlist Inc's Opposition to Defendant Inphi Corporation's Motion for Stay Pending Reexaminations and Interference Proceedings Regarding the Patents-In-Suit, filed May 3, 2010 in 23 pages.
U.S. District Court Central District of California, Case No. CV09 06900, *Netlist, Inc.* vs. *Inphi Corporation*, Plaintiff Netlist, Inc's First Amended Complaint for Patent Infringement, filed Dec. 23, 2009 in 8 pages.
U.S. District Court Northern District of California, Case No. CV08 04144, *Google Inc.* v. *Netlist, Inc.*, Defendant Netlist, Inc.'s Claim Construction Reply Brief, filed Sep. 22, 2009 in 19 pages.
U.S. District Court Northern District of California, Case No. CV08 04144, *Google Inc.* v. *Netlist, Inc.*, Defendant Netlist, Inc.'s Opening Claim Construction Brief, filed Jul. 28, 2009 in 21 pages.
U.S. District Court Northern District of California, Case No. CV08 04144, *Google Inc.* v. *Netlist, Inc.*, Defendant Netlist, Inc.'s Opposition to Google Inc's Motion for Summary Judgment of Invalidity, filed Jul. 6, 2010 in 13 pages.
U.S. District Court Northern District of California, Case No. CV08 04144, *Google Inc.* v. *Netlist, Inc.*, Exhibit A to Joint Claim Construction and Prehearing Statement, filed Jun. 12, 2009 in 2 pages.
U.S. District Court Northern District of California, Case No. CV08 04144, *Google Inc.* v. *Netlist, Inc.*, Exhibit B to Joint Claim Construction and Prehearing Statement, filed Jun. 12, 2009 in 36 pages.
U.S. District Court Northern District of California, Case No. CV08 04144, *Google Inc.* v. *Netlist, Inc.*, Joint Claim Construction and Prehearing Statement, filed Jun. 12, 2009 in 5 pages.
U.S. District Court Northern District of California, Case No. CV08 04144, *Google Inc.* v. *Netlist, Inc.*, Netlist, Inc.'s Answer to Complaint and Counterclaims, filed Nov. 18, 2008 in 9 pages.
U.S. District Court Northern District of California, Case No. CV08 04144, *Google Inc.* v. *Netlist, Inc.*, Order Re Claim Construction, filed Nov. 16, 2009 in 1 page.
U.S. District Court Northern District of California, Case No. CV08 04144, *Google Inc.* v. *Netlist, Inc.*, Plaintiff Google's Reply to Counterclaims, filed Dec. 8, 2008 in 4 pages.
U.S. District Court Northern District of California, Case No. CV08 04144, *Google Inc.* v. *Netlist, Inc.*, Stipulation Re: Additional Agreed-Upon Claim Constructions, filed Oct. 28, 2009 in 3 pages.
U.S. District Court Northern District of California, Case No. CV08 04144, *Google Inc.* vs. *Netlist, Inc.*, [Redacted] Google Inc.'s Responsive Claim Construction Brief, filed Aug. 25, 2009 in 30 pages.
U.S. District Court Northern District of California, Case No. CV08 04144, *Google Inc.* vs. *Netlist, Inc.*, Amended Exhibit A to Joint Claim Construction and Prehearing Statement, filed Oct. 28, 2009 in 1 page.
U.S. District Court Northern District of California, Case No. CV08 04144, *Google Inc.* vs. *Netlist, Inc.*, Appendix 1 to Google's Responsive Claim Construction Brief, filed Aug. 25, 2009 in 4 pages.
U.S. District Court Northern District of California, Case No. CV08 04144, *Google Inc.* vs. *Netlist, Inc.*, Attachment 2 to Exhibit B to Joint Claim Construction and Prehearing Statement, filed Jun. 12, 2009 in 12 pages.
U.S. District Court Northern District of California, Case No. CV08 04144, *Google Inc.* vs. *Netlist, Inc.*, Complaint for Declaratory Relief, filed Aug. 29, 2008 in 49 pages.
U.S. District Court Northern District of California, Case No. CV09 05718, *Netlist, Inc.* vs. *Google, Inc.*, Complaint for Patent Infringement, filed Dec. 4, 2009 in 47 pages.
U.S. District Court Northern District of California, Case No. CV09 05718, *Netlist, Inc.* vs. *Google, Inc.*, Defendant Google Inc's Responsive Claim Construction Brief, filed Aug. 4, 2010 in 27 pages.
U.S. District Court Northern District of California, Case No. CV09 05718, *Netlist, Inc.* vs. *Google, Inc.*, Exhibit A to Joint Claim Construction and Prehearing Statement under Patent L.R. 4-3, filed Jun. 25, 2010 in 2 pages.
U.S. District Court Northern District of California, Case No. CV09 05718, *Netlist, Inc.* vs. *Google, Inc.*, Exhibit B to Joint Claim Construction and Prehearing Statement under Patent L.R. 4-3, filed Jun. 25, 2010 in 23 pages.
U.S. District Court Northern District of California, Case No. CV09 05718, *Netlist, Inc.* vs. *Google, Inc.*, Google's Answer to Plaintiff's Complaint for Patent Infringement; and Assertion of Counterclaims, filed Feb. 12, 2010 in 13 pages.
U.S. District Court Northern District of California, Case No. CV09 05718, *Netlist, Inc.* vs. *Google, Inc.*, Joint Claim Construction and Prehearing Statement Under Patent Local Rule 4-3, filed Jun. 25, 2010 in 5 pages.
U.S. District Court Northern District of California, Case No. CV09 05718, *Netlist, Inc.* vs. *Google, Inc.*, Plaintiff Netlist, Inc.'s Reply to Defendant Google Inc.'s Counterclaim, filed Mar. 8, 2010 in 11 pages.
U.S. District Court Northern District of California, Case No. CV09 05718, *Netlist, Inc.* vs. *Google, Inc.*, Plaintiff Netlist, Inc's Opening Claim Construction Brief, filed Jul. 16, 2010 in 29 pages.
US District Court Civil Docket; *Netlist Inc.* v. *Google Inc.*; 4:09cv5718; Date filed Dec. 4, 2009. in 10 pages.
Vogt, Pete, "Fully Buffered DIMM (FB-DIMM) Server Memory Architecture: Capacity, Performance, Reliability, and Longevity," Intel, Feb. 18, 2004, 33 pages.
Yao, YL. High Density Memory Selection Circuit,: IP.com, IPCOM000078218D, 1972.
Anonymous. (May 2002). "Hynix HYMD512G726(L)8-K/H/L Registered DDR SDRAM DIMM, 128Mx72 bits Product Description," Rev. 0.1/May 2, pp. 1-16.
"Elipida Memory to Speak at Intel's Memory Implementers Forum Roundtable Event", Intel Developer Forum, [Online]. Retrieved from the Internet: <URSL: http://www.elpida.com/en/news/2004/02-18.html>, (Jun. 14, 2011), 1 pg.
Google, Inc. v. *Netlist, Inc.*, No. 4:08-cv-04144-SBA, Netlist Inc.'s Answer to Complaint and Counterclaim (N.D. Ca. Filed Nov. 18, 2008).
Google, Inc. v. *Netlist, Inc.*, No. C 08-04144 SBA Google Inc.'s Invalidity Contentions Pursuant to PAT. L.F. 3-3, dated Apr. 13, 2009.
Google, Inc. v. *Netlist, Inc.*, No. C08 04144, Complaint for Declaratory Relief, (N.D. Ca Dated Aug. 29, 2008).
Google, Inc. v. *Netlist, Inc.*, No. 4:08-cv-04144-SBA, Google Inc.'s Invalidity Contentions Pursuant to Pat. L.F. 3-3, dated Apr. 13, 2009.
International Preliminary Report on Patentability for International Application No. PCT/US2010/040826, dated Nov. 28, 2011 (NETL. 048VPC) in 34 pages.
International Search Report and Written Opinion for Related Application No. PCT/US2010/040826, dated Sep. 27, 2010, in 15 pages.
JEDEC Standard No. 21-C, 4.20.6-200 Pin. PC2700/PC2100/PC1600 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification, Revision 1.1, Release 11b, Apr. 26, 2002.
JEDEC Standard No. 21-C, 4.20-2-168 Pin, PC133 SDRAM Registered SO-DIMM, Reference Design Specification, Revision 1.02, Release 11. Published Oct. 2003.
JEDEC Standard No. 21-C, DDR SDRAM PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, Revision 1.3, Release 11b, Jan. 2002.
Karabatsos, C., "Quad Band Memory (QBM) Technology", Kentron Technologies, Inc., Apr. 2001, pp. 1-5.
Letter from G. Hopkins Guy III, Orrick, Herrington & Sutcliffe LLP, to R. Scott Oliver, Morrison & Foerster, (Apr. 14, 2009).
MetaRAM, Inc. v. *Netlist, Inc.* No. 3:09-cv-01309-VRW, MetaRam's Reply to Netlist's Counterclaims, (N.D. Ca. Filed Jun. 3, 2009).

(56) **References Cited**

OTHER PUBLICATIONS

MetaRam, Inc. v. *Netlist, Inc.*, No. 3:09-cv-01309-VRW, Netlist's Answer to Complaint and Counterclaims, (N.D. Ca, filed May 11, 2009).
MetaRAM, Inc. v. *Netlist, Inc.*, No. C09 01309, Complaint for Patent Infringement, (N.D. Ca. Filed Mar. 25, 2009).
Micron "DDR2 SDRAM Registered DIMM (RDIMM)," 2003 Micron Technology, Inc. 18 pages.
Miles J. Murdocca et al., "Principles of Computer Architecture", Prentice Hall, Inc., Upper Saddle River, NJ, 2000, pp. 243-252.
Netlist, Inc. v. *MetaRam, Inc.*, No. 09-165-GMS, MetaRAM, Inc.'s Answer and Affirmative Defenses to Plaintiff's Complaint, dated Apr. 20, 2009.
Netlist, Inc. v. *MetaRAM, Inc.*, No. 1:09-ccv-00165-GMS, Complaint for Patent Infringement, (D. Del. Filed Mar. 12, 2009).
Non-Final Action Closing Prosecution dated Sep. 1, 2010, for Control No. 95/001,339, filed Apr. 10, 2010, 17 pages.
Non-Final Action Closing Prosecution dated Jun. 21, 2011, for Control No. 95/001,381, filed Jun. 9, 2010, 34 pages.
Non-Final Action Closing Prosecution dated Mar. 12, 2012, for Control No. 95/001,337, filed Apr. 19, 2010, 33 pages.
Non-Final Action dated Aug. 27, 2010, for Control No. 95/000,546, filed May 11, 2010, 16 pages.
Non-Final Action dated Sep. 8, 2010, for Control No. 95/001,381, filed Jun. 9, 2010, 17 pages.
Non-Final Action dated Apr. 4, 2011, for Control No. 95/001,339, filed Apr. 20, 2010, 61 pages. (merged with 95/000,578 and 95/000,579).
Non-Final Action dated Jun. 15, 2011, for Control No. 95/001,381, filed Jun. 9, 2010, 33 pages.
Non-Final Action dated Sep. 27, 2011, for Control No. 95/001,337, filed Apr. 19, 2010, 19 pages.
Non-Final Action dated Oct. 4, 2011, for Control No. 95/001,339, filed Apr. 20, 2010, 77 pages. (merged with 95/000,578 and 95/000,579).
Non-Final Action dated Oct. 14, 2011, for Control No. 95/001,339, filed Apr. 30, 2010, 99 pages. (merged with 95/000,578 and 95/000,579).
Non-Final Office Action dated Nov. 16, 2011, for U.S. Appl. No. 95/001,758 filed Sep. 14, 2011, 25 pages.
Order Granting Request for Inter Partes Reexamination mailed Nov. 16, 2011, for U.S. Appl. No. 95/001,758, filed Sep. 14, 2011, 13 pages.
Order Granting Request for Inter Partes Reexamination mailed Aug. 9, 2010, for Control No. 95/000,546, filed May 11, 2010, 22 pages.
Order Granting Request for Inter Partes Reexamination mailed Aug. 27, 2010, for Control No. 95/001,337, filed Apr. 19, 2010, 21 pages.
Order Granting Request for Inter Partes Reexamination mailed Sep. 1, 2010, for Control No. 95/001,339, filed Apr. 20, 2010, 14 pages.
Order Granting Request for Inter Partes Reexamination mailed Sep. 8, 2010, for Control No. 95/000,381, filed Jun. 9, 2010, 21 pages.
Order Granting Request for Inter Partes Reexamination mailed Jan. 14, 2011, for Control No. 95/000,579, filed Oct. 21, 2010, 12 pages.
Order Granting Request for Inter Partes Reexamination mailed Jan. 18, 2011, for Control No. 95/000,577, filed Oct. 20, 2010, 17 pages.
Order Granting Request for Inter Partes Reexamination mailed Jan. 18, 2011, for Control No. 95/000,578, filed Oct. 20, 2010, 14 pages.
Request for Inter Partes Reexamination for U.S. Pat. No. 8,250,295, filed Sep. 15, 2012, 601 pages. (submitted in three parts.).
Right of appeal Notice mailed Feb. 7, 2012, for Control No. 95/001,381, 33 pages.
Right of Appeal Notice mailed Jun. 22, 2012, for Control No. 95/001,337, filed Jun. 4, 2010, 34 pages.
Russell, Gill, "Intel Micron Hybrid Memory Cube: The Future of Exascale Computing," Bright Side of News. Sep. 19, 2011, <http:www.brightsideofnews.com/news/2011/9/19/intel-mocron-hybrid-momory-cube-the-future-of-exascale-compting.aspx> Printed Oct. 13, 2011 in 8 pages.
U.S. District Court Northern District of California, Case No. CV08 04144, *Google Inc.* vs. *Netlist, Inc.*, Attachment 1 to Exhibit B to Joint Claim Construction and Prehearing Statement, filed Jun. 12, 2009 in 7 pages.
US District Court Civil Docket; *Google Inc.* v. *Netlist Inc.*; 4:08cv04144; Date filed Aug. 29, 2008.
US District Court Civil Docket; *Netlist Inc.* v. *Inphi Corporation*; 2:09cv6900; Date filed Sep. 22, 2009.
Written Opinion for International Application No. PCT/US2010/040826, dated Oct. 24, 2011 (NETL.048VPC) in 7 pages.
Anonymous. (Dec. 1996). "Applications Note: Understanding DRAM Operation," IBM, 10 pages.
Behrens, S. "HP Printer Memory Explained", The ZonkPage, Last Updated Jan. 21, 2004. Accessed Feb. 10, 2013, Retrieved from the Internet: URL <http://warshaft.com/hpmem.htm>. 7pp.
Non-Final Office Action, U.S. Appl. No. 13/412,243, dated Jan. 2, 2014, 20 pages.
Non-Final Office Action, U.S. Appl. No. 12/761,179, dated Sep. 13, 2012, 20 pages.
Non-final office action, U.S. Appl. No. 13/288,850, dated Oct. 14, 2013, 24 pages.
Non-final office action, U.S. Appl. No. 13/411,344, dated Dec. 31, 2013, 28 pages.
Non-final office action, U.S. Appl. No. 13/473,413, dated Nov. 17, 2011, 46 pages.
Non-Final Office Action, dated Jan. 2, 2014, for U.S. Appl. No. 13/287,042, filed Nov. 1, 2011, 42 pages.
Response to Non-Final Office Action dated Jan. 2, 2014 for U.S. Appl. No. 13/287,042, filed Apr. 2, 2014, 12 pages.
Response to non-final office action dated Sep. 13, 2012 for U.S. Appl. No. 12/761,179, filed Mar. 13, 2013, 16 pages.
Response to non-final office action dated Oct. 14, 2013 for U.S. Appl. No. 13/288,850, filed Jan. 14, 2014, 15 pages.
Response to non-final office action dated Dec. 31, 2013 for U.S. Appl. No. 13/411,344, filed Mar. 31, 2014, 12 pages.
Patent Owner's Response to Office Action dated Nov. 13, 2012 for Reexamination Control Nos. 95/000,578; 95/000,579, and 95/001,339, filed Jan. 14, 2013, 96 pages.
Patent Owner's Response to Office Action dated Dec. 19, 2012 for Reexamination Control No. 95/001,758, filed Mar. 19, 2013, 61 pages.
Patent Owner's Response to Office Action dated Sep. 26, 2013 for Reexamination Control No. 95/001,758, filed Nov. 26, 2013, 85 pages.
Third Party Requester's Comments after Non-Final Action dated Sep. 26, 2013 for Reexamination Control No. 95/001,758, filed Dec. 26, 2013.
Reexamination Control No. 95/002,399, filed Apr. 25, 2013, and its entire file history.
Patent Owner's Appeal Brief for Reexamination Control Nos. 95/000,546 and 95/000,577, filed Oct. 2, 2013, 46 pages.
Patent Trial and Appeal Board Decision on Appeal for Reexamination Control No. 95/001,337, mailed Jan. 16, 2014, 30 pages.
Patent Trial and Appeal Board Decision on Appeal for Reexamination Control No. 95/001,381, mailed Jan. 16, 2014, 24 pages.
Action Closing Prosecution dated Mar. 27, 2014 for Reexamination Control No. 95/001,758, filed Sep. 14, 2011, 40 pages.
Action Closing Prosecution dated Mar. 27, 2014 for Reexamination Control No. 95/001,339, filed Jun. 8, 2010, 106 pages.
Action Closing Prosecution dated Oct. 1, 2012, for Control Nos. 95/000,546 and 95/000,577, filed May 11, 2010 and Oct. 20, 2010 respectively, 39 pages.
Non-Final Office Action dated Nov. 13, 2012, for Control Nos. 95/001,339, 95/000,578 and 95/000,579, filed Apr. 20, 2010, Oct. 20, 2010 and Oct. 21, 2010 respectively, 81 pages.
Order Granting Request for Inter Partes Reexamination and Non-Final Office Action dated Dec. 7, 2012, for Control No. 95/002,399, filed Sep. 15, 2012, 89 pages.
Non-Final Office Action dated Dec. 19, 2012, for Control No. 95/001,758, filed Sep. 14, 2011, 36 Pages.
Request for Inter Partes Reexamination; Reexam U.S. Appl. No. 95/001,758, for U.S. Pat. No. 7,864,627, filed Sep. 15, 2011, 814 pages. (submitted in four parts.).
Request for Inter Partes Reexamination; Reexam U.S. Appl. No. 95/001,381, for U.S. Pat. No. 7,532,537, filed Jun. 9, 2010, 247 pages.

(56) **References Cited**

OTHER PUBLICATIONS

Notice of Allowance, U.S. Appl. No. 12/761,179, dated Jul. 11, 2013, 37 pages.
Notice of Allowance, U.S. Appl. No. 12/504,131, dated Feb. 12, 2013, 52 pages.
U.S. Appl. No. 13/411,344, filed Mar. 2, 2012, Lee.
U.S. Appl. No. 13/970,606, filed Aug. 20, 2013, Netlist, Inc.
U.S. Appl. No. 13/971,231, filed Aug. 20, 2013, Netlist, Inc.
U.S. Appl. No. 14/229,844, filed Mar. 29, 2014, Netlist, Inc.
U.S. Appl. No. 14/324,990, filed Jul. 7, 2014, Netlist, Inc.
U.S. Appl. No. 14/337,168, filed Jul. 21, 2014, Netlist, Inc.
Inter Partes Review of U.S. Pat. No. 7,881,150, IPR Case No. IPR2014-00882, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed Oct. 7, 2014.
Inter Partes Review of U.S. Pat. No. 7,881,150, IPR Case No. IPR2014-00882, Decision—Institution of Inter Partes Review 37 C.F.R. § 42.108, issued Dec. 16, 2014.
Inter Partes Review of U.S. Pat. No. 8,081,536, IPR Case No. IPR2014-00883, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed Oct. 7, 2014.
Inter Partes Review of U.S. Pat. No. 8,081,536, IPR Case No. IPR2014-00883, Decision—Institution of Inter Partes Review 37 C.F.R. § 42.108, issued Dec. 16, 2014.
Inter Partes Review of U.S. Pat. No. 7,881,150, IPR Case No. IPR2014-01011, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed Oct. 7, 2014.
Inter Partes Review of U.S. Pat. No. 7,881,150, IPR Case No. IPR2014-01011, Decision—Institution of Inter Partes Review 37 C.F.R. § 42.108, issued Dec. 16, 2014.
Inter Partes Review of U.S. Pat. No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3001 to Decision—Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued Dec. 16, 2014.
Inter Partes Review of U.S. Pat. No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3002 to Decision—Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued Dec. 16, 2014.
Inter Partes Review of U.S. Pat. No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3003 to Decision—Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued Dec. 16, 2014.
Inter Partes Review of U.S. Pat. No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3004 to Decision—Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued Dec. 16, 2014.
McCluskey, Edward J., *Logic Design Principles with Emphasis on Testable Semicustom Circuits*, Prentice Hall, 1986, pp. 104-107 and 119-120.
Inter Partes Review Case No. IPR2014-01029, Petition for Inter Partes Review of U.S. Pat. No. 8,516,185, filed on Jun. 24, 2014.
Inter Partes Review Case No. IPR2014-01029, Exhibit 1008 to Petition for Inter Partes Review, "Declaration of Charles J. Neuhauser, Ph.D. under 37 C.F.R. § 1.68," filed on Jun. 24, 2014.
Inter Partes Review Case No. IPR2014-01029, Supplemental Petition for Inter Partes Review of U.S. Pat. No. 8,516,185, filed on Jul. 23, 2014.
Inter Partes Review Case No. IPR2014-01029, Patent Owner's Preliminary Response pursuant to 37 C.F.R. § 42.107, filed on Oct. 17, 2014.
Inter Partes Review Case No. IPR2014-01029, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued Dec. 16, 2014.
Inter Partes Review Case No. IPR2014-01029, Petitioner's Request for Rehearing pursuant to 37 C.F.R. § 42.71, filed on Jan. 15, 2015.
Inter Partes Review Case No. IPR2014-01029, Decision Denying Request for Rehearing, Issued on Mar. 3, 2015.
Inter Partes Review Case No. IPR2014-01369, Corrected Petition for Inter Partes Review of Claims 1-19 of U.S. Pat. No. 8,516,185, filed on Sep. 22, 2014.
Inter Partes Review Case No. IPR2014-01369, Exhibit 1008 to Corrected Petition for Inter Partes Review, "Declaration of Dr. Nader Bagherzadeh under 37 C.F.R. § 1.68," filed on Sep. 22, 2014.
Inter Partes Review Case No. IPR2014-01369, Exhibit 1013 to Corrected Petition for Inter Partes Review, "Webster's II New College Dictionary," filed on Sep. 22, 2014.
Inter Partes ReView Case No. IPR2014-01369, Exhibit 1014 to Corrected Petition for Inter Partes Review, "Standard Dictionary of Electrical and Electronics Terms," IEEE 1988, filed on Sep. 22, 2014.
Inter Partes Review Case No. IPR2014-01369, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued Mar. 9, 2014.
U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc.* v. *Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Smart Storage Systems, Inc.'s Invalidity Contentions, dated Jun. 6, 2014.
U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc.* v. *Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Exhibits E.1-E.7 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated Jun. 6, 2014.
U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc.* v. *Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Diablo Technologies, Inc.'s Invalidity Contentions, dated Jun. 6, 2014.
U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc.* v. *Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Exhibits D-1 to D6 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated Jun. 6, 2014.
Office Action dated Apr. 2, 2014, for Japanese Patent Application No. 2012-520662 and English translation thereof, 7 pages.
International Search Report and Written Opinion, PCT/US2011/059209, dated Jan. 31, 2013.
Inter Partes Review Case No. 2014-00882, Patent Owner Response, filed May 8, 2015.
Inter Partes Review Case No. 2014-00882, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed Jun. 19, 2015.
Inter Partes Review Case No. 2014-00882, Petitioner's Request for Oral Argument, filed Jul. 1, 2015.
Inter Partes Review Case No. 2014-00882, Patent Owner's Request for Oral Argument, filed Jul. 3, 2015.
Inter Partes Review Case No. 2014-00882, Order—Request for Oral Argument—37 C.F.R. 42.70, filed Jul. 10, 2015.
Inter Partes Review Case No. 2014-00882, Record of Oral Hearing, filed Nov. 16, 2015.
Inter Partes Review Case No. 2014-00882, Final Written Decision 35 USC 318 and 37 CFR 42.73, filed Dec. 14, 2015.
Inter Partes Review Case No. 2014-00882, Netlist Inc.'s Notice of Appeal, filed Feb. 10, 2016.
Inter Partes Review Case No. 2014-00882, Exhibit 1022, 'Professor Carl Sechen Deposition Transcript,' filed Jun. 19, 2015.
Inter Partes Review Case No. 2014-00882, Exhibit 1023, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed Jun. 19, 2015.
Inter Partes Review Case No. 2014-00882, Exhibit 2002, 'Declaration of Professor Carl Sechen,' filed May 8, 2015.
Inter Partes Review Case No. 2014-00882, Exhibit 2003, 'Transcript of Videotaped Deposition of Srinivasan Jagannathan, Ph. D,' filed May 8, 2015.
Microsoft Computer Dictionary, Fifth Edition, Microsoft Press, p. 334, 2002.
Jacob, Bruce, et al. "Memory Systems—Cache, DRAM, Disk," Elsevier Inc. 2008, Chapters 7 and 10.
U.S. District Court Northern District of California, Case No. 4.13-cn-05889-YGR, *Netlist Inc.* v. *Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Joint Claim Construction and Prehearing Statement Pursuant to Patent L. T. 4-3, filed Aug. 27, 2014, in 28 pages.
Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 349-411.

(56) **References Cited**

OTHER PUBLICATIONS

Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 133-265.
Selected Entries in Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/view/Entry/175039?redirectedFrom=selectively#eid.
Web search results from the Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/search?searchType=dictionary&q=select&_searchBin=Search.
Inter Partes Review Case No. 2014-00883, Patent Owner Response, filed May 8, 2015.
Inter Partes Review Case No. 2014-00883, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed Jun. 19, 2015.
Inter Partes Review Case No. 2014-00883, Petitioner's Request for Oral Argument, filed Jul. 1, 2015.
Inter Partes Review Case No. 2014-00883, Patent Owner's Request for Oral Hearing, filed Jul. 3, 2015.
Inter Partes Review Case No. 2014-00883, Order—Request for Oral Argument—37 C.F.R. 42.70, filed Jul. 10, 2015.
Inter Partes Review Case No. 2014-00883, Record of Oral Hearing, filed Nov. 16, 2015.
Inter Partes Review Case No. 2014-00883, Final Written Decision—35 USC 318 and 37 CFR 42.73, filed Dec. 14, 2015.
Inter Partes Review Case No. 2014-00883, Netlist Inc.'s Notice of Appeal, filed Feb. 10, 2016.
Inter Partes Review Case No. 2014-00883, Exhibit 1025, 'Professor Carl Sechen Deposition Transcript,' filed Jun. 19, 2015.
Inter Partes Review Case No. 2014-00883, Exhibit 1026, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed Jun. 19, 2015.
Inter Partes Review Case No. 2014-01011, Patent Owner Response, filed May 8, 2015.
Inter Partes Review Case No. 2014-01011, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed Jun. 19, 2015.
Inter Partes Review Case No. 2014-01011, Petitioner's Request for Oral Argument, filed Jul. 1, 2015.
Inter Partes Review Case No. 2014-01011, Patent Owner's Request for Oral Hearing, filed Jul. 3, 2015.
Inter Partes Review Case No. 2014-01011, Order—Request for Oral Argument—37 C.F.R. 42.70, filed Jul. 10, 2015.
Inter Partes Review Case No. 2014-01011, Record of Oral Hearing, filed Nov. 16, 2015.
Inter Partes Review Case No. 2014-01011, Final Written Decision—35 USC 318 and 37 CFR 42.73, filed Dec. 14, 2015.
Inter Partes Review Case No. 2014-01011, Netlist Inc.'s Notice of Appeal, filed Feb. 10, 2016.
Inter Partes Review Case No. 2014-01011, Exhibit 1027, 'Professor Carl Sechen Deposition Transcript,' filed Jun. 19, 2015.
Inter Partes Review Case No. 2014-01011, Exhibit 1028, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed Jun. 19, 2015.
Petition for Inter Partes Review filed on Jun. 24, 2014 for U.S. Pat. No. 8,516,185, IPR Case No. IPR2014-01029, and all associated documents including cited references and expert declarations, available at https://ptabtrials.uspto.gov.
Petition for Inter Partes Review filed on Jun. 22, 2014 for U.S. Pat. No. 7,881,150, IPR Case No. IPR2014-00882 and IPR Case No. IPR2014-01011, and all associated documents including cited references and expert declarations, available at https://ptabtrials.uspto.gov.
Petition for Inter Partes Review filed on Jun. 24, 2014 for U.S. Pat. No. 8,081,536, IPR Case No. IPR2014-00883, and all associated documents including cited references and expert declarations, available at https://ptabtrials.uspto.gov.
Altera, ACEX iK, Programmable Logic Device Family, Data Sheet, May 2003, Ver 3.4.
Horowitz, "The Art of Electronics," Cambridge Univ. Press, 1989, selected pages.
JEDEC Standard No. 21-C Section 4.5.7, 168 Pin Registered SDRAM DIMM Family, Release 7.
JEDEC 21-C, Section 4.6.1, 278 Pin Buffered SDRAM DIMM Family.
JEDEC Standard No. 21-C Section 4.1.2.5, Appendix E, "Specific PD's for Synchronous DRAM (SDRAM)," pp. 1-25.
Inter Partes Review Case No. IPR2014-00882, Corrected Petition for Inter Partes Review of U.S. Pat. No. 7,881,150, filed on Jul. 8, 2014.
Inter Partes Review Case No. IPR2014-00882, Exhibit 1007 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on Jun. 22, 2014.
Inter Partes Review Case No. IPR2014-00883, Corrected Petition for Inter Partes Review of U.S. Pat. No. 8,081,536, filed on Jul. 8, 2014.
Inter Partes Review Case No. IPR2014-00883, Exhibit 1011 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on Jun. 21, 2014.
Inter Partes Review Case No. IPR2014-01011, Corrected Petition for Inter Partes Review of U.S. Pat. No. 7,881,150, filed on Jul. 8, 2014.
Inter Partes Review Case No. IPR2014-01011, Exhibit 1007 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan." filed on Jun. 22, 2014.
McCluskey, Edward J., *Logic Design Principles with Emphasis on Testable Semicusto Circuits*, Prentice Hall, 1986, pp. 104-107 and 119-120.
MICRON, DDR SDRAM DIMM Module: MT16VDDT3264A—256 MB; MT16VDDT6464A—512 MB, Data Sheet, 2002, Micron Technology, Inc.
U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc.* v. *Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Exhibits F.1-F.5 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated Jun. 6, 2014.
U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc.* v. *Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Exhibits G.1-G.6 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated Jun. 6, 2014.
U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc.* v. *Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Exhibit H to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated Jun. 6, 2014.
U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc.* v. *Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Exhibits F-1 to F-5 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated Jun. 6, 2014.
U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc.* v. *Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Exhibits G-1 to G-6 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated Jun. 6, 2014.
U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc.* v. *Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Exhibit H to "Diablo Technologies, Inc.'s Invalidity Contentions," dated Jun. 6, 2014.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Related Matters, filed Apr. 28, 2015.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Patent Owner Response to Petition, filed Feb. 22, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Petitioner's Objections to Evidence, filed Feb. 29, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Petitioner's Reply, filed May 19, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Petitioner Request for Oral Argument, filed Jun. 2, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Patent Owner Motion for Observations, filed Jun. 2, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Patent Owner Request for Oral Argument, filed Jun. 2, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Order Trial Hearing, filed Jun. 8, 2016.

(56) **References Cited**

OTHER PUBLICATIONS

Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Patent Owner's Submission on Propriety of Petitioner Reply, filed Jun. 9, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Petitioner's Response to Motion for Observations, filed Jun. 10, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Petitioner's Response to Netlist's Submission, filed Jun. 13, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Patent Owner's Objections to Petitioner's Demonstrative Exhibits, filed Jun. 23, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Patent Owner's Demonstrative Exhibits, filed Jun. 24, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Petitioner's Updated Exhibit List, filed Jun. 24, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, May 10, 2016 Deposition of Carl Sechen, filed May 19, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Petitioner's Demonstrative Exhibits, filed Jun. 24, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Exhibit 2001, "Declaration of Professor Carl Sechen," filed Feb. 22, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Exhibit 2002, "Videotaped Deposition of Srinivasan Jagannathan, Ph.D on Feb. 12, 2016," filed Feb. 22, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Exhibit 2003, "Videotaped Deposition of Srinivasan Jagannathan, Ph.D on Apr. 20, 2015," filed Feb. 22, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Exhibit 2007, "Deposition of Dr. Srinivasan Jagannathan on May 25, 2016," filed Jun. 2, 2016.
Inter Partes Review of U.S. Pat. No. 8,081,536, Case No. IPR2015-01021, Patent Owner Response to Petition, filed Feb. 22, 2016.
Inter Partes Review of U.S. Pat. No. 8,081,536, Case No. IPR2015-01021, Petitioner's Objections to Evidence, filed Feb. 29, 2016.
Inter Partes Review of U.S. Pat. No. 8,081,536, Case No. IPR2015-01021, Petitioner's Reply, filed May 19, 2016.
Inter Partes Review of U.S. Pat. No. 8,081,536, Case No. IPR2015-01021, Petitioner Request for Oral Argument, filed Jun. 2, 2016.
Inter Partes Review of U.S. Pat. No. 8,081,536, Case No. IPR2015-01021, Patent Owner Motion for Observations, filed Jun. 2, 2016.
Inter Partes Review of U.S. Pat. No. 8,081,536, Case No. IPR2015-01021, Patent Owner Request for Oral Argument, filed Jun. 2, 2016.
Inter Partes Review of U.S. Pat. No. 8,081,536, Case No. IPR2015-01021, Patent Owner's Submission on Propriety of Petitioner Reply, filed Jun. 9, 2016.
Inter Partes Review of U.S. Pat. No. 8,081,536, Case No. IPR2015-01021, Petitioner's Response to Motion for Observations, filed Jun. 10, 2016.
Inter Partes Review of U.S. Pat. No. 8,081,536, Case No. IPR2015-01021, Petitioner's Response to Patent Owner's Submission, filed Jun. 13, 2016.
Inter Partes Review of U.S. Pat. No. 8,081,536, Case No. IPR2015-01021, Patent Owner's Objections to Petitioner's Demonstrative Exhibits, filed Jun. 23, 2016.
Inter Partes Review of U.S. Pat. No. 8,081,536, Case No. IPR2015-01021, Patent Owner's Demonstrative Exhibits, filed Jun. 24, 2016.
Inter Partes Review of U.S. Pat. No. 8,081,536, Case No. IPR2015-01021, Petitioner's Updated Exhibit List, filed Jun. 24, 2016.
Inter Partes Review of U.S. Pat. No. 8,081,536, Case No. IPR2015-01021, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016.
Inter Partes Review of U.S. Pat. No. 8,081,536, Case No. IPR2015-01021, Exhibit 2001, "Declaration of Professor Carl Sechen," filed Feb. 22, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Record of Oral Hearing, dated Jul. 26, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Final Written Decision, issued Sep. 28, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Exhibit 3001 to Final Decision, issued Sep. 28, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Exhibit 3001-2 to Final Decision, issued Sep. 28, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Exhibit 3002 to Final Decision, issued Sep. 28, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Exhibit 3003 to Final Decision, issued Sep. 28, 2016.
Inter Partes Review of U.S. Pat. No. 7,881,150, Case No. IPR2015-01020, Exhibit 3004 to Final Decision, issued Sep. 28, 2016.
Inter Partes Review of U.S. Pat. No. 8,081,536, Case No. IPR2015-01021, Final Decision, issued Sep. 28, 2016.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Petition for Inter Partes Review, filed Dec. 30, 2016.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Exhibit 1003, "Declaration of Harold S. Stone," filed Dec. 30, 2016.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-00577, Petition for Inter Partes Review, filed Jan. 5, 2017.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-00577, Exhibit 1003, "Declaration of Harold S. Stone," filed Jan. 5, 2017.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Exhibit 1008, Declaration of John J. Kelly Regarding Records of Joint Electron Device Engineering Council (JEDEC), filed Dec. 30, 2016.
JEDEC Standard Double Data Rate (DDR) SDRAM Specification, JESD79 (Jun. 2000).
Texas Instruments SN74LS245 octal bus transceivers with 3-state outputs datasheet, 2002.
Stone, H.S. Microcomputer Interfacing, Reading, MA: Addison Wesley, 1982.
128Mbit SDRAM, Samsung datasheet K4S281632C, Rev. 00. Mar. 2000.
G. Moore, "Cramming more components onto integrated circuits," Electronics, vol. 38, No. 8, Apr. 19, 1965.
Business Wire, Samsung Announces Mass Production of DDR2; Industry's First 1 GigaByte DDR2 DIMM Offers High Speed and Low Power Necessary for Next-Generation PCs and Servers, Mar. 24, 2003.
Business Wire, Samsung DDR2 Ready to Support Market for Next Generation PCs and Servers, Sep. 16, 2003. 8. IEEE, Inc., "chip select," IEEE Standard Dictionary of Electrical and Electronic Terms, 5th Ed., 1993.
Patent Trial and Appeal Board Decision on Appeal for Reexamination Control Nos. 95/000,578; 95/000,579; and 95/001,339, mailed May 31, 2016, 106 pages.
Patent Trial and Appeal Board Decision on Appeal for Reexamination Control No. 95/001,758, dated May 31, 2016, 49 pages.
Patent Trial and Appeal Board Decision on Appeal for Reexamination Control Nos. 95/000,546 and 95/000,577, dated Feb. 25, 2015, 25 pages.
Patent Trial and Appeal Board Decision on Request for Rehearing for Reexamination Control Nos. 95/000,546 and 95/000,577, dated Aug. 27, 2015, 5 pages.
Smith, Van. "Kentron Q&A." Van's Hardware. www.vanshardware.com. Dec. 3, 2001, 4 pages.
Weste, Neil H.E. et al., "CMOS VLSI Design: A Circuits and Systems Perspective." 3rd Edition, 2005. 4 pages.
"Weste, Neil H.E. et al., ""CMOS VLSI Design: A Circuits and Systems Perspective."" 4thEdition, 2011. 4 pages."
Non-Final Action Closing Prosecution dated Mar. 21, 2014, for Control Nos. 95/001,339; 95/000,578; and 95/000,579, 92 pages.
Patent Trial and Appeal Board Decision on Appeal for Reexamination Control No. 95/001,381, dated Jan. 16, 2014, 24 pages.

(56) **References Cited**

OTHER PUBLICATIONS

Requester Request for Rehearing after Board Decision dated Feb. 18, 2014 for Reexamination Control No. 95/001,337.
Patent Owner Response after Board Decision dated Mar. 18, 2014 for Reexamination Control No. 95/001,337.
Affidavit-traversing rejectns or objectns rule 132 dated Mar. 18, 2014 for Reexamination Control No. 95/001,337.
Patent Owner Response after Board Decision dated Mar. 19, 2014 for Reexamination Control No. 95/001,337.
Affidavit-traversing rejectns or objectns rule 132 dated Mar. 19, 2014 for Reexamination Control No. 95/001,337.
Patent Owner Comments on Req for Rehearing timely dated Mar. 19, 2014 for Reexamination Control No. 95/001,337.
Reexam—Affidavit/Decl/Exhibit Filed by 3rd Party dated Apr. 17, 2014 for Reexamination Control No. 95/001,337.
Requester Comments on Patent Owner Response after Board Decision dated Apr. 17, 2014 for Reexamination Control No. 95/001,337.
New Board of Appeals Decision after Board Decision with New Ground of Rejection: New Ground of Rejection dated Jun. 26, 2014 for Reexamination Control No. 95/001,337.
Patent Owner Response after Board Decision dated Jul. 29, 2014 for Reexamination Control No. 95/001,337.
Reexam Petition Decision—Denied dated Aug. 5, 2014 for Reexamination Control No. 95/001,337.
Requester Comments on Patent Owner Response after Board Decision dated Sep. 5, 2014 for Reexamination Control No. 95/001,337.
Reexam—Affidavit/Decl/Exhibit Filed by 3rd Party dated Sep. 5, 2014 for Reexamination Control No. 95/001,337.
Examiner's Determination on Patent Owner Response/Requester Comments after Board Decision dated Jun. 15, 2015 for Reexamination Control No. 95/001,337.
Examiner's Determination on Patent Owner Response/Requester Comments after Board Decision dated Sep. 11, 2015 for Reexamination Control No. 95/001,337.
Ffidavit-traversing rejectns or objectns rule 132 dated Oct. 14, 2015 for Reexamination Control No. 95/001,337.
Affidavit-traversing rejectns or objectns rule 132 (26 pages) dated Oct. 14, 2015 for Reexamination Control No. 95/001,337.
Patent Owner Comments on Examiner's Determination after Board Decision dated Oct. 14, 2015 for Reexamination Control No. 95/001,337.
Reexam—Affidavit/Decl/Exhibit Filed by 3rd Party dated Nov. 13, 2015 for Reexamination Control No. 95/001,337.
Reqr Comments on Examiners Determ after Board Decision dated Nov. 13, 2015 for Reexamination Control No. 95/001,337.
Other Reference-Patent/App/Search documents dated Nov. 22, 2016 for Reexamination Control No. 95/001,337.
Petition under Rule 41.3 to Chief Admin Patent Judge dated Nov. 22, 2016 for Reexamination Control No. 95/001,337.
Administrative Remand to Examiner dated Jan. 19, 2017 for Reexamination Control No. 95/001,337.
Reexam Petition Decision—Granted—in-part dated Jan. 23, 2017 for Reexamination Control No. 95/001,337.
Affidavit-traversing rejectns or objectns rule 132 dated Feb. 22, 2017 for Reexamination Control No. 95/001,337.
Patent Owner Comments on Examiner's Determination after Board Decision dated Feb. 22, 2017 for Reexamination Control No. 95/001,337.
Reexam—Affidavit/Decl/Exhibit Filed by 3rd Party dated Mar. 22, 2017 for Reexamination Control No. 95/001,337.
Requester Comments on Patent Owner Response after Board Decision dated Mar. 22, 2017 for Reexamination U.S. Appl. No. 95/001,337.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Decision Institution of Inter Partes Review, entered May 15, 2017.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, Decision Institution of Inter Partes Review, entered Jul. 21, 2017.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00668, Decision Institution of Inter Partes Review, entered Jul. 21, 2017.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-00577, Decision Institution of Inter Partes Review, entered Jul. 7, 2017.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-00577, Scheduling Order, entered Jul. 7, 2017.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-0549, Patent Owner's Response, filed Sep. 15, 2017.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-0549, Exhibit 2001 (Declaration of Professor Carl Sechen), filed Sep. 15, 2017.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-0549, Petitioners' Objections to Evidence, filed Sep. 15, 2017.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-0577, Exhibit 2003 (Declaration of R. Jacob Baker, Ph.D., P.E.), filed Oct. 25, 2017.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-0577, Exhibit 2004 (Deposition of Harold S. Stone, Ph.D.), filed Oct. 25, 2017.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-0577, Exhibit 2005 (Memory Systems: Cache,DRAM, Disk), filed Oct. 25, 2017.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-0577, Exhibit 2006 (PC2100 and PC1600 DDR SDRAM Registered DIMM, Design Specification, Revision 1.3, Jan. 2002), filed Oct. 25, 2017.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-0577, Exhibit 2007 (DRAM Circuit Design: Fundamental and High-Speed Topics), filed Oct. 25, 2017.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-0577, Patent Owner's Response, filed Oct. 25, 2017.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-0577, Petitioners' Objections to Evidence, filed Oct. 31, 2017.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Petitioner's reply to Patent Owner's Response, filed Dec. 15, 2017.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Deposition Transcript of Carl Sechen, filed Dec. 15, 2017.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Supplemental Declaration of Harold S. Stone, filed Dec. 15, 2017.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Xilinx CoolRunner XPLA3 CPLD product specification (2000), filed Dec. 15, 201.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Exhibit 2003, 'Synchronous DRAM Architectures, Organization, and Alternative Technologies,' filed Jan. 18, 2018.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Xilinx Programmable Logic Design Quick Start Handbook (2004), filed Dec. 15, 2017.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Xilinx Xilinx TQFP package datasheet (2000), filed Dec. 15, 2017.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Xilinx Xilinx VQFP package datasheet (2002), filed Dec. 15, 2017.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Petitioner's Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed Jan. 9, 2018.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Patent Owner's Motion for Observations, filed Jan. 9, 2018.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Exhibit 2004, filed Jan. 9, 2018.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Petitioner's Response to Patent Owners Motion for Observations, filed Jan. 23, 2018.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Patent Owner's Opposition to Petitioner's Motion to Exclude, filed Jan. 23, 2018.

(56) **References Cited**

OTHER PUBLICATIONS

Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Petitioner's Reply in Support of Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed Jan. 30, 2018.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Petitioner's Updated Exhibit List, filed Feb. 9, 2018.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Patent Owner's Updated Exhibit List, filed Feb. 9, 2018.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Exhibit 2005, filed Feb. 9, 2018.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Hearing Transcript, filed Feb. 14, 2018.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Final Written Decision, filed Feb. 14, 2018.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-00577, Petitioners' Reply to Patent Owner's Response, filed Feb. 6, 2018.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-00577, Oral Testimony of R. Jacob Baker in Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (May 11, 2017), filed Feb. 6, 2018.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing Fast components and Slow components, filed Feb. 6, 2018.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing 4:1 MUX/DeMUX and 4 ranks of memory, filed Feb. 6, 2018.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing 4:1 MUX/DeMUX and 4 ranks of memory (corrected Ex. 1035), filed Feb. 6, 2018.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-00577, Excerpts from Brent Keeth and R. Jacob Baker, Dram Circuit Design: A Tutorial (IEEE Press 2001), filed Feb. 6, 2018.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-00577, Patent Owner's Motion to Exclude, filed Feb. 28, 2018.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-00577, Petitioner's Opposition to Patent Owner's Motion to Exclude, filed Mar. 14, 2018.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-00577, Patent Owner's Reply to Opposition to Motion to Exclude, filed Mar. 21, 2018.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-00577, Hearing Transcript, filed Apr. 6, 2018.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-00577, Termination Decision Document, filed Jul. 7, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, Petitioner's Objections to Evidence, filed Nov. 14, 2017.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, Petitioner's Supplemental Objections to Evidence, filed Nov. 14, 2017.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, Petitioner's Reply to Patent Owner's Response, filed Feb. 26, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, *Google, Inc. et al.* v. *Netlist, Inc.*, Appeal 2014-00777, filed Feb. 26, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, Patent Owner's Submission on Propriety of Petitioners Reply, filed Mar. 20, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, Petitioner's Response to Patent Owner's Submission on Propriety of Petitioner's Reply and Supplemental Stone Declaration 1, filed Mar. 27, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, Petitioner's Response to Patent Owner's Motion for Observations, filed Apr. 2, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537B2, Case No. IPR2017-00668, Petitioner's Reply to Patent Owner's Response, filed Feb. 26, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537B2, Case No. IPR2017-00668, Patent Owner's Opposition to Petitioner's Motion to Exclude, filed Apr. 2, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537B2, Case No. IPR2017-00668, Petitioner's Reply in Support of its Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed Apr. 9, 2018.
Inter Partes Review Owner's Objections of to U.S. Pat. No. 7,532,537B2, Case No. IPR2017-00668, Patent Petitioner's Demonstratives, filed Apr. 20, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537B2, Case No. IPR2017-00668, Final Written Decision, filed Jul. 18, 2018.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Xilinx Xilinx CS280 package datasheet (1999), filed Dec. 15, 2017.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Petitioner's Demonstratives, filed Feb. 9, 2018.
Inter Partes Review of U.S. Pat. No. 8,756,364, Case No. IPR2017-00549, Patent Owner's Supplemental Mandatory Notices, filed Apr. 19, 2018.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-00577, Deposition Transcript of R. Jacob Baker (Jan. 12, 2018), filed Feb. 6, 2018.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-00577, Patent Owner's Objections to Evidence, filed Feb. 13, 2018.
Inter Partes Review of U.S. Pat. No. 8,516,185, Case No. IPR2017-00577, Patent Owner's Request for Oral Argument, filed Feb. 28, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, Deposition of Carl Sechen, Ph.D. taken Dec. 8, 2017, filed Feb. 26, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, Deposition of Carl Sechen, Ph.D. taken Feb. 8, 2018, filed Feb. 26, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, Patent Owner's Objections to Evidence, filed Mar. 5, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, Petitioner's Motion to Exclude, filed Mar. 19, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, Patent Owner's Motion for Observations, filed Mar. 19, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, Patent Owner's Request for Oral Argument, filed Mar. 19, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, Exhibit 2007, Deposition of Harold S. Stone, filed Mar. 19, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, Petitioner's Updated Mandatory Notices, filed Apr. 2, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, Petitioner's Reply in Support of its Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed Apr. 2, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, Patent Owner's Objection to Petitioner's Demonstratives, filed Apr. 20, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, Hearing Transcript, filed Apr. 24, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537, Case No. IPR2017-00667, Final Written Decision, filed Jul. 18, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537B2, Case No. IPR2017-00668, Petitioner's Objections to Evidence, filed Nov. 14, 2017.
Inter Partes Review of U.S. Pat. No. 7,532,537B2, Case No. IPR2017-00668, Notice of Deposition of Carl Sechen, filed Jan. 30, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537B2, Case No. IPR2017-00668, Petitioner's Supplemental Objections to Evidence, filed Feb. 15, 2018.

(56) **References Cited**

OTHER PUBLICATIONS

Inter Partes Review of U.S. Pat. No. 7,532,537B2, Case No. IPR2017-00668, Patent Owner's Objections to Evidence, filed Mar. 5, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537B2, Case No. IPR2017-00668, Patent Owner's Motion for Observations, filed Mar. 19, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537B2, Case No. IPR2017-00668, Patent Owner's Request for Oral Argument, filed Mar. 19, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537B2, Case No. IPR2017-00668, Patent Owner's Submission on Propriety of Petitioner's Reply, filed Mar. 20, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537B2, Case No. IPR2017-00668, Petitioner's Response to Patent Owner's Submission on Propriety of Petitioner's Reply and Supplemental Stone Declaration, filed Mar. 27, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537B2, Case No. IPR2017-00668, Petitioner's Response to Patent Owner's Motion for Observations, filed Apr. 2, 2018.
Inter Partes Review of U.S. Pat. No. 7,532,537B2, Case No. IPR2017-00668, Hearing Transcript, filed Apr. 24, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00363, Petition, filed Dec. 22, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00363, Patent Owner's Preliminary Response, filed Apr. 10, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00363, Decision Granting Institution of Inter Partes Review, entered Jun. 29, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00364, Petition, filed Dec. 27, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00364, Petitioner's Power of Attorney, filed Dec. 27, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00364, File History of U.S. Pat. No. 9606907, filed Dec. 27, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00364, Declaration of Dr. Harold Stone, filed Dec. 27, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00364, Curriculum Vitae of Dr. Harold Stone, filed Dec. 27, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00364, Patent Owner's Preliminary Response, filed May 7, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00364, Decision Granting Institution of Inter Partes Review, entered Aug. 6, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00365, Petition, filed Dec. 27, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00365, Patent Owner's Preliminary Response, filed Dec. 27, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00365, Decision Granting Institution of Inter Partes Review, entered Aug. 6, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Petition, filed Dec. 22, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Declaration of Dr. Harold Stone, filed Dec. 22, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1022, Decision Denying Institution of Inter Partes Review, entered Dec. 16, 2014.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1023, Decision Denying Institution of Inter Partes Review, entered Mar. 9, 2015.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1024, Excepts from the Hearing in Certain Memory Modules and Components Thereof, and Products Containing Same, filed May 8, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1025, Complainant Netlist, Inc., Initial Post-Hearing Brief, filed May 30, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1026, Respondents' Post-Hearing Brief, filed May 30, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1027, Demonstrative-Graphics-from-hynix-post-hearing-brief, filed Dec. 22, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1028, Netlist-reply-post-hearing-brief, filed Dec. 22, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1029, Respondent's Reply Post-Hearing Brief, filed Dec. 22, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1030, High-Quality Versions of Demonstrative-Graphics-from-hynix-reply-post-hearing-brief, filed Dec. 22, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1031, Institution of the '185 patent, filed Dec. 22, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1032, Final Written Decision, *Diablo Techs., Inc* v. *Netlist Inc.*, Paper No. 33, filed Dec. 22, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1033, Decision, *Netlist Inc.*, v. *Diablo Techs., Inc.*, filed Dec. 22, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1034, Netlist's Infringement Claim Chart of, filed Dec. 22, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1035, Stone, H.S. Microcomputer Interfacing, Reading, MA Addison Wesley, filed Dec. 22, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1039, Intel E7525 Memory Controller Hub (MCH) Chipset Datasheet, filed Dec. 22, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1040, Initial Determination, Certain Memory Modules and Components Thereof, and Products Containing Same, filed Dec. 22, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1041, Memory-Systems-Cache-DRAM-Disk, Bruce Jacobs et al., filed Dec. 22, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1042, Direct DRAM Datasheet, Bruce Jacobs et al., filed Dec. 22, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Notice of Accorded Filing Date, filed Jan. 10, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Patent Owner's Preliminary Response, filed Apr. 10, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Granting Institution of Inter Partes Review, entered Jun. 29, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Patent Owner's Objection to Petition Evidence, filed Jul. 16, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Order 37 C.F.R. 42.5, filed Aug. 2, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, Exhibit 3001, 'email from Mehran Arjomand,' filed Jul. 30, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, Exhibit 3001, 'email from Michael D. Hatcher,' filed Jul. 30, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibits 1044, 'Deposition Transcript of R. Jacob Baker (Jan. 26, 2019),' filed Feb. 11, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibits 1045, 'Deposition Transcript of R. Jacob Baker (Jan. 12, 2018) in IPR2017-00577 concerning the parent to the '907 Patent,' filed Feb. 11, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibits 1047, 'Certified translation of the Examination Decision issued by the State Intellectual Property Office of the P.R.C. (dated May 30, 2018),' filed Feb. 11, 2019.

(56) **References Cited**

OTHER PUBLICATIONS

Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Petitioners' Reply to Patent Owner's Response, filed Feb. 11, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibits 1043, 'Chart comparing text in Dr. Baker's declaration [Ex. 2002] with identical text in Patent Owner's Response [Paper No. 14],' filed Feb. 11, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibits 1046, 'Final Office Action concerning U.S. Appl. No. 15/470,856 (dated Jul. 27, 2018),' filed Feb. 11, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibits 1048, 'Certified translation of the Preliminary Opinion issued by the German Patent and Trademark Office (dated Jan. 8, 2019),' filed Feb. 11, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Petitioners' Request for Oral Argument, filed Feb. 19, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Patent Owner Objections to Reply Evidence, filed Feb. 19, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Patent Owner Request for Oral Argument, filed Feb. 19, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Patent Owner Motion to Exclude, filed Feb. 19, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Corrected Petitioners' Reply to Patent Owner's Response, filed Feb. 20, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Petitioners' Opposition to Patent Owner's Motion to Exclude, filed Mar. 5, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Patent Owner's Sur-Reply to Petitioner's Corrected Reply, filed Mar. 8, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Patent Owner's Reply to Petitioner's Opposition to Motion to Exclude, filed Mar. 12, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibits 3002, 'Patent Owner's Request for Sur Reply,' filed Mar. 1, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Order—Trial Hearing, filed Mar. 22, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00364 Exhibits 1043, 'Deposition Transcript of R. Jacob Baker (Feb. 9, 2019),' filed Feb. 22, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00363, Exhibits 1044, 'Declaration of R. Jacob Baker in IPR2017-00577 concerning the parent to the '907 Patent (Oct. 25, 2017),' filed Feb. 22, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00363, Exhibits 1045, 'Deposition Transcript of R. Jacob Baker in IPR2017-00577 concerning the parent to the '907 Patent (Jan. 12, 2018),' filed Feb. 22, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00363, Exhibits 1046, 'Final Written Decision in IPR2017-00577 invalidating all challenged claims to the parent to the '907 Patent (Jul. 5, 2018),' filed Feb. 22, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00363, Exhibits 1048, 'U.S. Pat. No. 7,133,960,' filed Feb. 22, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00363, Petitioners' Reply to Patent Owner's Response, filed Feb. 22, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00363, Patent Owner's Objections to Reply Evidence, filed Mar. 1, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00363, Petitioners' Request for Oral Argument, filed Mar. 4, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00363, Patent Owner's Request for Oral Argument, filed Mar. 4, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00363, Patent Owner's Motion to Exclude, filed Mar. 4, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00363, Petitioners' Opposition to Patent Owner's Motion to Exclude, filed Mar. 11, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00363, Patent Owner's Sur-Reply to Petitioner's Reply, filed Mar. 15, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00363, Patent Owner's Reply to Petitioner's Opposition to Motion to Exclude, filed Mar. 18, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00363, Order, Trial Hearing, filed Mar. 1, 2019.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1003: Declaration of Dr. Harold Stone, filed Dec. 22, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Patent Owner's Supplemental Mandatory Notices, filed Sep. 17, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 2003: Deposition of Harold S. Stone, Ph. D, Oct. 5, 2018, filed Oct. 19, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 2004: United States International Trade Commission, Inv. No. 337-TA-1089, Joint List of Claim Terms for Construction and Proposed Constructions, filed Oct. 19, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 2002: Declaration of R. Jacob Baker, Ph.D, P.E., filed Oct. 19, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 2005: United States International Trade Commission, Inv. No. 337-TA-1089, Order No. 17: Construing Terms of the Asserted Patents, filed Oct. 19, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Patent Owner's Response, filed Oct. 19, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Exhibit 1011: JEDEC Standard DDR2 SDRAM Specification, JESD79-2B (Jan. 2005), filed Dec. 27, 2017.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00364, Patent Owner's Objections to Petition Evidence, filed Aug. 21, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00364, Patent Owner's Supplemental Mandatory Notices, filed Sep. 17, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00364, Patent Owner's Response, filed Nov. 16, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00364, Exhibit 2001: Annotated Fig. 4 of U.S. Pat. No. 7,024,518—Halbert, filed Nov. 16, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00364, Exhibit 2002: Declaration of R. Jacob Baker, Ph.D, P.E., filed Nov. 16, 2018.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Paper 29, 'Termination Decision Document,' filed Jun. 27, 2019, 94 pgs.
Inter Partes Review of U.S. Pat. No. 9,606,907, Case No. IPR2018-00362, Paper 30, 'Record of Oral Hearing,' filed Jun. 27, 2019, 131 pgs.

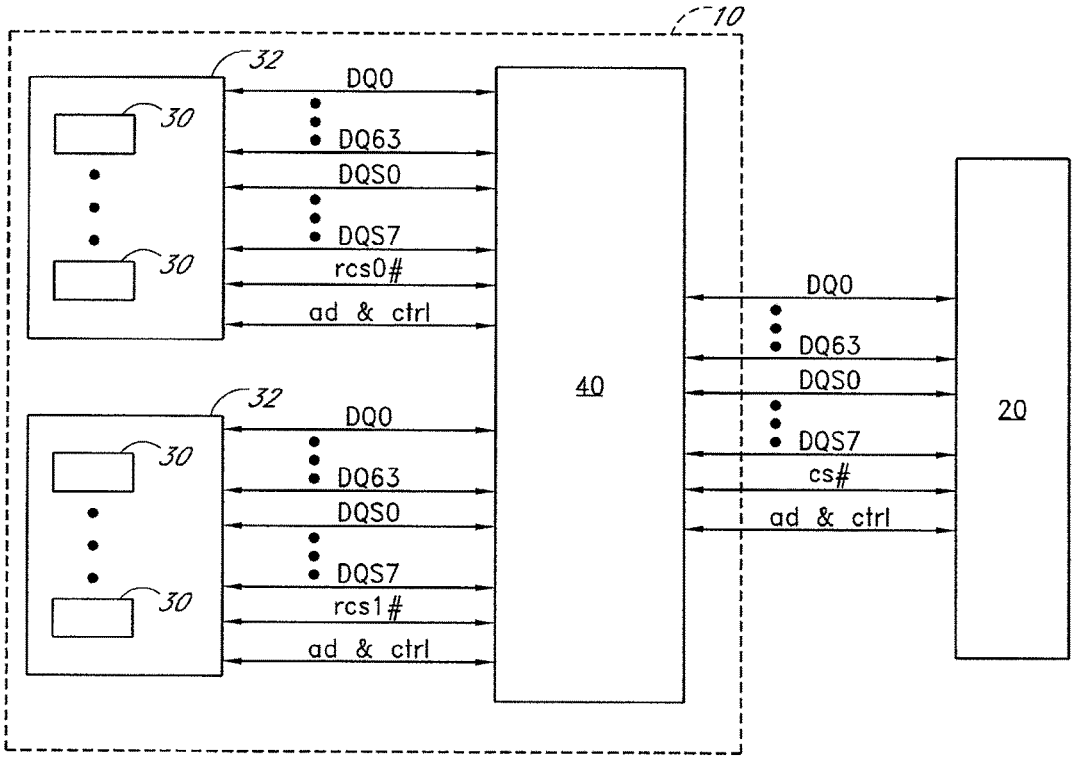

10
32
30
30
DQ0
DQ63
DQS0
DQS7
rcs0#
ad & ctrl
32
30
30
DQ0
DQ63
DQS0
DQS7
rcs1#
ad & ctrl
40
DQ0
DQ63
DQS0
DQS7
cs#
ad & ctrl
20

FIG. 1

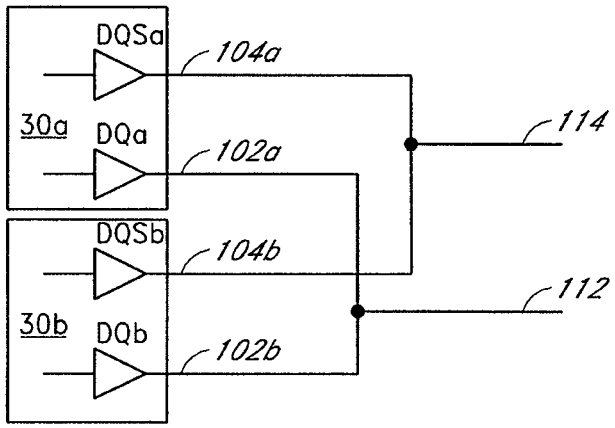


FIG. 2

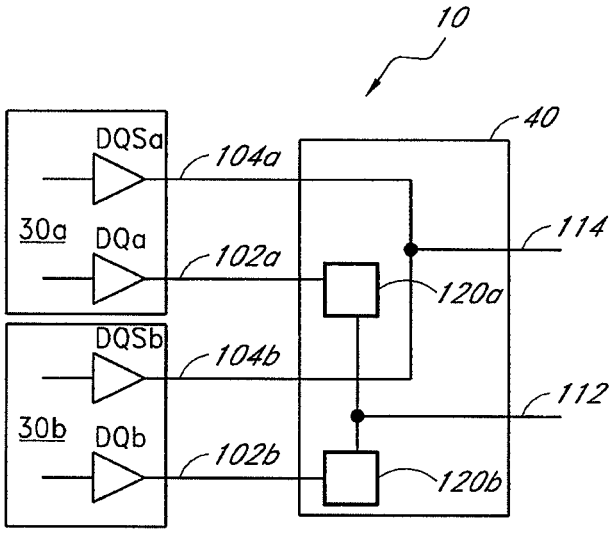

10
40
DQSa
104a
30a
DQa
102a
114
120a
DQSb
104b
112
30b
DQb
102b
120b

FIG. 3A

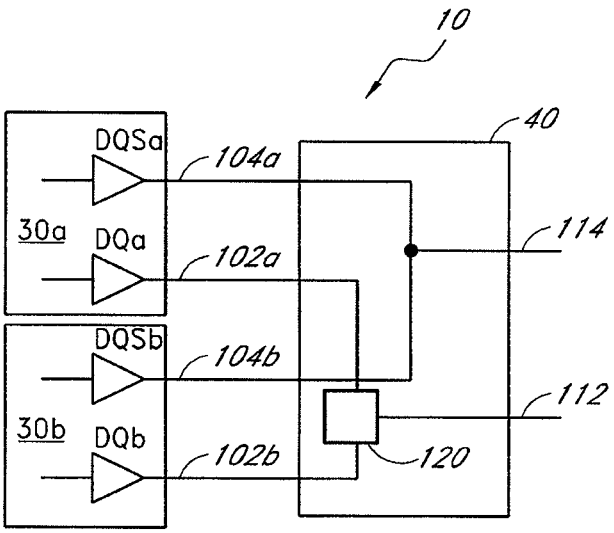

10
40
DQSa
104a
30a
DQa
102a
114
DQSb
104b
112
30b
DQb
102b
120

FIG. 3B

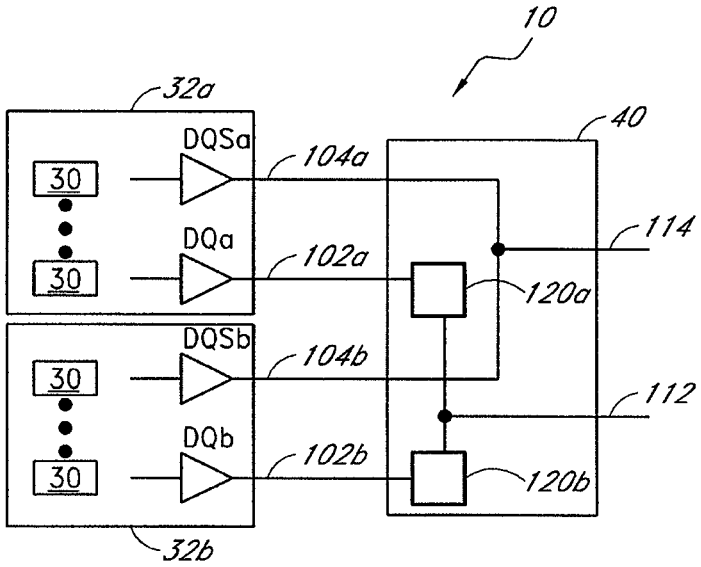

10
32a
40
DQSa
104a
30
DQa
102a
114
30
120a
DQSb
104b
30
112
DQb
102b
30
120b
32b

FIG. 4A

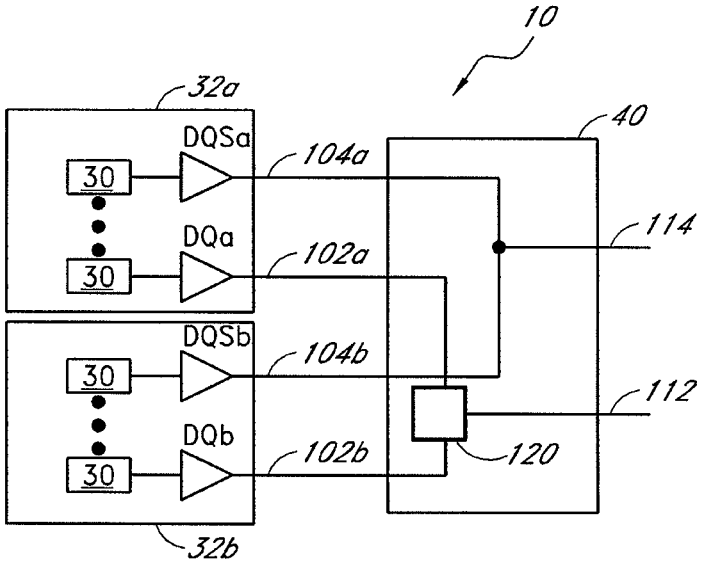

10
32a
40
DQSa
104a
30
DQa
102a
114
30
DQSb
104b
30
112
DQb
102b
30
120
32b

FIG. 4B

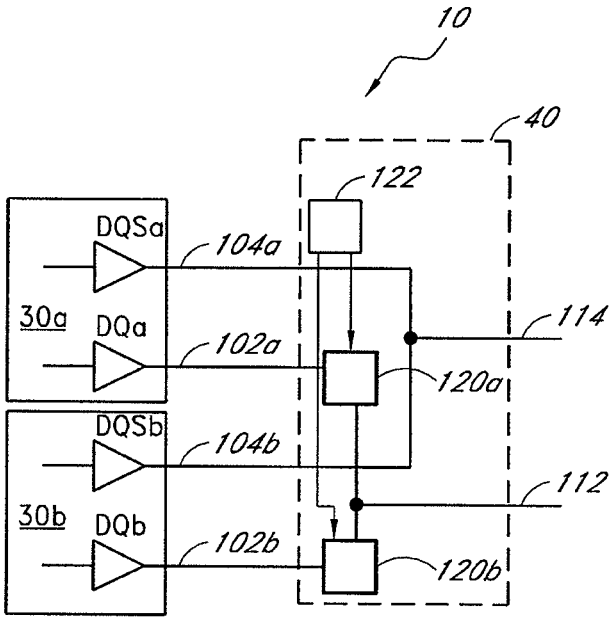

10
40
122
DQSa
104a
30a
DQa
102a
114
120a
DQSb
104b
112
30b
DQb
102b
120b

FIG. 5A

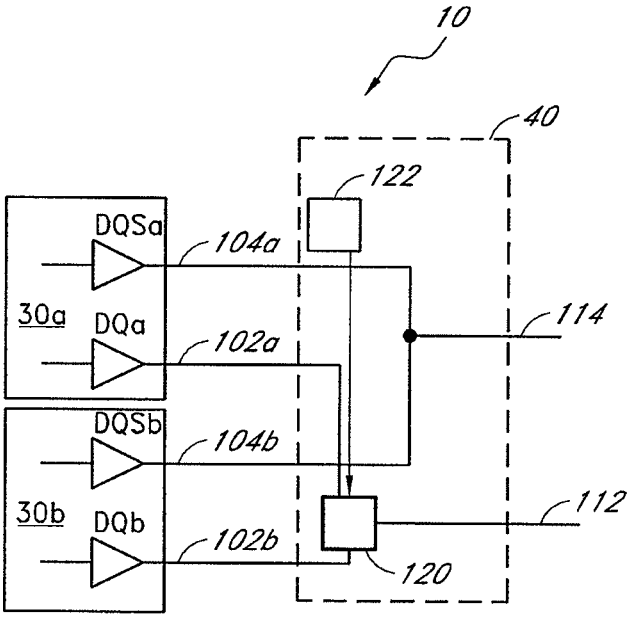

10
40
122
DQSa
104a
30a
DQa
102a
114
DQSb
104b
112
30b
DQb
102b
120

FIG. 5B

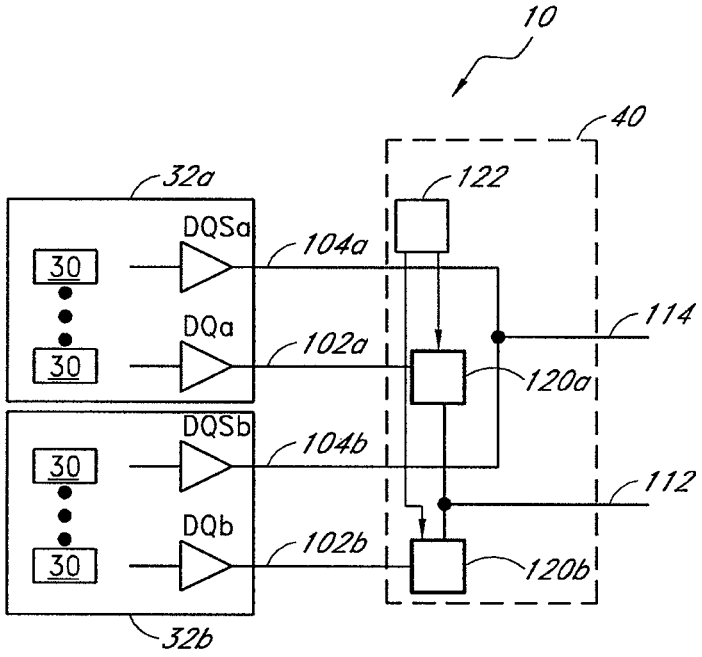

10
40
32a
122
DQSa
104a
30
DQa
102a
114
30
120a
DQSb
104b
30
112
DQb
102b
30
120b
32b

FIG. 5C

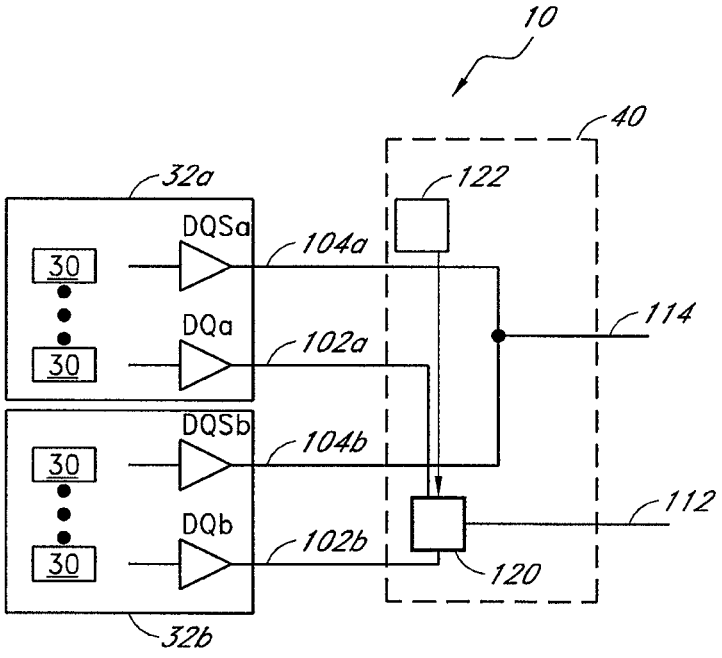

10
40
32a
122
DQSa
104a
30
DQa
102a
114
30
DQSb
104b
30
112
DQb
102b
30
120
32b

FIG. 5D

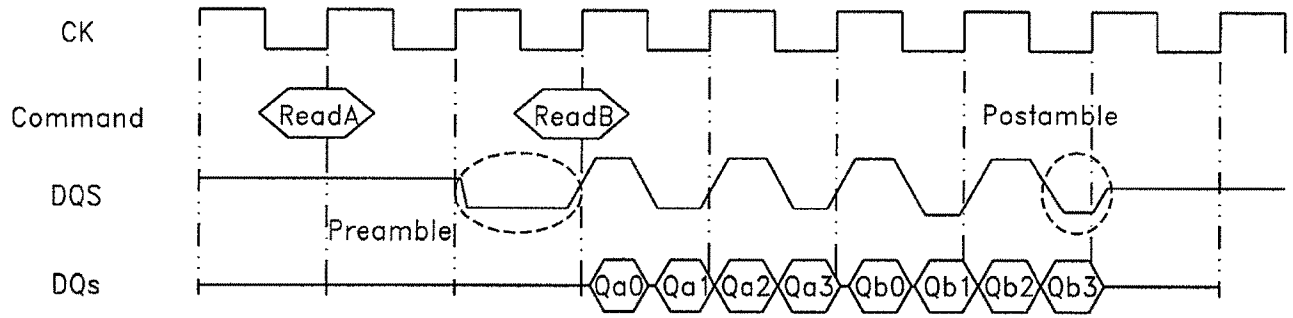

CK
Command
DQS
DQs
ReadA
ReadB
Postamble
Preamble
Qa0
Qa1
Qa2
Qa3
Qb0
Qb1
Qb2
Qb3

FIG. 6A

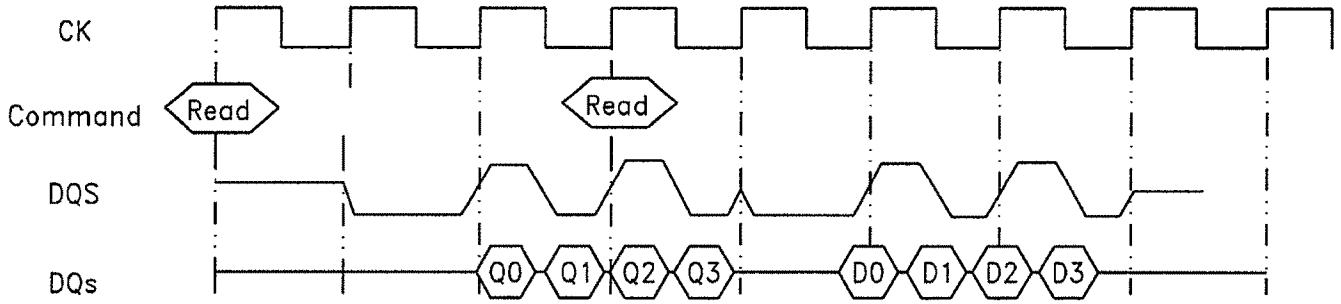

CK
Command
DQS
DQs
Read
Read
Q0
Q1
Q2
Q3
D0
D1
D2
D3

FIG. 6B

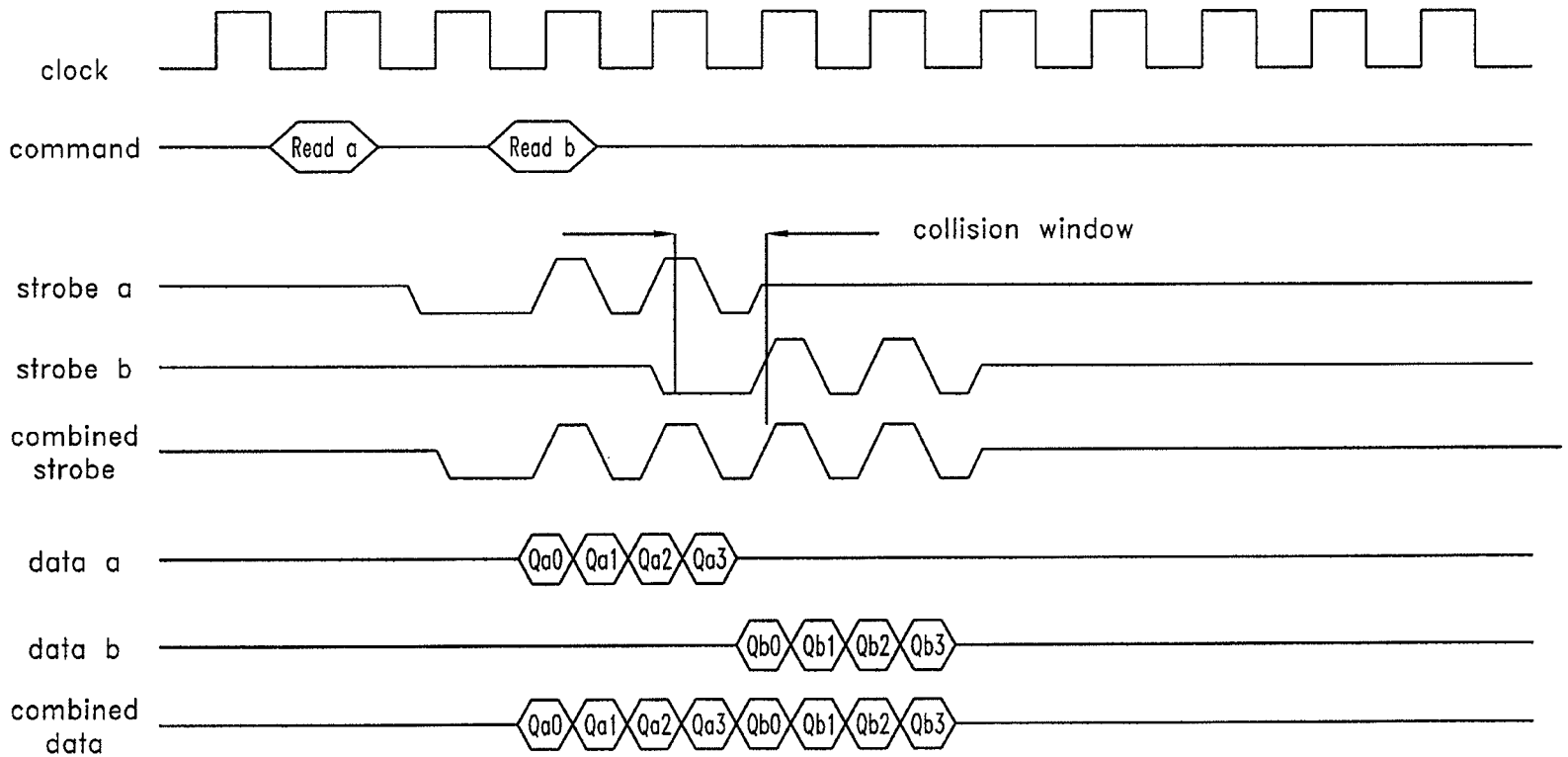

clock
command
Read a
Read b
collision window
strobe a
strobe b
combined strobe
data a
Qa0
Qa1
Qa2
Qa3
data b
Qb0
Qb1
Qb2
Qb3
combined data
Qa0
Qa1
Qa2
Qa3
Qb0
Qb1
Qb2
Qb3

FIG. 7

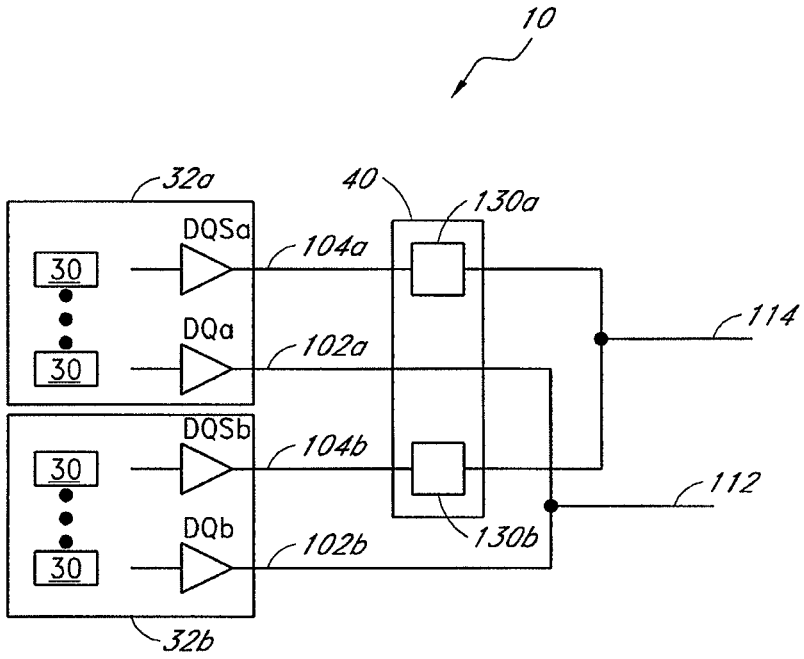

10
32a
40
130a
DQSa
104a
30
30
DQa
102a
114
DQSb
104b
30
30
112
DQb
102b
130b
32b

FIG. 8A

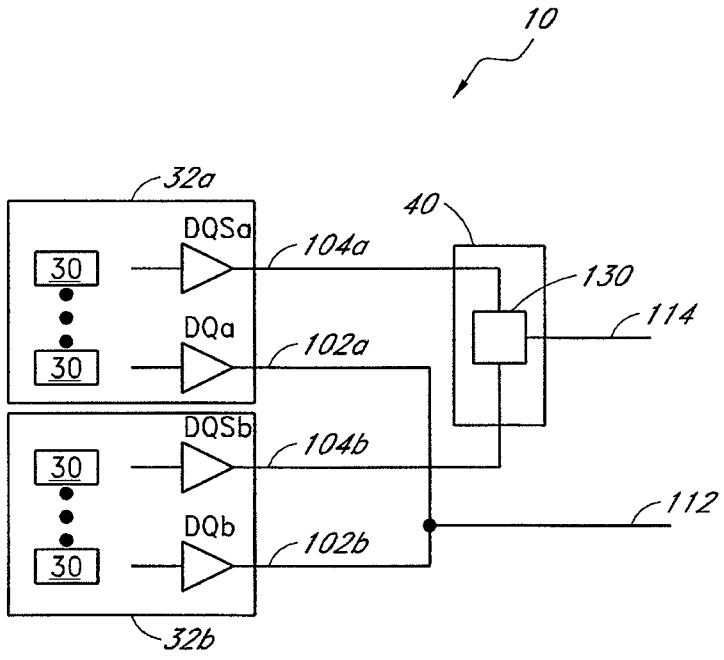

10
32a
40
DQSa
104a
30
30
130
114
DQa
102a
DQSb
104b
30
30
112
DQb
102b
32b

FIG. 8B

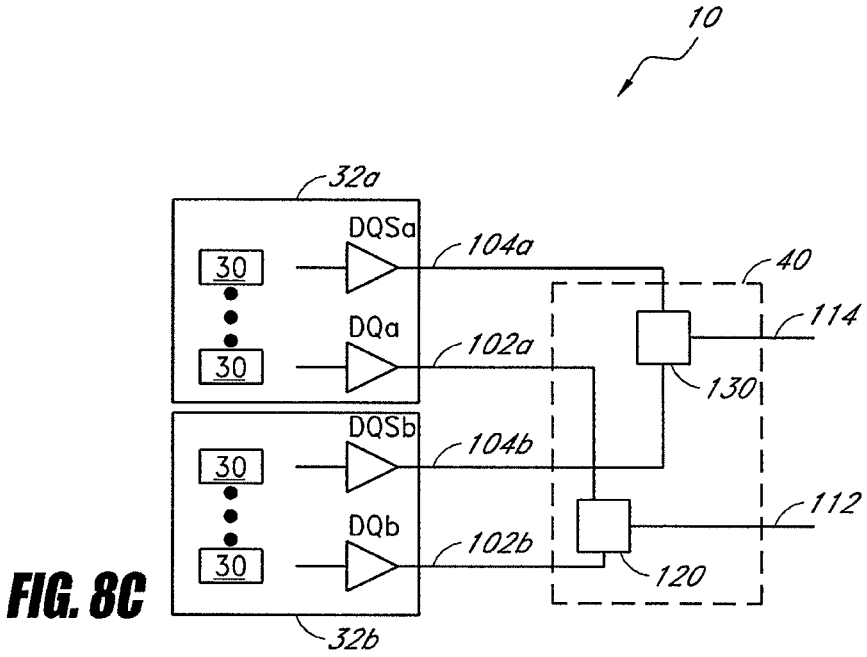

10
32a
DQSa
104a
30
30
DQa
102a
40
114
130
DQSb
104b
30
30
DQb
102b
112
120
32b

FIG. 8C

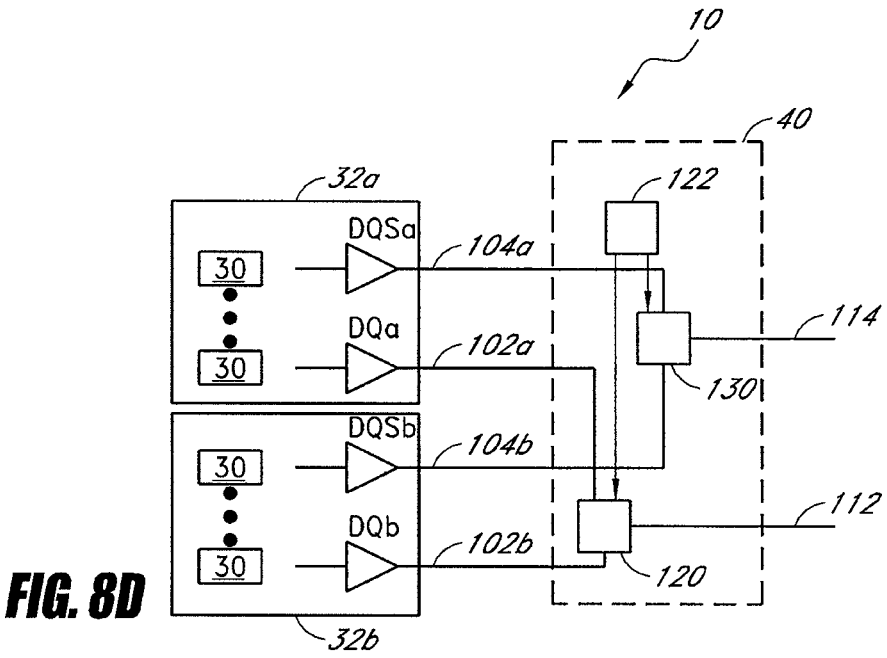

10
40
32a
122
DQSa
104a
30
30
DQa
102a
114
130
DQSb
104b
30
30
DQb
102b
112
120
32b

FIG. 8D

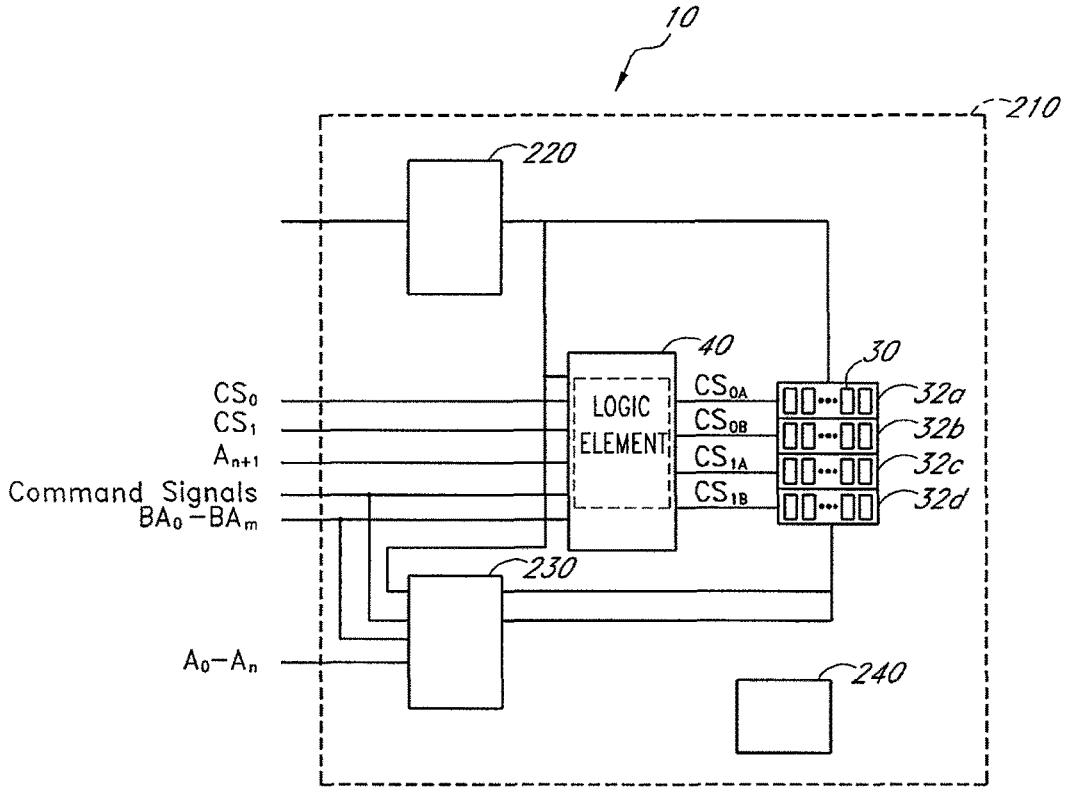

10
210
220
40
30
LOGIC ELEMENT
CS_0
CS_1
A_{n+1}
Command Signals
BA_0-BA_m
CS_{0A}
CS_{0B}
CS_{1A}
CS_{1B}
32a
32b
32c
32d
230
A_0-A_n
240

FIG. 9A

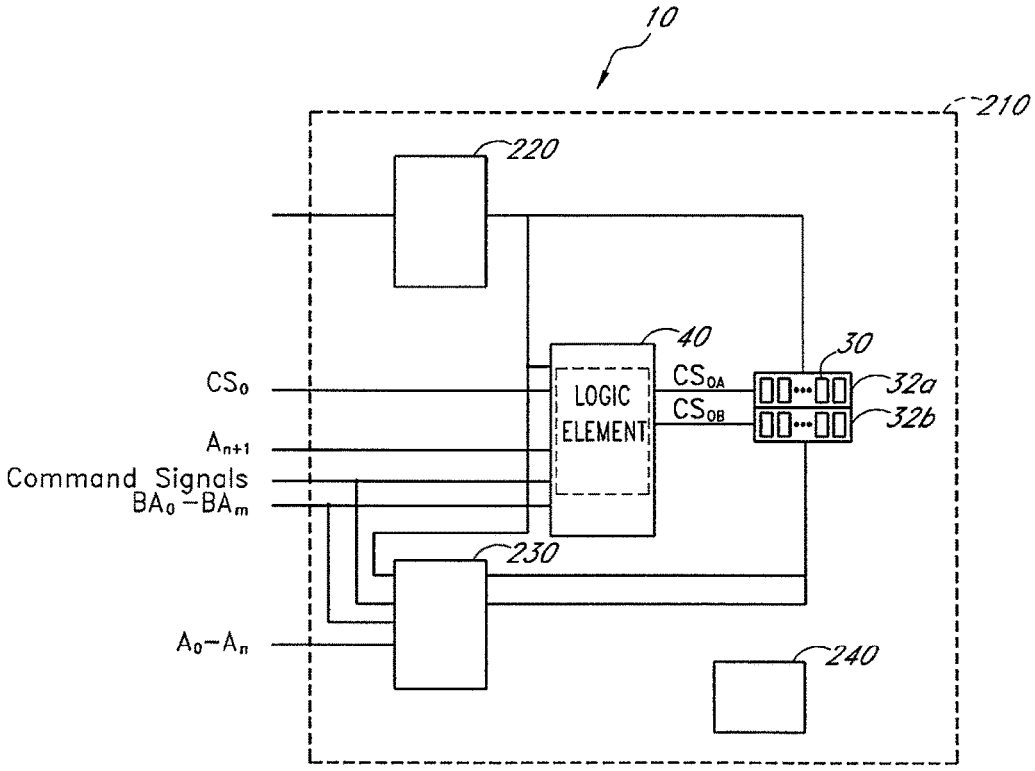

10
210
220
40
30
LOGIC ELEMENT
CS_0
A_{n+1}
Command Signals
BA_0-BA_m
CS_{0A}
CS_{0B}
32a
32b
230
A_0-A_n
240

FIG. 9B

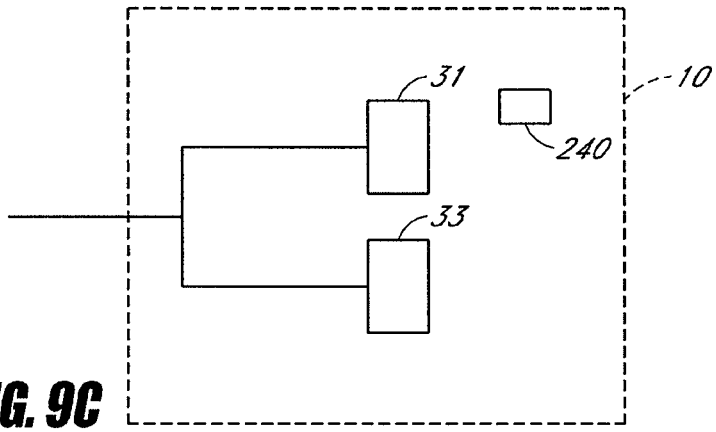


FIG. 9C

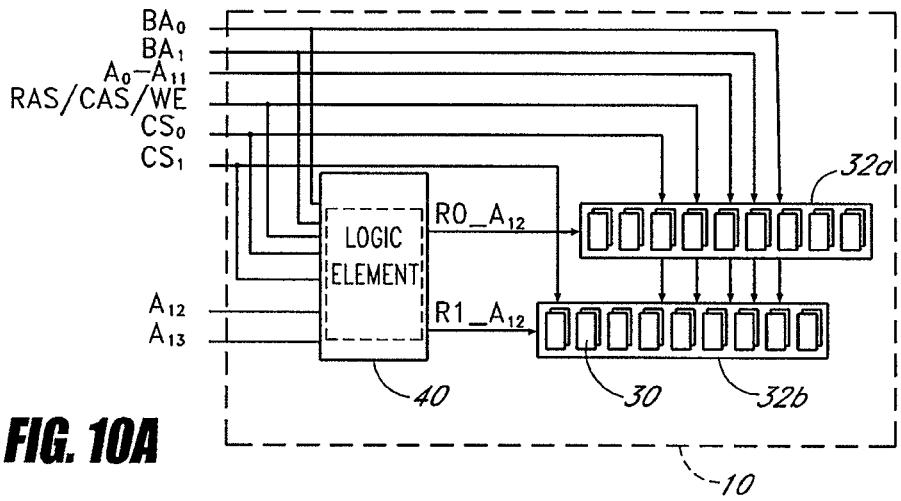


FIG. 10A

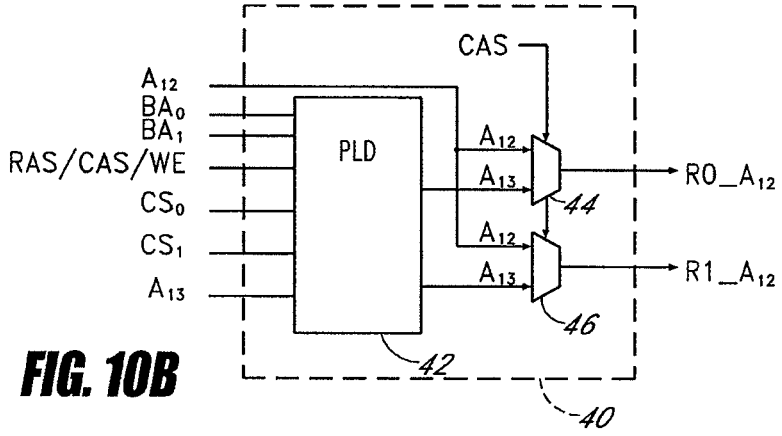


FIG. 10B

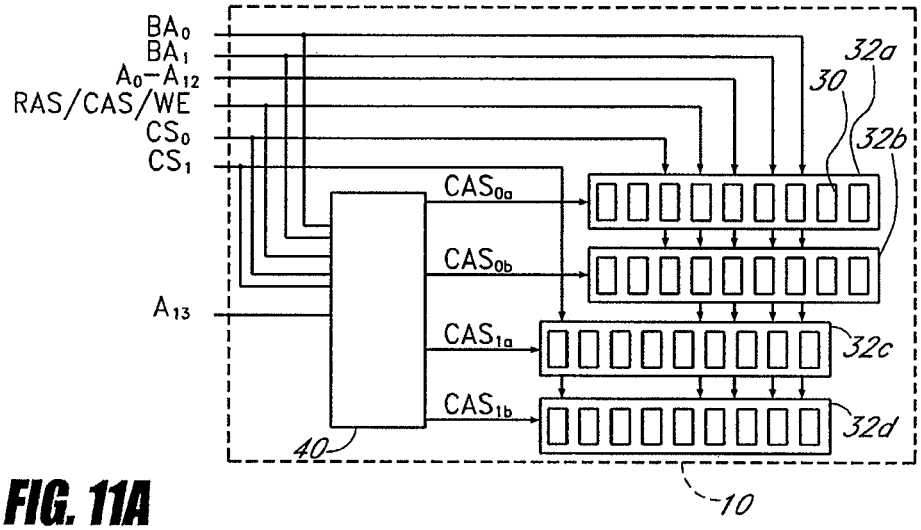


FIG. 11A

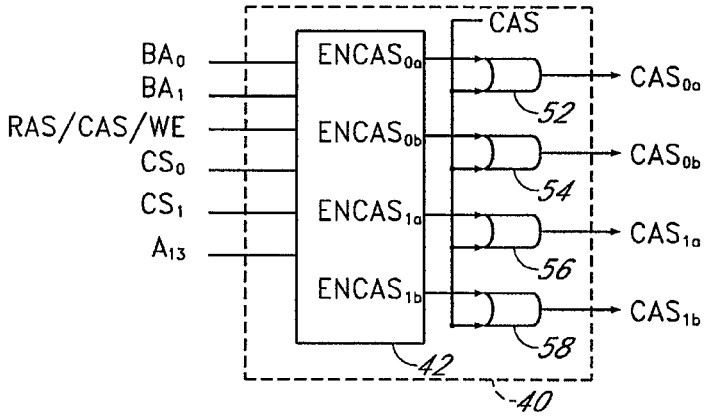


FIG. 11B

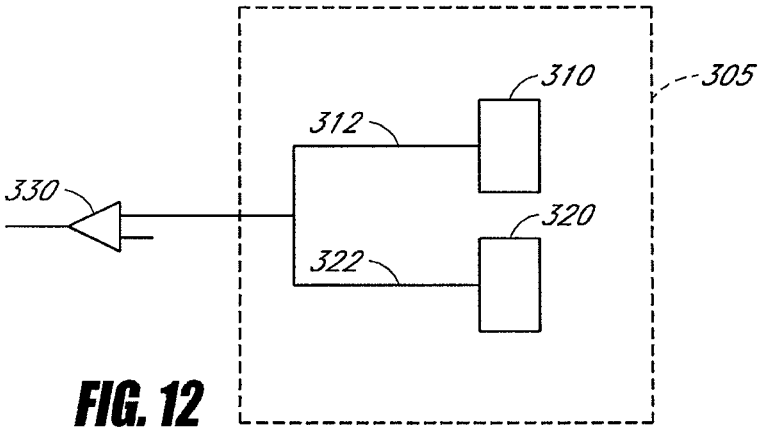


FIG. 12

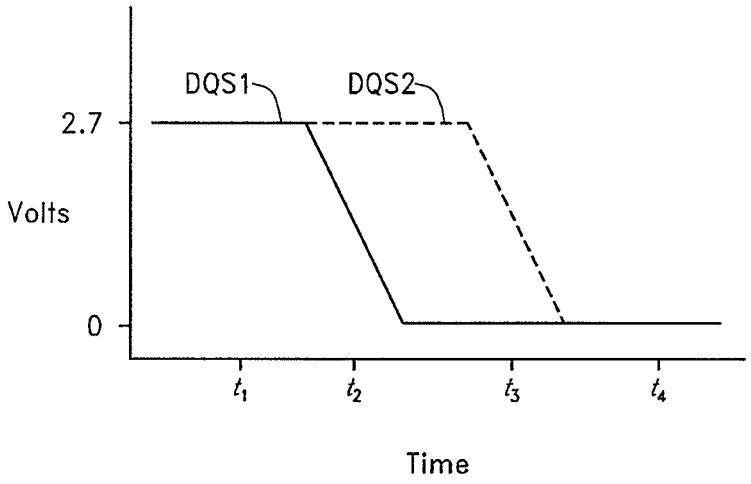


FIG. 13

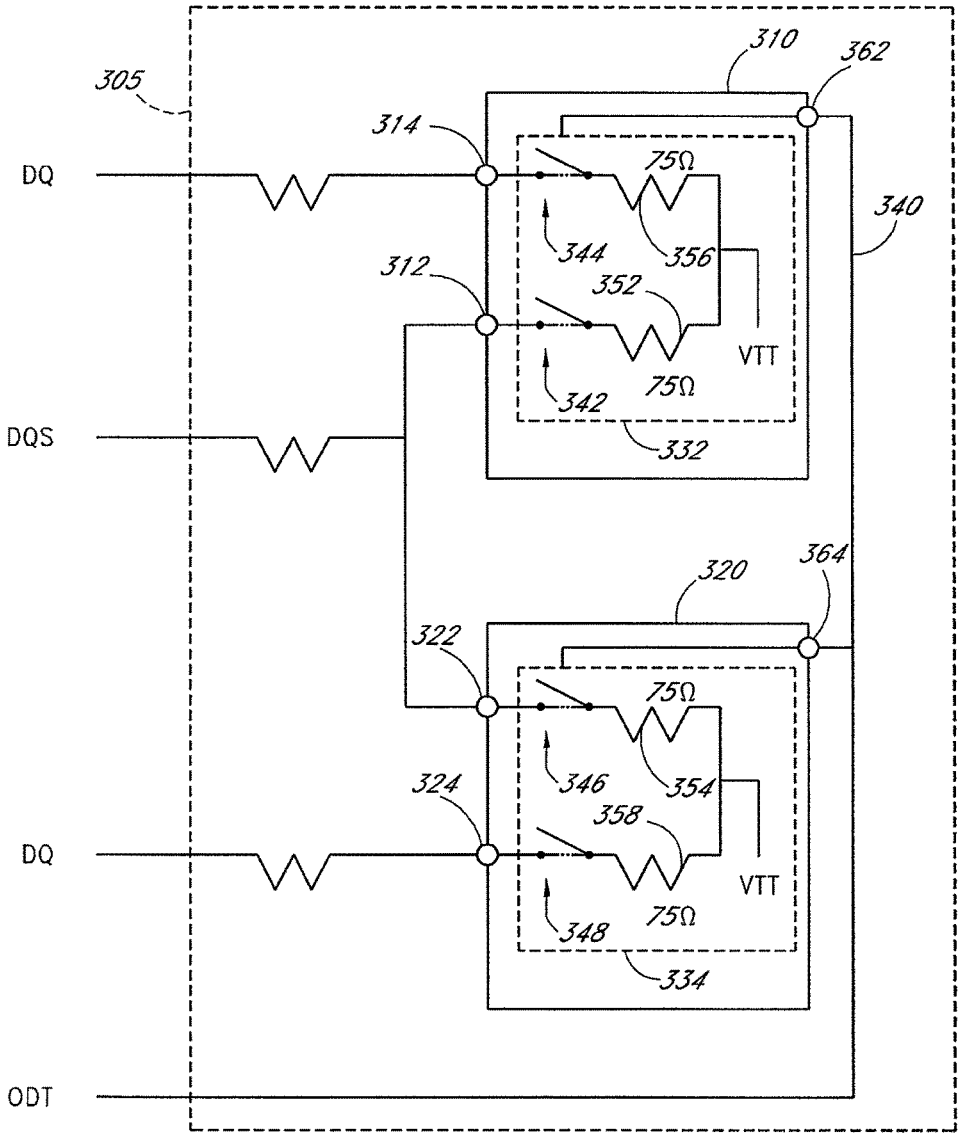

305
310
362
314
75Ω
DQ
340
344
356
312
352
VTT
75Ω
342
DQS
332
320
364
322
75Ω
346
354
324
358
DQ
VTT
75Ω
348
334
ODT

FIG. 14

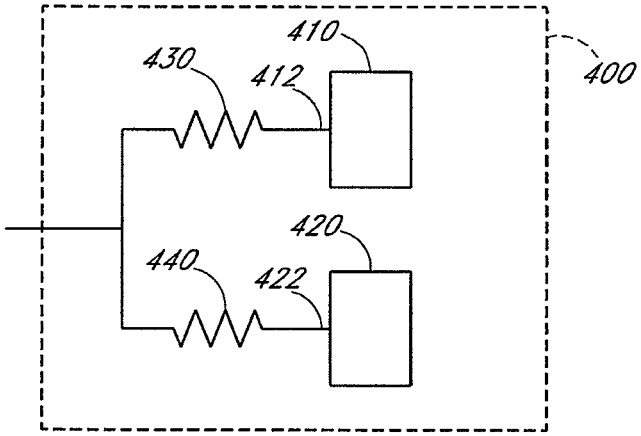


FIG. 15

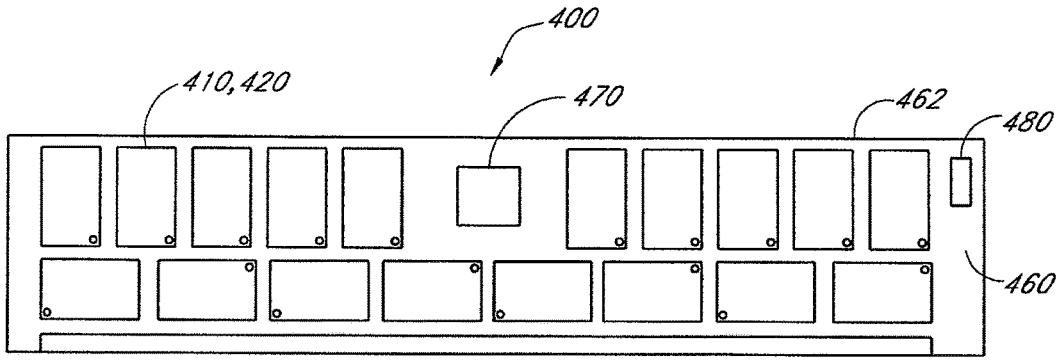


FIG. 16A

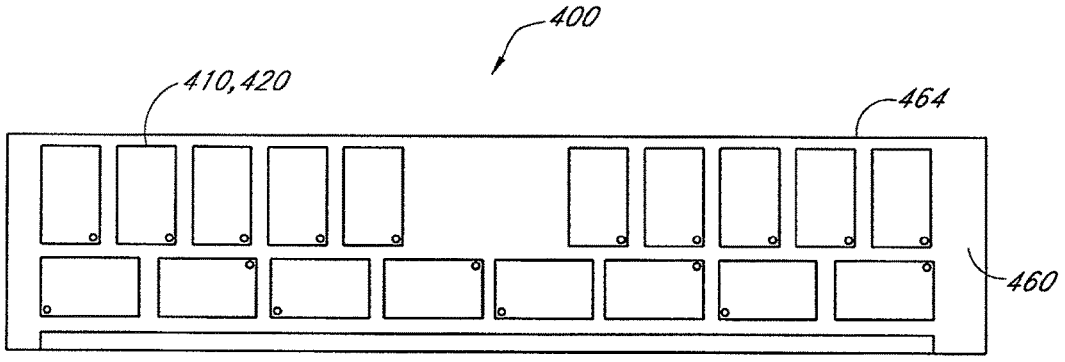


FIG. 16B

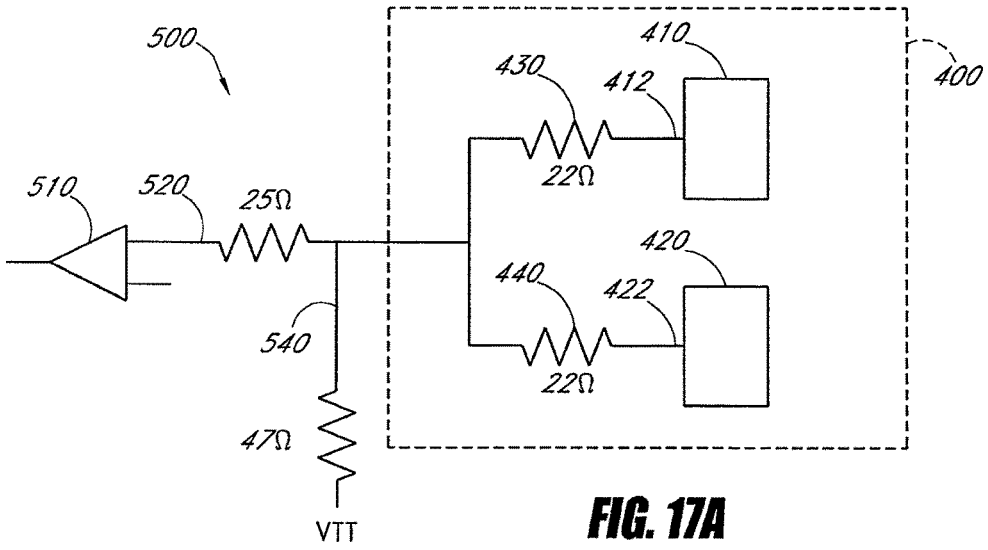


FIG. 17A

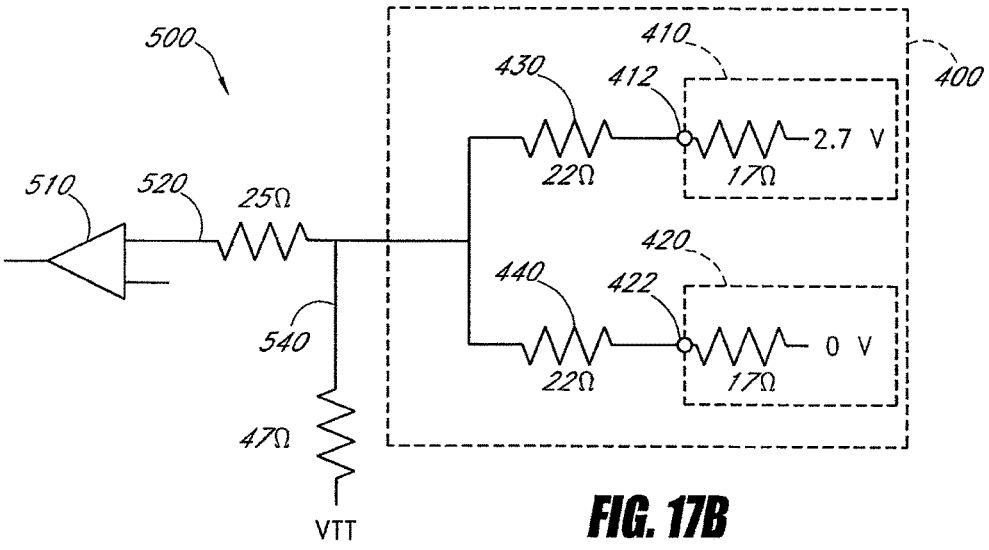


FIG. 17B

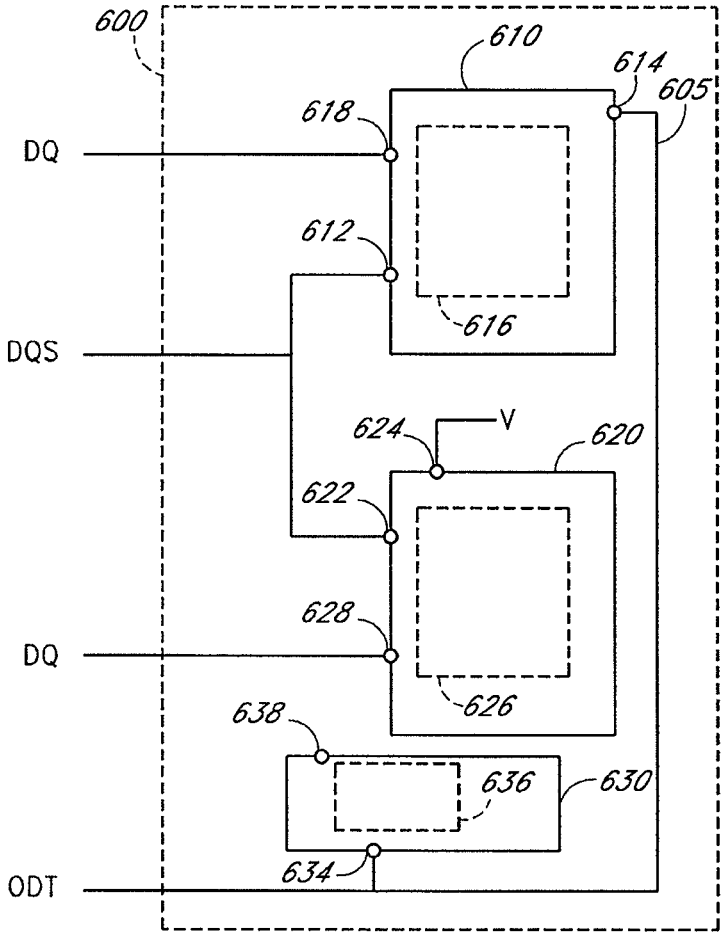

600
610
614
605
618
DQ
612
616
DQS
624
V
620
622
628
DQ
626
638
636
630
634
ODT

FIG. 18

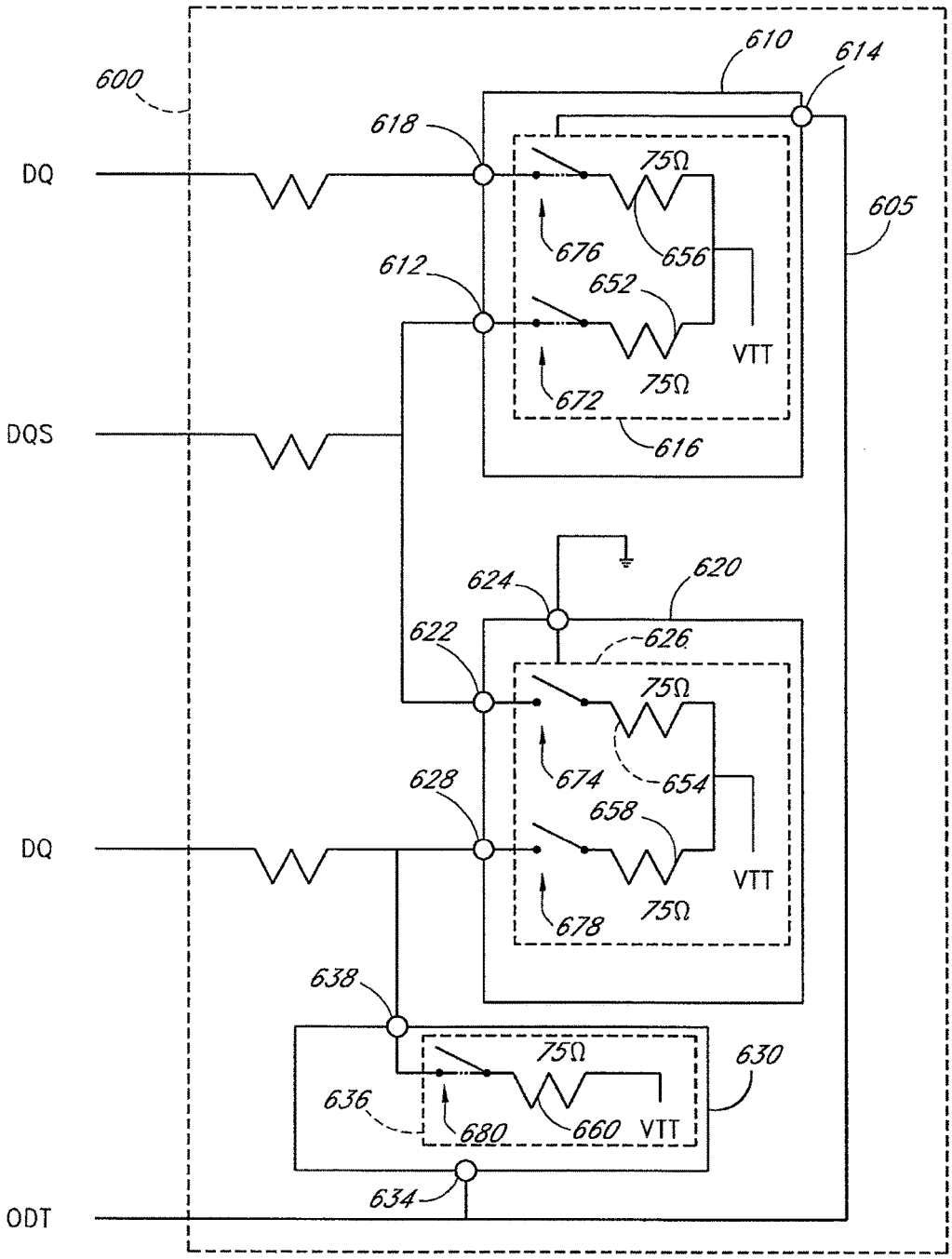

600
610
614
618
DQ
75Ω
605
676
656
612
652
VTT
672
75Ω
DQS
616
624
620
622
626
75Ω
674
654
628
658
DQ
VTT
678
75Ω
638
75Ω
630
636
680
660
VTT
634
ODT

FIG. 19

MEMORY MODULE WITH DATA BUFFERING

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a continuation of U.S. patent application Ser. No. 14/715,486, filed May 18, 2015, to be issued as U.S. Pat. No. 9,858,215 on Jan. 2, 2018, which is a continuation of U.S. patent application Ser. No. 13/971,231, filed Aug. 20, 2013, now U.S. Pat. No. 9,037,774, which is a continuation of U.S. patent application Ser. No. 13/287,081, filed Nov. 1, 2011, now U.S. Pat. No. 8,516,188, which is a continuation of U.S. patent application Ser. No. 13/032,470, filed Feb. 22, 2011, now U.S. Pat. No. 8,081,536, which is a continuation of U.S. patent application Ser. No. 12/955,711, filed Nov. 29, 2010, now U.S. Pat. No. 7,916,574, which is a continuation of U.S. patent application Ser. No. 12/629,827, filed Dec. 2, 2009, now U.S. Pat. No. 7,881,150, which is a continuation of U.S. patent application Ser. No. 12/408,652, filed Mar. 20, 2009, now U.S. Pat. No. 7,636,274, which is a continuation of U.S. patent application Ser. No. 11/335,875, filed Jan. 19, 2006, now U.S. Pat. No. 7,532,537, which claims the benefit of U.S. Provisional Appl. No. 60/645,087, filed Jan. 19, 2005 and which is a continuation-in-part of U.S. patent application Ser. No. 11/173,175, filed Jul. 1, 2005, now U.S. Pat. No. 7,289,386, which claims the benefit of U.S. Provisional Appl. No. 60/588,244, filed Jul. 15, 2004 and which is a continuation-in-part of U.S. patent application Ser. No. 11/075,395, filed Mar. 7, 2005, now U.S. Pat. No. 7,286,436, which claims the benefit of U.S. Provisional Appl. No. 60/550,668, filed Mar. 5, 2004, U.S. Provisional Appl. No. 60/575,595, filed May 28, 2004, and U.S. Provisional Appl. No. 60/590,038, filed Jul. 21, 2004, U.S. patent application Ser. Nos. 13/287,081, 13/032,470, 12/955,711, 12/629,827, 12/408,652, 11/335,875, 11/173,175, and 11/075,395, and U.S. Provisional Appl. Nos. 60/550,668, 60/575,595, 60/590,038, 60/588,244, and 60/645,087 are each incorporated in its entirety by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules.

2. Description of the Related Art

Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the processor of the computer system. Memory modules typically have a memory configuration with a unique combination of rows, columns, and banks which result in a total memory capacity for the memory module.

For example, a 512-Megabyte memory module (termed a "512-MB" memory module, which actually has 2^{29} or 536,870,912 bytes of capacity) will typically utilize eight 512-Megabit DRAM devices (each identified as a "512-Mb" DRAM device, each actually having 2^{29} or 536,870,912 bits of capacity). The memory cells (or memory locations) of each 512-Mb DRAM device can be arranged in four banks, with each bank having an array of 2^{24} (or 16,777,216) memory locations arranged as 2^{13} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 64 M 8-bit-wide memory locations (actually with four banks of 2^{27} or 134,217,728 one-bit memory cells arranged to provide a total of 2^{26} or 67,108,864 memory locations with 8 bits each) are identified as having a "64 Mb×8" or "64 M×8-bit" configuration, or as having a depth of 64 M and a bit width of 8. Furthermore, certain commercially-available 512-MB memory modules are termed to have a "64 M×8-byte" configuration or a "64 M×64-bit" configuration with a depth of 64 M and a width of 8 bytes or 64 bits.

Similarly, a 1-Gigabyte memory module (termed a "1-GB" memory module, which actually has 2^{30} or 1,073,741,824 bytes of capacity) can utilize eight 1-Gigabit DRAM devices (each identified as a "1-Gb" DRAM device, each actually having 2^{30} or 1,073,741,824 bits of capacity). The memory locations of each 1-Gb DRAM device can be arranged in four banks, with each bank having an array of memory locations with 2^{14} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 128 M 8-bit-wide memory locations (actually with a total of 2^{27} or 134,217,728 memory locations with 8 bits each) are identified as having a "128 Mb×8" or "128 M×8-bit" configuration, or as having a depth of 128 M and a bit width of 8. Furthermore, certain commercially-available 1-GB memory modules are identified as having a "128 M×8-byte" configuration or a "128 M×64-bit" configuration with a depth of 128 M and a width of 8 bytes or 64 bits.

The commercially-available 512-MB (64 M×8-byte) memory modules and the 1-GB (128 M×8-byte) memory modules described above are typically used in computer systems (e.g., personal computers) which perform graphics applications since such "×8" configurations are compatible with data mask capabilities often used in such graphics applications. Conversely, memory modules with "×4" configurations are typically used in computer systems such as servers which are not as graphics-intensive. Examples of such commercially available "×4" memory modules include, but are not limited to, 512-MB (128 M×4-byte) memory modules comprising eight 512-Mb (128 Mb×4) memory devices.

The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "×64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "×72" organization.

The memory capacity of a memory module increases with the number of memory devices. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks. For example, a memory module with four ranks has double the memory capacity of a memory module with two ranks and four times the memory capacity of a memory module with one rank. Rather than referring to the memory capacity of the memory module, in certain circumstances, the memory density of the memory module is referred to instead.

During operation, the ranks of a memory module are selected or activated by address and command signals that are received from the processor. Examples of such address and command signals include, but are not limited to, rank-

select signals, also called chip-select signals. Most computer and server systems support one-rank and two-rank memory modules. By only supporting one-rank and two-rank memory modules, the memory density that can be incorporated in each memory slot is limited.

Various aspects of the design of a memory module impose limitations on the size of the memory arrays of the memory module. Certain such aspects are particularly important for memory modules designed to operate at higher frequencies. Examples of such aspects include, but are not limited to, memory device (e.g., chip) densities, load fan-out, signal integrity, available rank selects, power dissipation, and thermal profiles.

SUMMARY OF THE INVENTION

In certain embodiments, a memory module is operable to communicate data with a memory controller via a data bus in response to memory commands received from the memory controller. The memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst. The memory module comprises a plurality of memory integrated circuits including at least one first memory integrated circuit and at least one second memory integrated circuit, and further comprises a buffer coupled between the at least one first memory integrated circuit and the data bus, and between the at least one second memory integrated circuit and the data bus. The buffer couples the at least one first memory integrated circuit to the data bus and isolates the at least one second memory integrated circuit from the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command. The buffer then couples the at least one second memory integrated circuit to the data bus and isolates the at least one first memory integrated circuit from the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command.

Certain embodiments provide a method of operating a memory module coupled to a memory controller via a memory bus that includes a control/address (C/A) bus and a data bus. The memory module comprises memory integrated circuits, including at least one first memory integrated circuit and at least one second memory integrated circuit. The method comprises receiving from the memory controller a first set of input C/A signals associated with a first memory command via the C/A bus, the first memory command to cause the memory module to receive or output a first data burst; generating a first set of output C/A signals in response to the first set of input C/A signals, the first set of output C/A signals causing the at least one first memory integrated circuit to receive or output the first data burst; receiving from the memory controller a second set of input control/address signals associated with a second memory command via the C/A bus, the second memory command to cause the memory module to receive or output a second data burst; generating a second set of output C/A signals in response to the second set of input C/A signals, the second set of output C/A signals causing the at least one second memory integrated circuit to receive or output the second data burst; coupling the at least one first memory integrated circuit to the data bus and isolating the at least one second memory integrated circuit from the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command; and coupling the at least one second memory integrated circuit to the data bus and isolating the at least one first memory integrated circuit from the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command.

In certain embodiments, a circuit is configured to be mounted on a memory module that is operable to communicate data with a memory controller via a data bus in response to memory commands received from the memory controller. The memory module including at least one first memory integrated circuit and at least one second memory integrated circuit. The memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the at least one first memory integrated circuit to receive or output a first data burst and the second memory command to cause the at least one second memory integrated circuit to receive or output a second data burst. The circuit comprises logic that couples the at least one first memory integrated circuit to the data bus and that isolates the at least one second memory integrated circuit from the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command. The logic then couples the at least one second memory integrated circuit to the data bus and isolates the at least one first memory integrated circuit from the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** schematically illustrates an example memory module in accordance with certain embodiments described herein.

FIG. **2** schematically illustrates a circuit diagram of two memory devices of a conventional memory module.

FIGS. **3**A and **3**B schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two memory devices from the computer system in accordance with certain embodiments described herein.

FIGS. **4**A and **4**B schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two ranks of memory devices from the computer system in accordance with certain embodiments described herein.

FIGS. **5**A-**5**D schematically illustrate example memory modules having a circuit comprising a logic element and one or more switches operatively coupled to the logic element in accordance with certain embodiments described herein.

FIG. **6**A shows an exemplary timing diagram of a gapless read burst for a back-to-back adjacent read condition from one memory device.

FIG. **6**B shows an exemplary timing diagram with an extra clock cycle between successive read commands issued to different memory devices for successive read accesses from different memory devices.

FIG. **7** shows an exemplary timing diagram in which the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b."

FIGS. **8**A-**8**D schematically illustrate circuit diagrams of example memory modules comprising a circuit which multiplexes the DQS data strobe signal lines from one another in accordance with certain embodiments described herein.

FIG. **9**A schematically illustrates an example memory module with four ranks of memory devices compatible with certain embodiments described herein.

FIG. **9**B schematically illustrates an example memory module with two ranks of memory devices compatible with certain embodiments described herein.

FIG. **9**C schematically illustrates another example memory module in accordance with certain embodiments described herein.

FIG. **10**A schematically illustrates an exemplary memory module which doubles the rank density in accordance with certain embodiments described herein.

FIG. **10**B schematically illustrates an exemplary circuit compatible with embodiments described herein.

FIG. **11**A schematically illustrates an exemplary memory module which doubles number of ranks in accordance with certain embodiments described herein.

FIG. **11**B schematically illustrates an exemplary circuit compatible with embodiments described herein.

FIG. **12** schematically illustrates an exemplary memory module in which a data strobe (DQS) pin of a first memory device is electrically connected to a DQS pin of a second memory device while both DQS pins are active.

FIG. **13** is an exemplary timing diagram of the voltages applied to the two DQS pins due to non-simultaneous switching.

FIG. **14** schematically illustrates another exemplary memory module in which a DQS pin of a first memory device is connected to a DQS pin of a second memory device.

FIG. **15** schematically illustrates an exemplary memory module in accordance with certain embodiments described herein.

FIGS. **16**A and **16**B schematically illustrate a first side and a second side, respectively, of a memory module with eighteen 64 M×4 bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board.

FIGS. **17**A and **17**B schematically illustrate an exemplary embodiment of a memory module in which a first resistor and a second resistor are used to reduce the current flow between the first DQS pin and the second DQS pin.

FIG. **18** schematically illustrates another exemplary memory module compatible with certain embodiments described herein.

FIG. **19** schematically illustrates a particular embodiment of the memory module schematically illustrated by FIG. **18**.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Load Isolation

FIG. **1** schematically illustrates an example memory module **10** compatible with certain embodiments described herein. The memory module **10** is connectable to a memory controller **20** of a computer system (not shown). The memory module **10** comprises a plurality of memory devices **30**, each memory device **30** having a corresponding load. The memory module **10** further comprises a circuit **40** electrically coupled to the plurality of memory devices **30** and configured to be electrically coupled to the memory controller **20** of the computer system. The circuit **40** selectively isolates one or more of the loads of the memory devices from the computer system. The circuit **40** comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module **10**.

As used herein, the term "load" is a broad term which includes, without limitation, electrical load, such as capacitive load, inductive load, or impedance load. As used herein, the term "isolation" is a broad term which includes, without limitation, electrical separation of one or more components from another component or from one another. As used herein, the term "circuit" is a broad term which includes, without limitation, an electrical component or device, or a configuration of electrical components or devices which are electrically or electromagnetically coupled together (e.g., integrated circuits), to perform specific functions.

Various types of memory modules **10** are compatible with embodiments described herein. For example, memory modules **10** having memory capacities of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, as well as other capacities, are compatible with embodiments described herein. Certain embodiments described herein are applicable to various frequencies including, but not limited to 100 MHz, 200 MHz, 400 MHz, 800 MHz, and above. In addition, memory modules **10** having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. In certain embodiments, the memory module **10** comprises a printed circuit board on which the memory devices **30** are mounted, a plurality of edge connectors configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, and a plurality of electrical conduits which electrically couple the memory devices **30** to the circuit **40** and which electrically couple the circuit **40** to the edge connectors. Furthermore, memory modules **10** compatible with embodiments described herein include, but are not limited to, single in-line memory modules (SIMMs), dual in-line memory modules (DIMMs), small-outline DIMMs (SO-DIMMs), unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), fully-buffered DIMM (FB-DIMM), rank-buffered DIMMs (RBDIMMs), mini-DIMMs, and micro-DIMMs.

Memory devices **30** compatible with embodiments described herein include, but are not limited to, random-access memory (RAM), dynamic random-access memory (DRAM), synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., SDR, DDR-1, DDR-2, DDR-3). In addition, memory devices **30** having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein. Memory devices **30** compatible with embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP). Memory devices **30** compatible with embodiments described herein are available from a number of sources, including but not limited to, Samsung Semiconductor, Inc. of San Jose, Calif., Infineon Technologies AG of San Jose, Calif., and Micron Technology, Inc. of Boise, Id. Persons skilled in the art can select appropriate memory devices **30** in accordance with certain embodiments described herein.

In certain embodiments, the plurality of memory devices **30** comprises a first number of memory devices **30**. In certain such embodiments, the circuit **40** selectively isolates a second number of the memory devices **30** from the computer system, with the second number less than the first number.

In certain embodiments, the plurality of memory devices **30** are arranged in a first number of ranks. For example, in certain embodiments, the memory devices **30** are arranged in

two ranks, as schematically illustrated by FIG. **1**. In other embodiments, the memory devices **30** are arranged in four ranks. Other numbers of ranks of the memory devices **30** are also compatible with embodiments described herein.

In certain embodiments, the circuit comprises a logic element selected from a group consisting of: a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, and a complex programmable-logic device (CPLD). In certain embodiments, the logic element of the circuit **40** is a custom device. Sources of logic elements compatible with embodiments described herein include, but are not limited to, Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif. In certain embodiments, the logic element comprises various discrete electrical elements, while in certain other embodiments, the logic element comprises one or more integrated circuits.

In certain embodiments, the circuit **40** further comprises one or more switches which are operatively coupled to the logic element to receive control signals from the logic element. Examples of switches compatible with certain embodiments described herein include, but are not limited to, field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex.

FIG. **2** schematically illustrates a circuit diagram of two memory devices **30***a*, **30***b* of a conventional memory module showing the interconnections between the DQ data signal lines **102***a*, **102***b* of the memory devices **30***a*, **30***b* and the DQS data strobe signal lines **104***a*, **104***b* of the memory devices **30***a*, **30***b*. Each of the memory devices **30***a*, **30***b* has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, however, for simplicity, FIG. **2** only illustrates a single DQ data signal line and a single DQS data strobe signal line for each memory device **30***a*, **30***b*. The DQ data signal lines **102***a*, **102***b* and the DQS data strobe signal lines **104***a*, **104***b* are typically conductive traces etched on the printed circuit board of the memory module. As shown in FIG. **2**, each of the memory devices **30***a*, **30***b* has their DQ data signal lines **102***a*, **102***b* electrically coupled to a common DQ line **112** and their DQS data strobe signal lines **104***a*, **104***b* electrically coupled to a common DQS line **114**. The common DQ line **112** and the common DQS line **114** are electrically coupled to the memory controller **20** of the computer system. Thus, the computer system is exposed to the loads of both memory devices **30***a*, **30***b* concurrently.

In certain embodiments, the circuit **40** selectively isolates the loads of at least some of the memory devices **30** from the computer system. The circuit **40** of certain embodiments is configured to present a significantly reduced load to the computer system. In certain embodiments in which the memory devices **30** are arranged in a plurality of ranks, the circuit **40** selectively isolates the loads of some (e.g., one or more) of the ranks of the memory module **10** from the computer system. In certain other embodiments, the circuit **40** selectively isolates the loads of all of the ranks of the memory module **10** from the computer system. For example, when a memory module **10** is not being accessed by the computer system, the capacitive load on the memory controller **20** of the computer system by the memory module **10** can be substantially reduced to the capacitive load of the circuit **40** of the memory module **10**.

As schematically illustrated by FIGS. **3**A and **3**B, an example memory module **10** compatible with certain embodiments described herein comprises a circuit **40** which selectively isolates one or both of the DQ data signal lines **102***a*, **102***b* of the two memory devices **30***a*, **30***b* from the common DQ data signal line **112** coupled to the computer system. Thus, the circuit **40** selectively allows a DQ data signal to be transmitted from the memory controller **20** of the computer system to one or both of the DQ data signal lines **102***a*, **102***b*. In addition, the circuit **40** selectively allows one of a first DQ data signal from the DQ data signal line **102***a* of the first memory device **30***a* or a second DQ data signal from the DQ data signal line **102***b* of the second memory device **30***b* to be transmitted to the memory controller **20** via the common DQ data signal line **112** (see, e.g., triangles on the DQ and DQS lines of FIGS. **3**A and **3**B which point towards the memory controller). While various figures of the present application denote read operations by use of DQ and DQS lines which have triangles pointing towards the memory controller, certain embodiments described herein are also compatible with write operations (e.g., as would be denoted by triangles on the DQ or DQS lines pointing away from the memory controller).

For example, in certain embodiments, the circuit **40** comprises a pair of switches **120***a*, **120***b* on the DQ data signal lines **102***a*, **102***b* as schematically illustrated by FIG. **3**A. Each switch **120***a*, **120***b* is selectively actuated to selectively electrically couple the DQ data signal line **102***a* to the common DQ signal line **112**, the DQ data signal line **102***b* to the common DQ signal line **112**, or both DQ data signal lines **102***a*, **102***b* to the common DQ signal line **112**. In certain other embodiments, the circuit **40** comprises a switch **120** electrically coupled to both of the DQ data signal lines **102***a*, **102***b*, as schematically illustrated by FIG. **3**B. The switch **120** is selectively actuated to selectively electrically couple the DQ data signal line **102***a* to the common DQ signal line **112**, the DQ data signal line **102***b* to the common DQ signal line **112**, or both DQ signal lines **102***a*, **102***b* to the common DQ signal line **112**. Circuits **40** having other configurations of switches are also compatible with embodiments described herein. While each of the memory devices **30***a*, **30***b* has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, FIGS. **3**A and **3**B only illustrate a single DQ data signal line and a single DQS data strobe signal line for each memory device **30***a*, **30***b* for simplicity. The configurations schematically illustrated by FIGS. **3**A and **3**B can be applied to all of the DQ data signal lines and DQS data strobe signal lines of the memory module **10**.

In certain embodiments, the circuit **40** selectively isolates the loads of ranks of memory devices **30** from the computer system. As schematically illustrated in FIGS. **4**A and **4**B, example memory modules **10** compatible with certain embodiments described herein comprise a first number of memory devices **30** arranged in a first number of ranks **32**. The memory modules **10** of FIGS. **4**A and **4**B comprises two ranks **32***a*, **32***b*, with each rank **32***a*, **32***b* having a corresponding set of DQ data signal lines and a corresponding set of DQS data strobe lines. Other numbers of ranks (e.g., four ranks) of memory devices **30** of the memory module **10** are also compatible with certain embodiments described herein. For simplicity, FIGS. **4**A and **4**B illustrate only a single DQ data signal line and a single DQS data strobe signal line from each rank **32**.

The circuit **40** of FIG. **4**A selectively isolates one or more of the DQ data signal lines **102***a*, **102***b* of the two ranks **32***a*, **32***b* from the computer system. Thus, the circuit **40** selectively allows a DQ data signal to be transmitted from the memory controller **20** of the computer system to the memory devices **30** of one or both of the ranks **32***a*, **32***b* via the DQ

data signal lines **102***a*, **102***b*. In addition, the circuit **40** selectively allows one of a first DQ data signal from the DQ data signal line **102***a* of the first rank **32***a* and a second DQ data signal from the DQ data signal line **102***b* of the second rank **32***b* to be transmitted to the memory controller **20** via the common DQ data signal line **112**. For example, in certain embodiments, the circuit **40** comprises a pair of switches **120***a*, **120***b* on the DQ data signal lines **102***a*, **102***b* as schematically illustrated by FIG. **4**A. Each switch **120***a*, **120***b* is selectively actuated to selectively electrically couple the DQ data signal line **102***a* to the common DQ data signal line **112**, the DQ data signal line **102***b* to the common DQ data signal line **112**, or both DQ data signal lines **102***a*, **102***b* to the common DQ data signal line **112**. In certain other embodiments, the circuit **40** comprises a switch **120** electrically coupled to both of the DQ data signal lines **102***a*, **102***b*, as schematically illustrated by FIG. **4**B. The switch **120** is selectively actuated to selectively electrically couple the DQ data signal line **102***a* to the common DQ data signal line **112**, the DQ data signal line **102***b* to the common DQ data signal line **112**, or both DQ data signal lines **102***a*, **102***b* to the common DQ data signal line **112**. Circuits **40** having other configurations of switches are also compatible with embodiments described herein.

In the example embodiments schematically illustrated by FIGS. **3**A, **3**B, **4**A, and **4**B, the circuit **40** comprises a logic element which is integral with and comprises the switches **120** which are coupled to the DQ data signal lines and the DQS data strobe signal lines. In certain such embodiments, each switch **120** comprises a data path multiplexer/demultiplexer. In certain other embodiments, the circuit **40** comprises a logic element **122** which is a separate component operatively coupled to the switches **120**, as schematically illustrated by FIGS. **5**A-**5**D. The one or more switches **120** are operatively coupled to the logic element **122** to receive control signals from the logic element **122** and to selectively electrically couple one or more data signal lines to a common data signal line. Example switches compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex. Example logic elements **122** compatible with certain embodiments described herein include, but are not limited to, programmable-logic devices (PLD), application-specific integrated circuits (ASIC), field-programmable gate arrays (FPGA), custom-designed semiconductor devices, and complex programmable-logic devices (CPLD). Example logic elements **122** are available from Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif.

In certain embodiments, the load isolation provided by the circuit **40** advantageously allows the memory module **10** to present a reduced load (e.g., electrical load, such as capacitive load, inductive load, or impedance load) to the computer system by selectively switching between the two ranks of memory devices **30** to which it is coupled. This feature is used in certain embodiments in which the load of the memory module **10** may otherwise limit the number of ranks or the number of memory devices per memory module. In certain embodiments, the memory module **10** operates as having a data path rank buffer which advantageously isolates the ranks of memory devices **30** of the memory module **10** from one another, from the ranks on other memory modules, and from the computer system. This data path rank buffer of certain embodiments advantageously provides DQ-DQS paths for each rank or sets of ranks of memory devices which are separate from one another, or which are separate from the memory controller of the computer system. In certain embodiments, the load isolation advantageously diminishes the effects of capacitive loading, jitter and other sources of noise. In certain embodiments, the load isolation advantageously simplifies various other aspects of operation of the memory module **10**, including but not limited to, setup-and-hold time, clock skew, package skew, and process, temperature, voltage, and transmission line variations.

For certain memory module applications that utilize multiple ranks of memory, increased load on the memory bus can degrade speed performance. In certain embodiments described herein, selectively isolating the loads of the ranks of memory devices **30** advantageously decreases the load on the computer system, thereby allowing the computer system (e.g., server) to run faster with improved signal integrity. In certain embodiments, load isolation advantageously provides system memory with reduced electrical loading, thereby improving the electrical topology to the memory controller **20**. In certain such embodiments, the speed and the memory density of the computer system are advantageously increased without sacrificing one for the other.

In certain embodiments, load isolation advantageously increases the size of the memory array supported by the memory controller **20** of the computer system. The larger memory array has an increased number of memory devices **30** and ranks of memory devices **30** of the memory module **10**, with a corresponding increased number of chip selects. Certain embodiments described herein advantageously provide more system memory using fewer chip selects, thereby avoiding the chip select limitation of the memory controller.

An exemplary section of Verilog code corresponding to logic compatible with a circuit **40** which provides load isolation is listed below in Example 1. The exemplary code of Example 1 corresponds to a circuit **40** comprising six FET switches for providing load isolation to DQ and DQS lines.

Example 1

```
//========================== declarations
  reg              rasN_R, casN_R, weN_R;
  wire             actv_cmd_R, pch_cmd_R, pch_all_cmd_R, ap_xfr_cmd_R_R;
  wire             xfr_cmd_R,mrs_cmd,rd_cmd_R;
  //- - - - - - - - - - - - - - - - - - - - - - - - DDR 2 FET
  reg              brs0N_R;                    // registered chip sel
  reg              brs1N_R;                    // registered chip sel
  reg              brs2N_R;                    // registered chip sel
  reg              brs3N_R;                    // registered chip sel
  wire             sel;
  wire             sel_01;
  wire             sel_23;
  wire             rd_R1;
```

-continued

```
  wire                    wr__cmd__R,wr__R1;
  reg                     rd__R2,rd__R3,rd__R4,rd__R5;
  reg                     wr__R2,wr__R3,wr__R4,wr__R5;
  reg                     enfet1,enfet2,enfet3,enfet4,enfet5,enfet6;
  wire                    wr__01__R1,wr__23__R1;
  reg                     wr__01__R2,wr__01__R3,wr__01__R4;
  reg                     wr__23__R2,wr__23__R3,wr__23__R4;
  wire                    rodt0__a,rodt0__b;
//============================ logic
  always @(posedge clk__in)
          begin
                  brs0N__R <= brs0__in__N;      // cs0
                  brs1N__R <= brs1__in__N;      // cs1
                  brs2N__R <= brs2__in__N;      // cs2
                  brs3N__R <= brs3__in__N;      // cs3
                  rasN__R <= brras__in__N ;
                  casN__R <= brcas__in__N ;
                  weN__R <= bwe__in__N ;
          end
assign sel = ~brs0N__R | ~brs1N__R | ~brs2N__R | ~brs3N__R ;
assign sel__01 = ~brs0N__R | ~brs1N__R ;
assign sel__23 = ~brs2N__R | ~brs3N__R ;
assign actv__cmd__R = !rasN__R & casN__R & weN__R; // activate cmd
assign pch__cmd__R = !rasN__R & casN__R & !weN__R ;// pchg cmd
assign xfr__cmd__R = rasN__R & !casN__R;                // xfr cmd
assign mrs__cmd = !rasN__R & !casN__R & !weN__R ;    // md reg set cmd
assign rd__cmd__R = rasN__R & !casN__R & weN__R ;    // read cmd
assign wr__cmd__R = rasN__R & !casN__R & !weN__R ;  // write cmd
//---------------------------------------
assign    rd__R1 = sel & rd__cmd__R;   // rd cmd cyc 1
assign    wr__R1 = sel & wr__cmd__R; // wr cmd cyc 1
//---------------------------------------
  always @(posedge clk__in)
          begin
                  rd__R2 <= rd__R1 ;
                  rd__R3 <= rd__R2;
                  rd__R4 <= rd__R3;
                  rd__R5 <= rd__R4;
//                rd0__o__R6 <= rd0__o__R5;
                  wr__R2 <= wr__R1 ;
                  wr__R3 <= wr__R2;
                  wr__R4 <= wr__R3;
                  wr__R5 <= wr__R4;
          end
//---------------------------------------
assign    wr__01__R1 = sel__01 & wr__cmd__R; // wr cmd cyc 1 for cs 2 & cs3
assign    wr__23__R1 = sel__23 & wr__cmd__R; // wr cmd cyc 1 for cs 2 & cs3
  always @(posedge clk__in)
          begin
                  wr__01__R2 <= wr__01__R1 ;
                  wr__01__R3 <= wr__01__R2;
                  wr__01__R4 <= wr__01__R3;
                  wr__23__R2 <= wr__23__R1 ;
                  wr__23__R3 <= wr__23__R2;
                  wr__23__R4 <= wr__23__R3;
          end
assign    rodt0__ab = (rodt0)           // odt cmd from sys
                  | (wr__23__R1)  // wr 1st cyc to other rnks (assume single dimm per channel)
                  | (wr__23__R2)  // wr 2nd cyc to other rnks (assume single dimm per channel)
                  | (wr__23__R3)  // wr 3rd cyc to other rnks (assume single dimm per channel)
                  ;
assign    rodt1__ab = (rodt1)           // odt cmd from sys
                  | (wr__01__R1)  // wr 1st cyc to other rnks (assume single dimm per channel)
                  | (wr__01__R2)  // wr 2nd cyc to other rnks (assume single dimm per channel)
                  | (wr__01__R3)  // wr 3rd cyc to other rnks (assume single dimm per channel)
                  ;
//---------------------------------------
  always @(posedge clk__in)
          begin
   if (
      | (rd__R2)                          // pre-am rd
      | (rd__R3)                          // 1st cyc of rd brst (cl3)
      | (rd__R4)                          // 2nd cyc of rd brst (cl3)
      | (wr__R1)                          // pre-am wr
      | (wr__R2)                          // wr brst 1st cyc
      | (wr__R3)                          // wr brst 2nd cyc
       ) begin
                  enfet1 <= 1'b1;         // enable fet
                  enfet2 <= 1'b1;         // enable fet
```

-continued

```
                enfet3 <= 1'b1;        // enable fet
                enfet4 <= 1'b1;        // enable fet
                enfet5 <= 1'b1;        // enable fet
                enfet6 <= 1'b1;        // enable fet
        end
    else
        begin
                enfet1 <= 1'b0;        // disable fet
                enfet2 <= 1'b0;        // disable fet
                enfet3 <= 1'b0;        // disable fet
                enfet4 <= 1'b0;        // disable fet
                enfet5 <= 1'b0;        // disable fet
                enfet6 <= 1'b0;        // disable fet
        end
end
```

Back-to-Back Adjacent Read Commands

Due to their source synchronous nature, DDR SDRAM (e.g., DDR1, DDR2, DDR3) memory devices operate with a data transfer protocol which surrounds each burst of data strobes with a pre-amble time interval and a post-amble time interval. The pre-amble time interval provides a timing window for the receiving memory device to enable its data capture circuitry when a known valid level is present on the strobe signal to avoid false triggers of the memory device's capture circuit. The post-amble time interval provides extra time after the last strobe for this data capture to facilitate good signal integrity. In certain embodiments, when the computer system accesses two consecutive bursts of data from the same memory device, termed herein as a "back-to-back adjacent read," the post-amble time interval of the first read command and the pre-amble time interval of the second read command are skipped by design protocol to increase read efficiency. FIG. **6**A shows an exemplary timing diagram of this "gapless" read burst for a back-to-back adjacent read condition from one memory device.

In certain embodiments, when the second read command accesses data from a different memory device than does the first read command, there is at least one time interval (e.g., clock cycle) inserted between the data strobes of the two memory devices. This inserted time interval allows both read data bursts to occur without the post-amble time interval of the first read data burst colliding or otherwise interfering with the pre-amble time interval of the second read data burst. In certain embodiments, the memory controller of the computer system inserts an extra clock cycle between successive read commands issued to different memory devices, as shown in the exemplary timing diagram of FIG. **6**B for successive read accesses from different memory devices.

In typical computer systems, the memory controller is informed of the memory boundaries between the ranks of memory of the memory module prior to issuing read commands to the memory module. Such memory controllers can insert wait time intervals or clock cycles to avoid collisions or interference between back-to-back adjacent read commands which cross memory device boundaries, which are referred to herein as "BBARX."

In certain embodiments described herein in which the number of ranks **32** of the memory module **10** is doubled or quadrupled, the circuit **40** generates a set of output address and command signals so that the selection decoding is transparent to the computer system. However, in certain such embodiments, there are memory device boundaries of which the computer system is unaware, so there are occasions in which BBARX occurs without the cognizance of the memory controller **20** of the computer system. As shown in FIG. **7**, the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b," resulting in a "collision window."

FIGS. **8**A-**8**D schematically illustrate circuit diagrams of example memory modules **10** comprising a circuit **40** which multiplexes the DQS data strobe signal lines **104***a*, **104***b* of two ranks **32***a*, **32***b* from one another in accordance with certain embodiments described herein. While the DQS data strobe signal lines **104***a*, **104***b* of FIGS. **8**A-**8**D correspond to two ranks **32***a*, **32***b* of memory devices **30**, in certain other embodiments, the circuit **40** multiplexes the DQS data strobe signal lines **104***a*, **104***b* corresponding to two individual memory devices **30***a*, **30***b*.

FIG. **8**A schematically illustrates a circuit diagram of an exemplary memory module **10** comprising a circuit **40** in accordance with certain embodiments described herein. In certain embodiments, BBARX collisions are avoided by a mechanism which electrically isolates the DQS data strobe signal lines **104***a*, **104***b* from one another during the transition from the first read data burst of one rank **32***a* of memory devices **30** to the second read data burst of another rank **32***b* of memory devices **30**.

In certain embodiments, as schematically illustrated by FIG. **8**A, the circuit **40** comprises a first switch **130***a* electrically coupled to a first DQS data strobe signal line **104***a* of a first rank **32***a* of memory devices **30** and a second switch **130***b* electrically coupled to a second DQS data strobe signal line **104***b* of a second rank **32***b* of memory devices **30**. In certain embodiments, the time for switching the first switch **130***a* and the second switch **130***b* is between the two read data bursts (e.g., after the last DQS data strobe of the read data burst of the first rank **32***a* and before the first DQS data strobe of the read data burst of the second rank **32***b*). During the read data burst for the first rank **32***a*, the first switch **130***a* is enabled. After the last DQS data strobe of the first rank **32***a* and before the first DQS data strobe of the second rank **32***b*, the first switch **130***a* is disabled and the second switch **130***b* is enabled.

As shown in FIG. **8**A, each of the ranks **32***a*, **32***b* otherwise involved in a BBARX collision have their DQS data strobe signal lines **104***a*, **104***b* selectively electrically coupled to the common DQS line **114** through the circuit **40**. The circuit **40** of certain embodiments multiplexes the DQS data strobe signal lines **104***a*, **104***b* of the two ranks **32***a*, **32***b* of memory devices **30** from one another to avoid a BBARX collision.

In certain embodiments, as schematically illustrated by FIG. **8**B, the circuit **40** comprises a switch **130** which multiplexes the DQS data strobe signal lines **104***a*, **104***b*

from one another. For example, the circuit **40** receives a DQS data strobe signal from the common DQS data strobe signal line **114** and selectively transmits the DQS data strobe signal to the first DQS data strobe signal line **104***a*, to the second DQS data strobe signal line **104***b*, or to both DQS data strobe signal lines **104***a*, **104***b*. As another example, the circuit **40** receives a first DQS data strobe signal from the first rank **32***a* of memory devices **30** and a second DQS data strobe signal from a second rank **32***b* of memory devices **30** and selectively switches one of the first and second DQS data strobe signals to the common DQS data strobe signal line **114**.

In certain embodiments, the circuit **40** also provides the load isolation described above in reference to FIGS. **1-5**. For example, as schematically illustrated by FIG. **8**C, the circuit **40** comprises both the switch **120** for the DQ data signal lines **102***a*, **102***b* and the switch **130** for the DQS data strobe signal lines **104***a*, **104***b*. While in certain embodiments, the switches **130** are integral with a logic element of the circuit **40**, in certain other embodiments, the switches **130** are separate components which are operatively coupled to a logic element **122** of the circuit **40**, as schematically illustrated by FIG. **8**D. In certain such embodiments, the control and timing of the switch **130** is performed by the circuit **40** which is resident on the memory module **10**. Example switches **130** compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex., and multiplexers, such as the SN74AUC2G53 2:1 analog multiplexer/demultiplexer available from Texas Instruments, Inc. of Dallas, Tex.

The circuit **40** of certain embodiments controls the isolation of the DQS data strobe signal lines **104***a*, **104***b* by monitoring commands received by the memory module **10** from the computer system and producing "windows" of operation whereby the appropriate switches **130** are activated or deactivated to enable and disable the DQS data strobe signal lines **104***a*, **104***b* to mitigate BBARX collisions. In certain other embodiments, the circuit **40** monitors the commands received by the memory module **10** from the computer system and selectively activates or deactivates the switches **120** to enable and disable the DQ data signal lines **102***a*, **102***b* to reduce the load of the memory module **10** on the computer system. In still other embodiments, the circuit **40** performs both of these functions together.

Command Signal Translation

Most high-density memory modules are currently built with 512-Megabit ("512-Mb") memory devices wherein each memory device has a 64 M×8-bit configuration. For example, a 1-Gigabyte ("1-GB") memory module with error checking capabilities can be fabricated using eighteen such 512-Mb memory devices. Alternatively, it can be economically advantageous to fabricate a 1-GB memory module using lower-density memory devices and doubling the number of memory devices used to produce the desired word width. For example, by fabricating a 1-GB memory module using thirty-six 256-Mb memory devices with 64 M×4-bit configuration, the cost of the resulting 1-GB memory module can be reduced since the unit cost of each 256-Mb memory device is typically lower than one-half the unit cost of each 512-Mb memory device. The cost savings can be significant, even though twice as many 256-Mb memory devices are used in place of the 512-Mb memory devices. For example, by using pairs of 512-Mb memory devices rather than single 1-Gb memory devices, certain embodiments described herein reduce the cost of the memory module by a factor of up to approximately five.

Market pricing factors for DRAM devices are such that higher-density DRAM devices (e.g., 1-Gb DRAM devices) are much more than twice the price of lower-density DRAM devices (e.g., 512-Mb DRAM devices). In other words, the price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices. This pricing difference often lasts for months or even years after the introduction of the higher-density DRAM devices, until volume production factors reduce the costs of the newer higher-density DRAM devices. Thus, when the cost of a higher-density DRAM device is more than the cost of two lower-density DRAM devices, there is an economic incentive for utilizing pairs of the lower-density DRAM devices to replace individual higher-density DRAM devices.

FIG. **9**A schematically illustrates an exemplary memory module **10** compatible with certain embodiments described herein. The memory module **10** is connectable to a memory controller **20** of a computer system (not shown). The memory module **10** comprises a printed circuit board **210** and a plurality of memory devices **30** coupled to the printed circuit board **210**. The plurality of memory devices **30** has a first number of memory devices **30**. The memory module **10** further comprises a circuit **40** coupled to the printed circuit board **210**. The circuit **40** receives a set of input address and command signals from the computer system. The set of input address and command signals correspond to a second number of memory devices **30** smaller than the first number of memory devices **30**. The circuit **40** generates a set of output address and command signals in response to the set of input address and command signals. The set of output address and command signals corresponds to the first number of memory devices **30**.

In certain embodiments, as schematically illustrated in FIG. **9**A, the memory module **10** further comprises a phase-lock loop device **220** coupled to the printed circuit board **210** and a register **230** coupled to the printed circuit board **210**. In certain embodiments, the phase-lock loop device **220** and the register **230** are each mounted on the printed circuit board **210**. In response to signals received from the computer system, the phase-lock loop device **220** transmits clock signals to the plurality of memory devices **30**, the circuit **40**, and the register **230**. The register **230** receives and buffers a plurality of command signals and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals), and transmits corresponding signals to the appropriate memory devices **30**. In certain embodiments, the register **230** comprises a plurality of register devices. While the phase-lock loop device **220**, the register **230**, and the circuit **40** are described herein in certain embodiments as being separate components, in certain other embodiments, two or more of the phase-lock loop device **220**, the register **230**, and the circuit **40** are portions of a single component. Persons skilled in the art are able to select a phase-lock loop device **220** and a register **230** compatible with embodiments described herein.

In certain embodiments, the memory module **10** further comprises electrical components which are electrically coupled to one another and are surface-mounted or embedded on the printed circuit board **210**. These electrical components can include, but are not limited to, electrical conduits, resistors, capacitors, inductors, and transistors. In certain embodiments, at least some of these electrical components are discrete, while in other certain embodiments, at

least some of these electrical components are constituents of one or more integrated circuits.

In certain embodiments, the printed circuit board **210** is mountable in a module slot of the computer system. The printed circuit board **210** of certain such embodiments has a plurality of edge connections electrically coupled to corresponding contacts of the module slot and to the various components of the memory module **10**, thereby providing electrical connections between the computer system and the components of the memory module **10**.

In certain embodiments, the plurality of memory devices **30** are arranged in a first number of ranks **32**. For example, in certain embodiments, the memory devices **30** are arranged in four ranks **32***a*, **32***b*, **32***c*, **32***d*, as schematically illustrated by FIG. **9**A. In certain other embodiments, the memory devices **30** are arranged in two ranks **32***a*, **32***b*, as schematically illustrated by FIG. **9**B. Other numbers of ranks **32** of the memory devices **30** are also compatible with embodiments described herein.

As schematically illustrated by FIGS. **9**A and **9**B, in certain embodiments, the circuit **40** receives a set of input command signals (e.g., refresh, precharge) and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) from the memory controller **20** of the computer system. In response to the set of input address and command signals, the circuit **40** generates a set of output address and command signals.

In certain embodiments, the set of output address and command signals corresponds to a first number of ranks in which the plurality of memory devices **30** of the memory module **10** are arranged, and the set of input address and command signals corresponds to a second number of ranks per memory module for which the computer system is configured. The second number of ranks in certain embodiments is smaller than the first number of ranks. For example, in the exemplary embodiment as schematically illustrated by FIG. **9**A, the first number of ranks is four while the second number of ranks is two. In the exemplary embodiment of FIG. **9**B, the first number of ranks is two while the second number of ranks is one. Thus, in certain embodiments, even though the memory module **10** actually has the first number of ranks of memory devices **30**, the memory module **10** simulates a virtual memory module by operating as having the second number of ranks of memory devices **30**. In certain embodiments, the memory module **10** simulates a virtual memory module when the number of memory devices **30** of the memory module **10** is larger than the number of memory devices **30** per memory module for which the computer system is configured to utilize. In certain embodiments, the circuit **40** comprises logic (e.g., address decoding logic, command decoding logic) which translates between a system memory domain of the computer system and a physical memory domain of the memory module **10**.

In certain embodiments, the computer system is configured for a number of ranks per memory module which is smaller than the number of ranks in which the memory devices **30** of the memory module **10** are arranged. In certain such embodiments, the computer system is configured for two ranks of memory per memory module (providing two chip-select signals CS_0, CS_1) and the plurality of memory modules **30** of the memory module **10** are arranged in four ranks, as schematically illustrated by FIG. **9**A. In certain other such embodiments, the computer system is configured for one rank of memory per memory module (providing one chip-select signal CS_0) and the plurality of memory modules **30** of the memory module **10** are arranged in two ranks, as schematically illustrated by FIG. **9**B.

In the exemplary embodiment schematically illustrated by FIG. **9**A, the memory module **10** has four ranks of memory devices **30** and the computer system is configured for two ranks of memory devices per memory module. The memory module **10** receives row/column address signals or signal bits (A_0-A_{n+1}), bank address signals (BA_0-BA_m), chip-select signals (CS_0 and CS_1), and command signals (e.g., refresh, precharge, etc.) from the computer system. The A_0-A_n row/column address signals are received by the register **230**, which buffers these address signals and sends these address signals to the appropriate ranks of memory devices **30**. The circuit **40** receives the two chip-select signals (CS_0, CS_1) and one row/column address signal (A_{n+1}) from the computer system. Both the circuit **40** and the register **230** receive the bank address signals (BA_0-BA_m) and at least one command signal (e.g., refresh, precharge, etc.) from the computer system.

Logic Tables

Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using chip-select signals.

TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:
1. CS_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

In Logic State 1: CS_0 is active low, A_{n+1} is non-active, and Command is active. CS_{0A} is pulled low, thereby selecting Rank 0.

In Logic State 2: CS_0 is active low, A_{n+1} is active, and Command is active. CS_{0B} is pulled low, thereby selecting Rank 1.

In Logic State 3: CS_0 is active low, A_{n+1} is Don't Care, and Command is active high. CS_{0A} and CS_{0B} are pulled low, thereby selecting Ranks 0 and 1.

In Logic State 4: CS_1 is active low, A_{n+1} is non-active, and Command is active. CS_{1A} is pulled low, thereby selecting Rank 2.

In Logic State 5: CS_1 is active low, A_{n+1} is active, and Command is active. CS_{1B} is pulled low, thereby selecting Rank 3.

In Logic State 6: CS_1 is active low, A_{n+1} is Don't Care, and Command is active. CS_{1A} and CS_1B are pulled low, thereby selecting Ranks 2 and 3.

In Logic State 7: CS_0 and CS_1 are pulled non-active high, which deselects all ranks, i.e., CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are pulled high.

The "Command" column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one

memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently.

Table 2 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using gated CAS signals.

TABLE 2

CS*	RAS*	CAS*	WE*	Density Bit	A_{10}	Command	CAS0*	CAS1*
1	x	x	x	x	x	NOP	x	x
0	1	1	1	x	x	NOP	1	1
0	0	1	1	0	x	ACTIVATE	1	1
0	0	1	1	1	x	ACTIVATE	1	1
0	1	0	1	0	x	READ	0	1
0	1	0	1	1	x	READ	1	0
0	1	0	0	0	x	WRITE	0	1
0	1	0	0	1	x	WRITE	1	0
0	0	1	0	0	0	PRECHARGE	1	1
0	0	1	0	1	0	PRECHARGE	1	1
0	0	1	0	x	1	PRECHARGE	1	1
0	0	0	0	x	x	MODE REG SET	0	0
0	0	0	1	x	x	REFRESH	0	0

In certain embodiments in which the density bit is a row address bit, for read/write commands, the density bit is the value latched during the activate command for the selected bank.

Serial-Presence-Detect Device

Memory modules typically include a serial-presence detect (SPD) device **240** (e.g., an electrically-erasable-programmable read-only memory or EEPROM device) comprising data which characterize various attributes of the memory module, including but not limited to, the number of row addresses the number of column addresses, the data width of the memory devices, the number of ranks, the memory density per rank, the number of memory devices, and the memory density per memory device. The SPD device **240** communicates this data to the basic input/output system (BIOS) of the computer system so that the computer system is informed of the memory capacity and the memory configuration available for use and can configure the memory controller properly for maximum reliability and performance.

For example, for a commercially-available 512-MB (64 M×8-byte) memory module utilizing eight 512-Mb memory devices each with a 64 M×8-bit configuration, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: Defines the number of row address bits in the DRAM device in the memory module [13 for the 512-Mb memory device].

Byte 4: Defines the number of column address bits in the DRAM device in the memory module [11 for the 512-Mb memory device].

Byte 13: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 512-Mb (64 M×8-bit) memory device].

Byte 14: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 512-Mb (64 M×8-bit) memory device].

Byte 17: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 512-Mb memory device].

In a further example, for a commercially-available 1-GB (128 M×8-byte) memory module utilizing eight 1-Gb memory devices each with a 128 M×8-bit configuration, as described above, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: Defines the number of row address bits in the DRAM device in the memory module [14 for the 1-Gb memory device].

Byte 4: Defines the number of column address bits in the DRAM device in the memory module [11 for the 1-Gb memory device].

Byte 13: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 1-Gb (128 M×8-bit) memory device].

Byte 14: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 1-Gb (128 M×8-bit) memory device].

Byte 17: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 1-Gb memory device].

In certain embodiments, the SPD device **240** comprises data which characterize the memory module **10** as having fewer ranks of memory devices than the memory module **10** actually has, with each of these ranks having more memory density. For example, for a memory module **10** compatible with certain embodiments described herein having two ranks of memory devices **30**, the SPD device **240** comprises data which characterizes the memory module **10** as having one rank of memory devices with twice the memory density per rank. Similarly, for a memory module **10** compatible with certain embodiments described herein having four ranks of memory devices **30**, the SPD device **240** comprises data which characterizes the memory module **10** as having two ranks of memory devices with twice the memory density per rank. In addition, in certain embodiments, the SPD device **240** comprises data which characterize the memory module **10** as having fewer memory devices than the memory module **10** actually has, with each of these memory devices having more memory density per memory device. For example, for a memory module **10** compatible with certain embodiments described herein, the SPD device **240** comprises data which characterizes the memory module **10** as having one-half the number of memory devices that the

memory module **10** actually has, with each of these memory devices having twice the memory density per memory device. Thus, in certain embodiments, the SPD device **240** informs the computer system of the larger memory array by reporting a memory device density that is a multiple of the memory devices **30** resident on the memory module **10**. Certain embodiments described herein advantageously do not require system level changes to hardware (e.g., the motherboard of the computer system) or to software (e.g., the BIOS of the computer system).

FIG. **9**C schematically illustrates an exemplary memory module **10** in accordance with certain embodiments described herein. The memory module **10** comprises a pair of substantially identical memory devices **31**, **33**. Each memory device **31**, **33** has a first bit width, a first number of banks of memory locations, a first number of rows of memory locations, and a first number of columns of memory locations. The memory module **10** further comprises an SPD device **240** comprising data that characterizes the pair of memory devices **31**, **33**. The data characterize the pair of memory devices **31**, **33** as a virtual memory device having a second bit width equal to twice the first bit width, a second number of banks of memory locations equal to the first number of banks, a second number of rows of memory locations equal to the first number of rows, and a second number of columns of memory locations equal to the first number of columns.

In certain such embodiments, the SPD device **240** of the memory module **10** is programmed to describe the combined pair of lower-density memory devices **31**, **33** as one virtual or pseudo-higher-density memory device. In an exemplary embodiment, two 512-Mb memory devices, each with a 128 M×4-bit configuration, are used to simulate one 1-Gb memory device having a 128 M×8-bit configuration. The SPD device **240** of the memory module **10** is programmed to describe the pair of 512-Mb memory devices as one virtual or pseudo-1-Gb memory device.

For example, to fabricate a 1-GB (128 M×8-byte) memory module, sixteen 512-Mb (128 M×4-bit) memory devices can be used. The sixteen 512-Mb (128 M×4-bit) memory devices are combined in eight pairs, with each pair serving as a virtual or pseudo-1-Gb (128 M×8-bit) memory device. In certain such embodiments, the SPD device **240** contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: 13 row address bits.

Byte 4: 12 column address bits.

Byte 13: 8 bits wide for the primary virtual 1-Gb (128 M×8-bit) memory device.

Byte 14: 8 bits wide for the error checking virtual 1-Gb (128 M×8-bit) memory device.

Byte 17: 4 banks.

In this exemplary embodiment, bytes 3, 4, and 17 are programmed to have the same values as they would have for a 512-MB (128 M×4-byte) memory module utilizing 512-Mb (128 M×4-bit) memory devices. However, bytes 13 and 14 of the SPD data are programmed to be equal to 8, corresponding to the bit width of the virtual or pseudo-higher-density 1-Gb (128 M×8-bit) memory device, for a total capacity of 1-GB. Thus, the SPD data does not describe the actual-lower-density memory devices, but instead describes the virtual or pseudo-higher-density memory devices. The BIOS accesses the SPD data and recognizes the memory module as having 4 banks of memory locations arranged in 2^{13} rows and 2^{12} columns, with each memory location having a width of 8 bits rather than 4 bits.

In certain embodiments, when such a memory module **10** is inserted in a computer system, the computer system's memory controller then provides to the memory module **10** a set of input address and command signals which correspond to the number of ranks or the number of memory devices reported by the SPD device **240**. For example, placing a two-rank memory module **10** compatible with certain embodiments described herein in a computer system compatible with one-rank memory modules, the SPD device **240** reports to the computer system that the memory module **10** only has one rank. The circuit **40** then receives a set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices **30** of the memory module **10**.

Similarly, when a two-rank memory module **10** compatible with certain embodiments described herein is placed in a computer system compatible with either one- or two-rank memory modules, the SPD device **240** reports to the computer system that the memory module **10** only has one rank. The circuit **40** then receives a set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices **30** of the memory module **10**.

Furthermore, a four-rank memory module **10** compatible with certain embodiments described herein simulates a two-rank memory module whether the memory module **10** is inserted in a computer system compatible with two-rank memory modules or with two- or four-rank memory modules. Thus, by placing a four-rank memory module **10** compatible with certain embodiments described herein in a module slot that is four-rank-ready, the computer system provides four chip-select signals, but the memory module **10** only uses two of the chip-select signals.

In certain embodiments, the circuit **40** comprises the SPD device **240** which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device **240** of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array. In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit **40**. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices **30** from the memory controller **20**. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three. In still other embodiments, the SPD device **240** does not utilize this extra cycle of time.

Memory Density Multiplication

In certain embodiments, two memory devices having a memory density are used to simulate a single memory device having twice the memory density, and an additional

address signal bit is used to access the additional memory. Similarly, in certain embodiments, two ranks of memory devices having a memory density are used to simulate a single rank of memory devices having twice the memory density, and an additional address signal bit is used to access the additional memory. As used herein, such simulations of memory devices or ranks of memory devices are termed as "memory density multiplication," and the term "density transition bit" is used to refer to the additional address signal bit which is used to access the additional memory by selecting which rank of memory devices is enabled for a read or write transfer operation.

For example, for computer systems which are normally limited to using memory modules which have a single rank of 128 M×4-bit memory devices, certain embodiments described herein enable the computer system to utilize memory modules which have double the memory (e.g., two ranks of 128 M×4-bit memory devices). The circuit **40** of certain such embodiments provides the logic (e.g., command and address decoding logic) to double the number of chip selects, and the SPD device **240** reports a memory device density of 256 M×4-bit to the computer system.

In certain embodiments utilizing memory density multiplication embodiments, the memory module **10** can have various types of memory devices **30** (e.g., DDR1, DDR2, DDR3, and beyond). The circuit **40** of certain such embodiments utilizes implied translation logic equations having variations depending on whether the density transition bit is a row, column, or internal bank address bit. In addition, the translation logic equations of certain embodiments vary depending on the type of memory module **10** (e.g., UDIMM, RDIMM, FBDIMM, etc.). Furthermore, in certain embodiments, the translation logic equations vary depending on whether the implementation multiplies memory devices per rank or multiplies the number of ranks per memory module.

TABLE 3A

	128-Mb	256-Mb	512-Mb	1-Gb
Number of banks	4	4	4	4
Number of row address bits	12	13	13	14
Number of column address bits for "x 4" configuration	11	11	12	12
Number of column address bits for "x 8" configuration	10	10	11	11
Number of column address bits for "x 16" configuration	9	9	10	10

Table 3A provides the numbers of rows and columns for DDR-1 memory devices, as specified by JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published February 2004, and incorporated in its entirety by reference herein.

As described by Table 3A, 512-Mb (128 M×4-bit) DRAM devices have 2^{13} rows and 2^{12} columns of memory locations, while 1-Gb (128 M×8-bit) DRAM devices have 2^{14} rows and 2^{11} columns of memory locations. Because of the differences in the number of rows and the number of columns for the two types of memory devices, complex address translation procedures and structures would typically be needed to fabricate a 1-GB (128 M×8-byte) memory module using sixteen 512-Mb (128 M×4-bit) DRAM devices.

Table 3B shows the device configurations as a function of memory density for DDR2 memory devices.

TABLE 3B

	Number of Rows	Number of Columns	Number of Internal Banks	Page Size (x4s or x8s)
256 Mb	13	11	4	1 KB
512 Mb	14	11	4	1 KB
1 Gb	14	11	8	1 KB
2 Gb	15	11	8	1 KB
4 Gb	16	11	8	1 KB

Table 4 lists the corresponding density transition bit for the density transitions between the DDR2 memory densities of Table 3B.

TABLE 4

Density Transition	Density Transition Bit
256 Mb to 512 Mb	A_{13}
512 Mb to 1 Gb	BA_2
1 Gb to 2 Gb	A_{14}
2 Gb to 4 Gb	A_{15}

Other certain embodiments described herein utilize a transition bit to provide a transition from pairs of physical 4-Gb memory devices to simulated 8-Gb memory devices.

In an example embodiment, the memory module comprises one or more pairs of 256-Mb memory devices, with each pair simulating a single 512-Mb memory device. The simulated 512-Mb memory device has four internal banks while each of the two 256-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 256-Mb memory devices. In certain embodiments, the additional row address bit is translated by the circuit **40** to the rank selection between each of the two 256-Mb memory devices of the pair. Although there are eight total internal banks in the rank-converted memory array, the computer system is only aware of four internal banks. When the memory controller activates a row for a selected bank, the circuit **40** activates the same row for the same bank, but it does so for the selected rank according to the logic state of the additional row address bit A_{13}.

In another example embodiment, the memory module comprises one or more pairs of 512-Mb memory devices, with each pair simulating a single 1-Gb memory device. The simulated 1-Gb memory device has eight internal banks while each of the two 512-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 512-Mb memory devices. In certain embodiments, the mapped BA_2 (bank 2) bit is used to select between the two ranks of 512-Mb memory devices to preserve the internal bank geometry expected by the memory controller of the computer system. The state of the BA_2 bit selects the upper or lower set of four banks, as well as the upper and lower 512-Mb rank.

In another example embodiment, the memory module comprises one or more pairs of 1-Gb memory devices, with each pair simulating a single 2-Gb memory device. Each of the two 1-Gb memory devices has eight internal banks for a total of sixteen internal banks, while the simulated 2-Gb memory device has eight internal banks. In certain embodiments, the additional row address bit translates to the rank selection between the two 1-Gb memory devices. Although there are sixteen total internal banks per pair of 1-Gb memory devices in the rank-converted memory array, the memory controller of the computer system is only aware of eight internal banks. When the memory controller activates a row of a selected bank, the circuit **40** activates the same

row for the same bank, but is does so for the selected rank according to the logic state of the additional row address bit A_{14}.

The circuit **40** of certain embodiments provides substantially all of the translation logic used for the decoding (e.g., command and address decoding). In certain such embodiments, there is a fully transparent operational conversion from the "system memory" density domain of the computer system to the "physical memory" density domain of the memory module **10**. In certain embodiments, the logic translation equations are programmed in the circuit **40** by hardware, while in certain other embodiments, the logic translation equations are programmed in the circuit **40** by software. Examples 1 and 2 provide exemplary sections of Verilog code compatible with certain embodiments described herein. As described more fully below, the code of Examples 1 and 2 includes logic to reduce potential problems due to "back-to-back adjacent read commands which cross memory device boundaries or "BBARX." Persons skilled in the art are able to provide additional logic translation equations compatible with embodiments described herein.

An exemplary section of Verilog code compatible with memory density multiplication from 512 Mb to 1 Gb using DDR2 memory devices with the BA_2 density transition bit is listed below in Example 2. The exemplary code of Example 2 corresponds to a circuit **40** which receives one chip-select signal from the computer system and which generates two chip-select signals.

Example 2

```
always @(posedge clk_in)
    begin
                rs0N_R <= rs0_in_N;    // cs0
                rasN_R <= ras_in_N;
                casN_R <= cas_in_N;
                weN_R <= we_in_N;
    end
// Gated Chip Selects
assign          pcs0a_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                          // ref,md reg set
                | (~rs0_in_N & ras_in_N & cas_in_N)                                    // ref exit, pwr dn
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)               // pchg all
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ~ba2_in)    // pchg single bnk
                | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N & ~ba2_in)               // activate
                | (~rs0_in_N & ras_in_N          & ~cas_in_N & ~ba2_in)                // xfr
                ;
assign          pcs0b_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                          // ref,md reg set
                | (~rs0_in_N & ras_in_N & cas_in_N)                                    // ref exit, pwr dn
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)               // pchg all
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ba2_in)     // pchg single bnk
                | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N & ba2_in)                // activate
                | (~rs0_in_N & ras_in_N          & ~cas_in_N & ba2_in)                 // xfr
                ;
//--------------------------------------
always @(posedge clk_in)
    begin
                a4_r <= a4_in ;
                a5_r <= a5_in ;
                a6_r <= a6_in ;
                a10_r <= a10_in ;
                ba0_r <= ba0_in ;
                ba1_r <= ba1_in ;
                ba2_r <= ba2_in ;
                q_mrs_cmd_cyc1 <= q_mrs_cmd ;
    end
////////////////////////////////////////////////////////////////////////
// determine the cas latency
////////////////////////////////////////////////////////////////////////
assign q_mrs_cmd_r = (!rasN_R & !casN_R & !weN_R)
                   & !rs0N_R
                   & (!ba0_r & !ba1_r)
                   ;       // md reg set cmd
    always @(posedge clk_in)
        if (~reset_N)       // lmr
                cl3 <= 1'b1 ;
        else if (q_mrs_cmd_cyc1)    // load mode reg cmd
      begin
                cl3 <= (~a6_r & a5_r & a4_r ) ;
      end
    always @(posedge clk_in)
        if (~reset_N)             // reset
                cl2 <= 1'b0 ;
        else if (q_mrs_cmd_cyc1)  // load mode reg cmd
      begin
                cl2 <= (~a6_r & a5_r & ~a4_r ) ;
      end
    always @(posedge clk_in)
        if (~reset_N)             // reset
                cl4 <= 1'b0 ;
        else if (q_mrs_cmd_cyc1)  // load mode reg cmd
      begin
```

-continued

```
                cl4 <= (a6_r & ~a5_r & ~a4_r ) ;
        end
    always @(posedge clk_in)
            if (~reset_N)               cl5 <= 1'b0 ;
            else if (q_mrs_cmd_cyc1)   // load mode reg cmd
        begin
                cl5 <= (a6_r & ~a5_r & a4_r ) ;
        end
assign          pre_cyc2_enfet = (wr_cmd_cyc1 & acs_cyc1 & cl3)      // wr brst cl3 preamble
                               ;
assign          pre_cyc3_enfet = (rd_cmd_cyc2 & cl3)                 // rd brst cl3 preamble
                               | (wr_cmd_cyc2 & cl3)                 // wr brst cl3 1st pair
                               | (wr_cmd_cyc2 & cl4)                 // wr brst cl4 preamble
                               ;
assign          pre_cyc4_enfet = (wr_cmd_cyc3 & cl3)                 // wr brst cl3 2nd pair
                               | (wr_cmd_cyc3 & cl4)                 // wr brst cl4 1st pair
                               | (rd_cmd_cyc3 & cl3)                 // rd brst cl3 1st pair
                               | (rd_cmd_cyc3 & cl4)                 // rd brst cl4 preamble
                               ;
assign          pre_cyc5_enfet = (rd_cmd_cyc4 & cl3)                 // rd brst cl3 2nd pair
                               | (wr_cmd_cyc4 & cl4)                 // wr brst cl4 2nd pair
                               | (rd_cmd_cyc4 & cl4)                 // rd brst cl4 1st pair
                               ;
// dq
assign          pre_dq_cyc = pre_cyc2_enfet
                    | pre_cyc3_enfet
                    | pre_cyc4_enfet
                    | pre_cyc5_enfet
                    ;
assign          pre_dq_ncyc = enfet_cyc2
                    | enfet_cyc3
                   | enfet_cyc4
                   | enfet_cyc5
                   ;
// dqs
assign          pre_dqsa_cyc = (pre_cyc2_enfet & ~ba2_r)
                   | (pre_cyc3_enfet & ~ba2_cyc2)
                   | (pre_cyc4_enfet & ~ba2_cyc3)
                   | (pre_cyc5_enfet & ~ba2_cyc4)
                   ;
assign          pre_dqsb_cyc = (pre_cyc2_enfet & ba2_r)
                   | (pre_cyc3_enfet & ba2_cyc2)
                  | (pre_cyc4_enfet & ba2_cyc3)
                  | (pre_cyc5_enfet & ba2_cyc4)
                  ;
assign          pre_dqsa_ncyc = (enfet_cyc2 & ~ba2_cyc2)
                   | (enfet_cyc3 & ~ba2_cyc3)
                   | (enfet_cyc4 & ~ba2_cyc4)
                   | (enfet_cyc5 & ~ba2_cyc5)
                   ;
assign          pre_dqsb_ncyc = (enfet_cyc2 & ba2_cyc2)
                   | (enfet_cyc3 & ba2_cyc3)
                   | (enfet_cyc4 & ba2_cyc4)
                   | (enfet_cyc5 & ba2_cyc5)
                   ;
always @(posedge clk_in)
        begin
                acs_cyc2 <= acs_cyc1 ;        // cs active
                ba2_cyc2 <= ba2_r ;
                ba2_cyc3 <= ba2_cyc2 ;
                ba2_cyc4 <= ba2_cyc3 ;
                ba2_cyc5 <= ba2_cyc4 ;
                rd_cmd_cyc2 <= rd_cmd_cyc1 & acs_cyc1;
                rd_cmd_cyc3 <= rd_cmd_cyc2 ;
                rd_cmd_cyc4 <= rd_cmd_cyc3 ;
                rd_cmd_cyc5 <= rd_cmd_cyc4 ;
                rd_cmd_cyc6 <= rd_cmd_cyc5 ;
                rd_cmd_cyc7 <= rd_cmd_cyc6 ;
                wr_cmd_cyc2 <= wr_cmd_cyc1 & acs_cyc1;
                wr_cmd_cyc3 <= wr_cmd_cyc2 ;
                wr_cmd_cyc4 <= wr_cmd_cyc3 ;
                wr_cmd_cyc5 <= wr_cmd_cyc4 ;
        end
 always @(negedge clk_in)
        begin
                dq_ncyc <= dq_cyc;
                dqs_ncyc_a <= dqs_cyc_a;
                dqs_ncyc_b <= dqs_cyc_b;
        end
```

-continued

```
// DQ FET enables
assign          enq_fet1 = dq_cyc | dq_ncyc          ;
assign          enq_fet2 = dq_cyc | dq_ncyc ;
assign        enq_fet3 = dq_cyc | dq_ncyc          ;
assign          enq_fet4 = dq_cyc | dq_ncyc ;
assign          enq_fet5 = dq_cyc | dq_ncyc ;
// DQS FET enables
assign          ens_fet1a = dqs_cyc_a | dqs_ncyc_a   ;
assign          ens_fet2a = dqs_cyc_a | dqs_ncyc_a   ;
assign          ens_fet3a = dqs_cyc_a | dqs_ncyc_a   ;
assign          ens_fet1b = dqs_cyc_b | dqs_ncyc_b   ;
assign          ens_fet2b = dqs_cyc_b | dqs_ncyc_b    ;
assign          ens_fet3b = dqs_cyc_b | dqs_ncyc_b   ;
```

Another exemplary section of Verilog code compatible with memory density multiplication from 256 Mb to 512 Mb using DDR2 memory devices and gated CAS signals with the row A_{13} density transition bit is listed below in Example 3. The exemplary code of Example 3 corresponds to a circuit **40** which receives one gated CAS signal from the computer system and which generates two gated CAS signals.

Example 3

```
// latched a13 flags cs0, banks 0-3
  always @(posedge clk_in)
    if (actv_cmd_R & ~rs0N_R & ~bnk1_R & ~bnk0_R )   // activate
    begin
                1_a13_00 <= a13_r ;
    end
  always @(posedge clk_in)
    if (actv_cmd_R & ~rs0N_R & ~bnk1_R & bnk0_R)      // activate
    begin
                1_a13_01 <= a13_r ;
    end
  always @(posedge clk_in)
    if (actv_cmd_R & ~rs0N_R & bnk1_R & ~bnk0_R)      // activate
    begin
                1_a13_10 <= a13_r ;
    end
  always @(posedge clk_in)
    if (actv_cmd_R & ~rs0N_R & bnk1_R & bnk0_R)       // activate
    begin
                1_a13_11 <= a13_r ;
    end
// gated cas
assign cas_i = ~(casN_R);
assign    cas0_o = ( ~rasN_R & cas_i)
                | ( rasN_R & ~1_a13_00 & ~bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & ~1_a13_01 & ~bnk1_R & bnk0_R & cas_i)
                | ( rasN_R & ~1_a13_10 & bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & ~1_a13_11 & bnk1_R & bnk0_R & cas_i)
                ;
assign    cas1_o = ( ~rasN_R & cas_i)
                | ( rasN_R & 1_a13_00          & ~bnk1_R & ~bnk0_R    & cas_i)
                | ( rasN_R & 1_a13_01          & ~bnk1_R & bnk0_R     & cas_i)
                | ( rasN_R & 1_a13_10          & bnk1_R & ~bnk0_R     & cas_i)
                | ( rasN_R & 1_a13_11          & bnk1_R & bnk0_R      & cas_i)
                ;
assign          pcas_0_N = ~cas0_o;
assign          pcas_1_N = ~cas1_o;
assign          rd0_o_R1 = rasN_R & cas0_o & weN_R & ~rs0N_R;    // rnk0 rd cmd cyc
assign          rd1_o_R1 = rasN_R & cas1_o & weN_R & ~rs0N_R;    // rnk1 rd cmd cyc
assign          wr0_o_R1 = rasN_R & cas0_o & ~weN_R & ~rs0N_R;   // rnk0 wr cmd cyc
assign          wr1_o_R1 = rasN_R & cas1_o & ~weN_R & ~rs0N_R ;   // rnk1 wr cmd cyc
      always @(posedge clk_in)
          begin
                rd0_o_R2 <= rd0_o_R1 ;
                rd0_o_R3 <= rd0_o_R2;
                rd0_o_R4 <= rd0_o_R3;
                rd0_o_R5 <= rd0_o_R4;
                rd1_o_R2 <= rd1_o_R1 ;
                rd1_o_R3 <= rd1_o_R2;
                rd1_o_R4 <= rd1_o_R3;
                rd1_o_R5 <= rd1_o_R4;
                wr0_o_R2 <= wr0_o_R1 ;
                wr0_o_R3 <= wr0_o_R2;
                wr0_o_R4 <= wr0_o_R3;
                wr1_o_R2 <= wr1_o_R1 ;
```

-continued

```
                wr1_o_R3 <= wr1_o_R2;
                wr1_o_R4 <= wr1_o_R3;
        end
    always @(posedge clk_in)
        begin
        if (
              (rd0_o_R2 & ~rd1_o_R4)                          // pre-am rd if no ped on rnk 1
            | rd0_o_R3                                        // 1st cyc of rd brst
            | rd0_o_R4                                        // 2nd cyc of rd brst
            | (rd0_o_R5 & ~rd1_o_R2 & ~rd1_o_R3)              // post-rd cyc if no ped on rnk 1
            | (wr0_o_R1)                                      // pre-am wr
            | wr0_o_R2 | wr0_o_R3                             // wr brst 1st & 2nd cyc
            | (wr0_o_R4)                                      // post-wr cyc (chgef9)
            | wr1_o_R1 | wr1_o_R2 | wr1_o_R3 | wr1_o_R4       // rank 1 (chgef9)
            )
                        en_fet_a <= 1'b1;                     // enable fet
        else
                        en_fet_a <= 1'b0;                     // disable fet
        end
always @(posedge clk_in)
        begin
        if (
                    (rd1_o_R2 & ~rd0_o_R4)
                  | rd1_o_R3
                  | rd1_o_R4
                  | (rd1_o_R5 & ~rd0_o_R2 & ~rd0_o_R3)
            | (wr1_o_R1)                                      // (chgef8)
            | wr1_o_R2 | wr1_o_R3
  | (wr1_o_R4)                                                // post-wr cyc      (chgef9)
  | wr0_o_R1 | wr0_o_R2 | wr0_o_R3 | wr0_o_R4                 // rank 0 (chgef9)
                  )
                      en_fet_b <= 1'b1;                       //
        else
                      en_fet_b <= 1'b0;
        end
```

In certain embodiments, the chipset memory controller of the computer system uses the inherent behavioral characteristics of the memory devices (e.g., DDR2 memory devices) to optimize throughput of the memory system. For example, for each internal bank in the memory array, a row (e.g., 1 KB page) is advantageously held activated for an extended period of time. The memory controller, by anticipating a high number of memory accesses or hits to a particular region of memory, can exercise this feature to advantageously eliminate time-consuming pre-charge cycles. In certain such embodiments in which two half-density memory devices are transparently substituted for a single full-density memory device (as reported by the SPD device **240** to the memory controller), the memory devices advantageously support the "open row" feature.

FIG. **10**A schematically illustrates an exemplary memory module **10** which doubles the rank density in accordance with certain embodiments described herein. The memory module **10** has a first memory capacity. The memory module **10** comprises a plurality of substantially identical memory devices **30** configured as a first rank **32***a* and a second rank **32***b*. In certain embodiments, the memory devices **30** of the first rank **32***a* are configured in pairs, and the memory devices **30** of the second rank **32***b* are also configured in pairs. In certain embodiments, the memory devices **30** of the first rank **32***a* are configured with their respective DQS pins tied together and the memory devices **30** of the second rank **32***b* are configured with their respective DQS pins tied together, as described more fully below. The memory module **10** further comprises a circuit **40** which receives a first set of address and command signals from a memory controller (not shown) of the computer system. The first set of address and command signals is compatible with a second memory capacity substantially equal to one-half of the first memory capacity. The circuit **40** translates the first set of address and command signals into a second set of address and command signals which is compatible with the first memory capacity of the memory module **10** and which is transmitted to the first rank **32***a* and the second rank **32***b*.

The first rank **32***a* of FIG. **10**A has 18 memory devices **30** and the second rank **32***b* of FIG. **10**A has 18 memory devices **30**. Other numbers of memory devices **30** in each of the ranks **32***a*, **32***b* are also compatible with embodiments described herein.

In the embodiment schematically illustrated by FIG. **10**A, the memory module **10** has a width of 8 bytes (or 64 bits) and each of the memory devices **30** of FIG. **10**A has a bit width of 4 bits. The 4-bit-wide ("×4") memory devices **30** of FIG. **10**A have one-half the width, but twice the depth of 8-bit-wide ("×8") memory devices. Thus, each pair of "×4" memory devices **30** has the same density as a single "×8" memory device, and pairs of "×4" memory devices **30** can be used instead of individual "×8" memory devices to provide the memory density of the memory module **10**. For example, a pair of 512-Mb 128 M×4-bit memory devices has the same memory density as a 1-Gb 128 M×8-bit memory device.

For two "×4" memory devices **30** to work in tandem to mimic a "×8" memory device, the relative DQS pins of the two memory devices **30** in certain embodiments are advantageously tied together, as described more fully below. In addition, to access the memory density of a high-density memory module **10** comprising pairs of "×4" memory devices **30**, an additional address line is used. While a high-density memory module comprising individual "×8" memory devices with the next-higher density would also utilize an additional address line, the additional address lines are different in the two memory module configurations.

For example, a 1-Gb 128 M×8-bit DDR-1 DRAM memory device uses row addresses A_{13}-A_0 and column addresses A_{11} and A_9-A_0. A pair of 512-Mb 128 M×4-bit DDR-1 DRAM memory devices uses row addresses A_{12}-A_0 and column addresses A_{12}, A_{11}, and A_9-A_0. In certain embodiments, a memory controller of a computer system utilizing a 1-GB 128 M×8 memory module **10** comprising pairs of the 512-Mb 128 M×4 memory devices **30** supplies the address and command signals including the extra row address (AD) to the memory module **10**. The circuit **40** receives the address and command signals from the memory controller and converts the extra row address (A_{13}) into an extra column address (A_{12}).

FIG. **10**B schematically illustrates an exemplary circuit **40** compatible with embodiments described herein. The circuit **40** is used for a memory module **10** comprising pairs of "×4" memory devices **30** which mimic individual "×8" memory devices. In certain embodiments, each pair has the respective DQS pins of the memory devices **30** tied together. In certain embodiments, as schematically illustrated by FIG. **10**B, the circuit **40** comprises a programmable-logic device (PLD) **42**, a first multiplexer **44** electrically coupled to the first rank **32***a* of memory devices **30**, and a second multiplexer **46** electrically coupled to the second rank **32***b* of memory devices **30**. In certain embodiments, the PLD **42** and the first and second multiplexers **44**, **46** are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42**, first multiplexer **44**, and second multiplexer **46** in accordance with embodiments described herein.

In the exemplary circuit **40** of FIG. **10**B, during a row access procedure (CAS is high), the first multiplexer **44** passes the A_{12} address through to the first rank **32**, the second multiplexer **46** passes the A_{12} address through to the second rank **34**, and the PLD **42** saves or latches the A_{13} address from the memory controller. In certain embodiments, a copy of the A_{13} address is saved by the PLD **42** for each of the internal banks (e.g., 4 internal banks) per memory device **30**. During a subsequent column access procedure (CAS is low), the first multiplexer **44** passes the previously-saved A_{13} address through to the first rank **32***a* as the A_{12} address and the second multiplexer **46** passes the previously-saved A_{13} address through to the second rank **32***b* as the A_{12} address. The first rank **32***a* and the second rank **32***b* thus interpret the previously-saved A_{13} row address as the current A_{12} column address. In this way, in certain embodiments, the circuit **40** translates the extra row address into an extra column address in accordance with certain embodiments described herein.

Thus, by allowing two lower-density memory devices to be used rather than one higher-density memory device, certain embodiments described herein provide the advantage of using lower-cost, lower-density memory devices to build "next-generation" higher-density memory modules. Certain embodiments advantageously allow the use of lower-cost readily-available 512-Mb DDR-2 SDRAM devices to replace more expensive 1-Gb DDR-2 SDRAM devices. Certain embodiments advantageously reduce the total cost of the resultant memory module.

FIG. **11**A schematically illustrates an exemplary memory module **10** which doubles number of ranks in accordance with certain embodiments described herein. The memory module **10** has a first plurality of memory locations with a first memory density. The memory module **10** comprises a plurality of substantially identical memory devices **30** configured as a first rank **32***a*, a second rank **32***b*, a third rank **32***c*, and a fourth rank **32***d*. The memory module **10** further comprises a circuit **40** which receives a first set of address and command signals from a memory controller (not shown). The first set of address and command signals is compatible with a second plurality of memory locations having a second memory density. The second memory density is substantially equal to one-half of the first memory density. The circuit **40** translates the first set of address and command signals into a second set of address and command signals which is compatible with the first plurality of memory locations of the memory module **10** and which is transmitted to the first rank **32***a*, the second rank **32***b*, the third rank **32***c*, and the fourth rank **32***d*.

Each rank **32***a*, **32***b*, **32***c*, **32***d* of FIG. **11**A has 9 memory devices **30**. Other numbers of memory devices **30** in each of the ranks **32***a*, **32***b*, **32***c*, **32***d* are also compatible with embodiments described herein.

In the embodiment schematically illustrated by FIG. **11**A, the memory module **10** has a width of 8 bytes (or 64 bits) and each of the memory devices **30** of FIG. **11**A has a bit width of 8 bits. Because the memory module **10** has twice the number of 8-bit-wide ("×8") memory devices **30** as does a standard 8-byte-wide memory module, the memory module **10** has twice the density as does a standard 8-byte-wide memory module. For example, a 1-GB 128 M×8-byte memory module with 36 512-Mb 128 M×8-bit memory devices (arranged in four ranks) has twice the memory density as a 512-Mb 128 M×8-byte memory module with 18 512-Mb 128 M×8-bit memory devices (arranged in two ranks).

To access the additional memory density of the high-density memory module **10**, the two chip-select signals (CS_0, CS_1) are used with other address and command signals to gate a set of four gated CAS signals. For example, to access the additional ranks of four-rank 1-GB 128 M×8-byte DDR-1 DRAM memory module, the CS_0 and CS_1 signals along with the other address and command signals are used to gate the CAS signal appropriately, as schematically illustrated by FIG. **11**A. FIG. **11**B schematically illustrates an exemplary circuit **40** compatible with embodiments described herein. In certain embodiments, the circuit **40** comprises a programmable-logic device (PLD) **42** and four "OR" logic elements **52**, **54**, **56**, **58** electrically coupled to corresponding ranks **32***a*, **32***b*, **32***c*, **32***d* of memory devices **30**.

In certain embodiments, the PLD **42** comprises an ASIC, an FPGA, a custom-designed semiconductor device, or a CPLD. In certain embodiments, the PLD **42** and the four "OR" logic elements **52**, **54**, **56**, **58** are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42** and appropriate "OR" logic elements **52**, **54**, **56**, **58** in accordance with embodiments described herein.

In the embodiment schematically illustrated by FIG. **11**B, the PLD **42** transmits each of the four "enabled CAS" ($ENCAS_0a$, $ENCAS_0b$, $ENCAS_1a$, $ENCAS_1b$) signals to a corresponding one of the "OR" logic elements **52**, **54**, **56**, **58**. The CAS signal is also transmitted to each of the four "OR" logic elements **52**, **54**, **56**, **58**. The CAS signal and the "enabled CAS" signals are "low" true signals. By selectively activating each of the four "enabled CAS" signals which are inputted into the four "OR" logic elements **52**, **54**, **56**, **58**, the PLD **42** is able to select which of the four ranks **32***a*, **32***b*, **32***c*, **32***d* is active.

In certain embodiments, the PLD **42** uses sequential and combinatorial logic procedures to produce the gated CAS

signals which are each transmitted to a corresponding one of the four ranks **32***a*, **32***b*, **32***c*, **32***d*. In certain other embodiments, the PLD **42** instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS_0a, CS_0b, CS_1a, and CS_1b) which are each transmitted to a corresponding one of the four ranks **32***a*, **32***b*, **32***c*, **32***d*.

Tied Data Strobe Signal Pins

For proper operation, the computer system advantageously recognizes a 1-GB memory module comprising 256-Mb memory devices with 64 M×4-bit configuration as a 1-GB memory module having 512-Mb memory devices with 64 M×8-bit configuration (e.g., as a 1-GB memory module with 128 M×8-byte configuration). This advantageous result is desirably achieved in certain embodiments by electrically connecting together two output signal pins (e.g., DQS or data strobe pins) of the two 256-Mb memory devices such that both output signal pins are concurrently active when the two memory devices are concurrently enabled. The DQS or data strobe is a bi-directional signal that is used during both read cycles and write cycles to validate or latch data. As used herein, the terms "tying together" or "tied together" refer to a configuration in which corresponding pins (e.g., DQS pins) of two memory devices are electrically connected together and are concurrently active when the two memory devices are concurrently enabled (e.g., by a common chip-select or CS signal). Such a configuration is different from standard memory module configurations in which the output signal pins (e.g., DQS pins) of two memory devices are electrically coupled to the same source, but these pins are not concurrently active since the memory devices are not concurrently enabled. However, a general guideline of memory module design warns against tying together two output signal pins in this way.

FIGS. **12** and **13** schematically illustrate a problem which may arise from tying together two output signal pins. FIG. **12** schematically illustrates an exemplary memory module **305** in which a first DQS pin **312** of a first memory device **310** is electrically connected to a second DQS pin **322** of a second memory device **320**. The two DQS pins **312**, **322** are both electrically connected to a memory controller **330**.

FIG. **13** is an exemplary timing diagram of the voltages applied to the two DQS pins **312**, **322** due to non-simultaneous switching. As illustrated by FIG. **13**, at time t_1, both the first DQS pin **312** and the second DQS pin **322** are high, so no current flows between them. Similarly, at time t_4, both the first DQS pin **312** and the second DQS pin **322** are low, so no current flows between them. However, for times between approximately t_2 and approximately t_3, the first DQS pin **312** is low while the second DQS pin **322** is high. Under such conditions, a current will flow between the two DQS pins **312**, **322**. This condition in which one DQS pin is low while the other DQS pin is high can occur for fractions of a second (e.g., 0.8 nanoseconds) during the dynamic random-access memory (DRAM) read cycle. During such conditions, the current flowing between the two DQS pins **312**, **322** can be substantial, resulting in heating of the memory devices **310**, **320**, and contributing to the degradation of reliability and eventual failure of these memory devices.

A second problem may also arise from tying together two output signal pins. FIG. **14** schematically illustrates another exemplary memory module **305** in which a first DQS pin **312** of a first memory device **310** is electrically connected to a second DQS pin **322** of a second memory device **320**. The two DQS pins **312**, **322** of FIG. **14** are both electrically connected to a memory controller (not shown). The DQ (data input/output) pin **314** of the first memory device **310** and the corresponding DQ pin **324** of the second memory device **320** are each electrically connected to the memory controller by the DQ bus (not shown). Typically, each memory device **310**, **320** will have a plurality of DQ pins (e.g., eight DQ pins per memory device), but for simplicity, FIG. **14** only shows one DQ pin for each memory device **310**, **320**.

Each of the memory devices **310**, **320** of FIG. **14** utilizes a respective on-die termination or "ODT" circuit **332**, **334** which has termination resistors (e.g., 75 ohms) internal to the memory devices **310**, **320** to provide signal termination. Each memory device **310**, **320** has a corresponding ODT signal pin **362**, **364** which is electrically connected to the memory controller via an ODT bus **340**. The ODT signal pin **362** of the first memory device **310** receives a signal from the ODT bus **340** and provides the signal to the ODT circuit **332** of the first memory device **310**. The ODT circuit **332** responds to the signal by selectively enabling or disabling the internal termination resistors **352**, **356** of the first memory device **310**. This behavior is shown schematically in FIG. **14** by the switches **342**, **344** which are either closed (dash-dot line) or opened (solid line). The ODT signal pin **364** of the second memory device **320** receives a signal from the ODT bus **340** and provides the signal to the ODT circuit **334** of the second memory device **320**. The ODT circuit **334** responds to the signal by selectively enabling or disabling the internal termination resistors **354**, **358** of the second memory device **320**. This behavior is shown schematically in FIG. **14** by the switches **346**, **348** which are either closed (dash-dot line) or opened (solid line). The switches **342**, **344**, **346**, **348** of FIG. **14** are schematic representations of the operation of the ODT circuits **332**, **334**, and do not signify that the ODT circuits **332**, **334** necessarily include mechanical switches.

Examples of memory devices **310**, **320** which include such ODT circuits **332**, **334** include, but are not limited to, DDR2 memory devices. Such memory devices are configured to selectively enable or disable the termination of the memory device in this way in response to signals applied to the ODT signal pin of the memory device. For example, when the ODT signal pin **362** of the first memory device **310** is pulled high, the termination resistors **352**, **356** of the first memory device **310** are enabled. When the ODT signal pin **362** of the first memory device **310** is pulled low (e.g., grounded), the termination resistors **352**, **356** of the first memory device **310** are disabled. By selectively disabling the termination resistors of an active memory device, while leaving the termination resistors of inactive memory devices enabled, such configurations advantageously preserve signal strength on the active memory device while continuing to eliminate signal reflections at the bus-die interface of the inactive memory devices.

In certain configurations, as schematically illustrated by FIG. **14**, the DQS pins **312**, **322** of each memory device **310**, **320** are selectively connected to a voltage VTT through a corresponding termination resistor **352**, **354** internal to the corresponding memory device **310**, **320**. Similarly, in certain configurations, as schematically illustrated by FIG. **14**, the DQ pins **314**, **324** are selectively connected to a voltage VTT through a corresponding termination resistor **356**, **358** internal to the corresponding memory device **310**, **320**. In certain configurations, rather than being connected to a voltage VTT, the DQ pins **314**, **324** and/or the DQS pins **312**, **322** are selectively connected to ground through the corresponding termination resistors **352**, **354**, **356**, **358**. The resistances of the internal termination resistors **352**, **354**, **356**, **358** are

selected to clamp the voltages so as to reduce the signal reflections from the corresponding pins. In the configuration schematically illustrated by FIG. **14**, each internal termination resistor **352**, **354**, **356**, **358** has a resistance of approximately 75 ohms.

When connecting the first memory device **310** and, the second memory device **320** together to form a double word width, both the first memory device **310** and the second memory device **320** are enabled at the same time (e.g., by a common CS signal). Connecting the first memory device **310** and the second memory device **320** by tying the DQS pins **312**, **322** together, as shown in FIG. **14**, results in a reduced effective termination resistance for the DQS pins **312**, **322**. For example, for the exemplary configuration of FIG. **14**, the effective termination resistance for the DQS pins **312**, **322** is approximately 37.5 ohms, which is one-half the desired ODT resistance (for 75-ohm internal termination resistors) to reduce signal reflections since the internal termination resistors **352**, **354** of the two memory devices **310**, **320** are connected in parallel. This reduction in the termination resistance can result in signal reflections causing the memory device to malfunction.

FIG. **15** schematically illustrates an exemplary memory module **400** in accordance with certain embodiments described herein. The memory module **400** comprises a first memory device **410** having a first data strobe (DQS) pin **412** and a second memory device **420** having a second data strobe (DQS) pin **422**. The memory module **400** further comprises a first resistor **430** electrically coupled to the first DQS pin **412**. The memory module **400** further comprises a second resistor **440** electrically coupled to the second DQS pin **422** and to the first resistor **430**. The first DQS pin **412** is electrically coupled to the second DQS pin **422** through the first resistor **430** and through the second resistor **440**.

In certain embodiments, the memory module **400** is a 1-GB unbuffered Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) high-density dual in-line memory module (DIMM). FIGS. **16**A and **16**B schematically illustrate a first side **462** and a second side **464**, respectively, of such a memory module **400** with eighteen 64 M×4-bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board (PCB) **460**. In certain embodiments, the memory module **400** further comprises a phase-lock-loop (PLL) clock driver **470**, an EEPROM for serial-presence detect (SPD) data **480**, and decoupling capacitors (not shown) mounted on the PCB in parallel to suppress switching noise on VDD and VDDQ power supply for DDR-1 SDRAM. By using synchronous design, such memory modules **400** allow precise control of data transfer between the memory module **400** and the system controller. Data transfer can take place on both edges of the DQS signal at various operating frequencies and programming latencies. Therefore, certain such memory modules **400** are suitable for a variety of high-performance system applications.

In certain embodiments, the memory module **400** comprises a plurality of memory devices configured in pairs, each pair having a first memory device **410** and a second memory device **420**. For example, in certain embodiments, a 128 M×72-bit DDR SDRAM high-density memory module **400** comprises thirty-six 64 M×4-bit DDR-1 SDRAM integrated circuits in FBGA packages configured in eighteen pairs. The first memory device **410** of each pair has the first DQS pin **412** electrically coupled to the second DQS pin **422** of the second memory device **420** of the pair. In addition, the first DQS pin **412** and the second DQS pin **422** are concurrently active when the first memory device **410** and the second memory device **420** are concurrently enabled.

In certain embodiments, the first resistor **430** and the second resistor **440** each has a resistance advantageously selected to reduce the current flow between the first DQS pin **412** and the second DQS pin **422** while allowing signals to propagate between the memory controller and the DQS pins **412**, **422**. In certain embodiments, each of the first resistor **430** and the second resistor **440** has a resistance in a range between approximately 5 ohms and approximately 50 ohms. For example, in certain embodiments, each of the first resistor **430** and the second resistor **440** has a resistance of approximately 22 ohms. Other resistance values for the first resistor **430** and the second resistor **440** are also compatible with embodiments described herein. In certain embodiments, the first resistor **430** comprises a single resistor, while in other embodiments, the first resistor **430** comprises a plurality of resistors electrically coupled together in series and/or in parallel. Similarly, in certain embodiments, the second resistor **440** comprises a single resistor, while in other embodiments, the second resistor **440** comprises a plurality of resistors electrically coupled together in series and/or in parallel.

FIGS. **17**A and **17**B schematically illustrate an exemplary embodiment of a memory module **400** in which the first resistor **430** and the second resistor **440** are used to reduce the current flow between the first DQS pin **412** and the second DQS pin **422**. As schematically illustrated by FIG. **17**A, the memory module **400** is part of a computer system **500** having a memory controller **510**. The first resistor **430** has a resistance of approximately 22 ohms and the second resistor **440** has a resistance of approximately 22 ohms. The first resistor **430** and the second resistor **440** are electrically coupled in parallel to the memory controller **510** through a signal line **520** having a resistance of approximately 25 ohms. The first resistor **430** and the second resistor **440** are also electrically coupled in parallel to a source of a fixed termination voltage (identified by VTT in FIGS. **17**A and **17**B) by a signal line **540** having a resistance of approximately 47 ohms. Such an embodiment can advantageously be used to allow two memory devices having lower bit widths (e.g., 4-bit) to behave as a single virtual memory device having a higher bit width (e.g., 8-bit).

FIG. **17**B schematically illustrates exemplary current-limiting resistors **430**, **440** in conjunction with the impedances of the memory devices **410**, **420**. During an exemplary portion of a data read operation, the memory controller **510** is in a high-impedance condition, the first memory device **410** drives the first DQS pin **412** high (e.g., 2.7 volts), and the second memory device **420** drives the second DQS pin **422** low (e.g., 0 volts). The amount of time for which this condition occurs is approximated by the time between t_2 and t_3 of FIG. **13**, which in certain embodiments is approximately twice the tDQSQ (data strobe edge to output data edge skew time, e.g., approximately 0.8 nanoseconds). At least a portion of this time in certain embodiments is caused by simultaneous switching output (SSO) effects.

In certain embodiments, as schematically illustrated by FIG. **17**B, the DQS driver of the first memory device **410** has a driver impedance R_1 of approximately 17 ohms, and the DQS driver of the second memory device **420** has a driver impedance R_4 of approximately 17 ohms. Because the upper network of the first memory device **410** and the first resistor **430** (with a resistance R_2 of approximately 22 ohms) is approximately equal to the lower network of the second memory device **420** and the second resistor **440** (with a resistance R_3 of approximately 22 ohms), the voltage at the

midpoint is approximately 0.5*(2.7−0)=1.35 volts, which equals VTT, such that the current flow across the 47-ohm resistor of FIG. **17**B is approximately zero.

The voltage at the second DQS pin **422** in FIG. **17**B is given by $V_{DQS2}=2.7*R_4/(R_1+R_2+R_3+R_4)=0.59$ volts and the current flowing through the second DQS pin **422** is given by $I_{DQS2}=0.59/R_4=34$ milliamps. The power dissipation in the DQS driver of the second memory device **420** is thus $P_{DQS2}=34$ mA*0.59 V=20 milliwatts. In contrast, without the first resistor **430** and the second resistor **440**, only the 17-ohm impedances of the two memory devices **410**, **420** would limit the current flow between the two DQS pins **412**, **422**, and the power dissipation in the DQS driver of the second memory device **420** would be approximately 107 milliwatts. Therefore, the first resistor **430** and the second resistor **440** of FIGS. **17**A and **17**B advantageously limit the current flowing between the two memory devices during the time that the DQS pin of one memory device is driven high and the DQS pin of the other memory device is driven low.

In certain embodiments in which there is overshoot or undershoot of the voltages, the amount of current flow can be higher than those expected for nominal voltage values. Therefore, in certain embodiments, the resistances of the first resistor **430** and the second resistor **440** are advantageously selected to account for such overshoot/undershoot of voltages.

For certain such embodiments in which the voltage at the second DQS pin **422** is $V_{DQS2}=0.59$ volts and the duration of the overdrive condition is approximately 0.8 nanoseconds at maximum, the total surge is approximately 0.59 V*1.2 ns=0.3 V-ns. For comparison, the JEDEC standard for overshoot/undershoot is 2.4 V-ns, so certain embodiments described herein advantageously keep the total surge within predetermined standards (e.g., JEDEC standards).

FIG. **18** schematically illustrates another exemplary memory module **600** compatible with certain embodiments described herein. The memory module **600** comprises a termination bus **605**. The memory module **600** further comprises a first memory device **610** having a first data strobe pin **612**, a first termination signal pin **614** electrically coupled to the termination bus **605**, a first termination circuit **616**, and at least one data pin **618**. The first termination circuit **616** selectively electrically terminating the first data strobe pin **612** and the first data pin **618** in response to a first signal received by the first termination signal pin **614** from the termination bus **605**. The memory module **600** further comprises a second memory device **620** having a second data strobe pin **622** electrically coupled to the first data strobe pin **612**, a second termination signal pin **624**, a second termination circuit **626**, and at least one data pin **628**. The second termination signal pin **624** is electrically coupled to a voltage, wherein the second termination circuit **626** is responsive to the voltage by not terminating the second data strobe pin **622** or the second data pin **628**. The memory module **600** further comprises at least one termination assembly **630** having a third termination signal pin **634**, a third termination circuit **636**, and at least one termination pin **638** electrically coupled to the data pin **628** of the second memory device **620**. The third termination signal pin **634** is electrically coupled to the termination bus **605**. The third termination circuit **636** selectively electrically terminates the data pin **628** of the second memory device **620** through the termination pin **638** in response to a second signal received by the third termination signal pin **634** from the termination bus **605**.

FIG. **19** schematically illustrates a particular embodiment of the memory module **600** schematically illustrated by FIG. **18**. The memory module **600** comprises an on-die termination (ODT) bus **605**. The memory module **600** comprises a first memory device **610** having a first data strobe (DQS) pin **612**, a first ODT signal pin **614** electrically coupled to the ODT bus **605**, a first ODT circuit **616**, and at least one data (DQ) pin **618**. The first ODT circuit **616** selectively electrically terminates the first DQS pin **612** and the DQ pin **618** of the first memory device **610** in response to an ODT signal received by the first ODT signal pin **614** from the ODT bus **605**. This behavior of the first ODT circuit **616** is schematically illustrated in FIG. **14** by the switches **672**, **676** which are selectively closed (dash-dot line) or opened (solid line).

The memory module **600** further comprises a second memory device **620** having a second DQS pin **622** electrically coupled to the first DQS pin **612**, a second ODT signal pin **624**, a second ODT circuit **626**, and at least one DQ pin **628**. The first DQS pin **612** and the second DQS pin **622** are concurrently active when the first memory device **610** and the second memory device **620** are concurrently enabled. The second ODT signal pin **624** is electrically coupled to a voltage (e.g., ground), wherein the second ODT circuit **626** is responsive to the voltage by not terminating the second DQS pin **622** or the second DQ pin **624**. This behavior of the second ODT circuit **626** is schematically illustrated in FIG. **14** by the switches **674**, **678** which are opened.

The memory module **600** further comprises at least one termination assembly **630** having a third ODT signal pin **634** electrically coupled to the ODT bus **605**, a third ODT circuit **636**, and at least one termination pin **638** electrically coupled to the DQ pin **628** of the second memory device **620**. The third ODT circuit **636** selectively electrically terminates the DQ pin **628** of the second memory device **620** through the termination pin **638** in response to an ODT signal received by the third ODT signal pin **634** from the ODT bus **605**. This behavior of the third ODT circuit **636** is schematically illustrated in FIG. **19** by the switch **680** which is either closed (dash-dot line) or opened (solid line).

In certain embodiments, the termination assembly **630** comprises discrete electrical components which are surface-mounted or embedded on the printed-circuit board of the memory module **600**. In certain other embodiments, the termination assembly **630** comprises an integrated circuit mounted on the printed-circuit board of the memory module **600**. Persons skilled in the art can provide a termination assembly **630** in accordance with embodiments described herein.

Certain embodiments of the memory module **600** schematically illustrated by FIG. **19** advantageously avoid the problem schematically illustrated by FIG. **12** of electrically connecting the internal termination resistances of the DQS pins of the two memory devices in parallel. As described above in relation to FIG. **14**, FIGS. **18** and **19** only show one DQ pin for each memory device for simplicity. Other embodiments have a plurality of DQ pins for each memory device. In certain embodiments, each of the first ODT circuit **616**, the second ODT circuit **626**, and the third ODT circuit **636** are responsive to a high voltage or signal level by enabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by disabling the corresponding termination resistors. In other embodiments, each of the first ODT circuit **616**, the second ODT circuit **626**, and the third ODT circuit **636** are responsive to a high voltage or signal level by disabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by enabling the corresponding termination resistors. Furthermore, the switches **672**, **674**, **676**, **678**, **680** of FIG. **18** are schematic

representations of the enabling and disabling operation of the ODT circuits **616**, **626**, **636** and do not signify that the ODT circuits **616**, **626**, **636** necessarily include mechanical switches.

The first ODT signal pin **614** of the first memory device **610** receives an ODT signal from the ODT bus **605**. In response to this ODT signal, the first ODT circuit **616** selectively enables or disables the termination resistance for both the first DQS pin **612** and the DQ pin **618** of the first memory device **610**. The second ODT signal pin **624** of the second memory device **620** is tied (e.g., directly hard-wired) to the voltage (e.g., ground), thereby disabling the internal termination resistors **654**, **658** on the second DQS pin **622** and the second DQ pin **628**, respectively, of the second memory device **620** (schematically shown by open switches **674**, **678** in FIG. **19**). The second DQS pin **622** is electrically coupled to the first DQS pin **612**, so the termination resistance for both the first DQS pin **612** and the second DQS pin **622** is provided by the termination resistor **652** internal to the first memory device **510**.

The termination resistor **656** of the DQ pin **618** of the first memory device **610** is enabled or disabled by the ODT signal received by the first ODT signal pin **614** of the first memory device **610** from the ODT bus **605**. The termination resistance of the DQ pin **628** of the second memory device **620** is enabled or disabled by the ODT signal received by the third ODT signal pin **634** of the termination assembly **630** which is external to the second memory device **620**. Thus, in certain embodiments, the first ODT signal pin **614** and the third ODT signal pin **634** receive the same ODT signal from the ODT bus **605**, and the termination resistances for both the first memory device **610** and the second memory device **620** are selectively enabled or disabled in response thereto when these memory devices are concurrently enabled. In this way, certain embodiments of the memory module **600** schematically illustrated by FIG. **19** provides external or off-chip termination of the second memory device **620**.

Certain embodiments of the memory module **600** schematically illustrated by FIG. **19** advantageously allow the use of two lower-cost readily-available 512-Mb DDR-2 SDRAM devices to provide the capabilities of a more expensive 1-GB DDR-2 SDRAM device. Certain such embodiments advantageously reduce the total cost of the resultant memory module **600**.

Certain embodiments described herein advantageously increase the memory capacity or memory density per memory slot or socket on the system board of the computer system. Certain embodiments advantageously allow for higher memory capacity in systems with limited memory slots. Certain embodiments advantageously allow for flexibility in system board design by allowing the memory module **10** to be used with computer systems designed for different numbers of ranks (e.g., either with computer systems designed for two-rank memory modules or with computer systems designed for four-rank memory modules). Certain embodiments advantageously provide lower costs of board designs.

In certain embodiments, the memory density of a memory module is advantageously doubled by providing twice as many memory devices as would otherwise be provided. For example, pairs of lower-density memory devices can be substituted for individual higher-density memory devices to reduce costs or to increase performance. As another example, twice the number of memory devices can be used to produce a higher-density memory configuration of the memory module. Each of these examples can be limited by the number of chip select signals which are available from the memory controller or by the size of the memory devices. Certain embodiments described herein advantageously provide a logic mechanism to overcome such limitations.

Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

We claim:

1. A memory module operable in a computer system to communicate data with a memory controller of the computer system at a specified data rate via a N-bit wide data bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first burst of N-bit wide data signals and a first burst of data strobes and the second memory command to cause the memory module to receive or output a second burst of N-bit wide data signals and a second burst of data strobes, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks include a first rank configured to receive or output the first burst of N-bit wide data signals and the first burst of data strobes at the specified data rate in response to the first memory command, and a second rank configured to receive or output the second burst of N-bit wide data signals and the second burst of data strobes at the specified data rate in response to the second memory command;

circuitry coupled between the plurality of N-bit wide ranks and the N-bit wide data bus; and

logic coupled to the circuitry and configured to respond to the first memory command by providing first control signals to the circuitry and to subsequently respond to the second memory command by providing second control signals to the circuitry, wherein the circuitry is configured to enable data transfers through the circuitry in response to the first control signals and subsequently in response to the second control signals, wherein respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred at the specified data rate between the first rank and the N-bit wide data bus through the circuitry, and wherein respective N-bit wide data signals of the second burst of N-bit wide data signals and respective data strobes of the second burst of data strobes are transferred at the specified data rate between the second rank and the N-bit wide data bus through the circuitry;

wherein the data transfers through the circuitry are registered data transfers enabled in accordance with an overall CAS latency of the memory module, and the circuitry is configured to add a predetermined amount of time delay for each registered data transfer through the circuitry so that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.

2. The memory module of claim 1, wherein each of the plurality memory integrated circuits has a corresponding load, and wherein the circuitry is configured to isolate the loads of the plurality of memory integrated circuits from the memory controller.

3. The memory module of claim 1, wherein the logic is coupled to the printed circuit board and is further configured to receive from the memory controller a first set of input address and control signals associated with the first memory command and to respond to the first memory command by outputting a first set of registered address and control signals, and wherein the logic is further configured to subsequently receive from the memory controller a second set of input address and control signals associated with the second memory command and to respond to the second memory command by outputting a second set of registered address and control signals, the first set of input address and control signals including a first set of input chip select signals corresponding to respective ranks of the plurality of ranks and the second set of input address and control signals including a second set of input chip select signals corresponding to respective ranks of the plurality of ranks, the first set of registered address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals, the second set of registered address and control signals including a second plurality of registered chip select signals corresponding to respective ones of the second plurality of input chip select signals, the first set of registered chip select signals including a first registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value, the second set of registered chip select signals including a second registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value, and wherein the logic is configured to output the first registered chip select signal to the first rank and to output the second registered chip select signal to the second rank.

4. The memory module of claim 1, further comprising an SPD device that reports the overall CAS latency of the memory module to the memory controller.

5. The memory module of claim 1, wherein the memory module is configured to receive from the memory controller an on-die-termination (ODT) signal, wherein each of the plurality of memory integrated circuits includes an ODT circuit, the memory module further comprising a termination circuit external to any of the plurality of memory integrated circuits, wherein the termination circuit is configured to receive the ODT signal and is coupled to the ODT circuit of at least one of the plurality of memory integrated circuits, wherein the termination circuit is configured to provide external termination for the at least one of the plurality of memory integrated circuits in response to the ODT signal, and wherein the ODT circuit of the at least one of the plurality of memory integrated circuits is disabled.

6. The memory module of claim 1, wherein the circuitry includes logic pipelines configured to enable the data transfers through the circuitry in response to the first control signals and subsequently in response to the second control signals.

7. The memory module of claim 1, wherein the logic is further configured to determine the overall CAS latency of the memory module.

8. The memory module of claim 1, wherein N is 64 or 72.

9. The memory module of claim 1, wherein each rank of the plurality of ranks is 72-bits wide, wherein each rank of the plurality of N-bit wide ranks includes 18 4-bit wide memory integrated circuits configured in 9 pairs, wherein a first pair of memory integrated circuits in the first rank is configured to communicate a respective byte of the first burst of N-bit wide data signals in each time interval of a first plurality of time intervals, and wherein a second pair of memory integrated circuits in the second rank is configured to communicate a respective byte of the second burst of N-bit wide data signals in each time interval of a second plurality of time intervals.

10. The memory module of claim 9, wherein the first pair of memory integrated circuits are configured to simulate an 8-bit wide memory device, and the second pair of memory integrated circuits are configured to simulate another 8-bit wide memory device.

11. The memory module of claim 9, further comprising an SPD device programmed with data to characterize each pair of memory integrated circuits as a virtual 8-bit wide memory device.

12. The memory module of claim 1, wherein the respective N-bit wide data signals of the first burst of N-bit wide data signals and the respective data strobes of the first burst of data strobes are transferred through the circuitry during respective time intervals of a first plurality of time intervals, and wherein the respective N-bit wide data signals of the second burst of N-bit wide data signals and the respective data strobes of the second burst of data strobes are transferred through the circuitry during respective time intervals of a second plurality of time intervals.

13. The memory module of claim 1, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.

14. The memory module of claim 13, wherein the memory integrated circuits are dynamic random access memory integrated circuits configured to operate synchronously with the clock signal, wherein each memory integrated circuit in the first rank is configured receive or output a respective set of bits of the first burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the first burst of data strobes, and wherein each memory integrated circuit in the second rank is configured receive or output a respective set of bits of the second burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the second burst of data strobes.

15. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to receive a first set of input address and control signals associated with a first read or write memory command and to output a first set of registered address and control signals in response to the first set of input address and control signals, the first set of input address and control signals including a first plurality of input chip select signals, the first set of registered address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals, the first plurality of registered chip select signals including a

first registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks are configured to receive respective ones of the first plurality of registered chip select signals, wherein a first N-bit wide rank in the plurality of N-bit wide ranks receiving the first registered chip select signal having the active signal value is configured to receive or output a first burst of N-bit wide data signals and a first burst of data strobes associated with the first read or write command;

circuitry coupled between data and strobe signal lines in the N-bit wide memory bus and corresponding data and strobe pins of memory devices in each of the plurality of N-bit wide ranks; and

wherein the logic is further configured to, in response to the first read or write memory command, output first control signals to the circuitry, and wherein the circuitry is configured to enable data transfers between the first rank and the memory bus through the circuitry in response to the first control signals so that respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred through the circuitry in accordance with an overall CAS latency of the memory module; and

wherein the data transfers between the first rank and the memory bus through the circuitry are registered data transfers and the circuitry is configured to add a predetermined amount of time delay for each registered data transfer through the circuitry such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

16. The memory module of claim **15**, wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus.

17. The memory module of claim **15**, wherein the first burst of N-bit wide data signals includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein the set of consecutively transmitted data bits are successively transferred through the circuitry in response to the first control signals.

18. The memory module of claim **15**, wherein each of the memory devices is 4-bits wide, and wherein each of the plurality of ranks is 72-bits wide and includes 18 memory devices configured in pairs, and wherein each pair of 4-bit-wide memory devices are configured to simulate an 8-bit-wide memory device.

19. The memory module of claim **15**, wherein the memory devices are organized in four ranks and the first set of input address and control signals include four chip select signals, one for each of the four ranks.

20. The memory module of claim **15**, wherein the circuitry includes logic pipelines configured to enable the data transfers between the first rank and the memory bus through the circuitry in response to the first control signals.

21. The memory module of claim **15**, wherein the logic is further configured to report the overall CAS latency to the memory controller in response to a mode register set command received from the memory controller.

22. The memory module of claim **15**, wherein the first burst of N-bit wide data signals and the first burst of data strobes are transferred between the first N-bit wide rank and the memory controller at a specified data rate.

23. The memory module of claim **15**, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.

24. The memory module of claim **23**, wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the first rank is configured receive or output a respective set of bits of the first burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the first burst of data strobes.

25. The memory module of claim **15**, wherein the logic is further configured to respond to a second set of input address and control signals associated with a second read or write memory command by outputting a second set of registered address and control signals, the second set of input address and control signals including a second plurality of input chip select signals, the second set of registered address and control signals including a second plurality of registered chip select signals corresponding to respective ones of the second plurality of input chip select signals, the second plurality of registered chip select signals including a second registered chip select signal having the active signal value and one or more other registered chip select signals each having the non-active signal value, wherein a second rank different from the first rank is configured to receive the second registered chip select signal having the active signal value and to output or receive a second burst of N-bit wide data signals and a second burst of data strobes associated with the second read or write command, wherein the logic is further configured to, in response to the second read or write memory command, output second control signals to the circuitry, and wherein the circuitry is configured to enable registered data transfers between the second rank and the memory bus through the circuitry in response to the second control signals so that the second burst of N-bit wide data signals and the second burst of data strobes are transferred between the second rank and the memory controller through the circuitry in accordance with the overall CAS latency of the memory module.

26. The memory module of claim **17**, wherein the first burst of N-bit wide data signals is transferred through the circuitry in a plurality of time intervals including at least a first time interval and a last time interval, wherein the circuitry includes a set of signal paths that are enabled before the first time interval and subsequently disabled after the last time interval.

27. The memory module of claim **26**, wherein:

the first read or write memory command is a read memory command;

the second read or write memory command is a write memory command;

the set of signal paths are enabled to transfer the first burst of N-bit wide data signals and the first burst of data strobes a first number of time intervals after the read memory command is received by the logic; and

the set of signal paths are enabled to transfer the second burst of N-bit wide data signals and the second burst of data strobes a second number of time intervals after the write memory command is received by the logic, the second number being different from the first number.

28. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or

write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to receive a set of input control and address signals associated with a read or write memory command via the memory bus and to output a set of registered control and address signals in response to the set of input control and address signals, the set of input control and address signals including a plurality of input chip select signals, the set of registered control and address signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals, the plurality of registered chip select signals including a registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks are configured to receive respective ones of the plurality of registered chip select signals, wherein a first N-bit wide rank receiving the registered chip select signal having the active signal value is configured to receive or output a first burst of N-bit wide data signals and a first burst of data strobes associated with the read/write command;

circuitry between data and data strobe signal lines in the memory bus and corresponding data and data strobe pins of the memory devices, wherein the circuitry includes logic pipelines configured to enable data transfers between the first rank and the memory bus in response to the first read or write memory command, wherein respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred between the first rank and the memory bus through the circuitry in accordance with an overall CAS latency of the memory module; and

wherein the data transfers between the first rank and the memory bus are registered data transfers; and

wherein the circuitry is configured to add a predetermined amount of time delay for each data transfer between the memory controller and the memory devices such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

29. The memory module of claim **28**, wherein the first burst of N-bit wide data signals includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein the circuitry includes a set of signal paths that are enabled before a first data bit of the set of consecutively transmitted data bits is transferred through the circuitry and disabled after a last data bit of the set of consecutively transmitted data bits is transferred through the circuitry.

30. The memory module of claim **28**, wherein the logic is further configured to respond to a subsequent set of input address and control signals associated with a subsequent read or write memory command by outputting a subsequent set of registered address and control signals, the subsequent set of input address and control signals including a subsequent plurality of input chip select signals, the subsequent set of registered address and control signals including a subsequent plurality of registered chip select signals corresponding to respective ones of the subsequent plurality of input chip select signals, the subsequent plurality of registered chip select signals including a subsequently registered chip select signal having the active signal value and one or more other subsequently registered chip select signals each having the non-active signal value, wherein a second rank different from the first rank is configured to receive the subsequently registered chip select signal having the active signal value and to output or receive a second burst of N-bit wide data signals and a second burst of data strobes associated with the subsequent read or write command, wherein the circuitry is further configured to enable registered data transfers between the memory devices and the memory bus in response to the subsequent read/write memory command so that the second burst of N-bit wide data signals and the second burst of data strobes are transferred between the second rank and the memory bus through the circuitry.

31. The memory module of claim **28**, wherein the first burst of N-bit wide data signals and the first burst of data strobes are transferred between the first N-bit wide rank and the memory controller at a specified data rate.

32. The memory module of claim **28**, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.

33. The memory module of claim **32**, wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the first rank is configured receive or output a respective set of bits of the first burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the first burst of data strobes.

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 10,489,314 B2
APPLICATION NO. : 15/857519
DATED : November 26, 2019
INVENTOR(S) : Solomon et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims

Claim 2, Column 43, Line 2, please delete "plurality memory" and insert --plurality of memory--;

Claim 14, Column 44, Line 39, please delete "configured receive" and insert --configured to receive--;

Claim 14, Column 44, Line 43, please delete "configured receive" and insert --configured to receive--;

Claim 33, Column 48, Lines 45-46, please delete "configured receive" and insert --configured to receive--.

Signed and Sealed this
Seventeenth Day of March, 2020

Andrei Iancu
Director of the United States Patent and Trademark Office