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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NETL.018P2C8
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
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Inventor 1 Remove

Legal Name

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	Jeffrey	C.	Solomon	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

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Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

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Application Information:

Title of the Invention	MEMORY MODULE WITH DATA BUFFERING		
Attorney Docket Number	NETL.018P2C8	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	23	**Suggested Figure for Publication (if any)**	8D

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☒ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Customer Number	79141		

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Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	13971231	2013-08-20

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Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13971231	Continuation of	13287081	2011-11-01	8516188	2013-08-20
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13287081	Continuation of	13032470	2011-02-22	8081536	2011-12-20
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13032470	Continuation of	12955711	2010-11-29	7916574	2011-03-29
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12955711	Continuation of	12629827	2009-12-02	7881150	2011-02-01
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12629827	Continuation of	12408652	2009-03-20	7636274	2009-12-22
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12408652	Continuation of	11335875	2006-01-19	7532537	2009-05-12
Prior Application Status	Expired			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11335875	non provisional of	60645087	2005-01-19		
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11335875	Continuation in part of	11173175	2005-07-01	7289386	2007-10-30
Prior Application Status	Expired			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11173175	non provisional of	60588244	2004-07-15		
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11173175	Continuation in part of	11075395	2005-03-07	7286436	2007-10-23
Prior Application Status	Expired			Remove	

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Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
11075395	non provisional of	60550668	2004-03-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
11075395	non provisional of	60575595	2004-05-28
Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
11075395	non provisional of	60590038	2004-07-21

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Application Number	Country i	Filing Date (YYYY-MM-DD)	Priority Claimed
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NETL.018P2C8
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

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Clear

(•) Assignee	( ) Legal Representative under 35 U.S.C. 117	( ) Joint Inventor
( ) Person to whom the inventor is obligated to assign.	( ) Person who shows sufficient proprietary interest	

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Name of the Deceased or Legally Incapacitated Inventor :

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Signature	/Jamie J. Zheng/			Date (YYYY-MM-DD)	2015-05-18
First Name	Jamie	Last Name	Zheng	Registration Number	51167

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MEMORY MODULE WITH DATA BUFFERING

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a continuation of U.S. Pat. Appl. No. 13/971,231, filed August 20, 2013, which is a continuation of U.S. Pat. Appl. No. 13/287,081, filed November 1, 2011, now U.S. Pat. No. 8,516,188, which is a continuation of U.S. Pat. Appl. No. 13/032,470, filed February 22, 2011, now U.S. Pat. No. 8,081,536, which is a continuation of U.S. Pat. Appl. No. 12/955,711, filed November 29, 2010, now U.S. Pat. No. 7,916,574, which is a continuation of U.S. Pat. Appl. No. 12/629,827, filed December 2, 2009, now U.S. Pat. No. 7,881,150, which is a continuation of U.S. Pat. Appl. No. 12/408,652, filed March 20, 2009, now U.S. Pat. No. 7,636,274, which is a continuation of U.S. Pat. Appl. No. 11/335,875, filed January 19, 2006, now U.S. Pat. No. 7,532,537, which claims the benefit of U.S. Provisional Appl. No. 60/645,087, filed January 19,2005 and which is a continuation-in-part of U.S. Pat. Appl. No. 11/173,175, filed July 1,2005, now U.S. Pat. No. 7,289,386, which claims the benefit of U.S. Provisional Appl. No. 60/588,244, filed July 15, 2004 and which is a continuation-in-part of U.S. Pat. Appl. No. 11/075,395, filed March 7, 2005, now U.S. Pat. No. 7,286,436, which claims the benefit of U.S. Provisional Appl. No. 60/550,668, filed March 5, 2004, U.S. Provisional Appl. No. 60/575,595, filed May 28, 2004, and U.S. Provisional Appl. No. 60/590,038, filed July 21, 2004. U.S. Pat. Appl. Nos. 13/287,081, 13/032,470, 12/955,711, 12/629,827, 12/408,652, 11/335,875, 11/173,175, and 11/075,395, and U.S. Provisional Appl. Nos. 60/550,668, 60/575,595, 60/590,038, 60/588,244, and 60/645,087 are each incorporated in its entirety by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules.

2. Description of the Related Art

[0003] Certain types of memory modules comprise a plurality of dynamic

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random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the processor of the computer system. Memory modules typically have a memory configuration with a unique combination of rows, columns, and banks which result in a total memory capacity for the memory module.

[0004] For example, a 512-Megabyte memory module (termed a "512-MB" memory module, which actually has 2^{29} or 536,870,912 bytes of capacity) will typically utilize eight 512-Megabit DRAM devices (each identified as a "512-Mb" DRAM device, each actually having 2^{29} or 536,870,912 bits of capacity). The memory cells (or memory locations) of each 512-Mb DRAM device can be arranged in four banks, with each bank having an array of 2^{24} (or 16,777,216) memory locations arranged as 2^{13} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 64 M 8-bit-wide memory locations (actually with four banks of 2^{27} or 134,217,728 one-bit memory cells arranged to provide a total of 2^{26} or 67,108,864 memory locations with 8 bits each) are identified as having a "64 Mb×8" or "64 M×8-bit" configuration, or as having a depth of 64 M and a bit width of 8. Furthermore, certain commercially-available 512-MB memory modules are termed to have a "64 M×8-byte" configuration or a "64 M×64-bit" configuration with a depth of 64 M and a width of 8 bytes or 64 bits.

[0005] Similarly, a 1-Gigabyte memory module (termed a "1-GB" memory module, which actually has 2^{30} or 1,073,741,824 bytes of capacity) can utilize eight 1-Gigabit DRAM devices (each identified as a "1-Gb" DRAM device, each actually having 2^{30} or 1,073,741,824 bits of capacity). The memory locations of each 1-Gb DRAM device can be arranged in four banks, with each bank having an array of memory locations with 2^{14} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 128 M 8-bit-wide memory locations (actually with a total of 2^{27} or 134,217,728 memory locations with 8 bits each) are identified as having a "128 Mb×8" or "128 M×8-bit" configuration, or as having a depth of 128 M and a bit width of 8. Furthermore, certain commercially-available 1-GB memory modules are identified as having a "128 M×8-byte" configuration or a "128 M×64-bit" configuration with a depth of 128 M and a width of 8 bytes or 64 bits.

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[0006] The commercially-available 512-MB (64 M×8-byte) memory modules and the 1-GB (128 M×8-byte) memory modules described above are typically used in computer systems (e.g., personal computers) which perform graphics applications since such "×8" configurations are compatible with data mask capabilities often used in such graphics applications. Conversely, memory modules with "×4" configurations are typically used in computer systems such as servers which are not as graphics-intensive. Examples of such commercially available "×4" memory modules include, but are not limited to, 512-MB (128 M×4-byte) memory modules comprising eight 512-Mb (128 Mb×4) memory devices.

[0007] The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "×64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "×72" organization.

[0008] The memory capacity of a memory module increases with the number of memory devices. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks. For example, a memory module with four ranks has double the memory capacity of a memory module with two ranks and four times the memory capacity of a memory module with one rank. Rather than referring to the memory capacity of the memory module, in certain circumstances, the memory density of the memory module is referred to instead.

[0009] During operation, the ranks of a memory module are selected or activated by address and command signals that are received from the processor. Examples of such address and command signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support one-rank and two-rank memory modules. By only supporting one-rank and two-rank memory modules, the memory density that can be incorporated in each memory slot is limited.

[0010] Various aspects of the design of a memory module impose limitations on the size of the memory arrays of the memory module. Certain such aspects are particularly important for memory modules designed to operate at higher frequencies. Examples of such aspects include, but are not limited to, memory device (e.g., chip) densities, load fan-out, signal integrity, available rank selects, power dissipation, and thermal profiles.

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SUMMARY OF THE INVENTION

[0011] In certain embodiments, a memory module is operable to communicate data with a memory controller via a data bus in response to memory commands received from the memory controller. The memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst. The memory module comprises a plurality of memory integrated circuits including at least one first memory integrated circuit and at least one second memory integrated circuit, and further comprises a buffer coupled between the at least one first memory integrated circuit and the data bus, and between the at least one second memory integrated circuit and the data bus. The buffer couples the at least one first memory integrated circuit to the data bus and isolates the at least one second memory integrated circuit from the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command. The buffer then couples the at least one second memory integrated circuit to the data bus and isolates the at least one first memory integrated circuit from the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command.

[0012] Certain embodiments provide a method of operating a memory module coupled to a memory controller via a memory bus that includes a control/address (C/A) bus and a data bus. The memory module comprises memory integrated circuits, including at least one first memory integrated circuit and at least one second memory integrated circuit. The method comprises receiving from the memory controller a first set of input C/A signals associated with a first memory command via the C/A bus, the first memory command to cause the memory module to receive or output a first data burst; generating a first set of output C/A signals in response to the first set of input C/A signals, the first set of output C/A signals causing the at least one first memory integrated circuit to receive or output the first data burst; receiving from the memory controller a second set of input control/address signals associated with a second memory command via the C/A bus, the second memory command to cause the memory module to receive or output a second data burst; generating a second set of output C/A signals in response to the second set of input C/A signals, the second set of output C/A signals causing the at least one second memory integrated circuit to receive or

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output the second data burst; coupling the at least one first memory integrated circuit to the data bus and isolating the at least one second memory integrated circuit from the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command; and coupling the at least one second memory integrated circuit to the data bus and isolating the at least one first memory integrated circuit from the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command.

[0013] In certain embodiments, a circuit is configured to be mounted on a memory module that is operable to communicate data with a memory controller via a data bus in response to memory commands received from the memory controller. The memory module including at least one first memory integrated circuit and at least one second memory integrated circuit. The memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the at least one first memory integrated circuit to receive or output a first data burst and the second memory command to cause the at least one second memory integrated circuit to receive or output a second data burst. The circuit comprises logic that couples the at least one first memory integrated circuit to the data bus and that isolates the at least one second memory integrated circuit from the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command. The logic then couples the at least one second memory integrated circuit to the data bus and isolates the at least one first memory integrated circuit from the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. 1 schematically illustrates an example memory module in accordance with certain embodiments described herein.

[0015] FIG. 2 schematically illustrates a circuit diagram of two memory devices of a conventional memory module.

[0016] FIGS. 3A and 3B schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two memory devices from the computer system in accordance with certain embodiments

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described herein.

[0017] FIGS. 4A and 4B schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two ranks of memory devices from the computer system in accordance with certain embodiments described herein.

[0018] FIGS. 5A-5D schematically illustrate example memory modules having a circuit comprising a logic element and one or more switches operatively coupled to the logic element in accordance with certain embodiments described herein.

[0019] FIG. 6A shows an exemplary timing diagram of a gapless read burst for a back-to-back adjacent read condition from one memory device.

[0020] FIG. 6B shows an exemplary timing diagram with an extra clock cycle between successive read commands issued to different memory devices for successive read accesses from different memory devices.

[0021] FIG. 7 shows an exemplary timing diagram in which the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b."

[0022] FIGS. 8A-8D schematically illustrate circuit diagrams of example memory modules comprising a circuit which multiplexes the DQS data strobe signal lines from one another in accordance with certain embodiments described herein.

[0023] FIG. 9A schematically illustrates an example memory module with four ranks of memory devices compatible with certain embodiments described herein.

[0024] FIG. 9B schematically illustrates an example memory module with two ranks of memory devices compatible with certain embodiments described herein.

[0025] FIG. 9C schematically illustrates another example memory module in accordance with certain embodiments described herein.

[0026] FIG. 10A schematically illustrates an exemplary memory module which doubles the rank density in accordance with certain embodiments described herein.

[0027] FIG. 10B schematically illustrates an exemplary circuit compatible with embodiments described herein.

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[0028] FIG. 11A schematically illustrates an exemplary memory module which doubles number of ranks in accordance with certain embodiments described herein.

[0029] FIG. 11B schematically illustrates an exemplary circuit compatible with embodiments described herein.

[0030] FIG. 12 schematically illustrates an exemplary memory module in which a data strobe (DQS) pin of a first memory device is electrically connected to a DQS pin of a second memory device while both DQS pins are active.

[0031] FIG. 13 is an exemplary timing diagram of the voltages applied to the two DQS pins due to non-simultaneous switching.

[0032] FIG. 14 schematically illustrates another exemplary memory module in which a DQS pin of a first memory device is connected to a DQS pin of a second memory device.

[0033] FIG. 15 schematically illustrates an exemplary memory module in accordance with certain embodiments described herein.

[0034] FIGS. 16A and 16B schematically illustrate a first side and a second side, respectively, of a memory module with eighteen 64 M×4 bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board.

[0035] FIGS. 17A and 17B schematically illustrate an exemplary embodiment of a memory module in which a first resistor and a second resistor are used to reduce the current flow between the first DQS pin and the second DQS pin.

[0036] FIG. 18 schematically illustrates another exemplary memory module compatible with certain embodiments described herein.

[0037] FIG. 19 schematically illustrates a particular embodiment of the memory module schematically illustrated by FIG. 18.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Load Isolation

[0038] FIG. 1 schematically illustrates an example memory module **10** compatible with certain embodiments described herein. The memory module **10** is

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connectable to a memory controller **20** of a computer system (not shown). The memory module **10** comprises a plurality of memory devices **30**, each memory device **30** having a corresponding load. The memory module **10** further comprises a circuit **40** electrically coupled to the plurality of memory devices **30** and configured to be electrically coupled to the memory controller **20** of the computer system. The circuit **40** selectively isolates one or more of the loads of the memory devices from the computer system. The circuit **40** comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module **10**.

[0039] As used herein, the term "load" is a broad term which includes, without limitation, electrical load, such as capacitive load, inductive load, or impedance load. As used herein, the term "isolation" is a broad term which includes, without limitation, electrical separation of one or more components from another component or from one another. As used herein, the term "circuit" is a broad term which includes, without limitation, an electrical component or device, or a configuration of electrical components or devices which are electrically or electromagnetically coupled together (e.g., integrated circuits), to perform specific functions.

[0040] Various types of memory modules **10** are compatible with embodiments described herein. For example, memory modules **10** having memory capacities of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, as well as other capacities, are compatible with embodiments described herein. Certain embodiments described herein are applicable to various frequencies including, but not limited to 100 MHz, 200 MHz, 400 MHz, 800 MHz, and above. In addition, memory modules **10** having widths of 4 bytes, 8 bytes, 16 bytes, 32bytes, or 32bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. In certain embodiments, the memory module **10** comprises a printed circuit board on which the memory devices **30** are mounted, a plurality of edge connectors configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, and a plurality of electrical conduits which electrically couple the memory devices **30** to the circuit **40** and which electrically couple the circuit **40** to the edge connectors. Furthermore, memory modules **10** compatible with embodiments described herein include, but are not limited to, single in-line memory modules (SIMMs), dual in-line memory modules (DIMMs), small-outline DIMMs (SO-DIMMs), unbuffered

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DIMMs (UDIMMs), registered DIMMs (RDIMMs), fully-buffered DIMM (FBDIMM), rank-buffered DIMMs (RBDIMMs), mini-DIMMs, and micro-DIMMs.

[0041] Memory devices **30** compatible with embodiments described herein include, but are not limited to, random-access memory (RAM), dynamic random-access memory (DRAM), synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., SDR, DDR-1, DDR-2, DDR-3). In addition, memory devices **30** having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein. Memory devices **30** compatible with embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP). Memory devices **30** compatible with embodiments described herein are available from a number of sources, including but not limited to, Samsung Semiconductor, Inc. of San Jose, Calif., Infineon Technologies AG of San Jose, Calif., and Micron Technology, Inc. of Boise, Id. Persons skilled in the art can select appropriate memory devices **30** in accordance with certain embodiments described herein.

[0042] In certain embodiments, the plurality of memory devices **30** comprises a first number of memory devices **30**. In certain such embodiments, the circuit **40** selectively isolates a second number of the memory devices **30** from the computer system, with the second number less than the first number.

[0043] In certain embodiments, the plurality of memory devices **30** are arranged in a first number of ranks. For example, in certain embodiments, the memory devices **30** are arranged in two ranks, as schematically illustrated by FIG. 1. In other embodiments, the memory devices **30** are arranged in four ranks. Other numbers of ranks of the memory devices **30** are also compatible with embodiments described herein.

[0044] In certain embodiments, the circuit comprises a logic element selected from a group consisting of: a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, and a complex programmable-logic device (CPLD). In certain embodiments, the logic element of the circuit **40** is a custom device. Sources of logic elements compatible with embodiments described herein include, but are not limited to, Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose,

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Calif., and Xilinx Incorporated of San Jose, Calif. In certain embodiments, the logic element comprises various discrete electrical elements, while in certain other embodiments, the logic element comprises one or more integrated circuits.

[0045] In certain embodiments, the circuit **40** further comprises one or more switches which are operatively coupled to the logic element to receive control signals from the logic element. Examples of switches compatible with certain embodiments described herein include, but are not limited to, field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex.

[0046] FIG. 2 schematically illustrates a circuit diagram of two memory devices **30a, 30b** of a conventional memory module showing the interconnections between the DQ data signal lines **102a**, **102b** of the memory devices **30a, 30b** and the DQS data strobe signal lines **104a**, **104b** of the memory devices **30a, 30b**. Each of the memory devices **30a, 30b** has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, however, for simplicity, FIG. 2 only illustrates a single DQ data signal line and a single DQS data strobe signal line for each memory device **30a, 30b**. The DQ data signal lines **102a**, **102b** and the DQS data strobe signal lines **104a**, **104b** are typically conductive traces etched on the printed circuit board of the memory module. As shown in FIG. 2, each of the memory devices **30a, 30b** has their DQ data signal lines **102a**, **102b** electrically coupled to a common DQ line **112** and their DQS data strobe signal lines **104a**, **104b** electrically coupled to a common DQS line **114**. The common DQ line **112** and the common DQS line **114** are electrically coupled to the memory controller **20** of the computer system. Thus, the computer system is exposed to the loads of both memory devices **30a, 30b** concurrently.

[0047] In certain embodiments, the circuit **40** selectively isolates the loads of at least some of the memory devices **30** from the computer system. The circuit **40** of certain embodiments is configured to present a significantly reduced load to the computer system. In certain embodiments in which the memory devices **30** are arranged in a plurality of ranks, the circuit **40** selectively isolates the loads of some (e.g., one or more) of the ranks of the memory module **10** from the computer system. In certain other embodiments, the circuit **40** selectively isolates the loads of all of the ranks of the memory module **10** from the computer system. For example, when a memory module **10** is not being accessed by the computer

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system, the capacitive load on the memory controller **20** of the computer system by the memory module **10** can be substantially reduced to the capacitive load of the circuit **40** of the memory module **10**.

[0048] As schematically illustrated by FIGS. 3A and 3B, an example memory module **10** compatible with certain embodiments described herein comprises a circuit **40** which selectively isolates one or both of the DQ data signal lines **102a**, **102b** of the two memory devices **30a, 30b** from the common DQ data signal line **112** coupled to the computer system. Thus, the circuit **40** selectively allows a DQ data signal to be transmitted from the memory controller **20** of the computer system to one or both of the DQ data signal lines **102a**, **102b**. In addition, the circuit **40** selectively allows one of a first DQ data signal from the DQ data signal line **102a** of the first memory device **30a** or a second DQ data signal from the DQ data signal line **102b** of the second memory device **30b** to be transmitted to the memory controller **20** via the common DQ data signal line **112** (see, e.g., triangles on the DQ and DQS lines of FIGS. 3A and 3B which point towards the memory controller). While various figures of the present application denote read operations by use of DQ and DQS lines which have triangles pointing towards the memory controller, certain embodiments described herein are also compatible with write operations (e.g., as would be denoted by triangles on the DQ or DQS lines pointing away from the memory controller).

[0049] For example, in certain embodiments, the circuit **40** comprises a pair of switches **120** *a*, **120** *b* on the DQ data signal lines **102a**, **102b** as schematically illustrated by FIG. 3A. Each switch **120** *a*, **120** *b* is selectively actuated to selectively electrically couple the DQ data signal line **102a** to the common DQ signal line **112**, the DQ data signal line **102b** to the common DQ signal line **112**, or both DQ data signal lines **102a**, **102b** to the common DQ signal line **112**. In certain other embodiments, the circuit **40** comprises a switch **120** electrically coupled to both of the DQ data signal lines **102a**, **102b**, as schematically illustrated by FIG. 3B. The switch **120** is selectively actuated to selectively electrically couple the DQ data signal line **102a** to the common DQ signal line **112**, the DQ data signal line **102b** to the common DQ signal line **112**, or both DQ signal lines **102a**, **102b** to the common DQ signal line **112**. Circuits **40** having other configurations of switches are also compatible with embodiments described herein. While each of the memory devices **30a, 30b** has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, FIGS.

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3A and 3B only illustrate a single DQ data signal line and a single DQS data strobe signal line for each memory device **30a, 30b** for simplicity. The configurations schematically illustrated by FIGS. 3A and 3B can be applied to all of the DQ data signal lines and DQS data strobe signal lines of the memory module **10**.

[0050] In certain embodiments, the circuit **40** selectively isolates the loads of ranks of memory devices **30** from the computer system. As schematically illustrated in FIGS. 4A and 4B, example memory modules **10** compatible with certain embodiments described herein comprise a first number of memory devices **30** arranged in a first number of ranks **32**. The memory modules **10** of FIGS. 4A and 4B comprises two ranks **32a**, **32b**, with each rank **32a**, **32b** having a corresponding set of DQ data signal lines and a corresponding set of DQS data strobe lines. Other numbers of ranks (e.g., four ranks) of memory devices **30** of the memory module **10** are also compatible with certain embodiments described herein. For simplicity, FIGS. 4A and 4B illustrate only a single DQ data signal line and a single DQS data strobe signal line from each rank **32**.

[0051] The circuit **40** of FIG. 4A selectively isolates one or more of the DQ data signal lines **102a**, **102b** of the two ranks **32a**, **32b** from the computer system. Thus, the circuit **40** selectively allows a DQ data signal to be transmitted from the memory controller **20** of the computer system to the memory devices **30** of one or both of the ranks **32a**, **32b** via the DQ data signal lines **102a**, **102b**. In addition, the circuit **40** selectively allows one of a first DQ data signal from the DQ data signal line **102a** of the first rank **32a** and a second DQ data signal from the DQ data signal line **102b** of the second rank **32b** to be transmitted to the memory controller **20** via the common DQ data signal line **112**. For example, in certain embodiments, the circuit **40** comprises a pair of switches **120** *a*, **120** *b* on the DQ data signal lines **102a**, **102b** as schematically illustrated by FIG. 4A. Each switch **120** *a*, **120** *b* is selectively actuated to selectively electrically couple the DQ data signal line **102a** to the common DQ data signal line **112**, the DQ data signal line **102b** to the common DQ data signal line **112**, or both DQ data signal lines **102a**, **102b** to the common DQ data signal line **112**. In certain other embodiments, the circuit **40** comprises a switch **120** electrically coupled to both of the DQ data signal lines **102a**, **102b**, as schematically illustrated by FIG. 4B. The switch **120** is selectively actuated to selectively electrically couple the DQ data signal line **102a** to the common DQ data signal line **112**, the DQ data signal line **102b** to the common

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DQ data signal line **112**, or both DQ data signal lines **102a**, **102b** to the common DQ data signal line **112**. Circuits **40** having other configurations of switches are also compatible with embodiments described herein.

[0052] In the example embodiments schematically illustrated by FIGS. 3A, **3**B, **4**A, and **4**B, the circuit **40** comprises a logic element which is integral with and comprises the switches **120** which are coupled to the DQ data signal lines and the DQS data strobe signal lines. In certain such embodiments, each switch **120** comprises a data path multiplexer/demultiplexer. In certain other embodiments, the circuit **40** comprises a logic element **122** which is a separate component operatively coupled to the switches **120**, as schematically illustrated by FIGS. 5A-5D. The one or more switches **120** are operatively coupled to the logic element **122** to receive control signals from the logic element **122** and to selectively electrically couple one or more data signal lines to a common data signal line. Example switches compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex. Example logic elements **122** compatible with certain embodiments described herein include, but are not limited to, programmable-logic devices (PLD), application-specific integrated circuits (ASIC), field-programmable gate arrays (FPGA), custom-designed semiconductor devices, and complex programmable-logic devices (CPLD). Example logic elements **122** are available from Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif.

[0053] In certain embodiments, the load isolation provided by the circuit **40** advantageously allows the memory module **10** to present a reduced load (e.g., electrical load, such as capacitive load, inductive load, or impedance load) to the computer system by selectively switching between the two ranks of memory devices **30** to which it is coupled. This feature is used in certain embodiments in which the load of the memory module **10** may otherwise limit the number of ranks or the number of memory devices per memory module. In certain embodiments, the memory module **10** operates as having a data path rank buffer which advantageously isolates the ranks of memory devices **30** of the memory module **10** from one another, from the ranks on other memory modules, and from the computer system. This data path rank buffer of certain embodiments advantageously provides DQ-DQS paths

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for each rank or sets of ranks of memory devices which are separate from one another, or which are separate from the memory controller of the computer system. In certain embodiments, the load isolation advantageously diminishes the effects of capacitive loading, jitter and other sources of noise. In certain embodiments, the load isolation advantageously simplifies various other aspects of operation of the memory module **10**, including but not limited to, setup-and-hold time, clock skew, package skew, and process, temperature, voltage, and transmission line variations.

[0054] For certain memory module applications that utilize multiple ranks of memory, increased load on the memory bus can degrade speed performance. In certain embodiments described herein, selectively isolating the loads of the ranks of memory devices **30** advantageously decreases the load on the computer system, thereby allowing the computer system (e.g., server) to run faster with improved signal integrity. In certain embodiments, load isolation advantageously provides system memory with reduced electrical loading, thereby improving the electrical topology to the memory controller **20**. In certain such embodiments, the speed and the memory density of the computer system are advantageously increased without sacrificing one for the other.

[0055] In certain embodiments, load isolation advantageously increases the size of the memory array supported by the memory controller **20** of the computer system. The larger memory array has an increased number of memory devices **30** and ranks of memory devices **30** of the memory module **10**, with a corresponding increased number of chip selects. Certain embodiments described herein advantageously provide more system memory using fewer chip selects, thereby avoiding the chip select limitation of the memory controller.

[0056] An exemplary section of Verilog code corresponding to logic compatible with a circuit **40** which provides load isolation is listed below in Example 1. The exemplary code of Example 1 corresponds to a circuit **40** comprising six FET switches for providing load isolation to DQ and DQS lines.

[0057] Example 1

```
//============================================ declarations
  reg                   rasN_R, casN_R, weN_R;
  wire                  actv_cmd_R, pch_cmd_R, pch_all_cmd_R, ap_xfr_cmd_R_R;
  wire                  xfr_cmd_R,mrs_cmd,rd_cmd_R;
```


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```
//- - - - - - - - - - - - - - - - - - - - - - - - - - - - DDR 2 FET
  reg                   brs0N_R;                        // registered chip sel
  reg                   brs1N_R;                        // registered chip sel
  reg                   brs2N_R;                        // registered chip sel
  reg                   brs3N_R;                        // registered chip sel
  wire                  sel;
  wire                  sel_01;
  wire                  sel_23;
  wire                  rd_R1;
  wire                  wr_cmd_R,wr_R1;
  reg                   rd_R2,rd_R3,rd_R4,rd_R5;
  reg                   wr_R2,wr_R3,wr_R4,wr_R5;
  reg                   cnfet1,cnfet2,cnfet3,cnfet4,cnfet5,cnfet6;
  wire                  wr_01_R1,wr_23_R1;
  reg                   wr_01_R2,wr_01_R3,wr_01_R4;
  reg                   wr_23_R2,wr_23_R3,wr_23_R4;
  wire                  rodt0_a,rodt0_b;

//=========================================== logic
 always @(posedge clk_in)
        begin
                brs0N_R <= brs0_in_N;    // cs0
                brs1N_R <= brs1_in_N;    // cs1
                brs2N_R <= brs2_in_N;    // cs2
                brs3N_R <= brs3_in_N;    // cs3
                rasN_R  <= brras_in_N ;
                casN_R  <= brcas_in_N ;
                weN_R   <= bwe_in_N ;
        end
assign sel = ~brs0N_R | ~brs1N_R | ~brs2N_R | ~brs3N_R ;
assign sel_01 = ~brs0N_R | ~brs1N_R ;
assign sel_23 = ~brs2N_R | ~brs3N_R ;
assign actv_cmd_R = !rasN_R & casN_R & weN_R; // activate cmd
assign pch_cmd_R = !rasN_R & casN_R & !weN_R ;// pchg cmd
assign xfr_cmd_R = rasN_R & !casN_R;                  // xfr cmd
assign mrs_cmd = !rasN_R & !casN_R & !weN_R ;   // md reg set cmd
assign rd_cmd_R = rasN_R & !casN_R & weN_R ;    // read cmd
assign wr_cmd_R = rasN_R & !casN_R & !weN_R ; // write cmd
//-----------------------------------
assign    rd_R1 = sel & rd_cmd_R;  // rd cmd cyc 1
assign    wr_R1 = sel & wr_cmd_R; // wr cmd cyc 1

//-----------------------------------
  always @(posedge clk_in)
        begin
                rd_R2 <= rd_R1 ;
                rd_R3 <= rd_R2;
```


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```
                rd_R4 <= rd_R3;
                rd_R5 <= rd_R4;
//              rd0_o_R6 <= rd0_o_R5;
                wr_R2 <= wr_R1 ;
                wr_R3 <= wr_R2;
                wr_R4 <= wr_R3;
                wr_R5 <= wr_R4;
        end
//-------------------------------------
assign  wr_01_R1 = sel_01 & wr_cmd_R;  // wr cmd cyc 1 for cs 2 & cs3
assign  wr_23_R1 = sel_23 & wr_cmd_R;  // wr cmd cyc 1 for cs 2 & cs3
  always @(posedge clk_in)
        begin
                wr_01_R2 <= wr_01_R1 ;
                wr_01_R3 <= wr_01_R2;
                wr_01_R4 <= wr_01_R3;
                wr_23_R2 <= wr_23_R1 ;
                wr_23_R3 <= wr_23_R2;
                wr_23_R4 <= wr_23_R3;
        end
assign  rodt0_ab = (rodt0)          // odt cmd from sys
                | (wr_23_R1)        // wr 1st cyc to other rnks (assume single dimm per channel)
                | (wr_23_R2)        // wr 2nd cyc to other rnks (assume single dimm per channel)
                | (wr_23_R3)        // wr 3rd cyc to other rnks (assume single dimm per channel)
                ;
assign  rodt1_ab = (rodt1)          // odt cmd from sys
                | (wr_01_R1)        // wr 1st cyc to other rnks (assume single dimm per channel)
                | (wr_01_R2)        // wr 2nd cyc to other rnks (assume single dimm per channel)
                | (wr_01_R3)        // wr 3rd cyc to other rnks (assume single dimm per channel)
                ;

//-------------------------------------
always @(posedge clk_in)
        begin
  if (
    | (rd_R2)                       // pre-am rd
    | (rd_R3)                       // 1st cyc of rd brst (cl3)
    | (rd_R4)                       // 2nd cyc of rd brst (cl3)
    | (wr_R1)                       // pre-am wr
    | (wr_R2)                       // wr brst 1st cyc
    | (wr_R3)                       // wr brst 2nd cyc
     ) begin
                enfet1 <= 1'b1;     // enable fet
                enfet2 <= 1'b1;     // enable fet
                enfet3 <= 1'b1;     // enable fet
                enfet4 <= 1'b1;     // enable fet
                enfet5 <= 1'b1;     // enable fet
                enfet6 <= 1'b1;     // enable fet
      end
```


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```
    else
        begin
                    enfet1 <= 1'b0;          // disable fet
                    enfet2 <= 1'b0;          // disable fet
                    enfet3 <= 1'b0;          // disable fet
                    enfet4 <= 1'b0;          // disable fet
                    enfet5 <= 1'b0;          // disable fet

                    enfet6 <= 1'b0;          // disable fet
        end
    end
```

Back-to-Back Adjacent Read Commands

[0058] Due to their source synchronous nature, DDR SDRAM (e.g., DDR1, DDR2, DDR3) memory devices operate with a data transfer protocol which surrounds each burst of data strobes with a pre-amble time interval and a post-amble time interval. The pre-amble time interval provides a timing window for the receiving memory device to enable its data capture circuitry when a known valid level is present on the strobe signal to avoid false triggers of the memory device's capture circuit. The post-amble time interval provides extra time after the last strobe for this data capture to facilitate good signal integrity. In certain embodiments, when the computer system accesses two consecutive bursts of data from the same memory device, termed herein as a "back-to-back adjacent read," the post-amble time interval of the first read command and the pre-amble time interval of the second read command are skipped by design protocol to increase read efficiency. FIG. 6A shows an exemplary timing diagram of this "gapless" read burst for a back-to-back adjacent read condition from one memory device.

[0059] In certain embodiments, when the second read command accesses data from a different memory device than does the first read command, there is at least one time interval (e.g., clock cycle) inserted between the data strobes of the two memory devices. This inserted time interval allows both read data bursts to occur without the post-amble time interval of the first read data burst colliding or otherwise interfering with the pre-amble time interval of the second read data burst. In certain embodiments, the memory controller of the computer system inserts an extra clock cycle between successive read commands issued to different memory devices, as shown in the exemplary timing diagram of FIG. 6B for successive read accesses from different memory devices.

[0060] In typical computer systems, the memory controller is informed of the

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memory boundaries between the ranks of memory of the memory module prior to issuing read commands to the memory module. Such memory controllers can insert wait time intervals or clock cycles to avoid collisions or interference between back-to-back adjacent read commands which cross memory device boundaries, which are referred to herein as "BBARX."

[0061] In certain embodiments described herein in which the number of ranks **32** of the memory module **10** is doubled or quadrupled, the circuit **40** generates a set of output address and command signals so that the selection decoding is transparent to the computer system. However, in certain such embodiments, there are memory device boundaries of which the computer system is unaware, so there are occasions in which BBARX occurs without the cognizance of the memory controller **20** of the computer system. As shown in FIG. 7, the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b," resulting in a "collision window."

[0062] FIGS. 8A-8D schematically illustrate circuit diagrams of example memory modules **10** comprising a circuit **40** which multiplexes the DQS data strobe signal lines **104a**, **104b** of two ranks **32a**, **32b** from one another in accordance with certain embodiments described herein. While the DQS data strobe signal lines **104a**, **104b** of FIGS. 8A-8D correspond to two ranks **32a**, **32b** of memory devices **30**, in certain other embodiments, the circuit **40** multiplexes the DQS data strobe signal lines **104a**, **104b** corresponding to two individual memory devices **30a, 30b**.

[0063] FIG. 8A schematically illustrates a circuit diagram of an exemplary memory module **10** comprising a circuit **40** in accordance with certain embodiments described herein. In certain embodiments, BBARX collisions are avoided by a mechanism which electrically isolates the DQS data strobe signal lines **104a**, **104b** from one another during the transition from the first read data burst of one rank **32a** of memory devices **30** to the second read data burst of another rank **32b** of memory devices **30**.

[0064] In certain embodiments, as schematically illustrated by FIG. 8A, the circuit **40** comprises a first switch **130a** electrically coupled to a first DQS data strobe signal line **104a** of a first rank **32a** of memory devices **30** and a second switch **130b** electrically coupled to a second DQS data strobe signal line **104b** of a second rank **32b** of memory devices **30**. In certain embodiments, the time for switching the first switch **130a** and the

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second switch **130b** is between the two read data bursts (e.g., after the last DQS data strobe of the read data burst of the first rank **32a** and before the first DQS data strobe of the read data burst of the second rank **32b**). During the read data burst for the first rank **32a**, the first switch **130a** is enabled. After the last DQS data strobe of the first rank **32a** and before the first DQS data strobe of the second rank **32b**, the first switch **130a** is disabled and the second switch **130b** is enabled.

[0065] As shown in FIG. 8A, each of the ranks **32a**, **32b** otherwise involved in a BBARX collision have their DQS data strobe signal lines **104a**, **104b** selectively electrically coupled to the common DQS line **114** through the circuit **40**. The circuit **40** of certain embodiments multiplexes the DQS data strobe signal lines **104a**, **104b** of the two ranks **32a**, **32b** of memory devices **30** from one another to avoid a BBARX collision.

[0066] In certain embodiments, as schematically illustrated by FIG. 8B, the circuit **40** comprises a switch **130** which multiplexes the DQS data strobe signal lines **104a**, **104b** from one another. For example, the circuit **40** receives a DQS data strobe signal from the common DQS data strobe signal line **114** and selectively transmits the DQS data strobe signal to the first DQS data strobe signal line **104a**, to the second DQS data strobe signal line **104b**, or to both DQS data strobe signal lines **104a**, **104b**. As another example, the circuit **40** receives a first DQS data strobe signal from the first rank **32a** of memory devices **30** and a second DQS data strobe signal from a second rank **32b** of memory devices **30** and selectively switches one of the first and second DQS data strobe signals to the common DQS data strobe signal line **114**.

[0067] In certain embodiments, the circuit **40** also provides the load isolation described above in reference to FIGS. 1-5. For example, as schematically illustrated by FIG. 8C, the circuit **40** comprises both the switch **120** for the DQ data signal lines **102a**, **102b** and the switch **130** for the DQS data strobe signal lines **104a**, **104b**. While in certain embodiments, the switches **130** are integral with a logic element of the circuit **40**, in certain other embodiments, the switches **130** are separate components which are operatively coupled to a logic element **122** of the circuit **40**, as schematically illustrated by FIG. 8D. In certain such embodiments, the control and timing of the switch **130** is performed by the circuit **40** which is resident on the memory module **10**. Example switches **130** compatible with embodiments described herein include, but are not limited to field-effect transistor (FET)

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switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex., and multiplexers, such as the SN74AUC2G53 2:1 analog multiplexer/demultiplexer available from Texas Instruments, Inc. of Dallas, Tex.

[0068] The circuit **40** of certain embodiments controls the isolation of the DQS data strobe signal lines **104a**, **104b** by monitoring commands received by the memory module **10** from the computer system and producing "windows" of operation whereby the appropriate switches **130** are activated or deactivated to enable and disable the DQS data strobe signal lines **104a**, **104b** to mitigate BBARX collisions. In certain other embodiments, the circuit **40** monitors the commands received by the memory module **10** from the computer system and selectively activates or deactivates the switches **120** to enable and disable the DQ data signal lines **102a**, **102b** to reduce the load of the memory module **10** on the computer system. In still other embodiments, the circuit **40** performs both of these functions together.

Command Signal Translation

[0069] Most high-density memory modules are currently built with 512-Megabit ("512-Mb") memory devices wherein each memory device has a 64 M×8-bit configuration. For example, a 1-Gigabyte ("1-GB") memory module with error checking capabilities can be fabricated using eighteen such 512-Mb memory devices. Alternatively, it can be economically advantageous to fabricate a 1-GB memory module using lower-density memory devices and doubling the number of memory devices used to produce the desired word width. For example, by fabricating a 1-GB memory module using thirty-six 256-Mb memory devices with 64 M×4-bit configuration, the cost of the resulting 1-GB memory module can be reduced since the unit cost of each 256-Mb memory device is typically lower than one-half the unit cost of each 512-Mb memory device. The cost savings can be significant, even though twice as many 256-Mb memory devices are used in place of the 512-Mb memory devices. For example, by using pairs of 512-Mb memory devices rather than single 1-Gb memory devices, certain embodiments described herein reduce the cost of the memory module by a factor of up to approximately five.

[0070] Market pricing factors for DRAM devices are such that higher-density DRAM devices (e.g., 1-Gb DRAM devices) are much more than twice the price of lower-density DRAM devices (e.g., 512-Mb DRAM devices). In other words, the price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices.

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This pricing difference often lasts for months or even years after the introduction of the higher-density DRAM devices, until volume production factors reduce the costs of the newer higher-density DRAM devices. Thus, when the cost of a higher-density DRAM device is more than the cost of two lower-density DRAM devices, there is an economic incentive for utilizing pairs of the lower-density DRAM devices to replace individual higher-density DRAM devices.

[0071] FIG. 9A schematically illustrates an exemplary memory module **10** compatible with certain embodiments described herein. The memory module **10** is connectable to a memory controller **20** of a computer system (not shown). The memory module **10** comprises a printed circuit board **210** and a plurality of memory devices **30** coupled to the printed circuit board **210**. The plurality of memory devices **30** has a first number of memory devices **30**. The memory module **10** further comprises a circuit **40** coupled to the printed circuit board **210**. The circuit **40** receives a set of input address and command signals from the computer system. The set of input address and command signals correspond to a second number of memory devices **30** smaller than the first number of memory devices **30**. The circuit **40** generates a set of output address and command signals in response to the set of input address and command signals. The set of output address and command signals corresponds to the first number of memory devices **30**.

[0072] In certain embodiments, as schematically illustrated in FIG. 9A, the memory module **10** further comprises a phase-lock loop device **220** coupled to the printed circuit board **210** and a register **230** coupled to the printed circuit board **210**. In certain embodiments, the phase-lock loop device **220** and the register **230** are each mounted on the printed circuit board **210**. In response to signals received from the computer system, the phase-lock loop device **220** transmits clock signals to the plurality of memory devices **30**, the circuit **40**, and the register **230**. The register **230** receives and buffers a plurality of command signals and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals), and transmits corresponding signals to the appropriate memory devices **30**. In certain embodiments, the register **230** comprises a plurality of register devices. While the phase-lock loop device **220**, the register **230**, and the circuit **40** are described herein in certain embodiments as being separate components, in certain other embodiments, two or more of the phase-lock loop

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device **220**, the register **230**, and the circuit **40** are portions of a single component. Persons skilled in the art are able to select a phase-lock loop device **220** and a register **230** compatible with embodiments described herein.

[0073] In certain embodiments, the memory module **10** further comprises electrical components which are electrically coupled to one another and are surface-mounted or embedded on the printed circuit board **210**. These electrical components can include, but are not limited to, electrical conduits, resistors, capacitors, inductors, and transistors. In certain embodiments, at least some of these electrical components are discrete, while in other certain embodiments, at least some of these electrical components are constituents of one or more integrated circuits.

[0074] In certain embodiments, the printed circuit board **210** is mountable in a module slot of the computer system. The printed circuit board **210** of certain such embodiments has a plurality of edge connections electrically coupled to corresponding contacts of the module slot and to the various components of the memory module **10**, thereby providing electrical connections between the computer system and the components of the memory module **10**.

[0075] In certain embodiments, the plurality of memory devices **30** are arranged in a first number of ranks **32**. For example, in certain embodiments, the memory devices **30** are arranged in four ranks **32a**, **32b**, **32** *c*, **32** *d*, as schematically illustrated by FIG. 9A. In certain other embodiments, the memory devices **30** are arranged in two ranks **32a**, **32b**, as schematically illustrated by FIG. 9B. Other numbers of ranks **32** of the memory devices **30** are also compatible with embodiments described herein.

[0076] As schematically illustrated by FIGS. 9A and 9B, in certain embodiments, the circuit **40** receives a set of input command signals (e.g., refresh, precharge) and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) from the memory controller **20** of the computer system. In response to the set of input address and command signals, the circuit **40** generates a set of output address and command signals.

[0077] In certain embodiments, the set of output address and command signals corresponds to a first number of ranks in which the plurality of memory devices **30** of the

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memory module **10** are arranged, and the set of input address and command signals corresponds to a second number of ranks per memory module for which the computer system is configured. The second number of ranks in certain embodiments is smaller than the first number of ranks. For example, in the exemplary embodiment as schematically illustrated by FIG. 9A, the first number of ranks is four while the second number of ranks is two. In the exemplary embodiment of FIG. 9B, the first number of ranks is two while the second number of ranks is one. Thus, in certain embodiments, even though the memory module **10** actually has the first number of ranks of memory devices **30**, the memory module **10** simulates a virtual memory module by operating as having the second number of ranks of memory devices **30**. In certain embodiments, the memory module **10** simulates a virtual memory module when the number of memory devices **30** of the memory module **10** is larger than the number of memory devices **30** per memory module for which the computer system is configured to utilize. In certain embodiments, the circuit **40** comprises logic (e.g., address decoding logic, command decoding logic) which translates between a system memory domain of the computer system and a physical memory domain of the memory module **10**.

[0078] In certain embodiments, the computer system is configured for a number of ranks per memory module which is smaller than the number of ranks in which the memory devices **30** of the memory module **10** are arranged. In certain such embodiments, the computer system is configured for two ranks of memory per memory module (providing two chip-select signals CS_0, CS_1) and the plurality of memory modules **30** of the memory module **10** are arranged in four ranks, as schematically illustrated by FIG. 9A. In certain other such embodiments, the computer system is configured for one rank of memory per memory module (providing one chip-select signal CS_0) and the plurality of memory modules **30** of the memory module **10** are arranged in two ranks, as schematically illustrated by FIG. 9B.

[0079] In the exemplary embodiment schematically illustrated by FIG. 9A, the memory module **10** has four ranks of memory devices **30** and the computer system is configured for two ranks of memory devices per memory module. The memory module **10** receives row/column address signals or signal bits (A_0-A_{n+1}), bank address signals (BA_0-BA_m), chip-select signals (CS_0 and CS_1), and command signals (e.g., refresh, precharge, etc.) from the computer system. The A_0-A_n row/column address signals are received by the register **230**, which buffers these address signals and sends these address signals to the

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appropriate ranks of memory devices **30**. The circuit **40** receives the two chip-select signals (CS_0, CS_1) and one row/column address signal (A_{n+1}) from the computer system. Both the circuit **40** and the register **230** receive the bank address signals (BA_0-BA_m) and at least one command signal (e.g., refresh, precharge, etc.) from the computer system.

Logic Tables

[0080] Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using chip-select signals.

TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:
1. CS_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

[0081] In Logic State 1: CS_0 is active low, A_{n+1} is non-active, and Command is active. CS_{0A} is pulled low, thereby selecting Rank **0**.

[0082] In Logic State 2: CS_0 is active low, A_{n+1} is active, and Command is active. CS_{0B} is pulled low, thereby selecting Rank **1**.

[0083] In Logic State 3: CS_0 is active low, A_{n+1} is Don't Care, and Command is active high. CS_{0A} and CS_{0B} are pulled low, thereby selecting Ranks **0** and **1**.

[0084] In Logic State 4: CS_1 is active low, A_{n+1} is non-active, and Command is active. CS_{1A} is pulled low, thereby selecting Rank **2**.

[0085] In Logic State 5: CS_1 is active low, A_{n+1} is active, and Command is active. CS_1B is pulled low, thereby selecting Rank **3**.

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[0086] In Logic State 6: CS_1 is active low, A_{n+1} is Don't Care, and Command is active. CS_{1A} and CS_1B are pulled low, thereby selecting Ranks **2** and **3**.

[0087] In Logic State 7: CS_0 and CS_1 are pulled non-active high, which deselects all ranks, i.e., CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are pulled high.

[0088] The "Command" column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently.

[0089] Table 2 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using gated CAS signals.

TABLE 2

CS*	RAS*	CAS*	WE*	Density Bit	A_{10}	Command	CAS0*	CAS1*
1	x	x	x	x	x	NOP	x	x
0	1	1	1	x	x	NOP	1	1
0	0	1	1	0	x	ACTIVATE	1	1
0	0	1	1	1	x	ACTIVATE	1	1
0	1	0	1	0	x	READ	0	1
0	1	0	1	1	x	READ	1	0
0	1	0	0	0	x	WRITE	0	1
0	1	0	0	1	x	WRITE	1	0
0	0	1	0	0	0	PRE-CHARGE	1	1
0	0	1	0	1	0	PRE-CHARGE	1	1
0	0	1	0	x	1	PRE-CHARGE	1	1
0	0	0	0	x	x	MODE REG SET	0	0
0	0	0	1	x	x	REFRESH	0	0

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[0090] In certain embodiments in which the density bit is a row address bit, for read/write commands, the density bit is the value latched during the activate command for the selected bank.

Serial-Presence-Detect Device

[0091] Memory modules typically include a serial-presence detect (SPD) device **240** (e.g., an electrically-erasable-programmable read-only memory or EEPROM device) comprising data which characterize various attributes of the memory module, including but not limited to, the number of row addresses the number of column addresses, the data width of the memory devices, the number of ranks, the memory density per rank, the number of memory devices, and the memory density per memory device. The SPD device **240** communicates this data to the basic input/output system (BIOS) of the computer system so that the computer system is informed of the memory capacity and the memory configuration available for use and can configure the memory controller properly for maximum reliability and performance.

[0092] For example, for a commercially-available 512-MB (64 M×8-byte) memory module utilizing eight 512-Mb memory devices each with a 64 M×8-bit configuration, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte **3**: Defines the number of row address bits in the DRAM device in the memory module [13 for the 512-Mb memory device].

Byte **4**: Defines the number of column address bits in the DRAM device in the memory module [11 for the 512-Mb memory device].

Byte **13**: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 512-Mb (64 M×8-bit) memory device].

Byte **14**: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 512-Mb (64 M×8-bit) memory device].

Byte **17**: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 512-Mb memory device].

[0093] In a further example, for a commercially-available 1-GB (128 M×8-byte) memory module utilizing eight 1-Gb memory devices each with a 128 M×8-bit configuration, as described above, the SPD device contains the following SPD data (in appropriate bit fields

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of these bytes):

Byte **3**: Defines the number of row address bits in the DRAM device in the memory module [14 for the 1-Gb memory device].

Byte **4**: Defines the number of column address bits in the DRAM device in the memory module [11 for the 1-Gb memory device].

Byte **13**: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 1-Gb (128 M×8-bit) memory device].

Byte **14**: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 1-Gb (128 M×8-bit) memory device].

Byte **17**: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 1-Gb memory device].

[0094] In certain embodiments, the SPD device **240** comprises data which characterize the memory module **10** as having fewer ranks of memory devices than the memory module **10** actually has, with each of these ranks having more memory density. For example, for a memory module **10** compatible with certain embodiments described herein having two ranks of memory devices **30**, the SPD device **240** comprises data which characterizes the memory module **10** as having one rank of memory devices with twice the memory density per rank. Similarly, for a memory module **10** compatible with certain embodiments described herein having four ranks of memory devices **30**, the SPD device **240** comprises data which characterizes the memory module **10** as having two ranks of memory devices with twice the memory density per rank. In addition, in certain embodiments, the SPD device **240** comprises data which characterize the memory module **10** as having fewer memory devices than the memory module **10** actually has, with each of these memory devices having more memory density per memory device. For example, for a memory module **10** compatible with certain embodiments described herein, the SPD device **240** comprises data which characterizes the memory module **10** as having one-half the number of memory devices that the memory module **10** actually has, with each of these memory devices having twice the memory density per memory device. Thus, in certain embodiments, the SPD device **240** informs the computer system of the larger memory array by reporting a memory device density that is a multiple of the memory devices **30** resident on the memory module **10**. Certain embodiments described herein advantageously do not require system level changes to hardware (e.g., the motherboard of the computer system) or to software (e.g., the

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BIOS of the computer system).

[0095] FIG. 9C schematically illustrates an exemplary memory module **10** in accordance with certain embodiments described herein. The memory module **10** comprises a pair of substantially identical memory devices **31**, **33**. Each memory device **31**, **33** has a first bit width, a first number of banks of memory locations, a first number of rows of memory locations, and a first number of columns of memory locations. The memory module **10** further comprises an SPD device **240** comprising data that characterizes the pair of memory devices **31**, **33**. The data characterize the pair of memory devices **31**, **33** as a virtual memory device having a second bit width equal to twice the first bit width, a second number of banks of memory locations equal to the first number of banks, a second number of rows of memory locations equal to the first number of rows, and a second number of columns of memory locations equal to the first number of columns.

[0096] In certain such embodiments, the SPD device **240** of the memory module **10** is programmed to describe the combined pair of lower-density memory devices **31**, **33** as one virtual or pseudo-higher-density memory device. In an exemplary embodiment, two 512-Mb memory devices, each with a 128 M×4-bit configuration, are used to simulate one 1-Gb memory device having a 128 M×8-bit configuration. The SPD device **240** of the memory module **10** is programmed to describe the pair of 512-Mb memory devices as one virtual or pseudo-1-Gb memory device.

[0097] For example, to fabricate a 1-GB (128 M×8-byte) memory module, sixteen 512-Mb (128 M×4-bit) memory devices can be used. The sixteen 512-Mb (128 M×4-bit) memory devices are combined in eight pairs, with each pair serving as a virtual or pseudo-1-Gb (128 M×8-bit) memory device. In certain such embodiments, the SPD device **240** contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: 13 row address bits.

Byte 4: 12 column address bits.

Byte 13: 8 bits wide for the primary virtual 1-Gb (128 M×8-bit) memory device.

Byte 14: 8 bits wide for the error checking virtual 1-Gb (128 M×8-bit) memory device.

Byte 17: 4 banks.

[0098] In this exemplary embodiment, bytes **3**, **4**, and **17** are programmed to have

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the same values as they would have for a 512-MB (128 M×4-byte) memory module utilizing 512-Mb (128 M×4-bit) memory devices. However, bytes **13** and **14** of the SPD data are programmed to be equal to 8, corresponding to the bit width of the virtual or pseudo-higher-density 1-Gb (128 M×8-bit) memory device, for a total capacity of 1-GB. Thus, the SPD data does not describe the actual-lower-density memory devices, but instead describes the virtual or pseudo-higher-density memory devices. The BIOS accesses the SPD data and recognizes the memory module as having 4 banks of memory locations arranged in 2^{13} rows and 2^{12} columns, with each memory location having a width of 8 bits rather than 4 bits.

[0099] In certain embodiments, when such a memory module **10** is inserted in a computer system, the computer system's memory controller then provides to the memory module **10** a set of input address and command signals which correspond to the number of ranks or the number of memory devices reported by the SPD device **240**. For example, placing a two-rank memory module **10** compatible with certain embodiments described herein in a computer system compatible with one-rank memory modules, the SPD device **240** reports to the computer system that the memory module **10** only has one rank. The circuit **40** then receives a set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices **30** of the memory module **10**.

[00100] Similarly, when a two-rank memory module **10** compatible with certain embodiments described herein is placed in a computer system compatible with either one- or two-rank memory modules, the SPD device **240** reports to the computer system that the memory module **10** only has one rank. The circuit **40** then receives a set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices **30** of the memory module **10**.

[00101] Furthermore, a four-rank memory module **10** compatible with certain embodiments described herein simulates a two-rank memory module whether the memory module **10** is inserted in a computer system compatible with two-rank memory modules or with two- or four-rank memory modules. Thus, by placing a four-rank memory module **10** compatible with certain embodiments described herein in a module slot that is four-rank-

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ready, the computer system provides four chip-select signals, but the memory module **10** only uses two of the chip-select signals.

[00102] In certain embodiments, the circuit **40** comprises the SPD device **240** which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device **240** of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array. In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit **40**. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices **30** from the memory controller **20**. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three. In still other embodiments, the SPD device **240** does not utilize this extra cycle of time.

Memory Density Multiplication

[00103] In certain embodiments, two memory devices having a memory density are used to simulate a single memory device having twice the memory density, and an additional address signal bit is used to access the additional memory. Similarly, in certain embodiments, two ranks of memory devices having a memory density are used to simulate a single rank of memory devices having twice the memory density, and an additional address signal bit is used to access the additional memory. As used herein, such simulations of memory devices or ranks of memory devices are termed as "memory density multiplication," and the term "density transition bit" is used to refer to the additional address signal bit which is used to access the additional memory by selecting which rank of memory devices is enabled for a read or write transfer operation.

[00104] For example, for computer systems which are normally limited to using

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memory modules which have a single rank of 128 M×4-bit memory devices, certain embodiments described herein enable the computer system to utilize memory modules which have double the memory (e.g., two ranks of 128 M×4-bit memory devices). The circuit **40** of certain such embodiments provides the logic (e.g., command and address decoding logic) to double the number of chip selects, and the SPD device **240** reports a memory device density of 256 M×4-bit to the computer system.

[00105] In certain embodiments utilizing memory density multiplication embodiments, the memory module **10** can have various types of memory devices **30** (e.g., DDR1, DDR2, DDR3, and beyond). The circuit **40** of certain such embodiments utilizes implied translation logic equations having variations depending on whether the density transition bit is a row, column, or internal bank address bit. In addition, the translation logic equations of certain embodiments vary depending on the type of memory module **10** (e.g., UDIMM, RDIMM, FBDIMM, etc.). Furthermore, in certain embodiments, the translation logic equations vary depending on whether the implementation multiplies memory devices per rank or multiplies the number of ranks per memory module.

TABLE 3A

	128-Mb	256-Mb	512-Mb	1-Gb
Number of banks	4	4	4	4
Number of row address bits	12	13	13	14
Number of column address bits for "x 4" configuration	11	11	12	12
Number of column address bits for "x 8" configuration	10	10	11	11
Number of column address bits for "x 16" configuration	9	9	10	10

[00106] Table 3A provides the numbers of rows and columns for DDR-1 memory devices, as specified by JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published February 2004, and incorporated in its entirety by reference herein.

[00107] As described by Table 3A, 512-Mb (128 M×4-bit) DRAM devices have 2^{13} rows and 2^{12} columns of memory locations, while 1-Gb (128 M×8-bit) DRAM devices have 2^{14} rows and 2^{11} columns of memory locations. Because of the differences in the number of rows and the number of columns for the two types of memory devices, complex address

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translation procedures and structures would typically be needed to fabricate a 1-GB (128 M×8-byte) memory module using sixteen 512-Mb (128 M×4-bit) DRAM devices.

[00108] Table 3B shows the device configurations as a function of memory density for DDR2 memory devices.

TABLE 3B

	Number of Rows	Number of Columns	Number of Internal Banks	Page Size (x4s or x8s)
256 Mb	13	11	4	1 KB
512 Mb	14	11	4	1 KB
1 Gb	14	11	8	1 KB
2 Gb	15	11	8	1 KB
4 Gb	16	11	8	1 KB

Table 4 lists the corresponding density transition bit for the density transitions between the DDR2 memory densities of Table 3B.

TABLE 4

Density Transition	Density Transition Bit
256 Mb to 512 Mb	A_{13}
512 Mb to 1 Gb	BA_2
1 Gb to 2 Gb	A_{14}
2 Gb to 4 Gb	A_{15}

Other certain embodiments described herein utilize a transition bit to provide a transition from pairs of physical 4-Gb memory devices to simulated 8-Gb memory devices.

[00109] In an example embodiment, the memory module comprises one or more pairs of 256-Mb memory devices, with each pair simulating a single 512-Mb memory device. The simulated 512-Mb memory device has four internal banks while each of the two 256-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 256-Mb memory devices. In certain embodiments, the additional row address bit is translated by the circuit **40** to the rank selection between each of the two 256-Mb memory devices of the pair. Although there are eight total internal banks in the rank-converted memory array, the computer system is only aware of four internal banks. When the memory controller activates a row for a selected bank, the circuit **40** activates the same row for the same bank, but it does

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so for the selected rank according to the logic state of the additional row address bit A_{13}.

[00110] In another example embodiment, the memory module comprises one or more pairs of 512-Mb memory devices, with each pair simulating a single 1-Gb memory device. The simulated 1-Gb memory device has eight internal banks while each of the two 512-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 512-Mb memory devices. In certain embodiments, the mapped BA_2 (bank **2**) bit is used to select between the two ranks of 512-Mb memory devices to preserve the internal bank geometry expected by the memory controller of the computer system. The state of the BA_2 bit selects the upper or lower set of four banks, as well as the upper and lower 512-Mb rank.

[00111] In another example embodiment, the memory module comprises one or more pairs of 1-Gb memory devices, with each pair simulating a single 2-Gb memory device. Each of the two 1-Gb memory devices has eight internal banks for a total of sixteen internal banks, while the simulated 2-Gb memory device has eight internal banks. In certain embodiments, the additional row address bit translates to the rank selection between the two 1-Gb memory devices. Although there are sixteen total internal banks per pair of 1-Gb memory devices in the rank-converted memory array, the memory controller of the computer system is only aware of eight internal banks. When the memory controller activates a row of a selected bank, the circuit **40** activates the same row for the same bank, but is does so for the selected rank according to the logic state of the additional row address bit A_{14}.

[00112] The circuit **40** of certain embodiments provides substantially all of the translation logic used for the decoding (e.g., command and address decoding). In certain such embodiments, there is a fully transparent operational conversion from the "system memory" density domain of the computer system to the "physical memory" density domain of the memory module **10**. In certain embodiments, the logic translation equations are programmed in the circuit **40** by hardware, while in certain other embodiments, the logic translation equations are programmed in the circuit **40** by software. Examples 1 and 2 provide exemplary sections of Verilog code compatible with certain embodiments described herein. As described more fully below, the code of Examples 1 and 2 includes logic to reduce potential problems due to "back-to-back adjacent read commands which cross memory device boundaries or "BBARX." Persons skilled in the art are able to provide additional logic

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translation equations compatible with embodiments described herein.

[00113] An exemplary section of Verilog code compatible with memory density multiplication from 512 Mb to 1 Gb using DDR2 memory devices with the BA_2 density transition bit is listed below in Example 2. The exemplary code of Example 2 corresponds to a circuit **40** which receives one chip-select signal from the computer system and which generates two chip-select signals.

[00114] Example 2

```
always @(posedge clk_in)
    begin
                rs0N_R <= rs0_in_N;    // cs0
                rasN_R <= ras_in_N;
                casN_R <= cas_in_N;
                weN_R <= we_in_N;
    end
// Gated Chip Selects
assign          pcs0s_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                          // ref,mrd reg set
                | (~rs0_in_N & ras_in_N & cas_in_N)                                    // ref exit, pwr dn
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)               // pchg all
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ~ba2_in)    // pchg single bnk
                | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N       & ~ba2_in)         // activate
                | (~rs0_in_N & ras_in_N & ~cas_in_N              & ~ba2_in)            // xfr
                ;
assign          pcs0b_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                          // ref,mrd reg set
                | (~rs0_in_N & ras_in_N & cas_in_N)                                    // ref exit, pwr dn
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)               // pchg all
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ba2_in)     // pchg single bnk
                | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N       & ba2_in)          // activate
                | (~rs0_in_N & ras_in_N & ~cas_in_N              & ba2_in) // xfr
                ;
//.....................................................
 always @(posedge clk_in)
    begin
                a4_r <= a4_in ;
                a5_r <= a5_in ;
                a6_r <= a6_in ;
                a10_r <= a10_in ;
                ba0_r <= ba0_in ;
                ba1_r <= ba1_in ;
                ba2_r <= ba2_in ;
                q_mrs_cmd_cyc1 <= q_mrs_cmd ;
    end
//////////////////////////////////////////////////////
// determine the cas latency
//////////////////////////////////////////////////////
assign q_mrs_cmd_r = (!rasN_R & !casN_R & !weN_R)
                       & !rs0N_R
                    & (!ba0_r & !ba1_r)
                    ;     // mrd reg set cmd
    always @(posedge clk_in)
        if (~reset_N)     // init
                    cl3 <= 1'b1 ;
        else if (q_mrs_cmd_cyc1)  // load mode reg cmd
      begin
                    cl3 <= (~a6_r & a5_r & a4_r ) ;
        end
    always @(posedge clk_in)
        if (~reset_N)           // reset
```


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```
                cl2 <= 1'b0 ;
            else if (q_mrs_cmd_cyc1)  // load mode reg cmd
        begin
                cl2 <= (~a6_r & a5_r & ~a4_r ) ;
        end
    always @(posedge clk_ia)
            if (~reset_N)             // reset
                cl4 <= 1'b0 ;
            else if (q_mrs_cmd_cyc1)  // load mode reg cmd
        begin
                cl4 <= (a6_r & ~a5_r & ~a4_r ) ;
        end
  always @(posedge clk_ia)
            if (~reset_N)             cl5 <= 1'b0 ;
            else if (q_mrs_cmd_cyc1)  // load mode reg cmd
        begin
                cl5 <= (a6_r & ~a5_r & a4_r ) ;
        end
assign          pre_cyc2_enfet = (wr_cmd_cyc1 & acs_cyc1 & cl3)     // wr brst cl3 preamble
                               ;
assign          pre_cyc3_enfet = (rd_cmd_cyc2 & cl3)                // rd brst cl3 preamble
                               | (wr_cmd_cyc2 & cl3)                // wr brst cl3 1st pair
                               | (wr_cmd_cyc2 & cl4)                // wr brst cl4 preamble
                               ;
assign          pre_cyc4_enfet = (wr_cmd_cyc3 & cl3)                // wr brst cl3 2nd pair
                               | (wr_cmd_cyc3 & cl4)                // wr brst cl4 1st pair
                               | (rd_cmd_cyc3 & cl3)                // rd brst cl3 1st pair
                               | (rd_cmd_cyc3 & cl4)                // rd brst cl4 preamble
                               ;
assign          pre_cyc5_enfet = (rd_cmd_cyc4 & cl3)                // rd brst cl3 2nd pair
                               | (wr_cmd_cyc4 & cl4)                // wr brst cl4 2nd pair
                               | (rd_cmd_cyc4 & cl4)                // rd brst cl4 1st pair
                               ;
// dq
assign          pre_dq_cyc = pre_cyc2_enfet
                   | pre_cyc3_enfet
                   | pre_cyc4_enfet
                   | pre_cyc5_enfet
                   ;
assign          pre_dq_ncyc = enfet_cyc2
                   | enfet_cyc3
                   | enfet_cyc4
                   | enfet_cyc5
                   ;
// dqs
assign          pre_dqsa_cyc = (pre_cyc2_enfet & ~ba2_r)
                   | (pre_cyc3_enfet & ~ba2_cyc2)
                   | (pre_cyc4_enfet & ~ba2_cyc3)
                   | (pre_cyc5_enfet & ~ba2_cyc4)
                   ;
assign          pre_dqsb_cyc = (pre_cyc2_enfet & ba2_r)
                   | (pre_cyc3_enfet & ba2_cyc2)
                   | (pre_cyc4_enfet & ba2_cyc3)
                   | (pre_cyc5_enfet & ba2_cyc4)
                   ;
assign          pre_dqsa_ncyc = (enfet_cyc2 & ~ba2_cyc2)
                   | (enfet_cyc3 & ~ba2_cyc3)
                   | (enfet_cyc4 & ~ba2_cyc4)
                   | (enfet_cyc5 & ~ba2_cyc5)
                   ;
assign          pre_dqsb_ncyc = (enfet_cyc2 & ba2_cyc2)
                   | (enfet_cyc3 & ba2_cyc3)
                   | (enfet_cyc4 & ba2_cyc4)
                   | (enfet_cyc5 & ba2_cyc5)
                   ;
```


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```
always @(posedge clk_in)
        begin
                        acs_cyc2 <= acs_cyc1 ;        // cs active
                        ba2_cyc2 <= ba2_r ;
                        ba2_cyc3 <= ba2_cyc2 ;
                        ba2_cyc4 <= ba2_cyc3 ;
                        ba2_cyc5 <= ba2_cyc4 ;
                        rd_cmd_cyc2 <= rd_cmd_cyc1 & acs_cyc1;
                        rd_cmd_cyc3 <= rd_cmd_cyc2 ;
                        rd_cmd_cyc4 <= rd_cmd_cyc3 ;
                        rd_cmd_cyc5 <= rd_cmd_cyc4 ;
                        rd_cmd_cyc6 <= rd_cmd_cyc5 ;
                        rd_cmd_cyc7 <= rd_cmd_cyc6 ;
                        wr_cmd_cyc2 <= wr_cmd_cyc1 & acs_cyc1;
                        wr_cmd_cyc3 <= wr_cmd_cyc2 ;
                        wr_cmd_cyc4 <= wr_cmd_cyc3 ;
                        wr_cmd_cyc5 <= wr_cmd_cyc4 ;
        end
 always @(negedge clk_in)
        begin
                        dq_neye <= dq_cyc;
                        dqs_neye_a <= dqs_cyc_a;
                        dqs_neye_b <= dqs_cyc_b;
        end
// DQ FET enables
assign                  enq_fet1 = dq_cyc | dq_neye             ;
assign                  enq_fet2 = dq_cyc | dq_neye ;
assign                enq_fet3 = dq_cyc | dq_neye             ;
assign                  enq_fet4 = dq_cyc | dq_neye ;
assign                  enq_fet5 = dq_cyc | dq_neye ;
// DQS FET enables
assign                  ens_fet1a = dqs_cyc_a | dqs_neye_a    ;
assign                  ens_fet2a = dqs_cyc_a | dqs_neye_a    ;
assign                  ens_fet3a = dqs_cyc_a | dqs_neye_a    ;
assign                  ens_fet1b = dqs_cyc_b | dqs_neye_b    ;
assign                  ens_fet2b = dqs_cyc_b | dqs_neye_b    ;
assign                  ens_fet3b = dqs_cyc_b | dqs_neye_b    ;
```

[00115] Another exemplary section of Verilog code compatible with memory density multiplication from 256 Mb to 512 Mb using DDR2 memory devices and gated CAS signals with the row A_{13} density transition bit is listed below in Example 3. The exemplary code of Example 3 corresponds to a circuit **40** which receives one gated CAS signal from the computer system and which generates two gated CAS signals.

[00116] Example 3

```
// latched a13 flags cs0, banks 0-3
   always @(posedge clk_in)
      if (actv_cmd_R & ~rs0N_R & ~bnk1_R & ~bnk0_R )    // activate
      begin
                        1_a13_00 <= a13_r ;
      end
   always @(posedge clk_in)
      if (actv_cmd_R & ~rs0N_R & ~bnk1_R & bnk0_R)       // activate
      begin
                        1_a13_01 <= a13_r ;
      end
   always @(posedge clk_in)
      if (actv_cmd_R & ~rs0N_R & bnk1_R & ~bnk0_R)       // activate
```


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```
    begin
            1_a13_10 <= a13_r ;
    end
  always @(posedge clk_in)
    if (actv_cmd_R & ~rs0N_R & bnk1_R & bnk0_R)      // activate
    begin
            1_a13_11 <= a13_r ;
    end
// gated cas
assign cas_i = ~(casN_R);
assign   cas0_o = ( ~rasN_R & cas_i)
                | ( rasN_R & ~1_a13_00 & ~bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & ~1_a13_01 & ~bnk1_R & bnk0_R & cas_i)
                | ( rasN_R & ~1_a13_10 & bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & ~1_a13_11 & bnk1_R & bnk0_R & cas_i)
                ;
assign   cas1_o = ( ~rasN_R & cas_i)
                | ( rasN_R & 1_a13_00          & ~bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & 1_a13_01          & ~bnk1_R & bnk0_R & cas_i)
                | ( rasN_R & 1_a13_10          & bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & 1_a13_11          & bnk1_R & bnk0_R & cas_i)
                ;
assign          pcas_0_N = ~cas0_o;
assign          pcas_1_N = ~cas1_o;
assign          rd0_o_R1 = rasN_R & cas0_o & weN_R & ~rs0N_R;   // rnk0 rd cmd cyc
assign          rd1_o_R1 = rasN_R & cas1_o & weN_R & ~rs0N_R;   // rnk1 rd cmd cyc
assign          wr0_o_R1 = rasN_R & cas0_o & ~weN_R & ~rs0N_R;  // rnk0 wr cmd cyc
assign          wr1_o_R1 = rasN_R & cas1_o & ~weN_R & ~rs0N_R ;  // rnk1 wr cmd cyc
    always @(posedge clk_in)
        begin
                rd0_o_R2 <= rd0_o_R1 ;
                rd0_o_R3 <= rd0_o_R2;
                rd0_o_R4 <= rd0_o_R3;
                rd0_o_R5 <= rd0_o_R4;
                rd1_o_R2 <= rd1_o_R1 ;
                rd1_o_R3 <= rd1_o_R2;
                rd1_o_R4 <= rd1_o_R3;
                rd1_o_R5 <= rd1_o_R4;
                wr0_o_R2 <= wr0_o_R1 ;
                wr0_o_R3 <= wr0_o_R2;
                wr0_o_R4 <= wr0_o_R3;
                wr1_o_R2 <= wr1_o_R1 ;
                wr1_o_R3 <= wr1_o_R2;
                wr1_o_R4 <= wr1_o_R3;
        end
    always @(posedge clk_in)
        begin
        if (
              (rd0_o_R2 & ~rd1_o_R4)                                  // pre-am rd if no ped on rnk 1
            | rd0_o_R3                                                // 1st cyc of rd brst
            | rd0_o_R4                                                // 2nd cyc of rd brst
            | (rd0_o_R5 & ~rd1_o_R2 & ~rd1_o_R3)                      // post-rd cyc if no ped on rnk 1
            | (wr0_o_R1)                                              // pre-am wr
            | wr0_o_R2 | wr0_o_R3                                     // wr brst 1st & 2nd cyc
            | (wr0_o_R4)                                              // post-wr cyc (chge#9)
            | wr1_o_R1 | wr1_o_R2 | wr1_o_R3 | wr1_o_R4               // rank 1 (chge#9)
            )
                                en_fet_a <= 1'b1;                     // enable fet
        else
                                en_fet_a <= 1'b0;                     // disable fet
        end
```


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```
always @(posedge clk_in)
        begin
        if (
                (rd1_o_R2 & ~rd0_o_R4)
              | rd1_o_R3
              | rd1_o_R4
              | (rd1_o_R5 & ~rd0_o_R2 & ~rd0_o_R3)
          | (wr1_o_R1)                                          // (chgef8)
          | wr1_o_R2 | wr1_o_R3
  | (wr1_o_R4)                                                  // post-wr cyc      (chgef9)
  | wr0_o_R1 | wr0_o_R2 | wr0_o_R3 | wr0_o_R4                   // rank 0 (chgef9)
                )
                        en_fet_b <= 1'b1;                       //
        else
                        en_fet_b <= 1'b0;
        end
```

[00117] In certain embodiments, the chipset memory controller of the computer system uses the inherent behavioral characteristics of the memory devices (e.g., DDR2 memory devices) to optimize throughput of the memory system. For example, for each internal bank in the memory array, a row (e.g., 1 KB page) is advantageously held activated for an extended period of time. The memory controller, by anticipating a high number of memory accesses or hits to a particular region of memory, can exercise this feature to advantageously eliminate time-consuming pre-charge cycles. In certain such embodiments in which two half-density memory devices are transparently substituted for a single full-density memory device (as reported by the SPD device **240** to the memory controller), the memory devices advantageously support the "open row" feature.

[00118] FIG. 10A schematically illustrates an exemplary memory module **10** which doubles the rank density in accordance with certain embodiments described herein. The memory module **10** has a first memory capacity. The memory module **10** comprises a plurality of substantially identical memory devices **30** configured as a first rank **32a** and a second rank **32b**. In certain embodiments, the memory devices **30** of the first rank **32a** are configured in pairs, and the memory devices **30** of the second rank **32b** are also configured in pairs. In certain embodiments, the memory devices **30** of the first rank **32a** are configured with their respective DQS pins tied together and the memory devices **30** of the second rank **32b** are configured with their respective DQS pins tied together, as described more fully below. The memory module **10** further comprises a circuit **40** which receives a first set of address and command signals from a memory controller (not shown) of the computer system. The first set of address and command signals is compatible with a second memory capacity substantially equal to one-half of the first memory capacity. The circuit **40** translates the first

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set of address and command signals into a second set of address and command signals which is compatible with the first memory capacity of the memory module **10** and which is transmitted to the first rank **32a** and the second rank **32b**.

[00119] The first rank **32a** of FIG. 10A has 18 memory devices **30** and the second rank **32b** of FIG. 10A has 18 memory devices **30**. Other numbers of memory devices **30** in each of the ranks **32a**, **32b** are also compatible with embodiments described herein.

[00120] In the embodiment schematically illustrated by FIG. 10A, the memory module **10** has a width of 8 bytes (or 64 bits) and each of the memory devices **30** of FIG. 10A has a bit width of 4 bits. The 4-bit-wide ("×4") memory devices **30** of FIG. 10A have one-half the width, but twice the depth of 8-bit-wide ("×8") memory devices. Thus, each pair of "×4" memory devices **30** has the same density as a single "×8" memory device, and pairs of "×4" memory devices **30** can be used instead of individual "×8" memory devices to provide the memory density of the memory module **10**. For example, a pair of 512-Mb 128 M×4-bit memory devices has the same memory density as a 1-Gb 128 M×8-bit memory device.

[00121] For two "×4" memory devices **30** to work in tandem to mimic a "×8" memory device, the relative DQS pins of the two memory devices **30** in certain embodiments are advantageously tied together, as described more fully below. In addition, to access the memory density of a high-density memory module **10** comprising pairs of "×4" memory devices **30**, an additional address line is used. While a high-density memory module comprising individual "×8" memory devices with the next-higher density would also utilize an additional address line, the additional address lines are different in the two memory module configurations.

[00122] For example, a 1-Gb 128 M×8-bit DDR-1 DRAM memory device uses row addresses A_{13}-A_0 and column addresses A_{11} and A_9-A_0. A pair of 512-Mb 128 M×4-bit DDR-1 DRAM memory devices uses row addresses A_{12}-A_0 and column addresses A_{12}, A_{11}, and A_9-A_0. In certain embodiments, a memory controller of a computer system utilizing a 1-GB 128 M×8 memory module **10** comprising pairs of the 512-Mb 128 M×4 memory devices **30** supplies the address and command signals including the extra row address (A_{13}) to the memory module **10**. The circuit **40** receives the address and command signals from the memory controller and converts the extra row address (A_{13}) into an extra column address

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(A_{12}).

[00123] FIG. 10B schematically illustrates an exemplary circuit **40** compatible with embodiments described herein. The circuit **40** is used for a memory module **10** comprising pairs of "×4" memory devices **30** which mimic individual "×8" memory devices. In certain embodiments, each pair has the respective DQS pins of the memory devices **30** tied together. In certain embodiments, as schematically illustrated by FIG. 10B, the circuit **40** comprises a programmable-logic device (PLD) **42**, a first multiplexer **44** electrically coupled to the first rank **32a** of memory devices **30**, and a second multiplexer **46** electrically coupled to the second rank **32b** of memory devices **30**. In certain embodiments, the PLD **42** and the first and second multiplexers **44**, **46** are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42**, first multiplexer **44**, and second multiplexer **46** in accordance with embodiments described herein.

[00124] In the exemplary circuit **40** of FIG. 10B, during a row access procedure (CAS is high), the first multiplexer **44** passes the A_{12} address through to the first rank **32**, the second multiplexer **46** passes the A_{12} address through to the second rank **34**, and the PLD **42** saves or latches the A_{13} address from the memory controller. In certain embodiments, a copy of the A_{13} address is saved by the PLD **42** for each of the internal banks (e.g., 4 internal banks) per memory device **30**. During a subsequent column access procedure (CAS is low), the first multiplexer **44** passes the previously-saved A_{13} address through to the first rank **32a** as the A_{12} address and the second multiplexer **46** passes the previously-saved A_{13} address through to the second rank **32b** as the A_{12} address. The first rank **32a** and the second rank **32b** thus interpret the previously-saved A_{13} row address as the current A_{12} column address. In this way, in certain embodiments, the circuit **40** translates the extra row address into an extra column address in accordance with certain embodiments described herein.

[00125] Thus, by allowing two lower-density memory devices to be used rather than one higher-density memory device, certain embodiments described herein provide the advantage of using lower-cost, lower-density memory devices to build "next-generation" higher-density memory modules. Certain embodiments advantageously allow the use of lower-cost readily-available 512-Mb DDR-2 SDRAM devices to replace more expensive 1-Gb DDR-2 SDRAM devices. Certain embodiments advantageously reduce the total cost of

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the resultant memory module.

[00126] FIG. 11A schematically illustrates an exemplary memory module **10** which doubles number of ranks in accordance with certain embodiments described herein. The memory module **10** has a first plurality of memory locations with a first memory density. The memory module **10** comprises a plurality of substantially identical memory devices **30** configured as a first rank **32a**, a second rank **32b**, a third rank **32** *c*, and a fourth rank **32** *d*. The memory module **10** further comprises a circuit **40** which receives a first set of address and command signals from a memory controller (not shown). The first set of address and command signals is compatible with a second plurality of memory locations having a second memory density. The second memory density is substantially equal to one-half of the first memory density. The circuit **40** translates the first set of address and command signals into a second set of address and command signals which is compatible with the first plurality of memory locations of the memory module **10** and which is transmitted to the first rank **32a**, the second rank **32b**, the third rank **32** *c*, and the fourth rank **32** *d*.

[00127] Each rank **32a**, **32b**, **32** *c*, **32** *d* of FIG. 11A has 9 memory devices **30**. Other numbers of memory devices **30** in each of the ranks **32a**, **32b**, **32** *c*, **32** *d* are also compatible with embodiments described herein.

[00128] In the embodiment schematically illustrated by FIG. 11A, the memory module **10** has a width of 8 bytes (or 64 bits) and each of the memory devices **30** of FIG. 11A has a bit width of 8 bits. Because the memory module **10** has twice the number of 8-bit-wide ("×8") memory devices **30** as does a standard 8-byte-wide memory module, the memory module **10** has twice the density as does a standard 8-byte-wide memory module. For example, a 1-GB 128 M×8-byte memory module with 36 512-Mb 128 M×8-bit memory devices (arranged in four ranks) has twice the memory density as a 512-Mb 128 M×8-byte memory module with 18 512-Mb 128 M×8-bit memory devices (arranged in two ranks).

[00129] To access the additional memory density of the high-density memory module **10**, the two chip-select signals (CS_0, CS_1) are used with other address and command signals to gate a set of four gated CAS signals. For example, to access the additional ranks of four-rank 1-GB 128 M×8-byte DDR-1 DRAM memory module, the CS_0 and CS_1 signals along with the other address and command signals are used to gate the CAS signal appropriately, as schematically illustrated by FIG. 11A. FIG. 11B schematically illustrates an

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exemplary circuit **40** compatible with embodiments described herein. In certain embodiments, the circuit **40** comprises a programmable-logic device (PLD) **42** and four "OR" logic elements **52**, **54**, **56**, **58** electrically coupled to corresponding ranks **32a**, **32b**, **32** *c*, **32** *d* of memory devices **30**.

[00130] In certain embodiments, the PLD **42** comprises an ASIC, an FPGA, a custom-designed semiconductor device, or a CPLD. In certain embodiments, the PLD **42** and the four "OR" logic elements **52**, **54**, **56**, **58** are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42** and appropriate "OR" logic elements **52**, **54**, **56**, **58** in accordance with embodiments described herein.

[00131] In the embodiment schematically illustrated by FIG. 11B, the PLD **42** transmits each of the four "enabled CAS" ($ENCAS_0a$, $ENCAS_0b$, $ENCAS_1a$, $ENCAS_1b$) signals to a corresponding one of the "OR" logic elements **52**, **54**, **56**, **58**. The CAS signal is also transmitted to each of the four "OR" logic elements **52**, **54**, **56**, **58**. The CAS signal and the "enabled CAS" signals are "low" true signals. By selectively activating each of the four "enabled CAS" signals which are inputted into the four "OR" logic elements **52**, **54**, **56**, **58**, the PLD **42** is able to select which of the four ranks **32a**, **32b**, **32** *c*, **32** *d* is active.

[00132] In certain embodiments, the PLD **42** uses sequential and combinatorial logic procedures to produce the gated CAS signals which are each transmitted to a corresponding one of the four ranks **32a**, **32b**, **32** *c*, **32** *d*. In certain other embodiments, the PLD **42** instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS_0a, CS_0b, CS_1a, and CS_1b) which are each transmitted to a corresponding one of the four ranks **32a**, **32b**, **32** *c*, **32** *d*.

Tied Data Strobe Signal Pins

[00133] For proper operation, the computer system advantageously recognizes a 1-GB memory module comprising 256-Mb memory devices with 64 M×4-bit configuration as a 1-GB memory module having 512-Mb memory devices with 64 M×8-bit configuration (e.g., as a 1-GB memory module with 128 M×8-byte configuration). This advantageous result is desirably achieved in certain embodiments by electrically connecting together two output signal pins (e.g., DQS or data strobe pins) of the two 256-Mb memory devices such

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that both output signal pins are concurrently active when the two memory devices are concurrently enabled. The DQS or data strobe is a bi-directional signal that is used during both read cycles and write cycles to validate or latch data. As used herein, the terms "tying together" or "tied together" refer to a configuration in which corresponding pins (e.g., DQS pins) of two memory devices are electrically connected together and are concurrently active when the two memory devices are concurrently enabled (e.g., by a common chip-select or CS signal). Such a configuration is different from standard memory module configurations in which the output signal pins (e.g., DQS pins) of two memory devices are electrically coupled to the same source, but these pins are not concurrently active since the memory devices are not concurrently enabled. However, a general guideline of memory module design warns against tying together two output signal pins in this way.

[00134] FIGS. 12 and 13 schematically illustrate a problem which may arise from tying together two output signal pins. FIG. 12 schematically illustrates an exemplary memory module **305** in which a first DQS pin **312** of a first memory device **310** is electrically connected to a second DQS pin **322** of a second memory device **320**. The two DQS pins **312**, **322** are both electrically connected to a memory controller **330**.

[00135] FIG. 13 is an exemplary timing diagram of the voltages applied to the two DQS pins **312**, **322** due to non-simultaneous switching. As illustrated by FIG. 13, at time t_1, both the first DQS pin **312** and the second DQS pin **322** are high, so no current flows between them. Similarly, at time t_4, both the first DQS pin **312** and the second DQS pin **322** are low, so no current flows between them. However, for times between approximately t_2 and approximately t_3, the first DQS pin **312** is low while the second DQS pin **322** is high. Under such conditions, a current will flow between the two DQS pins **312**, **322**. This condition in which one DQS pin is low while the other DQS pin is high can occur for fractions of a second (e.g., 0.8 nanoseconds) during the dynamic random-access memory (DRAM) read cycle. During such conditions, the current flowing between the two DQS pins **312**, **322** can be substantial, resulting in heating of the memory devices **310**, **320**, and contributing to the degradation of reliability and eventual failure of these memory devices.

[00136] A second problem may also arise from tying together two output signal pins. FIG. 14 schematically illustrates another exemplary memory module **305** in which a first DQS pin **312** of a first memory device **310** is electrically connected to a second DQS pin

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322 of a second memory device **320**. The two DQS pins **312**, **322** of FIG. 14 are both electrically connected to a memory controller (not shown). The DQ (data input/output) pin **314** of the first memory device **310** and the corresponding DQ pin **324** of the second memory device **320** are each electrically connected to the memory controller by the DQ bus (not shown). Typically, each memory device **310**, **320** will have a plurality of DQ pins (e.g., eight DQ pins per memory device), but for simplicity, FIG. 14 only shows one DQ pin for each memory device **310**, **320**.

[00137] Each of the memory devices **310**, **320** of FIG. 14 utilizes a respective on-die termination or "ODT" circuit **332**, **334** which has termination resistors (e.g., 75 ohms) internal to the memory devices **310**, **320** to provide signal termination. Each memory device **310**, **320** has a corresponding ODT signal pin **362**, **364** which is electrically connected to the memory controller via an ODT bus **340**. The ODT signal pin **362** of the first memory device **310** receives a signal from the ODT bus **340** and provides the signal to the ODT circuit **332** of the first memory device **310**. The ODT circuit **332** responds to the signal by selectively enabling or disabling the internal termination resistors **352**, **356** of the first memory device **310**. This behavior is shown schematically in FIG. 14 by the switches **342**, **344** which are either closed (dash-dot line) or opened (solid line). The ODT signal pin **364** of the second memory device **320** receives a signal from the ODT bus **340** and provides the signal to the ODT circuit **334** of the second memory device **320**. The ODT circuit **334** responds to the signal by selectively enabling or disabling the internal termination resistors **354**, **358** of the second memory device **320**. This behavior is shown schematically in FIG. 14 by the switches **346**, **348** which are either closed (dash-dot line) or opened (solid line). The switches **342**, **344**, **346**, **348** of FIG. 14 are schematic representations of the operation of the ODT circuits **332**, **334**, and do not signify that the ODT circuits **332**, **334** necessarily include mechanical switches.

[00138] Examples of memory devices **310**, **320** which include such ODT circuits **332**, **334** include, but are not limited to, DDR2 memory devices. Such memory devices are configured to selectively enable or disable the termination of the memory device in this way in response to signals applied to the ODT signal pin of the memory device. For example, when the ODT signal pin **362** of the first memory device **310** is pulled high, the termination resistors **352**, **356** of the first memory device **310** are enabled. When the ODT signal pin **362**

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of the first memory device **310** is pulled low (e.g., grounded), the termination resistors **352**, **356** of the first memory device **310** are disabled. By selectively disabling the termination resistors of an active memory device, while leaving the termination resistors of inactive memory devices enabled, such configurations advantageously preserve signal strength on the active memory device while continuing to eliminate signal reflections at the bus-die interface of the inactive memory devices.

[00139] In certain configurations, as schematically illustrated by FIG. 14, the DQS pins **312**, **322** of each memory device **310**, **320** are selectively connected to a voltage VTT through a corresponding termination resistor **352**, **354** internal to the corresponding memory device **310**, **320**. Similarly, in certain configurations, as schematically illustrated by FIG. 14, the DQ pins **314**, **324** are selectively connected to a voltage VTT through a corresponding termination resistor **356**, **358** internal to the corresponding memory device **310**, **320**. In certain configurations, rather than being connected to a voltage VTT, the DQ pins **314**, **324** and/or the DQS pins **312**, **322** are selectively connected to ground through the corresponding termination resistors **352**, **354**, **356**, **358**. The resistances of the internal termination resistors **352**, **354**, **356**, **358** are selected to clamp the voltages so as to reduce the signal reflections from the corresponding pins. In the configuration schematically illustrated by FIG. 14, each internal termination resistor **352**, **354**, **356**, **358** has a resistance of approximately 75 ohms.

[00140] When connecting the first memory device **310** and, the second memory device **320** together to form a double word width, both the first memory device **310** and the second memory device **320** are enabled at the same time (e.g., by a common CS signal). Connecting the first memory device **310** and the second memory device **320** by tying the DQS pins **312**, **322** together, as shown in FIG. 14, results in a reduced effective termination resistance for the DQS pins **312**, **322**. For example, for the exemplary configuration of FIG. 14, the effective termination resistance for the DQS pins **312**, **322** is approximately 37.5 ohms, which is one-half the desired ODT resistance (for 75-ohm internal termination resistors) to reduce signal reflections since the internal termination resistors **352**, **354** of the two memory devices **310**, **320** are connected in parallel. This reduction in the termination resistance can result in signal reflections causing the memory device to malfunction.

[00141] FIG. 15 schematically illustrates an exemplary memory module **400** in accordance with certain embodiments described herein. The memory module **400** comprises

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a first memory device **410** having a first data strobe (DQS) pin **412** and a second memory device **420** having a second data strobe (DQS) pin **422**. The memory module **400** further comprises a first resistor **430** electrically coupled to the first DQS pin **412**. The memory module **400** further comprises a second resistor **440** electrically coupled to the second DQS pin **422** and to the first resistor **430**. The first DQS pin **412** is electrically coupled to the second DQS pin **422** through the first resistor **430** and through the second resistor **440**.

[00142] In certain embodiments, the memory module **400** is a 1-GB unbuffered Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) high-density dual in-line memory module (DIMM). FIGS. 16A and 16B schematically illustrate a first side **462** and a second side **464**, respectively, of such a memory module **400** with eighteen 64 M×4-bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board (PCB) **460**. In certain embodiments, the memory module **400** further comprises a phase-lock-loop (PLL) clock driver **470**, an EEPROM for serial-presence detect (SPD) data **480**, and decoupling capacitors (not shown) mounted on the PCB in parallel to suppress switching noise on VDD and VDDQ power supply for DDR-1 SDRAM. By using synchronous design, such memory modules **400** allow precise control of data transfer between the memory module **400** and the system controller. Data transfer can take place on both edges of the DQS signal at various operating frequencies and programming latencies. Therefore, certain such memory modules **400** are suitable for a variety of high-performance system applications.

[00143] In certain embodiments, the memory module **400** comprises a plurality of memory devices configured in pairs, each pair having a first memory device **410** and a second memory device **420**. For example, in certain embodiments, a 128 M×72-bit DDR SDRAM high-density memory module **400** comprises thirty-six 64 M×4-bit DDR-1 SDRAM integrated circuits in FBGA packages configured in eighteen pairs. The first memory device **410** of each pair has the first DQS pin **412** electrically coupled to the second DQS pin **422** of the second memory device **420** of the pair. In addition, the first DQS pin **412** and the second DQS pin **422** are concurrently active when the first memory device **410** and the second memory device **420** are concurrently enabled.

[00144] In certain embodiments, the first resistor **430** and the second resistor **440** each has a resistance advantageously selected to reduce the current flow between the first

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DQS pin **412** and the second DQS pin **422** while allowing signals to propagate between the memory controller and the DQS pins **412**, **422**. In certain embodiments, each of the first resistor **430** and the second resistor **440** has a resistance in a range between approximately 5 ohms and approximately 50 ohms. For example, in certain embodiments, each of the first resistor **430** and the second resistor **440** has a resistance of approximately 22 ohms. Other resistance values for the first resistor **430** and the second resistor **440** are also compatible with embodiments described herein. In certain embodiments, the first resistor **430** comprises a single resistor, while in other embodiments, the first resistor **430** comprises a plurality of resistors electrically coupled together in series and/or in parallel. Similarly, in certain embodiments, the second resistor **440** comprises a single resistor, while in other embodiments, the second resistor **440** comprises a plurality of resistors electrically coupled together in series and/or in parallel.

[00145] FIGS. 17A and 17B schematically illustrate an exemplary embodiment of a memory module **400** in which the first resistor **430** and the second resistor **440** are used to reduce the current flow between the first DQS pin **412** and the second DQS pin **422**. As schematically illustrated by FIG. 17A, the memory module **400** is part of a computer system **500** having a memory controller **510**. The first resistor **430** has a resistance of approximately 22 ohms and the second resistor **440** has a resistance of approximately 22 ohms. The first resistor **430** and the second resistor **440** are electrically coupled in parallel to the memory controller **510** through a signal line **520** having a resistance of approximately 25 ohms. The first resistor **430** and the second resistor **440** are also electrically coupled in parallel to a source of a fixed termination voltage (identified by VTT in FIGS. 17A and 17B) by a signal line **540** having a resistance of approximately 47 ohms. Such an embodiment can advantageously be used to allow two memory devices having lower bit widths (e.g., 4-bit) to behave as a single virtual memory device having a higher bit width (e.g., 8-bit).

[00146] FIG. 17B schematically illustrates exemplary current-limiting resistors **430**, **440** in conjunction with the impedances of the memory devices **410**, **420**. During an exemplary portion of a data read operation, the memory controller **510** is in a high-impedance condition, the first memory device **410** drives the first DQS pin **412** high (e.g., 2.7 volts), and the second memory device **420** drives the second DQS pin **422** low (e.g., 0 volts). The amount of time for which this condition occurs is approximated by the time between t_2

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and t_3 of FIG. 13, which in certain embodiments is approximately twice the tDQSQ (data strobe edge to output data edge skew time, e.g., approximately 0.8 nanoseconds). At least a portion of this time in certain embodiments is caused by simultaneous switching output (SSO) effects.

[00147] In certain embodiments, as schematically illustrated by FIG. 17B, the DQS driver of the first memory device **410** has a driver impedance R_1 of approximately 17 ohms, and the DQS driver of the second memory device **420** has a driver impedance R_4 of approximately 17 ohms. Because the upper network of the first memory device **410** and the first resistor **430** (with a resistance R_2 of approximately 22 ohms) is approximately equal to the lower network of the second memory device **420** and the second resistor **440** (with a resistance R_3 of approximately 22 ohms), the voltage at the midpoint is approximately 0.5*(2.7−0)=1.35 volts, which equals VTT, such that the current flow across the 47-ohm resistor of FIG. 17B is approximately zero.

[00148] The voltage at the second DQS pin **422** in FIG. 17B is given by $V_{DQS2}=2.7*R_4/(R_1+R_2+R_3+R_4)=0.59$ volts and the current flowing through the second DQS pin **422** is given by $I_{DQS2}=0.59/R_4=34$ milliamps. The power dissipation in the DQS driver of the second memory device **420** is thus $P_{DQS2}=34$ mA*0.59 V=20 milliwatts. In contrast, without the first resistor **430** and the second resistor **440**, only the 17-ohm impedances of the two memory devices **410**, **420** would limit the current flow between the two DQS pins **412**, **422**, and the power dissipation in the DQS driver of the second memory device **420** would be approximately 107 milliwatts. Therefore, the first resistor **430** and the second resistor **440** of FIGS. 17A and 17B advantageously limit the current flowing between the two memory devices during the time that the DQS pin of one memory device is driven high and the DQS pin of the other memory device is driven low.

[00149] In certain embodiments in which there is overshoot or undershoot of the voltages, the amount of current flow can be higher than those expected for nominal voltage values. Therefore, in certain embodiments, the resistances of the first resistor **430** and the second resistor **440** are advantageously selected to account for such overshoot/undershoot of voltages.

[00150] For certain such embodiments in which the voltage at the second DQS pin **422** is $V_{DQS2}=0.59$ volts and the duration of the overdrive condition is approximately 0.8

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nanoseconds at maximum, the total surge is approximately 0.59 V*1.2 ns=0.3 V-ns. For comparison, the JEDEC standard for overshoot/undershoot is 2.4 V-ns, so certain embodiments described herein advantageously keep the total surge within predetermined standards (e.g., JEDEC standards).

[00151] FIG. 18 schematically illustrates another exemplary memory module **600** compatible with certain embodiments described herein. The memory module **600** comprises a termination bus **605**. The memory module **600** further comprises a first memory device **610** having a first data strobe pin **612**, a first termination signal pin **614** electrically coupled to the termination bus **605**, a first termination circuit **616**, and at least one data pin **618**. The first termination circuit **616** selectively electrically terminating the first data strobe pin **612** and the first data pin **618** in response to a first signal received by the first termination signal pin **614** from the termination bus **605**. The memory module **600** further comprises a second memory device **620** having a second data strobe pin **622** electrically coupled to the first data strobe pin **612**, a second termination signal pin **624**, a second termination circuit **626**, and at least one data pin **628**. The second termination signal pin **624** is electrically coupled to a voltage, wherein the second termination circuit **626** is responsive to the voltage by not terminating the second data strobe pin **622** or the second data pin **628**. The memory module **600** further comprises at least one termination assembly **630** having a third termination signal pin **634**, a third termination circuit **636**, and at least one termination pin **638** electrically coupled to the data pin **628** of the second memory device **620**. The third termination signal pin **634** is electrically coupled to the termination bus **605**. The third termination circuit **636** selectively electrically terminates the data pin **628** of the second memory device **620** through the termination pin **638** in response to a second signal received by the third termination signal pin **634** from the termination bus **605**.

[00152] FIG. 19 schematically illustrates a particular embodiment of the memory module **600** schematically illustrated by FIG. 18. The memory module **600** comprises an on-die termination (ODT) bus **605**. The memory module **600** comprises a first memory device **610** having a first data strobe (DQS) pin **612**, a first ODT signal pin **614** electrically coupled to the ODT bus **605**, a first ODT circuit **616**, and at least one data (DQ) pin **618**. The first ODT circuit **616** selectively electrically terminates the first DQS pin **612** and the DQ pin **618** of the first memory device **610** in response to an ODT signal received by the first ODT signal

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pin **614** from the ODT bus **605**. This behavior of the first ODT circuit **616** is schematically illustrated in FIG. 14 by the switches **672**, **676** which are selectively closed (dash-dot line) or opened (solid line).

[00153] The memory module **600** further comprises a second memory device **620** having a second DQS pin **622** electrically coupled to the first DQS pin **612**, a second ODT signal pin **624**, a second ODT circuit **626**, and at least one DQ pin **628**. The first DQS pin **612** and the second DQS pin **622** are concurrently active when the first memory device **610** and the second memory device **620** are concurrently enabled. The second ODT signal pin **624** is electrically coupled to a voltage (e.g., ground), wherein the second ODT circuit **626** is responsive to the voltage by not terminating the second DQS pin **622** or the second DQ pin **624**. This behavior of the second ODT circuit **626** is schematically illustrated in FIG. 14 by the switches **674**, **678** which are opened.

[00154] The memory module **600** further comprises at least one termination assembly **630** having a third ODT signal pin **634** electrically coupled to the ODT bus **605**, a third ODT circuit **636**, and at least one termination pin **638** electrically coupled to the DQ pin **628** of the second memory device **620**. The third ODT circuit **636** selectively electrically terminates the DQ pin **628** of the second memory device **620** through the termination pin **638** in response to an ODT signal received by the third ODT signal pin **634** from the ODT bus **605**. This behavior of the third ODT circuit **636** is schematically illustrated in FIG. 19 by the switch **680** which is either closed (dash-dot line) or opened (solid line).

[00155] In certain embodiments, the termination assembly **630** comprises discrete electrical components which are surface-mounted or embedded on the printed-circuit board of the memory module **600**. In certain other embodiments, the termination assembly **630** comprises an integrated circuit mounted on the printed-circuit board of the memory module **600**. Persons skilled in the art can provide a termination assembly **630** in accordance with embodiments described herein.

[00156] Certain embodiments of the memory module **600** schematically illustrated by FIG. 19 advantageously avoid the problem schematically illustrated by FIG. 12 of electrically connecting the internal termination resistances of the DQS pins of the two memory devices in parallel. As described above in relation to FIG. 14, FIGS. 18 and 19 only show one DQ pin for each memory device for simplicity. Other embodiments have a

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plurality of DQ pins for each memory device. In certain embodiments, each of the first ODT circuit **616**, the second ODT circuit **626**, and the third ODT circuit **636** are responsive to a high voltage or signal level by enabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by disabling the corresponding termination resistors. In other embodiments, each of the first ODT circuit **616**, the second ODT circuit **626**, and the third ODT circuit **636** are responsive to a high voltage or signal level by disabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by enabling the corresponding termination resistors. Furthermore, the switches **672**, **674**, **676**, **678**, **680** of FIG. 18 are schematic representations of the enabling and disabling operation of the ODT circuits **616**, **626**, **636** and do not signify that the ODT circuits **616**, **626**, **636** necessarily include mechanical switches.

[00157] The first ODT signal pin **614** of the first memory device **610** receives an ODT signal from the ODT bus **605**. In response to this ODT signal, the first ODT circuit **616** selectively enables or disables the termination resistance for both the first DQS pin **612** and the DQ pin **618** of the first memory device **610**. The second ODT signal pin **624** of the second memory device **620** is tied (e.g., directly hard-wired) to the voltage (e.g., ground), thereby disabling the internal termination resistors **654**, **658** on the second DQS pin **622** and the second DQ pin **628**, respectively, of the second memory device **620** (schematically shown by open switches **674**, **678** in FIG. 19). The second DQS pin **622** is electrically coupled to the first DQS pin **612**, so the termination resistance for both the first DQS pin **612** and the second DQS pin **622** is provided by the termination resistor **652** internal to the first memory device **510**.

[00158] The termination resistor **656** of the DQ pin **618** of the first memory device **610** is enabled or disabled by the ODT signal received by the first ODT signal pin **614** of the first memory device **610** from the ODT bus **605**. The termination resistance of the DQ pin **628** of the second memory device **620** is enabled or disabled by the ODT signal received by the third ODT signal pin **634** of the termination assembly **630** which is external to the second memory device **620**. Thus, in certain embodiments, the first ODT signal pin **614** and the third ODT signal pin **634** receive the same ODT signal from the ODT bus **605**, and the termination resistances for both the first memory device **610** and the second memory device **620** are selectively enabled or disabled in response thereto when these memory devices are

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concurrently enabled. In this way, certain embodiments of the memory module **600** schematically illustrated by FIG. 19 provides external or off-chip termination of the second memory device **620**.

[00159] Certain embodiments of the memory module **600** schematically illustrated by FIG. 19 advantageously allow the use of two lower-cost readily-available 512-Mb DDR-2 SDRAM devices to provide the capabilities of a more expensive 1-GB DDR-2 SDRAM device. Certain such embodiments advantageously reduce the total cost of the resultant memory module **600**.

[00160] Certain embodiments described herein advantageously increase the memory capacity or memory density per memory slot or socket on the system board of the computer system. Certain embodiments advantageously allow for higher memory capacity in systems with limited memory slots. Certain embodiments advantageously allow for flexibility in system board design by allowing the memory module **10** to be used with computer systems designed for different numbers of ranks (e.g., either with computer systems designed for two-rank memory modules or with computer systems designed for four-rank memory modules). Certain embodiments advantageously provide lower costs of board designs.

[00161] In certain embodiments, the memory density of a memory module is advantageously doubled by providing twice as many memory devices as would otherwise be provided. For example, pairs of lower-density memory devices can be substituted for individual higher-density memory devices to reduce costs or to increase performance. As another example, twice the number of memory devices can be used to produce a higher-density memory configuration of the memory module. Each of these examples can be limited by the number of chip select signals which are available from the memory controller or by the size of the memory devices. Certain embodiments described herein advantageously provide a logic mechanism to overcome such limitations.

[00162] Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

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We Claim:

1. A memory module operable to communicate data with a memory controller via a data bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising:

a plurality of memory integrated circuits including at least one first memory integrated circuit and at least one second memory integrated circuit; and

a buffer coupled between the at least one first memory integrated circuit and the data bus, and between the at least one second memory integrated circuit and the data bus, wherein the buffer couples the at least one first memory integrated circuit to the data bus and isolates the at least one second memory integrated circuit from the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command, the buffer couples the at least one second memory integrated circuit to the data bus and isolates the at least one first memory integrated circuit from the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command.

2. The memory module of claim 1, wherein the buffer isolates both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the data bus when the memory module is not being accessed by the memory controller.

3. The memory module of claim 1, wherein the first memory command includes at least one first chip select signal and the second memory command includes at least one second chip select signal that is the same as the at least one first chip select signal.

4. The memory module of claim 3, wherein the memory module produces at least third and fourth chip select signals in response to the first memory command, the third chip select signal being provided to the at least one first memory integrated circuit and having an active value to select the at least one first memory integrated circuit to receive or output data signals

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in response to the first memory command, the fourth chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals.

5. The memory module of claim 4, wherein the memory module produces at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an active value to select the at least one second memory integrated circuit to receive or output data signals in response to the second memory command.

6. The memory module of claim 1, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein memory module outputs the first data burst together with a first burst of data strobes in response to the first read command, wherein memory module outputs the second data burst together with a second burst of data strobes in response to the second read command, wherein the second data burst follows the first data burst on the data bus, and wherein the buffer prevents the first burst of data strobes and the second burst of data strobes from colliding with each other.

7. The memory module of claim 6, wherein each of the first burst of data strobes and the second burst of data strobes includes a pre-amble interval and a post-amble interval, and wherein the buffer combines the first burst of data strobes and the second burst of data strobes into a combined burst of data strobes that does not include the post-amble interval of the first burst of data strobes and the pre-amble interval of the second burst of data strobes.

8. The memory module of claim 1, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of the memory integrated circuits.

9. The memory module of claim 1, further comprising an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS

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latency having one more cycle than an actual operational CAS latency of the memory integrated circuits.

10. The memory module of claim 1, wherein the memory commands further includes a third memory command, the third memory command being one of a refresh command or a precharge command, and wherein the buffer couples both the at least one first memory integrated circuit and the at least one second memory integrated circuit to the data bus in response to the third memory command.

11. A method of operating a memory module coupled to a memory controller via a memory bus including a control/address (C/A) bus and a data bus, the memory module comprising memory integrated circuits, including at least one first memory integrated circuit and at least one second memory integrated circuit, the method comprising:

receiving from the memory controller a first set of input C/A signals associated with a first memory command via the C/A bus, the first memory command to cause the memory module to receive or output a first data burst;

generating a first set of output C/A signals in response to the first set of input C/A signals, the first set of output C/A signals causing the at least one first memory integrated circuit to receive or output the first data burst;

receiving from the memory controller a second set of input control/address signals associated with a second memory command via the C/A bus, the second memory command to cause the memory module to receive or output a second data burst;

generating a second set of output C/A signals in response to the second set of input C/A signals, the second set of output C/A signals causing the at least one second memory integrated circuit to receive or output the second data burst;

coupling the at least one first memory integrated circuit to the data bus and isolating the at least one second memory integrated circuit from the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command; and

coupling the at least one second memory integrated circuit to the data bus and isolating the at least one first memory integrated circuit from the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command.

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12. The method of claim 11, further comprising isolating the at least one first memory integrated circuit and the at least one second memory integrated circuit from the data bus when the memory module is not being accessed by the memory system.

13. The method of claim 11, wherein the first set of input C/A signals include at least one input chip-select signal, the method further comprising generating a greater number of output chip-select signals than the at least one input chip-select signal, the greater number of output chip-select signals including a first chip select signal and a second chip select signal, the first chip-select signal being provided to at least one first memory integrated circuit and having an active value to select the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the second chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals.

14. The method of claim 11, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the memory module outputs the first data burst together with a first burst of data strobes in response to the first read command, wherein the memory module outputs the second data burst together with a second burst of data strobes in response to the second read command, wherein the second data burst follows the first data burst on the data bus, the method further comprising combining the first burst of data strobes and the second burst of data strobes to form a third burst of data strobes on the data bus.

15. The method of claim 14, wherein each of the first burst of data strobes and the second burst of data strobes includes a pre-amble interval and a post-amble interval, and wherein the third burst of data strobes does not include the post-amble interval of the first burst of data strobes and the pre-amble interval of the second burst of data strobes.

16. The method of claim 11, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of the memory integrated circuits.

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17. The method of claim 11, further comprising reporting an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more cycle than an actual operational CAS latency of the memory integrated circuits.

18. The method of claim 1, further comprising:

receiving from the memory controller a third set of input C/A signals associated with a third memory command via the C/A bus, the third memory command being one of a refresh or precharge command;

generating a third set of output C/A signals in response to the third set of input C/A signals, the third set of output C/A signals causing the at least one first memory integrated circuit and the at least one second memory integrated circuit to perform one of a refresh operation and a pre-charge operation; and

in response to the third memory command, coupling both the at least one first memory integrated circuit and the at least one second memory integrated circuit to the data bus.

19. A circuit in a memory module that is operable to communicate data with a memory controller via a data bus in response to memory commands received from the memory controller, the memory module including at least one first memory integrated circuit and at least one second memory integrated circuit, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the at least one first memory integrated circuit to receive or output a first data burst and the second memory command to cause the at least one second memory integrated circuit to receive or output a second data burst, the circuit comprising:

a first data path coupled to the at least one first memory integrated circuit and not coupled to the at least one second memory integrated circuit;

a second data path coupled to the at least one second memory integrated circuit and not coupled to the at least one first memory integrated circuit; and

logic that couples the at least one first memory integrated circuit to the data bus via the first data path and that isolates the at least one second memory integrated circuit from the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command, and wherein the logic couples the at least one second memory integrated circuit to the data bus via the second data path and isolates the at least one first

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memory integrated circuit from the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command.

20. The circuit of claim 19, wherein the logic isolates both the first data path and the second data path from the data bus when the memory module is not being accessed by the memory controller.

21. The circuit of claim 19, wherein the memory commands further includes a third memory command, the third memory command being one of a refresh command or a precharge command, and wherein the logic couples both the at least one first memory integrated circuit and the at least one second memory integrated circuit to the data bus in response to the third memory command.

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MEMORY MODULE WITH DATA BUFFERING

ABSTRACT OF THE DISCLOSURE

A memory module is operable to communicate data with a memory controller via a data bus in response to memory commands received from the memory controller. The memory module comprises a plurality of memory integrated circuits including at least one first memory integrated circuit and at least one second memory integrated circuit, and further comprises a buffer that couples the at least one first memory integrated circuit to the data bus and isolates the at least one second memory integrated circuit from the data bus while the memory module is receiving or outputting a first data burst in response to a first memory command. The buffer then couples the at least one second memory integrated circuit to the data bus and isolates the at least one first memory integrated circuit from the data bus while the memory module is receiving or outputting a second data burst in response to a second memory command.

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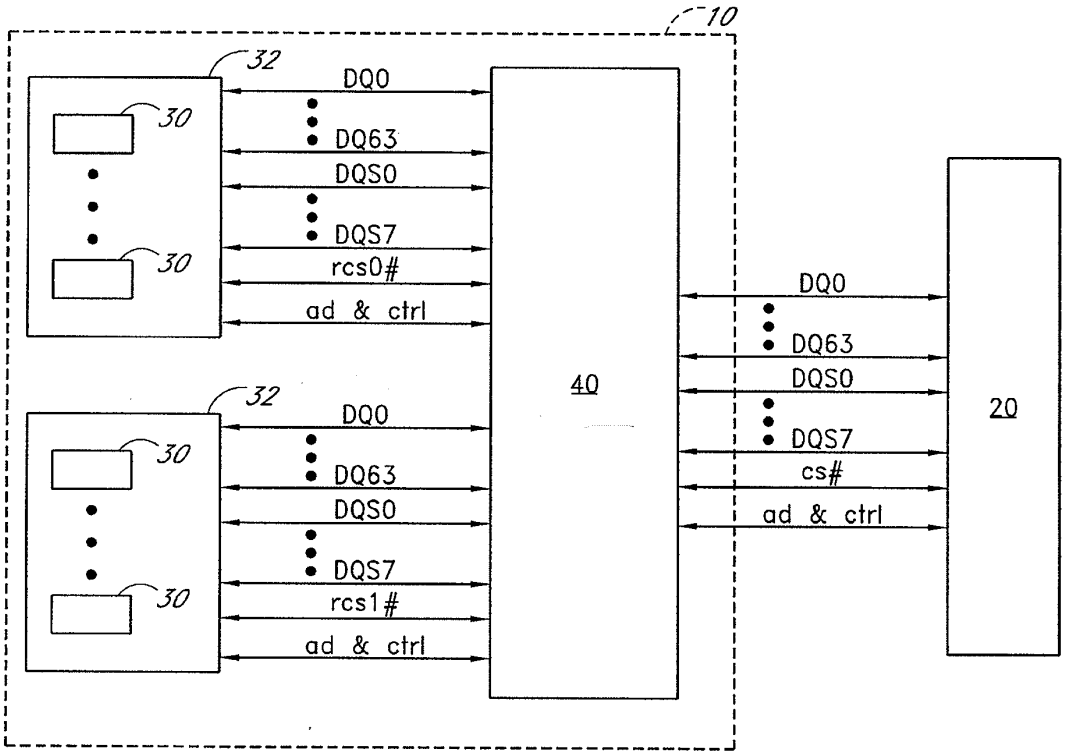

10
32
30
30
DQ0
DQ63
DQS0
DQS7
rcs0#
ad & ctrl
32
30
30
DQ0
DQ63
DQS0
DQS7
rcs1#
ad & ctrl
40
DQ0
DQ63
DQS0
DQS7
cs#
ad & ctrl
20

FIG. 1

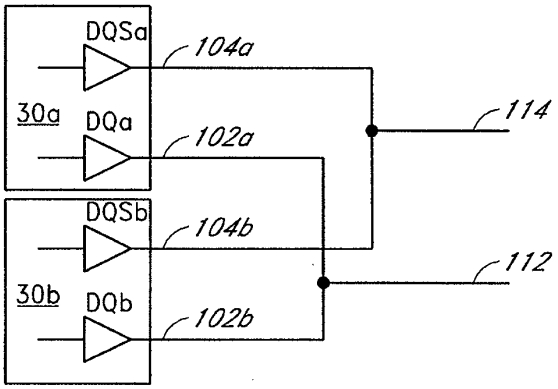


FIG. 2

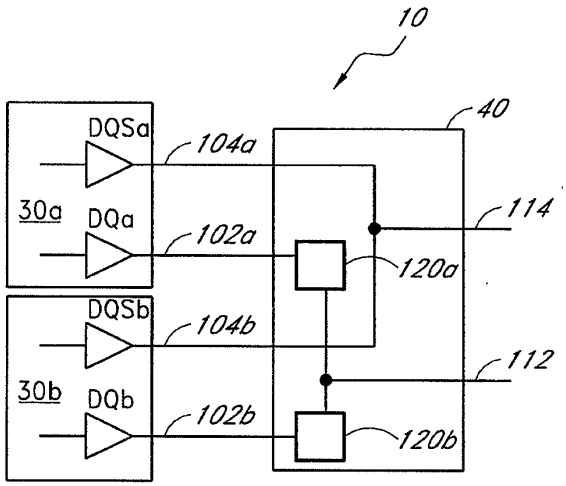

10
40
DQSa
104a
30a
DQa
102a
114
120a
DQSb
104b
112
30b
DQb
102b
120b

FIG. 3A

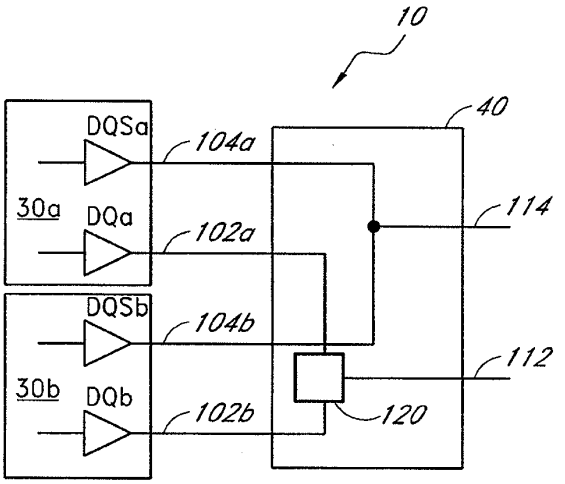

10
40
DQSa
104a
30a
DQa
102a
114
DQSb
104b
112
30b
DQb
102b
120

FIG. 3B

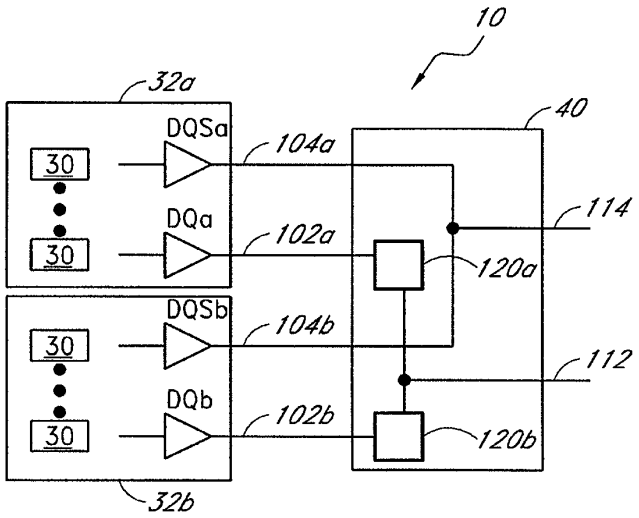

10
32a
40
DQSa
104a
30
DQa
102a
114
30
120a
DQSb
104b
30
112
DQb
102b
30
120b
32b

FIG. 4A

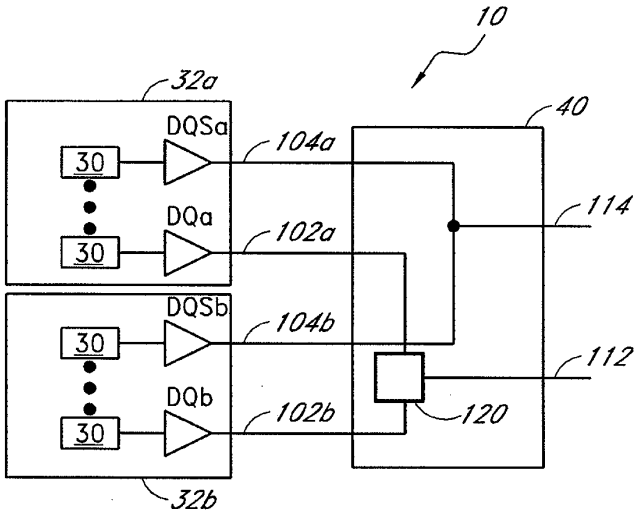

10
32a
40
DQSa
104a
30
114
DQa
102a
30
DQSb
104b
30
112
DQb
102b
30
120
32b

FIG. 4B

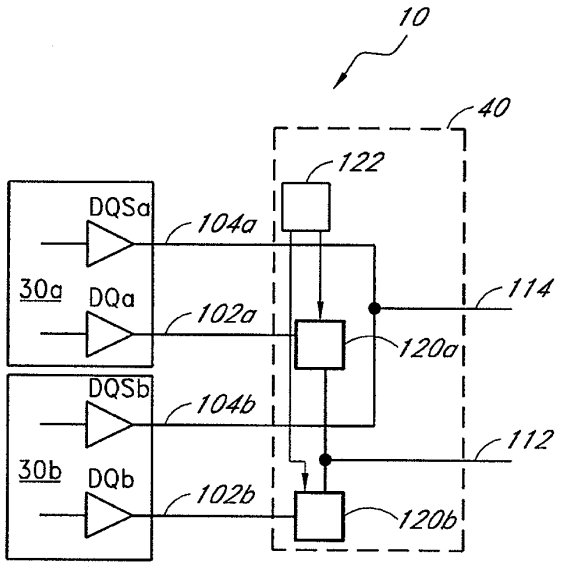

10
40
122
DQSa
104a
30a
DQa
102a
114
120a
DQSb
104b
112
30b
DQb
102b
120b

FIG. 5A

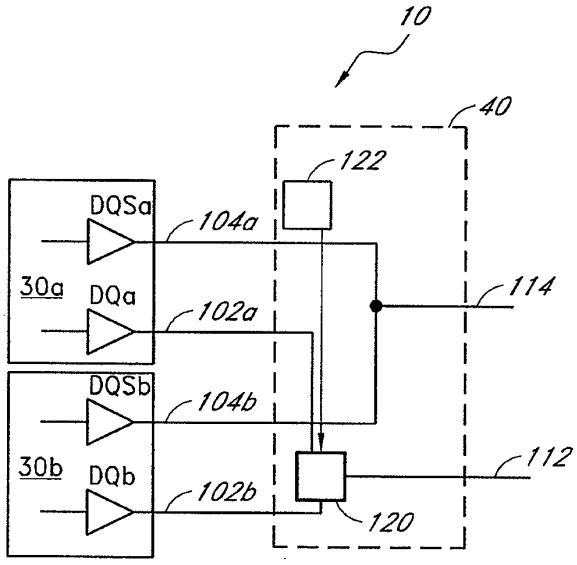

10
40
122
DQSa
104a
30a
DQa
102a
114
DQSb
104b
112
30b
DQb
102b
120

FIG. 5B

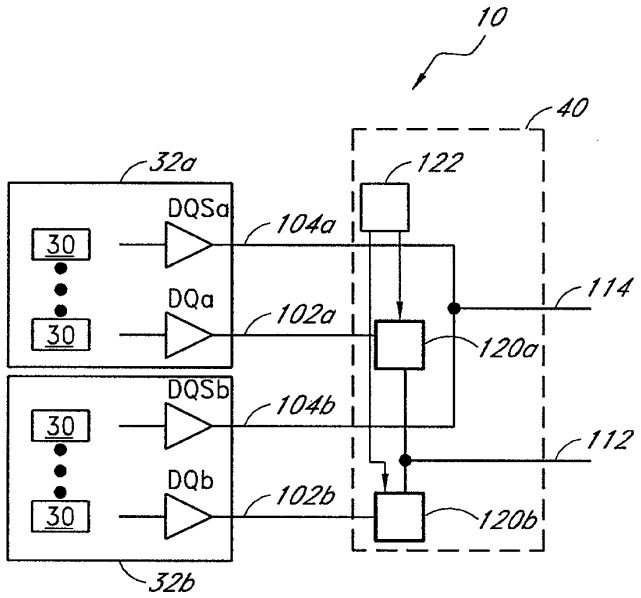

10
40
32a
122
DQSa
104a
30
DQa
102a
114
120a
DQSb
104b
112
DQb
102b
120b
32b

FIG. 5C

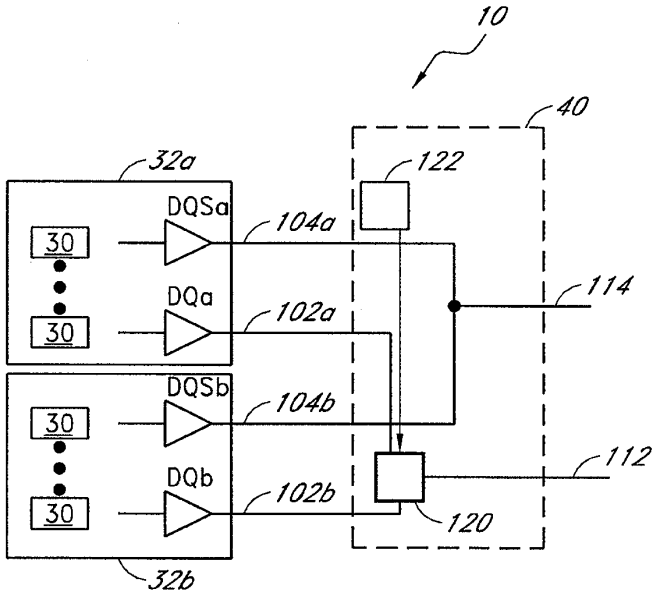

10
40
32a
122
DQSa
104a
30
DQa
102a
114
DQSb
104b
112
DQb
102b
120
32b

FIG. 5D

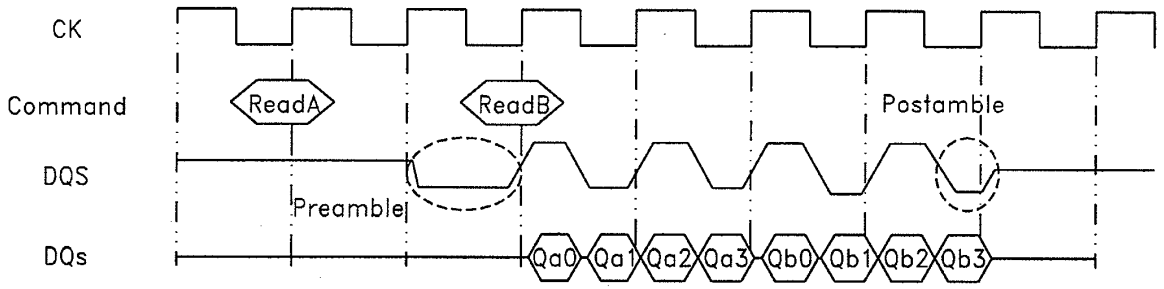

CK
Command
ReadA
ReadB
Postamble
DQS
Preamble
DQs
Qa0
Qa1
Qa2
Qa3
Qb0
Qb1
Qb2
Qb3

FIG. 6A

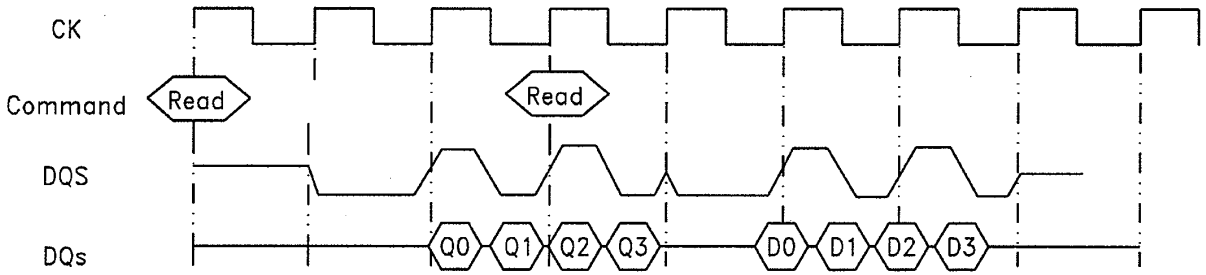

CK
Command
Read
Read
DQS
DQs
Q0
Q1
Q2
Q3
D0
D1
D2
D3

FIG. 6B

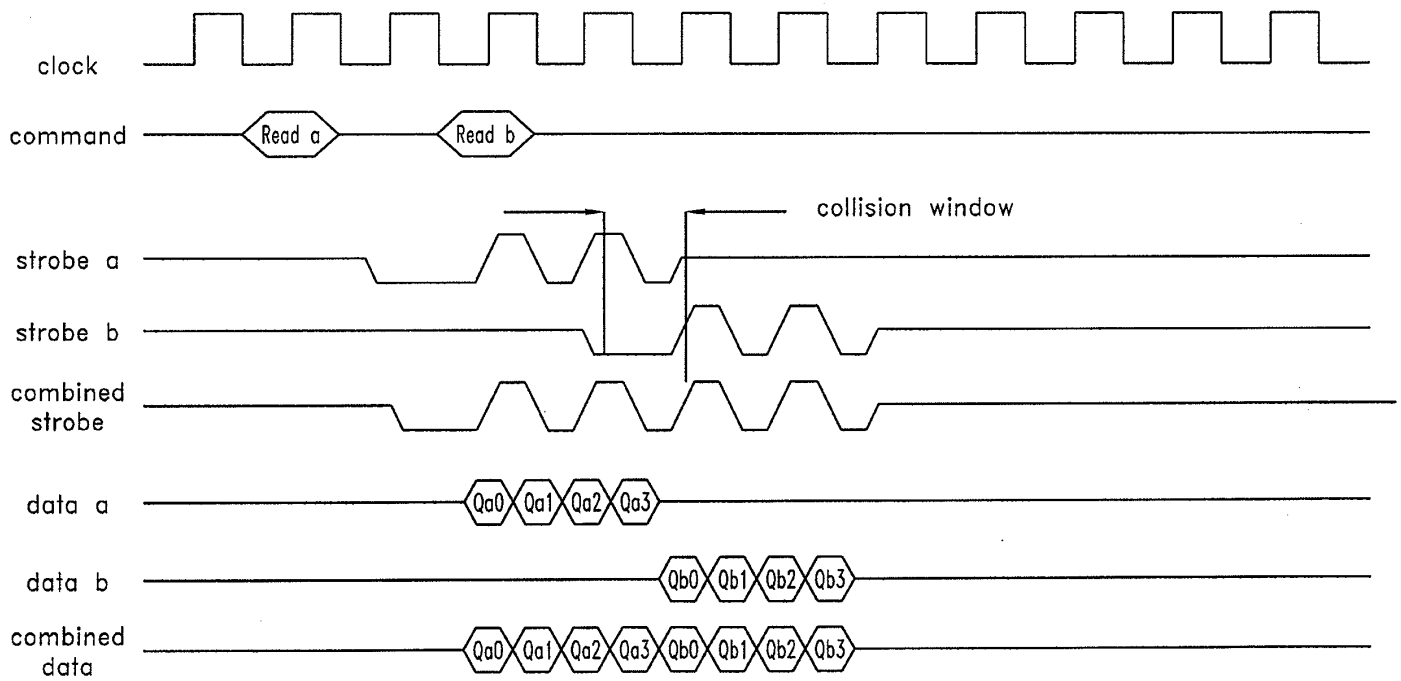

clock
command
Read a
Read b
collision window
strobe a
strobe b
combined strobe
data a
Qa0
Qa1
Qa2
Qa3
data b
Qb0
Qb1
Qb2
Qb3
combined data
Qa0
Qa1
Qa2
Qa3
Qb0
Qb1
Qb2
Qb3

FIG. 7

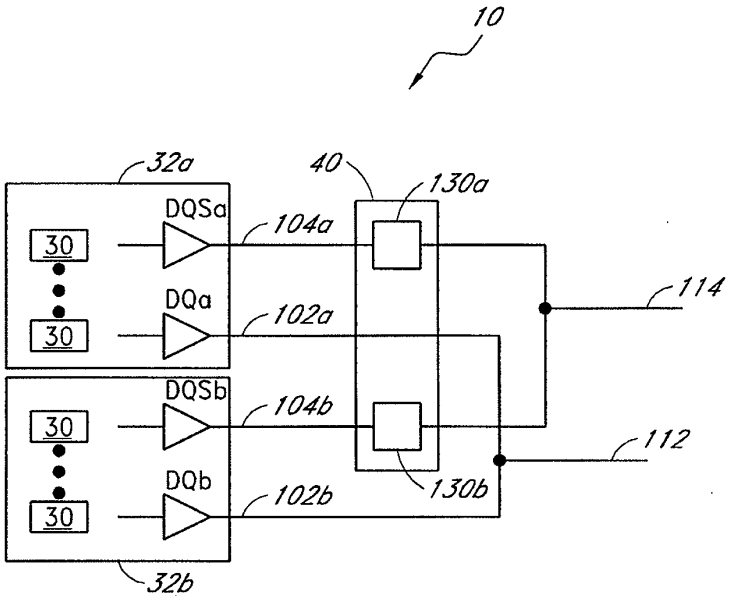

10
32a
40
130a
DQSa
104a
30
30
DQa
102a
114
DQSb
104b
30
30
112
DQb
102b
130b
32b

FIG. 8A

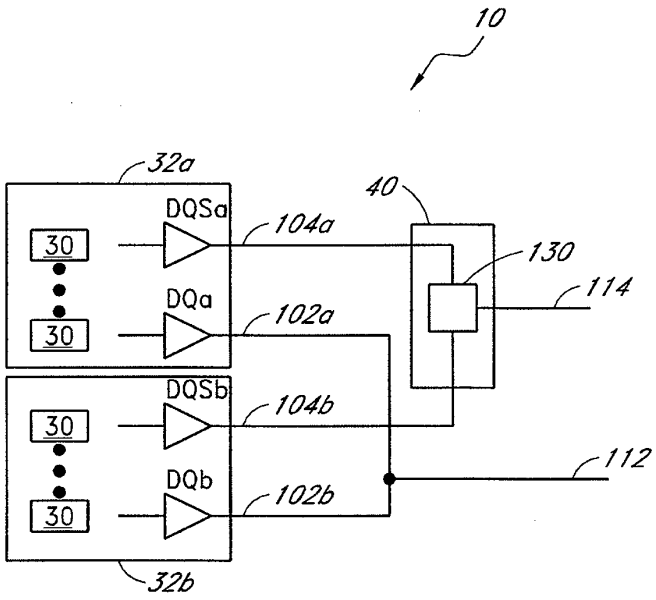

10
32a
40
DQSa
104a
130
30
30
114
DQa
102a
DQSb
104b
30
30
112
DQb
102b
32b

FIG. 8B

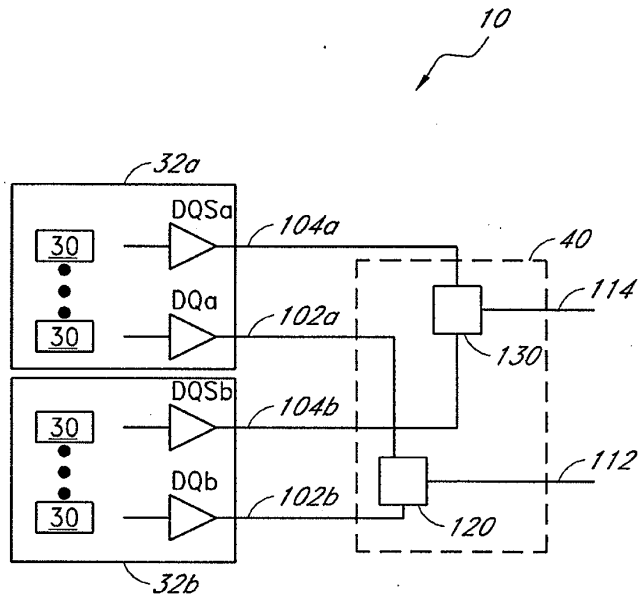

10
32a
DQSa
104a
40
30
DQa
102a
114
30
130
DQSb
104b
30
112
DQb
102b
30
120
32b

FIG. 8C

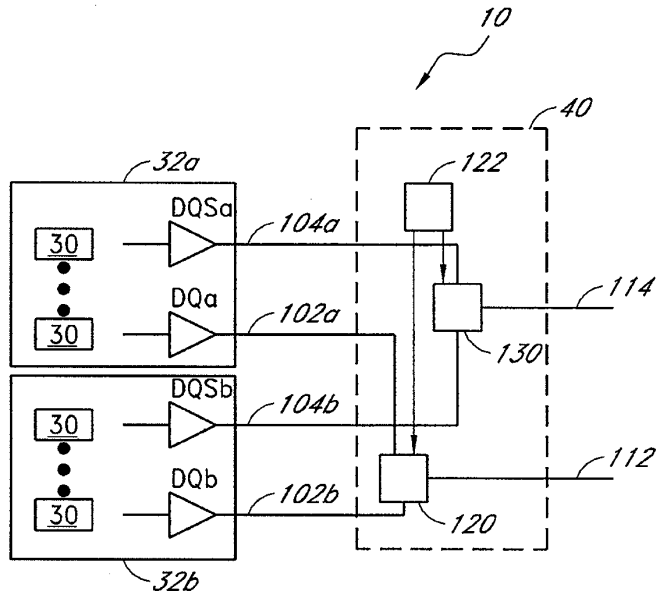

10
40
32a
122
DQSa
104a
30
114
DQa
102a
30
130
DQSb
104b
30
112
DQb
102b
30
120
32b

FIG. 8D

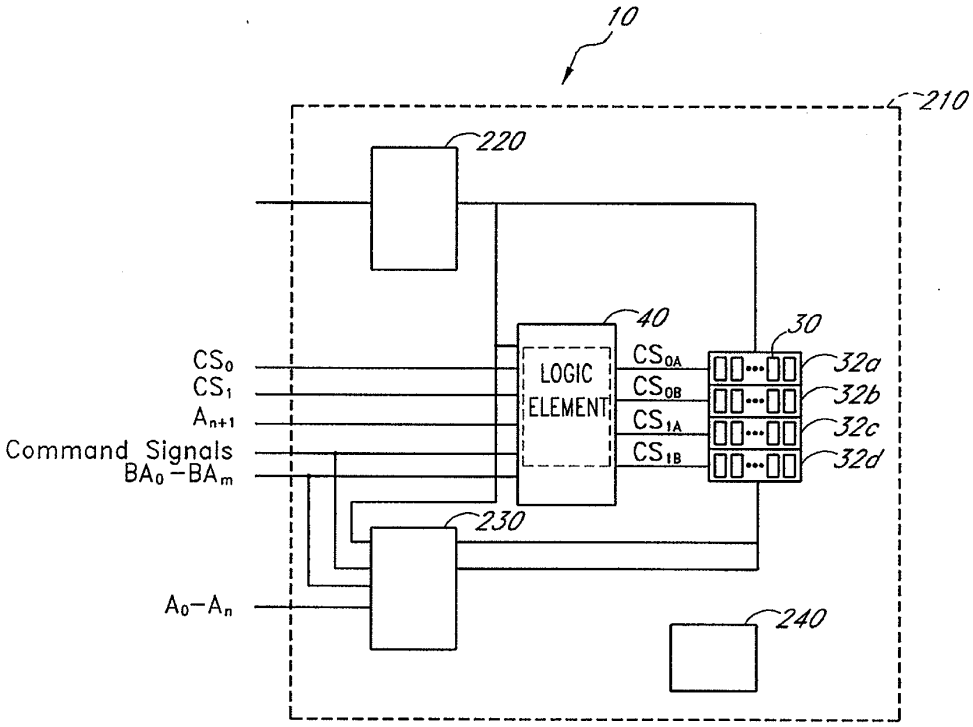

10
210
220
40
30
LOGIC ELEMENT
CS_0
CS_1
A_{n+1}
Command Signals
BA_0-BA_m
CS_{0A}
CS_{0B}
CS_{1A}
CS_{1B}
32a
32b
32c
32d
230
A_0-A_n
240

FIG. 9A

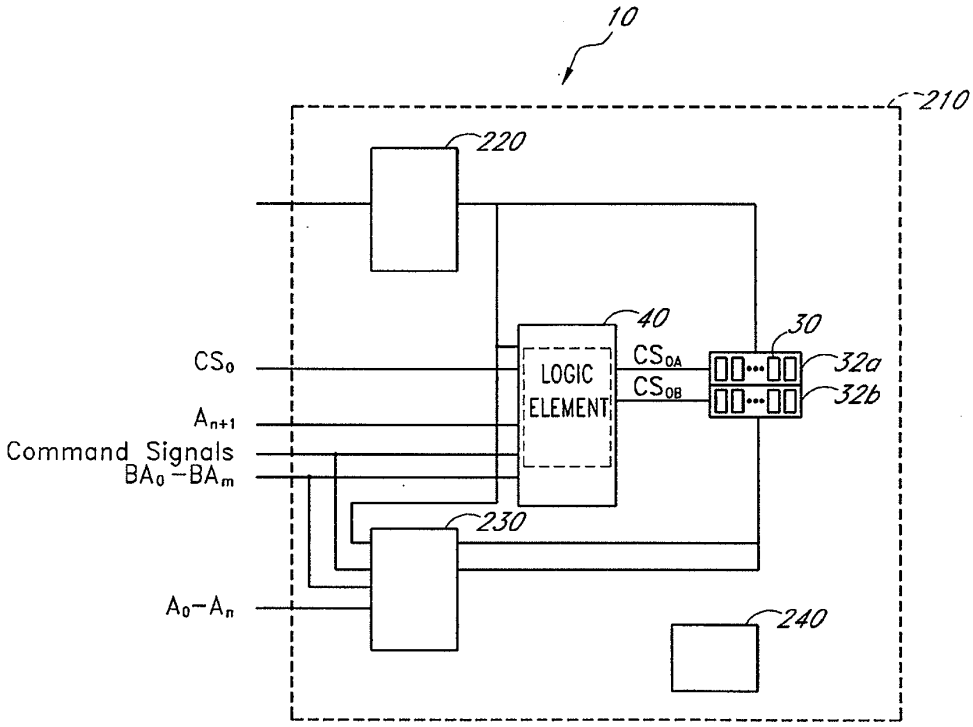

10
210
220
40
30
LOGIC ELEMENT
CS_0
CS_{0A}
CS_{0B}
32a
32b
A_{n+1}
Command Signals
$BA_0 - BA_m$
230
$A_0 - A_n$
240

FIG. 9B

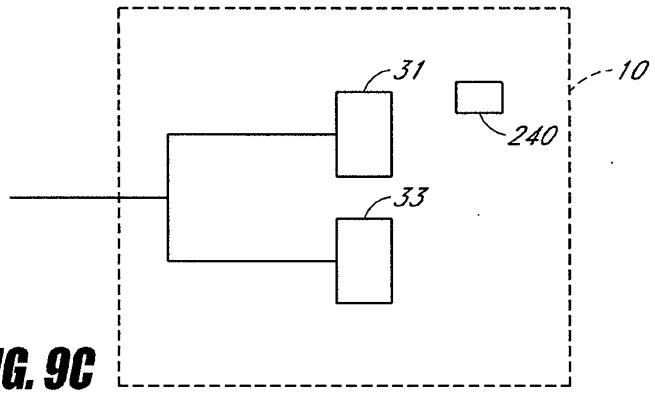


FIG. 9C

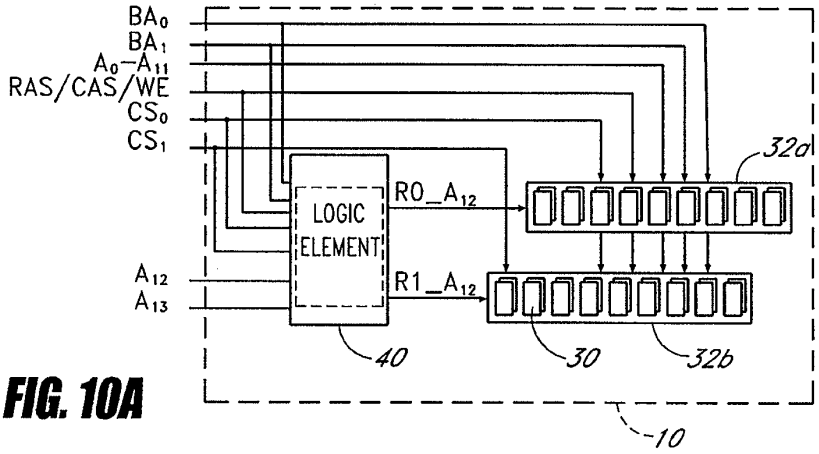


FIG. 10A

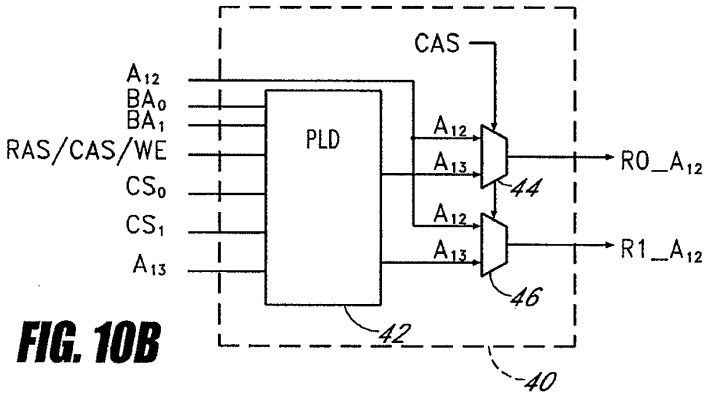


FIG. 10B

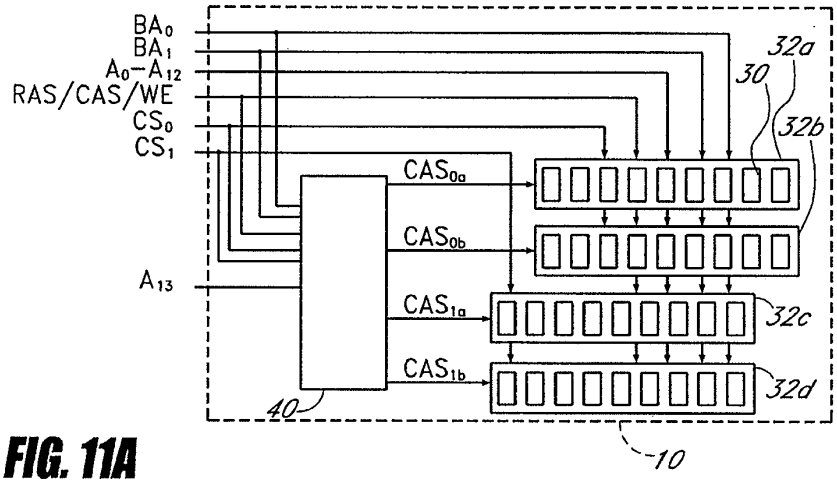


FIG. 11A

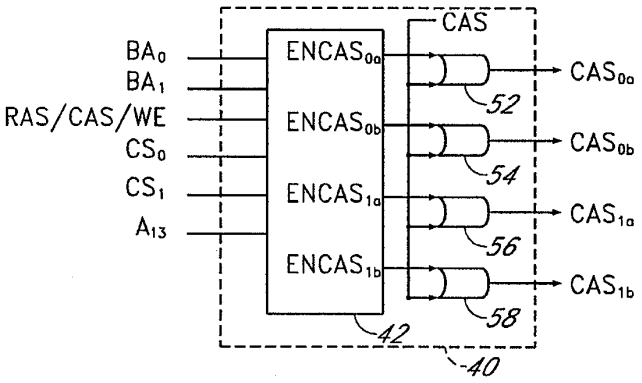


FIG. 11B

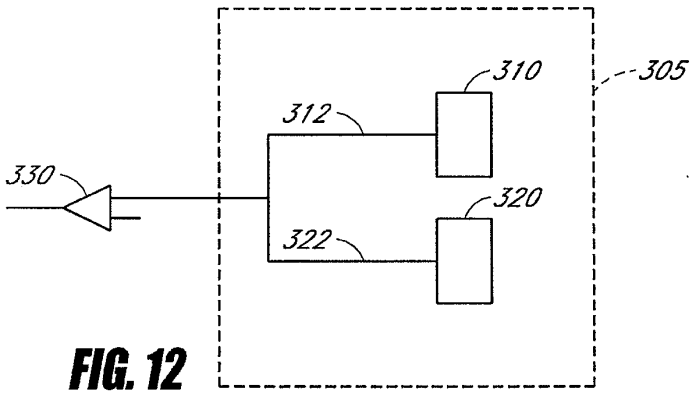


FIG. 12

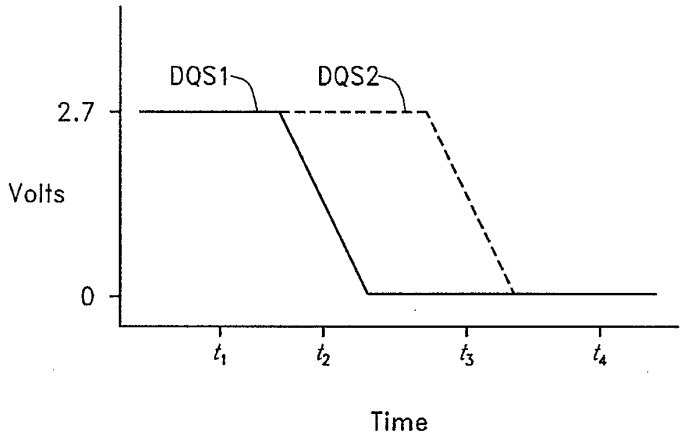


FIG. 13

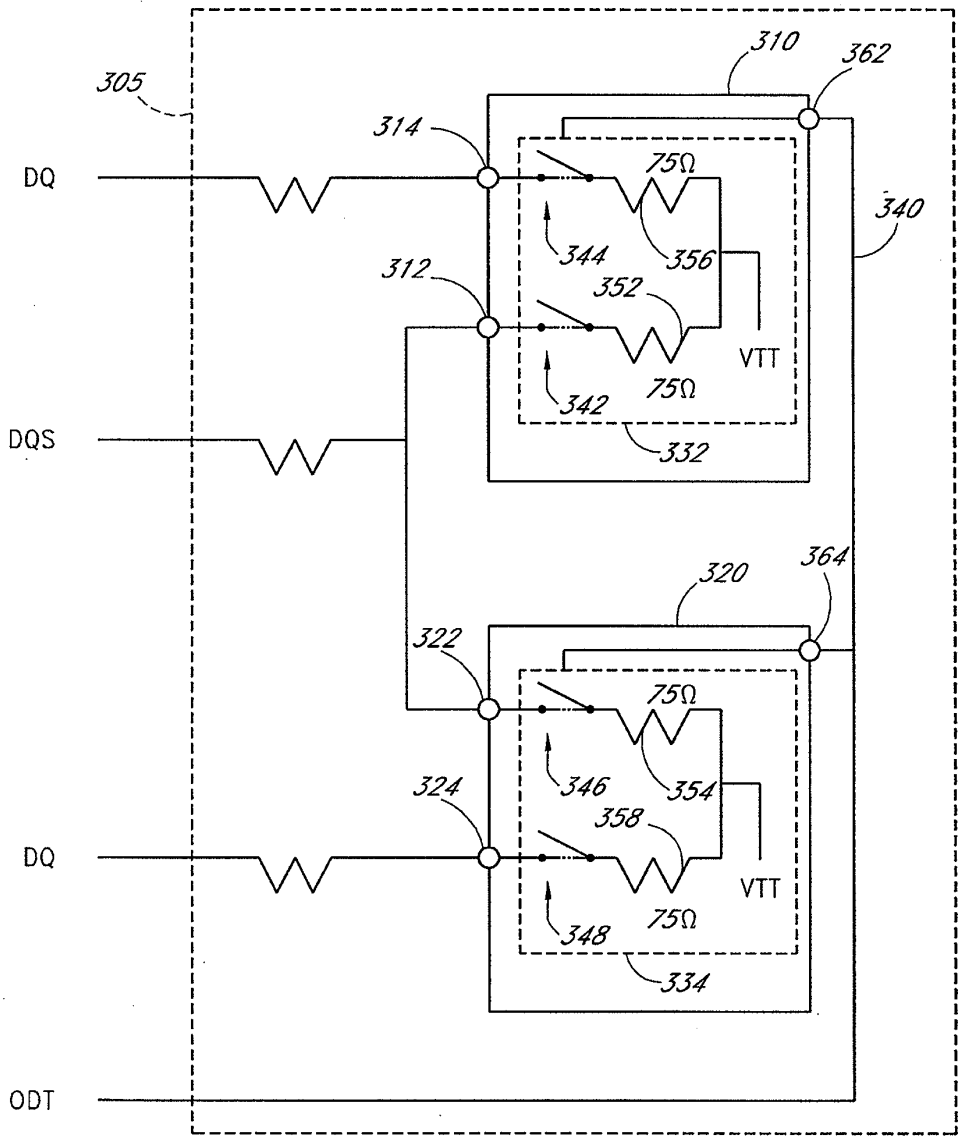

305
310
362
314
75Ω
340
DQ
344
356
312
352
VTT
75Ω
342
DQS
332
320
364
322
75Ω
346
354
324
358
DQ
VTT
75Ω
348
334
ODT

FIG. 14

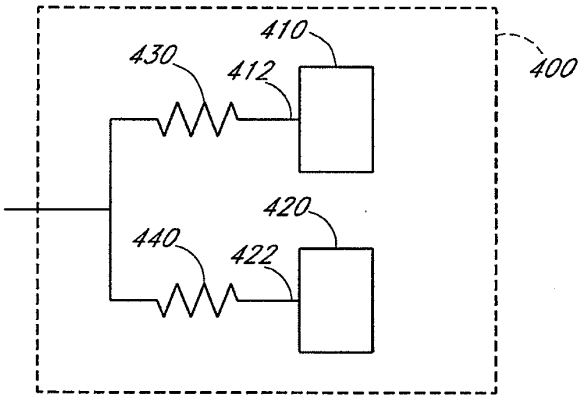


FIG. 15

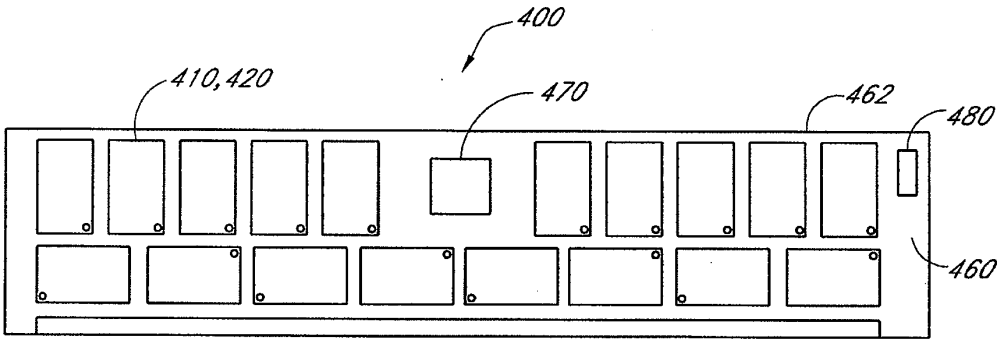


FIG. 16A

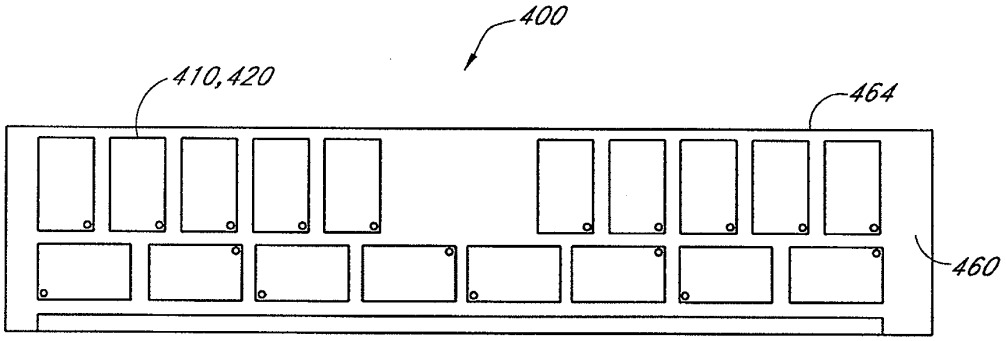


FIG. 16B

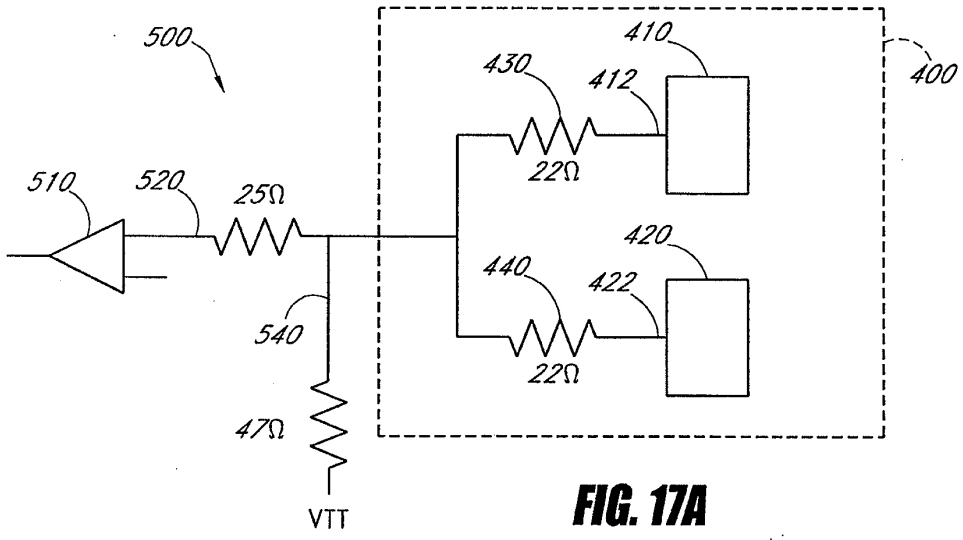


FIG. 17A

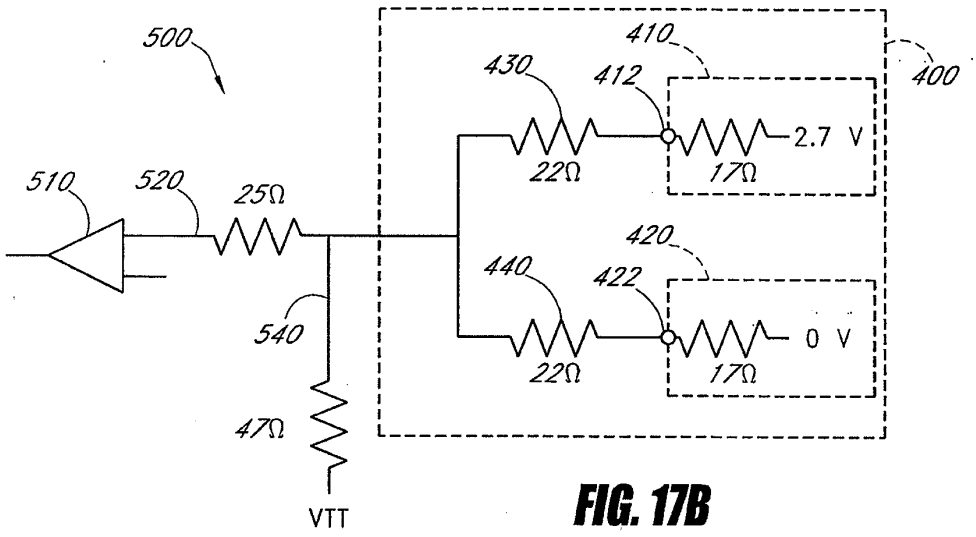


FIG. 17B

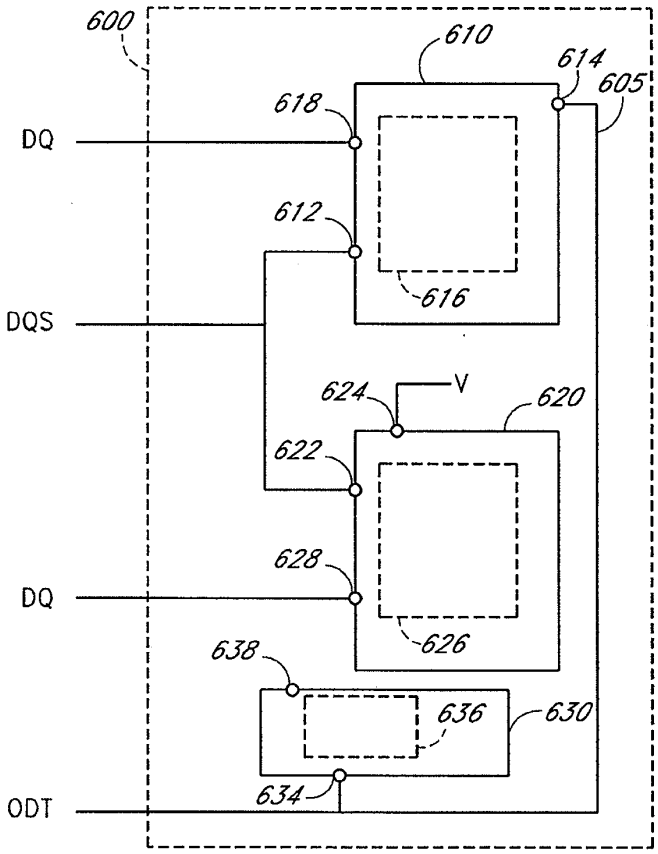

600
610
614
605
618
DQ
612
616
DQS
624
V
620
622
628
DQ
626
638
636
630
634
ODT

FIG. 18

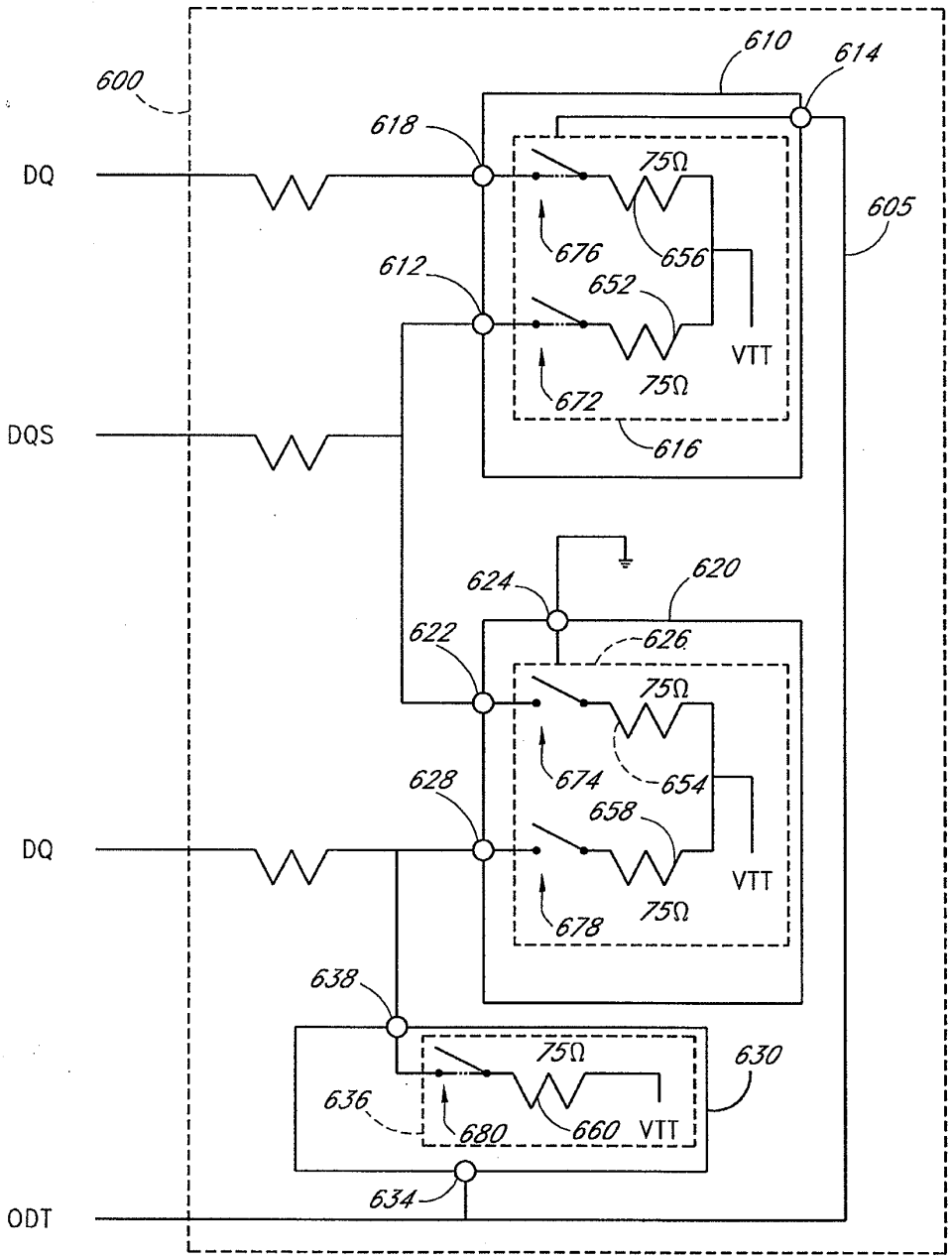

600
610
614
618
DQ
75Ω
605
676
656
612
652
VTT
672
75Ω
DQS
616
624
620
622
626
75Ω
674
654
628
658
DQ
VTT
678
75Ω
638
75Ω
630
636
680
660
VTT
634
ODT

FIG. 19

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NETL.018P2C8

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility filing Fee (Electronic filing)	4011	1	70	70
Utility Search Fee	2111	1	300	300
Utility Examination Fee	2311	1	360	360
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**730**

Electronic Acknowledgement Receipt

EFS ID:	22381411
Application Number:	14715486
International Application Number:	
Confirmation Number:	1537
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C8
Receipt Date:	18-MAY-2015
Filing Date:	
Time Stamp:	21:05:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$730
RAM confirmation Number	8011
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	2015-05-18_ApplicationDataSheet_NETL018P2C8.pdf	1170846 7fe852adbde3d210f3f42825eb5ba2afd088179a	no	7
Warnings:					
Information:					
2		2015-05-18_Spec_NETL018P2C8.pdf	1009846 52fe20d792e0dbc35b82b0e5cbc506cc4fbb97e2	yes	59

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	52
Claims	53	58
Abstract	59	59

Warnings:					
Information:					
3	Drawings-only black and white line drawings	2015-05-18_Drawings_NETL018P2C8.pdf	542321 871777f34297efea8a1a3205cdd202c2cc239937	no	23
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	35098 05114155a767f475759b6856fd852f2c2c0497cd	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2758111		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/715,486	05/18/2015	Jeffrey C. Solomon	NETL.018P2C8

CONFIRMATION NO. 1537

79141
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

FORMALITIES LETTER

OC000000075447158

Date Mailed: 06/01/2015

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing.

Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- Additional claim fees of $ **40** as a small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. Small entity discount is in effect. If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **70** surcharge.
- $ **40** for **1** total claims over 20.
- $(**0**) previous unapplied payment amount.
- $ **110** TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's

oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Jeffrey C. Solomon
  Jayesh R. Bhakta

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/jmilani/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/715,486	05/18/2015	2139	730	NETL.018P2C8	21	3

CONFIRMATION NO. 1537

79141
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

FILING RECEIPT

OC000000075447157

Date Mailed: 06/01/2015

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Inventor(s)

Jeffrey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 13/971,231 08/20/2013 PAT 9037774
which is a CON of 13/287,081 11/01/2011 PAT 8516188
which is a CON of 13/032,470 02/22/2011 PAT 8081536
which is a CON of 12/955,711 11/29/2010 PAT 7916574
which is a CON of 12/629,827 12/02/2009 PAT 7881150
which is a CON of 12/408,652 03/20/2009 PAT 7636274
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7289386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7286436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004
and claims benefit of 60/590,038 07/21/2004

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.

Petitioners
Ex. 1057, p. 97

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 05/27/2015

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/715,486**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

**** SMALL ENTITY ****

Title

MEMORY MODULE WITH DATA BUFFERING

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

Petitioners
Ex. 1057, p. 100

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/715,486

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	300		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	21 minus 20 =	* 1	x 40 =	40	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*	x 210 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	770		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

Electronic Patent Application Fee Transmittal

Application Number:	14715486
Filing Date:	18-May-2015
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NETL.018P2C8

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Claims in excess of 20	2202	1	40	40
Miscellaneous-Filing:				
Late Filing Fee for Oath or Declaration	2051	1	70	70
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**110**

Electronic Acknowledgement Receipt

EFS ID:	23090677
Application Number:	14715486
International Application Number:	
Confirmation Number:	1537
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C8
Receipt Date:	03-AUG-2015
Filing Date:	18-MAY-2015
Time Stamp:	02:22:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$110
RAM confirmation Number	7970
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Fee Worksheet (SB06)	fee-info.pdf	31958 c54d3107a58431769c1645d1426b12c22b443705	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	31958

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
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National Stage of an International Application under 35 U.S.C. 371
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New International Application Filed with the USPTO as a Receiving Office
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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/715,486	05/18/2015	2139	840	NETL.018P2C8	21	3

CONFIRMATION NO. 1537

UPDATED FILING RECEIPT

79141
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

OC000000077993911

Date Mailed: 10/13/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jeffrey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 13/971,231 08/20/2013 PAT 9037774
which is a CON of 13/287,081 11/01/2011 PAT 8516188
which is a CON of 13/032,470 02/22/2011 PAT 8081536
which is a CON of 12/955,711 11/29/2010 PAT 7916574
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which is a CON of 12/408,652 03/20/2009 PAT 7636274
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7289386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7286436
which claims benefit of 60/550,668 03/05/2004
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and claims benefit of 60/590,038 07/21/2004

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 05/27/2015

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/715,486**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

**** SMALL ENTITY ****

Title

MEMORY MODULE WITH DATA BUFFERING

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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Petitioners
Ex. 1057, p. 109

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/715,486	05/18/2015	Jeffrey C. Solomon	NETL.018P2C8

CONFIRMATION NO. 1537

79141
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

INFORMAL NOTICE

OC000000077993912

Date Mailed: 10/13/2015

INFORMATIONAL NOTICE TO APPLICANT

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Jeffrey C. Solomon
  Jayesh R. Bhakta

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/yteferra/

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/715,486

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	300		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	21 minus 20 =	* 1	x 40 =	40	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*	x 210 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	770		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	2

Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number / Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1.	Patent Trial and Appeal Board Decision on Request for Rehearing for Reexamination Control No. 95/001,381, mailed August 13, 2014, 7 pages.	
	2.	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control Nos. 95/000,546 and 95/000,577, mailed February 25,2015, 25 pages.	
	3.	Patent Trial and Appeal Board Decision on Request for Rehearing for Reexamination Control Nos. 95/000,546 and 95/000,577, mailed August 27, 2015, 5 pages.	
	4.	Examiner's Determination after Board Decision on Appeal for Reexamination Control No. 95/001,337, mailed September 11, 2015, 16 pages.	
	5.	Inter Partes Review Case No. IPR2015-01020, Petition for Inter Partes Review of U.S. Patent No. 7,881,150, filed on April 7, 2015.	
	6.	Inter Partes Review Case No. IPR2014-01020, Exhibit 1002 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on April 7, 2015.	
	7.	Inter Partes Review Case No. IPR2014-01020, Exhibit 1023 to Petition for Inter Partes Review, curriculum vitae of Dr. Srinivasan Jagannathan, filed on April 7, 2015.	
	8.	Inter Partes Review Case No. IPR2014-01020, Exhibit 1025 to Petition for Inter Partes Review, "operational," *The Pocket Oxford American Dictionary of Current English,* Oxford University Press, 2002, filed on April 7, 2015.	
	9.	Inter Partes Review Case No. IPR2014-01020, Decision to Institute Inter Partes Review of D U.S. Patent No. 7,881,150, dated October 8, 2015.	
	10.	Inter Partes Review Case No. IPR2015-01 021, Petition for Inter Partes Review of U.S. Patent No. 8,081,536, filed on April 7, 2015	
	11.	Inter Partes Review Case No. IPR2014-01 021, Corrected Exhibit 1002 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on April 22, 2015.	
	12.	Inter Partes Review Case No. IPR2014-01 021, Exhibit 1026 to Petition for Inter Partes Review, curriculum vitae of Dr. Srinivasan Jagannathan, filed on April 7, 2015.	
	13.	Inter Partes Review Case No. IPR2014-01 021, Decision to Institute Inter Partes Review of U.S. Patent No. 8,081,536, dated October 8, 2015	
	14.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.,* Corrected Joint Claim Construction and Prehearing Statement Pursuant to Patent L.R. 4-3, including Exhibit A, filed August 27,2014, 28 pages.	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	2	of	2

Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	15.	U.S. Court of Appeals for the Federal Circuit, Decision on Appeal for Reexamination Control No. 95/001,381, filed November 13, 2015, 14 pages	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

Electronic Acknowledgement Receipt

EFS ID:	24261000
Application Number:	14715486
International Application Number:	
Confirmation Number:	1537
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C8
Receipt Date:	04-DEC-2015
Filing Date:	18-MAY-2015
Time Stamp:	02:44:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	2015-12-03_IDS_Cover_NETL018P2C7.pdf	58913 b17c93eefd6bea9d611a9790f467bb7048a67031	no	2
Warnings:					
Information:					

2	Information Disclosure Statement (IDS) Form (SB08)	2015-12-03_IDS_NETL018P2C8.pdf	122241 fb38354d60e010adbcf626e4fa1aafa865f93e91	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Non Patent Literature	2015-08-13_Board_Decision_95001381.pdf	238050 7a7cb3b0d5f936c617ada76fedfcd93f805d5495	no	7
Warnings:					
Information:					
4	Non Patent Literature	2015-02-25_Board_Decision_95000546.pdf	1010173 b5b4059d097c591e1dd310567852cf2422b8594f	no	25
Warnings:					
Information:					
5	Non Patent Literature	2015-08-27_Board_Decision_95000546.pdf	126624 d8c8732f1fde30cc1382e5966112c49d0f127d2f	no	5
Warnings:					
Information:					
6	Non Patent Literature	2015-09-11_Examiner_Determination_95001337.pdf	488400 afeca947a08dd84d0336e0499b7633114077de52	no	16
Warnings:					
Information:					
7	Non Patent Literature	2015-10-08_Petition_IPR2015-01020.pdf	2621086 4d019c5391e0a87b96971f5a35206230b4df7677	no	66
Warnings:					
Information:					
8	Non Patent Literature	2015-10-08_Exhibit-1020_IPR2015-01020.pdf	10238684 c228d565ad4e88237929466cf1c70ffeafacfeaf	no	222
Warnings:					
Information:					
9	Non Patent Literature	2015-10-08_Exhibit-1023_IPR2015-01020.pdf	172578 5c76283ee872b7d8b1a3c999679d569f8c47df85	no	3
Warnings:					
Information:					
10	Non Patent Literature	2015-10-08_Exhibit-1025_IPR2015-01020.pdf	1387589 c30c63b0791e252ce1bd9ea345f486626e459a73	no	4

Warnings:					
Information:					
11	Non Patent Literature	2015-10-08_Institution_Decision_IPR2015-01020.pdf	805786 4300cce3f82da42f9fac98a201b08a31a757ab80	no	19
Warnings:					
Information:					
12	Non Patent Literature	2015-04-07_Petition_IPR2015-01021.pdf	2550553 3f96133154a25a707d06a740b2671764a4f5453b	no	64
Warnings:					
Information:					
13	Non Patent Literature	2015-04-07_CV_Jagannathan_IPR2015-01021.pdf	172882 dc200f30d7417b3e4db1ae1bbc59afaaaa3d2aed	no	3
Warnings:					
Information:					
14	Non Patent Literature	2015-10-08_Institution_Decision_IPR2015-01021.pdf	842769 14f9922d13453f23ce20b2988dd22cfa5cde344b	no	19
Warnings:					
Information:					
15	Non Patent Literature	2015-04-07_Corrected_Exh_1002_IPR2015-01021.pdf	8687841 8a5683b6e8db0de1fc0ffb2eda3b4237b270b684	no	189
Warnings:					
Information:					
16	Non Patent Literature	2014-08-27_Corrected_Joint_Claim_Constr_CV05889.pdf	1704793 cdca7726114aba661d7f3c2ad8b0b15df7d3f0fb	no	28
Warnings:					
Information:					
17	Non Patent Literature	2015-11-13_Court_Appeal_Decision_95001337.pdf	594470 6cf6a49434a07601aa5528831883d1315d464b48	no	14
Warnings:					
Information:					
		Total Files Size (in bytes):	31823432		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
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New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT

Applicant	:	Netlist, Inc.
App. No.	:	14/715,486
Filed	:	May 18, 2015
For	:	MEMORY MODULE WITH DATA BUFFERING
Examiner	:	UNKNOWN
Art Unit	:	2139
Conf No.	:	1537

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 15 references. Copies of foreign documents and/or their translation and non-patent literature are submitted herewith.

The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

This Information Disclosure Statement is being filed before the receipt of a first Office Action on the merits, and presumably no fee is required. If a first Office Action on the merits

was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 50-5963.

Respectfully submitted,

Dated: December 3, 2015

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 521-4828

PTO/SB/08a/b(07-09)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	17

Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	4218740	08-19-1980	MOTOROLA INC	
	2.	4249253	02-03-1981	Gentili et al.	
	3.	4368515	01-11-1983	Nielsen	
	4.	4392212	07-05-1983	Miyasaka et al.	
	5.	4571676	02-18-1986	Mantellina et al.	
	6.	4592011	05-27-1986	Mantellina et al.	
	7.	4633429	12-30-1986	Lewandowski et al.	
	8.	4670748	06-02-1987	Williams	
	9.	4706214	11-10-1987	Mitsubishi Denki Kabushiki Kaisha	
	10.	4866603	09-02-1989	Chiba	
	11.	4958322	09-18-1990	Kosugi et al.	
	12.	4961172	10-02-1990	Shubat et al.	
	13.	4961204	10-02-1990	Hitachi Ltd	
	14.	4980850	12-25-1990	Morgan	
	15.	5060188	10-22-1991	Zulian et al.	
	16.	5247643	09-21-1993	Shottan	
	17.	5272664	12-21-1993	Silicon Graphics Inc	
	18.	5345412	09-06-1994	Shiratsuchi	
	19.	5357478	10-18-1994	Mitsubishi Electric Corp	
	20.	5388072	02-07-1995	IBM	
	21.	5392252	02-21-1995	Visi Technology Inc	
	22.	5426753	06-20-1995	Moon	
	23.	5463590	10-31-1995	Watanabe	
	24.	5483497	01-09-1996	Mochizuki et al.	
	25.	5485589	01-16-1996	Dell Usa Lp	
	26.	5495435	02-27-1996	Sugahara	
	27.	5513135	04-30-1996	Dell et al.	
	28.	5532954	07-02-1996	Bechtolsheim et al.	
	29.	5541448	07-30-1996	Carpenter	
	30.	5572691	11-05-1996	Koudmani	
	31.	5581498	12-03-1996	Ludwig et al.	
	32.	5590071	12-31-1996	Kolor et al.	
	33.	5602999	02-11-1997	Hyatt; Gilbert P.	

EXAMINER **DATE CONSIDERED**

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Attorney Docket Number	NETL.018P2C8

US PATENT DOCUMENTS

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known	
Application Number	14/715,486
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First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

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Sheet	4	of	17

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First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

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First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

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First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
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Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

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Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
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Application Number	14/715,486
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First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

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First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

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First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
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				Art Unit	2827
				Examiner Name	Unknown
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	338.	Google, Inc. v. Netlist, Inc., No. 4:08-cv-04144-SBA, Netlist Inc.'s Answer to Complaint and Counterclaim (N.D. Ca. Filed Nov. 18, 2008).	
	339.	Google, Inc. v. Netlist, Inc., No. C 08-04144 SBA Google Inc.'s Invalidity Contentions Pursuant to PAT. L.F. 3-3, dated Apr. 13, 2009.	
	340.	Google, Inc. v. Netlist, Inc., No. C08 04144, Complaint for Declaratory Relief, (N.D. Ca Dated Aug. 29, 2008).	
	341.	Google, Inc. v. Netlist, Inc., No.4:08-cv-04144-SBA, Google Inc.'s Invalidity Contentions Pursuant to Pat. L.F. 3-3, dated 13 April 2009.	
	342.	International Preliminary Report on Patentability for International Application No. PCT/US2010/040826, date of mailing November 28, 2011 (NETL.048VPC) in 34 pages.	
	343.	International Search Report and Written Opinion for Related Application No. PCT/US2010/040826, mailed on September 27, 2010, in 15 pages.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	15	of	17

Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	344.	JEDEC Standard No. 21-C, 4.20.6-200 Pin. PC2700/PC2100/PC1600 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification, Revision 1.1, Release 11b, Apr. 26, 2002.	
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	354.	Netlist, Inc. v. MetaRam, Inc., No. 09-165-GMS, MetaRAM, Inc.'s Answer and Affirmative Defenses to Plaintiff's Complaint, dated Apr. 20, 2009.	
	355.	Netlist, Inc. v. MetaRAM, Inc., No. 1:09-ccv-00165-GMS, Complaint for Patent Infringement, (D. Del. Filed Mar. 12, 2009).	
	356.	Non-Final Action Closing Prosecution mailed September 1, 2010, for Control No. 95/001,339, filed April 10, 2010, 17 pages.	
	357.	Non-Final Action Closing Prosecution mailed June 21, 2011, for Control No. 95/001,381, filed June 9, 2010, 34 pages.	
	358.	Non-Final Action Closing Prosecution mailed March 12, 2012, for Control No. 95/001,337, filed April 19, 2010, 33 pages.	
	359.	Non-Final Action mailed August 27, 2010, for Control No. 95/000,546, filed May 11, 2010, 16 pages.	
	360.	Non-Final Action mailed September 8, 2010, for Control No. 95/001,381, filed June 9, 2010, 17 pages.	
	361.	Non-Final Action mailed April 4, 2011, for Control No. 95/001,339, filed April 20, 2010, 61 pages. (merged with 95/000,578 and 95/000,579)	
	362.	Non-Final Action mailed June 15, 2011, for Control No. 95/001,381, filed June 9, 2010, 33 pages.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

Sheet 16 of 17

NON PATENT LITERATURE DOCUMENTS

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	363.	Non-Final Action mailed September 27, 2011, for Control No. 95/001,337, filed April 19, 2010, 19 pages.	
	364.	Non-Final Action mailed October 4, 2011, for Control No. 95/001,339, filed April 20, 2010, 77 pages. (merged with 95/000,578 and 95/000,579)	
	365.	Non-Final Action mailed October 14, 2011, for Control No. 95/001,339, filed April 30, 2010, 99 pages. (merged with 95/000,578 and 95/000,579)	
	366.	Non-Final Office Action mailed November 16, 2011, for Application No. 95/001,758 filed September 14, 2011, 25 pages.	
	367.	Order Granting Request for Inter Partes Reexamination mailed November 16, 2011, for Application No. 95/001,758, filed September 14, 2011, 13 pages.	
	368.	Order Granting Request for Inter Partes Reexamination mailed August 9, 2010, for Control No. 95/000,546, filed May 11, 2010, 22 pages.	
	369.	Order Granting Request for Inter Partes Reexamination mailed August 27, 2010, for Control No. 95/001,337, filed April 19, 2010, 21 pages.	
	370.	Order Granting Request for Inter Partes Reexamination mailed September 1, 2010, for Control No. 95/001,339, filed April 20, 2010, 14 pages.	
	371.	Order Granting Request for Inter Partes Reexamination mailed September 8, 2010, for Control No. 95/000,381, filed June 9, 2010, 21 pages.	
	372.	Order Granting Request for Inter Partes Reexamination mailed January 14, 2011, for Control No. 95/000,579, filed October 21, 2010, 12 pages.	
	373.	Order Granting Request for Inter Partes Reexamination mailed January 18, 2011, for Control No. 95/000,577, filed October 20, 2010, 17 pages.	
	374.	Order Granting Request for Inter Partes Reexamination mailed January 18, 2011, for Control No. 95/000,578, filed October 20, 2010, 14 pages.	
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Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

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	381.	US District Court Civil Docket; Google Inc. v. Netlist Inc.; 4:08cv04144; Date filed Aug. 29, 2008.	
	382.	US District Court Civil Docket; Netlist Inc. v. Inphi Corporation; 2:09cv6900; Date filed Sep. 22, 2009. cited by other.	
	383.	Written Opinion for International Application No. PCT/US2010/040826, date of mailing October 24, 2011 (NETL.048VPC) in 7 pages.	

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Electronic Acknowledgement Receipt

EFS ID:	24958599
Application Number:	14715486
International Application Number:	
Confirmation Number:	1537
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C8
Receipt Date:	18-FEB-2016
Filing Date:	18-MAY-2015
Time Stamp:	23:11:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	2016-02-18_IDS_Cover_NETL018P2C8.pdf	59062 d398eb44f4e909e2909664355e070c2b953cfc67	no	2
Warnings:					
Information:					

2	Information Disclosure Statement (IDS) Form (SB08)	2016-02-18_IDS1_NETL018P2C8.pdf	468621 58929eb95797e423bf5dc285725cc1aa60357f22	no	17

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National Stage of an International Application under 35 U.S.C. 371

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If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT

Applicant	:	Netlist, Inc.
App. No.	:	14/715,486
Filed	:	May 18, 2015
For	:	MEMORY MODULE WITH DATA BUFFERING
Examiner	:	UNKNOWN
Art Unit	:	2139
Conf No.	:	1537

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 383 references. Copies of foreign documents and/or their translation and non-patent literature are submitted in the parent application U.S. Pat. App. No. 13,287,042, filed November 1, 2011, now U.S. Patent No. 8,756,364, which are accessible via PAIR.

The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

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was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 50-5963.

Respectfully submitted,

Dated: February 18, 2016

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 521-4828

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

Sheet	1	of	1

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	20080025137	01-31-2008	Natarajan et al.	
	2	2006233012	10-19-2006	Tomonori et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Foreign Patent Document	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	3	EP 1 816 570 A2	08-08-2007	Rambus, Inc.		

NON PATENT LITERATURE DOCUMENTS

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	4	International Search Report and Written Opinion, PCT/US2011/059209, January 31, 2013	

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App. No.	:	14/715,486
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Examiner	:	UNKNOWN
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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 45 references. Copies of foreign documents and/or their translation and non-patent literature are submitted on April 7, 2014 in the parent application U.S. Pat. App. No. 13/971,231, filed August 20, 2013, now U.S. Patent No. 9,037,774, which are accessible via PAIR.

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First Named Inventor	Jayesh R. Bhakta
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	1	6717855	04-06-2004	Underwood	

FOREIGN PATENT DOCUMENTS

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	2	Action Closing Prosecution mailed October 1, 2012, for Control Nos. 95/000,546 and 95/000,577, filed May 11, '2010 and October 20, 2010 respectively, 39 pages.	
	3	Non-Final Office Action mailed November 13, 2012, for Control Nos. 95/001,339, 95/000,578 and 95/000,579, filed April 20, 2010, October 20, 2010 and October 21, 2010 respectively, 81 pages	
	4	Order Granting Request for Inter Partes Reexamination and Non-Final Office Action mailed December 7,2012, for Control No. 95/002,399, filed September 15, 2012, 89 pages.	
	5	Non-Final Office Action mailed December 19, 2012, for Control No. 95/001,758, filed September 14, 2011, 36 Pages.	
	6	Request for Inter Partes Reexamination; Reexam U.S. Patent Application No. 95/001,758, for U.S. Patent No. 7,864,627, filed September 15, 2011, 814 pages (submitted in four parts.)	
	7	Request for Inter Partes Reexamination; Reexam U.S. Patent Application No. 95/001,381, for U.S. Patent No. 7,532,537, filed June 9, 2010, 247 pages	

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Examiner	:	UNKNOWN
Art Unit	:	2139
Conf No.	:	1537

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Alexandria, VA 22313-1450

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	2

Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	5345412	09-06-1994	Shiratsuchi	
	2.	5537584	07-16-1996	Miyai et al.	
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	21.	7379361	05-27-2008	Co et al.	
	22.	20050010737	01-13-2005	Ware et al.	
	23.	20070293094	12-20-2007	Aekins, Robert A.	

NON PATENT LITERATURE DOCUMENTS

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	24.	Anonymous. (December 1996). "Applications Note: Understanding DRAM Operation," IBM, 10 pages.	
	25.	Behrens, S. "HP Printer Memory Explained", The ZonkPage, Last Updated 01-21-2004. Accessed 02-10-2013, Retrieved from the Internet: URL <http://warshaft.com/hpmem.htm>. 7pp.	
	26.	Non-Final Office Action, U.S. Pat. App. 13/412,243, January 2, 2014, 20 pages	
	27.	Non-Final Office Action, U.S. Pat. App. 12/761,179, September 13, 2012, 20 pages	
	28.	Non-final office action, U.S. Patent Application No. 13/288,850, October 14, 2013, 24 pages	
	29.	Non-final office action, U.S. Patent Application No. 13/411,344, December 31, 2013, 28 pages	

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				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2139
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	30.	Non-final office action, U.S. Patent Application No. 13/473,413, November 17, 2011, 46 pages	
	31.	Response to non-final office action dated September 13, 2012 for U.S. Patent Application No. 12/761,179, filed March 13, 2013, 16 pages	
	32.	Response to non-final office action dated October 14, 2013 for U.S. Patent Application No. 13/288,850, filed January 14, 2014, 15 pages	
	33.	Response to non-final office action dated 12/31/2013 for U.S. Patent Application No. 13/411,344, filed March 31, 2014, 12 pages	
	34.	Patent Owner's Response to Office Action mailed November 13, 2012 for Reexamination Control Nos.95/000,578; 95/000,579, and 95/001,339, filed January 14, 2013, 96 pages.	
	35.	Patent Owner's Response to Office Action mailed December 19, 2012 for Reexamination Control No. 95/001,758, filed March 19, 2013, 61 pages	
	36.	Patent Owner's Response to Office Action mailed September 26, 2013 for Reexamination Control No. 95/001,758, filed November 26, 2013, 85 pages	
	37.	Third Party Requester's Comments after Non-Final Action mailed September 26, 2013 for Reexamination Control No. 95/001,758, filed December 26, 2013,	
	38.	Reexamination Control No. 95/002,399, filed April 25, 2013, and its entire file history	
	39.	Patent Owner's Appeal Brief for Reexamination Control Nos. 95/000,546 and 95/000,577, filed October 2, 2013, 46 pages	
	40.	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control No.95/001/337, mailed January 16, 2014, 30 pages	
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INFORMATION DISCLOSURE STATEMENT

Applicant	:	Netlist, Inc.
App. No.	:	14/715,486
Filed	:	May 18, 2015
For	:	MEMORY MODULE WITH DATA BUFFERING
Examiner	:	UNKNOWN
Art Unit	:	2139
Conf No.	:	1537

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 5 references. Copies of foreign documents and/or their translation and non-patent literature are submitted on April 8, 2014 in the parent application U.S. Pat. App. No. 13/971,231, filed August 20, 2013, now U.S. Patent No. 9,037,774, which are accessible via PAIR.

The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

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Respectfully submitted,

Dated: February 18, 2016

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 521-4828

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Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

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	1.	6011710	01-04-2000	Wiggers	
	2.	20010008006	07-12-2001	Klein	
	3.	20050257109	11-17-2005	Averbuj	
	4.	20070070669	03-29-2007	Tsern	

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	5.	Petition for Inter Partes Review filed on 6/24/2014 for U.S. Patent No. 8,516,185, IPR Case Number IPR2014-01029, and all associated documents including cited references and expert declarations, available at https://ptabtrials.uspto.gov	
	6.	Petition for Inter Partes Review filed on 6/22/2014 for U.S. Patent No. 7,881,150, IPR Case Number IPR2014-00882 and IPR Case Number IPR2014-01011, and all associated documents including cited references and expert declarations, available at https://ptabtrials.uspto.gov	
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	8.	Altera, ACEX iK, Programmable Logic Device Family, Data Sheet, May 2003, Ver 3.4	
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	11.	JEDEC Standard No. 21-C Section 4.5.7, 168 Pin Registered SDRAM DIMM Family, Release 7	
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App. No.	:	14/715,486
Filed	:	May 18, 2015
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Examiner	:	UNKNOWN
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Conf No.	:	1537

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	1.	20060262586	11-23-2006	Solomon, et al	
	2.	20080162790	07-03-2008	Im, Jeon-Taek	
	3.	20090103387	04-23-2009	Shau, Jeng-Jye	

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	4.	JPH10092169 A	9/9/97	Toshiba Corp.		
	5.	JP2000311485 A	10/13/00	Fujitsu Ltd.		

NON PATENT LITERATURE DOCUMENTS

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	6.	Office Action mailed April 2, 2014, for Japanese Patent Application No. 2012-520662 and English translation thereof, 7 pages	

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First Named Inventor	Jayesh R. Bhakta
Art Unit	2189
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	NETL.018P2C7

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	1.	6747887	06-08-2004	Halbert et al.	
	2.	7093066	08-15-2006	Klein	
	3.	6832303	12/14/2004	Tanaka	

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	10.	McCluskey, Edward J., *Logic Design Principles with Emphasis on Testable Semicusto Circuits*, Prentice Hall, 1986, pp. 104-107 and 119-120.	
	11.	MICRON, DDR SDRAM DIMM Module: MT16VDDT3264A – 256 MB; MT16VDDT6464A – 512 MB, Data Sheet, 2002, Micron Technology, Inc.	
	12.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.,* Smart Storage Systems, Inc.'s Invalidity Contentions, dated June 6, 2014	
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Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 8 references. Copies of foreign documents and/or their translation and non-patent literature are submitted on January 12, 2015 in the parent application U.S. Pat. App. No. 13/971,231, filed August 20, 2013, now U.S. Patent No. 9,037,774, which are accessible via PAIR.

The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

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Respectfully submitted,

Dated: February 18, 2016

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 521-4828

PTO/SB/08a/b(07-09)
Approved for use through 7/31/2012. OMB 0651-0031
US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

Sheet 1 of 1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
	2.	Inter Partes Review of U.S. Patent No. 8,081,536, IPR Case No. IPR2014-00883, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
	3.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
	4.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3001 to Decision – Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued December 16, 2014	
	5.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3002 to Decision – Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued December 16, 2014	
	6.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3003 to Decision – Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued December 16, 2014	
	7.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3004 to Decision – Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued December 16, 2014	
	8.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014.	

EXAMINER **DATE CONSIDERED**

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INFORMATION DISCLOSURE STATEMENT

Applicant	:	Netlist, Inc.
App. No.	:	14/715,486
Filed	:	May 18, 2015
For	:	MEMORY MODULE WITH DATA BUFFERING
Examiner	:	UNKNOWN
Art Unit	:	2139
Conf No.	:	1537

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 54 references. Copies of foreign documents and/or their translation and non-patent literature are submitted on March 21, 2015 in the parent application U.S. Pat. App. No. 13/971,231, filed August 20, 2013, now U.S. Patent No. 9,037,774, which are accessible via PAIR.

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Application No.: 14/715,486
Filing Date: MAY 18, 2015

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Respectfully submitted,

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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	3

Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	5388240	02-01-1995	IBM Corporation	
	2.	5463590	10-31-1995	Watanabe	
	3.	5953280	09-14-1999	Matsui	
	4.	6188641	02-13-2001	Uchida	
	5.	6205516	03-20-2001	Usami	
	6.	6480439	11-12-2002	Tokutome et al.	
	7.	7464225	12-09-2008	Tsern	
	8.	7865674	01-04-2011	Gower et al.	
	9.	8089795	01-03-2012	Rajan	
	10.	8130560	03-06-2012	Rajan	
	11.	8189328	05-29-2012	Kanapathippillai	
	12.	8233303	07-31-2012	Best	
	13.	8250295	08-21-2012	Amidi et al.	
	14.	8417870	04-09-2013	Lee et al.	
	15.	8516185	08-20-2013	Lee et al.	
	16.	8516188	08-20-2013	Solomon et al.	
	17.	8756364	06-17-2014	Bhakta et al.	
	18.	20070058409	03-15-2007	Ruckerbauer	
	19.	20080104352	05-01-2008	Talbot	
	20.	20080104352	05-01-2008	Talbot	
	21.	RE36229	06-15-1999	Cady	

US PATENT APPLICATIONS

Examiner Initials *	Cite No. [1]	Application Number	Filing Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	22.	13/411,344	3/2/2012	Lee	Entire Prosecution History
	23.	13/970,606	8/20/2013	Netlist, Inc.	Entire Prosecution History
	24.	13/971,231	8/20/2013	Netlist, Inc.	Entire Prosecution History
	25.	14/229,844	3/29/2014	Netlist, Inc.	Entire Prosecution History
	26.	14/324,990	7/7/2014	Netlist, Inc.	Entire Prosecution History
	27.	14/337,168	7/21/2014	Netlist, Inc.	Entire Prosecution History

NON PATENT LITERATURE DOCUMENTS

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	14/715,486
				Filing Date	May 18, 2015
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2139
				Examiner Name	Unknown
Sheet	2	of	3	Attorney Docket Number	NETL.018P2C8

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	28.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
	29.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
	30.	Inter Partes Review of U.S. Patent No. 8,081,536, IPR Case No. IPR2014-00883, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
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	32.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
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	38.	McCluskey, Edward J., *Logic Design Principles with Emphasis on Testable Semicustom Circuits*, Prentice Hall, 1986, pp. 104-107 and 119-120.	
	39.	Inter Partes Review Case No. IPR2014-01029, Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on June 24, 2014.	
	40.	Inter Partes Review Case No. IPR2014-01029, Exhibit 1008 to Petition for Inter Partes Review, "Declaration of Charles J. Neuhauser, Ph.D. under 37 C.F.R. § 1.68," filed on June 24, 2014.	
	41.	Inter Partes Review Case No. IPR2014-01029, Supplemental Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on July 23, 2014.	
	42.	Inter Partes Review Case No. IPR2014-01029, Patent Owner's Preliminary Response pursuant to 37 C.F.R. § 42.107, filed on October 17, 2014.	
	43.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014.	
	44.	Inter Partes Review Case No. IPR2014-01029, Petitioner's Request for Rehearing pursuant to 37 C.F.R. § 42.71, filed on January 15, 2015.	

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				Application Number	14/715,486
				Filing Date	May 18, 2015
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2139
				Examiner Name	Unknown
Sheet	3	of	3	Attorney Docket Number	NETL.018P2C8

NON PATENT LITERATURE DOCUMENTS			
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	45.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Request for Rehearing, Issued on March 3, 2015.	
	46.	Inter Partes Review Case No. IPR2014-01369, Corrected Petition for Inter Partes Review of Claims 1-19 of U.S. Patent No. 8,516,185, filed on September 22, 2014.	
	47.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1008 to Corrected Petition for Inter Partes Review, "Declaration of Dr. Nader Bagherzadeh under 37 C.F.R. § 1.68," filed on September 22, 2014.	
	48.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1013 to Corrected Petition for Inter Partes Review, "Webster's II New College Dictionary," filed on September 22, 2014.	
	49.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1014 to Corrected Petition for Inter Partes Review, "Standard Dictionary of Electrical and Electronics Terms," IEEE 1988, filed on September 22, 2014.	
	50.	Inter Partes Review Case No. IPR2014-01369, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued March 9, 2014.	
	51.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Smart Storage Systems, Inc.'s Invalidity Contentions, dated June 6, 2014	
	52.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits E.1-E.7 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	53.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Diablo Technologies, Inc.'s Invalidity Contentions, dated June 6, 2014.	
	54.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits D-1 to D6 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.	

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Electronic Acknowledgement Receipt

EFS ID:	24958748
Application Number:	14715486
International Application Number:	
Confirmation Number:	1537
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C8
Receipt Date:	19-FEB-2016
Filing Date:	18-MAY-2015
Time Stamp:	01:09:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	2016-02-18_IDS2_Cover_NETL018P2C8.pdf	59222 9f7be5b866f8a4c679fec0473ae31c56fe3b0c5b	no	2
Warnings:					
Information:					

2	Information Disclosure Statement (IDS) Form (SB08)	2016-02-18_IDS2_NETL018P2C8.pdf	97272 cbba2c6b0c0ad4f40ec093c04cbcf60d5079dbe8	no	1
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3	Transmittal Letter	2016-02-18_IDS3_Cover_NETL018P2C8.pdf	59127 44d218d9a3991e9a9ef3ee0cd415753b7d1f619b	no	2
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Information:					
4	Information Disclosure Statement (IDS) Form (SB08)	2016-02-18_IDS3_NETL018P2C8.pdf	92691 b62ed1f04e10346aac2335927c7774f41b5f8238	no	1
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Information:					
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7	Transmittal Letter	2016-02-18_IDS5_Cover_NETL018P2C8.pdf	59119 bf3f433b5e838f803fd63247b058decd77171223	no	2
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8	Information Disclosure Statement (IDS) Form (SB08)	2016-02-18_IDS5_NETL018P2C8.pdf	92108 ee9e33a86bb6fa6ea2c77ce9de462e7025989aa0	no	1
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Information:					
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9	Transmittal Letter	2016-02-18_IDS6_Cover_NETL018P2C8.pdf	59153 5bb6bd6acdb8ff11c28da2d026f374c1e39f3b93	no	2
Warnings:					
Information:					

10	Information Disclosure Statement (IDS) Form (SB08)	2016-02-18_IDS6_NETL018P2C8.pdf	98976 c353ac7985f891cfd19d2b4fad579600a19ff66e	no	1
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This is not an USPTO supplied IDS fillable form					
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Information:					
16	Information Disclosure Statement (IDS) Form (SB08)	2016-02-18_IDS9_NETL018P2C8.pdf	92275 dc5fe37ae094617bd841eec4ee162de93c0ee790	no	1
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This is not an USPTO supplied IDS fillable form					
17	Transmittal Letter	2016-02-18_IDS10_Cover_NETL018P2C8.pdf	59285 81c4447c539499bd56ac536722af1ad31f422047	no	2
Warnings:					
Information:					

18	Information Disclosure Statement (IDS) Form (SB08)	2016-02-18_IDS10_NETL018P2C8.pdf	153098 c355c6293740e06e7a21431736a8d8a4f06984c2	no	3

Warnings:

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Total Files Size (in bytes):	1507153

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT

Applicant	:	Netlist, Inc.
App. No.	:	14/715,486
Filed	:	May 18, 2015
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Examiner	:	UNKNOWN
Art Unit	:	2139
Conf No.	:	1537

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P.O. Box 1450
Alexandria, VA 22313-1450

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Respectfully submitted,

Dated: February 18, 2016

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
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PTO/SB/08a/b(07-09)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

Sheet	1	of	1

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	2003/0070052	04-2003	Lai, Jiin	
	2	2004/0098528	05-2004	Janzen, Jefferey W.	
	3	2002/0048195	04-2002	Klein, Dean A.	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	4	Non-Final Office Action, dated January 2, 2014, for U.S. Pat. App. No. 13/287,042 filed November 1, 2011, 42 pages	
	5	Response to Non-Final Office Action dated January 2, 2014 for U.S. Pat. App. No. 13/287,042, filed April 2, 2014, 12 pages	

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INFORMATION DISCLOSURE STATEMENT

Applicant	:	Netlist, Inc.
App. No.	:	14/715,486
Filed	:	May 18, 2015
For	:	MEMORY MODULE WITH DATA BUFFERING
Examiner	:	UNKNOWN
Art Unit	:	2139
Conf No.	:	1537

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing13 references. Copies of foreign documents and/or their translation and non-patent literature are submitted on August 7, 2014 in the parent application U.S. Pat. App. No. 13/971,231, filed August 20, 2013, now U.S. Patent No. 9,037,774, which are accessible via PAIR.

The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

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Respectfully submitted,

Dated: February 18, 2016

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 521-4828

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Sheet	1	of	3

Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
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Attorney Docket Number	NETL.018P2C8

US PATENT DOCUMENTS

Examiner Initials *	Cite No.[1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	6381140	04-30-2002	Liao, Sheng-Chi	
	2.	7254036	08-07-2007	Pauley et al.	

FOREIGN PATENT DOCUMENTS

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	3.	WO99/30240	06-17-1999	Intel Corporation		

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	4.	Inter Partes Review Case No. 2014-00882, Patent Owner Response, filed May 8, 2015	
	5.	Inter Partes Review Case No. 2014-00882, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015	
	6.	Inter Partes Review Case No. 2014-00882, Petitioner's Request for Oral Argument, filed July 1, 2015	
	7.	Inter Partes Review Case No. 2014-00882, Patent Owner's Request for Oral Argument, filed July 3, 2015	
	8.	Inter Partes Review Case No. 2014-00882, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015	
	9.	Inter Partes Review Case No. 2014-00882, Record of Oral Hearing, filed November 16, 2015	
	10.	Inter Partes Review Case No. 2014-00882, Final Written Decision 35 USC 318 and 37 CFR 42.73, filed December 14, 2015	
	11.	Inter Partes Review Case No. 2014-00882, Netlist Inc.'s Notice of Appeal, filed February 10, 2016	
	12.	Inter Partes Review Case No. 2014-00882, Exhibit 1022, 'Professor Carl Sechen Deposition Transcript,' filed June,19,2015	
	13.	Inter Partes Review Case No. 2014-00882, Exhibit 1023, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015	
	14.	Inter Partes Review Case No. 2014-00882, Exhibit 2002, 'Declaration of Professor Carl Sechen,' filed May 8,2015	
	15.	Inter Partes Review Case No. 2014-00882, Exhibit 2003, 'Transcript of Videotaped Deposition of Srinivasan Jagannathan, Ph. D,' filed May 8,2015	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	14/715,486
				Filing Date	May 18, 2015
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2139
				Examiner Name	Unknown
Sheet	2	of	3	Attorney Docket Number	NETL.018P2C8

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	16.	Microsoft Computer Dictionary, Fifth Edition, Microsoft Press, p. 334, 2002	
	17.	Jacob, Bruce, et al. "Memory Systems - Cache, DRAM, Disk," Elsevier Inc. 2008, Chapters 7 and 10	
	18.	U.S. District Court Northern District of California, Case No. 4.13-cn-05889-YGR, Netlist Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Joint Claim Construction and Prehearing Statement Pursuant to Patent L. T. 4-3, filed August 27, 2014, in 28 pages	
	19.	Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 349-411	
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	21.	Selected Entries in Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/view/Entry/175039?redirectedFrom=selectively#eid	
	22.	Web search results from the Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/search?searchType=dictionary&q=select&_searchBin=Search	
	23.	Inter Partes Review Case No. 2014-00883, Patent Owner Response, filed May 8, 2015	
	24.	Inter Partes Review Case No. 2014-00883, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015	
	25.	Inter Partes Review Case No. 2014-00883, Petitioner's Request for Oral Argument, filed July 1, 2015	
	26.	Inter Partes Review Case No. 2014-00883, Patent Owner's Request for Oral Hearing, filed July 3, 2015	
	27.	Inter Partes Review Case No. 2014-00883, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015	
	28.	Inter Partes Review Case No. 2014-00883, Record of Oral Hearing, filed November 16, 2015	
	29.	Inter Partes Review Case No. 2014-00883, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015	
	30.	Inter Partes Review Case No. 2014-00883, Netlist Inc.'s Notice of Appeal, filed February 10, 2016	
	31.	Inter Partes Review Case No. 2014-00883, Exhibit 1025, 'Professor Carl Sechen Deposition Transcript,' filed June 19,2015	
	32.	Inter Partes Review Case No. 2014-00883, Exhibit 1026, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015	
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	35.	Inter Partes Review Case No. 2014-01011, Petitioner's Request for Oral Argument, filed July 1, 2015	

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				Filing Date	May 18, 2015
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2139
				Examiner Name	Unknown
Sheet	3	of	3	Attorney Docket Number	NETL.018P2C8

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	36.	Inter Partes Review Case No. 2014-01011, Patent Owner's Request for Oral Hearing, filed July 3, 2015	
	37.	Inter Partes Review Case No. 2014-01011, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015	
	38.	Inter Partes Review Case No. 2014-01011, Record of Oral Hearing, filed November 16, 2015	
	39.	Inter Partes Review Case No. 2014-01011, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015	
	40.	Inter Partes Review Case No. 2014-01011, Netlist Inc.'s Notice of Appeal, filed February 10, 2016	
	41.	Inter Partes Review Case No. 2014-01011, Exhibit 1027, 'Professor Carl Sechen Deposition Transcript,' filed June 19,2015	
	42.	Inter Partes Review Case No. 2014-01011, Exhibit 1028, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015	

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(71) Applicant *(for all designated States except US)*: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

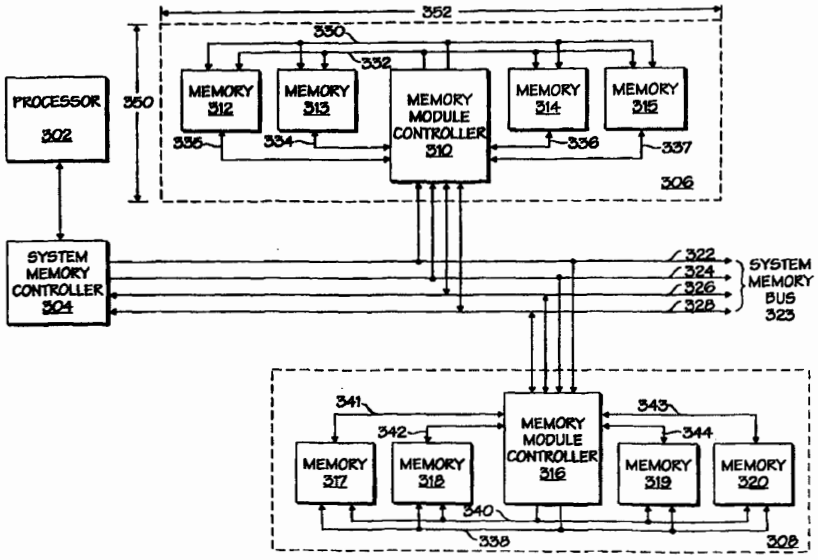
(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: HOLMAN, Thomas, J. [US/US]; 3045 N.W. Bauer Woods Drive, Portland, OR 97229 (US).

(74) Agents: TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

(81) Designated States: AL, AM, AT, AT (Utility model), AU (Petty patent), AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

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(54) Title: MEMORY SYSTEM INCLUDING A MEMORY MODULE HAVING A MEMORY MODULE CONTROLLER



(57) Abstract

A system (300) that has a system memory controller (304) and memory module (306, 308). The memory modules (306, 308) include memory module controller (310, 316) coupled to the system memory controller (304) and a plurality of memory devices (312–315, 317–320) coupled to the memory module controllers (310, 316).

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MEMORY SYSTEM INCLUDING A MEMORY MODULE HAVING A MEMORY MODULE CONTROLLER

RELATED APPLICATIONS

This application is related to and claims the benefit of the filing dates of the following United States Provisional Patent Applications: (1) Provisional Application No. _____, entitled DISTRIBUTED CONTROL MEMORY BUS ARCHITECTURE, filed on December 5, 1997; and (2) Provisional Application No._____, entitled DISTRIBUTED CONTROL MEMORY BUS ARCHITECTURE, filed on December 5, 1997. These applications are assigned to the same assignee as the present application.

This application is also related to U.S. Patent Application No. _____, entitled MEMORY MODULE INCLUDING A MEMORY MODULE CONTROLLER filed on February 13, 1998, and U.S. Patent Application No. _____, entitled MEMORY MODULE CONTROLLER filed on February 13, 1998, each of which is assigned to the assignee of the present application.

FIELD OF THE INVENTION

The present invention pertains to the field of memory systems. More particularly, the present invention relates to a memory system that includes a memory controller on a memory module.

BACKGROUND

Memory modules such as single in-line memory modules (SIMMs) and dual in-line memory modules (DIMMs) are typically used to store data, instructions, and other information in computers or other digital systems. Figure 1 shows a typical memory system in which processor 102 communicates with dynamic random access memory (DRAM) devices 110-117 on memory modules 106 and 108, respectively, via memory controller 104. Memory controller 104 communicates appropriate memory instructions (e.g., write, read, refresh, etc.) to memory module 106 via address and command bus 118, and to memory module 108 via address and command bus 120. Data is transferred from memory controller 104 to both modules via bus 122.

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There are at least two disadvantages associated with the conventional memory system of Figure 1: (1) buses 118, 120, and 122 are multi-drop buses that have high capacitive loads which require large drivers in memory controller 104 and in DRAMs 110-117 (to drive bus 122); and (2) there tends to be large mismatches in loading between the address and command buses and data bus 122. These disadvantages combine to reduce the maximum operating frequency, increase power consumption, and decrease performance of the system. Additionally, memory controller 104 may include a high number of pins (e.g., approximately 190 pins for a 4 DIMM SDRAM system) to support access to memory modules 106 and 108. The bus width of data bus 122 is often 64 or 72 bits wide to support larger bandwidths, for example, of up to 100 mega transmissions per second (MT/s).

Figure 2 shows another typical memory system that uses technology from Rambus, Inc. of Mountain View, California. In this system, processor 202 communicates with Rambus dynamic random access memory (RDRAM™) devices 210-217 on memory modules 206 and 208 (also called Rambus in-line memory modules or RIMM™ modules), respectively, via memory controller 204. Memory controller 204 communicates appropriate memory instructions (e.g., write, read, refresh, etc.) and data in a time-multiplexed fashion to memory modules 206 and 208 via memory specific bus 226. Each of the RDRAM™ devices 210-217 include interface logic 218-225, respectively, that enables the RDRAM™ devices to interface to memory specific bus 226. Memory specific bus 226 may operate at a high frequency (e.g., 250 to 400 MHz), have a small bus width (e.g., 16 or 18 signal lines), have symmetric loading for address, command, and data information, and have a bandwidth of up to 800 MT/s. In other embodiments, the address and control information may be separated (demultiplexed) from the data bus in this environment.

The system of Figure 2 has a number of disadvantages. Each RDRAM™ device includes a significant amount of logic in the interface logic which makes implementation of the RDRAM™ devices more

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difficult and more expensive than other DRAM devices, and which causes the RDRAM™ devices to draw more power and dissipate more heat than if the logic was not present. This may lead to thermal and reliability problems. Additionally, each RDRAM™ typically includes a delay locked loop (DLL) circuit coupled to a plurality of clock signals on bus 226. The DLL circuits are typically always functioning and drawing significant amounts of power which contributes to thermal and reliability issues. Additionally, memory controller 204 must include relatively large drivers to drive bus 226

In each of the memory systems described in Figures 1 and 2, the memory controller must be designed to provide the appropriate memory transactions to the memory devices in a predetermined format and at predetermined times. The memory devices and memory controller must then be designed to work together. It would be advantageous to decouple the design of the memory devices and the memory controller such that independent advances may be made in each technology. It would also be desirable to decouple the operation of the memory devices from the memory controller to decrease power drawn by each memory device and by the entire memory system.

Other features and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description that follows.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention are illustrated by way of example and not limitation in the figures of the accompanying drawings in which like references indicate similar elements and in which:

Figure 1 is a block diagram of one embodiment of a conventional memory system;

Figure 2 is a block diagram of another embodiment of a conventional memory system;

Figure 3 is a block diagram of one embodiment of a memory system according to the present invention;

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Figure 4 is a block diagram of another embodiment of a memory system according to the present invention;

Figure 5 is a block diagram of one embodiment of a dynamic random access memory (DRAM) module including a DRAM memory module controller;

Figure 6 is a block diagram of one embodiment of a static random access memory (SRAM) module including an SRAM memory module controller;

Figure 7 is a block diagram of one embodiment of nonvolatile memory module including a nonvolatile memory module controller;

Figure 8 is a block diagram of one embodiment of the memory module controller of Figure 3 coupled to a time multiplexed system memory bus;

Figure 9 is a flow chart of one embodiment of the process implemented by the memory module controller of Figure 8;

Figure 10 is a block diagram of one embodiment of the memory module controller of Figure 3 coupled to a demultiplexed system memory bus;

Figure 11 is a flow chart of one embodiment of the process implemented by the memory module controller of Figure 10;

Figure 12 is a block diagram of one embodiment of a memory module including a memory module controller interfacing SDRAM devices with a system memory bus using a Direct Rambus™ protocol;

Figure 13 is a flow chart of one embodiment of a read transaction implemented by the memory module controller of Figure 12;

Figure 14 is an exemplary timing diagram of the read transaction implemented by the memory module controller of Figure 12;

Figure 15 is a flow chart of one embodiment of a write transaction implemented by the memory module controller of Figure 12;

Figure 16 is an exemplary timing diagram of the write transaction implemented by the memory module controller of Figure 12;

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Figure 17 is an exemplary timing diagram of a read transaction implemented by the memory module controller of Figure 12 using a modified protocol; and

Figure 18 is an exemplary timing diagram of a write transaction implemented by the memory module controller of Figure 12 using a modified protocol.

SUMMARY OF THE INVENTION

One embodiment of the present invention includes a system that has a system memory controller and a memory module. The memory module includes a memory module controller coupled to the system memory controller and a plurality of memory devices coupled to the memory module controller.

Other objects, features, and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description that follows.

DETAILED DESCRIPTION

A memory system including distributed control of memory devices on memory modules is described. The present invention includes a memory module controller device on each memory module in the system. The memory module controller communicates with the system memory controller over a system memory bus and with the individual memory devices at the module level. The system memory bus may be a low pin count, high frequency, multiplexed or demultiplexed bus. The memory module controller may communicate with the individual memory devices over wider, lower frequency, demultiplexed signals lines. As the system memory controller communicates directly with only the memory module controllers, the loading on the system memory bus may be reduced and the size of the bus drivers in the system memory controller may also be reduced.

The memory module controller on each memory module is the interface between the system memory controller and the individual memory devices on the modules. This architecture decouples the

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individual memory devices from the system memory bus and the system memory controller. This may allow for the independent development of the memory device technology. For example, the memory devices may be developed to be faster, wider, to operate at different operating supply voltages, or to operate with reduced voltage swings than if the memory devices where directly communicating with the system memory controller.

The memory module may have its own memory address lines, control lines, and data lines between the memory module controller and the individual memory devices. The signal lines for these point-to-point or bus connections may be significantly shorter than the system interconnection buses used in conventional memory systems. This may allow for reduced loading, better control of capacitance on the address and data lines, and may increase the maximum operating frequency of the module while reducing power drawn by the system. Additionally, power may be further reduced by omitting DLLs from the individual memory devices. A DLL may be included within the memory module controller if required for interfacing with the system memory bus.

Figure 3 is a block diagram of one embodiment of the present invention. System 300 includes processor 302, system memory controller 304, and memory modules 306 and 308. Processor 302 communicates with system memory controller 304. Processor 302 may be any control logic or microprocessor that communicates write, read, and other memory transactions to system memory controller 304. System memory controller 304 communicates the memory transactions to memory module controllers 310 and 316 of memory modules 306 and 308, respectively, via system memory bus 323. System memory controller 304 may be part of a chip set for a personal computer, for example, or it may be other independent logic.

Memory modules 306 and 308 may be SIMMs, DIMMs, RIMM™ modules, or any other type of memory modules. Each memory module includes a memory module controller and one or more memory devices. For example, memory module 306 includes memory module controller 310 and memory devices 312-315, and memory module 308 includes memory

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module controller 316 and memory devices 317-320. The memory module controllers may be separate integrated circuits from the memory devices. While system 300 is illustrated as including two memory modules, any number of memory modules may be used. The memory devices may be placed on one side of the module, on both sides of the module, and/or they may be stacked on top of each other. The module may also be a multi-chip module. For one embodiment, a memory module may have an approximate height 350 of from 1 to 2 inches, and an approximate length 352 of from 4 to 6 inches.

Memory modules 310 and 316 communicate memory transactions with system memory controller 304 via system memory bus 323. System memory bus 323 may be a low pin count (e.g., approximately 16 to 35 address, data and control signal lines) bus operating at a high frequency. For one embodiment, system memory bus 323 may operate at a frequency of approximately 200 to 500 MHz. Other frequencies may be used. System memory bus 323 includes a command/address bus 324 and a data bus 328. Command/address bus 324 may time-multiplex commands and address information on one or more of the signal lines. The command and address bus 324 may also be split into separate command and address buses as in SDRAMs. System memory bus 323 may optionally include clock bus 322 that may carry one or more clock signals on the same or separate signal lines, and handshaking bus 326 that may carry a handshaking signal between system memory controller 304 and memory module controllers 310 and 316. The handshaking signal may be generated by system memory controller 304, for example, at the start of a memory request packet or when it is transmitting valid data on data bus 328. The handshaking signal may be generated by memory module controllers 310 and 316 when they are providing valid data requested by system memory controller 304 to data bus 328.

For one embodiment, system memory bus 323 may be compatible with the Direct Rambus™ bus architecture that includes 16 or 18 data bits on bus 328, one or more clock signals on bus 322, and command and address

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information on bus 324. The clock signals for this embodiment may run at rates of approximately 400 MHz enabling a data transmission rate of up to 800 MT/s. For this embodiment, system memory controller 304 may be any controller that may be able to implement the Direct Rambus™ protocol for memory transactions on system memory bus 323. Additionally, system memory bus 323 may use Rambus Signaling Levels (RSL) for the signals transferred on the bus. For alternative embodiments, any other type of appropriate signaling levels may be used including TTL, CMOS, GTL, SSTL, CTT or other signaling levels.

For another embodiment, system bus 323 may be one general purpose bus that carries time-multiplexed address, data, and control information. For example, system bus 323 may be compatible with Concurrent and Base Rambus™ architectures. For these embodiments, system memory controller 304 may be any controller that may be able to implement these protocols for memory transactions on system memory bus 323.

System memory bus 323 may by physically placed on a printed circuit board (PCB) that includes system memory controller 304 and interconnection slots for modules 306 and 308 as shown in Figure 3. Alternatively, system memory bus 323 may be routed through separate channels of memory modules 306 and 308 such as channels 402, 404, 406, and 408 as shown in Figure 4.

Memory module controllers 310 and 316 operate as bridges between system memory bus 323, that operates in one protocol or format, and local or memory module buses (e.g., lines 330, 332, and 334-337) that operate in a second different protocol or format. Each memory module includes control logic necessary to interpret the memory transaction on system memory bus 323 and translate that transaction into the appropriate control, address, and data signals for its memory devices on the memory module. Similarly, the memory modules interpret the memory transactions on the local or memory module bus into the format required to transmit the transaction to the system memory controller 304 via system memory bus 323.

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Memory module controllers 310 and 316 may also include circuitry necessary to perform refresh operations of dynamic memory devices, prefetch operations, error correction functions that may use, for example, ECC bits, current calibration if system memory bus 323 is a current bus, serial presence detect circuitry, a DLL circuit, power management circuitry that may shut off the clock signals or clock enable signals for the memory devices or provide other power down circuits, program and erasing voltages for nonvolatile memory circuits, and/or levelizing circuitry to generate signals on system memory bus 323 in the appropriate clock domains (if there is more than one clock domain on system memory bus 323).

Each memory device on the memory modules communicates memory transactions with its memory module controller via address, data, and control signals. Memory transactions are those transactions that are appropriate for each type of memory device used. For example, the memory transactions may include write, read, refresh, prefetch, power down, reset, erase, and the like. Memory module 306, for example, may communicate memory addresses to memory devices 312-315 via signal lines 330, control information (e.g., chip enable signals, write enable signals, RAS, CAS, output enable signals, etc.) via signal lines 332, and data via point-to-point connections 334-337. Each of the signal lines 330, 332, and 334-337 may be one or more signal lines. Signal lines 330 and 332 may be buses that connect to all four memory devices 312-315, to groups of memory devices (e.g., two at a time), or they may be point-to-point connections to memory module controller 310. Similarly, memory module 308 may communicate memory addresses to memory devices 317-320 via signal lines 338, control information via signal lines 340, and data via point-to-point connections 341-344. Each of the signal lines 338, 340, and 341-344 may be one or more signal lines.

For one embodiment, the number of signal lines 334-337 may be the same as the number of signal line carrying data for system memory bus 323. For another embodiment, the number of signal lines 334-337 may be collectively greater than the number of signal lines carrying data from

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system memory controller 304 to memory module controller 310 on system memory bus 323. This may increase the bandwidth of the data transfer on the memory module. For example, system memory bus 323 may carry 16 data signals in parallel on bus 328 and memory module controller 310 may simultaneously provide 16 data signals to each of memory devices 312-315. Because the data bus width may be wider (e.g., 64 or 72 bits wide) than that of system memory bus 323 (e.g., 16 bits wide), memory module controller 310 may supply a clock signal on bus 330 to memory devices 312-315 that is a lower frequency than that running on system memory bus 323. For one embodiment, the clock frequency on bus 330 may be approximately 50 to 200 MHz, for example, when the frequency of the clock signal on clock bus 322 is approximately 100 to 400 MHz. The frequency of the clock signal on clock bus 322 may also be double-pumped, that is, perform an action (e.g., load data) on each clock edge.

By having local address, control, and data lines on the memory modules which are decoupled from system bus 323, the length of these signals may be reduced over those on the system memory bus, the loading of these lines may be reduced over that of the system memory, and the loading may be more accurately controlled between the different lines so as to more closely achieve symmetric loading between the signals lines. For example, the loading on the data lines and the address and control lines may have approximately the same loading (e.g., approximately 10 to 40 pF) plus or minus approximately 10 percent. This may advantageously decrease the amount of power drawn by the module and increase the maximum operating frequency of the module for a given memory transaction.

Additionally, by decoupling the memory devices from system memory bus 323 and system memory controller 304, memory device 312-315 and 317-320 may operate from reduced or different power supply voltages than those provided to the balance of system 300. For example, memory devices 312-315 and 317-320 (and/or memory module controllers 310 and 316) may operate from power supplies of approximately 1.8 volts to 2.5 volts while the balance of the components in system 300 may operate at 3.3 volts

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or 5.0 volts. This may also operate to decrease the amount of power drawn by the module and thus by system 300. Additionally, the voltage swing of the signals on lines 330, 332, and 334-337 may be advantageously chosen to be small (e.g., approximately 1.0 to 2.0 volts) to further reduce power drawn by memory devices 312-315.

Power may be further reduced for each memory device and for the system as a whole when a DLL is required to interface with system memory bus 323. The DLL may be included within memory module controller 310 rather than each of memory devices 312-315 as my have been required in conventional systems.

For another embodiment, address lines 330, control lines 332, and/or data lines 334-337 may be combined into a time-multiplexed bus coupled between memory devices 312-215 and memory module controller 310.

The memory devices 312-315 and 317-320 may be any type of volatile or nonvolatile memory devices such as DRAMs, synchronous DRAMs (SDRAMs), Fast Page Mode DRAMs (FPM DRAMs), extended data out DRAMs (EDO DRAMs), Rambus DRAMs (RDRAM™ devices), synchronous or asynchronous static random access memory (SRAM) devices, read only memory (ROM) devices, programmable ROM (PROM) devices, erasable PROMs (EPROMs), electrically erasable PROMs (EEPROMs), flash memory devices, and the like. Each memory module may include different types of memory devices. For example, memory module 306 may include SDRAMs and memory module 308 may include EDO DRAMs, or memory module 306 may include nonvolatile memory devices and memory module 308 may include volatile memory devices.

Figure 5 is a block diagram of memory module 500 that is one embodiment of memory module 306 configured as a DRAM memory module. Module 500 includes DRAM memory module controller 510 that provides an interface between DRAM devices 512-515 and system memory bus 323. DRAM memory module controller 510 translates memory transactions received from system memory bus 323 and generates DRAM memory operations (e.g. write, read, prefetch, refresh) including addresses

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on address bus 516, data signals on data lines 523-526, and control signals such as write enable WE on line 518, RAS on line 520, and CAS on line 522. DRAM memory module controller 510 may also provide additional control signals to DRAMs 512-515 including clock signals for synchronous operation (i.e., for SDRAMs), memory bank select signals, and/or chip select or chip enable signals. DRAM memory module controller may also generate refresh commands, prefetch commands, and/or power management commands to DRAMs 512-515.

Figure 6 is a block diagram of memory module 600 that is one embodiment of memory module 306 configured as an SRAM memory module. Module 600 includes SRAM memory module controller 610 that provides an interface between SRAM devices 612-615 and system memory bus 323. SRAM memory module controller 610 translates memory transactions received from system memory bus 323 and generates SRAM memory operations (e.g., write, read, reset, power down) including addresses on address bus 616, data signals on data lines 623-626, and control signals such as chip select or chip enable CE on line 618, write enable WE on line 620, and output enable on line 622. SRAM memory module controller 610 may also provide additional control signals to SRAMs 612-615 including clock signals for synchronous operation, burst control signals, interrupt signals, reset signals, write and read signals (e.g., for a first-in-first-out FIFO device), power management signals, byte enable signals, and/or expansion signals.

Figure 7 is a block diagram of memory module 700 that is one embodiment of memory module 307 configured as an nonvolatile memory module. Module 700 includes nonvolatile memory module controller 710 that provides an interface between nonvolatile devices 712-715 and system memory bus 323. Nonvolatile memory module controller 710 translates memory transactions received from system memory bus 323 and generates nonvolatile memory operations (e.g., write or program, read, reset, power down, erase, etc.) including addresses on address bus 716, data signals on data lines 723-726, and control signals such as chip select or chip enable CE

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on line 718, write enable WE on line 720, output enable on line 722, and a programming voltage on line 728. Nonvolatile memory module controller 710 may also provide additional control signals to nonvolatile memory devices 712-715 including clock signals for synchronous operation, burst control signals, reset signals, power management signals, or other signals or commands.

With reference again to Figure 3, system memory controller 304 and memory module controllers 310 and 316 may communicate using any number of protocols as previously mentioned. In general, these protocols may be multiplexed such that some or all of the address, control, and data information is sent over the same bus lines of system memory bus 323. Alternatively, the protocols may be demultiplexed as shown in Figure 3 with the data transmitted over a separate data bus from address and control information. Whether the protocol is multiplexed or demultiplexed, the protocol may also be coupled or decoupled. That is, the protocol may be coupled if the system memory controller sends its memory transactions to system memory bus 323 at a first point in time and expects the requested data (in the case of a read transaction) or an acknowledgment signal at a second point in time (i.e., a timed response). The protocol may be decoupled by using a handshaking or valid signal to indicate the start of a memory transaction or to indicate when valid data is transmitted to system memory bus 323 by system memory controller 304 of memory module controllers 310 or 316.

Figure 8 is a block diagram of memory module controller 800 that is one embodiment of memory module controller 310 using a time multiplexed protocol. One embodiment of a time multiplexed protocol may be the Base and Concurrent Rambus™ protocols. Other protocols may be also be used. It will also be appreciated that memory module controller 800 is only one embodiment of a memory module controller. Other embodiments may also be used without departing from the spirit and scope of the present invention.

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Memory module controller 800 interfaces between system memory bus 823 that includes one or more clock signal lines 824, a transaction bus 826, and may optionally include a valid signal 828. The transaction bus 826 is a general purpose bus that may carry address, data, and control information for a memory transaction. Valid signal 828 is one or more handshaking signals that may be used for a decoupled protocol to indicate the start of a memory transaction or to indicate when valid data is present on transaction bus 826. Valid signal 828 may be monitored and generated by handshake logic 806 under the control of control logic 802. Valid signal 828 may be omitted for a coupled protocol. Memory module controller 800 also interfaces with memory devices on a memory module (as in Figure 3) by providing a clock signal 830, address signals 832, control signals 823, and data signals 836. Clock signal 830 may be omitted for asynchronous memory devices.

Memory module controller 800 includes request handling logic 804 for interfacing with transaction bus 826. Request handling logic 804 may include deserializing logic that may separate the multiplexed control, address, and data information provided on transaction bus 826 and provide these signals to control logic 802 via lines 838, 840, and 842, respectively. Request handling logic 804 may also include serializing logic that may serialize control, address, and data information on lines 838, 840, and 842, respectively, into a time-multiplexed series of signals to be provided to transaction bus 826.

Control logic 802 is the intelligence of memory module controller 800, and generates the appropriate control, address, and data signals for the memory module memory devices in response to the signals received from request handling logic 804. Each memory module controller device in each module may have different control logic that may be implement a specific translation between the signal types and protocol on the system memory bus and the specific memory signals and protocol expected by the memory devices on the memory module. For example, control logic 802 may provide the appropriate address signals to address interface circuit 818 via

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lines 844, the appropriate control signals to control interface circuit 820 via lines 846, and the appropriate data signals to data I/O circuitry 822 via lines 848. The interface circuits may include buffers and register elements to drive address 832, memory control signals 834, and data 836.

Interface circuits 818, 820, and 822 may be clocked by a clock signal generated by clock generator 810. Clock generator 810 may also provide a clock signal to control logic 802 and to clock buffers 816 which may drive clock signal 830 and/or clock enable signals to memory devices on a memory module. Clock generator 810 may generate clock signals in response to clock 824 provided from system memory bus 823. CLK 830 may be a different frequency than clock 824. Memory module controller 800 or clock generator 810 may further include a DLL, clock buffer, or clock divider circuit that shapes or alters clock 824 before it reaches clock generator 810.

Memory module controller 800 may also include a power manager unit 808 that, under the control of control logic 802, may enable or disable clock generator 810. This may, in turn, enable or disable clock 830 or a clock enable signal provided to the memory devices on a memory module so as to control power dissipated by the memory devices.

Memory module controller 800 may further include refresh logic 814 and prefetch logic 812. Under the control of control logic 802, refresh logic 814 may send refresh control signals to memory devices on a memory module via control interface circuit 820. Control logic 802 may generate the refresh command at an appropriate time, or it may generate a refresh command in response to a refresh command sent over transaction bus 826 from system memory controller 304. Prefetch logic 812 may, under the control of control logic 802, prefetch a page of data from memory devices (e.g., DRAM devices) and store the prefetched data for use in memory read transactions.

Memory module controller 800 may further include serial presence detect circuitry, ECC circuitry, current calibration circuitry, and other circuitry that may be removed from either the system memory controller or from the memory devices to reduce the complexity of the designs of these

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parts. This may reduce the number of pins on the system memory controller.

Figure 9 shows a flow chart that illustrates one embodiment of the operation of memory module controller 800 for write and read transactions. The process may be a pipelined process or implemented a single stage process. It will be appreciated that memory module controller 800 may perform many more functions besides translating write and read transactions between a system memory controller and memory devices on a memory module.

The process starts at step 902. At step 904, memory module controller 800 receives a memory transaction request on transaction bus 826. Data handling logic 804 deserializes the transaction at step 906 to obtain the address, control, and data information of the transaction. At step 908, control logic 802 inspects the deserialized information and determines if the transaction is directed to a memory device of the module controlled by memory module controller 800. This may be accomplished by inspecting the memory address received to see if it corresponds to an address occupied by one of the memory devices in the memory module. If the transaction is not directed to a memory device controlled by memory module controller 800, the process returns to step 902. If the transaction is directed to a memory device controlled by memory module controller 800, control logic 802 determines what type of transaction is requested at step 910. If the transaction is a write transaction, control logic 802 generates the appropriate write control signals (e.g., WE, CS, etc.) at step 912 and provides these signals to control interface circuit 820. At step 914, control logic 802 then provides the write data in the appropriate data format to data I/O circuitry 822 and the address of the selected memory device to address interface circuit 818. The write data may be buffered in a write buffer (not shown). The data may then be written into the desired memory location of the selected memory device. At step 916, an optional acknowledge signal may be sent back to the system memory controller after the write operation is completed. The process then returns to step 902.

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If the transaction is a read transaction, , control logic 802 then provides the read address of the selected memory device to address interface circuit. At step 920 control logic 802 generates the appropriate read control signals (e.g., WE, CS, OE, etc.) and provides these signals to control interface circuit 820. The data may then be read from the desired memory location of the selected memory device. The read data may be buffered in a read buffer (not shown), stored in control logic 802, or registered. At step 922, the read data may be provided to request handling logic 804 where it is serialized and may be framed by other data including, for example, a request number indicating this particular read transaction. At step 924, the read data may then be sent back to the system memory controller when system memory bus 823 is free or when all other previous transactions have been completed. For one embodiment, handshake logic 806 or other logic (e.g., request handling logic 804, control logic 802, or other bus monitoring logic) may monitor the activity on system memory bus 823 and indicate to control logic 802 when it is the turn of memory module controller 800 to send its read data to the system memory controller on bus system memory bus 823. The read data may be sent back with valid signal 828 in a decoupled system. The process then returns to step 902.

Figure 10 is a block diagram of memory module controller 1000 that is one embodiment of memory module controller 310 using a demultiplexed protocol. One embodiment of a de multiplexed protocol may be Direct Rambus™ protocol. Other protocols may be also be used. It will also be appreciated that memory module controller 1000 is only one embodiment of a memory module controller. Other embodiments may also be used without departing from the spirit and scope of the present invention.

Memory module controller 1000 interfaces between system memory bus 1023 that includes one or more clock signal lines 1024, a command and address bus CMD/ADDR 1026, data bus 1027, and may optionally include a valid signal 1028. CMD/ADDR bus 1026 may carry both address and control information for a memory transaction. Alternatively, CMD/ADDR bus

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1026 may be separated into separate command and address buses. Valid signal 1028 is a handshaking signal that may be used for a decoupled protocol to indicate the start of a memory transaction or to indicate when valid data is present on transaction bus 1026. Valid signal may be monitored and generated by handshake logic 1006 under the control of control logic 1002. Valid signal 1028 may be omitted for a coupled protocol. Memory module controller 1000 also interfaces with memory devices on a memory module (as in Figure 3) by providing a clock signal 1030, address signals 1032, control signals 1023, and data signals 1036. Clock signal 1030 may be omitted for asynchronous memory devices.

Memory module controller 1000 includes request handling logic 1004 for interfacing with transaction bus 1026. Request handling logic 1004 may include deserializing logic that may separate the multiplexed control and address information provided on CMD/ADDR bus 1026 and provide these signals to control logic 1002 via lines 1042 and 1044, respectively. Request handling logic 1004 may also include serializing logic that may serialize control and address information on lines 1042 and 144, respectively, into a series of signals to be provided to CMD/ADDR bus 1026.

Memory module controller 1000 further includes data handling logic 1046 that may receive data from data bus 1027, reformat the data into a format appropriate for the memory devices of the memory module and provide the reformatted data to write buffer 1012. For one embodiment, data handling logic 1046 may include deserializing or unpacking logic to perform the translation between, for example, a narrow (e.g., 16 bit) data bus 1027 and a wider (e.g., 64 bit) memory device data bus 1036. The data may be stored in write buffer 1012 until it needs to be provided to a memory device via data I/O circuitry 1022. A corresponding address for the write data may be stored in address storage unit 1014. For an alternative embodiment, write buffer 1012 may be omitted. Data handling logic 1046 may also receive data from the memory devices of a memory module via data I/O circuitry 1022 and/or read buffer 1038. Data handling logic may then reformat the data into a format expected by the protocol of system memory bus 1023. For

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one embodiment, data handling logic 1046 may include serializing or packing logic to perform the translation between, for example, a wider (e.g., 64 bit)) memory device data bus 1036 and a narrower (e.g., 16 bit) data bus 1027. For yet another embodiment, data handling logic may be omitted and the formatting of data may be performed by control logic 1002.

Control logic 1002 is the intelligence of memory module controller 1000, and provides the appropriate control, address, and data signals for the memory module memory devices in response to the signals received from request handling logic 1004. Each memory module controller device in each mode may have different control logic that may be implement a specific translation between the signal types and protocol on the system memory bus and the specific memory signals and protocol expected by the memory devices on the memory module. For example, control logic 1002 may provide the appropriate address signals to address interface circuit 1018 via lines 1048, the appropriate control signals to control interface circuit 1020 via lines 1050, and the appropriate data signals to data I/O circuitry 1022 by controlling write buffer 1012 via line 1052 and address storage 1014 via lines 1054. Control logic 1002 may also provide the appropriate control signal to read buffer 1038 to control when data read from a memory device on a memory module is provided to data handling logic 1046. The interface circuits may include buffers and register elements to drive address 1032, memory control signals 1034 and data 1036.

Interface circuits 1018, 1020, and 1022 may be clocked by a clock signal generated by clock generator 1010. Clock generator 1010 may also provide a clock signal to control logic 1002 and to clock buffers 1016 which may drive clock signal 1030 and/or clock enable signals to memory devices on a memory module. Clock generator 1010 may generate clock signals in response to a clock signal provided by DLL 1058. DLL 1058 may receive on or more clock signals 1024 provided from system memory bus 1023. CLK 1030 may be a different frequency than clock 1024.

Memory module controller 1000 may also include a power manager unit 1008 that, under the control of control logic 1002 may enable or disable

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the clock generator. This may, in turn, enable or disable clock 1030 or a clock enable signal provided to the memory devices on a memory module so as to control power dissipated by these memory devices.

Memory module controller 1000 may optionally include address storage unit 1040 coupled to control logic 1002, address interface circuit 1018, and optionally to clock generator 1010. Address storage 1040 may be used to store address information that may be provided from CMD/ADDR 1026.

Memory module controller 1000 may further include refresh and prefetch logic as illustrated in Figure 8 which operates under the control of control logic 1002. Memory module controller 1000 may further include serial presence detect circuitry, ECC circuitry, current calibration circuitry, and other circuitry that may be removed from either the system memory controller or from the memory devices to reduce the complexity of the designs of these parts. This may reduce the number of pins on the system memory controller.

Figure 11 shows a flow chart that illustrates one embodiment of the operation of memory module controller 1000 for write and read transactions. The process may be a pipelined process or implemented a single stage process. It will be appreciated that memory module controller 1000 may perform many more functions besides translating write and read transaction between a system memory controller and memory devices on a memory module.

The process starts at step 1102. At step 1104, memory module controller 1000 receives a memory transaction request on CMD/ADDR bus 1026. At step 1006, data handling logic 1004 unpacks or deserializes the command and address information and transmits this information to control logic 1002. At step 1106, control logic 1002 inspects the unpacked or deserialized information and determines if the transaction is directed to a memory device in the module controlled by memory module controller 1000. This may be accomplished by inspecting the memory address received to see if it corresponds to an address occupied by one of the memory devices in the memory module. If the transaction is not directed to a memory

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device controlled by memory module controller 1000, the process returns to step 1102. If the transaction is directed to a memory device controlled by memory module controller 1000, control logic 1002 determines what type of transaction is requested at step 1110. If the transaction is a write transaction, control logic 1002 generates the appropriate write control signals (e.g., WE, CS, etc.) at step 1112 and provides these signals to control interface circuit 1020. Request handling logic 1004 may also provide the write address to address storage 1014. Alternatively, control logic 1002 may provide the write address to address interface circuit 1018, for example, when write buffer 1012 is not used. At step 1114, data handling logic 1046 accepts write data from 1027, unpacks or deserializes the write data, and provide the write data to write buffer 1012. At step 1116, the write data is provided in the appropriate data format to data I/O circuitry 1022. The data may then be written into the desired memory location of the selected memory device. At step 1118, an optional acknowledge signal may be sent back to the system memory controller after the write operation is completed. The process then returns to step 1102.

If the transaction is a read transaction, control logic 1002 generates the appropriate read control signals (e.g., WE, CS, OE, etc.) at step 1120 and provides these signals to control interface circuit 1020. At step 1122, control logic 1002 then provides the read address of the selected memory device to address interface circuit 1018. The data may then be read from the desired memory location of the selected memory device. The read data may be buffered in read buffer 1038, stored in control logic 1002, or registered. At step 1124, the read data may be provided to data handling logic 1046 where it is serialized or packed and may be framed by other data including, for example, a request number indicating this particular read transaction. At step 1126, the read data may then be sent back to the system memory when the system memory bus is free or when all other previous transactions have been completed. For one embodiment, handshake logic 1006 or other logic (e.g., request handling logic 1004, data handling logic 1046, control logic 1002, or other bus monitoring logic) may monitor the activity on system memory

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bus 1023 and indicate to control logic 1002 when it is the turn of memory module controller 1000 to send its read data to the system memory controller on bus system memory bus 1023. Valid read data may be sent back with valid signal 1028 in a decoupled system. The process then returns to step 1102.

Figure 12 is a block diagram of memory module 1200 that is one embodiment of memory module 306 of Figure 3. Memory module 1200 is an SDRAM module that includes SDRAM devices 1204-1207 and memory module controller 1202. Memory module controller 1202 provides a bridge between system memory bus 1242 using a Direct Rambus™ protocol (and coupled to a system memory controller) and SDRAM devices 1204-1207. The Direct Rambus™ protocol includes clock signals CLK 1228, /CLK 1230 (where the symbol "/" indicates a complementary signal), data lines 1232, row address lines 1234, and column address lines 1236. The data may include 16 signals lines, the row address may include 3 signal lines, and the column address may include 5 signal lines as described in the Advance Information Direct RDRAM™ 64/72-Mbit (256Kx16/18x16d) data sheet. For one embodiment, CLK 1228 and /CLK 1230 may have a frequency of approximately 400 MHz. Other signals used by this protocol are not shown so as not to obscure the present invention.

Memory module controller 1202 provides memory transactions received from system memory bus 1242 to SDRAMs 1204-1207. For one embodiment, SDRAMs 1204-1207 may be 64Mb SDRAMs such as described in the preliminary data sheet of IBM's IBM0364804C, IBM 0364164C, IBM0364404C, and IBM03644B4C products published in November 1997. Other SDRAMs may also be used.

Memory module controller 1202 provides first control information to SDRAMs 1204 and 1205 over control bus 1238, and second control information to SDRAMs 1206 and 1207 over control bus 1240. Control bus 1238 may include a clock signal CLK 1208, a clock enable signal CKE 1209, a write enable signal WE 1210, a column address strobe signal CAS 1211, a row address strobe RAS 1212, and one or chip select signals CS 1213. Similarly,

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control bus 1240 may include a clock signal CLK 1216, a clock enable signal CKE 1217, a write enable signal WE 1218, a column address strobe signal CAS 1219, a row address strobe RAS 1220, and one or chip select signals CS 1221. For one embodiment, the frequency of the CLK 1208 and CLK 1216 may be approximately 100 MHz to 200 MHz. Other frequencies may be used. Memory module controller also communicates memory address signals SDRAMs 1204 and 1205 via address bus 1214, and to SDRAMs 1206 and 1207 via address bus 1222. For one embodiment, each address bus may include 12 address lines and an additional two bank select lines for selecting banks of memory in each SDRAM device. In an alternative embodiment, control bus 1238 and 1240 may be the same bus as shown in Figure 3. Similarly, address buses 1214 and 1222 may be the same bus. Memory module controller also communicates read and write data with SDRAMs 1204, 1205, 1206, and 1207 via signal lines 1224, 1225, 1226, and 1227, respectively. For one embodiment, each group of signal lines may include 16 data lines.

Figure 13 shows one embodiment of a process implemented by memory module controller 1202 to perform a read transaction from one or more of SDRAMs 1204-1207 after receiving a read request from system memory bus 1242. Figure 13 is described with the aid of the exemplary timing diagram of Figure 14. It will be appreciated that Figure 14 shows CLK 1228 having approximately twice the frequency of CLK 1208. For one embodiment, CLK 1228 may have a frequency of approximately 400 MHz and CLK 1208 may have a frequency of approximately 200 MHz. For other embodiments, different ratios of frequencies, and/or different frequencies, may be used.

Memory module controller 1202 may implement the process of Figure 13 using the circuitry shown in memory module 1000 of Figure 10. For example, CLK 1024 corresponds to CLK 1228, CMD/ADDR 1026 corresponds to row 1234 and column 1236, data 1027 corresponds to data 1232, CLK 1030 corresponds to CLK 1208, address 1032 corresponds to address 1214, memory control signals 1034 corresponds to control bus 1238, and data

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1036 corresponds to data 1224. For other embodiments, other circuitry may be used to implement the process of Figure 13.

The process starts at step 1302. At step 1304 and from time t0 to time t1, an activate command is sent on row lines 1234 including a device, bank, and row address of selected memory locations in one or more of SDRAMs 1204-1207. At step 1306 and from time t2 to time t3, data request logic 1004 deserializes the command and address information and provides this information to control logic 1002. Control logic 1002 then provides the row address to the selected SDRAMs over address bus 1214 and/or 1222, and the appropriate bank activate command to the selected SDRAMs over control bus 1238 and/or 1240. For one embodiment, the appropriate bank activate command includes disabling CAS lines 1211 and/or 1219 and WE lines 1210 and/or 1218, and enabling CS lines 1213 and/or 1221 and RAS lines 1212 and/or 1220 at the rising edge of CLK 1208 and/or 1216.

Because the memory addressing scheme protocol used by Direct RDRAM™ devices may be different than that used by the selected SDRAMs, the activate command supplied on row address lines 1234 may include column address information for the selected SDRAMs. In this example, this column address information may be stored in address storage unit 1040 until such time that the column address information is issued to the selected SDRAMs.

At step 1308 and from time t4 to time t6, a read command is sent on column lines 1236. The read command includes device, bank, and column address information for the desired read location in the selected SDRAMs. At step 1310 and from time t6 to time t7, request handling logic 1004 deserializes the read command and provides this information to control logic 1002. Control logic 1002 then provides the column address and the read command to the selected SDRAMs over address bus 1214 and/or 1222 and over control bus 1238 and/or 1240, respectively. For one embodiment, the appropriate read command includes disabling RAS lines 1212 and/or 1220 and WE lines 1210 and/or 1218, and enabling CS lines 1213 and/or 1221

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and CAS lines 1211 and/or 1219 at the rising edge of CLK 1208 and/or CLK 1216.

If there is a difference between the number of bytes selected in the selected SDRAMs and the number of bytes expected from a single read transaction by the system memory controller, then steps 1308 and 1310 may be repeated a desired number of times to match the number of bytes. For example, as shown in Figure 14, if the first read command READ1 on column 1236 (together with the activate command on row 1234) addresses 16 bytes of data and the read command to the selected SDRAMs addresses 32 bytes of data, then a second read command READ2 may be issued from time t6 to time t9 to address the second 16 bytes.

At step 1312 and from time t8 to time t15, data I/O circuitry 1022 may receive data read from the selected SDRAMs. For example, 32 bytes of data may be read from the four SDRAMs 1204-1207 in the following manner: from time t8 to time t10 data I/O circuitry 1022 may receive data packet DO that includes the first eight bytes, two bytes from each of the four SDRAMs 1204-1207; from time t10 to time t12 data packet D1 that includes the second eight bytes, two bytes from each of the four SDRAMs; from time t12 to time t13 data packet D2 that includes the third eight bytes, two bytes from each of the four SDRAMs; and, from time t13 to time t14 data packet D3 that includes the last eight bytes, two bytes from each of the four SDRAMs. It will be appreciated that for other embodiments a different number of bytes and a different number of cycles may be required to read the selected data from the selected SDRAMs.

When the read data is received, it may be stored in read buffer 1038 prior to providing the data to data handling logic 1046. Alternatively, it may be provided directly to data handling logic 1046. At step 1314, data handling logic may serialize or pack the data into the proper format expected by the system memory controller on data bus 1232. For one embodiment, data packets D0 and D1, including a total of 16 bytes of data from SDRAMs 1204-1207, may be packed into one uninterrupted transmission DATA1 that may provided to data bus 1232 at step 1316 and

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from time t11 to time t15. Similarly, data packets D2 and D3, including a second 16 bytes of data from SDRAMs 1204-1207 may be packed into one uninterrupted transmission DATA2 that may provided to data bus 1232 at step 1316 and from time t14 to time t16.

Figure 15 shows one embodiment of a process implemented by memory module controller 1202 to perform a write transaction to one or more of SDRAMs 1204-1207 after receiving a write request from system memory bus 1242. The same process may be used to write data to any of the SDRAMs. Figure 15 is described with the aid of the exemplary timing diagram of Figure 16. Memory module controller 1202 may implement the process of Figure 13 using the circuitry shown in memory module 1000 of Figure 10.

It will be appreciated that Figure 15 shows CLK 1228 having approximately twice the frequency of CLK 1208. For one embodiment, CLK 1228 may have a frequency of approximately 400 MHz and CLK 1208 may have a frequency of approximately 200 MHz. For other embodiments, different ratios of frequencies, and/or different frequencies, may be used.

The process starts at step 1502. At step 1504 and from time t0 to time t1, an activate command is sent on row lines 1234 including a device, bank, and row address of memory locations in one or more of selected SDRAMs 1204-1207. At step 1506, data request logic 1004 deserializes the command and address information and provides this information to control logic 1002.

Because the memory addressing scheme protocol used by Direct RDRAM™ devices may be different than that used by SDRAMs 1204-1207, the activate command supplied on row address lines 1234 may include column address information for the selected SDRAMs. In this example, this column address information may be stored in address storage unit 1040 until such time that the column address information is issued to the selected SDRAMs.

At step 1508 and from time t2 to time t3, a write command is sent on column lines 1236. The write command includes device, bank, and column

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address information for the desired write locations in the selected SDRAMs. At step 1510, request handling logic 1004 deserializes the write command and provides this information to control logic 1002. If there is a difference between the number of bytes selected for writing in the selected SDRAMs and the number of bytes selected by the system memory controller, then steps 1508 and 1510 may be repeated a desired number of times to match the number of bytes. For example, as shown in Figure 16, if the first write command WRITE1 on column 1236 (together with the activate command on row 1234) selects 16 bytes of data and the write command to the selected SDRAMs addresses 32 bytes of data, then a second write command WRITE2 may be issued from time t3 to time t4 to address the second 16 bytes.

At step 1512 and from time t5 to time t6, data handling logic 1046 may receive write data DATA1 from data bus 1232 and may unpack or deserialize the write data. Data handling logic 1046 may store the write data DATA1 into write buffer 1012, and address storage 1014 may store the write address output by request handling logic 1004. If a subsequent write or read command is received, control logic 1002 may inspect write buffer 1012 and address storage 1014 for the requested address. If the address is located in address storage 1014, then the corresponding data in write buffer 1012 may be read or overwritten. If a subsequent write command WRITE2 is issued, then DATA2 received from time t8 to time t10, and associated with this command, may be unpacked or deserialized and also stored in write buffer 1012.

At step 1516 and from time t6 to time t7, control logic 1002 then provides the row address to the selected SDRAMs over address bus 1214 and/or 1222, and the appropriate bank activate command to the selected SDRAMs over control bus 1238 and/or 1240. For one embodiment, the appropriate bank activate command includes disabling CAS lines 1211 and/or 1219 and WE lines 1210 and/or 1218, and enabling CS lines 1213 and/or 1221 and RAS lines 1212 and/or 1220 at the rising edge of CLK 1208 and/or CLK 1216. At step 1518 and from time t9 to time t11, control logic 1002 then provides the column address and the write command to the

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selected SDRAMs over address bus 1214 and/or 1222 and control bus 1238 and/or 1240, respectively. For one embodiment, the appropriate write command includes disabling RAS lines 1212 and/or 1210 and enabling CS lines 1213 and/or 1221, RAS lines 1212 and/or 1210, and WE lines 1210 and/or 1218 at the rising edge of CLK 1208 and/or CLK 1216.

At step 1520 and from time t9 to time t14, control logic may cause the write data to be provided to the selected SDRAMs on data lines 1224, 1225, 1226, and/or 1227 from data I/O circuitry 1022. For example, 32 bytes of data may be written to the four SDRAMs 1204-1207 in the following manner: from time t9 to time t11 data I/O circuitry 1022 may provide data packet D0 including the first eight bytes, two bytes to each of the four SDRAMs; and from time t11 to time t12 data packet D1 including the second eight bytes, two bytes to each of SDRAMs 1204-1207. D0 and D1 may correspond to DATA1. Additionally, from time t12 to time t13 data I/O circuitry 1022 may provide data packet D2 including the third eight bytes, two bytes to each of SDRAMs 1204-1207, and from time t13 to time t14 data packet D3 including the last eight bytes, two bytes to each of SDRAMs 1204-1207. D2 and D3 may correspond to DATA2. It will be appreciated that for other embodiments a different number of bytes and a different number of cycles may be required to write the selected the data to the selected SDRAMs. Although in this example all DRAMs are written to, in alternative embodiments a partial write to one (or less than all) of the SDRAMs may be executed.

In an alternative embodiment, memory module controller 102 may also provide a bridge between system memory bus 1242 and SDRAMs 1204-1207 using a modified protocol. The modified protocol may be demultiplexed having a data bus and a separate control bus that transmits control information and address between a system memory controller (e.g., system memory controller 304 of Figure 3) and memory module controller 1202.

In this embodiment, a read transaction from one or more of SDRAMs 1204-1207 may be performed as shown in Figure 17 wherein row bus 1234 and column bus 1236 are used as one control bus 1235 having eight

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signal lines. For other embodiments, a different number of signal lines may be used.

From time t0 to time t1, an activate command is sent on control bus 1235 including a device, bank, and row address of selected memory locations in SDRAMs 1204-1207. In this embodiment, the activate command may be spread over two cycles (i.e., cycle 0 and cycle 1 in Table 1 below) of CLK 1228 in which data is transferred on each clock edge of the CLK 1228 (i.e., double-pumped). For one embodiment the packet format is as shown in Table 1 where RQ[7:0] correspond to the signal lines of control bus 1235.

Cycle	RQ[7]	RQ[6]	RQ[5]	RQ[4]	RQ[3]	RQ[2]	RQ[1]	RQ[0]
0	ST	SF	D[4]	D[3]	D[2]	D[1]	D[0]	B[0]
0	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	B[1]
1	R[13]	R[12]	R[11]	R[10]	R[9]	R[8]	R[7]	B[2]

TABLE 1

The activate command includes several fields:

B[2:0] Bank Select: Selects one of eight banks in SDRAMs 1204-1207;

D[4:0] Device Select: Selects one of 2^5 or 32 memory module controllers;

R[13:0] Row Address: Provides a row address for one or more locations selected in SDRAMs 1204-1207; and

ST, SF Encoded Frame/Fast Command: Bits used to indicate whether a command is framed as indicated in Table 2. The Extended commands may include noop, precharge, refresh, and other commands.

ST	SF	Operation
0	0	No Framing
0	1	Frame an Active Command (page activate)
1	0	Frame a Read/Write Command

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		(page hit)
1	1	Frame an Extended Command

TABLE 2

From time t2 to time t3, data request logic 1004 deserializes the command and address information and provides this information to control logic 1002. Control logic 1002 then provides the row address to the selected SDRAMs over address bus 1214 and/or 1222, and the appropriate bank activate command to the selected SDRAMs over control bus 1238 and/or 1240 (e.g., as described above with respect to Figures 13 and 14).

From time t4 to time t5, a read command is sent on control bus 1235. The read command includes device, bank, and column address information for the desired read locations in the SDRAMs. In this embodiment, the read command may be spread over two cycles (i.e., cycle 0 and cycle 1 in Table 3 below) of CLK 1228, and have a packet format as shown in Table 3.

Cycle	RQ[7]	RQ[6]	RQ[5]	RQ[4]	RQ[3]	RQ[2]	RQ[1]	RQ[0]
0	ST	SF	D[4]	D[3]	D[2]	D[1]	D[0]	B[0]
0	C[6]	C[5]	C[4]	C[3]	C[2]	C[1]	C[0]	C[1]
1	AP	R/W	C[11]	C[10]	C[9]	C[8]	C[7]	C[2]

TABLE 3

The read command includes several different fields not present in the activate command:

C[11:0] Row Address: Provides a column address for one or more locations selected in SDRAMs 1204-1207;

R/W Read Write: indicates whether the command is a read transaction or a write transaction. When this signal is in one logical state it indicates a read transaction, and when it is in the complementary logic state it indicates a write transaction; and

AP Autoprecharge: Indicates whether the selected column (or row) of selected memory cells should be precharged after reading.

From time t6 to time t8, request handling logic 1004 deserializes the read command and provides this information to control logic 1002. Control

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logic 1002 then provides the column address and the read command to the selected SDRAMs over address bus 1214 and/or 1222 and over control bus 1238 and/or 1240, respectively, (e.g., as described above with respect to Figures 13 and 14). If the first read command READ1 on control bus 1235 addresses less bytes of data and the read command issued to SDRAMs 1204-1207, then a second read command READ2 may be issued from time t7 to time t9.

From time t10 to time t16, data I/O circuitry 1022 may receive data read from the selected SDRAMs. For example, 32 bytes of data may be read from the four SDRAMs 1204-1207 in the following manner: from time t10 to time t11 data I/O circuitry 1022 may receive data packet DO that includes the first eight bytes, two bytes from each of the four SDRAMs 1204-1207; from time t11 to time t12 data packet D1 that includes the second eight bytes two bytes from each of the four SDRAMs; from time t13 to time t14 data packet D2 that includes the third eight bytes, two bytes from each of the four SDRAMs; and, from time t14 to time t16 data packet D3 that includes the last eight bytes, two bytes from each of the four SDRAMs. It will be appreciated that for other embodiments a different number of bytes and a different number of cycles may be required to read the selected data from the selected SDRAMs.

When the read data is received, it may be stored in read buffer 1038 prior to providing the data to data handling logic 1046. Alternatively, it may be provided directly to data handling logic 1046. At step 1314, data handling logic may serialize or pack the data into the proper format expected by the system memory controller on data bus 1232. For one embodiment, data packets D0 and D1, including a total of 16 bytes of data from SDRAMs 1204-1207, may be packed into one uninterrupted transmission DATA1 that may provided to data bus 1232 from time t12 to time t15. Similarly, data packets D2 and D3, including a second 16 bytes of data from SDRAMs 1204-1207 may be packed into one uninterrupted transmission DATA2 that may provided to data bus 1232 from time t15 to time t17.

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For this embodiment, a write transaction to one or more of SDRAMs 1204-1207 may be performed as shown in Figure 18. From time t0 to time t1, an activate command as shown in Table 1 is sent on control bus 1235 including a device, bank, and row address of memory locations in one or more of SDRAMs 1204-1207. Data request logic 1004 deserializes the command and address information and provides this information to control logic 1002.

From time t2 to time t3, a write command is sent on control bus 1235 that includes device, bank, and column address information for the desired write locations in SDRAMs 1204-1207. The write command uses the packet format shown in Table 3 with the R/W bit set appropriately to indicate a write transaction. Request handling logic 1004 deserializes the write command and provides this information to control logic 1002. If there is a difference between the number of bytes selected for writing in SDRAMs 1204-1207(e.g., 32 bytes) and the number of bytes selected by the single write transaction issued by the system memory controller (e.g., 16 bytes), then the first write command WRITE1 on control bus 1235 may write a first amount (e.g., 16 bytes) of data, and a second write command WRITE2 may be issued from time t4 to time t5 to write a second amount of data (e.g., another 16 bytes).

From time t6 to time t9, data handling logic 1046 may receive write data DATA1 from data bus 1232 and may unpack or deserialize the write data. Data handling logic 1046 may store the write data DATA1 into write buffer 1012, and address storage 1014 may store the write address output by request handling logic 1004. If a subsequent write or read command is received, control logic 1002 may inspect write buffer 1012 and address storage 1014 for the requested address. If the address is located in address storage 1014, then the corresponding data in write buffer 1012 may be read or overwritten. If a subsequent write command WRITE2 is issued, then DATA2 received from time t9 to time t11, and associated with this command, may be unpacked or deserialized and also stored in write buffer 1012.

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From time t7 to time t8, control logic 1002 then provides the row address to the selected SDRAMs over address bus 1214 and/or 1222, and the appropriate bank activate command to SDRAMs 1204-1207 over control bus 1238 and/or 1240 (e.g., as described above with respect to Figures 15 and 16). From time t11 to time t12, control logic 1002 then provides the column address and the write command to the selected SDRAMs over address bus 1214 and/or 1222 and over control bus 1238 and/or 1240, respectively (e.g., as described above with respect to Figures 15 and 16).

From time t10 to time t15, control logic may cause the write data to be provided to the selected SDRAMs on data lines 1224, 1225, 1226, and/or 1227 from data I/O circuitry 1022. For example, 32 bytes of data may be written to the four SDRAMs 1204-1207 in the following manner: from time t10 to time t12 data I/O circuitry 1022 may provide data packet D0 including the first eight bytes, two bytes to each of the four SDRAMs; and from time t12 to time t13 data packet D1 including the second eight bytes, two bytes to each of SDRAMs 1204-1207. D0 and D1 may correspond to DATA1. Additionally, from time t13 to time t14 data I/O circuitry 1022 may provide data packet D2 including the third eight bytes, two bytes to each of SDRAMs 1204-1207, and from time t14 to time t15 data packet D3 including the last eight bytes, two bytes to each of SDRAMs 1204-1207. D2 and D3 may correspond to DATA2. It will be appreciated that for other embodiments a different number of bytes and a different number of cycles may be required to write the selected the data to the selected SDRAMs. Although in this example all DRAMs are written to, in alternative embodiments a partial write to one (or less than all) of the SDRAMs may be executed.

Although the present invention has been described in terms of specific embodiments, it will be appreciated that various modifications and alterations might be made by those skilled in the art without departing from the spirit and scope of the invention. The invention should therefore be measured in terms of the claims which follow.

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CLAIMS

What is claimed is:

1. A system comprising:
a system memory controller; and
a first memory module comprising:
a first memory module controller coupled to the system memory controller; and
a first plurality of memory devices coupled to the first memory module controller.

2. The system of claim 1, further comprising a first memory bus coupled between the system first memory module and the first memory module controller.

3. The system of claim 2, wherein the first memory bus comprises a clock signal.

4. The system of claim 2, wherein the first memory bus comprises a handshake signal that indicates when the first memory module controller is communicating data to the system memory controller.

5. The system of claim 2, further comprising a second memory bus coupled between first memory module controller and the first plurality of memory devices.

6. The system of claim 5, wherein the second memory bus comprises a clock signal.

7. The system of claim 5, wherein the first memory bus operates at a first data rate and the second memory bus operates at a second data rate, wherein the first data rate is different than the second data rate.

8. The system of claim 5, wherein the first memory bus has a first number of signal lines and the second memory bus has a second number of

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signal lines, wherein the first number of signal lines is different than the second number of signal lines.

9. The system of claim 5, wherein the first memory module controller comprises:

request handling circuitry structured to receive a first memory transaction from the first memory bus; and

control logic coupled to the request handling circuitry and generating a second memory transaction on the second memory bus corresponding to the first memory transaction on the first bus.

10. The system of claim 2, wherein the first memory bus carries time-multiplexed data and address information, and the second memory bus includes separate address and data lines.

11. The system of claim 1, wherein the first memory module is a dual in-line first memory module (DIMM).

12. The system of claim 1, wherein the first memory module is a single in-line first memory module (SIMM).

13. The system of claim 1, wherein the first plurality of memory devices comprise volatile memory devices.

14. The system of claim 1, wherein the first plurality of memory devices comprise nonvolatile memory devices.

15. The system of claim 1, further comprising a second memory module comprising:

a second memory module controller coupled to the system memory controller; and

a second plurality of memory devices coupled to the second memory module controller.

16. The system of claim 15, wherein the first plurality of memory devices stores data in a different way than the second plurality of memory devices.

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17. A system comprising:

a system memory controller;

a memory bus coupled to the system memory controller; and

a memory comprising:

a memory module controller coupled to the memory bus; and

a plurality of memory devices coupled to the memory module controller, wherein the memory module controller receives a first memory transaction from the memory bus in a first format and provides a second memory transaction in a second format to at least one of the second plurality of memory devices.

18. A method of communicating a memory transaction between a system memory controller and at least one of a plurality of memory devices on a memory module including a memory module controller, the method comprising the steps of:

sending a memory transaction from the system memory controller to the memory module controller, the memory transaction having a first format;

reformatting the memory transaction for the at least one of the memory devices; and

sending the reformatted memory transaction to the at least one of the memory devices.

19. The method of claim 18, wherein the memory transaction is a read transaction.

20. The method of claim 18, wherein the memory transaction is a write transaction.

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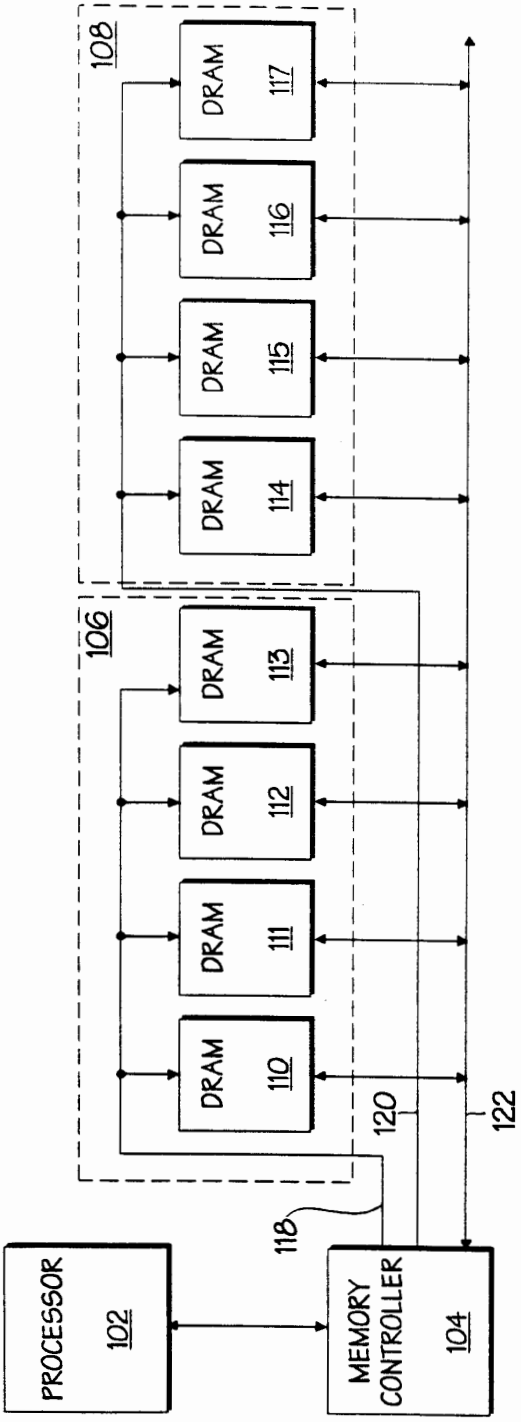


FIG. 1
(PRIOR ART)

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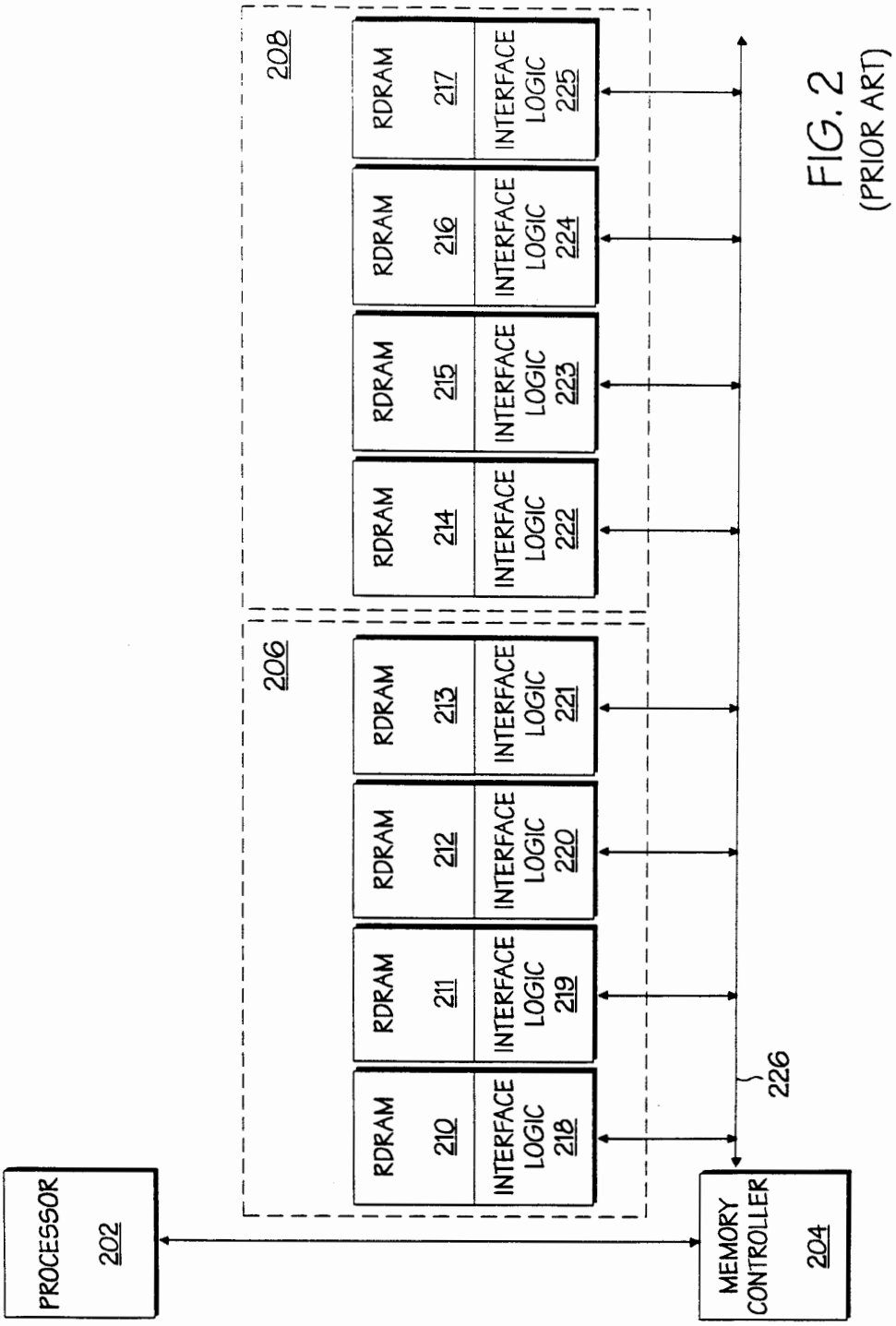


FIG. 2
(PRIOR ART)

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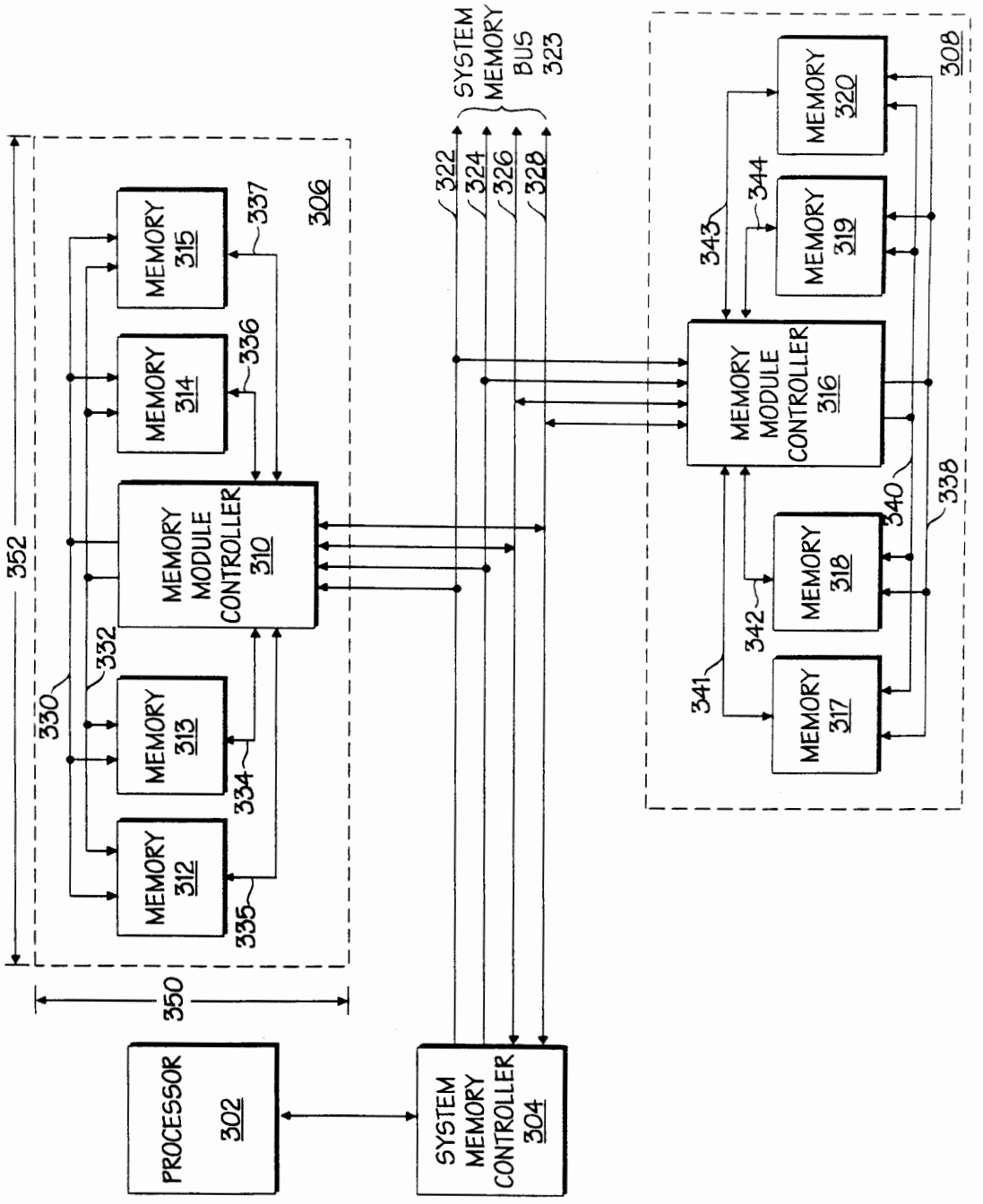


FIG. 3

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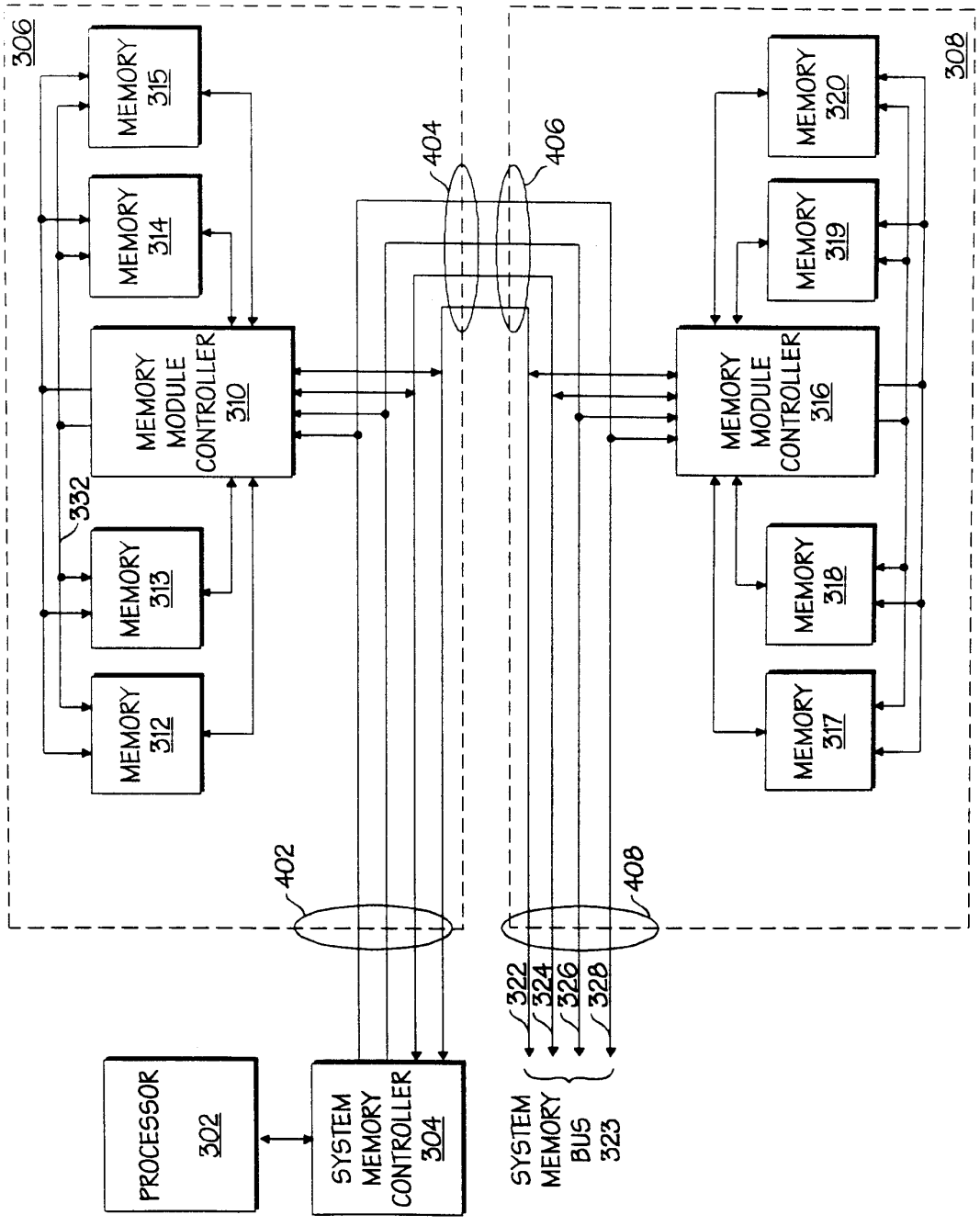


FIG. 4

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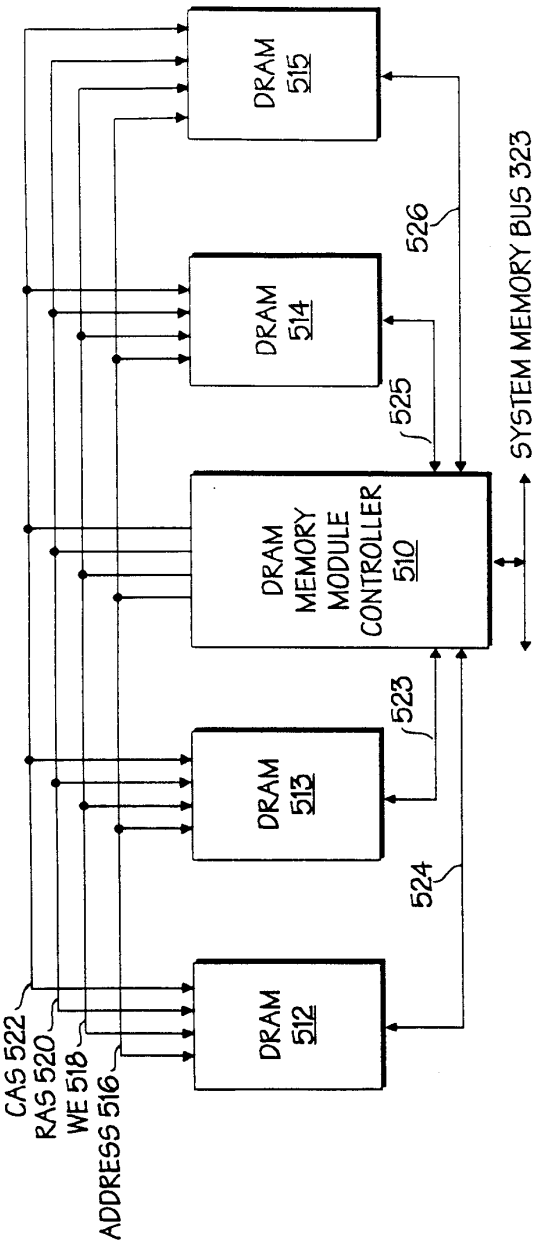


FIG. 5

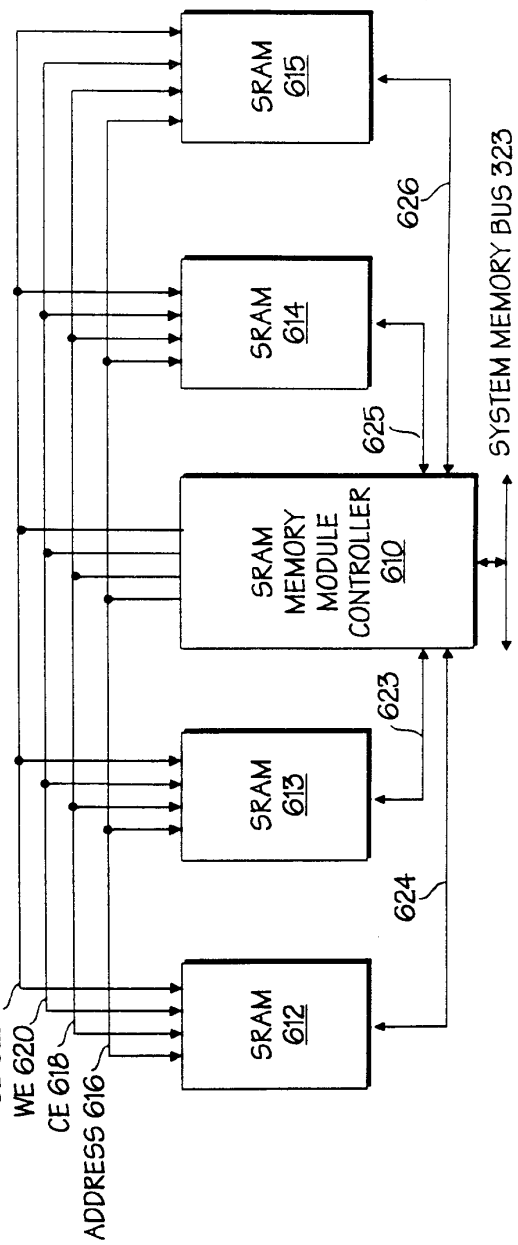


FIG. 6

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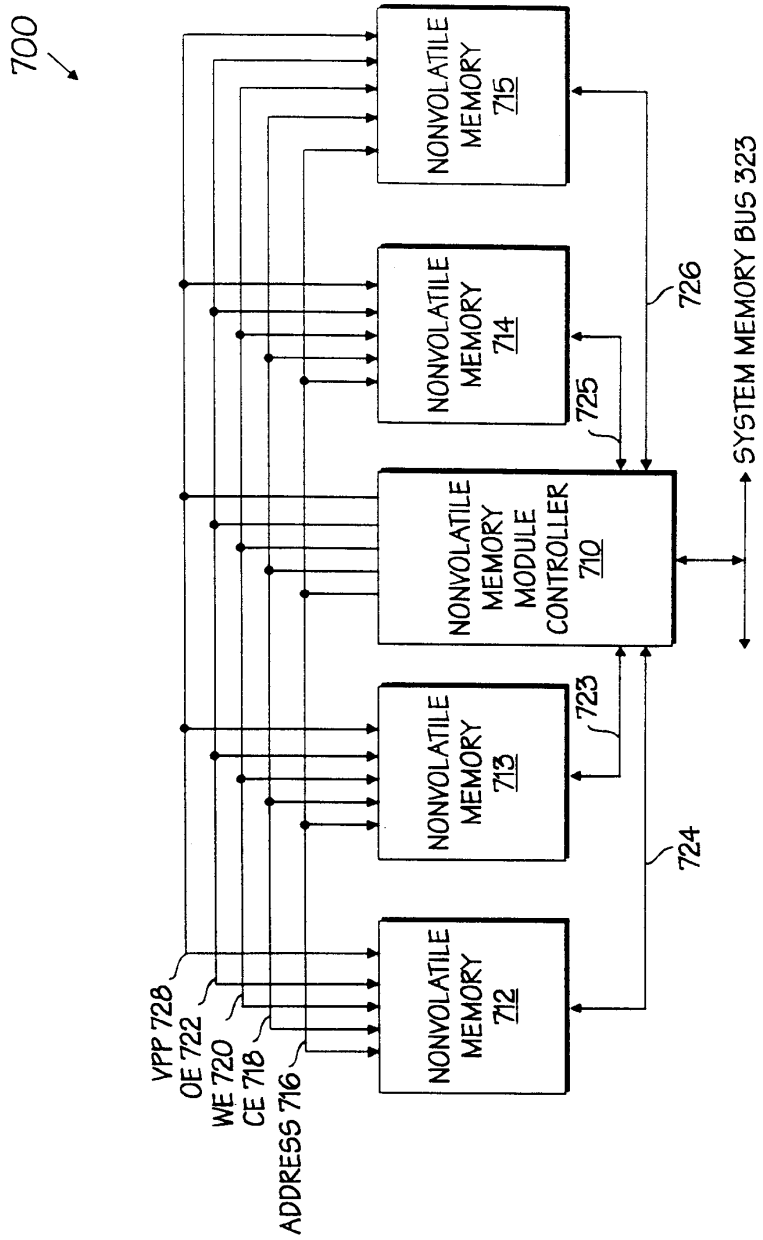


FIG. 7

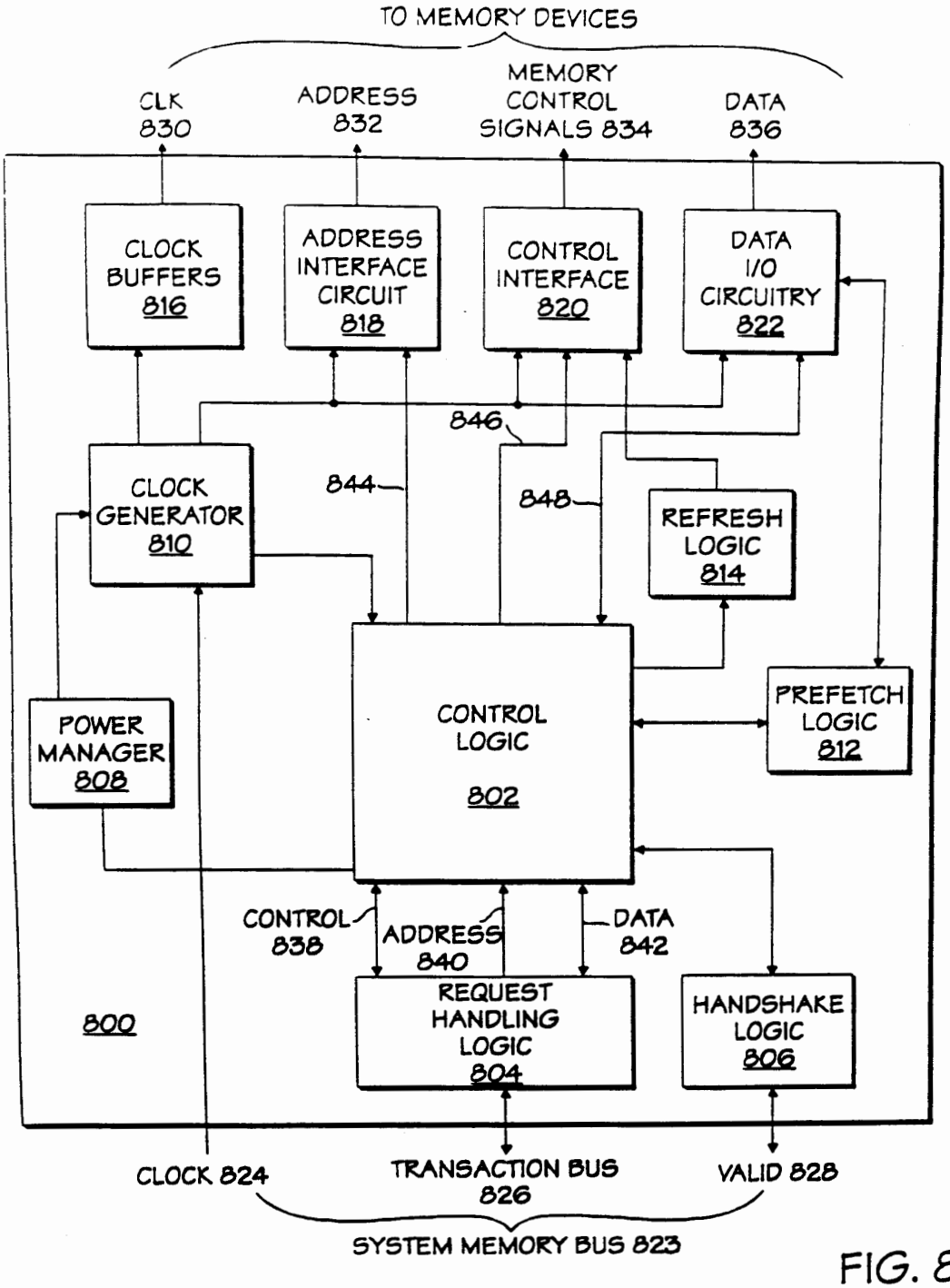


FIG. 8

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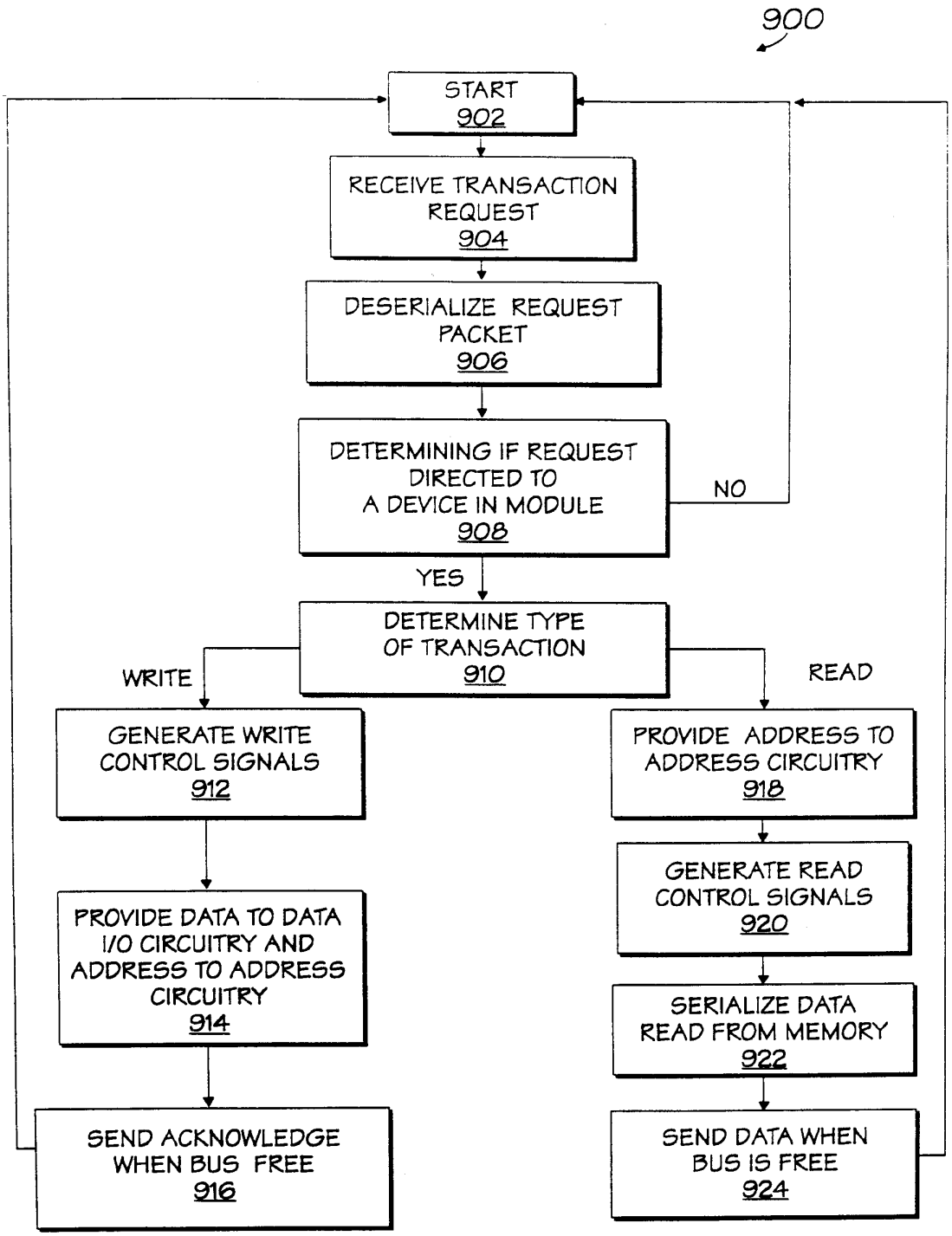


FIG. 9

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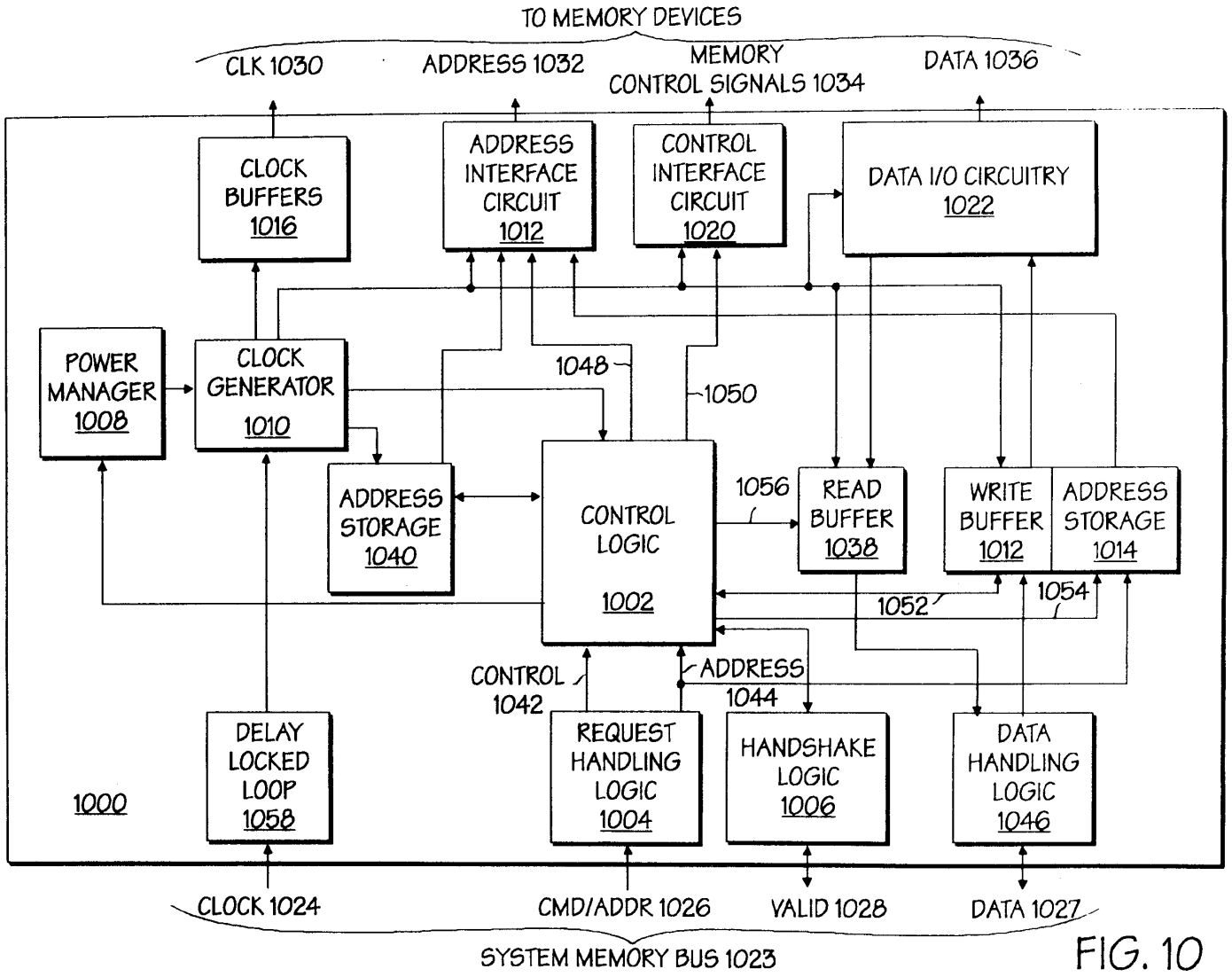

TO MEMORY DEVICES
CLK 1030
ADDRESS 1032
MEMORY CONTROL SIGNALS 1034
DATA 1036
CLOCK BUFFERS 1016
ADDRESS INTERFACE CIRCUIT 1012
CONTROL INTERFACE CIRCUIT 1020
DATA I/O CIRCUITRY 1022
POWER MANAGER 1008
CLOCK GENERATOR 1010
1048
1050
ADDRESS STORAGE 1040
CONTROL LOGIC 1002
1056
READ BUFFER 1038
WRITE BUFFER 1012
ADDRESS STORAGE 1014
1052
1054
CONTROL 1042
ADDRESS 1044
DELAY LOCKED LOOP 1058
REQUEST HANDLING LOGIC 1004
HANDSHAKE LOGIC 1006
DATA HANDLING LOGIC 1046
1000
CLOCK 1024
CMD/ADDR 1026
VALID 1028
DATA 1027
SYSTEM MEMORY BUS 1023

FIG. 10

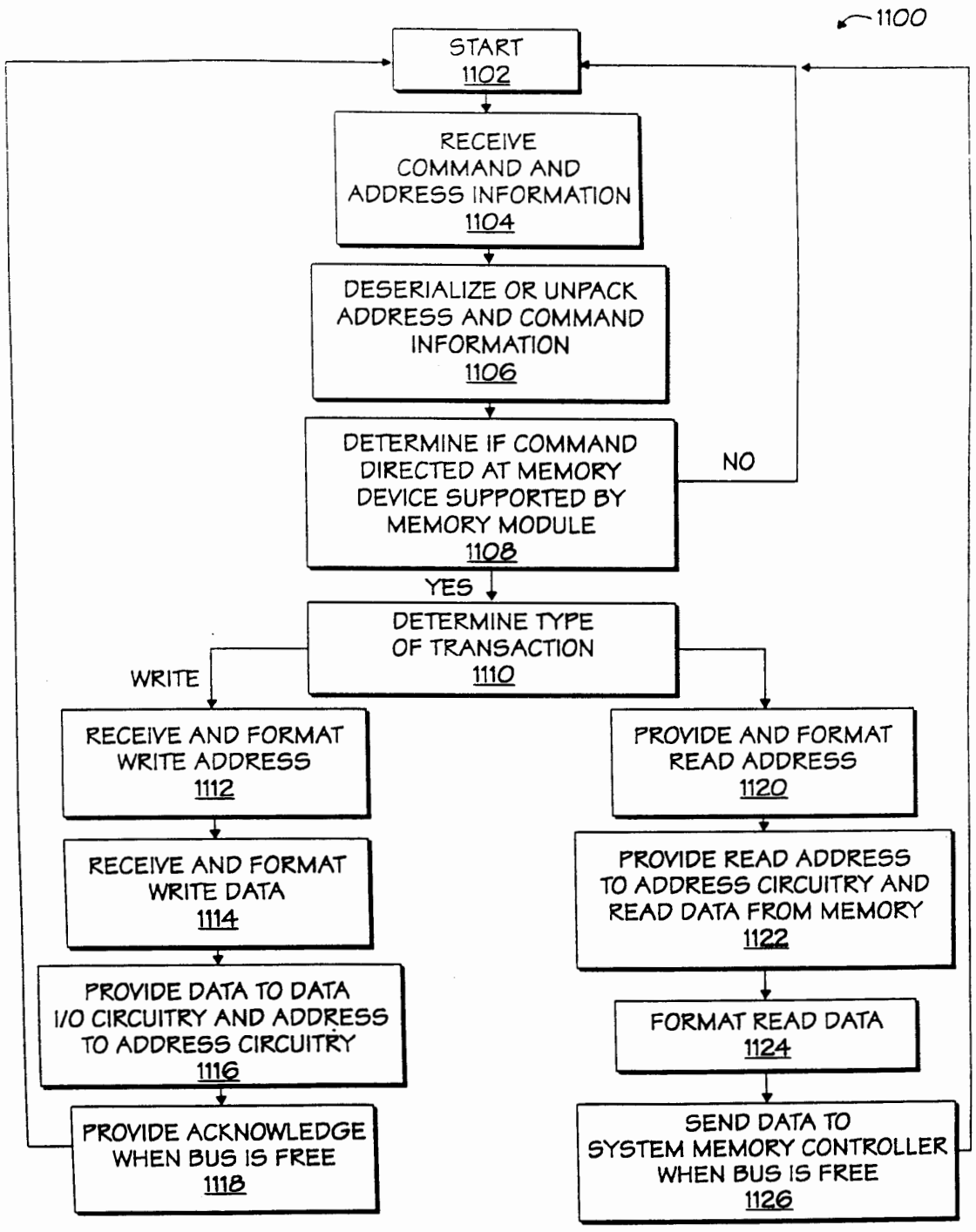


FIG. 11

Petitioners
Ex. 1057, p. 226

SUBSTITUTE SHEET (RULE 26)

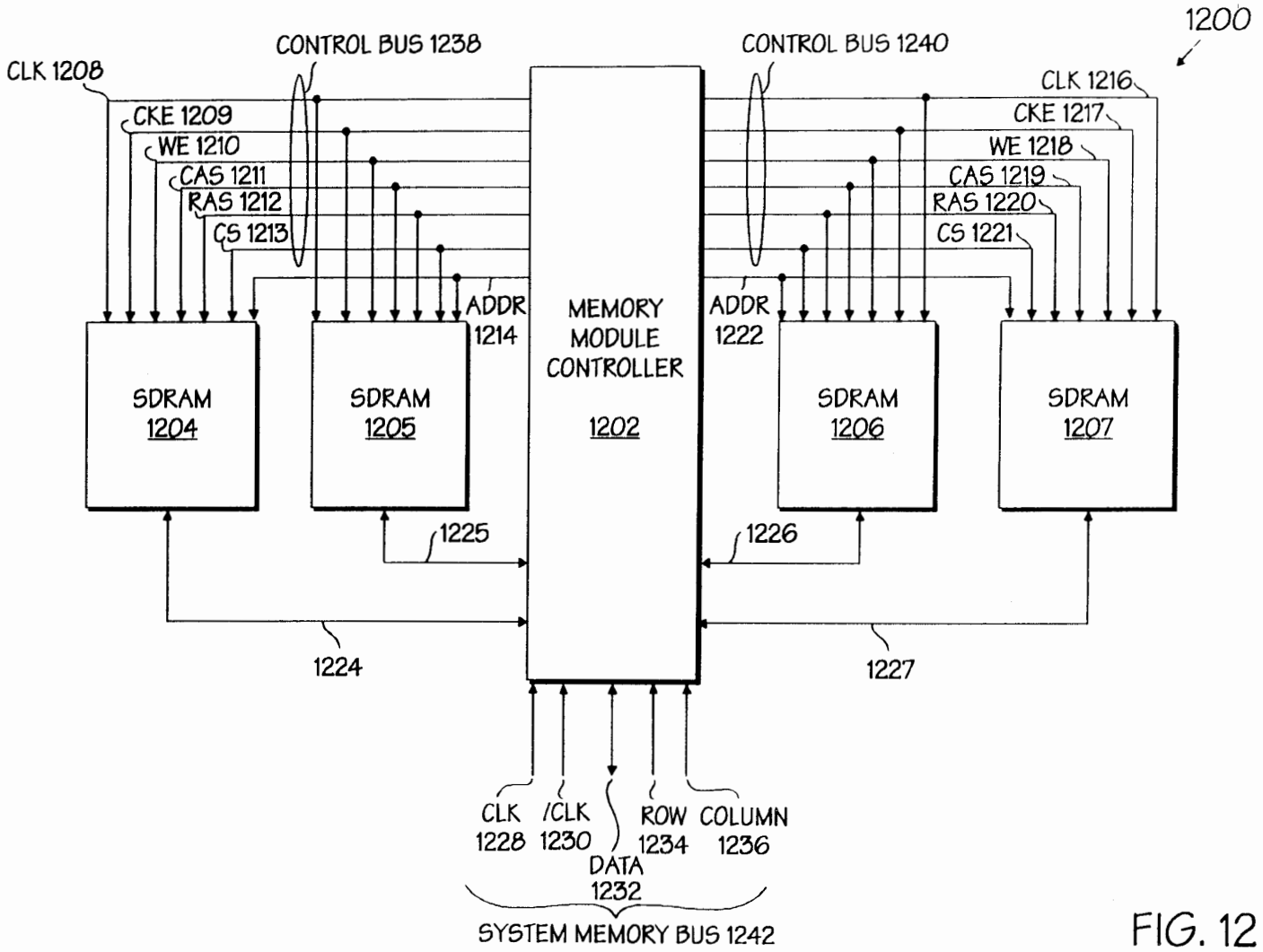


FIG. 12

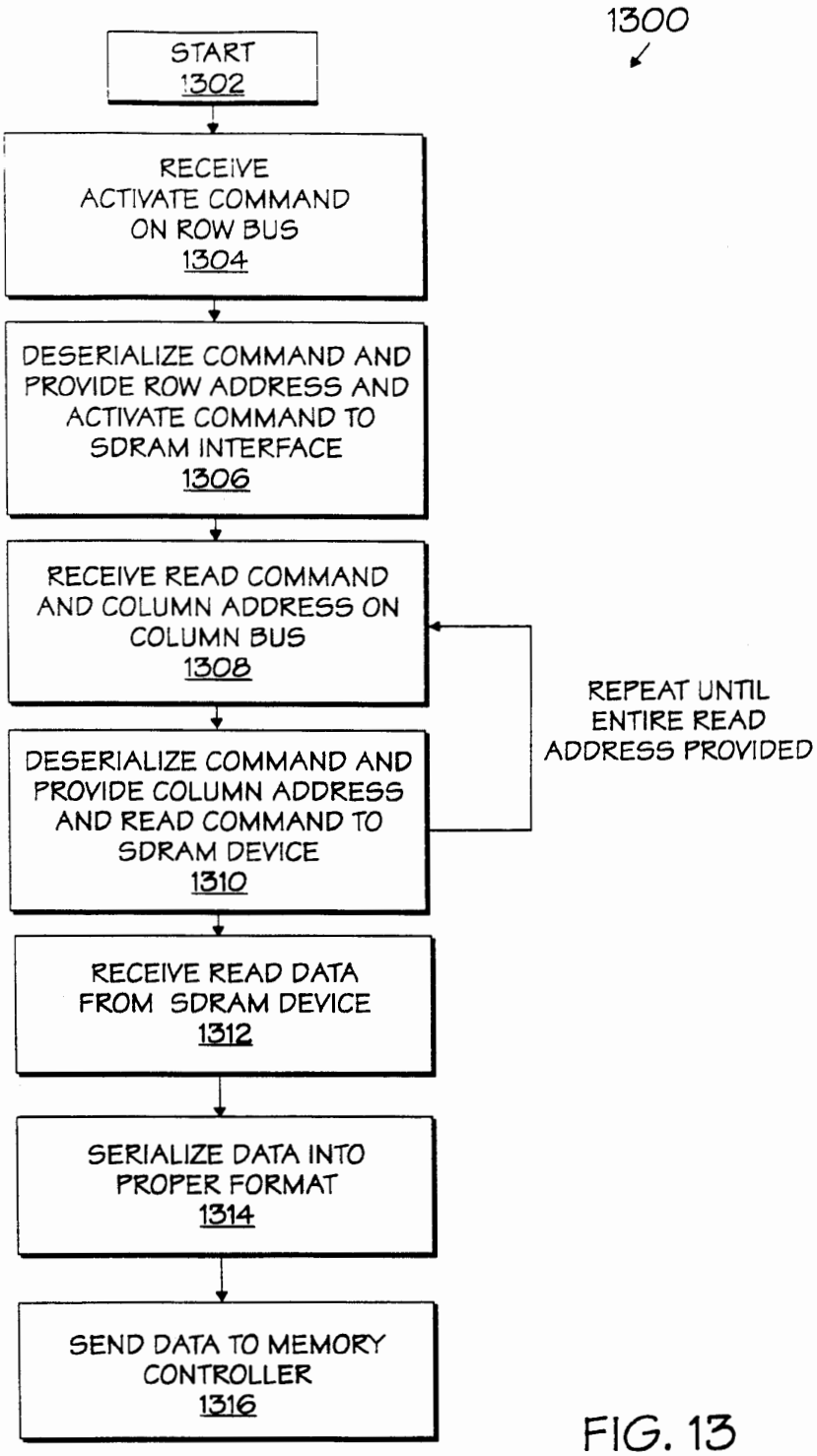


FIG. 13

Petitioners
Ex. 1057, p. 228

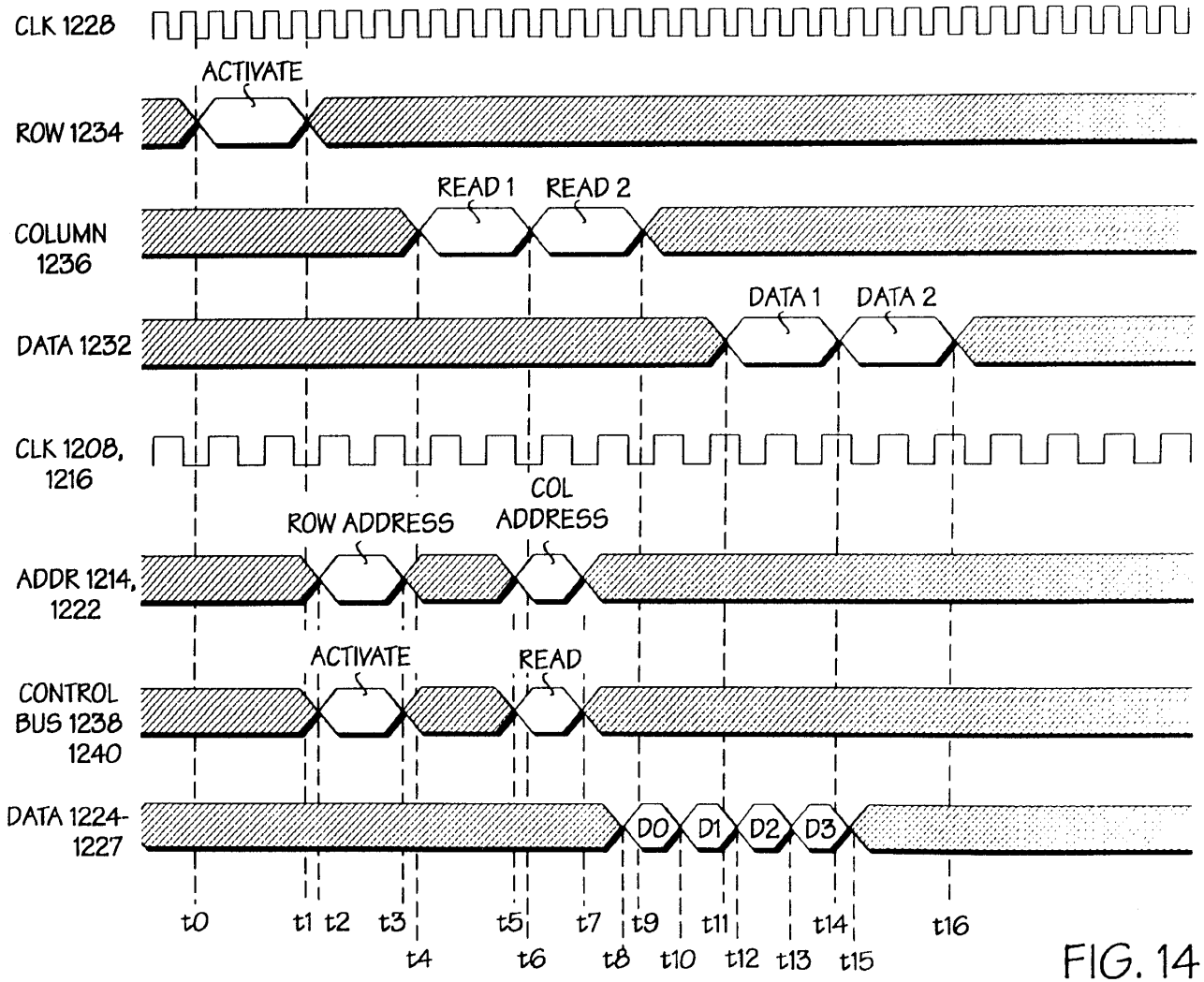


FIG. 14

SUBSTITUTE SHEET (RULE 26)

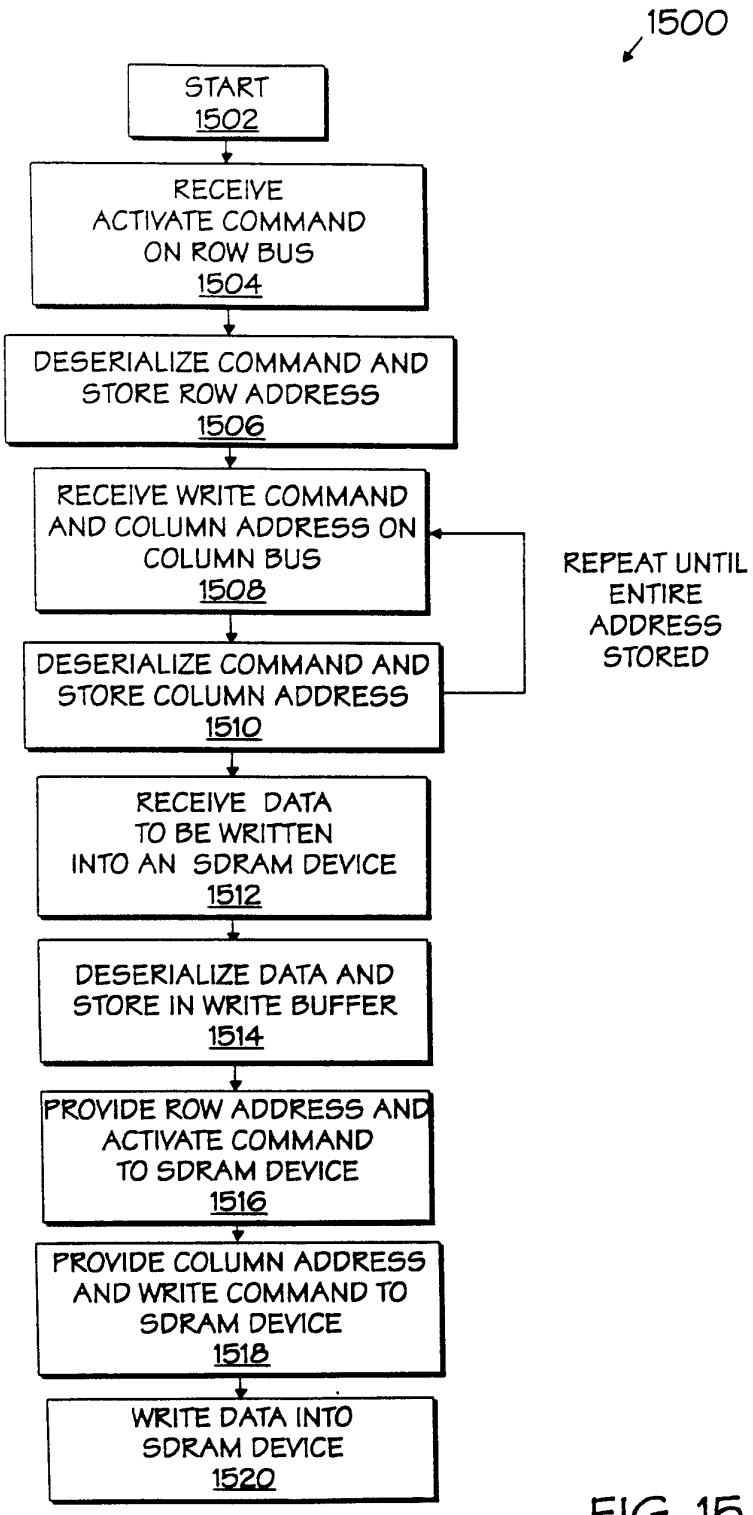


FIG. 15

Petitioners
Ex. 1057, p. 230

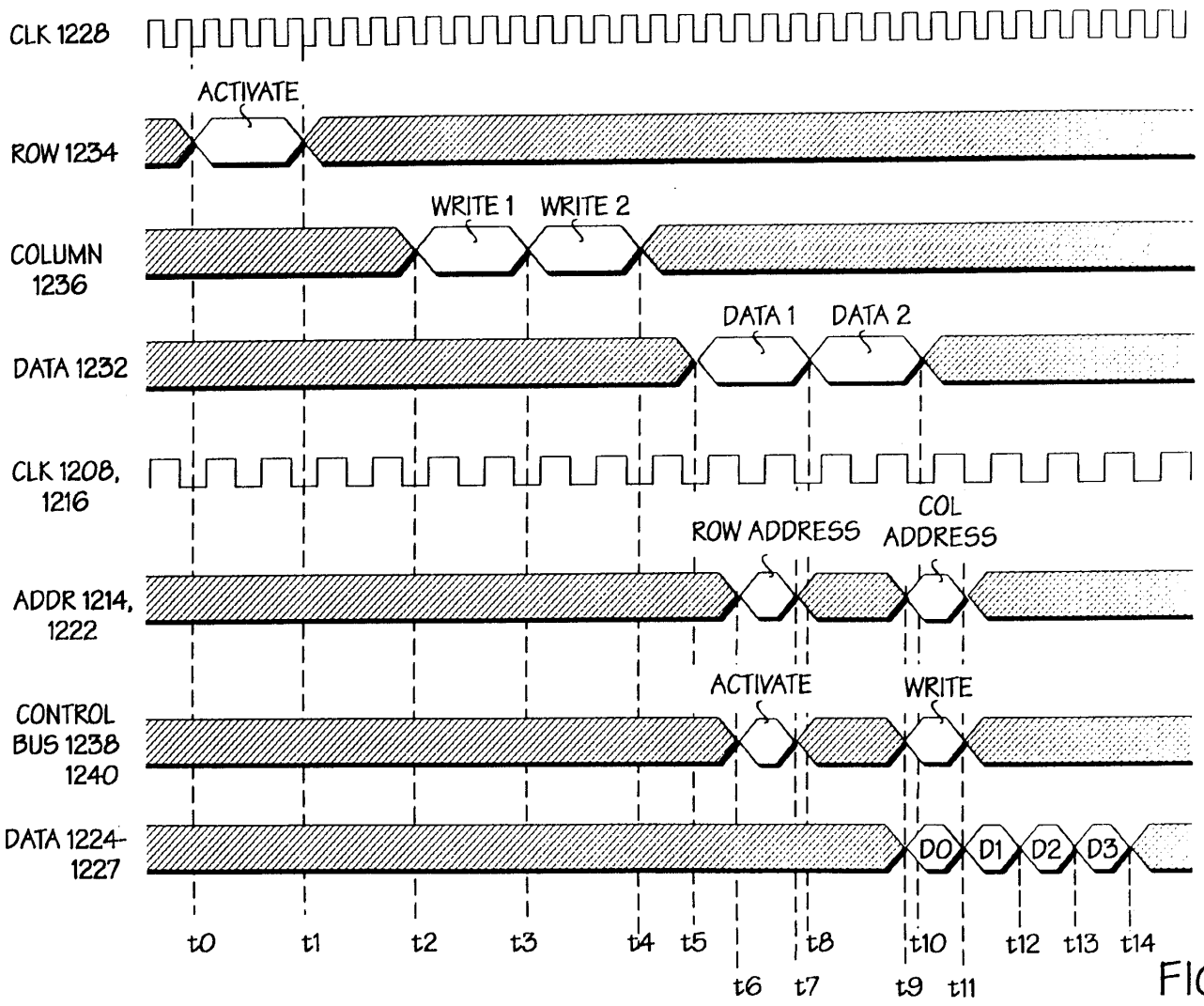

CLK 1228
ACTIVATE
ROW 1234
WRITE 1
WRITE 2
COLUMN 1236
DATA 1
DATA 2
DATA 1232
CLK 1208, 1216
ROW ADDRESS
COL ADDRESS
ADDR 1214, 1222
ACTIVATE
WRITE
CONTROL BUS 1238 1240
DATA 1224-1227
DO
D1
D2
D3
t0
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12
t13
t14

FIG. 16

SUBSTITUTE SHEET (RULE 26)

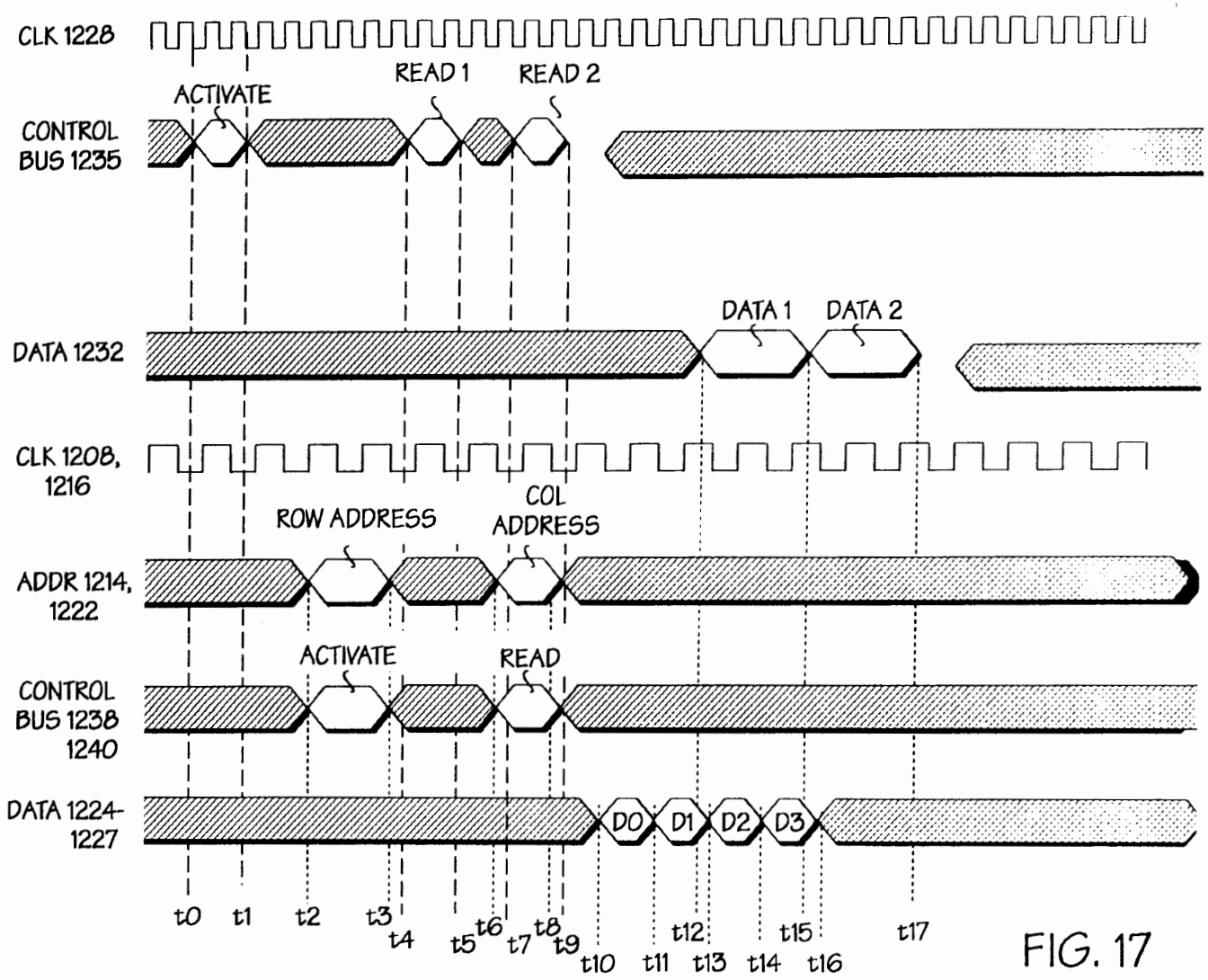


FIG. 17

SUBSTITUTE SHEET (RULE 26)

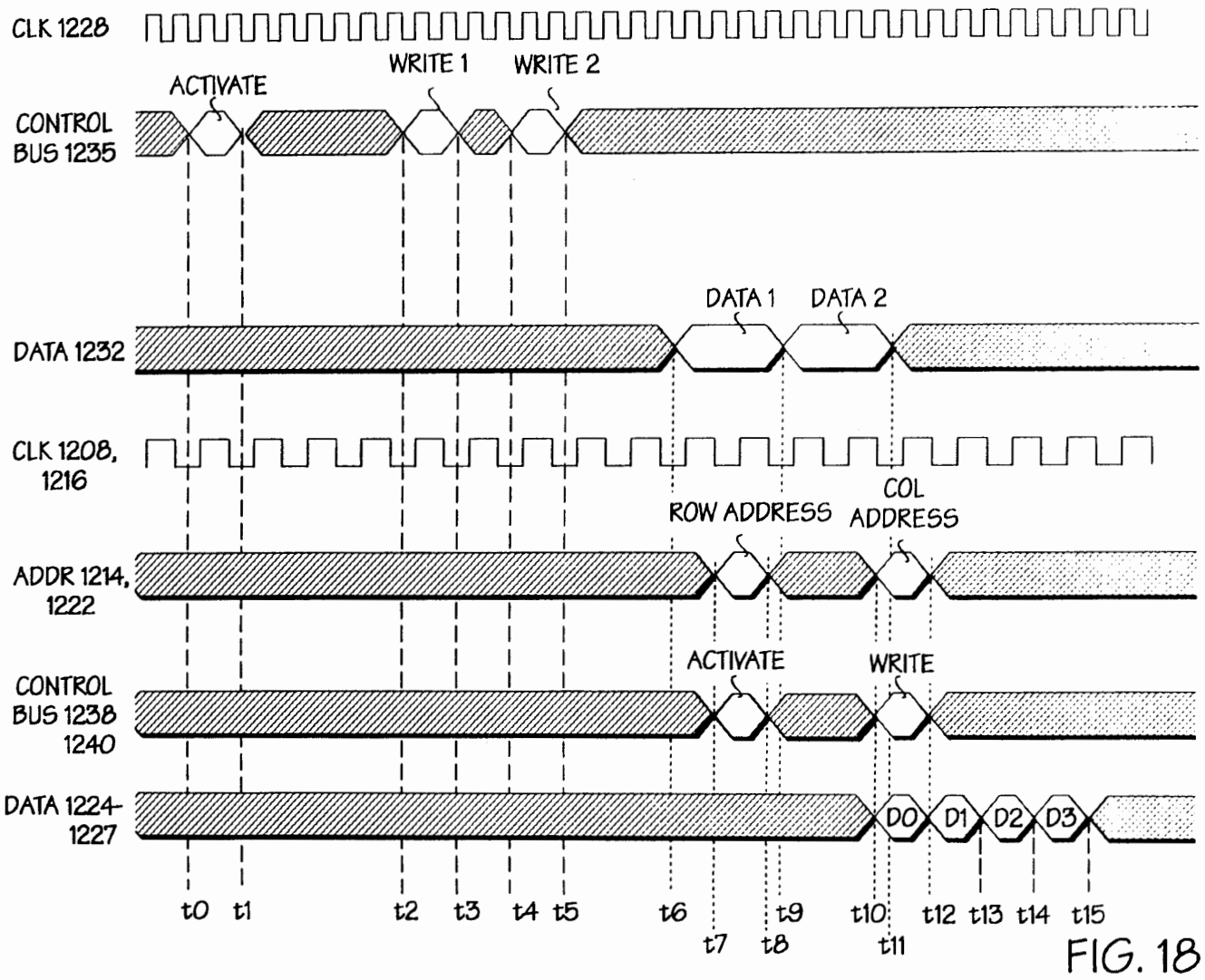


FIG. 18

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/25181

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :G06F 12/06
US CL :711/5
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 711/5

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	BURSKY, Dave. Memory Systems Design and Applications. 1980. Hayden Book Company, Inc. pp. 213-220.	1-20.

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 28 JANUARY 1999	Date of mailing of the international search report 02 APR 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer Kevin Verbrugge Telephone No. (703) 308-6663

Form PCT/ISA/210 (second sheet)(July 1992) ★

Electronic Acknowledgement Receipt

EFS ID:	24973924
Application Number:	14715486
International Application Number:	
Confirmation Number:	1537
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C8
Receipt Date:	22-FEB-2016
Filing Date:	18-MAY-2015
Time Stamp:	00:49:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	2016-02-21_IDS_Cover_NETL018P2C8.pdf	58742 9fb88cbe29a2e78f0202dd05d8c2de43b8bc43d4	no	2
Warnings:					
Information:					

2	Information Disclosure Statement (IDS) Form (SB08)	2016-02-21_IDS_NETL018P2C8.pdf	135909 6fa30d6d1f4b67c2592abe58c173d215ea5d3647	no	3
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Non Patent Literature	Items_4-13.pdf	3896670 5434cfbf4e80b6c82addc83ae9ca39f0c14284f9	no	526
Warnings:					
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4	Non Patent Literature	Items_14-22.pdf	24308407 a299c965feaa6d78b0e25f51269581b57380b4d6	no	841
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5	Non Patent Literature	Items_23-32.pdf	4410503 0420813c487c9483950cbbf78b105bcdf7900dae	no	487
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Information:					
6	Non Patent Literature	Items_33-42.pdf	4028014 f77999bc8195cf8ac1e85464a9ef7f2786a22e46	no	513
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Information:					
		Total Files Size (in bytes):	39355133		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT

Applicant	:	Netlist, Inc.
App. No.	:	14/715,486
Filed	:	May 18, 2015
For	:	MEMORY MODULE WITH DATA BUFFERING
Examiner	:	UNKNOWN
Art Unit	:	2139
Conf No.	:	1537

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 42 references. Copies of foreign documents and/or their translation and non-patent literature are submitted herewith.

The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

This Information Disclosure Statement is being filed before the receipt of a first Office Action on the merits, and presumably no fee is required. If a first Office Action on the merits

was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 50-5963.

Respectfully submitted,

Dated: February 21, 2016

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 521-4828

PTO/SB/08a/b(07-09)
Approved for use through 7/31/2012. OMB 0651-0031
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	3

Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number / Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Related Matters, filed April 28, 2015	
	2.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner Response to Petition, filed February 22, 2016	
	3.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Objections to Evidence, filed February 29, 2016	
	4.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Reply, filed May 19, 2016	
	5.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner Request for Oral Argument, filed June 2, 2016	
	6.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER MOTION FOR OBSERVATIONS, filed June 2, 2016	
	7.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016	
	8.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, ORDER Trial Hearing, filed June 8, 2016	
	9.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016	
	10.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Response to Motion for Observations, filed June 10, 2016	
	11.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Response to Netlist's Submission, filed June 13, 2016	
	12.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's Objections to Petitioner's Demonstrative Exhibits, filed June 23, 2016	

EXAMINER **DATE CONSIDERED**

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PTO/SB/08a/b(07-09)
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US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	14/715,486
				Filing Date	May 18, 2015
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2139
				Examiner Name	Unknown
Sheet	2	of	3	Attorney Docket Number	NETL.018P2C8

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	13.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's Demonstrative Exhibits, filed June 24, 2016	
	14.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Updated Exhibit List, filed June 24, 2016	
	15.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016	
	16.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, May 10, 2016 Deposition of Carl Sechen, filed May 19, 2016	
	17.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Demonstrative Exhibits, filed June 24, 2016	
	18.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016	
	19.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2002, "Videotaped Deposition of Srinivasan Jagannathan, Ph.D on February 12, 2016," filed February 22, 2016	
	20.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2003, "Videotaped Deposition of Srinivasan Jagannathan, Ph.D on April 20, 2015," filed February 22, 2016	
	21.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2007, "Deposition of Dr. Srinivasan Jagannathan on May 25, 2016," filed June 2, 2016	
	22.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner Response to Petition, filed February 22, 2016	
	23.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Objections to Evidence, filed February 29, 2016	
	24.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Reply, filed May 19, 2016	
	25.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner Request for Oral Argument, filed June 2, 2016	
	26.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, PATENT OWNER MOTION FOR OBSERVATIONS, filed June 2, 2016	

EXAMINER **DATE CONSIDERED**

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Substitute for form 1449/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** *(Use as many sheets as necessary)*				***Complete if Known***	
				Application Number	14/715,486
				Filing Date	May 18, 2015
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2139
				Examiner Name	Unknown
Sheet	3	of	3	Attorney Docket Number	NETL.018P2C8

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	27.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016	
	28.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner's SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016	
	29.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Response to Motion for Observations, filed June 10, 2016	
	30.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Response to Patent Owner's Submission, filed June 13, 2016	
	31.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner's Objections to Petitioner's Demonstrative Exhibits, filed June 23, 2016	
	32.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner's Demonstrative Exhibits, filed June 24, 2016	
	33.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Updated Exhibit List, filed June 24, 2016	
	34.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016	
	35.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

Electronic Acknowledgement Receipt

EFS ID:	26218962
Application Number:	14715486
International Application Number:	
Confirmation Number:	1537
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C8
Receipt Date:	30-JUN-2016
Filing Date:	18-MAY-2015
Time Stamp:	00:58:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	2016-06-29_IDS_Cover_NETL018P2C8.pdf	49120 a2c75584a32a727995fb7422aabe2b70d132e9c7	no	2

Warnings:

Information:					
2	Non Patent Literature	1-RM.pdf	42935 698b5f47e18468ab435894c4d46c22f8c3a21f3b	no	7
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3	Non Patent Literature	2-PORP.pdf	376069 6267d25eb5ccfaf2f370b1220f258021b1cc21ee	no	48
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Information:					
4	Non Patent Literature	3-POTE.pdf	1155135 b0aa345c69daf1f3e50a8dc51e9655831872680b	no	5
Warnings:					
Information:					
5	Non Patent Literature	4-PR.pdf	1616745 27e8719b4c9d272d79066825f1b33050e7de3f7b	no	36
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Information:					
6	Non Patent Literature	5-PRFOA.pdf	93433 81d8a7ca83eaeb942ef43e1bce633b0a57b303ad	no	3
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Information:					
7	Non Patent Literature	6-POMFO.pdf	55159 b2da908898e249387a33029358166c090ec7b89d	no	9
Warnings:					
Information:					
8	Non Patent Literature	7-PORFOA.pdf	32545 7899e5003862bc7c2cb4252a3d5b1498c7aa4fec	no	4
Warnings:					
Information:					

9	Non Patent Literature	8-OTH.pdf	90511 47151d2a05dc2bf6cd8f25b247c391fc8e840170	no	4
Warnings:					
Information:					
10	Non Patent Literature	9-POSOPOPR.pdf	99502 a7dd4d48b370af88e812a454a3c72ece46676802	no	4
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Information:					
11	Non Patent Literature	10-PRTMFO.pdf	163560 31fb95ffed70442683aed3541720563ec567a9b8	no	13
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12	Non Patent Literature	11-PRTNS.pdf	947187 882e93f69c0dfe6923d224adaf6d7d22a3f2d74e	no	5
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22	Non Patent Literature	21-DODSJ.pdf	514090 9c26061e023fa78e9b7f59ab9a7b82383fecdce6	no	139
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23	Non Patent Literature	22-PORTP.pdf	259928 80d882a2bf3cd9c35d6f1827b296de87a0dbeec8	no	29
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26	Non Patent Literature	25-PRFOA.pdf	93217 56d2db35ba5f0c392f4ba316e03757bfc8ec6943	no	3
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28	Non Patent Literature	27-PORFOA.pdf	31676 7d5cb43fdbb047a0ff0a34b44ca081bb7f5cc902	no	4
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Information:					

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Information:					
31	Non Patent Literature	30-PRTPOS.pdf	751439 506cf23144cc059153269bd6a71c984772656a89	no	5
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32	Non Patent Literature	31-POOTPDE.pdf	71161 a2677ee98b3921d413748dc8847addb0c6d4c619	no	3
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Information:					
33	Non Patent Literature	32-PODE.pdf	1065513 bf4c0dd34bd2843be745bd891a47bcc80b9e01fa	no	48
Warnings:					
Information:					
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Warnings:					
Information:					
35	Non Patent Literature	34-SDODJ.pdf	616055 d6b21e5c3bf99e612490db6b21e950d35d95a1e1	no	19
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Information:					
36	Non Patent Literature	35-DOPCS.pdf	564714 9d00fd0a060cd6f118715d1df8b0987a2b1db08d	no	65
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37	Information Disclosure Statement (IDS) Form (SB08)	2016-06-29_IDS_NETL018P2C8.pdf	84432 fff04956dd300b067d542e76aedd40f61eba939e	no	3

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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INFORMATION DISCLOSURE STATEMENT

Applicant	:	Netlist, Inc.
App. No.	:	14/715,486
Filed	:	May 18, 2015
For	:	MEMORY MODULE WITH DATA BUFFERING
Examiner	:	UNKNOWN
Art Unit	:	2139
Conf No.	:	1537

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 35 references. Copies of foreign documents and/or their translation and non-patent literature are submitted herewith.

The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

This Information Disclosure Statement is being filed before the receipt of a first Office Action on the merits, and presumably no fee is required. If a first Office Action on the merits

was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 50-5963.

Respectfully submitted,

Dated: June 29, 2016

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 521-4828

PTO/SB/08a/b(07-09)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	2

Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	4,739,473	1988-04-19	Ng	
	2.	5,313,624	1994-05-17	Harriman	
	3.	5,630,096	1997-05-13	Zuravleff	
	4.	5,905,401	1999-05-18	Sher	
	5.	6,011,710	2000-01-04	Wiggers	
	6.	6,061,754	2000-05-09	Cepulis	
	7.	6,141,245	2000-10-31	Bertin	
	8.	6,223,650	2001-05-15	Johnson	
	9.	6,262,938	2001-07-17	Lee	
	10.	6,546,476	2003-04-08	Gillingham	
	11.	6,636,446	2003-10-21	Lee	
	12.	6,704,910	2004-03-09	Hong	
	13.	7,191,302	2007-03-13	Usami	
	14.	7,225,303	2007-05-29	Choi	
	15.	8,856,464	2014-10-07	Karamcheti	
	16.	20010008006	2001-07-12	Klein	
	17.	20020112119	2002-08-15	Halbert et al.	
	18.	20030070052	2003-04-10	Lai	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	19.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Record of Oral Hearing, dated July 26, 2016	
	20.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Final Written Decision, issued September 28, 2016	
	21.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3001 to Final Decision, issued September 28, 2016	
	22.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3001-2 to Final Decision, issued September 28, 2016	

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Substitute for form 1449/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** *(Use as many sheets as necessary)*				***Complete if Known***	
				Application Number	14/715,486
				Filing Date	May 18, 2015
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2139
				Examiner Name	Unknown
Sheet	2	of	2	Attorney Docket Number	NETL.018P2C8

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	23.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3002 to Final Decision, issued September 28, 2016	
	24.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3003 to Final Decision, issued September 28, 2016	
	25.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3004 to Final Decision, issued September 28, 2016	
	26.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Final Decision, issued September 28, 2016	
	27.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Petition for Inter Partes Review, filed December 30, 2016	
	28.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Exhibit 1003, "Declaration of Harold S. Stone," filed December 30, 2016	
	29.	Inter Partes Review of U.S. Patent No. 8516185, Case No. IPR2017-00577, Petition for Inter Partes Review, filed January 5, 2017	
	30.	Inter Partes Review of U.S. Patent No. 8516185, Case No. IPR2017-00577, Exhibit 1003, "Declaration of Harold S. Stone," filed January 5, 2017	
	31.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Exhibit 1008, Declaration of John J. Kelly Regarding Records of Joint Electron Device Engineering Council (JEDEC), filed December 30, 2016	
	32.	JEDEC Standard Double Data Rate (DDR) SDRAM Specification, JESD79 (June 2000)	
	33.	Texas Instruments SN74LS245 octal bus transceivers with 3-state outputs datasheet, 2002	
	34.	Stone, H.S. Microcomputer Interfacing, Reading, MA: Addison Wesley, 1982	
	35.	128Mbit SDRAM, Samsung datasheet K4S281632C, Rev. 00. March 2000	
	36.	G. Moore, "Cramming more components onto integrated circuits," Electronics, volume 38, no. 8, April 19, 1965	

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Electronic Acknowledgement Receipt

EFS ID:	28144402
Application Number:	14715486
International Application Number:	
Confirmation Number:	1537
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C8
Receipt Date:	24-JAN-2017
Filing Date:	18-MAY-2015
Time Stamp:	01:33:56
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	2016-01-23_IDS_Cover_NETL018P2C8.pdf	48694 d79eae392d54bdbeb9942d9efd037f582b34a1b8	no	2

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3	Non Patent Literature	2016-07-26_Oral_Hearing_01020.pdf	426370 1ca1ae3efbf5d2535b03a019e1529c5f70d0313c	no	81
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Information:					
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Information:					
14	Non Patent Literature	Stone_Declaration.pdf	4139489 93018645f8b27353870e2aa60aba1388c273ed75	no	127
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Information:					
15	Non Patent Literature	Kelly_Declaration.pdf	118976 ae64c1ce2733724b3c3a4ba715f829fc18f8fd71	no	3
Warnings:					
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22	Non Patent Literature	Moore_Article.pdf	1196855 6b8d48cc9f9c5eacfa89ff67a26154dce9a3175a	no	4
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New International Application Filed with the USPTO as a Receiving Office
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INFORMATION DISCLOSURE STATEMENT

Applicant	:	Netlist, Inc.
App. No.	:	14/715,486
Filed	:	May 18, 2015
For	:	MEMORY MODULE WITH DATA BUFFERING
Examiner	:	UNKNOWN
Art Unit	:	2139
Conf No.	:	1537

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 36 references. Copies of foreign documents and/or their translation and non-patent literature are submitted herewith.

The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

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Respectfully submitted,

Dated: January 23, 2017

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 521-4828

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14715486
Filing Date	2015-05-18
First Named Inventor	Jeffrey C. Solomon
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	N3044.10002US21

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5357478		1994-10-18	Kikuda et al	
	2	5559970		1996-09-24	Sharma	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14715486
	Filing Date	2015-05-18
	First Named Inventor	Jeffrey C. Solomon
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1	BUSINESS WIRE, Samsung Announces Mass Production of DDR2; Industry's First 1 GigaByte DDR2 DIMM Offers High Speed and Low Power Necessary for Next-Generation PCs and Servers, March 24, 2003.	
	2	BUSINESS WIRE, Samsung DDR2 Ready To Support Market For Next Generation PCs and Servers, September 16, 2003. 8. IEEE, INC., "chip select," IEEE Standard Dictionary of Electrical and Electronic Terms, 5th Ed., 1993.	
	3	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control Nos. 95/000,578; 95/000,579; and 95/001,339, mailed May 31, 2016, 106 pages.	
	4	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control No. 95/001,758, mailed May 31, 2016, 49 pages.	
	5	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control Nos. 95/000,546 and 95/000,577, mailed February 25, 2015, 25 pages.	
	6	Patent Trial and Appeal Board Decision on Request for Rehearing for Reexamination Control Nos. 95/000,546 and 95/000,577, mailed August 27, 2015, 5 pages.	
	7	SMITH, VAN. "Kentron Q&A." Van's Hardware. www.vanshardware.com. December 3, 2001, 4 pages.	
	8	WESTE, NEIL H.E. et al., "CMOS VLSI Design: A Circuits and Systems Perspective." 3rd Edition, 2005. 4 pages.	
	9	"WESTE, NEIL H.E. et al., ""CMOS VLSI Design: A Circuits and Systems Perspective."" 4thEdition, 2011. 4 pages."	
	10	Non-Final Action Closing Prosecution mailed March 21, 2014, for Control Nos. 95/001,339; 95/000,578; and 95/000,579, 92 pages.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14715486
	Filing Date	2015-05-18
	First Named Inventor	Jeffrey C. Solomon
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

	11	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control No. 95/001,381, mailed January 16, 2014, 24 pages.	
	12	Requester Request for Rehearing after Board Decision dated 02/18/2014 for Reexamination Control No. 95/001337	
	13	Patent Owner Response after Board Decision dated 03/18/2014 for Reexamination Control No. 95/001337	
	14	Affidavit-traversing rejectns or objectns rule 132 dated 03/18/2014 for Reexamination Control No. 95/001337	
	15	Patent Owner Response after Board Decision dated 03/19/2014 for Reexamination Control No. 95/001337	
	16	Affidavit-traversing rejectns or objectns rule 132 dated 03/19/2014 for Reexamination Control No. 95/001337	
	17	Patent Owner Comments on Req for Rehearing timely dated 03/19/2014 for Reexamination Control No. 95/001337	
	18	Reexam - Affidavit/Decl/Exhibit Filed by 3rd Party dated 04/17/2014 for Reexamination Control No. 95/001337	
	19	Requester Comments on Patent Owner Response after Board Decision dated 04/17/2014 for Reexamination Control No. 95/001337	
	20	New Board of Appeals Decision after Board Decision with New Ground of Rejection: New Ground of Rejection dated 06/26/2014 for Reexamination Control No. 95/001337	
	21	Patent Owner Response after Board Decision dated 07/29/2014 for Reexamination Control No. 95/001337	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14715486
	Filing Date	2015-05-18
	First Named Inventor	Jeffrey C. Solomon
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

	22	Reexam Petition Decision - Denied dated 08/05/2014 for Reexamination Control No. 95/001337	
	23	Requester Comments on Patent Owner Response after Board Decision dated 09/05/2014 for Reexamination Control No. 95/001337	
	24	Reexam - Affidavit/Decl/Exhibit Filed by 3rd Party dated 09/05/2014 for Reexamination Control No. 95/001337	
	25	Examiner's Determination on Patent Owner Response/Requester Comments after Board Decision dated 06/15/2015 for Reexamination Control No. 95/001337	
	26	Examiner's Determination on Patent Owner Response/Requester Comments after Board Decision dated 09/11/2015 for Reexamination Control No. 95/001337	
	27	Affidavit-traversing rejectns or objectns rule 132 dated 10/14/2015 for Reexamination Control No. 95/001337	
	28	Affidavit-traversing rejectns or objectns rule 132 (26 pages) dated 10/14/2015 for Reexamination Control No. 95/001337	
	29	Patent Owner Comments on Examiner's Determination after Board Decision dated 10/14/2015 for Reexamination Control No. 95/001337	
	30	Reexam - Affidavit/Decl/Exhibit Filed by 3rd Party dated 11/13/2015 for Reexamination Control No. 95/001337	
	31	Reqr Comments on Examiners Determ after Board Decision dated 11/13/2015 for Reexamination Control No. 95/001337	
	32	Other Reference-Patent/App/Search documents dated 11/22/2016 for Reexamination Control No. 95/001337	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14715486
	Filing Date	2015-05-18
	First Named Inventor	Jeffrey C. Solomon
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

	33	Petition under Rule 41.3 to Chief Admin Patent Judge dated 11/22/2016 for Reexamination Control No. 95/001337	
	34	Administrative Remand to Examiner dated 01/19/2017 for Reexamination Control No. 95/001337	
	35	Reexam Petition Decision - Granted - in-part dated 01/23/2017 for Reexamination Control No. 95/001337	
	36	Affidavit-traversing rejectns or objectns rule 132 dated 02/22/2017 for Reexamination Control No. 95/001337	
	37	Patent Owner Comments on Examiner's Determination after Board Decision dated 02/22/2017 for Reexamination Control No. 95/001337	
	38	Reexam - Affidavit/Decl/Exhibit Filed by 3rd Party dated 03/22/2017 for Reexamination Control No. 95/001337	
	39	Requester Comments on Patent Owner Response after Board Decision dated 03/22/2017 for Reexamination Control No. 95/001337	

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Examiner Signature		Date Considered	

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14715486
	Filing Date	2015-05-18
	First Named Inventor	Jeffrey C. Solomon
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/JAMIE J. ZHENG/	Date (YYYY-MM-DD)	2017-05-09
Name/Print	Jamie J. Zheng	Registration Number	51167

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	29164126
Application Number:	14715486
International Application Number:	
Confirmation Number:	1537
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/Brian Gonzalez
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	N3044.10002US21
Receipt Date:	09-MAY-2017
Filing Date:	18-MAY-2015
Time Stamp:	20:07:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	2017-05-09_IDS_N3044-10002US21.pdf	1036742 3a78a1fd4f95f71e21aff3bee01c259edaf01e2c	no	7

Warnings:

Information:					
2	Non Patent Literature	Business-Wire_2003-03-24.pdf	92377 2f6aa175fa7a3bf63e5f8bcf570bc5d7e333a588	no	2
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3	Non Patent Literature	Business-Wire_2003-09-16.pdf	106148 ab47c7e4bf24490009948905ad2fe2f320e44e02	no	3
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Information:					
4	Non Patent Literature	95000578-95000579-95001339_Decision-on-Appeal_2016-05-31.pdf	9033867 9e492823a033911b76f221235f306ca191a449a4	no	106
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5	Non Patent Literature	95001758_Decision-on-Appeal_2016-05-31.pdf	3959423 350b49eed3ff219f2589999f999744e8cf635758	no	49
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6	Non Patent Literature	95000546-95000577_Decision-on-Appeal_2015-02-25.pdf	1009092 94c281b3cb8729037255882a8747607f1f0e48a5	no	25
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7	Non Patent Literature	95000546-95000577_Decision-on-Request-for-Rehearing_2015-08-27.pdf	126675 df75627ba755ac2bfde7529c927bc364a35373da	no	5
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8	Non Patent Literature	Smith_Kentron-Qand-A.pdf	365071 80a0ea42852d700e4463ad6a0207a64b5614e5f2	no	4
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9	Non Patent Literature	Weste_3rd-Edition.pdf	929185 6c6eb9702fb07bdf85c3d42e167c91703f14b23c	no	4
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10	Non Patent Literature	weste_4th-Edition.pdf	658808 40df392684a4b1f9b421a723992192454e6aa31a	no	4
Warnings:					
Information:					
11	Non Patent Literature	95001339-95000578-95000579_Action-Closing-Prosecution_2014-03-21.pdf	3273640 6f7a1294ae21867fbc61b1fcf5a74cec2234de14	no	92
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12	Non Patent Literature	95001381_Decision-on-Appeal_2014-01-16.pdf	925588 019c3ad465a09f6bfd24b83a8c24708f4a1a38d1	no	24
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13	Non Patent Literature	95001337_2014-02-18_Requester-Request-for-Rehearing-after-Board-Decision.pdf	769384 28e1893af091d7e5a9b99d540cf8d3969de7a57d	no	11
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14	Non Patent Literature	95001337_2014-03-18_Affidavit-traversing-rejectns-or-objectns-rule132.pdf	6026161 e33f08c3aedfe9045b56060aee7dac9e9a5adc0d	no	60
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15	Non Patent Literature	95001337_2014-03-18_Patent-Owner-Response-after-Board-Decision.pdf	1730765 79b31e49ade1bffca44f55270581597f60fca0f7	no	38
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16	Non Patent Literature	95001337_2014-03-19_Affidavit-traversing-rejectns-or-objectns-rule-132.pdf	6026175 1fe5e3195ca478cf8fd9a1140e0219a1a5cba07a	no	60
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17	Non Patent Literature	95001337_2014-03-19_Patent-Owner-Comments-on-Req-for-Rehearing-timely.pdf	322120 0804d27f82766fa9a65161f289bf1f468b20f1ce	no	7
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18	Non Patent Literature	95001337_2014-03-19_Patent-Owner-Response-after-Board-Decision.pdf	1738617 cce3f0fab20754eca914ada5bb16b2e57515eedc	no	38
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21	Non Patent Literature	95001337_2014-06-26_New-Board-of-Appeals-Decision-after-Board-Decision-with-New-Ground.pdf	322737 794c278753c51774758fc3d535997251f7d10906	no	9
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26	Non Patent Literature	95001337_2015-06-15_Examiners-Determination-on-Patent-Owner.pdf	402856 2b6e12c58eb0e3189337d3520f816111030e9290	no	13
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27	Non Patent Literature	95001337_2015-09-11_Examiners-Determination-on-Patent-Owner.pdf	470102 c0c964bfd8f6909a527160afb27b861f5b38f2c6	no	15
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28	Non Patent Literature	95001337_2015-10-14_Affidavit-traversing-rejectns-or-objectns-rule-132-26Pages.pdf	1378921 7d0b69262e37d99687297b141663580692558741	no	26
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30	Non Patent Literature	95001337_2015-10-14_Patent-Owner-Comments-on-Examiners-Determination-after-Board-Decision.pdf	768885 ce8d35aa57da84edf53ac8c3b4f11685940dc2f4	no	18
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33	Non Patent Literature	95001337_2016-11-22_Other-Reference-Patent-App-Search-documents.pdf	36548 bca4e3f949e24f1666697681d5c3110f3132da59	no	2
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34	Non Patent Literature	95001337_2016-11-22_Petition-under-Rule-41-3-to-Chief-Admin-Patent-Judge.pdf	699941 8e27deae1c5a55a73d020bb1c85a9e5d4e6696b9	no	17
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		Total Files Size (in bytes):	67968295		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 05/11/2017

Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

EXAMINER	
BANSAL, GURTEJ	
ART UNIT	PAPER NUMBER
2139	

DATE MAILED: 05/11/2017

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/715,486	05/18/2015	Jeffrey C. Solomon	N3044.10002US21	1537

TITLE OF INVENTION: MEMORY MODULE WITH DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	08/11/2017

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

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II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Petitioners
Ex. 1057, p. 275

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 05/11/2017
Jamie J. Zheng, Ph.D Esq.
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Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/715,486	05/18/2015	Jeffrey C. Solomon	N3044.10002US21	1537

TITLE OF INVENTION: MEMORY MODULE WITH DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	08/11/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
BANSAL, GURTEJ	2139	711-105000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Petitioners
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/715,486	05/18/2015	Jeffrey C. Solomon	N3044.10002US21	1537

79141 7590 05/11/2017

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EXAMINER	
BANSAL, GURTEJ	

ART UNIT	PAPER NUMBER
2139	

DATE MAILED: 05/11/2017

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice Requiring Inventor's Oath or Declaration	Application No. 14/715,486	Applicant(s) Jeffrey C. Solomon	
	Examiner BANSAL, GURTEJ	Art Unit 2139	

This notice is an attachment to the Notice of Allowability (PTOL-37), or the Notice of Allowability For A Design Application (PTOL-37D).

An inventor's oath or declaration in compliance with 37 CFR 1.63 or 1.64 executed by or with respect to each inventor has not yet been submitted.

An oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each inventor (for any inventor for which a compliant oath, declaration, or substitute statement has not yet been submitted) MUST be filed no later than the date on which the issue fee is paid. See 35 U.S.C. 115(f). Failure to timely comply will result in ABANDONMENT of this application.

A properly executed inventor's oath to declaration has not been received for the following inventor(s):

If applicant previously filed one or more oaths, declarations, or substitute statements, applicant may have received an informational notice regarding deficiencies therein.

The following deficiencies are noted:

INFORMAL ACTION PROBLEMS

- A properly executed inventor's oath or declaration has not been received for the following inventor(s): **Jeffrey C. Solomon** and **Jayesh R. Bhakta**.
  Applicant may submit the inventor's oath or declaration at any time before the Notice of Allowance and Fee(s) Due, PTOL-85, is mailed.

Questions relating to this Notice should be directed to the Application Assistance Unit at 571-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	14/715,486	SOLOMON ET AL.	
	Examiner	Art Unit	
	GURTEJ BANSAL	2139	

All participants (applicant, applicant's representative, PTO personnel):

(1) *GURTEJ BANSAL*. (3)_____.

(2) *JAMIE ZHENG*. (4)_____.

Date of Interview: *27 April 2017*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☒102 ☒103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1*.

Identification of prior art discussed: *Applicant cited prior art in IDS*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Examiner and Applicant discussed the state of the prior art with respect to the breadth of the claims. Examiner suggested amendments to the claims which would clarify the language of the claims and distinguish the claims from the cited prior art. Applicant agreed with the amendments and authorized the Examiner to make the necessary amendments via an Examiner's amendment to claims the claims in condition for allowance.

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	

Notice of Allowability	Application No. 14/715,486	Applicant(s) SOLOMON ET AL.	
	Examiner GURTEJ BANSAL	Art Unit 2139	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Examiner interview dated 04/27/2017*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-18 and 22-29*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date See Continuation Sheet
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20170430* .
5. ☒ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

Continuation of Attachment(s) 2. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date: 12/04/2015;02/18/2016;02/19/2016;02/19/2016; 02/19/2016;02/19/2016; 02/19/2016; 02/19/2016; 02/19/2016; 02/19/2016; 02/19/2016; 02/22/2016; 06/30/2016; 01/24/2017.

Petitioners
Ex. 1057, p. 282

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in an interview with Jamie Zheng on April 27, 2017.

The application has been amended as follows:

IN THE CLAIMS

1. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a data bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank, wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command; and

a buffer coupled between the at least one first memory integrated circuit and the data bus, and between the at least one second memory integrated circuit and the data bus, wherein the buffer ~~couples~~ is configured in response to the first memory command to provide a first data path between the at least one first memory integrated circuit ~~to~~ and the data bus ~~and isolates the at least one second memory integrated circuit from the data bus~~ while the memory module is receiving or outputting the first data burst in response to the first memory command, and wherein the buffer is configured in response to the second memory command to provide a second data path between ~~couples~~ the at least one second memory integrated circuit ~~to~~ and the data bus ~~and isolates the at least one first memory integrated circuit from the data bus~~ while the memory module is receiving or outputting the second data burst in response to the second memory command, the second data path being different from the first data path.

2. (Original) The memory module of claim 1, wherein the buffer isolates both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the data bus when the memory module is not being accessed by the memory controller.

3. (Original) The memory module of claim 1, wherein the first memory command includes at least one first chip select signal and the second memory command includes at least one second chip select signal that is the same as the at least one first chip select signal.

4. (Original) The memory module of claim 3, wherein the memory module produces at least third and fourth chip select signals in response to the first memory command, the third chip select signal being provided to the at least one first memory integrated circuit and having an active value to select the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the fourth chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals.

5. (Original) The memory module of claim 4, wherein the memory module produces at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an

active value to select the at least one second memory integrated circuit to receive or output data signals in response to the second memory command.

6. (Currently Amended) The memory module of claim 1, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the memory module outputs the first data burst together with a first burst of data strobes in response to the first read command, wherein memory module outputs the second data burst together with a second burst of data strobes in response to the second read command, wherein the second data burst follows the first data burst on the data bus, and wherein the buffer prevents the first burst of data strobes and the second burst of data strobes from colliding with each other.

7. (Original) The memory module of claim 6, wherein each of the first burst of data strobes and the second burst of data strobes includes a pre-amble interval and a post-amble interval, and wherein the buffer combines the first burst of data strobes and the second burst of data strobes into a combined burst of data strobes that does not include the post-amble interval of the first burst of data strobes and the pre-amble interval of the second burst of data strobes.

8. (Currently Amended) The memory module of claim 1, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.

9. (Currently Amended) The memory module of claim 1, further comprising an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits.

10. (Currently Amended) The memory module of claim 1, ~~wherein the memory commands further includes a third memory command, the third memory command being one of a refresh command or a precharge command, and~~ wherein the buffer couples both the at least one first memory integrated circuit and the at least one second memory integrated circuit to the data bus in response to the memory module receiving a refresh command or a precharge command ~~in response to the third memory command~~.

11. (Currently Amended) A method of operating a memory module coupled to a memory controller via a memory bus including a control/address (C/A) bus and a data bus, the memory module comprising memory integrated circuits arranged in ranks and mounted on a printed circuit board having a plurality of edge connections coupled to the memory bus, the memory integrated circuits including at least one first memory integrated circuit in a first rank and at least one second memory integrated circuit in a second rank, the method comprising:

receiving from the memory controller a first set of input C/A signals associated with a first memory command via the C/A bus, the first memory command to cause the memory module to receive or output a first data burst;

generating a first set of output C/A signals in response to the first set of input C/A signals, the first set of output C/A signals causing the first rank ~~at least one first memory integrated circuit~~ to receive or output the first data burst;

receiving from the memory controller a second set of input control/address signals associated with a second memory command via the C/A bus, the second memory command to cause the memory module to receive or output a second data burst;

generating a second set of output C/A signals in response to the second set of input C/A signals, the second set of output C/A signals causing the second rank ~~at least one second memory integrated circuit~~ to receive or output the second data burst;

~~coupling~~ in response to the first memory command, providing a first data path between the at least one first memory integrated circuit ~~to~~ and the data bus ~~and isolating the at least one second memory integrated circuit from the data bus~~ while the memory module is receiving or outputting the first data burst in response to the first memory command; and

~~coupling~~ in response to the second memory command, providing a second data path between the at least one second memory integrated circuit ~~to~~ and the data bus ~~and isolating the at least one first memory integrated circuit from the data bus~~ while the memory module is receiving or outputting the second data burst in response to the second memory command, the second data path being different from the first data path.

12. (Original) The method of claim 11, further comprising isolating the at least one first memory integrated circuit and the at least one second memory integrated

circuit from the data bus when the memory module is not being accessed by the memory system.

13. (Original) The method of claim 11, wherein the first set of input C/A signals include at least one input chip-select signal, the method further comprising generating a greater number of output chip-select signals than the at least one input chip-select signal, the greater number of output chip-select signals including a first chip select signal and a second chip select signal, the first chip-select signal being provided to at least one first memory integrated circuit and having an active value to select the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the second chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals.

14. (Original) The method of claim 11, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the memory module outputs the first data burst together with a first burst of data strobes in response to the first read command, wherein the memory module outputs the second data burst together with a second burst of data strobes in response to the second read command, wherein the second data burst follows the first data burst on the data bus, the method further comprising combining the first burst of data strobes and the second burst of data strobes to form a third burst of data strobes on the data bus.

15. (Original) The method of claim 14, wherein each of the first burst of data strobes and the second burst of data strobes includes a pre-amble interval and a post-amble interval, and wherein the third burst of data strobes does not include the post-amble interval of the first burst of data strobes and the pre-amble interval of the second burst of data strobes.

16. (Original) The method of claim 11, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of the memory integrated circuits.

17. (Original) The method of claim 11, further comprising reporting an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more cycle than an actual operational CAS latency of the memory integrated circuits.

18. (Currently Amended) The method of claim 11 ~~1~~, further comprising:

receiving from the memory controller a third set of input C/A signals associated with a third memory command via the C/A bus, the third memory command being one of a refresh or precharge command;

generating a third set of output C/A signals in response to the third set of input C/A signals, the third set of output C/A signals causing the at least one first memory integrated circuit and the at least one second memory integrated circuit to perform one of a refresh operation and a pre-charge operation; and

in response to the third memory command, coupling both the at least one first memory integrated circuit and the at least one second memory integrated circuit to the data bus.

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (New) The memory module of claim 1, wherein the buffer includes circuit components common to both the first data path and the second data path, and wherein at least one of the circuit components is configured to provide the first data path or the second data path depending on whether the first rank or the second rank is selected to communicate data with the memory controller.

23. (New) The memory module of claim 22, further comprising a logic element that configures the at least one of the circuit components to provide the first data path in response to the first memory command, and that configures the at least one circuit components to provide the second data path in response to the second memory command.

24. (New) The memory module of claim 22, wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits.

25. (New) The memory module of claim 24, wherein the logic element is configured to determine a latency value, and wherein the first data path and the second data path are provided in accordance with the latency value.

26. (New) The memory module of claim 22, wherein the buffer comprises combinatorial logic, registers, and logic pipelines that are configured to provide the first data path in response to the first memory command and to provide the second data path in response to the second memory command.

27. (New) The method of claim 11, wherein the first data path and the second data path have common circuit components, and wherein at least one of the common circuit components is configured differently to provide the first data path or the second data path depending on whether the first rank or the second rank is caused to communicate data with the memory controller.

28. (New) The method of claim 27, wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits.

29. (New) The memory module of claim 28, further comprising determining a latency value, wherein the first data path and the second data path are provided in accordance with the latency value.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GURTEJ BANSAL whose telephone number is (571)270-5588. The examiner can normally be reached on Monday - Friday, 7:30 a.m. - 5:00 p.m., EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571)272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GURTEJ BANSAL
Primary Examiner
Art Unit 2139

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	14/715,486	SOLOMON ET AL.	
	Examiner	Art Unit	
	GURTEJ BANSAL	2139	

All participants (applicant, applicant's representative, PTO personnel):

(1) *GURTEJ BANSAL*. (3)_____.

(2) *JAMIE ZHENG*. (4)_____.

Date of Interview: *27 April 2017*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☒102 ☒103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1*.

Identification of prior art discussed: *Applicant cited prior art in IDS*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Examiner and Applicant discussed the state of the prior art with respect to the breadth of the claims. Examiner suggested amendments to the claims which would clarify the language of the claims and distinguish the claims from the cited prior art. Applicant agreed with the amendments and authorized the Examiner to make the necessary amendments via an Examiner's amendment to claims the claims in condition for allowance.

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	2

Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	5345412	09-06-1994	Shiratsuchi	
	2.	5537584	07-16-1996	Miyai et al.	
	3.	5617559	04-01-1997	Le et al.	
	4.	5649159	07-15-1997	Le et al.	
	5.	5717851	02-10-1998	Yishay et al.	
	6.	5724604	03-03-1998	Moyer	
	7.	5729716	05-17-1998	Lee et al.	
	8.	5784705	07-21-1998	Leung, Wingyu	
	9.	5802541	09-01-1998	Reed	
	10.	5973392	10-26-1999	Senba et al.	
	11.	6173357	01-09-2011	Ju	
	12.	6260127	07-10-2001	Olarig et al.	
	13.	6446158	09-03-2002	Karabatsos	
	14.	6553449	04-22-2003	Dodd et al.	
	15.	6618791	09-09-2003	Dodd et al.	
	16.	6717855	04-06-2004	Underwood	
	17.	6788592	09-07-2004	Nakata et al.	
	18.	6948084	09-20-2005	Manapat et al	
	19.	7130308	10-31-2006	Haddock et al.	
	20.	7133960	11-07-2006	Thompson et al.	
	21.	7379361	05-27-2008	Co et al.	
	22.	20050010737	01-13-2005	Ware et al.	
	23.	20070293094	12-20-2007	Aekins, Robert A.	

NON PATENT LITERATURE DOCUMENTS

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	24.	Anonymous. (December 1996). "Applications Note: Understanding DRAM Operation," IBM, 10 pages.	
	25.	Behrens, S. "HP Printer Memory Explained", The ZonkPage, Last Updated 01-21-2004. Accessed 02-10-2013, Retrieved from the Internet: URL <http://warshaft.com/hpmem.htm>. 7pp.	
	26.	Non-Final Office Action, U.S. Pat. App. 13/412,243, January 2, 2014, 20 pages	
	27.	Non-Final Office Action, U.S. Pat. App. 12/761,179, September 13, 2012, 20 pages	
	28.	Non-final office action, U.S. Patent Application No. 13/288,850, October 14, 2013, 24 pages	
	29.	Non-final office action, U.S. Patent Application No. 13/411,344, December 31, 2013, 28 pages	

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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	14/715,486
				Filing Date	May 18, 2015
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2139
				Examiner Name	Unknown
Sheet	2	of	2	Attorney Docket Number	NETL.018P2C8

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	30.	Non-final office action, U.S. Patent Application No. 13/473,413, November 17, 2011, 46 pages	
	31.	Response to non-final office action dated September 13, 2012 for U.S. Patent Application No. 12/761,179, filed March 13, 2013, 16 pages	
	32.	Response to non-final office action dated October 14, 2013 for U.S. Patent Application No. 13/288,850, filed January 14, 2014, 15 pages	
	33.	Response to non-final office action dated 12/31/2013 for U.S. Patent Application No. 13/411,344, filed March 31, 2014, 12 pages	
	34.	Patent Owner's Response to Office Action mailed November 13, 2012 for Reexamination Control Nos.95/000,578; 95/000,579, and 95/001,339, filed January 14, 2013, 96 pages.	
	35.	Patent Owner's Response to Office Action mailed December 19, 2012 for Reexamination Control No. 95/001,758, filed March 19, 2013, 61 pages	
	36.	Patent Owner's Response to Office Action mailed September 26, 2013 for Reexamination Control No. 95/001,758, filed November 26, 2013, 85 pages	
	37.	Third Party Requester's Comments after Non-Final Action mailed September 26, 2013 for Reexamination Control No. 95/001,758, filed December 26, 2013,	
	38.	Reexamination Control No. 95/002,399, filed April 25, 2013, and its entire file history	
	39.	Patent Owner's Appeal Brief for Reexamination Control Nos. 95/000,546 and 95/000,577, filed October 2, 2013, 46 pages	
	40.	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control No.95/001/337, mailed January 16, 2014, 30 pages	
	41.	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control No.95/001/381, mailed January 16, 2014, 24 pages	
	42.	Action Closing Prosecution mailed March 27, 2014 for Reexamination Control No. 95/001,758, filed September 14, 2011, 40 pages	
	43.	Action Closing Prosecution mailed March 27, 2014 for Reexamination Control No. 95/001,339, filed June 8, 2010, 106 pages	
	44.	Notice of Allowance, U.S. Pat. App. 12/761,179, July 11, 2013, 37 pages	
	45.	Notice of Allowance, U.S. Pat. App. 12/504,131, February 12, 2013, 52 pages	

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	1.	6011710	01-04-2000	Wiggers	
	2.	20010008006	07-12-2001	Klein	
	3.	20050257109	11-17-2005	Averbuj	
	4.	20070070669	03-29-2007	Tsern	

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	5.	Petition for Inter Partes Review filed on 6/24/2014 for U.S. Patent No. 8,516,185, IPR Case Number IPR2014-01029, and all associated documents including cited references and expert declarations, available at https://ptabtrials.uspto.gov	
	6.	Petition for Inter Partes Review filed on 6/22/2014 for U.S. Patent No. 7,881,150, IPR Case Number IPR2014-00882 and IPR Case Number IPR2014-01011, and all associated documents including cited references and expert declarations, available at https://ptabtrials.uspto.gov	
	7.	Petition for Inter Partes Review filed on 6/24/2014 for U.S. Patent No. 8,081,536, IPR Case Number IPR2014-00883, and all associated documents including cited references and expert declarations, available at https://ptabtrials.uspto.gov	
	8.	Altera, ACEX iK, Programmable Logic Device Family, Data Sheet, May 2003, Ver 3.4	
	9.	Horowitz, "The Art of Electronics," Cambridge Univ. Press, 1989, selected pages	
	10.	Jacob, Bruce L.; "Synchronous DRAM Architectures, Organizations, and Alternative Technologies". University of Maryland, Dec. 10, 2002.	
	11.	JEDEC Standard No. 21-C Section 4.5.7, 168 Pin Registered SDRAM DIMM Family, Release 7	
	12.	JEDEC 21-C, Section 4.6.1, 278 Pin Buffered SDRAM DIMM Family	
	13.	JEDEC Standard No. 21-C Section 4.1.2.5, Appendix E, "Specific PD's for Synchronous DRAM (SDRAM)," pp. 1-25,	

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First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

Sheet 1 of 3

US PATENT DOCUMENTS

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	1.	6381140	04-30-2002	Liao, Sheng-Chi	
	2.	7254036	08-07-2007	Pauley et al.	

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Examiner Initials *	Cite No. [1]	Foreign Patent Document	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [6]
	3.	WO99/30240	06-17-1999	Intel Corporation		

NON PATENT LITERATURE DOCUMENTS

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	4.	Inter Partes Review Case No. 2014-00882, Patent Owner Response, filed May 8, 2015	
	5.	Inter Partes Review Case No. 2014-00882, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015	
	6.	Inter Partes Review Case No. 2014-00882, Petitioner's Request for Oral Argument, filed July 1, 2015	
	7.	Inter Partes Review Case No. 2014-00882, Patent Owner's Request for Oral Argument, filed July 3, 2015	
	8.	Inter Partes Review Case No. 2014-00882, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015	
	9.	Inter Partes Review Case No. 2014-00882, Record of Oral Hearing, filed November 16, 2015	
	10.	Inter Partes Review Case No. 2014-00882, Final Written Decision 35 USC 318 and 37 CFR 42.73, filed December 14, 2015	
	11.	Inter Partes Review Case No. 2014-00882, Netlist Inc.'s Notice of Appeal, filed February 10, 2016	
	12.	Inter Partes Review Case No. 2014-00882, Exhibit 1022, 'Professor Carl Sechen Deposition Transcript,' filed June,19,2015	
	13.	Inter Partes Review Case No. 2014-00882, Exhibit 1023, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015	
	14.	Inter Partes Review Case No. 2014-00882, Exhibit 2002, 'Declaration of Professor Carl Sechen,' filed May 8,2015	
	15.	Inter Partes Review Case No. 2014-00882, Exhibit 2003, 'Transcript of Videotaped Deposition of Srinivasan Jagannathan, Ph. D,' filed May 8,2015	

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	16.	Microsoft Computer Dictionary, Fifth Edition, Microsoft Press, p. 334, 2002	
	17.	Jacob, Bruce, et al. "Memory Systems - Cache, DRAM, Disk," Elsevier Inc. 2008, Chapters 7 and 10	
	18.	U.S. District Court Northern District of California, Case No. 4.13-cn-05889-YGR, Netlist Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Joint Claim Construction and Prehearing Statement Pursuant to Patent L. T. 4-3, filed August 27, 2014, in 28 pages	
	19.	Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 349-411	
	20.	Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 133-265	
	21.	Selected Entries in Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/view/Entry/175039?redirectedFrom=selectively#eid	
	22.	Web search results from the Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/search?searchType=dictionary&q=select&_searchBin=Search	
	23.	Inter Partes Review Case No. 2014-00883, Patent Owner Response, filed May 8, 2015	
	24.	Inter Partes Review Case No. 2014-00883, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015	
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	31.	Inter Partes Review Case No. 2014-00883, Exhibit 1025, 'Professor Carl Sechen Deposition Transcript,' filed June 19,2015	
	32.	Inter Partes Review Case No. 2014-00883, Exhibit 1026, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015	
	33.	Inter Partes Review Case No. 2014-01011, Patent Owner Response, filed May 8, 2015	
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				Examiner Name	Unknown
Sheet	3	of	3	Attorney Docket Number	NETL.018P2C8

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	36.	Inter Partes Review Case No. 2014-01011, Patent Owner's Request for Oral Hearing, filed July 3, 2015	
	37.	Inter Partes Review Case No. 2014-01011, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015	
	38.	Inter Partes Review Case No. 2014-01011, Record of Oral Hearing, filed November 16, 2015	
	39.	Inter Partes Review Case No. 2014-01011, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015	
	40.	Inter Partes Review Case No. 2014-01011, Netlist Inc.'s Notice of Appeal, filed February 10, 2016	
	41.	Inter Partes Review Case No. 2014-01011, Exhibit 1027, 'Professor Carl Sechen Deposition Transcript,' filed June 19,2015	
	42.	Inter Partes Review Case No. 2014-01011, Exhibit 1028, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015	

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14715486	SOLOMON ET AL.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

CPC						
Symbol					**Type**	**Version**
G06F		13	/	1673	F	2013-01-01
G11C		7	/	1072	I	2013-01-01
G11C		15	/	00	I	2013-01-01
G06F		13	/	4282	I	2013-01-01
G06F		13	/	4243	I	2013-01-01
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CPC Combination Sets							
Symbol				**Type**	**Set**	**Ranking**	**Version**
			/				
			/				

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 26	
/GURTEJ BANSAL/ Primary Examiner.Art Unit 2139 (Primary Examiner)	04/30/2017 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14715486	SOLOMON ET AL.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
		G	0	6	F	12 / 00 (2006.01.01)						
CROSS REFERENCE(S)												
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)											

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 26	
/GURTEJ BANSAL/ Primary Examiner.Art Unit 2139 (Primary Examiner)	04/30/2017 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14715486	SOLOMON ET AL.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	20	17												
2	2	21	18												
6	3		19												
7	4		20												
8	5		21												
9	6	11	22												
10	7	12	23												
3	8	14	24												
4	9	15	25												
5	10	13	26												
16	11	24	27												
17	12	25	28												
18	13	26	29												
22	14														
23	15														
19	16														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 26	
/GURTEJ BANSAL/ Primary Examiner.Art Unit 2139 (Primary Examiner)	04/30/2017 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	9041	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	US-PGPUB; USPAT	OR	OFF	2017/04/30 15:23
S1	3717	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2011/07/03 21:54
S2	75	365/189.2.ccls.	USPAT	OR	OFF	2011/07/03 21:54
S3	104	365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:27
S4	6392	abstract$3 with (DRAM DIMM memory)	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:40
S5	48	abstracted adj2 (DRAM DIMM memory)	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:40
S6	109	abstracted adj2 (DRAM DIMM memory) or aDRAM	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:42
S7	1	"7515453".pn.	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:00
S8	771	interface same (DDR2 and (DDR or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:17
S9	504	interface with (DDR2 and (DDR or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:18
S10	5	365/189.2.ccls. and (DDR2 and (DDR or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:19
S11	10	365/189.2.ccls. and (DDR and (DDR2 or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:24
S12	1	"20070088995".pn.	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:29
S13	241	CKE with precharge	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:48
S14	0	365/189.2.ccls and CKE with precharge	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:48
S15	111	CKE with precharge same power	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:48
S16	36	silent with alarm with clock	US-	OR	OFF	2011/07/05

			PGPUB; USPAT			21:54
S17	0	silent with alarm with clock and lark.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:54
S18	0	silent with alarm with clock and hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:54
S19	4	alarm with clock and hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:55
S20	0	julia-hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:58
S21	2	julia.in. and hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:59
S22	16	lark.as.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:00
S23	629	precharge same power and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:01
S24	3	precharge same power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:03
S25	1	self with refresh and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:08
S26	3	pre$1charge with power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:09
S27	11	pre$1chargesame power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:09
S28	3	pre$1charge same power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:09
S29	55	pre$1charge same power and CKE and DRAM same DDR same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:22
S30	59	pre$1charge same power and CKE and DRAM same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:25
S31	73	pre$1charge same power and CKE and DDR same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:26
S32	89	refresh same power and CKE and DDR same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:17
S33	10	365/189.2.ccls. and (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:27
S34	54	SPD and (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:29
S35	16	SPD same (pre$1charge refresh) and CKE	US-	OR	OFF	2011/07/06

			PGPUB; USPAT			00:29
S36	0	module with transmit same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:45
S37	19	memory with transmit same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:45
S38	23	configure same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:48
S39	14	configure with (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:48
S40	1	DDR with DRAM and tCKE with timing with memory	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:52
S41	273	intelligent adj3 (buffer or register)	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:01
S42	9	intelligent adj3 (buffer or register) and pre$charge	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:01
S43	298	SPD same2 (pre$1charge refresh)	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:03
S44	197	SPD same (pre$1charge refresh)	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:03
S45	59	SPD same2 (pre$1charge refresh) and DDR same DRAM	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:03
S46	38	SPD same (pre$1charge refresh) and DDR same DRAM	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:04
S47	3	SPD same (pre$1charge refresh) and DDR same DRAM and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:05
S48	59	SPD same2 (pre$1charge refresh) and DDR same DRAM	US-PGPUB; USPAT	OR	OFF	2011/07/06 10:59
S49	1	SPD same pre$1charge with power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:01
S50	25	SPD same self adj refresh	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:01
S51	0	SPD same self adj refresh and DDR	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:04
S52	2	SPD same self adj refresh and DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:04
S53	22	SPD same self adj refresh same power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:07
S54	2	SPD same self adj refresh and CKE	US-	OR	OFF	2011/07/06

			PGPUB; USPAT			11:24
S55	0	SPD same self adj refresh and tCKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:26
S56	0	SPD same pre$1charge and tCKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:27
S57	2617837	SPD swith power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:29
S58	578	SPD with power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:29
S59	16	SPD with power same (self adj refresh self$1refresh pre adj charge pre$charge)	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:30
S60	21	SPD same self adj refresh and (pre$1charge or pre adj charge)	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:37
S61	1	"20050246558".pn.	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:41
S62	2	SPD same power with management with mode	US-PGPUB; USPAT	OR	OFF	2011/07/06 12:40
S63	13	365/189.2.ccls. and CS	USPAT	OR	OFF	2011/07/06 12:55
S64	21	365/189.2.ccls. and CS	US-PGPUB; USPAT	OR	OFF	2011/07/06 12:55
S65	171	DIMM same CS	US-PGPUB; USPAT	OR	OFF	2011/07/06 13:00
S66	53	365/189.2.ccls. and (tRP tRCD TWL tRFC timing tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:34
S67	7	365/189.2.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:34
S68	1631	"365".clas. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S69	0	365/189.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S70	446	365/189.$.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S71	36	365/189.$.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR) and DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S72	1	365/189.$.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR) same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:37
S73	3	burst with plurality with DIMM	US-PGPUB;	OR	OFF	2011/07/06 14:43

			USPAT			
S74	0	burst with each with DIMM	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:44
S75	6	burst with multiple with DIMM	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:44
S76	6	burst with multiple with DIMM and read	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:46
S77	5	burst with multiple with DIMM same read	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:47
S78	11	burst with DIMMs same read	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:47
S79	0	365/189.2.ccls. and CKE with (high and low)	USPAT	OR	OFF	2011/07/06 16:19
S80	529	CKE with (high and low)	USPAT	OR	OFF	2011/07/06 16:20
S81	17	CKE with (high and low) and DDR2	USPAT	OR	OFF	2011/07/06 16:20
S82	0	365/189.2.ccls. and CKE with (high and low)	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:20
S83	44	CKE with (high and low) and DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:21
S84	87	CKE with (high and low) same pre$1charge	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:24
S85	0	CKE with (high and low) same pre$1charge same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:24
S86	0	CKE with (high and low) same self adj refresh same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:25
S87	0	CKE with ((high and low) or assert) same self adj refresh same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:25
S88	0	CKE with ((high and low) or assert) same pre$1fetch same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:25
S89	0	CKE with (high or low or assert) same pre$1fetch same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:26
S90	0	CKE with (high or low or assert) same pre$1fetch same2 SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:26
S91	2	CKE with (high or low or assert) same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:26
S92	10	SPD same2 CKE with (high or low or assert)	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:27
S93	1	"20090216936".pn.	US-	OR	OFF	2012/01/20

			PGPUB; USPAT			18:08
S94	1	"20090216939".pn.	US-PGPUB; USPAT	OR	OFF	2012/01/20 18:17
S95	152	buffer with DRAM with protocol	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:25
S96	152	buffer$3 with DRAM with protocol	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:37
S97	572	buffer with $1RAM with protocol	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:38
S98	1	"20030131160".pn.	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:47
S99	1729	buffer with $1RAM with (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:48
S100	626	buffer with DRAM with (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:48
S101	124	buffer with chip with DRAM with (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:51
S102	185	buffer near5 DRAM near5 (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:14
S103	499	buffer with DRAM with type	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:18
S104	51	buffer with DRAM with type with (multiple different tim$3 various)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:19
S105	224	buffer with DRAM with DDR	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:21
S106	3	buffer with DRAM with (timing signal) with adjust	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:32
S107	146	buffer with DRAM with (timing signal) with delay	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:32
S108	31	buffer with DRAM with (timing signal) with DDR$1	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:32
S109	70	buffer with DRAM with (timing signal protocol) and buffer with DDR$1 with (timing signal protocol)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:37
S110	118	buffer with DRAM with (timing signal protocol) and buffer with SDRAM with (timing signal protocol)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:48
S111	36	buffer with DRAM with SDRAM with interface	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:52
S112	48	buffer with DRAM with (SDRAM DDR2	US-	OR	OFF	2012/01/21

		DDR3) with interface	PGPUB; USPAT			00:52
S113	73	interface with buffer with DRAM with (DDR$1 SDRAM)	US-PGPUB; USPAT	OR	OFF	2012/01/21 02:03
S114	141	interface same buffer with DRAM with (DDR$1 SDRAM)	US-PGPUB; USPAT	OR	OFF	2012/01/21 02:10
S115	2	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/15 14:11
S116	64	DIMM with DRAM and CS with (DIMM DRAM) and buffer with (DIMM DRAM)	US-PGPUB; USPAT	OR	OFF	2013/01/15 14:12
S117	1	"5918229".pn.	US-PGPUB; USPAT	OR	OFF	2013/01/18 14:08
S118	1	"20060184942".pn.	US-PGPUB; USPAT	OR	OFF	2013/01/18 14:35
S119	130	(different multiple distinct) with file adj locking	US-PGPUB; USPAT	OR	OFF	2013/01/18 17:46
S120	0	abstracted with DIMM and DRAM	USPAT	OR	OFF	2013/01/21 13:21
S121	0	abstracted with DIMM	USPAT	OR	OFF	2013/01/21 13:21
S122	2	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 13:21
S123	56	US-5278796-$.DID. OR US-5282177-$.DID. OR US-5384745-$.DID. OR US-1241995-$.DID. OR US-5388265-$.DID. OR US-5467455-$.DID. OR US-5498886-$.DID. OR US-5598376-$.DID. OR US-5610864-$.DID. OR US-5675549-$.DID. OR US-5692202-$.DID. OR US-5706247-$.DID. OR US-5757703-$.DID. OR US-5949254-$.DID. OR US-6034916-$.DID. OR US-6034918-$.DID. OR US-6035365-$.DID. OR US-6330683-$.DID. OR US-6631086-$.DID. OR US-6754129-$.DID. OR US-6970968-$.DID. OR US-20030002262-$.DID. OR US-20040196732-$.DID. OR US-20050149662-$.DID. OR US-7172005-$.DID. OR US-20050259504-$.DID. OR US-20080025108-$.DID. OR US-20080025136-$.DID. OR US-5241266-$.DID. OR US-5843799-$.DID. OR US-5966727-$.DID. OR US-20060026484-$.DID. OR US-20080239858-$.DID. OR US-20080115006-$.DID. OR US-20070288686-$.DID. OR US-7120727-$.DID. OR US-7472220-$.DID. OR US-6317352-$.DID. OR US-6317381-$.DID. OR US-20010019509-$.DID. OR US-3800292-$.DID. OR US-4069452-$.DID. OR US-4323965-$.DID. OR US-4334307-$.DID. OR US-4345319-$.DID. OR US-	US-PGPUB; USPAT	OR	OFF	2013/01/21 17:23

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S137	31	DRAM with DIMM and DIMM with virtual$5	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:35
S138	43	DRAM with DIMM and CS with module	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:39
S139	43	virtual with DIMM and DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:49
S140	57	buffer with CS and DIMM with DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:16
S141	2	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:22
S142	37	virtual$5 near3 DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:22
S143	29	virtual$5 near3 DIMM and DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:22
S144	541	(plurality multiple) with DIMM with single	US-PGPUB; USPAT	OR	ON	2013/01/21 23:25
S145	200	(plurality multiple) near3 DIMM with single	US-PGPUB; USPAT	OR	ON	2013/01/21 23:25
S146	170	(plurality multiple) near3 DIMM with single and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/21 23:25
S147	132	logical with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/21 23:35
S148	112	logical with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/21 23:35
S149	334	(group) with DIMM and DRAM	US-PGPUB;	OR	ON	2013/01/22 00:47

			USPAT			
S150	55	emulat$3 with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/22 00:52
S151	71	virtual with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/22 09:39
S152	10	(plurality multiple) with virtual with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/22 09:40
S153	47	(plurality multiple) with (virtual logical emulat$3) with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/22 09:40
S154	1	"7133960".pn.	US-PGPUB; USPAT	OR	ON	2013/01/22 09:42
S155	17	rank with (appear$3) with DIMM	USPAT	OR	OFF	2013/01/30 13:21
S159	180	(virtual logical abstract$3) with DIMM	US-PGPUB; USPAT	OR	ON	2013/02/18 23:49
S160	22	(virtual logical abstract$3) adj DIMM	US-PGPUB; USPAT	OR	ON	2013/02/18 23:49
S161	344	(virtual logical abstract$3) adj RAM	US-PGPUB; USPAT	OR	ON	2013/02/19 00:01
S162	98	(virtual logical abstract$3) adj DRAM	US-PGPUB; USPAT	OR	ON	2013/02/19 00:01
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S170	105	(virtual logical abstract$3) adj DRAM	US-PGPUB; USPAT	OR	ON	2013/07/24 15:59
S171	60	emulat$3 with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/07/24 15:59

S172	4337	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/07/24 16:02
S173	3	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/07/24 16:04
S178	1054	buffer with data with CS	US-PGPUB; USPAT	OR	OFF	2017/04/26 15:45
S179	1637	buffer with DIMM	US-PGPUB; USPAT	OR	OFF	2017/04/26 15:49
S180	100	buffer and fan$4 with (rank dimm)	US-PGPUB; USPAT	OR	OFF	2017/04/26 16:14
S181	249	buffer same parallel with (rank dimm)	US-PGPUB; USPAT	OR	OFF	2017/04/26 16:26
S182	112	buffer same parallel with (ranks dimms)	US-PGPUB; USPAT	OR	OFF	2017/04/26 16:26
S183	60	daisy with chain with DIMM same buffer	US-PGPUB; USPAT	OR	OFF	2017/04/27 00:11

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	4964	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	USPAT	OR	OFF	2017/04/30 15:24
L3	6228	data.clm. adj path.clm.	USPAT	OR	OFF	2017/04/30 15:28
L4	120	L2 and L3	USPAT	OR	OFF	2017/04/30 15:28
L5	8	L2 and L3 and rank.clm.	USPAT	OR	OFF	2017/04/30 15:28
S156	4194	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/01/30 13:35
S157	1321	emulated.clm.	USPAT	OR	OFF	2013/01/30 13:45
S158	3	S156 and S157	USPAT	OR	OFF	2013/01/30 13:45
S163	4205	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/02/19 00:04
S164	1330	emulated.clm.	USPAT	OR	OFF	2013/02/19 00:04
S165	4205	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/02/19 00:04
S166	1330	emulated.clm.	USPAT	OR	OFF	2013/02/19 00:04
S167	3	S165 and S166	USPAT	OR	OFF	2013/02/19 00:04
S174	4343	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/07/24 16:04
S175	4343	711/5.ccls. 711/105.ccls. 711/167.ccls.	USPAT	OR	OFF	2013/07/24

		365/189.2.ccls.				16:06
S176	1399	emulated.clm.	USPAT	OR	OFF	2013/07/24 16:06
S177	4	S175 and S176	USPAT	OR	OFF	2013/07/24 16:06

4/30/2017 3:32:33 PM
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 17

Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	4218740	08-19-1980	MOTOROLA INC	
	2.	4249253	02-03-1981	Gentili et al.	
	3.	4368515	01-11-1983	Nielsen	
	4.	4392212	07-05-1983	Miyasaka et al.	
	5.	4571676	02-18-1986	Mantellina et al.	
	6.	4592011	05-27-1986	Mantellina et al.	
	7.	4633429	12-30-1986	Lewandowski et al.	
	8.	4670748	06-02-1987	Williams	
	9.	4706214	11-10-1987	Mitsubishi Denki Kabushiki Kaisha	
	10.	4866603	09-02-1989	Chiba	
	11.	4958322	09-18-1990	Kosugi et al.	
	12.	4961172	10-02-1990	Shubat et al.	
	13.	4961204	10-02-1990	Hitachi Ltd	
	14.	4980850	12-25-1990	Morgan	
	15.	5060188	10-22-1991	Zulian et al.	
	16.	5247643	09-21-1993	Shottan	
	17.	5272664	12-21-1993	Silicon Graphics Inc	
	18.	5345412	09-06-1994	Shiratsuchi	
	19.	5357478	10-18-1994	Mitsubishi Electric Corp	
	20.	5388072	02-07-1995	IBM	
	21.	5392252	02-21-1995	Visi Technology Inc	
	22.	5426753	06-20-1995	Moon	
	23.	5463590	10-31-1995	Watanabe	
	24.	5483497	01-09-1996	Mochizuki et al.	
	25.	5485589	01-16-1996	Dell Usa Lp	
	26.	5495435	02-27-1996	Sugahara	
	27.	5513135	04-30-1996	Dell et al.	
	28.	5532954	07-02-1996	Bechtolsheim et al.	
	29.	5541448	07-30-1996	Carpenter	
	30.	5572691	11-05-1996	Koudmani	
	31.	5581498	12-03-1996	Ludwig et al.	
	32.	5590071	12-31-1996	Kolor et al.	
	33.	5602999	02-11-1997	Hyatt; Gilbert P.	

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Sheet 2 of 17

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Application Number	14/715,486
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First Named Inventor	Jayesh R. Bhakta
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Examiner Name	Unknown
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	34.	5638534	06-10-1997	Samsung Electronics Co Ltd	
	35.	5655153	08-05-1997	EMC CORP	
	36.	5699542	12-16-1997	Mehta et al.	
	37.	5702984	12-30-1997	Bertin et al.	
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	39.	5745914	04-28-1998	Connolly et al.	
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	41.	5784705	07-21-1998	Leung, Wingyu	
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	43.	5805520	09-08-1998	Anglada et al.	
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	45.	5909388	06-01-1999	Siemens Ag	
	46.	5926827	07-20-1999	Dell et al.	
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	48.	5953215	09-14-1999	Karabatsos, Chris	
	49.	5953280	09-14-1999	Watsui	
	50.	5958025	09-28-1999	Nippon Electric Co	
	51.	5959930	09-28-1999	Sakurai	
	52.	5963464	10-05-1999	Dell et al.	
	53.	5966736	10-12-1999	Gittinger et al.	
	54.	5974493	10-26-1999	Mitsubishi Electric Corp	
	55.	6018787	01-25-2000	Ip	
	56.	6044032	03-28-2000	Li	
	57.	6070217	05-30-2000	Connolly et al.	
	58.	6070227	05-30-2000	Rokicki	
	59.	6097652	08-01-2000	Roh	
	60.	6108745	08-22-2000	Gupta et al.	
	61.	6115278	09-05-2000	Deneroff et al.	
	62.	6134638	10-17-2000	Olarig et al.	
	63.	6151271	11-21-2000	Lee	
	64.	6154418	11-28-2000	Li	
	65.	6154419	11-28-2000	Shakkarwar	
	66.	6185654	02-06-2001	Van Doren	

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Sheet 3 of 17

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First Named Inventor	Jayesh R. Bhakta
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Examiner Name	Unknown
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Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Sheet 4 of 17

Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

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Sheet 5 of 17

Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

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Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

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Sheet 7 of 17

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Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

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Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

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Sheet 9 of 17

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Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

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				Filing Date	May 18, 2015
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2827
				Examiner Name	Unknown
Sheet	10	of	17	Attorney Docket Number	NETL.018P2C8

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				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2827
				Examiner Name	Unknown
Sheet	11	of	17	Attorney Docket Number	NETL.018P2C8

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				First Named Inventor	Jayesh R. Bhakta
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				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2827
				Examiner Name	Unknown
Sheet	15	of	17	Attorney Docket Number	NETL.018P2C8

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
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	359.	Non-Final Action mailed August 27, 2010, for Control No. 95/000,546, filed May 11, 2010, 16 pages.	
	360.	Non-Final Action mailed September 8, 2010, for Control No. 95/001,381, filed June 9, 2010, 17 pages.	
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	362.	Non-Final Action mailed June 15, 2011, for Control No. 95/001,381, filed June 9, 2010, 33 pages.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 16 of 17

Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

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	363.	Non-Final Action mailed September 27, 2011, for Control No. 95/001,337, filed April 19, 2010, 19 pages.	
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	369.	Order Granting Request for Inter Partes Reexamination mailed August 27, 2010, for Control No. 95/001,337, filed April 19, 2010, 21 pages.	
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	371.	Order Granting Request for Inter Partes Reexamination mailed September 8, 2010, for Control No. 95/000,381, filed June 9, 2010, 21 pages.	
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Substitute for form 1449/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** *(Use as many sheets as necessary)*				***Complete if Known***	
				Application Number	14/715,486
				Filing Date	May 18, 2015
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2827
				Examiner Name	Unknown
Sheet	17	of	17	Attorney Docket Number	NETL.018P2C8

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	381.	US District Court Civil Docket; Google Inc. v. Netlist Inc.; 4:08cv04144; Date filed Aug. 29, 2008.	
	382.	US District Court Civil Docket; Netlist Inc. v. Inphi Corporation; 2:09cv6900; Date filed Sep. 22, 2009. cited by other.	
	383.	Written Opinion for International Application No. PCT/US2010/040826, date of mailing October 24, 2011 (NETL.048VPC) in 7 pages.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	14/715,486
				Filing Date	May 18, 2015
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2139
				Examiner Name	Unknown
Sheet	1	of	1	Attorney Docket Number	NETL.018P2C8

US PATENT DOCUMENTS					
Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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	2	2004/0098528	05-2004	Janzen, Jefferey W.	
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	4	Non-Final Office Action, dated January 2, 2014, for U.S. Pat. App. No. 13/287,042 filed November 1, 2011, 42 pages	
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				Examiner Name	Unknown
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	2.	20080162790	07-03-2008	Im, Jeon-Taek	
	3.	20090103387	04-23-2009	Shau, Jeng-Jye	

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	4.	JPH10092169 A	9/9/97	Toshiba Corp.		
	5.	JP2000311485 A	10/13/00	Fujitsu Ltd.		

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	6.	Office Action mailed April 2, 2014, for Japanese Patent Application No. 2012-520662 and English translation thereof, 7 pages	

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Sheet 1 of 1

Complete if Known	
Application Number	13/971,231
Filing Date	August 20, 2013
First Named Inventor	Jayesh R. Bhakta
Art Unit	2189
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	NETL.018P2C7

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	4.	Inter Partes Review Case No. IPR2014-00882, Corrected Petition for Inter Partes Review of U.S. Patent No. 7,881,150, filed on July 8, 2014.	
	5.	Inter Partes Review Case No. IPR2014-00882, Exhibit 1007 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on June 22, 2014.	
	6.	Inter Partes Review Case No. IPR2014-00883, Corrected Petition for Inter Partes Review of U.S. Patent No. 8,081,536, filed on July 8, 2014.	
	7.	Inter Partes Review Case No. IPR2014-00883, Exhibit 1011 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on June 21, 2014.	
	8.	Inter Partes Review Case No. IPR2014-01011, Corrected Petition for Inter Partes Review of U.S. Patent No. 7,881,150, filed on July 8, 2014.	
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	12.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.,* Smart Storage Systems, Inc.'s Invalidity Contentions, dated June 6, 2014	
	13.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.,* Exhibits F.1-F.5 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	14.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.,* Exhibits G.1-G.6 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	15.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.,* Exhibit H to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	

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Sheet	1	of	3

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	2.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner Response to Petition, filed February 22, 2016	
	3.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Objections to Evidence, filed February 29, 2016	
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	5.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner Request for Oral Argument, filed June 2, 2016	
	6.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER MOTION FOR OBSERVATIONS, filed June 2, 2016	
	7.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016	
	8.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, ORDER Trial Hearing, filed June 8, 2016	
	9.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016	
	10.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Response to Motion for Observations, filed June 10, 2016	
	11.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Response to Netlist's Submission, filed June 13, 2016	
	12.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's Objections to Petitioner's Demonstrative Exhibits, filed June 23, 2016	

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Sheet	2	of	3

Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	13.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's Demonstrative Exhibits, filed June 24, 2016	
	14.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Updated Exhibit List, filed June 24, 2016	
	15.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016	
	16.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, May 10, 2016 Deposition of Carl Sechen, filed May 19, 2016	
	17.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Demonstrative Exhibits, filed June 24, 2016	
	18.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016	
	19.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2002, "Videotaped Deposition of Srinivasan Jagannathan, Ph.D on February 12, 2016," filed February 22, 2016	
	20.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2003, "Videotaped Deposition of Srinivasan Jagannathan, Ph.D on April 20, 2015," filed February 22, 2016	
	21.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2007, "Deposition of Dr. Srinivasan Jagannathan on May 25, 2016," filed June 2, 2016	
	22.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner Response to Petition, filed February 22, 2016	
	23.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Objections to Evidence, filed February 29, 2016	
	24.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Reply, filed May 19, 2016	
	25.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner Request for Oral Argument, filed June 2, 2016	
	26.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, PATENT OWNER MOTION FOR OBSERVATIONS, filed June 2, 2016	

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	27.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016	
	28.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner's SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016	
	29.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Response to Motion for Observations, filed June 10, 2016	
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	33.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Updated Exhibit List, filed June 24, 2016	
	34.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016	
	35.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016	

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Dual-port **buffer**-to-**memory** interface
JB Halbert, JM Dodd, C Lam, RM Bonella - US Patent 6,742,098, 2004 - Google Patents
... be written separately to **memory** when it arrives by splitting each **rank** of **memory** in ... Oct 31, 2000, Texas Instruments Incorporated, **Memory** Interface supporting access to **memories** using different ... Method and system for terminating write commands in a hub-based **memory** system. ...
Cited by 228 Related articles All 2 versions Cite Save

3D-stacked **memory** architectures for multi-core processors
GH Loh - Computer Architecture, 2008. ISCA'08. 35th ..., 2008 - ieeexplore.ieee.org
... of bitcells (c). On a DRAM read, bits from the physical address select the **rank**, bank and ... of the required latencies, the topol- ogy and overall architecture of these processor-**memory** 3D organizations are no different than that used in traditional off-chip **memories**. ...
Cited by 581 Related articles All 14 versions Cite Save

Buffer to multiply **memory** interface
JM Dodd, MW Williams, JB Halberi, RM Bonella... - US Patent ..., 2003 - Google Patents
... Multi-**rank memory** module that emulates a **memory** module having a different number of **ranks**. US8631193, May 17, 2012, Jan 14, 2014, Google Inc. ... Transferring **data** between **memories** over a local **bus**. US8726064, Apr 17, 2006, May 13, 2014, Violin **Memory** Inc. ...
Cited by 181 Related articles All 2 versions Cite Save

Write clock and **data** window tuning based on **rank** select
PA LaBerge, J Dodd - US Patent 6,804,764, 2004 - Google Patents
... shift by the fine tap delay line for a corresponding request to a specific **rank** 32A-32H. ... such as the output **buffer** 48 may be tied to the individual **buses** on the **memory data bus** 34. ... the look-up table 46 would include impedances value corresponding to each of the **ranks** 32A-32H. ...
Cited by 165 Related articles All 4 versions Cite Save

Mini-**rank**: Adaptive DRAM architecture for improving **memory** power efficiency
H Zheng, J Lin, Z Zhang, E Gorbatov, H David... - Proceedings of the 41st ..., 2008 - dl.acm.org
... With conventional DDRx **memories**, the **data** are burst for four **bus** cycles (the 4th row), which is 7.5ns if the **memory** is DDR3 ... With x32 mini-**rank**, the **data** are first burst into the MRB for eight **bus** cycles (the 5th row), and then onto the x64 **bus** for four cycles (the 6th row) in a ...
Cited by 203 Related articles All 13 versions Cite Save

Integral **memory buffer** and serial presence detect capability for fully-**buffered** **memory** modules
K Bains, R Ellis, C Freeman, J Halbert... - US Patent App. 10/ ..., 2003 - Google Patents
... The configuration register parameters can then be used to adjust how DRAM interface 340 communicates with a **rank** or **ranks** of DRAMs on the module. [0034]. BIST function 350 can initiate test sequences to test the device's **memory** channels and/or test the DRAM devices. ...
Cited by 184 Related articles All 2 versions Cite Save

Memory rank decoder for a multi-**rank** Dual Inline **Memory** Module (DIMM)
S Raghuram - US Patent 7,266,639, 2007 - Google Patents
... All DRAM chips are clocked by a clock signal CLK which is **buffered** by a clock signal **buffer** which is also mounted on the Dual Inline **Memory** Module (DIMM). ... 2 comprises two **memory** **ranks** or **memory** levels, ie **memory rank** 0 and **memory rank** 1. ...
Cited by 81 Related articles All 4 versions Cite Save

High density **memory** modules with improved **data bus** performance
BJ Connolly, MW Kellogg, BG Hazelzet - US Patent 5,802,395, 1998 - Google Patents
... US8009495, Apr 26, 2010, Aug 30, 2011, S. Aqua Semiconductor, Llc, **Memories** with front end precharge. ... Multi-**rank memory** module that emulates a **memory** module having a different number of **ranks**. ... Configurable **memory** circuit system and method. ...
Cited by 129 Related articles All 2 versions Cite Save

Petitioners
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High density **memory** module with in-line **bus** switches being enabled in response to read/write selection state of connected RAM banks to improve **data bus** ...

BJ Connolly, BG Hazelzet, MW Kellogg - US Patent 6,070,217, 2000 - Google Patents

... US8626998, Aug 21, 2013, Jan 7, 2014, Smart Modular Technologies, Inc. Multi-**rank memory** module that emulates a **memory** module having a different number of **ranks**. US8631193, May 17, 2012, Jan 14, 2014, Google Inc. **...**

Cited by 112 Related articles All 2 versions Cite Save

Buffer chip for a multi-**rank** dual inline **memory** module (DIMM)

S Raghuram - US Patent App. 11/010,247, 2004 - Google Patents

... All DRAM chips are clocked by a clock signal CLK which is **buffered** by a clock signal **buffer** which is also mounted on the Dual Inline **Memory** Module (DIMM). **...** 2 comprises two **memory ranks** or **memory** levels, ie **memory rank** 0 and **memory rank** 1. [0016]. To increase **...**

Cited by 61 Related articles All 2 versions Cite Save

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Ex. 1057, p. 351

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	14/715,486
				Filing Date	May 18, 2015
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2139
				Examiner Name	Unknown
Sheet	1	of	2	Attorney Docket Number	NETL.018P2C8

US PATENT DOCUMENTS					
Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1.	Patent Trial and Appeal Board Decision on Request for Rehearing for Reexamination Control No. 95/001,381, mailed August 13, 2014, 7 pages.	
	2.	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control Nos. 95/000,546 and 95/000,577, mailed February 25,2015, 25 pages.	
	3.	Patent Trial and Appeal Board Decision on Request for Rehearing for Reexamination Control Nos. 95/000,546 and 95/000,577, mailed August 27, 2015, 5 pages.	
	4.	Examiner's Determination after Board Decision on Appeal for Reexamination Control No. 95/001,337, mailed September 11, 2015, 16 pages.	
	5.	Inter Partes Review Case No. IPR2015-01020, Petition for Inter Partes Review of U.S. Patent No. 7,881,150, filed on April 7, 2015.	
	6.	Inter Partes Review Case No. IPR2014-01020, Exhibit 1002 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on April 7, 2015.	
	7.	Inter Partes Review Case No. IPR2014-01020, Exhibit 1023 to Petition for Inter Partes Review, curriculum vitae of Dr. Srinivasan Jagannathan, filed on April 7, 2015.	
	8.	Inter Partes Review Case No. IPR2014-01020, Exhibit 1025 to Petition for Inter Partes Review, "operational," *The Pocket Oxford American Dictionary of Current English,* Oxford University Press, 2002, filed on April 7, 2015.	
	9.	Inter Partes Review Case No. IPR2014-01020, Decision to Institute Inter Partes Review of D U.S. Patent No. 7,881,150, dated October 8, 2015.	
	10.	Inter Partes Review Case No. IPR2015-01 021, Petition for Inter Partes Review of U.S. Patent No. 8,081,536, filed on April 7, 2015	
	11.	Inter Partes Review Case No. IPR2014-01 021, Corrected Exhibit 1002 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on April 22, 2015.	
	12.	Inter Partes Review Case No. IPR2014-01 021, Exhibit 1026 to Petition for Inter Partes Review, curriculum vitae of Dr. Srinivasan Jagannathan, filed on April 7, 2015.	
	13.	Inter Partes Review Case No. IPR2014-01 021, Decision to Institute Inter Partes Review of U.S. Patent No. 8,081,536, dated October 8, 2015	
	14.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.,* Corrected Joint Claim Construction and Prehearing Statement Pursuant to Patent L.R. 4-3, including Exhibit A, filed August 27,2014, 28 pages.	

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	15.	U.S. Court of Appeals for the Federal Circuit, Decision on Appeal for Reexamination Control No. 95/001,381, filed November 13, 2015, 14 pages	

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14715486	SOLOMON ET AL.
	Examiner	Art Unit
	GURTEJ BANSAL	2139

CPC- SEARCHED		
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CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Text Search in EAST (See Attached)	04/30/2017	GB
Inventor Search in PE2E	04/30/2017	GB
NPL Search in Google Scholar (See Attached)	04/30/2017	GB

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	04/30/2017	GB

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	1	6717855	04-06-2004	Underwood	

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	2	Action Closing Prosecution mailed October 1, 2012, for Control Nos. 95/000,546 and 95/000,577, filed May 11, '2010 and October 20, 2010 respectively, 39 pages.	
	3	Non-Final Office Action mailed November 13, 2012, for Control Nos. 95/001,339, 95/000,578 and 95/000,579, filed April 20, 2010, October 20, 2010 and October 21, 2010 respectively, 81 pages	
	4	Order Granting Request for Inter Partes Reexamination and Non-Final Office Action mailed December 7,2012, for Control No. 95/002,399, filed September 15, 2012, 89 pages.	
	5	Non-Final Office Action mailed December 19, 2012, for Control No. 95/001,758, filed September 14, 2011, 36 Pages.	
	6	Request for Inter Partes Reexamination; Reexam U.S. Patent Application No. 95/001,758, for U.S. Patent No. 7,864,627, filed September 15, 2011, 814 pages (submitted in four parts.)	
	7	Request for Inter Partes Reexamination; Reexam U.S. Patent Application No. 95/001,381, for U.S. Patent No. 7,532,537, filed June 9, 2010, 247 pages	

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	1	20080025137	01-31-2008	Natarajan et al.	
	2	2006233012	10-19-2006	Tomonori et al.	

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	3	EP 1 816 570 A2	08-08-2007	Rambus, Inc.		

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	4	International Search Report and Written Opinion, PCT/US2011/059209, January 31, 2013	

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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	14/715,486
				Filing Date	May 18, 2015
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2139
				Examiner Name	Unknown
Sheet	1	of	1	Attorney Docket Number	NETL.018P2C8

NON PATENT LITERATURE DOCUMENTS			
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	2.	Inter Partes Review of U.S. Patent No. 8,081,536, IPR Case No. IPR2014-00883, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
	3.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
	4.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3001 to Decision – Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued December 16, 2014	
	5.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3002 to Decision – Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued December 16, 2014	
	6.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3003 to Decision – Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued December 16, 2014	
	7.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3004 to Decision – Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued December 16, 2014	
	8.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014.	

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First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

US PATENT DOCUMENTS

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	2.	5,313,624	1994-05-17	Harriman	
	3.	5,630,096	1997-05-13	Zuravleff	
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	18.	20030070052	2003-04-10	Lai	

NON PATENT LITERATURE DOCUMENTS

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	19.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Record of Oral Hearing, dated July 26, 2016	
	20.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Final Written Decision, issued September 28, 2016	
	21.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3001 to Final Decision, issued September 28, 2016	
	22.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3001-2 to Final Decision, issued September 28, 2016	

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	25.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3004 to Final Decision, issued September 28, 2016	
	26.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Final Decision, issued September 28, 2016	
	27.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Petition for Inter Partes Review, filed December 30, 2016	
	28.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Exhibit 1003, "Declaration of Harold S. Stone," filed December 30, 2016	
	29.	Inter Partes Review of U.S. Patent No. 8516185, Case No. IPR2017-00577, Petition for Inter Partes Review, filed January 5, 2017	
	30.	Inter Partes Review of U.S. Patent No. 8516185, Case No. IPR2017-00577, Exhibit 1003, "Declaration of Harold S. Stone," filed January 5, 2017	
	31.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Exhibit 1008, Declaration of John J. Kelly Regarding Records of Joint Electron Device Engineering Council (JEDEC), filed December 30, 2016	
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Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

US PATENT DOCUMENTS

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	1.	5388240	02-01-1995	IBM Corporation	
	2.	5463590	10-31-1995	Watanabe	
	3.	5953280	09-14-1999	Matsui	
	4.	6188641	02-13-2001	Uchida	
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	12.	8233303	07-31-2012	Best	
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	21.	RE36229	06-15-1999	Cady	

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	22.	13/411,344	3/2/2012	Lee	Entire Prosecution History
	23.	13/970,606	8/20/2013	Netlist, Inc.	Entire Prosecution History
	24.	13/971,231	8/20/2013	Netlist, Inc.	Entire Prosecution History
	25.	14/229,844	3/29/2014	Netlist, Inc.	Entire Prosecution History
	26.	14/324,990	7/7/2014	Netlist, Inc.	Entire Prosecution History
	27.	14/337,168	7/21/2014	Netlist, Inc.	Entire Prosecution History

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	39.	Inter Partes Review Case No. IPR2014-01029, Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on June 24, 2014.	
	40.	Inter Partes Review Case No. IPR2014-01029, Exhibit 1008 to Petition for Inter Partes Review, "Declaration of Charles J. Neuhauser, Ph.D. under 37 C.F.R. § 1.68," filed on June 24, 2014.	
	41.	Inter Partes Review Case No. IPR2014-01029, Supplemental Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on July 23, 2014.	
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	43.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014.	
	44.	Inter Partes Review Case No. IPR2014-01029, Petitioner's Request for Rehearing pursuant to 37 C.F.R. § 42.71, filed on January 15, 2015.	

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	45.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Request for Rehearing, Issued on March 3, 2015.	
	46.	Inter Partes Review Case No. IPR2014-01369, Corrected Petition for Inter Partes Review of Claims 1-19 of U.S. Patent No. 8,516,185, filed on September 22, 2014.	
	47.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1008 to Corrected Petition for Inter Partes Review, "Declaration of Dr. Nader Bagherzadeh under 37 C.F.R. § 1.68," filed on September 22, 2014.	
	48.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1013 to Corrected Petition for Inter Partes Review, "Webster's II New College Dictionary," filed on September 22, 2014.	
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	50.	Inter Partes Review Case No. IPR2014-01369, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued March 9, 2014.	
	51.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Smart Storage Systems, Inc.'s Invalidity Contentions, dated June 6, 2014	
	52.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits E.1-E.7 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	53.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Diablo Technologies, Inc.'s Invalidity Contentions, dated June 6, 2014.	
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	4386	711/5.ccls. 711/147.ccls.	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:37
S2	4481	DQS	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:38
S3	88990	DS	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:38
S4	32759	DQ	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:38
S5	3171	S2 and S4	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:38
S6	134822	rank	US-PGPUB; USPAT	OR	ON	2013/12/02 23:38
S7	329	S5 and S6	US-PGPUB; USPAT	OR	ON	2013/12/02 23:38
S8	201	US-4218740-$.DID. OR US-4368515-$.DID. OR US-4392212-$.DID. OR US-4633429-$.DID. OR US-4670748-$.DID. OR US-4706214-$.DID. OR US-4866603-$.DID. OR US-4958322-$.DID. OR US-4961172-$.DID. OR US-4961204-$.DID. OR US-4980850-$.DID. OR US-5247643-$.DID. OR US-5272664-$.DID. OR US-5345412-$.DID. OR US-5357478-$.DID. OR US-5388072-$.DID. OR US-5392252-$.DID. OR US-5426753-$.DID. OR US-5483497-$.DID. OR US-5485589-$.DID. OR US-5495435-$.DID. OR US-5513135-$.DID. OR US-5532954-$.DID. OR US-5541448-$.DID. OR US-5572691-$.DID. OR US-5581498-$.DID. OR US-5590071-$.DID. OR US-5602999-$.DID. OR US-5638534-$.DID. OR US-5655153-$.DID. OR US-5699542-$.DID. OR US-5702984-$.DID. OR US-5703826-$.DID. OR US-5745914-$.DID. OR US-5764590-$.DID. OR US-5784705-$.DID. OR US-5802395-$.DID. OR US-5805520-$.DID. OR US-5822251-$.DID. OR US-5909388-$.DID. OR US-5926827-$.DID. OR US-5926839-$.DID. OR US-5953215-$.DID. OR US-5958025-$.DID. OR US-5959930-$.DID. OR US-5963464-$.DID. OR US-5966736-$.DID. OR US-5974493-$.DID. OR US-6018787-$.DID. OR US-6044032-$.DID. OR US-6070217-$.DID.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/12/03 00:02

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S9	1184	multiplex$3 with (DQS and DQ)	US-PGPUB; USPAT	OR	ON	2013/12/03 00:07
S10	359	multiplex$3 with (DQS and DQ) with delay$3	US-PGPUB; USPAT	OR	ON	2013/12/03 00:08
S11	850	multiplex$3 with DQS and delay with delay$3	US-PGPUB; USPAT	OR	ON	2013/12/03 00:12
S12	562	multiplex$3 with DQS and DQ with delay$3	US-PGPUB; USPAT	OR	ON	2013/12/03 00:12
S13	401	multiplex$3 with DQS same DQ with delay$3	US-PGPUB; USPAT	OR	ON	2013/12/03 00:12
S14	0	13/287042.app.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S15	0	13/287042.ap.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S16	0	"13287042".ap.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S17	0	"13287042".app.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S18	294	multiplex$3 with DQS same delay$3 with data with signals	US-PGPUB;	OR	ON	2013/12/03 00:28

			USPAT			
S19	307	multiplex$3 with DQS same delay$3 with data with (signals lines)	US-PGPUB; USPAT	OR	ON	2013/12/03 00:28
S20	9	multiplex$3 with DQS same delay$3 with data with (signals lines) same2 rank	US-PGPUB; USPAT	OR	ON	2013/12/03 00:28
S21	26	multiplex$3 with DQS same delay$3 with data with (signals lines) and rank	US-PGPUB; USPAT	OR	ON	2013/12/03 00:29
S22	238	multiplex$3 with DQS same delay$3 with data with (signals lines) same memory	US-PGPUB; USPAT	OR	ON	2013/12/03 00:30
S23	347	isolat$3 with DQ with DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 00:47
S24	21	isolat$3 with DQ with DQS same Rank	US-PGPUB; USPAT	OR	ON	2013/12/03 00:47
S25	1353	DQS with select$3 with (memory rank)	US-PGPUB; USPAT	OR	ON	2013/12/03 00:50
S26	54	chip$1select with rank and DQ and DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:25
S27	56	chip$1select same rank and DQ and DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:26
S28	61	chip$1select and rank and DQ and DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:27
S29	5	rank with DQ with DQS with low	US-PGPUB; USPAT	OR	ON	2013/12/03 18:39
S30	300	rank with DQ with DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:40
S31	82	rank and (DQ with DQS) with off	US-PGPUB; USPAT	OR	ON	2013/12/03 19:03
S32	271	rank and (DQ with DQS) with high	US-PGPUB; USPAT	OR	ON	2013/12/03 19:07
S33	29	rank with (DQ with DQS) with high	US-PGPUB; USPAT	OR	ON	2013/12/03 19:07
S34	1	"6873533".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 19:07
S35	7	rank with (DQ with DQS) with terminat$3	US-PGPUB; USPAT	OR	ON	2013/12/03 19:10
S36	20	rank with (DQ with DQS) with isolat$3	US-PGPUB; USPAT	OR	ON	2013/12/03 19:11
S37	21	rank same (DQ with DQS) with isolat$3	US-PGPUB;	OR	ON	2013/12/03 19:11

			USPAT			
S38	57	rank same (DQ with DQS) with high	US-PGPUB; USPAT	OR	ON	2013/12/03 19:11
S39	7	rank same (DQ with DQS) with (mux multiplexer)	US-PGPUB; USPAT	OR	ON	2013/12/03 19:15
S40	37	rank and (DQ with DQS) with (mux multiplexer)	US-PGPUB; USPAT	OR	ON	2013/12/03 19:16
S41	1040	(DQ with DQS) with (mux multiplexer)	US-PGPUB; USPAT	OR	ON	2013/12/03 19:21
S42	1024	(DQ with DQS) with (mux multiplexer) and memory	US-PGPUB; USPAT	OR	ON	2013/12/03 19:21
S43	634	(DQ with DQS) with (mux multiplexer) same memory	US-PGPUB; USPAT	OR	ON	2013/12/03 19:21
S44	231	(DQ with DQS) with (mux multiplexer) with memory	US-PGPUB; USPAT	OR	ON	2013/12/03 19:21
S45	1	"20040098428".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 19:40
S46	1	"20040098528".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 19:41
S47	1	"20030070052".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 19:42
S48	1	"20050047250".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 20:07
S49	1599	G06F12/0607.cpc. G06F12/0813.cpc.	US-PGPUB; USPAT	OR	OFF	2013/12/20 11:11
S50	2437	latency with memory adj controller with memory	US-PGPUB; USPAT	OR	ON	2014/04/04 14:15
S51	59	latency with memory adj controller with (measur$3 test$3)	US-PGPUB; USPAT	OR	ON	2014/04/04 14:16
S52	22	rank same (DQ with DQS) with isolat$3	US-PGPUB; USPAT	OR	ON	2014/04/04 15:16
S53	22	isolat$3 with DQ with DQS same Rank	US-PGPUB; USPAT	OR	ON	2014/04/04 15:29
S54	26	multiplex$3 with DQS same delay$3 with data with (signals lines) and rank	US-PGPUB; USPAT	OR	ON	2014/04/04 15:29
S55	1	"6553450".pn.	US-PGPUB; USPAT	OR	ON	2014/04/04 15:33
S56	1	"6742098".pn.	US-PGPUB;	OR	ON	2014/04/04 15:48

			USPAT			
S60	644	isolat$3 with load with memory	US-PGPUB; USPAT	OR	ON	2014/04/04 15:58
S61	46	isolat$3 with load with memory with controller	US-PGPUB; USPAT	OR	ON	2014/04/04 15:58
S62	28	US-5345412-$.DID. OR US-5537584-$.DID. OR US-5617559-$.DID. OR US-5649159-$.DID. OR US-5717851-$.DID. OR US-5724604-$.DID. OR US-5729716-$.DID. OR US-5784705-$.DID. OR US-5802541-$.DID. OR US-5973392-$.DID. OR US-6173357-$.DID. OR US-6260127-$.DID. OR US-6446158-$.DID. OR US-6553449-$.DID. OR US-6618791-$.DID. OR US-6717855-$.DID. OR US-6788592-$.DID. OR US-6948084-$.DID. OR US-7130308-$.DID. OR US-7133960-$.DID. OR US-7379361-$.DID. OR US-20050010737-$.DID. OR US-20070293094-$.DID. OR US-3412243-$.DID. OR US-2201420-$.DID. OR US-2761179-$.DID. OR US-2201346-$.DID. OR US-2504131-$.DID.	US-PGPUB; USPAT	OR	ON	2014/05/05 00:39
S63	2355572	read$only with non$1volatile with main memory	US-PGPUB; USPAT	OR	OFF	2014/05/08 19:12
S64	2126	read$only with non$1volatile with main with memory	US-PGPUB; USPAT	OR	OFF	2014/05/08 19:12
S65	1	"20080080261".pn.	US-PGPUB; USPAT	OR	OFF	2014/05/11 20:14
S66	4529	711/5.ccls. 711/147.ccls.	US-PGPUB; USPAT	OR	OFF	2014/05/15 16:09
S67	3613	DQS and DQ	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:10
S68	1574	DQS and DQ with (coupl$3 connect$3 isolat$3 select$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:10
S69	1309	DQS and DQ with (connect$3 isolat$3 select$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:11
S70	1108	DQS and DQ with (coupl$3 isolat$3 select$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:11
S71	569	DQS and DQ with (coupl$3 isolat$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:12
S72	149	DQS and DQ with (decoupl$3 isolat$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:15
S73	149	DQS and DQ with (decoupl$3 isolat$3 detach$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:17
S74	167	DQS and DQ with (decoupl$3 isolat$3	US-	OR	OFF	2015/01/01

		detach$3 disconnect$3)	PGPUB; USPAT			23:17
S75	20	DQS and DQ with (disconnect$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:18
S76	3	"20010008006".pn. "20050257109".pn. "20070070669".pn.	US-PGPUB; USPAT	OR	OFF	2015/01/02 00:02
S77	3	"6747887".pn. "7093066".pn. "6832303".pn.	US-PGPUB; USPAT	OR	OFF	2015/01/02 00:03
S83	25	rank same (DQ with DQS) with isolat$3	US-PGPUB; USPAT	OR	ON	2015/03/30 14:21
S84	29	multiplex$3 with DQS same delay$3 with data with (signals lines) and rank	US-PGPUB; USPAT	OR	ON	2015/03/30 14:23
S85	1	"5388240".pn.	US-PGPUB; USPAT	OR	ON	2015/03/30 14:24
S86	18	"5388240".pn. "5463590".pn. "5953280".pn. "6188641".pn. "6205516".pn. "64804393".pn. "7464225".pn. "7865674".pn. "8089795".pn. "8130560".pn. "8189328".pn. "8233303".pn. "8250295".pn. "8417870".pn. "8516185".pn. "8516188".pn. "8756364".pn. "20070058409".pn. "20080104352".pn. "20080104352".pn.	US-PGPUB; USPAT	OR	ON	2015/03/30 14:28
S87	69	chip$1select same rank and DQ and DQS	US-PGPUB; USPAT	OR	ON	2015/03/30 14:31
S88	10	rank same (DQ with DQS) with (mux multiplexer)	US-PGPUB; USPAT	OR	ON	2015/03/30 14:32

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S57	3448	711/5.ccls. 711/147.ccls.	USPAT; * No UPAD	OR	OFF	2014/04/04 15:50
S58	171076	isolat$3.clm.	USPAT; * No UPAD	OR	OFF	2014/04/04 15:52
S59	45	S57 and S58	USPAT; * No UPAD	OR	OFF	2014/04/04 15:52
S78	3626	711/5.ccls. 711/147.ccls.	USPAT; * No UPAD	OR	OFF	2015/01/02 00:11
S79	5815	isolates.clm.	USPAT; * No UPAD	OR	OFF	2015/01/02 00:12
S80	0	S78 and "L143"	USPAT; * No UPAD	OR	OFF	2015/01/02 00:12
S81	7	S78 and S79	USPAT; * No UPAD	OR	OFF	2015/01/02 00:12
S82	0	S78 and S79 and DQS.clm.	USPAT; * No UPAD	OR	OFF	2015/01/02 00:15

S89	1049	G06F12/0607.cpc. G06F12/0813.cpc.	USPAT; * No UPAD	OR	OFF	2015/03/30 14:34
S90	181517	isolat$3.clm.	USPAT; * No UPAD	OR	OFF	2015/03/30 14:34
S91	5909	isolates.clm.	USPAT; * No UPAD	OR	OFF	2015/03/30 14:34
S92	0	S89 and S91	USPAT; * No UPAD	OR	OFF	2015/03/30 14:34

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14/715,486	05/18/2015 RULE	711	2139	N3044.10002US21

APPLICANTS
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INVENTORS
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Jayesh R. Bhakta, Cerritos, CA;

**** CONTINUING DATA ***************************
This application is a CON of 13/971,231 08/20/2013 PAT 9037774
which is a CON of 13/287,081 11/01/2011 PAT 8516188
which is a CON of 13/032,470 02/22/2011 PAT 8081536
which is a CON of 12/955,711 11/29/2010 PAT 7916574
which is a CON of 12/629,827 12/02/2009 PAT 7881150
which is a CON of 12/408,652 03/20/2009 PAT 7636274
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7289386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7286436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004
and claims benefit of 60/590,038 07/21/2004

**** FOREIGN APPLICATIONS ***************************

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05/27/2015

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /GURTEJ BANSAL/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	23	21	3

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UNITED STATES

TITLE
MEMORY MODULE WITH DATA BUFFERING

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14715486
Filing Date	2015-05-18
First Named Inventor	Jeffrey C. Solomon
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	N3044.10002US21

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5357478		1994-10-18	Kikuda et al	
	2	5559970		1996-09-24	Sharma	

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	Application Number	14715486
	Filing Date	2015-05-18
	First Named Inventor	Jeffrey C. Solomon
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1	BUSINESS WIRE, Samsung Announces Mass Production of DDR2; Industry's First 1 GigaByte DDR2 DIMM Offers High Speed and Low Power Necessary for Next-Generation PCs and Servers, March 24, 2003.	
	2	BUSINESS WIRE, Samsung DDR2 Ready To Support Market For Next Generation PCs and Servers, September 16, 2003. 8. IEEE, INC., "chip select," IEEE Standard Dictionary of Electrical and Electronic Terms, 5th Ed., 1993.	
	3	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control Nos. 95/000,578; 95/000,579; and 95/001,339, mailed May 31, 2016, 106 pages.	
	4	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control No. 95/001,758, mailed May 31, 2016, 49 pages.	
	5	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control Nos. 95/000,546 and 95/000,577, mailed February 25, 2015, 25 pages.	
	6	Patent Trial and Appeal Board Decision on Request for Rehearing for Reexamination Control Nos. 95/000,546 and 95/000,577, mailed August 27, 2015, 5 pages.	
	7	SMITH, VAN. "Kentron Q&A." Van's Hardware. www.vanshardware.com. December 3, 2001, 4 pages.	
	8	WESTE, NEIL H.E. et al., "CMOS VLSI Design: A Circuits and Systems Perspective." 3rd Edition, 2005. 4 pages.	
	9	"WESTE, NEIL H.E. et al., ""CMOS VLSI Design: A Circuits and Systems Perspective."" 4thEdition, 2011. 4 pages."	
	10	Non-Final Action Closing Prosecution mailed March 21, 2014, for Control Nos. 95/001,339; 95/000,578; and 95/000,579, 92 pages.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14715486
	Filing Date	2015-05-18
	First Named Inventor	Jeffrey C. Solomon
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

	11	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control No. 95/001,381, mailed January 16, 2014, 24 pages.	
	12	Requester Request for Rehearing after Board Decision dated 02/18/2014 for Reexamination Control No. 95/001337	
	13	Patent Owner Response after Board Decision dated 03/18/2014 for Reexamination Control No. 95/001337	
	14	Affidavit-traversing rejectns or objectns rule 132 dated 03/18/2014 for Reexamination Control No. 95/001337	
	15	Patent Owner Response after Board Decision dated 03/19/2014 for Reexamination Control No. 95/001337	
	16	Affidavit-traversing rejectns or objectns rule 132 dated 03/19/2014 for Reexamination Control No. 95/001337	
	17	Patent Owner Comments on Req for Rehearing timely dated 03/19/2014 for Reexamination Control No. 95/001337	
	18	Reexam - Affidavit/Decl/Exhibit Filed by 3rd Party dated 04/17/2014 for Reexamination Control No. 95/001337	
	19	Requester Comments on Patent Owner Response after Board Decision dated 04/17/2014 for Reexamination Control No. 95/001337	
	20	New Board of Appeals Decision after Board Decision with New Ground of Rejection: New Ground of Rejection dated 06/26/2014 for Reexamination Control No. 95/001337	
	21	Patent Owner Response after Board Decision dated 07/29/2014 for Reexamination Control No. 95/001337	

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	Attorney Docket Number	N3044.10002US21

	22	Reexam Petition Decision - Denied dated 08/05/2014 for Reexamination Control No. 95/001337	
	23	Requester Comments on Patent Owner Response after Board Decision dated 09/05/2014 for Reexamination Control No. 95/001337	
	24	Reexam - Affidavit/Decl/Exhibit Filed by 3rd Party dated 09/05/2014 for Reexamination Control No. 95/001337	
	25	Examiner's Determination on Patent Owner Response/Requester Comments after Board Decision dated 06/15/2015 for Reexamination Control No. 95/001337	
	26	Examiner's Determination on Patent Owner Response/Requester Comments after Board Decision dated 09/11/2015 for Reexamination Control No. 95/001337	
	27	Affidavit-traversing rejectns or objectns rule 132 dated 10/14/2015 for Reexamination Control No. 95/001337	
	28	Affidavit-traversing rejectns or objectns rule 132 (26 pages) dated 10/14/2015 for Reexamination Control No. 95/001337	
	29	Patent Owner Comments on Examiner's Determination after Board Decision dated 10/14/2015 for Reexamination Control No. 95/001337	
	30	Reexam - Affidavit/Decl/Exhibit Filed by 3rd Party dated 11/13/2015 for Reexamination Control No. 95/001337	
	31	Reqr Comments on Examiners Determ after Board Decision dated 11/13/2015 for Reexamination Control No. 95/001337	
	32	Other Reference-Patent/App/Search documents dated 11/22/2016 for Reexamination Control No. 95/001337	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2015-05-18
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	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

	33	Petition under Rule 41.3 to Chief Admin Patent Judge dated 11/22/2016 for Reexamination Control No. 95/001337	
	34	Administrative Remand to Examiner dated 01/19/2017 for Reexamination Control No. 95/001337	
	35	Reexam Petition Decision - Granted - in-part dated 01/23/2017 for Reexamination Control No. 95/001337	
	36	Affidavit-traversing rejectns or objectns rule 132 dated 02/22/2017 for Reexamination Control No. 95/001337	
	37	Patent Owner Comments on Examiner's Determination after Board Decision dated 02/22/2017 for Reexamination Control No. 95/001337	
	38	Reexam - Affidavit/Decl/Exhibit Filed by 3rd Party dated 03/22/2017 for Reexamination Control No. 95/001337	
	39	Requester Comments on Patent Owner Response after Board Decision dated 03/22/2017 for Reexamination Control No. 95/001337	

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EXAMINER SIGNATURE

Examiner Signature	/GURTEJ BANSAL/	Date Considered	06/02/2017

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	First Named Inventor	Jeffrey C. Solomon
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/JAMIE J. ZHENG/	Date (YYYY-MM-DD)	2017-05-09
Name/Print	Jamie J. Zheng	Registration Number	51167

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/715,486	05/18/2015	Jeffrey C. Solomon	N3044.10002US21	1537

79141 7590 06/07/2017

Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

EXAMINER
BANSAL, GURTEJ

ART UNIT	PAPER NUMBER
2139	

NOTIFICATION DATE	DELIVERY MODE
06/07/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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U.S. Patent and Trademark Office
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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
14/715,486	18 May, 2015	SOLOMON ET AL.	N3044.10002US21

		EXAMINER	
Jamie J. Zheng, Ph.D Esq. MASCHOFF BRENNAN 1389 Center Drive Suite 300 Park City, UT 84098		GURTEJ BANSAL	
		ART UNIT	PAPER
		2139	20170602

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

IDS dated 05/09/2017 has been fully considered.

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

PTO-90C (Rev.04-03)

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	14715486
Filing Date	2015-05-18
First Named Inventor	Jeffrey C. Solomon
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	N3044.10002US21

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14715486
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	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

	1	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, DECISION Institution of Inter Partes Review, entered May 15, 2017.	
	2	Inter Partes Review of U.S. Patent No. 7,532,537, Case No. IPR2017-00667, DECISION Institution of Inter Partes Review, entered July 21, 2017.	
	3	Inter Partes Review of U.S. Patent No. 7,532,537, Case No. IPR2017-00668, DECISION Institution of Inter Partes Review, entered July 21, 2017.	
	4	Inter Partes Review of U.S. Patent No. , Case No. IPR2017-00577, DECISION Institution of Inter Partes Review, entered May 15, 2017.	
	5	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, DECISION Institution of Inter Partes Review, entered July 7, 2017.	
	6	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, SCHEDULING ORDER, entered July 7, 2017.	

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	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

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OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/JAMIE J. ZHENG/	Date (YYYY-MM-DD)	2017-08-11
Name/Print	Jamie J. Zheng	Registration Number	51167

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-14)
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	14715486	Filing Date	2015-05-18	Docket Number (if applicable)	N3044.10002US21	Art Unit	2139
First Named Inventor	Jeffrey C. Solomon			Examiner Name	BANSAL, GURTEJ		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, to any international application that does not comply with the requirements of 35 U.S.C. 371, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV.

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 505394

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

Applicant Signature

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Signature of Registered U.S. Patent Practitioner			
Signature	/JAMIE J. ZHENG/	Date (YYYY-MM-DD)	2017-08-11
Name	Jamie J. Zheng	Registration Number	51167

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Customer No. 79141
Attorney Docket No.: NETL.018P2C7

Modified PTO/AIA/01 (06-12)

DECLARATION FOR UTILITY OR DESIGN APPLICATION

Title of Invention	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE

As a below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

■ United States application or PCT international application number 13/971,231 filed on August 20, 2013.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Note to Inventor: 37 C.F.R. § 1.63(c) states: "A person may not execute an oath or declaration for an application unless that person has reviewed and understands the contents of the application, including the claims, and is aware of the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56."

First Inventor (Legal Name): Jeffrey C. Solomon

Signature: Jeffrey C. Solomon Date (Optional): 10-14-2013

Second Inventor (Legal Name): Jayesh R. Bhakta

Signature: Jayesh Bhakta Date (Optional): 10-14-2013

Remarks

This Amendment is in response to the Notice of Allowance issued on May 11, 2017, in which the Examiner allowed claims 1-18 and 22-29 after an Applicant authorized Examiner's Amendment.

Claims 10 and 18 are cancelled. Claims 1-7, 9, 11, 13-15, 17, and 22-29 are amended. New claims 30-34 are presented. After entry of this amendment, the pending claims are 1-9, 11-17, and 22-34.

Support for the amendments and the new claims can be found throughout the Specification and Drawings. Therefore, no new matter is added. Specifically, support for the amendments and new claims 31-34 can be found in, for example, paragraphs [0045], [0052]-[0053], [0056]-[0057], and [0102]; and support for new claim 30 can be found in, for example, paragraphs [0152]-[0158].

The Examiner is invited to call the undersigned attorney at (650) 521-4828, if a telephone call could help answer any questions regarding this matter.

Respectfully submitted,

Dated: August 11, 2017

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 521-4828

IN THE CLAIMS

1. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a data bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank, wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command; ~~and~~

a buffer coupled between the at least one first memory integrated circuit and the data bus, and between the at least one second memory integrated circuit and the data bus~~, wherein the buffer is configured in response to the first memory command to provide a first data path between the at least one first memory integrated circuit and the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command, and wherein the buffer is configured in response to the second memory command to provide a second data path between the at least one second memory integrated circuit and the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command, the second data path being different from the first data path~~; and

logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between

the at least one first memory integrated circuit and the memory controller through the buffer, wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.

2. (Currently Amended) The memory module of claim 1, wherein the buffer ~~isolates~~ is configured to isolate both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the data bus when the memory module is not being accessed by the memory controller.

3. (Currently Amended) The memory module of claim 1, wherein the first memory command includes at least one first chip select signal and the second memory command includes at least one second chip select signal ~~that is the same as the at least one first chip select signal~~.

4. (Currently Amended) The memory module of claim 3, wherein the memory module produces at least third and fourth chip select signals in response to the first memory command, the third chip select signal being provided to the at least one first memory integrated circuit and having an active value to cause ~~select~~ the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the fourth chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.

5. (Currently Amended) The memory module of claim 4, wherein the memory module produces at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first memory command, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an active value to ~~select~~ cause the at least one second memory integrated circuit to receive or output data signals in response to the second memory command.

6. (Currently Amended) The memory module of claim 1, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the memory module outputs the first data burst together with a first burst of data strobe signals ~~data strobes~~ in response to the first read command, wherein memory module outputs the second data burst together with a second burst of data strobe signals ~~data strobes~~ in response to the second read command, wherein the second data burst follows the first data burst on the data bus, and wherein the buffer ~~prevents~~ is configured to prevent the first burst of data strobe signals ~~data strobes~~ and the second burst of data strobe signals ~~data strobes~~ from colliding with each other.

7. (Currently Amended) The memory module of claim 6, wherein each of the first burst of data strobe signals ~~data strobes~~ and the second burst of data strobe signals ~~data strobes~~ includes a pre-amble interval and a post-amble interval, and wherein the buffer ~~combines~~ is configured to combine the first burst of data strobe signals ~~data strobes~~ and the second burst of data strobe signals ~~data strobes~~ into a combined burst of data strobe signals ~~data strobes~~ that does not include the post-amble interval of the first burst of data strobe signals ~~data strobes~~ and the pre-amble interval of the second burst of data strobe signals~~data strobes~~.

8. (Previously Presented) The memory module of claim 1, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.

9. (Currently Amended) The memory module of claim 1, further comprising an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits.

10. (Cancelled)

11. (Currently Amended) A method of operating a memory module coupled to a memory controller via a memory bus including a control/address (C/A) bus and a data bus, the memory module comprising memory integrated circuits arranged in ranks and mounted on a printed circuit board having a plurality of edge connections coupled to the memory bus, the memory

integrated circuits including at least one first memory integrated circuit in a first rank and at least one second memory integrated circuit in a second rank, the method comprising:

receiving from the memory controller a first set of input control/address (C/A) signals associated with a first memory command via the C/A bus, the first memory command to cause the memory module to receive or output a first data burst;

generating a first set of output C/A signals in response to the first set of input C/A signals, the first set of output C/A signals causing the first rank to receive or output the first data burst;

receiving from the memory controller a second set of input control/address signals associated with a second memory command via the C/A bus, the second memory command to cause the memory module to receive or output a second data burst;

generating a second set of output C/A signals in response to the second set of input C/A signals, the second set of output C/A signals causing the second rank to receive or output the second data burst;

in response to the first memory command, providing ~~a first data path~~ first control signals to a buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer ~~data bus while the memory module is receiving or outputting the first data burst in response to the first memory command~~; and

in response to the second memory command, providing ~~a second data path~~ second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals ~~data bus while the memory module is receiving or outputting the second data burst in response to the second memory command, the second data path being different from the first data path~~.

12. (Original) The method of claim 11, further comprising isolating the at least one first memory integrated circuit and the at least one second memory integrated circuit from the data bus when the memory module is not being accessed by the memory system.

13. (Currently Amended) The method of claim 11, wherein the first set of input C/A signals include at least one input chip-select signal, the method further comprising generating ~~a greater number of output chip-select signals than the at least one input chip-select signal, the greater~~

~~number of output chip select signals including~~ a first chip select signal and a second chip select signal in response to the first set of input C/A signals, the first chip-select signal being provided to the at least one first memory integrated circuit and having an active value to ~~select~~ cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the second chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.

14. (Currently Amended) The method of claim 11, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the memory module outputs the first data burst together with a first burst of data strobe signals ~~data strobes~~ in response to the first read command, wherein the memory module outputs the second data burst together with a second burst of data strobe signals ~~data strobes~~ in response to the second read command, wherein the second data burst follows the first data burst on the data bus, the method further comprising combining the first burst of data strobe signals ~~data strobes~~ and the second burst of data strobes to form a third burst of data strobe signals ~~data strobes~~ on the data bus.

15. (Currently Amended) The method of claim 14, wherein each of the first burst of data strobe signals ~~data strobes~~ and the second burst of data strobe signals ~~data strobes~~ includes a pre-amble interval and a post-amble interval, and wherein the third burst of data strobes does not include the post-amble interval of the first burst of data strobe signals ~~data strobes~~ and the pre-amble interval of the second burst of data strobe signals~~data strobes~~.

16. (Original) The method of claim 11, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of the memory integrated circuits.

17. (Currently Amended) The method of claim 11, further comprising reporting an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of the memory integrated circuits.

18. (Cancelled)

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Currently Amended) The memory module of claim 1, wherein the buffer includes circuit components ~~common to both the~~ configurable to provide a first data path ~~and the~~ or a second data path~~, and wherein at least one of the circuit components is configured to provide the first data path or the second data path~~ depending on whether the first rank or the second rank is selected to communicate data with the memory controller.

23. (Currently Amended) The memory module of claim 22, ~~further comprising a logic element that configures~~ the at least one of the circuit components is configured to provide the first data path in response to the first control signals ~~memory command~~, and ~~that configures the at least one circuit components~~ is configured to provide the second data path in response to the second control signals ~~memory command~~.

24. (Currently Amended) The memory module of claim 1~~-22~~, wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits.

25. (Currently Amended) The memory module of claim 1~~-24~~, wherein the logic ~~element~~ is configured to ~~determine a latency value, and wherein~~ enable the communication of the first data burst between the at least one first memory integrated circuit and the memory controller ~~first data path and the second data path are provided~~ in accordance with a ~~the~~ latency value.

26. (Currently Amended) The memory module of claim 25~~-22~~, wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the first data burst through the buffer ~~that are configured to provide the first data path in response to the first memory command and to provide the second data path in response to the second memory command~~.

27. (Currently Amended) The method of claim 11, wherein the buffer includes circuit components configurable to provide a the first data path or a and the second data path have common circuit components, and wherein at least one of the common circuit components is configured differently to provide the first data path or the second data path depending on whether the first rank or the second rank is caused to communicate data with the memory controller.

28. (Currently Amended) The method of claim 11 27, wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits.

29. (Currently Amended) The method memory module of claim 1 28, further comprising determining a latency value, wherein the communication of the first data burst between the at least one first memory integrated circuit and the memory controller is enabled first data path and the second data path are provided in accordance with the latency value.

30. (New) The memory module of claim 1, wherein the memory module is further coupled to the memory controller using an on-die-termination (ODT) bus, wherein each of the plurality of memory devices includes an ODT circuit, the memory module further comprising a termination circuit external to any of the plurality of memory devices, wherein the termination circuit is coupled to the ODT bus and to the ODT circuit of at least one of the plurality of memory devices, wherein the termination circuit is configured to provide external termination of the at least one of the plurality of memory devices in response to an ODT signal on the ODT bus, and wherein the ODT circuit in the at least one of the plurality of memory devices is disabled.

31. (New) The memory module of claim 1, wherein the buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the first data burst or the second data burst through the buffer.

32. (New) The memory module of claim 25, wherein the logic is further configured to determine the latency value.

33. (New) The memory module of claim 25, wherein the logic is further configured to enable the communication of the second data burst between the at least one second memory integrated circuit and the memory controller in accordance with the latency value.

34. (New) The memory module of claim 33, wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the second data burst through the buffer.

Petitioners
Ex. 1057, p. 397

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist, Inc.
App. No.	:	14/715,486
Filed	:	18-MAY-2015
For	:	MEMORY MODULE WITH DATA BUFFERING
Examiner	:	BANSAL, GURTEJ
Art Unit	:	2139
Conf. No.	:	1537
Docket No.	:	N3044.10002US21

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I hereby certify that this correspondence and any other attachment noted on the Automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web Server on:

August 11, 2017

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

AMENDMENT AND RQUEST FOR CONTINUED EXAMINATION

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant submits the following amendments and a Request for Continued Examination in response to Notice of Allowance issued on May 11, 2017 in the above-identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5394.

Amendments to the Claims: Begin on page 2 of this paper.

Remarks: Begin on page 9 of this paper.

Electronic Patent Application Fee Transmittal

Application Number:	14715486
Filing Date:	18-May-2015
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Filer:	Jamie Jie Zheng/Brian Gonzalez
Attorney Docket Number:	N3044.10002US21

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	2202	3	40	120
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
RCE- 1st Request	2801	1	600	600
		Total in USD ($)		**720**

Electronic Acknowledgement Receipt

EFS ID:	30060853
Application Number:	14715486
International Application Number:	
Confirmation Number:	1537
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/Brian Gonzalez
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	N3044.10002US21
Receipt Date:	11-AUG-2017
Filing Date:	18-MAY-2015
Time Stamp:	18:01:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$720
RAM confirmation Number	081417INTEFSW18031000
Deposit Account	505394
Authorized User	Brian Gonzalez
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	2017-08-11_IDS_N3044-10002US21.pdf	1042981 81772f5b821a295176e63b6ab6a0f9a96a62e10f	no	4
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
2	Request for Continued Examination (RCE)	2017-08-11_RCE_N3044-10002US21.pdf	1349953 9d0cecf53b727c4433a0ba9cdaa93606589ee77d	no	3
Warnings:					
Information:					
3	Oath or Declaration filed	2017-08-11_Parent-Declaration_N3044-10002US21.pdf	67890 cd1bc510a3c4c88226acabdc460bc97c80482ab5	no	1
Warnings:					
Information:					
4		2017-08-11_Amendment_N3044-10002US21.pdf	722189 c49eb3322aa0ba7c2e7468a36db461999052db16	yes	10

Multipart Description/PDF files in .zip description

Document Description	Start	End
Applicant Arguments/Remarks Made in an Amendment	10	10
Claims	2	9
Amendment Submitted/Entered with Filing of CPA/RCE	1	1

Warnings:	
Information:	

5	Fee Worksheet (SB06)	fee-info.pdf	32320 2e2a8eec8601b1913e91cc39fa35de717898c7cb	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	3215333	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14715486
Filing Date	2015-05-18
First Named Inventor	Jeffrey C. Solomon
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	N3044.10002US21

U.S.PATENTS Remove

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14715486
	Filing Date	2015-05-18
	First Named Inventor	Jeffrey C. Solomon
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

	1	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, DECISION Institution of Inter Partes Review, entered May 15, 2017.	
	2	Inter Partes Review of U.S. Patent No. 7,532,537, Case No. IPR2017-00667, DECISION Institution of Inter Partes Review, entered July 21, 2017.	
	3	Inter Partes Review of U.S. Patent No. 7,532,537, Case No. IPR2017-00668, DECISION Institution of Inter Partes Review, entered July 21, 2017.	
	4	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, DECISION Institution of Inter Partes Review, entered July 7, 2017.	
	5	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, SCHEDULING ORDER, entered July 7, 2017.	

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14715486
	Filing Date	2015-05-18
	First Named Inventor	Jeffrey C. Solomon
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/JAMIE J. ZHENG/	Date (YYYY-MM-DD)	2017-08-11
Name/Print	Jamie J. Zheng	Registration Number	51167

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	30061975
Application Number:	14715486
International Application Number:	
Confirmation Number:	1537
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	N3044.10002US21
Receipt Date:	11-AUG-2017
Filing Date:	18-MAY-2015
Time Stamp:	20:09:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	2017-08-11_Updated-IDS_N3044-10002US21.pdf	1042985 55947d2015d91336e543eda177a3d54cdbdaa9cd	no	4

Warnings:

Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
2	Non Patent Literature	a-IPR2017-00549_2017-05-15_Decision.pdf	4402747 d896d67db4d3c6448d6c7a4b70477d2f1aea99a7	no	13
Warnings:					
Information:					
3	Non Patent Literature	a-IPR2017-00577_2017-07-07_Decision.pdf	8699683 87b4c4b5ea26c5b285c0b23b5e112dbf12bec688	no	22
Warnings:					
Information:					
4	Non Patent Literature	a-IPR2017-00577_2017-07-07_SO.pdf	1615453 a50f8ff7e91f5c61ef6a115abb5001ab03f99e7f	no	6
Warnings:					
Information:					
5	Non Patent Literature	a-IPR2017-00667_2017-07-21_Decision.pdf	10135206 54a877e1630c938557287fd04b5d3970f5c44e31	no	26
Warnings:					
Information:					
6	Non Patent Literature	a-IPR2017-00668_2017-07-21_Decision.pdf	8875355 9dacbfd9e61da404b6f79181bb11c3d9ab0da7ad	no	23
Warnings:					
Information:					
			Total Files Size (in bytes):	34771429	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/715,486	Filing Date 05/18/2015	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 08/11/2017

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 29	Minus	** 21	= 8	X $40 =	320
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $210 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	320

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
TAMMY D. MCBETH BROWN

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 08/22/2017

Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

EXAMINER
BANSAL, GURTEJ

ART UNIT	PAPER NUMBER
2139	

DATE MAILED: 08/22/2017

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/715,486	05/18/2015	Jeffrey C. Solomon	N3044.10002US21	1537

TITLE OF INVENTION: MEMORY MODULE WITH DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	11/22/2017

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Petitioners
Ex. 1057, p. 412

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 08/22/2017
Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/715,486	05/18/2015	Jeffrey C. Solomon	N3044.10002US21	1537

TITLE OF INVENTION: MEMORY MODULE WITH DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	11/22/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
BANSAL, GURTEJ	2139	711-105000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Petitioners
Ex. 1057, p. 413

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/715,486	05/18/2015	Jeffrey C. Solomon	N3044.10002US21	1537

79141 7590 08/22/2017

Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

EXAMINER	
BANSAL, GURTEJ	

ART UNIT	PAPER NUMBER
2139	

DATE MAILED: 08/22/2017

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/715,486	Applicant(s) SOLOMON ET AL.	
	Examiner GURTEJ BANSAL	Art Unit 2139	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Examiner initiated interview dated August 16, 2017*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-9, 11-17, and 22-34*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date See Continuation Sheet
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20170816* .
5. ☒ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

Continuation of Attachment(s) 2. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date: 08/11/2017; 08/11/2017.

Petitioners
Ex. 1057, p. 417

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in an interview with JAMIE ZHENG on August 15, 2017.

The application has been amended as follows:

IN THE SPECIFICATION

Please replace Paragraphs [0011]-[0013] with the following:

[0011] In certain embodiments, a memory module is operable in a computer system to communicate data with a memory controller of the computer system via a memory ~~data~~ bus in response to memory commands received from the memory controller. The memory commands including a first memory command and a subsequent second memory command~~,~~. The ~~the~~ first memory command is to cause the memory module to receive or output a first data burst and the second memory command is to cause the memory module to receive or output a second data burst. The memory module comprises a printed circuit board, a register coupled to the printed circuit board, a

plurality of memory integrated circuits mounted on the printed circuit board, a buffer, and logic coupled to the buffer ~~a plurality of memory integrated circuits including at least one first memory integrated circuit and at least one second memory integrated circuit, and further comprises a buffer coupled~~ coupled between the at least one first memory integrated circuit and the data bus, and between the at least one second memory integrated circuit and the data bus. The buffer couples the at least one first memory integrated circuit to the data bus and isolates the at least one second memory integrated circuit from the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command. The buffer then couples the at least one second memory integrated circuit to the data bus and isolates the at least one first memory integrated circuit from the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command.

[0012] In certain embodiments, the printed circuit board has a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system. The register is configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command. The plurality of memory integrated circuits are arranged in a plurality of ranks including a first rank and a second rank, and including at least one first memory integrated circuit in the first rank and at least one second memory integrated

circuit in the second rank. The first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command. The second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command ~~Certain embodiments provide a method of operating a memory module coupled to a memory controller via a memory bus that includes a control/address (C/A) bus and a data bus. The memory module comprises memory integrated circuits, including at least one first memory integrated circuit and at least one second memory integrated circuit. The method comprises receiving from the memory controller a first set of input C/A signals associated with a first memory command via the C/A bus, the first memory command to cause the memory module to receive or output a first data burst; generating a first set of output C/A signals in response to the first set of input C/A signals, the first set of output C/A signals causing the at least one first memory integrated circuit to receive or output the first data burst; receiving from the memory controller a second set of input control/address signals associated with a second memory command via the C/A bus, the second memory command to cause the memory module to receive or output a second data burst; generating a second set of output C/A signals in response to the second set of input C/A signals, the second set of output C/A signals causing the at least one second memory integrated circuit to receive or output the second data burst; coupling the at least one first memory integrated circuit to the data bus and isolating the~~

~~at least one second memory integrated circuit from the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command; and coupling the at least one second memory integrated circuit to the data bus and isolating the at least one first memory integrated circuit from the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command~~.

.

[0013] In certain embodiments, the buffer is coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus. The logic is configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer. The logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer. The second control signals are different from the first control signals. a circuit is configured to be mounted on a memory module that is operable to communicate data with a memory controller via a data bus in response to memory commands received from the memory controller. ~~The memory module including at least one first memory integrated circuit and at least one second memory integrated circuit. The memory commands including a first memory command and a subsequent second memory command, the~~

~~first memory command to cause the at least one first memory integrated circuit to receive or output a first data burst and the second memory command to cause the at least one second memory integrated circuit to receive or output a second data burst. The circuit comprises logic that couples the at least one first memory integrated circuit to the data bus and that isolates the at least one second memory integrated circuit from the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command. The logic then couples the at least one second memory integrated circuit to the data bus and isolates the at least one first memory integrated circuit from the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command~~

Please replace the Abstract of the Disclosure with the following:

ABSTRACT OF THE DISCLOSURE

A memory module is operable to communicate data with a memory controller via a memory ~~data~~ bus in response to memory commands received from the memory controller. The memory module comprises a plurality of memory integrated circuits arranged in ranks and including at least one first memory integrated circuit in a first rank and at least one second memory integrated circuit in a second rank, and further comprises a buffer ~~that couples~~ coupled between the at least one first memory integrated circuit and ~~to~~ the memory~~data~~ bus and between ~~isolates~~ the at least one second memory integrated circuit and ~~from~~ the memory~~data~~ bus. The memory module further comprises logic providing first control signals to the buffer to enable communication of ~~while the memory module is receiving or outputting~~ a first data burst between the memory controller and the at least one first memory integrated circuit through the buffer in response to a first memory command, and providing second control signals to the buffer to enable communication of a second data burst between~~.~~ ~~The buffer then couples~~ the at least one second memory integrated circuit and the memory bus through the buffer ~~to the data bus and isolates the at least one first memory integrated circuit from the data bus while the memory module is receiving or outputting a second data burst~~ in response to a second memory command.

IN THE CLAIMS

1. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory ~~data~~ bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command;

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank, wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected

to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command;

a buffer coupled between the at least one first memory integrated circuit and the memory ~~data~~ bus, and between the at least one second memory integrated circuit and the memory ~~data~~ bus; and

logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.

2. (Currently Amended) The memory module of claim 1, wherein the buffer is configured to isolate both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory ~~data~~ bus when the memory module is not being accessed by the memory controller.

3. (Previously Presented) The memory module of claim 1, wherein the first memory command includes at least one first chip select signal and the second memory command includes at least one second chip select signal.

4. (Previously Presented) The memory module of claim 3, wherein the memory module produces at least third and fourth chip select signals in response to the first memory command, the third chip select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the fourth chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.

5. (Previously Presented) The memory module of claim 4, wherein the memory module produces at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first memory command, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an active value to cause the at least one second memory integrated circuit to receive or output data signals in response to the second memory command.

6. (Currently Amended) The memory module of claim 1, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to

back adjacent read commands, and wherein the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory ~~data~~ bus, and wherein the buffer is configured to prevent the first burst of data strobe signals and the second burst of data strobe signals from colliding with each other.

7. (Previously Presented) The memory module of claim 6, wherein each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval, and wherein the buffer is configured to combine the first burst of data strobe signals and the second burst of data strobe signals into a combined burst of data strobe signals that does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals.

8. (Previously Presented) The memory module of claim 1, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.

9. (Previously Presented) The memory module of claim 1, further comprising an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits.

10. (Cancelled)

11. (Currently Amended) A method of operating a memory module coupled to a memory controller via a memory bus ~~including a control/address (C/A) bus and a data bus~~, the memory module comprising memory integrated circuits arranged in ranks and mounted on a printed circuit board having a plurality of edge connections coupled to the memory bus, the memory integrated circuits including at least one first memory integrated circuit in a first rank and at least one second memory integrated circuit in a second rank, the method comprising:

receiving at one or more circuits coupled to the printed circuit board a first set of input command and address signals representing a first memory command from the memory controller ~~a first set of input control/address (C/A) signals associated with a first memory command~~ via the memory ~~C/A~~ bus, the first memory command to cause the memory module to receive or output a first data burst;

generating a first set of output command and address ~~C/A~~ signals in response to the first set of input command and address ~~C/A~~ signals, the first set of output command and address ~~C/A~~ signals selecting ~~causing t~~he first rank to receive or output the first data burst;

receiving at the one or more circuits a second set of input command and address signals representing a second memory command from the memory controller ~~a second set of input control/address signals associated with a second memory command~~ via the memory ~~C/A~~ bus, the second memory command to cause the memory module to receive or output a second data burst;

generating a second set of output command and address ~~C/A~~ signals in response to the second set of input command and address ~~C/A~~ signals, the second set of output command and address ~~C/A~~ signals selecting ~~causing~~ the second rank to receive or output the second data burst;

in response to the first memory command, providing first control signals to a buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer; and

in response to the second memory command, providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.

12. (Original) The method of claim 11, further comprising isolating the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory ~~data~~ bus when the memory module is not being accessed by the memory system.

13. (Currently Amended) The method of claim 11, wherein the first set of input command and address ~~C/A~~ signals include at least one input chip-select signal, the method further comprising generating a first chip select signal and a second chip select signal in response to the first set of input command and address ~~C/A~~ signals, the first chip-select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to

receive or output data signals in response to the first memory command, the second chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.

14. (Currently Amended) The method of claim 11, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein the memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory ~~data~~ bus, the method further comprising combining the first burst of data strobe signals and the second burst of data strobes to form a third burst of data strobe signals on the memory ~~data~~ bus.

15. (Previously Presented) The method of claim 14, wherein each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval, and wherein the third burst of data strobes does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals.

16. (Original) The method of claim 11, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of the memory integrated circuits.

17. (Previously Presented) The method of claim 11, further comprising reporting an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of the memory integrated circuits.

18. (Cancelled)

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Previously Presented) The memory module of claim 1, wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is selected to communicate data with the memory controller.

23. (Previously Presented) The memory module of claim 22, the at least one of the circuit components is configured to provide the first data path in response to the first control signals, and is configured to provide the second data path in response to the second control signals.

24. (Previously Presented) The memory module of claim 1, wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits.

25. (Previously Presented) The memory module of claim 1, wherein the logic is configured to enable the communication of the first data burst between the at least one first memory integrated circuit and the memory controller in accordance with a latency value.

26. (Previously Presented) The memory module of claim 25, wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the first data burst through the buffer.

27. (Previously Presented) The method of claim 11, wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is caused to communicate data with the memory controller.

28. (Previously Presented) The method of claim 11, wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits.

29. (Currently Amended) The memory module ~~method~~ of claim 1, further comprising determining a latency value, wherein the communication of the first data burst between

the at least one first memory integrated circuit and the memory controller is enabled in accordance with the latency value.

30. (Previously Presented) The memory module of claim 1, wherein the memory module is further coupled to the memory controller using an on-die-termination (ODT) bus, wherein each of the plurality of memory devices includes an ODT circuit, the memory module further comprising a termination circuit external to any of the plurality of memory devices, wherein the termination circuit is coupled to the ODT bus and to the ODT circuit of at least one of the plurality of memory devices, wherein the termination circuit is configured to provide external termination of the at least one of the plurality of memory devices in response to an ODT signal on the ODT bus, and wherein the ODT circuit in the at least one of the plurality of memory devices is disabled.

31. (Previously Presented) The memory module of claim 1, wherein the buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the first data burst or the second data burst through the buffer.

32. (Previously Presented) The memory module of claim 25, wherein the logic is further configured to determine the latency value.

33. (Previously Presented) The memory module of claim 25, wherein the logic is further configured to enable the communication of the second data burst between the at least one second memory integrated circuit and the memory controller in accordance with the latency value.

34. (Previously Presented) The memory module of claim 33, wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the second data burst through the buffer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GURTEJ BANSAL whose telephone number is (571)270-5588. The examiner can normally be reached on Monday - Friday, 7:30 a.m. - 5:00 p.m., EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571)272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GURTEJ BANSAL
Primary Examiner
Art Unit 2139

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	14/715,486	SOLOMON ET AL.	
	Examiner	Art Unit	
	GURTEJ BANSAL	2139	

All participants (applicant, applicant's representative, PTO personnel):

(1) *GURTEJ BANSAL*. (3)_____.

(2) *JAMIE ZHENG*. (4)_____.

Date of Interview: *16 August 2017*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☒103 ☒Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1*.

Identification of prior art discussed: _____.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Examiner discussed amendments to the claims to further distinguish the claimed invention from the cited prior art. Applicant agreed with the amendments and authorized the Examiner to make the suggested amendments to place the claims in condition for allowance.

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	

Memory **rank** decoder for a multi-**rank** Dual Inline Memory Module (**DIMM**)

S Raghuram - US Patent 7,266,639, 2007 - Google Patents

... of their printed circuit boards (PCB) a dual inline memory modules (**DIMMS**) comprise memory **...** The invention further provides a dual inline memory module (**DIMM**) having a predetermined number (N **...** memory module 3 has a minimum number S of memory **rank** selection **signals ...**

Cited by 85 Related articles All 4 versions Cite Save

Single **rank** memory module for use in a two-**rank** memory module system

T Wong, CC Fang, DJ Jeffrey, NN Duncan - US Patent 6,961,281, 2005 - Google Patents

... noted that depending on the implementation, address **signals** AD12-AD15 received on the **DIMM** connector from **...** 2 while using higher capacity 256 MB SDRAM devices in a single **rank** 16 MB **...** family of memory modules that are referred to as next generation (NG) **DIMMs** by Sun **...**

Cited by 109 Related articles All 4 versions Cite Save

DRAM interface circuits having enhanced skew, slew rate and impedance **control**

P Murtagh, RT Knaack - US Patent 7,079,446, 2006 - Google Patents

... US8386722, Jun 23, 2008, Feb 26, 2013, Google Inc. Stacked **DIMM** memory interface. **...** Hybrid memory module. US8438328, Feb 14, 2009, May 7, 2013, Google Inc. Emulation of abstracted **DIMMs** using abstracted DRAMs. **...** Multi-**rank** partial width memory modules. **...**

Cited by 107 Related articles All 4 versions Cite Save

Non-standard dual in-line memory modules with more than two **ranks** of memory per module and multiple serial-presence-detect devices to simulate multiple modules

R Pauley, J Bhakta, W Gervasi - US Patent App. 10/913,700, 2004 - Google Patents

... relates generally to configurations of Dual In-Line Memory Modules (**DIMMs**) that contain more than two **ranks** of memory per **DIMM**. **...** [0007]. While DDR **DIMMs** have two **...** use only two **rank**-select inputs (S0#, S1#) for each memory slot, leaving the remaining two **rank**-select inputs **...**

Cited by 54 Related articles All 2 versions Cite Save

Logical to physical address mapping of chip selects

DA Thompson, DS McGinnis, SA McKinnon - US Patent 7,133,960, 2006 - Google Patents

... by **CS**(6), which **controls** the first **rank** and **CS**(7), which **controls** the second **rank** of the **...** the primary memory module of the second mirrored memory pair may be located at **DIMM**#2 140 **...** **CS**(4). Additionally, for the purpose of this example, it will be assumed that the **DIMMs** may be **...**

Cited by 103 Related articles All 2 versions Cite Save

Method and apparatus for refreshing a non-clocked memory

M Bermingham, CS Maclellan, R Sheikh - US Patent 6,058,451, 2000 - Google Patents

... US8386722, Jun 23, 2008, Feb 26, 2013, Google Inc. Stacked **DIMM** memory interface. **...** US8438328, Feb 14, 2009, May 7, 2013, Google Inc. Emulation of abstracted **DIMMs** using abstracted DRAMs. **...** Multi-**rank** partial width memory modules. **...**

Cited by 74 Related articles All 2 versions Cite Save

Memory expansion module with stacked memory packages and a serial storage unit

T Wong, J Carrillo, J Robinson, C Fang… - US Patent …, 2004 - Google Patents

... US8250295, Jan 5, 2004, Aug 21, 2012, Smart Modular Technologies, Inc. Multi-**rank** memory module that emulates a memory module having a different number of **ranks**. **...** Stacked **DIMM** memory interface. **...** Emulation of abstracted **DIMMs** using abstracted DRAMs. **...**

Cited by 131 Related articles All 2 versions Cite Save

Petitioners
Ex. 1057, p. 437

Write clock and data window tuning based on **rank** select

PA LaBerge, J Dodd - US Patent 6,804,764, 2004 - Google Patents

... Each **DIMM** generally includes a plurality of memory devices such as Synchronous Dynamic Random Access **...** In this embodiment, each of the eight memory **ranks** 32A-32H is capable of **...** 36 may include an error detection and correction (ECC) bus for each memory **rank** 32A-32H **...**

Cited by 167 Related articles All 4 versions Cite Save

Memory devices with buffered command address bus

PA LaBerge - US Patent 7,149,841, 2006 - Google Patents

... In an alternative embodiment, if the switches are implemented on the **DIMMs** and there is more than **...** bus is driven to the **DIMM** when any one of the **ranks** on the **DIMM** is selected **...** module 506, which has one **rank** of memory devices **controlled** by CS1 and another **rank** of memory **...**

Cited by 30 Related articles All 4 versions Cite Save

Dynamically setting burst length of memory device by applying **signal** to at least one external pin during a read or write transaction

CS Johnson - US Patent 7,149,824, 2006 - Google Patents

... US8386722, Jun 23, 2008, Feb 26, 2013, Google Inc. Stacked **DIMM** memory interface. **...** Hybrid memory module. US8438328, Feb 14, 2009, May 7, 2013, Google Inc. Emulation of abstracted **DIMMs** using abstracted DRAMs. **...** Multi-**rank** partial width memory modules. **...**

Cited by 66 Related articles All 2 versions Cite Save

Petitioners
Ex. 1057, p. 438

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14715486
Filing Date	2015-05-18
First Named Inventor	Jeffrey C. Solomon
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	N3044.10002US21

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	Application Number	14715486
	Filing Date	2015-05-18
	First Named Inventor	Jeffrey C. Solomon
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	Attorney Docket Number	N3044.10002US21

	1	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, DECISION Institution of Inter Partes Review, entered May 15, 2017.	
	2	Inter Partes Review of U.S. Patent No. 7,532,537, Case No. IPR2017-00667, DECISION Institution of Inter Partes Review, entered July 21, 2017.	
	3	Inter Partes Review of U.S. Patent No. 7,532,537, Case No. IPR2017-00668, DECISION Institution of Inter Partes Review, entered July 21, 2017.	
	4	Inter Partes Review of U.S. Patent No. , Case No. IPR2017-00577, DECISION Institution of Inter Partes Review, entered May 15, 2017.	
	5	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, DECISION Institution of Inter Partes Review, entered July 7, 2017.	
	6	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, SCHEDULING ORDER, entered July 7, 2017.	

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Examiner Signature	/GURTEJ BANSAL/	Date Considered	08/17/2017

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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	Application Number	14715486
	Filing Date	2015-05-18
	First Named Inventor	Jeffrey C. Solomon
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	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

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The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/JAMIE J. ZHENG/	Date (YYYY-MM-DD)	2017-08-11
Name/Print	Jamie J. Zheng	Registration Number	51167

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	38	burst with rank with select$3	US-PGPUB; USPAT	OR	ON	2017/08/17 08:16
L2	141	burst same rank$1 same select$3	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:16
L3	113	buffer same parallel with (ranks dimms)	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:34
L4	5288	G06F13/1673.cpc. G011C7/1072.cpc. G011C15/00.cpc. G06F13/4282.cpc. G06F13/4243.cpc.	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:36
L5	299	DIMM same CS	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:46
L6	322	DIMM same (CS chip$1select)	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:46
S1	3717	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2011/07/03 21:54
S2	75	365/189.2.ccls.	USPAT	OR	OFF	2011/07/03 21:54
S3	104	365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:27
S4	6392	abstract$3 with (DRAM DIMM memory)	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:40
S5	48	abstracted adj2 (DRAM DIMM memory)	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:40
S6	109	abstracted adj2 (DRAM DIMM memory) or aDRAM	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:42
S7	1	"7515453".pn.	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:00
S8	771	interface same (DDR2 and (DDR or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:17
S9	504	interface with (DDR2 and (DDR or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:18
S10	5	365/189.2.ccls. and (DDR2 and (DDR or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:19
S11	10	365/189.2.ccls. and (DDR and (DDR2 or	US-	OR	OFF	2011/07/05

		DRAM or SRAM or DDR3 or flash))	PGPUB; USPAT			19:24
S12	1	"20070088995".pn.	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:29
S13	241	CKE with precharge	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:48
S14	0	365/189.2.ccls and CKE with precharge	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:48
S15	111	CKE with precharge same power	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:48
S16	36	silent with alarm with clock	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:54
S17	0	silent with alarm with clock and lark.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:54
S18	0	silent with alarm with clock and hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:54
S19	4	alarm with clock and hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:55
S20	0	julia-hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:58
S21	2	julia.in. and hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:59
S22	16	lark.as.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:00
S23	629	precharge same power and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:01
S24	3	precharge same power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:03
S25	1	self with refresh and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:08
S26	3	pre$1charge with power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:09
S27	11	pre$1chargesame power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:09
S28	3	pre$1charge same power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:09
S29	55	pre$1charge same power and CKE and DRAM same DDR same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:22
S30	59	pre$1charge same power and CKE and	US-	OR	OFF	2011/07/05

		DRAM same DDR2	PGPUB; USPAT			22:25
S31	73	pre$1charge same power and CKE and DDR same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:26
S32	89	refresh same power and CKE and DDR same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:17
S33	10	365/189.2.ccls. and (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:27
S34	54	SPD and (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:29
S35	16	SPD same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:29
S36	0	module with transmit same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:45
S37	19	memory with transmit same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:45
S38	23	configure same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:48
S39	14	configure with (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:48
S40	1	DDR with DRAM and tCKE with timing with memory	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:52
S41	273	intelligent adj3 (buffer or register)	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:01
S42	9	intelligent adj3 (buffer or register) and pre$charge	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:01
S43	298	SPD same2 (pre$1charge refresh)	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:03
S44	197	SPD same (pre$1charge refresh)	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:03
S45	59	SPD same2 (pre$1charge refresh) and DDR same DRAM	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:03
S46	38	SPD same (pre$1charge refresh) and DDR same DRAM	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:04
S47	3	SPD same (pre$1charge refresh) and DDR same DRAM and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:05
S48	59	SPD same2 (pre$1charge refresh) and DDR same DRAM	US-PGPUB; USPAT	OR	OFF	2011/07/06 10:59
S49	1	SPD same pre$1charge with power	US-	OR	OFF	2011/07/06

			PGPUB; USPAT			11:01
S50	25	SPD same self adj refresh	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:01
S51	0	SPD same self adj refresh and DDR	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:04
S52	2	SPD same self adj refresh and DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:04
S53	22	SPD same self adj refresh same power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:07
S54	2	SPD same self adj refresh and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:24
S55	0	SPD same self adj refresh and tCKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:26
S56	0	SPD same pre$1charge and tCKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:27
S57	2617837	SPD swith power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:29
S58	578	SPD with power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:29
S59	16	SPD with power same (self adj refresh self$1refresh pre adj charge pre$charge)	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:30
S60	21	SPD same self adj refresh and (pre$1charge or pre adj charge)	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:37
S61	1	"20050246558".pn.	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:41
S62	2	SPD same power with management with mode	US-PGPUB; USPAT	OR	OFF	2011/07/06 12:40
S63	13	365/189.2.ccls. and CS	USPAT	OR	OFF	2011/07/06 12:55
S64	21	365/189.2.ccls. and CS	US-PGPUB; USPAT	OR	OFF	2011/07/06 12:55
S65	171	DIMM same CS	US-PGPUB; USPAT	OR	OFF	2011/07/06 13:00
S66	53	365/189.2.ccls. and (tRP tRCD TWL tRFC timing tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:34
S67	7	365/189.2.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:34
S68	1631	"365".clas. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC	US-PGPUB;	OR	OFF	2011/07/06 14:36

		tRRD tRTP tWR tWTR)	USPAT			
S69	0	365/189.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S70	446	365/189.$.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S71	36	365/189.$.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR) and DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S72	1	365/189.$.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR) same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:37
S73	3	burst with plurality with DIMM	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:43
S74	0	burst with each with DIMM	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:44
S75	6	burst with multiple with DIMM	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:44
S76	6	burst with multiple with DIMM and read	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:46
S77	5	burst with multiple with DIMM same read	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:47
S78	11	burst with DIMMs same read	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:47
S79	0	365/189.2.ccls. and CKE with (high and low)	USPAT	OR	OFF	2011/07/06 16:19
S80	529	CKE with (high and low)	USPAT	OR	OFF	2011/07/06 16:20
S81	17	CKE with (high and low) and DDR2	USPAT	OR	OFF	2011/07/06 16:20
S82	0	365/189.2.ccls. and CKE with (high and low)	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:20
S83	44	CKE with (high and low) and DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:21
S84	87	CKE with (high and low) same pre$1charge	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:24
S85	0	CKE with (high and low) same pre$1charge same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:24
S86	0	CKE with (high and low) same self adj refresh same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:25
S87	0	CKE with ((high and low) or assert) same self adj refresh same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:25
S88	0	CKE with ((high and low) or assert) same	US-	OR	OFF	2011/07/06

		pre$1fetch same SPD	PGPUB; USPAT			16:25
S89	0	CKE with (high or low or assert) same pre$1fetch same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:26
S90	0	CKE with (high or low or assert) same pre$1fetch same2 SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:26
S91	2	CKE with (high or low or assert) same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:26
S92	10	SPD same2 CKE with (high or low or assert)	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:27
S93	1	"20090216936".pn.	US-PGPUB; USPAT	OR	OFF	2012/01/20 18:08
S94	1	"20090216939".pn.	US-PGPUB; USPAT	OR	OFF	2012/01/20 18:17
S95	152	buffer with DRAM with protocol	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:25
S96	152	buffer$3 with DRAM with protocol	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:37
S97	572	buffer with $1RAM with protocol	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:38
S98	1	"20030131160".pn.	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:47
S99	1729	buffer with $1RAM with (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:48
S100	626	buffer with DRAM with (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:48
S101	124	buffer with chip with DRAM with (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:51
S102	185	buffer near5 DRAM near5 (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:14
S103	499	buffer with DRAM with type	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:18
S104	51	buffer with DRAM with type with (multiple different tim$3 various)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:19
S105	224	buffer with DRAM with DDR	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:21
S106	3	buffer with DRAM with (timing signal) with adjust	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:32
S107	146	buffer with DRAM with (timing signal)	US-	OR	OFF	2012/01/21

		with delay	PGPUB; USPAT			00:32
S108	31	buffer with DRAM with (timing signal) with DDR$1	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:32
S109	70	buffer with DRAM with (timing signal protocol) and buffer with DDR$1 with (timing signal protocol)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:37
S110	118	buffer with DRAM with (timing signal protocol) and buffer with SDRAM with (timing signal protocol)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:48
S111	36	buffer with DRAM with SDRAM with interface	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:52
S112	48	buffer with DRAM with (SDRAM DDR2 DDR3) with interface	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:52
S113	73	interface with buffer with DRAM with (DDR$1 SDRAM)	US-PGPUB; USPAT	OR	OFF	2012/01/21 02:03
S114	141	interface same buffer with DRAM with (DDR$1 SDRAM)	US-PGPUB; USPAT	OR	OFF	2012/01/21 02:10
S115	2	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/15 14:11
S116	64	DIMM with DRAM and CS with (DIMM DRAM) and buffer with (DIMM DRAM)	US-PGPUB; USPAT	OR	OFF	2013/01/15 14:12
S117	1	"5918229".pn.	US-PGPUB; USPAT	OR	OFF	2013/01/18 14:08
S118	1	"20060184942".pn.	US-PGPUB; USPAT	OR	OFF	2013/01/18 14:35
S119	130	(different multiple distinct) with file adj locking	US-PGPUB; USPAT	OR	OFF	2013/01/18 17:46
S120	0	abstracted with DIMM and DRAM	USPAT	OR	OFF	2013/01/21 13:21
S121	0	abstracted with DIMM	USPAT	OR	OFF	2013/01/21 13:21
S122	2	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 13:21
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S133	3	("20050038924" | "20080052462" | "6681301").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/01/21 22:03
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S136	2185	DRAM with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:35
S137	31	DRAM with DIMM and DIMM with virtual$5	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:35
S138	43	DRAM with DIMM and CS with module	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:39
S139	43	virtual with DIMM and DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:49
S140	57	buffer with CS and DIMM with DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:16
S141	2	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:22
S142	37	virtual$5 near3 DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:22
S143	29	virtual$5 near3 DIMM and DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:22
S144	541	(plurality multiple) with DIMM with single	US-PGPUB;	OR	ON	2013/01/21 23:25

			USPAT			
S145	200	(plurality multiple) near3 DIMM with single	US-PGPUB; USPAT	OR	ON	2013/01/21 23:25
S146	170	(plurality multiple) near3 DIMM with single and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/21 23:25
S147	132	logical with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/21 23:35
S148	112	logical with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/21 23:35
S149	334	(group) with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/22 00:47
S150	55	emulat$3 with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/22 00:52
S151	71	virtual with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/22 09:39
S152	10	(plurality multiple) with virtual with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/22 09:40
S153	47	(plurality multiple) with (virtual logical emulat$3) with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/22 09:40
S154	1	"7133960".pn.	US-PGPUB; USPAT	OR	ON	2013/01/22 09:42
S155	17	rank with (appear$3) with DIMM	USPAT	OR	OFF	2013/01/30 13:21
S159	180	(virtual logical abstract$3) with DIMM	US-PGPUB; USPAT	OR	ON	2013/02/18 23:49
S160	22	(virtual logical abstract$3) adj DIMM	US-PGPUB; USPAT	OR	ON	2013/02/18 23:49
S161	344	(virtual logical abstract$3) adj RAM	US-PGPUB; USPAT	OR	ON	2013/02/19 00:01
S162	98	(virtual logical abstract$3) adj DRAM	US-PGPUB; USPAT	OR	ON	2013/02/19 00:01
S168	2	"201100052062".pn. "5910010".pn. "5222014".pn.	US-PGPUB; USPAT	OR	OFF	2013/04/16 23:55
S169	18	US-20030110339-$.DID. OR US-20030174569-$.DID. OR US-20040049624-$.DID. OR US-20050044302-$.DID. OR US-20060277355-$.DID. OR US-20080130364-$.DID. OR US-20080282084-$.DID. OR US-20080282341-$.DID. OR US-20090049266-$.DID. OR US-20090070520-$.DID. OR US-	US-PGPUB; USPAT	OR	OFF	2013/07/24 15:48

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S170	105	(virtual logical abstract$3) adj DRAM	US-PGPUB; USPAT	OR	ON	2013/07/24 15:59
S171	60	emulat$3 with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/07/24 15:59
S172	4337	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/07/24 16:02
S173	3	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/07/24 16:04
S178	1054	buffer with data with CS	US-PGPUB; USPAT	OR	OFF	2017/04/26 15:45
S179	1637	buffer with DIMM	US-PGPUB; USPAT	OR	OFF	2017/04/26 15:49
S180	100	buffer and fan$4 with (rank dimm)	US-PGPUB; USPAT	OR	OFF	2017/04/26 16:14
S181	249	buffer same parallel with (rank dimm)	US-PGPUB; USPAT	OR	OFF	2017/04/26 16:26
S182	112	buffer same parallel with (ranks dimms)	US-PGPUB; USPAT	OR	OFF	2017/04/26 16:26
S183	60	daisy with chain with DIMM same buffer	US-PGPUB; USPAT	OR	OFF	2017/04/27 00:11
S184	9041	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	US-PGPUB; USPAT	OR	OFF	2017/04/30 15:23
S189	1	bust with rank$1 with select$3	US-PGPUB; USPAT	OR	OFF	2017/08/17 00:07
S190	38	burst with rank$1 with select$3	US-PGPUB; USPAT	OR	OFF	2017/08/17 00:07

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S156	4194	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/01/30 13:35
S157	1321	emulated.clm.	USPAT	OR	OFF	2013/01/30 13:45
S158	3	S156 and S157	USPAT	OR	OFF	2013/01/30 13:45

S163	4205	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/02/19 00:04
S164	1330	emulated.clm.	USPAT	OR	OFF	2013/02/19 00:04
S165	4205	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/02/19 00:04
S166	1330	emulated.clm.	USPAT	OR	OFF	2013/02/19 00:04
S167	3	S165 and S166	USPAT	OR	OFF	2013/02/19 00:04
S174	4343	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/07/24 16:04
S175	4343	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/07/24 16:06
S176	1399	emulated.clm.	USPAT	OR	OFF	2013/07/24 16:06
S177	4	S175 and S176	USPAT	OR	OFF	2013/07/24 16:06
S185	4964	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	USPAT	OR	OFF	2017/04/30 15:24
S186	6228	data.clm. adj path.clm.	USPAT	OR	OFF	2017/04/30 15:28
S187	120	S185 and S186	USPAT	OR	OFF	2017/04/30 15:28
S188	8	S185 and S186 and rank.clm.	USPAT	OR	OFF	2017/04/30 15:28

8/ 17/ 2017 9:18:39 AM
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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14715486
Filing Date	2015-05-18
First Named Inventor	Jeffrey C. Solomon
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	N3044.10002US21

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

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	Filing Date	2015-05-18
	First Named Inventor	Jeffrey C. Solomon
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	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

	1	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, DECISION Institution of Inter Partes Review, entered May 15, 2017.	
	2	Inter Partes Review of U.S. Patent No. 7,532,537, Case No. IPR2017-00667, DECISION Institution of Inter Partes Review, entered July 21, 2017.	
	3	Inter Partes Review of U.S. Patent No. 7,532,537, Case No. IPR2017-00668, DECISION Institution of Inter Partes Review, entered July 21, 2017.	
	4	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, DECISION Institution of Inter Partes Review, entered July 7, 2017.	
	5	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, SCHEDULING ORDER, entered July 7, 2017.	

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EXAMINER SIGNATURE

Examiner Signature	/GURTEJ BANSAL/	Date Considered	08/17/2017

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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	Attorney Docket Number	N3044.10002US21

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/JAMIE J. ZHENG/	Date (YYYY-MM-DD)	2017-08-11
Name/Print	Jamie J. Zheng	Registration Number	51167

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14715486	SOLOMON ET AL.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

CPC						
Symbol					**Type**	**Version**
G06F		13	/	1673	F	2013-01-01
G11C		7	/	1072	I	2013-01-01
G11C		15	/	00	I	2013-01-01
G06F		13	/	4282	I	2013-01-01
G06F		13	/	4243	I	2013-01-01
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CPC Combination Sets							
Symbol				**Type**	**Set**	**Ranking**	**Version**
			/				
			/				

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	29	
/GURTEJ BANSAL/ Primary Examiner.Art Unit 2139	08/17/2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

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	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
`		G 0 6 F 12 / 00 (2006.01.01)	

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 29	
/GURTEJ BANSAL/ Primary Examiner.Art Unit 2139 (Primary Examiner)	08/17/2017 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Petitioners
Ex. 1057, p. 469

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14715486	SOLOMON ET AL.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	25	17	19	33										
2	2		18	20	34										
9	3		19												
10	4		20												
11	5		21												
12	6	14	22												
13	7	15	23												
3	8	5	24												
4	9	16	25												
	10	17	26												
21	11	26	27												
22	12	27	28												
23	13	6	29												
28	14	7	30												
29	15	8	31												
24	16	18	32												

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 29	
/GURTEJ BANSAL/ Primary Examiner.Art Unit 2139 (Primary Examiner)	08/17/2017 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14715486	SOLOMON ET AL.
	Examiner	Art Unit
	GURTEJ BANSAL	2139

CPC- SEARCHED		
Symbol	Date	Examiner
G06F13/1673.cpc. G011C7/1072.cpc. G011C15/00.cpc. G06F13/4282.cpc. G06F13/4243.cpc.	08/17/2017	GB

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
Text Search in EAST (See Attached)	04/30/2017	GB
Inventor Search in PE2E	04/30/2017	GB
NPL Search in Google Scholar (See Attached)	04/30/2017	GB
Updated Text Search in EAST (See Attached)	08/16/2017	GB
UpdatedNPL Search in Google Scholar (See Attached)	08/16/2017	GB

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	04/30/2017	GB

	/GURTEJ BANSAL/ Primary Examiner.Art Unit 2139

INTERFERENCE SEARCH			
US Class/ CPC Symbol	**US Subclass / CPC Group**	**Date**	**Examiner**
	G06F13/1673.cpc. G011C7/1072.cpc. G011C15/00.cpc. G06F13/4282.cpc. G06F13/4243.cpc.	08/17/2017	GB

	/GURTEJ BANSAL/ Primary Examiner.Art Unit 2139

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L5	35	DIMM same rank same burst	US-PGPUB; USPAT	OR	OFF	2017/08/17 15:23
S1	3717	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2011/07/03 21:54
S2	75	365/189.2.ccls.	USPAT	OR	OFF	2011/07/03 21:54
S3	104	365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:27
S4	6392	abstract$3 with (DRAM DIMM memory)	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:40
S5	48	abstracted adj2 (DRAM DIMM memory)	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:40
S6	109	abstracted adj2 (DRAM DIMM memory) or aDRAM	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:42
S7	1	"7515453".pn.	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:00
S8	771	interface same (DDR2 and (DDR or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:17
S9	504	interface with (DDR2 and (DDR or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:18
S10	5	365/189.2.ccls. and (DDR2 and (DDR or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:19
S11	10	365/189.2.ccls. and (DDR and (DDR2 or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:24
S12	1	"20070088995".pn.	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:29
S13	241	CKE with precharge	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:48
S14	0	365/189.2.ccls and CKE with precharge	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:48
S15	111	CKE with precharge same power	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:48
S16	36	silent with alarm with clock	US-	OR	OFF	2011/07/05

			PGPUB; USPAT			21:54
S17	0	silent with alarm with clock and lark.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:54
S18	0	silent with alarm with clock and hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:54
S19	4	alarm with clock and hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:55
S20	0	julia-hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:58
S21	2	julia.in. and hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:59
S22	16	lark.as.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:00
S23	629	precharge same power and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:01
S24	3	precharge same power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:03
S25	1	self with refresh and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:08
S26	3	pre$1charge with power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:09
S27	11	pre$1chargesame power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:09
S28	3	pre$1charge same power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:09
S29	55	pre$1charge same power and CKE and DRAM same DDR same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:22
S30	59	pre$1charge same power and CKE and DRAM same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:25
S31	73	pre$1charge same power and CKE and DDR same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:26
S32	89	refresh same power and CKE and DDR same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:17
S33	10	365/189.2.ccls. and (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:27
S34	54	SPD and (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:29
S35	16	SPD same (pre$1charge refresh) and CKE	US-	OR	OFF	2011/07/06

			PGPUB; USPAT			00:29
S36	0	module with transmit same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:45
S37	19	memory with transmit same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:45
S38	23	configure same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:48
S39	14	configure with (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:48
S40	1	DDR with DRAM and tCKE with timing with memory	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:52
S41	273	intelligent adj3 (buffer or register)	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:01
S42	9	intelligent adj3 (buffer or register) and pre$charge	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:01
S43	298	SPD same2 (pre$1charge refresh)	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:03
S44	197	SPD same (pre$1charge refresh)	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:03
S45	59	SPD same2 (pre$1charge refresh) and DDR same DRAM	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:03
S46	38	SPD same (pre$1charge refresh) and DDR same DRAM	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:04
S47	3	SPD same (pre$1charge refresh) and DDR same DRAM and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:05
S48	59	SPD same2 (pre$1charge refresh) and DDR same DRAM	US-PGPUB; USPAT	OR	OFF	2011/07/06 10:59
S49	1	SPD same pre$1charge with power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:01
S50	25	SPD same self adj refresh	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:01
S51	0	SPD same self adj refresh and DDR	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:04
S52	2	SPD same self adj refresh and DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:04
S53	22	SPD same self adj refresh same power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:07
S54	2	SPD same self adj refresh and CKE	US-	OR	OFF	2011/07/06

			PGPUB; USPAT			11:24
S55	0	SPD same self adj refresh and tCKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:26
S56	0	SPD same pre$1charge and tCKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:27
S57	2617837	SPD swith power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:29
S58	578	SPD with power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:29
S59	16	SPD with power same (self adj refresh self$1refresh pre adj charge pre$charge)	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:30
S60	21	SPD same self adj refresh and (pre$1charge or pre adj charge)	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:37
S61	1	"20050246558".pn.	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:41
S62	2	SPD same power with management with mode	US-PGPUB; USPAT	OR	OFF	2011/07/06 12:40
S63	13	365/189.2.ccls. and CS	USPAT	OR	OFF	2011/07/06 12:55
S64	21	365/189.2.ccls. and CS	US-PGPUB; USPAT	OR	OFF	2011/07/06 12:55
S65	171	DIMM same CS	US-PGPUB; USPAT	OR	OFF	2011/07/06 13:00
S66	53	365/189.2.ccls. and (tRP tRCD TWL tRFC timing tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:34
S67	7	365/189.2.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:34
S68	1631	"365".clas. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S69	0	365/189.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S70	446	365/189.$.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S71	36	365/189.$.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR) and DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S72	1	365/189.$.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR) same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:37
S73	3	burst with plurality with DIMM	US-PGPUB;	OR	OFF	2011/07/06 14:43

			USPAT			
S74	0	burst with each with DIMM	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:44
S75	6	burst with multiple with DIMM	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:44
S76	6	burst with multiple with DIMM and read	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:46
S77	5	burst with multiple with DIMM same read	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:47
S78	11	burst with DIMMs same read	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:47
S79	0	365/189.2.ccls. and CKE with (high and low)	USPAT	OR	OFF	2011/07/06 16:19
S80	529	CKE with (high and low)	USPAT	OR	OFF	2011/07/06 16:20
S81	17	CKE with (high and low) and DDR2	USPAT	OR	OFF	2011/07/06 16:20
S82	0	365/189.2.ccls. and CKE with (high and low)	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:20
S83	44	CKE with (high and low) and DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:21
S84	87	CKE with (high and low) same pre$1charge	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:24
S85	0	CKE with (high and low) same pre$1charge same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:24
S86	0	CKE with (high and low) same self adj refresh same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:25
S87	0	CKE with ((high and low) or assert) same self adj refresh same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:25
S88	0	CKE with ((high and low) or assert) same pre$1fetch same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:25
S89	0	CKE with (high or low or assert) same pre$1fetch same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:26
S90	0	CKE with (high or low or assert) same pre$1fetch same2 SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:26
S91	2	CKE with (high or low or assert) same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:26
S92	10	SPD same2 CKE with (high or low or assert)	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:27
S93	1	"20090216936".pn.	US-	OR	OFF	2012/01/20

			PGPUB; USPAT			18:08
S94	1	"20090216939".pn.	US-PGPUB; USPAT	OR	OFF	2012/01/20 18:17
S95	152	buffer with DRAM with protocol	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:25
S96	152	buffer$3 with DRAM with protocol	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:37
S97	572	buffer with $1RAM with protocol	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:38
S98	1	"20030131160".pn.	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:47
S99	1729	buffer with $1RAM with (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:48
S100	626	buffer with DRAM with (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:48
S101	124	buffer with chip with DRAM with (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:51
S102	185	buffer near5 DRAM near5 (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:14
S103	499	buffer with DRAM with type	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:18
S104	51	buffer with DRAM with type with (multiple different tim$3 various)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:19
S105	224	buffer with DRAM with DDR	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:21
S106	3	buffer with DRAM with (timing signal) with adjust	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:32
S107	146	buffer with DRAM with (timing signal) with delay	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:32
S108	31	buffer with DRAM with (timing signal) with DDR$1	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:32
S109	70	buffer with DRAM with (timing signal protocol) and buffer with DDR$1 with (timing signal protocol)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:37
S110	118	buffer with DRAM with (timing signal protocol) and buffer with SDRAM with (timing signal protocol)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:48
S111	36	buffer with DRAM with SDRAM with interface	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:52
S112	48	buffer with DRAM with (SDRAM DDR2	US-	OR	OFF	2012/01/21

		DDR3) with interface	PGPUB; USPAT			00:52
S113	73	interface with buffer with DRAM with (DDR$1 SDRAM)	US-PGPUB; USPAT	OR	OFF	2012/01/21 02:03
S114	141	interface same buffer with DRAM with (DDR$1 SDRAM)	US-PGPUB; USPAT	OR	OFF	2012/01/21 02:10
S115	2	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/15 14:11
S116	64	DIMM with DRAM and CS with (DIMM DRAM) and buffer with (DIMM DRAM)	US-PGPUB; USPAT	OR	OFF	2013/01/15 14:12
S117	1	"5918229".pn.	US-PGPUB; USPAT	OR	OFF	2013/01/18 14:08
S118	1	"20060184942".pn.	US-PGPUB; USPAT	OR	OFF	2013/01/18 14:35
S119	130	(different multiple distinct) with file adj locking	US-PGPUB; USPAT	OR	OFF	2013/01/18 17:46
S120	0	abstracted with DIMM and DRAM	USPAT	OR	OFF	2013/01/21 13:21
S121	0	abstracted with DIMM	USPAT	OR	OFF	2013/01/21 13:21
S122	2	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 13:21
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S131	104	US-20050289292-$.DID. OR US-20050289317-$.DID. OR US-20060002201-$.DID. OR US-6986118-$.DID. OR US-20060010339-$.DID. OR US-6992501-$.DID. OR US-6992950-$.DID. OR US-20060248387-$.DID. OR US-20060041730-$.DID. OR US-7000062-$.DID. OR US-7003618-$.DID. OR US-7003639-$.DID. OR US-20060038597-$.DID. OR US-20060039204-$.DID. OR US-20060039205-$.DID. OR US-20060041711-$.DID. OR US-7007095-$.DID. OR US-7007175-$.DID. OR US-20060044913-$.DID. OR US-20060044909-$.DID. OR US-7010642-$.DID. OR US-7010736-$.DID. OR US-20060049502-$.DID. OR US-20060050574-$.DID. OR US-20060056244-$.DID. OR US-20060062047-$.DID. OR US-20060067141-$.DID. OR US-7024518-$.DID. OR US-7028215-$.DID. OR US-7026708-$.DID. OR US-7028234-$.DID. OR US-20060085616-$.DID. OR US-7033861-$.DID. OR US-7035150-$.DID. OR US-20060087900-$.DID. OR US-20060090054-$.DID. OR US-20060090031-$.DID. OR US-7043599-$.DID. OR US-7045396-$.DID. OR US-7045901-$.DID. OR US-7046538-$.DID. OR US-20060106951-$.DID. OR US-20060112219-$.DID. OR US-20060112214-$.DID. OR US-7053470-$.DID. OR US-7053478-$.DID. OR US-20060117160-$.DID. OR US-20060117152-$.DID. OR US-7058776-$.DID. OR US-662006D-$.DID. OR US-7058863-$.DID. OR US-20060118933-$.DID. OR US-20060120193-$.DID. OR US-20060123265-$.DID. OR US-7061784-$.DID. OR US-7061823-$.DID. OR US-20060129712-$.DID. OR US-20060126369-$.DID. OR US-20060129755-$.DID. OR US-20060129740-$.DID. OR US-20060133173-$.DID. OR US-20060136791-$.DID. OR US-7066741-$.DID. OR US-20060149982-$.DID. OR US-7075175-$.DID. OR US-7079396-$.DID. OR US-7079441-$.DID. OR US-7079446-$.DID. OR US-7085941-$.DID. OR US-20060174082-$.DID. OR US-7089438-$.DID. OR US-20060176744-$.DID. OR US-20060179333-$.DID. OR US-20060179334-$.DID. OR US-7085152-$.DID. OR US-7093101-$.DID. OR US-20060180926-$.DID. OR US-	US-PGPUB; USPAT	OR	OFF	2013/01/21 21:54

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S132	83	DIMM with CS and DIMM with DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 21:55
S133	3	("20050038924" | "20080052462" | "6681301").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/01/21 22:03
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S135	140	US-20060198178-$.DID. OR US-20060203590-$.DID. OR US-20060206738-$.DID. OR US-7119428-$.DID. OR US-20060236165-$.DID. OR US-20060236201-$.DID. OR US-20060233012-$.DID. OR US-7127567-$.DID. OR US-7126399-$.DID. OR US-20060248261-$.DID. OR US-7133960-$.DID. OR US-7136978-$.DID. OR US-20060262586-$.DID. OR US-7149145-$.DID. OR US-7149824-$.DID. OR US-20060294295-$.DID. OR US-20070005998-$.DID. OR US-7173863-$.DID. OR US-20070050530-$.DID. OR US-20070058471-$.DID. OR US-20070070669-$.DID. OR US-20070088995-$.DID. OR US-7200021-$.DID. OR US-7205789-$.DID. OR US-7210059-$.DID. OR US-20070091696-$.DID. OR US-7215561-$.DID. OR US-20070106860-$.DID. OR US-7218566-	US-PGPUB; USPAT; USOCR	OR	OFF	2013/01/21 22:17

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S136	2185	DRAM with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:35
S137	31	DRAM with DIMM and DIMM with virtual$5	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:35
S138	43	DRAM with DIMM and CS with module	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:39
S139	43	virtual with DIMM and DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:49
S140	57	buffer with CS and DIMM with DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:16
S141	2	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:22
S142	37	virtual$5 near3 DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:22
S143	29	virtual$5 near3 DIMM and DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:22
S144	541	(plurality multiple) with DIMM with single	US-PGPUB; USPAT	OR	ON	2013/01/21 23:25
S145	200	(plurality multiple) near3 DIMM with single	US-PGPUB; USPAT	OR	ON	2013/01/21 23:25
S146	170	(plurality multiple) near3 DIMM with single and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/21 23:25
S147	132	logical with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/21 23:35
S148	112	logical with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/21 23:35
S149	334	(group) with DIMM and DRAM	US-PGPUB;	OR	ON	2013/01/22 00:47

			USPAT			
S150	55	emulat$3 with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/22 00:52
S151	71	virtual with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/22 09:39
S152	10	(plurality multiple) with virtual with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/22 09:40
S153	47	(plurality multiple) with (virtual logical emulat$3) with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/22 09:40
S154	1	"7133960".pn.	US-PGPUB; USPAT	OR	ON	2013/01/22 09:42
S155	17	rank with (appear$3) with DIMM	USPAT	OR	OFF	2013/01/30 13:21
S159	180	(virtual logical abstract$3) with DIMM	US-PGPUB; USPAT	OR	ON	2013/02/18 23:49
S160	22	(virtual logical abstract$3) adj DIMM	US-PGPUB; USPAT	OR	ON	2013/02/18 23:49
S161	344	(virtual logical abstract$3) adj RAM	US-PGPUB; USPAT	OR	ON	2013/02/19 00:01
S162	98	(virtual logical abstract$3) adj DRAM	US-PGPUB; USPAT	OR	ON	2013/02/19 00:01
S168	2	"201100052062".pn. "5910010".pn. "5222014".pn.	US-PGPUB; USPAT	OR	OFF	2013/04/16 23:55
S169	18	US-20030110339-$.DID. OR US-20030174569-$.DID. OR US-20040049624-$.DID. OR US-20050044302-$.DID. OR US-20060277355-$.DID. OR US-20080130364-$.DID. OR US-20080282084-$.DID. OR US-20080282341-$.DID. OR US-20090049266-$.DID. OR US-20090070520-$.DID. OR US-20090063865-$.DID. OR US-20090063896-$.DID. OR US-20090089480-$.DID. OR US-6047361-$.DID. OR WO-199725674-$.DID. OR KR-2005120344-$.DID. OR US-3201318-$.DID. OR KR-1020087019582-$.DID. OR US-1201321-$.DID. OR US-6201324-$.DID. OR US-4201331-$.DID. OR US-9201340-$.DID. OR US-182013D-$.DID.	US-PGPUB; USPAT	OR	OFF	2013/07/24 15:48
S170	105	(virtual logical abstract$3) adj DRAM	US-PGPUB; USPAT	OR	ON	2013/07/24 15:59
S171	60	emulat$3 with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/07/24 15:59

S172	4337	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/07/24 16:02
S173	3	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/07/24 16:04
S178	1054	buffer with data with CS	US-PGPUB; USPAT	OR	OFF	2017/04/26 15:45
S179	1637	buffer with DIMM	US-PGPUB; USPAT	OR	OFF	2017/04/26 15:49
S180	100	buffer and fan$4 with (rank dimm)	US-PGPUB; USPAT	OR	OFF	2017/04/26 16:14
S181	249	buffer same parallel with (rank dimm)	US-PGPUB; USPAT	OR	OFF	2017/04/26 16:26
S182	112	buffer same parallel with (ranks dimms)	US-PGPUB; USPAT	OR	OFF	2017/04/26 16:26
S183	60	daisy with chain with DIMM same buffer	US-PGPUB; USPAT	OR	OFF	2017/04/27 00:11
S184	9041	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	US-PGPUB; USPAT	OR	OFF	2017/04/30 15:23
S189	1	bust with rank$1 with select$3	US-PGPUB; USPAT	OR	OFF	2017/08/17 00:07
S190	38	burst with rank$1 with select$3	US-PGPUB; USPAT	OR	OFF	2017/08/17 00:07
S191	38	burst with rank with select$3	US-PGPUB; USPAT	OR	ON	2017/08/17 08:16
S192	141	burst same rank$1 same select$3	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:16
S193	113	buffer same parallel with (ranks dimms)	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:34
S194	5288	G06F13/1673.cpc. G011C7/1072.cpc. G011C15/00.cpc. G06F13/4282.cpc. G06F13/4243.cpc.	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:36
S195	299	DIMM same CS	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:46
S196	322	DIMM same (CS chip$1select)	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:46
S197	83	DIMM with DRAM and CS with (DIMM) and buffer with (DIMM DRAM)	US-PGPUB; USPAT	OR	OFF	2017/08/17 09:29
S198	195	DIMM with rank with select$3	US-PGPUB; USPAT	OR	OFF	2017/08/17 10:08

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	5127	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	USPAT	OR	OFF	2017/08/17 15:22
L3	0	L2 and buffer.clm. and rank.clm. and burst.clm.	USPAT	OR	OFF	2017/08/17 15:22
L4	8	DIMM with rank with selection	USPAT	OR	OFF	2017/08/17 15:23
S156	4194	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/01/30 13:35
S157	1321	emulated.clm.	USPAT	OR	OFF	2013/01/30 13:45
S158	3	S156 and S157	USPAT	OR	OFF	2013/01/30 13:45
S163	4205	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/02/19 00:04
S164	1330	emulated.clm.	USPAT	OR	OFF	2013/02/19 00:04
S165	4205	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/02/19 00:04
S166	1330	emulated.clm.	USPAT	OR	OFF	2013/02/19 00:04
S167	3	S165 and S166	USPAT	OR	OFF	2013/02/19 00:04
S174	4343	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/07/24 16:04
S175	4343	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/07/24 16:06
S176	1399	emulated.clm.	USPAT	OR	OFF	2013/07/24 16:06
S177	4	S175 and S176	USPAT	OR	OFF	2013/07/24 16:06
S185	4964	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	USPAT	OR	OFF	2017/04/30 15:24
S186	6228	data.clm. adj path.clm.	USPAT	OR	OFF	2017/04/30 15:28
S187	120	S185 and S186	USPAT	OR	OFF	2017/04/30 15:28
S188	8	S185 and S186 and rank.clm.	USPAT	OR	OFF	2017/04/30 15:28
S199	5127	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	USPAT	OR	OFF	2017/08/17 10:17

8/17/2017 3:34:05 PM
C:\Users\gbansal\Documents\EAST\Workspaces\14715486.wsp

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14715486
Filing Date	2015-05-18
First Named Inventor	Jeffrey C. Solomon
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	N3044.10002US21

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14715486
	Filing Date	2015-05-18
	First Named Inventor	Jeffrey C. Solomon
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

	1	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-0549, Patent Owner's Response, filed September 15, 2017.	
	2	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-0549, Exhibit 2001 (DECLARATION OF PROFESSOR CARL SECHEN), filed September 15, 2017.	
	3	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-0549, Exhibit 2001 (DECLARATION OF PROFESSOR CARL SECHEN), filed September 15, 2017.	
	4	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-0549, PETITIONERS' OBJECTIONS TO EVIDENCE, filed September 15, 2017.	
	5	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2003 (DECLARATION OF R. JACOB BAKER, PH.D., P.E.), filed October 25, 2017.	
	6	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2004 (Deposition of HAROLD S. STONE, PH.D.), filed October 25, 2017.	
	7	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2005 (Memory Systems: Cache, DRAM, Disk), filed October 25, 2017.	
	8	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2006 (PC2100 and PC1600 DDR SDRAM Registered DIMM, Design Specification, Revision 1.3, January 2002), filed October 25, 2017.	
	9	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2007 (DRAM CIRCUIT DESIGN: Fundamental and High-Speed Topics), filed October 25, 2017.	
	10	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, PATENT OWNER'S RESPONSE, filed October 25, 2017.	
	11	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, PETITIONERS' OBJECTIONS TO EVIDENCE, filed October 31, 2017.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	14715486
	Filing Date	2015-05-18
	First Named Inventor	Jeffrey C. Solomon
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

If you wish to add additional non-patent literature document citation information please click the Add button	Add		
EXAMINER SIGNATURE			
Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14715486
	Filing Date	2015-05-18
	First Named Inventor	Jeffrey C. Solomon
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

X That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

X The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/JAMIE J .ZHENG/	Date (YYYY-MM-DD)	2017-11-10
Name/Print	Jamie Zheng	Registration Number	51167

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	14715486
Filing Date:	18-May-2015
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Filer:	Jamie Jie Zheng/Brian Gonzalez
Attorney Docket Number:	N3044.10002US21

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	2806	1	90	90
		Total in USD ($)		**90**

Electronic Acknowledgement Receipt

EFS ID:	30915984
Application Number:	14715486
International Application Number:	
Confirmation Number:	1537
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/Brian Gonzalez
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	N3044.10002US21
Receipt Date:	10-NOV-2017
Filing Date:	18-MAY-2015
Time Stamp:	19:16:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$90
RAM confirmation Number	111317INTEFSW19175200
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	2017-11-10_IDS_N3044-10002 US21.pdf	1043493 71f1273b90e4ecf6f6946ff4a4a858d1b1af2ba2	no	5
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
2	Non Patent Literature	NPL001_IPR2017-00549_Patent OwnerResponse.pdf	2571487 e0a8405c527cce9dfd2079aa582f455fe0257ff3	no	47
Warnings:					
Information:					
3	Non Patent Literature	NPL002_IPR2017-00549_Exhibit2001.pdf	4533447 1e94933855ddfc8c2461376e6d6d32d39ace621b	no	73
Warnings:					
Information:					
4	Non Patent Literature	NPL003_IPR2017-00549_Exhibit2002.pdf	10360526 241a5991a5aadde17d12ce702f01181c16b383ca	no	139
Warnings:					
Information:					
5	Non Patent Literature	NPL004_IPR2017-00549_PetitionersObjectionstoEvidence.pdf	212822 bafec33b62c31f49a34fbb30b9081564fb8b4f6e	no	5
Warnings:					
Information:					

6	Non Patent Literature	NPL005_IPR2017-00577_Exhibit2003.pdf	7408003 1c906c4a6cd69a3ce8d9fa8ff13408103ae11b4e	no	104
Warnings:					
Information:					
7	Non Patent Literature	NPL006_IPR2017-00577_Exbhibit2004.pdf	1133229 f640bcaacea38a1b659db5bef92a2bd0bc96250e	no	243
Warnings:					
Information:					
8	Non Patent Literature	NPL007_IPR2017-00577_Exhibit2005.pdf	3551522 e33fa2aff747dd76170c980a7b64e89be97c28af	no	38
Warnings:					
Information:					
9	Non Patent Literature	NPL008_IPR2017-00577_Exhibit2006.pdf	5068458 9e9372d58c16388d23ac7852eb56c5936e67d7b4	no	82
Warnings:					
Information:					
10	Non Patent Literature	NPL009_IPR2017-00577_Exhibit2007.pdf	2422569 058ebcbfe5b6699b24538d57a036613ba34dea9c	no	43
Warnings:					
Information:					
11	Non Patent Literature	NPL010_IPR2017-00577_PatentOwnersResponse.pdf	4185261 706ed4b7eed5131862cd0bd4972250b8b72c1fd3	no	65
Warnings:					
Information:					
12	Non Patent Literature	NPL011_IPR2017-00577_PetitionersObjectionstoEvidence.pdf	262207 cf38d3e772a68f7fd466497bfab16226497e7cec	no	6
Warnings:					
Information:					

13	Fee Worksheet (SB06)	fee-info.pdf	30607 b4586e62c02a294a141557813cb6416875f6fc4d	no	2
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			Total Files Size (in bytes):	42783631	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of :	Jeffrey C. Solomon	
Application No.:	14/715,486	Art Unit 2139
Filed:	May 18, 2015	
Conf. No.:	1537	
For:	MEMORY MODULE WITH DATA BUFFERING	
Examiner:	BANSAL, GURTEJ	
Customer No.:	79141	
Attorney Docket No.:	N3044.10002US21	

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant acknowledges Examiner's statements of Reasons for Allowance of the above-referenced patent application and agrees that the claimed subject matter is patentable. However, Applicant takes no position regarding the Reasons for Allowance presented by the Examiner other than the positions Applicant may have previously taken during prosecution. Therefore, the Examiner's Reasons for Allowance should not be attributed to Applicant as an indication of the basis for Applicant's belief that the claims are patentable. Furthermore, Applicant respectfully asserts that there may also be additional reasons for patentability of the claimed subject matter not explicitly stated in this record and Applicant does not waive its rights to such arguments by not further addressing such reasons herein.

Dated this 13th day of November, 2017.

Respectfully submitted,

/Jamie J. Zheng, Reg. no. 51167/

JAMIE J. ZHENG
Registration No. 51,167
Attorney for Applicant
Telephone No. (650) 521-4828

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 08/22/2017
Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/715,486	05/18/2015	Jeffrey C. Solomon	N3044.10002US21	1537

TITLE OF INVENTION: MEMORY MODULE WITH DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	11/22/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
BANSAL, GURTEJ	2139	711-105000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 MASCHOFF BRENNAN
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Netlist, Inc.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Irvine, California

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☑ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

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5. **Change in Entity Status** (from status indicated above)
☐ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
☐ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
☑ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Jamie J. Zheng/ Date November 13, 2017
Typed or printed name Jamie J. Zheng Registration No. 51167

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Petitioners
Ex. 1057, p. 506

Electronic Patent Application Fee Transmittal

Application Number:	14715486
Filing Date:	18-May-2015
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Filer:	Jamie Jie Zheng/Brian Gonzalez
Attorney Docket Number:	N3044.10002US21

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**960**

Electronic Acknowledgement Receipt

EFS ID:	30931359
Application Number:	14715486
International Application Number:	
Confirmation Number:	1537
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/Brian Gonzalez
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	N3044.10002US21
Receipt Date:	13-NOV-2017
Filing Date:	18-MAY-2015
Time Stamp:	15:20:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$960
RAM confirmation Number	111417INTEFSW15210200
Deposit Account	505394
Authorized User	Brian Gonzalez
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.20 (Post Issuance fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Post Allowance Communication - Incoming	2017-11-13_Comments_N3044-10002US21.pdf	226832 b13458fc057287c73828f2f11070517e8512c29b	no	1
Warnings:					
Information:					
2	Issue Fee Payment (PTO-85B)	2017-11-13_Issue-Fee-Transmittal_N3044-10002US21.pdf	267492 99828de006f8b354925355542c35ed90c67ece92	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30804 8d86031202802aef2da13a9c6f07ba22dd35b342	no	2
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		Total Files Size (in bytes):	525128		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14/715,486	Solomon et al.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

CPC						
Symbol					**Type**	**Version**
G06F	/	13	/	1673	F	2013-01-01
G11C	/	7	/	1072	I	2013-01-01
G11C	/	15	/	00	I	2013-01-01
G06F	/	13	/	4282	I	2013-01-01
G06F	/	13	/	4243	I	2013-01-01

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	29	
/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	14 November 2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office — Part of Paper No.: 20171114

Petitioners
Ex. 1057, p. 511

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14/715,486	Solomon et al.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

INTERNATIONAL CLASSIFICATION					
CLAIMED					
G06F	/	00	/		

NON-CLAIMED					
	/		/		

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
`	

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 29	
/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139 (Primary Examiner)	14 November 2017 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

U.S. Patent and Trademark Office — Part of Paper No.: 20171114

Petitioners
Ex. 1057, p. 512

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14/715,486	Solomon et al.
	Examiner	Art Unit
	GURTEJ BANSAL	2139

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		10		19	27	28								
2	2	21	11		20	6	29								
9	3	22	12		21	7	30								
10	4	23	13	14	22	8	31								
11	5	28	14	15	23	18	32								
12	6	29	15	5	24	19	33								
13	7	24	16	16	25	20	34								
3	8	25	17	17	26										
4	9		18	26	27										

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	29	
/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	14 November 2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office — Part of Paper No.: 20171114

Petitioners
Ex. 1057, p. 513

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/715,486	05/18/2015	Jeffrey C. Solomon	N3044.10002US21	1537

79141 7590 11/22/2017

Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

EXAMINER	
BANSAL, GURTEJ	

ART UNIT	PAPER NUMBER
2139	

NOTIFICATION DATE	DELIVERY MODE
11/22/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

d@mabr.com
bisraelsen@mabr.com

Corrected Notice of Allowability	Application No. 14/715,486	Applicant(s) Solomon et al.	
	Examiner GURTEJ BANSAL	Art Unit 2139	AIA Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to IDS dated 11/10/2017 .
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____ .

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-9,11-17 and 22-34 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information , please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 11/10/2017
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____ .

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14715486
Filing Date	2015-05-18
First Named Inventor	Jeffrey C. Solomon
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	N3044.10002US21

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14715486
	Filing Date	2015-05-18
	First Named Inventor	Jeffrey C. Solomon
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

	1	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-0549, Patent Owner's Response, filed September 15, 2017.	
	2	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-0549, Exhibit 2001 (DECLARATION OF PROFESSOR CARL SECHEN), filed September 15, 2017.	
	3	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-0549, Exhibit 2001 (DECLARATION OF PROFESSOR CARL SECHEN), filed September 15, 2017.	
	4	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-0549, PETITIONERS' OBJECTIONS TO EVIDENCE, filed September 15, 2017.	
	5	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2003 (DECLARATION OF R. JACOB BAKER, PH.D., P.E.), filed October 25, 2017.	
	6	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2004 (Deposition of HAROLD S. STONE, PH.D.), filed October 25, 2017.	
	7	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2005 (Memory Systems: Cache, DRAM, Disk), filed October 25, 2017.	
	8	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2006 (PC2100 and PC1600 DDR SDRAM Registered DIMM, Design Specification, Revision 1.3, January 2002), filed October 25, 2017.	
	9	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2007 (DRAM CIRCUIT DESIGN: Fundamental and High-Speed Topics), filed October 25, 2017.	
	10	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, PATENT OWNER'S RESPONSE, filed October 25, 2017.	
	11	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, PETITIONERS' OBJECTIONS TO EVIDENCE, filed October 31, 2017.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14715486
	Filing Date	2015-05-18
	First Named Inventor	Jeffrey C. Solomon
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	N3044.10002US21

If you wish to add additional non-patent literature document citation information please click the Add button [Add]

EXAMINER SIGNATURE

Examiner Signature	/GURTEJ BANSAL/	Date Considered	11/14/2017

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14715486
Filing Date	2015-05-18
First Named Inventor	Jeffrey C. Solomon
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	N3044.10002US21

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/JAMIE J .ZHENG/	Date (YYYY-MM-DD)	2017-11-10
Name/Print	Jamie Zheng	Registration Number	51167

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Approved for use through 7/31/2012. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	3

Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

Change(s) applied to document, /P.A.P./ 5/30/2017

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	5388240	02-01-1995	~~IBM Corporation~~ Olderdissen, et al.	
	2.	5463590	10-31-1995	Watanabe	
	3.	5953280	09-14-1999	Matsui	
	4.	6188641	02-13-2001	Uchida	
	5.	6205516	03-20-2001	Usami	
	6.	6480439	11-12-2002	Tokutome et al.	
	7.	7464225	12-09-2008	Tsern	
	8.	7865674	01-04-2011	Gower et al.	
	9.	8089795	01-03-2012	Rajan	
	10.	8130560	03-06-2012	Rajan	
	11.	8189328	05-29-2012	Kanapathippillai	
	12.	8233303	07-31-2012	Best	
	13.	8250295	08-21-2012	Amidi et al.	
	14.	8417870	04-09-2013	Lee et al.	
	15.	8516185	08-20-2013	Lee et al.	
	16.	8516188	08-20-2013	Solomon et al.	
	17.	8756364	06-17-2014	Bhakta et al.	
	18.	20070058409	03-15-2007	Ruckerbauer	
	19.	20080104352	05-01-2008	Talbot	
	20.	20080104352	05-01-2008	Talbot	
	21.	RE36229	06-15-1999	Cady	

US PATENT APPLICATIONS

Examiner Initials *	Cite No. [1]	Application Number	Filing Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	22.	13/411,344	3/2/2012	Lee	Entire Prosecution History
	23.	13/970,606	8/20/2013	Netlist, Inc.	Entire Prosecution History
	24.	13/971,231	8/20/2013	Netlist, Inc.	Entire Prosecution History
	25.	14/229,844	3/29/2014	Netlist, Inc.	Entire Prosecution History
	26.	14/324,990	7/7/2014	Netlist, Inc.	Entire Prosecution History
	27.	14/337,168	7/21/2014	Netlist, Inc.	Entire Prosecution History

NON PATENT LITERATURE DOCUMENTS

EXAMINER /GURTEJ BANSAL/ DATE CONSIDERED 04/30/2017

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

PTO/SB/08a/b(07-09)
Approved for use through 7/31/2012. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 5 of 17

Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

Change(s) applied to document, /P.A.P/ 5/30/2017

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	137.	7047361	05-16-2006	~~Phison Electronics~~ Corp	Chong, et al.
	138.	7054179	05-30-2006	Cogdill et al.	
	139.	7065626	06-20-2006	Schumacher et al.	
	140.	7072231	07-04-2006	Pax	
	141.	7073041	07-04-2006	Dwyer et al.	
	142.	7078793	07-18-2006	Ruckerbauer et al.	
	143.	7120727	10-10-2006	Lee et al.	
	144.	7124260	10-17-2006	LaBerge et al.	
	145.	7127584	10-24-2006	Thompson et al.	
	146.	7130952	10-31-2006	Nanki et al.	
	147.	7133960	11-07-2006	Thompson et al.	
	148.	7133972	11-07-2006	Jeddeloh	
	149.	7142461	11-28-2006	Janzen	
	150.	7149841	12-12-2006	LaBerge	
	151.	7167967	01-23-2007	Bungo et al.	
	152.	7181591	02-20-2007	Tsai	
	153.	7200021	04-03-2007	Raghuram	
	154.	7227910	06-05-2007	Lipka	
	155.	7266639	09-04-2007	Raghuram	
	156.	7272709	09-18-2007	Zitlaw et al.	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 4 of 17

Complete if Known	
Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

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Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Sheet 1 of 17

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Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

Change(s) applied to document, /P.A.P/ 5/30/2017

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Sheet 1 of 2

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Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

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First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

Change(s) applied to document, /S.D./ 6/9/2017

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Sheet 3 of 17

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Application Number	14/715,486
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First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

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Sheet 2 of 17

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Application Number	14/715,486
Filing Date	May 18, 2015
First Named Inventor	Jayesh R. Bhakta
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C8

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Attorney Docket Number	NETL.018P2C8

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Change(s) applied to document, /S.D./ 6/9/2017

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

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14/715,486	01/02/2018	9858215	N3044.10002US21	1537

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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 192 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

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