JEDEC STANDARD

DDR2 SDRAM SPECIFICATION

JESD79-2

SEPTEMBER 2003

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

Petitioners
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JEDEC Solid State Technology Association 2001
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1 Package Pinout & Addressing

1.1 DDR2 SDRAM Package Ballout

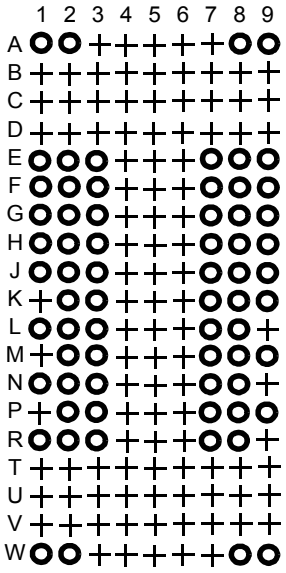
(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
										D
A	VDD	NC	VSS				VSSQ	$\overline{DQS}$	VDDQ	E
B	NC	VSSQ	DM				DQS	VSSQ	NC	F
C	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
D	NC	VSSQ	DQ3				DQ2	VSSQ	NC	H
E	VDDL	VREF	VSS				VSSDL	CK	VDD	J
F		CKE	$\overline{WE}$				$\overline{RAS}$	$\overline{CK}$	ODT	K
G	NC, BA2	BA0	BA1				$\overline{CAS}$	$\overline{CS}$		L
H		A10/AP	A1				A2	A0	VDD	M
J	VSS	A3	A5				A6	A4		N
K		A7	A9				A11	A8	VSS	P
L	VDD	A12	NC, A14				NC, A15	NC, A13		R
										T
										U
										V
	NC	NC						NC	NC	W

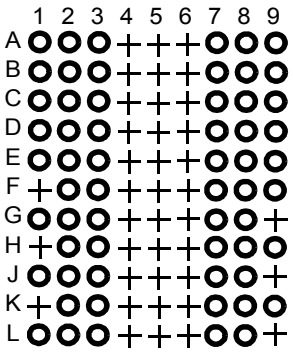
Variation DJ-z without support balls

Variation DM-z with support balls

Variation DM-z (x4/x8) with support balls



Variation DJ-z (x4 x8)



O Populated ball
+ Ball not populated

Figure 1 — DDR2 SDRAM x4 Ballout Using MO-207

1 Package Pinout & Addressing (cont'd)

1.1 DDR2 SDRAM Package Ballout (cont'd)

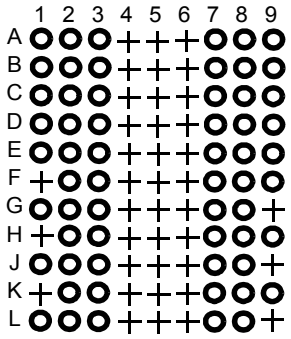
(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
										D
A	VDD	NU/$\overline{\text{RDQS}}$	VSS				VSSQ	$\overline{\text{DQS}}$	VDDQ	E
B	DQ6	VSSQ	DM/RDQS				DQS	VSSQ	DQ7	F
C	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
D	DQ4	VSSQ	DQ3				DQ2	VSSQ	DQ5	H
E	VDDL	VREF	VSS				VSSDL	CK	VDD	J
F		CKE	$\overline{\text{WE}}$				$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT	K
G	NC, BA2	BA0	BA1				$\overline{\text{CAS}}$	$\overline{\text{CS}}$		L
H		A10/AP	A1				A2	A0	VDD	M
J	VSS	A3	A5				A6	A4		N
K		A7	A9				A11	A8	VSS	P
L	VDD	A12	NC, A14				NC, A15	NC, A13		R
										T
										U
										V
	NC	NC						NC	NC	W

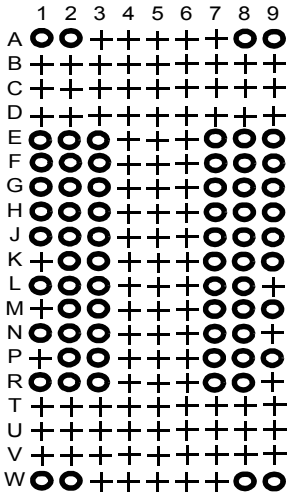
Variation DJ-z without support balls

Variation DM-z with support balls

Variation DJ-z (x4 x8)



Variation DM-z (x4/x8) with support balls



O Populated ball
+ Ball not populated

Figure 2 — DDR2 SDRAM x8 Ballout Using MO-207

1 Package Pinout & Addressing (cont'd)

1.1 DDR2 SDRAM Package Ballout (cont'd)

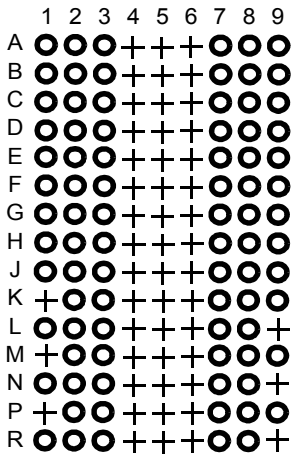
(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
A	VDD	NC	VSS				VSSQ	$\overline{\text{UDQS}}$	VDDQ	D
B	DQ14	VSSQ	UDM				UDQS	VSSQ	DQ15	E
C	VDDQ	DQ9	VDDQ				VDDQ	DQ8	VDDQ	F
D	DQ12	VSSQ	DQ11				DQ10	VSSQ	DQ13	G
E	VDD	NC	VSS				VSSQ	$\overline{\text{LDQS}}$	VDDQ	H
F	DQ6	VSSQ	LDM				LDQS	VSSQ	DQ7	J
G	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	K
H	DQ4	VSSQ	DQ3				DQ2	VSSQ	DQ5	L
J	VDDL	VREF	VSS				VSSDL	CK	VDD	M
K		CKE	$\overline{\text{WE}}$				$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT	N
L	NC, BA2	BA0	BA1				$\overline{\text{CAS}}$	$\overline{\text{CS}}$		P
M		A10/AP	A1				A2	A0	VDD	R
N	VSS	A3	A5				A6	A4		T
P		A7	A9				A11	A8	VSS	U
R	VDD	A12	NC, A14				NC, A15	NC, A13		V
										W
										X
	NC	NC						NC	NC	AA

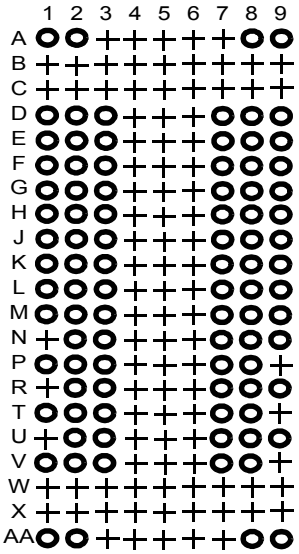
Variation DK-z without support balls

Variation DL-z with support balls

Variation DK-z (x16)



Variation DL-z (x16) with support balls



O Populated ball
+ Ball not populated

Figure 3 — DDR2 SDRAM x16 Ballout Using MO-207

1 Package Pinout & Addressing (cont'd)

1.1 DDR2 SDRAM Package Ballout (cont'd)

(Top view: see balls through package)

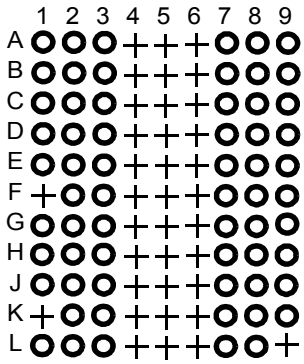
	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
										D
A	VDD	NC	VSS				VSSQ	$\overline{DQS}$	VDDQ	E
B	NC	VSSQ	DM				DQS	VSSQ	NC	F
C	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
D	NC	VSSQ	DQ3				DQ2	VSSQ	NC	H
E	VDDL	VREF	VSS				VSSDL	CK	VDD	J
F		CKE0	$\overline{WE}$				$\overline{RAS}$	$\overline{CK}$	ODT0	K
G	NC, BA2	BA0	BA1				$\overline{CAS}$	$\overline{CS0}$	$\overline{CS1}$	L
H	CKE1	A10/AP	A1				A2	A0	VDD	M
J	VSS	A3	A5				A6	A4	ODT1	N
K		A7	A9				A11	A8	VSS	P
L	VDD	A12	NC, A14				NC, A15	NC, A13		R
										T
										U
										V
	NC	NC						NC	NC	W

Variation tbd. without support balls

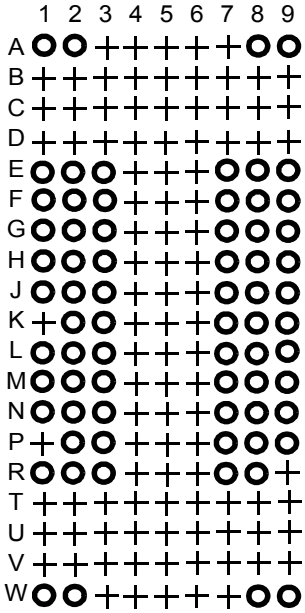
Variation tbd. with support balls

NOTE This stacked ballout does not represent the nonstacked ballout; it is intended only for use in a stacked package.

Variation tbd. (x4 x8)



Variation tbd.(x4/x8) with support balls



O Populated ball
+ Ball not populated

Figure 4 — Stacked/Dual-Die DDR2 SDRAM x4 Ballout Using MO-TBD.

1 Package Pinout & Addressing (cont'd)

1.1 DDR2 SDRAM Package Ballout (cont'd)

(Top view: see balls through package)

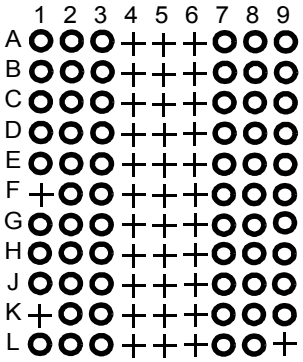
	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
										D
A	VDD	NU/$\overline{\text{RDQS}}$	VSS				VSSQ	$\overline{\text{DQS}}$	VDDQ	E
B	DQ6	VSSQ	DM/RDQS				DQS	VSSQ	DQ7	F
C	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
D	DQ4	VSSQ	DQ3				DQ2	VSSQ	DQ5	H
E	VDDL	VREF	VSS				VSSDL	CK	VDD	J
F		CKE0	$\overline{\text{WE}}$				$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT0	K
G	NC, BA2	BA0	BA1				$\overline{\text{CAS}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$	L
H	CKE1	A10/AP	A1				A2	A0	VDD	M
J	VSS	A3	A5				A6	A4	ODT1	N
K		A7	A9				A11	A8	VSS	P
L	VDD	A12	NC, A14				NC, A15	NC, A13		R
										T
										U
										V
	NC	NC						NC	NC	W

Variation tbd. without support balls

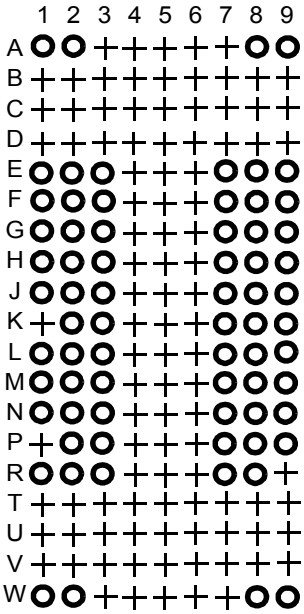
Variation tbd. with support balls

NOTE This stacked ballout is intended for use only in a stacked package, it does not represent the nonstacked package.

Variation tbd. (x4 x8)



Variation tbd.(x4/x8) with support balls



O Populated ball
+ Ball not populated

Figure 5 — Stacked/Dual-Die DDR2 SDRAM x8 Ballout Using MO-TBD

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1 Package Pinout & Addressing (cont'd)

1.2 Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, and DM signal for x4x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (UDM), (LDM)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/$\overline{RDQS}$ is enabled by EMRS command.
BA0 - BA2	Input	**Bank Address Inputs:** BA0 and BA1 for 256 and 512Mb, BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A15	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands.
DQ	Input/Output	**Data Input/ Output:** Bi-directional data bus.
DQS, ($\overline{DQS}$) (UDQS), ($\overline{UDQS}$) (LDQS), ($\overline{LDQS}$) (RDQS), ($\overline{RDQS}$)	Input/Output	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15. For the x8, an RDQS option using DM pin can be enabled via the EMRS(1) to simplify read timing. The data strobes DQS, LDQS, UDQS, and RDQS may be used in single ended mode or paired with optional complementary signals DQS, LDQS, UDQS, and RDQS to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables all complementary data strobe signals.
NC		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 1.8V +/- 0.1V
V_{SSQ}	Supply	**DQ Ground**
V_{DDL}	Supply	**DLL Power Supply:** 1.8V +/- 0.1V
V_{SSDL}	Supply	**DLL Ground**
V_{DD}	Supply	**Power Supply:** 1.8V +/- 0.1V
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**Reference voltage**

In this data sheet, "differential DQS signals" refers to any of the following with A10 = 0 of EMRS(1)

x4 DQS/$\overline{DQS}$
x8 DQS/$\overline{DQS}$ if EMRS(1)[A11] = 0
x8 DQS/$\overline{DQS}$, RDQS/$\overline{RDQS}$, if EMRS(1)[A11] = 1
x16 LDQS/$\overline{LDQS}$ and UDQS/$\overline{UDQS}$

"single-ended DQS signals" refers to any of the following with A10 = 1 of EMRS(1)

x4 DQS
x8 DQS if EMRS(1)[A11] = 0
x8 DQS, RDQS, if EMRS(1)[A11] = 1
x16 LDQS and UDQS

1 Package Pinout & Addressing (cont'd)

1.3 DDR2 SDRAM Addressing

Table 1 — 256Mb Addressing

Configuration	64Mb x4	32Mb x 8	16Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A12	A0 ~ A12	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A8
Page size*1	1 KB	1 KB	1 KB

Table 2 — 512Mb Addressing

Configuration	128Mb x4	64Mb x 8	32Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 3 — 1Gb Addressing

Configuration	256Mb x4	128Mb x 8	64Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 4 — 2Gb Addressing

Configuration	512Mb x4	256Mb x 8	128Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A14	A0 ~ A14	A0 ~ A13
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

1 Package Pinout & Addressing (cont'd)

1.3 DDR2 SDRAM Addressing (cont'd)

Table 5 — 4 Gb Addressing

Configuration	1 Gb x4	512Mb x 8	256Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	tbd	tbd	tbd
Column Address	tbd	tbd	tbd
Page size *1	tbd	tbd	tbd

NOTE Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per bank, calculated as follows:

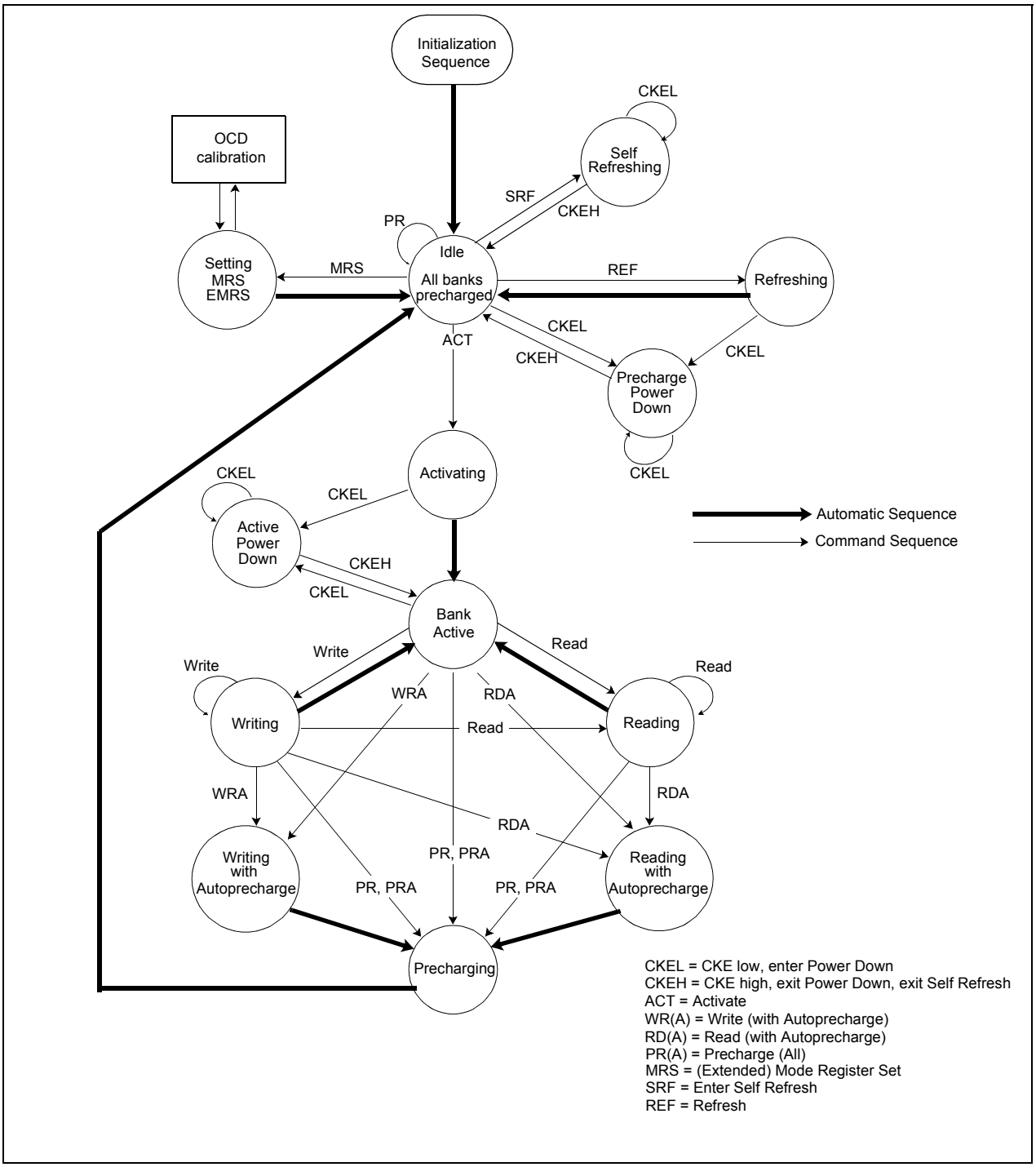
$$\text{page size} = 2^{\text{COLBITS}} * \text{ORG} \div 8$$

where

COLBITS = the number of column address bits
ORG = the number of I/O (DQ) bits

2 Functional Description

2.1 Simplified State Diagram



NOTE Use caution with this diagram. It is indented to provide a floorplan of the possible state transitions and the commands to control them, not all details. In particular situations involving more than one bank, enabling/disabling on-die termination, Power Down entry/exit - among other things - are not captured in full detail.

Figure 6 — DDR2 SDRAM Simplified State Diagram

2 Functional Description (cont'd)

2.2 Basic Functionality

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the active command are used to select the bank and row to be accessed (BA0-BA2 select the bank; A0-A15 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the auto precharge command is to be issued.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

2.2.1 Power up and Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

2.2.1.1 Power-up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain CKE below 0.2*VDDQ and ODT[*1] at a low state (all other inputs may be undefined.)

   - VDD, VDDL and VDDQ are driven from a single power converter output, AND
   - VTT is limited to 0.95 V max, AND
   - Vref tracks VDDQ/2.

   or

   - Apply VDD before or at the same time as VDDL.
   - Apply VDDL before or at the same time as VDDQ.
   - Apply VDDQ before or at the same time as VTT & Vref.

   at least one of these two sets of conditions must be met.

2. Start clock and maintain stable condition.
3. For the minimum of 200 us after stable power and clock (CK, $\overline{CK}$), then apply NOP or deselect & take CKE high.
4. Wait minimum of 400ns then issue precharge all command. NOP or deselect applied during 400ns period.
5. Issue EMRS(2) command. (To issue EMRS(2) command, provide "Low" to BA0 and BA2, "High" to BA1.)
6. Issue EMRS(3) command. (To issue EMRS(3) command, provide "Low" to BA2, "High" to BA0 and BA1.)
7. Issue EMRS to enable DLL. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1-2 and A13~A15.)
8. Issue a Mode Register Set command for "DLL reset".
   (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2, and A13~15.)
9. Issue precharge all command.

Petitioners
Ex. 1064, p. 10

2.2.1 Power up and Initialization (cont'd)

2.2.1.1 Power-up and Initialization Sequence (cont'd)

10. Issue 2 or more auto-refresh commands.
11. Issue a mode register set command with low to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL.)
12. At least 200 clocks after Step 8, execute OCD Calibration (Off Chip Driver impedance adjustment). If OCD calibration is not used, EMRS OCD Default command (A9=A8= A7=1) followed by EMRS OCD Calibration Mode Exit command (A9=A8=A7=0) must be issued with other operating parameters of EMRS.
13. The DDR2 SDRAM is now ready for normal operation.

*1) To guarantee ODT off, VREF must be valid and a low level must be applied to the ODT pin.

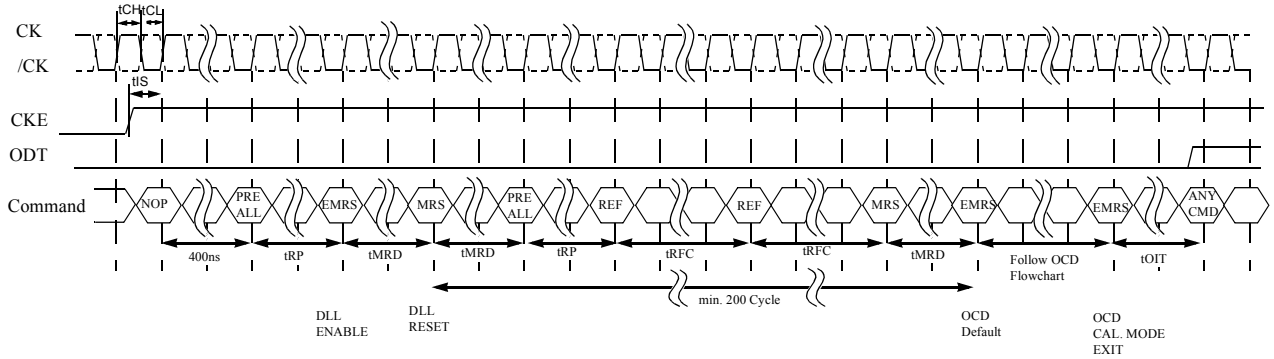


Figure 7 — Initialization Sequence after Power Up

2.2.2 Programming the Mode and Extended Mode Registers

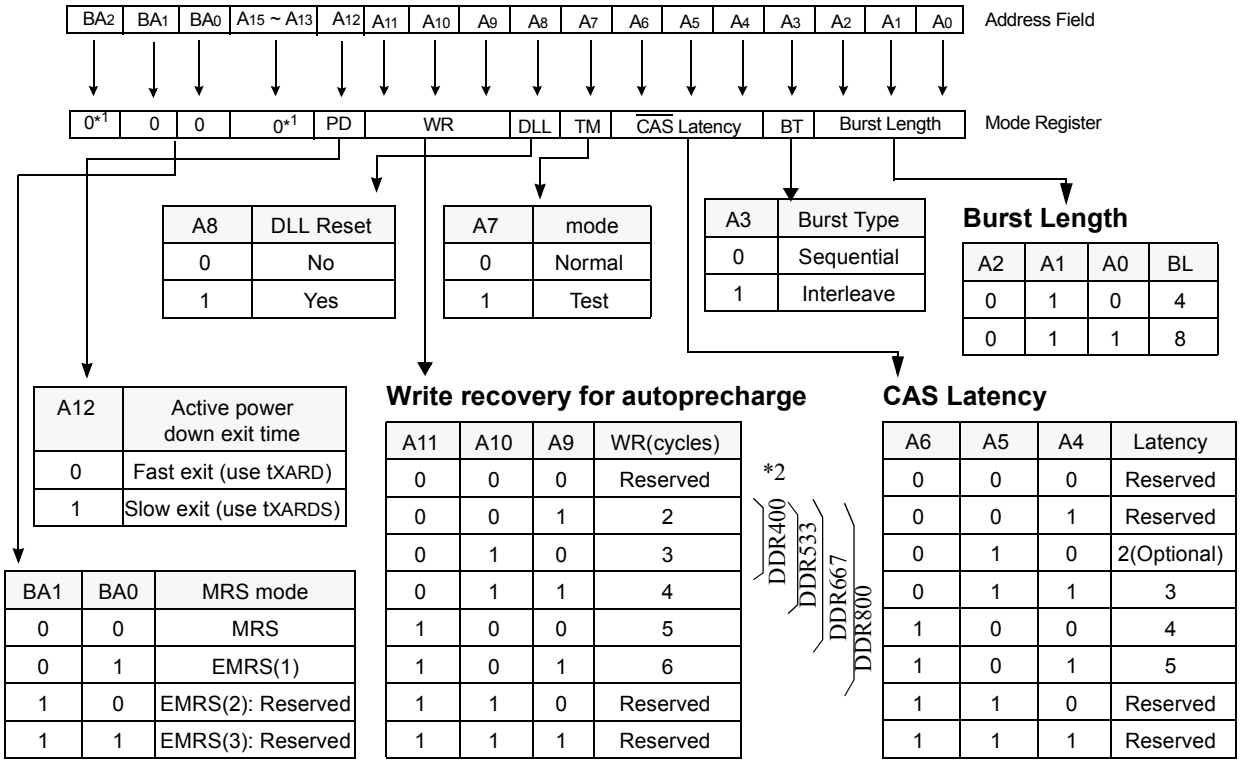
For application flexibility, burst length, burst type, $\overline{\text{CAS}}$ latency, DLL reset function, write recovery time(tWR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, driver impedance, additive CAS latency, ODT (On Die Termination), single-ended strobe, and OCD (off chip driver impedance adjustment) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register (MR) or Extended Mode Registers (EMR(#)) can be altered by re-executing the MRS and EMRS Commands. If the user chooses to modify only a subset of the MRS or EMRS variables, all variables must be redefined when the MRS or EMRS commands are issued.

MRS, EMRS and Reset DLL do not affect array contents, which means reinitialization including those can be executed any time after power-up without affecting array contents.

2.2.2 Programming the Mode and Extended Mode Registers (cont'd)

2.2.2.1 DDR2 SDRAM Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls $\overline{\text{CAS}}$ latency, burst length, burst sequence, test mode, DLL reset, tWR and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, BA0 and BA1, while controlling the state of address pins A0 ~ A15. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 ~ A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, $\overline{\text{CAS}}$ latency is defined by A4 ~ A6. The DDR2 doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Write recovery time tWR is defined by A9 ~ A11. Refer to Figure 8 for specific codes.



A8	DLL Reset
0	No
1	Yes

A7	mode
0	Normal
1	Test

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	BL
0	1	0	4
0	1	1	8

A12	Active power down exit time
0	Fast exit (use tXARD)
1	Slow exit (use tXARDS)

BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2): Reserved
1	1	EMRS(3): Reserved

A11	A10	A9	WR(cycles)
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	Reserved
1	1	1	Reserved

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2(Optional)
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	Reserved
1	1	1	Reserved

1. BA2 and A13~A15 are reserved for future use and must be programmed to 0 when setting the mode register.

2. WR(write recovery for autoprecharge) min is determined by tCK max and WR max is determined by tCK min. WR in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer (WR[cycles] = tWR(ns)/tCK(ns)). The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

Figure 8 — DDR2 SDRAM Mode Register Set (MRS)

2.2.2 Programming the Mode and Extended Mode Registers (cont'd)

2.2.2.2 DDR2 SDRAM Extended Mode Register Set

EMRS(1)

The extended mode register(1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, ODT, $\overline{DQS}$ disable, OCD program, RDQS enable. The default value of the extended mode register(1) is not defined, therefore the extended mode register(1) must be written after power-up for proper operation. The extended mode register(1) is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA0 and low on BA1, while controlling the states of address pins A0 ~ A15. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register(1). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register(1). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a half strength output driver. A3~A5 determines the additive latency, A7~A9 are used for OCD control, A10 is used for $\overline{DQS}$ disable and A11 is used for RDQS enable. A2 and A6 are used for ODT setting.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAC or tDQSCK parameters.

2.2.2.2 DDR2 SDRAM Extended Mode Register Set (cont'd)

BA2	BA1	BA0	A15 ~ A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0*[1]	0	1	0*[1]	Qoff	RDQS	$\overline{\text{DQS}}$	OCD program			Rtt	Additive latency			Rtt	D.I.C	DLL	Extended Mode Register

BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2): Reserved
1	1	EMRS(3): Reserved

A6	A2	Rtt (NOMINAL)
0	0	ODT Disabled
0	1	75 ohm
1	0	150 ohm
1	1	Reserved

A0	DLL Enable
0	Enable
1	Disable

A9	A8	A7	OCD Calibration Program
0	0	0	OCD Calibration mode exit; maintain setting
0	0	1	Drive(1)
0	1	0	Drive(0)
1	0	0	Adjust mode[a]
1	1	1	OCD Calibration default [b]

a: When Adjust mode is issued, AL from previously set value must be applied.
b: After setting to default, OCD mode needs to be exited by setting A9-A7 to 000. Refer to the following 2.2.2.3 section for detailed information

A5	A4	A3	Additive Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A12	Qoff (Optional)[a]
0	Output buffer enabled
1	Output buffer disabled

a. Outputs disabled - DQs, DQSs, $\overline{\text{DQS}}$s, RDQS, $\overline{\text{RDQS}}$. This feature is used in conjunction with dimm IDD meaurements when IDDQ is not desired to be included.

A1	Output Driver Impedance Control	Driver Size
0	Normal	100%
1	Weak	60%

A10	$\overline{\text{DQS}}$
0	Enable
1	Disable

A11	RDQS Enable
0	Disable
1	Enable

* If RDQS is enabled, the DM function is disabled. RDQS is active for reads and don't care for writes.

A11 (RDQS Enable)	A10 ($\overline{\text{DQS}}$ Enable)	Strobe Function Matrix			
		RDQS/DM	RDQS	DQS	DQS
0 (Disable)	0 (Enable)	DM	Hi-z	DQS	DQS
0 (Disable)	1 (Disable)	DM	Hi-z	DQS	Hi-z
1 (Enable)	0 (Enable)	RDQS	RDQS	DQS	DQS
1 (Enable)	1 (Disable)	RDQS	Hi-z	DQS	Hi-z

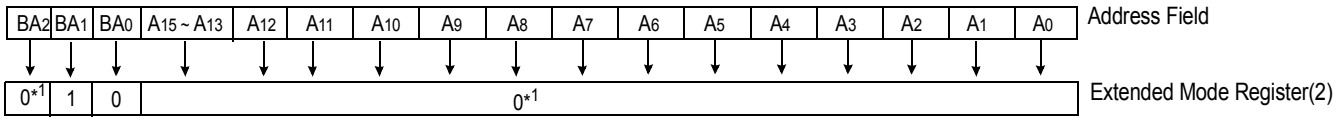
* BA2 and A13~A15 are reserved for future use and must be programmed to 0 when setting the mode register.

Figure 9 — EMRS(1) Programming

2.2.2.2 DDR2 SDRAM Extended Mode Register Set (cont'd)

EMRS(2)

1

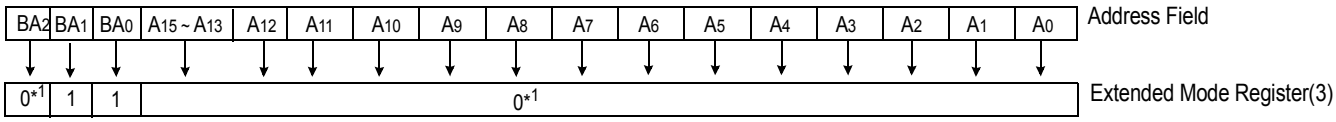


EMRS(2) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

Figure 10 — EMRS(2) Programming: Reserved

EMRS(3)

1



EMRS(3) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

Figure 11 — EMRS(3) Programming: Reserved

2.2.2.3 Off-Chip Driver (OCD) Impedance Adjustment

DDR2 SDRAM supports driver calibration feature and the flow chart below is an example of sequence. Every calibration mode command should be followed by "OCD calibration mode exit" before any other command being issued. MRS should be set before entering OCD impedance adjustment and ODT (On DieTermination) should be carefully controlled depending on system environment

Extended Mode Register Set for OCD impedance adjustment

OCD impedance adjustment can be done using the following EMRS mode. In drive mode all outputs are driven out by DDR2 SDRAM and drive of RDQS is dependent on EMRS bit enabling RDQS operation. In Drive(1) mode, all DQ, DQS (and RDQS) signals are driven high and all $\overline{DQS}$ signals are driven low. In drive(0) mode, all DQ, DQS (and RDQS) signals are driven low and all $\overline{DQS}$ signals are driven high. In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics have a nominal impedance value of 18 ohms during nominal temperature and voltage conditions. Output driver characteristics for OCD calibration default are specified in Table 6. OCD applies only to normal full strength output drive setting defined by EMRS(1) and if half strength is set, OCD default output driver characteristics are not applicable. When OCD calibration adjust mode is used, OCD default output driver characteristics are not applicable. After OCD calibration is completed or driver strength is set to default, subsequent EMRS commands not intended to adjust OCD characteristics must specify A9-A7 as '000' in order to maintain the default or calibrated value.

Table 6 — OCD Drive Mode Program

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive(1) DQ, DQS, (RDQS) high and $\overline{DQS}$ low
0	1	0	Drive(0) DQ, DQS, (RDQS) low and $\overline{DQS}$ high
1	0	0	Adjust mode
1	1	1	OCD calibration default

2.2.2.3 Off-Chip Driver (OCD) Impedance Adjustment (cont'd)

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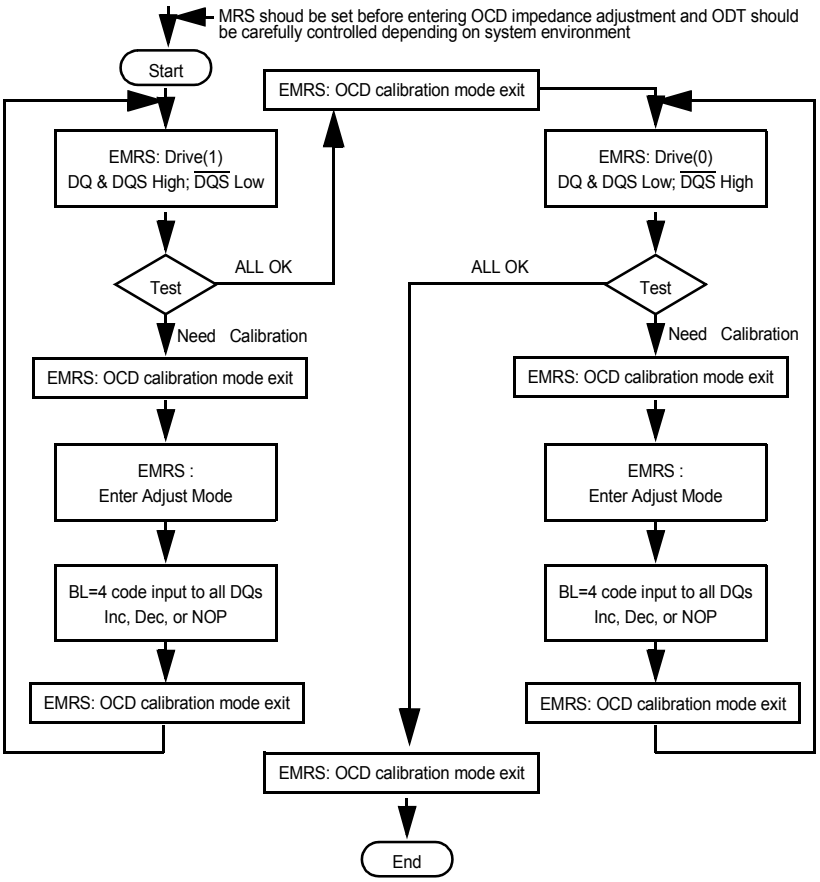


Figure 12 — OCD Impedance Adjustment

OCD Impedance Adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS command along with a 4bit burst code to DDR2 SDRAM as in Table 7. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive this burst code to all DQs at the same time. DT0 in table X means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the 16 step range. When Adjust mode command is issued, AL from previously set value must be applied.

2.2.2.3 Off-Chip Driver (OCD) Impedance Adjustment (cont'd)

Table 7 — OCD Adjust Mode Program

4bit burst code inputs to all DQs				Operation	
DT0	DT1	DT2	DT3	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP (No operation)	NOP (No operation)
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other Combinations				Reserved	

For proper operation of adjust mode, WL = RL - 1 = AL + CL - 1 clocks and tDS/tDH should be met as shown in Figure 13. For input data pattern for adjustment, DT0 - DT3 is a fixed order and "not affected by MRS addressing mode (i.e. sequential or interleave).

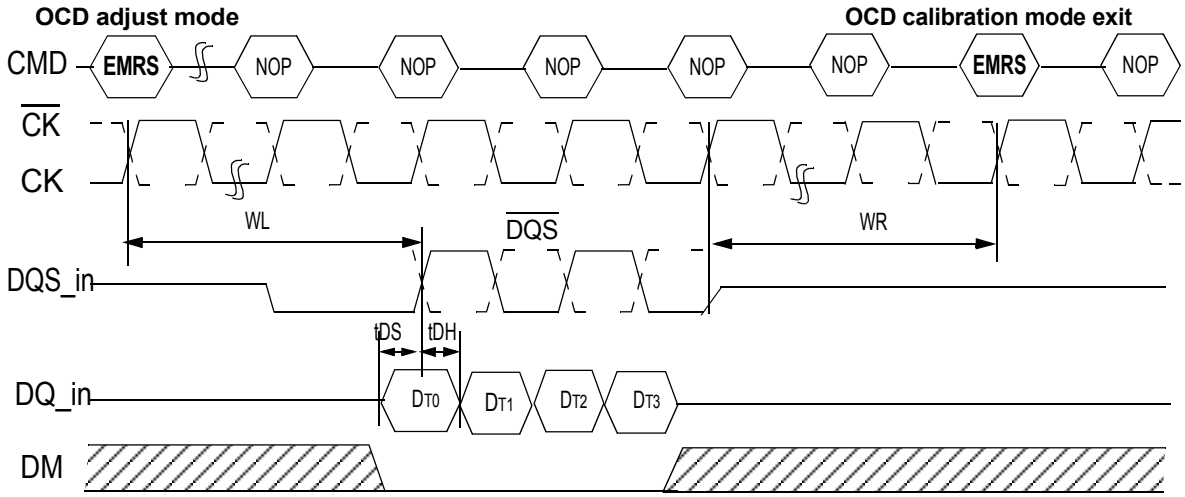


Figure 13 — OCD Adjust Mode

Drive Mode

Drive mode, both Drive(1) and Drive(0), is used for controllers to measure DDR2 SDRAM Driver impedance. In this mode, all outputs are driven out tOIT after "enter drive mode" command and all output drivers are turned-off tOIT after "OCD calibration mode exit" command as shown in Figure 14.

2.2.2.3 Off-Chip Driver (OCD) Impedance Adjustment (cont'd)

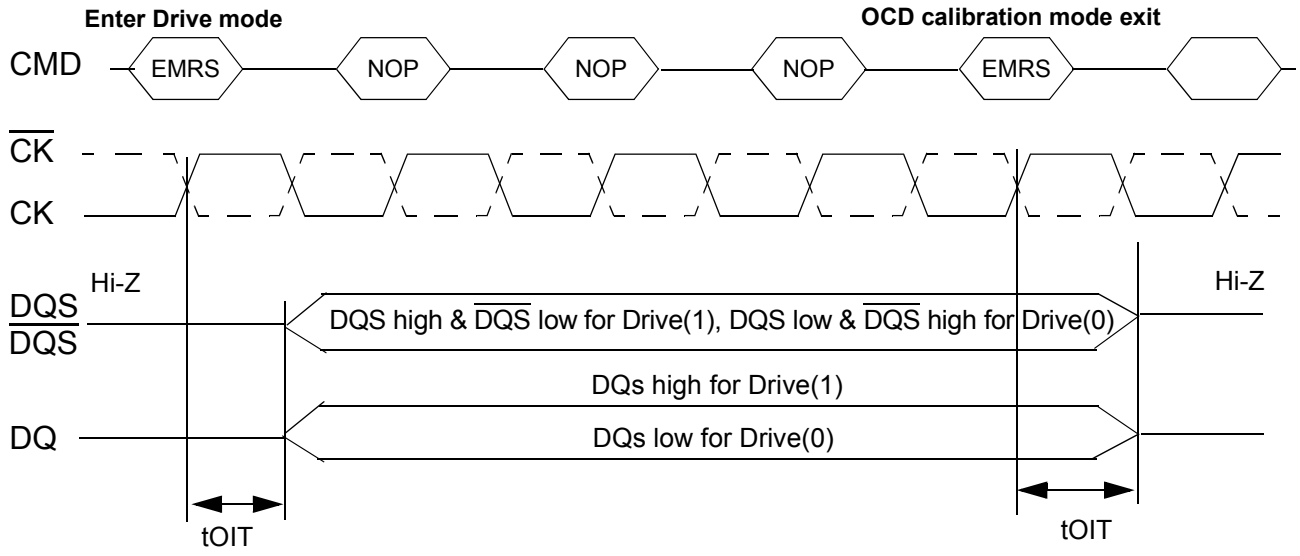


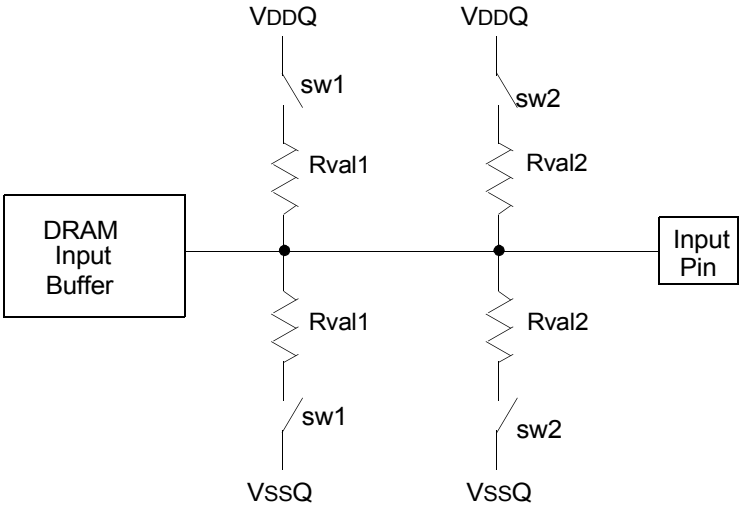
Figure 14 — OCD Drive Mode

2.2.2.4 ODT (On Die Termination)

On Die Termination (ODT) is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQS/DQS, RDQS/RDQS, and DM signal for x4x8 configurations via the ODT control pin. For x16 configuration ODT is applied to each DQ, UDQS/UDQS, LDQS/LDQS, UDM, and LDM signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function is supported for ACTIVE and STANDBY modes. ODT is turned off and not supported in SELF REFRESH mode.

2.2.2.4 ODT (On Die Termination) (cont'd)



Switch sw1 or sw2 is enabled by ODT pin.
Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.
Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

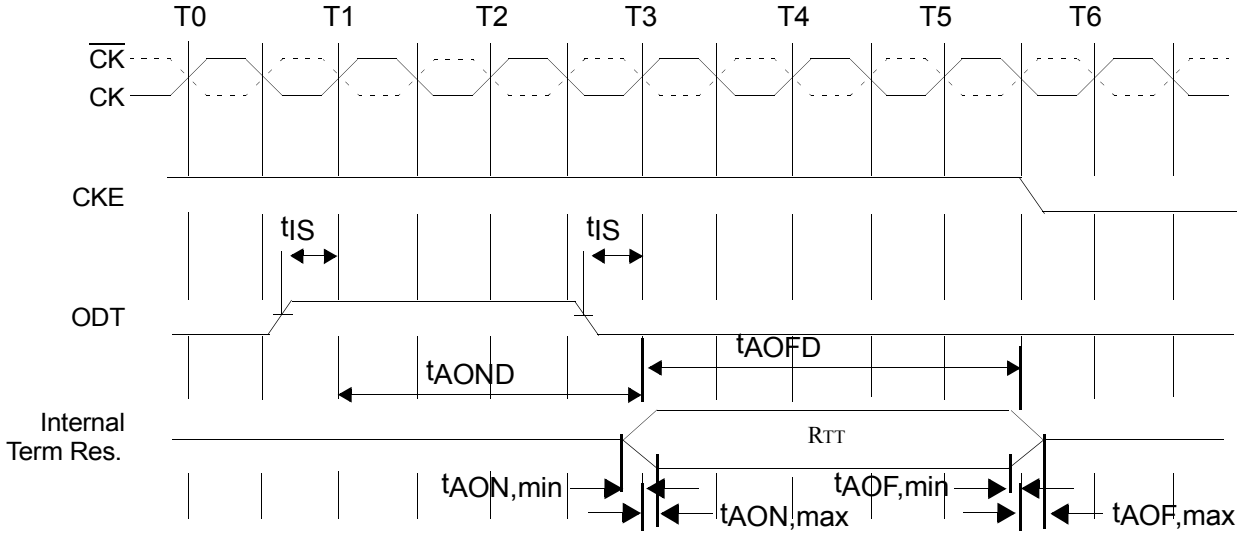


Figure 16 — ODT Timing for Active/Standby Mode

2.2.2.4 ODT (On Die Termination) (cont'd)

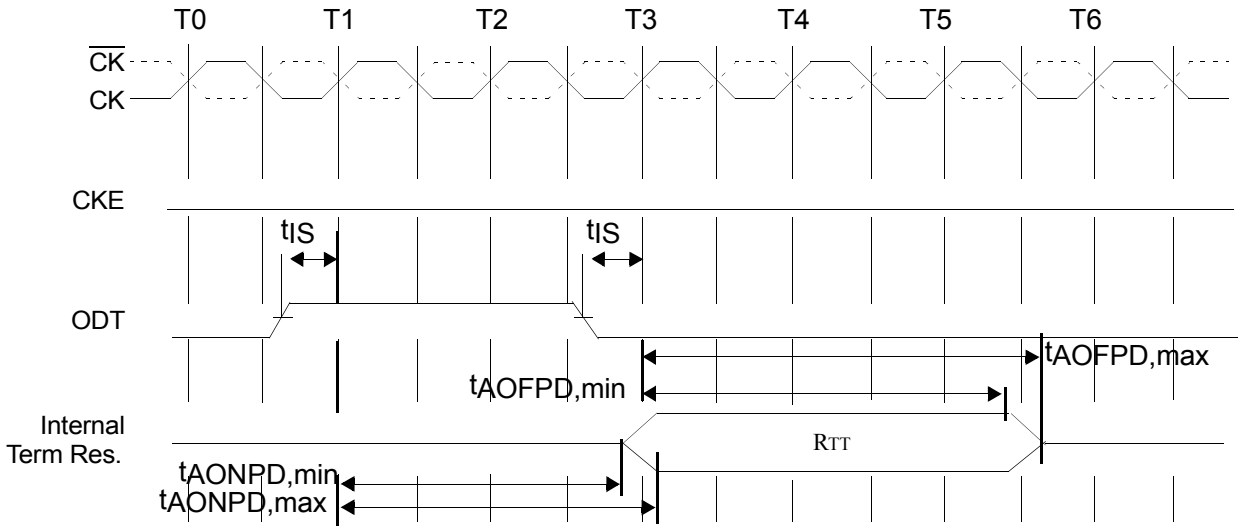


Figure 17 — ODT Timing for Powerdown Mode

2.2.2.4 ODT (On Die Termination) (cont'd)

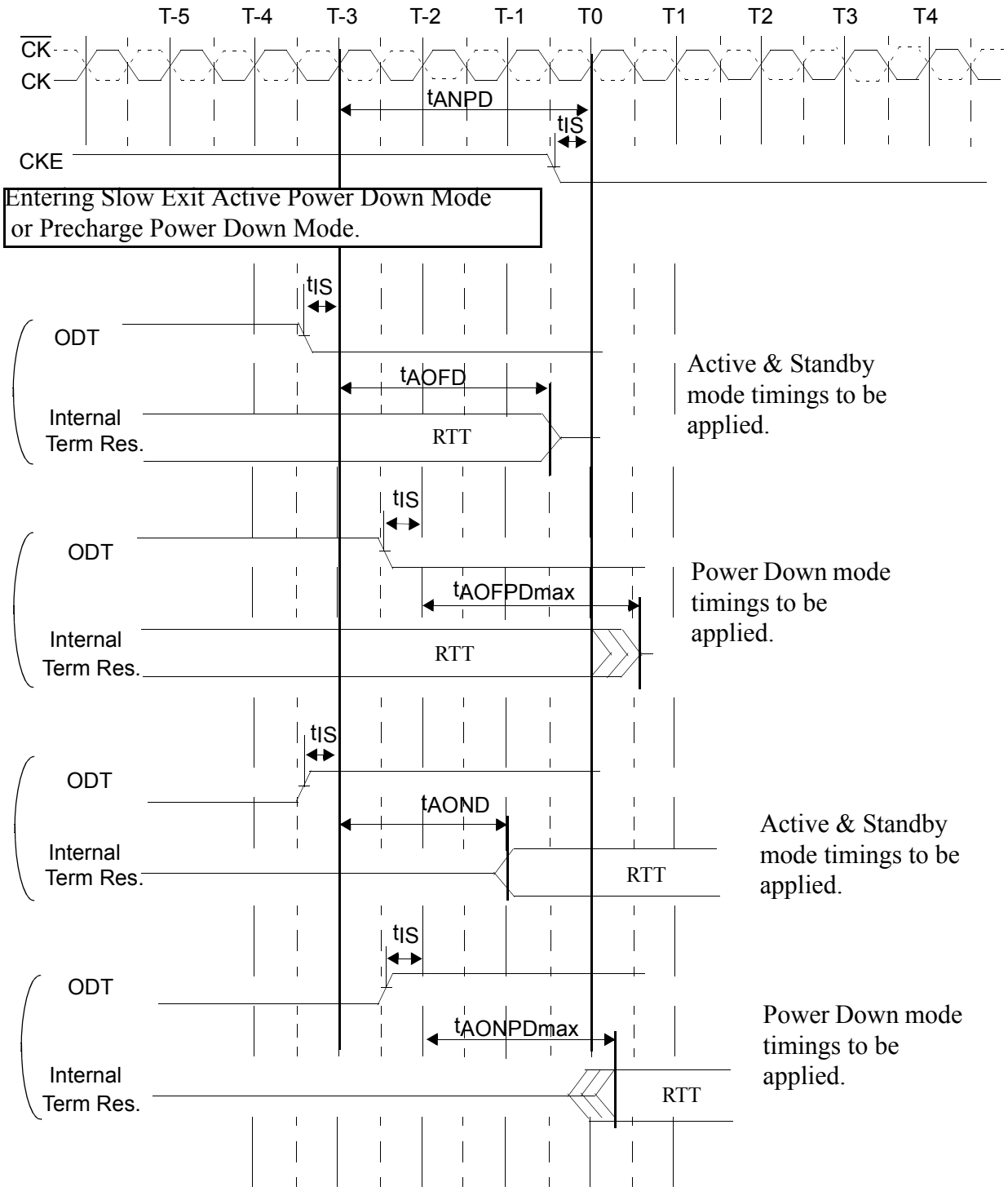


Figure 18 — ODT Timing Mode Switch at Entering Power Down Mode

2.2.2.4 ODT (On Die Termination) (cont'd)

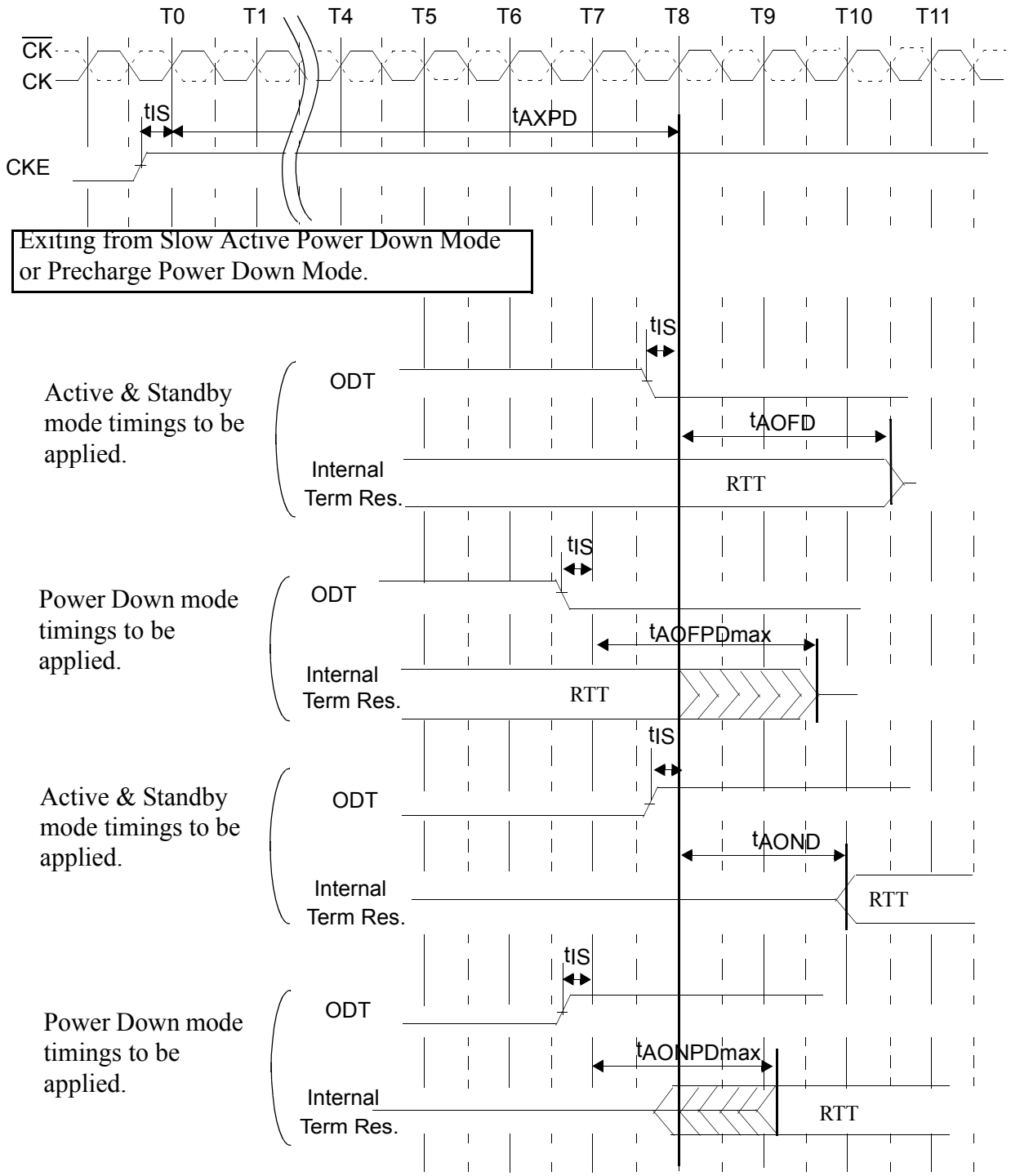


Figure 19 — ODT Timing Mode Switch at Exiting Power Down Mode

2.2.3 Bank Activate Command

The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The bank addresses BA0 ~ BA2 are used to select the desired bank. The row address A0 through A15 is used to determine which row to activate in the selected bank. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the tRCDmin specification, then additive latency must be programmed into the device to delay when the R/W command is internally issued to the device. The additive latency value must be chosen to assure tRCDmin is satisfied. Additive latencies of 0, 1, 2, 3 and 4 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between Bank Activate commands is t_{RRD}.

In order to ensure that 8 bank devices do not exceed the instantaneous current supplying capability of 4 bank devices, certain restrictions on operation of the 8 bank devices must be observed. There are two rules, one for restricting the number of sequential ACT commands that can be issued and another for allowing more time for $\overline{RAS}$ precharge for a Precharge All command. The rules are as follows:

1. 8 bank device Sequential Bank Activation Restriction: No more than 4 banks may be activated in a rolling 4 * tRRD + 2 * tCK window. tRRD must be converted to clocks prior to multiplying by 4 and prior to adding 2*tCK. Converting to clocks is done by dividing tRRD(ns) by tCK(ns) and rounding up to next integer value.
2. 8 bank device Precharge All Allowance: tRP for a Precharge All command for an 8 Bank device will equal to tRP + 1 * tCK, where tRP is the value for a single bank pre-charge.

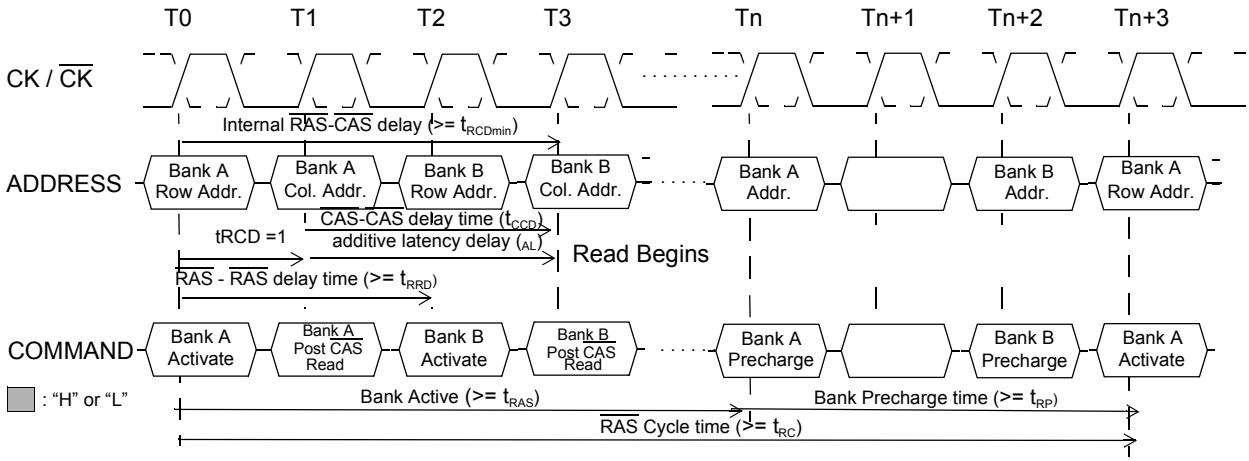


Figure 20 — Bank Activate Command Cycle: tRCD = 3, AL = 2, tRP = 3, tRRD = 2, tCCD = 2

2.2.4 Read and Write Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting $\overline{RAS}$ high, $\overline{CS}$ and $\overline{CAS}$ low at the clock's rising edge. $\overline{WE}$ must also be defined at this time to determine whether the access cycle is a read operation ($\overline{WE}$ high) or a write operation ($\overline{WE}$ low).

The DDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is strictly restricted to specific segments of the page length. For example, the 32Mbit x 4 I/O x 4 Bank chip has a page length of 2048 bits (defined by CA0-CA9, CA11). The page length of 2048 is divided into 512 or 256 uniquely addressable boundary segments depending on burst length, 512 for 4 bit burst, 256 for 8 bit burst respectively. A 4-bit or 8 bit burst operation will occur entirely within one of the 512 or 256 groups beginning with the column address supplied to the device during the Read or Write Command (CA0-CA9, CA11). The second, third and fourth access will also occur within this group segment, however, the burst order is a function of the starting address, and the burst sequence.

A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. However, in case of BL = 8 setting, two cases of interrupt by a new burst access are allowed, one reads interrupted by a read, the other writes interrupted by a write with 4 bit burst boundary respectively. The minimum $\overline{CAS}$ to $\overline{CAS}$ delay is defined by tCCD, and is a minimum of 2 clocks for read or write cycles.

2.2.4.1 Posted $\overline{CAS}$

Posted $\overline{CAS}$ operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a $\overline{CAS}$ read or write command to be issued immediately after the $\overline{RAS}$ bank activate command (or any time during the $\overline{RAS}$-$\overline{CAS}$-delay time, tRCD, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the $\overline{CAS}$ latency (CL). Therefore if a user chooses to issue a R/W command before the tRCDmin, then AL (greater than 0) must be written into the EMRS(1). The Write Latency (WL) is always defined as RL - 1 (read latency -1) where read latency is defined as the sum of additive latency plus $\overline{CAS}$ latency (RL=AL+CL). Read or Write operations using AL allow seamless bursts (refer to seamless operation timing diagram examples in Read burst and Write burst section).

Examples of posted $\overline{CAS}$ operation

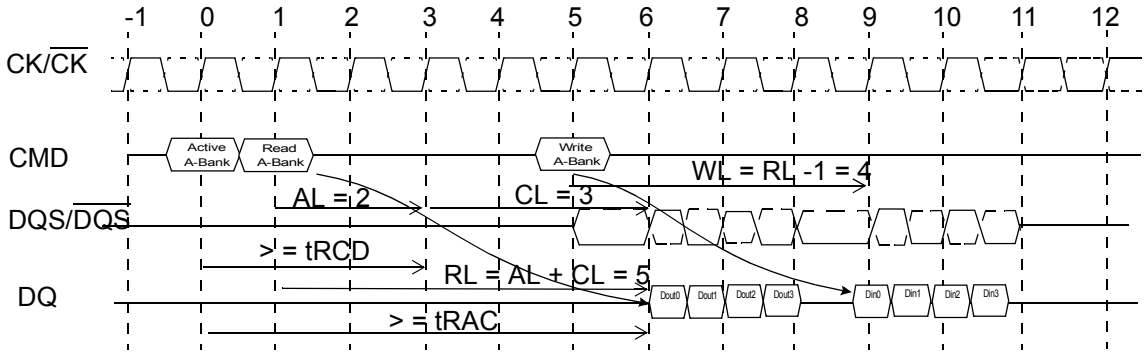


Figure 21 — Example 1: Read Followed by a Write to the Same Bank
[AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4]

2.2.4 Read and Write Access Modes (cont'd)

2.2.4.1 Posted $\overline{CAS}$ (cont'd)

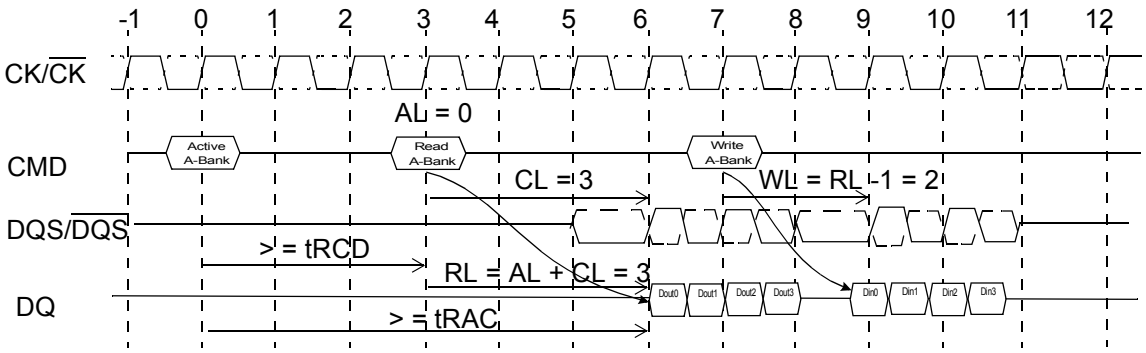


Figure 22 — Example 2: Read Followed by a Write to the Same Bank
[AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4]

2.2.4.2 Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. DDR2 SDRAM supports 4 bit burst and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MRS, which is similar to the DDR SDRAM operation. Seamless burst read or write operations are supported. Unlike DDR devices, interruption of a burst read or write cycle during BL = 4 mode operation is prohibited. However in case of BL = 8 mode, interruption of a burst read or write operation is limited to two cases, reads interrupted by a read, or writes interrupted by a write. Therefore the Burst Stop command is not supported on DDR2 SDRAM devices.

Table 8 — Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	0 0 0	0, 1, 2, 3	0, 1, 2, 3
	0 0 1	1, 2, 3, 0	1, 0, 3, 2
	0 1 0	2, 3, 0, 1	2, 3, 0, 1
	0 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

NOTE Page length is a function of I/O organization and column addressing.

2.2.4 Read and Write Access Modes (cont'd)

2.2.4.3 Burst Read Command

The Burst Read command is initiated by having $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low 1 clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus $\overline{CAS}$ latency (CL). The CL is defined by the Mode Register Set (MRS), similar to the existing SDR and DDR SDRAMs. The AL is defined by the Extended Mode Register Set (1)(EMRS(1)).

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single-ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at V_{REF}. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 ohm to 10 Kohm resistor to insure proper operation.

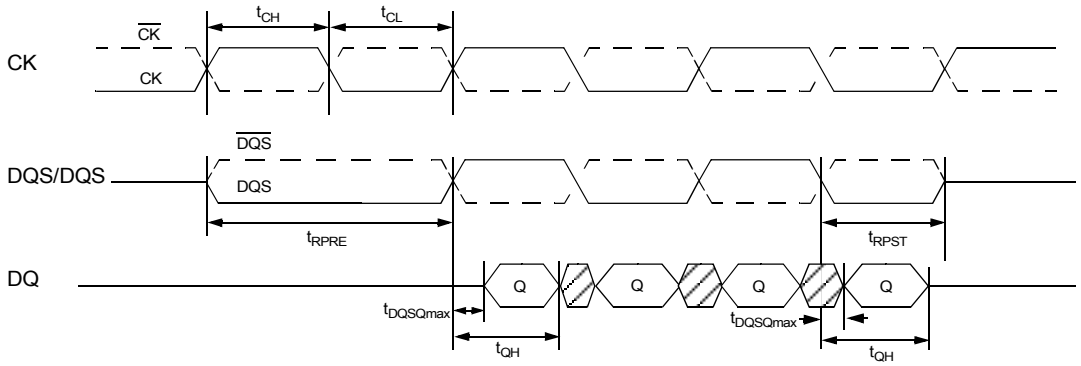


Figure 23 — Data Output (Read) Timing

2.2.4.3 Burst Read Command (cont'd)

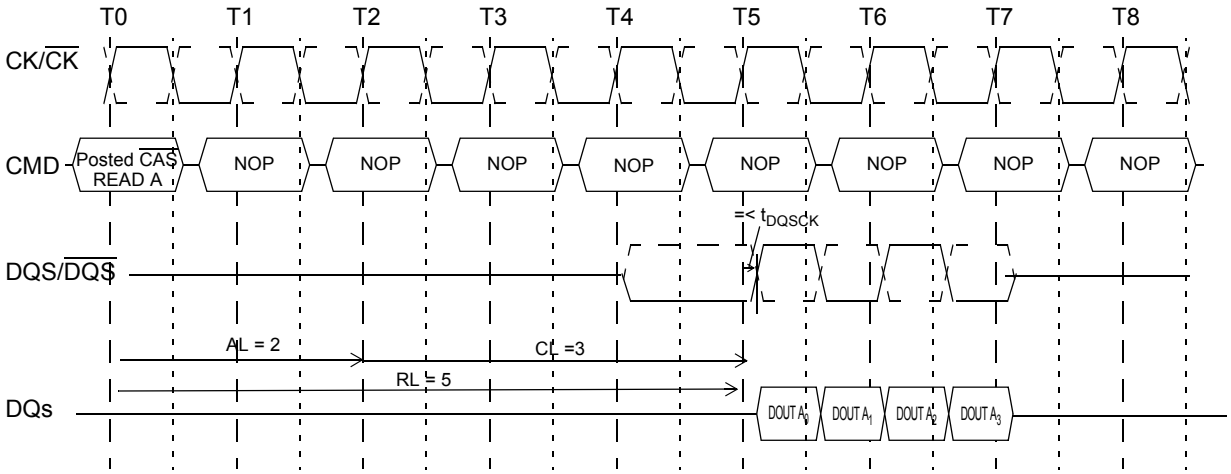


Figure 24 — Burst Read Operation: RL = 5 (AL = 2, CL = 3, BL = 4)

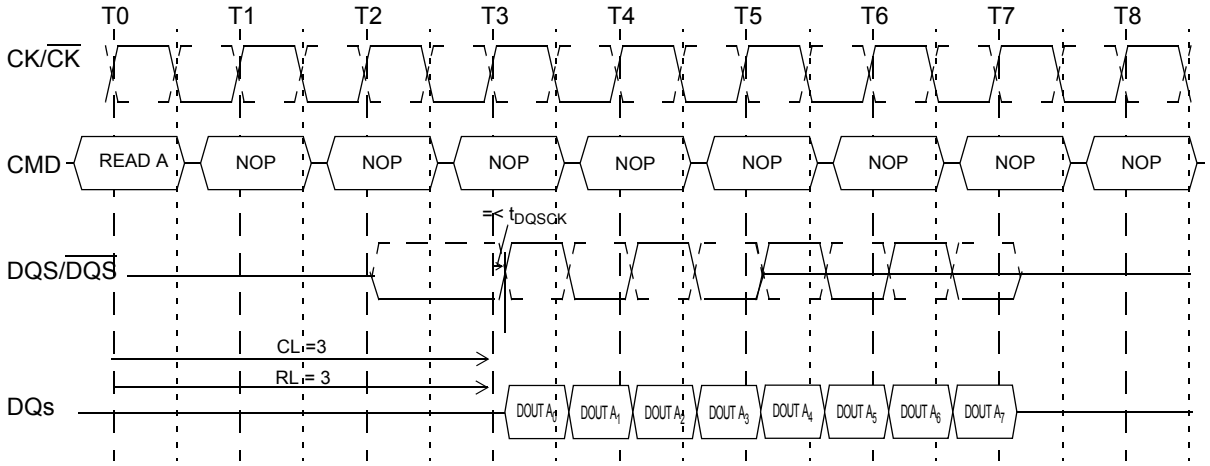
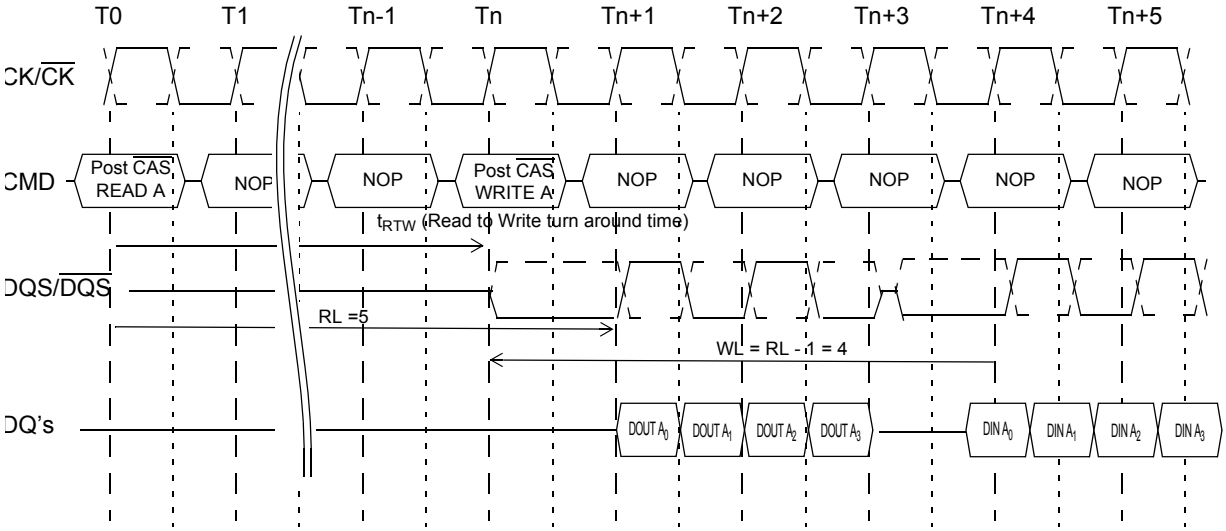


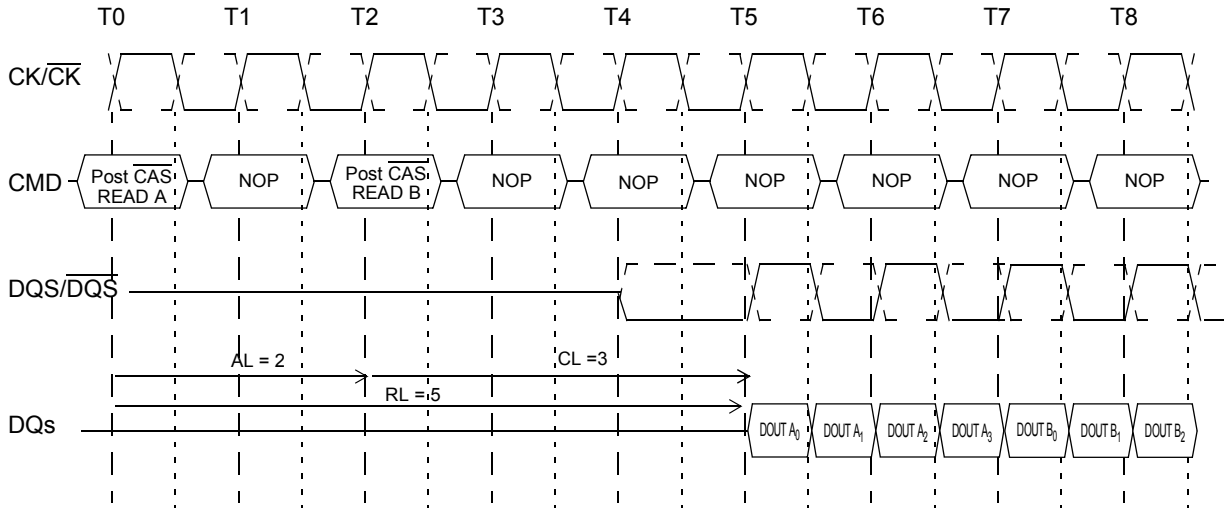
Figure 25 — Burst Read Operation: RL = 3 (AL = 0 and CL = 3, BL = 8)

2.2.4.3 Burst Read Command (cont'd)



The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation.

Figure 26 — Burst Read Followed by Burst Write: RL = 5, WL = (RL-1) = 4, BL = 4



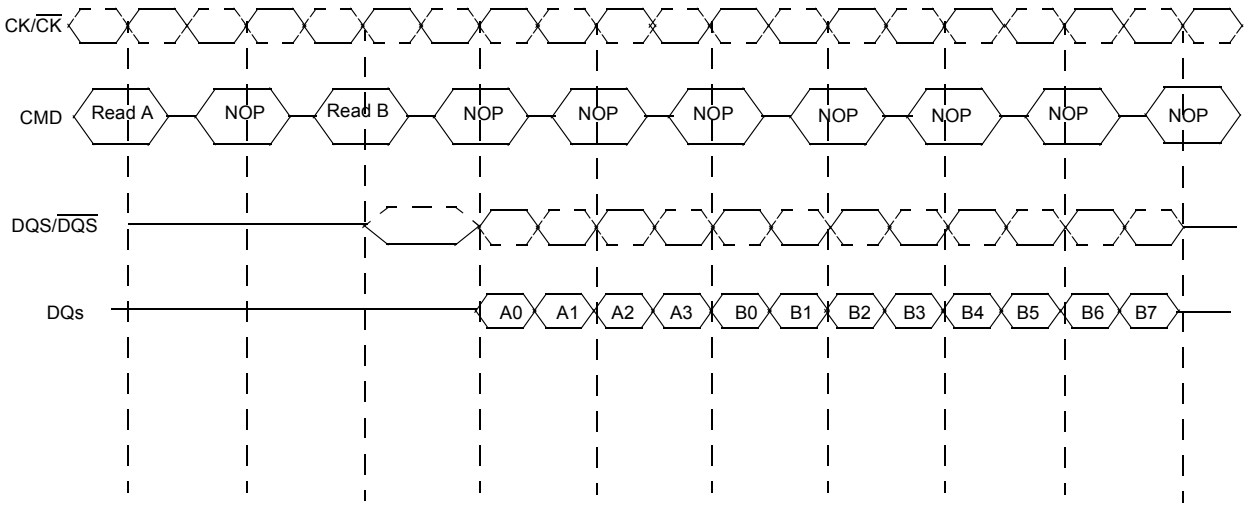
The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 27 — Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

Reads Interrupted by a Read

Burst read can only be interrupted by another read with 4 bit burst boundary. Any other case of read interrupt is not allowed.

2.2.4.3 Burst Read Command (cont'd)



NOTE 1 Read burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.
NOTE 2 Read burst of 8 can only be interrupted by another Read command. Read burst interruption by Write command or Precharge command is prohibited.
NOTE 3 Read burst interrupt must occur exactly two clocks after previous Read command. Any other Read burst interrupt timings are prohibited.
NOTE 4 Read burst interruption is allowed to any bank inside DRAM.
NOTE 5 Read burst with Auto Precharge enabled is not allowed to interrupt.
NOTE 6 Read burst interruption is allowed by another Read with Auto Precharge command.
NOTE 7 All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, Minimum Read to Precharge timing is AL + BL/2 where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt).

Figure 28 — Read Burst Interrupt Timing Example: (CL=3, AL=0, RL=3, BL=8)

2.2.4.4 Burst Write Operation

The Burst Write command is initiated by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1). A data strobe signal (DQS) should be driven low (preamble) one clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed, which is 4 or 8 bit burst. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ Signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is the write recovery time (WR).

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at V_{REF}. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 ohm to 10 Kohm resistor to insure proper operation.

2.2.4.4 Burst Write Operation (cont'd)

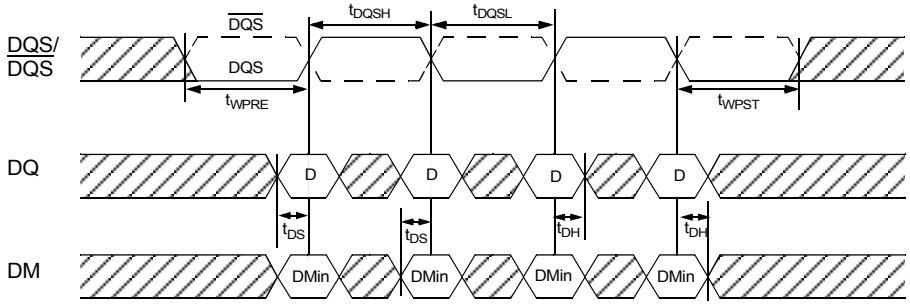


Figure 29 — Data Input (Write) Timing

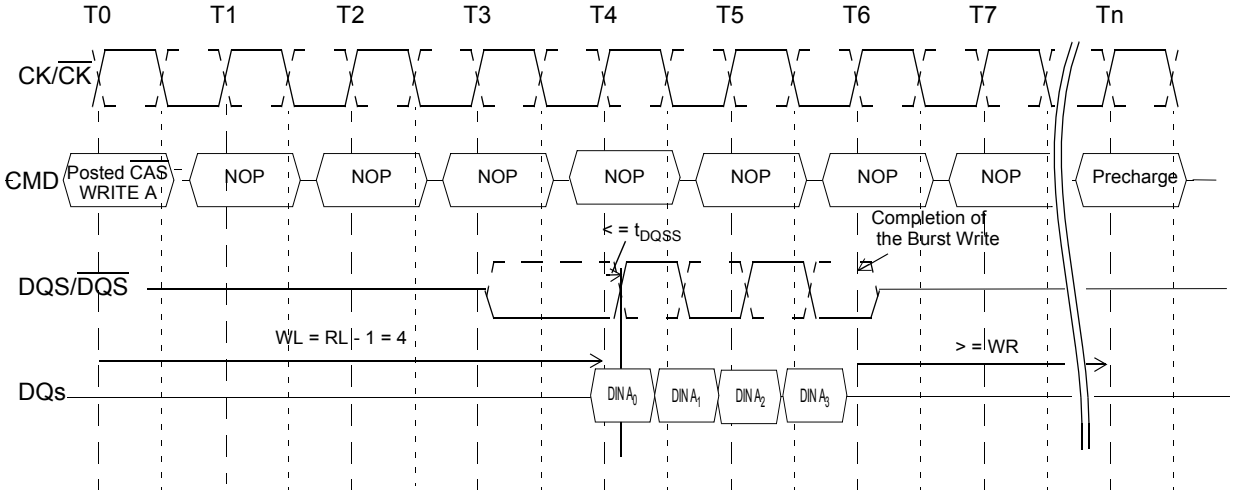


Figure 30 — Burst Write Operation: RL = 5, WL = 4, tWR = 3 (AL=2, CL=3), BL = 4

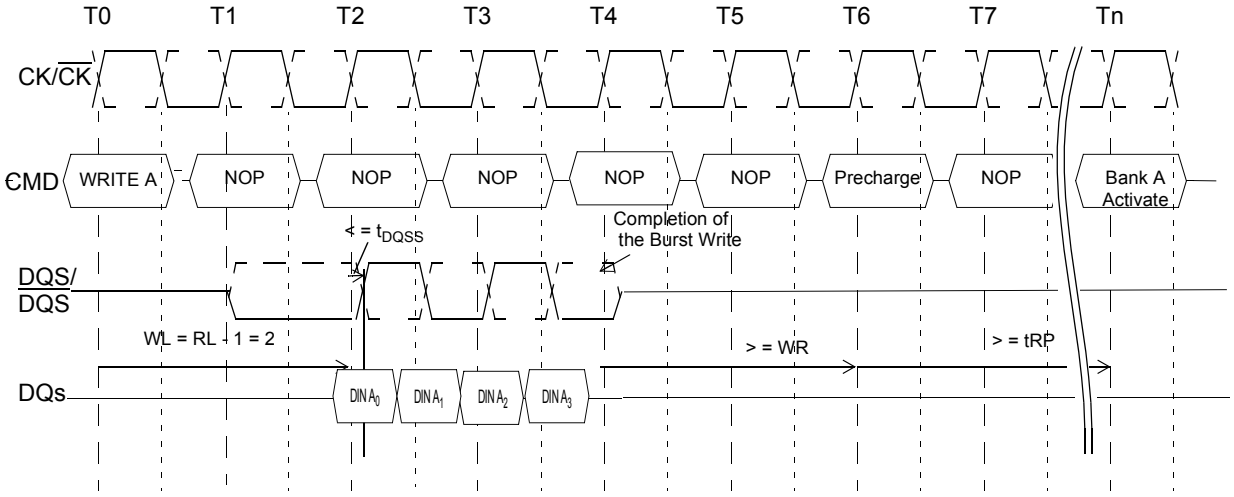
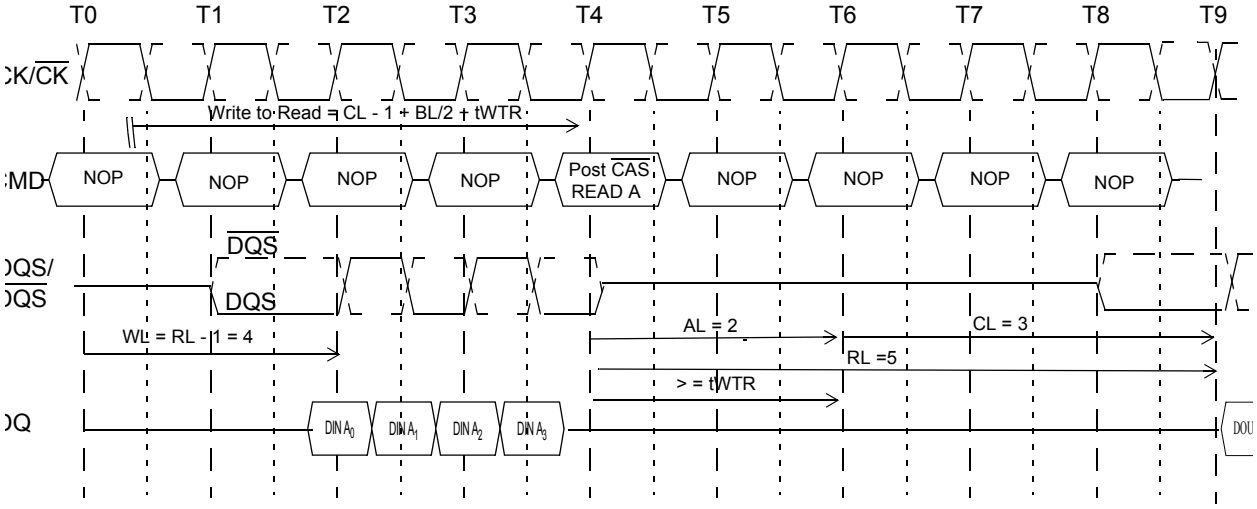


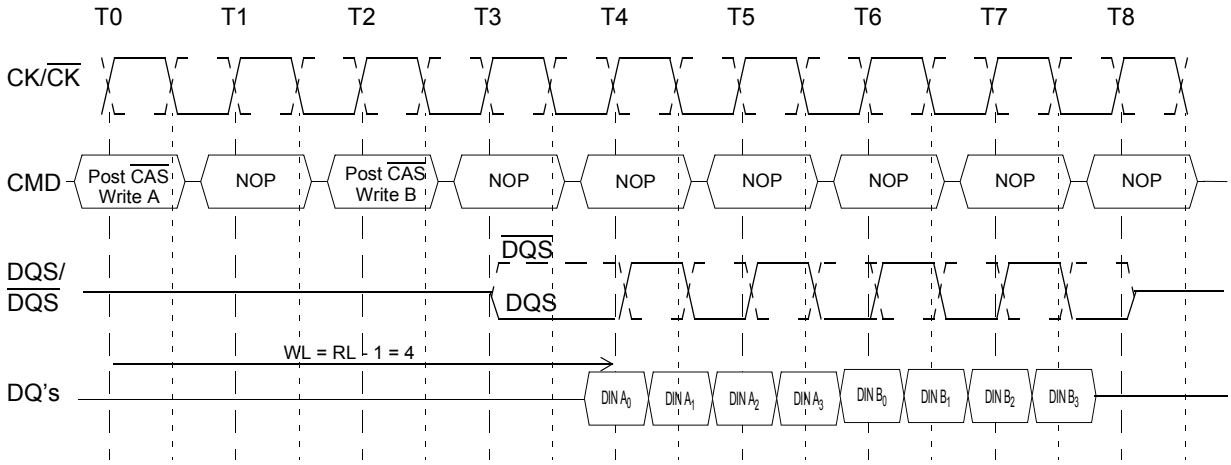
Figure 31 — Burst Write Operation: RL = 3, WL = 2, tWR = 2 (AL=0, CL=3), BL = 4

2.2.4.4 Burst Write Operation (cont'd)



The minimum number of clock from the burst write command to the burst read command is [CL - 1 + BL/2 + tWTR]. This tWTR is not a write recovery time (tWR) but the time required to transfer the 4bit write data from the input buffer into sense amplifiers in the array. tWTR is defined in AC spec table of this data sheet.

Figure 32 — Burst Write Followed by Burst Read: RL = 5 (AL=2, CL=3), WL = 4, tWTR = 2, BL = 4



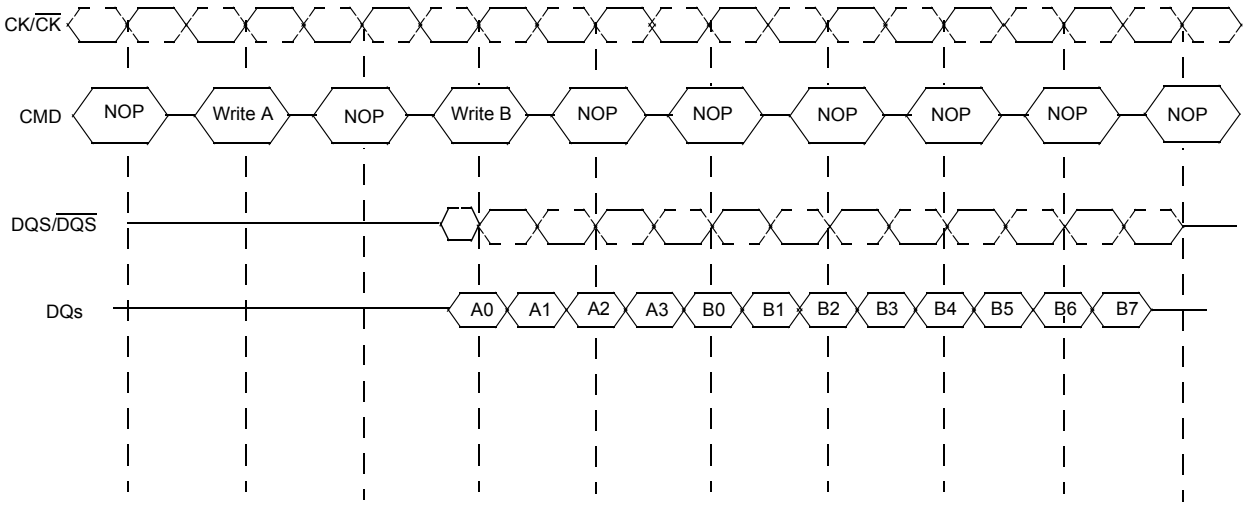
The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for
BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 33 — Seamless Burst Write Operation: RL = 5, WL = 4, BL = 4

Writes Interrupted by a Write

Burst write can only be interrupted by another write with 4 bit burst boundary. Any other case of write interrupt is not allowed.

2.2.4.4 Burst Write Operation (cont'd)



NOTE 1 Write burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.

NOTE 2 Write burst of 8 can only be interrupted by another Write command. Write burst interruption by Read command or Precharge command is prohibited.

NOTE 3 Write burst interrupt must occur exactly two clocks after previous Write command. Any other Write burst interrupt timings are prohibited.

NOTE 4 Write burst interruption is allowed to any bank inside DRAM.

NOTE 5 Write burst with Auto Precharge enabled is not allowed to interrupt.

NOTE 6 Write burst interruption is allowed by another Write with Auto Precharge command.

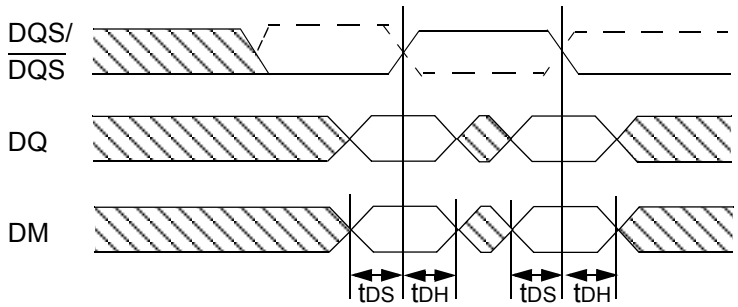
NOTE 7 All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, minimum Write to Precharge timing is WL+BL/2+tWR where tWR starts with the rising clock after the un-interrupted burst end and not from the end of actual burst end.

Figure 34 — Write Burst Interrupt Timing Example: (CL=3, AL=0, RL=3, WL=2, BL=8)

2.2.4.5 Write Data Mask

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR2 SDRAMs, consistent with the implementation on DDR SDRAMs. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to insure matched system timing. DM of x4 and x16 bit organization is not used during read cycles. However DM of x8 bit organization can be used as RDQS during read cycles by EMRS(1) setting.

Data Mask Timing



Data Mask Function, WL=3, AL=0, BL = 4 shown

Case 1: min t_{DQSS}

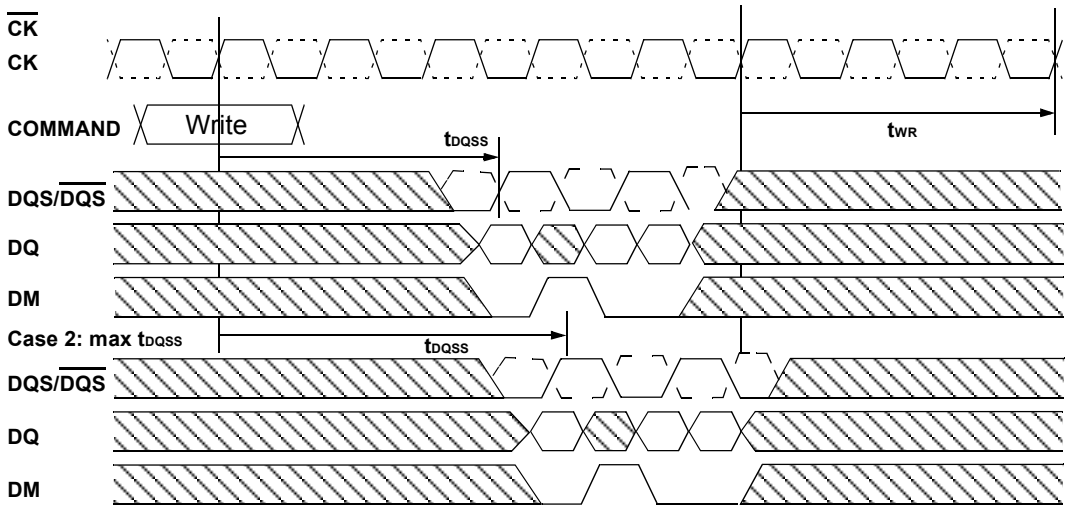


Figure 35 — Write Data Mask

2.2.5 Precharge Operation

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA0 and BA1 for 256Mb and 512Mb and four address bits A10, BA0 ~ BA2 for 1Gb and higher densities are used to define which bank to precharge when the command is issued. For 8 bank devices, refer to Section 2.2.3 of this data sheet.

2.2.5 Precharge Operation (cont'd)

Table 9 — Bank Selection for Precharge by Address Bits

A10	BA2	BA0	BA1	Precharged Bank(s)	Remarks
LOW	LOW	LOW	LOW	Bank 0 only	
LOW	LOW	LOW	HIGH	Bank 1 only	
LOW	LOW	HIGH	LOW	Bank 2 only	
LOW	LOW	HIGH	HIGH	Bank 3 only	
LOW	HIGH	LOW	LOW	Bank 4 only	1 Gb and higher
LOW	HIGH	LOW	HIGH	Bank 5 only	1 Gb and higher
LOW	HIGH	HIGH	LOW	Bank 6 only	1 Gb and higher
LOW	HIGH	HIGH	HIGH	Bank 7 only	1 Gb and higher
HIGH	DON'T CARE	DON'T CARE	DON'T CARE	All Banks	

2.2.5.1 Burst Read Operation Followed by Precharge

Minimum Read to precharge command spacing to the same bank = AL + BL/2 clocks
For the earliest possible precharge, the precharge command may be issued on the rising edge which is "Additive latency(AL) + BL/2 clocks" after a Read command. A new bank active (command) may be issued to the same bank after the RAS precharge time (t_{RP}). A precharge command cannot be issued until t_{RAS} is satisfied.

The minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read to Precharge command. This time is called tRTP (Read to Precharge). For BL = 4 this is the time from the actual read (AL after the Read command) to Precharge command. For BL = 8 this is the time from AL + 2 clocks after the Read to the Precharge command.

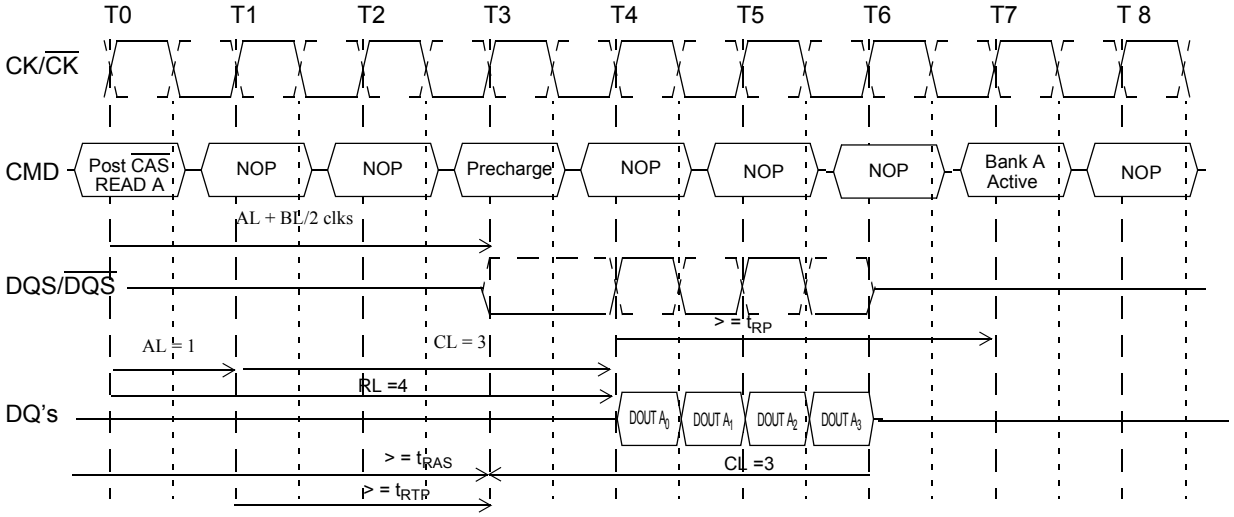


Figure 36 — Example 1: Burst Read Operation Followed by Precharge: RL = 4, AL = 1, CL = 3, BL = 4, t_{RTP} <= 2 clocks

2.2.5.1 Burst Read Operation Followed by Precharge (cont'd)

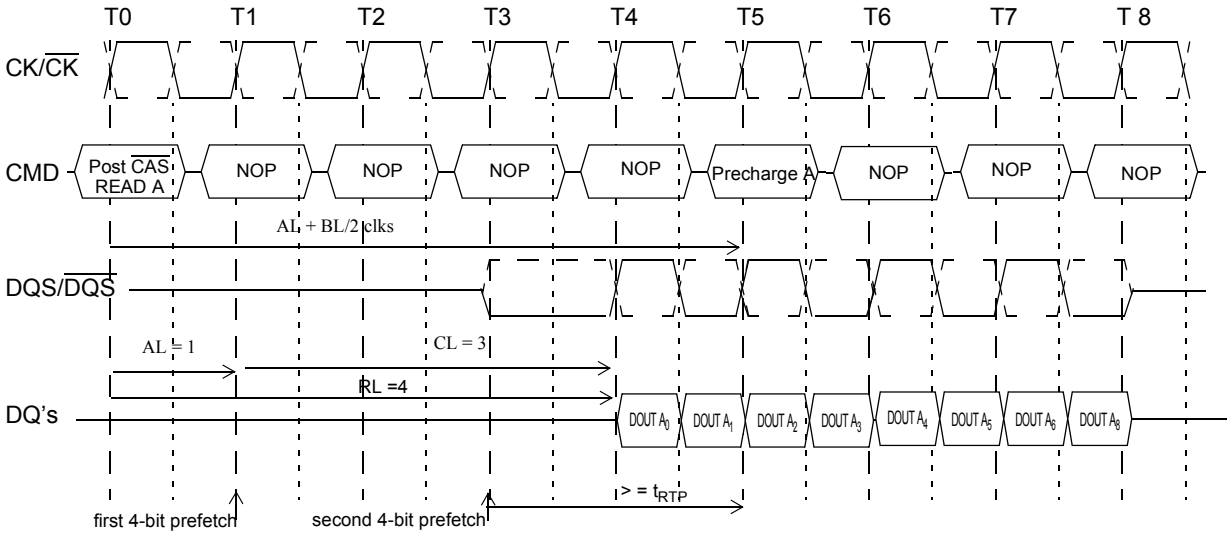


Figure 37 — Example 2: Burst Read Operation Followed by Precharge: RL = 4, AL = 1, CL = 3, BL = 8, t_{RTP} <= 2 clocks

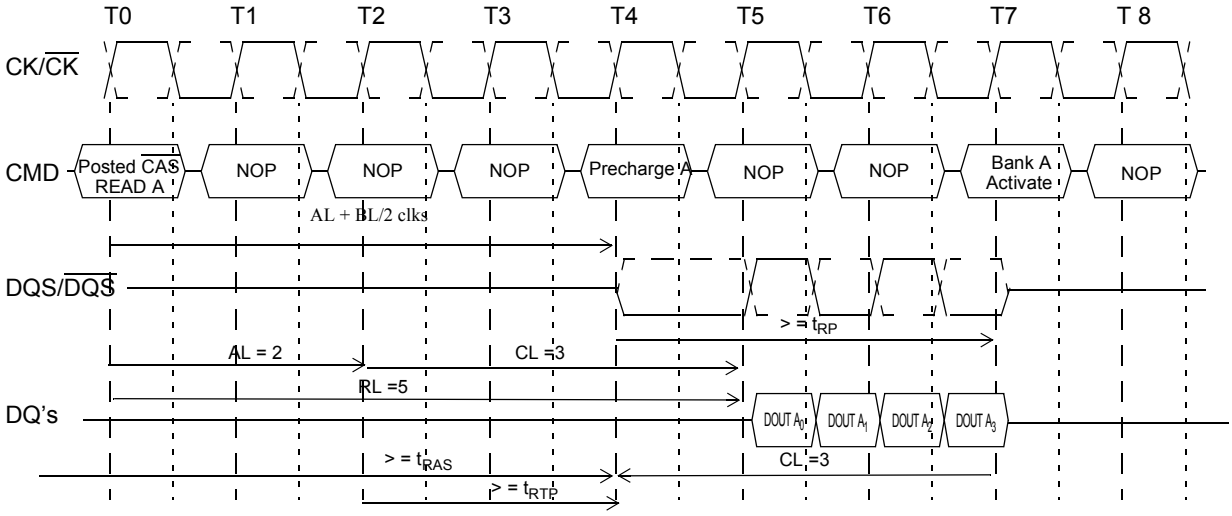


Figure 38 — Example 3: Burst Read Operation Followed by Precharge: RL = 5, AL = 2, CL = 3, BL = 4, t_{RTP} <= 2 clocks

2.2.5.1 Burst Read Operation Followed by Precharge (cont'd)

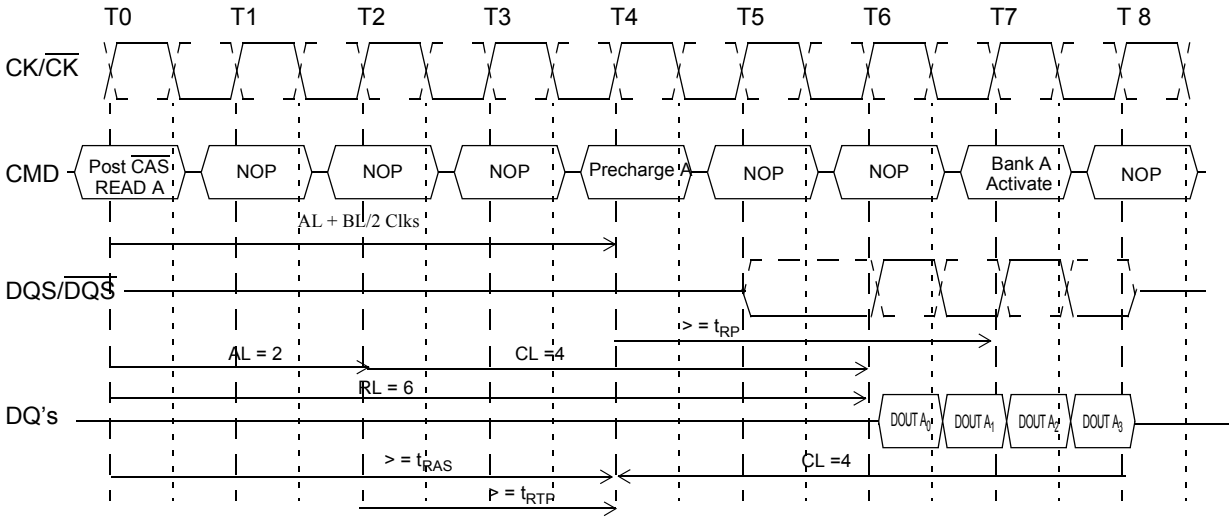
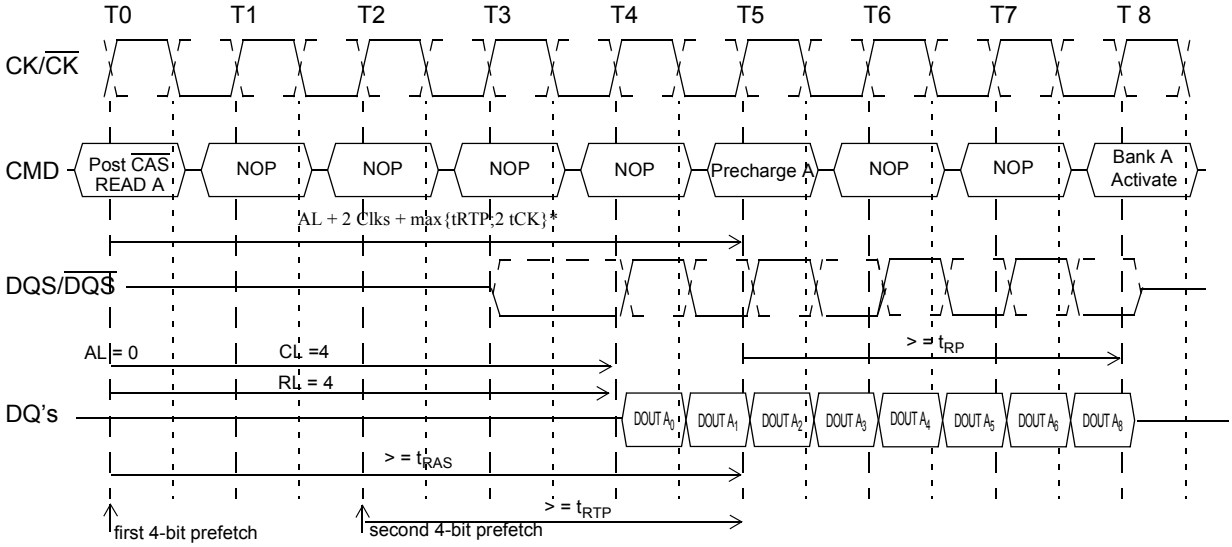


Figure 39 — Example 4: Burst Read Operation Followed by Precharge: RL = 6, AL = 2, CL = 4, BL = 4, t_{RTP} <= 2 clocks



*: rounded to next integer

Figure 40 — Example 5: Burst Read Operation Followed by Precharge: RL = 4, AL = 0, CL = 4, BL = 8, t_{RTP} > 2 clocks

2.2.5.2 Burst Write followed by Precharge

Minimum Write to Precharge Command spacing to the same bank = WL + BL/2 clks + tWR

For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge Command can be issued. This delay is known as a write recovery time (tWR) referenced from the completion of the burst write to the precharge command. No Precharge command should be issued prior to the tWR delay.

2.2.5.2 Burst Write followed by Precharge (cont'd)

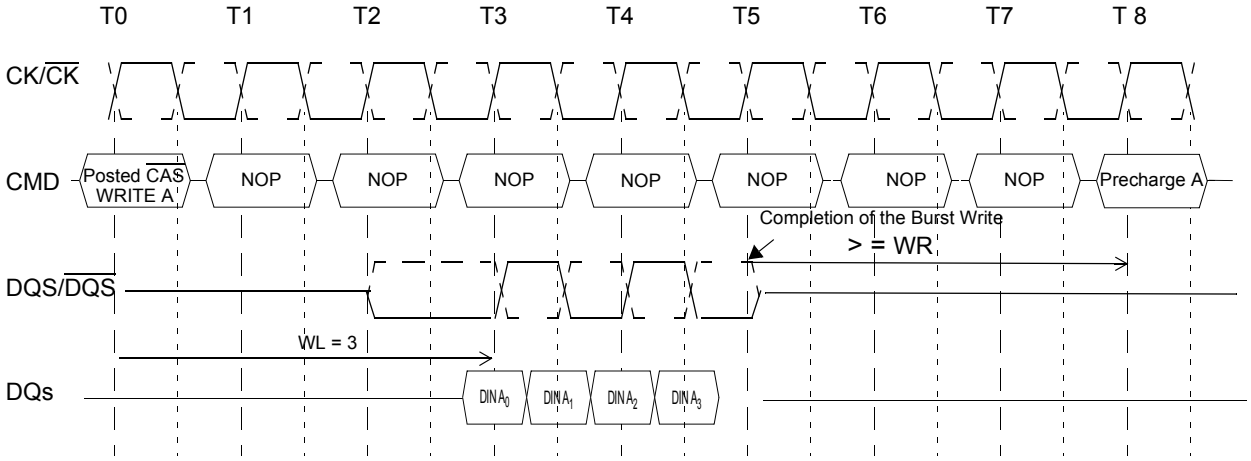


Figure 41 — Example 1: Burst Write followed by Precharge: WL = (RL-1) =3

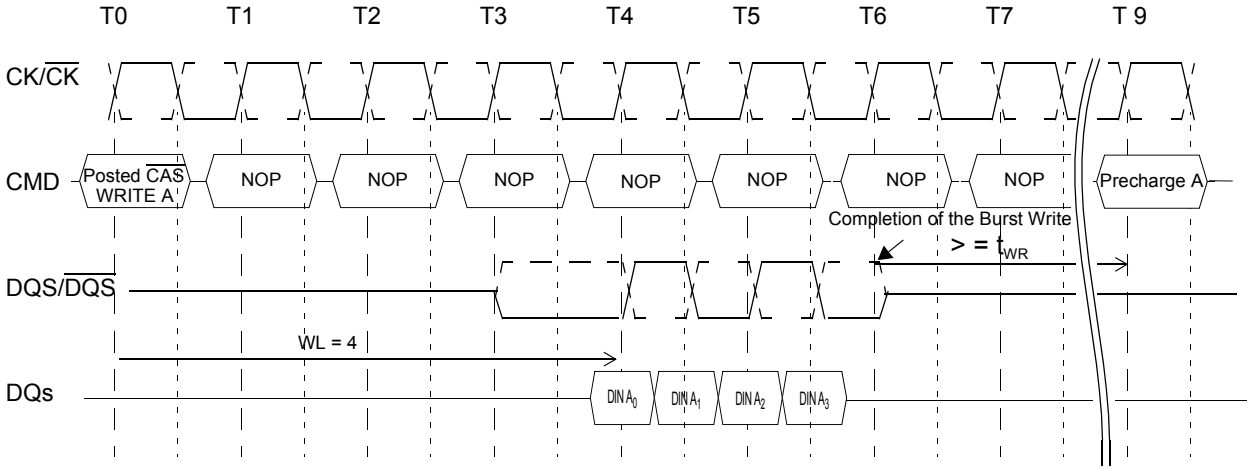


Figure 42 — Example 2: Burst Write followed by Precharge: WL = (RL-1) = 4

2.2.6 Auto Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is given to the DDR2 SDRAM, the $\overline{CAS}$ timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the READ or WRITE command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write command is issued, then the auto-precharge function is engaged. During auto-precharge, a Read command will execute as normal with the exception that the active bank will begin to precharge on the rising edge which is $\overline{CAS}$ latency (CL) clock cycles before the end of the read burst.

Auto-precharge is also implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.

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2.2.6 Auto Precharge Operation (cont'd)

This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon $\overline{CAS}$ latency) thus improving system performance for random data access. The $\overline{RAS}$ lockout circuit internally delays the Precharge operation until the array restore operation has been completed (tRAS satisfied) so that the auto precharge command may be issued with any read or write command.

2.2.6.1 Burst Read with Auto Precharge

If A10 is high when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR2 SDRAM starts an Auto Precharge operation on the rising edge which is (AL + BL/2) cycles later than the read with AP command if tRAS(min) and tRTP(min) are satisfied.

If tRAS(min) is not satisfied at the edge, the start point of auto-precharge operation will be delayed until tRAS(min) is satisfied.

If tRTP(min) is not satisfied at the edge, the start point of auto-precharge operation will be delayed until tRTP(min) is satisfied.

In case the internal precharge is pushed out by tRTP, tRP starts at the point where the internal precharge happens (not at the next rising clock edge after this event). So for BL = 4 the minimum time from Read_AP to the next Activate command becomes AL + (tRTP + tRP)* (see example 2) for BL = 8 the time from Read_AP to the next Activate is AL + 2 + (tRTP + tRP)*, where "*" means: "rounded up to the next integer". In any event internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

A new bank activate (command) may be issued to the same bank if the following two conditions are satisfied simultaneously.
(1) The $\overline{RAS}$ precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
(2) The $\overline{RAS}$ cycle time (tRC) from the previous bank activation has been satisfied.

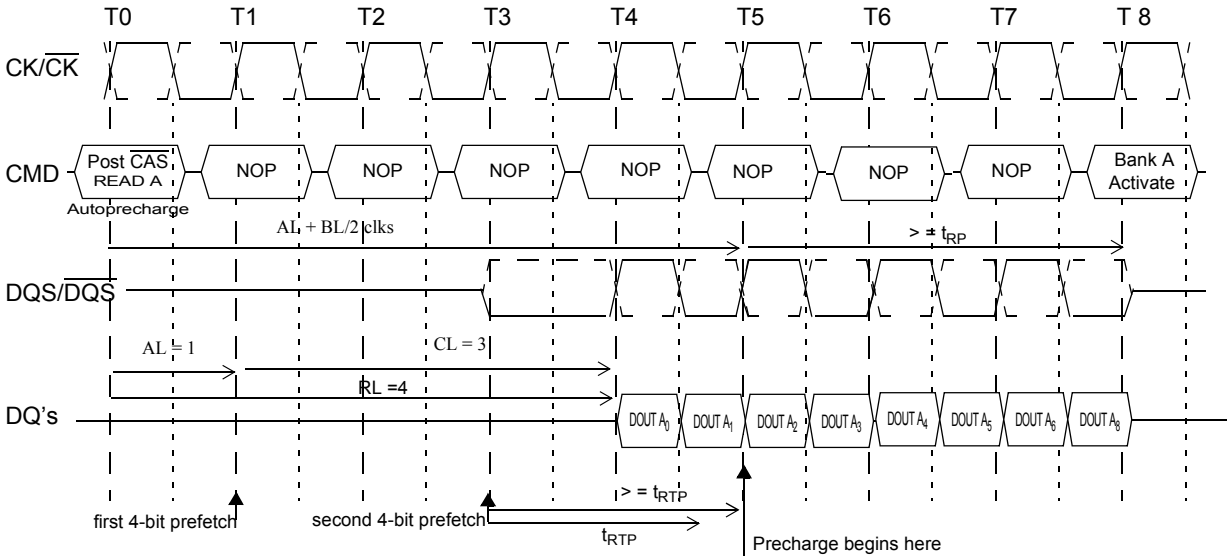


Figure 43 — Example 1: Burst Read Operation with Auto Precharge: RL = 4, AL = 1, CL = 3, BL = 8, t_{RTP} <= 2 clocks

2.2.6.1 Burst Read with Auto Precharge (cont'd)

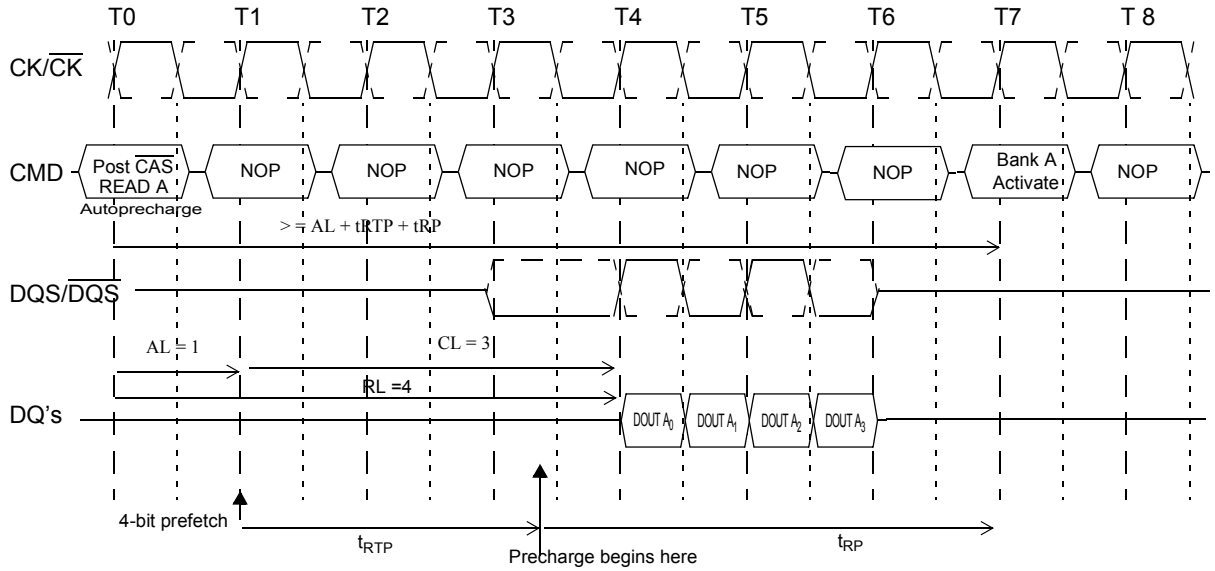


Figure 44 — Example 2: Burst Read Operation with Auto Precharge: RL = 4, AL = 1, CL = 3, BL = 4, t_{RTP} > 2 clocks

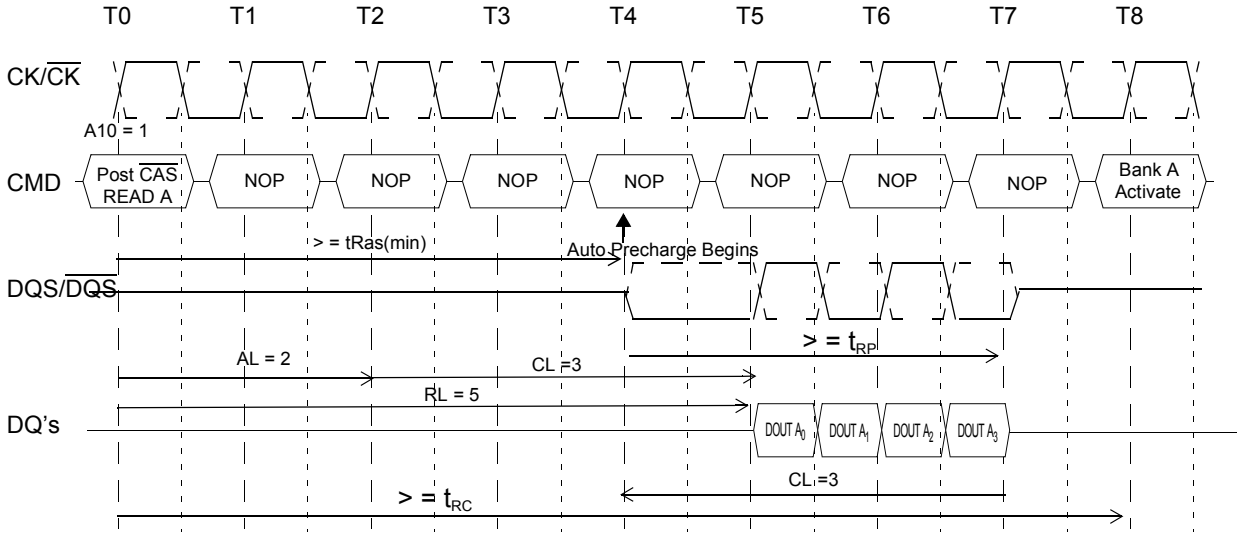


Figure 45 — Example 3: Burst Read with Auto Precharge Followed by an Activation to the Same Bank(tRC Limit): RL = 5 (AL = 2, CL = 3, internal tRCD = 3, BL = 4, t_{RTP} <= 2 clocks)

2.2.6.1 Burst Read with Auto Precharge (cont'd)

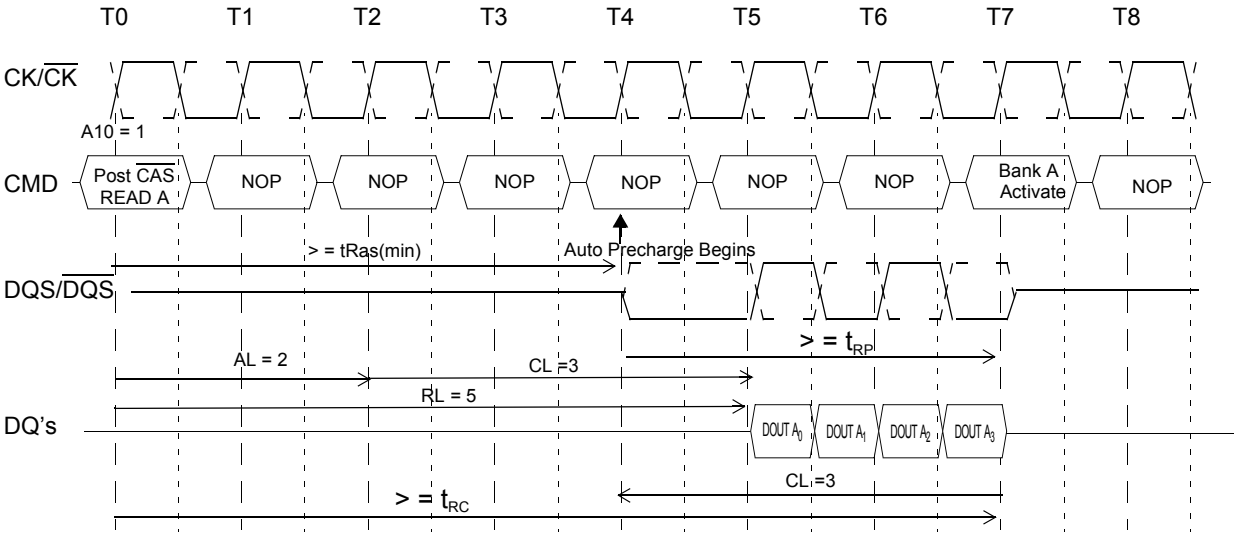


Figure 46 — Example 4: Burst Read with Auto Precharge Followed by an Activation to the Same Bank (tRP Limit): RL = 5 (AL = 2, CL = 3, internal tRCD = 3, BL = 4, t_{RTP} <= 2 clocks)

2.2.6.2 Burst Write with Auto-Precharge

If A10 is high when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the burst write plus write recovery time (tWR). The bank undergoing auto-precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

1) The data-in to bank activate delay time (WR + tRP) has been satisfied.
2) The RAS cycle time (tRC) from the previous bank activation has been satisfied.

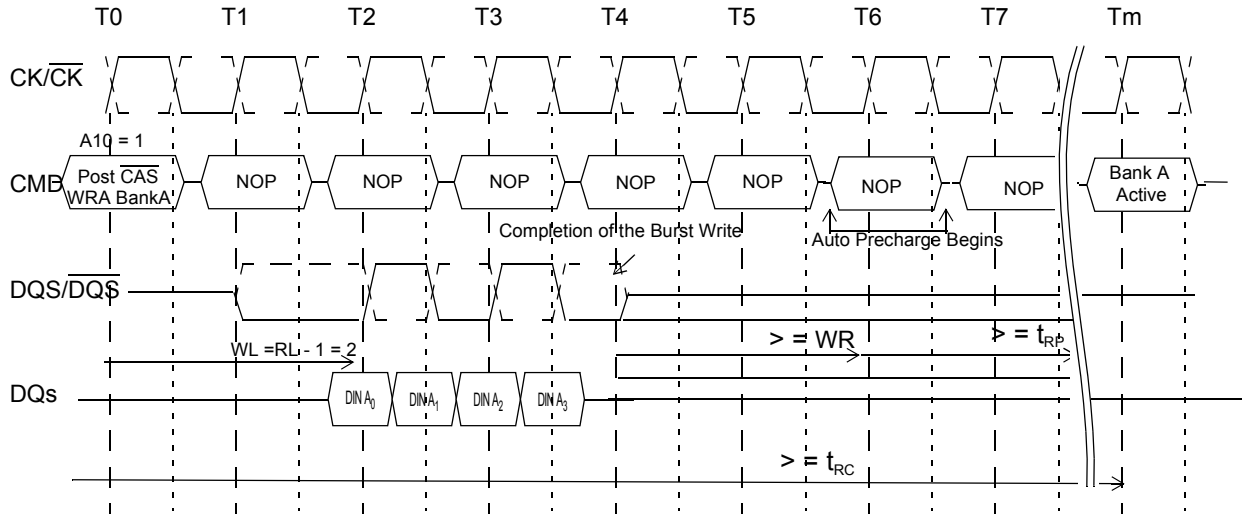


Figure 47 — Burst Write with Auto-Precharge (tRC Limit): WL = 2, tWR =2, BL = 4, tRP=3

2.2.6.2 Burst Write with Auto-Precharge (cont'd)

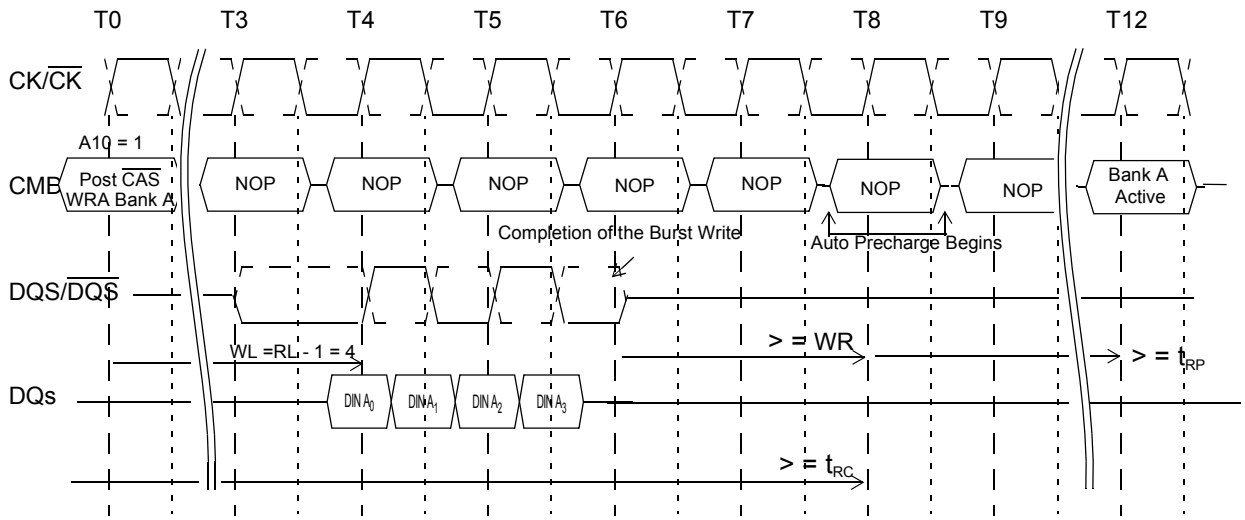


Figure 48 — Burst Write with Auto-Precharge (tWR + tRP): WL = 4, tWR =2, BL = 4, tRP=3

2.2.7 Refresh Command

When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held low and $\overline{WE}$ high at the rising edge of the clock, the chip enters the Refresh mode (REF). All banks of the DDR2 SDRAM must be precharged and idle for a minimum of the Precharge time (tRP) before the Refresh command (REF) can be applied. An address counter, internal to the device, supplies the bank address during the refresh cycle. No control of the external address bus is required once this cycle has started.
When the refresh cycle has completed, all banks of the DDR2 SDRAM will be in the precharged (idle) state. A delay between the Refresh command (REF) and the next Activate command or subsequent Refresh command must be greater than or equal to the Refresh cycle time (tRFC).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 * tREFI.

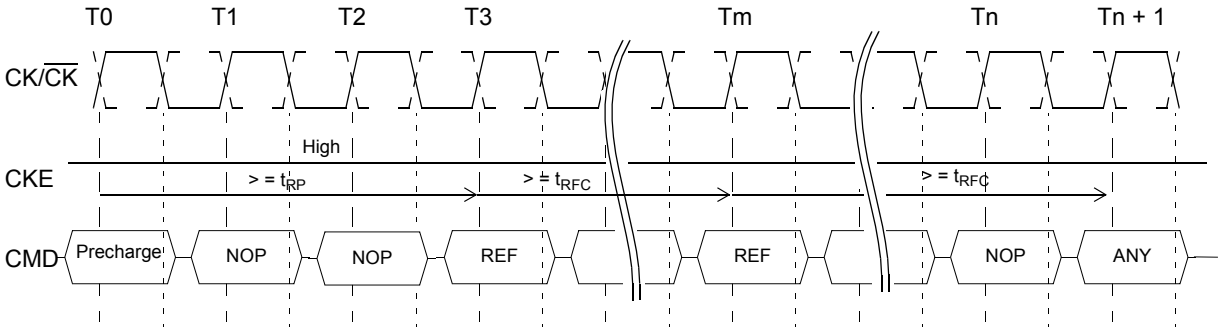
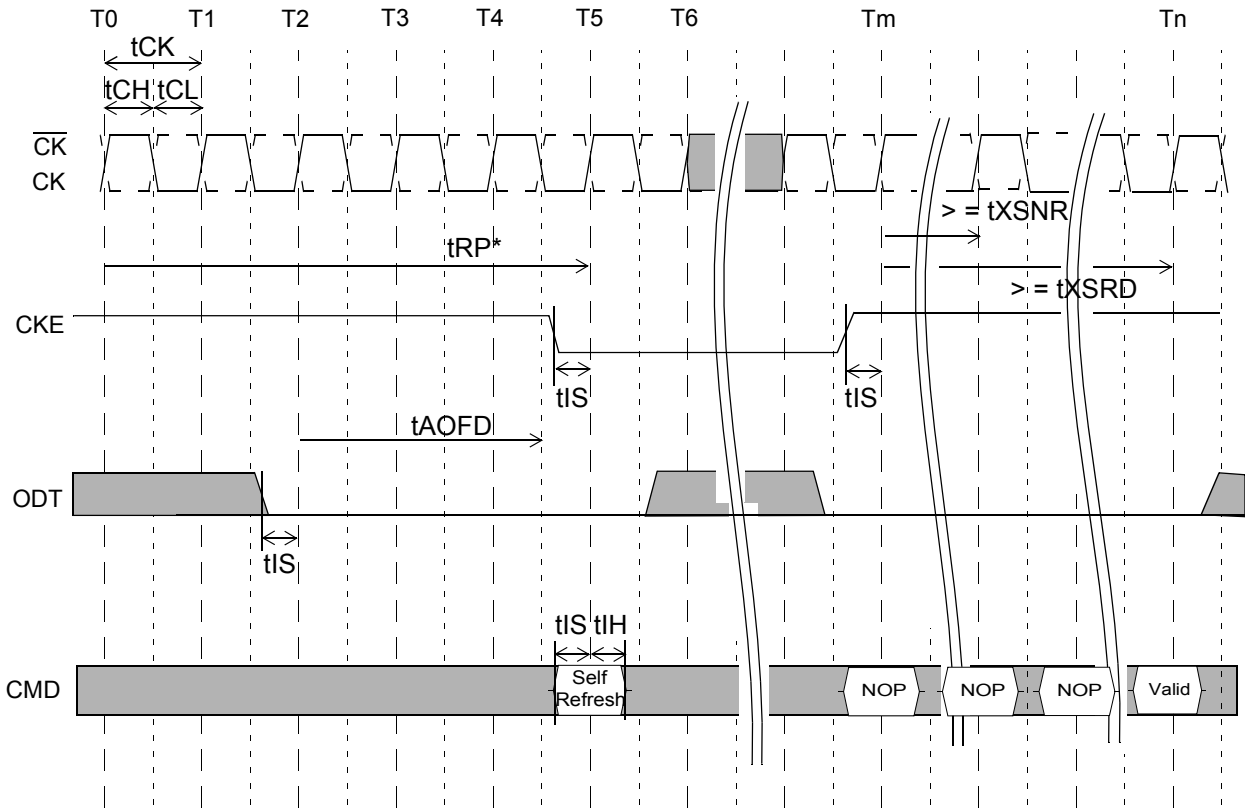


Figure 49 — Refresh Command

2.2.8 Self Refresh Operation

The DDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. ODT must be turned off before issuing Self Refresh command, by either driving ODT pin low or using EMRS command. Once the Command is registered, CKE must be held low to keep the device in Self Refresh mode. When the DDR2 SDRAM has entered Self Refresh mode all of the external signals except CKE, are “don’t care”. The clock is internally disabled during Self Refresh Operation to save power. The user may change the external clock frequency or halt the external clock one clock after Self-Refresh entry is registered, however, the clock must be restarted and stable before the device can exit Self Refresh operation. Once Self Refresh Exit command is registered, a delay equal to or longer than the tXSNR or tXSRD must be satisfied before a valid command can be issued to the device. CKE must remain high for the entire Self Refresh exit period tXSRD for proper operation. NOP or deselect commands must be registered on each positive clock edge during the Self Refresh exit interval. ODT should also be turned off during tXSRD.



- Device must be in the “All banks idle” state prior to entering Self Refresh mode.
- ODT must be turned off tAOFD before entering Self Refresh mode, and can be turned on again when tXSRD timing is satisfied.
- tXSRD is applied for a Read or a Read with autoprecharge command
- tXSNR is applied for any command except a Read or a Read with autoprecharge command.

Figure 50 — Self Refresh Operation

2.2.9 Power-Down

Power-down is synchronously entered when CKE is registered low (along with Nop or Deselect command). CKE is not allowed to go low while mode register or extended mode register command time, or read or write operation is in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or autoprecharge, or auto-refresh is in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in Figures 51 through 59 with details for entry into power down.

The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation.

If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$, ODT and CKE. Also the DLL is disabled upon entering precharge power-down or slow exit active power-down, but the DLL is kept enabled during fast exit active power-down. In power-down mode, CKE low and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and ODT should be in a valid state but all other input signals are “Don’t Care”. CKE low must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a Nop or Deselect command). CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP, tXARD, or tXARDS, after CKE goes high. Power-down exit latency is defined at AC spec table of this data sheet.

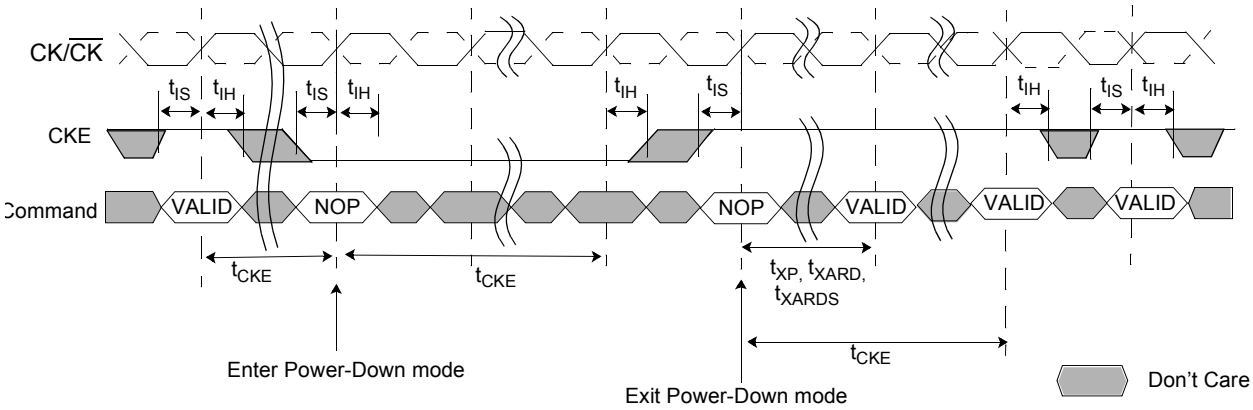


Figure 51 — Basic Power Down Entry and Exit Timing Diagram

2.2.9 Power-Down (cont'd)

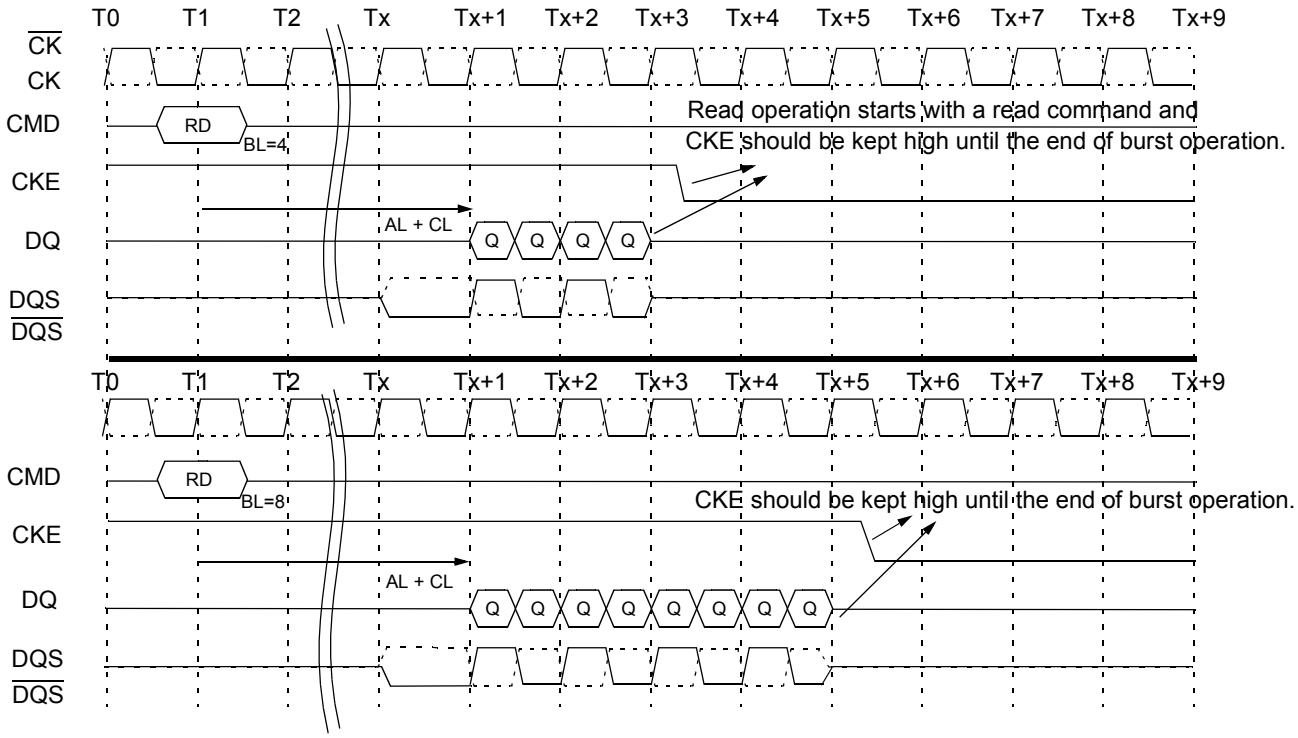


Figure 52 — Read to Power Down Entry

2.2.9 Power-Down (cont'd)

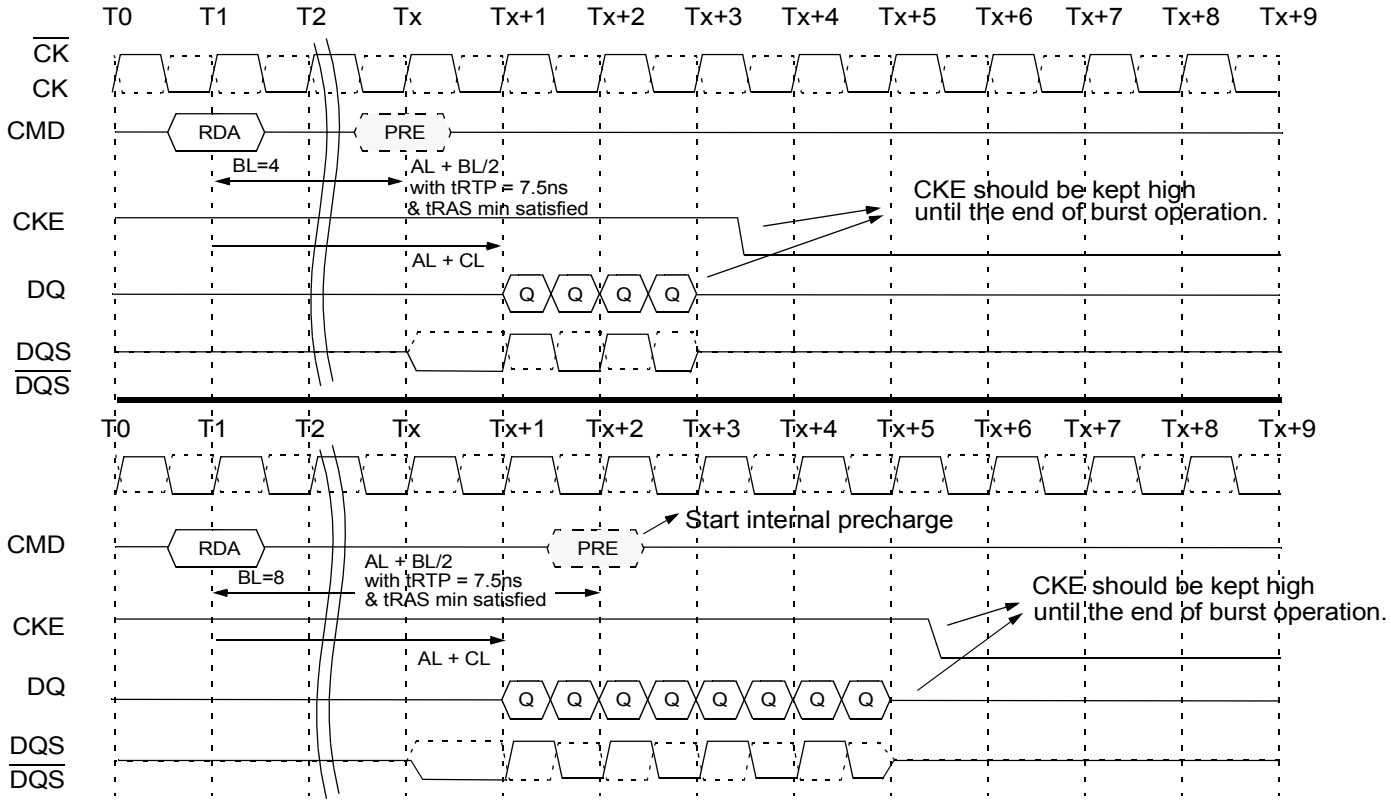


Figure 53 — Read with Autoprecharge to Power Down Entry

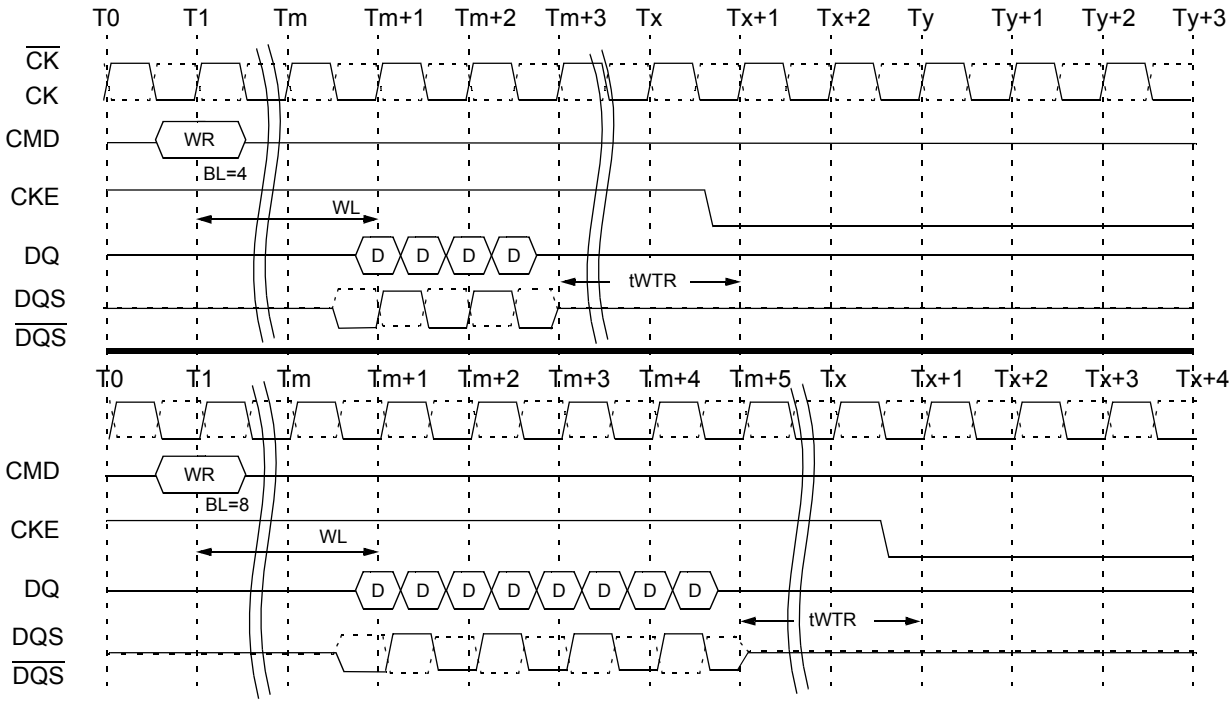


Figure 54 — Write to Power Down Entry

2.2.9 Power-Down (cont'd)

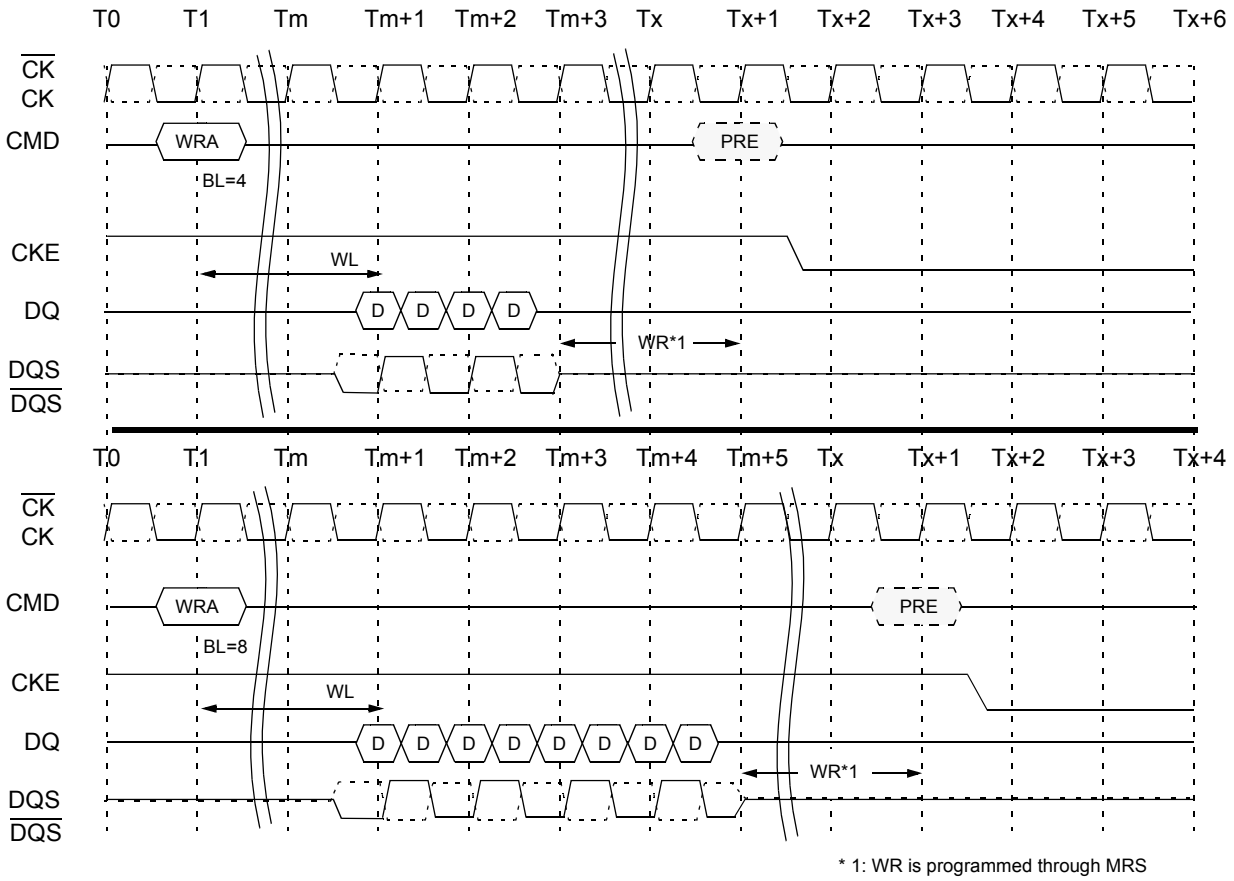


Figure 55 — Write with Autoprecharge to Power Down Entry

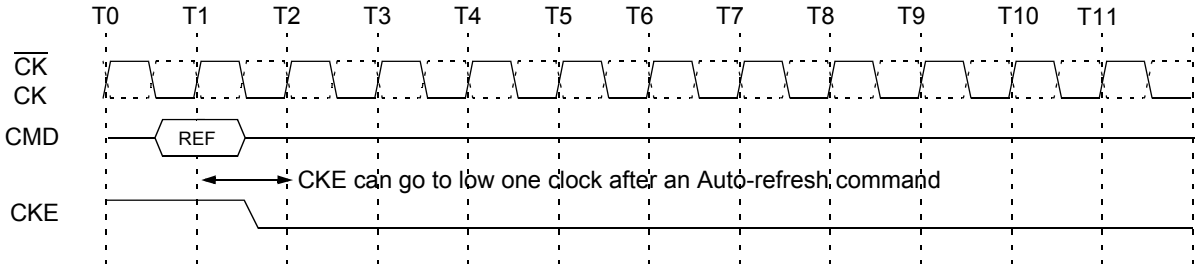


Figure 56 — Refresh Command to Power Down Entry

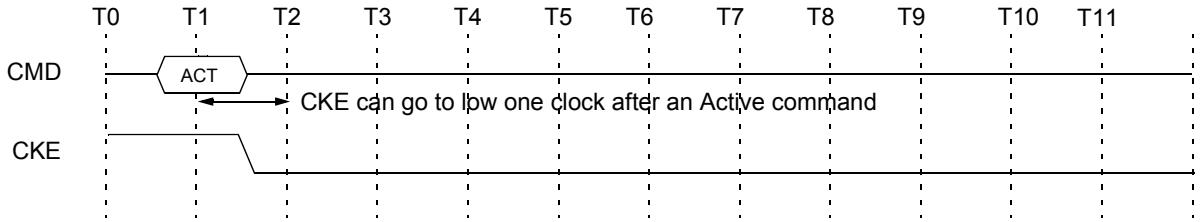


Figure 57 — Active Command to Power Down Entry

2.2.9 Power-Down (cont'd)

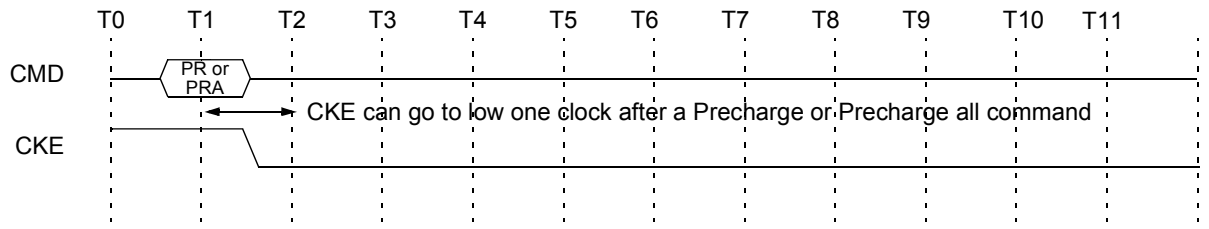


Figure 58 — Precharge/Precharge all Command to Power Down Entry

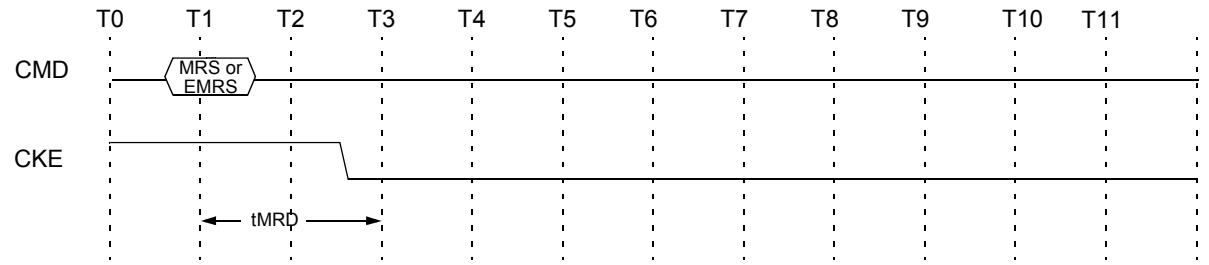


Figure 59 — MRS/EMRS Command to Power Down Entry

2.2.10 Asynchronous CKE Low Event

DRAM requires CKE to be maintained "HIGH" for all valid operations as defined in this data sheet. If CKE asynchronously drops "LOW" during any valid operation DRAM is not guaranteed to preserve the contents of array. If this event occurs, memory controller must satisfy DRAM timing specification tDelay before turning off the clocks. Stable clocks must exist at the input of DRAM before CKE is raised "HIGH" again. DRAM must be fully re-initialized (steps 4 thru 13) as described in initialization sequence. DRAM is ready for normal operation after the initialization sequence. See Table 35 for tDelay specification.

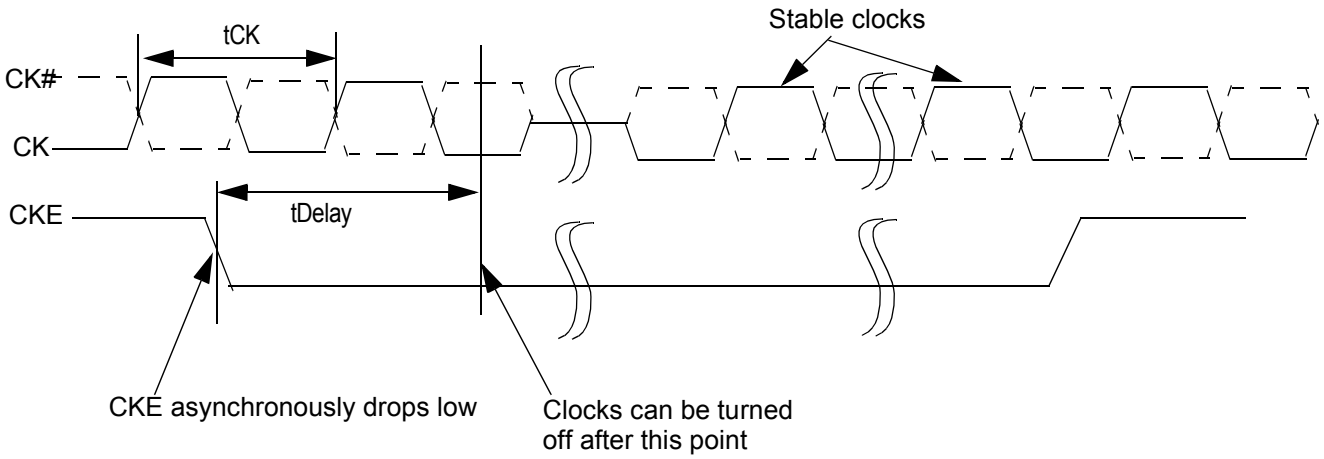


Figure 60 — Asynchronous CKE Low Event

2.2.11 Input Clock Frequency Change during Precharge Power Down

DDR2 SDRAM input clock frequency can be changed under following condition:

DDR2 SDRAM is in precharged power down mode. ODT must be turned off and CKE must be at logic LOW level. A minimum of 2 clocks must be waited after CKE goes LOW before clock frequency may change. SDRAM input clock frequency is allowed to change only within minimum and maximum operating frequency specified for the particular speed grade. During input clock frequency change, ODT and CKE must be held at stable LOW levels. Once input clock frequency is changed, stable new clocks must be provided to DRAM before precharge power down may be exited and DLL must be RESET via EMRS after precharge power down exit. Depending on new clock frequency an additional MRS command may need to be issued to appropriately set the WR, CL etc. During DLL re-lock period, ODT must remain off. After the DLL lock time, the DRAM is ready to operate with new clock frequency.

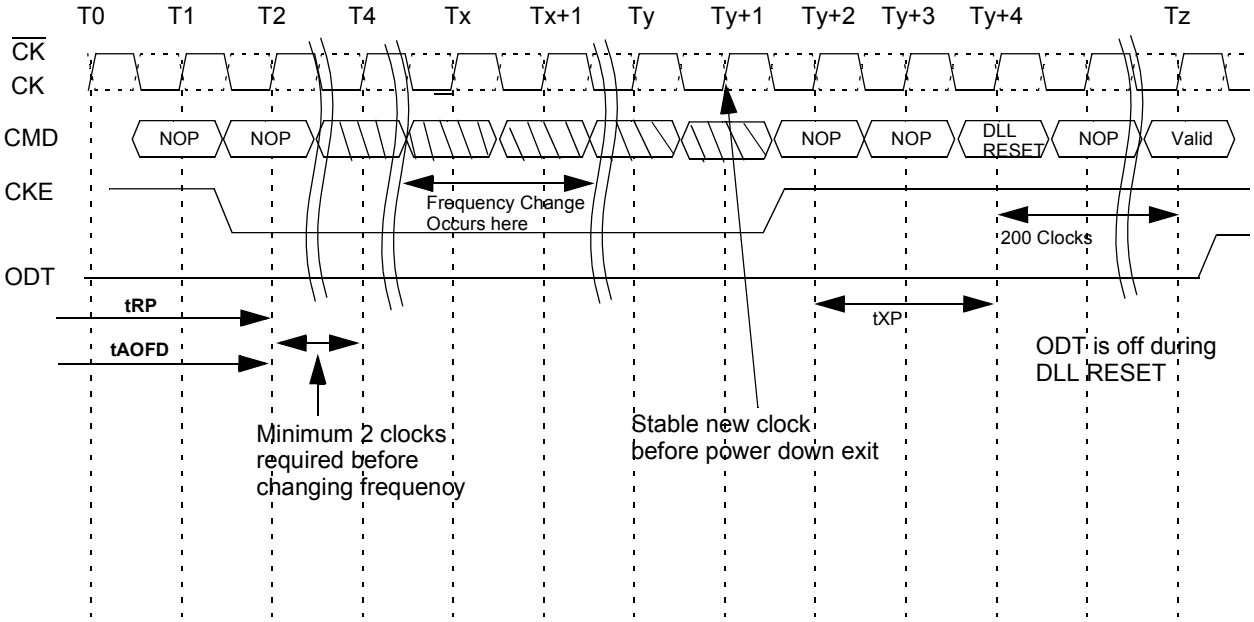


Figure 61 — Clock Frequency Change in Precharge Power

2.2.12 No Operation Command

The No Operation command should be used in cases when the DDR2 SDRAM is in an idle or a wait state. The purpose of the No Operation command (NOP) is to prevent the DDR2 SDRAM from registering any unwanted commands between operations. A No Operation command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ held high at the rising edge of the clock. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

2.2.13 Deselect Command

The Deselect command performs the same function as a No Operation command. Deselect command occurs when $\overline{CS}$ is brought high at the rising edge of the clock, the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals become don't cares.

3 Truth Tables

Table 10 — Command truth table.

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1,2
Refresh (REF)	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1,7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.

NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

NOTE 3 Burst reads or writes at BL=4 cannot be terminated or interrupted. See sections "Reads interrupted by a Read" and "Writes interrupted by a Write" in section 2.2.4 for details.

NOTE 4 The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined in section 2.2.7.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See section 2.2.2.4.

NOTE 6 “X” means “H or L (but a defined logic level)”.

NOTE 7 Self refresh exit is asynchronous.

3 Truth Tables (cont'd)

Table 11 — Clock Enable (CKE) Truth Table for Synchronous Transitions

Current State [2]	CKE		Command (N) [3]	Action (N) [3]	Notes
	Previous Cycle[1] (N-1)	Current Cycle[1] (N)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$		
Power Down	L	L	X	Maintain Power-Down	11, 13, 15
	L	H	DESELECT or NOP	Power Down Exit	4, 8, 11,13
Self Refresh	L	L	X	Maintain Self Refresh	11, 15
	L	H	DESELECT or NOP	Self Refresh Exit	4, 5,9
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	4,8,10,11,13
All Banks Idle	H	L	DESELECT or NOP	Precharge Power Down Entry	4, 8, 10,11,13
	H	L	REFRESH	Self Refresh Entry	6, 9, 11,13
	H	H	Refer to the Command Truth Table		7

NOTE 1 CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.

NOTE 2 Current state is the state of the DDR SDRAM immediately prior to clock edge N.

NOTE 3 COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N).

NOTE 4 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

NOTE 5 On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the t_{XSNR} period. Read commands may be issued only after t_{XSRD} (200 clocks) is satisfied.

NOTE 6 Self Refresh mode can only be entered from the All Banks Idle state.

NOTE 7 Must be a legal command as defined in the Command Truth Table.

NOTE 8 Valid commands for Power Down Entry and Exit are NOP and DESELECT only.

NOTE 9 Valid commands for Self Refresh Exit are NOP and DESELECT only.

NOTE 10 Power Down and Self Refresh can not be entered while Read or Write operations, (Extended) Mode Register Set operations or Precharge operations are in progress. See section 2.2.9 "Power Down" and 2.2.8 "Self Refresh Command" for a detailed list of restrictions.

NOTE 11 Minimum CKE high time is three clocks.; minimum CKE low time is three clocks.

NOTE 12 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See section 2.2.2.4.

NOTE 13 The Power Down does not perform any refresh operations. The duration of Power Down Mode is therefore limited by the refresh requirements outlined in section 2.2.7.

NOTE 14 CKE must be maintained high while the SDRAM is in OCD calibration mode.

NOTE 15 "X" means "don't care (including floating around VREF)" in Self Refresh and Power Down. However ODT must be driven high or low in Power Down if the ODT function is enabled (Bit A2 or A6 set to "1" in EMRS(1)).

Table 12 — DM Truth Table

Name (Functional)	DM	DQs	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

NOTE 1 Used to mask write data, provided coincident with the corresponding data

4 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 1.0 V ~ 2.3 V	V	1
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
VDDL	Voltage on VDDL pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1

NOTE 1 Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5 AC & DC Operating Conditions

Table 13 — Recommended DC Operating Conditions (SSTL_1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	4
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	4, 5
VDD	Supply Voltage	2.3	2.5	2.7	V	4, 6
VDDL	Supply Voltage for DLL	2.3	2.5	2.7	V	4, 5, 6
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	5, 6
VREF	Input Reference Voltage	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	mV	1.2
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04	V	3

NOTE 1 There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.

NOTE 2 The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically, the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.

NOTE 3 Peak to peak ac noise on VREF may not exceed +/-2% VREF (dc).

NOTE 4 VTT of transmitting device must track VREF of receiving device.

NOTE 5 DDR2 parts with 2.5 V Vdd may exist in the market, but devices with 1.8 V Vdd are expected to be the preferred mass production parts

NOTE 6 VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDDL tied together

NOTE 7 Note 5 does not apply when Vdd = 2.5 V nominal

5 AC & DC Operating Conditions (cont'd)

Table 14 — ODT DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
Rtt effective impedance value for EMRS(A6,A2)=0,1; 75 ohm	Rtt1(eff)	60	75	90	ohm	1
Rtt effective impedance value for EMRS(A6,A2)=1,0; 150 ohm	Rtt2(eff)	120	150	180	ohm	1
Deviation of VM with respect to VDDQ/2	delta VM	-3.75		+3.75	%	1

NOTE 1 Test condition for Rtt measurements

Measurement Definition for Rtt(eff): Apply V_{IH} (ac) and V_{IL} (ac) to test pin separately, then measure current I(V_{IH} (ac)) and I(V_{IL} (ac)) respectively. V_{IH} (ac), V_{IL} (ac), and VDDQ values defined in SSTL_18

$$\text{Rtt(eff)} = \frac{V_{IH}(ac) - V_{IL}(ac)}{I(V_{IH}(ac)) - I(V_{IL}(ac))}$$

Measurement Definition for VM: Measure voltage (VM) at test pin (midpoint) with no load.

$$\text{delta VM} = \left(\frac{2 \times Vm}{VDDQ} - 1\right) \times 100\%$$

Table 15 — Input DC Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH}(dc)	dc input logic high	VREF + 0.125	VDDQ + 0.3	V	
V_{IL}(dc)	dc input logic low	- 0.3	VREF - 0.125	V	

Table 16 — Input AC Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH} (ac)	ac input logic high	VREF + 0.250	-	V	
V_{IL} (ac)	ac input logic low	-	VREF - 0.250	V	

Table 17 — AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 * V_{DDQ}	V	1
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

NOTE 1 Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test.
NOTE 2 The input signal minimum slew rate is to be maintained over the range from $V_{IL(dc)}$ max to $V_{IH(ac)}$ min for rising edges and the range from $V_{IH(dc)}$ min to $V_{IL(ac)}$ max for falling edges as shown in the below figure.
NOTE 3 AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.

5 AC & DC Operating Conditions (cont'd)

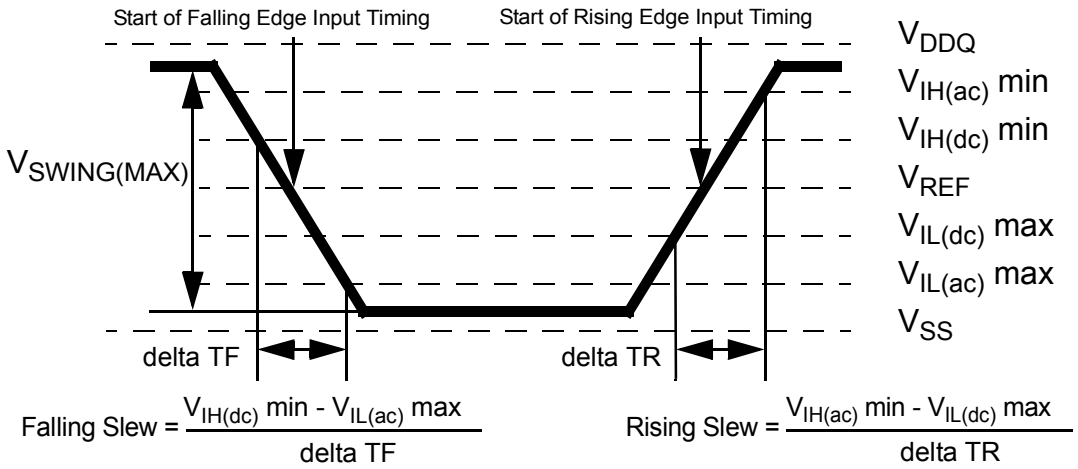


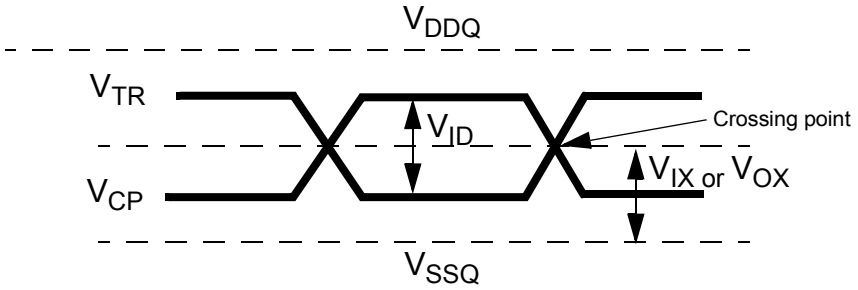
Figure 62 — AC Input Test Signal Waveform

Table 18 — Differential Input AC logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{ID} (ac)	ac differential input voltage	0.5	VDDQ + 0.6	V	1
V_{IX} (ac)	ac differential cross point voltage	0.5 * VDDQ - 0.175	0.5 * VDDQ + 0.175	V	2

NOTE 1 VIN(DC) specifies the allowable DC execution of each input of differential pair such as CK, $\overline{CK}$, DQS, $\overline{DQS}$, LDQS, $\overline{LDQS}$, UDQS and $\overline{UDQS}$.

NOTE 2 VID(DC) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input (such as CK, DQS, LDQS or UDQS) level and VCP is the complementary input (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$) level. The minimum value is equal to VIH(DC) - V IL(DC).



NOTE 1 VID(AC) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input signal (such as CK, DQS, LDQS or UDQS) and VCP is the complementary input signal (such as CK, DQS, LDQS or UDQS). The minimum value is equal to V IH(AC) - V IL(AC).

NOTE 2 The typical value of VIX(AC) is expected to be about 0.5 * VDDQ of the transmitting device and VIX(AC) is expected to track variations in VDDQ. VIX(AC) indicates the voltage at which differential input signals must cross.

Figure 63 — Differential signal levels

5 AC & DC Operating Conditions (cont'd)

Table 19 — Differential AC output parameters

Symbol	Parameter	Min.	Max.	Units	Notes
V_{OX} (ac)	ac differential cross point voltage	0.5 * VDDQ - 0.125	0.5 * VDDQ + 0.125	V	1

NOTE 1 The typical value of VOX(AC) is expected to be about 0.5 * V DDQ of the transmitting device and VOX(AC) is expected to track variations in VDDQ. VOX(AC) indicates the voltage at which differential output signals must cross.

Overshoot/Undershoot Specification

Table 20 — AC Overshoot/Undershoot Specification for Address and Control Pins A0-A15, BA0-BA2, CS, RAS, CAS, WE, CKE, ODT

Parameter	Specification		
	DDR2-400	DDR2-533	DDR2-667
Maximum peak amplitude allowed for overshoot area (See Figure 64):	0.9V	0.9V	0.9V
Maximum peak amplitude allowed for undershoot area (See Figure 64):	0.9V	0.9V	0.9V
Maximum overshoot area above VDD (See Figure 64).	0.75 V-ns	0.56 V-ns	0.45 V-ns
Maximum undershoot area below VSS (See Figure 64).	0.75 V-ns	0.56 V-ns	0.45 V-ns

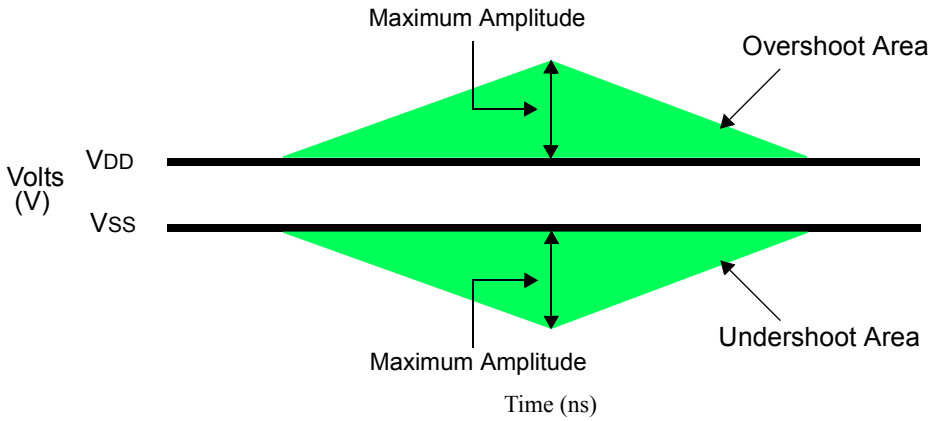


Figure 64 — AC Overshoot and Undershoot Definition for Address and Control Pins

Table 21 — AC Overshoot/Undershoot Specification for Clock, Data, Strobe, and Mask Pins DQ, DQS, DM, CK, CK

Parameter	Specification		
	DDR2-400	DDR2-533	DDR2-667
Maximum peak amplitude allowed for overshoot area (See Figure 65):	0.9V	0.9V	0.9V
Maximum peak amplitude allowed for undershoot area (See Figure 65):	0.9V	0.9V	0.9V
Maximum overshoot area above VDDQ (See Figure 65).	0.38 V-ns	0.28 V-ns	0.23 V-ns
Maximum undershoot area below VSSQ (See Figure 65).	0.38 V-ns	0.28 V-ns	0.23 V-ns

5 AC & DC Operating Conditions (cont'd)

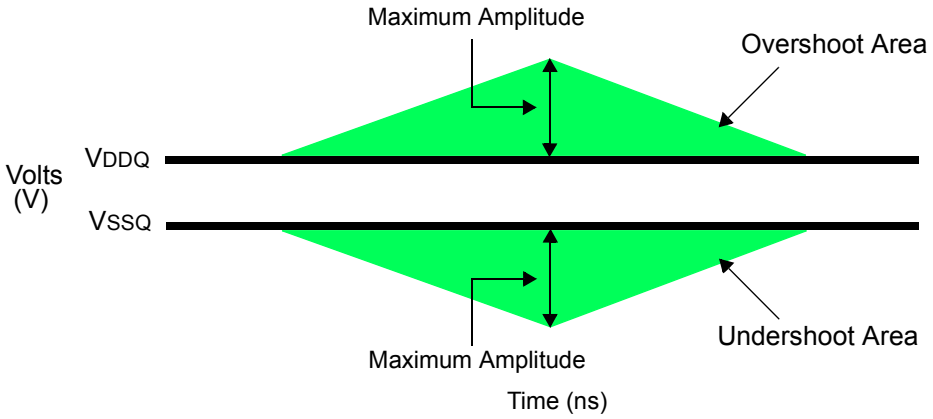


Figure 65 — AC Overshoot and Undershoot Definition for Clock, Data, Strobe, and Mask Pins

Power and ground clamps are required on the following input only pins:

1. BA0-BA2
2. A0-A15
3. $\overline{RAS}$
4. $\overline{CAS}$
5. $\overline{WE}$
6. $\overline{CS}$
7. ODT
8. CKE

Table 22 — Characteristics for Input Only Pins with Clamps

Voltage across clamp (V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0	0
0.1	0	0
0.2	0	0
0.3	0	0
0.4	0	0
0.5	0	0
0.6	0	0
0.7	0	0
0.8	0.1	0.1
0.9	1.0	1.0
1.0	2.5	2.5
1.1	4.7	4.7
1.2	6.8	6.8
1.3	9.1	9.1
1.4	11.0	11.0
1.5	13.5	13.5
1.6	16.0	16.0
1.7	18.2	18.2
1.8	21.0	21.0

5 AC & DC Operating Conditions (cont'd)

Output Buffer Levels

Table 23 — Output AC Test Conditions

Symbol	Parameter	SSTL_18 Class II	Units	Notes
V_{OH}	Minimum Required Output Pull-up under AC Test Load	V_{TT} + 0.603	V	
V_{OL}	Maximum Required Output Pull-down under AC Test Load	V_{TT} - 0.603	V	
V_{OTR}	Output Timing Measurement Reference Level	0.5 * V_{DDQ}	V	1

NOTE 1 The VDDQ of the device under test is referenced.

Table 24 — Output DC Current Drive

Symbol	Parameter	SSTI_18 Class II	Units	Notes
$I_{OH(dc)}$	Output Minimum Source DC Current	- 13.4	mA	1, 3, 4
$I_{OL(dc)}$	Output Minimum Sink DC Current	13.4	mA	2, 3, 4

NOTE 1 V_{DDQ} = 1.7 V; V_{OUT} = 1420 mV. (V_{OUT} - V_{DDQ})/I_{OH} must be less than 21 ohm for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280 mV.

NOTE 2 V_{DDQ} = 1.7 V; V_{OUT} = 280 mV. V_{OUT}/I_{OL} must be less than 21 ohm for values of V_{OUT} between 0 V and 280 mV.

NOTE 3 The dc value of V_{REF} applied to the receiving device is set to V_{TT}

NOTE 4 The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} min plus a noise margin and V_{IL} max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see Table 12) along a 21 ohm load line to define a convenient driver current for measurement.

Table 25 — OCD Default Characteristics

Description	Parameter	Min	Nom	Max	Unit	Notes
Output impedance		12.6	18	23.4	ohms	1,2
Pull-up and pull-down mismatch		0		4	ohms	1,2,3
Output slew rate		tbd		tbd	V/ns	1,4,5

NOTE 1 Absolute Specifications (0°C £ TCASE £ +tbd°C; VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V)

NOTE 2 Impedance measurement condition for output source dc current: VDDQ = 1.7V; VOUT = 1420mV; (VOUT-VDDQ)/Ioh must be less than 23.4 ohms for values of VOUT between VDDQ and VDDQ-280mV. Impedance measurement condition for output sink dc current: VDDQ = 1.7V; VOUT = 280mV; VOUT/Iol must be less than 23.4 ohms for values of VOUT between 0V and 280mV.

NOTE 3 Mismatch is absolute value between pull-up and pull-down, both are measured at same temperature and voltage.

NOTE 4 Slew rate measured from vil(ac) to vih(ac).

NOTE 5 The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.

5 AC & DC Operating Conditions (cont'd)

DDR2 SDRAM Default Output Driver V–I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength default operation as selected by the EMRS1 bits A7-A9 = '111'. Figures 66 and 67 show the driver characteristics graphically, while Tables 26 and 27 show the same data in tabular format suitable for input into simulation tools. The driver characteristics evaluation conditions are:

- Nominal Default 25 ^{o}C (T case), VDDQ = 1.8 V, typical process
- Minimum TBD ^{o}C (T case), VDDQ = 1.7 V, slow–slow process
- Maximum 0 ^{o}C (T case), VDDQ = 1.9 V, fast–fast process

Default Output Driver Characteristic Curves Notes:

1. The full variation in driver current from minimum to maximum process, temperature, and voltage will lie within the outer bounding lines of the V–I curve of the Figures.
2. It is recommended that the "typical" IBIS V–I curve lie within the inner bounding lines of the V–I curves of the Figures.

Table 26 — Full Strength Default Pulldown Driver Characteristics

	Pulldown Current (mA)			
Voltage (V)	Minimum (23.4 Ohms)	Nominal Default Low (18 ohms)	Nominal Default High (18 ohms)	Maximum (12.6 Ohms)
0.2	8.5	11.3	11.8	15.9
0.3	12.1	16.5	16.8	23.8
0.4	14.7	21.2	22.1	31.8
0.5	16.4	25.0	27.6	39.7
0.6	17.8	28.3	32.4	47.7
0.7	18.6	30.9	36.9	55.0
0.8	19.0	33.0	40.9	62.3
0.9	19.3	34.5	44.6	69.4
1.0	19.7	35.5	47.7	75.3
1.1	19.9	36.1	50.4	80.5
1.2	20.0	36.6	52.6	84.6
1.3	20.1	36.9	54.2	87.7
1.4	20.2	37.1	55.9	90.8
1.5	20.3	37.4	57.1	92.9
1.6	20.4	37.6	58.4	94.9
1.7	20.6	37.7	59.6	97.0
1.8		37.9	60.9	99.1
1.9				101.1

5 AC & DC Operating Conditions (cont'd)

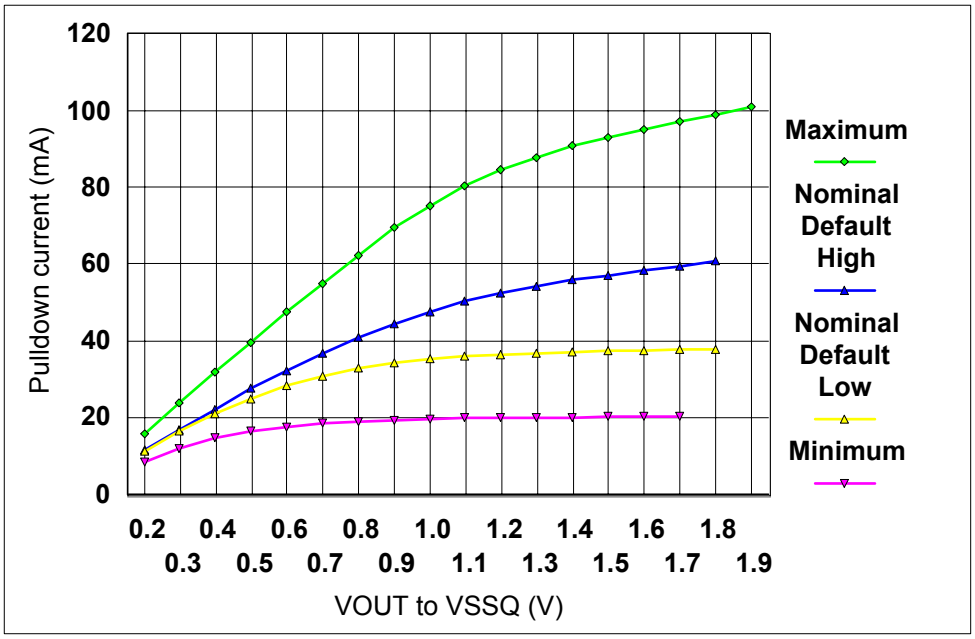


Figure 66 — DDR2 Default Pulldown Characteristics for Full Strength Driver

Table 27 — Full Strength Default Pullup Driver Characteristics

	Pullup Current (mA)			
Voltage (V)	Minimum (23.4 Ohms)	Nominal Default Low (18 ohms)	Nominal Default High (18 ohms)	Maximum (12.6 Ohms)
0.2	-8.5	-11.1	-11.8	-15.9
0.3	-12.1	-16.0	-17.0	-23.8
0.4	-14.7	-20.3	-22.2	-31.8
0.5	-16.4	-24.0	-27.5	-39.7
0.6	-17.8	-27.2	-32.4	-47.7
0.7	-18.6	-29.8	-36.9	-55.0
0.8	-19.0	-31.9	-40.8	-62.3
0.9	-19.3	-33.4	-44.5	-69.4
1.0	-19.7	-34.6	-47.7	-75.3
1.1	-19.9	-35.5	-50.4	-80.5
1.2	-20.0	-36.2	-52.5	-84.6
1.3	-20.1	-36.8	-54.2	-87.7
1.4	-20.2	-37.2	-55.9	-90.8
1.5	-20.3	-37.7	-57.1	-92.9
1.6	-20.4	-38.0	-58.4	-94.9
1.7	-20.6	-38.4	-59.6	-97.0
1.8		-38.6	-60.8	-99.1
1.9				-101.1

5 AC & DC Operating Conditions (cont'd)

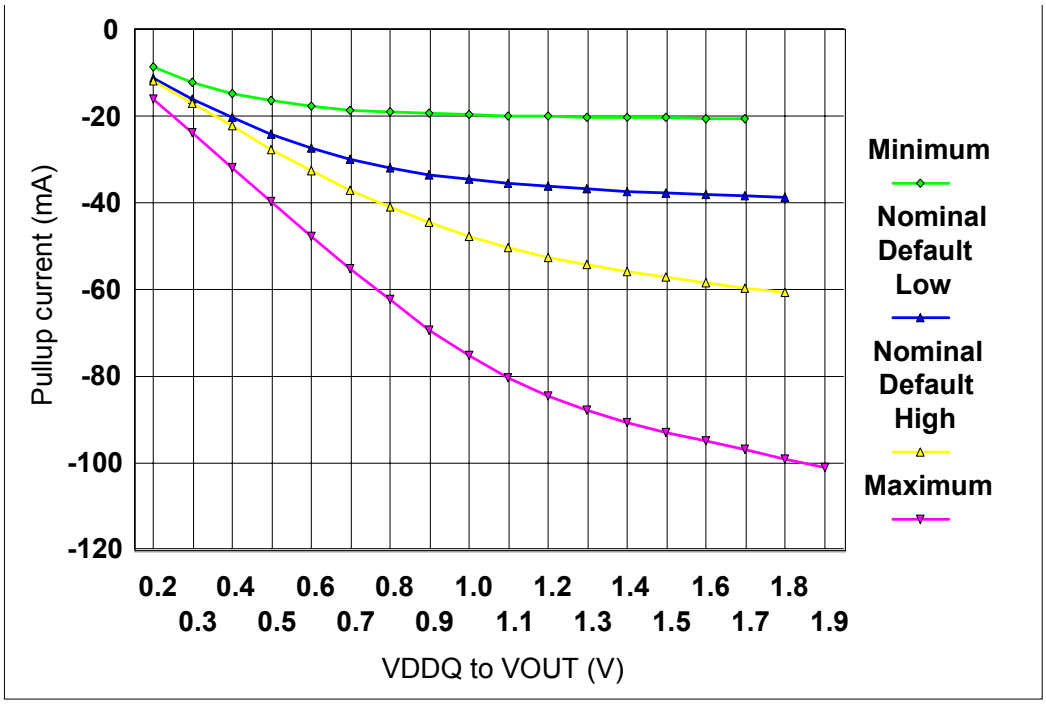


Figure 67 — DDR2 Default Pullup Characteristics for Full Strength Output Driver

DDR2 SDRAM Calibrated Output Driver V–I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength calibrated operation as selected by the procedure outlined in Section 2.2.2.3, Off-Chip Driver (OCD) Impedance Adjustment. Tables 28 and 29 show the data in tabular format suitable for input into simulation tools. The nominal points represent a device at exactly 18 ohms. The nominal low and nominal high values represent the range that can be achieved with a maximum 1.5 ohm step size with no calibration error at the exact nominal conditions only (i.e., perfect calibration procedure, 1.5 ohm maximum step size guaranteed by specification). Real system calibration error needs to be added to these values. It must be understood that these V-I curves as represented here or in supplier IBIS models need to be adjusted to a wider range as a result of any system calibration error. Since this is a system specific phenomena, it cannot be quantified here. The values in the calibrated tables represent just the DRAM portion of uncertainty while looking at one DQ only. If the calibration procedure is used, it is possible to cause the device to operate outside the bounds of the default device characteristics tables and figures. In such a situation, the timing parameters in the specification cannot be guaranteed. It is solely up to the system application to ensure that the device is calibrated between the minimum and maximum default values at all times. If this can't be guaranteed by the system calibration procedure, re-calibration policy, and uncertainty with DQ to DQ variation, then it is recommended that only the default values be used. The nominal maximum and minimum values represent the change in impedance from nominal low and high as a result of voltage and temperature change from the nominal condition to the maximum and minimum conditions. If calibrated at an extreme condition, the amount of variation could be as much as from the nominal minimum to the nominal maximum or vice versa. The driver characteristics evaluation conditions are:

- Nominal 25 ^{o}C (T case), VDDQ = 1.8 V, typical process
- Nominal Low and Nominal High 25 ^{o}C (T case), VDDQ = 1.8 V, any process
- Nominal Minimum TBD ^{o}C (T case), VDDQ = 1.7 V, any process
- Nominal Maximum 0 ^{o}C (T case), VDDQ = 1.9 V, any process

5 AC & DC Operating Conditions (cont'd)

Table 28 — Full Strength Calibrated Pulldown Driver Characteristics

	Calibrated Pulldow n Current (mA)				
Voltage (V)	Nominal Minimum (21 ohms)	Nominal Low (18.75 ohms)	Nominal (18 ohms)	Nominal High (17.25 ohms)	Nominal Maximum (1 ohms)
0.2	9.5	10.7	11.5	11.8	13.3
0.3	14.3	16.0	16.6	17.4	20.0
0.4	18.7	21.0	21.6	23.0	27.0

Table 29 — Full Strength Calibrated Pullup Driver Characteristics

	Calibrated Pullup Current (mA)				
Voltage (V)	Nominal Minimum (21 ohms)	Nominal Low (18.75 ohms)	Nominal (18 ohms)	Nominal High (17.25 ohms)	Nominal Maximum (1 ohms)
0.2	-9.5	-10.7	-11.4	-11.8	-13.3
0.3	-14.3	-16.0	-16.5	-17.4	-20.0
0.4	-18.7	-21.0	-21.2	-23.0	-27.0

Table 30 — IDD Specification Parameters and Test Conditions

(IDD values are for full operating range of Voltage and Temperature, Notes 1 - 5

Symbol	Conditions	Max	Units	Notes
IDD0	**Operating one bank active-precharge current;** $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD1	**Operating one bank active-read-precharge current;** IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC\ (IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$, $t_{RCD} = t_{RCD(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA	
IDD2P	**Precharge power-down current;** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA	
IDD2Q	**Precharge quiet standby current;** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA	

Table 30 — IDD Specification Parameters and Test Conditions
(IDD values are for full operating range of Voltage and Temperature, Notes 1 - 5

Symbol	Conditions		Max	Units	Notes
IDD2N	**Precharge standby current;** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING			mA	
IDD3P	**Active power-down current;** All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0		mA	
		Slow PDN Exit MRS(12) = 1		mA	
IDD3N	**Active standby current;** All banks open; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING			mA	
IDD4W	**Operating burst write current;** All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING			mA	
IDD4R	**Operating burst read current;** All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W			mA	
IDD5B	**Burst refresh current;** $t_{CK} = t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING			mA	
IDD6	**Self refresh current;** CK and $\overline{CK}$ at 0V; CKE £ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING			mA	
IDD7	**Operating bank interleave read current;** All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = $t_{RCD(IDD)}$-1*$t_{CK(IDD)}$; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RRD} = t_{RRD(IDD)}$, t_{RCD} = 1*$t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; - Refer to the following page for detailed timing conditions			mA	

Table 30 — IDD Specification Parameters and Test Conditions
(IDD values are for full operating range of Voltage and Temperature, Notes 1 - 5

NOTE 1 IDD specifications are tested after the device is properly initialized

NOTE 2 Input slew rate is specified by AC Parametric Test Condition

NOTE 3 IDD parameters are specified with ODT disabled.

NOTE 4 Data bus consists of DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, LDQS, $\overline{LDQS}$, UDQS, and $\overline{UDQS}$. IDD values must be met with all combinations of EMRS bits 10 and 11.

NOTE 5 Definitions for IDD

LOW	=	Vin £ VILAC(max)
HIGH	=	Vin Š VIHAC(min)
STABLE	=	inputs stable at a HIGH or LOW level
FLOATING	=	inputs at VREF = VDDQ/2
SWITCHING	=	inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

IDD Testing Parameters

For purposes of IDD testing, the following parameters are to be utilized.

Table 31 — IDD Testing Parameters

	DDR2-667	DDR2-533			DDR2-400		
Parameter	**4-4-4**	**3-3-3**	**4-4-4**	**5-5-5**	**3-3-3**	**4-4-4**	**Units**
CL(IDD)	4	3	4	5	3	4	tCK
$t_{RCD(IDD)}$	12	11.25	15	18.75	15	20	ns
$t_{RC(IDD)}$	57	56.25	60	63.75	60	65	ns
$t_{RRD(IDD)}$-x4/x8	7.5	7.5	7.5	7.5	7.5	7.5	ns
$t_{RRD(IDD)}$-x16	10	10	10	10	10	10	ns
$t_{CK(IDD)}$	3	3.75	3.75	3.75	5	5	ns
$t_{RASmin(IDD)}$	45	45	45	45	45	45	ns
$t_{RASmax(IDD)}$	70000	70000	70000	70000	70000	70000	ns
$t_{RP(IDD)}$	12	11.25	15	18.75	15	20	ns
$t_{RFC(IDD)}$-256Mb	75	75	75	75	75	75	ns
$t_{RFC(IDD)}$-512Mb	105	105	105	105	105	105	ns
$t_{RFC(IDD)}$-1Gb	127.5	127.5	127.5	127.5	127.5	127.5	ns
$t_{RFC(IDD)}$-2Gb	197.5	197.5	197.5	197.5	197.5	197.5	ns

5 AC & DC Operating Conditions (cont'd)

Detailed IDD7

The detailed timings are shown below for IDD7. Changes will be required if timing parameter changes are made to the specification.

Legend: A = Active; RA = Read with Autoprecharge; D = Deselect

IDD7: Operating Current: All Bank Interleave Read operation
All banks are being interleaved at minimum ^{t}RC(IDD) without violating ^{t}RRD(IDD) using a burst length of 4. Control and address bus inputs are STABLE during DESELECTs. IOUT = 0mA

Timing Patterns for 4 bank devices x4/ x8/ x16
-DDR2-400 4/4/4: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D D D

-DDR2-400 3/3/3: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D D

-DDR2-533 5/4/4: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D

-DDR2-533 4/4/4: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D

Timing Patterns for 8 bank devices x4/x8
-DDR2-400 and DDR2-533 all bins: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D A4 RA4 A5 RA5 A6 RA6 A7 RA7 D D

Timing Patterns for 8 bank devices x16
-DDR2-400 all bins: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D A4 RA4 A5 RA5 A6 RA6 A7 RA7 D D

-DDR2-533 all bins: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D D

Table 32 — Input/Output capacitance

Parameter	Symbol	Min	Max	Units
Input capacitance, CK and $\overline{CK}$	CCK	1.5	2.5	pF
Input capacitance delta, CK and $\overline{CK}$	CDCK	x	0.25	pF
Input capacitance, all other input-only pins	CI	1.5	2.5	pF
Input capacitance delta, all other input-only pins	CDI	x	0.25	pF
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	3.0	4.0	pF
Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	CDIO	x	0.5	pF

Electrical Characteristics & AC Timing for DDR2-400/533/667 - Absolute Specification

(0 °C ≤ T_{CASE} ≤ xx °C; V_{DDQ} = 1.8V +/– 0.1V; V_{DD} = 1.8V +/– 0.1V)

Table 33 — Refresh Parameters by Device Density

Parameter	Symbol	256Mb	512Mb	1Gb	2Gb	4Gb	Units
Refresh to active/Refresh command time	tRFC	75	105	127.5	195	tbd	ns
Average periodic refresh interval	tREFI	7.8	7.8	7.8	7.8	7.8	µs

5 AC & DC Operating Conditions (cont'd)

Table 34 — DDR2 SDRAM Standard Speed Bins and tRCD, tRP and tRC for Corresponding Bin

Speed	DDR2-667	DDR2-533	DDR2-533	DDR2-533	DDR2-400	DDR2-400	Units
Bin (CL - tRCD - tRP)	4 - 4 - 4	3 - 3 - 3	4 - 4 - 4	5 - 5 - 5	3 - 3 - 3	4 - 4 - 4	
Parameter	min	min	min	min	min	min	
$\overline{CAS}$ Latency	4	3	4	5	3	4	tCK
tRCD	12	11.25	15	18.75	15	20	ns
tRP Note1	12	11.25	15	18.75	15	20	ns
tRC	57	56.25	60	63.75	60	65	ns

NOTE 1 8 bank device Precharge All Allowance: tRP for a Precharge All command for an 8 Bank device will be equal to tRP + 1 * tCK, where tRP are the values for a single bank pre-charge, which are shown in the above table.

Table 35 — Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)
(Refer to notes for information related to this table at the bottom)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Notes
		min	max	min	max		
DQ output access time from CK/$\overline{CK}$	tAC	-600	+600	-500	+500	ps	
DQS output access time from CK/$\overline{CK}$	tDQSCK	-500	+500	-450	+450	ps	
CK high-level width	tCH	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min(tCL,tCH)	x	min(tCL,tCH)	x	ps	11,12
Clock cycle time, CL=x	tCK	5000	8000	3750	8000	ps	15
DQ and DM input hold time	tDH	400	x	350	x	ps	6,7,8
DQ and DM input setup time	tDS	400	x	350	x	ps	6,7,8
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	tCK	
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	x	tAC max	ps	
Data-out low-impedance time from CK/$\overline{CK}$	tLZ	tAC min	tAC max	tAC min	tAC max	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	350	x	300	ps	13
DQ hold skew factor	tQHS	x	450	x	400	ps	12

Table 35 — Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)
(Refer to notes for information related to this table at the bottom)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Notes
		min	max	min	max		
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	ps	
Write command to first DQS latching transition	tDQSS	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	tCK	
DQS input high pulse width	tDQSH	0.35	x	0.35	x	tCK	
DQS input low pulse width	tDQSL	0.35	x	0.35	x	tCK	
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	tCK	
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK	
Mode register set command cycle time	tMRD	2	x	2	x	tCK	
Write preamble setup time	tWPRES	0	x	0	x	ps	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	10
Write preamble	tWPRE	0.25	x	0.25	x	tCK	
Address and control input hold time	tIH	600	x	500	x	ps	5,7,9
Address and control input setup time	tIS	600	x	500	x	ps	5,7,9
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	
Active to precharge command	tRAS	45	70000	45	70000	ns	3
Active to active command period for 1KB page size products	tRRD	7.5	x	7.5	x	ns	4
Active to active command period for 2KB page size products	tRRD	10	x	10	x	ns	4
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2		2		tCK	
Write recovery time	tWR	15	x	15	x	ns	
Auto precharge write recovery + precharge time	tDAL	tWR+tRP*	x	tWR+tRP*	x	tCK	14
Internal write to read command delay	tWTR	10	x	7.5	x	ns	
Internal read to precharge command delay	tRTP	7.5		7.5		ns	3
Exit self refresh to a non-read command	tXSNR	tRFC + 10		tRFC + 10		ns	

Table 35 — Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)
(Refer to notes for information related to this table at the bottom)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Notes
		min	max	min	max		
Exit self refresh to a read command	tXSRD	200		200		tCK	
Exit precharge power down to any non-read command	tXP	2	x	2	x	tCK	
Exit active power down to read command	tXARD	2	x	2	x	tCK	1
Exit active power down to read command (Slow exit, Lower power)	tXARDS	6 - AL		6 - AL		tCK	1, 2
CKE minimum pulse width (high and low pulse width)	t_{CKE}	3		3		tCK	
ODT turn-on delay	t_{AOND}	2	2	2	2	tCK	
ODT turn-on	t_{AON}	tAC(min)	tAC(max)+1	tAC(min)	tAC(max) +1	ns	16
ODT turn-on (Power-Down mode)	t_{AONPD}	tAC(min)+2	2tCK+tAC(max)+1	tAC(min)+2	2tCK+tAC (max)+1	ns	
ODT turn-off delay	t_{AOFD}	2.5	2.5	2.5	2.5	tCK	
ODT turn-off	t_{AOF}	tAC(min)	tAC(max)+ 0.6	tAC(min)	tAC(max) + 0.6	ns	17
ODT turn-off (Power-Down mode)	t_{AOFPD}	tAC(min)+2	2.5tCK+tAC(max)+1	tAC(min)+2	2.5tCK+tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3		3		tCK	
ODT power down exit latency	tAXPD	8		8		tCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		tIS+tCK+tIH		ns	15

5 AC & DC Operating Conditions (cont'd)

Table 36 — Timing Parameters by Speed Grade (DDR2-667 and DDR2-SS800)

(Refer to notes for information related to this table at the bottom)

Parameter	Symbol	DDR2-667		DDR2-SS800		Units	Notes
		min	max	min	max		
DQ output access time from CK/$\overline{CK}$	tAC					ps	
DQS output access time from CK/$\overline{CK}$	tDQSCK					ps	
CK high-level width	tCH	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min(tCL,tCH)	x	min(tCL,tCH)	x	ps	11,12
Clock cycle time, CL=x	tCK	3000	8000	2500		ps	15
DQ and DM input hold time	tDH		x		x	ps	6,7
DQ and DM input setup time	tDS		x		x	ps	6,7
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	tCK	
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	x	tAC max	ps	
Data-out low-impedance time from CK/$\overline{CK}$	tLZ	tAC min	tAC max	tAC min	tAC max	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x		x		ps	13
DQ hold skew factor	tQHS	x		x	400	ps	12
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	ps	
Write command to first DQS latching transition	tDQSS	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	tCK	
DQS input high pulse width	tDQSH	0.35	x	0.35	x	tCK	
DQS input low pulse width	tDQSL	0.35	x	0.35	x	tCK	
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	tCK	
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK	
Mode register set command cycle time	tMRD	2	x	2	x	tCK	
Write preamble setup time	tWPRES	0	x	0	x	ps	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	10
Write preamble	tWPRE	0.25	x	0.25	x	tCK	
Address and control input hold time	tIH		x		x	ps	5,7,9
Address and control input setup time	tIS		x		x	ps	5,7,9

Table 36 — Timing Parameters by Speed Grade (DDR2-667 and DDR2-SS800)
(Refer to notes for information related to this table at the bottom)

Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	
Activate to precharge command	tRAS	45	70000		70000	ns	3
Activate to activate command period for 1KB page size products	tRRD	7.5	x	7.5	x	ns	4
Activate to activate command period for 2KB page size products	tRRD	10	x	10	x	ns	4
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2		2		tCK	
Write recovery time	tWR	15	x	15	x	ns	
Auto precharge write recovery + precharge time	tDAL	tWR+tRP*	x	tWR+tRP*	x	tCK	14
Internal write to read command delay	tWTR	7.5	x	7.5		ns	
Internal read to precharge command delay	tRTP	7.5		7.5		ns	3
Exit self refresh to a non-read command	tXSNR	tRFC + 10		tRFC + 10		ns	
Exit self refreh to a read command	tXSRD	200		200		tCK	
Exit precharge power down to any command	tXP	2	x	2	x	tCK	
Exit active power down to read command	tXARD	2	x	2	x	tCK	1
Exit active power down to read command (Slow exit, Lower power)	tXARDS	6 - AL		TBD		tCK	1, 2
CKE minimum pulse width (high and low pulse width)	tCKE	3		3		tCK	
ODT turn-on delay	t_{AOND}	2	2	2	2	tCK	
ODT turn-on	t_{AON}	tAC(min)	tAC(max)+1	tAC(min)	tAC(max)+1	ns	16
ODT turn-on (Power-Down mode)	t_{AONPD}	tAC(min)+2	2tCK+tAC (max)+1	tAC(min)+2	2tCK+tAC (max)+1	ns	
ODT turn-off delay	t_{AOFD}	2.5	2.5	2.5	2.5	tCK	
ODT turn-off	t_{AOF}	tAC(min)	tAC(max)+ 0.6	tAC(min)	tAC(max)+ 0.6	ns	17
ODT turn-off (Power-Down mode)	t_{AOFPD}	tAC(min)+2	2.5tCK+tAC (max)+1	tAC(min)+2	2.5tCK+tA C(max)+1	ns	
ODT to power down entry latency	tANPD	3		3		tCK	
ODT Power Down Exit Latency	tAXPD	8		8		tCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	

Table 36 — Timing Parameters by Speed Grade (DDR2-667 and DDR2-SS800)
(Refer to notes for information related to this table at the bottom)

Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		tIS+tCK+tIH		ns	15

General Notes, Which May Apply for all AC Parameters

NOTE 1 Slew Rate Measurement Levels

a) Output slew rate for falling and rising edges is measured between VTT - 250 mV & VTT + 250 mV for single ended signals. For differential signals (e.g., DQS - $\overline{DQS}$) output slew rate is measured between DQS - $\overline{DQS}$ = -500 mV and DQS - $\overline{DQS}$ = +500mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

b) Input slew rate for single ended signals is measured from dc-level to ac-level: from VREF - 125 mV to VREF + 250 mV for rising edges and from VREF + 125 mV and VREF - 250 mV for falling edges. For differential signals (e.g., CK - $\overline{CK}$) slew rate for rising edges is measured from CK - $\overline{CK}$ = -250 mV to CK - $\overline{CK}$ = +500 mV (250mV to -500 mV for falling edges).

c) VID is the magnitude of the difference between the input voltage on CK and the input voltage on $\overline{CK}$, or between DQS and $\overline{DQS}$ for differential strobe.

NOTE 2 DDR2 SDRAM AC timing reference load. Figure 68 represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

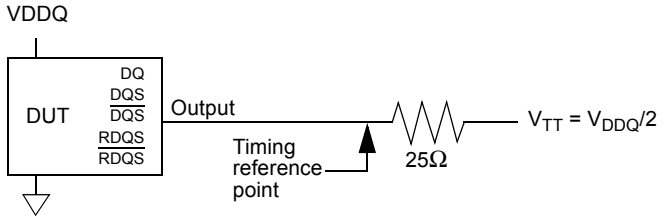


Figure 68 — AC Timing Reference Load

The output timing reference voltage level for single ended signals is the crosspoint with VTT. The output timing reference voltage level for differential signals is the crosspoint of the true (e.g., DQS) and the complement (e.g., DQS) signal.

NOTE 3 DDR2 SDRAM output slew rate test load. Output slew rate is characterized under the test conditions as shown in Figure 69.

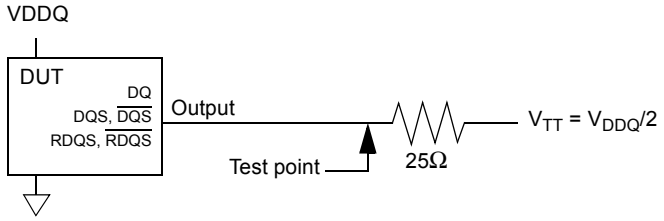


Figure 69 — Slew Rate Test Load

NOTE 4 Differential data strobe. DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. When differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 Ω to 10K Ω resistor to insure proper operation.

5 AC & DC Operating Conditions (cont'd)

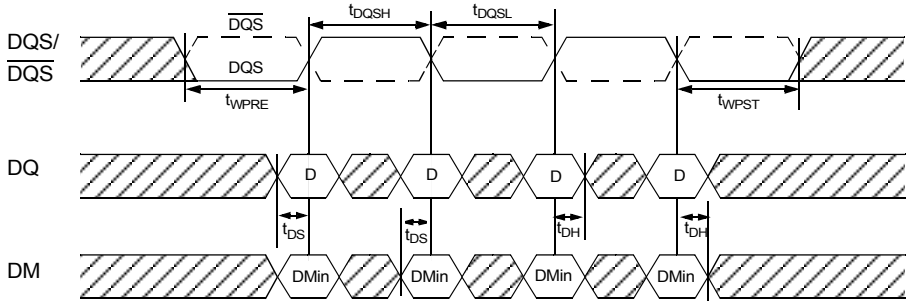


Figure 70 — Data Input (Write) Timing

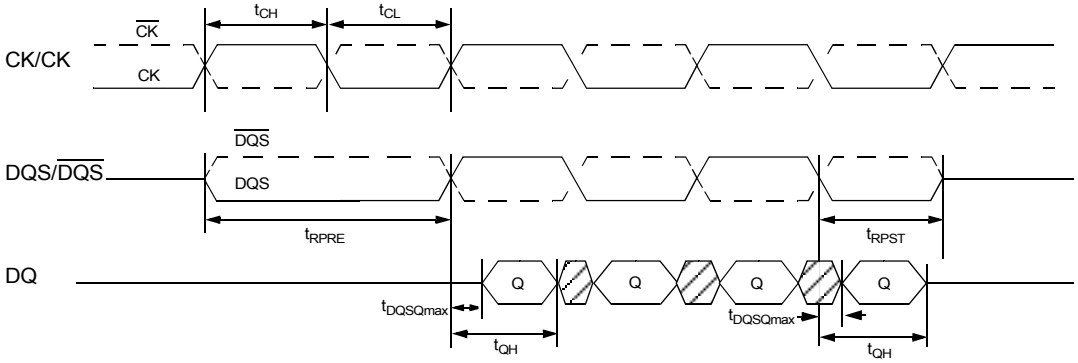


Figure 71 — Data Output (Read) Timing

NOTE 5 AC timings are for linear signal transitions. See System Derating for other signal transitions.

NOTE 6 These parameters guarantee device behavior, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.

NOTE 7 All voltages referenced to VSS.

NOTE 8 Tests for AC timing, IDD, and electrical (AC and DC) characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

Specific Notes for Dedicated AC Parameters

NOTE 1 User can choose which active power down exit timing to use via MRS(bit 12). tXARD is expected to be used for fast active power down exit timing. tXARDS is expected to be used for slow active power down exit timing where a lower power value is defined by each vendor data sheet.

NOTE 2 AL = Additive Latency

NOTE 3 This is a minimum requirement. Minimum read to precharge timing is AL + BL/2 providing the tRTP and tRAS(min) have been satisfied.

NOTE 4 A minimum of two clocks (2 * tCK) is required irrespective of operating frequency

NOTE 5 Timings are guaranteed with command/address input slew rate of 1.0 V/ns. See System Derating for other slew rate values.

NOTE 6 Timings are guaranteed with data, mask, and (DQS/RDQS in singled ended mode) input slew rate of 1.0 V/ns. See System Derating for other slew rate values.

NOTE 7 Timings are guaranteed with CK/$\overline{CK}$ differential slew rate of 2.0 V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0 V/ns in differential strobe mode and a slew rate of 1V/ns in single ended mode. See System Derating for other slew rate values.

Specific Notes for Dedicated AC Parameters Cont'd)

NOTE 8 tDS and tDH (data setup and hold) derating: TBD

NOTE 9 tIS and tIH (input setup and hold) derating: TBD

NOTE 10 The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

NOTE 11 MIN (t CL, t CH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t CL and t CH). For example, t CL and t CH are = 50% of the period, less the half period jitter (t JIT(HP)) of the clock source, and less the half period jitter due to crosstalk (t JIT(crosstalk)) into the clock traces.

NOTE 12 t QH = t HP – t QHS, where:
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL).

tQHS accounts for:

a. The pulse duration distortion of on-chip clock circuits; and

b. The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

NOTE 13 tDQSQ: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.

NOTE 14 t DAL = (nWR) + (tRP/tCK): For each of the terms above, if not already an integer, round to the next highest integer. tCK refers to the application clock period. nWR refers to the t WR parameter stored in the MRS.

Example: For DDR533 at t CK = 3.75 ns with t WR programmed to 4 clocks. tDAL = 4 + (15 ns / 3.75 ns) clocks = 4 +(4)clocks=8clocks.

NOTE 15 The clock frequency is allowed to change during self–refresh mode or precharge power-down mode. In case of clock frequency change during precharge power-down, a specific procedure is required as described in Section 2.2.9.

NOTE 16 ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND.

NOTE 17 ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD.

Annex A (informative) Revision Log

Rev	Contents of Modification
02/06/2003	JESD79-2 revision 0.9 for committee ballot for March 2003 committee meeting. If pass committee ballot, it will be announced as JESD79-2 Rev1.0 (DDR2 SDRAM Data Sheet Revision 1.0)
03/26/2003	Draft version of JESD79-2 has been finished with following changes made after March 2003 committee meeting. 1. Type corrections and editorial changes based on comments on committee ballot material 2. Updated power up and initialization sequence: committee ballot passed at March 2003 meeting 3. Added “Asynchronous CKE low event & Clock frequency change procedure” in section 2.2.9: committee ballot passed at March 2003 meeting 4. Added overshoot/Undershoot specification: committee ballot passed at March 2003 meeting 5. Added Full Strength Driver I/C curve: committee ballot passed at March 2003 meeting 6. Removed derating table: derating table is still under discussion
09/04/2003	Source file edited and formatted.

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