I, Julie Carlson, declare as follows:

1. I have personal knowledge of the facts set forth herein, and if called to testify, I could and would competently testify to the same.

2. I have been involved in semiconductor standardization and publication services for over twenty years. For nearly all of this time, I have worked at JEDEC, a standards-setting organization for the microelectronics industry, to edit, publish, and maintain JEDEC business records and standards developed by its numerous committees and subcommittees.

3. I have been involved with the standardization and publication activities of JEDEC continuously since 1997. I was the Manager of Standards and Publications at JEDEC from February 1997 through June 2005. Since June 2005, I have continued to work for JEDEC as a Consultant where my responsibilities include the maintenance and publication of JEDEC documents and standards. In addition, I am familiar with JEDEC's historical record-keeping and publication practices since at least 1992, based on my review of JEDEC's business records since that time and my regular discussions with JEDEC employees and members.

4. For over 50 years, JEDEC has been the global leader in developing and publishing open standards for the microelectronics industry. JEDEC's membership consists of more than 3,000 volunteers representing nearly 300

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member companies, and includes key technical individuals from most device, assembly, system and testing companies. JEDEC publications and standards are adopted worldwide. JEDEC is accredited by ANSI and maintains liaisons with numerous standards bodies throughout the world.

5. Since at least 2000, JEDEC standards have been publicly available for download from the JEDEC website (https://www.jedec.org), where they are cataloged and indexed by keyword and technological subject matter. By 2000, the JEDEC website was publicly available and commonly used by manufactures, companies in the microelectronics industry, and other interested parties to access and obtain standards information pertaining to that industry. Anyone interested can join JEDEC online, at JEDEC.org.

6. This declaration concerns JEDEC STANDARD, DDR2 SDRAM Specification, JESD79-2 (September 2003) (hereinafter, "JESD79-2 Standard"), which is a standard published by JEDEC. I have reviewed the JESD79-2 Standard. The copy of the JESD79-2 Standard attached to this declaration as Exhibit A is identical to the copy of the JESD79-2 Standard in JEDEC's files.

7. The following statements on the public availability of the JESD79-2 Standard as of September 2003 are based on personal knowledge. The development of all JEDEC documents follows the process set forth in JM21: JEDEC Manual of Organization and Procedure. According to that process, the

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date on the cover of a JEDEC document is the month the document was finalized, approved by legal, and posted to the website. For the JESD79-2 Standard, the date on the cover (and thus the date it was posted to JEDEC's website) is September 2003.

8. I am familiar with the circulation and publication procedures used by JEDEC. Upon approval of the Board of Directors, the JEDEC publications department prepares documents for publication, and seeks final review and approval to publish from the JEDEC legal department. Once legal approval is received, the JEDEC publications department uploads the approved document to the JEDEC website with a brief description. An email announcement is then sent to the sponsoring committee and any approved resellers. By 2000, JEDEC made its published standards available for download from www.jedec.org, as mentioned above.

9. Based on my personal knowledge of JEDEC's policies, the JESD79-2 Standard was made publicly available in September 2003 for download from the JEDEC website (https://www.jedec.org), consistent with the date on the cover page of the JESD79-2 Standard. My knowledge of the procedures surrounding the creation of the date notation and publication is based on JEDEC's policies and practices as I understand them through my work at JEDEC. I rely on these policies and practices in the course of my work. I have no reason to believe that JEDEC's

typical practice was not followed. I have no reason to believe that the JESD79-2 Standard was not made publicly accessible in September 2003.

10. To further confirm my statements above, I have visited the Internet Archive to look at the first capture of the online catalog at www.jedec.org after September 2003, which occurred on November 22, 2003: <http://web.archive.org/web/20031122085652/http://www.jedec.org:80/Catalog/display.cfm>. A printout of this capture is attached as Exhibit B and is consistent with my personal recollection of the JEDEC website. As can be seen from this capture on November 22, 2003, the JESD79-2 Standard was cataloged, indexed under the "RAM Memories" technical subject matter and under the keywords "SDRAM" and "DDR2," and was available to the public by that date, consistent with my statements above. *See* Exhibit B at pages 21, 46, 50, 64.

11. Exhibit C is a printout of <http://web.archive.org/web/20031001181456/http://jedec.org/service_members/New_Members/memberco.cfm>, which is a capture on October 1, 2003, of the list of member companies on JEDEC's website as of that date, which is consistent with my personal recollection of JEDEC's membership. All of those member companies would have had access to the JESD79-2 Standard attached as Exhibit A no later than that date.

I, Julie Carlson, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on 2021/09/16 Julie D. Carlson

Julie D. Carlson

Exhibit A

JEDEC STANDARD

DDR2 SDRAM SPECIFICATION

JESD79-2

SEPTEMBER 2003

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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DDR2 SDRAM SPECIFICATION

1 Package Pinout & Addressing

1.1 DDR2 SDRAM Package Ballout

(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
										D
A	VDD	NC	VSS				VSSQ	$\overline{DQS}$	VDDQ	E
B	NC	VSSQ	DM				DQS	VSSQ	NC	F
C	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
D	NC	VSSQ	DQ3				DQ2	VSSQ	NC	H
E	VDDL	VREF	VSS				VSSDL	CK	VDD	J
F		CKE	$\overline{WE}$				$\overline{RAS}$	$\overline{CK}$	ODT	K
G	NC, BA2	BA0	BA1				$\overline{CAS}$	$\overline{CS}$		L
H		A10/AP	A1				A2	A0	VDD	M
J	VSS	A3	A5				A6	A4		N
K		A7	A9				A11	A8	VSS	P
L	VDD	A12	NC, A14				NC, A15	NC, A13		R
										T
										U
										V
	NC	NC						NC	NC	W

Variation DJ-z without support balls

Variation DM-z with support balls

Variation DJ-z (x4 x8)

	1	2	3	4	5	6	7	8	9
A	O	O	O	+	+	+	O	O	O
B	O	O	O	+	+	+	O	O	O
C	O	O	O	+	+	+	O	O	O
D	O	O	O	+	+	+	O	O	O
E	O	O	O	+	+	+	O	O	O
F	+	O	O	+	+	+	O	O	O
G	O	O	O	+	+	+	O	O	+
H	+	O	O	+	+	+	O	O	O
J	O	O	O	+	+	+	O	O	+
K	+	O	O	+	+	+	O	O	O
L	O	O	O	+	+	+	O	O	+

Variation DM-z (x4/x8) with support balls

	1	2	3	4	5	6	7	8	9
A	O	O	+	+	+	+	+	O	O
B	+	+	+	+	+	+	+	+	+
C	+	+	+	+	+	+	+	+	+
D	+	+	+	+	+	+	+	+	+
E	O	O	O	+	+	+	O	O	O
F	O	O	O	+	+	+	O	O	O
G	O	O	O	+	+	+	O	O	O
H	O	O	O	+	+	+	O	O	O
J	O	O	O	+	+	+	O	O	O
K	+	O	O	+	+	+	O	O	O
L	O	O	O	+	+	+	O	O	+
M	+	O	O	+	+	+	O	O	O
N	O	O	O	+	+	+	O	O	+
P	+	O	O	+	+	+	O	O	O
R	O	O	O	+	+	+	O	O	+
T	+	+	+	+	+	+	+	+	+
U	+	+	+	+	+	+	+	+	+
V	+	+	+	+	+	+	+	+	+
W	O	O	+	+	+	+	+	O	O

O Populated ball
+ Ball not populated

Figure 1 — DDR2 SDRAM x4 Ballout Using MO-207

1 Package Pinout & Addressing (cont'd)

1.1 DDR2 SDRAM Package Ballout (cont'd)

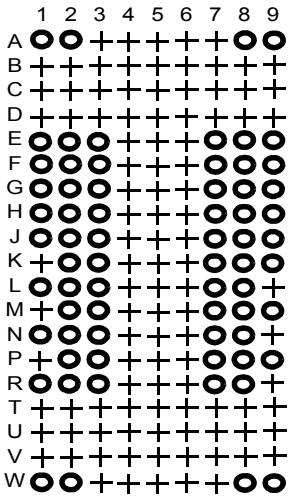
(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
										D
A	VDD	NU/$\overline{\text{RDQS}}$	VSS				VSSQ	$\overline{\text{DQS}}$	VDDQ	E
B	DQ6	VSSQ	DM/RDQS				DQS	VSSQ	DQ7	F
C	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
D	DQ4	VSSQ	DQ3				DQ2	VSSQ	DQ5	H
E	VDDL	VREF	VSS				VSSDL	CK	VDD	J
F		CKE	$\overline{\text{WE}}$				$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT	K
G	NC, BA2	BA0	BA1				$\overline{\text{CAS}}$	$\overline{\text{CS}}$		L
H		A10/AP	A1				A2	A0	VDD	M
J	VSS	A3	A5				A6	A4		N
K		A7	A9				A11	A8	VSS	P
L	VDD	A12	NC, A14				NC, A15	NC, A13		R
										T
										U
										V
	NC	NC						NC	NC	W

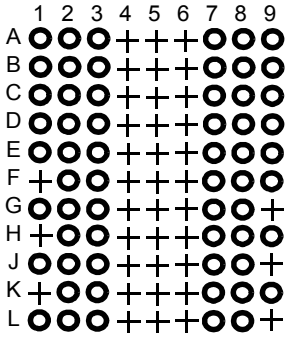
Variation DJ-z without support balls

Variation DM-z with support balls

Variation DM-z (x4/x8) with support balls



Variation DJ-z (x4 x8)



O Populated ball
+ Ball not populated

Figure 2 — DDR2 SDRAM x8 Ballout Using MO-207

1 Package Pinout & Addressing (cont'd)

1.1 DDR2 SDRAM Package Ballout (cont'd)

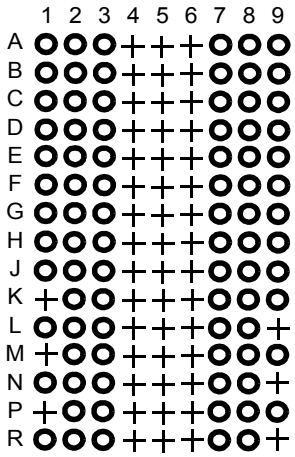
(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
A	VDD	NC	VSS				VSSQ	$\overline{\text{UDQS}}$	VDDQ	D
B	DQ14	VSSQ	UDM				UDQS	VSSQ	DQ15	E
C	VDDQ	DQ9	VDDQ				VDDQ	DQ8	VDDQ	F
D	DQ12	VSSQ	DQ11				DQ10	VSSQ	DQ13	G
E	VDD	NC	VSS				VSSQ	$\overline{\text{LDQS}}$	VDDQ	H
F	DQ6	VSSQ	LDM				LDQS	VSSQ	DQ7	J
G	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	K
H	DQ4	VSSQ	DQ3				DQ2	VSSQ	DQ5	L
J	VDDL	VREF	VSS				VSSDL	CK	VDD	M
K		CKE	$\overline{\text{WE}}$				$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT	N
L	NC, BA2	BA0	BA1				$\overline{\text{CAS}}$	$\overline{\text{CS}}$		P
M		A10/AP	A1				A2	A0	VDD	R
N	VSS	A3	A5				A6	A4		T
P		A7	A9				A11	A8	VSS	U
R	VDD	A12	NC, A14				NC, A15	NC, A13		V
										W
										X
	NC	NC						NC	NC	AA

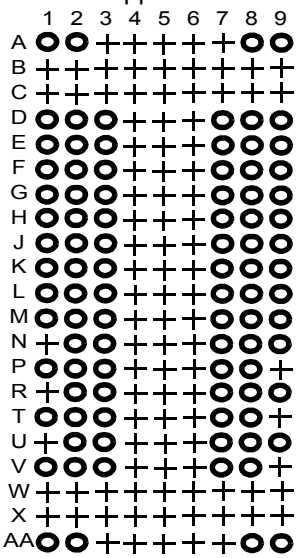
Variation DK-z without support balls

Variation DL-z with support balls

Variation DK-z (x16)



Variation DL-z (x16) with support balls



○ Populated ball
+ Ball not populated

Figure 3 — DDR2 SDRAM x16 Ballout Using MO-207

1 Package Pinout & Addressing (cont'd)

1.1 DDR2 SDRAM Package Ballout (cont'd)

(Top view: see balls through package)

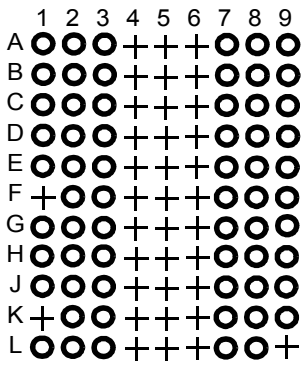
	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
										D
A	VDD	NC	VSS				VSSQ	$\overline{DQS}$	VDDQ	E
B	NC	VSSQ	DM				DQS	VSSQ	NC	F
C	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
D	NC	VSSQ	DQ3				DQ2	VSSQ	NC	H
E	VDDL	VREF	VSS				VSSDL	CK	VDD	J
F		CKE0	$\overline{WE}$				$\overline{RAS}$	$\overline{CK}$	ODT0	K
G	NC, BA2	BA0	BA1				$\overline{CAS}$	$\overline{CS0}$	$\overline{CS1}$	L
H	CKE1	A10/AP	A1				A2	A0	VDD	M
J	VSS	A3	A5				A6	A4	ODT1	N
K		A7	A9				A11	A8	VSS	P
L	VDD	A12	NC, A14				NC, A15	NC, A13		R
										T
										U
										V
	NC	NC						NC	NC	W

Variation tbd. without support balls

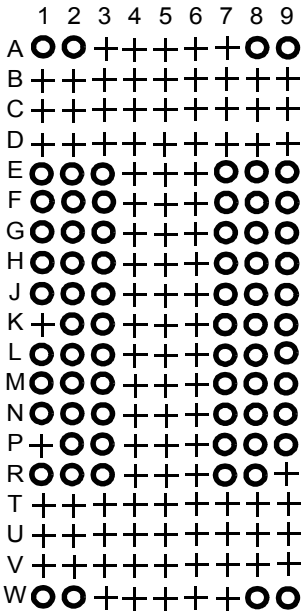
Variation tbd. with support balls

NOTE This stacked ballout does not represent the nonstacked ballout; it is intended only for use in a stacked package.

Variation tbd. (x4 x8)



Variation tbd.(x4/x8)
with support balls



O Populated ball
+ Ball not populated

Figure 4 — Stacked/Dual-Die DDR2 SDRAM x4 Ballout Using MO-TBD.

1 Package Pinout & Addressing (cont'd)

1.1 DDR2 SDRAM Package Ballout (cont'd)

(Top view: see balls through package)

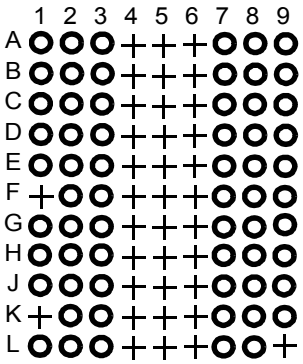
	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
										D
A	VDD	NU/$\overline{\text{RDQS}}$	VSS				VSSQ	$\overline{\text{DQS}}$	VDDQ	E
B	DQ6	VSSQ	DM/RDQS				DQS	VSSQ	DQ7	F
C	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
D	DQ4	VSSQ	DQ3				DQ2	VSSQ	DQ5	H
E	VDDL	VREF	VSS				VSSDL	CK	VDD	J
F		CKE0	$\overline{\text{WE}}$				$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT0	K
G	NC, BA2	BA0	BA1				$\overline{\text{CAS}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$	L
H	CKE1	A10/AP	A1				A2	A0	VDD	M
J	VSS	A3	A5				A6	A4	ODT1	N
K		A7	A9				A11	A8	VSS	P
L	VDD	A12	NC, A14				NC, A15	NC, A13		R
										T
										U
										V
	NC	NC						NC	NC	W

Variation tbd. without support balls

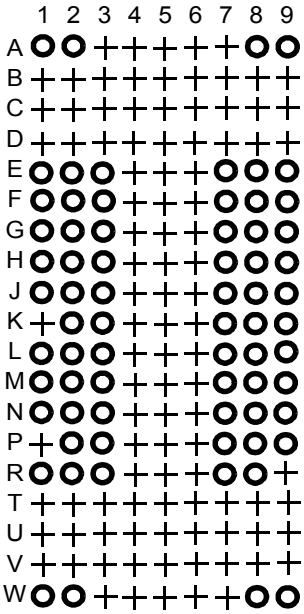
Variation tbd. with support balls

NOTE This stacked ballout is intended for use only in a stacked package, it does not represent the nonstacked package.

Variation tbd. (x4 x8)



Variation tbd.(x4/x8)
with support balls



O Populated ball
+ Ball not populated

Figure 5 — Stacked/Dual-Die DDR2 SDRAM x8 Ballout Using MO-TBD

1 Package Pinout & Addressing (cont'd)

1.2 Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, and $\overline{DM}$ signal for x4x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (UDM), (LDM)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/$\overline{RDQS}$ is enabled by EMRS command.
BA0 - BA2	Input	**Bank Address Inputs:** BA0 and BA1 for 256 and 512Mb, BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A15	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands.
DQ	Input/Output	**Data Input/ Output:** Bi-directional data bus.
DQS, ($\overline{DQS}$) (UDQS), ($\overline{UDQS}$) (LDQS), ($\overline{LDQS}$) (RDQS), ($\overline{RDQS}$)	Input/Output	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15. For the x8, an RDQS option using DM pin can be enabled via the EMRS(1) to simplify read timing. The data strobes DQS, LDQS, UDQS, and RDQS may be used in single ended mode or paired with optional complementary signals $\overline{DQS}$, $\overline{LDQS}$, $\overline{UDQS}$, and $\overline{RDQS}$ to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables all complementary data strobe signals.
NC		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 1.8V +/- 0.1V
V_{SSQ}	Supply	**DQ Ground**
V_{DDL}	Supply	**DLL Power Supply:** 1.8V +/- 0.1V
V_{SSDL}	Supply	**DLL Ground**
V_{DD}	Supply	**Power Supply:** 1.8V +/- 0.1V
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**Reference voltage**

In this data sheet, "differential DQS signals" refers to any of the following with A10 = 0 of EMRS(1)

x4 DQS/$\overline{DQS}$
x8 DQS/$\overline{DQS}$ if EMRS(1)[A11] = 0
x8 DQS/$\overline{DQS}$, RDQS/$\overline{RDQS}$, if EMRS(1)[A11] = 1
x16 LDQS/$\overline{LDQS}$ and UDQS/$\overline{UDQS}$

"single-ended DQS signals" refers to any of the following with A10 = 1 of EMRS(1)

x4 DQS
x8 DQS if EMRS(1)[A11] = 0
x8 DQS, RDQS, if EMRS(1)[A11] = 1
x16 LDQS and UDQS

1 Package Pinout & Addressing (cont'd)

1.3 DDR2 SDRAM Addressing

Table 1 — 256Mb Addressing

Configuration	64Mb x4	32Mb x 8	16Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A12	A0 ~ A12	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A8
Page size*1	1 KB	1 KB	1 KB

Table 2 — 512Mb Addressing

Configuration	128Mb x4	64Mb x 8	32Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 3 — 1Gb Addressing

Configuration	256Mb x4	128Mb x 8	64Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 4 — 2Gb Addressing

Configuration	512Mb x4	256Mb x 8	128Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A14	A0 ~ A14	A0 ~ A13
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

1 Package Pinout & Addressing (cont'd)

1.3 DDR2 SDRAM Addressing (cont'd)

Table 5 — 4 Gb Addressing

Configuration	1 Gb x4	512Mb x 8	256Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	tbd	tbd	tbd
Column Address	tbd	tbd	tbd
Page size *1	tbd	tbd	tbd

NOTE Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per bank, calculated as follows:

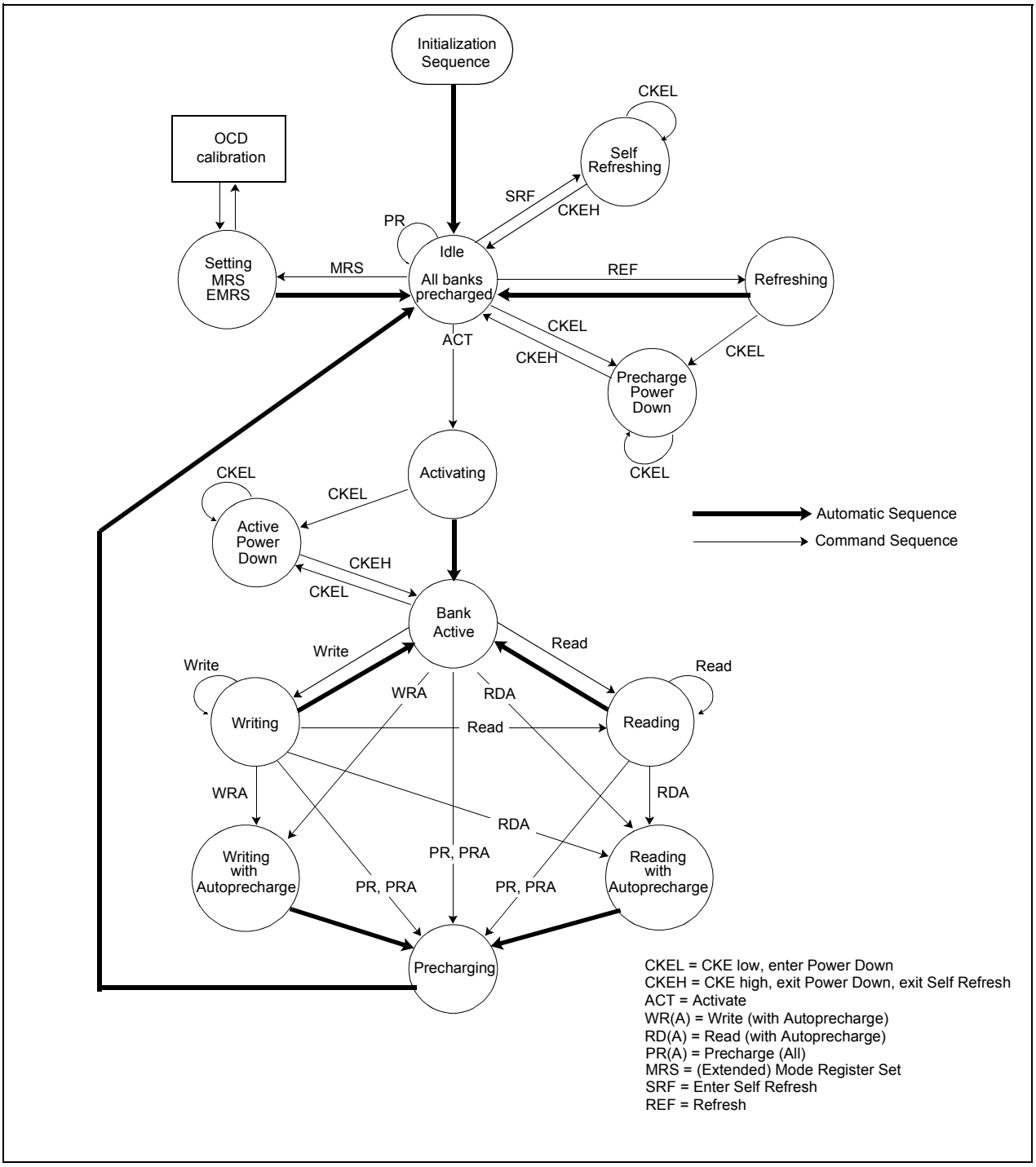
$$\text{page size} = 2^{\text{COLBITS}} * \text{ORG} \div 8$$

where

COLBITS = the number of column address bits
ORG = the number of I/O (DQ) bits

2 Functional Description

2.1 Simplified State Diagram



NOTE Use caution with this diagram. It is indented to provide a floorplan of the possible state transitions and the commands to control them, not all details. In particular situations involving more than one bank, enabling/disabling on-die termination, Power Down entry/exit - among other things - are not captured in full detail.

Figure 6 — DDR2 SDRAM Simplified State Diagram

2 Functional Description (cont'd)

2.2 Basic Functionality

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the active command are used to select the bank and row to be accessed (BA0-BA2 select the bank; A0-A15 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the auto precharge command is to be issued.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

2.2.1 Power up and Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

2.2.1.1 Power-up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain CKE below 0.2*VDDQ and ODT[*1] at a low state (all other inputs may be undefined.)

   - VDD, VDDL and VDDQ are driven from a single power converter output, AND
   - VTT is limited to 0.95 V max, AND
   - Vref tracks VDDQ/2.

   or

   - Apply VDD before or at the same time as VDDL.
   - Apply VDDL before or at the same time as VDDQ.
   - Apply VDDQ before or at the same time as VTT & Vref.

   at least one of these two sets of conditions must be met.

2. Start clock and maintain stable condition.
3. For the minimum of 200 us after stable power and clock (CK, $\overline{CK}$), then apply NOP or deselect & take CKE high.
4. Wait minimum of 400ns then issue precharge all command. NOP or deselect applied during 400ns period.
5. Issue EMRS(2) command. (To issue EMRS(2) command, provide "Low" to BA0 and BA2, "High" to BA1.)
6. Issue EMRS(3) command. (To issue EMRS(3) command, provide "Low" to BA2, "High" to BA0 and BA1.)
7. Issue EMRS to enable DLL. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1-2 and A13~A15.)
8. Issue a Mode Register Set command for "DLL reset".
   (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2, and A13~15.)
9. Issue precharge all command.

2.2.1 Power up and Initialization (cont'd)

2.2.1.1 Power-up and Initialization Sequence (cont'd)

10. Issue 2 or more auto-refresh commands.
11. Issue a mode register set command with low to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL.)
12. At least 200 clocks after Step 8, execute OCD Calibration (Off Chip Driver impedance adjustment). If OCD calibration is not used, EMRS OCD Default command (A9=A8= A7=1) followed by EMRS OCD Calibration Mode Exit command (A9=A8=A7=0) must be issued with other operating parameters of EMRS.
13. The DDR2 SDRAM is now ready for normal operation.

    *1) To guarantee ODT off, VREF must be valid and a low level must be applied to the ODT pin.

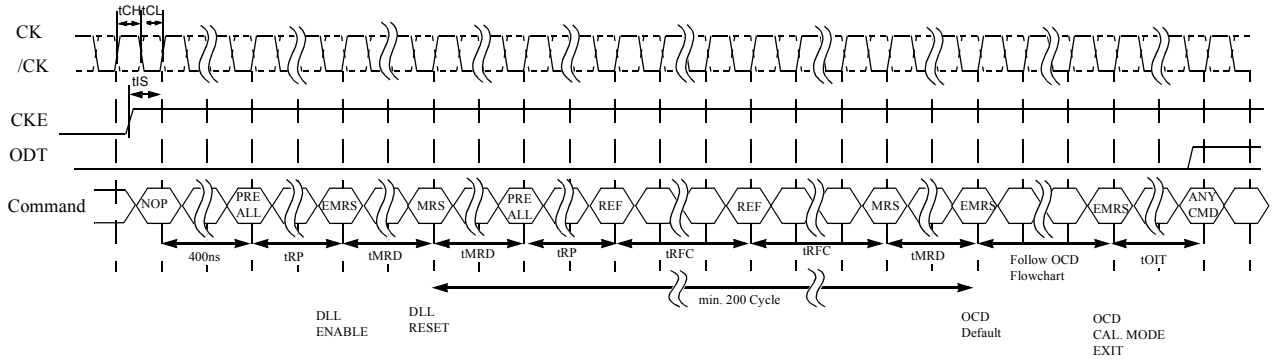


Figure 7 — Initialization Sequence after Power Up

2.2.2 Programming the Mode and Extended Mode Registers

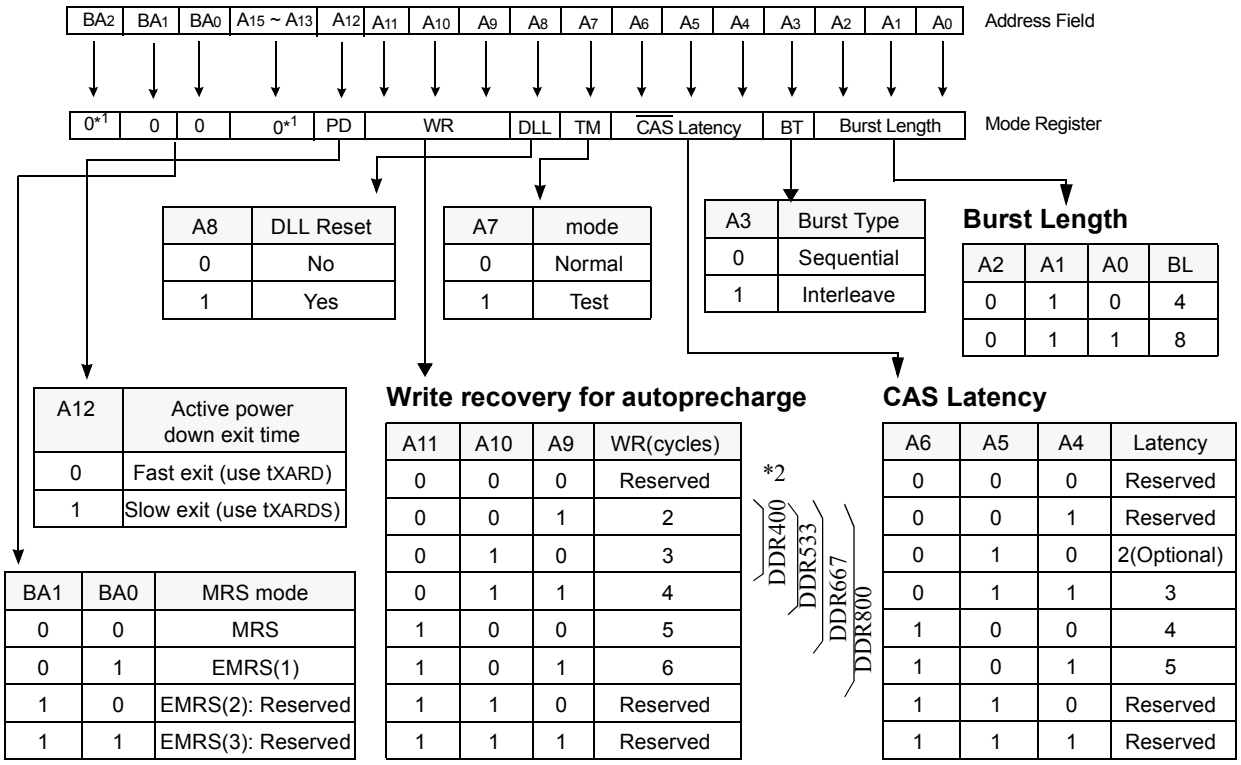
For application flexibility, burst length, burst type, $\overline{\text{CAS}}$ latency, DLL reset function, write recovery time(tWR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, driver impedance, additive CAS latency, ODT (On Die Termination), single-ended strobe, and OCD (off chip driver impedance adjustment) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register (MR) or Extended Mode Registers (EMR(#)) can be altered by re-executing the MRS and EMRS Commands. If the user chooses to modify only a subset of the MRS or EMRS variables, all variables must be redefined when the MRS or EMRS commands are issued.

MRS, EMRS and Reset DLL do not affect array contents, which means reinitialization including those can be executed any time after power-up without affecting array contents.

2.2.2 Programming the Mode and Extended Mode Registers (cont'd)

2.2.2.1 DDR2 SDRAM Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls $\overline{\text{CAS}}$ latency, burst length, burst sequence, test mode, DLL reset, tWR and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, BA0 and BA1, while controlling the state of address pins A0 ~ A15. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 ~ A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, $\overline{\text{CAS}}$ latency is defined by A4 ~ A6. The DDR2 doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Write recovery time tWR is defined by A9 ~ A11. Refer to Figure 8 for specific codes.



1. BA2 and A13~A15 are reserved for future use and must be programmed to 0 when setting the mode register.

2. WR(write recovery for autoprecharge) min is determined by tCK max and WR max is determined by tCK min. WR in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer (WR[cycles] = tWR(ns)/tCK(ns)). The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

Figure 8 — DDR2 SDRAM Mode Register Set (MRS)

2.2.2 Programming the Mode and Extended Mode Registers (cont'd)

2.2.2.2 DDR2 SDRAM Extended Mode Register Set

EMRS(1)

The extended mode register(1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, ODT, $\overline{DQS}$ disable, OCD program, RDQS enable. The default value of the extended mode register(1) is not defined, therefore the extended mode register(1) must be written after power-up for proper operation. The extended mode register(1) is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA0 and low on BA1, while controlling the states of address pins A0 ~ A15. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register(1). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register(1). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a half strength output driver. A3~A5 determines the additive latency, A7~A9 are used for OCD control, A10 is used for $\overline{DQS}$ disable and A11 is used for RDQS enable. A2 and A6 are used for ODT setting.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAC or tDQSCK parameters.

2.2.2.2 DDR2 SDRAM Extended Mode Register Set (cont'd)

BA2	BA1	BA0	A15 ~ A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0*[1]	0	1	0*[1]	Qoff	RDQS	$\overline{DQS}$	OCD program			Rtt	Additive latency			Rtt	D.I.C	DLL	Extended Mode Register

BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2): Reserved
1	1	EMRS(3): Reserved

A6	A2	Rtt (NOMINAL)
0	0	ODT Disabled
0	1	75 ohm
1	0	150 ohm
1	1	Reserved

A0	DLL Enable
0	Enable
1	Disable

A9	A8	A7	OCD Calibration Program
0	0	0	OCD Calibration mode exit; maintain setting
0	0	1	Drive(1)
0	1	0	Drive(0)
1	0	0	Adjust mode[a]
1	1	1	OCD Calibration default [b]

a: When Adjust mode is issued, AL from previously set value must be applied.
b: After setting to default, OCD mode needs to be exited by setting A9-A7 to 000. Refer to the following 2.2.2.3 section for detailed information

A5	A4	A3	Additive Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A12	Qoff (Optional)[a]
0	Output buffer enabled
1	Output buffer disabled

a. Outputs disabled - DQs, DQSs, $\overline{DQS}$s, RDQS, $\overline{RDQS}$. This feature is used in conjunction with dimm IDD meaurements when IDDQ is not desired to be included.

A1	Output Driver Impedance Control	Driver Size
0	Normal	100%
1	Weak	60%

A10	$\overline{DQS}$
0	Enable
1	Disable

A11	RDQS Enable
0	Disable
1	Enable

* If RDQS is enabled, the DM function is disabled. RDQS is active for reads and don't care for writes.

A11 (RDQS Enable)	A10 ($\overline{DQS}$ Enable)	Strobe Function Matrix			
		RDQS/DM	RDQS	DQS	DQS
0 (Disable)	0 (Enable)	DM	Hi-z	DQS	DQS
0 (Disable)	1 (Disable)	DM	Hi-z	DQS	Hi-z
1 (Enable)	0 (Enable)	RDQS	RDQS	DQS	DQS
1 (Enable)	1 (Disable)	RDQS	Hi-z	DQS	Hi-z

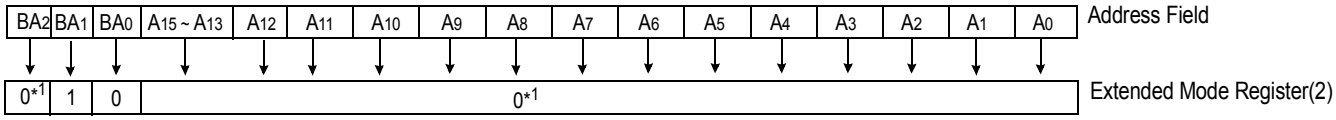
* BA2 and A13~A15 are reserved for future use and must be programmed to 0 when setting the mode register.

Figure 9 — EMRS(1) Programming

2.2.2.2 DDR2 SDRAM Extended Mode Register Set (cont'd)

EMRS(2)

1

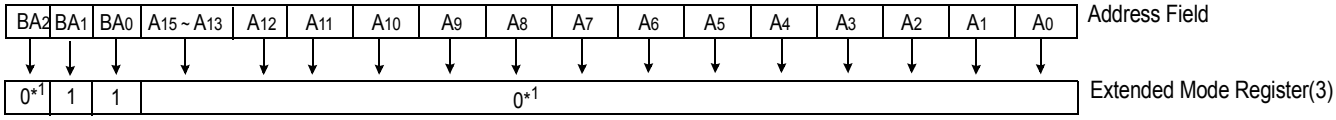


EMRS(2) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

Figure 10 — EMRS(2) Programming: Reserved

EMRS(3)

1



EMRS(3) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

Figure 11 — EMRS(3) Programming: Reserved

2.2.2.3 Off-Chip Driver (OCD) Impedance Adjustment

DDR2 SDRAM supports driver calibration feature and the flow chart below is an example of sequence. Every calibration mode command should be followed by "OCD calibration mode exit" before any other command being issued. MRS should be set before entering OCD impedance adjustment and ODT (On DieTermination) should be carefully controlled depending on system environment

Extended Mode Register Set for OCD impedance adjustment

OCD impedance adjustment can be done using the following EMRS mode. In drive mode all outputs are driven out by DDR2 SDRAM and drive of RDQS is dependent on EMRS bit enabling RDQS operation. In Drive(1) mode, all DQ, DQS (and RDQS) signals are driven high and all $\overline{DQS}$ signals are driven low. In drive(0) mode, all DQ, DQS (and RDQS) signals are driven low and all $\overline{DQS}$ signals are driven high. In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics have a nominal impedance value of 18 ohms during nominal temperature and voltage conditions. Output driver characteristics for OCD calibration default are specified in Table 6. OCD applies only to normal full strength output drive setting defined by EMRS(1) and if half strength is set, OCD default output driver characteristics are not applicable. When OCD calibration adjust mode is used, OCD default output driver characteristics are not applicable. After OCD calibration is completed or driver strength is set to default, subsequent EMRS commands not intended to adjust OCD characteristics must specify A9-A7 as '000' in order to maintain the default or calibrated value.

Table 6 — OCD Drive Mode Program

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive(1) DQ, DQS, (RDQS) high and $\overline{DQS}$ low
0	1	0	Drive(0) DQ, DQS, (RDQS) low and $\overline{DQS}$ high
1	0	0	Adjust mode
1	1	1	OCD calibration default

2.2.2.3 Off-Chip Driver (OCD) Impedance Adjustment (cont'd)

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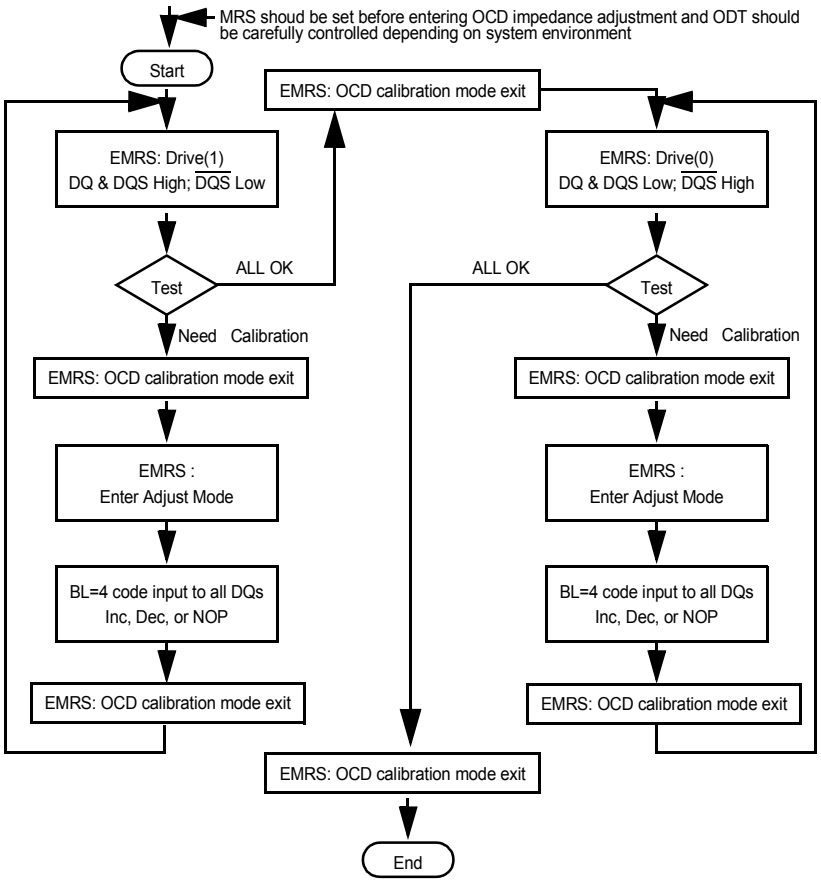


Figure 12 — OCD Impedance Adjustment

OCD Impedance Adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS command along with a 4bit burst code to DDR2 SDRAM as in Table 7. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive this burst code to all DQs at the same time. DT0 in table X means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the 16 step range. When Adjust mode command is issued, AL from previously set value must be applied.

2.2.2.3 Off-Chip Driver (OCD) Impedance Adjustment (cont'd)

Table 7 — OCD Adjust Mode Program

4bit burst code inputs to all DQs				Operation	
DT_0	DT_1	DT_2	DT_3	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP (No operation)	NOP (No operation)
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other Combinations				Reserved	

For proper operation of adjust mode, WL = RL - 1 = AL + CL - 1 clocks and tDS/tDH should be met as shown in Figure 13. For input data pattern for adjustment, DT0 - DT3 is a fixed order and "not affected by MRS addressing mode (i.e. sequential or interleave).

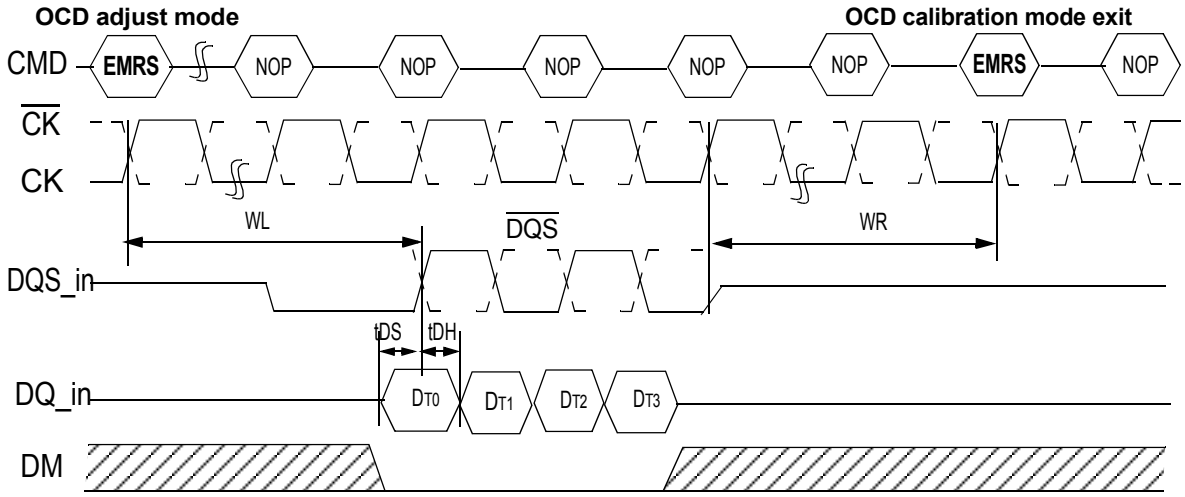


Figure 13 — OCD Adjust Mode

Drive Mode

Drive mode, both Drive(1) and Drive(0), is used for controllers to measure DDR2 SDRAM Driver impedance. In this mode, all outputs are driven out tOIT after "enter drive mode" command and all output drivers are turned-off tOIT after "OCD calibration mode exit" command as shown in Figure 14.

2.2.2.3 Off-Chip Driver (OCD) Impedance Adjustment (cont'd)

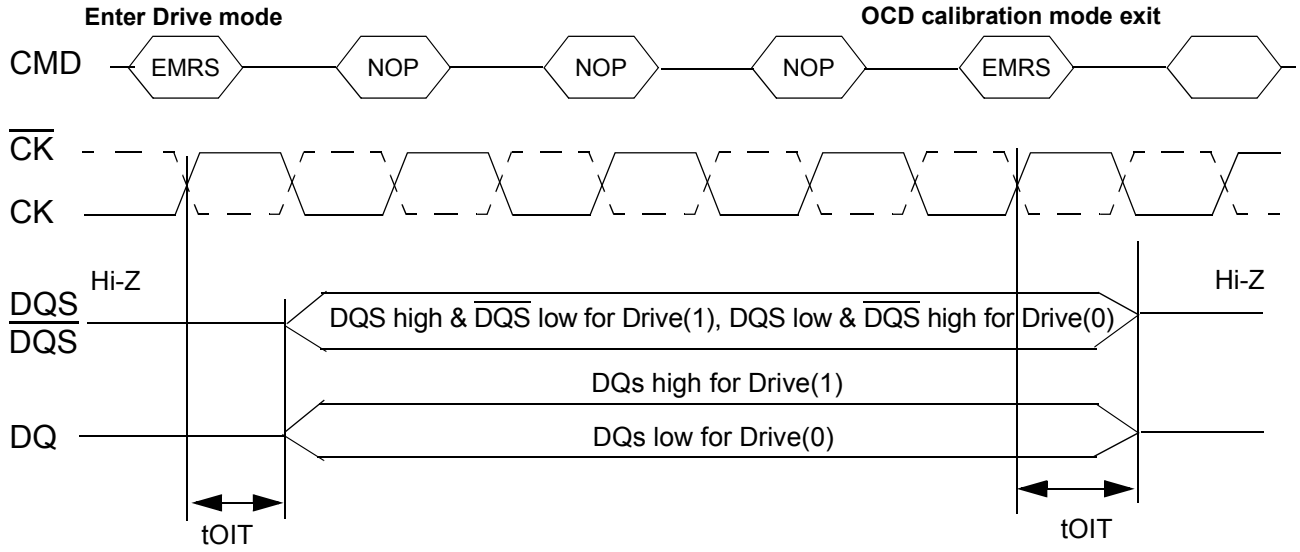


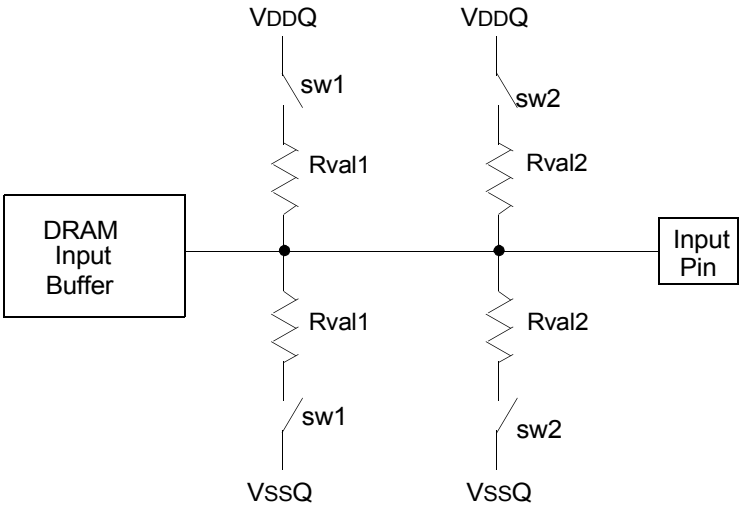
Figure 14 — OCD Drive Mode

2.2.2.4 ODT (On Die Termination)

On Die Termination (ODT) is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQS/DQS, RDQS/RDQS, and DM signal for x4x8 configurations via the ODT control pin. For x16 configuration ODT is applied to each DQ, UDQS/UDQS, LDQS/LDQS, UDM, and LDM signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function is supported for ACTIVE and STANDBY modes. ODT is turned off and not supported in SELF REFRESH mode.

2.2.2.4 ODT (On Die Termination) (cont'd)



Switch sw1 or sw2 is enabled by ODT pin.
Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
Termination included on all DQs, DM, DQS, $\overline{DQS}$, RDQS, and $\overline{RDQS}$ pins.
Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

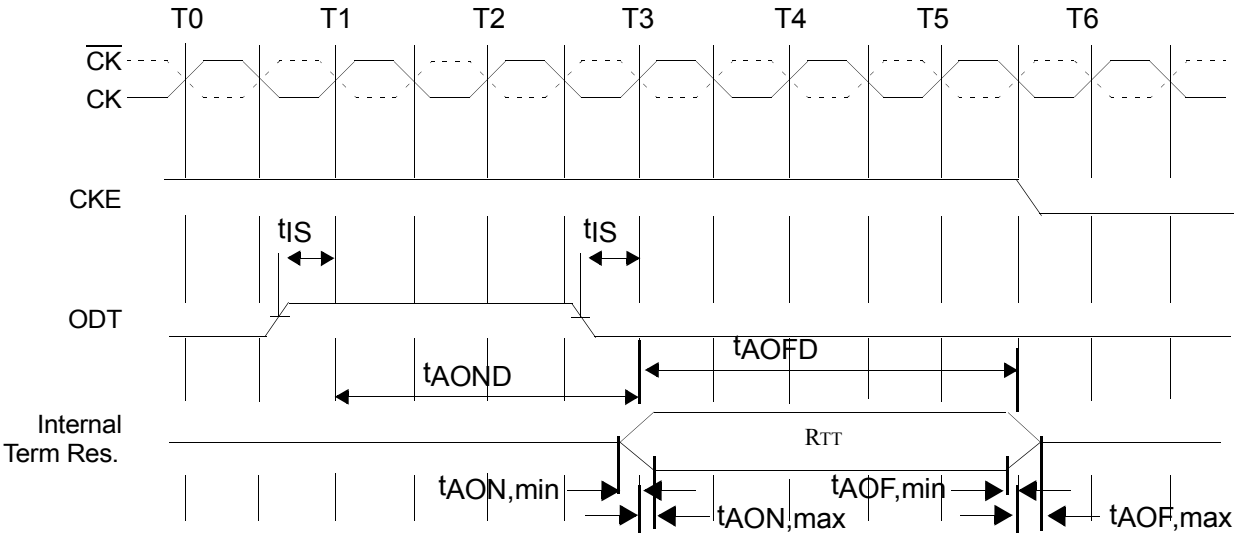


Figure 16 — ODT Timing for Active/Standby Mode

2.2.2.4 ODT (On Die Termination) (cont'd)

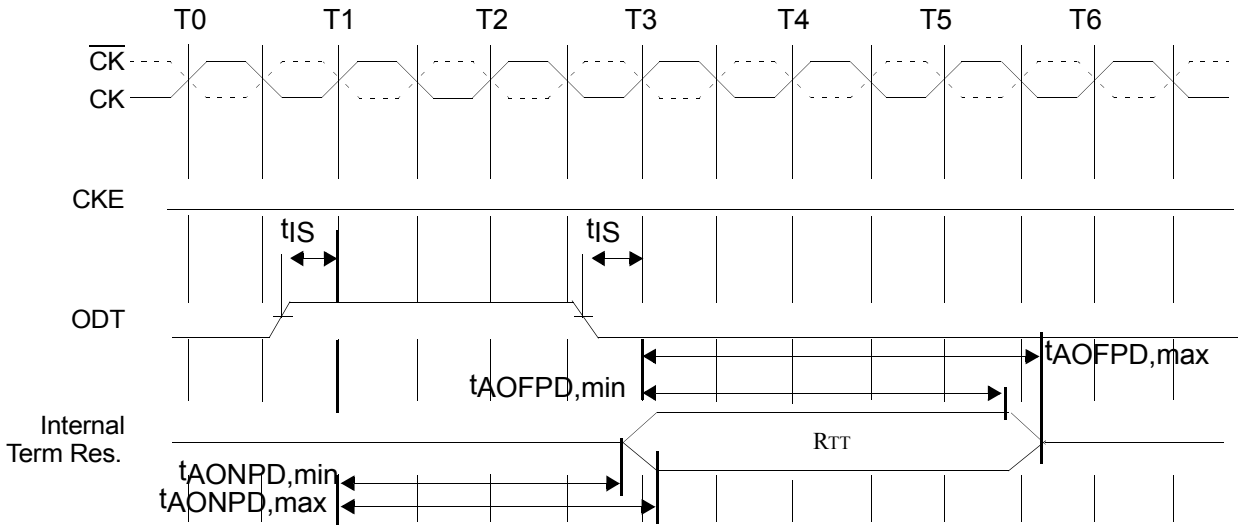


Figure 17 — ODT Timing for Powerdown Mode

2.2.2.4 ODT (On Die Termination) (cont'd)

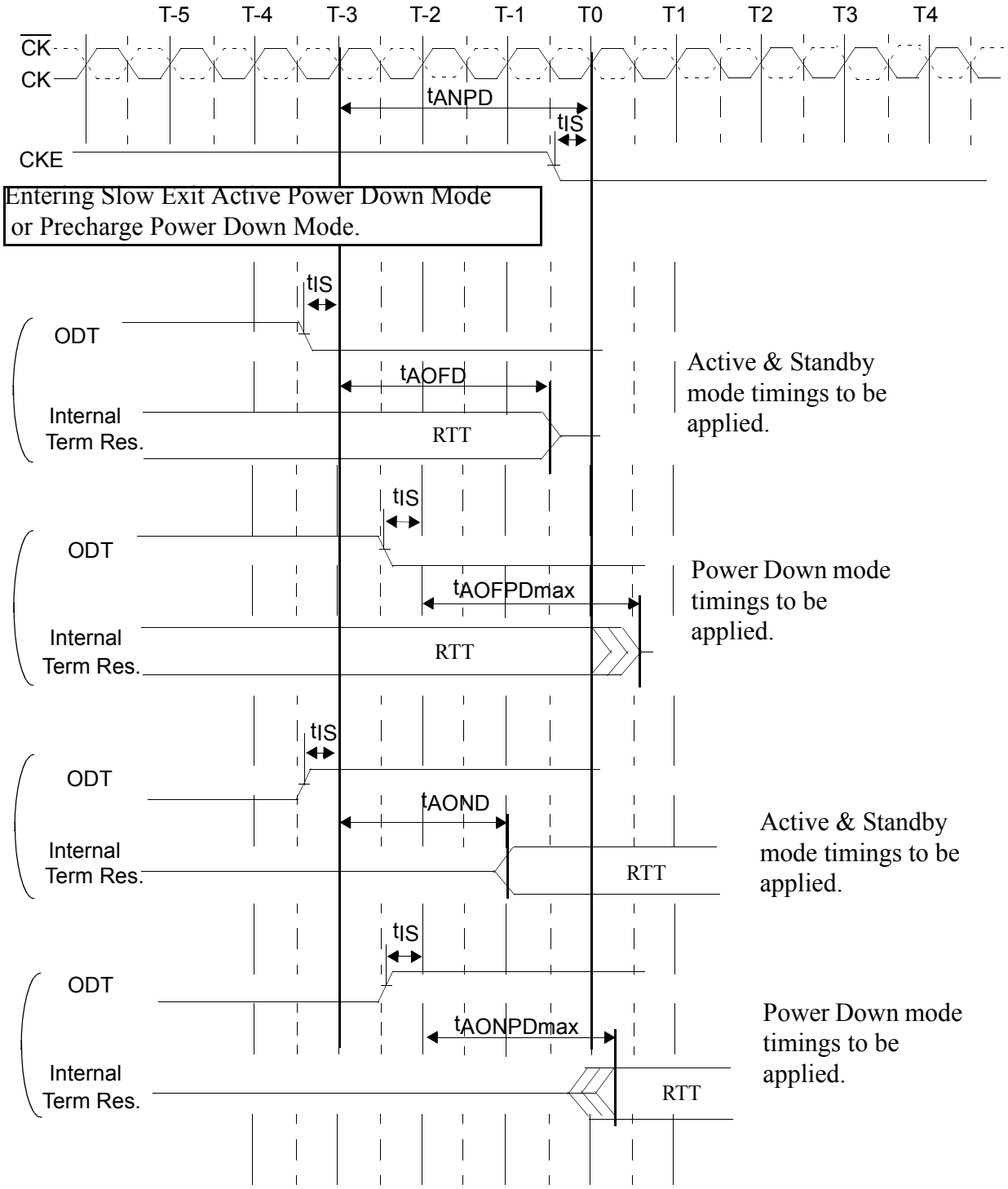


Figure 18 — ODT Timing Mode Switch at Entering Power Down Mode

2.2.2.4 ODT (On Die Termination) (cont'd)

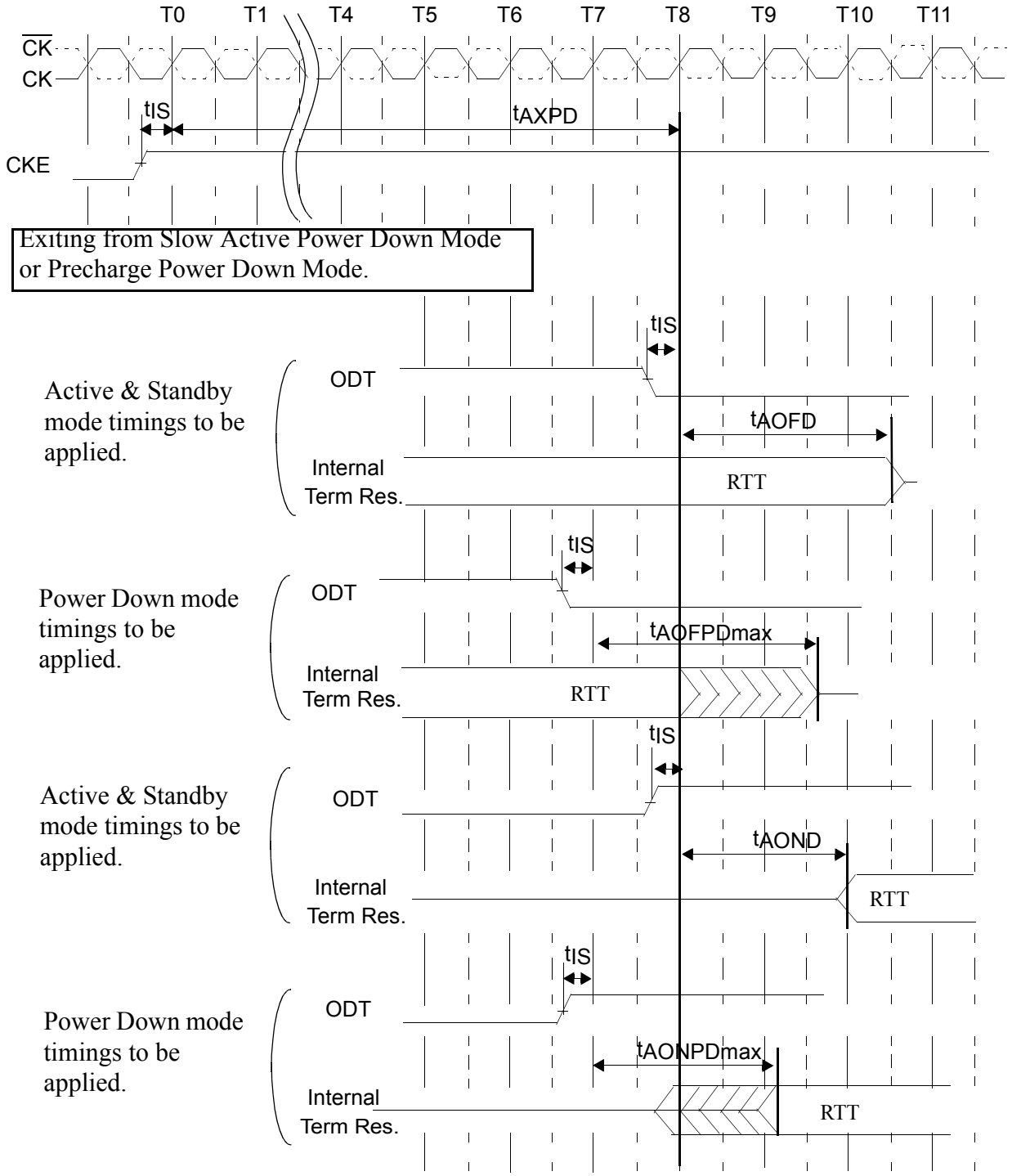


Figure 19 — ODT Timing Mode Switch at Exiting Power Down Mode

2.2.3 Bank Activate Command

The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The bank addresses BA0 ~ BA2 are used to select the desired bank. The row address A0 through A15 is used to determine which row to activate in the selected bank. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the tRCDmin specification, then additive latency must be programmed into the device to delay when the R/W command is internally issued to the device. The additive latency value must be chosen to assure tRCDmin is satisfied. Additive latencies of 0, 1, 2, 3 and 4 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between Bank Activate commands is t_{RRD}.

In order to ensure that 8 bank devices do not exceed the instantaneous current supplying capability of 4 bank devices, certain restrictions on operation of the 8 bank devices must be observed. There are two rules, one for restricting the number of sequential ACT commands that can be issued and another for allowing more time for $\overline{RAS}$ precharge for a Precharge All command. The rules are as follows:

1. 8 bank device Sequential Bank Activation Restriction: No more than 4 banks may be activated in a rolling 4 * tRRD + 2 * tCK window. tRRD must be converted to clocks prior to multiplying by 4 and prior to adding 2*tCK. Converting to clocks is done by dividing tRRD(ns) by tCK(ns) and rounding up to next integer value.
2. 8 bank device Precharge All Allowance: tRP for a Precharge All command for an 8 Bank device will equal to tRP + 1 * tCK, where tRP is the value for a single bank pre-charge.

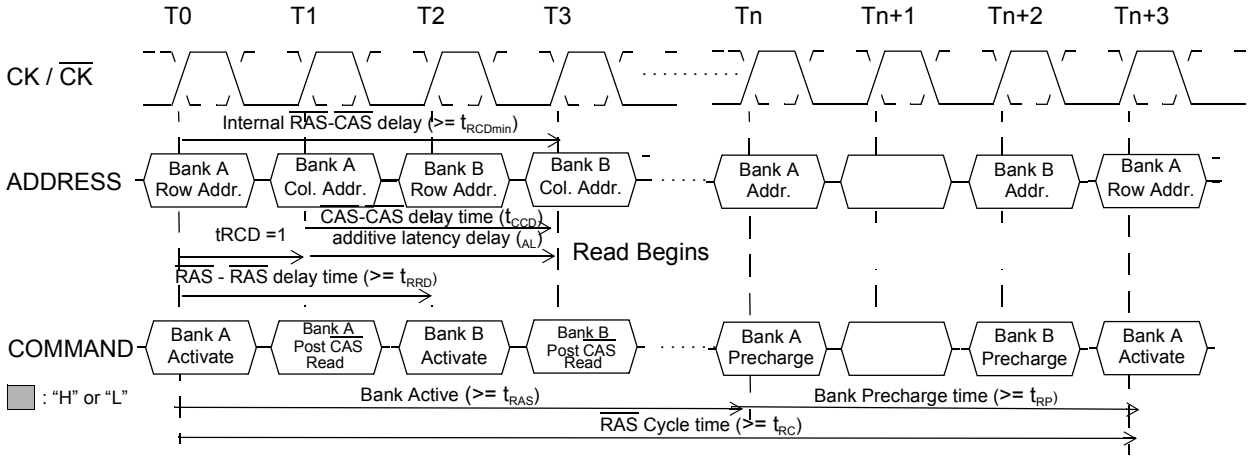


Figure 20 — Bank Activate Command Cycle: tRCD = 3, AL = 2, tRP = 3, tRRD = 2, tCCD = 2

2.2.4 Read and Write Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting $\overline{RAS}$ high, $\overline{CS}$ and $\overline{CAS}$ low at the clock's rising edge. $\overline{WE}$ must also be defined at this time to determine whether the access cycle is a read operation ($\overline{WE}$ high) or a write operation ($\overline{WE}$ low).

The DDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is strictly restricted to specific segments of the page length. For example, the 32Mbit x 4 I/O x 4 Bank chip has a page length of 2048 bits (defined by CA0-CA9, CA11). The page length of 2048 is divided into 512 or 256 uniquely addressable boundary segments depending on burst length, 512 for 4 bit burst, 256 for 8 bit burst respectively. A 4-bit or 8 bit burst operation will occur entirely within one of the 512 or 256 groups beginning with the column address supplied to the device during the Read or Write Command (CA0-CA9, CA11). The second, third and fourth access will also occur within this group segment, however, the burst order is a function of the starting address, and the burst sequence.

A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. However, in case of BL = 8 setting, two cases of interrupt by a new burst access are allowed, one reads interrupted by a read, the other writes interrupted by a write with 4 bit burst boundary respectively. The minimum $\overline{CAS}$ to $\overline{CAS}$ delay is defined by tCCD, and is a minimum of 2 clocks for read or write cycles.

2.2.4.1 Posted $\overline{CAS}$

Posted $\overline{CAS}$ operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a $\overline{CAS}$ read or write command to be issued immediately after the $\overline{RAS}$ bank activate command (or any time during the $\overline{RAS}$-$\overline{CAS}$-delay time, tRCD, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the $\overline{CAS}$ latency (CL). Therefore if a user chooses to issue a R/W command before the tRCDmin, then AL (greater than 0) must be written into the EMRS(1). The Write Latency (WL) is always defined as RL - 1 (read latency -1) where read latency is defined as the sum of additive latency plus $\overline{CAS}$ latency (RL=AL+CL). Read or Write operations using AL allow seamless bursts (refer to seamless operation timing diagram examples in Read burst and Write burst section).

Examples of posted $\overline{CAS}$ operation

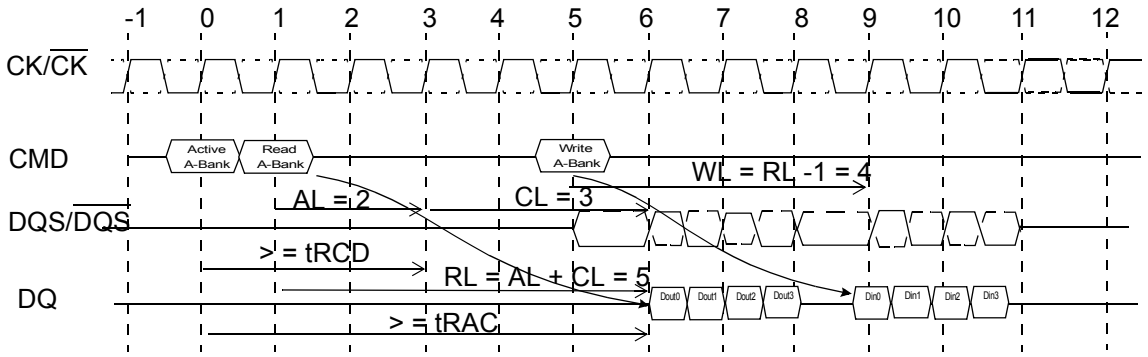


Figure 21 — Example 1: Read Followed by a Write to the Same Bank
[AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4]

2.2.4 Read and Write Access Modes (cont'd)

2.2.4.1 Posted $\overline{CAS}$ (cont'd)

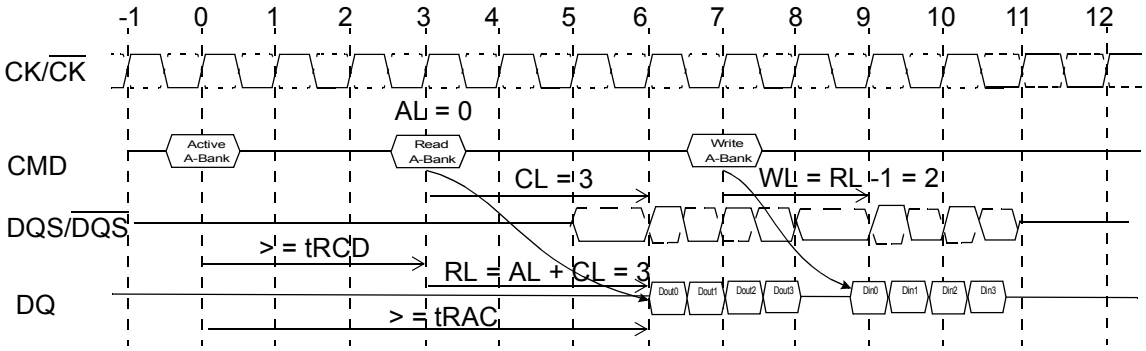


Figure 22 — Example 2: Read Followed by a Write to the Same Bank [AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4]

2.2.4.2 Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. DDR2 SDRAM supports 4 bit burst and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MRS, which is similar to the DDR SDRAM operation. Seamless burst read or write operations are supported. Unlike DDR devices, interruption of a burst read or write cycle during BL = 4 mode operation is prohibited. However in case of BL = 8 mode, interruption of a burst read or write operation is limited to two cases, reads interrupted by a read, or writes interrupted by a write. Therefore the Burst Stop command is not supported on DDR2 SDRAM devices.

Table 8 — Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	0 0 0	0, 1, 2, 3	0, 1, 2, 3
	0 0 1	1, 2, 3, 0	1, 0, 3, 2
	0 1 0	2, 3, 0, 1	2, 3, 0, 1
	0 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

NOTE Page length is a function of I/O organization and column addressing.

2.2.4 Read and Write Access Modes (cont'd)

2.2.4.3 Burst Read Command

The Burst Read command is initiated by having $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low 1 clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus $\overline{CAS}$ latency (CL). The CL is defined by the Mode Register Set (MRS), similar to the existing SDR and DDR SDRAMs. The AL is defined by the Extended Mode Register Set (1)(EMRS(1)).

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single-ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at V_{REF}. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 ohm to 10 Kohm resistor to insure proper operation.

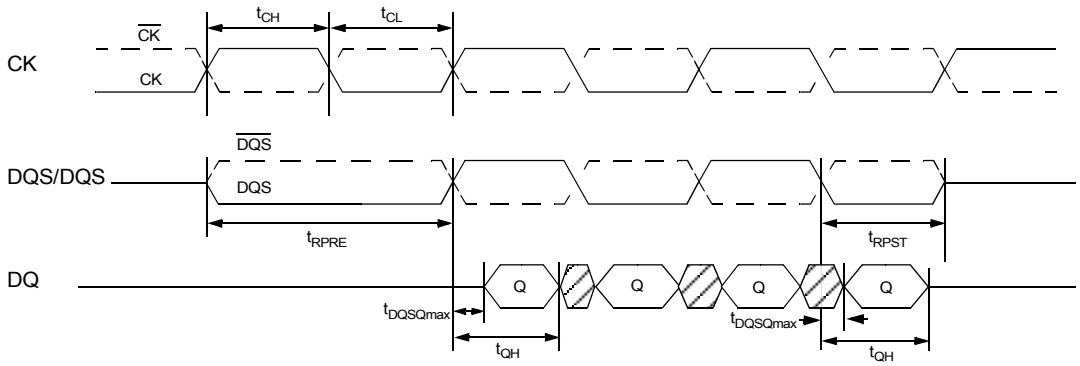


Figure 23 — Data Output (Read) Timing

2.2.4.3 Burst Read Command (cont'd)

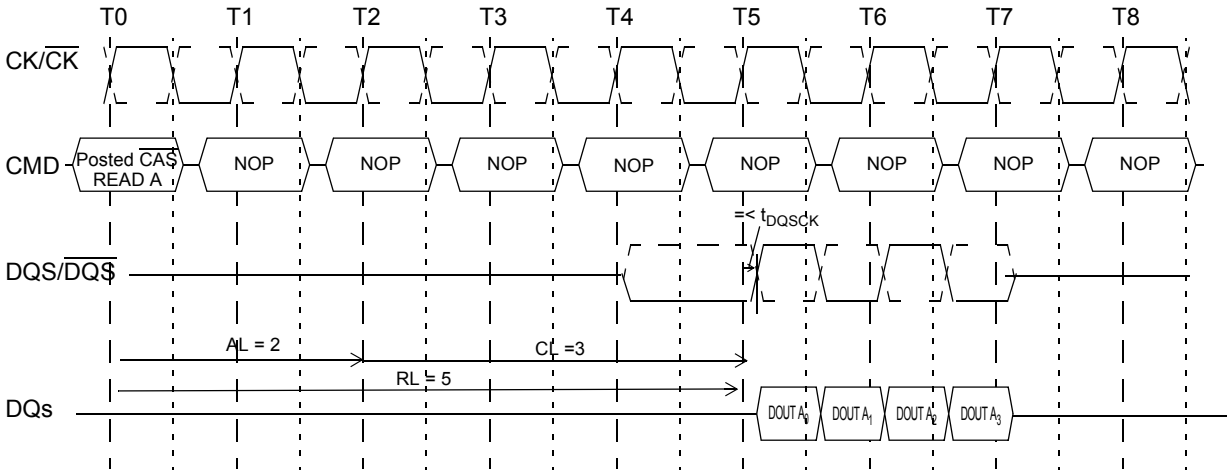


Figure 24 — Burst Read Operation: RL = 5 (AL = 2, CL = 3, BL = 4)

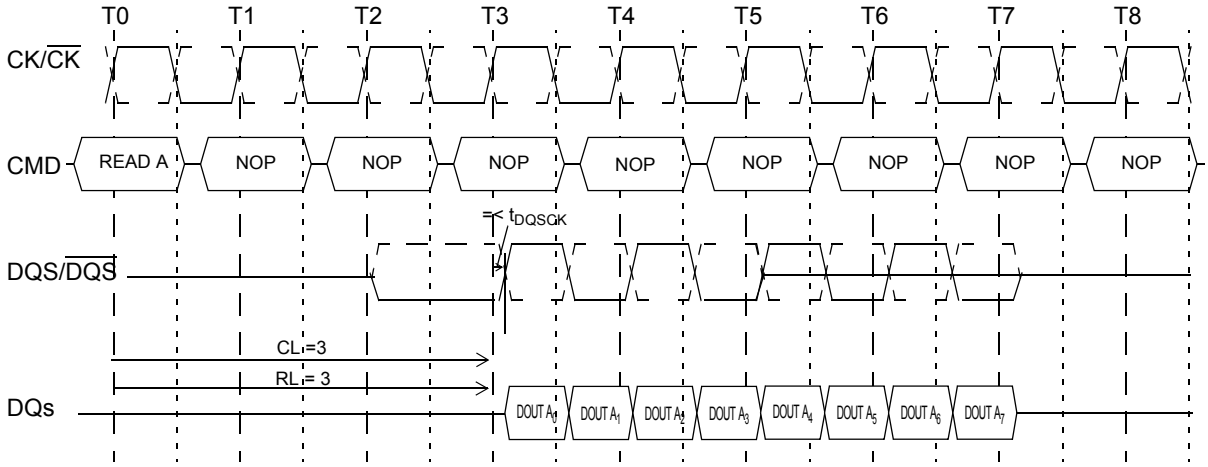
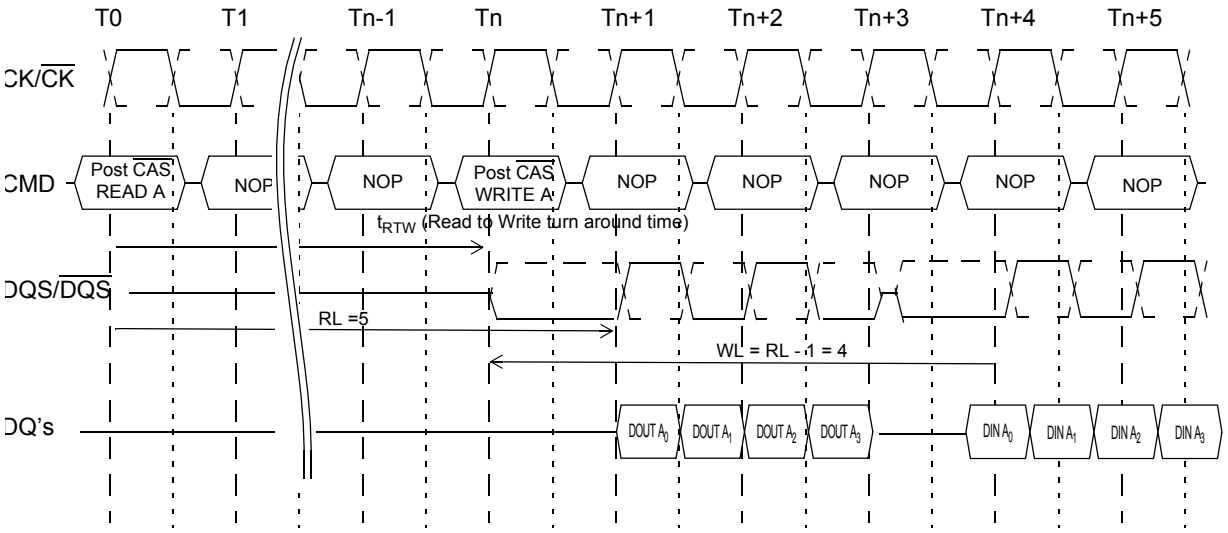


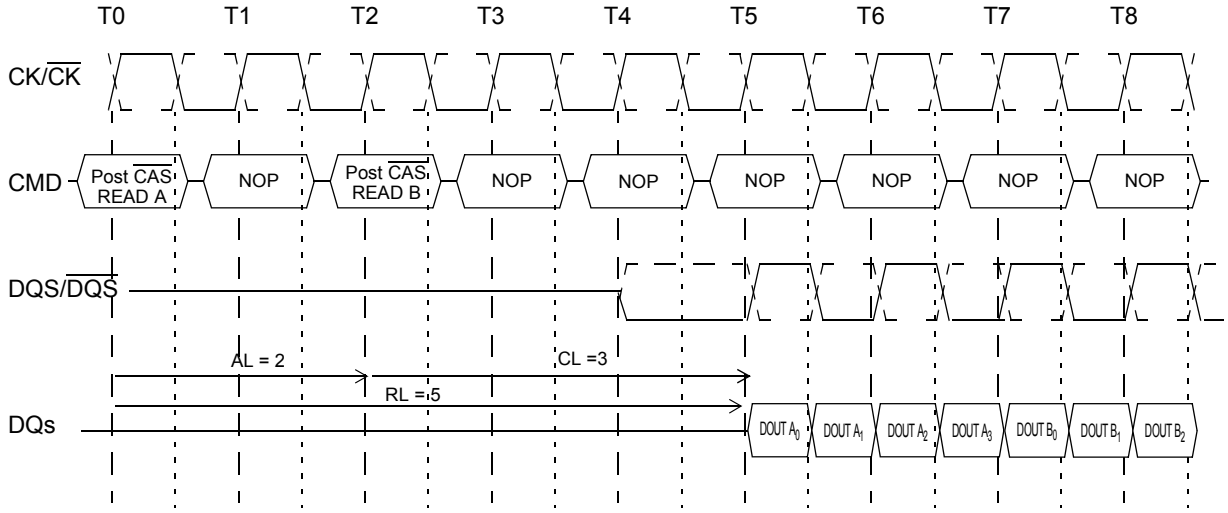
Figure 25 — Burst Read Operation: RL = 3 (AL = 0 and CL = 3, BL = 8)

2.2.4.3 Burst Read Command (cont'd)



The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation.

Figure 26 — Burst Read Followed by Burst Write: RL = 5, WL = (RL-1) = 4, BL = 4



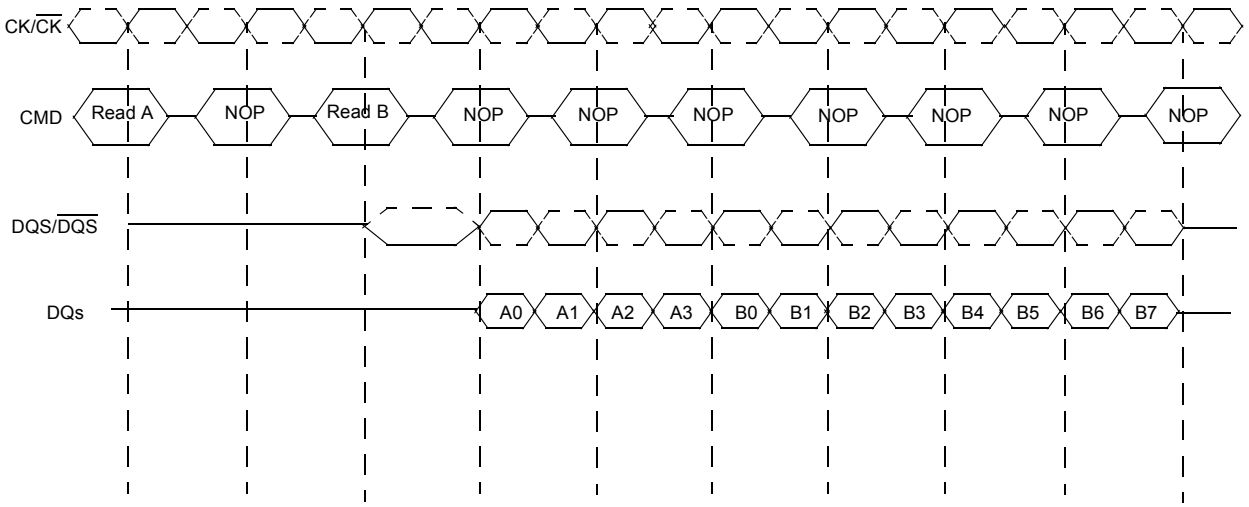
The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 27 — Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

Reads Interrupted by a Read

Burst read can only be interrupted by another read with 4 bit burst boundary. Any other case of read interrupt is not allowed.

2.2.4.3 Burst Read Command (cont'd)



NOTE 1 Read burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.
NOTE 2 Read burst of 8 can only be interrupted by another Read command. Read burst interruption by Write command or Precharge command is prohibited.
NOTE 3 Read burst interrupt must occur exactly two clocks after previous Read command. Any other Read burst interrupt timings are prohibited.
NOTE 4 Read burst interruption is allowed to any bank inside DRAM.
NOTE 5 Read burst with Auto Precharge enabled is not allowed to interrupt.
NOTE 6 Read burst interruption is allowed by another Read with Auto Precharge command.
NOTE 7 All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, Minimum Read to Precharge timing is AL + BL/2 where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt).

Figure 28 — Read Burst Interrupt Timing Example: (CL=3, AL=0, RL=3, BL=8)

2.2.4.4 Burst Write Operation

The Burst Write command is initiated by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1). A data strobe signal (DQS) should be driven low (preamble) one clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed, which is 4 or 8 bit burst. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ Signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is the write recovery time (WR).

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at V_{REF}. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 ohm to 10 Kohm resistor to insure proper operation.

2.2.4.4 Burst Write Operation (cont'd)

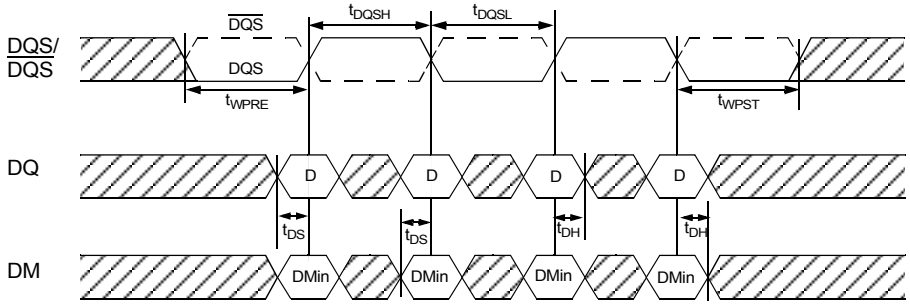


Figure 29 — Data Input (Write) Timing

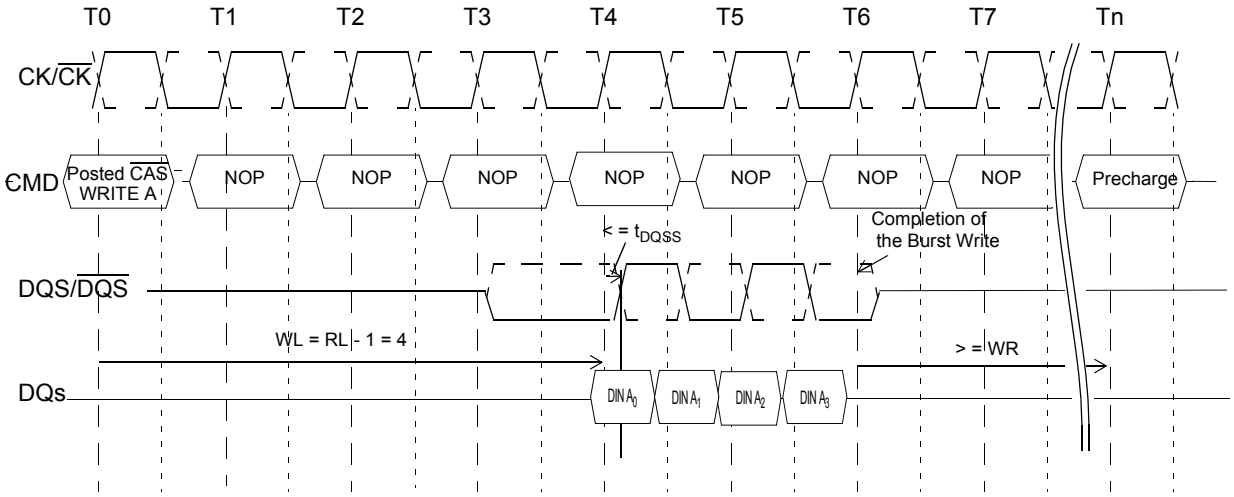


Figure 30 — Burst Write Operation: RL = 5, WL = 4, tWR = 3 (AL=2, CL=3), BL = 4

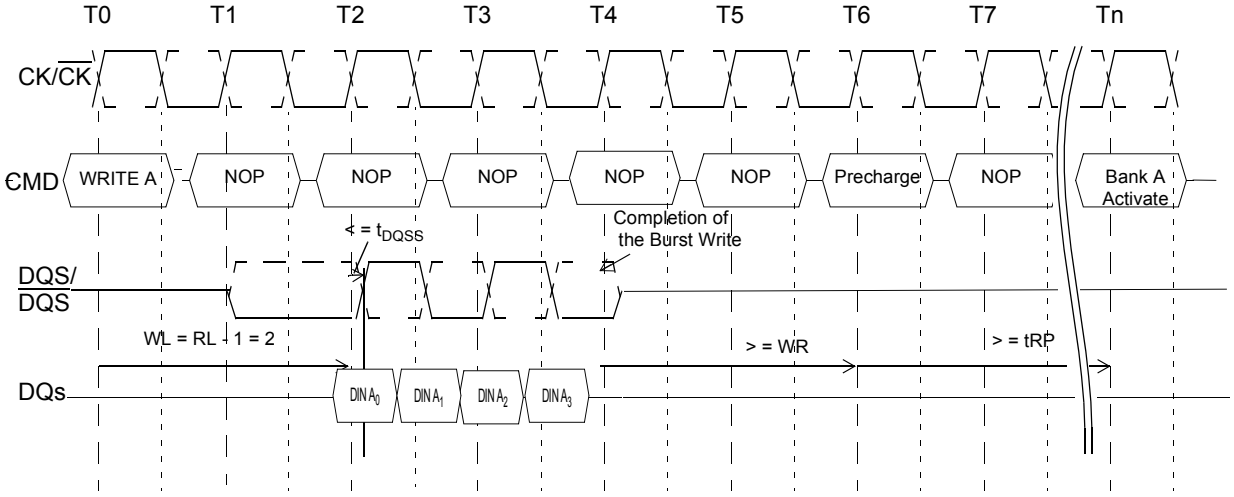
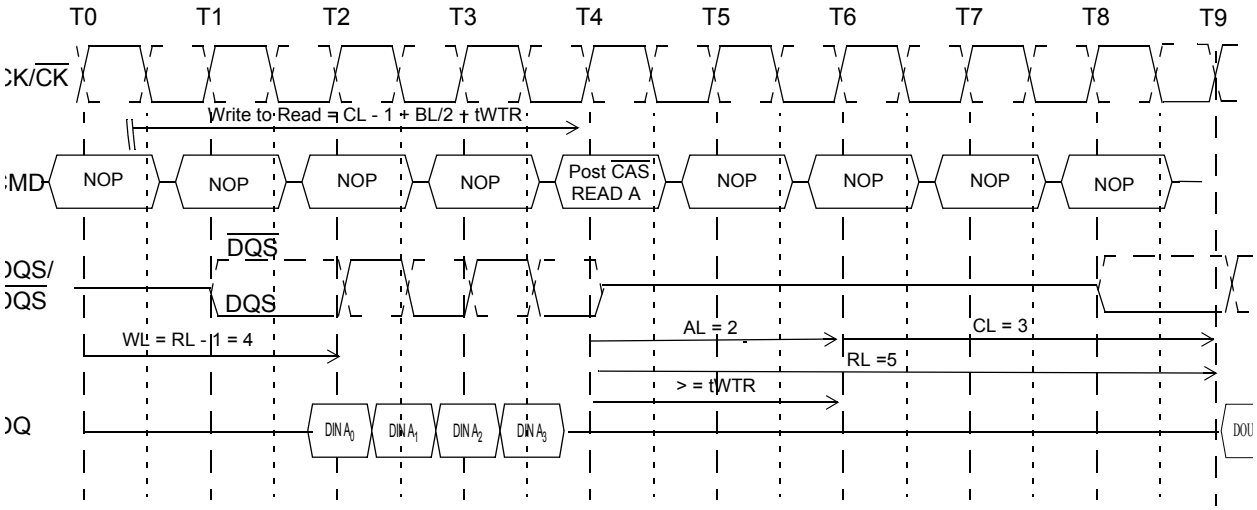


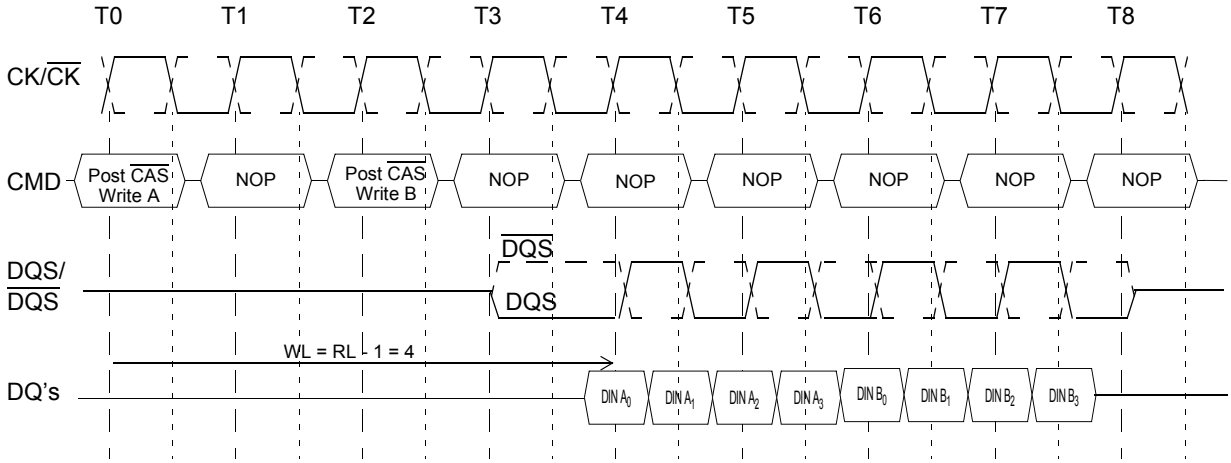
Figure 31 — Burst Write Operation: RL = 3, WL = 2, tWR = 2 (AL=0, CL=3), BL = 4

2.2.4.4 Burst Write Operation (cont'd)



The minimum number of clock from the burst write command to the burst read command is [CL - 1 + BL/2 + tWTR]. This tWTR is not a write recovery time (tWR) but the time required to transfer the 4bit write data from the input buffer into sense amplifiers in the array. tWTR is defined in AC spec table of this data sheet.

Figure 32 — Burst Write Followed by Burst Read: RL = 5 (AL=2, CL=3), WL = 4, tWTR = 2, BL = 4



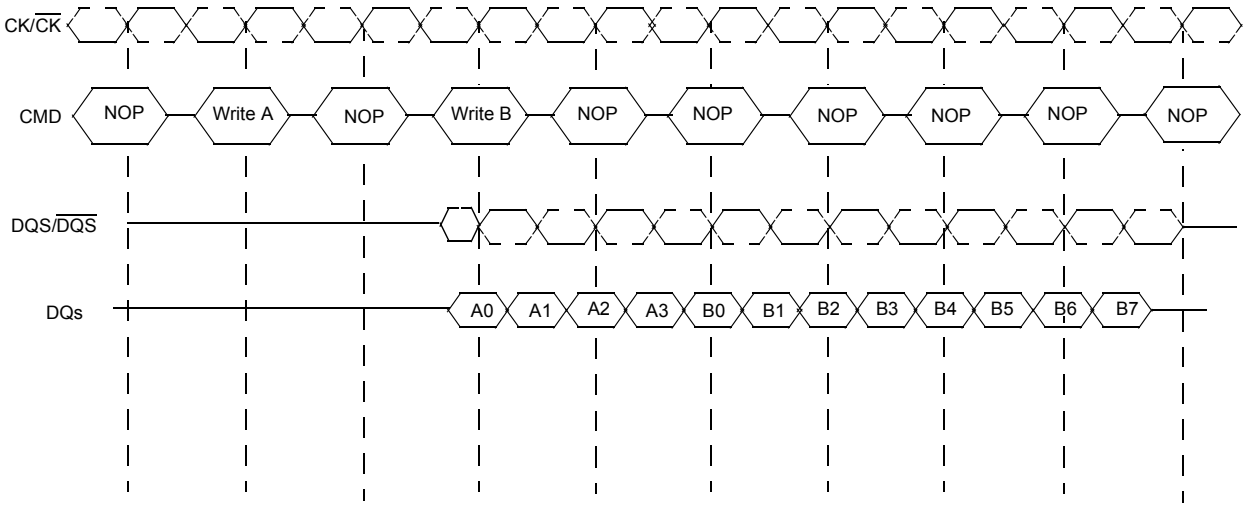
The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for
BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 33 — Seamless Burst Write Operation: RL = 5, WL = 4, BL = 4

Writes Interrupted by a Write

Burst write can only be interrupted by another write with 4 bit burst boundary. Any other case of write interrupt is not allowed.

2.2.4.4 Burst Write Operation (cont'd)



NOTE 1 Write burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.

NOTE 2 Write burst of 8 can only be interrupted by another Write command. Write burst interruption by Read command or Precharge command is prohibited.

NOTE 3 Write burst interrupt must occur exactly two clocks after previous Write command. Any other Write burst interrupt timings are prohibited.

NOTE 4 Write burst interruption is allowed to any bank inside DRAM.

NOTE 5 Write burst with Auto Precharge enabled is not allowed to interrupt.

NOTE 6 Write burst interruption is allowed by another Write with Auto Precharge command.

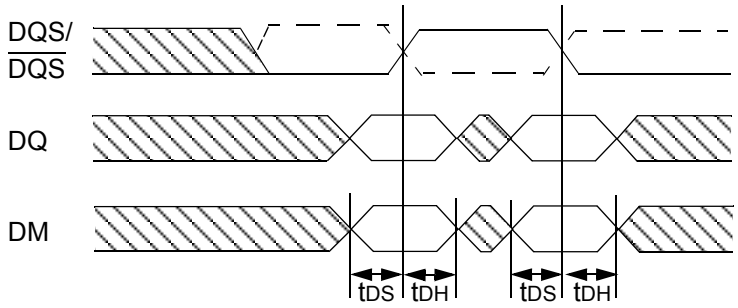
NOTE 7 All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, minimum Write to Precharge timing is WL+BL/2+tWR where tWR starts with the rising clock after the un-interrupted burst end and not from the end of actual burst end.

Figure 34 — Write Burst Interrupt Timing Example: (CL=3, AL=0, RL=3, WL=2, BL=8)

2.2.4.5 Write Data Mask

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR2 SDRAMs, consistent with the implementation on DDR SDRAMs. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to insure matched system timing. DM of x4 and x16 bit organization is not used during read cycles. However DM of x8 bit organization can be used as RDQS during read cycles by EMRS(1) setting.

Data Mask Timing



Data Mask Function, WL=3, AL=0, BL = 4 shown

Case 1: min t_{DQSS}

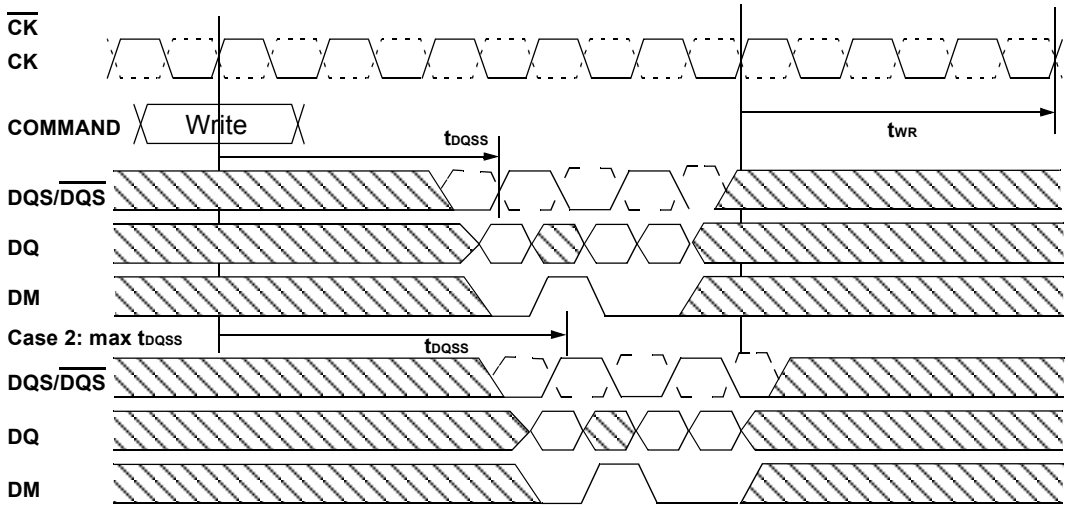


Figure 35 — Write Data Mask

2.2.5 Precharge Operation

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when CS, RAS and WE are low and CAS is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA0 and BA1 for 256Mb and 512Mb and four address bits A10, BA0 ~ BA2 for 1Gb and higher densities are used to define which bank to precharge when the command is issued. For 8 bank devices, refer to Section 2.2.3 of this data sheet.

2.2.5 Precharge Operation (cont'd)

Table 9 — Bank Selection for Precharge by Address Bits

A10	BA2	BA0	BA1	Precharged Bank(s)	Remarks
LOW	LOW	LOW	LOW	Bank 0 only	
LOW	LOW	LOW	HIGH	Bank 1 only	
LOW	LOW	HIGH	LOW	Bank 2 only	
LOW	LOW	HIGH	HIGH	Bank 3 only	
LOW	HIGH	LOW	LOW	Bank 4 only	1 Gb and higher
LOW	HIGH	LOW	HIGH	Bank 5 only	1 Gb and higher
LOW	HIGH	HIGH	LOW	Bank 6 only	1 Gb and higher
LOW	HIGH	HIGH	HIGH	Bank 7 only	1 Gb and higher
HIGH	DON'T CARE	DON'T CARE	DON'T CARE	All Banks	

2.2.5.1 Burst Read Operation Followed by Precharge

Minimum Read to precharge command spacing to the same bank = AL + BL/2 clocks
For the earliest possible precharge, the precharge command may be issued on the rising edge which is "Additive latency(AL) + BL/2 clocks" after a Read command. A new bank active (command) may be issued to the same bank after the RAS precharge time (t_{RP}). A precharge command cannot be issued until t_{RAS} is satisfied.

The minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read to Precharge command. This time is called tRTP (Read to Precharge). For BL = 4 this is the time from the actual read (AL after the Read command) to Precharge command. For BL = 8 this is the time from AL + 2 clocks after the Read to the Precharge command.

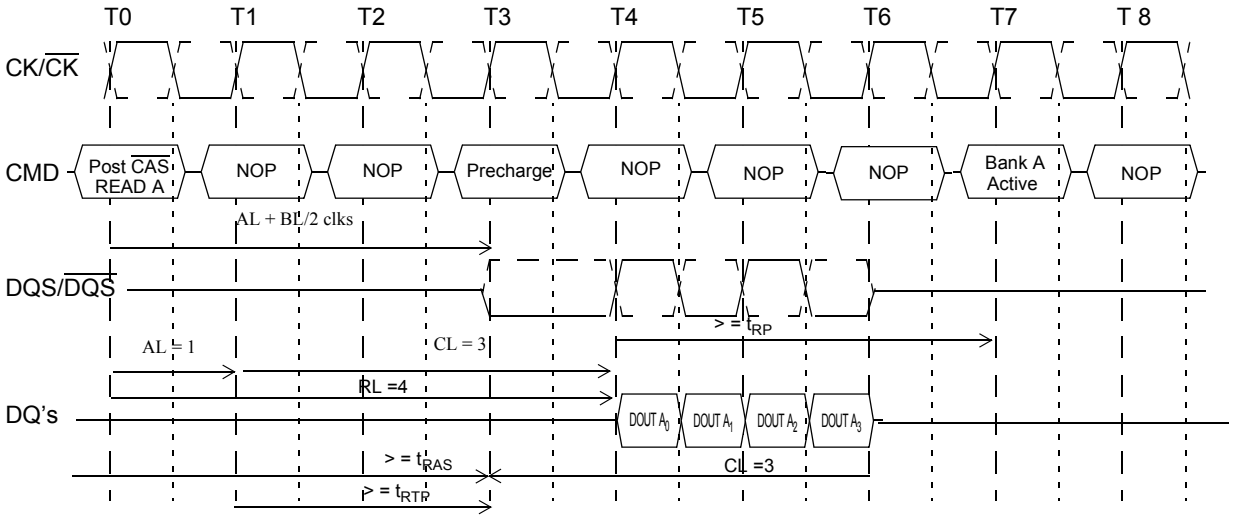


Figure 36 — Example 1: Burst Read Operation Followed by Precharge: RL = 4, AL = 1, CL = 3, BL = 4, t_{RTP} <= 2 clocks

2.2.5.1 Burst Read Operation Followed by Precharge (cont'd)

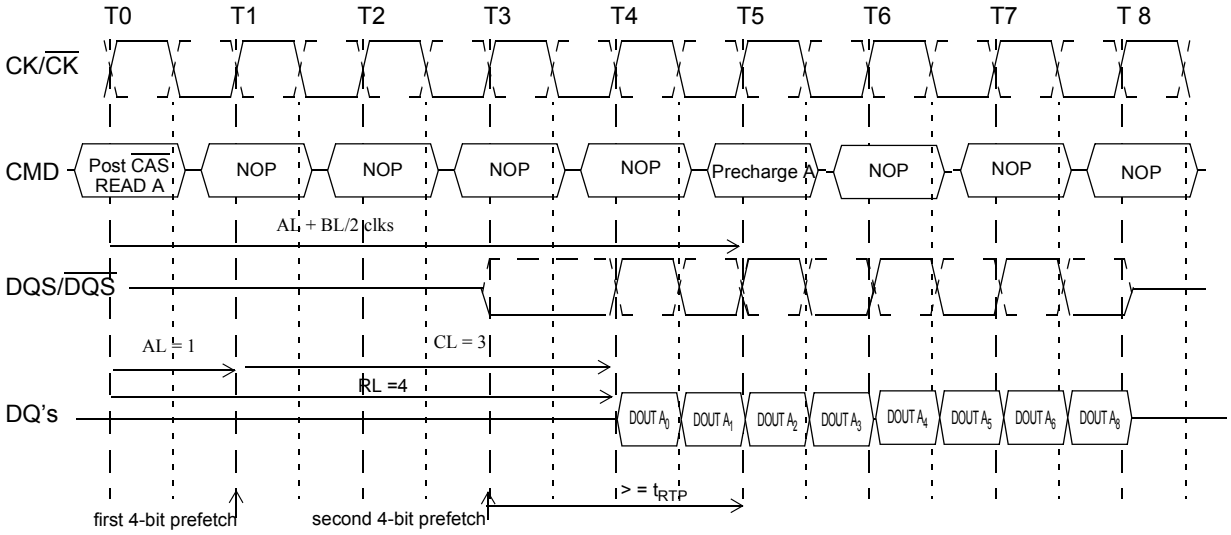


Figure 37 — Example 2: Burst Read Operation Followed by Precharge: RL = 4, AL = 1, CL = 3, BL = 8, t_{RTP} <= 2 clocks

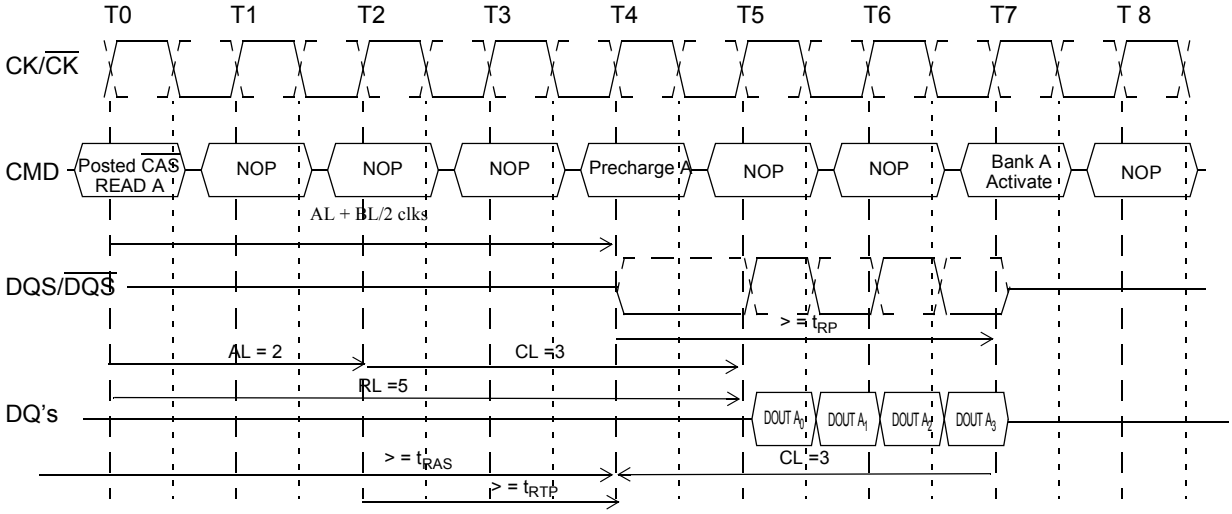


Figure 38 — Example 3: Burst Read Operation Followed by Precharge: RL = 5, AL = 2, CL = 3, BL = 4, t_{RTP} <= 2 clocks

2.2.5.1 Burst Read Operation Followed by Precharge (cont'd)

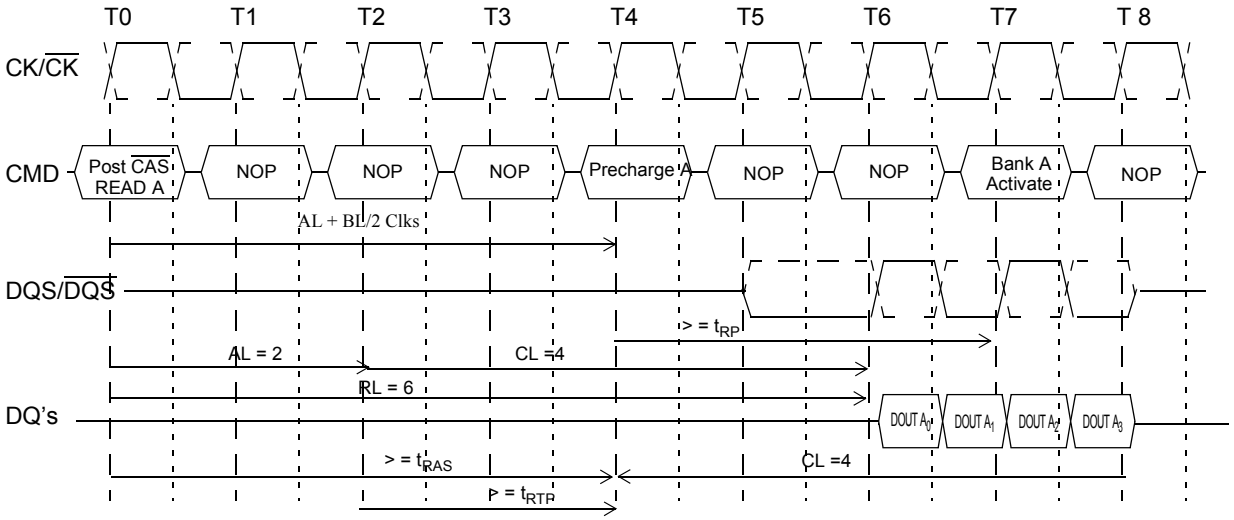
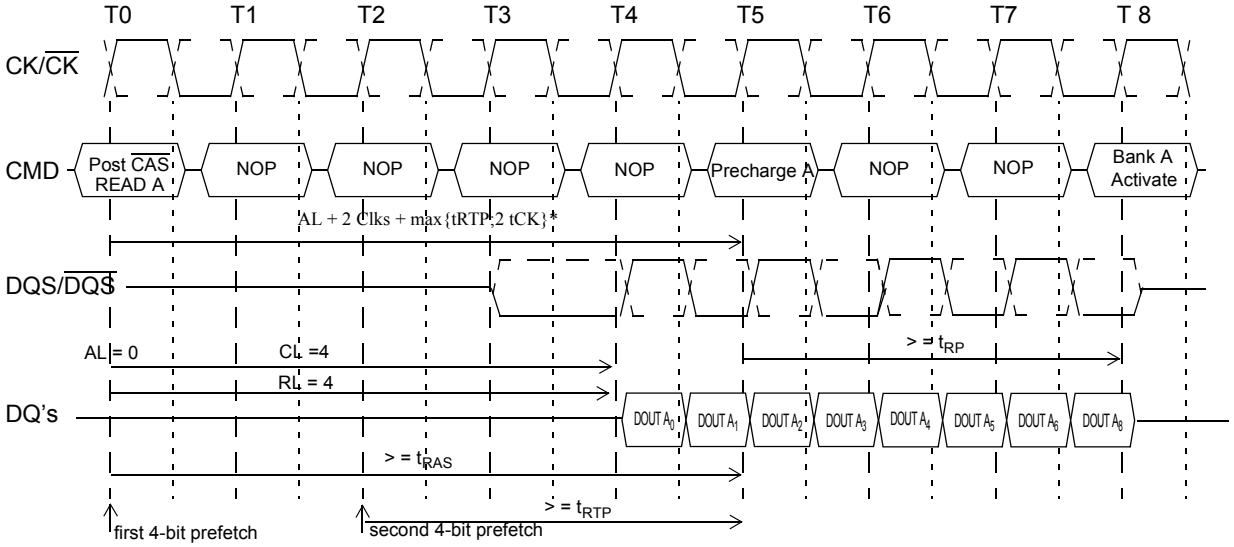


Figure 39 — Example 4: Burst Read Operation Followed by Precharge: RL = 6, AL = 2, CL = 4, BL = 4, t_{RTP} <= 2 clocks



*: rounded to next integer

Figure 40 — Example 5: Burst Read Operation Followed by Precharge: RL = 4, AL = 0, CL = 4, BL = 8, t_{RTP} > 2 clocks

2.2.5.2 Burst Write followed by Precharge

Minimum Write to Precharge Command spacing to the same bank = WL + BL/2 clks + tWR

For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge Command can be issued. This delay is known as a write recovery time (tWR) referenced from the completion of the burst write to the precharge command. No Precharge command should be issued prior to the tWR delay.

2.2.5.2 Burst Write followed by Precharge (cont'd)

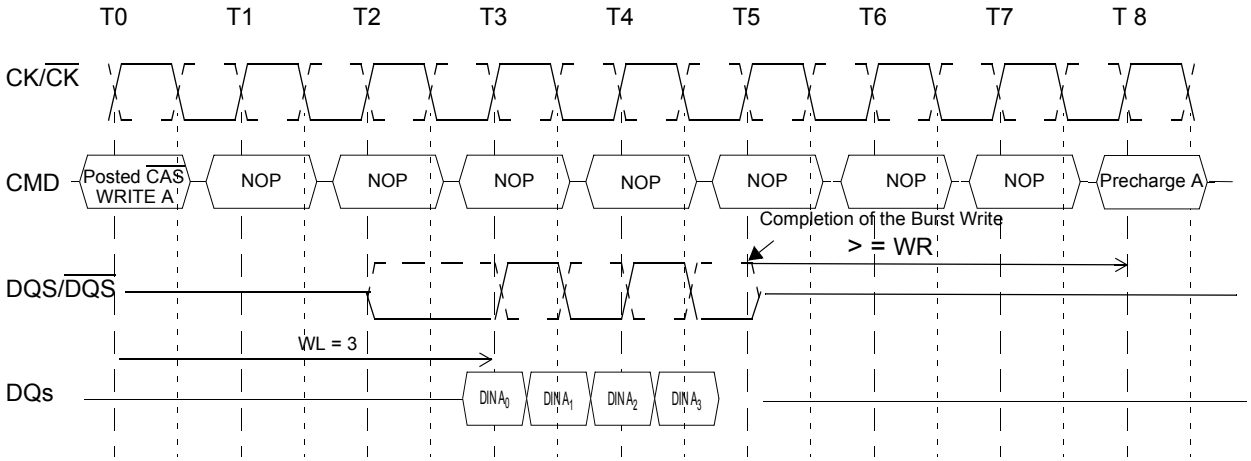


Figure 41 — Example 1: Burst Write followed by Precharge: WL = (RL-1) =3

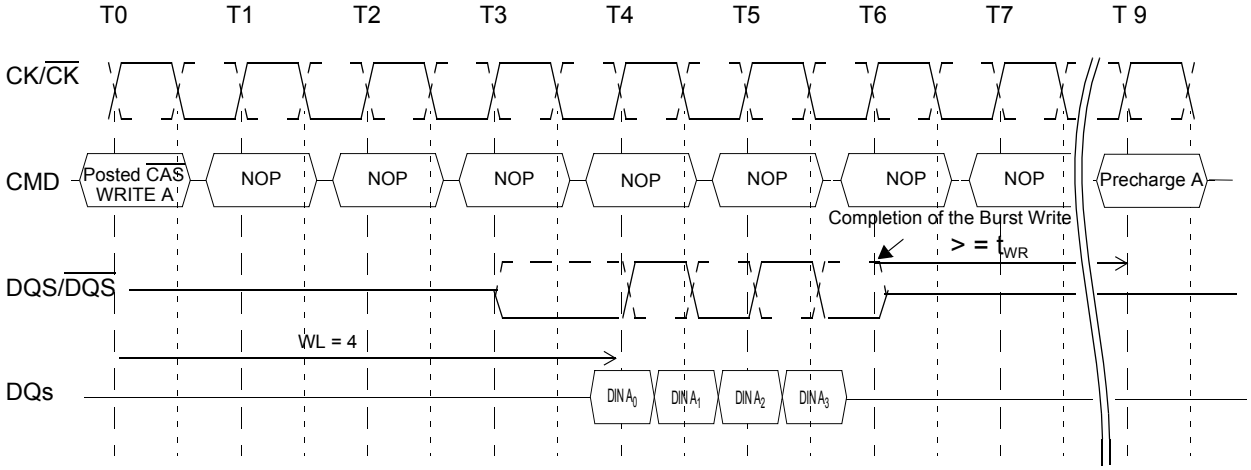


Figure 42 — Example 2: Burst Write followed by Precharge: WL = (RL-1) = 4

2.2.6 Auto Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is given to the DDR2 SDRAM, the $\overline{CAS}$ timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the READ or WRITE command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write command is issued, then the auto-precharge function is engaged. During auto-precharge, a Read command will execute as normal with the exception that the active bank will begin to precharge on the rising edge which is $\overline{CAS}$ latency (CL) clock cycles before the end of the read burst.

Auto-precharge is also implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.

2.2.6 Auto Precharge Operation (cont'd)

This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon $\overline{CAS}$ latency) thus improving system performance for random data access. The $\overline{RAS}$ lockout circuit internally delays the Precharge operation until the array restore operation has been completed (tRAS satisfied) so that the auto precharge command may be issued with any read or write command.

2.2.6.1 Burst Read with Auto Precharge

If A10 is high when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR2 SDRAM starts an Auto Precharge operation on the rising edge which is (AL + BL/2) cycles later than the read with AP command if tRAS(min) and tRTP(min) are satisfied.

If tRAS(min) is not satisfied at the edge, the start point of auto-precharge operation will be delayed until tRAS(min) is satisfied.

If tRTP(min) is not satisfied at the edge, the start point of auto-precharge operation will be delayed until tRTP(min) is satisfied.

In case the internal precharge is pushed out by tRTP, tRP starts at the point where the internal precharge happens (not at the next rising clock edge after this event). So for BL = 4 the minimum time from Read_AP to the next Activate command becomes AL + (tRTP + tRP)* (see example 2) for BL = 8 the time from Read_AP to the next Activate is AL + 2 + (tRTP + tRP)*, where "*" means: "rounded up to the next integer". In any event internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

A new bank activate (command) may be issued to the same bank if the following two conditions are satisfied simultaneously.
(1) The $\overline{RAS}$ precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
(2) The $\overline{RAS}$ cycle time (tRC) from the previous bank activation has been satisfied.

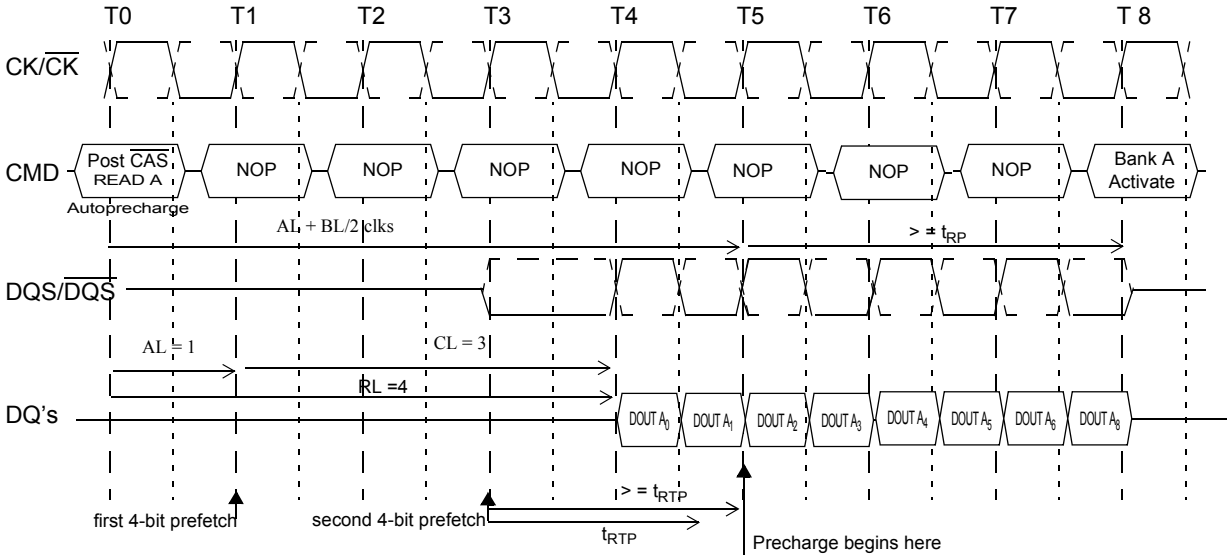


Figure 43 — Example 1: Burst Read Operation with Auto Precharge: RL = 4, AL = 1, CL = 3, BL = 8, t_{RTP} <= 2 clocks

2.2.6.1 Burst Read with Auto Precharge (cont'd)

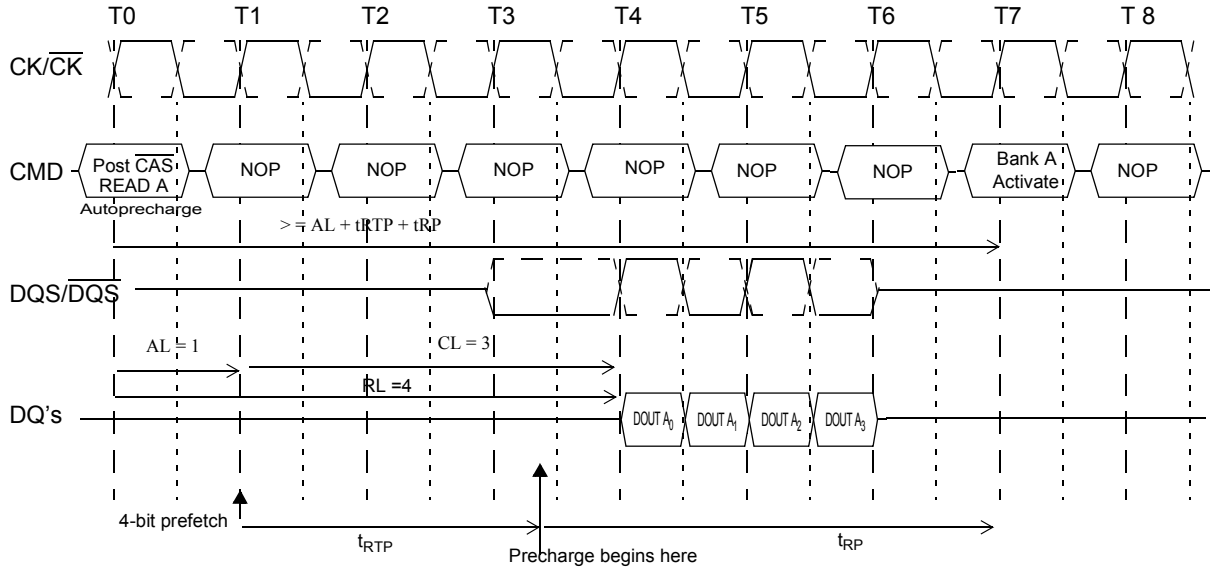


Figure 44 — Example 2: Burst Read Operation with Auto Precharge: RL = 4, AL = 1, CL = 3, BL = 4, t_{RTP} > 2 clocks

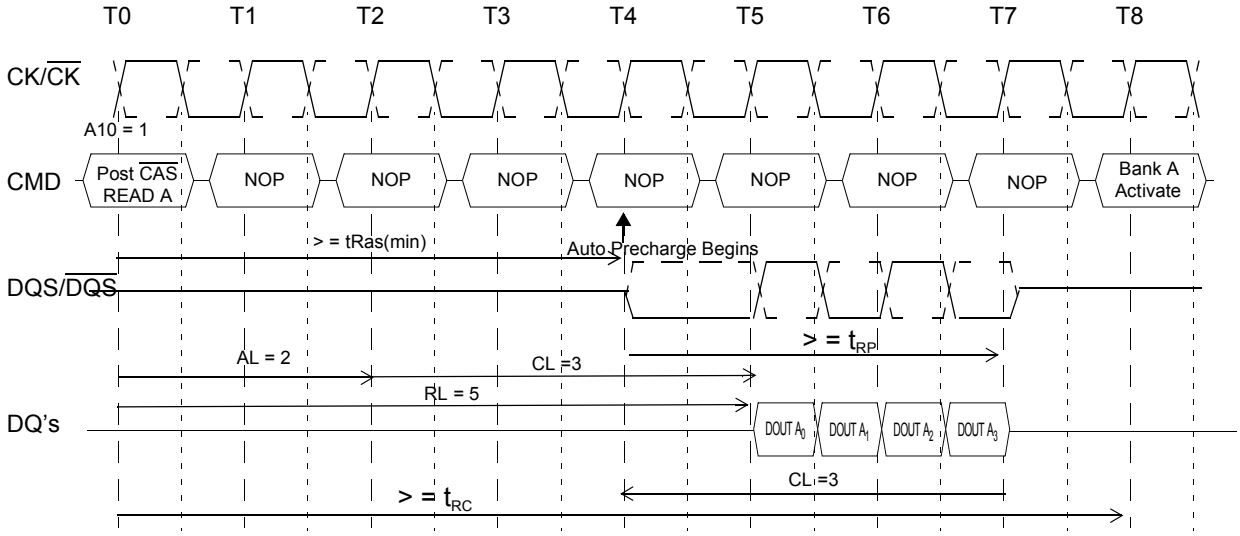


Figure 45 — Example 3: Burst Read with Auto Precharge Followed by an Activation to the Same Bank(tRC Limit): RL = 5 (AL = 2, CL = 3, internal tRCD = 3, BL = 4, t_{RTP} <= 2 clocks)

2.2.6.1 Burst Read with Auto Precharge (cont'd)

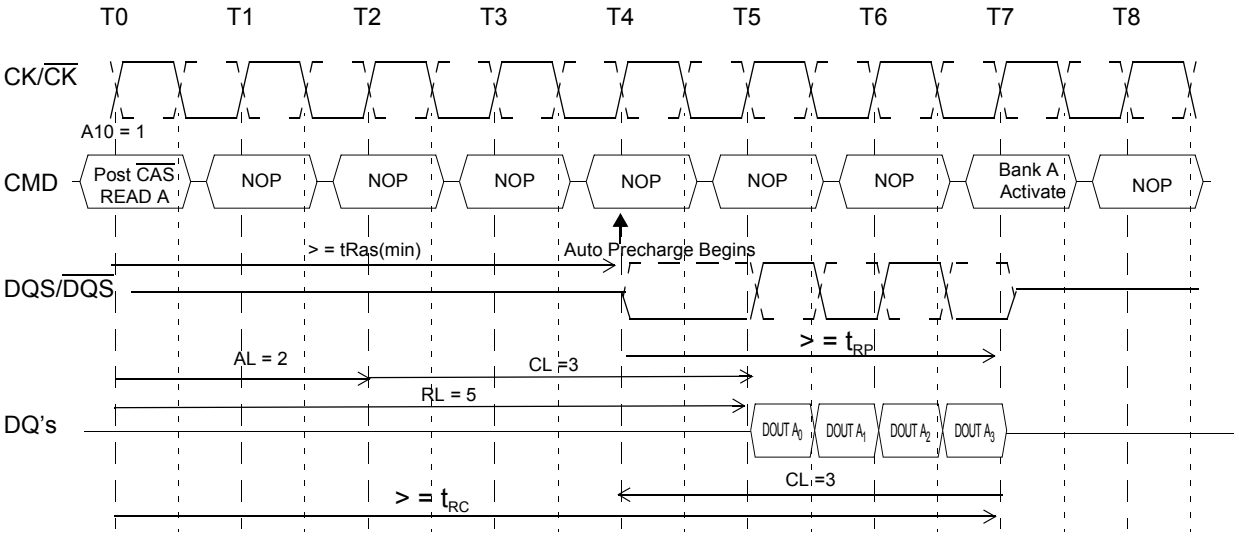


Figure 46 — Example 4: Burst Read with Auto Precharge Followed by an Activation to the Same Bank (tRP Limit): RL = 5 (AL = 2, CL = 3, internal tRCD = 3, BL = 4, t_{RTP} <= 2 clocks)

2.2.6.2 Burst Write with Auto-Precharge

If A10 is high when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the burst write plus write recovery time (tWR). The bank undergoing auto-precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

1) The data-in to bank activate delay time (WR + tRP) has been satisfied.
2) The RAS cycle time (tRC) from the previous bank activation has been satisfied.

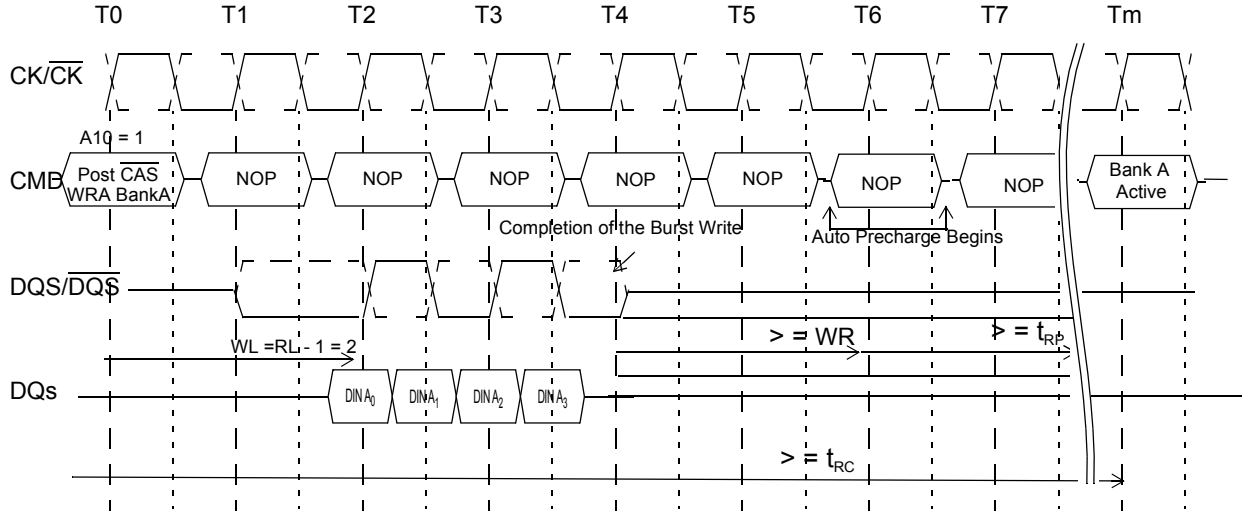


Figure 47 — Burst Write with Auto-Precharge (tRC Limit): WL = 2, tWR =2, BL = 4, tRP=3

2.2.6.2 Burst Write with Auto-Precharge (cont'd)

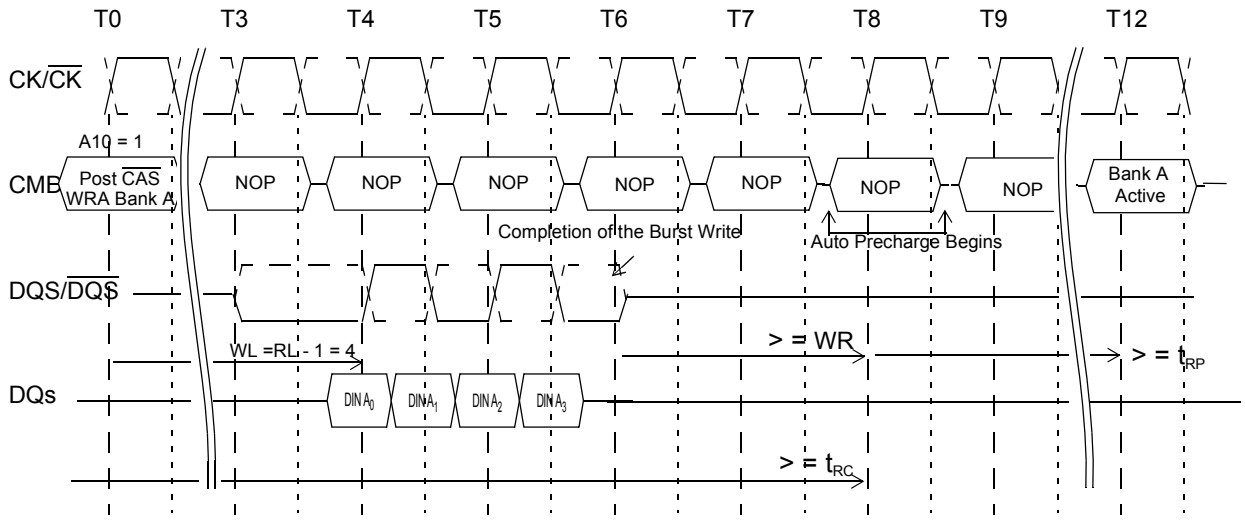


Figure 48 — Burst Write with Auto-Precharge (tWR + tRP): WL = 4, tWR =2, BL = 4, tRP=3

2.2.7 Refresh Command

When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held low and $\overline{WE}$ high at the rising edge of the clock, the chip enters the Refresh mode (REF). All banks of the DDR2 SDRAM must be precharged and idle for a minimum of the Precharge time (tRP) before the Refresh command (REF) can be applied. An address counter, internal to the device, supplies the bank address during the refresh cycle. No control of the external address bus is required once this cycle has started.
When the refresh cycle has completed, all banks of the DDR2 SDRAM will be in the precharged (idle) state. A delay between the Refresh command (REF) and the next Activate command or subsequent Refresh command must be greater than or equal to the Refresh cycle time (tRFC).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 * tREFI.

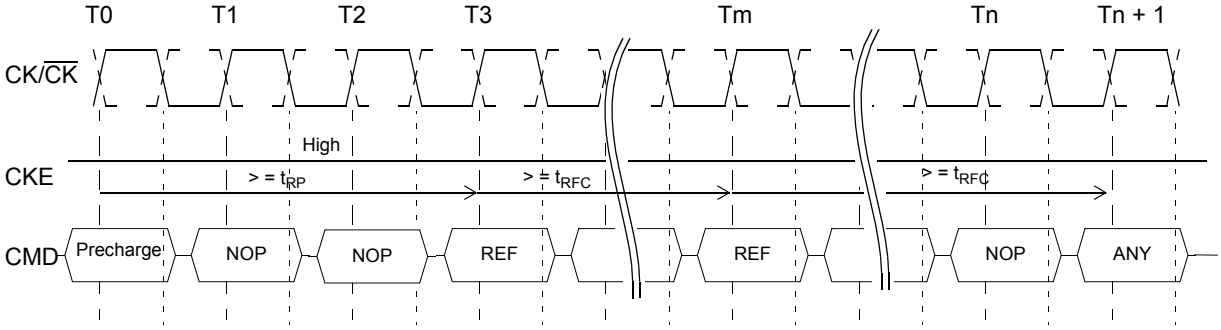
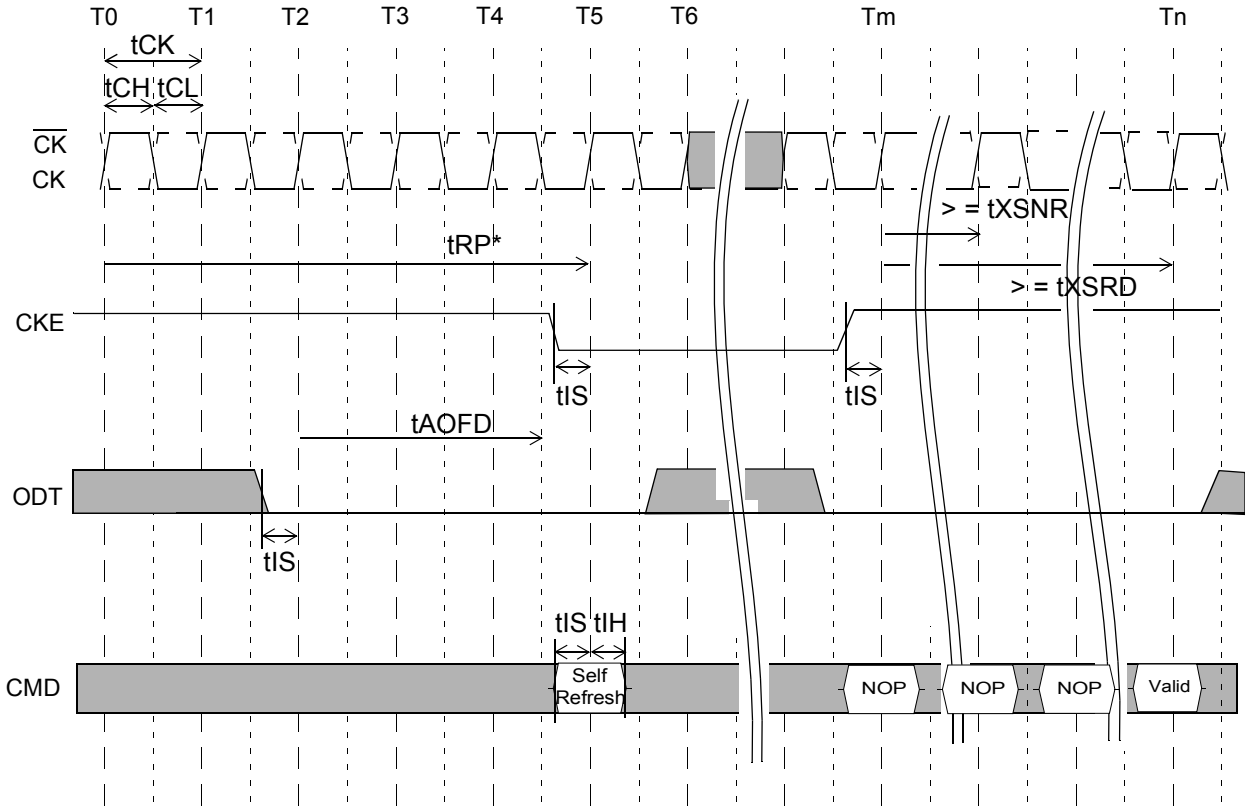


Figure 49 — Refresh Command

2.2.8 Self Refresh Operation

The DDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. ODT must be turned off before issuing Self Refresh command, by either driving ODT pin low or using EMRS command. Once the Command is registered, CKE must be held low to keep the device in Self Refresh mode. When the DDR2 SDRAM has entered Self Refresh mode all of the external signals except CKE, are “don’t care”. The clock is internally disabled during Self Refresh Operation to save power. The user may change the external clock frequency or halt the external clock one clock after Self-Refresh entry is registered, however, the clock must be restarted and stable before the device can exit Self Refresh operation. Once Self Refresh Exit command is registered, a delay equal to or longer than the tXSNR or tXSRD must be satisfied before a valid command can be issued to the device. CKE must remain high for the entire Self Refresh exit period tXSRD for proper operation. NOP or deselect commands must be registered on each positive clock edge during the Self Refresh exit interval. ODT should also be turned off during tXSRD.



- Device must be in the “All banks idle” state prior to entering Self Refresh mode.
- ODT must be turned off tAOFD before entering Self Refresh mode, and can be turned on again when tXSRD timing is satisfied.
- tXSRD is applied for a Read or a Read with autoprecharge command
- tXSNR is applied for any command except a Read or a Read with autoprecharge command.

Figure 50 — Self Refresh Operation

2.2.9 Power-Down

Power-down is synchronously entered when CKE is registered low (along with Nop or Deselect command). CKE is not allowed to go low while mode register or extended mode register command time, or read or write operation is in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or autoprecharge, or auto-refresh is in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in Figures 51 through 59 with details for entry into power down.

The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation.

If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$, ODT and CKE. Also the DLL is disabled upon entering precharge power-down or slow exit active power-down, but the DLL is kept enabled during fast exit active power-down. In power-down mode, CKE low and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and ODT should be in a valid state but all other input signals are “Don’t Care”. CKE low must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a Nop or Deselect command). CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP, tXARD, or tXARDS, after CKE goes high. Power-down exit latency is defined at AC spec table of this data sheet.

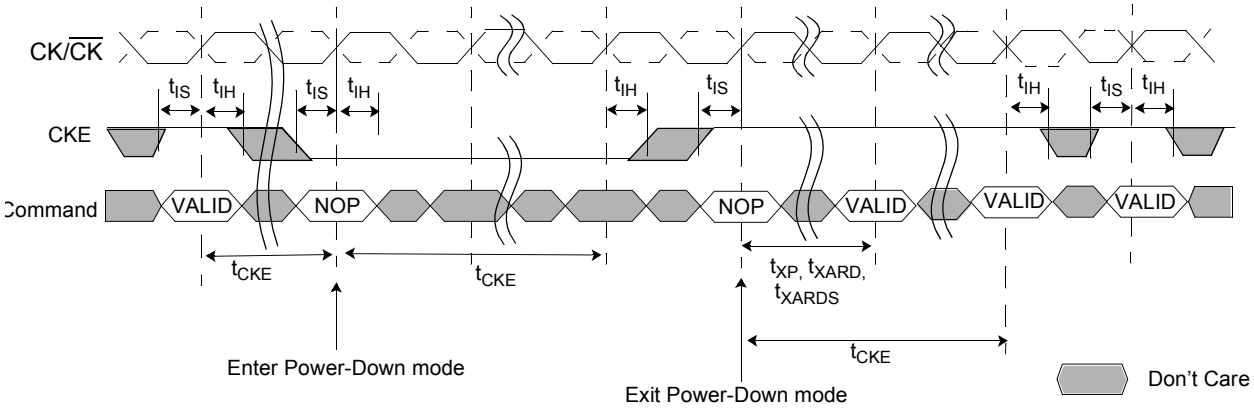


Figure 51 — Basic Power Down Entry and Exit Timing Diagram

2.2.9 Power-Down (cont'd)

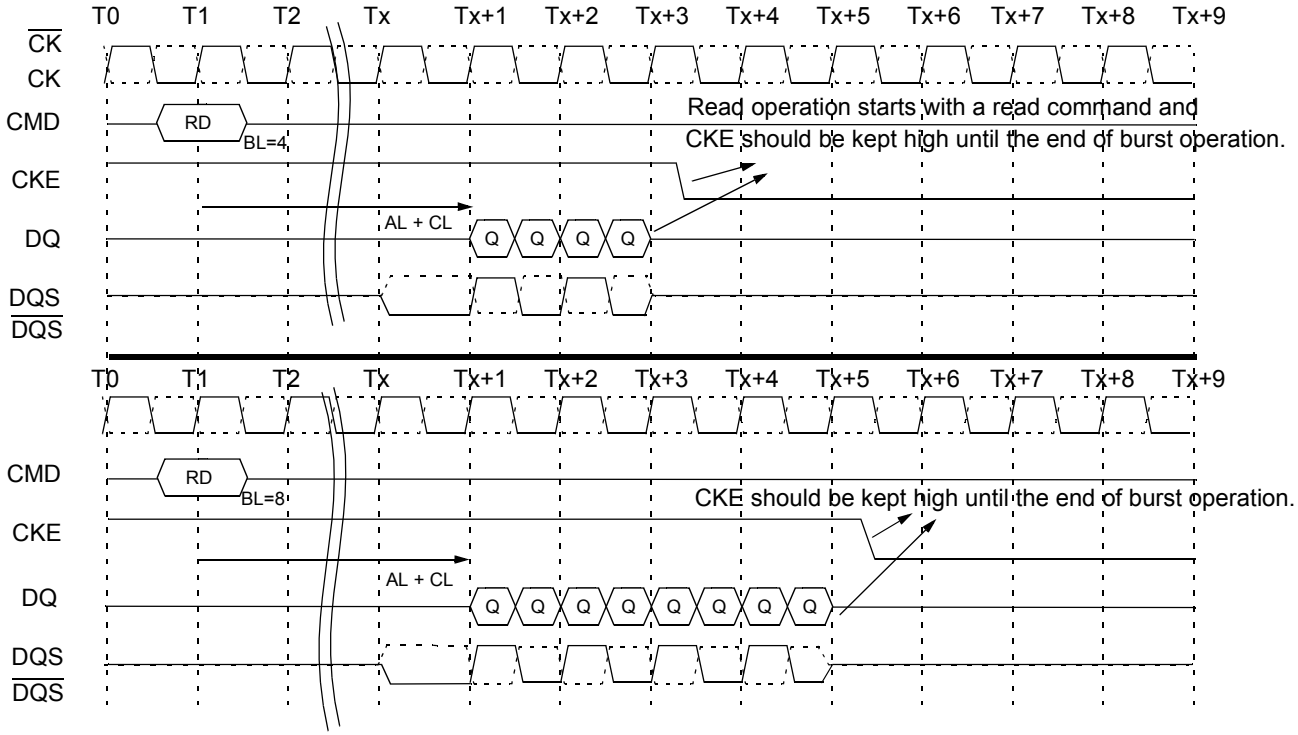


Figure 52 — Read to Power Down Entry

2.2.9 Power-Down (cont'd)

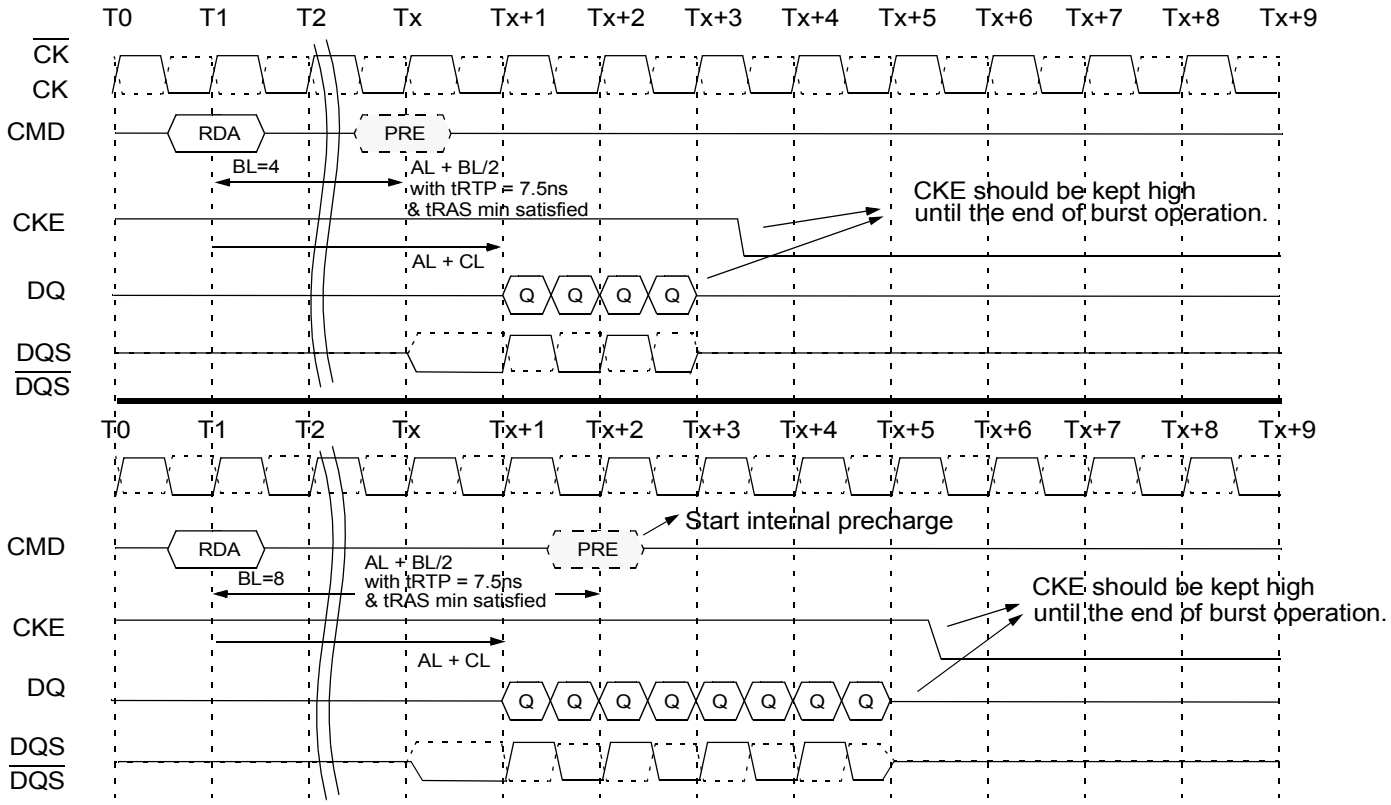


Figure 53 — Read with Autoprecharge to Power Down Entry

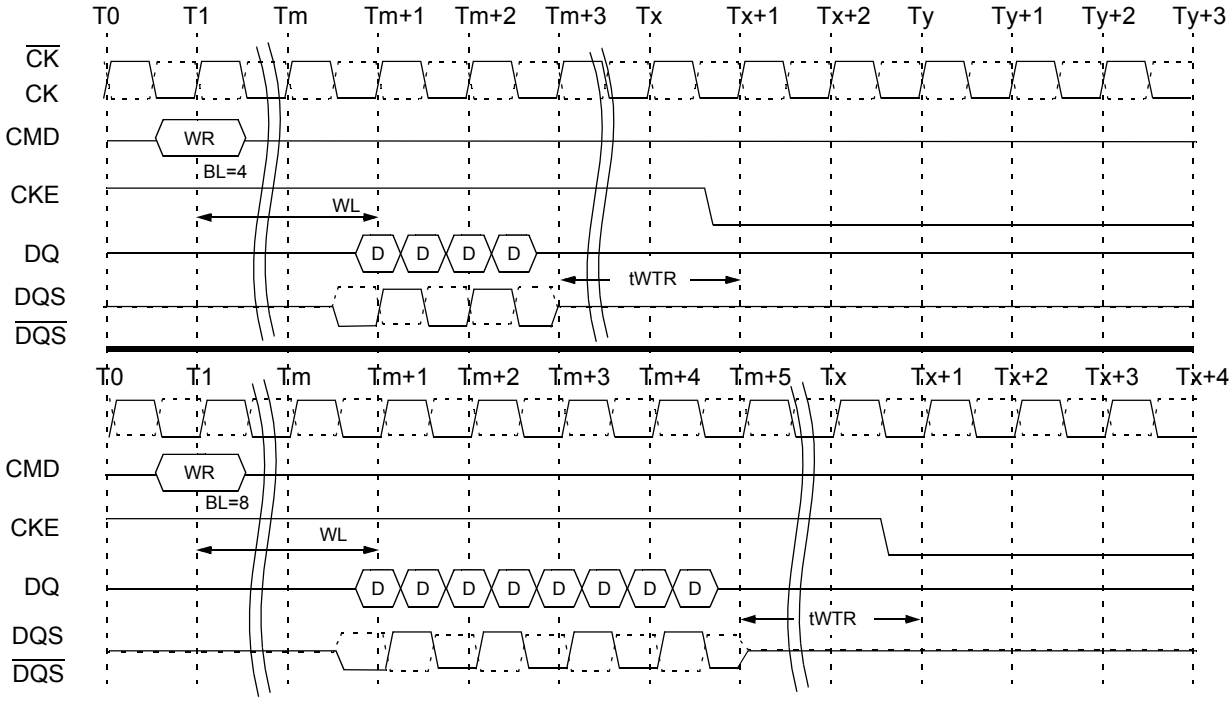


Figure 54 — Write to Power Down Entry

2.2.9 Power-Down (cont'd)

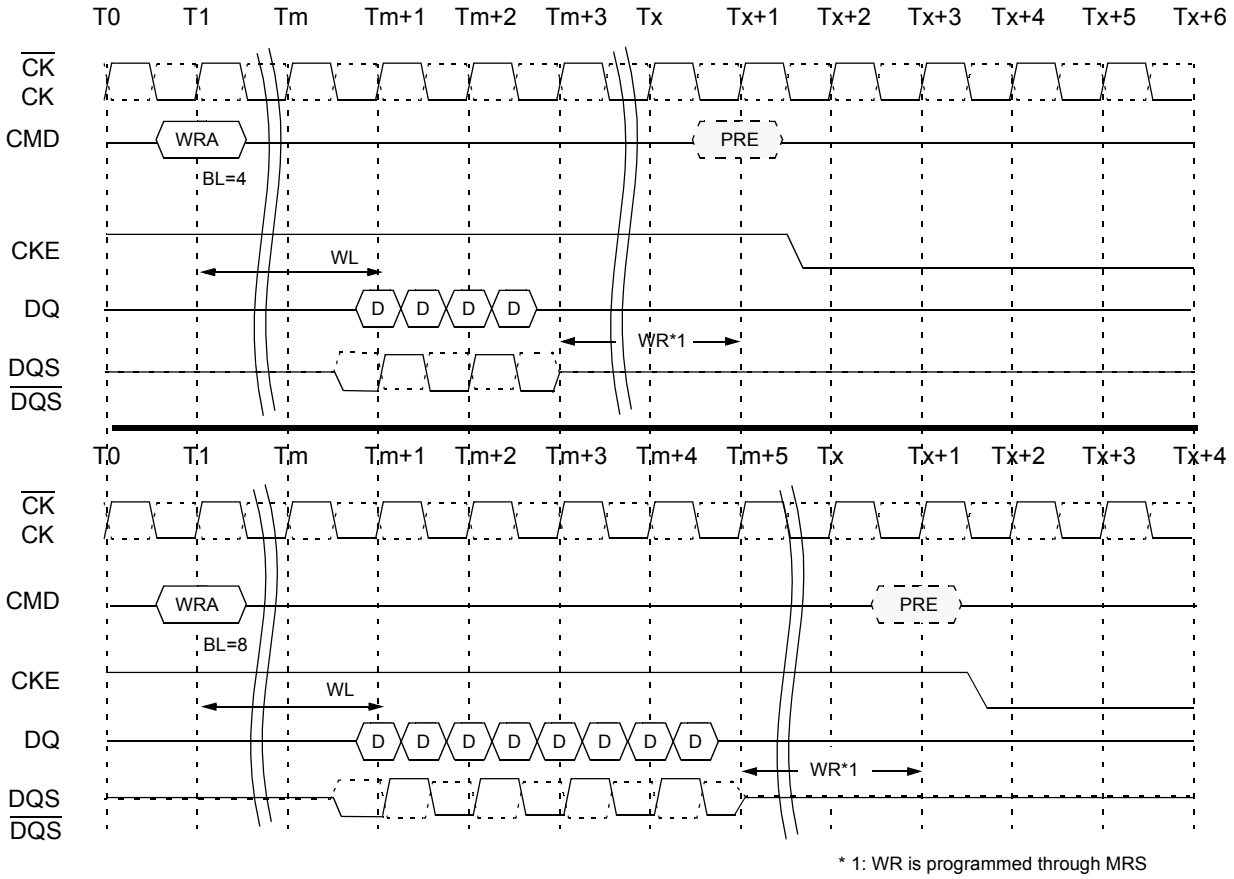


Figure 55 — Write with Autoprecharge to Power Down Entry

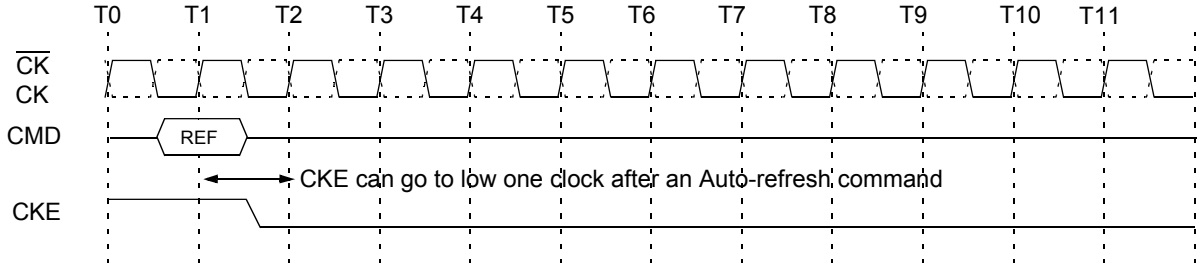


Figure 56 — Refresh Command to Power Down Entry

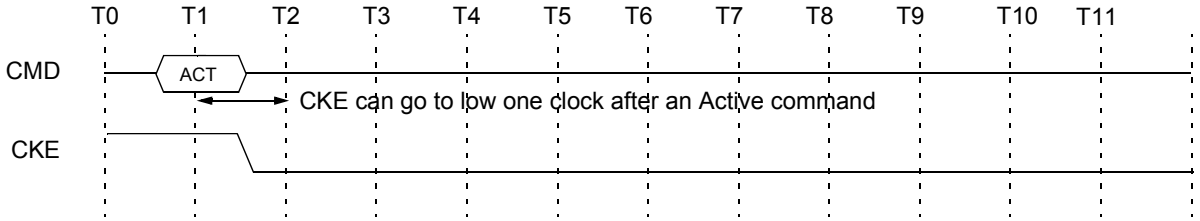


Figure 57 — Active Command to Power Down Entry

2.2.9 Power-Down (cont'd)

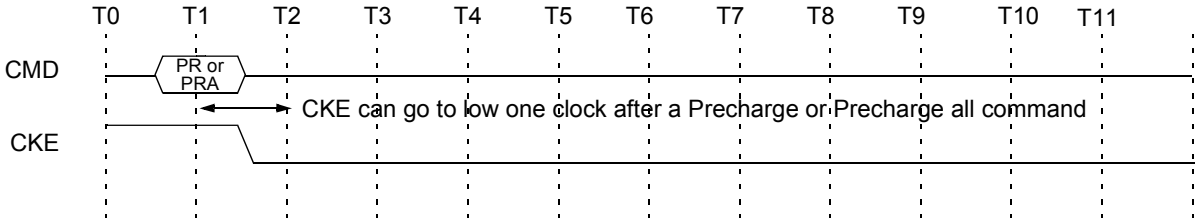


Figure 58 — Precharge/Precharge all Command to Power Down Entry

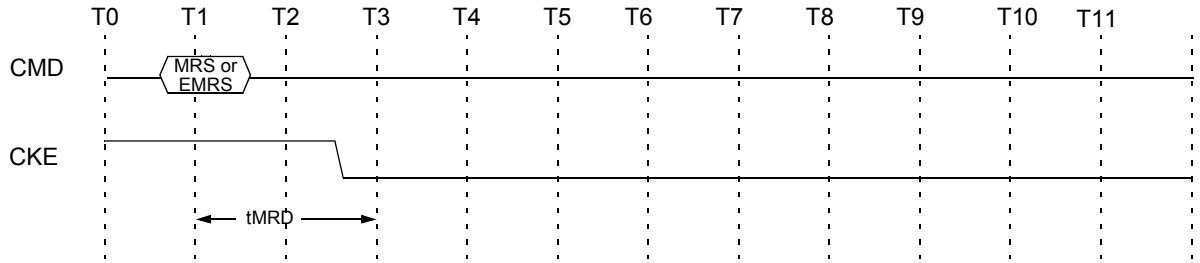


Figure 59 — MRS/EMRS Command to Power Down Entry

2.2.10 Asynchronous CKE Low Event

DRAM requires CKE to be maintained "HIGH" for all valid operations as defined in this data sheet. If CKE asynchronously drops "LOW" during any valid operation DRAM is not guaranteed to preserve the contents of array. If this event occurs, memory controller must satisfy DRAM timing specification tDelay before turning off the clocks. Stable clocks must exist at the input of DRAM before CKE is raised "HIGH" again. DRAM must be fully re-initialized (steps 4 thru 13) as described in initialization sequence. DRAM is ready for normal operation after the initialization sequence. See Table 35 for tDelay specification.

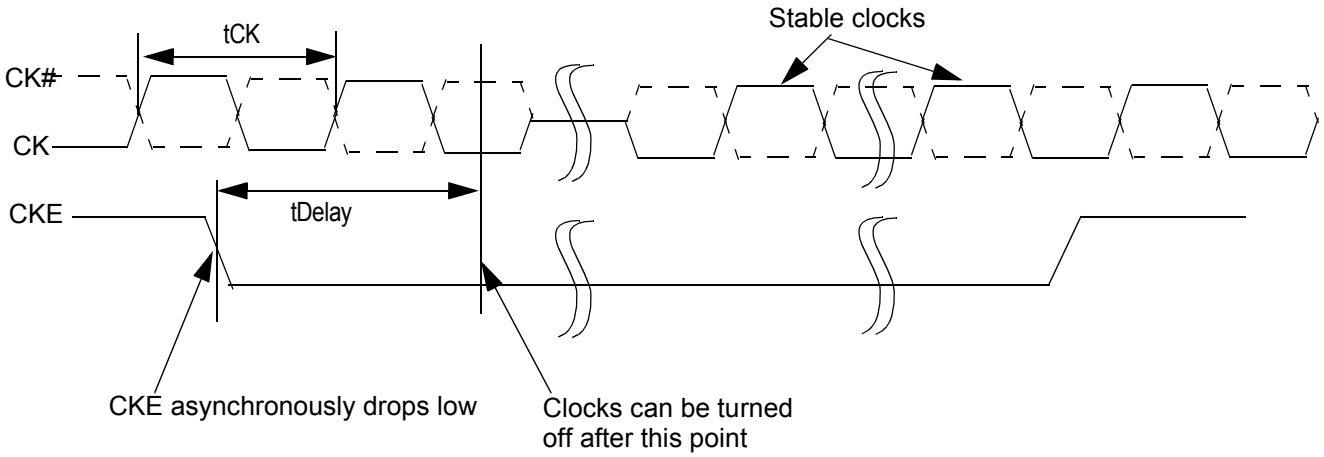


Figure 60 — Asynchronous CKE Low Event

2.2.11 Input Clock Frequency Change during Precharge Power Down

DDR2 SDRAM input clock frequency can be changed under following condition:

DDR2 SDRAM is in precharged power down mode. ODT must be turned off and CKE must be at logic LOW level. A minimum of 2 clocks must be waited after CKE goes LOW before clock frequency may change. SDRAM input clock frequency is allowed to change only within minimum and maximum operating frequency specified for the particular speed grade. During input clock frequency change, ODT and CKE must be held at stable LOW levels. Once input clock frequency is changed, stable new clocks must be provided to DRAM before precharge power down may be exited and DLL must be RESET via EMRS after precharge power down exit. Depending on new clock frequency an additional MRS command may need to be issued to appropriately set the WR, CL etc. During DLL re-lock period, ODT must remain off. After the DLL lock time, the DRAM is ready to operate with new clock frequency.

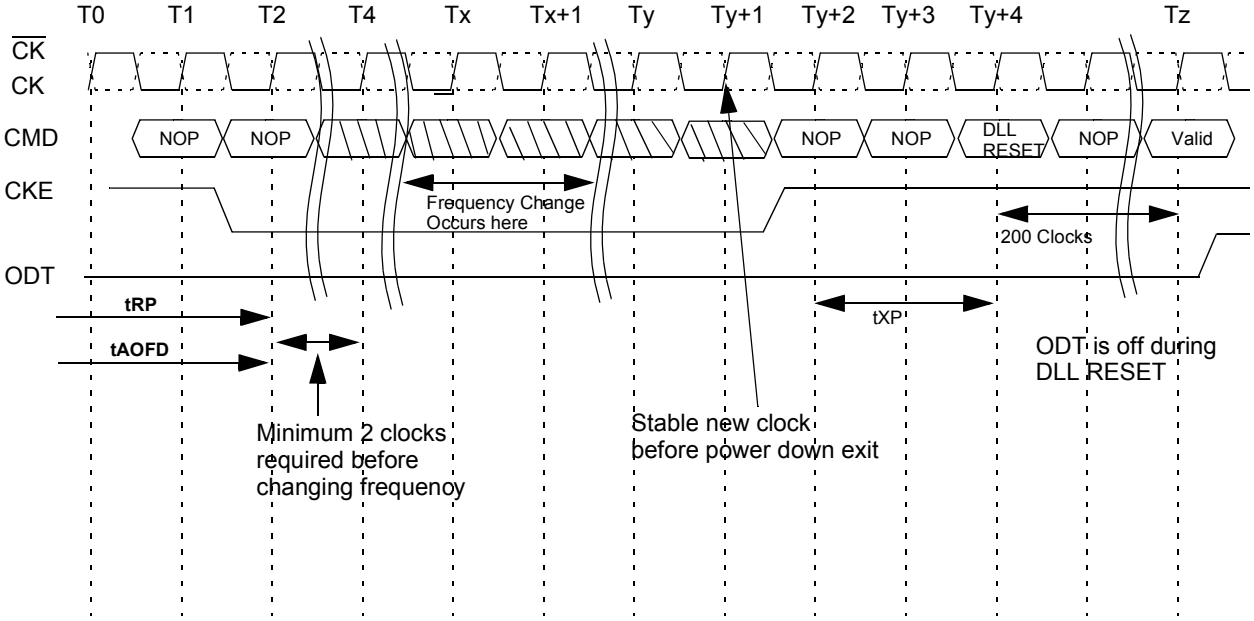


Figure 61 — Clock Frequency Change in Precharge Power

2.2.12 No Operation Command

The No Operation command should be used in cases when the DDR2 SDRAM is in an idle or a wait state. The purpose of the No Operation command (NOP) is to prevent the DDR2 SDRAM from registering any unwanted commands between operations. A No Operation command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ held high at the rising edge of the clock. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

2.2.13 Deselect Command

The Deselect command performs the same function as a No Operation command. Deselect command occurs when $\overline{CS}$ is brought high at the rising edge of the clock, the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals become don't cares.

3 Truth Tables

Table 10 — Command truth table.

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1,2
Refresh (REF)	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1,7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.

NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

NOTE 3 Burst reads or writes at BL=4 cannot be terminated or interrupted. See sections "Reads interrupted by a Read" and "Writes interrupted by a Write" in section 2.2.4 for details.

NOTE 4 The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined in section 2.2.7.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See section 2.2.2.4.

NOTE 6 “X” means “H or L (but a defined logic level)”.

NOTE 7 Self refresh exit is asynchronous.

3 Truth Tables (cont'd)

Table 11 — Clock Enable (CKE) Truth Table for Synchronous Transitions

Current State [2]	CKE		Command (N) [3]	Action (N) [3]	Notes
	Previous Cycle[1] (N-1)	Current Cycle[1] (N)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$		
Power Down	L	L	X	Maintain Power-Down	11, 13, 15
	L	H	DESELECT or NOP	Power Down Exit	4, 8, 11,13
Self Refresh	L	L	X	Maintain Self Refresh	11, 15
	L	H	DESELECT or NOP	Self Refresh Exit	4, 5,9
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	4,8,10,11,13
All Banks Idle	H	L	DESELECT or NOP	Precharge Power Down Entry	4, 8, 10,11,13
	H	L	REFRESH	Self Refresh Entry	6, 9, 11,13
	H	H	Refer to the Command Truth Table		7

NOTE 1 CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.

NOTE 2 Current state is the state of the DDR SDRAM immediately prior to clock edge N.

NOTE 3 COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N).

NOTE 4 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

NOTE 5 On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the t_{XSNR} period. Read commands may be issued only after t_{XSRD} (200 clocks) is satisfied.

NOTE 6 Self Refresh mode can only be entered from the All Banks Idle state.

NOTE 7 Must be a legal command as defined in the Command Truth Table.

NOTE 8 Valid commands for Power Down Entry and Exit are NOP and DESELECT only.

NOTE 9 Valid commands for Self Refresh Exit are NOP and DESELECT only.

NOTE 10 Power Down and Self Refresh can not be entered while Read or Write operations, (Extended) Mode Register Set operations or Precharge operations are in progress. See section 2.2.9 "Power Down" and 2.2.8 "Self Refresh Command" for a detailed list of restrictions.

NOTE 11 Minimum CKE high time is three clocks.; minimum CKE low time is three clocks.

NOTE 12 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See section 2.2.2.4.

NOTE 13 The Power Down does not perform any refresh operations. The duration of Power Down Mode is therefore limited by the refresh requirements outlined in section 2.2.7.

NOTE 14 CKE must be maintained high while the SDRAM is in OCD calibration mode.

NOTE 15 "X" means "don't care (including floating around VREF)" in Self Refresh and Power Down. However ODT must be driven high or low in Power Down if the ODT function is enabled (Bit A2 or A6 set to "1" in EMRS(1)).

Table 12 — DM Truth Table

Name (Functional)	DM	DQs	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

NOTE 1 Used to mask write data, provided coincident with the corresponding data

4 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 1.0 V ~ 2.3 V	V	1
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
VDDL	Voltage on VDDL pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1

NOTE 1 Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5 AC & DC Operating Conditions

Table 13 — Recommended DC Operating Conditions (SSTL_1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	4
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	4, 5
VDD	Supply Voltage	2.3	2.5	2.7	V	4, 6
VDDL	Supply Voltage for DLL	2.3	2.5	2.7	V	4, 5, 6
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	5, 6
VREF	Input Reference Voltage	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	mV	1.2
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04	V	3

NOTE 1 There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.

NOTE 2 The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically, the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.

NOTE 3 Peak to peak ac noise on VREF may not exceed +/-2% VREF (dc).

NOTE 4 VTT of transmitting device must track VREF of receiving device.

NOTE 5 DDR2 parts with 2.5 V Vdd may exist in the market, but devices with 1.8 V Vdd are expected to be the preferred mass production parts

NOTE 6 VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDDL tied together

NOTE 7 Note 5 does not apply when Vdd = 2.5 V nominal

5 AC & DC Operating Conditions (cont'd)

Table 14 — ODT DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
Rtt effective impedance value for EMRS(A6,A2)=0,1; 75 ohm	Rtt1(eff)	60	75	90	ohm	1
Rtt effective impedance value for EMRS(A6,A2)=1,0; 150 ohm	Rtt2(eff)	120	150	180	ohm	1
Deviation of VM with respect to VDDQ/2	delta VM	-3.75		+3.75	%	1

NOTE 1 Test condition for Rtt measurements

Measurement Definition for Rtt(eff): Apply V_{IH} (ac) and V_{IL} (ac) to test pin separately, then measure current I(V_{IH} (ac)) and I(V_{IL} (ac)) respectively. V_{IH} (ac), V_{IL} (ac), and VDDQ values defined in SSTL_18

$$\text{Rtt(eff)} = \frac{V_{IH}(ac) - V_{IL}(ac)}{I(V_{IH}(ac)) - I(V_{IL}(ac))}$$

Measurement Definition for VM: Measure voltage (VM) at test pin (midpoint) with no load.

$$\text{delta VM} = \left(\frac{2 \times Vm}{VDDQ} - 1\right) \times 100\%$$

Table 15 — Input DC Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH}(dc)	dc input logic high	VREF + 0.125	VDDQ + 0.3	V	
V_{IL}(dc)	dc input logic low	- 0.3	VREF - 0.125	V	

Table 16 — Input AC Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH} (ac)	ac input logic high	VREF + 0.250	-	V	
V_{IL} (ac)	ac input logic low	-	VREF - 0.250	V	

Table 17 — AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 * V_{DDQ}	V	1
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

NOTE 1 Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test.
NOTE 2 The input signal minimum slew rate is to be maintained over the range from $V_{IL(dc)}$ max to $V_{IH(ac)}$ min for rising edges and the range from $V_{IH(dc)}$ min to $V_{IL(ac)}$ max for falling edges as shown in the below figure.
NOTE 3 AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.

5 AC & DC Operating Conditions (cont'd)

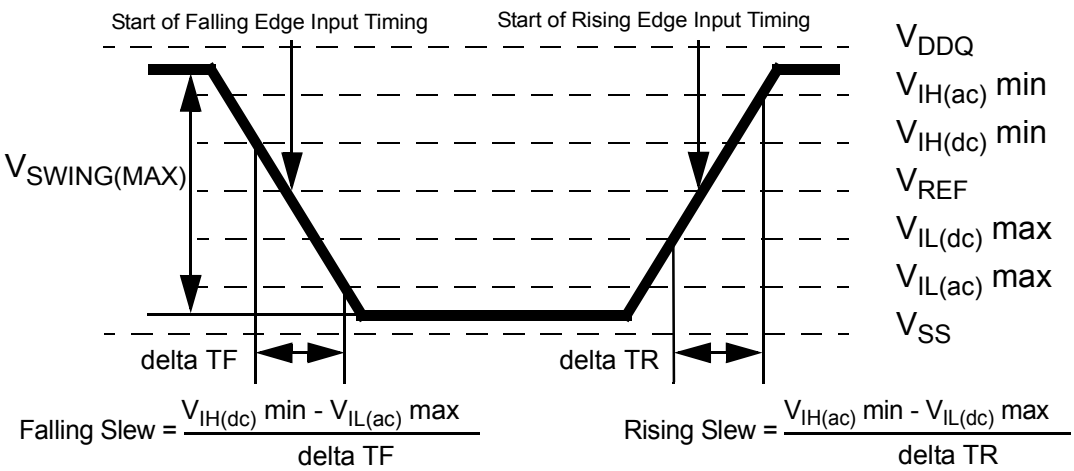


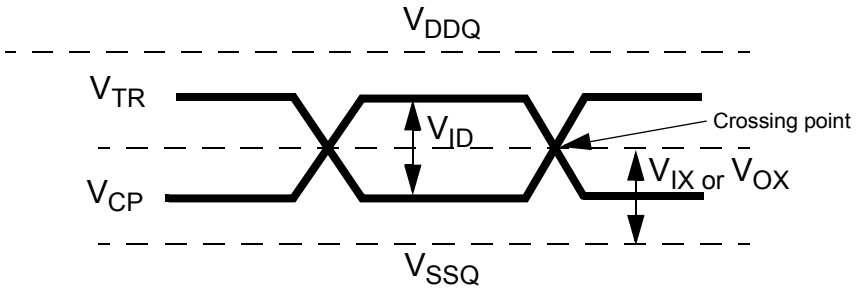
Figure 62 — AC Input Test Signal Waveform

Table 18 — Differential Input AC logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{ID} (ac)	ac differential input voltage	0.5	VDDQ + 0.6	V	1
V_{IX} (ac)	ac differential cross point voltage	0.5 * VDDQ - 0.175	0.5 * VDDQ + 0.175	V	2

NOTE 1 VIN(DC) specifies the allowable DC execution of each input of differential pair such as CK, $\overline{CK}$, DQS, $\overline{DQS}$, LDQS, $\overline{LDQS}$, UDQS and $\overline{UDQS}$.

NOTE 2 VID(DC) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input (such as CK, DQS, LDQS or UDQS) level and VCP is the complementary input (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$) level. The minimum value is equal to VIH(DC) - V IL(DC).



NOTE 1 VID(AC) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input signal (such as CK, DQS, LDQS or UDQS) and VCP is the complementary input signal (such as CK, DQS, LDQS or UDQS). The minimum value is equal to V IH(AC) - V IL(AC).

NOTE 2 The typical value of VIX(AC) is expected to be about 0.5 * VDDQ of the transmitting device and VIX(AC) is expected to track variations in VDDQ. VIX(AC) indicates the voltage at which differential input signals must cross.

Figure 63 — Differential signal levels

5 AC & DC Operating Conditions (cont'd)

Table 19 — Differential AC output parameters

Symbol	Parameter	Min.	Max.	Units	Notes
V_{OX} (ac)	ac differential cross point voltage	0.5 * VDDQ - 0.125	0.5 * VDDQ + 0.125	V	1

NOTE 1 The typical value of VOX(AC) is expected to be about 0.5 * V DDQ of the transmitting device and VOX(AC) is expected to track variations in VDDQ. VOX(AC) indicates the voltage at which differential output signals must cross.

Overshoot/Undershoot Specification

Table 20 — AC Overshoot/Undershoot Specification for Address and Control Pins A0-A15, BA0-BA2, CS, RAS, CAS, WE, CKE, ODT

Parameter	Specification		
	DDR2-400	DDR2-533	DDR2-667
Maximum peak amplitude allowed for overshoot area (See Figure 64):	0.9V	0.9V	0.9V
Maximum peak amplitude allowed for undershoot area (See Figure 64):	0.9V	0.9V	0.9V
Maximum overshoot area above VDD (See Figure 64).	0.75 V-ns	0.56 V-ns	0.45 V-ns
Maximum undershoot area below VSS (See Figure 64).	0.75 V-ns	0.56 V-ns	0.45 V-ns

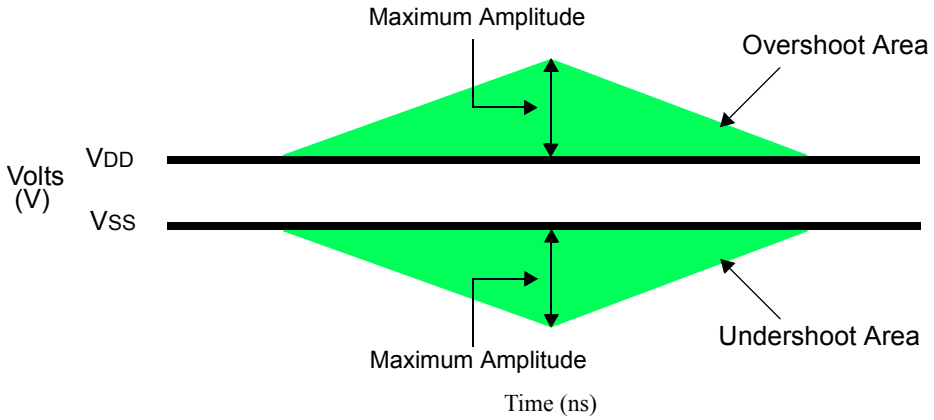


Figure 64 — AC Overshoot and Undershoot Definition for Address and Control Pins

Table 21 — AC Overshoot/Undershoot Specification for Clock, Data, Strobe, and Mask Pins DQ, DQS, DM, CK, CK

Parameter	Specification		
	DDR2-400	DDR2-533	DDR2-667
Maximum peak amplitude allowed for overshoot area (See Figure 65):	0.9V	0.9V	0.9V
Maximum peak amplitude allowed for undershoot area (See Figure 65):	0.9V	0.9V	0.9V
Maximum overshoot area above VDDQ (See Figure 65).	0.38 V-ns	0.28 V-ns	0.23 V-ns
Maximum undershoot area below VSSQ (See Figure 65).	0.38 V-ns	0.28 V-ns	0.23 V-ns

5 AC & DC Operating Conditions (cont'd)

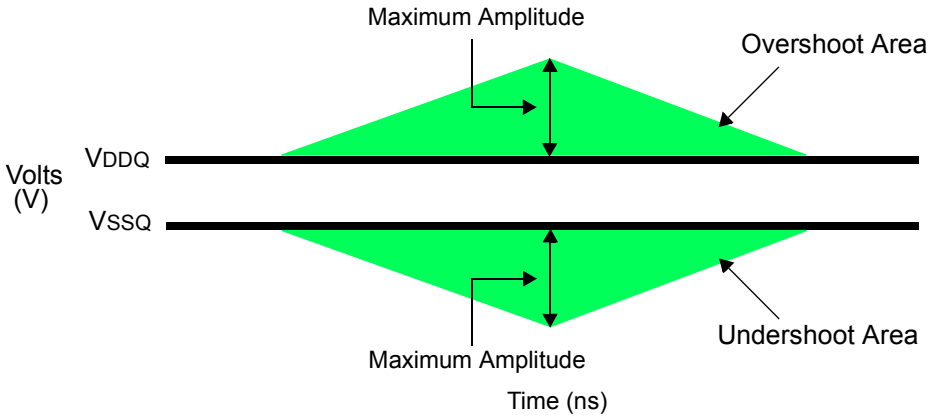


Figure 65 — AC Overshoot and Undershoot Definition for Clock, Data, Strobe, and Mask Pins

Power and ground clamps are required on the following input only pins:

1. BA0-BA2
2. A0-A15
3. $\overline{RAS}$
4. $\overline{CAS}$
5. $\overline{WE}$
6. $\overline{CS}$
7. ODT
8. CKE

Table 22 — Characteristics for Input Only Pins with Clamps

Voltage across clamp (V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0	0
0.1	0	0
0.2	0	0
0.3	0	0
0.4	0	0
0.5	0	0
0.6	0	0
0.7	0	0
0.8	0.1	0.1
0.9	1.0	1.0
1.0	2.5	2.5
1.1	4.7	4.7
1.2	6.8	6.8
1.3	9.1	9.1
1.4	11.0	11.0
1.5	13.5	13.5
1.6	16.0	16.0
1.7	18.2	18.2
1.8	21.0	21.0

5 AC & DC Operating Conditions (cont'd)

Output Buffer Levels

Table 23 — Output AC Test Conditions

Symbol	Parameter	SSTL_18 Class II	Units	Notes
V_{OH}	Minimum Required Output Pull-up under AC Test Load	V_{TT} + 0.603	V	
V_{OL}	Maximum Required Output Pull-down under AC Test Load	V_{TT} - 0.603	V	
V_{OTR}	Output Timing Measurement Reference Level	0.5 * V_{DDQ}	V	1

NOTE 1 The VDDQ of the device under test is referenced.

Table 24 — Output DC Current Drive

Symbol	Parameter	SSTI_18 Class II	Units	Notes
$I_{OH(dc)}$	Output Minimum Source DC Current	- 13.4	mA	1, 3, 4
$I_{OL(dc)}$	Output Minimum Sink DC Current	13.4	mA	2, 3, 4

NOTE 1 V_{DDQ} = 1.7 V; V_{OUT} = 1420 mV. (V_{OUT} - V_{DDQ})/I_{OH} must be less than 21 ohm for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280 mV.

NOTE 2 V_{DDQ} = 1.7 V; V_{OUT} = 280 mV. V_{OUT}/I_{OL} must be less than 21 ohm for values of V_{OUT} between 0 V and 280 mV.

NOTE 3 The dc value of V_{REF} applied to the receiving device is set to V_{TT}

NOTE 4 The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} min plus a noise margin and V_{IL} max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see Table 12) along a 21 ohm load line to define a convenient driver current for measurement.

Table 25 — OCD Default Characteristics

Description	Parameter	Min	Nom	Max	Unit	Notes
Output impedance		12.6	18	23.4	ohms	1,2
Pull-up and pull-down mismatch		0		4	ohms	1,2,3
Output slew rate		tbd		tbd	V/ns	1,4,5

NOTE 1 Absolute Specifications (0°C £ TCASE £ +tbd°C; VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V)

NOTE 2 Impedance measurement condition for output source dc current: VDDQ = 1.7V; VOUT = 1420mV; (VOUT-VDDQ)/Ioh must be less than 23.4 ohms for values of VOUT between VDDQ and VDDQ-280mV. Impedance measurement condition for output sink dc current: VDDQ = 1.7V; VOUT = 280mV; VOUT/Iol must be less than 23.4 ohms for values of VOUT between 0V and 280mV.

NOTE 3 Mismatch is absolute value between pull-up and pull-down, both are measured at same temperature and voltage.

NOTE 4 Slew rate measured from vil(ac) to vih(ac).

NOTE 5 The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.

5 AC & DC Operating Conditions (cont'd)

DDR2 SDRAM Default Output Driver V–I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength default operation as selected by the EMRS1 bits A7-A9 = '111'. Figures 66 and 67 show the driver characteristics graphically, while Tables 26 and 27 show the same data in tabular format suitable for input into simulation tools. The driver characteristics evaluation conditions are:

- Nominal Default 25 ^{o}C (T case), VDDQ = 1.8 V, typical process
- Minimum TBD ^{o}C (T case), VDDQ = 1.7 V, slow–slow process
- Maximum 0 ^{o}C (T case), VDDQ = 1.9 V, fast–fast process

Default Output Driver Characteristic Curves Notes:

1. The full variation in driver current from minimum to maximum process, temperature, and voltage will lie within the outer bounding lines of the V–I curve of the Figures.
2. It is recommended that the "typical" IBIS V–I curve lie within the inner bounding lines of the V–I curves of the Figures.

Table 26 — Full Strength Default Pulldown Driver Characteristics

	Pulldown Current (mA)			
Voltage (V)	Minimum (23.4 Ohms)	Nominal Default Low (18 ohms)	Nominal Default High (18 ohms)	Maximum (12.6 Ohms)
0.2	8.5	11.3	11.8	15.9
0.3	12.1	16.5	16.8	23.8
0.4	14.7	21.2	22.1	31.8
0.5	16.4	25.0	27.6	39.7
0.6	17.8	28.3	32.4	47.7
0.7	18.6	30.9	36.9	55.0
0.8	19.0	33.0	40.9	62.3
0.9	19.3	34.5	44.6	69.4
1.0	19.7	35.5	47.7	75.3
1.1	19.9	36.1	50.4	80.5
1.2	20.0	36.6	52.6	84.6
1.3	20.1	36.9	54.2	87.7
1.4	20.2	37.1	55.9	90.8
1.5	20.3	37.4	57.1	92.9
1.6	20.4	37.6	58.4	94.9
1.7	20.6	37.7	59.6	97.0
1.8		37.9	60.9	99.1
1.9				101.1

5 AC & DC Operating Conditions (cont'd)

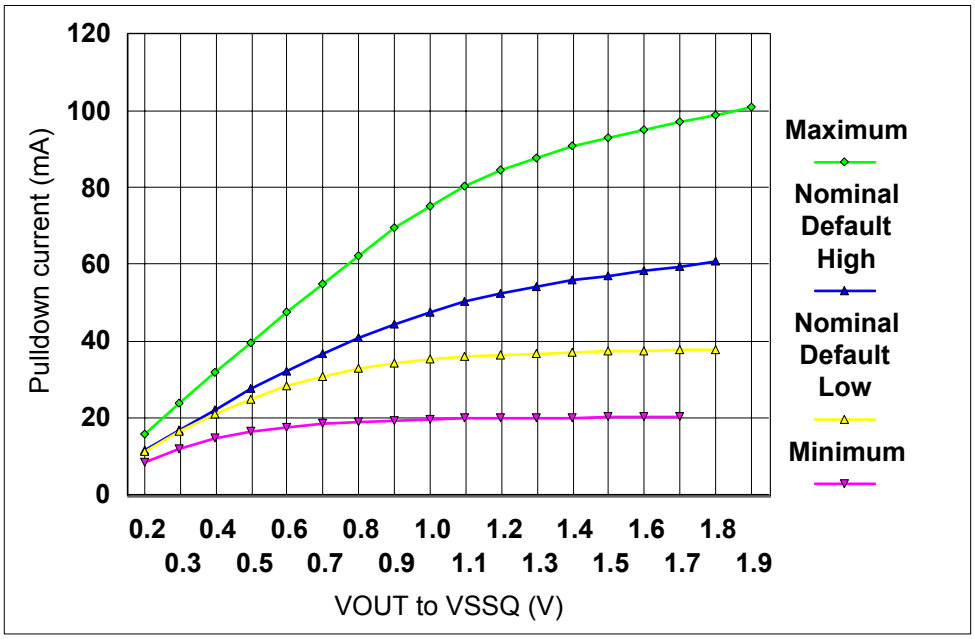


Figure 66 — DDR2 Default Pulldown Characteristics for Full Strength Driver

Table 27 — Full Strength Default Pullup Driver Characteristics

	Pullup Current (mA)			
Voltage (V)	Minimum (23.4 Ohms)	Nominal Default Low (18 ohms)	Nominal Default High (18 ohms)	Maximum (12.6 Ohms)
0.2	-8.5	-11.1	-11.8	-15.9
0.3	-12.1	-16.0	-17.0	-23.8
0.4	-14.7	-20.3	-22.2	-31.8
0.5	-16.4	-24.0	-27.5	-39.7
0.6	-17.8	-27.2	-32.4	-47.7
0.7	-18.6	-29.8	-36.9	-55.0
0.8	-19.0	-31.9	-40.8	-62.3
0.9	-19.3	-33.4	-44.5	-69.4
1.0	-19.7	-34.6	-47.7	-75.3
1.1	-19.9	-35.5	-50.4	-80.5
1.2	-20.0	-36.2	-52.5	-84.6
1.3	-20.1	-36.8	-54.2	-87.7
1.4	-20.2	-37.2	-55.9	-90.8
1.5	-20.3	-37.7	-57.1	-92.9
1.6	-20.4	-38.0	-58.4	-94.9
1.7	-20.6	-38.4	-59.6	-97.0
1.8		-38.6	-60.8	-99.1
1.9				-101.1

5 AC & DC Operating Conditions (cont'd)

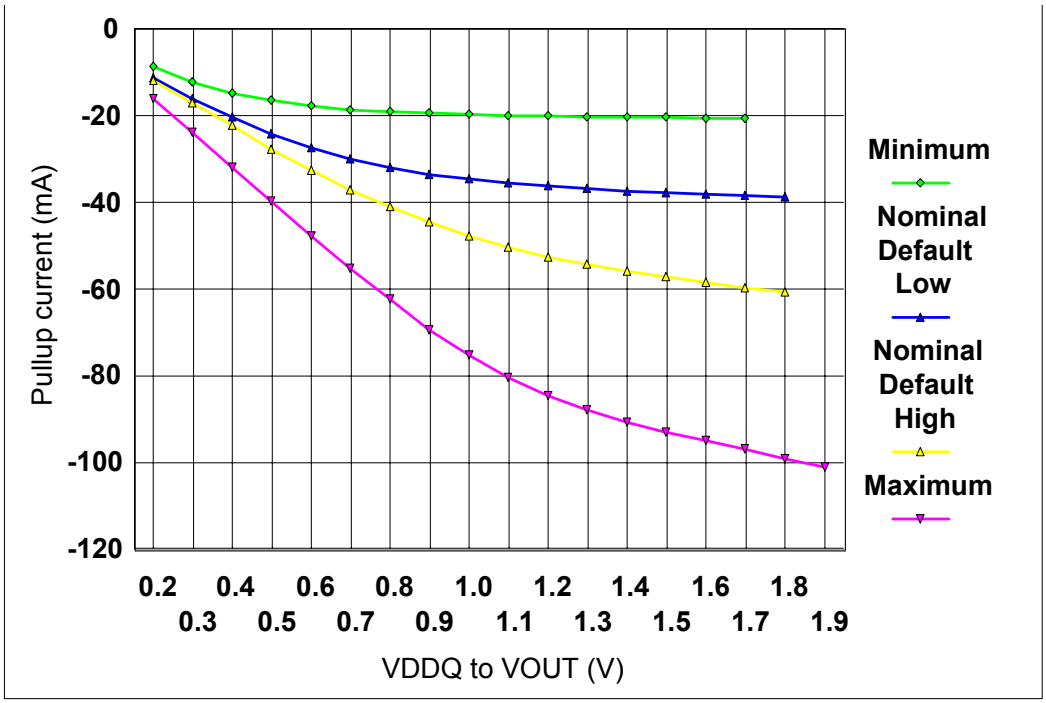


Figure 67 — DDR2 Default Pullup Characteristics for Full Strength Output Driver

DDR2 SDRAM Calibrated Output Driver V–I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength calibrated operation as selected by the procedure outlined in Section 2.2.2.3, Off-Chip Driver (OCD) Impedance Adjustment. Tables 28 and 29 show the data in tabular format suitable for input into simulation tools. The nominal points represent a device at exactly 18 ohms. The nominal low and nominal high values represent the range that can be achieved with a maximum 1.5 ohm step size with no calibration error at the exact nominal conditions only (i.e., perfect calibration procedure, 1.5 ohm maximum step size guaranteed by specification). Real system calibration error needs to be added to these values. It must be understood that these V-I curves as represented here or in supplier IBIS models need to be adjusted to a wider range as a result of any system calibration error. Since this is a system specific phenomena, it cannot be quantified here. The values in the calibrated tables represent just the DRAM portion of uncertainty while looking at one DQ only. If the calibration procedure is used, it is possible to cause the device to operate outside the bounds of the default device characteristics tables and figures. In such a situation, the timing parameters in the specification cannot be guaranteed. It is solely up to the system application to ensure that the device is calibrated between the minimum and maximum default values at all times. If this can't be guaranteed by the system calibration procedure, re-calibration policy, and uncertainty with DQ to DQ variation, then it is recommended that only the default values be used. The nominal maximum and minimum values represent the change in impedance from nominal low and high as a result of voltage and temperature change from the nominal condition to the maximum and minimum conditions. If calibrated at an extreme condition, the amount of variation could be as much as from the nominal minimum to the nominal maximum or vice versa. The driver characteristics evaluation conditions are:

- Nominal 25 ^{o}C (T case), VDDQ = 1.8 V, typical process
- Nominal Low and Nominal High 25 ^{o}C (T case), VDDQ = 1.8 V, any process
- Nominal Minimum TBD ^{o}C (T case), VDDQ = 1.7 V, any process
- Nominal Maximum 0 ^{o}C (T case), VDDQ = 1.9 V, any process

5 AC & DC Operating Conditions (cont'd)

Table 28 — Full Strength Calibrated Pulldown Driver Characteristics

	Calibrated Pulldow n Current (mA)				
Voltage (V)	Nominal Minimum (21 ohms)	Nominal Low (18.75 ohms)	Nominal (18 ohms)	Nominal High (17.25 ohms)	Nominal Maximum (1 ohms)
0.2	9.5	10.7	11.5	11.8	13.3
0.3	14.3	16.0	16.6	17.4	20.0
0.4	18.7	21.0	21.6	23.0	27.0

Table 29 — Full Strength Calibrated Pullup Driver Characteristics

	Calibrated Pullup Current (mA)				
Voltage (V)	Nominal Minimum (21 ohms)	Nominal Low (18.75 ohms)	Nominal (18 ohms)	Nominal High (17.25 ohms)	Nominal Maximum (1 ohms)
0.2	-9.5	-10.7	-11.4	-11.8	-13.3
0.3	-14.3	-16.0	-16.5	-17.4	-20.0
0.4	-18.7	-21.0	-21.2	-23.0	-27.0

Table 30 — IDD Specification Parameters and Test Conditions

(IDD values are for full operating range of Voltage and Temperature, Notes 1 - 5

Symbol	Conditions	Max	Units	Notes
IDD0	**Operating one bank active-precharge current;** $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD1	**Operating one bank active-read-precharge current;** IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC\ (IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$, $t_{RCD} = t_{RCD(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA	
IDD2P	**Precharge power-down current;** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA	
IDD2Q	**Precharge quiet standby current;** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA	

Table 30 — IDD Specification Parameters and Test Conditions
(IDD values are for full operating range of Voltage and Temperature, Notes 1 - 5

Symbol	Conditions		Max	Units	Notes
IDD2N	**Precharge standby current;** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING			mA	
IDD3P	**Active power-down current;** All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0		mA	
		Slow PDN Exit MRS(12) = 1		mA	
IDD3N	**Active standby current;** All banks open; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING			mA	
IDD4W	**Operating burst write current;** All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING			mA	
IDD4R	**Operating burst read current;** All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W			mA	
IDD5B	**Burst refresh current;** $t_{CK} = t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING			mA	
IDD6	**Self refresh current;** CK and $\overline{CK}$ at 0V; CKE £ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING			mA	
IDD7	**Operating bank interleave read current;** All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = $t_{RCD(IDD)}$-1*$t_{CK(IDD)}$; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RRD} = t_{RRD(IDD)}$, t_{RCD} = 1*$t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; - Refer to the following page for detailed timing conditions			mA	

Table 30 — IDD Specification Parameters and Test Conditions
(IDD values are for full operating range of Voltage and Temperature, Notes 1 - 5

NOTE 1 IDD specifications are tested after the device is properly initialized

NOTE 2 Input slew rate is specified by AC Parametric Test Condition

NOTE 3 IDD parameters are specified with ODT disabled.

NOTE 4 Data bus consists of DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, LDQS, $\overline{LDQS}$, UDQS, and $\overline{UDQS}$. IDD values must be met with all combinations of EMRS bits 10 and 11.

NOTE 5 Definitions for IDD

LOW	=	Vin £ VILAC(max)
HIGH	=	Vin Š VIHAC(min)
STABLE	=	inputs stable at a HIGH or LOW level
FLOATING	=	inputs at VREF = VDDQ/2
SWITCHING	=	inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

IDD Testing Parameters

For purposes of IDD testing, the following parameters are to be utilized.

Table 31 — IDD Testing Parameters

	DDR2-667	DDR2-533			DDR2-400		
Parameter	**4-4-4**	**3-3-3**	**4-4-4**	**5-5-5**	**3-3-3**	**4-4-4**	**Units**
CL(IDD)	4	3	4	5	3	4	tCK
$t_{RCD(IDD)}$	12	11.25	15	18.75	15	20	ns
$t_{RC(IDD)}$	57	56.25	60	63.75	60	65	ns
$t_{RRD(IDD)}$-x4/x8	7.5	7.5	7.5	7.5	7.5	7.5	ns
$t_{RRD(IDD)}$-x16	10	10	10	10	10	10	ns
$t_{CK(IDD)}$	3	3.75	3.75	3.75	5	5	ns
$t_{RASmin(IDD)}$	45	45	45	45	45	45	ns
$t_{RASmax(IDD)}$	70000	70000	70000	70000	70000	70000	ns
$t_{RP(IDD)}$	12	11.25	15	18.75	15	20	ns
$t_{RFC(IDD)}$-256Mb	75	75	75	75	75	75	ns
$t_{RFC(IDD)}$-512Mb	105	105	105	105	105	105	ns
$t_{RFC(IDD)}$-1Gb	127.5	127.5	127.5	127.5	127.5	127.5	ns
$t_{RFC(IDD)}$-2Gb	197.5	197.5	197.5	197.5	197.5	197.5	ns

5 AC & DC Operating Conditions (cont'd)

Detailed IDD7

The detailed timings are shown below for IDD7. Changes will be required if timing parameter changes are made to the specification.

Legend: A = Active; RA = Read with Autoprecharge; D = Deselect

IDD7: Operating Current: All Bank Interleave Read operation
All banks are being interleaved at minimum ^{t}RC(IDD) without violating ^{t}RRD(IDD) using a burst length of 4. Control and address bus inputs are STABLE during DESELECTs. IOUT = 0mA

Timing Patterns for 4 bank devices x4/ x8/ x16
-DDR2-400 4/4/4: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D D D

-DDR2-400 3/3/3: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D D

-DDR2-533 5/4/4: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D

-DDR2-533 4/4/4: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D

Timing Patterns for 8 bank devices x4/x8
-DDR2-400 and DDR2-533 all bins: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D A4 RA4 A5 RA5 A6 RA6 A7 RA7 D D

Timing Patterns for 8 bank devices x16
-DDR2-400 all bins: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D A4 RA4 A5 RA5 A6 RA6 A7 RA7 D D

-DDR2-533 all bins: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D D

Table 32 — Input/Output capacitance

Parameter	Symbol	Min	Max	Units
Input capacitance, CK and $\overline{CK}$	CCK	1.5	2.5	pF
Input capacitance delta, CK and $\overline{CK}$	CDCK	x	0.25	pF
Input capacitance, all other input-only pins	CI	1.5	2.5	pF
Input capacitance delta, all other input-only pins	CDI	x	0.25	pF
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	3.0	4.0	pF
Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	CDIO	x	0.5	pF

Electrical Characteristics & AC Timing for DDR2-400/533/667 - Absolute Specification

(0 °C ≤ T_{CASE} ≤ xx °C; V_{DDQ} = 1.8V +/– 0.1V; V_{DD} = 1.8V +/– 0.1V)

Table 33 — Refresh Parameters by Device Density

Parameter	Symbol	256Mb	512Mb	1Gb	2Gb	4Gb	Units
Refresh to active/Refresh command time	tRFC	75	105	127.5	195	tbd	ns
Average periodic refresh interval	tREFI	7.8	7.8	7.8	7.8	7.8	µs

5 AC & DC Operating Conditions (cont'd)

Table 34 — DDR2 SDRAM Standard Speed Bins and tRCD, tRP and tRC for Corresponding Bin

Speed	DDR2-667	DDR2-533	DDR2-533	DDR2-533	DDR2-400	DDR2-400	Units
Bin (CL - tRCD - tRP)	4 - 4 - 4	3 - 3 - 3	4 - 4 - 4	5 - 5 - 5	3 - 3 - 3	4 - 4 - 4	
Parameter	min	min	min	min	min	min	
$\overline{CAS}$ Latency	4	3	4	5	3	4	tCK
tRCD	12	11.25	15	18.75	15	20	ns
tRP Note1	12	11.25	15	18.75	15	20	ns
tRC	57	56.25	60	63.75	60	65	ns

NOTE 1 8 bank device Precharge All Allowance: tRP for a Precharge All command for an 8 Bank device will be equal to tRP + 1 * tCK, where tRP are the values for a single bank pre-charge, which are shown in the above table.

Table 35 — Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)
(Refer to notes for information related to this table at the bottom)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Notes
		min	max	min	max		
DQ output access time from CK/$\overline{CK}$	tAC	-600	+600	-500	+500	ps	
DQS output access time from CK/$\overline{CK}$	tDQSCK	-500	+500	-450	+450	ps	
CK high-level width	tCH	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min(tCL,tCH)	x	min(tCL,tCH)	x	ps	11,12
Clock cycle time, CL=x	tCK	5000	8000	3750	8000	ps	15
DQ and DM input hold time	tDH	400	x	350	x	ps	6,7,8
DQ and DM input setup time	tDS	400	x	350	x	ps	6,7,8
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	tCK	
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	x	tAC max	ps	
Data-out low-impedance time from CK/$\overline{CK}$	tLZ	tAC min	tAC max	tAC min	tAC max	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	350	x	300	ps	13
DQ hold skew factor	tQHS	x	450	x	400	ps	12

Table 35 — Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)
(Refer to notes for information related to this table at the bottom)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Notes
		min	max	min	max		
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	ps	
Write command to first DQS latching transition	tDQSS	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	tCK	
DQS input high pulse width	tDQSH	0.35	x	0.35	x	tCK	
DQS input low pulse width	tDQSL	0.35	x	0.35	x	tCK	
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	tCK	
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK	
Mode register set command cycle time	tMRD	2	x	2	x	tCK	
Write preamble setup time	tWPRES	0	x	0	x	ps	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	10
Write preamble	tWPRE	0.25	x	0.25	x	tCK	
Address and control input hold time	tIH	600	x	500	x	ps	5,7,9
Address and control input setup time	tIS	600	x	500	x	ps	5,7,9
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	
Active to precharge command	tRAS	45	70000	45	70000	ns	3
Active to active command period for 1KB page size products	tRRD	7.5	x	7.5	x	ns	4
Active to active command period for 2KB page size products	tRRD	10	x	10	x	ns	4
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2		2		tCK	
Write recovery time	tWR	15	x	15	x	ns	
Auto precharge write recovery + precharge time	tDAL	tWR+tRP*	x	tWR+tRP*	x	tCK	14
Internal write to read command delay	tWTR	10	x	7.5	x	ns	
Internal read to precharge command delay	tRTP	7.5		7.5		ns	3
Exit self refresh to a non-read command	tXSNR	tRFC + 10		tRFC + 10		ns	

Table 35 — Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)
(Refer to notes for information related to this table at the bottom)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Notes
		min	max	min	max		
Exit self refresh to a read command	tXSRD	200		200		tCK	
Exit precharge power down to any non-read command	tXP	2	x	2	x	tCK	
Exit active power down to read command	tXARD	2	x	2	x	tCK	1
Exit active power down to read command (Slow exit, Lower power)	tXARDS	6 - AL		6 - AL		tCK	1, 2
CKE minimum pulse width (high and low pulse width)	^{t}CKE	3		3		tCK	
ODT turn-on delay	^{t}AOND	2	2	2	2	tCK	
ODT turn-on	^{t}AON	tAC(min)	tAC(max)+1	tAC(min)	tAC(max) +1	ns	16
ODT turn-on (Power-Down mode)	^{t}AONPD	tAC(min)+2	2tCK+tAC(max)+1	tAC(min)+2	2tCK+tAC (max)+1	ns	
ODT turn-off delay	^{t}AOFD	2.5	2.5	2.5	2.5	tCK	
ODT turn-off	^{t}AOF	tAC(min)	tAC(max)+ 0.6	tAC(min)	tAC(max) + 0.6	ns	17
ODT turn-off (Power-Down mode)	^{t}AOFPD	tAC(min)+2	2.5tCK+tAC(max)+1	tAC(min)+2	2.5tCK+tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3		3		tCK	
ODT power down exit latency	tAXPD	8		8		tCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		tIS+tCK+tIH		ns	15

5 AC & DC Operating Conditions (cont'd)

Table 36 — Timing Parameters by Speed Grade (DDR2-667 and DDR2-SS800)

(Refer to notes for information related to this table at the bottom)

Parameter	Symbol	DDR2-667		DDR2-SS800		Units	Notes
		min	max	min	max		
DQ output access time from CK/$\overline{CK}$	tAC					ps	
DQS output access time from CK/$\overline{CK}$	tDQSCK					ps	
CK high-level width	tCH	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min(tCL,tCH)	x	min(tCL,tCH)	x	ps	11,12
Clock cycle time, CL=x	tCK	3000	8000	2500		ps	15
DQ and DM input hold time	tDH		x		x	ps	6,7
DQ and DM input setup time	tDS		x		x	ps	6,7
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	tCK	
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	x	tAC max	ps	
Data-out low-impedance time from CK/$\overline{CK}$	tLZ	tAC min	tAC max	tAC min	tAC max	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x		x		ps	13
DQ hold skew factor	tQHS	x		x	400	ps	12
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	ps	
Write command to first DQS latching transition	tDQSS	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	tCK	
DQS input high pulse width	tDQSH	0.35	x	0.35	x	tCK	
DQS input low pulse width	tDQSL	0.35	x	0.35	x	tCK	
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	tCK	
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK	
Mode register set command cycle time	tMRD	2	x	2	x	tCK	
Write preamble setup time	tWPRES	0	x	0	x	ps	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	10
Write preamble	tWPRE	0.25	x	0.25	x	tCK	
Address and control input hold time	tIH		x		x	ps	5,7,9
Address and control input setup time	tIS		x		x	ps	5,7,9

Table 36 — Timing Parameters by Speed Grade (DDR2-667 and DDR2-SS800)
(Refer to notes for information related to this table at the bottom)

Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	
Activate to precharge command	tRAS	45	70000		70000	ns	3
Activate to activate command period for 1KB page size products	tRRD	7.5	x	7.5	x	ns	4
Activate to activate command period for 2KB page size products	tRRD	10	x	10	x	ns	4
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2		2		tCK	
Write recovery time	tWR	15	x	15	x	ns	
Auto precharge write recovery + precharge time	tDAL	tWR+tRP*	x	tWR+tRP*	x	tCK	14
Internal write to read command delay	tWTR	7.5	x	7.5		ns	
Internal read to precharge command delay	tRTP	7.5		7.5		ns	3
Exit self refresh to a non-read command	tXSNR	tRFC + 10		tRFC + 10		ns	
Exit self refreh to a read command	tXSRD	200		200		tCK	
Exit precharge power down to any command	tXP	2	x	2	x	tCK	
Exit active power down to read command	tXARD	2	x	2	x	tCK	1
Exit active power down to read command (Slow exit, Lower power)	tXARDS	6 - AL		TBD		tCK	1, 2
CKE minimum pulse width (high and low pulse width)	tCKE	3		3		tCK	
ODT turn-on delay	^{t}AOND	2	2	2	2	tCK	
ODT turn-on	^{t}AON	tAC(min)	tAC(max)+1	tAC(min)	tAC(max)+1	ns	16
ODT turn-on (Power-Down mode)	^{t}AONPD	tAC(min)+2	2tCK+tAC (max)+1	tAC(min)+2	2tCK+tAC (max)+1	ns	
ODT turn-off delay	^{t}AOFD	2.5	2.5	2.5	2.5	tCK	
ODT turn-off	^{t}AOF	tAC(min)	tAC(max)+ 0.6	tAC(min)	tAC(max)+ 0.6	ns	17
ODT turn-off (Power-Down mode)	^{t}AOFPD	tAC(min)+2	2.5tCK+tAC (max)+1	tAC(min)+2	2.5tCK+tA C(max)+1	ns	
ODT to power down entry latency	tANPD	3		3		tCK	
ODT Power Down Exit Latency	tAXPD	8		8		tCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	

Table 36 — Timing Parameters by Speed Grade (DDR2-667 and DDR2-SS800)
(Refer to notes for information related to this table at the bottom)

Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		tIS+tCK+tIH		ns	15

General Notes, Which May Apply for all AC Parameters

NOTE 1 Slew Rate Measurement Levels

a) Output slew rate for falling and rising edges is measured between VTT - 250 mV & VTT + 250 mV for single ended signals. For differential signals (e.g., DQS - $\overline{DQS}$) output slew rate is measured between DQS - $\overline{DQS}$ = -500 mV and DQS - $\overline{DQS}$ = +500mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

b) Input slew rate for single ended signals is measured from dc-level to ac-level: from VREF - 125 mV to VREF + 250 mV for rising edges and from VREF + 125 mV and VREF - 250 mV for falling edges. For differential signals (e.g., CK - $\overline{CK}$) slew rate for rising edges is measured from CK - $\overline{CK}$ = -250 mV to CK - $\overline{CK}$ = +500 mV (250mV to -500 mV for falling edges).

c) VID is the magnitude of the difference between the input voltage on CK and the input voltage on $\overline{CK}$, or between DQS and $\overline{DQS}$ for differential strobe.

NOTE 2 DDR2 SDRAM AC timing reference load. Figure 68 represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

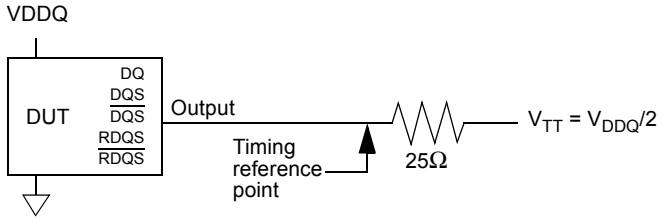


Figure 68 — AC Timing Reference Load

The output timing reference voltage level for single ended signals is the crosspoint with VTT. The output timing reference voltage level for differential signals is the crosspoint of the true (e.g., DQS) and the complement (e.g., DQS) signal.

NOTE 3 DDR2 SDRAM output slew rate test load. Output slew rate is characterized under the test conditions as shown in Figure 69.

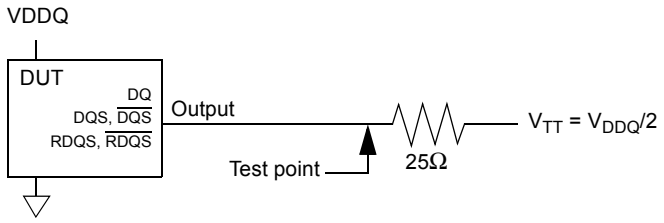


Figure 69 — Slew Rate Test Load

NOTE 4 Differential data strobe. DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. When differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 Ω to 10K Ω resistor to insure proper operation.

5 AC & DC Operating Conditions (cont'd)

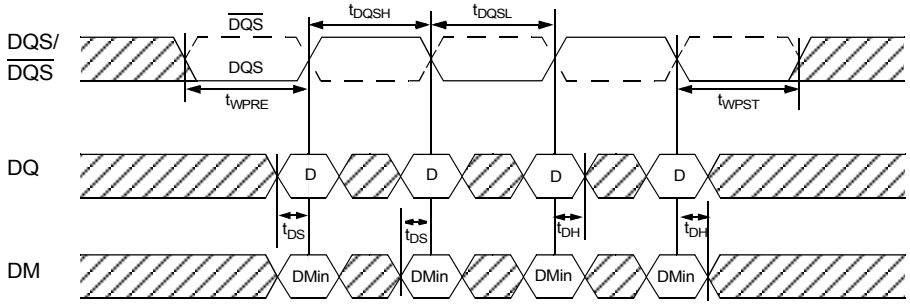


Figure 70 — Data Input (Write) Timing

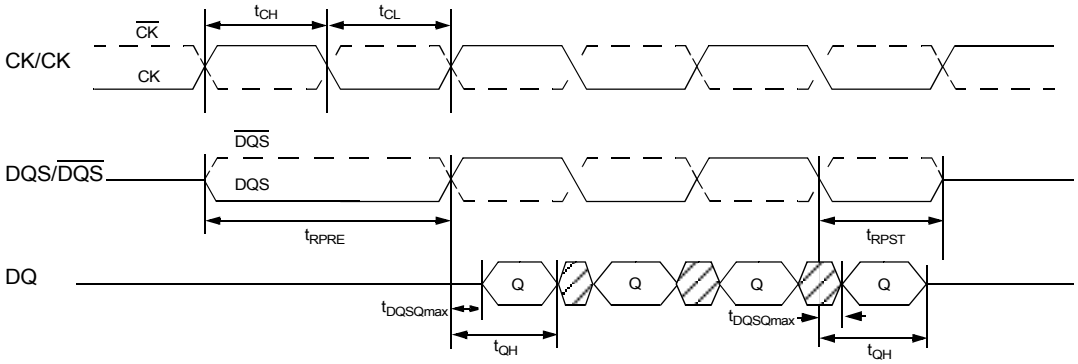


Figure 71 — Data Output (Read) Timing

NOTE 5 AC timings are for linear signal transitions. See System Derating for other signal transitions.

NOTE 6 These parameters guarantee device behavior, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.

NOTE 7 All voltages referenced to VSS.

NOTE 8 Tests for AC timing, IDD, and electrical (AC and DC) characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

Specific Notes for Dedicated AC Parameters

NOTE 1 User can choose which active power down exit timing to use via MRS(bit 12). tXARD is expected to be used for fast active power down exit timing. tXARDS is expected to be used for slow active power down exit timing where a lower power value is defined by each vendor data sheet.

NOTE 2 AL = Additive Latency

NOTE 3 This is a minimum requirement. Minimum read to precharge timing is AL + BL/2 providing the tRTP and tRAS(min) have been satisfied.

NOTE 4 A minimum of two clocks (2 * tCK) is required irrespective of operating frequency

NOTE 5 Timings are guaranteed with command/address input slew rate of 1.0 V/ns. See System Derating for other slew rate values.

NOTE 6 Timings are guaranteed with data, mask, and (DQS/RDQS in singled ended mode) input slew rate of 1.0 V/ns. See System Derating for other slew rate values.

NOTE 7 Timings are guaranteed with CK/$\overline{CK}$ differential slew rate of 2.0 V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0 V/ns in differential strobe mode and a slew rate of 1V/ns in single ended mode. See System Derating for other slew rate values.

Specific Notes for Dedicated AC Parameters Cont'd)

NOTE 8 tDS and tDH (data setup and hold) derating: TBD

NOTE 9 tIS and tIH (input setup and hold) derating: TBD

NOTE 10 The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

NOTE 11 MIN (t CL, t CH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t CL and t CH). For example, t CL and t CH are = 50% of the period, less the half period jitter (t JIT(HP)) of the clock source, and less the half period jitter due to crosstalk (t JIT(crosstalk)) into the clock traces.

NOTE 12 t QH = t HP – t QHS, where:
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL).

tQHS accounts for:

a. The pulse duration distortion of on-chip clock circuits; and

b. The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

NOTE 13 tDQSQ: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.

NOTE 14 t DAL = (nWR) + (tRP/tCK): For each of the terms above, if not already an integer, round to the next highest integer. tCK refers to the application clock period. nWR refers to the t WR parameter stored in the MRS.

Example: For DDR533 at t CK = 3.75 ns with t WR programmed to 4 clocks. tDAL = 4 + (15 ns / 3.75 ns) clocks = 4 +(4)clocks=8clocks.

NOTE 15 The clock frequency is allowed to change during self–refresh mode or precharge power-down mode. In case of clock frequency change during precharge power-down, a specific procedure is required as described in Section 2.2.9.

NOTE 16 ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND.

NOTE 17 ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD.

Annex A (informative) Revision Log

Rev	Contents of Modification
02/06/2003	JESD79-2 revision 0.9 for committee ballot for March 2003 committee meeting. If pass committee ballot, it will be announced as JESD79-2 Rev1.0 (DDR2 SDRAM Data Sheet Revision 1.0)
03/26/2003	Draft version of JESD79-2 has been finished with following changes made after March 2003 committee meeting. 1. Type corrections and editorial changes based on comments on committee ballot material 2. Updated power up and initialization sequence: committee ballot passed at March 2003 meeting 3. Added “Asynchronous CKE low event & Clock frequency change procedure” in section 2.2.9: committee ballot passed at March 2003 meeting 4. Added overshoot/Undershoot specification: committee ballot passed at March 2003 meeting 5. Added Full Strength Driver I/C curve: committee ballot passed at March 2003 meeting 6. Removed derating table: derating table is still under discussion
09/04/2003	Source file edited and formatted.

JEDEC

Exhibit B

Displayed by Document Type

NUMBER	JEDEC Engineering Bulletins (JEB)	PRICE
JEB 5-A	METHODS OF MEASUREMENT FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS: The purpose of this bulletin is to recommend for use in the rating of semiconductor logic gating microcircuits which use the binary states to represent and process logic information. Both static and dynamic measurements are covered. January 1970; Reaffirmed February 1984 /JEDEC Committee	$63.00
JEB 6	STANDARD MEASURMENTS OF THE ELECTRICAL CHARACTERISTICS OF SEMICONDUCTOR INTEGRATED CIRCUITS December 1966; Rescinded October 1984 /JEDEC	
JEB 15	TERMINOLOGY AND METHODS OF MEASUREMENT FOR BISTABLE SEMICONDUCTOR MICROCIRCUITS: This bulletin explains the terminology and methods of measurement for bistable semiconductor microcircuits. It is also intended to be used with the EIA Registration Data Format for semiconductor integrated bistable logic circuits. November 1969 /JC-40 Committee	$109.00
JEB 16	USER GUIDE FOR MICROCIRCUIT FAILURE ANALYSIS: This guide defines generalized procedures for the failure analysis of monolithic integrated microelectronic circuits. Although the generalized procedural steps may apply to all microelectronic circuits, additional analysis steps unique to thin/thick film hybrid devices are not covered. July 1970 /JC-14 Committee	$41.00
JEB 17	USER GUIDELINES FOR QUALITY AND RELIABILITY ASSURANCE OF LSI COMPONENTS November 1970; Rescinded April 1987 April 1987	
JEB 19	RECOMMENDED CHARACTERIZATION OF MOS SHIFT REGISTERS: This recommendation applies to MOS Shift Registers. Definitions are given for P-channel registers but are applicable to all CMOS and N-channel with changes in power supply notation. November 1972 /JC-40 Committee	$40.00
JEB 20	ACCEPTED PRACTICES FOR MAKING MICROELECTRONIC DEVICE THERMAL CHARACTERISTICS TESTS January 1975; Rescinded November 1988 /JC-11 Committee	

NUMBER	Tentative Standards (TENTSTD)	PRICE
TENTSTD 11	HANDLING AND INSTALLATION OF POWER SEMICONDUCTORS IN DISC TYPE PACKAGES: Included in JESD282 and EIA397. July 1973; Rescinded June 1992 June 1992 /JC-22.2 Subcommittee	
TENTSTD 12	STANDARD FOR SELENIUM SURGE SUPPRESSORS: The suppresser furnished under this standard shall be a product that has been tested and meets the definitions and minimum requirements specified herein. November 1973 /JC-22.5 Subcommittee	$49.00

NUMBER	JEDEC Specifications (JES)	PRICE
JES 2	TRANSISTOR, GALLIUM ARSENIDE POWER FET, GENERIC SPECIFICATION: Establishes guideline requirements and quality assurance provisions for gallium arsenide power field-effect transistors (FETs, also know as MESFETs) designed for use in high-reliability space application such as spacecraft communications transmitters. Identifies the electrical parameters, wafer acceptance tests, screening tests, qualification tests, and lot acceptance tests pertinent to power GaAs FETs. Applicable to packaged and chip-carrier parts; portions may not be applicable to unpackaged and unmounted chips. July 1992 /JC-14.7 Subcommittee	$71.00

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NUMBER	JEDEC Standards (JESD)	PRICE
JESD 1	LEADLESS CHIP CARRIER PINOUTS STANDARDIZED FOR LINEARS: This standard shows how to convert existing DIP pinouts for op-amps, comparators, and D/A converters, to chip carrier packages. April 1982 / Committee!33JC41	$41.00
JESD 2	DIGITAL BIPOLAR LOGIC PINOUTS FOR CHIP CARRIERS: This standard provides a chip carrier format for digital devices by defining pin functions and locations for 20, 38, 44, 52, and 68-terminal devices. December 1982 JC-40.1	$41.00
JESD 3-C	STANDARD DATA TRANSFER FORMAT BETWEEN DATA PREPARATION SYSTEM AND PROGRAMMABLE LOGIC DEVICE PROGRAMMER: This standard was developed to prevent the proliferation of data transfer formats that occurred with microprocessor development systems. The focus of the standard is on field programmable devices and their support tools. It is not intended for other types of semicustom logic devices or other types of fabrication or testing equipment. June 1994 / Committee!33JC421	$61.00
JESD 4	DEFINITION OF EXTERNAL CLEARANCE AND CREEPAGE DISTANCES OF DISCRETE SEMICONDUCTOR PACKAGES FOR THYRISTORS AND RECTIFIER DIODES: This standard defines reference distances between terminals of the device and the external package at specific voltages. November 1983; Reaffirmed January 1991, April 1999, April 2002 April 2002 /JC-22.2 Subcommittee	$38.00
JESD 5	MEASUREMENT OF TEMPERATURE COEFFICIENT OF VOLTAGE REGULATOR DIODES: This standard is designed to define voltage-temperature characteristic measurement techniques and a method of calculation. Although many methods could be defined, this method provides a desired uniformity and lends itself to production testing. Formerly JEDEC Suggested Standard No. 5A February 1982; Reaffirmed April 1999, April 2002 April 2002 /JC-22.4 Subcommittee	$38.00
JESD 6	MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE: This standard gives a test method for measuring transistor capacitance using a three-terminal bridge which employs a guard-circuit that eliminates the effect of extraneous capacitance. February 1967; Reaffirmed September 1981, April 1999 /JC-25 Committee	$47.00
JESD 7-A	STANDARD FOR DESCRIPTION OF 54/74HCXXXX AND 54/74HCTXXXX HIGH SPEED CMOS DEVICES: This standard provides uniformity, multiplicity of sources, eliminate confusion, and ease of device specification and design by users for HC, and HCT CMOS devices. This standard specifies electrical parameters. It also includes appendices listing part numbers. August 1986 JC-40.2	$109.00
JESD 8- 1	ADDENDUM No. 1 to JESD8: INTERFACE STANDARD FOR LOW VOLTAGE TTL-COMPATIBLE (LVTTL) VLSI DIGITAL CIRCUITS June 1994; Incorporated into JESD8-A, June 1994 /JC-16 Committee	
JESD 8- 1-A	INTERFACE STANDARD FOR NOMINAL 0.3 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS June 1994; Incorporated into JESD8-A, June 1994 /JC-16 Committee	
JESD 8- 2	ADDENDUM No. 2 to JESD8 - STANDARD FOR OPERATING VOLTAGES AND INTERFACE LEVELS FOR LOW VOLTAGE EMITTER-COUPLED LOGIC (ECL) INTEGRATED CIRCUITS: This Addendum No. 2 to JEDEC Standard No. 8 provides standard operating voltage and interface levels that can be used by designers and application engineers as they develop and introduce new products. Covers the ECL logic family designated 300K ECL. The 300K ECL family is Voltage and Temperature Compensated, with I/O interface levels compatible with the existing 100K ECL and 101K ECl families. March 1993 /JC-16 Committee	$40.00
JESD 8- 3	ADDENDUM No. 3 to JESD8 - GUNNING TRANSCEIVER LOGIC (GTL) LOW-LEVEL, HIGH-	

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SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS: This Addendum No. 3 to JEDEC Standard No. 8 defines the dc input and output specifications for a low-level, high-speed interface for integrated devices.

November 1993 /JC-16 Committee $38.00

JESD 8- 4 **ADDENDUM No. 4 to JESD8 - CENTER-TAP-TERMINATED (CTT) INTERFACE LOW-LEVEL, HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:** This Addendum No. 4 to JEDEC Standard No. 8 defines the dc input and output specifications for a low-level, high-speed interface for integrated devices that can be a super-set of LVCMOS and LVTTL.

November 1993 /JC-16 Committee $38.00

JESD 8- 5 **ADDENDUM No. 5 to JESD8 - 2.5 V 0.2 V (NORMAL RANGE), AND 1.8 V TO 2.7 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT:** This standard defines power supply voltage ranges, dc interface parameters for a high speed, low voltage family of non-terminated digital circuits driving/driven by parts of the same family. The specifications in this standard represent a minimum set of 'base line' set of interface specifications for CMOS-compatible circuits.

October 1995 /JC-16 Committee $40.00

JESD 8- 6 **ADDENDUM No. 6 to JESD8 - HIGH SPEED TRANSCEIVER LOGIC (HSTL)- A 1.5 V OUTPUT BUFFER SUPPLY VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:** This standard is a 1.5 volt high performance CMOS-based interface document suitable for high I/O count CMOS and BiCMOS devices operating at frequencies in excess of 200 Mhz.

August 1995 /JC-16 Committee $48.00

JESD 8- 7 **ADDENDUM No. 7 to JESD8 - 1.8 V + -0.15 V (NORMAL RANGE), AND 1.2 V - 1.95 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT:** This standard continues the voltage specification migration to the next level beyond the 2.5 V specification already established. Since this migration is driven by both process changes and performance/power, more entries can be expected in supporting required voltage levels. The rapidity of this evolution is expecting to increase because of the same feature sizes expected.

February 1997 /JC-16 Committee $40.00

JESD 8- 8 **ADDENDUM No. 8 to JESD8 - STUB SERIES TERMINATED LOGIC FOR 3.3 VOLTS (SSTL_3) A 3.3 V VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:** This standard is a result of a major effort by the JC-16 Committee to develop a high performance CMOS-based interface suitable for high speed main memory applications in excess of 125 MHz.

August 1996 /JC-16 Committee $47.00

JESD 8- 9B **ADDENDUM No. 9B to JESD8 - STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2): Includes Errata and Corrected Page 7 as of October 18, 2002.** This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the SSTL_2 logic switching range, nominally 0 V to 2.5 V. The standard may be applied to ICs operating with separate VDD and VDDQ supply voltages. This standard has been developed particularly with the objective of providing a relatively simple upgrade path from MOS push-pull interface designs. The standard is particularly intended to improve operation in situations where busses must be isolated from relatively large stubs.

May 2002 /JC-16 Committee $55.00

JESD 8-11 **ADDENDUM No. 11 to JESD8 - 1.5 V +/- 0.1 V (NORMAL RANGE) AND 0.9 - 1.6 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS:** This new standard provides specifications that will be used by several companies in new 1.5 V products designed in 0.12-0.15 um CMOS technologies, and in components that interface with them. The specifications allow limited interoperability with products using the existing JEDEC HSTL specification (JESD8-6).

October 2000 /JC-16 Committee $38.00

JESD 8-12 **1.2 V +/- 0.1 V (NORMAL RANGE) AND 0.8 - 1.3 V (WIDE RANGE) POWER SUPPLY**

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VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS: This standard defines power supply voltage ranges, dc interface and switching parameters for a high speed, low voltage family of nonterminated digital circuits driving/driven by parts of the same family, or mixed families which comply with the input receiver specifications. The specifications in this standard represent a minimum set of interface specifications for CMOS compatible circuits.

May 2001 /JC-16 Committee $37.00

JESD 8-13

SCALABLE LOW-VOLTAGE SIGNALING FOR 400 MV (SLVS-400): This standard defines the input, output, and termination specifications for differential signaling in the SLVS-400 environment, nominally between 0 and 400 mV. Power supplies other than the nominal 800 mV power for the SLVS interface are not specified.

October 2001 /JC-16 Committee $41.00

JESD 8-14

1.0 V +/- 0.1 V (NORMAL RANGE) AND 0.7 V - 1.1 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS: This new standard provides specifications that will be used by several companies in new 1.0 V products designed in 0.10-0.12 um CMOS technologies, and in components that interface with them. This standard defines power supply voltage ranges, dc interface and switching parameters for a high speed, low voltage family of nonterminated digital circuits driving/driven by parts of the same family, or mixed families which comply with the input receiver specifications. The specifications in this standard represent a minimum set of interface specifications for CMOS compatible circuits.

December 2001 /JC-16 Committee $38.00

JESD 8-15A

STUB SERIES TERMINATED LOGIC FOR 1.8 V (SSTL_18): This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the SSTL_18 logic switching range, nominally 0 V to 1.8 V. The standard may be applied to ICs operating with separate VDD and VDDQ supply voltages. The VDD value is not specified in this standard; however VDD and VDDQ will have the same voltage level in many cases.

September 2003 /JC-16 Committee $49.00

JESD 8-B

INTERFACE STANDARD FOR NOMINAL 0.3 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS: This standard (a replacement of JEDEC Standards No. 8, 8-1, 8-1-A, and 8-A) defines dc interface parameters for a family of digital circuits operating from a power supply of nominal 3.0 V/3.3. V and driving/driven by parts of the same family. The specifications in this standard represent a minimum set of 'base line' set of interface specifications for LVTTL-compatible and LVCMOS-compatible circuits.

September 1999 /JC-16 Committee $40.00

JESD 9-A

METAL PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES AND COVERS: This standard establishes the general requirements and quality assurance provisions that can be specified and met in procuring microelectronics packages and covers, manufactured from matched seal with and without high thermal conductivity base materials, intended for use in fabricating hybrid microelectronics circuits. This document details those minimum requirements necessary for metal packages' use exclusively.

April 1987; Under Revision /JC-13.5 Subcommittee $71.00

JESD 10

LOW FREQUENCY POWER TRANSISTORS: This standard consists of a listing of letter symbols, terms, and definitions that are used in power transistors. It also includes information on JEDEC registration procedures, verification tests, and thermal characteristics.

September 1981; Reaffirmed April 1999 /JC-25 Committee $147.00

JESD 11

CHIP CARRIER PINOUTS STANDARDIZED FOR CMOS 4000, HC AND HCT SERIES OF LOGIC CIRCUITS: This standard indicates the procedures used to convert existing DIP and flat packages for digital parts (SSI & MSI) to chip carrier packages.

December 1984 JC-40.2 $41.00

JESD 12

SEMICUSTOM INTEGRATED CIRCUITS (FORMERLY PUBLISHED AS STANDARD FOR GATE ARRAY BENCHMARK SET): The purpose of these benchmarks is to provide a common set of high level functions which serve as vehicles for comparing the performance of gate arrays implemented in any technology using any internal structure. These benchmarks effectively

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provide an unbiased measure of gate array vendors' ability to implement a desired complex function on a particular gate array at a known level of performance.

June 1985 / Committee!33JC44 $43.00

JESD 12-1B **ADDENDUM No. 1 to JESD12 - TERMS AND DEFINITIONS FOR GATE ARRAYS AND CELL-BASED INTEGRATED CIRCUITS:** The purpose of this standard is to promote the uniform use of abbreviations, terms, and definitions throughout the semiconductor industry. It is a useful guide for users, manufactures, educators, technical writers, and others interested in the characterization, nomenclature, and classification of semicustom integrated circuits.

August 1993 / Committee!33JC44 $48.00

JESD 12-2 **ADDENDUM No. 2 to JESD12 - STANDARD FOR CELL-BASED INTEGRATED CIRCUIT BENCHMARK SET:** The purpose of these benchmarks is to provide a common set of high level functions that serve as vehicles for comparing the performance of cell-based ICs implemented in any technology using any internal structure. JESD12-2 extends the gate array benchmark set (JESD12) to cell-based ICs.

February 1986 / Committee!33JC44 $61.00

JESD 12-3 **ADDENDUM No. 3 to JESD12 - CMOS GATE ARRAY MACROCELL STANDARD:** This standard defines a minimum set of macro cell standards for CMOS gate arrays. A total of 41 macro cell types are addressed, all of which are commonly used by gate array designers to implement Application Specific Integrated Circuits.

June 1986 / Committee!33JC44 $47.00

JESD 12-4 **ADDENDUM No. 4 to JESD12 - METHOD OF SPECIFICATION OF PERFORMANCE PARAMETERS FOR CMOS SEMICUSTOM INTEGRATED CIRCUITS:** This standard defines how to specify various performance parameters of semicustom ICs, including cell and interconnect propagation delays, input/output levels and capacitance, and power dissipation.

April 1987 / Committee!33JC44 $48.00

JESD 12-5 **ADDENDUM No. 5 to JESD12 - DESIGN FOR TESTABILITY GUIDELINES:** This standard is intended to provide circuit designers with the information needed to develop complex integrated circuits that can be reliably and economically tested without compromising flexibility.

August 1988 / Committee!33JC44 $109.00

JESD 12-6 **ADDENDUM No. 6 to JESD12 - INTERFACE STANDARD FOR SEMICUSTOM INTEGRATED CIRCUITS:** This standard defines logic interface levels for CMOS, TTL, ECL, and BiCC inputs and outputs. This standard is intended to provide an industry-wide set of specifications, for Application Specific Integrated Circuit (ASIC) signal inputs and outputs, both necessary and sufficient to define a circuits electrical interfacing with the external environment. JESD12-6 is intended to provide the ASIC manufacturer and user with a common set of signal interface levels. The standard defines interface levels for 5 volt operation.

March 1991 / Committee!33JC44 $43.00

JESD 13-B **STANDARD SPECIFICATION FOR DESCRIPTION OF B SERIES CMOS DEVICES:** This standard provides for uniformity, multiplicity of sources, elimination of confusion, and ease of device specifications and system design by users. It gives electrical levels and timing diagrams for B Series CMOS devices.

May 1980 JC-40.2 $63.00

JESD 14 **SEMICONDUCTOR POWER CONTROL MODULES:** Semiconductor Power Control Modules (SPCM) are modules consisting of thyristors or transistors, or both, as the primary controlling elements. Methods of manufacture of semiconductor power control modules include the assembling of individual components and the use of semiconductor hybrids or monolithic processing technologies, or both.

November 1986; Reaffirmed June 1992, April 1999, April 2002 April 2002 /JC-22.2 Subcommittee $47.00

JESD 16-A **ASSESSMENT OF AVERAGE OUTGOING QUALITY LEVELS IN PARTS PER MILLION (PPM):** This standard was revised to clarify assumptions necessary to estimate AOQ, revise the minimum sample size algorithm, address small sample size concerns, and provide methods

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for combining groups for AOQ estimation. Derivation of any new methods for combing groups for AOQ estimation. Derivation of any new methods introduced into this document have been provided in annexes. A statistical method is based on confidence interval statistics. A procedure was established for reporting AOQ when the minimum sample size criterion is not met.

April 1995 /JC-13 Committee $61.00

JESD 17 **LATCH-UP IN CMOS INTEGRATED CIRCUITS - SUPERSEDED BY JESD78, February 1999**

August 1988; Rescinded February 1999 February 1999 JC-40.2

JESD 18-A **STANDARD FOR DESCRIPTION OF FAST CMOS TTL COMPATIBLE LOGIC:** The purpose of this standard is to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users. The standard covers specifications for description of '54/74FCTXXXX' series fast CMOS TTL compatible devices.

January 1993 JC-40.2 $63.00

JESD 19 **GENERAL STANDARD FOR STATISTICAL PROCESS CONTROL (SPC) - SUPERSEDED by EIA-557-A**

July 1988; Rescinded July 1995 /JC-13 Committee

JESD 20 **STANDARD FOR DESCRIPTION OF 54/74ACXXXXX AND 54/74ACTXXXXX ADVANCED HIGH-SPEED CMOS DEVICES:** This standard describes electrical parameters for this class of CMOS devices.

September 1990 JC-40.2 $147.00

JESD 21-C **CONFIGURATIONS FOR SOLID STATE MEMORIES:** This revision of JESD21 is substantially different from previous issues because it reflects advancement in semiconductor technology and computer design needs. A new class of memory devices, the multiport DRAM (MPDRAM) C also know as 'Video Ram' because of the most common application for the devices C is represented. A new family of SRAMs which addresses the increasing need for high speed is introduced. Additional families of devices in the SOJ and Zip packages are included. The material in this revision is organized primarily by function (ROM, EPROM, SRAM, DRAM, etc.) rather than by technology and word length. Pinouts for SIMM and DIMM are included along with presence detect schemes. A current set of terms has also been included. JESD21-C is a compilation of all memory device standards that have been developed by the JC-42 Committee and approved by the JEDEC Council from September 1989. This latest issue has changed to a loose-leaf format and comes in a three-ring binder so that new drawings can be added without requiring a new publication.

September 1989 /JC-42 Committee $150.00

JESD 21-C AUS **ANNUAL UPDATING SERVICE:** The JEDEC Office has generated a mailing list for those who wish to subscribe to updates of this publication. A payment is required for subscription to this updating service.

September 2000 / Committee!33JCJEDC $50.00

JESD 22-A100-B **CYCLED TEMPERATURE HUMIDITY BIAS LIFE TEST:** The Cycled Temperature-humidity-bias Life Test is performed for the purpose of evaluating the reliability of nonhermetic packaged solid state devices in humid environments. It employs conditions of temperature cycling, humidity, and bias that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors that pass through it. The Cycled Temperature-Humidity-Bias Life Test is typically performed on cavity packages (e.g. MQUADs, lidded ceramic pin grid arrays, etc.) as an alternative to JESD22-A101 or JESD22-A110.

April 2000 /JC-14.1 Subcommittee $40.00

JESD 22-A101-B **STEADY-STATE TEMPERATURE HUMIDITY BIAS LIFE TEST:** This standard establishes a defined method and conditions for performing a temperature humidity life test with bias applied. The test is used to evaluate the reliability of non-hermetic packaged solid state devices in humid environments. It employs high temperature and humidity conditions to accelerate the penetration of moisture through external protective material or along interfaces between the external protective coating and conductors or other features which

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pass through it. This revision enhances the ability to perform this test on a device which cannot be biased to achieve very low power dissipation.

April 1997 /JC-14.1 Subcommittee $40.00

JESD 22-A102-C **ACCELERATED MOISTURE RESISTANCE - UNBIASED AUTOCLAVE:** This test allows the user to evaluate the moisture resistance of nonhermetic packaged solid state devices. The Unbiased Autoclave Test is performed to evaluate the moisture resistance integrity of non-hermetic packaged solid state devices using moisture condensing or moisture saturated steam environments. It is a highly accelerated test which employs conditions of pressure, humidity and temperature under condensing conditions to accelerate moisture penetration through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors passing through it. This test is used to identify failure mechanisms internal to the package and is destructive.

December 2000 /JC-14.1 Subcommittee $38.00

JESD 22-A103-B **HIGH TEMPERATURE STORAGE LIFE:** The test is applicable for evaluation, screening, monitoring, and/or qualification of all solid state devices. High Temperature storage test is typically used to determine the effect of time and temperature, understorage conditions, for thermally activated failure mechanisms of solid state electronic devices, includingnonvolatile memory devices (data retention failure mechanisms). During the test elevated temperatures(accelerated test conditions) are used without electrical stress applied. This test may be destructive,depending on Time, Temperature and Packaging (if any).

August 2001 /JC-14.1 Subcommittee $38.00

JESD 22-A104-B **TEMPERATURE CYCLING:** This standard provides a method for determining solid state devices capability to withstand extreme temperature cycling. Changes in this revision include requirements that the worst-case load temperature must reach the specific extremes rather than just requiring that the chamber ambient temperature reach the extremes. This ensures that the test specimens will reach the specified temperature extremes regardless of chamber loading. Definitions are provided for Load, Monitoring Sensor, Worst-Case Load Temperature, and Working Zone. The transfer time has been tightened from 5 minutes to 1 minute. Five new test conditions have been added as well as a caution on test conditions which exceed the glass transition temperature of plastic package solid devices.

July 2000 /JC-14.1 Subcommittee $43.00

JESD 22-A105-B **POWER AND TEMPERATURE CYCLING:** This Power and Temperature Cycling Test is performed to determine the ability of a device to withstand alternate exposures at high and low temperature extremes with operating biases periodically applied and removed. It is intended to simulate worst-case conditions encountered in typical applications. This test method is considered destructive, and is intended primarily for device qualification.

February 1996; Under Revision /JC-14.1 Subcommittee $38.00

JESD 22-A106-A **THERMAL SHOCK:** This test is conducted to determine the resistance of a part to sudden exposure to extreme changes in temperature and to the effect of alternate exposures to these extremes.

April 1995; Under Revision /JC-14.1 Subcommittee $41.00

JESD 22-A107-A **SALT ATMOSPHERE:** This standard provides a method for determining solid state devices resistance to corrosion as a result of salt atmosphere exposure. Changes in this revision include making preconditioning optional, making the temperature tolerance in the chamber +3 degrees C and the deposition tolerance +10 grams. This will allow better correlation among test chambers. Added was a requirement for the pH of the salt solution to be maintained between 6.0 and 7.5 at 35 degrees C minimum.

December 1989; Reaffirmed January 1998, Under Revision January 1998 /JC-14.1 Subcommittee $38.00

JESD 22-A108-B **TEMPERATURE, BIAS, AND OPERATING LIFE:** A revised method for determining the effects of bias conditions and temperature, over time, on solid state devices is now available. Revision B of A108 includes low temperature operating life (LTOL) and high temperature gate bias (HTGB) stress conditions, revised cool down requirements for high temperature stress, and a procedure to follow if parts are not tested within the allowed time window.

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December 2000 /JC-14.1 Subcommittee $40.00

JESD 22-A109-A **HERMETICITY:** This revised test method establishes a standard procedure for determining the effectiveness of the seal of hermetically sealed solid state devices. The objective of this revision was to modify the test parameters to reflect current practice and to eliminate the specification of fluorocarbons, banned from use due to environmental concerns.

July 2001 /JC-14.1 Subcommittee $43.00

JESD 22-A110-B **HIGHLY ACCELERATED TEMPERATURE AND HUMIDITY STRESS TEST (HAST)** The purpose of this new test method is to evaluate the reliability of nonhermetic packaged solid state devices in humid environments. It employs severe conditions of temperature, humidity, and bias that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it.

February 1999; Under Revision /JC-14.1 Subcommittee $40.00

JESD 22-A112-A **MOISTURE-INDUCED STRESS SENSITIVITY FOR PLASTIC SURFACE MOUNT DEVICES - SUPERSEDED BY J-STD-020A, April 1999.** See J-STD-020B, published July 2002.

November 1995; Rescinded May 2000 May 2000 /JC-14.1 Subcommittee

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JESD 22-A113D **PRECONDITIONING OF PLASTIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING:** This Test Method establishes an industry standard preconditioning flow for nonhermetic solid state SMDs (surface mount devices) that is representative of a typical industry multiple solder reflow operation. These SMDs should be subjected to the appropriate preconditioning sequence of this document by the semiconductor manufacturer prior to being submitted to specific in-house reliability testing (qualification and reliability monitoring) to evaluate long term reliability (which might be impacted by solder reflow).

August 2003 /JC-14.1 Subcommittee $45.00

JESD 22-A114-B **ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING HUMAN BODY MODEL (HBM):** This test method establishes a standard procedure for testing and classifying microcircuits according to their susceptibility to damage or degradation by exposure to a defined electrostatic Human Body Model (HBM) discharge (ESD). The objective is to provide reliable, repeatable HBM ESD test results so that accurate classifications can be performed.

June 2000 /JC-14.1 Subcommittee $45.00

JESD 22-A115-A **ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING MACHINE MODEL (MM):** This method establishes a standard procedure for testing and classifying microcircuits according to their susceptibility to damage or degradation by exposure to a defined Machine Model (MM) electrostatic discharge (ESD). The objective is to provide reliable, repeatable MM ESD test results so that accurate classifications can be performed.

October 1997; Under Revision /JC-14.1 Subcommittee $45.00

JESD 22-A117 **ELECTRICALLY ERASABLE PROGRAMMABLE ROM (EEPROM) PROGRAM/ERASE ENDURANCE AND DATA RETENTION TEST:** This method establishes a standard procedure for determining the data cycling endurance and data retention capability of non-volatile memory cells. It is intended as a qualification and monitor test procedure. This test is also applicable to FLASH EEPROM integrated circuits and Erasable Programmable Logic Devices (EPLD) with embedded EEPROM or FLASH memory.

January 2000 /JC-14.1 Subcommittee $40.00

JESD 22-A118 **ACCELERATED MOISTURE RESISTANCE - UNBIASED HAST:** The Unbiased HAST is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It is a highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion). This test is used to identify failure mechanisms internal to the package and is destructive.

December 2000 /JC-14.1 Subcommittee $41.00

JESD 22-A120 **TEST METHOD FOR THE MEASUREMENT OF MOISTURE DIFFUSIVITY AND WATER SOLUBILITY**

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IN ORGANIC MATERIALS USED IN INTEGRATED CIRCUITS: This specification details the procedures for the measurement of characteristic bulk material properties of moisture diffusivity and water solubility in organic materials used in the packaging of IC components. These two material properties are important parameters for the effective reliability performance of plastic packaged ICs after exposure to moisture and subjected to high temperature solder reflow.

June 2001 /JC-14.1 Subcommittee $41.00

JESD 22-B100-B **PHYSICAL DIMENSION:** The standard provides a method for determining whether the external physical dimensions of the device are in accordance with the applicable procurement document. This revision includes a change in details to be specified by the procurement document.

June 2003 September 2002 /JC-14.1 Subcommittee $38.00

JESD 22-B101 **EXTERNAL VISUAL:** The purpose of this inspection is to verify that the materials, design, construction, markings, and workmanship of the device are in accordance with the applicable procurement document. External visual is a nondestructive test and applicable for all package types. The test is useful for qualification, process monitor, or lot acceptance.

September 1987; Under Revision /JC-14.1 Subcommittee $37.00

JESD 22-B102-C **SOLDERABILITY:** The purpose of this test method is to provide a means of determining the solderability of device package terminations that are intended to be joined to another surface using solder for the attachment. It also provides optional conditions for aging and soldering for the purpose of allowing simulation of the soldering process to be used in the device applications. It provides procedures for dip and look solderability testing of through hole, axial and surface mount devices and reflow simulated use testing for surface mount packages.

September 1998; Under Revision /JC-14.1 Subcommittee $49.00

JESD 22-B103-B **VIBRATION, VARIABLE FREQUENCY:** The Vibration, Variable Frequency Test Method is intended to determine the ability of component(s) to withstand moderate to severe vibration as a result of motion produced by transportation or filed operation of electrical equipment. This is a destructive test that is intended forcomponent qualification.

June 2002; Under Revision /JC-14.1 Subcommittee $43.00

JESD 22-B104-B **MECHANICAL SHOCK:** This test is intended to determine the suitability of component parts for use in electronic equipment that may be subjected to moderately severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. Shock of this type may disturb operating characteristics, particularly if the shock pulses are repetitive. This is a destructive test intended for device qualification. It is normally applicable to cavity-type packages.

May 2001 /JC-14.1 Subcommittee $38.00

JESD 22-B105C **LEAD INTEGRITY:** This test method provides various tests for determining the integrity lead/package interface and the lead itself when the lead(s) are bent due to faulty board assembly followed by rework of the part for reassembly. For hermetic packages it is rececommend that this test be followed by hermeticity tests in accordance with Test Method A109 to determine if there are any adverse effects from the stresses applied to the seals as well as to the leads. These tests, including each of its test conditions, is considered destructive and is only recommended for qualification testing. This test is applicable to all through-hole devices and surface-mount devices requiring lead forming by the user.

May 2003 /JC-14.1 Subcommittee $48.00

JESD 22-B106-B **RESISTANCE TO SOLDERING TEMPERATURE FOR THROUGH-HOLE MOUNTED DEVICES:** This method established a standard procedure for determining whether through-hole solid state devices can withstand the effects of the temperature to which they will be subject during soldering of their leads. This revision updates the references to currently military standards.

February 1999 /JC-14.1 Subcommittee $38.00

JESD 22-B107-A **MARKING PERMANENCY:** The purpose of this test method is to verify that the markings on solid state semiconductor devices will not become illegible when subjected to solvents or cleaning solutions commonly used during the removal of solder flux residue from printed

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circuit board assembly process. The primary reasons for revising this test method are: 1) eliminate chemicals containing carcinogens; 2) reduce CFCs and 3) to align with MIL-STD-883 basic document.

September 1995; Under Revision /JC-14.1 Subcommittee $40.00

JESD 22-B108A **COPLANARITY TEST FOR SURFACE-MOUNT SEMICONDUCTOR DEVICES:** The purpose of this test is to measure the deviation of the terminals (leads or solder balls) from coplanarity for surface-mount semiconductor devices.

January 2003 /JC-14.1 Subcommittee $41.00

JESD 22-B109 **FLIP CHIP TENSILE PULL:** The Flip Chip Tensile Pull Test Method is performed to determine the fracture mode and strength of the solder bump interconnection between the flip chip die and the substrate. It should be used to assess the consistency of the chip join process. This test method is a destructive test.

June 2002 /JC-14.1 Subcommittee $41.00

JESD 22-B110 **SUBASSEMBLY MECHANICAL SHOCK:** The new test method JESD22-B110 provides guidance for in-situ testing of mechanical shock resistance of components as mounted in a subassembly. Using terms, procedures, and test levels in common with JESD22-B104B, this test method provides a range of test level options to improve test applicability and compatibility with fragility test procedures. Test procedures are detailed, including test card and fixture needs, test tolerances, test documentation, component preparation, and definition of terms.

May 2001 /JC-14.1 Subcommittee $41.00

JESD 22-B116 **WIRE BOND SHEAR TEST:** This test method establishes a standard procedure for determining the strength of an integrated circuit wire bond by shearing the wire from the surface it is bonded to and measuring the force required. This method serves as an alternative to pulling the wire vertically until the wire separates from one of it's two bonded surfaces. It also provides guidelines for determining an appropriate minimum shear force for gold balls on aluminum alloy bonding surfaces.

July 1998 /JC-14.1 Subcommittee $45.00

JESD 22-B117 **BALL GRID ARRAY (BGA) BALL SHEAR:** Test method for BGA Ball Shear. This test method has ball shear terms and definitions; apparatus description; the BGA ball shear procedure; and BGA ball shear failure modes and their criteria. Where applicable, figures are included to show the apparatus and six typical failure modes.

July 2000 /JC-14.1 Subcommittee $41.00

JESD 22-C100-A **HIGH TEMPERATURE CONTINUITY - RESCINDED, November 1999**

April 1990; Rescinded November 1999 /JC-14.1 Subcommittee

JESD 22-C101-A **FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC DISCHARGE WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS:** This new test method describes a uniform method for establishing charged-device model electrostatic discharge withstand thresholds. The charged-device-model simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing. One of many examples is a device sliding down a shipping tube hitting a metal surface. Discharges to devices on unterminated circuit assemblies are also well-modeled by the CDM test. DM ESD events not only reduce assembly yields but can also produce device damage that goes undetected by factory test and later is the cause of a latent failure.

June 2000 /JC-14.1 Subcommittee $41.00

JESD 23 **TEST METHODS AND CHARACTER DESIGNATION FOR LIQUID CRYSTAL DEVICES:** This standard specifies a collection of procedures for testing and character designation of liquid crystal devices.

May 1982 $57.00

JESD 24 **POWER MOSFETS:** This standard contains a listing of terms and definitions and letter symbols; a description of established procedures that are followed in the assignment of

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semiconductor-industry-type designations to power transistors; electrical verification test; thermal characteristics; and a user's guide.

July 1985 /JC-25 Committee $71.00

JESD 24- 1 **ADDENDUM No. 1 to JESD24 - METHOD FOR MEASUREMENT OF POWER DEVICE TURN-OFF SWITCHING LOSS:** Describes the method of a typical oscilloscope waveform and the basic test circuit employed in the measurement of turn off loss for bipolar, IGBT and MOSFET power semiconductors. This method can be used as a standard for evaluating power semiconductor turn-off switching loss capability and defines standard terminology that should be referenced within the electronic industry.

October 1989; Reaffirmed April 1999 /JC-25 Committee $41.00

JESD 24- 2 **ADDENDUM No. 2 to JESD24 - GATE CHARGE TEST METHOD:** This addendum establishes a method for measuring power device gate charge. A gate charge test is performed by driving the device gate with a constant current and measuring the resulting gate voltage response. Constant gate current scales the gate voltage, a function of time, to a function of coulombs. The slope of the generated response reflects the active device capacitance as it varies during the switching transition . Gate charge measurements are useful for characterizing the large signal switching performance of power MOS and IGBT devices. Developed over a four year span by the JEDEC JC-25 Committee, the method defines a repeatable means of measuring the widely published Qgd charge values.

January 1991; Reaffirmed April 1999 /JC-25 Committee $41.00

JESD 24- 3 **ADDENDUM No. 3 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR VERTICAL POWER MOSFETS (DELTA SOURCE-DRAIN VOLTAGE METHOD):** The purpose of this test method is to measure the thermal impedance of the MOSFET under the specified conditions of applied voltage, current and pulse duration. The temperature sensitivity if the forward voltage drop of the source-drain is used as the junction temperature indicator. This method is particularly suitable to enhancement mode, power MOSFETs having relatively long thermal response times. This test method may be used to measure the thermal response of junction to a heating pulse, to ensure proper die mountdown to its case, or the dc thermal resistance, by the proper choice of the pulse duration and magnitude if the heating pulse.

November 1990; Reaffirmed April 1999 /JC-25 Committee $47.00

JESD 24- 4 **ADDENDUM No. 4 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR BIPOLAR TRANSISTORS (DELTA BASE-EMITTER VOLTAGE METHOD):** The purpose of this test method is to measure the thermal impedance of the Bipolar Transistor under the specified conditions of applied voltage, current and pulse duration. The temperature sensitivity of the base-emitter voltage is used as the junction temperature indicator. This test method is used to measure the thermal response of the junction to a heating pulse. Specifically, the test may be used to measure dc thermal resistance, and to ensure proper die mountdown to its case. This is accomplished through the appropriate choice of pulse duration and heating power magnitude.

November 1990; Reaffirmed April 1999 /JC-25 Committee $47.00

JESD 24- 5 **ADDENDUM No. 5 to JESD24 - SINGLE PULSE UNCLAMPED INDUCTIVE SWITCHING (UIS) AVALANCHE TEST METHOD:** This method describes a means for testing the ability of a power switching device to withstand avalanche breakdown.

August 1990; Reaffirmed April 1999 /JC-25 Committee $38.00

JESD 24- 6 **ADDENDUM No. 6 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR INSULATED GATE BIPOLAR TRANSISTORS:** This standard describes in detail the method for thermal measurements of Insulated Gate Bipolar Transistors (IGBTs) and is suitable for use both in manufacturing and application of the devices. The method covers both thermal transient and thermal equilibrium measurements for manufacturing process control and device characterization purposes. Properly implemented, JESD24-6 provides a basis for obtaining realistic thermal parametric values that will benefit supplier's internal effectiveness and will be useful to the design and manufacturer of reliable IGBT circuits.

October 1991; Reaffirmed April 1999 /JC-25 Committee $47.00

JESD 24- 7 **ADDENDUM No. 7 to JESD24 - COMMUTATING DIODE SAFE OPERATING AREA TEST PROCEDURE FOR MEASURING dv/dt DURING REVERSE RECOVERY OF POWER TRANSISTORS:** Defines methods for verifying the diode recovery stress capability of power transistors.

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	August 1982; Reaffirmed April 1999 /JC-25 Committee	$40.00
JESD 24- 8	**ADDENDUM No. 8 to JESD24 - METHOD FOR REPETITIVE INDUCTIVE LOAD AVALANCHE SWITCHING:** Determines the repetitive inductive avalanche switching capability of power switching transistors. August 1992; Reaffirmed April 1999 /JC-25 Committee	$40.00
JESD 24- 9	**ADDENDUM No. 9 to JESD24 - SHORT CIRCUIT WITHSTAND TIME TEST METHOD:** Test method to determine how long a device can survive a short circuit condition with a given drive level. August 1992; Reaffirmed April 1999 /JC-25 Committee	$40.00
JESD 24-10	**ADDENDUM No. 10 to JESD24 - TEST METHOD FOR MEASUREMENT OF REVERSE RECOVERY TIME trr FOR POWER MOSFET DRAIN-SOURCE DIODES:** Test method to measure the reverse recovery characteristics of the drain source diode of a power MOSFET. August 1994; Reaffirmed April 1999 /JC-25 Committee	$41.00
JESD 24-11	**ADDENDUM No. 11 to JESD24 - POWER MOSFET EQUIVALENT SERIES GATE RESISTANCE TEST METHOD:** Test method to measure the equivalent resistance of the gate to source of a power MOSFET. August 1996; Reaffirmed March 2001 /JC-25 Committee	$38.00
JESD 25	**MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS:** This standard provides a test method and definition for small-signal conditions at microwave frequencies. November 1972; Reaffirmed September 1981, April 2000 /JC-25 Committee	$57.00
JESD 26-A	**GENERAL SPECIFICATION FOR PLASTIC ENCAPSULATED MICROCIRCUITS FOR USE IN RUGGED APPLICATIONS - RESCINDED, July 2001** April 1990; Rescinded July 2001 /JC-13.2 Subcommittee	
JESD 27	**CERAMIC PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES:** The intent of this standard is to be a guide in the manufacture and procurement of ceramic packages, especially for the hybrid industry. Manufacturers or ceramic packages and procuring activities for these packages will now be able to use this document as the means for agreement in the imposition of minimum requirements in qualification, screening, and quality conformance. August 1993; Under Revision , will be merged with JESD9-A /JC-13.5 Subcommittee	$67.00
JESD 28-1	**N-CHANNEL MOSFET HOT CARRIER DATA ANALYSIS:** This addendum provides data analysis examples useful in analyzing MOSFET n-channel hot-carrier-induced degradation data. This addendum to JESD28 (Hot carrier n-channel testing standard) suggests hot-carrier data analysis techniques. September 2001 /JC-14.2 Subcommittee	$43.00
JESD 28-A	**A PROCEDURE FOR MEASURING N-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION UNDER DC STRESS:** This document describes an accelerated test for measuring the hot-carrier-induced degradation of a single n-channel MOSFET using dc bias. The purpose of this document is to specify a minimum set of measurements so that valid comparisons can be made between different technologies, IC processes, and process variations in a simple, consistent and controlled way. The measurements specified should be viewed as a starting point in the characterization and benchmarking of the transistor manufacturing process. December 2001 /JC-14.2 Subcommittee	$47.00
JESD 29-A	**FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING - SUPERSEDED BY EIA/ANSI-659, July 1996.** July 1996; Superseded July 1996 /JC-14.3 Subcommittee	
JESD 30C	**DESCRIPTIVE DESIGNATION SYSTEM FOR SEMICONDUCTOR-DEVICE PACKAGES:** This standard describes a systematic method for generating universal descriptive designators for semiconductor-device packages. The descriptive designator is intended to provide a useful communication tool but has no implied control for assuring package interchangeability. September 2003 January 2001 /JC-11 Committee	$55.00

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JESD 31C

GENERAL REQUIREMENTS FOR DISTRIBUTORS OF COMMERCIAL AND MILITARY SEMICONDUCTOR DEVICES: This publication identifies the general requirements for Distributors that supply Commercial and Military products. This document identifies the general requirements for Distributors that supply Commercial and Military products. Now updated to provide clarification, these requirements apply to all discrete semiconductors, integrated circuits and hybrids, whether packaged or in wafer/die form, manufactured by all component Manufacturers. This revision was incorporated to better define the requirements for the handling of moisture-sensitive devices in distribution. The addition of IPC/JEDEC J-STD-020 and IPC/JEDEC J-STD-033 ensure consistent requirements throughout the distribution channel.

September 2003 January 2003 /JC-14.4 Subcommittee $52.00

JESD 32

STANDARD FOR CHAIN DESCRIPTION FILE: This document provides a standard for describing an ISP device chain, opening up the possibility for third-party companies to provide value-added ISP software. The purpose of the Chain Description File is to describe the configuration of a programming chain made up of devices that can be connected in some serial fashion. No assumptions are made about how data is used by the device, nor about the nature or configuration of the control signals that affect programming. It will support devices configured using electrically-erasable(EE), Flash, SRAM, or any other reconfigurable cell. For devices programmed via an IEEE programmable devices in the same chain.

June 1996 / Committee!33JC421 $47.00

JESD 33-A

STANDARD METHOD FOR MEASURING AND USING THE TEMPERATURE COEFFICIENT OF RESISTANCE TO DETERMINE THE TEMPERATURE OF A METALLIZATION LINE: This revised standard provides the results of an interlaboratory experiment to determine the reproducibility and repeatability of the methods for measuring the temperature coefficient of resistance (TCR) of a metallization and for using the TCR to determine the temperature rise in a metal line due to joule heating and to use the metal line to monitor its temperature. It provides a list of potential measurement interference's to be considered in determining the TCR of a metallization and provides a number of precautions in the use of the TCR to measure joule heating and to monitor ambient temperature. This standard is designed for both wafer and package-level measurements.

October 1995 /JC-14.2 Subcommittee $55.00

JESD 34

FAILURE-MECHANISM-DRIVEN RELIABILITY QUALIFICATION OF SILICON DEVICES: This document applies to the reliability qualification of new or changed silicon devices, and their materials or manufacturing processes. Does not address qualification of product quality or functionality. Provides an alternative to traditional stress-driven qualification.

March 1993 /JC-14.2 Subcommittee $43.00

JESD 35-1

ADDENDUM No. 1 to JESD35 - GENERAL GUIDELINES FOR DESIGNING TEST STRUCTURES FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS: This addendum expands the usefulness of the Standard 35 (JESD35) by detailing the various sources of measurement error that could effect the test results obtained by the ramped tests described in JESD35. Each source of error is described and its implications on test structure design is noted. This addendum can be used as a guide when designing test structures for the qualification and characterization of thin oxide reliability, specifically, by implementing accelerated voltage or current ramp tests.

September 1995 /JC-14.2 Subcommittee $52.00

JESD 35-2

ADDENDUM No. 2 to JESD35 - TEST CRITERIA FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS: This addendum includes test criteria to supplement JESD35. JESD35 describes procedures developed for estimating the overall integrity of thin oxides in the MOS Integrated Circuit manufacturing industry. Two test procedures are included in JESD35: a Voltage-Ramp (V-Ramp) and a Current-Ramp (J-Ramp). As JESD35 became implemented into production facilities on a variety of test structures and oxide attributes, a need arose to clarify end point determination and point out some of the obstacles that could be overcome by careful characterization of the equipment and test structures.

February 1996 /JC-14.2 Subcommittee $43.00

JESD 35-A

PROCEDURE FOR WAFER-LEVEL-TESTING OF THIN DIELECTRICS: The revised JESD35 is intended for use in the MOS Integrated Circuit manufacturing industry. It describes

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procedures developed for estimating the overall integrity and reliability of thin gate oxides. Three basic test procedures are described, the Voltage-Ramp (V-Ramp), the Current-Ramp (J-Ramp) and the new Constant Current (Bounded J-Ramp) test. Each test is designed for simplicity, speed and ease of use. The standard has been updated to include breakdown criteria that are more robust in detecting breakdown in thinner gate oxides that may not experience hard thermal breakdown.

April 2001 /JC-14.2 Subcommittee $67.00

JESD 36 **STANDARD DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE, 5 V TOLERANT CMOS LOGIC DEVICES:** This standard outlines the standard dc specifications, test conditions, and test loading for logic products that are designed to tolerate input and output voltages which exceed the device's power supply. More specifically this standardizes 5 V - tolerant logic prducts that run from 'low voltage' (2.7 V to 3.6 V) power supplies. Products that meet this standard can be used to effectively interface between LVCMOS/LVTTL and 5 V TTL buses, bridging the gap between low-voltage and 5 V TTL busses.

June 1996 /JC-40 Committee $45.00

JESD 37 **STANDARD LOGNORMAL ANALYSIS OF UNCENSORED DATA, AND OF SINGLY RIGHT -CENSORED DATA UTILIZING THE PERSSON AND ROOTZEN METHOD:** This standard details techniques for estimating the values of a two parameter lognormal distribution from complete lifetime data (all samples in an experiment have failed) or singly right-censored lifetime data (the experiment have failed) or singly right-censored lifetime data gathered from rapid stress test; however, not all types of failure data can be analyzed with these techniques.

October 1992 /JC-14.2 Subcommittee $59.00

JESD 38 **STANDARD FOR FAILURE ANALYSIS REPORT FORMAT:** This standard is to promote unification of content and format of semiconductor device failure-analysis reports so that reports from diverse laboratories may be easily read, compared, and understood by customers. Additional objectives are to ensure that reports can be easily ready by users, satisfactorily reproduced on copying machines, adequately transmitted by telefax, and conveniently stored in standard filing cabinets.

December 1995 /JC-14.6 Subcommittee $43.00

JESD 39-A **QUALITY SYSTEM ASSESSMENT - SUPERSEDED BY ANSI/EIA-670, June 1997.**

June 1997; Superseded /JC-14.4 Subcommittee

JESD 40 **PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS - SUPERSEDED BY EIA-623, July 1994**

July 1994 /JC-13 Committee

JESD 41 **REVERSE RECOVERY CHARACTERISTICS OF SILICON DIODES: Rescinded June 2002.**

May 1995; Rescinded June 2002 /JC-22.1 Subcommittee

JESD 42 **REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES - SUPERSEDED BY EIA-625, November 1994.**

March 1994; Superseded /JC-13 Committee

JESD 43 **COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS - SUPERSEDED BY EIA-671, November 1996.**

November 1996; Superseded /JC-14.4 Subcommittee

JESD 45 **MEASUREMENT METHOD FOR THERMAL RESISTANCE OF BRIDGE RECTIFIER ASSEMBLIES: Rescinded June 2002. Replaced by JESD282-B.**

December 1994; Rescinded June 2002 /JC-22.2 Subcommittee

JESD 46-B **CUSTOMER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS:** This standard establishes procedures to notify customers of semiconductor product and process changes. Requirements include: documentation; procedures for classification, notification and customer response; content; and records.Documentation of a suppliers change notification system should set clear and understandable expectations for both the originators of the change and their end customers.

August 2001 /JC-14.4 Subcommittee $38.00

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JESD 47B

STRESS-TEST-DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS: This standard contains a set of most frequently encountered and accepted reliability stress tests. These tests are used for qualifying new and changed technology/process/ product families as well as individual products. These reliability stress tests have been found capable of stimulating and precipitating semiconductor device failures, in an accelerated manner. This document does not relieve the supplier of the responsibility to meet internal qualification programs. NOTE The headers in this document wer corrected on 9/23/03, if you printed the document prior to this date please discard.

August 2003 January 2003 /JC-14.3 Subcommittee $55.00

JESD 48-A

PRODUCT DISCONTINUANCE: This standard establishes the requirements for timely customer notification of planned productdiscontinuance, which will assist customers in managing end-of-life supply, or to transition on-goingrequirements to alternate products.

August 2001 /JC-14.4 Subcommittee $37.00

JESD 49

PROCUREMENT STANDARD FOR KNOWN GOOD DIE (KGD): This standard was created to facilitate the procurement and use of high reliability semiconductor microcircuits or discrete devices provided in bare die form, commonly known as Known Good Die (KGD).

February 1996 /JC-13 Committee $45.00

JESD 50

SPECIAL REQUIREMENTS FOR MAVERICK PRODUCT ELIMINATION: This standard applies to the identification and control of Maverick Product that can occur during fabrication, assembly, packaging, or test of any electronic component. It can be implemented for an entire product line or to segregate product that has a higher probability of adversely impacting quality or reliability.

December 1995 /JC-14.3 Subcommittee $40.00

JESD 51

METHODOLOGY FOR THE THERMAL MEASUREMENT OF COMPONENT PACKAGES (SINGLE SEMICONDUCTOR DEVICE) This standard and its subsequent addendum's, provides a standard for thermal measurement that, if followed fully, will provide correct and meaningful data that will allow for determination of junction temperature for specific conditions. The data can be used for package design evaluation, device characterization and reliability predictions.

December 1995 /JC-15.1 Subcommittee $40.00

JESD 51- 1

INTEGRATED CIRCUIT THERMAL MEASUREMENT METHOD - ELECTRICAL TEST METHOD (SINGLE SEMICONDUCTOR DEVICE): The purpose of this test method is to define a standard Electrical Test Method (ETM) that can be used to determine the thermal characteristics of single integrated circuit devices housed in some form of electrical package. This method will provide a basis for comparison of different devices housed in the same electronic package or similar devices housed in different electronic packages.

December 1995 /JC-15 Committee $61.00

JESD 51- 2

INTEGRATED CIRCUITS THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - NATURAL CONVECTION (STILL AIR): This document outlines the environmental conditions necessary to ensure accuracy and repeatability for a standard junction-to-ambient thermal resistance measurement in natural convection.

December 1995 /JC-15 Committee $47.00

JESD 51- 3

LOW EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES: This standard describes design requirements for a single layer, leaded surface mount integrated circuit package thermal test board. The standard describes board material and geometry requirements, minimum trace lenghts, trace thickness, and routing considerations. Application includes still air and moving air thermal tests.

August 1996 /JC-15.1 Subcommittee $41.00

JESD 51- 4

THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP): This guideline describes design requirements for wire bond type semiconductor chips to be used for thermal resistance listing of IC packages. This document provides specific guidelines for chip design but allows flexibility in the materials and layout requirements.

February 1997 /JC-15.1 Subcommittee $45.00

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JESD 51- 5 **EXTENSION OF THERMAL TEST BOARD STANDARDS FOR PACKAGES WITH DIRECT THERMAL ATTACHMENT MECHANISMS:** This extension of the thermal standards provides a standard fixture for direct attach type packages such as deep-downset of thermally tabbed packages. This specification provides additional design detail for use in developing thermal test boards with application to these package types. This document is in addition to and not replacement for the design specifications in other standards.

February 1999 /JC-15.1 Subcommittee $38.00

JESD 51- 6 **INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - FORCED CONVECTION (MOVING AIR):** This standard specifies the environmental conditions for determining thermal performance of an integrated circuit device in a forced convection environment when mounted on a standard thermal test board.

March 1999 /JC-15.1 Subcommittee $38.00

JESD 51- 7 **HIGH EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES:** This fixturing further defines the environment for thermal test of packaged microelectronic devices. Its function is to provide an alternate mounting surface for the analysis of heat flow in electronic components. The objective of the standard is to provide a high effective thermal conductivity mounting surface that can be compared equally against standard tests done in different laboratories with typical variations of less than or equal to 10%.

February 1999 /JC-15.1 Subcommittee $41.00

JESD 51- 8 **INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - JUNCTION-TO-BOARD:** This specification should be used in conjunction with the overview document JESD51, Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device) [1] and the electrical test procedures described in JESD51-1, 'Integrated Circuit Thermal Measurement Method (Single Semiconductor Device' [2. The environmental conditions described in this document are specifically designed for testing of integrated circuit devices that are mounted on standard test boards with two internal copper planes [3]. This standard is not applicable to packages that have asymmetric heat flow paths to the printed board caused by such thermal enhancements as fused leads (leads connected to the die pad) or power style packages with the exposed heat slug on one side of the package.

October 1999 /JC-15.1 Subcommittee $45.00

JESD 51- 9 **TEST BOARDS FOR AREA ARRAY SURFACE MOUNT PACKAGE THERMAL MEASUREMENTS:** This standard covers the design of printed circuit boards (PCBs) used in the thermal characterization of ball grid array (BGA) and land grid array (LGA) packages. It is intended to be used in conjunction with the JESD51 series of standards that cover the test methods and test environments. JESD51-9 was developed to give a figure-of-merit of thermal performance that allows for accurate comparisons of packages from different suppliers. It can be used to give a first order approximation of system performance and, in conjunction with the other JESD51 PCB standards, allows for comparisons of the various package families.

July 2000 /JC-15.1 Subcommittee $48.00

JESD 51-10 **TEST BOARDS FOR THROUGH-HOLE PERIMETER LEADED PACKAGE THERMAL MEASUREMENTS:** This standard covers the design of printed circuit boards (PCBs) used in the thermal characterization of Dual-Inline Packages (DIP) and Single-Inline Packages (SIP). It is intended to be used in conjunction with the JESD51 series of standards that cover the test methods and test environments. JESD51-10 was developed to give a figure-of-merit of thermal performance that allows for accurate comparisons of packages from different suppliers. It can be used to give a first order approximation of system performance and, in conjunction with the other JESD51 PCB standards, allows for comparisons of the various package families.

July 2000 /JC-15.1 Subcommittee $45.00

JESD 51-11 **TEST BOARDS FOR THROUGH-HOLE AREA ARRAY LEADED PACKAGE THERMAL MEASUREMENT:** This standard covers the design of printed circuit boards (PCBs) used in the thermal characterization of Pin Grid Array (PGA) packages. It is intended to be used in conjunction with the JESD51 series of standards that cover the test methods and test environments. JESD51-11 was developed to give a figure-of-merit of thermal performance that allows for accurate comparisons of packages from different suppliers. It can be used to give a first

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order approximation of system performance and, in conjunction with the other JESD51 PCB standards, allows for comparisons of the various package families.

June 2001 /JC-15.1 Subcommittee $47.00

JESD 52 **STANDARD FOR DESCRIPTION OF LOW VOLTAGE TTL-COMPATIBLE CMOS LOGIC DEVICES:** This standard describes dc interface specifications and test environment for these devices that operate with 2.7 V to 3.6 V power supplies. The goal is to provide a consistent set of dc specifications for reference by logic suppliers and users alike.

November 1995 /JC-40 Committee $45.00

JESD 53 **MANAGEMENT OF COMPONENT OBSOLESCENCE BY GOVERNMENT CONTRACTORS: Rescinded, October 2002**

January 1996; Rescinded October 2002 /JC-13.2 Subcommittee

JESD 54 **STANDARD FOR DESCRIPTION OF 54/74ABTXXX AND 74BCXXX TTL-COMPATIBLE BiCMOS LOGIC DEVICES:** The purpose is to provide a standard of BiCMOS Logic series specifications to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

February 1996 /JC-40 Committee $61.00

JESD 55 **STANDARD FOR DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE BiCMOS LOGIC DEVICES:** The purpose is to provide a standard of BiCMOS Logic series specifications for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

May 1996 /JC-40 Committee $49.00

JESD 57 **TEST PROCEDURE FOR THE MANAGEMENT OF SINGLE-EVENT EFFECTS IN SEMICONDUCTOR DEVICES FROM HEAVY ION IRRADIATION:** This test method defines requirements and procedures for ground simulation and single event effects (SEE) and implementation of the method in testing integrated circuits. This standard is valid when using a cyclotron or Van de Graaff accelerator. Microcircuits under test must be delidded. The ions used at the facilities have an atomic number Z > 2. It does not apply to SEE testing that uses protons, neutrons, or other lighter particles. This standard is designed to eliminate any misunderstanding between users of the method and test facilities, to minimize delays, and to promote standardization of testing and test data.

December 1996 /JC-13.4 Subcommittee $67.00

JESD 59 **BOND WIRE MODELING STANDARD:** This standard describes the modeling of a bond wire from an integrated circuit (IC) die to a package lead in a ball or wedge type wire bond configuration.

June 1997 /JC-15 Committee $45.00

JESD 60 **A PROCEDURE FOR MEASURING P-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION AT MAXIMUM GATE CURRENT UNDER DC STRESS:** This method establishes a standard procedure for accelerated testing of the hot-carrier-induced change of a p-channel MOSFET. The objective is to provide a minimum set of measurements so that accurate comparisons can be made.

April 1997 /JC-14.2 Subcommittee $45.00

JESD 61 **ISOTHERMAL ELECTROMIGRATION TEST PROCEDURE:** This standard describes an algorithm for the execution of the isothermal test, using computer-controlled instrumentation. The primary use of this test is for the monitoring of microelectronic metallization lines at water level (1) in process development, to evaluate process options, (2) in manufacturing, to monitor metallization reliability and (3) to monitor/evaluate process equipment. While it is developed as a fast WLR test, it can also be an effective tool for controlling the uniformity of stress applied during the standard package level electromigration test.

April 1997 /JC-14.2 Subcommittee $49.00

JESD 62-A **OUTLIER IDENTIFICATION AND MANAGEMENT SYSTEM FOR ELECTRONIC COMPONENTS:** This revision incorporates recommended tests and an example of a statistics-based method for identifying and removing outliers, i.e., parts that meet supplier specifications and end-user requirements but lie outside typical distribution limits. Outlier product can occur during fabrication, assembly, packaging, or test of any electronic components.

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May 2002 /JC-14.3 Subcommittee $45.00

JESD 63 **STANDARD METHOD FOR CALCULATING THE ELECTROMIGRATION MODEL PARAMETERS FOR CURRENT DENSITY AND TEMPERATURE:** This method provides procedures to calculate sample estimates and their confidence intervals for the electromigration model parameters of current density and temperature. The model parameter for current density is the exponent (n) to which the current density is raised in Black's equation. The parameter for temperature is the activation energy for the electromigration failure process.

February 1998 /JC-14.2 Subcommittee $61.00

JESD 64-A **STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES WITH 3.6 V CMOS TOLERANT INPUTS AND OUTPUTS:** The purpose is to provide a standard for 2.5 V nominal supply voltage logic devices for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. This specification provides for compatibility between devices operating between either the Standard Range of 1.8 V to 2.7 V or the optional Extended Range of 1.65 V to 2.7 V supply voltages, as well as over-voltage tolerance with devices operating at 3.6 V.

October 2000 /JC-40 Committee $40.00

JESD 65B **DEFINITION OF SKEW SPECIFICATIONS FOR STANDARD LOGIC DEVICES:** This standard defines skew specifications and skew testing for standard logic devices. The purpose is to provide a standard for specifications to achieve uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

September 2003 /JC-40 Committee $48.00

JESD 66 **TRANSIENT VOLTAGE SUPPRESSOR STANDARD FOR THYRISTOR SURGE PROTECTIVE DEVICE:** This standard is applicable to Thyristor Surge Protective Devices. It describes terms and definitions and explains methods for verifying device ratings and measuring device characteristics. The intended users of this standard are those interested in Thyristor Surge Protective Device characterization and rating verification. These devices are used primarily by the telecommunications industry to protect circuits from harmful overvoltages. The Thyristor Surge Protective Device (TSPD) is a semiconductor device that is finding widespread application in the telecommunication industry. The intent of this stand is to provide information on test methods that will reduce the possibility of disagreement and misunderstanding between TSPD vendors and users, and facilitate the determination of device interchangeability.

November 1999 /JC-22.5 Subcommittee $91.00

JESD 67 **I/O DRIVERS AND RECEIVERS WITH CONFIGURABLE COMMUNICATION VOLTAGE, IMPEDANCE, AND RECEIVER THRESHOLD:** This standard attempts to aid in the design of electronic systems comprised of components that operate at several different supply voltages. This document covers respectively configurable I/O voltage, receiver type and switchpoint, and driver impedance.

February 1999 /JC-16 Committee $45.00

JESD 68.01 **COMMON FLASH INTERFACE (CFI):** The Common Flash Interface (CFI) specification outlines a device and host system software interrogation handshake that allows specific software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward- and backward-compatible software support for the specific flash families. It allows flash vendors to standardize their existing interfaces for long-term compatibility. The changes for this minor revision are indicated in Annex A on page 11.

September 2003 December 2002 /JC-42.4 Subcommittee $48.00

JESD 69 **INFORMATION REQUIREMENTS FOR THE QUALIFICATION OF SILICON DEVICES:** This standard establishes the information required by semiconductor users from IC manufacturers and distributors in order to judge whether a semiconductor component is fit for use in their particular application. It establishes a set of data elements that describes the component and defines what each element means. It does not define the quality and reliability requirements that the component must satisfy. This standard can be used in conjunction with other reliability qualification standards, such as JESD34 'Failure Mechanism-Driven Reliability Qualification of Silicon Devices' and JESD47 'Stress Test Driven Qualification of Integrated Circuits'.

April 2000 /JC-14.3 Subcommittee $40.00

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JESD 70 **2.5 V BiCMOS LOGIC DEVICE FAMILY SPECIFICATION WITH 5 V TOLERANT INPUTS AND OUTPUTS:** The purpose is to provide a standard for 2.5 V nominal supply voltage logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use, thus providing compatibility between devices operating between 2.3 V and 2.7 V supply voltages, as well as overvoltage tolerance with devices operating at 3.3 V, or 5 V.

June 1999 /JC-40 Committee $41.00

JESD 71 **STANDARD TEST AND PROGRAMMING LANGUAGE (STAPL):** STAPL is a vendor- and platform-independent language for programming and testing devices via the IEEE standard 1149.1 interface, commonly known as JTAG. STAPL enables programming of designs into programmable logic devices (PLDs) offered by a variety of PLD vendors. STAPL is also suitable for testing 1149.1-compliant devices.

August 1999 / Committee!33JC421 $67.00

JESD 72 **TEST METHODS AND ACCEPTANCE PROCEDURES FOR THE EVALUATION OF POLYMERIC MATERIALS:** This Test Method covers the minimum requirements that should be in effect for the evaluation and acceptance of polymeric materials for use in industrial, military, space, and other special-condition products which may require capabilities beyond standard commercial microelectronics applications. It is not the intent of this Publication to specify a material, but to evaluate the material to assure that the quality and reliability of the microelectronic devices are not compromised. This document replaces JEP105, JEP107 and JEP112.

June 2001 January 2001 /JC-13.5 Subcommittee $52.00

JESD 73 **DESCRIPTION OF 5 V BUS SWITCH WITH TTL-COMPATIBLE CONTROL INPUTS:** This standard covers specifications for a family of 5 V NMOS FET bus switch devices with 5 V TTL compatible control inputs. Not included in this document are device-specific parameters and performance levels that the vendor must also apply for full device description.

June 1999 /JC-40 Committee $40.00

JESD 73-1 **STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES:** This standard covers specifications for a family of 3.3 V NMOS FET bus switch devices. Not included in this document are device specific parameters and performance levels that the vendor must also supply for full device description. The purpose of this document is to provide a set of uniform data sheet parameters for the description of bus switch devices. This standard includes required parameters, test conditions, test levels, and measurement methods for data sheet descriptions of bus switch devices.

August 2001 /JC-40 Committee $40.00

JESD 73-2 **STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES WITH INTEGRATED CHARGE PUMPS:** This standard covers specifications for a family of 3.3 V NMOS FET bus switch devices with integrated charge pumps. Not included in this document are device specific parameters and performance levels that the vendor must also supply for full device description. The purpose of this standard is to provide a set of uniform data sheet parameters for the description of bus switch devices. This standard includes required parameters, test conditions, test levels, and measurement methods for data sheet descriptions of bus switch devices.

August 2001 /JC-40 Committee $40.00

JESD 73-3 **STANDARD FOR DESCRIPTION OF 3867 - 2.5 V, SINGLE 10-BIT, 2-PORT, DDR FET SWITCH:** This standard provides a set of uniform data sheet parameters for the description of a single 10-bit, 2.5 V FET transmission-gate bus switch device for DDR memory module and motherboard applications. This bus switch device has a low ON resistance allowing inputs to be connected directly to outputs, with near zero propagation delay.

November 2001 JC-40.2 $40.00

JESD 73-4 **STANDARD FOR DESCRIPTION OF 3877 - 2.5 V, DUAL 5-BIT, 2-PORT, DDR FET SWITCH:** This standard provides a set of uniform data sheet parameters for the description of a dual 5-bit, 2.5 V FET transmission-gate bus switch device for DDR memory module and motherboard applications. This bus switch device has a low ON resistance allowing inputs to be connected directly to outputs, with near zero propagation delay.

November 2001 JC-40.2 $40.00

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JESD 74

EARLY LIFE FAILURE RATE CALCULATION PROCEDURE FOR ELECTRONIC COMPONENTS: This new standard defines a procedure for calculating the point estimate of the time-dependent failure rate of electronic components from early life failure rate (ELFR) reliability test data. Calculation techniques are developed for constant failure rate and decreasing failure rate distributions. Projections can be used to compare reliability performance with objectives, provide line feedback, support service cost estimates, and set product test and reliability screen strategies.

April 2000 /JC-14.3 Subcommittee $43.00

JESD 75

BALL GRID ARRAY PINOUTS STANDARDIZED FOR 32-BIT LOGIC FUNCTIONS: The purpose of this standard is to provide a pinout standard for dual-die 32-bit logic devices offered in a 96- and 144-ball grid array package for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease use. This standard defines device output for 32-bit wide buffer, driver and transceiver functions. This pinout specifically applies to the conversion of DIP-packaged 16-bit logic devices to LFBGA-packaged dual-die 32-bit logic devices.

November 1999 /JC-40 Committee $38.00

JESD 75-1

BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16, 18, AND 20-BIT LOGIC FUNCTIONS USING A 54 BALL PACKAGE: This standard establishes a 54 Ball Grid Array pinout for 16, 18 and 20-bit standard logic devices that are currently being produced in 48 and 56 Pin SSOP and TSSOP packages. The 54 Ball Grid Array Package is organized as a 6 x 9 array with balls on a .8mm x .8mm grid pitch.

October 2001 /JC-40 Committee $38.00

JESD 75-2

BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16-BIT LOGIC FUNCTIONS: This standard provides a pinout standard for 16-bit wide logic devices offered in a 56-ball areagrid array package to provide for uniformity, multiplicity of sources, elimination of confusion,ease of device specification, and ease of use.

July 2001 /JC-40 Committee $38.00

JESD 75-3

BALL GRID ARRAY PINOUTS STANDARDIZED FOR 8-BIT LOGIC FUNCTIONS: This standard provides a pinout standard for 8-bit logic devices offered in a 20-ball area gridarray package to provide for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

July 2001 /JC-40 Committee $37.00

JESD 76

DESCRIPTION OF 1.8 V CMOS LOGIC DEVICES: This standard continues the voltage specification migration to the next level beyond the 2.5 V specification already established in JESD80. In this standard, the input and output conditions are described for CMOS Logic products in a 1.8 V (Normal Range) application.

April 2000 JC-40.1 $38.00

JESD 76-1

STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (WIDE RANGE OPERATION): This standard defines dc interface, switching parameters and test loading for digital logic devices based on 1.2 V (nominal) power supply levels. The purpose is to provide a standard specification for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

June 2001 /JC-40 Committee $38.00

JESD 76-2

STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (NORMAL RANGE OPERATION): This standard defines dc interface, switching parameters and test loading for digital logic devices based on 1.2 V (normal range) power supply levels. The purpose is to provide a standard specification for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

June 2001 /JC-40 Committee $38.00

JESD 76-3

STANDARD DESCRIPTION OF 1.5 V CMOS LOGIC DEVICES: This standard continues the voltage specification migration to the next level beyond the 1.8 V specification already established. The purpose is to provide a standard for 1.5 V nominal supply voltage CMOS logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

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August 2001 JC-40.1 $38.00

JESD 77B **TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR DISCRETE SEMICONDUCTOR AND OPTOELECTRONIC DEVICES:** A revised and significantly expanded reference for technical writers and educators, manufacturers, buyers and users of discrete semiconductor and optoelectronic devices, is now available. Revision B of JEDEC Standard No. 77 includes extensive information on: letter symbol conventions; diodes and rectifiers (including signal, rectifier, microwave, tunnel and backward, voltage-regulator, voltage-reference, current regulator, and varactor diodes); transistors (including FETs, JFETs, and IGBTs); photosensitive devices, photoemitters, and optocouplers; thyristors and PUTs; and transient voltage suppressors. Terms and symbols, with their definitions, are arranged alphabetically by product type. Where applicable, graphical symbols are also included.

February 2000 /JC-10 Committee $162.00

JESD 78 **IC LATCH-UP TEST:** This standard has been adopted by the Defense Logistics Agency (DLA) as project 5962-1880. This standard establishes a defined method for latch-up testing of ICs. It defines Classes and Levels for a device's latch-up capability so that both the user and supplier understand a device's latch-up capabilities. It is applicable to NMOS, CMOS, Bipolar, and all variations and combinations of these technologies. Latch-up is an extremely important factor in determining product reliability.

March 1997 /JC-14.1 Subcommittee $48.00

JESD 79-2 **DDR2 SDRAM SPECIFICATION** This comprehensive standard defines all required aspects of 256Mb through 4Gb DDR2 SDRAMs with x4/x8/x16 data interfaces, including pinout, addressing, functional description, features, ac and dc parametrics, truth tables, and packages. Standard JESD79-2 uses a SSTL_18 interface, which is described in another JEDEC standard called JESD8-15. The purpose of this Standard is to define the minimum set of requirements for compliant devices 256Mb through 4Gb, x4/x8/x16 DDR2 SDRAMs. System designs based on the required aspects of this specification will be supported by all DDR2 SDRAM vendors providing compliant devices.

September 2003 /JC-42.3 Subcommittee $91.00

JESD 79C **DOUBLE DATA RATE (DDR) SDRAM SPECIFICATION:** This comprehensive standard defines all required aspects of 64Mb through 1Gb DDR SDRAMs with X4/X8/X16 data interfaces, including features, functionality, ac and dc parametrics, packages and pin assignments. This scope will subsequently be expanded to formally apply to x32 devices, and higher density devices as well. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 64Mb through 1Gb, X4/X8/X16 DDR SDRAMs. System designs based on the required aspects of this specification will be supported by all DDR SDRAM vendors providing JEDEC compliant devices.

March 2003 JC-42.3C $109.00

JESD 80 **STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES:** The purpose of this standard is to provide a standard for 2.5 V nominal supply-voltage CMOS logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. This standard defines dc interface parameters and test loading for CMOS digital logic family based on 2.5 V (nominal) power supply levels at 2.5 V input tolerance.

November 1999 /JC-40 Committee $38.00

JESD 82 **DEFINITION OF CDCV857 PLL CLOCK DRIVER FOR REGISTERED DDR DIMM APPLICATIONS:** This specification is a reference for Registered DDR DIMM designers. JESD82 defines the physical, electrical, interface and timing requirements of a 1:10 PLL clock driver for DDR Registered DIMMs from DDR200 to DDR266 as refined in revision C of JEDEC Standard 21-C (JESD21-C). JESD82 was also written to meet the future performance requirements of Registered DIMMs for DDR300 and DDR333.

July 2000 /JC-40 Committee $47.00

JESD 82-1 **DEFINITION OF CV857 PLL CLOCK DRIVER FOR REGISTERED PC1600, PC2100, AND PC2700 DIMM APPLICATIONS:** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a CV857 PLL clock device for registered PC1600, PC2100 and PC2700 DIMM applications. The purpose is to provide a standard for a CV857 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

October 2002 /JC-40 Committee $48.00

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JESD 82-2	**STANDARD FOR DESCRIPTION OF A 3.3 V, 18-BIT, LVTTL I/O REGISTER FOR PC133 REGISTERED DIMM APPLICATIONS:** This standard defines the register support devices needed for standard height and low profile registered PC133 SDRAM DIMM modules. The objective of the standard is to clearly define the functionality, pinout and electrical characteristics required for this type of SDRAM module. July 2001 /JC-40 Committee	$45.00
JESD 82-3A	**DEFINITION OF THE SSTV16857 2.5 V, 14-BIT SSTL_2 REGISTERED BUFFER FOR DDR DIMM APPLICATIONS:** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTV16857 14-bit SSTL_2 registered buffer for DDR DIMM applications.The purpose is to provide a standard for the SSTV16857 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. October 2002 /JC-40 Committee	$43.00
JESD 82-4B	**STANDARD FOR DEFINITION OF THE SSTV16859 2.5 V, 13-BIT TO 26-BIT SSTL_2 REGISTERED BUFFER FOR STACKED DDR DIMM APPLICATIONS:** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTV16859 13-bit to 26-bit SSTL_2 registered buffer for stacked DDR DIMM applications. The purpose is to provide a standard for the SSTV16859 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. May 2003 /JC-40 Committee	$47.00
JESD 82-5	**STANDARD FOR DESCRIPTION OF A 3.3 V, ZERO DELAY CLOCK DISTRIBUTION DEVICE COMPLIANT WITH THE JESD21-C PC133 REGISTERED DIMM SPECIFICATION** This standard defines the PLL support devices required for standard height and low profile registered PC133 SDRAM DIMM modules. The objective of the standard is to clearly define the functionality, pinout and electrical characteristics of the PLL used on JEDEC standard modules.JESD82-5 is the latest specification to be added to the JESD82 family of specifications for memory module support devices. Additional specifications are currently under development for DDRII support devices. July 2002 /JC-40 Committee	$43.00
JESD 82-6	**DEFINITION OF THE SSTV32852 2.5-V 24-BIT TO 48-BIT SSTL_2 REGISTERED BUFFER FOR 1U STACKED DDR DIMM APPLICATIONS:** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTV32852 24-bit to 48-bit SSTL_2 registered buffer for stacked DDR DIMM applications. The purpose is to provide a standard for the SSTV32852 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. November 2002 JC-40.4	$43.00
JESD 82-7	**DEFINITION OF THE SSTU32864 1.8-V CONFIGURABLE REGISTERED BUFFER FOR DDRII RDIMM APPLICATIONS:** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTU32864 configurable registered buffer for DDR-II RDIMM applications. The purpose is to provide a standard for the SSTU32864 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. November 2002 JC-40.4	$47.00
JESD 82-9	**Definition of SSTU32865 Registered Buffer with Parity for 2R x 4 DDR2 RDIMM Applications** This standard provides the functional definition, ball-out configuration and package outline, signal definitions and input/output characteristics for a 28-bit 1:2 registered driver with parity suitable for use on DDR2 RDIMMs. The SSTU32865 integrates the functional equivalent of two SSTU32864 devices (as defined in JESD82-7) into a single device, thereby easing layout and board design constraints especially on high density RDIMMs such as dual rank, by four configurations. Moreover, the optional use of a parity function is provided for, permitting detection and reporting of parity errors across its 22 data inputs. JESD82-9 specifies a 160-pin Thin-profile, fine-pitch ball-grid array (TFBGA) package. September 2003 March 2003 JC-40.4	$49.00

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JESD 85

METHODS FOR CALCULATING FAILURE RATES IN UNITS OF FITS: This standard establishes methods for calculating failure rates in units of FITs by using data in varying degrees of detail such that results can be obtained from almost any data set. The objective is to provide a reference to the way failure rates are calculated.

July 2001 /JC-14.3 Subcommittee $55.00

JESD 86

ELECTRICAL PARAMETERS ASSESSMENT: This standard is intended to describe various methods for obtaining electrical variate data on devices currently produced on the manufacturing and testing process to be qualified. The intent is to assess the device's capability to function within the specification parameters over time and the application environment (operating range of temperature, voltage, humidity, input/output levels, noise, power supply stability etc.).

August 2001 /JC-14.3 Subcommittee $38.00

JESD 87

STANDARD TEST STRUCTURE FOR RELIABILITY ASSESSMENT OF AlCu METALLIZATIONS WITH BARRIER MATERIALS This document describes design of test structures needed to assess the reliability of aluminum-copper, refractory metal barrier interconnect systems. This includes any metal interconnect system where a refractory metal barrier or other barrier material prevents the flow of aluminum and/or copper metal ions from moving between interconnect layers. This document is not intended to show design of test structures to assess aluminum or aluminum-copper alloy systems, without barriers to Al and Cu ion movement, nor for Cu only metal systems. Some total interconnect systems might not include barrier materials on all metal layers. The structures in this standard are designed for cases where a barrier material separates two Al or Al alloy metal layers. The purpose of this document is to describe the design of test structures needed to assess electromigration (EM) and stress-induced-void (SIV) reliability of AlCu barrier metal systems.

July 2001 /JC-14.2 Subcommittee $43.00

JESD 88

DICTIONARY OF TERMS FOR SOLID STATE TECHNOLOGY, First Edition: This reference for technical writers and educators, manufacturers, and buyers and users of discrete solid state devices is now available. It should aid the technical committees of JEDEC in the avoidance of multiple definitions and reduce the proliferation of redundant definitions. The long-term goal is to include definitions from all JEDEC publications and standards. Even in this first edition, that goal has been largely met. Each of the approximately two thousand entries is referenced to its source publication, and an annex listing the names of the source publications and their releases dates is included. All entries were reviewed for punctuation, grammar, and clarity, as well as accuracy, and reworded if such was considered warranted. The purpose of this dictionary is to promote the uniform use of terms, definitions, abbreviations, and symbols throughout the solid state industry.

September 2001 /JC-10 Committee $50.00

JESD 89

MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES: This specification defines the standard requirements and procedures for terrestrial soft-error-rate (SER)testing of integrated circuits and reporting of results. Both real-time (unaccelerated) and acceleratedtesting procedures are described. At terrestrial, Earth-based altitudes, the predominant sources ofradiation include both cosmic-ray radiation and alpha-particle radiation from radioisotopic impurities in the package and chip materials. An overall assessment of a device's SER is complete, only when an unaccelerated test is done, or accelerated SER data for the alpha-particle component and the cosmic-radiation component has been obtained.

August 2001 /JC-13.4 Subcommittee $83.00

JESD 91-A

METHOD FOR DEVELOPING ACCELERATION MODELS FOR ELECTRONIC COMPONENT FAILURE MECHANISMS: The method described in this document applies to all reliability mechanisms associated with electronic components.The purpose of this standard is to provide a reference for developing acceleration models for defect-related and wear-out mechanisms in electronic components.

August 2003 /JC-14.3 Subcommittee $49.00

JESD 92

PROCEDURE FOR CHARACTERIZING TIME-DEPENDENT DIELECTRIC BREAKDOWN OF ULTRA-THIN GATE DIELECTRICS: This document defines a constant voltage stress test procedure for characterizing time-dependent dielectric breakdown or "wear-out" of thin gate

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dielectrics used in integrated circuit technologies. The test is designed to obtain voltage and temperature acceleration parameters required to estimate oxide life at use conditions. The test procedure includes sophisticated techniques to detect breakdown in ultra-thin films that typically exhibit large tunneling currents and soft or noisy breakdown characteristics. This document includes an annex that discusses test structure design, methods to determine the oxide electric field in ultra-thin films, statistical models, extrapolation models, and example failure-rate calculations.

August 2003 July 2002 /JC-14.2 Subcommittee $57.00

JESD 99-1 **ADDENDUM No. 1 to JESD99 - TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS:** This addendum has now been incorporated into JESD99-A.

July 1989; Incorporated into JESD99-A, May 2000 /JC-10 Committee

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JESD 99A.01 **TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROELECTRONIC DEVICES:** This standard will be useful to users, manufacturers, educators, technical writers, and others interested in the characterization, nomenclature, and classification of microelectronics devices. There are general guidelines for both letter symbols and abbreviations applicable to all integrated circuits, and detailed sections for digital ICs, linear (analog) ICs, interface ICs (including D/A and A/D converters), voltage regulators, charge-transfer devices. The standard lists and defines more than 400 of the most common physical and electrical terms applicable to these devices and shows the industry-standard symbol and abbreviations that have been established for such terms. JESD99A.01 is the first minor revision of JESD99A, May 2000. Annex A briefly shows entries that have changed.

May 2003 /JC-10 Committee $127.00

JESD 100B.01 **TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS, MICROPROCESSORS, AND MEMORY INTEGRATED CIRCUITS:** A revised reference for technical writers and educators, manufacturers, buyers and users of microprocessors, microcomputers, mircocontrollers, memory ICs, and other complex devices. The terms and their definitions in this standard have been updated and are in general agreement with the latest publications of the IEEE and the IEC. The companion standard for other integrated circuits is JESD99A. Also included is a system for generating symbols for time intervals found in complex sequential circuits, including memories. JESD100B.01 is the first minor revision of JESD100-B, December 1999. Annex A briefly shows entries that have changed.

December 2002 /JC-10 Committee $71.00

JESD 22-B111 **BOARD LEVEL DROP TEST METHOD OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS:** This Board Level Drop Test Method is intended to evaluate and compare drop performance of surface mount electronic components for handheld electronic product applications in an accelerated test environment, where excessive flexure of a circuit board causes product failure. The purpose is to standardize the test board and test methodology to provide a reproducible assessment of the drop test performance of surface mounted components while duplicating the failure modes normally observed during product level test.

July 2003 /JC-14.1 Subcommittee $48.00

JESD 282B.01 **SILICON RECTIFIER DIODES:** This standard provided definitions, electrical characteristics circuit technology, letter symbols and registration format for diodes and stacks. It also covers rating and characteristics, manufacturing and performance as well as test practices to demonstrate the performance of semiconductor rectifier diodes and rectifier stacks used for the conversion and/or control of electric power. This version contains minor revisions to JESD282-B, April 2000.

November 2002 /JC-22.2 Subcommittee $177.00

JESD 284-A **TEST METHODS FOR THE COLLECTOR-BASE TIME CONSTANT AND FOR THE RESISTIVE PART OF THE COMMON-EMITTER INPUT IMPEDANCE:** The test methods described in this Standard are generally applicable to alloy-like devices for which the usual simplified equivalent circuits can be employed.

November 1963; Reaffirmed November 1963, June 1972, April 1981, April 1999, October 2002 /JC-25 Committee $38.00

JESD 286-B **STANDARD FOR MEASURING FORWARD SWITCHING CHARACTERISTICS OF SEMICONDUCTOR DIODES:** This method updates the standard procedure for characterizing the switching of

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signal or switching diodes when a step function of forward current is applied. The objective is to provide a standard so that accurate comparisons can be made.

February 2000 /JC-22.4 Subcommittee $40.00

JESD 307

VOLTAGE REGULATOR DIODE NOISE VOLTAGE MEASUREMENT: This standard is intended to cover the measurement of noise voltage in voltage regulator diodes in the reverse breakdown region. It describes noise voltage measurements at specified conditions, but may be used as a guide for making such measurements at other than specified conditions. (Formerly EIA-307)

May 1965; Reaffirmed January 1992, April 1999, April 2002 April 2002 /JC-22.4 Subcommittee $38.00

JESD 313-B

THERMAL RESISTANCE MEASUREMENTS OF CONDUCTION COOLED POWER TRANSISTORS: This standard provides a test method for measuring thermal resistance for conduction cooled power transistors.

October 1975; Reaffirmed April 1981, March 2001 /JC-25 Committee $45.00

JESD 320-A

CONDITIONS FOR MEASUREMENT OF DIODE STATIC PARAMETERS: This standard provides guidance for achieving equilibrium when measuring temperature sensitive static parameters of signal diodes. (Formerly EIA-302-A)

December 1992; Reaffirmed April 1999, April 2002 (Original publication July 1965) /JC-22.4 Subcommittee $37.00

JESD 381-A

METHOD OF DIODE Q MEASUREMENT: This standard was updated and revised for the purpose of clarifying the method used to measure Q of a Voltage-Variable-Capacitance Diode in the low VHF range using an RF admittance bridge. Originally published November 1981. Approved as ANSI/EIA-381-A-1992, July 1992. Became JESD381-A after ANSI expiration July 2002.

November 1981; Reaffirmed April 1999, April 2002 April 1999 /JC-22.4 Subcommittee $48.00

JESD 419-A

STANDARD LIST OF VALUES TO BE USED IN SEMICONDUCTOR DEVICE SPECIFICATIONS AND REGISTRATION FORMAT: This document contains standard lists of values which are recommended for use in semiconductor device specification and JEDEC Registration Formats. Good reasons should exist in those cases where values are used that are not included in these lists.

October 1980; Reaffirmed March 2001 /JC-25 Committee $37.00

JESD 482-A

LIST OF PREFERRED VALUES FOR USE ON VARIOUS TYPES OF SMALL SIGNAL AND REGULATOR DIODES: This standard specifies preferred values to be used on signal and regulator diodes. It will facilitate the standardization for nominal values used on small signal regulator diodes previously established in JEDEC Suggested Standard No. 2. (Formerly EIA-482-A)

August 1984; Reaffirmed April 1999, April 2002 April 2002 /JC-22.4 Subcommittee $38.00

JESD 531

THERMAL RESISTANCE TEST METHOD FOR SIGNAL AND REGULATOR DIODES (FORWARD VOLTAGE, SWITCHING METHOD): This standard describes a test method for measuring the thermal resistance of signal and regulator diodes. The need for modification of this test method arose out of the limited description that existed earlier for both signal and regulator diode applications in testing for thermal resistance. Previously published as ID-13. ANSI/EIA-531-1986 (July) expired June 1996. Became JESD531 after reaffirmation April 2002.

July 1986; Reaffirmed April 1999, April 2002 April 1999 /JC-22.4 Subcommittee $47.00

JESD 625-A

REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES: This standard establishes the minimum requirements for Electrostatic Discharge (ESD) control methods and materials used to protect electronic devices that are susceptible to damage or degradation from electrostatic discharge (ESD). The passage of a static charge through an electrostatic-discharge-sensitive (ESDS) device can result in catastrophic failure or performance degradation of the part. Device sensitivity to ESD is determined by test methods such as EIA/JESD22-A114. ESDS devices with human body model sensitivities of less than +200 volts may need additional protective measures beyond those specified in this standard.

December 1999 /JC-14.1 Subcommittee $55.00

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JESD 659-A	**FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING:** This method establishes requirements for application of Statistical Reliability Monitoring 'SRM' technology to monitor and improve the reliability of electronic components and subassemblies. The standard also describes the condition under with a monitor may be replaced or eliminated. September 1999 /JC-14.3 Subcommittee	$48.00
JESD 671-A	**COMPONENT QUALITY PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS (INCLUDING ADMINISTRATIVE QUALITY PROBLEMS):** This revision now encompasses administrative quality problems, in addition to the electrical and visual/mechanical quality problems that were addressed in the original release. A standard set of problem categories for each of these three types of component problems is presented for tracking and reporting purposes. A common set of customer and supplier expectations and requirements are set forth to help facilitate the successful problem analysis and corrective action of any type of component quality problem. December 1999 /JC-14.4 Subcommittee	$43.00
JESD 82-8	**STANDARD FOR DEFINITION OF ◆CU877 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a ◆CU877 PLL clock device for registered DDR2 DIMM applications. The purpose is to provide a standard for a ◆CU877 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. July 2003 /JC-40 Committee	$49.00

NUMBER	Joint IPC/JEDEC Standards (J-STD-)	PRICE
J-STD- 002B	**SOLDERABILITY TESTS FOR COMPONENT LEADS, TERMINATIONS, LUGS, TERMINALS AND WIRES:** This standard prescribes test methods, defect definitions, acceptance criteria, and illustrations for assessing the solderability of electronic component leads, terminations, solid wire, stranded wire, lugs, and tabs. This standard is intended for use by both vendor and user. February 2003 /JC-13 Committee	
J-STD- 020B	**JOINT IPC/JEDEC STANDARD FOR MOISTURE/REFLOW SENSITIVITY CLASSIFICATION FOR NONHERMETIC SOLID STATE SURFACE-MOUNT DEVICES:** This document identifies the classification level of nonhermetic solid-state surface mount devices (SMDs) that are sensitive to moisture-induced stress. It is used to determine what classification level should be used for initial reliability qualification. Once identified, the SMDs can be properly packaged, stored and handled to avoid subsequent thermal and mechanical damage during the assembly solder reflow attachment and/or repair operation. This revision now covers components to be processed at higher temperatures for lead-free assembly. A hard cop version is available for $20 each for IPC/JEDEC members and $40 for nonmembers. July 2002 /JC-14.1 Subcommittee	
J-STD- 033A	**JOINT IPC/JEDEC STANDARD FOR HANDLING, PACKING, SHIPPING AND USE OF MOISTURE/REFLOW SENSITIVE SURFACE-MOUNT DEVICES:** This document provides SMD manufacturers and users with standardized methods for handling, packing, shipping and use of moisture/reflow sensitive SMDs. Now updated to support components that may need to be processed at higher temperatures, such as lead-free processes, these methods help avoid damage from moisture absorption and exposure to solder reflow temperatures that can result in yield and reliability degradation. IPC/JEDEC J-STD-033A helps achieve safe and damage-free reflow with the dry packing process and provides a minimum shelf life of 12 months from the seal date when using sealed dry bags. Hard copies of this document are available for $20 each for IPC/JEDEC members and $40 for nonmembers. July 2002 /JC-14.1 Subcommittee	
J-STD- 035	**JOINT IPC/JEDEC STANDARD FOR ACOUSTIC MICROSCOPY FOR NONHERMETRIC ENCAPSULATED ELECTRONIC COMPONENTS:** This test method defines the procedures for performing acoustic microscopy on non-hermetic encapsulated electronic components. This method provides users with an acoustic microscopy process reflow for detecting defects non-destructively in plastic packages while achieving reproducibility. May 1999; Under Revision /JC-14.1 Subcommittee	$35.00

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NUMBER	Joint Publication (JP)	PRICE
JP 001	**FOUNDRY PROCESS QUALIFICATION GUIDELINES (Wafer Fabrication Manufacturing Sites)** This document provides a guideline for the minimum set of measurements to qualify a new semiconductor wafer process. It is written with particular reference to a generic silicon based CMOS logic technology. While it may be applicable to other technologies (e.g. analog CMOS, bipolar, BICMOS, GaAs, etc.), some sections apply specifically to CMOS. No effort was made in the present document to cover all the qualification requirements for specific other technologies, e.g. Cu/Low K interconnects or ultra thin gate oxide. This publication, is co-sponsored by JEDEC JC-14.2 and the FSA (Fabless Semiconductor Association). It originated at the FSA as a technology specific document, and has evolved into a generic set of qualification requirements. September 2002 /JC-14.2 Subcommittee	$65.00

NUMBER	JEDEC Publications (JEP)	PRICE
JEP 64	**SOLID STATE PRODUCTS REGISTRATION LIST(ORDER FROM TYPE ADMINISTRATION OFFICE):** This publication includes addenda from 1976 to August 1986. The purpose of this list is to determine release numbers (file numbers) for JEDEC Type Designations. (See page 6 for more information.) September 1986; Reaffirmed November 2002 / Committee!33JCJEDC	$162.00
JEP 65	**TEST PROCEDURES FOR VERIFICATION OF MAXIMUM RATINGS OF POWER TRANSISTORS:** This publication describes tests which are intended to represent the verification of maximum ratings for data sheets; they are not tests for performance or quality level. This material is to be used in conjunction with formats developed for device registration and defining data. December 1967; Reaffirmed September 1981, April 1999 /JC-25 Committee	$52.00
JEP 69-B	**PREFERRED LEAD CONFIGURATION FOR FIELD-EFFECT TRANSISTORS:** This publication indicates preferred pinouts for FETs in various package designs. November 1973; Reaffirmed September 1981, April 1999 /JC-25 Committee	$38.00
JEP 70-B	**QUALITY AND RELIABILITY STANDARDS AND PUBLICATIONS:** Contains a listing and description of commonly used quality and reliability related standards and publications that are applicable to the semiconductor industry. It is intended to be a reference aid in finding available standards and obtaining a copy from the source of the standard. It is not intended to recommend or imply the applicability of any standard for a specific purpose. This revision has been updated to include recent releases as well as revisions, in addition, URLs have been added to the October 1999 /JC-14.4 Subcommittee	$57.00
JEP 74	**STANDARD LIST OF VALUES TO BE USED IN POWER TRANSISTOR DEVICE REGISTRATION AND MINIMUM DIFFERENCES FOR DISCRETENESS OF REGISTRATIONS - SUPERSEDED BY EIA-419-A, February 1996.** July 1969; Rescinded February 1996 /JC-25 Committee	$38.00
JEP 75	**LETTER SYMBOLS USED WITH INFRARED DEVICES - INCORPORATED INTO JESD77-A.** August 1984; Rescinded August 1984 /JC-10 Committee	
JEP 78	**RELATIVE SPECTRAL RESPONSE CURVES FOR SEMICONDUCTOR INFRARED DETECTORS:** The intent of this publication is to facilitate the specification of infrared detector diodes, particularly in conjunction with the preparation of data for JEDEC type registration. October 1969 /JEDEC Committee	$52.00
JEP 79	**LIFE TEST METHODS FOR PHOTOCONDUCTIVE CELLS:** This publication is for photoconductive cells sensitive primarily in the visible and near infrared region. September 1969	$52.00
JEP 84	**RECOMMENDED PRACTICE FOR MEASUREMENT OF TRANSISTOR LEAD TEMPERATURE:** This publication covers recommended methods for measurement of transistor lead temperatures under various load conditions. The techniques described are sufficiently accurate for most applications.	

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February 1973; Reaffirmed February 1982 /JC-25 Committee $38.00

JEP 86-A **RECOMMENDED PRACTICE FOR DUAL DIMENSIONING**

May 1976; Rescinded November 1999 /JC-11 Committee

JEP 87 **FORWARD TURN-ON TIME MEASUREMENT ON SEMI-DIODES - INCORPORATED INTO EIA-282-A.**

June 1992; Rescinded June 1985 /JC-22.2 Subcommittee

JEP 88 **THERMAL RESISTANCE AND THERMAL IMPEDANCE TEST METHODS FOR STUD AND BASE-MOUNTED RECTIFIER DIODES AND THYRISTORS**

January 1974; Rescinded June 1992 /JC-22.1 Subcommittee

JEP 90 **THERMAL RESISTANCE FOR TEST METHODS FOR SIGNAL DIODES - SUPERSEDED BY EIA-531, July 1986. See JESD531, April 2002.**

September 1983; Rescinded September 1986 /JC-22.4 Subcommittee

JEP 93 **MICROELECTRONIC DEVICE TYPE ASSIGNMENTS**

August 1975; Rescinded June 1992 June 1992 / Committee!33JCJEDC

JEP 95 **JEDEC REGISTERED AND STANDARD OUTLINES FOR SOLID STATE AND RELATED PRODUCTS:** This publication is a compilation of some 1800 pages of outline drawings for microelectronic packages including transistors, diodes, DIPS, chip carriers and package interface BGA outlines in both inch and metric versions.

January 2000 /JC-11 Committee $350.00

JEP 95 AUS **ANNUAL UPDATING SERVICE:** Subscription to this updating service is available from the JEDEC Office. New outlines are shipped to subscribers for insertion into the appropriate sections of Publication No. 95. JEP95 and Updating Service can be ordered through JEDEC at (703)907-7540 or ptanner@jedec.org.

January 2000 /JC-11 Committee $110.00

JEP 95-1 **DESIGN REQUIREMENTS (Book 1, Section 4)** Type 'section' in the 'by document number' to see the contents of this document. This is currently under construction. Once it has been completed you will be able to click on the 'entire document' icon below and see all the sections contained in this document.

January 2000 /JC-11 Committee

JEP 96 **GUIDELINES FOR NONDESTRUCTIVE PULL TESTING OF WIRE BONDS ON HYBRID DEVICES**

March 1977; Rescinded April 2000 /JC-13.5 Subcommittee

JEP 99 **GLOSSARY OF MICROELECTRONIC TERMS, DEFINITIONS, AND SYMBOLS: ELEVATED TO JESD99, June 1985.**

July 1977; Rescinded June 1985 /JC-10 Committee

JEP 100 **TERMS, DEFINTIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS AND MEMORY INTEGRATED CIRCUITS: ELEVATED TO JESD100, August 1993.**

September 1979; Rescinded October 1983 /JC-10 Committee

JEP 101-C **JEDEC REQUIREMENTS FOR CLASS B MICROCIRCUITS:** This revision reflects the following changes in MIL-Specs: 1) The conversion form MIL-M-38510 to MIL-I-38535 (renamed MIL-PRF-38535) as the General Specification for Microelectronics Devices. 2)The transfer of "Compliancy Requirements" from General Provisions paragraph 1.2.1 of MIL-STD-883 to Appendix A of MIL-PRF-38535.

November 1995 /JC-13.2 Subcommittee $38.00

JEP 102 **STANDARD FOR 64K x 1 DYNAMIC RAM - SUPERSEDED BY JESD21-C.**

September 1978; Rescinded April 1985 April 1985 /JC-42 Committee

JEP 103A **SUGGESTED PRODUCT-DOCUMENTATION, CLASSIFICATIONS, AND DISCLAIMERS** In order to improve understanding between manufacturers and users, a consistent set of product-documentation classifications associated with the stages of product development.

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July 1996; Reaffirmed November 1999, May 2003 /JC-10 Committee $38.00

JEP 104C.01 **REFERENCE GUIDE TO LETTER SYMBOLS FOR SEMICONDUCTOR DEVICES:** This publication provides a quick reference to the letter symbols and corresponding terms that are defined in JESD77-B, Terms, Definitions, and Letter Symbols for Discrete Semiconductor and Optoelectronic Devices; JESD99-A, Terms, Definitions, and Letter Symbols for Microelectronic Devices, and JESD100-B, Terms, Definitions, and Letter Symbols for Microcomputers, Microprocessors, and Memory Integrated Circuits. It is intended to simplify interpretation of data sheets and specifications and to promote the uniform use of these symbols. The symbols relate to ratings and characteristics found in data sheets and other specifications. Some abbreviations used in lieu of symbols are also included. The newly added Annex B is provided as an aid to determining what symbol should be used and is organized by term, whereas the main body of the publication is organized by symbol or abbreviation as in previous versions. This version contains minor revisions.

May 2003 /JC-10 Committee $91.00

JEP 105 **JEDEC GUIDELINE FOR THE CHARACTERIZATION OF HYBRID POLYMERIC MATERIALS - SUPERSEDED BY JESD72, June 2001**

April 1983; Rescinded June 2001 /JC-13.5 Subcommittee

JEP 106M **STANDARD MANUFACTURERS IDENTIFICATION CODE:** The manufacturers identification code is defined by one or more 8 bit fields, each consisting of 7 data bits plus 1 odd parity bit. The manufacturers identification code is assigned, maintained and updated by the JEDEC Office. The intent of this identification code is that it may be used whenever a digital field is required, e.g., hardware, software, documentation, etc.

May 2003 /JC-42.3 Subcommittee $48.00

JEP 107 **TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF PARTICLE GETTERS FOR USE IN HYBRID MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001**

April 1985; Rescinded June 2001 /JC-13.5 Subcommittee

JEP 108-B **DISTRIBUTOR REQUIREMENTS FOR HANDLING ELECTROSTATIC -DISCHARGE SENSITIVE (ESDS) DEVICES: SUPERSEDED BY JESD42, March 1994.**

April 1991; Superseded /JC-14.1 Subcommittee

JEP 109-C **GENERAL REQUIREMENTS FOR DISTRIBUTORS OF MILITARY SEMICONDUCTOR DEVICES:** Superseded by JESD31-A, June 2001.

March 1995; Rescinded November 2001 /JC-13 Committee

JEP 110 **GUIDELINES FOR THE MEASUREMENT OF THERMAL RESISTANCE OF GaAs FETS:** This publication is intended for power GaAs FET applications requiring high reliability. An accurate measurement of thermal resistance is extremely important to provide the user with knowledge of the FETs operating temperature so that more accurate life estimates can be made. FET failure mechanisms and failure rates have, in general, an exponential dependence on temperature (which is why temperature-accelerated testing is successful). Because of the exponential relationship of failure rate with temperature, the thermal resistance should be referenced to the hottest part of the FET.

July 1988 /JC-14.7 Subcommittee $43.00

JEP 111 **TEST PROCEDURES FOR CUSTOM MONOLITHIC MICROCIRCUITS - SUPERSEDED BY MIL-PRF-38535C.**

July 1986; Rescinded June 1996 June 1996 /JC-13.2 Subcommittee

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JEP 112 **TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF CIRCUIT SUPPORT FILMS FOR USE IN MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001**

June 1987; Rescinded June 2001 /JC-13 Committee $52.00

JEP 113-B **SYMBOL AND LABELS FOR MOISTURE-SENSITIVE DEVICES:** Certain PSMC (Plastic Surface-mount Components) are subject to permanent damage due to moisture-induced failures encountered during high-temperature surface-mount processing unless appropriate precautions are observed. The purpose of this publication is to provide a distinctive symbol and labels to be used to identify those devices that require special packing and handling precautions.

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May 1999 /JC-14.1 Subcommittee $45.00

JEP 114 **GUIDELINES FOR PARTICLE IMPACT NOISE DETECTION (PIND) TESTING, OPERATOR TRAINING, AND CERTIFICATION:** This publication was developed to help the user of this test methodology avoid common interference's to successful application. The guide contains sections on typical specification requirements, sources of particles, PIND test systems, calibration, maintenance, test interference's, operator training, particle recovery and failure analysis. Application of the information contained in the guide will improve the quality and affectivity for any PIND testing operation.

December 1989; Under Revision /JC-13 Committee $61.00

JEP 115 **POWER MOSFET ELECTRICAL DOSE RATE TEST METHOD:** The purpose of this Test Method is to establish electrical criteria for comparing and specifying power MOSFET performance under high dose rate radiation.

August 1989; Reaffirmed April 1999 /JC-25 Committee $41.00

JEP 116 **CMOS SEMICUSTOM DESIGN GUIDELINES:** The design of ASIC circuits is becoming a significant part of system or product design, yet many problems continue to exist in current design practice. The guidelines in this document provide an explanation of common ASIC design problems and concerns and where possible offer solutions.

November 1991 / Committee!33JC44 $109.00

JEP 117 **GUIDELINES FOR USER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS - SUPERSEDED BY JESD46, August 1997.**

April 1994; Rescinded July 1994 /JC-14.4 Subcommittee

JEP 118 **GUIDELINES FOR GaAs MMIC AND FET LIFE TESTING:** These guidelines apply to monolithic microwave GaAs integrated circuits (MMICs) and their individual component building blocks, such as GaAs field effect transistors (FETs), resistors, and capacitors. The purpose of this document is to define a standard approach for evaluating the expected live of GaAs MMICs so that results from different life tests can be compared and so that wording of this document that the MMIC contains at least one FET, but the use of this document has no such limitation.

January 1993 /JC-14.7 Subcommittee $48.00

JEP 119A **A PROCEDURE FOR EXECUTING SWEAT:** This document describes an algorithm for performing the Standard Wafer Level Electromigration Accelerated Test (SWEAT) method with computer controlled instrumentation. The algorithm requires a separate iterative technique (not provided) to calculate the force current for a given target time to failure. This document does not specify what test structure to use with this procedure. However, users of this algorithm report its effectiveness on both straight-lines and via-terminated test structures. Some test-structures design features are provided in JESD87 and in ASTM 1259M - 96.

August 2003 /JC-14.2 Subcommittee $57.00

JEP 120-A **INDEX OF TERMS DEFINED IN JEDEC PUBLICATIONS:** This publication provides an index to terms that are defined in certain JEDEC publications. It is intended to promote the uniform use of these terms and their definitions while reducing the proliferation of new definitions for old terms.

May 2000 /JC-10 Committee $109.00

JEP 121 **GUIDELINES FOR MIL-STD-883 SCREENING AND QCI OPTIMIZATION:** The intent of this publication was developed to establish uniform guidelines, which would allow the use of In-Line Process Controls and Statistical Process Control as viable alternatives to the 100% screens and

April 1995 /JC-13 Committee $109.00

JEP 122-B **FAILURE MECHANISMS AND MODELS FOR SILICON SEMICONDUCTOR DEVICES:** This publication provides a list of failure mechanisms and their associated activation energies or acceleration factors that may be used in making system failure rate estimations when the only available data is based on tests performed at accelerated stress test conditions. The method to be used is the Sum of the Failure Rates method.

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August 2003 /JC-14.1 Subcommittee $63.00

JEP 123 **GUIDELINE FOR MEASUREMENT OF ELECTRONIC PACKAGE INDUCTANCE AND CAPACITANCE MODEL PARAMETERS:** The need for this guideline arose from widespread lack of consistency in characterizing electrical parameters of electronic packages, which existed in the industry until the early 1990s. Then, the JEDEC Committee JC-15 provided the forum where various methods were discussed and commonality in approach emerged. The result is that today we have relatively consistent results in measuring and reporting electrical package parameters, as well as specialized tools (e.g., the IPA-510, the interconnect parameter analyzer) which were developed to support the methodology.

October 1995 /JC-15.2 Subcommittee $49.00

JEP 124 **GUIDELINES FOR THE PACKING, HANDLING, AND REPACKING OF MOISTURE-SENSITIVE COMPONENTS - SUPERSEDED BY J-STD-033, May 1999.**

December 1995; Rescinded November 1999 November 1999 /JC-14.4 Subcommittee

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JEP 126 **GUIDELINE FOR DEVELOPING AND DOCUMENTING PACKAGE ELECTRICAL MODELS DERIVED FROM COMPUTATIONAL ANALYSIS:** This publication provides a guideline to suppliers of IC components with a template for documenting the numerical simulation assumptions. In addition this guideline also suggests a model environment to reference when comparing various packages or component suppliers. This publication should improve the communication between the package model suppliers. This publication should improve the communication between the package model supplier and the end user.

May 1996 /JC-15.2 Subcommittee $38.00

JEP 128 **GUIDE FOR STANDARD PROBE PAD SIZES AND LAYOUTS FOR WAFER LEVEL ELECTRICAL TESTING:** This guide was developed to expedite inter-laboratory experiments used to evaluate or develop standard test methods that involve test-structure measurements or tests. It also facilitates, generally, any electrical tests that require wafer-probe card to make electrical contact to test structures. Widespread use of this guide will afford the efficient and cost-effective use of water-probe test stations because of the need for fewer probe cards and probe-card changes to accommodate the various test structures that may need to be tested.

November 1996 /JC-14.2 Subcommittee $40.00

JEP 129 **THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP)- SUPERSEDED BY JESD51-4, September 1997.**

February 1997; Elevated September 1997 /JC-15.1 Subcommittee

JEP 130 **GUIDELINES FOR PACKING AND LABELING OF INTEGRATED CIRCUITS IN UNIT CONTAINER PACKING:** This document establishes guidelines for integrated circuit unit container and the next level (intermediate) container packing and labeling. The guidelines include tube/rail standardization, intermediate packing, date codes, tube labeling, intermediate container and shipping labels, and standardize tube quantities. Future revisions of this document will also include tray and reel guidelines. The objective of this publication is to promote the standardization of practices between manufacturers and distributors resulting in improved efficiency, profitability, and product quality.

August 1997 /JC-14.4 Subcommittee $40.00

JEP 131 **PROCESS FAILURE MODE AND EFFECTS ANALYSIS (FMEA):** This publication was created in response to the need for a straight forward FMEA procedure. The objective is to provide a guideline for the application of FMEA techniques to improve quality, reliability and/or consistency of electronic components and subassemblies by continually evaluating processes/products against potential failure modes.

February 1998 /JC-14.3 Subcommittee $48.00

JEP 132 **PROCESS CHARACTERIZATION GUIDELINE:** This guideline provides a methodology to characterize a new or existing process and is applicable to any manufacturing or service process. It describes when to use specific tools such as failure mode effects analysis (FEMA), design or experiments (DOE), measurement system evaluation (MSE), capability analysis (CpK), statistical process control (SPC), and problem solving tools. It also provides a brief description of each tool.

July 1998 /JC-13 Committee $59.00

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JEP 133-A

GUIDE FOR THE PRODUCTION AND ACQUISITION OF RADIATION-HARDNESS ASSURED MULTICHIP MODULES AND HYBRID MICROCIRCUITS: A revised and expanded publication for suppliers and users of radiation hardness assured (RHA) multichip modules (MCMs) and hybrid microcircuits, is now available. Revision A of JEP133 includes modifications to the introduction, clarification of a definition and clarification of several technical issues within the document. In addition, the Bibliography section was updated to include added references. The document provides guidance as to how to achieve, maintain and ensure required levels of radiation-hardness given the fact that the constituent dice can have different levels of hardness assurance. It also describes how to deal with the various radiation hardness situations that an MCM/Hybrid developer, procuring activity or user will encounter. The guide is intended to supplement three relevant performance specifications: MIL-PRF-38534, MIL-PRF-38535 and MIL-PRF-19500.

July 2001 /JC-13.5 Subcommittee $59.00

JEP 134

GUIDELINES FOR PREPARING CUSTOMER-SUPPLIED BACKGROUND INFORMATION RELATING TO A SEMICONDUCTOR-DEVICE FAILURE ANALYSIS: The purpose of this Guideline is to provide a vehicle for acquiring and transmitting the necessary information in a concise, organized, and consistent format. Included in the Guideline is a sample form that facilitates transferring the maximum amount of background data to the failure analyst in a readily interpretable format. Immediate availability of this key information assists that analyst in completing a timely and accurate failure analysis.

September 1998 /JC-14.6 Subcommittee $45.00

JEP 136

SIGNATURE ANALYSIS: Signature Analysis is a method to reduce the number of comprehensive physical failure analyses by the application of statistical inference techniques. The purpose of this document is to promote a common definition of Signature Analysis by inference, using the same statistical techniques, and to recognize that it is formal means of doing failure analysis.

July 1999 /JC-14.6 Subcommittee $47.00

JEP 137-A

COMMON FLASH INTERFACE (CFI) IDENTIFICATION CODES: This publication is a companion document to the Common Flash Interface (CFI) standard, JESD68, which outlines the device and host system software interrogation handshake. JEP137 documents ID Code assignments for: 1)) the Algorithm-specific Command Set and Control Interfaces and 2) the Device Interfaces. It is published as needed when additions are made to either of these lists of codes. To make a request for an ID Code please contact the JEDEC Office at (703)907-7558.

September 2001 /JC-42.4 Subcommittee $41.00

JEP 138

USER GUIDELINES FOR IR THERMAL IMAGING DETERMINATION OF DIE TEMPERATURE: The purpose of these user guidelines is to provide background and an example for the use of an infrared (IR) microscope to determine die temperature of electronic devices for calculations such as thermal resistance.

September 1999 /JC-25 Committee $41.00

JEP 139

GUIDELINE FOR CONSTANT TEMPERATURE AGING TO CHARACTERIZE ALUMINUM INTERCONNECT METALLIZATIONS FOR STRESS-INDUCED VOIDING: This document describes a constant temperature (isothermal) aging method for testing aluminum (Al) metallization test structures on microelectronics wafers for susceptibility to stress-induced voiding. This method is valid for metallization/dielectric systems in which the dielectric is deposited onto the metallization at a temperature considerably above the intended use temperature, and above or equal to the deposition temperature of the metal. Although this is a wafer test, it is not a fast (less than 5 minutes per probe) test. It is intended to be used for lifetime prediction and failure analysis, not for production Go-NoGo lot checking.

December 2000 /JC-14.2 Subcommittee $47.00

JEP 140

BEADED THERMOCOUPLE TEMPERATURE MEASUREMENT OF SEMICONDUCTOR PACKAGES: The beaded thermocouple temperature measurement guideline provides a procedure to accurately and consistently measure the temperature of semiconductor packages during exposure to thermal excursions. The guideline applications can include, but not limited to, temperature profile measurement in reliability test chambers and solder reflow operations that are associated with component assembly to printed wiring boards.

June 2002 /JC-14.1 Subcommittee $43.00

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JEP 142	GUIDELINE FOR OBTAINING AND ACCEPTING MATERIAL FOR USE IN HYBRID / MCM PRODUCTS: This document provides guidance regarding design considerations, material assessment techniques, and recommendations for material acceptance prior to use in Hybrid / MCM Products. As part of the risk assessment process, both technical requirements and cost should be carefully considered with regard to testing / evaluating the elements of a hybrid microcircuit or Multi-chip Module (MCM) prior to material release for assembly. The intent of this document is to highlight various options that are available to the Hybrid / MCM manufacturer and provide associated guidance, not to impose a specific set of tests. May 2002 /JC-13.5 Subcommittee	$55.00
JEP 143	SOLID STATE RELIABILITY ASSESSMENT QUALIFICATION METHODOLOGIES: This publication is a reference for the suite of reliability, modeling and qualification documents and publications that available through JEDEC. It provides background on reliability assessment and qualification methodologies and includes a brief overview on each of the pertinent documents and publications. November 2001 /JC-14.3 Subcommittee	$45.00
JEP 144	GUIDELINE FOR RESIDUAL GAS ANALYSIS (RGA) FOR MICROELECTRONIC PACKAGES The intent of this document is to give guidance on the Residual Gas Analysis (RGA) process and surrounding issues. The guideline describes how to select a suitable test lab and includes RGA history, measurement methodology, and issues that arise with the test. Interpreting the lab results along with common failure mechanisms are discussed at length along with process controls and alternative test techniques for measuring the moisture content within packages. July 2002 /JC-13 Committee	$57.00
JEP 145	GUIDELINE FOR ASSESSING THE CURRENT-CARRYING CAPABILITY OF THE LEADS IN A POWER PACKAGE SYSTEM: This publication is intended as a guideline to establish procedures, consideration and common practices that will allow a manufacturer, an application entity, a system designer and other interested parties to define current capability limitations in the leads of components and power systems with semiconductor components. This is a guideline, not a standardized method, it was developed over several years to clarify questions that had been posed to committee members in their respective engineering functions. February 2003 /JC-25 Committee	$41.00
JEP 146	GUIDELINES FOR SUPPLIER PERFORMANCE RATING: The intent of this document is to establish guidelines and provide examples by which customers can measure their suppliers based on mutually agreed upon objective criteria. These results can then be used to improve communications between customers and suppliers. June 2003 September 2002 /JC-14.4 Subcommittee	$47.00
JEP 147	PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER (VNA): This procedure describes a recommended way to measure pin capacitance of devices with SSTL (Stub Series Terminated Logic) interface pins by use of a Vector Network Analyzer. One purpose of this standard procedure is to reduce the lengthy and often inaccurate footnote - usually found around the specification of pin parasitics - to a simple reference to this document. In special cases modifying statements may adjust this procedure to the special needs of certain component. October 2003 December 2002 JC-16.2	$41.00

NUMBER	EIA Standards (EIA)	PRICE
EIA 236-C	COLOR CODING OF DISCRETE SEMICONDUCTOR DEVICES: This standard details the methods to be followed if color coding is used to identify JEDEC-assigned type numbers or for cathode identification of discrete semiconductor devices. ANSI/EIA-236-C-1986. March 1986; Reaffirmed November 1999 /JC-10 Committee	$38.00
EIA 282-A	STANDARD FOR SILICON RECTIFIER DIODES: SEE JESD282-B ANSI/EIA-282-A-1989 February 1990 Became JESD282-B after revision April 2000 /JC-22.2 Subcommittee	
EIA 283	TEST METHOD FOR TRANSISTOR NOISE FIGURE MEASUREMENTS AT MEDIUM FREQUENCIES - SUPERSEDED BY EIA-311-A.	

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November 1963; Rescinded November 1981 November 1981 /JC-25 Committee

EIA 284-A **TEST METHODS FOR THE COLLECTOR-BASE TIME CONSTANT AND FOR THE RESISTIVE PART OF THE COMMON-EMITTER INPUT IMPEDANCE: SEE JESD284A.** EIA-284-A became JESD284A after reaffirmation in October 2002.

November 1963; Reaffirmed /JC-25 Committee

EIA 286-A **STANDARD FOR MEASURING FORWARD SWITCHING CHARACTERISTICS OF SEMICONDUCTOR DIODES: SEE JESD286-B.** ANSI/EIA-286-A-1991.

February 1991 Became JESD286-B after revision February 2000 /JC-22.4 Subcommittee

EIA 302 **RANGES AND CONDITIONS FOR SPECIFYING BETA FOR LOW POWER, AUDIO FREQUENCY TRANSISTORS FOR ENTERTAINMENT SERVICE:** This standard establishes the preferred rating ranges and conditions for specifying beta for low power, audio frequency transistors intended for entertainment service.

January 1965; Reaffirmed April 1981, April 1999 /JC-25 Committee $37.00

EIA 306 **MEASUREMENT OF SMALL SIGNAL HF, VHF, AND UHF POWER GAIN OF TRANSISTORS:** This standard provides a method of measurement for small-signal HF, VHF, and UHF power gain of low power transistors.

May 1965; Reaffirmed April 1981, April 1999 /JC-25 Committee $38.00

EIA 308-A **PREPARATION OF OUTLINE DRAWINGS OF SOLID-STATE PRODUCTS FOR JEDEC TYPE REGISTRATION:** This standard is intended to serve as a guide to manufacturers of solid state products for the preparation of outline drawings of solid state product packages for JEDEC type registration.

August 1981 /JC-11 Committee $38.00

EIA 311-A **MEASUREMENT OF TRANSISTOR NOISE FIGURE AT MF, HF, AND VHF:** This standard describes a test method for measurement of transistor noise figure and effective input noise temperature at MF, HF, and VHF. This standard also adds the necessary information to make 'effective input noise temperature measurements'. This method is a revision of EIA-311 and incorporates material previously found in EIA-283.

November 1981; Reaffirmed April 1999 /JC-25 Committee $48.00

EIA 318-B **MEASUREMENT OF REVERSE RECOVERY TIME FOR SEMICONDUCTOR SIGNAL DIODES:** This standard describes the measurement of signal diodes (I_F <=500mA dc) reverse recovery times of less than 300 ns duration. It may, however, also be used for the measurement of longer recovery times. This standard is also intended to establish a method which to characterize the test fixture used for this measurement.

July 1996; Reaffirmed April 1999 /JC-22.4 Subcommittee $47.00

EIA 321-C **NUMBERING OF LIKE-NAMED TERMINAL FUNCTIONS IN SEMICONDUCTOR DEVICES AND DESIGNATION OF UNITS IN MULTIPLE-UNIT SEMICONDUCTOR DEVICES:** This standard gives the system for numbering like-named electrodes or terminal functions in semiconductor devices and for assigning numerical designations to units of multiple-unit semiconductor devices. It applies to both integrated circuits and discrete devices. ANSI/EIA-321-C-1987

February 1987; Reaffirmed November 1995 November 1995 /JC-10 Committee $41.00

EIA 323 **AIR-CONVECTION-COOLED, LIFE TEST ENVIRONMENT FOR LEAD-MOUNTED SEMICONDUCTOR DEVICES:** This standard is applicable to life testing of lead-mounted semiconductor devices intended for applications in a natural air-cooled environment where most of the power dissipation is obtained by convection and radiation losses from the body to the device.

March 1966; Reaffirmed February 1972 February 1972 /JC-22.1 Subcommittee $40.00

EIA 340 **STANDARD FOR THE MEASUREMENT OF CRE:** This standard offers an easily measured parameter which is one of the significant characteristics in determining the stability of a transistor intended for small-signal operation. The measurement technique allows rapid testing. Its correlation to AC stability will help to establish the interchangeability of a device.

November 1967; Reaffirmed April 1981, April 1999 /JC-25 Committee $43.00

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EIA 353 **THE MEASUREMENT OF TRANSISTOR NOISE FIGURE AT FREQUENCIES UP TO 20 kHz BY SINUSOIDAL SIGNAL-GENERATOR METHOD:** This noise measurement method applies to transistors whose noise has a Gaussian power distribution, to transistors whose noise has a flat (white) power distribution, and to transistors whose noise has a l/f (power inversely proportional to frequency) power distribution.

April 1968; Reaffirmed April 1981, April 1999 /JC-25 Committee $40.00

EIA 354 **THE MEASUREMENT OF TRANSISTOR EQUIVALENT NOISE VOLTAGE AND EQUIVALENT NOISE CURRENT AT FREQUENCIES OF UP TO 20 kHz:** This standard provides a method for determining values, for device registration purposes, for transistor equivalent noise voltage and equivalent noise current at frequencies up to 20 kHz. This method is applicable to transistors whose noise has a Gaussian, flat (white) or I/f power distribution.

April 1968; Reaffirmed April 1981, April 1999 /JC-25 Committee $40.00

EIA 365 **PERFORMANCE TEST PROCEDURE FOR SOLAR CELLS AND CALIBRATION PROCEDURE FOR SOLAR CELL STANDARDS FOR SPACE VEHICLE SERVICE:** The purpose of this standard is to classify the output of solar cells for space vehicle service in accordance with requirements of EIA Format JS4-RDF4.

November 1969; Reaffirmed February 1984 / Committee!33JC231 $47.00

EIA 371 **THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR SHORT-CIRCUIT FORWARD CURRENT TRANSFER RATIO:** This standard describes the method to be used for the measurement of small-signal VHF-UHF transistor short-circuit forward current transfer ratio, in preparing data sheets for JEDEC registration of low power transistors.

February 1970; Reaffirmed April 1981, April 1999 /JC-25 Committee $41.00

EIA 372 **THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR ADMITTANCE PARAMETERS:** This standard describes the method to be used for the measurement of small-signal VHF-UHF transistor admittance parameters, in preparing data sheets for JEDEC registration of low power transistors.

May 1970; Reaffirmed April 1981, April 1999 /JC-25 Committee $43.00

EIA 390-A **STANDARD TEST PROCEDURE FOR NOISE MARGIN MEASUREMENTS FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS:** The purpose of this standard is to define the dc (Steady-State) noise margin and the ac (Transient) Noise Margin in Semiconductor Logic Gating Microcircuits, and to describe the procedures used to measure these parameters. The standardization of the definitions and test procedures is intended to improve the ability to ensure interchangeability of elements by test specification, and to eliminate misunderstandings between manufacturers and users.

February 1981 /JC-13 Committee $43.00

EIA 397 **RECOMMENDED STANDARD FOR THYRISTORS:** One section of this standard presents a thorough explanation of thyristor principals, defining thedifferent classes of these devices, their Physical structure and detailing the numerous test methods and ratings required in their application to electronic and power circuitry. Another section presents a universally accepted listing of letter symbols. Considerable effort is devoted to the use of JEDEC Type Registration System as related to thyristors. This will permit the device manufacturer to employ a uniform procedure in the development of maximum rating and presentation of performance data.

June 1972 /JC-22.1 Subcommittee $177.00

EIA 397-1 **ADDENDUM No. 1 TO EIA-397:** A compilation of 12 new or revised thyristor test methods which have been adopted since the original standard was issued in 1972.

July 1980 /JC-22.1 Subcommittee $83.00

EIA 398 **MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE:** This standard contains a three-terminal procedure for capacitance measurement with due precautions for shielding of extraneous effects due to terminal leads and metal enclosures.

July 1972; Reaffirmed April 1981, April 1999 /JC-25 Committee $43.00

EIA 428-A **TYPE DESIGNATION SYSTEM FOR MICROELECTRONIC DEVICES**

October 1988; Rescinded September 1993 September 1993 /JC-10 Committee

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EIA 435 **STANDARD FOR THE MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS:** This standard specifies the standard for the measurement of small-signal transistor scattering parameters.

June 1976; Reaffirmed April 1999 /JC-25 Committee $49.00

EIA 471 **SYMBOL AND LABEL FOR ELECTROSTATIC SENSITIVE DEVICES:** This standard will be useful to anyone engaged in handling semiconductor devices and integrated circuits that are subject to permanent damage due to electrostatic potentials. The standard establishes a symbol and label that will gain the attention of those persons who might inflict electrostatic damage to the device. The label which is placed on the lowest practical level of packaging contains the words 'ATTENTION - OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES'. The symbol contained in this label, which may be used on the device itself, shows a hand in a triangle with a bar through it.

February 1980; Reaffirmed October 1988, September 1996, November 1996 /JC-10 Committee $38.00

EIA 557-A **STATISTICAL PROCESS CONTROL SYSTEMS:** SPC embraces a management philosophy of continuous process improvement that has a primary focus on prevention of defects. After a process has been characterized using statistical techniques (i.e., design experiments (DOE), capability studies, etc.), SPC is a tool that can be applied to control and optimize the process and reduce variability. An acceptable approach toward an SPC system involves the use of 'end-of-process' data to control the process through the application of SPC techniques. However, the intent of this standard is to emphasize the use of in-process data in order to better control and forecast system quality. This proactive use of SPC in conjunction with other techniques and the appropriate responsiveness to out-of-control situations serves to make SPC techniques critical in continuous process improvement and achieving excellence.

July 1995 /JC-13.5 Subcommittee $61.00

EIA 599-A **NATIONAL ELECTRONIC PROCESS CERTIFICATION STANDARD; GOVERNMENT CONTRACTORS:** Due to notification from the JC-14.4 subcommittee that the material contained in EIA599 has been replaced by the ISO 9000 series, the JEDEC Board of Directors, at its August 2003 meeting, approved to remove this standard from the JEDEC Free Download Area.

June 1998 August 2003 /JC-14.4 Subcommittee

EIA 623 **PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS:** This standard defines the practices to be used by government contractors related to the procurement of solid state components. These practices include parts selection, supplier management, and receiving inspection and test.

July 1994 /JC-13 Committee $40.00

EIA 625 **REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES (SUPERSEDES JEP108-B): SEE JESD625-A.**

November 1994 Became JESD625A after Revision December 1999 /JC-13 Committee

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EIA 659 **FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING (SUPERSEDES JESD29-A): SEE JESD659-A.**

July 1996 Became JESD659A after Revision September 1999 /JC-14.3 Subcommittee

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EIA 670 **QUALITY SYSTEM ASSESSMENT (SUPERSEDES JESD39-A):** This standard is used by the electronic industry for preparation of audit checklists for assessing compliance of quality systems to the requirements of ANSI/ASQC Q9001 (ISO9001), ANSI/ASQC Q9002 (ISO9002), ANSI/ASQC Q9003 (ISO9003), and ANSI/EIA599, National Electronic Process Certification Standard. It also provides a tool for quality system evaluation in accordance with the guidelines of ANSI/ASQC Q9004 (ISO9004) and the Malcolm Baldrige National Quality Award Criteria.

June 1997 /JC-14.4 Subcommittee $63.00

EIA 671 **COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS: SEE JESD671-A.**

November 1996 Became JESD671A after revision December 1999 /JC-14.4 Subcommittee

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JESD 370B **DESIGNATION SYSTEM FOR SEMICONDUCTOR DEVICES:** This standard includes several new

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items and has been completely rewritten from the original EIA-370. The first is a new letter symbol C so that a JEDEC type designation may now be 2C1234, to indicate that a chip is being designated that if it were properly mounted on the package registered for the 2N1234, it would display characteristics similar to those of the 2N1234. The second major addition is the method for assigning the first numeric symbol for type designations of optoelectronic devices. ANSI/EIA-370-B-1992.

February 1982; Reaffirmed November 1995, November 1999, May 2003 /JC-10 Committee $43.00

Displayed by Committee

JC-10 Terms/Defin/Symbols

EIA 236-C	COLOR CODING OF DISCRETE SEMICONDUCTOR DEVICES:
EIA 321-C	NUMBERING OF LIKE-NAMED TERMINAL FUNCTIONS IN SEMICONDUCTOR DEVICES AND DESIGNATION OF UNITS IN MULTIPLE-UNIT SEMICONDUCTOR DEVICES:
JESD 370B	DESIGNATION SYSTEM FOR SEMICONDUCTOR DEVICES:
EIA 428-A	TYPE DESIGNATION SYSTEM FOR MICROELECTRONIC DEVICES
EIA 471	SYMBOL AND LABEL FOR ELECTROSTATIC SENSITIVE DEVICES:
JEP 100	TERMS, DEFINTIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS AND MEMORY INTEGRATED CIRCUITS: ELEVATED TO JESD100, August 1993.
JEP 103A	SUGGESTED PRODUCT-DOCUMENTATION, CLASSIFICATIONS, AND DISCLAIMERS
JEP 120-A	INDEX OF TERMS DEFINED IN JEDEC PUBLICATIONS:
JEP 75	LETTER SYMBOLS USED WITH INFRARED DEVICES - INCORPORATED INTO JESD77-A.
JEP 99	GLOSSARY OF MICROELECTRONIC TERMS, DEFINITIONS, AND SYMBOLS: ELEVATED TO JESD99, June 1985.
JESD 100B.01	TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS, MICROPROCESSORS, AND MEMORY INTEGRATED CIRCUITS:
JESD 99A.01	TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROELECTRONIC DEVICES:
JESD 99-1	ADDENDUM No. 1 to JESD99 - TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS:
JEP 104C.01	REFERENCE GUIDE TO LETTER SYMBOLS FOR SEMICONDUCTOR DEVICES:
JESD 77B	TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR DISCRETE SEMICONDUCTOR AND OPTOELECTRONIC DEVICES:
JESD 88	DICTIONARY OF TERMS FOR SOLID STATE TECHNOLOGY, First Edition:

JC-11 Mechanical Pkg Outlines

EIA 308-A	PREPARATION OF OUTLINE DRAWINGS OF SOLID-STATE PRODUCTS FOR JEDEC TYPE REGISTRATION:
JEB 20	ACCEPTED PRACTICES FOR MAKING MICROELECTRONIC DEVICE THERMAL CHARACTERISTICS TESTS
JEP 86-A	RECOMMENDED PRACTICE FOR DUAL DIMENSIONING
JEP 95 AUS	ANNUAL UPDATING SERVICE:
JEP 95	JEDEC REGISTERED AND STANDARD OUTLINES FOR SOLID STATE AND RELATED PRODUCTS:
JEP 95-1	DESIGN REQUIREMENTS (Book 1, Section 4)
JESD 30C	DESCRIPTIVE DESIGNATION SYSTEM FOR SEMICONDUCTOR-DEVICE PACKAGES:

JC-13 Government Liaison

EIA 390-A	STANDARD TEST PROCEDURE FOR NOISE MARGIN MEASUREMENTS FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS:
EIA 623	PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS:
EIA 625	REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES

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(SUPERSEDES JEP108-B): SEE JESD625-A.

JEP 109-C GENERAL REQUIREMENTS FOR DISTRIBUTORS OF MILITARY SEMICONDUCTOR DEVICES:

JEP 112 TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF CIRCUIT SUPPORT FILMS FOR USE IN MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001

JEP 114 GUIDELINES FOR PARTICLE IMPACT NOISE DETECTION (PIND) TESTING, OPERATOR TRAINING, AND CERTIFICATION:

JEP 121 GUIDELINES FOR MIL-STD-883 SCREENING AND QCI OPTIMIZATION:

JEP 132 PROCESS CHARACTERIZATION GUIDELINE:

JESD 16-A ASSESSMENT OF AVERAGE OUTGOING QUALITY LEVELS IN PARTS PER MILLION (PPM):

JESD 19 GENERAL STANDARD FOR STATISTICAL PROCESS CONTROL (SPC) - SUPERSEDED by EIA-557-A

JESD 40 PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS - SUPERSEDED BY EIA-623, July 1994

JESD 42 REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES - SUPERSEDED BY EIA-625, November 1994.

JESD 49 PROCUREMENT STANDARD FOR KNOWN GOOD DIE (KGD):

JEP 144 GUIDELINE FOR RESIDUAL GAS ANALYSIS (RGA) FOR MICROELECTRONIC PACKAGES

J-STD- 002B SOLDERABILITY TESTS FOR COMPONENT LEADS, TERMINATIONS, LUGS, TERMINALS AND WIRES:

JC-13.2 Microelec. Devices

JEP 101-C JEDEC REQUIREMENTS FOR CLASS B MICROCIRCUITS:

JEP 111 TEST PROCEDURES FOR CUSTOM MONOLITHIC MICROCIRCUITS - SUPERSEDED BY MIL-PRF-38535C.

JESD 26-A GENERAL SPECIFICATION FOR PLASTIC ENCAPSULATED MICROCIRCUITS FOR USE IN RUGGED APPLICATIONS - RESCINDED, July 2001

JESD 53 MANAGEMENT OF COMPONENT OBSOLESCENCE BY GOVERNMENT CONTRACTORS: Rescinded, October 2002

JC-13.4 Radiation Hardness

JESD 57 TEST PROCEDURE FOR THE MANAGEMENT OF SINGLE-EVENT EFFECTS IN SEMICONDUCTOR DEVICES FROM HEAVY ION IRRADIATION:

JESD 89 MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES:

JC-13.5 Committee on Hybrid

EIA 557-A STATISTICAL PROCESS CONTROL SYSTEMS:

JEP 105 JEDEC GUIDELINE FOR THE CHARACTERIZATION OF HYBRID POLYMERIC MATERIALS - SUPERSEDED BY JESD72, June 2001

JEP 107 TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF PARTICLE GETTERS FOR USE IN HYBRID MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001

JEP 133-A GUIDE FOR THE PRODUCTION AND ACQUISITION OF RADIATION-HARDNESS ASSURED MULTICHIP MODULES AND HYBRID MICROCIRCUITS:

JEP 96 GUIDELINES FOR NONDESTRUCTIVE PULL TESTING OF WIRE BONDS ON HYBRID DEVICES

JESD 27 CERAMIC PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES:

JESD 9-A METAL PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES AND COVERS:

JESD 72 TEST METHODS AND ACCEPTANCE PROCEDURES FOR THE EVALUATION OF POLYMERIC MATERIALS:

JEP 142 GUIDELINE FOR OBTAINING AND ACCEPTING MATERIAL FOR USE IN HYBRID / MCM PRODUCTS:

JC-14 Quality/Reliability

JEB 16 USER GUIDE FOR MICROCIRCUIT FAILURE ANALYSIS:

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JC-14.1 Rel.Test Meth.Pkg.Dev.

J-STD- 020B	JOINT IPC/JEDEC STANDARD FOR MOISTURE/REFLOW SENSITIVITY CLASSIFICATION FOR NONHERMETIC SOLID STATE SURFACE-MOUNT DEVICES:
J-STD- 033A	JOINT IPC/JEDEC STANDARD FOR HANDLING, PACKING, SHIPPING AND USE OF MOISTURE/REFLOW SENSITIVE SURFACE-MOUNT DEVICES:
JEP 108-B	DISTRIBUTOR REQUIREMENTS FOR HANDLING ELECTROSTATIC -DISCHARGE SENSITIVE (ESDS) DEVICES: SUPERSEDED BY JESD42, March 1994.
JEP 113-B	SYMBOL AND LABELS FOR MOISTURE-SENSITIVE DEVICES:
JEP 122-B	FAILURE MECHANISMS AND MODELS FOR SILICON SEMICONDUCTOR DEVICES:
JESD 22-A100-B	CYCLED TEMPERATURE HUMIDITY BIAS LIFE TEST:
JESD 22-A101-B	STEADY-STATE TEMPERATURE HUMIDITY BIAS LIFE TEST:
JESD 22-A102-C	ACCELERATED MOISTURE RESISTANCE - UNBIASED AUTOCLAVE:
JESD 22-A103-B	HIGH TEMPERATURE STORAGE LIFE:
JESD 22-A104-B	TEMPERATURE CYCLING:
JESD 22-A105-B	POWER AND TEMPERATURE CYCLING:
JESD 22-A106-A	THERMAL SHOCK:
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JESD 22-A109-A	HERMETICITY:
JESD 22-A110-B	HIGHLY ACCELERATED TEMPERATURE AND HUMIDITY STRESS TEST (HAST)
JESD 22-A112-A	MOISTURE-INDUCED STRESS SENSITIVITY FOR PLASTIC SURFACE MOUNT DEVICES - SUPERSEDED BY J-STD-020A, April 1999.
JESD 22-A113D	PRECONDITIONING OF PLASTIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING:
JESD 22-A114-B	ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING HUMAN BODY MODEL (HBM):
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JESD 22-B101	EXTERNAL VISUAL:
JESD 22-B102-C	SOLDERABILITY:
JESD 22-B103-B	VIBRATION, VARIABLE FREQUENCY:
JESD 22-B104-B	MECHANICAL SHOCK:
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JEP 131	PROCESS FAILURE MODE AND EFFECTS ANALYSIS (FMEA):
JESD 29-A	FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING - SUPERSEDED BY EIA/ANSI-659, July 1996.
JESD 47B	STRESS-TEST-DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS:
JESD 50	SPECIAL REQUIREMENTS FOR MAVERICK PRODUCT ELIMINATION:
JESD 62-A	OUTLIER IDENTIFICATION AND MANAGEMENT SYSTEM FOR ELECTRONIC COMPONENTS:
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EIA 671	COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS: SEE JESD671-A.
JEP 117	GUIDELINES FOR USER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS - SUPERSEDED BY JESD46, August 1997.
JEP 124	GUIDELINES FOR THE PACKING, HANDLING, AND REPACKING OF MOISTURE-SENSITIVE COMPONENTS - SUPERSEDED BY J-STD-033, May 1999.
JEP 130	GUIDELINES FOR PACKING AND LABELING OF INTEGRATED CIRCUITS IN UNIT CONTAINER PACKING:
JEP 70-B	QUALITY AND RELIABILITY STANDARDS AND PUBLICATIONS:
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JESD 39-A	QUALITY SYSTEM ASSESSMENT - SUPERSEDED BY ANSI/EIA-670, June 1997.
JESD 43	COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS - SUPERSEDED BY EIA-671, November 1996.
JESD 46-B	CUSTOMER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS:
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JEP 134	GUIDELINES FOR PREPARING CUSTOMER-SUPPLIED BACKGROUND INFORMATION RELATING TO A SEMICONDUCTOR-DEVICE FAILURE ANALYSIS:
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JC-14.7 GaAs Rel. & Quality

JEP 110	GUIDELINES FOR THE MEASUREMENT OF THERMAL RESISTANCE OF GaAs FETS:
JEP 118	GUIDELINES FOR GaAs MMIC AND FET LIFE TESTING:
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JC-15.1 Thermal Character.

JEP 129	THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP)- SUPERSEDED BY JESD51-4, September 1997.
JESD 51	METHODOLOGY FOR THE THERMAL MEASUREMENT OF COMPONENT PACKAGES (SINGLE SEMICONDUCTOR DEVICE)
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JC-15.2 Elec. Char. Tech.

JEP 123	GUIDELINE FOR MEASUREMENT OF ELECTRONIC PACKAGE INDUCTANCE AND CAPACITANCE MODEL PARAMETERS:
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JC-16 Elec. Intrfcs/Pwr Supply

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JESD 8- 2	ADDENDUM No. 2 to JESD8 - STANDARD FOR OPERATING VOLTAGES AND INTERFACE LEVELS FOR LOW VOLTAGE EMITTER-COUPLED LOGIC (ECL) INTEGRATED CIRCUITS:
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JESD 8- 4	ADDENDUM No. 4 to JESD8 - CENTER-TAP-TERMINATED (CTT) INTERFACE LOW-LEVEL, HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:
JESD 8- 5	ADDENDUM No. 5 to JESD8 - 2.5 V 0.2 V (NORMAL RANGE), AND 1.8 V TO 2.7 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT:
JESD 8- 6	ADDENDUM No. 6 to JESD8 - HIGH SPEED TRANSCEIVER LOGIC (HSTL)- A 1.5 V OUTPUT BUFFER SUPPLY VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:
JESD 8- 7	ADDENDUM No. 7 to JESD8 - 1.8 V + -0.15 V (NORMAL RANGE), AND 1.2 V - 1.95 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT:
JESD 8- 8	ADDENDUM No. 8 to JESD8 - STUB SERIES TERMINATED LOGIC FOR 3.3 VOLTS (SSTL_3) A 3.3 V VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:
JESD 8- 9B	ADDENDUM No. 9B to JESD8 - STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2): Includes Errata and Corrected Page 7 as of October 18, 2002.
JESD 67	I/O DRIVERS AND RECEIVERS WITH CONFIGURABLE COMMUNICATION VOLTAGE, IMPEDANCE, AND

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JESD 8- 1-A INTERFACE STANDARD FOR NOMINAL 0.3 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS

JESD 8-B INTERFACE STANDARD FOR NOMINAL 0.3 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS:

JESD 8-11 ADDENDUM No. 11 to JESD8 - 1.5 V +/- 0.1 V (NORMAL RANGE) AND 0.9 - 1.6 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS:

JESD 8-12 1.2 V +/- 0.1 V (NORMAL RANGE) AND 0.8 - 1.3 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS:

JESD 8-13 SCALABLE LOW-VOLTAGE SIGNALING FOR 400 MV (SLVS-400):

JESD 8-14 1.0 V +/- 0.1 V (NORMAL RANGE) AND 0.7 V - 1.1 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS:

JESD 8-15A STUB SERIES TERMINATED LOGIC FOR 1.8 V (SSTL_18):

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EIA 323 AIR-CONVECTION-COOLED, LIFE TEST ENVIRONMENT FOR LEAD-MOUNTED SEMICONDUCTOR DEVICES:

EIA 397-1 ADDENDUM No. 1 TO EIA-397:

JEP 88 THERMAL RESISTANCE AND THERMAL IMPEDANCE TEST METHODS FOR STUD AND BASE-MOUNTED RECTIFIER DIODES AND THYRISTORS

JESD 41 REVERSE RECOVERY CHARACTERISTICS OF SILICON DIODES: Rescinded June 2002.

EIA 397 RECOMMENDED STANDARD FOR THYRISTORS:

JC-22.2 Rectifier Diodes

EIA 282-A STANDARD FOR SILICON RECTIFIER DIODES: SEE JESD282-B

JEP 87 FORWARD TURN-ON TIME MEASUREMENT ON SEMI-DIODES - INCORPORATED INTO EIA-282-A.

JESD 14 SEMICONDUCTOR POWER CONTROL MODULES:

JESD 4 DEFINITION OF EXTERNAL CLEARANCE AND CREEPAGE DISTANCES OF DISCRETE SEMICONDUCTOR PACKAGES FOR THYRISTORS AND RECTIFIER DIODES:

JESD 45 MEASUREMENT METHOD FOR THERMAL RESISTANCE OF BRIDGE RECTIFIER ASSEMBLIES: Rescinded June 2002. Replaced by JESD282-B.

TENTSTD 11 HANDLING AND INSTALLATION OF POWER SEMICONDUCTORS IN DISC TYPE PACKAGES: Included in JESD282 and EIA397.

JESD 282B.01 SILICON RECTIFIER DIODES:

JC-22.4 Signal Regltr Diodes

EIA 286-A STANDARD FOR MEASURING FORWARD SWITCHING CHARACTERISTICS OF SEMICONDUCTOR DIODES: SEE JESD286-B.

JESD 307 VOLTAGE REGULATOR DIODE NOISE VOLTAGE MEASUREMENT:

EIA 318-B MEASUREMENT OF REVERSE RECOVERY TIME FOR SEMICONDUCTOR SIGNAL DIODES:

JESD 320-A CONDITIONS FOR MEASUREMENT OF DIODE STATIC PARAMETERS:

JESD 381-A METHOD OF DIODE Q MEASUREMENT:

JESD 482-A LIST OF PREFERRED VALUES FOR USE ON VARIOUS TYPES OF SMALL SIGNAL AND REGULATOR DIODES:

JESD 531 THERMAL RESISTANCE TEST METHOD FOR SIGNAL AND REGULATOR DIODES (FORWARD VOLTAGE, SWITCHING METHOD):

JEP 90 THERMAL RESISTANCE FOR TEST METHODS FOR SIGNAL DIODES - SUPERSEDED BY EIA-531, July 1986. See JESD531, April 2002.

JESD 5 MEASUREMENT OF TEMPERATURE COEFFICIENT OF VOLTAGE REGULATOR DIODES:

JESD 286-B STANDARD FOR MEASURING FORWARD SWITCHING CHARACTERISTICS OF SEMICONDUCTOR DIODES:

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JC-22.5 Transient Voltage Supp

JESD 66	TRANSIENT VOLTAGE SUPPRESSOR STANDARD FOR THYRISTOR SURGE PROTECTIVE DEVICE:
TENTSTD 12	STANDARD FOR SELENIUM SURGE SUPPRESSORS:

JC-25 Transistors

EIA 283	TEST METHOD FOR TRANSISTOR NOISE FIGURE MEASUREMENTS AT MEDIUM FREQUENCIES - SUPERSEDED BY EIA-311-A.
JESD 284-A	TEST METHODS FOR THE COLLECTOR-BASE TIME CONSTANT AND FOR THE RESISTIVE PART OF THE COMMON-EMITTER INPUT IMPEDANCE:
EIA 302	RANGES AND CONDITIONS FOR SPECIFYING BETA FOR LOW POWER, AUDIO FREQUENCY TRANSISTORS FOR ENTERTAINMENT SERVICE:
EIA 306	MEASUREMENT OF SMALL SIGNAL HF, VHF, AND UHF POWER GAIN OF TRANSISTORS:
EIA 311-A	MEASUREMENT OF TRANSISTOR NOISE FIGURE AT MF, HF, AND VHF:
JESD 313-B	THERMAL RESISTANCE MEASUREMENTS OF CONDUCTION COOLED POWER TRANSISTORS:
EIA 340	STANDARD FOR THE MEASUREMENT OF CRE:
EIA 353	THE MEASUREMENT OF TRANSISTOR NOISE FIGURE AT FREQUENCIES UP TO 20 kHz BY SINUSOIDAL SIGNAL-GENERATOR METHOD:
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EIA 371	THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR SHORT-CIRCUIT FORWARD CURRENT TRANSFER RATIO:
EIA 372	THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR ADMITTANCE PARAMETERS:
EIA 398	MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE:
JESD 419-A	STANDARD LIST OF VALUES TO BE USED IN SEMICONDUCTOR DEVICE SPECIFICATIONS AND REGISTRATION FORMAT:
EIA 435	STANDARD FOR THE MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS:
JEP 115	POWER MOSFET ELECTRICAL DOSE RATE TEST METHOD:
JEP 138	USER GUIDELINES FOR IR THERMAL IMAGING DETERMINATION OF DIE TEMPERATURE:
JEP 65	TEST PROCEDURES FOR VERIFICATION OF MAXIMUM RATINGS OF POWER TRANSISTORS:
JEP 69-B	PREFERRED LEAD CONFIGURATION FOR FIELD-EFFECT TRANSISTORS:
JEP 74	STANDARD LIST OF VALUES TO BE USED IN POWER TRANSISTOR DEVICE REGISTRATION AND MINIMUM DIFFERENCES FOR DISCRETENESS OF REGISTRATIONS - SUPERSEDED BY EIA-419-A, February 1996.
JEP 84	RECOMMENDED PRACTICE FOR MEASUREMENT OF TRANSISTOR LEAD TEMPERATURE:
JESD 24	POWER MOSFETS:
JESD 24- 1	ADDENDUM No. 1 to JESD24 - METHOD FOR MEASUREMENT OF POWER DEVICE TURN-OFF SWITCHING LOSS:
JESD 24-10	ADDENDUM No. 10 to JESD24 - TEST METHOD FOR MEASUREMENT OF REVERSE RECOVERY TIME trr FOR POWER MOSFET DRAIN-SOURCE DIODES:
JESD 24-11	ADDENDUM No. 11 to JESD24 - POWER MOSFET EQUIVALENT SERIES GATE RESISTANCE TEST METHOD:
JESD 24- 2	ADDENDUM No. 2 to JESD24 - GATE CHARGE TEST METHOD:
JESD 24- 3	ADDENDUM No. 3 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR VERTICAL POWER MOSFETS (DELTA SOURCE-DRAIN VOLTAGE METHOD):
JESD 24- 4	ADDENDUM No. 4 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR BIPOLAR TRANSISTORS (DELTA BASE-EMITTER VOLTAGE METHOD):
JESD 24- 5	ADDENDUM No. 5 to JESD24 - SINGLE PULSE UNCLAMPED INDUCTIVE SWITCHING (UIS) AVALANCHE TEST METHOD:
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JESD 24- 7	ADDENDUM No. 7 to JESD24 - COMMUTATING DIODE SAFE OPERATING AREA TEST PROCEDURE

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JESD 24- 9	ADDENDUM No. 9 to JESD24 - SHORT CIRCUIT WITHSTAND TIME TEST METHOD:
JESD 25	MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS:
JESD 6	MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE:
JESD 10	LOW FREQUENCY POWER TRANSISTORS:
EIA 284-A	TEST METHODS FOR THE COLLECTOR-BASE TIME CONSTANT AND FOR THE RESISTIVE PART OF THE COMMON-EMITTER INPUT IMPEDANCE: SEE JESD284A.
JEP 145	GUIDELINE FOR ASSESSING THE CURRENT-CARRYING CAPABILITY OF THE LEADS IN A POWER PACKAGE SYSTEM:

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JEB 15	TERMINOLOGY AND METHODS OF MEASUREMENT FOR BISTABLE SEMICONDUCTOR MICROCIRCUITS:
JEB 19	RECOMMENDED CHARACTERIZATION OF MOS SHIFT REGISTERS:
JESD 36	STANDARD DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE, 5 V TOLERANT CMOS LOGIC DEVICES:
JESD 52	STANDARD FOR DESCRIPTION OF LOW VOLTAGE TTL-COMPATIBLE CMOS LOGIC DEVICES:
JESD 54	STANDARD FOR DESCRIPTION OF 54/74ABTXXX AND 74BCXXX TTL-COMPATIBLE BiCMOS LOGIC DEVICES:
JESD 55	STANDARD FOR DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE BiCMOS LOGIC DEVICES:
JESD 65B	DEFINITION OF SKEW SPECIFICATIONS FOR STANDARD LOGIC DEVICES:
JESD 70	2.5 V BiCMOS LOGIC DEVICE FAMILY SPECIFICATION WITH 5 V TOLERANT INPUTS AND OUTPUTS:
JESD 73	DESCRIPTION OF 5 V BUS SWITCH WITH TTL-COMPATIBLE CONTROL INPUTS:
JESD 80	STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES:
JESD 64-A	STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES WITH 3.6 V CMOS TOLERANT INPUTS AND OUTPUTS:
JESD 75	BALL GRID ARRAY PINOUTS STANDARDIZED FOR 32-BIT LOGIC FUNCTIONS:
JESD 82	DEFINITION OF CDCV857 PLL CLOCK DRIVER FOR REGISTERED DDR DIMM APPLICATIONS:
JESD 76-1	STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (WIDE RANGE OPERATION):
JESD 76-2	STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (NORMAL RANGE OPERATION):
JESD 82-2	STANDARD FOR DESCRIPTION OF A 3.3 V, 18-BIT, LVTTL I/O REGISTER FOR PC133 REGISTERED DIMM APPLICATIONS:
JESD 75-2	BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16-BIT LOGIC FUNCTIONS:
JESD 75-3	BALL GRID ARRAY PINOUTS STANDARDIZED FOR 8-BIT LOGIC FUNCTIONS:
JESD 82-3A	DEFINITION OF THE SSTV16857 2.5 V, 14-BIT SSTL_2 REGISTERED BUFFER FOR DDR DIMM APPLICATIONS:
JESD 73-1	STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES:
JESD 73-2	STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES WITH INTEGRATED CHARGE PUMPS:
JESD 82-4B	STANDARD FOR DEFINITION OF THE SSTV16859 2.5 V, 13-BIT TO 26-BIT SSTL_2 REGISTERED BUFFER FOR STACKED DDR DIMM APPLICATIONS:
JESD 75-1	BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16, 18, AND 20-BIT LOGIC FUNCTIONS USING A 54 BALL PACKAGE:
JESD 82-5	STANDARD FOR DESCRIPTION OF A 3.3 V, ZERO DELAY CLOCK DISTRIBUTION DEVICE COMPLIANT WITH THE JESD21-C PC133 REGISTERED DIMM SPECIFICATION
JESD 82-1	DEFINITION OF CV857 PLL CLOCK DRIVER FOR REGISTERED PC1600, PC2100, AND PC2700 DIMM APPLICATIONS:
JESD 82-8	STANDARD FOR DEFINITION OF ◆CU877 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS

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JEP 102	STANDARD FOR 64K x 1 DYNAMIC RAM - SUPERSEDED BY JESD21-C.
JESD 21-C	CONFIGURATIONS FOR SOLID STATE MEMORIES:

JC-42.3 RAM Memories

JEP 106M	STANDARD MANUFACTURERS IDENTIFICATION CODE:
JESD 79-2	DDR2 SDRAM SPECIFICATION

JC-42.4 Non-Volatile Memories

JEP 137-A	COMMON FLASH INTERFACE (CFI) IDENTIFICATION CODES:
JESD 68.01	COMMON FLASH INTERFACE (CFI):

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JEB 5-A	METHODS OF MEASUREMENT FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS:

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JEP 78	RELATIVE SPECTRAL RESPONSE CURVES FOR SEMICONDUCTOR INFRARED DETECTORS:

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Acceleration Factor	JEP 122-B JESD 85
Acceleration Models	JESD 91-A
Acoustic Microscopy	J-STD- 035
Acronyms - packages	JESD 30C
Activation Energy	JEP 122-B JESD 85
Administrative Quality Problems	JESD 671-A
Air Convection Cooled Life Test	EIA 323
AlCu	JESD 87
Alpha Particles	JESD 89
Analysis - Heat Flow	JESD 51- 7
Analyzer	JEP 147
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144 Pin	MODULE 4_5_5 MODULE 4_5_6 MODULE 4_5_09 MODULE 4_20_03 MODULE 4_5_13 MODULE 4_5_8 MO 214-B
16-Bit Logic	JESD 75-2
168 Pin	MODULE 4_5_1 MODULE 4_5_3 MODULE 4_5_13 MODULE 4_5_07 MODULE 4_20_02
172 pin	MO 214-B
184 Pin	MODULE 4_05_10 MODULE 4_20_05 MODULE 4_20_04 MODULE 4_5_11 MODULE 4_5_12 MO 206-C
184-Pin	MODULE 4_20_07 MODULE 4_20_08
2.5 V	JESD 8- 9B
200 Pin	MODULE 4_5_2 MO 224-B
21C	TOC21C
240 pin	SO 001-B
240-Pin	MODULE 4_05_14
244 Pin	MO 244-A
278 Pin	MODULE 4_6_1
3 Leads	TO 273-B
3.3 V	JESD 8-B
32-Bit Logic Functions	JESD 75
5 V Tolerant - CMOS Devices	JESD 36
54 Ball Package	JESD 75-1
64 pin	MODULE 4_4_1
72 pin	MODULE 4_4_1 MODULE 4_4_2 MODULE 4_4_4
8 lead	MO 240-A
8-Bit	JESD 75-3
80 Pin	MODULE 4_4_7

Displayed by revision status

EIA 283 TEST METHOD FOR TRANSISTOR NOISE FIGURE MEASUREMENTS AT MEDIUM FREQUENCIES - SUPERSEDED BY EIA-311-A.
November 1963; Rescinded November 1981

EIA 318-1 ADDENDUM No. 1 to EIA-318 - CHARACTERIZATION OF A REVERSE TEST FIXTURE: SUPERSEDED BY EIA-318-B, July 1996.
February 1981; Rescinded

EIA 428-A TYPE DESIGNATION SYSTEM FOR MICROELECTRONIC DEVICES
October 1988; Rescinded September 1993

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JEB 17 USER GUIDELINES FOR QUALITY AND RELIABILITY ASSURANCE OF LSI COMPONENTS
November 1970; Rescinded April 1987

JEB 20 ACCEPTED PRACTICES FOR MAKING MICROELECTRONIC DEVICE THERMAL CHARACTERISTICS TESTS
January 1975; Rescinded November 1988

JEB 6 STANDARD MEASURMENTS OF THE ELECTRICAL CHARACTERISTICS OF SEMICONDUCTOR INTEGRATED CIRCUITS
December 1966; Rescinded

JEP 100 TERMS, DEFINTIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS AND MEMORY INTEGRATED CIRCUITS: ELEVATED TO JESD100, August 1993.
September 1979; Rescinded October 1983

JEP 102 STANDARD FOR 64K x 1 DYNAMIC RAM - SUPERSEDED BY JESD21-C.
September 1978; Rescinded April 1985

JEP 105 JEDEC GUIDELINE FOR THE CHARACTERIZATION OF HYBRID POLYMERIC MATERIALS - SUPERSEDED BY JESD72, June 2001
April 1983; Rescinded June 2001

JEP 107 TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF PARTICLE GETTERS FOR USE IN HYBRID MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001
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JEP 108-B DISTRIBUTOR REQUIREMENTS FOR HANDLING ELECTROSTATIC -DISCHARGE SENSITIVE (ESDS) DEVICES: SUPERSEDED BY JESD42, March 1994.
April 1991; Superseded

JEP 109-C GENERAL REQUIREMENTS FOR DISTRIBUTORS OF MILITARY SEMICONDUCTOR DEVICES:
March 1995; Rescinded November 2001

JEP 111 TEST PROCEDURES FOR CUSTOM MONOLITHIC MICROCIRCUITS - SUPERSEDED BY MIL-PRF-38535C.
July 1986; Rescinded June 1996

JEP 112 TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF CIRCUIT SUPPORT FILMS FOR USE IN MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001
June 1987; Rescinded June 2001

JEP 117 GUIDELINES FOR USER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS - SUPERSEDED BY JESD46, August 1997.
April 1994; Rescinded July 1994

JEP 124 GUIDELINES FOR THE PACKING, HANDLING, AND REPACKING OF MOISTURE-SENSITIVE COMPONENTS - SUPERSEDED BY J-STD-033, May 1999.
December 1995; Rescinded November 1999

JEP 74 STANDARD LIST OF VALUES TO BE USED IN POWER TRANSISTOR DEVICE REGISTRATION AND MINIMUM DIFFERENCES FOR DISCRETENESS OF REGISTRATIONS - SUPERSEDED BY EIA-419-A, February 1996.
July 1969; Rescinded February 1996

JEP 75 LETTER SYMBOLS USED WITH INFRARED DEVICES - INCORPORATED INTO JESD77-A.
August 1984; Rescinded August 1984

JEP 86-A RECOMMENDED PRACTICE FOR DUAL DIMENSIONING
May 1976; Rescinded November 1999

JEP 87 FORWARD TURN-ON TIME MEASUREMENT ON SEMI-DIODES - INCORPORATED INTO EIA-282-A.
June 1992; Rescinded June 1985

JEP 88 THERMAL RESISTANCE AND THERMAL IMPEDANCE TEST METHODS FOR STUD AND BASE-MOUNTED RECTIFIER DIODES AND THYRISTORS

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January 1974; Rescinded June 1992

JEP 90 THERMAL RESISTANCE FOR TEST METHODS FOR SIGNAL DIODES - SUPERSEDED BY EIA-531, July 1986. See JESD531, April 2002.
September 1983; Rescinded September 1986

JEP 93 MICROELECTRONIC DEVICE TYPE ASSIGNMENTS
August 1975; Rescinded June 1992

JEP 96 GUIDELINES FOR NONDESTRUCTIVE PULL TESTING OF WIRE BONDS ON HYBRID DEVICES
March 1977; Rescinded April 2000

JEP 99 GLOSSARY OF MICROELECTRONIC TERMS, DEFINITIONS, AND SYMBOLS: ELEVATED TO JESD99, June 1985.
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JESD 17 LATCH-UP IN CMOS INTEGRATED CIRCUITS - SUPERSEDED BY JESD78, February 1999
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JESD 19 GENERAL STANDARD FOR STATISTICAL PROCESS CONTROL (SPC) - SUPERSEDED by EIA-557-A
July 1988; Rescinded July 1995

JESD 22-A112-A MOISTURE-INDUCED STRESS SENSITIVITY FOR PLASTIC SURFACE MOUNT DEVICES - SUPERSEDED BY J-STD-020A, April 1999.
November 1995; Rescinded May 2000

JESD 22-C100-A HIGH TEMPERATURE CONTINUITY - RESCINDED, November 1999
April 1990; Rescinded November 1999

JESD 26-A GENERAL SPECIFICATION FOR PLASTIC ENCAPSULATED MICROCIRCUITS FOR USE IN RUGGED APPLICATIONS - RESCINDED, July 2001
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July 1996; Superseded July 1996

JESD 39-A QUALITY SYSTEM ASSESSMENT - SUPERSEDED BY ANSI/EIA-670, June 1997.
June 1997; Superseded

JESD 41 REVERSE RECOVERY CHARACTERISTICS OF SILICON DIODES: Rescinded June 2002.
May 1995; Rescinded June 2002

JESD 42 REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES - SUPERSEDED BY EIA-625, November 1994.
March 1994; Superseded

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November 1996; Superseded

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January 1996; Rescinded October 2002

TENTSTD 11 HANDLING AND INSTALLATION OF POWER SEMICONDUCTORS IN DISC TYPE PACKAGES: Included in JESD282 and EIA397.
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mm Pitch. Item 11.14-044.
June 1999; Rescinded June 2001

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Exhibit C

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