4.20.10 - 240-Pin PC-3200/PC2-4200/PC2-5300/PC2-6400 DDR2 SDRAM Registered DIMM Design Specification

PC2-3200/PC2-4200/PC2-5300/PC2-6400 DDR2 SDRAM Registered DIMM Design Specification

Revision 3.2

Oct 04 2005

Petitioners
Ex. 1066, p. 1

Contents

1. Product Description 4
Product Family Attributes 4

2. Environmental Requirements 6

3. Architecture 6
Pin Description 6
Input/Output Functional Description 7
DDR2 240pin DIMM Pinout 8
Block Diagram: Raw Card Version A and F, x72 one physical rank of x8 9
Block Diagram: Raw Card Version B and G, x72 two physical ranks of x8 10
Block Diagram: Raw Card Version C and H, x72 one physical rank of x4 11
Block Diagram: Raw Card Version D, x72 two physical rank of x4 12
Block Diagram: Raw Card Version E, x72 two physical rank of x4 13
Block Diagram: Raw Card Version J, x72 two physical rank of x4 14
Block Diagram: Raw Card Version K, x72 two physical rank of x4 15
Block Diagram: Raw Card Version M, x72 four physical rank of x4 16
Block Diagram: Raw Card Version N, x72 four physical rank of x8 17
Block Diagram: Raw Card Version P, x72 two physical rank of x4 18
Differential Clock Net Wiring (CK0, $\overline{CK0}$) 19

4. Component Details 20
Pin Assignments for 256Mb to 4Gb; DDR2 SDRAM 21
Pin Assignments for 1:2, 1:1 Register 27
Pin Assignments for 10 differential pairs output PLL 34
Register Component Specification 35
PLL Component Specification 40

5. DDR2 Registered DIMM Details 42
DDR2 SDRAM Module Configuration 42
Input Loading Matrix 43
DDR2 Registered DIMM Design File Releases 43
Component Types and Placement 44
Example Component Placement 44

6. DDR2 Registered DIMM Wiring Details 49
Signal Groups 49
General Net Structure Routing Guidelines 49
Explanation of Net Structure Diagrams 53
Differential Clock Net Structures 54
Data Net Structures 62
Address/Command/Control Net Structures 65
Address and Command Parity Net Structures 84
Cross Section Recommendations 87

Petitioners
Ex. 1066, p. 2

PCB Electrical Specification 87
Example Six Layer Stackup 87
Example Eight Layer Stackup 88
Example Eight Layer Stackup 89

7. Timing Budget 90

8. Serial Presence Detect Definition 94

9. DDR2 DIMM Label Format 97

10. DIMM Mechanical Specifications 99

11. Application Note. 100

12. Revision Log. 107

Petitioners
Ex. 1066, p. 3

Product Description

This specification defines the electrical and mechanical requirements for 240-pin, 1.8Volt, PC2-3200/PC2-4200/PC2-5300/PC2-6400, 72 bit-wide, Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR2 SDRAM DIMMs).These SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations. PC2-3200/PC2-4200/PC2-5300/PC2-6400 refers to the JEDEC standard DIMM naming convention in which PC2-3200/PC2-4200/PC2-5300/PC2-6400 indicates a 240-pin DIMM running at 200/266/333/400 MHz clock speed and offering 3200/4200/5300/6400 MB/s bandwidth.

Reference design examples are included which provide an initial basis for Registered DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC2-3200/PC2-4200/PC2-5300/PC2-6400 support. All registered DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

Product Family Attributes

DIMM organization	x72 ECC
DIMM dimensions : height (nom.) x width(nom.) x thickness(max.) / MO-number, Variation	30.0 mm x 133.35 mm x 4.00 mm / MO-237, Variation AB 30.0 mm x 133.35 mm x 6.75 mm / MO-237, Variation BB 30.0 mm x 133.35 mm x 7.55 mm / MO-237, Variation CB
Pin count	240
SDRAMs supported	256 Mb, 512 Mb, 1 Gb, 2 Gb, 4 Gb
Capacity	256 MB, 512 MB, 1 GB, 2 GB, 4 GB, 8 GB, 16 GB, 32 GB
Serial PD	Consistent with DDR2 SPD, Rev. 1.2
Voltage options	1.8 volt (V_{DD}/V_{DDQ})
Interface	SSTL_18

Petitioners
Ex. 1066, p. 4

Module Configurations

Raw Card	Number of DDR2 SDRAMs	SDRAM Organization	Number of Ranks	PC2-4200 PC2-3200	PC2-5300	PC2-6400	DRAM Size	Parity Support	Notes
A	9	x8, planar, single row	1	x			Tall	No	
B	18	x8, planar, single row	2	x			Tall	No	
C	18	x4, planar, single row	1	x			Tall	No	
D	36	x4, stacked, single row	2	x	x	x	Tall	Yes	R/C D - 8 layer, Blind Via
E	36	x4, stacked, single row	2	x			Wide	Yes	
F	9	x8, planar, single row	1	x	x	x	Tall	Yes	
G	18	x8, planar, single row	2	x	x	x	Tall	Yes	
H	18	x4, planar, single row	1	x	x	x	Tall	Yes	
J	36	x4, planar, double row	2	x	x		Wide	Yes	
K	36	x4, stacked, single row	2	x	x	x	Tall	Yes	R/C K - 8 layer, Through Via
M	72	x4, stacked, double row	4	x			Wide	Yes	
N	36	x8, planar, double row	4	x			Wide	Yes	
P	36	x4, stacked, single row	2	x	x		Wide	Yes	

Note: X will reflect past committee ballot at the time when specification is issued at BOD ballot.

Petitioners
Ex. 1066, p. 5

Environmental Requirements

DDR2 SDRAM Registered DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating temperature	See Note		3
H_{OPR}	Operating humidity (relative)	10 to 90	%	1
T_{STG}	Storage temperature	-50 to +100	°C	1
H_{STG}	Storage humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric pressure (operating & storage)	105 to 69	K Pascal	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. The designer must meet the case temperature specifications for individual module components.

Architecture

Pin Description

Pin Name	Description	Number	Pin Name	Description	Number
CK0	Clock Input, positive line	1	ODT[1:0]	On Die Termination Inputs	2
$\overline{CK0}$	Clock input, negative line	1	DQ[63:0]	Data Input/Output	64
CKE[1:0]	Clock Enables	2	CB[7:0]	Data check bits Input/Output	8
$\overline{RAS}$	Row Address Strobe	1	DQS[8:0]	Data strobes	9
$\overline{CAS}$	Column Address Strobe	1	$\overline{DQS}$[8:0]	Data strobes, negative line	9
$\overline{WE}$	Write Enable	1	DM[8:0]/ DQS[17:9]	Data Masks / Data strobes	9
$\overline{S}$[3:0]	Chip Selects	4	$\overline{DQS}$[17:9]	Data strobes, negative line	9
A[9:0],A[15:11]	Address Inputs	15	RFU	Reserved for Future Use	2
A10/AP	Address Input/Autoprecharge	1	NC	No Connect	1
BA[2:0]	SDRAM Bank Addresses	3	TEST	Memory bus test tool (Not Connected and Not Useable on DIMMs)	1
SCL	Serial Presence Detect (SPD) Clock Input	1	V_{DD}	Core Power	11
SDA	SPD Data Input/Output	1	V_{DDQ}	I/O Power	11
SA[2:0]	SPD Address Inputs	3	V_{SS}	Ground	64
Par_In	Parity bit for the Address and Control bus	1	V_{REF}	Input/Output Reference	1
$\overline{Err_Out}$	Parity error found on the Address and Control bus	1	V_{DDSPD}	SPD Power	1
$\overline{RESET}$	Register and PLL control pin	1		total	240

Petitioners
Ex. 1066, p. 6

Registered DIMM Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0	IN	Positive Edge	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM PLL.
$\overline{CK0}$	IN	Negative Edge	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM PLL.
CKE[1:0]	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
$\overline{S}$[3:0]	IN	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. These input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When both $\overline{S}$[0:1] are high, all register outputs (except CKE, ODT and Chip select) remain in the previous state. For modules supporting 4 ranks, $\overline{S}$[2:3] operate similarly to $\overline{S}$[0:1] for a second set of register outputs.
ODT[1:0]	IN	Active High	On-Die Termination control signals
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	IN	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL18 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA[2:0]	IN	—	Selects which SDRAM bank of four or eight is activated.
A[15:11, 10/AP,9:0]	IN	—	During a Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1,BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1 or BA2. If AP is low, BA0 and BA1 and BA2 are used to define which bank to precharge.
DQ[63:0], CB[7:0]	I/O	—	Data and Check Bit Input/Output pins
DM[8:0]	IN	Active High	Masks write data when high, issued concurrently with input data.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic.
DQS[17:0]	I/O	Positive Edge	Positive line of the differential data strobe for input and output data.
$\overline{DQS}$[17:0]	I/O	Negative Edge	Negative line of the differential data strobe for input and output data.
SA[2:0]	IN	—	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA	I/O	—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pullup.
SCL	IN	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DDSPD} on the system planar to act as a pullup.
V_{DDSPD}	Supply		Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports from 1.7 Volt to 3.6 Volt (nominal 1.8 Volt, 2.5 Volt and 3.3 Volt) operation.
$\overline{RESET}$	IN		The $\overline{RESET}$ pin is connected to the $\overline{RST}$ pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and register(s) will be set to low level (the PLL will remain synchronized with the input clock)
Par_In	IN		Parity bit for the Address and Control bus. (“1 “: Odd, “0 “: Even)
$\overline{Err_Out}$	OUT		Parity error found in the Address and Control bus

Petitioners
Ex. 1066, p. 7

Registered DIMM Input/Output Functional Description

Symbol	Type	Polarity	Function
TEST			Used by memory bus analysis tools (unused on memory DIMMs)

DDR2 240-pin DIMM Pinout

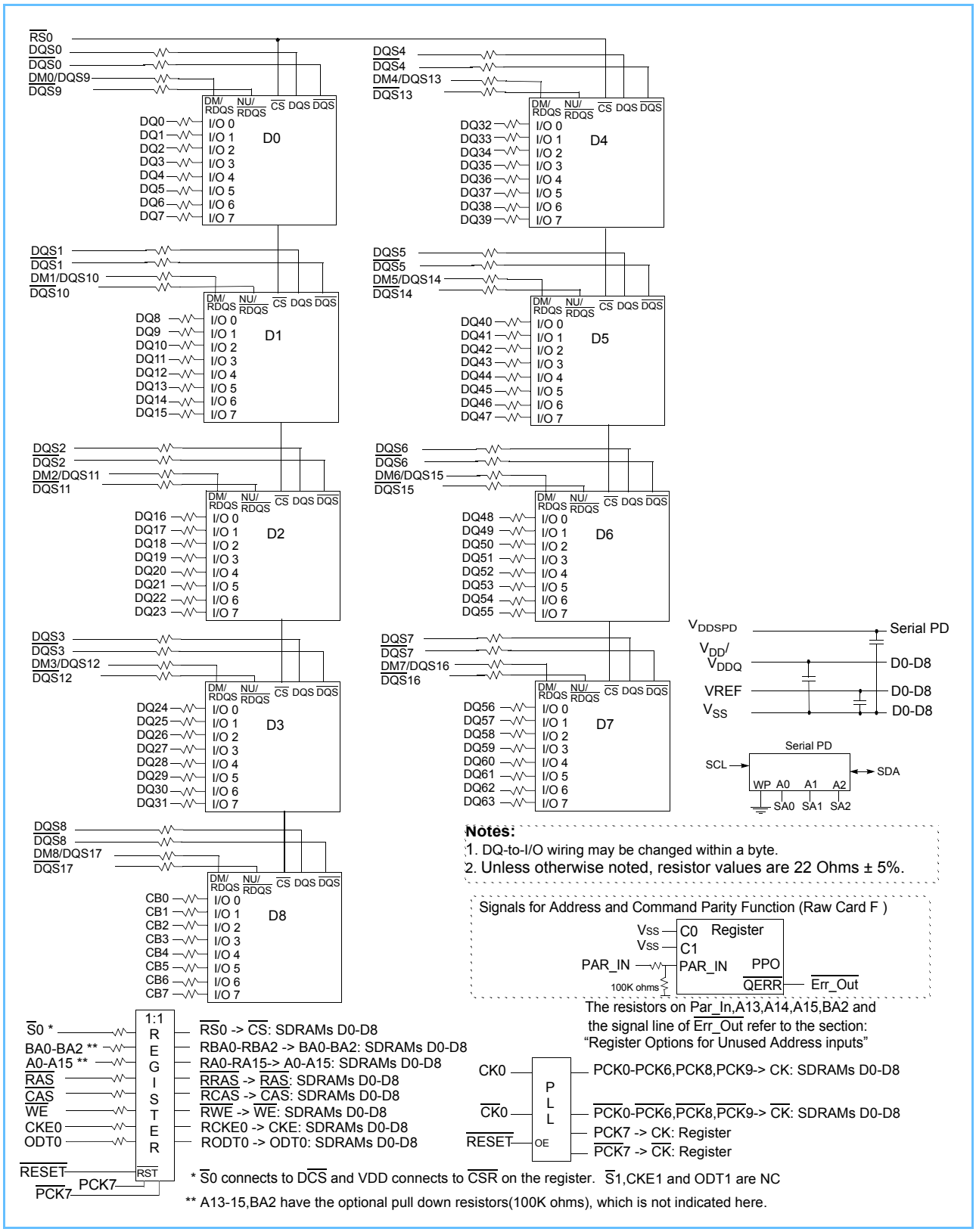
Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V_{REF}	121	V_{SS}	31	DQ19	151	V_{SS}	61	A4	181	V_{DDQ}	91	V_{SS}	211	DM5/DQS14
2	V_{SS}	122	DQ4	32	V_{SS}	152	DQ28	62	V_{DDQ}	182	A3	92	$\overline{DQS5}$	212	NC, $\overline{DQS14}$
3	DQ0	123	DQ5	33	DQ24	153	DQ29	63	A2	183	A1	93	DQS5	213	V_{SS}
4	DQ1	124	V_{SS}	34	DQ25	154	V_{SS}	64	V_{DD}	184	V_{DD}	94	V_{SS}	214	DQ46
5	V_{SS}	125	DM0/DQS9	35	V_{SS}	155	DM3/DQS12	KEY				95	DQ42	215	DQ47
6	$\overline{DQS0}$	126	NC, $\overline{DQS9}$	36	$\overline{DQS3}$	156	NC, $\overline{DQS12}$	65	V_{SS}	185	CK0	96	DQ43	216	V_{SS}
7	DQS0	127	V_{SS}	37	DQS3	157	V_{SS}	66	V_{SS}	186	$\overline{CK0}$	97	V_{SS}	217	DQ52
8	V_{SS}	128	DQ6	38	V_{SS}	158	DQ30	67	V_{DD}	187	V_{DD}	98	DQ48	218	DQ53
9	DQ2	129	DQ7	39	DQ26	159	DQ31	68	NC, Par_In	188	A0	99	DQ49	219	V_{SS}
10	DQ3	130	V_{SS}	40	DQ27	160	V_{SS}	69	V_{DD}	189	V_{DD}	100	V_{SS}	220	RFU, $\overline{S2}$
11	V_{SS}	131	DQ12	41	V_{SS}	161	CB4	70	A10/ AP	190	BA1	101	SA2	221	RFU, $\overline{S3}$
12	DQ8	132	DQ13	42	CB0	162	CB5	71	BA0	191	V_{DDQ}	102	NC(TEST)	222	V_{SS}
13	DQ9	133	V_{SS}	43	CB1	163	V_{SS}	72	V_{DDQ}	192	$\overline{RAS}$	103	V_{SS}	223	DM6/DQS15
14	V_{SS}	134	DM1/DQS10	44	V_{SS}	164	DM8/DQS17	73	$\overline{WE}$	193	$\overline{S0}$	104	$\overline{DQS6}$	224	NC, $\overline{DQS15}$
15	$\overline{DQS1}$	135	NC, $\overline{DQS10}$	45	$\overline{DQS8}$	165	NC, $\overline{DQS17}$	74	$\overline{CAS}$	194	V_{DDQ}	105	DQS6	225	V_{SS}
16	DQS1	136	VSS	46	DQS8	166	V_{SS}	75	V_{DDQ}	195	ODT0	106	V_{SS}	226	DQ54
17	V_{SS}	137	RFU	47	V_{SS}	167	CB6	76	NC, $\overline{S1}$	196	A13, NC	107	DQ50	227	DQ55
18	$\overline{RESET}$	138	RFU	48	CB2	168	CB7	77	NC, ODT1	197	V_{DD}	108	DQ51	228	V_{SS}
19	NC	139	V_{SS}	49	CB3	169	V_{SS}	78	V_{DDQ}	198	V_{SS}	109	V_{SS}	229	DQ60
20	V_{SS}	140	DQ14	50	V_{SS}	170	V_{DDQ}	79	V_{SS}	199	DQ36	110	DQ56	230	DQ61
21	DQ10	141	DQ15	51	V_{DDQ}	171	NC, CKE1	80	DQ32	200	DQ37	111	DQ57	231	V_{SS}
22	DQ11	142	V_{SS}	52	CKE0	172	V_{DD}	81	DQ33	201	V_{SS}	112	V_{SS}	232	DM7/DQS16
23	V_{SS}	143	DQ20	53	V_{DD}	173	A15, NC	82	V_{SS}	202	DM4/DQS13	113	$\overline{DQS7}$	233	NC, $\overline{DQS16}$
24	DQ16	144	DQ21	54	BA2, NC	174	A14, NC	83	$\overline{DQS4}$	203	NC, $\overline{DQS13}$	114	DQS7	234	V_{SS}
25	DQ17	145	V_{SS}	55	NC, Err_Out	175	V_{DDQ}	84	DQS4	204	V_{SS}	115	V_{SS}	235	DQ62
26	V_{SS}	146	DM2/DQS11	56	V_{DDQ}	176	A12	85	V_{SS}	205	DQ38	116	DQ58	236	DQ63
27	$\overline{DQS2}$	147	NC, $\overline{DQS11}$	57	A11	177	A9	86	DQ34	206	DQ39	117	DQ59	237	V_{SS}
28	DQS2	148	V_{SS}	58	A7	178	V_{DD}	87	DQ35	207	V_{SS}	118	V_{SS}	238	VDDSPD
29	V_{SS}	149	DQ22	59	V_{DD}	179	A8	88	V_{SS}	208	DQ44	119	SDA	239	SA0
30	DQ18	150	DQ23	60	A5	180	A6	89	DQ40	209	DQ45	120	SCL	240	SA1
								90	DQ41	210	V_{SS}				

NC = No Connect; NU = Not Useable, RFU = Reserved Future Use.
1. CK1,$\overline{CK1}$,CK2, $\overline{CK2}$ (pins 137,138,220,221) are for Unbuffered DIMM clock.
   Pins 137, 138 are RFU on registered DIMMs; pins 220, 221 are used for 4 rank RDIMMs.
2. $\overline{RESET}$ (pin 18) is connected to both OE of the PLL and Reset of the register.
3. The TEST pin (pin 102) is reserved for bus analysis probes and is not connected on normal modules (DIMMs).
4. NC/Err_Out (pin 55) and NC/Par_In (pin 68) are optional function to check address and command parity.

Petitioners
Ex. 1066, p. 8

Block Diagram: Raw Card Version A and F

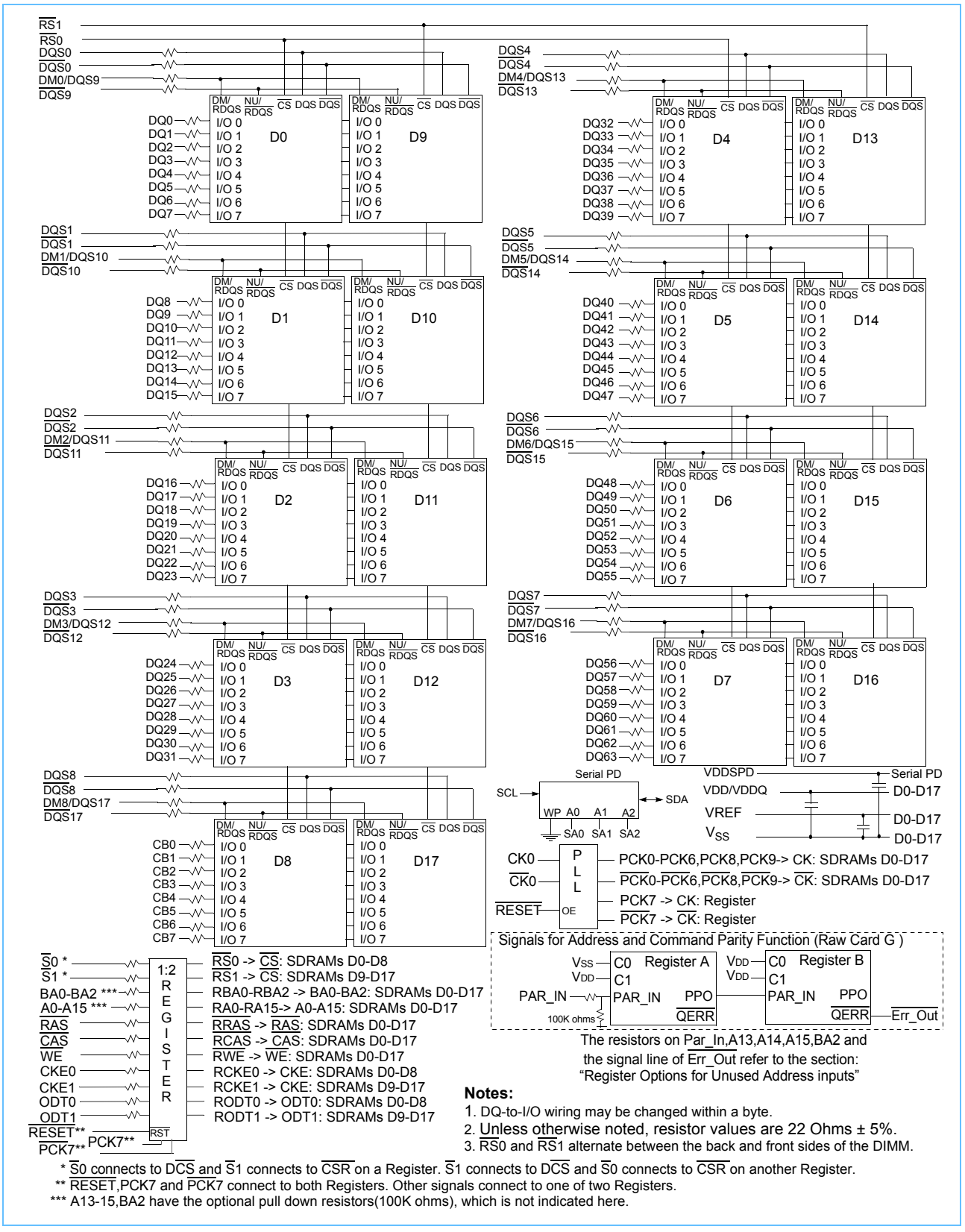
(x72 DIMM, populated as one physical rank of x8 DDR2 SDRAMs)



Petitioners
Ex. 1066, p. 9

Block Diagram: Raw Card Version B and G

(x72 DIMM, populated as two physical ranks of x8 DDR2 SDRAMs)



The resistors on Par_In,A13,A14,A15,BA2 and the signal line of Err_Out refer to the section: "Register Options for Unused Address inputs"

Notes:

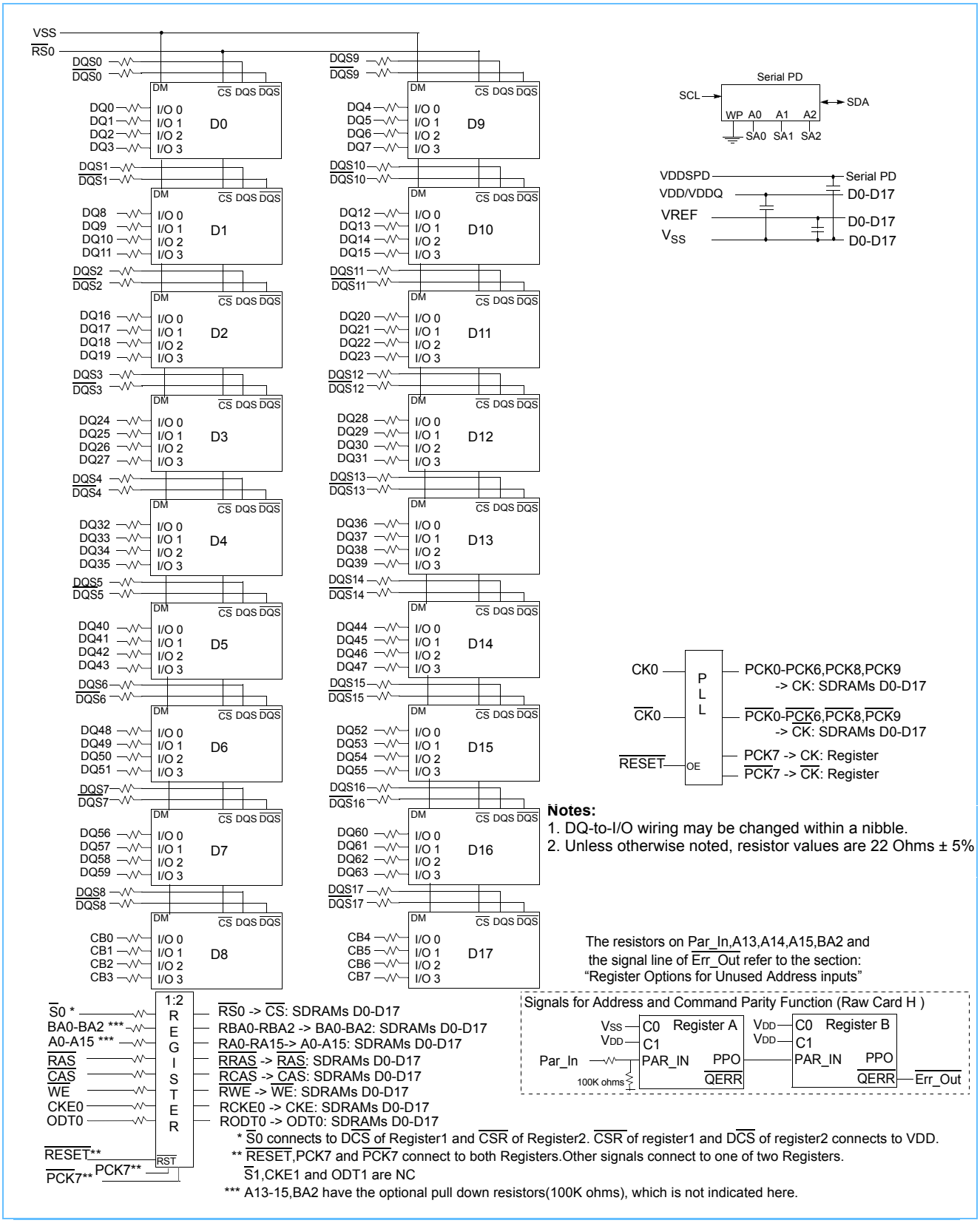
1. DQ-to-I/O wiring may be changed within a byte.
2. Unless otherwise noted, resistor values are 22 Ohms ± 5%.
3. RS0 and RS1 alternate between the back and front sides of the DIMM.

* S0 connects to DCS and S1 connects to CSR on a Register. S1 connects to DCS and S0 connects to CSR on another Register.
** RESET,PCK7 and PCK7 connect to both Registers. Other signals connect to one of two Registers.
*** A13-15,BA2 have the optional pull down resistors(100K ohms), which is not indicated here.

Petitioners
Ex. 1066, p. 10

Block Diagram: Raw Card Version C and H

(x72 DIMM Populated as one physical rank of x4 DDR2 SDRAMs)



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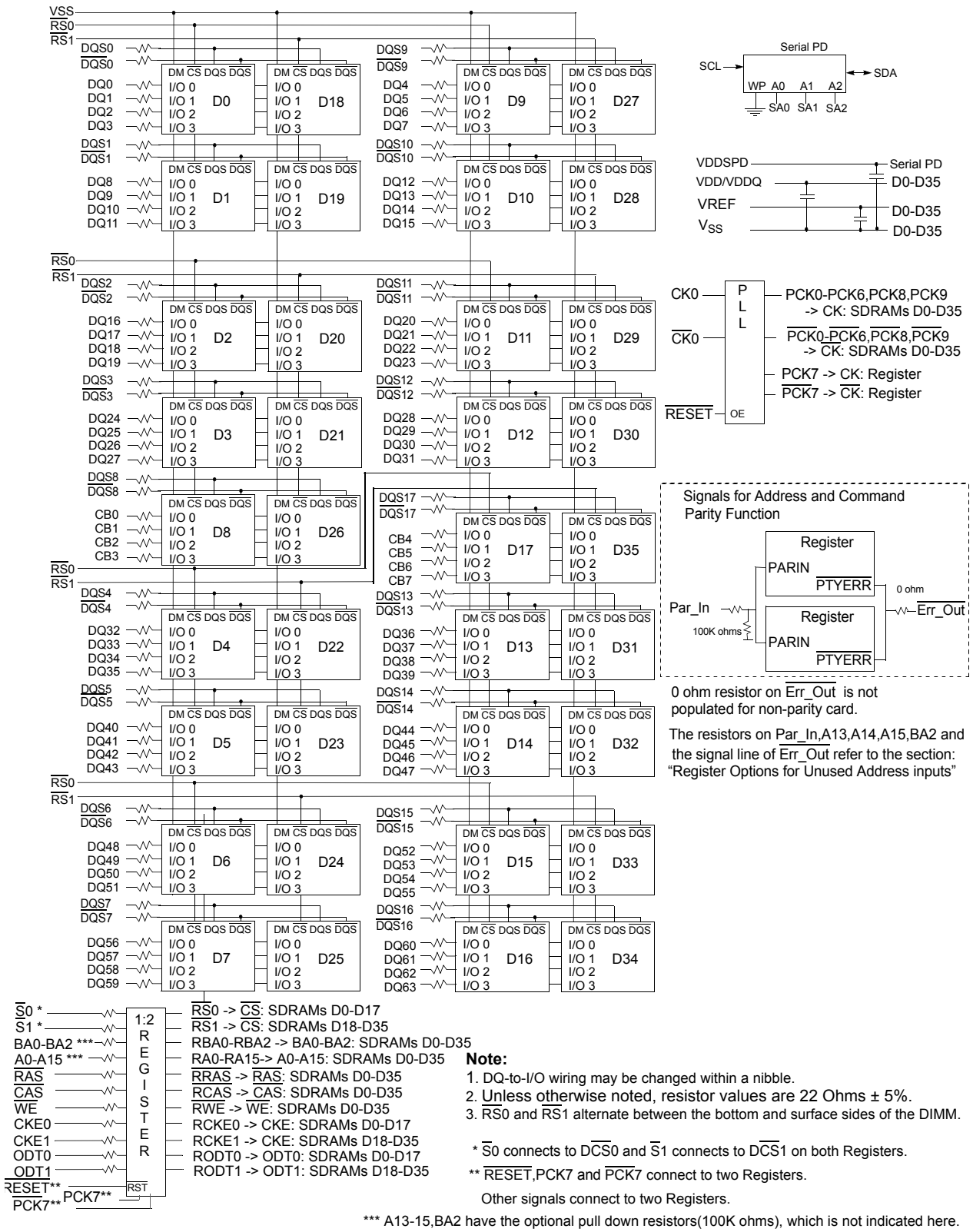
Ex. 1066, p. 11

Block Diagram: Raw Card Version D

(x72 DIMM, populated as two physical ranks of x4 stacked DDR2 SDRAMs)



Note:

1. DQ-to-I/O wiring may be changed within a nibble.
2. Unless otherwise noted, resistor values are 22 Ohms ± 5%.
3. RS0 and RS1 alternate between the bottom and surface sides of the DIMM.

* S0 connects to DCS0 and S1 connects to DCS1 on both Registers.

** RESET,PCK7 and PCK7 connect to two Registers.

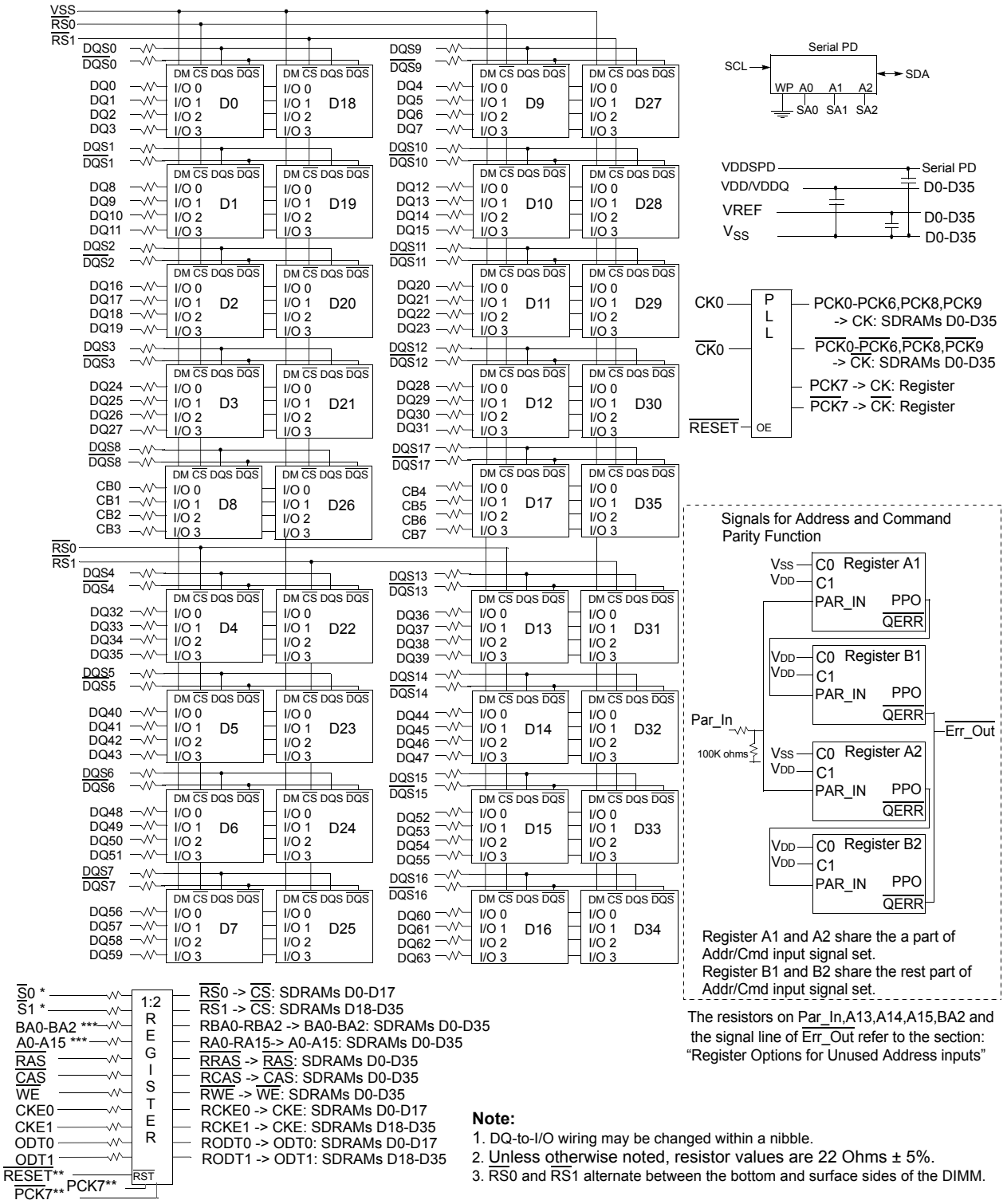
Other signals connect to two Registers.

*** A13-15,BA2 have the optional pull down resistors(100K ohms), which is not indicated here.

Petitioners
Ex. 1066, p. 12

Block Diagram: Raw Card Version E

(x72 DIMM, populated as two physical ranks of x4 stacked DDR2 SDRAMs)



Note:

1. DQ-to-I/O wiring may be changed within a nibble.
2. Unless otherwise noted, resistor values are 22 Ohms ± 5%.
3. RS0 and RS1 alternate between the bottom and surface sides of the DIMM.

* S0 connects to DCS and S1 connects to CSR on a pair of Registers. S1 connects to DCS and S0 connects to CSR on another pair of Registers.

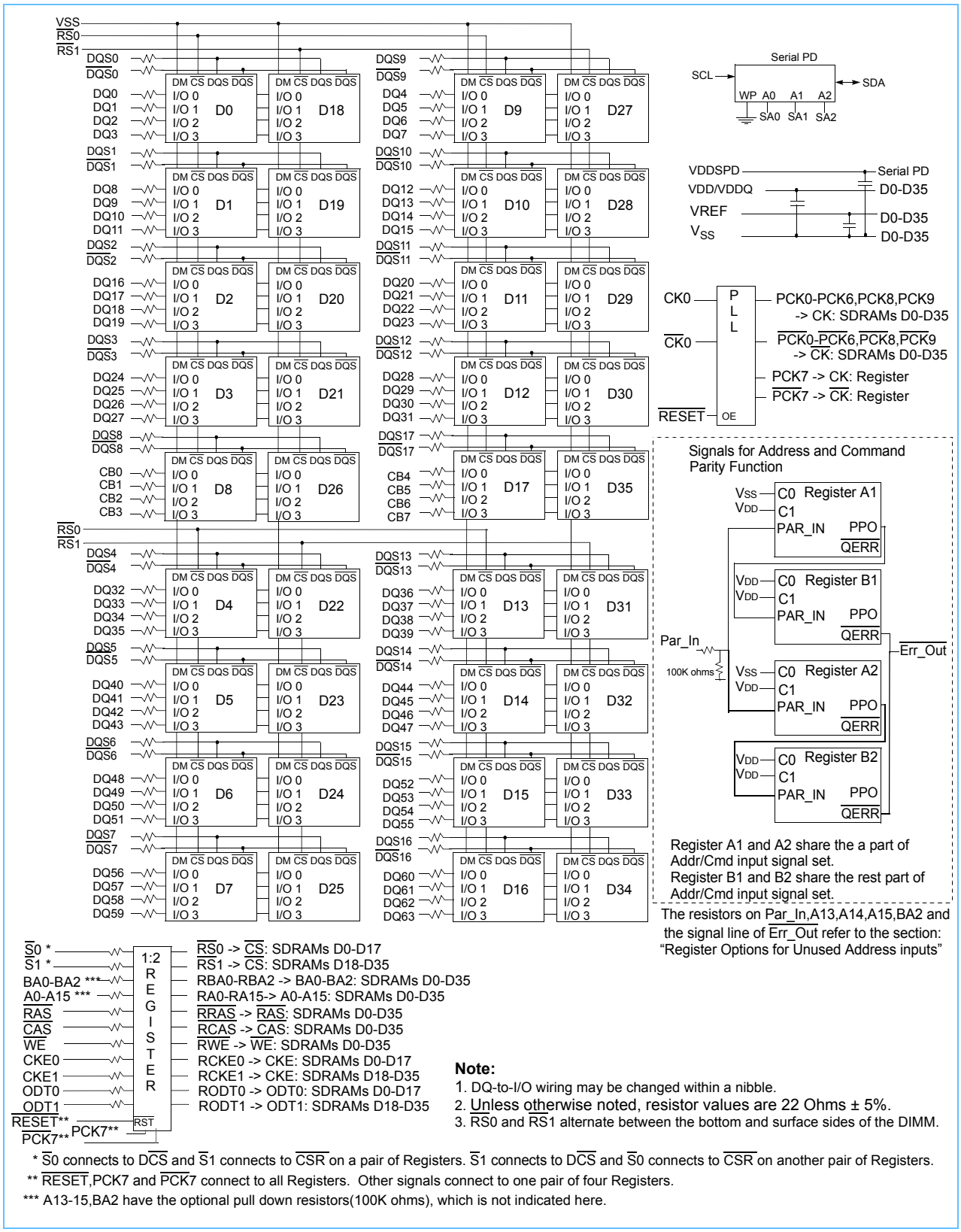
** RESET,PCK7 and PCK7 connect to all Registers. Other signals connect to one pair of four Registers.

*** A13-15,BA2 have the optional pull down resistors(100K ohms), which is not indicated here.

Petitioners
Ex. 1066, p. 13

Block Diagram: Raw Card Version J

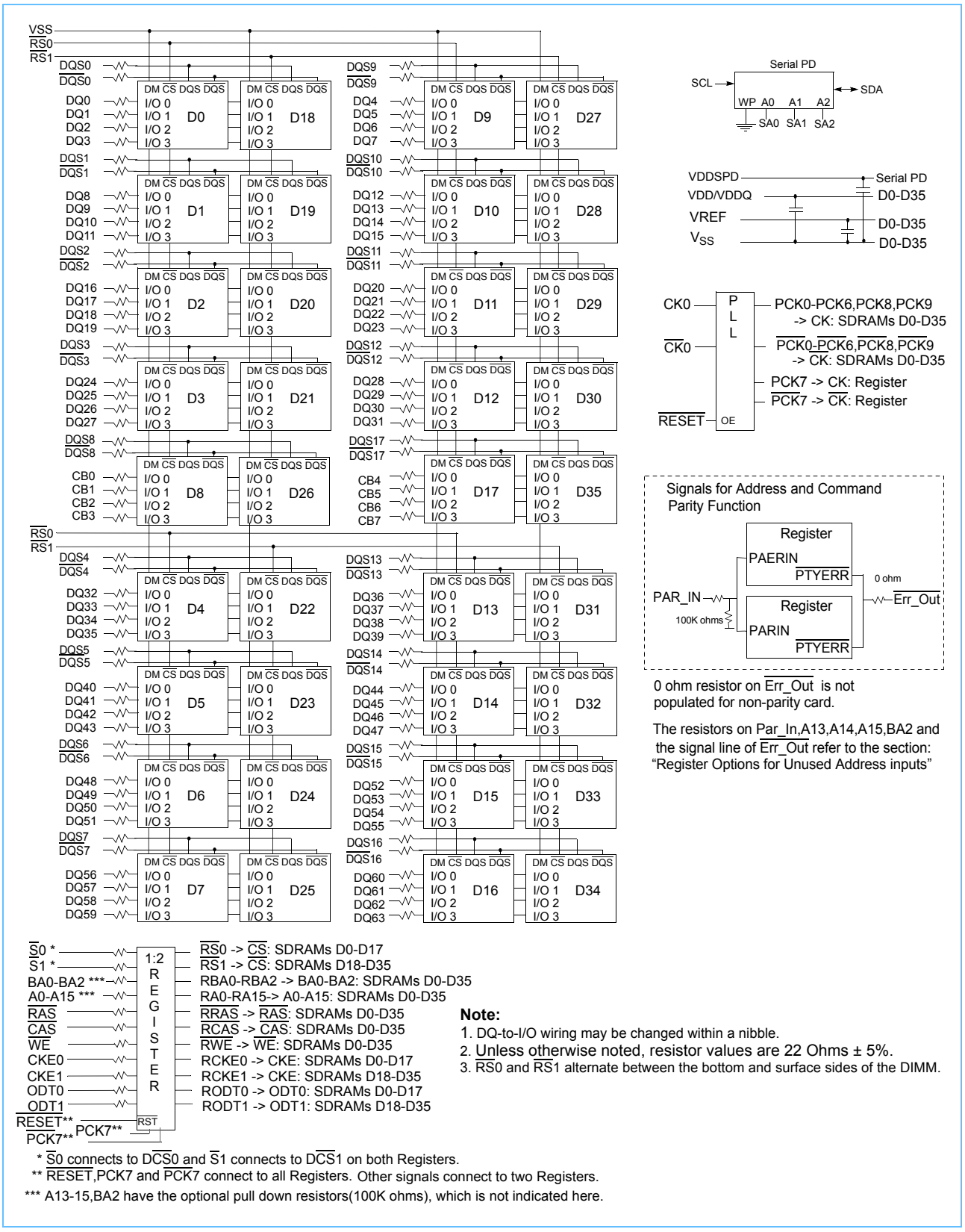
(x72 DIMM, populated as two physical ranks of x4 planar DDR2 SDRAMs)



Petitioners
Ex. 1066, p. 14

Block Diagram: Raw Card Version K

(x72 DIMM, populated as two physical ranks of x4 stacked DDR2 SDRAMs)



0 ohm resistor on Err_Out is not populated for non-parity card.

The resistors on Par_In,A13,A14,A15,BA2 and the signal line of Err_Out refer to the section: "Register Options for Unused Address inputs"

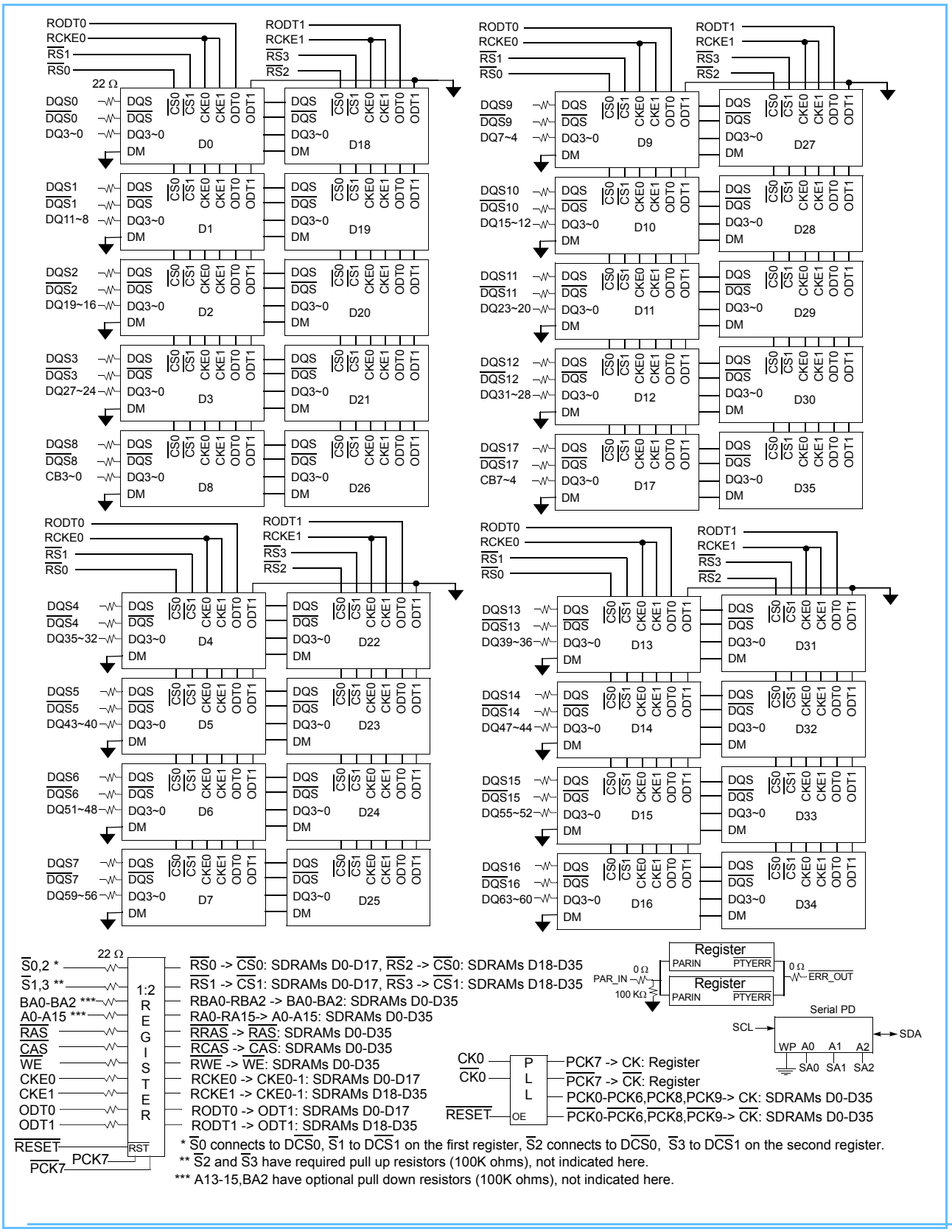
Note:

1. DQ-to-I/O wiring may be changed within a nibble.
2. Unless otherwise noted, resistor values are 22 Ohms ± 5%.
3. RS0 and RS1 alternate between the bottom and surface sides of the DIMM.

Petitioners
Ex. 1066, p. 15

Block Diagram: Raw Card Version M

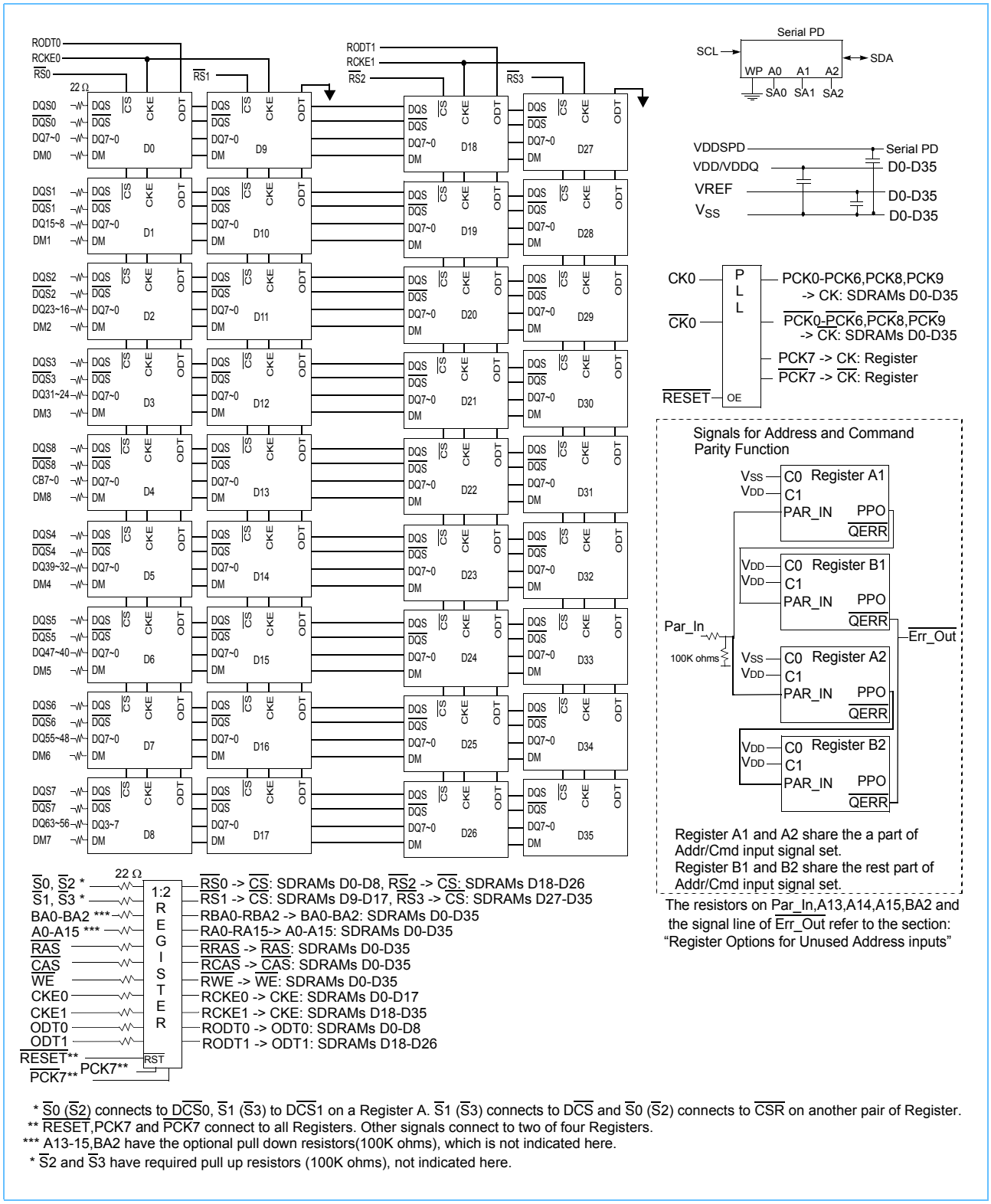
(x72 DIMM, populated as four ranks using 2-high stacked x4 DDR2 SDRAMs)



Petitioners
Ex. 1066, p. 16

Block Diagram: Raw Card Version N

(x72 DIMM, populated as four ranks of non-stacked x8 DDR2 SDRAMs)

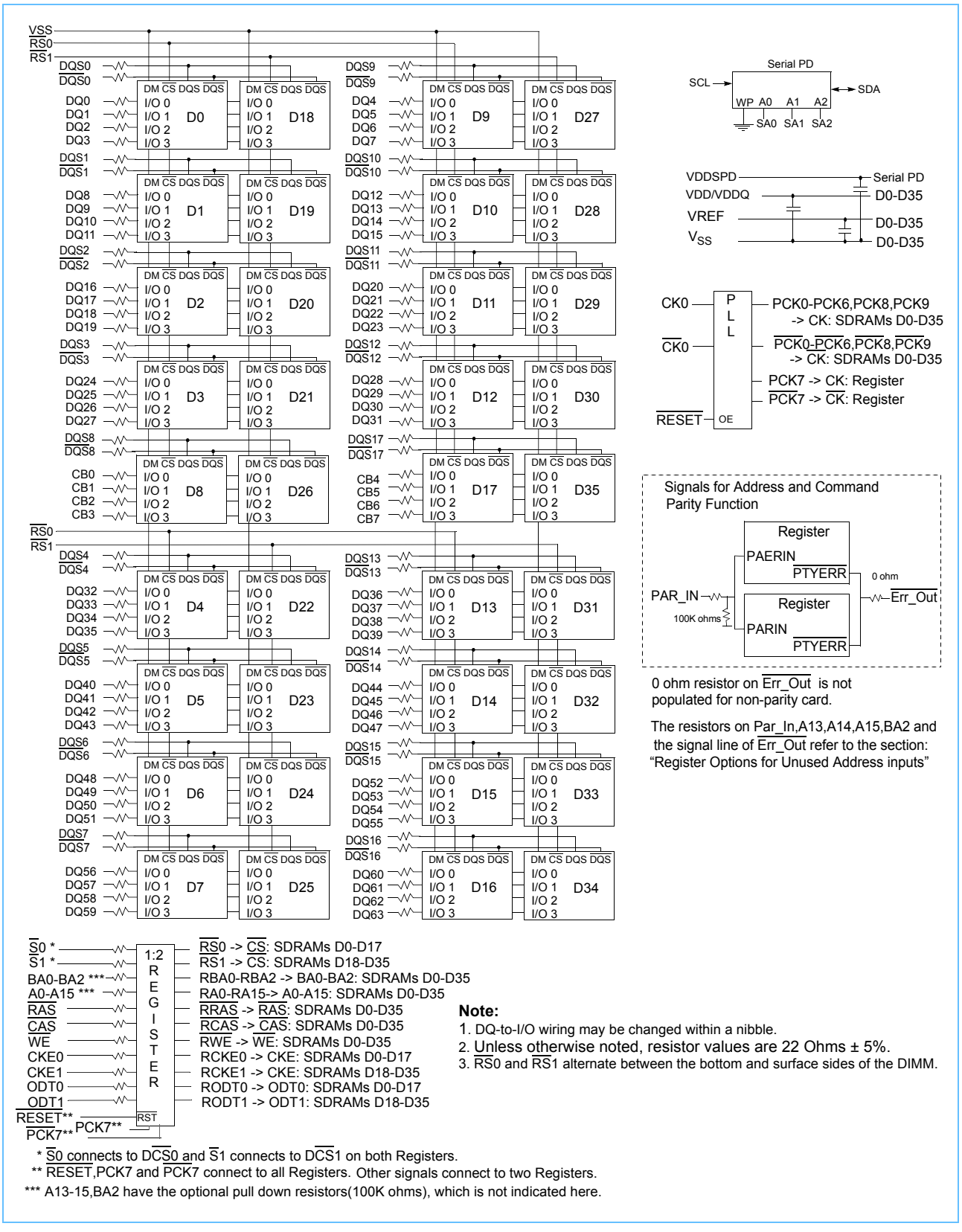


* S0 (S2) connects to DCS0, S1 (S3) to DCS1 on a Register A. S1 (S3) connects to DCS and S0 (S2) connects to CSR on another pair of Register.
** RESET,PCK7 and PCK7 connect to all Registers. Other signals connect to two of four Registers.
*** A13-15,BA2 have the optional pull down resistors(100K ohms), which is not indicated here.
* S2 and S3 have required pull up resistors (100K ohms), not indicated here.

Petitioners
Ex. 1066, p. 17

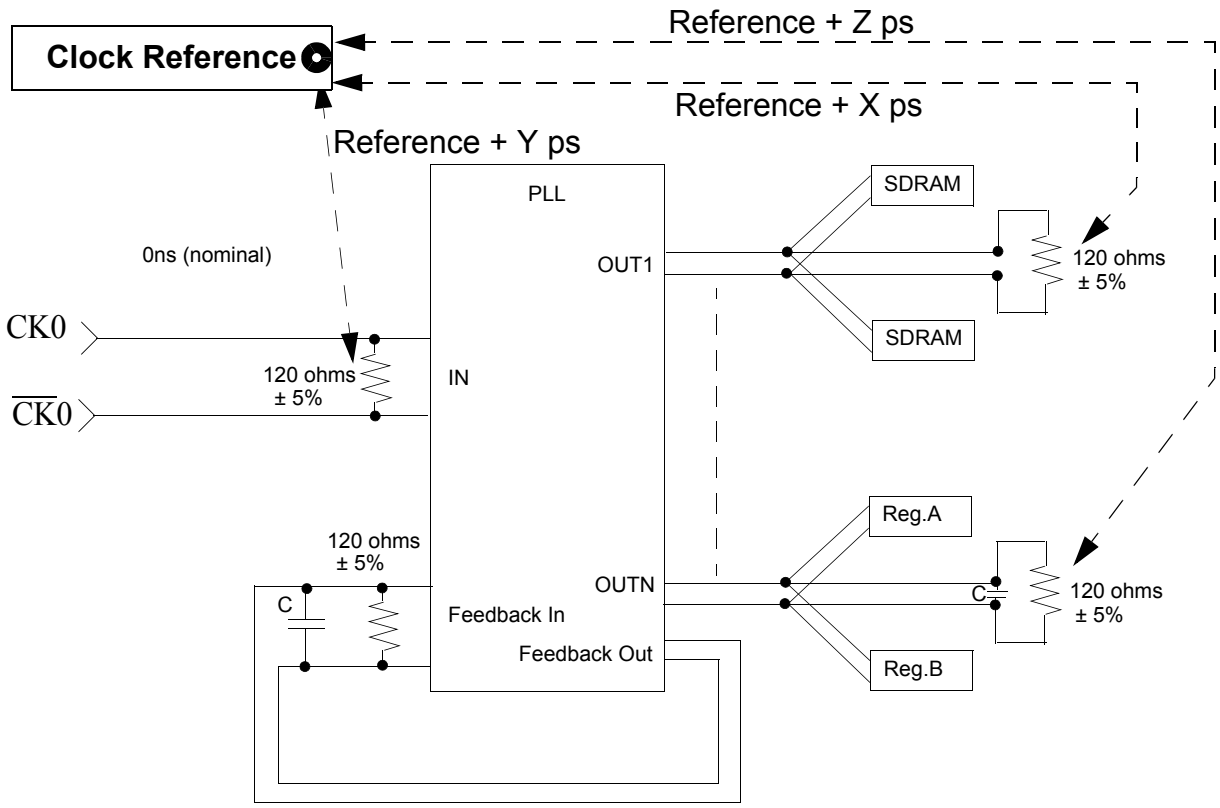
Block Diagram: Raw Card Version P

(x72 DIMM, populated as two physical ranks of x4 stacked DDR2 SDRAMs)



Petitioners
Ex. 1066, p. 18

Differential Clock Wiring CK0, $\overline{CK0}$



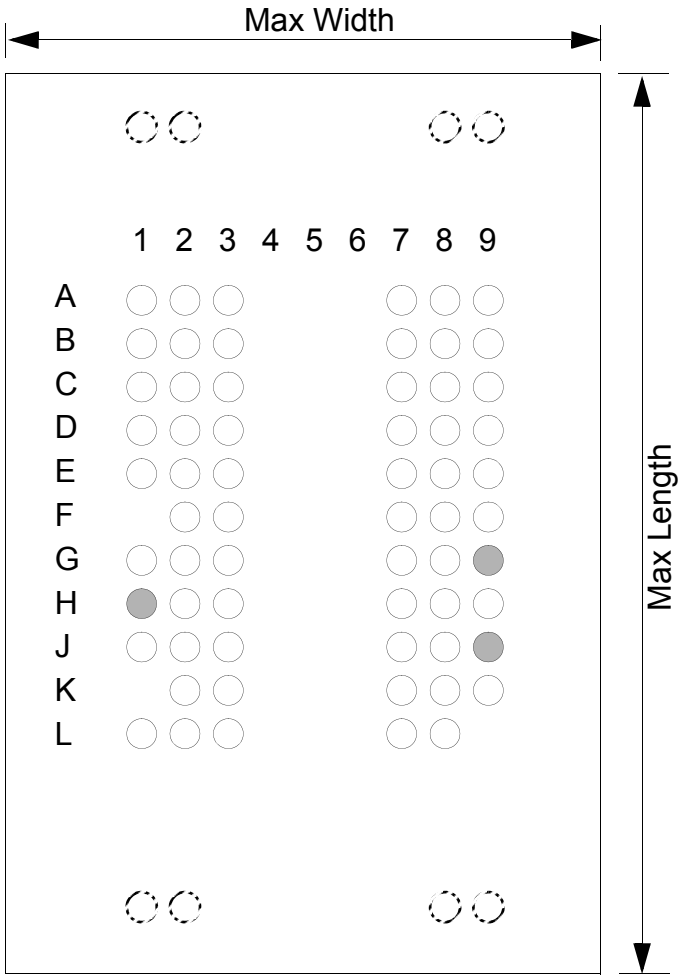
1. All clock nets are resistively terminated from line to line as shown, and not from line to ground.
2. Only one PLL output is shown per output type. Any additional PLL outputs will be wired in a similar manner.
3. Termination resistors are located as close to the CK/$\overline{CK}$ input balls as possible.
4. All clocks are referenced to a single timing reference (see section: “Supporting Hardware”)
5. Clocks are measured at the respective termination resistor.
6. There is a table for each raw card for the assumed offset $T_{SK(OFFSET)}$ (X, Y, Z) between the CK/$\overline{CK}$ input balls of the device and the measured clock at the termination resistor
7. The DRAM clocks (at CK/$\overline{CK}$ input balls of the DRAMs) are designed to be aligned with the Clock Reference (0 ns) (see section: Supporting Hardware)
8. The PLL input clock (at CK/$\overline{CK}$ input balls of the PLL) is typically designed to be very close to aligned with the Clock Reference (typically 0 ns; systematic deviations should be noted in the skew table for the raw card)
9. The Register input clock (at CK/$\overline{CK}$ input balls of the register) are designed to be aligned with the Clock Reference (0 ns); deviation must be noted explicitly, as this puts additional requirements onto the input setup/hold times of the register used.
10. For more details (especially about X, Y, Z), please refer to the section “Supporting Hardware” about the use of the clock reference board

Petitioners
Ex. 1066, p. 19

Component Details

Supported SDRAM Components Maximum size for 256Mb to 4Gb; DDR2 SDRAM

Raw Card	Supported DRAM Outline (Width x Lenght) max.	Package Type	MO-207 variation	MO-242 variation
A, B, C, F, G, H	11.3 (12.3 [1]) mm x 21.0 mm	Planar	DJ-z, DM-z	-
D, K	11.5 [2] (12.5 [1,2]) mm x 21.0 mm	Stacked	-	AA, AD
E	13.0 [1]mm x 16.3 mm	Stacked	-	AA, AD
J	11.0 mm x 11.5 mm	Planar	DJ-z	-
M	12.0 mm x 11.5 mm	Stacked	-	AA
N	11.0 mm x 11.5 mm	Planar	DJ-z	-
P	13.5 [1]mm x 16.5 mm	Stacked	-	AA, AD
1. supported only if no-decapling capacitor are placed in between the DRAMs 2. 0.4 mm DRAM to DRAM spacing				



Note: Dotted circles indicate the location of support balls of Variation DM-z
Gray circles indicate the balls for stacked only

Petitioners
Ex. 1066, p. 20

Pin Assignments for 256Mb to 4Gb; DDR2 SDRAM (Top View)

Without support balls (MO-207 Variation DJ-z, 60Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs (Top view)

	1	2	3	7	8	9
A	VDD	NC	VSS	VSSQ	$\overline{\text{DQS}}$	VDDQ
B	NC	VSSQ	DM	DQS	VSSQ	NC
C	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
D	NC	VSSQ	DQ3	DQ2	VSSQ	NC
E	VDDL	VREF	VSS	VSSDL	CK	VDD
F		CKE	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
G	BA2	BA0	BA1	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
H		A10	A1	A2	A0	VDD
J	VSS	A3	A5	A6	A4	
K		A7	A9	A11	A8	VSS
L	VDD	A12	A14,NC	A15,NC	A13,NC	

x8 Ballout of DDR2 SDRAMs (Top view)

1	2	3	7	8	9
VDD	NU/ RDQS	VSS	VSSQ	$\overline{\text{DQS}}$	VDDQ
DQ6	VSSQ	DM/ RDQS	DQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	VSSDL	CK	VDD
	CKE	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
BA2	BA0	BA1	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10	A1	A2	A0	VDD
VSS	A3	A5	A6	A4	
	A7	A9	A11	A8	VSS
VDD	A12	A14,NC	A15,NC	A13,NC	

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.
2. Above coordinates of ball out corresponds to footprint on PCB (page 25 ~).
3. “NC” means that the ball is present and is not connected to any signal in the SDRAM package. NC balls may be mated with any solder pad on PCB.
4. “NU” means that the ball is present and may or may not be electrically connected a an active signal in the SDRAM package. NU balls may only be mated with NC solder pads on PCB.

Petitioners
Ex. 1066, p. 21

Without support balls (MO-242 Variation AA, 63 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs for Stacked DIMM (Top view)

	1	2	3	7	8	9
A	VDD	NC	VSS	VSSQ	$\overline{\text{DQS}}$	VDDQ
B	NC	VSSQ	DM	DQS	VSSQ	NC
C	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
D	NC	VSSQ	DQ3	DQ2	VSSQ	NC
E	VDDL	VREF	VSS	VSSDL	CK	VDD
F		CKE0	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT0
G	BA2	BA0	BA1	$\overline{\text{CAS}}$	$\overline{\text{CS}}$0	$\overline{\text{CS}}$1
H	CKE1	A10	A1	A2	A0	VDD
J	VSS	A3	A5	A6	A4	ODT1
K		A7	A9	A11	A8	VSS
L	VDD	A12	A14,NC	A15,NC	A13,NC	

1. The thick line area indicates the minimum ball out for x4 DDR2 SDRAMs.
2. Above coordinates of ball out corresponds to footprint on PCB (page 25 ~).
3. “NC” means that the ball is present and is not connected to any signal in the SDRAM package. NC balls may be mated with any solder pad on PCB.

Petitioners
Ex. 1066, p. 22

With support balls (MO-207 Variation DM-z, 68 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs (Top view)

	1	2	3	7	8	9
A	NC	NC			NC	NC
B						
C						
D						
E	VDD	NC	VSS	VSSQ	$\overline{DQS}$	VDDQ
F	NC	VSSQ	DM	DQS	VSSQ	NC
G	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
H	NC	VSSQ	DQ3	DQ2	VSSQ	NC
J	VDDL	VREF	VSS	VSSDL	CK	VDD
K		CKE	$\overline{WE}$	$\overline{RAS}$	$\overline{CK}$	ODT
L	BA2	BA0	BA1	$\overline{CAS}$	$\overline{CS}$	
M		A10	A1	A2	A0	VDD
N	VSS	A3	A5	A6	A4	
P		A7	A9	A11	A8	VSS
R	VDD	A12	A14,NC	A15,NC	A13,NC	
T						
U						
V						
W	NC	NC			NC	NC

x8 Ballout of DDR2 SDRAMs (Top view)

	1	2	3	7	8	9
A	NC	NC			NC	NC
B						
C						
D						
E	VDD	NU/ $\overline{RDQS}$	VSS	VSSQ	$\overline{DQS}$	VDDQ
F	DQ6	VSSQ	DM/ RDQS	DQS	VSSQ	DQ7
G	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
H	DQ4	VSSQ	DQ3	DQ2	VSSQ	DQ5
J	VDDL	VREF	VSS	VSSDL	CK	VDD
K		CKE	$\overline{WE}$	$\overline{RAS}$	$\overline{CK}$	ODT
L	BA2	BA0	BA1	$\overline{CAS}$	$\overline{CS}$	
M		A10	A1	A2	A0	VDD
N	VSS	A3	A5	A6	A4	
P		A7	A9	A11	A8	VSS
R	VDD	A12	A14,NC	A15,NC	A13,NC	
T						
U						
V						
W	NC	NC			NC	NC

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.
2. NC balls on A1, A2, A8, A9, W1, W2, W8 and W9 in the double line area, are optional support balls.
3. Above coordinates of ball out corresponds to footprint on PCB (page 25 ~).
4. On the actual DIMM A1 & A9 in the double line area, have via connections to VDD and VDDQ respectively.
5. “NC” means that the ball is present and is not connected to any signal in the SDRAM package.
   NC balls may be mated with any solder pad on PCB.
6. “NU” means that the ball is present and may or may not be electrically connected a an active signal in the SDRAM package. NU balls may only be mated with NC solder pads on PCB.

Petitioners
Ex. 1066, p. 23

With support balls (MO-242 Variation AD, 71 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs for Stacked DIMM (Top view)

	1	2	3	7	8	9
A	NC	NC			NC	NC
B						
C						
D						
E	VDD	NC	VSS	VSSQ	$\overline{DQS}$	VDDQ
F	NC	VSSQ	DM	DQS	VSSQ	NC
G	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
H	NC	VSSQ	DQ3	DQ2	VSSQ	NC
J	VDDL	VREF	VSS	VSSDL	CK	VDD
K		CKE0	$\overline{WE}$	$\overline{RAS}$	$\overline{CK}$	ODT0
L	BA2	BA0	BA1	$\overline{CAS}$	$\overline{CS}$0	$\overline{CS}$1
M	CKE1	A10	A1	A2	A0	VDD
N	VSS	A3	A5	A6	A4	ODT1
P		A7	A9	A11	A8	VSS
R	VDD	A12	A14,NC	A15,NC	A13,NC	
T						
U						
V						
W	NC	NC			NC	NC

1. The thick line area indicates the minimum ball out for x4 DDR2 SDRAMs.
2. NC balls on A1, A2, A8, A9, W1, W2, W8 and W9 in the double line area, are optional support balls.
3. Above coordinates of ball out corresponds to footprint on PCB (page 25 ~).
4. On the actual DIMM A1 & A9 in the double line area, have via connections to VDD and VDDQ respectively.
5. “NC” means that the ball is present and is not connected to any signal in the SDRAM package.
   NC balls may be mated with any solder pad on PCB.

Petitioners
Ex. 1066, p. 24

SDRAM Landing Pattern on DIMM (Top View)

x4 footprint on PCB (Top view)

	1	2	3	7	8	9
A	NU	NU			NU	NU
B						
C						
D	VDD	NU	VSS	VSS	NU	VDD
E	NU	NU	NU	NU	NU	NU
F	NU	NU	NU	NU	NU	NU
G	NU	NU	NU	NU	NU	NU
H	VDD	NC	VSS	VSS	$\overline{DQS}$	VDD
J	NU	VSS	DM	DQS	VSS	NU
K	VDD	DQ1	VDD	VDD	DQ0	VDD
L	NU	VSS	DQ3	DQ2	VSS	NU
M	VDD	VREF	VSS	VSS	CK	VDD
N		CKE	$\overline{WE}$	$\overline{RAS}$	$\overline{CK}$	ODT
P	BA2	BA0	BA1	$\overline{CAS}$	$\overline{CS}$	
R		A10/AP	A1	A2	A0	VDD
T	VSS	A3	A5	A6	A4	
U		A7	A9	A11	A8	VSS
V	VDD	A12	A14	A15	A13	
W						
Y						
AA	NU	NU			NU	NU
AB	NU	NU			NU	NU

x8 footprint on PCB (Top view)

1	2	3	7	8	9
NU	NU			NU	NU
VDD	NU	VSS	VSS	NU	VDD
NU	NU	NU	NU	NU	NU
NU	NU	NU	NU	NU	NU
NU	NU	NU	NU	NU	NU
VDD	$\overline{RDQS}$	VSS	VSS	$\overline{DQS}$	VDD
DQ6	VSS	DM/ RDQS	DQS	VSS	DQ7
VDD	DQ1	VDD	VDD	DQ0	VDD
DQ4	VSS	DQ3	DQ2	VSS	DQ5
VDD	VREF	VSS	VSS	CK	VDD
	CKE	$\overline{WE}$	$\overline{RAS}$	$\overline{CK}$	ODT
BA2	BA0	BA1	$\overline{CAS}$	$\overline{CS}$	
	A10/AP	A1	A2	A0	VDD
VSS	A3	A5	A6	A4	
	A7	A9	A11	A8	VSS
VDD	A12	A14	A15	A13	
NU	NU			NU	NU
NU	NU			NU	NU

1. Above coordinates of footprint corresponds to previous ballout of DDR2 SDRAMs.
2. “NC” means that a solder pad is present and is not connected to any signal on the PCB. NC solder pads may be mated with any balls of an SDRAM.
3. “NU” means that the solder pad is present and may or may not be electrically connected a an active signal on the PCB. NU solder pads may only be mated with NC balls of an SDRAMs

Petitioners
Ex. 1066, p. 25

SDRAM Landing Pattern on DIMM (Top View)

x4 footprint on PCB for Stacked DIMM (Top view)

	1	2	3	7	8	9
A	NU	NU			NU	NU
B						
C						
D	VDD	NU	VSS	VSS	NU	VDD
E	NU	NU	NU	NU	NU	NU
F	NU	NU	NU	NU	NU	NU
G	NU	NU	NU	NU	NU	NU
H	VDD	NC	VSS	VSS	$\overline{DQS}$	VDD
J	NU	VSS	DM	DQS	VSS	NU
K	VDD	DQ1	VDD	VDD	DQ0	VDD
L	NU	VSS	DQ3	DQ2	VSS	NU
M	VDD	VREF	VSS	VSS	CK	VDD
N		CKE0	$\overline{WE}$	$\overline{RAS}$	$\overline{CK}$	ODT0
P	BA2	BA0	BA1	$\overline{CAS}$	$\overline{CS0}$	$\overline{CS1}$
R	CKE1	A10/AP	A1	A2	A0	VDD
T	VSS	A3	A5	A6	A4	ODT1
U		A7	A9	A11	A8	VSS
V	VDD	A12	A14	A15	A13	
W						
Y						
AA	NU	NU			NU	NU
AB	NU	NU			NU	NU

1. Above coordinates of footprint corresponds to previous ballout of DDR2 SDRAMs.
2. “NC” means that a solder pad is present and is not connected to any signal on the PCB.
   NC solder pads may be mated with any balls of an SDRAM.
3. “NU” means that the solder pad is present and may or may not be electrically connected a an active signal on the PCB. NU solder pads may only be mated with NC balls of an SDRAMs

Petitioners
Ex. 1066, p. 26

Pin Assignments for SSTU32864 1:2 / 1:1 Register without Address and Command Parity Function (Top View)

96-Ball LFBGA 0.8 x 0.8 mm pitch [MO-205 CC], programmable pinout configuration

1:2 Register A (C0 = 0, C1 = 1)

	1	2	3	4	5	6
A	DCKE	NC	VREF	VDD	QCKEA	QCKEB
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	VDD	VDD	Q3A	Q3B
D	DODT	NC	GND	GND	QODTA	QODTB
E	D5	DNU	VDD	VDD	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	NC	$\overline{RST}$	VDD	VDD	C1	C0
H	CK	D$\overline{CS}$	GND	GND	Q$\overline{CS}$A	Q$\overline{CS}$B
J	$\overline{CK}$	$\overline{CSR}$	VDD	VDD	ZOH	ZOL
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	VDD	VDD	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11	DNU	VDD	VDD	Q11A	Q11B
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	VDD	VDD	Q13A	Q13B
T	D14	DNU	VREF	VDD	Q14A	Q14B

1:2 Register B (C0 = 1, C1 = 1)

	1	2	3	4	5	6
A	D1	NC	VREF	VDD	Q1A	Q1B
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	VDD	VDD	Q3A	Q3B
D	D4	NC	GND	GND	Q4A	Q4B
E	D5	DNU	VDD	VDD	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	NC	$\overline{RST}$	VDD	VDD	C1	C0
H	CK	D$\overline{CS}$	GND	GND	Q$\overline{CS}$A	Q$\overline{CS}$B
J	$\overline{CK}$	$\overline{CSR}$	VDD	VDD	ZOH	ZOL
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	VDD	VDD	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	DODT	DNU	VDD	VDD	QODTA	QODTB
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	VDD	VDD	Q13A	Q13B
T	DCKE	DNU	VREF	VDD	QCKEA	QCKEB

Petitioners
Ex. 1066, p. 27

1:1 Register (C0 = 0, C1 = 0)

	1	2	3	4	5	6
A	DCKE	NC	VREF	VDD	QCKE	DNU
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	VDD	VDD	Q3	Q16
D	DODT	NC	GND	GND	QODT	DNU
E	D5	D17	VDD	VDD	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	NC	$\overline{RST}$	VDD	VDD	C1	C0
H	CK	D$\overline{CS}$	GND	GND	Q$\overline{CS}$	DNU
J	$\overline{CK}$	$\overline{CSR}$	VDD	VDD	ZOH	ZOL
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	VDD	VDD	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	VDD	VDD	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	VDD	VDD	Q13	Q24
T	D14	D25	VREF	VDD	Q14	Q25

1. NC (: No-Connect) denotes a ball that is not connected to the die.
2. DNU (: Do-Not-Use) denotes a ball that is connected to the die but it should be left open circuit.

Petitioners
Ex. 1066, p. 28

Pin Assignments for SSTU32866/SSTUA32866/SSTUB32866 1:2 / 1:1 Register with Address and Command Parity Function (Top View)

96-Ball LFBGA 0.8 x 0.8 mm pitch [MO-205 CC], programmable pinout configuration

1:2 Register A (C0 = 0, C1 = 1)

	1	2	3	4	5	6
A	DCKE	PPO	VREF	VDD	QCKEA	QCKEB
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	VDD	VDD	Q3A	Q3B
D	DODT	$\overline{\text{QERR}}$	GND	GND	QODTA	QODTB
E	D5	DNU	VDD	VDD	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	PAR_IN	$\overline{\text{RST}}$	VDD	VDD	C1	C0
H	CK	D$\overline{\text{CS}}$	GND	GND	Q$\overline{\text{CS}}$A	Q$\overline{\text{CS}}$B
J	$\overline{\text{CK}}$	$\overline{\text{CSR}}$	VDD	VDD	ZOH	ZOL
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	VDD	VDD	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11	DNU	VDD	VDD	Q11A	Q11B
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	VDD	VDD	Q13A	Q13B
T	D14	DNU	VREF	VDD	Q14A	Q14B

1:2 Register B (C0 = 1, C1 = 1)

	1	2	3	4	5	6
A	D1	PPO	VREF	VDD	Q1A	Q1B
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	VDD	VDD	Q3A	Q3B
D	D4	$\overline{\text{QERR}}$	GND	GND	Q4A	Q4B
E	D5	DNU	VDD	VDD	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	PAR_IN	$\overline{\text{RST}}$	VDD	VDD	C1	C0
H	CK	D$\overline{\text{CS}}$	GND	GND	Q$\overline{\text{CS}}$A	Q$\overline{\text{CS}}$B
J	$\overline{\text{CK}}$	$\overline{\text{CSR}}$	VDD	VDD	ZOH	ZOL
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	VDD	VDD	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	DODT	DNU	VDD	VDD	QODTA	QODTB
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	VDD	VDD	Q13A	Q13B
T	DCKE	DNU	VREF	VDD	QCKEA	QCKEB

Petitioners
Ex. 1066, p. 29

1:1 Register (C0 = 0, C1 = 0)

	1	2	3	4	5	6
A	DCKE	PPO	VREF	VDD	QCKE	DNU
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	VDD	VDD	Q3	Q16
D	DODT	$\overline{\text{QERR}}$	GND	GND	QODT	DNU
E	D5	D17	VDD	VDD	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	PAR_IN	$\overline{\text{RST}}$	VDD	VDD	C1	C0
H	CK	D$\overline{\text{CS}}$	GND	GND	Q$\overline{\text{CS}}$	DNU
J	$\overline{\text{CK}}$	$\overline{\text{CSR}}$	VDD	VDD	ZOH	ZOL
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	VDD	VDD	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	VDD	VDD	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	VDD	VDD	Q13	Q24
T	D14	D25	VREF	VDD	Q14	Q25

1. NC (: No-Connect) denotes a ball that is not connected to the die.
2. DNU (: Do-Not-Use) denotes a ball that is connected to the die but it should be left open circuit.

Petitioners
Ex. 1066, p. 30

Pin Assignments for SSTU32865/SSTUA32S865/SSTUA32D865/SSTUB32S865/SSTUB32D865 1:2 Register with Address and Command Parity Function (Top View)

160-Ball TFBGA 0.65 x 0.65 mm pitch [MO-246A]

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	NC	PARIN	NC	NC	QCKE1A	QCKE0A	Q21A	Q19A	Q18A	Q17B	Q17A
B	D1	D2	NC	NC	NC	QCKE1B	QCKE0B	Q21B	Q19B	Q18B	QODT0B	QODT0A
C	D3	D4									QODT1B	QODT1A
D	D6	D5		VDDL	GND	NC	NC	GND	GND		Q20B	Q20A
E	D7	D8		VDDL	GND	VDDL	VDDR	GND	GND		Q16B	Q16A
F	D11	D9		VDDL	GND			VDDR	VDDR		Q1B	Q1A
G	D18	D12		VDDL	GND			VDDR	VDDR		Q2B	Q2A
H	CSGate EN	D15		VDDL	GND			GND	GND		Q5B	Q5A
J	CK	D$\overline{\text{CS}}$0		GND	GND			VDDR	VDDR		Q$\overline{\text{CS}}$0B	Q$\overline{\text{CS}}$0A
K	$\overline{\text{CK}}$	D$\overline{\text{CS}}$1		VDDL	VDDL			GND	GND		Q$\overline{\text{CS}}$1B	Q$\overline{\text{CS}}$1A
L	$\overline{\text{RESET}}$	D14		GND	GND			VDDR	VDDR		Q6B	Q6A
M	D0	D10		GND	GND			GND	GND		Q10B	Q10A
N	D17	D16		VDDL	VDDL			VDDR	VDDR		Q9B	Q9A
P	D19	D21		GND	VDDL	VDDL	VDDR	VDDR	GND		Q11B	Q11A
R	D13	D20		GND	VDDL	VDDL	GND	GND	GND		Q15B	Q15A
T	DODT1	DODT0									Q14B	Q14A
U	DCKE0	DCKE1	MCL	$\overline{\text{PTYERR}}$	MCH	Q3B	Q12B	Q7B	Q4B	Q13B	Q0B	Q8B
V	VREF	MCL	MCL	NC	MCH	Q3A	Q12A	Q7A	Q4A	Q13A	Q0A	Q8A

1. MCL denotes a pin that Must be Connected to logic Low.
   MCH denotes a pin that Must be Connected to logic High.
2. NC denotes a ball that is not connect to the die. A empty cell denotes no ball is populated.
3. CSGateEN is Tied High.

Petitioners
Ex. 1066, p. 31

Pin Assignments for SSTU32868/SSTUA32S868/SSTUA32D868/SSTUB32S868/SSTUB32D868 1:2 Register with Address and Command Parity Function (Top View)

176-Ball TFBGA 0.65 x 0.65 mm pitch [MO-TBD]

Register A (C = 0)

	1	2	3	4	5	6	7	8
A	D2	D1	C0	GND	VREF	GND	QA1	QB1
B	D4	D3	VDD	VDD	VDD	VDD	QA2	QB2
C	D6 (DCKE1)	D5	GND	GND	GND	GND	QA3	QB3
D	D8 (DCKE0)	D7	VDD	VDD	VDD	VDD	QA4	QB4
E	D9	QA6 (QACKE1)	GND	GND	GND	GND	QA5	QB5
F	D10	QA8 (QACKE0)	VDD	VDD	VDD	VDD	QA7	QB6 (QBCKE1)
G	D11	QA10	GND	GND	GND	GND	QA9	QB7
H	D12	QA12	VDD	VDD	VDD	VDD	QA11	QB8 (QBCKE0)
J	D13 (DCS1)	QA13 (QACS1)	GND	GND	GND	GND	QB10	QB9
K	D14 (DCS0)	QA14 (QACS0)	VDD	VDD	VDD	VDD	QB12	QB11
L	CK	CSGateEN	PARIN	GND	GND	GND	QB14 (QBCS0)	QB13 (QBCS1)
M	$\overline{CK}$	$\overline{RST}$	$\overline{PTYERR}$	VDD	VDD	VDD	QB15 (QBODT0)	QB16 (QBODT1)
N	D15 (DODT0)	QA15 (QAODT0)	GND	GND	GND	GND	QB17	QB18
P	D16 (DODT1)	QA16 (QAODT1)	VDD	VDD	VDD	VDD	QB19	QB20
R	D17	QA17	GND	GND	GND	GND	QA18	QB21
T	D18	QA19	VDD	VDD	VDD	VDD	QA20	QB22
U	D19	QA21	GND	GND	GND	GND	QA22	QB23
V	D20	QA23	VDD	VDD	VDD	VDD	QA24	QB24
W	D21	D22	GND	GND	GND	GND	QA25	QB25
Y	D23	D24	VDD	VDD	VDD	VDD	QA26	QB26
AA	D25	D26	GND	GND	GND	GND	QA27	QB27
AB	D27	D28	NC	VDD	VREF	VDD	QA28	QB28

1. NC denotes a ball that is not connect to the die.
2. CSGateEN is Tied High.

Petitioners
Ex. 1066, p. 32

Register B (C = 1)

	1	2	3	4	5	6	7	8
A	D2	D1	C0	GND	VREF	GND	QA1	QB1
B	D4	D3	VDD	VDD	VDD	VDD	QA2	QB2
C	D6	D5	GND	GND	GND	GND	QA3	QB3
D	D8	D7	VDD	VDD	VDD	VDD	QA4	QB4
E	D9	QA6	GND	GND	GND	GND	QA5	QB5
F	D10	QA8	VDD	VDD	VDD	VDD	QA7	QB6
G	D11	QA10	GND	GND	GND	GND	QA9	QB7
H	D12	QA12	VDD	VDD	VDD	VDD	QA11	QB8
J	D13 (DODT1)	QA13 (QAODT1)	GND	GND	GND	GND	QB10	QB9
K	D14 (DODT0)	QA14 (QAODT0)	VDD	VDD	VDD	VDD	QB12	QB11
L	CK	CSGateEN	PARIN	GND	GND	GND	QB14 (QBODT0)	QB13 (QBODT1)
M	$\overline{CK}$	$\overline{RST}$	$\overline{PTYERR}$	VDD	VDD	VDD	QB15 (QBCS0)	QB16 (QBCS1)
N	D15 (DCS0)	QA15 (QACS0)	GND	GND	GND	GND	QB17	QB18
P	D16 (DCS1)	QA16 (QACS1)	VDD	VDD	VDD	VDD	QB19	QB20
R	D17	QA17	GND	GND	GND	GND	QA18	QB21 (QBCKE0)
T	D18	QA19	VDD	VDD	VDD	VDD	QA20	QB22
U	D19	QA21 (QACKE0)	GND	GND	GND	GND	QA22	QB23 (QBCKE1)
V	D20	QA23 (QACKE1)	VDD	VDD	VDD	VDD	QA24	QB24
W	D21 (DCKE0)	D22	GND	GND	GND	GND	QA25	QB25
Y	D23 (DCKE1)	D24	VDD	VDD	VDD	VDD	QA26	QB26
AA	D25	D26	GND	GND	GND	GND	QA27	QB27
AB	D27	D28	NC	VDD	VREF	VDD	QA28	QB28

1. NC denotes a ball that is not connect to the die.
2. CSGateEN is Tied High.

Petitioners
Ex. 1066, p. 33

Pin Assignments for PLL Clock Driver CU877/CUA877 (Top View)

52-Ball FBGA 0.65 mm x 0.65 mm pitch [MO-225 BA]

	1	2	3	4	5	6
A	Y1	Y0	$\overline{Y0}$	$\overline{Y5}$	Y5	Y6
B	$\overline{Y1}$	GND	GND	GND	GND	$\overline{Y6}$
C	$\overline{Y2}$	GND			GND	$\overline{Y7}$
D	Y2	VDDQ	VDDQ	VDDQ	OS	Y7
E	CK	VDDQ			VDDQ	Fbin
F	$\overline{CK}$	VDDQ			OE	$\overline{Fbin}$
G	AGND	VDDQ	VDDQ	VDDQ	VDDQ	$\overline{Fbout}$
H	AVDD	GND			GND	Fbout
J	Y3	GND	GND	GND	GND	Y8
K	$\overline{Y3}$	$\overline{Y4}$	Y4	Y9	$\overline{Y9}$	$\overline{Y8}$

Petitioners
Ex. 1066, p. 34

Register Component Specifications

Please refer to the vendor register data sheets for all technical specifications and requirements. Below is a chart explaining which registers should be used on each DIMM type.

DIMM Register Use

Raw Card Version	# of Ranks	# of SDRAMs per output	Register Type	Register Speed Grade PC2-4200/PC2-3200	Register Speed Grade PC2-5300	Register Speed Grade PC2-6400	Quantity
A	1	9	1:1 25-bit 1.8V	SSTU32864	-	-	1
B	2	10/ 8 /5 /4	1:2 14-bit 1.8V	SSTU32864	-	-	2
C	1	10/ 8	1:2 14-bit 1.8V	SSTU32864	-	-	2
D	2	10/ 8/ 5/ 4	1:2 28-bit 1.8V	SSTU32865 / SSTUA32S865 / SSTUA32D865[2] / SSTUB32S865 / SSTUB32D865[2]	SSTUA32S865 / SSTUA32D865[2] / SSTUB32S865 / SSTUB32D865[2]	SSTUB32S865[2] / SSTUB32D865[2]	2
E	2	12/ 10 / 8	1:2 14-bit 1.8V	SSTU32866 / SSTU32864[1] / SSTUA32866	-	-	4
F	1	9	1:1 25-bit 1.8V	SSTU32866 / SSTU32864[1] / SSTUA32866	SSTUA32866 / SSTUB32866	SSTUB32866	1
G	2	10/ 8 /5 /4	1:2 14-bit 1.8V	SSTU32866 / SSTU32864[1] / SSTUA32866	SSTUA32866 / SSTUB32866	SSTUB32866	2
H	1	10/ 8	1:2 14-bit 1.8V	SSTU32866 / SSTU32864[1] / SSTUA32866 / SSTUB32866	SSTUA32866 / SSTUB32866	SSTUB32866	2
J	2	10/ 8	1:2 14-bit 1.8V	SSTUA32866 / SSTUB32866	SSTUB32866	-	4
K	2	12/ 8/ 6/ 4	1:2 28-bit 1.8V	SSTU32868 / SSTUA32S868 / SSTUA32D868[2] / SSTUB32S868 / SSTUB32D868[2]	SSTUA32S868 / SSTUA32D868[2] / SSTUB32S868 / SSTUB32D868[2]	SSTUB32S868[2] / SSTUB32D868[2]	2
M	4	20/ 16/ 10/ 8	1:2 28-bit 1.8V	SSTU32868 / SSTUA32S868 / SSTUA32D868[2]	-	-	2
N	4	10/ 8	1:2 14-bit 1.8V	SSTU32866 / SSTU32864[1]	-	-	4
P	2	12/ 8/ 6/ 4	1:2 28-bit 1.8V	SSTU32868 / SSTUA32S868 / SSTUA32D868[2] / SSTUB32S868 / SSTUB32D868[2]	SSTUA32S868 / SSTUA32D868[2] / SSTUB32S868 / SSTUB32D868[2]	-	2

1. The SSTU32864 is an optional part number which may be used to assemble a non-parity DIMM using these raw cards. The different register options are explained on the following page.
2. The SSTUA32S865/S868,SSTUB32S865/S868 has a single die in its package. The SSTUA32D865/D868,SSTUB32D865/D868 has dual die in its package.

Petitioners
Ex. 1066, p. 35

The following specifications for the register are critical for proper operation of the DDR2 SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the device.

Critical Register Specifications for PC2-3200/PC2-4200

Register	Symbol	Parameter	Conditions	T_A = 0 - 70 ºC V_{DD} = 1.8 V ± 0.1 V		Units	Notes
				Min	Max		
1:1 25-bit and 1:2 14-bit and 1:2 28-bit	f_{CK}	Clock Frequency			270	MHz	
	t_W	Pulse duration, CK, $\overline{CK}$ high or low	TBD	1		ns	
	t_{PDM}	Clock to Output Time	Includes 350 ps test-load transmission-line delay	1.41	2.15	ns	2,3
	t_{PDMSS}	Clock to Output Time (Simultaneous switching)	Includes 350 ps test-load transmission-line delay		2.35	ns	2
	t_{ACT}	Differential inputs active time			10	ns	
	t_{INACT}	Differential inputs inactive time			15	ns	
	t_{SU}	D$\overline{CS}$ and $\overline{CSR}$ signals	Previous $\overline{CSR}$=High	0.7		ns	1
	t_{SU}	All other input signals		0.5		ns	1
	t_H	Hold Time		0.5		ns	1
	$C_{IN(DATA)}$	Data Input Capacitance		2.5	3.5	pF	
	$C_{IN(CLOCK)}$	Clock Input Capacitance		2.0	3.0	pF	
	$C_{IN(RST)}$	Reset Input Capacitance		TBD	TBD	pF	

1. All input slew rate = 1 V/ns ± 20 %
2. Load circuit is specified in JESD82-6 for the SSTU32864, JESD82-9 for the SSTU32865
3. For PC2-4200 RC J a number of tPDM = 1.8 ns / tPDMSS = 2.0 ns is currently beeing discussed.

Petitioners
Ex. 1066, p. 36

Critical Register Specifications for PC2-5300

Register	Symbol	Parameter	Conditions	T_A = 0 - 70 °C V_{DD} = 1.8 V ± 0.1 V		Units	Notes
				Min	Max		
1:1 25-bit and 1:2 14-bit and 1:2 28-bit	f_{CK}	Clock Frequency			410	MHz	
	t_W	Pulse duration, CK, $\overline{CK}$ high or low	TBD	1		ns	
	t_{PDM}	Clock to Output Time	Includes 350 ps test-load transmission-line delay	1.2	1.9	ns	2
	t_{PDMSS}	Clock to Output Time (Simultaneous switching)	Includes 350 ps test-load transmission-line delay		2.0	ns	2
	t_{ACT}	Differential inputs active time			10	ns	
	t_{INACT}	Differential inputs inactive time			15	ns	
	t_{SU}	$\overline{DCS}$ and $\overline{CSR}$ signals	Previous $\overline{CSR}$=High	0.7		ns	1
	t_{SU}	All other input signals		0.5		ns	1
	t_H	Hold Time		0.5		ns	1
	$C_{IN(DATA)}$	Data(Except of $\overline{DCS}$ for Dual-die) Input Capacitance		2.5	4.0	pF	
		$\overline{DCS}$ Input Capacitance (for Dual-die)		4.0	6.0	pF	
	$C_{IN(CLOCK)}$	Clock Input Capacitance (for Single-die)		2.0	3.0	pF	
		Clock Input Capacitance (for Dual-die)		4.0	6.0	pF	
	$C_{IN(RST)}$	Reset Input Capacitance		TBD	TBD	pF	

1. All input slew rate = 1 V/ns ± 20 %
2. Load circuit is specified in JESD82-xxx for the SSTUA32866, JESD82-xxx for the SSTUA32S868/SSTUA32D868 and JESD82-xxx for the SSTUA32S865 / SSTUA32D865
3. Some register parameter may vary from one register part number to another register part number. Refer to appropriate register datasheet for exact detailed information.

Critical Register Specifications for PC2-6400

Register	Symbol	Parameter	Conditions	T_A = 0 - 70 °C V_{DD} = 1.8 V ± 0.1 V		Units	Notes
				Min	Max		
1:1 25-bit and 1:2 14-bit and 1:2 28-bit	f_{CK}	Clock Frequency			TBD	MHz	
	t_W	Pulse duration, CK, $\overline{CK}$ high or low	TBD	1		ns	
	t_{PDM}	Clock to Output Time	Includes 350 ps test-load transmission-line delay	1.1	1.5	ns	2
	t_{PDMSS}	Clock to Output Time (Simultaneous switching)	Includes 350 ps test-load transmission-line delay		1.6	ns	2
	t_{ACT}	Differential inputs active time			10	ns	
	t_{INACT}	Differential inputs inactive time			15	ns	
	t_{SU}	$\overline{DCS}$ and $\overline{CSR}$ signals	Previous $\overline{CSR}$=High	0.7		ns	1
	t_{SU}	All other input signals		0.5		ns	1
	t_H	Hold Time		0.5		ns	1
	$C_{IN(DATA)}$	Data Input Capacitance		2.5	3.5	pF	
	$C_{IN(CLOCK)}$	Clock Input Capacitance		2.0	3.0	pF	
	$C_{IN(RST)}$	Reset Input Capacitance		TBD	TBD	pF	

1. All input slew rate = 1 V/ns ± 20 %
2. Load circuit is specified in JESD82-xxx for the SSTUB32866, JESD82-xxx for the SSTUB32868 and JESD82-xxx for the SSTUB32865.
3. Some register parameter may vary from one register part number to another register part number. Refer to appropriate register datasheet for exact detailed information.

Petitioners
Ex. 1066, p. 37

Register Options for Unused Address inputs

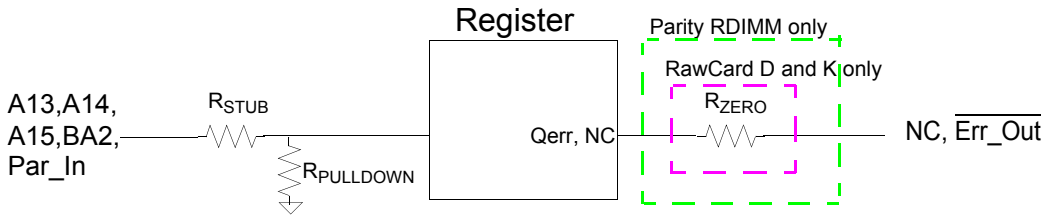
Unused inputs to the register(s) on the DIMM are not allowed to float so resistors on the DIMM are used to guarantee the input logic level to the register(s). The following table describes the resistor options used on the DIMMs (defined in the DIMM bill of material) to assemble both non-parity and parity modules. The section below this (Applicable DIMM Type in Systems) explains where non-parity and parity DIMMs may be used.

Type	Raw Card with Register used	DRAM density	A13		A14		A15		BA2		Par_In	
			Stub resistor	Pull-down resistor	Stub resistor	Pull-down resistor	Stub resistor	Pull-down resistor	Stub resistor	Pull-down resistor	Stub resistor	Pull-down resistor
Non-Parity RDIMM	A, B, C, E, G, H, N with SSTU32864	256 Mb	-[1]	X[2]	-	X	-	X	-	X	-	-
		512 Mb	X	-	-	X	-	X	-	X	-	-
		1 Gb	X	-	-	X	-	X	X	-	-	-
		2 Gb	X	-	X	-	-	X	X	-	-	-
		4 Gb	X	-	X	-	X	-	X	-	-	-
	D [3] with SSTU32865 series[5], K [3], M [3] P [3]with SSTU32868 series[5]	256 Mb	-	X	-	X	-	X	-	X	-	X
		512 Mb	X	-	-	X	-	X	-	X	-	X
		1 Gb	X	-	-	X	-	X	X	-	-	X
		2 Gb	X	-	X	-	-	X	X	-	-	X
		4 Gb	X	-	X	-	X	-	X	-	-	X
Parity RDIMM	D with SSTU32865 series[5], E, G, H, J, N with SSTU32866 series[5], K, M, P with SSTU32868 series[5]	256 Mb	X	X	X	X	X	X	X	X	X	X
		512 Mb	X	-	X	X	X	X	X	X	X	X
		1 Gb	X	-	X	X	X	X	X	-	X	X
		2 Gb	X	-	X	-	X	X	X	-	X	X
		4 Gb	X	-	X	-	X	-	X	-	X	X
	F [4] with SSTU32866 series[5]	256 Mb	X	-	X	X	X	X	X	-	X	X
		512 Mb	X	-	X	X	X	X	X	-	X	X
		1 Gb	X	-	X	X	X	X	X	-	X	X
		2 Gb	X	-	X	-	X	X	X	-	X	X
		4 Gb	X	-	X	-	X	-	X	-	X	X

1 "-" means: resistor not placed
2. "X" means: resistor placed; stub resistor value is 22 ohms .; pulldown resistor value is 100 k ohms.
3. If a non-parity RDIMM with raw card D uses a parity register, then a pull-down must be present on Par_In and the resistor RZERO must not be placed.
4. A Parity DIMM plugged into a non-parity system is O.K. if the system drives A13 and BA2
5. SSTU32865 series means SSTU32865,SSTUA32S865,SSTUA32D865,SSTUB32S865 and SSTUB32D865
SSTU32866 series means SSTU32866,SSTUA32866 and SSTUB32866
SSTU32868 series means SSTU32868,SSTUA32S868,SSTUA32D868,SSTUB32S868 and SSTUB32D868
Applicable Register parts for each speed grade must comply with the table of DIMM Register Use in section of Register Component Specifications

Petitioners
Ex. 1066, p. 38

The unused address pins on non-parity RDIMMs are disabled via resistor options (bill of material option). This is achieved by removing the stub resistor of the respective address lead-in net and tying the register input node to GND via a 100k ohms pulldown resistor. For Parity RDIMMs, all addresses and Par_In have to be driven from the controller to allow for correct parity calculation. In this case, there are no floating inputs to the register.



Applicable DIMM types in Systems

The following table describes the recommended use of non-parity and parity DIMMs in non-parity and parity systems.

DIMM Type	Non - Parity DIMM System	Parity DIMM System
Non-Parity RDIMM	O.K.	O.K.
Parity RDIMM (RC-D,E,G,H,J,K,M,N,P)	O.K.	O.K.
Parity DIMM (RC-F)	Not Allowed [1]	O.K.

1. A Parity DIMM plugged into a non-parity system is O.K. if the system drives A13 and BA2

Register Sourcing

This document is not intended to be an approved vendor list for support chip components. Although it is recommended that all DDR2 SDRAM RDIMM registers meet the specifications documented above, it is up to each DIMM producer to select the registers and register vendors which meet these requirements, and to guarantee robustly designed DIMMs.
The register driver in conjunction with the unterminated postregister nets may cause severe overshoots and undershoots at the DRAM input terminals. The DIMM manufacturer needs to ensure that the guaranteed maximum induced over/undershoot (see register vendor datasheet) does not exceed the max. allowed value for the DRAM inputs (see DRAM vendor datasheet)

Petitioners
Ex. 1066, p. 39

PLL Component Specifications

Please refer to the vendor PLL data sheets for all technical specifications and requirements. Below is a chart explaining which PLLs are used on each DIMM type.

DIMM PLL Use

Raw Card Version	# of Ranks	# of SDRAMs per output	PLL Type	PLL Speed Grade PC2-4200 / PC2-3200	PLL Speed Grade PC2-5300 / PC2-6400	Quantity
A, F	1	1	1:10, 1.8Volt	CU877 / CUA877	CUA877	1
B, G	2	2	1:10, 1.8Volt	CU877 / CUA877	CUA877	1
C, H	1	2	1:10, 1.8Volt	CU877 / CUA877	CUA877	1
D, E, J, K, P	2	4	1:10, 1.8Volt	CU877 / CUA877	CUA877	1
M	4	8	1:10, 1.8Volt	CUA877	-	1
N	4	4	1:10, 1.8Volt	CU877	-	1
1. The reference design uses a PLL in 52-ball FBGA package (MO225 BA)						

The following specifications for the PLL are critical for proper operation of the DDR2 SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the device.

Critical PLL Specifications for PC2-4200/PC2-3200

Device	Symbol	Parameter	Conditions	T_A = 0-70× C V_{DD} = 1.8V ± 0.1V		Units	Notes
				Min	Max		
1:10, 1.8Volt	f_{CK}	Operating clock frequency		125	270	MHz	1
	f_{CK}	Application clock frequency		160	270	MHz	2
	t_{DC}	Input clock duty cycle		40	60	%	
	tL	Stabilization time			15	µs	
	$t_{jit(cc+)}$	Cycle-to-cycle period jitter		0	40	ps	
	tjit(cc-)	Cycle-to-cycle period jitter		0	-40	ps	
	$t_{jit(per)}$	Period jitter		-40	40	ps	
	$t_{jit(hper)}$	Half-period jitter		-75	75	ps	
	ten,tdis	OE to any Y/$\overline{Y}$			8	ns	
	t(f)	Static phase offset		-50	50	ps	
	t(f)dyn	Dynamic phase offset		-50	50	ps	
	tsk(o)	Output clock skew			40	ps	
	C_{IN}	Input Capacitance	VI=VDDQ or GND	2	3	pF	
	slr(i)	OE slew rate		0.5		V/ns	
		Input clock slew rate		1	4	V/ns	
	slr(o)	Output clock slew rate		1.5	3	V/ns	
1. Operating clock frequency indicates a range over which the PLL must be able to lock, but in which other timing parameters are not guaranteed. 2. Application clock frequency indicates a range over which the PLL must meet all timing parameters.							

Petitioners
Ex. 1066, p. 40

Critical PLL Specifications for PC2-6400/PC2-5300

Device	Symbol	Parameter	Conditions	T_A = 0-70× C V_{DD} = 1.8V ± 0.1V		Units	Notes
				Min	Max		
1:10, 1.8Volt	f_{CK}	Operating clock frequency		125	410	MHz	1
	f_{CK}	Application clock frequency		160	410	MHz	2
	t_{DC}	Input clock duty cycle		40	60	%	
	tL	Stabilization time			6	µs	
	$t_{jit(cc+)}$	Cycle-to-cycle period jitter		0	40	ps	
	tjit(cc-)	Cycle-to-cycle period jitter		0	-40	ps	
	$t_{jit(per)}$	Period jitter	fCK:160MHz to 270MHz	-40	40	ps	
			fCK:271MHz to 410MHz	$t_{jit(per)min}$	$t_{jit(per)max}$	ps	
	$t_{jit(hper)}$	Half-period jitter		-50	50	ps	
	ten,tdis	OE to any Y/$\overline{Y}$			8	ns	
	t(ϕ)	Static phase offset		-50	50	ps	
	t(ϕ)dyn	Dynamic phase offset	fCK:160MHz to 270MHz	-50	50	ps	
			fCK:271MHz to 410MHz	t(ϕ)dyn(min)	t(ϕ)dyn(max)	ps	
	tsk(o)	Output clock skew	fCK:160MHz to 270MHz		40	ps	
			fCK:271MHz to 410MHz		tsk(o)max	ps	
	Σt(su)	|tjit(per)|+|t(ϕ)dyn|+tsk(o)	fCK:271MHz to 410MHz		80	ps	
	Σt(h)	|t(ϕ)dyn|+tsk(o)	fCK:271MHz to 410MHz		60	ps	
	C_{IN}	Input Capacitance	VI=VDDQ or GND	2	3	pF	
	slr(i)	OE slew rate		0.5		V/ns	
		Input clock slew rate		1	4	V/ns	
	slr(o)	Output clock slew rate		1.5	3	V/ns	

1. Operating clock frequency indicates a range over which the PLL must be able to lock, but in which other timing parameters are not guaranteed.
2. Application clock frequency indicates a range over which the PLL must meet all timing parameters.

PLL Sourcing

This document is not intended to be an approved vendor list for support chip components. Although it is recommended that all DDR2 SDRAM Registered DIMM PLLs meet the specifications documented above, it is up to each DIMM producer to select the PLL and PLL vendors which meet these requirements, and to guarantee robustly operating DIMMs.

Petitioners
Ex. 1066, p. 41

DDR2 Registered DIMM Details

DDR2 SDRAM Module Configurations (Reference Designs)

Raw Card Version	DIMM		SDRAM		# of SDRAMs	SDRAM Package Type	# of Physical Ranks	# of Banks in SDRAM	# of Address bits row/col/Bank
	Capacity	Organization	Density	Organization					
A,F	256MB	32Mx72	256Mbit	32Mx8	9	60/68 Ball FBGA	1	4	13/10/2
	512MB	64Mx72	512Mbit	64Mx8	9	60/68 Ball FBGA	1	4	14/10/2
	1GB	128Mx72	1Gbit	128Mx8	9	60/68 Ball FBGA	1	8	14/10/3
	2GB	256Mx72	2Gbit	256Mx8	9	60/68 Ball FBGA	1	8	15/10/3
	4GB	512Mx72	4Gbit	512Mx8	9	60/68 Ball FBGA	1	8	16/10/3
B,G	512MB	64Mx72	256Mbit	32Mx8	18	60/68 Ball FBGA	2	4	13/10/2
	1GB	128Mx72	512Mbit	64Mx8	18	60/68 Ball FBGA	2	4	14/10/2
	2GB	256Mx72	1Gbit	128Mx8	18	60/68 Ball FBGA	2	8	14/10/3
	4GB	512Mx72	2Gbit	256Mx8	18	60/68 Ball FBGA	2	8	15/10/3
	8GB	1Gx72	4Gbit	512Mx8	18	60/68 Ball FBGA	2	8	16/10/3
C,H	512MB	64Mx72	256Mbit	64Mx4	18	60/68 Ball FBGA	1	4	13/11/2
	1GB	128Mx72	512Mbit	128Mx4	18	60/68 Ball FBGA	1	4	14/11/2
	2GB	256Mx72	1Gbit	256Mx4	18	60/68 Ball FBGA	1	8	14/11/3
	4GB	512Mx72	2Gbit	512Mx4	18	60/68 Ball FBGA	1	8	15/11/3
	8GB	1Gx72	4Gbit	1Gbx4	18	60/68 Ball FBGA	1	8	16/11/3
D,E, K,P	1GB	64Mx72	256Mbit	64Mx4	36	63/71 Ball stacked FBGA	2	4	13/11/2
	2GB	128Mx72	512Mbit	128Mx4	36	63/71 Ball stacked FBGA	2	4	14/11/2
	4GB	256Mx72	1Gbit	256Mx4	36	63/71 Ball stacked FBGA	2	8	14/11/3
	8GB	512Mx72	2Gbit	512Mx4	36	63/71 Ball stacked FBGA	2	8	15/11/3
	16GB	1Gx72	4Gbit	1Gbx4	36	63/71 Ball stacked FBGA	2	8	16/11/3
J	1GB	64Mx72	256Mbit	64Mx4	36	60 Ball FBGA	2	4	13/11/2
	2GB	128Mx72	512Mbit	128Mx4	36	60 Ball FBGA	2	4	14/11/2
	4GB	256Mx72	1Gbit	256Mx4	36	60 Ball FBGA	2	8	14/11/3
	8GB	512Mx72	2Gbit	512Mx4	36	60 Ball FBGA	2	8	15/11/3
	16GB	1Gx72	4Gbit	1Gbx4	36	60 Ball FBGA	2	8	16/11/3
M	2 GB	256Mx72	256 Mbit	64Mx4	72	63 Ball stacked FBGA	4	4	13/11/2
	4 GB	512Mx72	512 Mbit	128Mx4	72	63 Ball stacked FBGA	4	4	14/11/2
	8 GB	1Gx72	1 Gbit	256Mx4	72	63 Ball stacked FBGA	4	8	14/11/3
	16 GB	2Gx72	2 Gbit	512Mx4	72	63 Ball stacked FBGA	4	8	15/11/3
	32 GB	4Gx72	4 Gbit	1Gbx4	72	63 Ball stacked FBGA	4	8	16/11/3
N	1GB	128Mx72	256Mbit	32Mx8	36	60 Ball FBGA	4	4	13/10/2
	2GB	256Mx72	512Mbit	64Mx8	36	60 Ball FBGA	4	4	14/10/2
	4GB	512Mx72	1Gbit	128Mx8	36	60 Ball FBGA	4	8	14/10/3
	8GB	1Gx72	2Gbit	256Mx8	36	60 Ball FBGA	4	8	15/10/3
	16GB	2Gx72	4Gbit	512Mx8	36	60 Ball FBGA	4	8	16/10/3

Example:RC C has 2G bytes.

8 bytes (2^3) x 1 Rank (2^0) x 14 rows (A0 - A13:2^{14}) x 11 columns (A0 - A9, A11:2^{11}) x 8 banks (BA0 - BA2: 2^3)

= $2^{31(=3+0+14+11+3)}$ bytes = 2G bytes

Petitioners
Ex. 1066, p. 42

Input Loading Matrix

Signal Names	Input Device	Raw Card Version												
		A	B	C	D	E	F	G	H	J	K	M	N	P
CK0, $\overline{CK0}$	PLL	1	1	1	1	1	1	1	1	1	1	1	1	1
$\overline{RESET}$	PLL + Register	1 + 1	1 + 2	1 + 2	1 + 2	1 + 4	1 + 1	1 + 2	1 + 2	1 + 4	1 + 2	1 + 2	1 + 4	1 + 2
CKE0, ODT0	Register	1	1	1	2	1	1	1	1	1	2	1	2	2
CKE1, ODT1	Register	N/A	1	N/A	2	1	N/A	1	N/A	1	2	1	2	2
Addr, BA, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Register	1	1	1	2	2	1	1	1	2	2	2	2	2
$\overline{S}0$	Register	1	2	2	2	4	1	2	2	4	2	1	2	2
$\overline{S}1$	Register	N/A	2	N/A	2	4	N/A	2	N/A	4	2	1	2	2
$\overline{S}2$	Register	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1	2	N/A
$\overline{S}3$	Register	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1	2	N/A
DQ, CB, DQS, $\overline{DQS}$	DDR SDRAM	1	2	1	2	2	1	2	1	2	2	4	4	2
DM, RDQS, $\overline{RDQS}$	DDR SDRAM	1	2	N/A	N/A	N/A	1	2	N/A	N/A	N/A	N/A	4	N/A
SCL,SDA,SA	EEPROM	1	1	1	1	1	1	1	1	1	1	1	1	1
Par_In	Register	N/A	N/A	N/A	2	2	1	1	1	2	2	2	2	2

DDR2 Registered DIMM Design File Releases

‘Reference’ Design file updates will be released as needed. This Registered DIMM specification will reflect the most recent Design files, but may also be updated to reflect clarifications to the specification only; in these cases the Design files will not be updated. The following table outlines the most recent Design file releases.

Raw Card Version	Specfica-tion Revision	Applicable Design File	Applicable BOM	Notes
A0	1.10	PC2-4200_RDIMM_V100_RC_A0_20040109.brd	PC2-4200_RDIMM_V100_RC_A0_20040109_Bom	Non-parity DIMM mod-ules.
B0	0.56	PC2-4200_RDIMM_V056_RC_B0_20030708.brd	PC2-4200_RDIMM_V056_RC_B0_20030708_Bom	
B1	1.10	PC2-4200_RDIMM_V100_RC_B1_20040109.brd	PC2-4200_RDIMM_V100_RC_B1_20040109_Bom	
C0	1.10	PC2-4200_RDIMM_V100_RC_C0_20030710.brd	PC2-4200_RDIMM_V100_RC_C0_20030710_Bom	
D0	1.10	PC2-4200_RDIMM_V100_RC_D0_20040202.brd	PC2-4200_RDIMM_V110_RC_D0_20040902_Bom	Non-parity DIMM mod-ules using raw cards designed for parity. This is further explained on page 38 under Register Options for Unused Inputs.
E0	1.10	PC2-4200_RDIMM_V100_RC_E0_20040205.brd	PC2-4200_RDIMM_V100_RC_E0_20040205_Bom	
G0	1.10	PC2-4200_RDIMM_V101_RC_G0_20040406.brd	PC2-4200_RDIMM_V101_RC_G0_20040531_Bom	
H0	1.10	PC2-4200_RDIMM_V101_RC_H0_20040205.brd	PC2-4200_RDIMM_V101_RC_H0_20040126_Bom	
J1	2.10	PC2-4200_RDIMM_V210_RC_J1_20041014.brd	PC2-4200_RDIMM_V101_RC_J1_20050303_Bom	
K0	1.10	PC2-4200_RDIMM_V101_RC_K0_20040402.brd	PC2-4200_RDIMM_V101_RC_K0_20040402_Bom	
N0	2.10	PC2-4200_RDIMM_V210_RC_N0_20050110.brd	PC2-4200_RDIMM_V210_RC_N0_20050110_Bom	
P0	3.10	PC2-5300_RDIMM_V310_RC_P0_20050221.brd	PC2-5300_RDIMM_V310_RC_P0_20050221_Bom	
D0	1.10	PC2-4200_RDIMM_V100_RC_D0_20040202.brd	PC2-4200_RPDIMM_V110_RC_D0_20041007_Bom	Parity DIMM module.
E0	1.10	PC2-4200_RDIMM_V100_RC_E0_20040205.brd	PC2-4200_RPDIMM_V100_RC_E0_20040205_Bom	
F0	1.10	PC2-4200_RDIMM_V101_RC_F0_20040211.brd	PC2-4200_RPDIMM_V101_RC_F0_20040211_Bom	
G0	1.10	PC2-4200_RDIMM_V101_RC_G0_20040406.brd	PC2-4200_RPDIMM_V101_RC_G0_20040406_Bom	
H0	1.10	PC2-4200_RDIMM_V101_RC_H0_20040205.brd	PC2-4200_RPDIMM_V101_RC_H0_20040126_Bom	
J1	2.10	PC2-4200_RDIMM_V210_RC_J1_20041014.brd	PC2-4200_RPDIMM_V101_RC_J1_20050303_Bom	
K0	1.10	PC2-4200_RDIMM_V101_RC_K0_20040402.brd	PC2-4200_RPDIMM_V101_RC_K0_20040402_Bom	
N0	2.10	PC2-4200_RDIMM_V210_RC_N0_20050110.brd	PC2-4200_RPDIMM_V210_RC_N0_20050110_Bom	
P0	3.10	PC2-5300_RDIMM_V310_RC_P0_20050221.brd	PC2-5300_RPDIMM_V310_RC_P0_20050221_Bom	
R/C-B1:Optional resistors for A13,A14,A15,BA2 were added on R/C-B0 R/C-J1: Non-Parity DIMM has not been authorized yet.				

Petitioners
Ex. 1066, p. 43

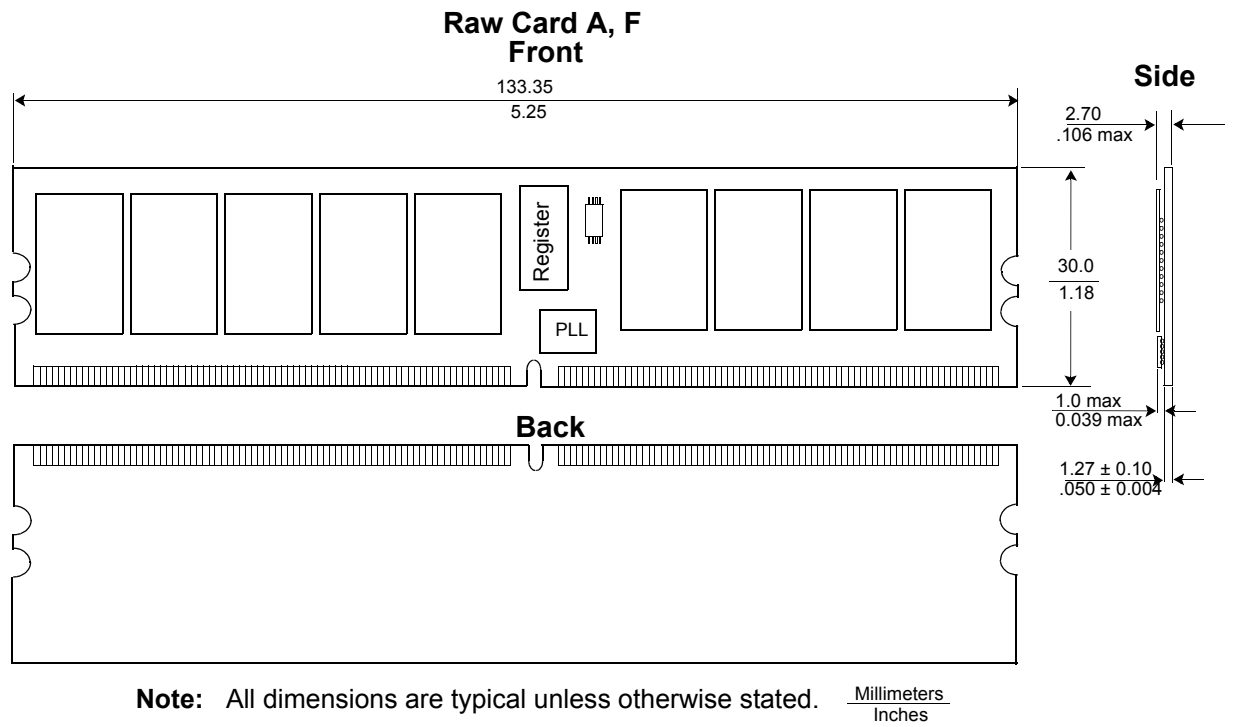
Component Types and Placement

Components shall be surface mounted on one or both sides of the PCB and positioned on the PCB to meet the minimum and maximum trace lengths required for DDR2 SDRAM signals. Bypass capacitors for DDR SDRAM devices must be located near the device power pins. PCB has x16/x8/x4 common footprint (only x8,x4 are wired).

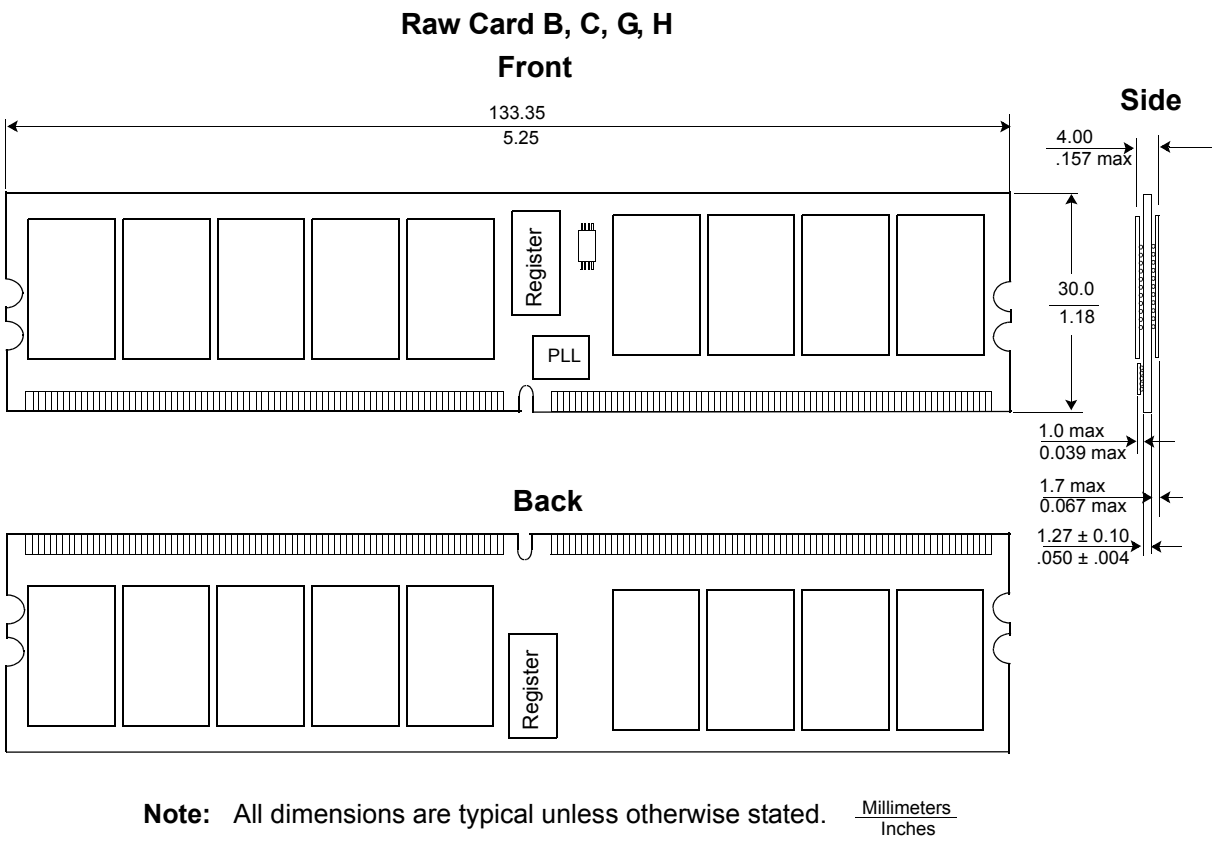
The following layouts suggest placement for the Raw Cards. Exact spacing is not provided, but should be based on manufacturing constraints and signal routing constraints imposed by this design guide. The minimun center-to-center spacing of DRAMs is 12.8 mm and the height of the DRAM outline is 21.9 mm for raw cards A, B and C reference designs.

These examples and dimensions are for reference only. Dimensions are controlled by JC-11 document MO-237.

Example Component Placement

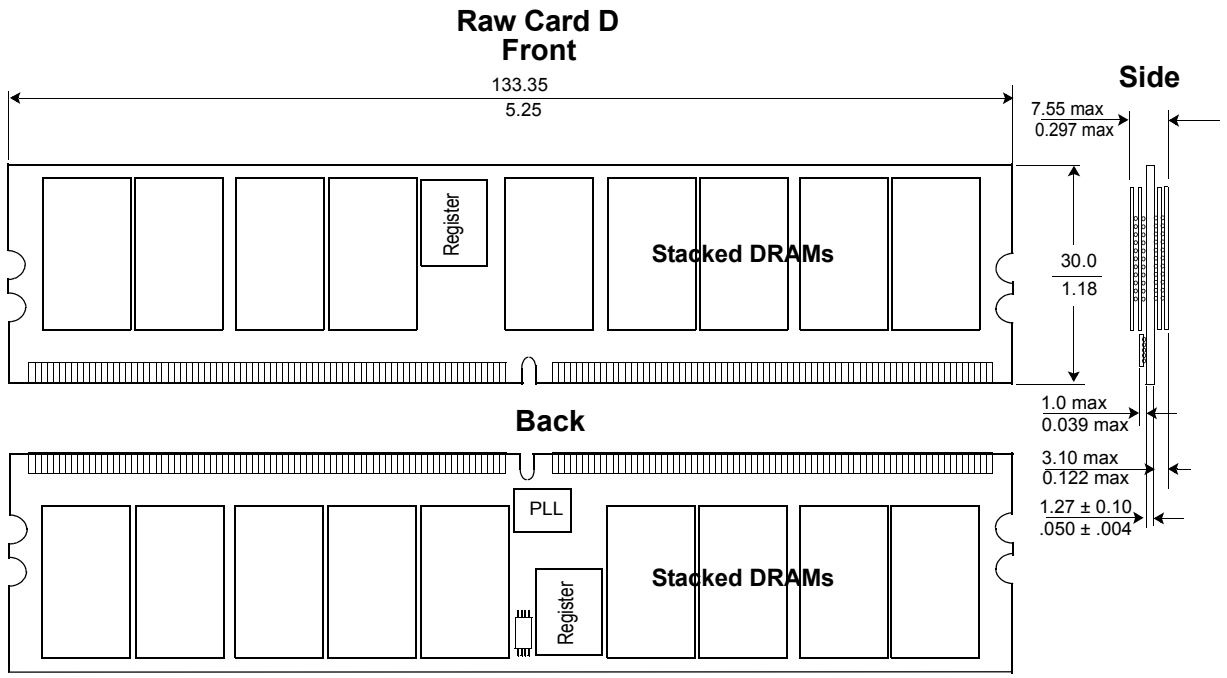


Petitioners
Ex. 1066, p. 44

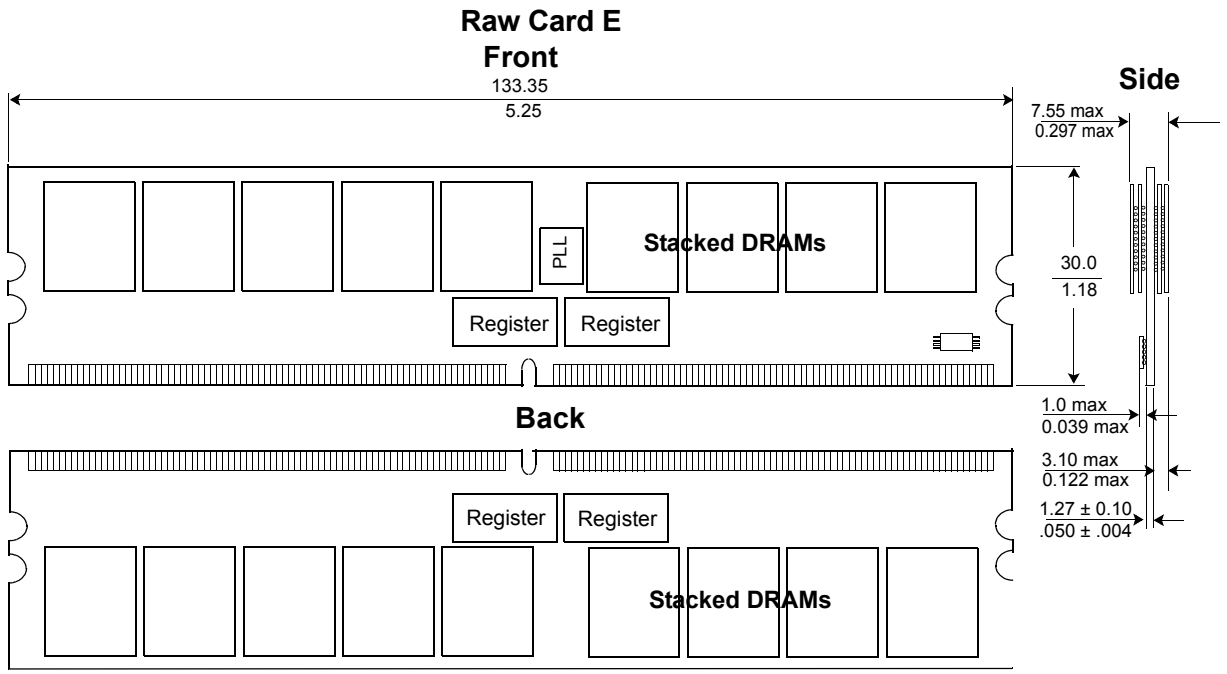


Note: All dimensions are typical unless otherwise stated. Millimeters / Inches

Petitioners
Ex. 1066, p. 45

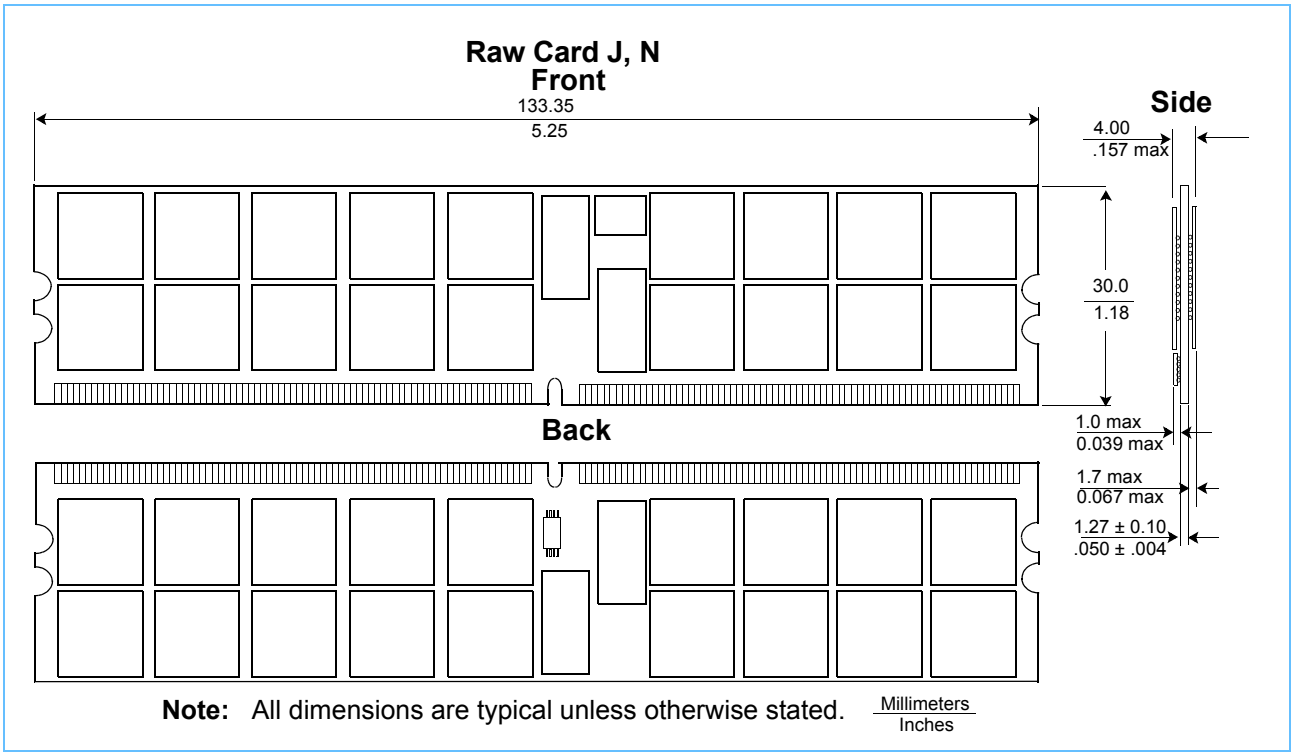


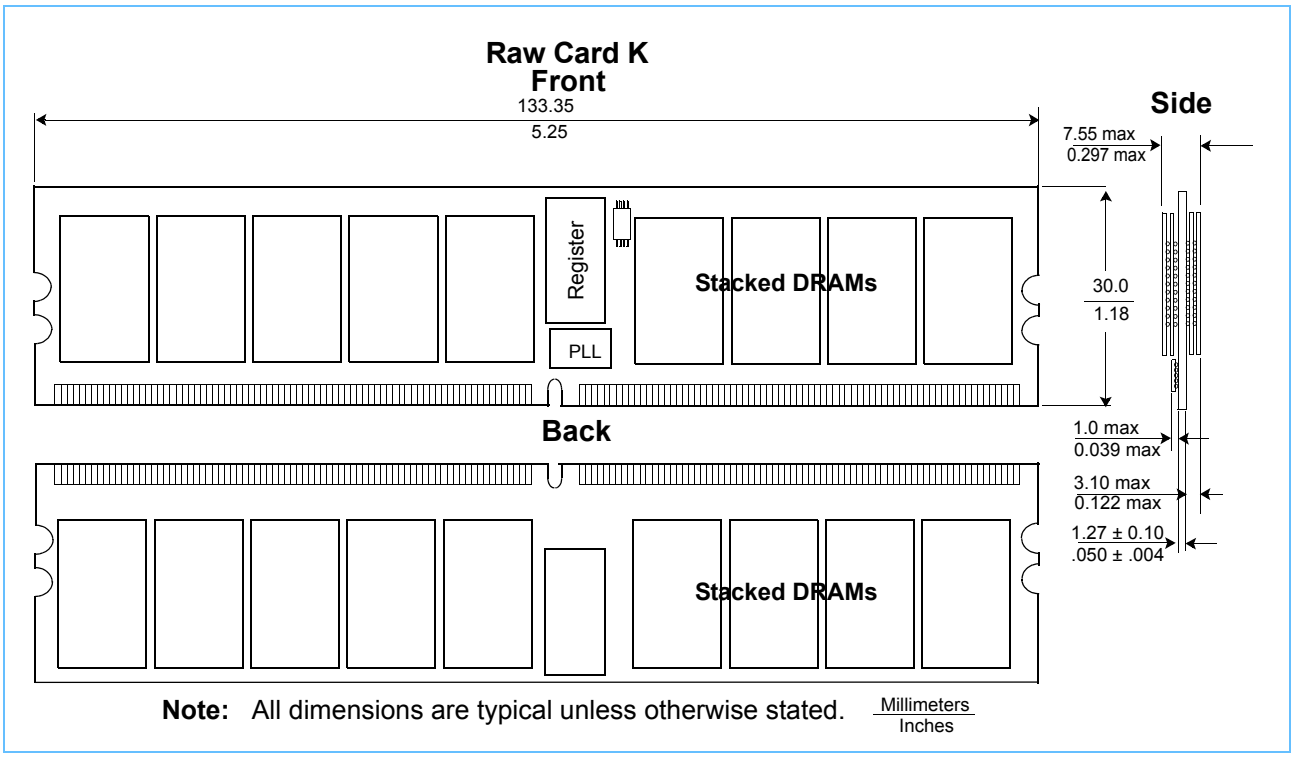
Note: All dimensions are typical unless otherwise stated. Millimeters / Inches



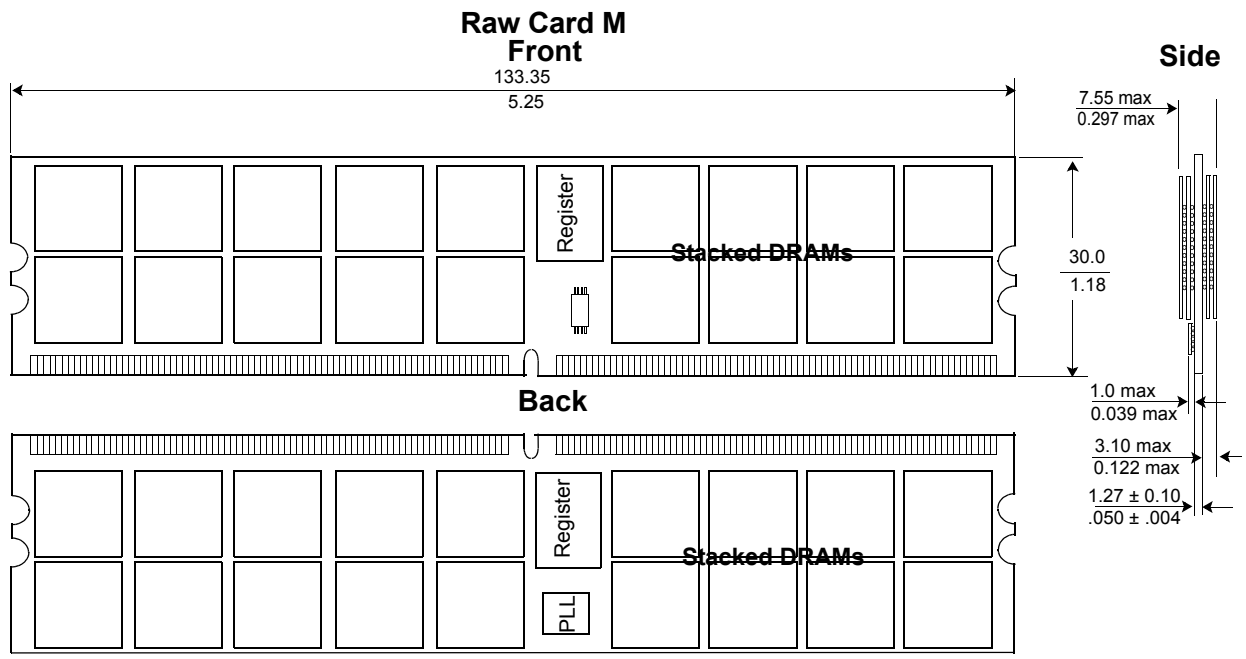
Note: All dimensions are typical unless otherwise stated. Millimeters / Inches

Petitioners
Ex. 1066, p. 46

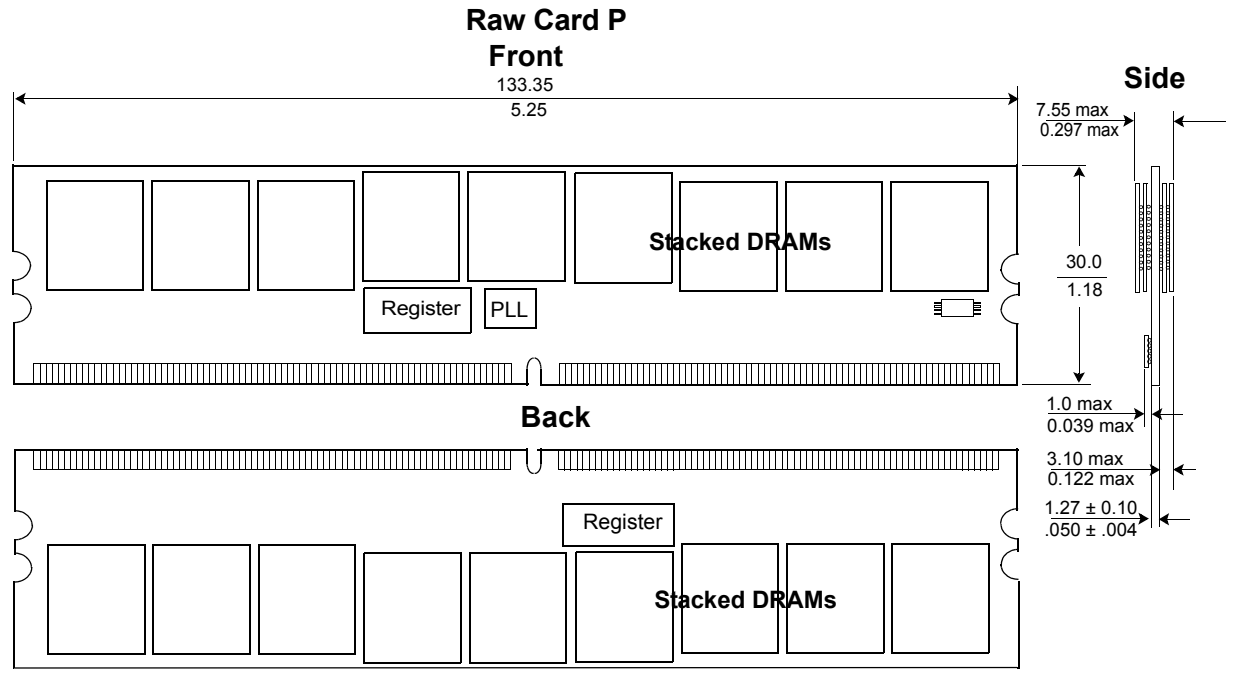




Petitioners
Ex. 1066, p. 47



Note: All dimensions are typical unless otherwise stated. Millimeters / Inches



Note: All dimensions are typical unless otherwise stated. Millimeters / Inches

Petitioners
Ex. 1066, p. 48

DDR2 Registered DIMM Wiring Details

Signal Groups

This specification categorizes DDR SDRAM timing-critical signals into four groups. The following table summarizes the signals contained in each group.

Signal Group	Signals In Group	Raw Card Version	Page
PLL Input / Unused Clocks	CK, $\overline{CK}$	A, B, C, D, E, F, G, H, J, K, N, P	54
PLL Output	FBKOUT,$\overline{FBKOUT}$,PCK[9:0]	A, B, C, D, E, F, G, H, J, K, N, P	55-61
Data, DQS, $\overline{DQS}$, DM	DQ[63:0],CB[7:0],DQS[8:0],$\overline{DQS}$[8:0], DM[8:0]/RDQS[17:9],$\overline{RDQS}$[17:9]	A, B, C, D, E, F, G, H, J, K, N, P	62-64
Address and Control Chip Select, Clock Enable, ODT	A[15:0], BA[2:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ $\overline{S}$[3:0], CKE[1:0], ODT[1:0]	A, B, C, D, E, F, G, H, J, K, N, P	65-83
Address and Command Parity	Par_In, $\overline{Err_Out}$	D, E, F, G, H, J, K, N, P	85

General Net Structure Routing Guidelines

Net structures and lengths must satisfy signal quality and setup/hold time requirements for the memory interface. Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace length table that lists the minimum and maximum allowable lengths for each trace segment and/or net.

The general routing requirements are as follows

- Route all signal traces except clocks using 0.1/0.1 rules, i.e., 0.1 mm traces and 0.1 mm minimum spacing between adjacent traces.But spacing should be as wide as possible to prevent crosstalk.
- Route clocks using 0.1 mm lines and 0.1 mm spaces between differential clock pairs and differential DQS,$\overline{DQS}$.
- Route clocks using at least 90% of the total trace length in the inner layers.
- Signals are referenced to Vss or Vdd on adjacent layers. Data signals (DQ,DQS, $\overline{DQS}$,and DM) are referenced to Vss. Address and Command signals are referenced to VDD.

Signal referencing information

Signal groups	Referencing
DQ/DQS pair /DM	Ground layer
Clock nets	Ground layer

Signal groups	Referencing
Pre-register address and command net	Vdd shape
Post-register address and command net	Ground layer

- Test points are required and are provided on the reference designs for the following signal groups:

Test Points

Test points are provided on the DIMMs for probing purposes where signals can not be probed using existing vias or components. These test points vary by DIMM design. Most signals can be probed on the back side of a single-sided DIMM (R/C A and F) using the existing vias. Test points were added on the double-sided DIMMs (R/C B, C, D, E, G, H, J, K and N) to measure signals closer to the DRAMs. Probing can also be done directly on the DRAM pads on the double-sided/double-rank DIMM (R/C B and G) by removing a DRAM and operating the DIMM as a single-rank DIMM (also add a capacitor to emulate the missing DRAM load). The test point signals are summarized in the table below and are documented in the schematics as well as in an assembly drawing showing the location of the test points.

Petitioners
Ex. 1066, p. 49

Test Points

Signal Group	Signal Location	Raw Card A, F	Raw Card B, G	Raw Card C, H
Address /Command	Pre register	All signal: A[15:0], BA[2:0], $\overline{S}$0, CKE0, $\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$, ODT0 (at vias on back side)	A[0,4,10],BA[0,1], S0,$\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$, ODT0	A[0, 7:4, 11:9, 13], BA[0, 1], S0,$\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$,CKE0, ODT0
	Post register		A[0,1,3,4,10], BA0, $\overline{S}$0, CKE0, ODT0	
DQ,CB		DQ[0,1,2,3,8,9,10,11,16,17,18, 19,32,33,34,35,40,41,42,43,48, 49,50,51,56,57,58,59], CB[0,1]	DQ[0,2,3,6,7,8,9,11,15,16,17,19, 23,24,25,27,28,29,34,35,38,39,40, 44,46,48,51,55,56,57,59,60,61,63], CB[0,1], Others*	DQ[0,1,2*,3,6,7,8,9,11,12,15,16,17, 19,20,23,24,25,28,29,34*,35,39,40, 43,44,47,48,51,52,53,55,56,58*,59, 60,61,63*], CB[0,1,4,5]
DQS ,$\overline{DQS}$		DQS,$\overline{DQS}$[8:0] (at vias on back side)	DQS,$\overline{DQS}$[3,4] , Others*	DQS,$\overline{DQS}$[0*,2,3,4*,7,8,9*,12,13*, 16*,17]
DM		DM[8:0] (at vias on back side)	DM[3,8], Others*	-
Clock	Pre PLL	CK0,$\overline{CK}$0 (at vias on back side)	CK0,$\overline{CK}$0 (at vias on opposite side)	
	Post PLL (at SDRAMs, at Register)	CK0,$\overline{CK}$0 (at vias on back side)	CK0,$\overline{CK}$0 (at term. resistors on clock inputs of registers and SDRAMs)	
Notes: * Need to remove SDRAM to probe				

Signal Group	Signal Location	Raw Card D	Raw Card E
Address /Command	Pre register	A[15:0],BA[2:0],$\overline{S}$[1:0],ODT[1:0],CKE[1:0], $\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$,CKE[1:0] ,Par_In (at stub resistor)	A1,A3,A14,A15,$\overline{S}$0,$\overline{S}$1,ODT0,ODT1,CKE0, CKE1
	Post register	$\overline{S}$[1:0],ODT[1:0],CKE[1:0], Err_out,	A[0,7,15],$\overline{S}$1,CAS, ODT1
DQ,CB		DQ[63:0],CB[7:0] (at stub resistor)	DQ[2,3,7*,8,12,13,17:15,19,20,21,24,25,28, 29,34,35,38,39,42,43,48:46,52:50,56:54,60, 63*], CB[0,1,4,5]
DQS ,$\overline{DQS}$		DQS,$\overline{DQS}$[17:0](at stub resistor)	DQS,$\overline{DQS}$[0*,4:2, 7*,8,9*,12,13,16*,17]
DM		-	
Clock	Pre PLL	CK0,$\overline{CK}$0 (at term. resistor)	CK0,$\overline{CK}$0 (at vias on opposite side)
	Post PLL (at SDRAMs, at Register)	CK0,$\overline{CK}$0 (at term. resistors on clock inputs of registers and SDRAMs)	
Notes: * Need to remove SDRAM to probe			

Petitioners
Ex. 1066, p. 50

Signal Group	Signal Location	Raw Card J	Raw Card K
Address /Command	Pre register	A[1,2,5,6],BA[1:0], RAS,CAS,WE,S[1:0]CKE0	A[1,2,5,6],BA[1:0], RAS,CAS,WE,S[1:0]CKE0
	Post register	A[0,3,7,10,15],BA2,$\overline{S}$1,CAS, ODT0,CKE1	A[0,3,7,10,15],BA2,$\overline{S}$1,CAS, ODT0,CKE1
DQ,CB		DQ[0,1,3,4,5,11,12,15,16,17,20,21,24,25,285,29,34,35,38,39,43,47,48,51,52,56,59,60,61,63], CB[1,4,5]	DQ[0,1,3,4,5,11,12,15,16,17,20,21,24,25,285,29,34,35,38,39,43,47,48,51,52,56,59,60,61,63], CB[1,4,5]
DQS ,$\overline{DQS}$		DQS,$\overline{DQS}$[3,8,12,17]	DQS,$\overline{DQS}$[3,8,12,17]
DM		-	
Clock	Pre PLL	CK0,$\overline{CK}$0 (at term. resistor)	CK0,$\overline{CK}$0 (at vias on opposite side)
	Post PLL (at SDRAMs, at Register)	CK0,$\overline{CK}$0 (at term. resistors on clock inputs of registers and SDRAMs)	
Notes: * Need to remove SDRAM to probe			

Signal Group	Signal Location	Raw Card M	Raw Card N
Address /Command	Pre register	-	A[1,2,5,6],BA[1:0], RAS,CAS,WE,S[1:0]CKE0
	Post register	-	A[3,4,7,12],$\overline{S}$2,CAS, ODT1,CKE1
DQ,CB		-	DQ[0,1,3,4,5,11,12,15,16,17,20,21,24,25,285,29,34,35,38,39,43,47,48,51,52,56,59,60,61,63], CB[1,4,5]
DQS ,$\overline{DQS}$		-	DQS,$\overline{DQS}$[3,7]
DM		-	DM[2,7]
Clock	Pre PLL	-	CK0,$\overline{CK}$0 (at term. resistor)
	Post PLL (at SDRAMs, at Register)	CK0,$\overline{CK}$0 (at term. resistors on clock inputs of registers and SDRAMs)	
Notes: * Need to remove SDRAM to probe			

Petitioners
Ex. 1066, p. 51

Signal Group	Signal Location	Raw Card P	
Address /Command	Pre register	All signals	
	Post register	A[7, 15],CAS,$\overline{S}$1,ODT1	
DQ,CB		-	
DQS ,$\overline{DQS}$		-	
DM		-	
Clock	Pre PLL	CK0,$\overline{CK}$0 (at term. resistor)	
	Post PLL (at SDRAMs, at Register)	CK0,$\overline{CK}$0 at via on opposite side of the registers. CK0,$\overline{CK}$0 at term. resistors on clock inputs of SDRAMs	
Notes: * Need to remove SDRAM to probe			

Petitioners
Ex. 1066, p. 52

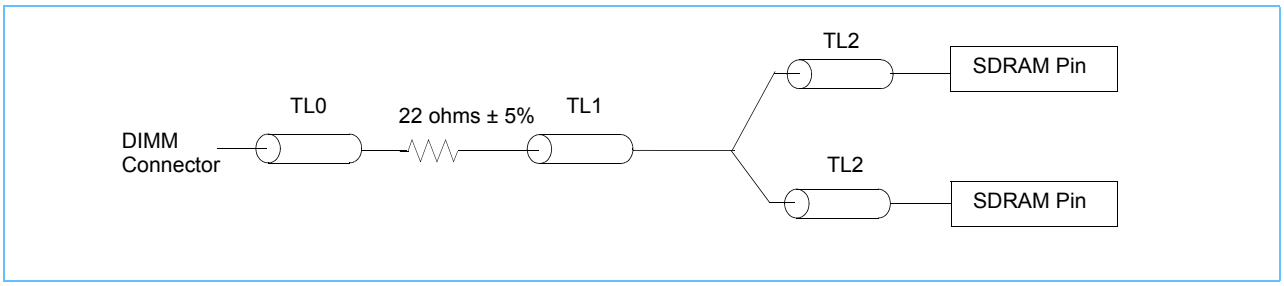
Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for registered DIMM designs. The diagrams should be used to determine individual signal wiring on a DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify DIMM functionality, a full simulation of all signal integrity and timing is required. **The given net structures and trace lengths are not inclusive for all solutions.**

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one SDRAM input. **It is highly recommended that the net structure routing data in this document be simulated by the user.**

Net Structure Example

A 1 GB double-sided x72 DIMM using 512 Mbit, 64Mx8 SDRAM devices would have a data net structure as shown in the following diagram.



Petitioners
Ex. 1066, p. 53

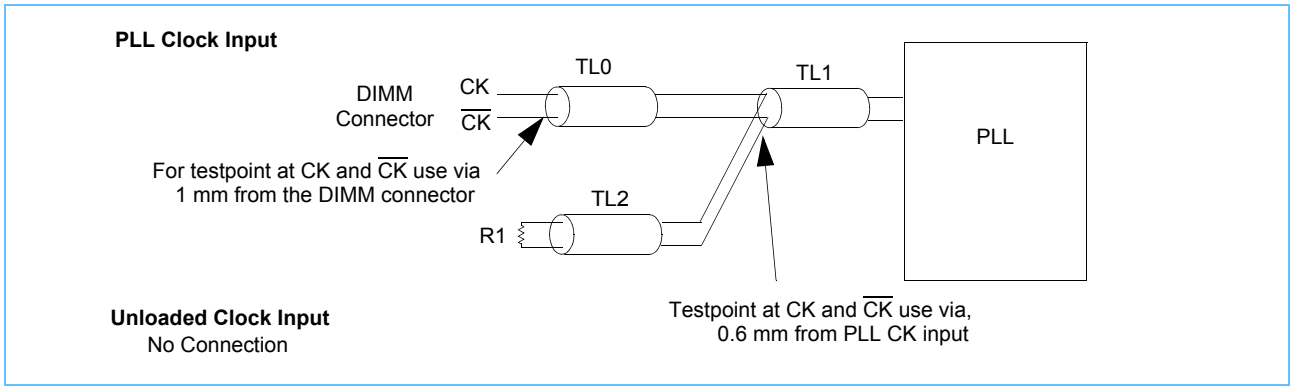
Differential Clock Net Structures

CK, $\overline{CK}$

DDR2 SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality
- Rise/Fall time
- Cross point of the differential pair into the SDRAM and register
- JEDEC-compatible reference delays
- Minimal segment length differences (less than 2.54mm total) between clocks of the same function
- PLL input net segment length is newly defined and optimized for high speed DDR2 Registered DIMMs.

Net Structure Routing for PLL Input



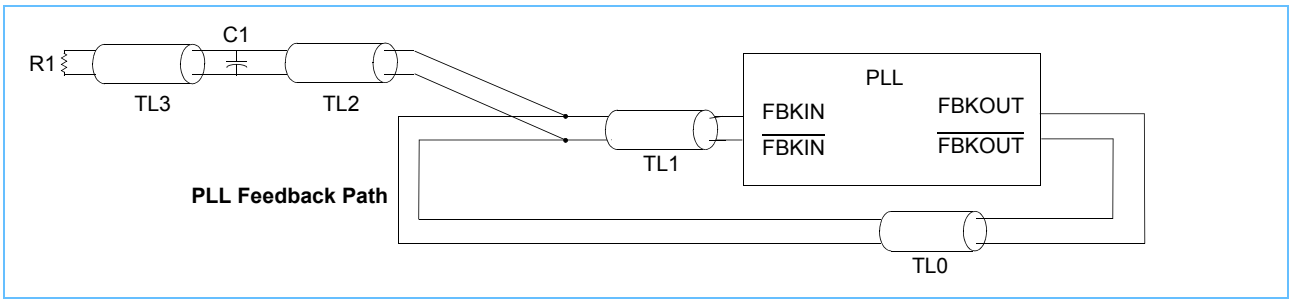
Clock Net Lengths for PLL Input Net Structures

Raw Card	TL0	TL1	TL2	R1 (Ohms)	Notes
A, F	24.8	0.6	1.4	120 ± 5%	1, 2
B, G	24.8	0.6	1.4	120 ± 5%	1, 2
C, H	24.8	0.6	1.4	120 ± 5%	1, 2
D	24.8	0.6	1.4	120 ± 5%	1, 2
E	24.8	0.6	0.8	120 ± 5%	1, 2
J	24.8	0.6	1.3	120 ± 5%	1, 2
K	24.8	0.6	1.1	120 ± 5%	1, 2
N	27.0	0.6	1.1	120 ± 5%	1, 2
P	24.7	0.7	1.0	120 ± 5%	1, 2

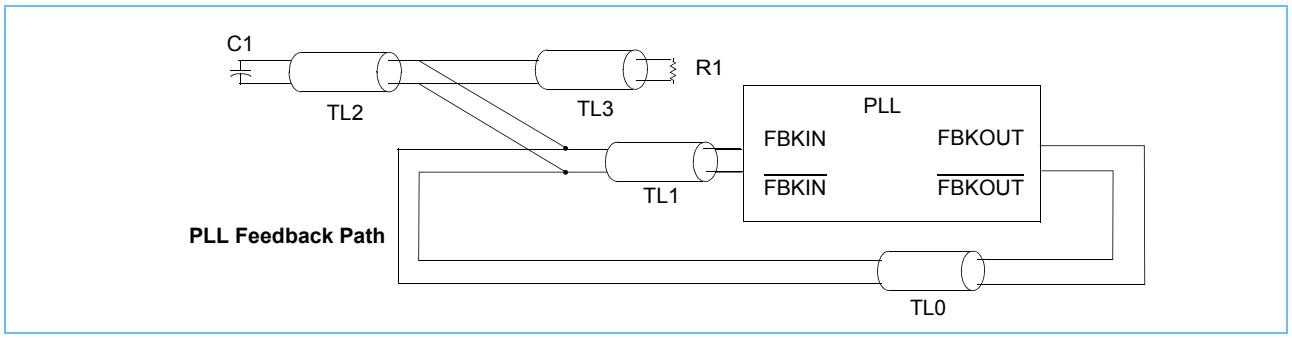
1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.
2. TL0 + TL1 = 25.4 mm

Petitioners
Ex. 1066, p. 54

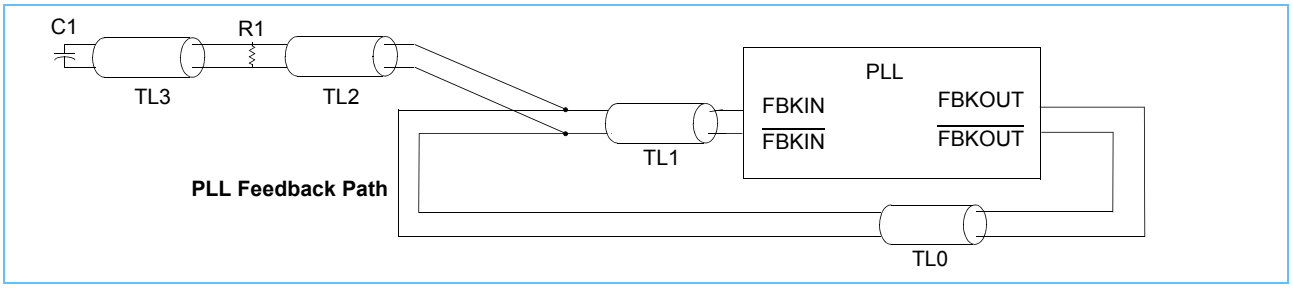
Net Structure Routing for PLL Feedback Path (Raw Card A, F)



Net Structure Routing for PLL Feedback Path (Raw Cards B, C ,D, G, H, J, K, N)



Net Structure Routing for PLL Feedback Path (Raw Card E, P)



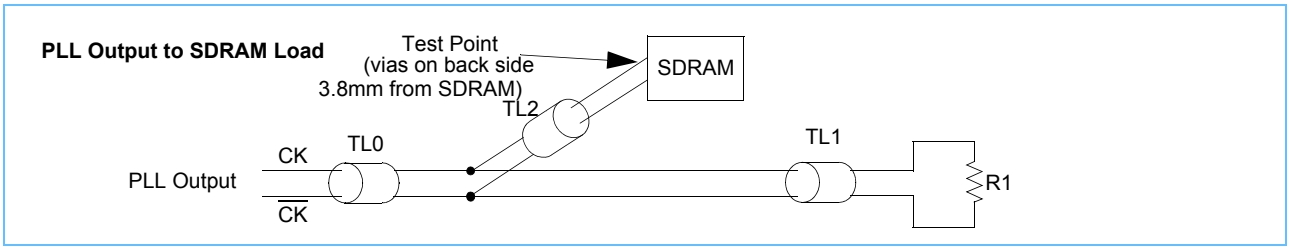
Trace Lengths for PLL Feedback Path Net Structure

Raw Card	TL0		TL1	TL2	TL3	R1 (Ohms)	C1 [pF]	Notes
	Min	Max						
A, F	57.1	57.3	0.5	0.6	1.0	120 ± 5%	TBD	1, 2, 3
B, G	57.1	57.3	0.9	0.6	0.9	120 ± 5%	TBD	1, 2, 3
C, H	50.0	50.1	0.6	0.8	0.8	120 ± 5%	TBD	1, 2, 3
D	76.6	76.7	7.6	0.8	0.8	120 ± 5%	TBD	1, 2, 3
E	69.4	69.5	1.2	0.7	0.9	120 ± 5%	TBD	1, 2, 3
J, N	63.3	63.4	0.8	1.0	1.3	120 ± 5%	TBD	1, 2, 3
K	70.0	70.1	0.6	0.8	0.8	120 ± 5%	TBD	1, 2, 3
P	70.0	70.1	1.0	0.8	0.9	120 ± 5%	TBD	1, 2, 3

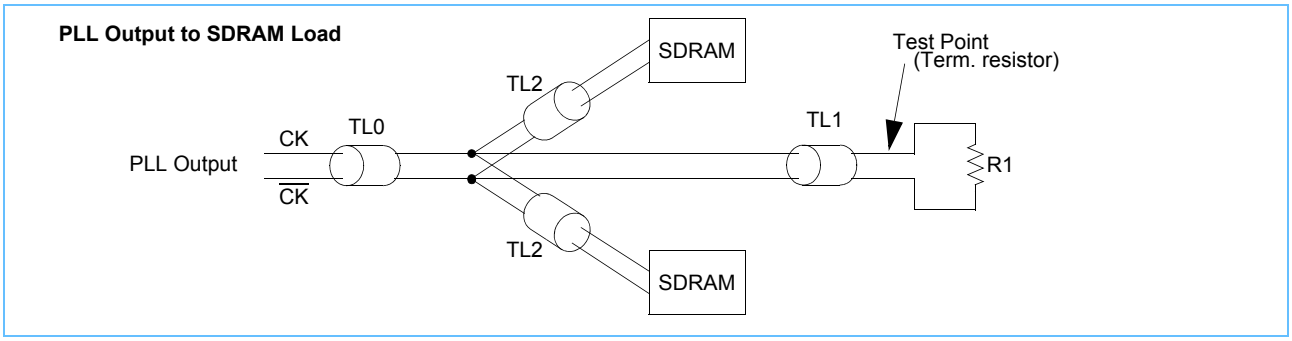
1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.
2. All capacitances are given in pF and must be kept within a tolerance of ± TBD%.
3. The termination resistor and loading capacitor are both placed as close to the pin of the PLL as possible.

Petitioners
Ex. 1066, p. 55

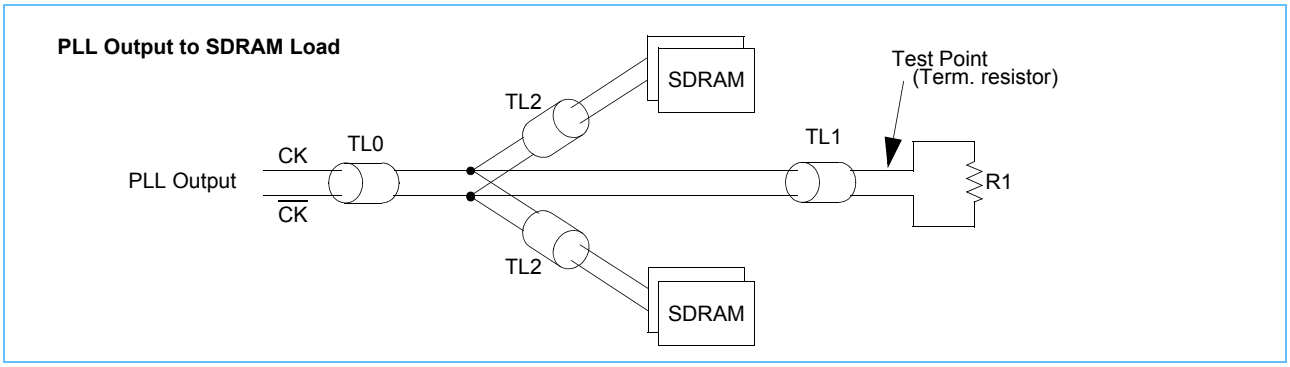
Net Structure Routing for PLL Output to SDRAM Load (Raw Card A, F)



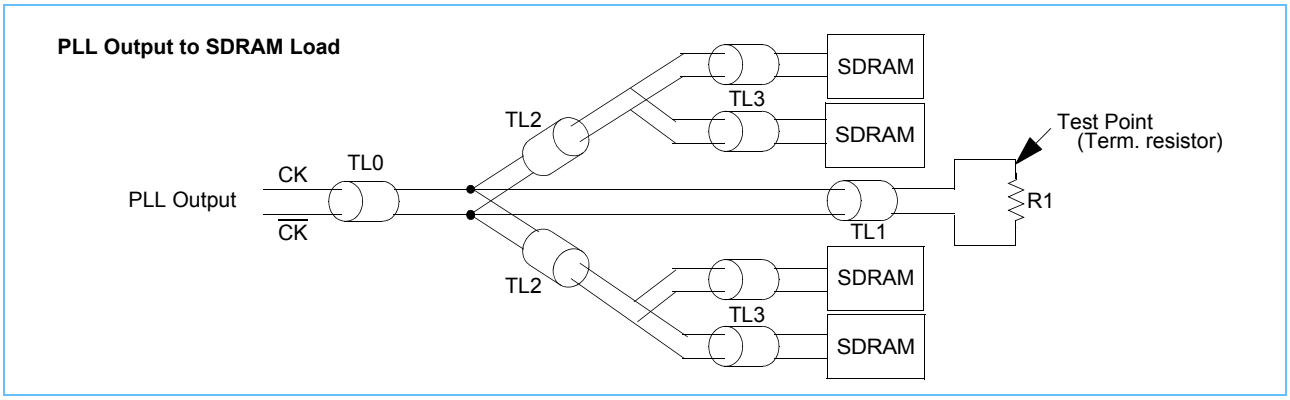
Net Structure Routing for PLL Output to SDRAM Load (Raw Cards B, C, G, H)



Net Structure Routing for PLL Output to SDRAM Load (Raw Cards D, E, K, P)



Net Structure Routing for PLL Output to SDRAM Load (Raw Card J, N)



Petitioners
Ex. 1066, p. 56

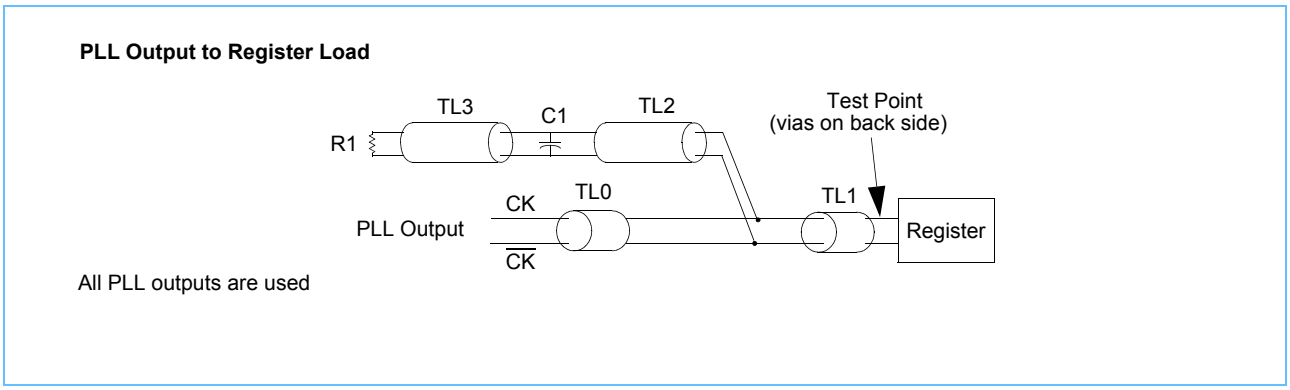
Trace Lengths for PLL Clock Output to SDRAM Load Net Structure

Raw Card	TL0		TL1		TL2		TL3		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max		
A, F	68.5	68.6	15.0	15.1	3.8	3.9	-	-	120 ± 5%	1, 2
B, G	68.1	68.2	15.3	15.4	4.2	4.3	-	-	120 ± 5%	1, 2
C, H	68.5	68.6	16.5	16.6	3.8	3.9	-	-	120 ± 5%	1, 2
D	69.1	69.2	10.4	10.5	4.5	4.6	-	-	120 ± 5%	1, 2, 3
			9.5	9.6	10.0	10.1	-	-		1, 2, 4
E	68.5	68.6	15.0	15.1	6.6	6.7	-	-	120 ± 5%	1, 2
J	70.0	71.0	3.5	3.6	12.8	12.9	4.1	4.2	120 ± 5%	1, 2
K	68.5	68.6	15.0	15.1	4.8	4.9	-	-	120 ± 5%	1, 2
N	70	70.1	3.5	3.6	12.8	12.9	4.0	4.1	120 ± 5%	1, 2
P	68.5	68.6	15.0	15.1	6.6	6.7	-	-	120 ± 5%	1, 2

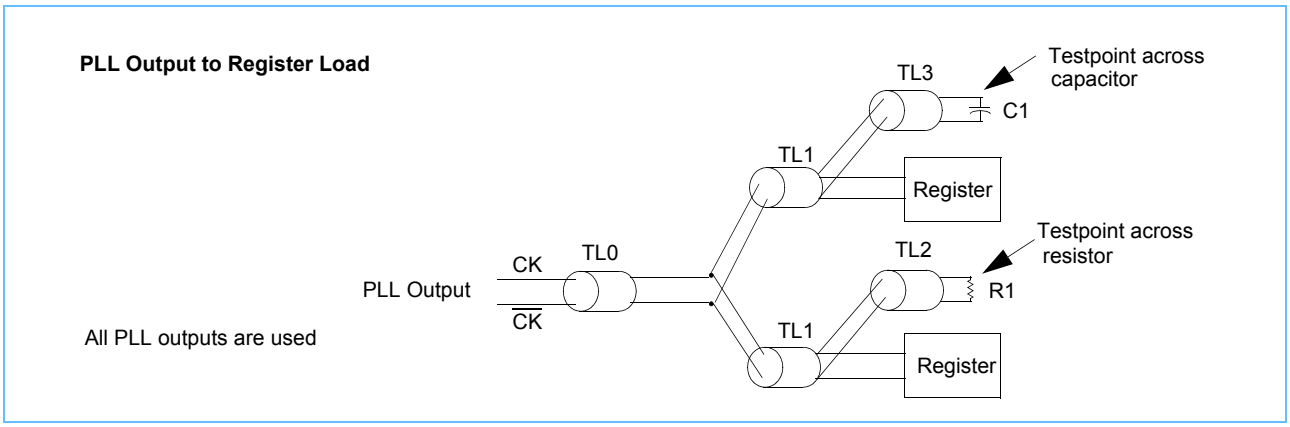
1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.
2. All capacitances are given in pF and should be kept within a tolerance of ± TBD%.
3. For non ECC DRAM
4. For ECC DRAM

Petitioners
Ex. 1066, p. 57

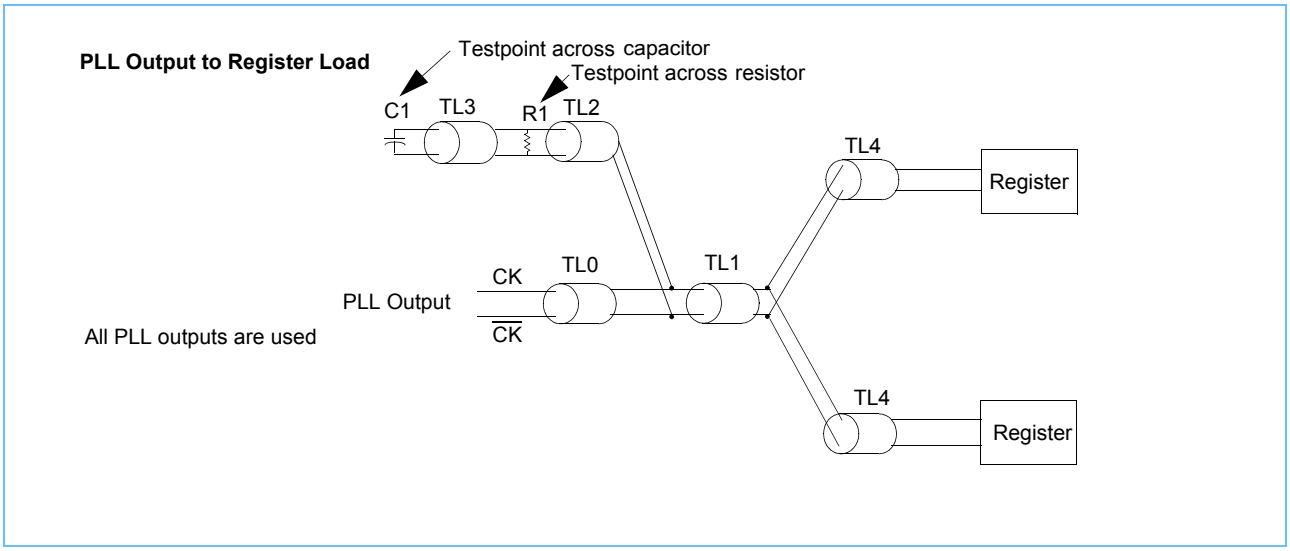
Net Structure Routing for PLL Output to Register Load (Raw Card A , F)



Net Structure Routing for PLL Output to Register Load (Raw Card B, C, G, H)

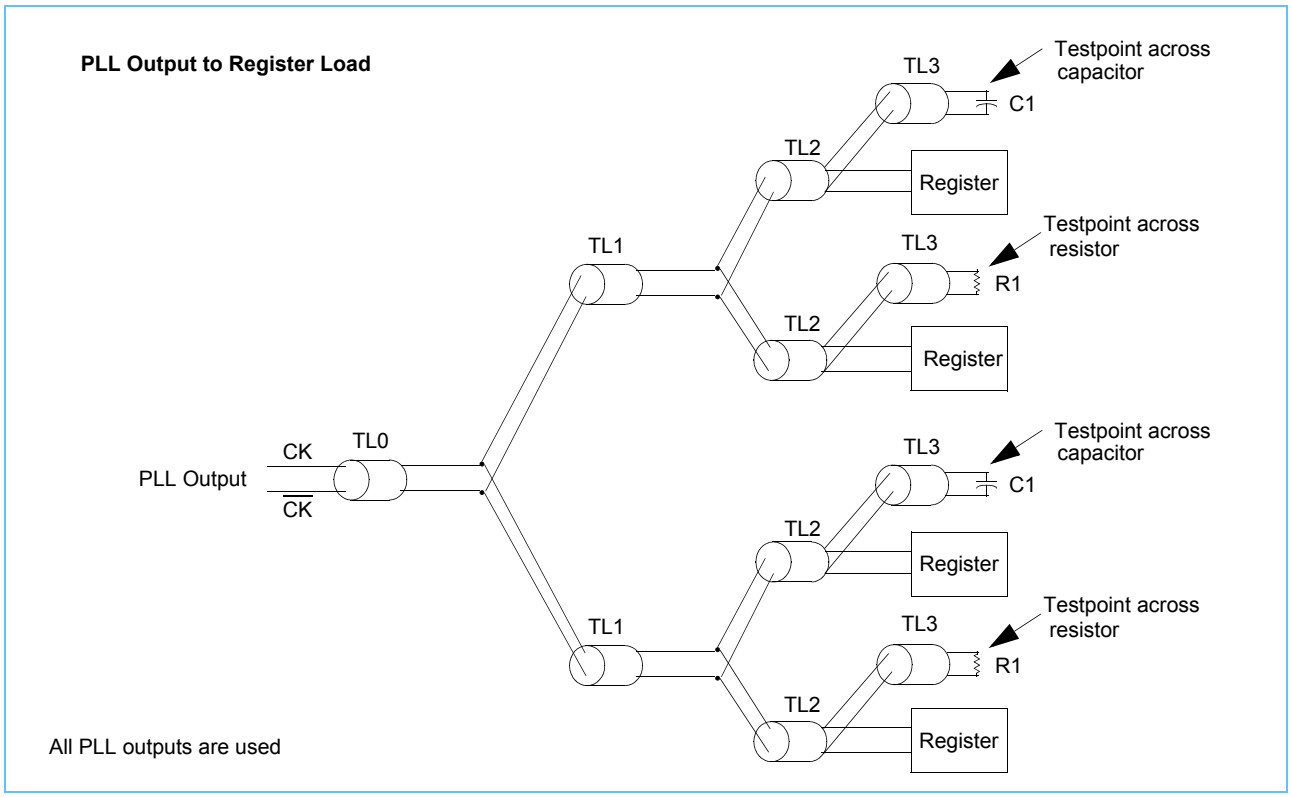


Net Structure Routing for PLL Output to Register Load (Raw Card D)



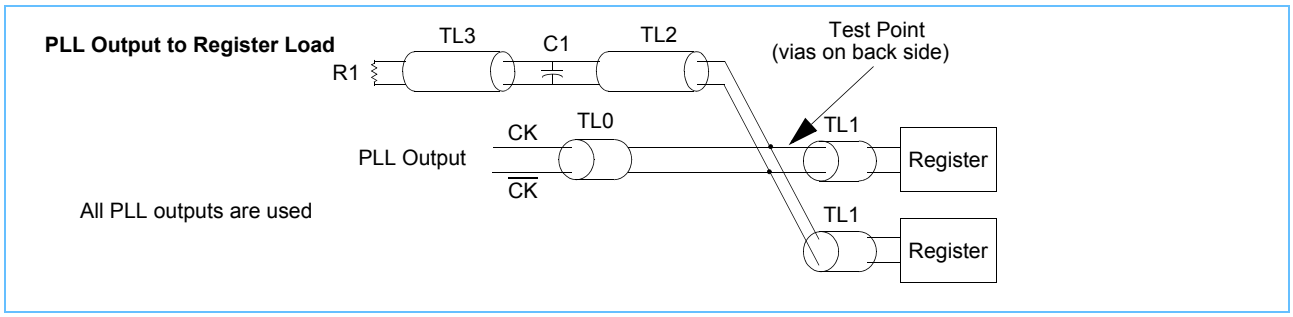
Petitioners
Ex. 1066, p. 58

Net Structure Routing for PLL Output to Register Load (Raw Card E)

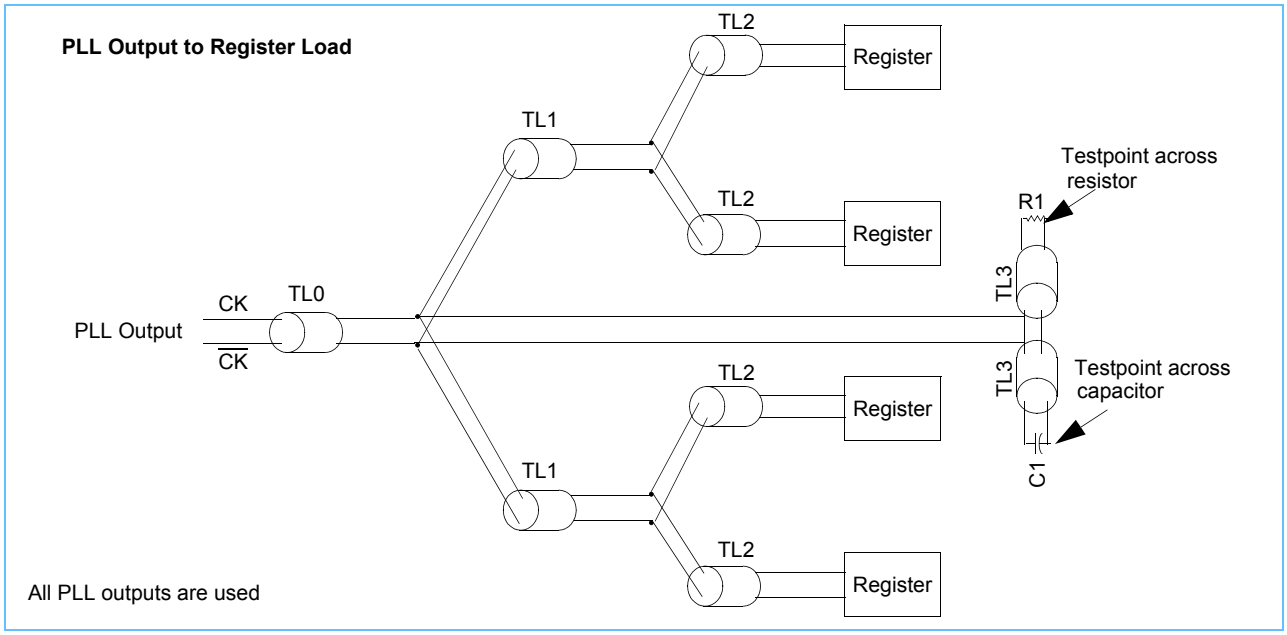


Petitioners
Ex. 1066, p. 59

Net Structure Routing for PLL Output to Register Load (Raw Card K)



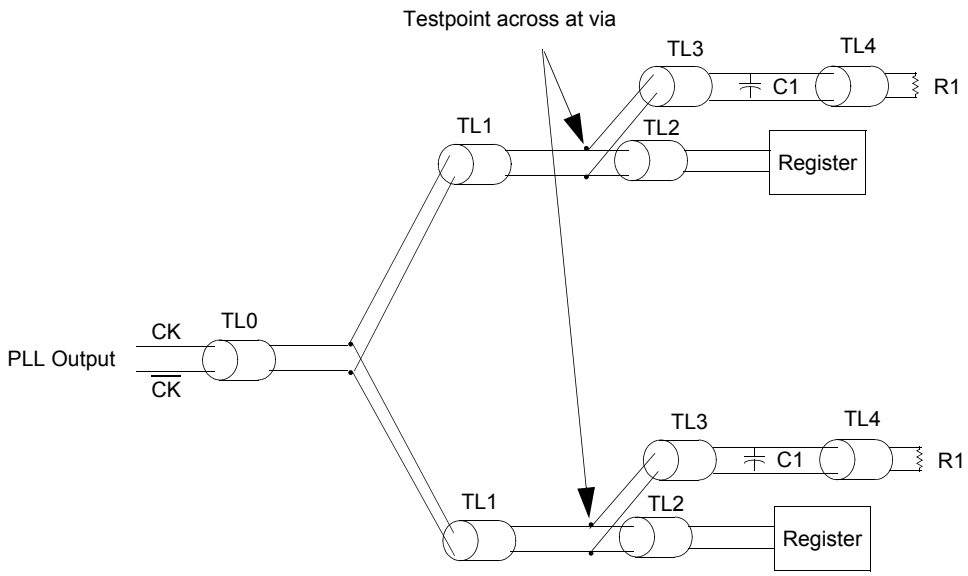
Net Structure Routing for PLL Output to Register Load (Raw Card J and N)



Petitioners
Ex. 1066, p. 60

Net Structure Routing for PLL Output to Register Load (Raw Card P)

PLL Output to Register Load



All PLL outputs are used

Trace Lengths for PLL Clock Output to Register Load Net Structure

Raw Card	TL0		TL1		TL2		TL3		TL4		R1 [Ohms[	C1 [pF]	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
A, F	50.2	50.3	0.5	0.6	2.9	3.0	0.9	1.0	-	-	120 ± 5%	TBD	1, 2
B, G	50.2	50.3	0.5	0.6	1.7	1.8	1.5	1.6	-	-	120 ± 5%	TBD	1, 2
C, H	50.2	50.3	0.5	0.6	1.7	1.8	1.5	1.6	-	-	120 ± 5%	TBD	1, 2
D	71.9	72.6	10.3	10.4	1.0	1.1	1.6	1.7	4.5	4.6	120 ± 5%	TBD	1, 2
E	25.0	25.0	9.4	9.5	0.5	0.6	1.5	1.6	-	-	240 ± 5%	TBD	1, 2
J	46.7	46.8	10.1	10.2	0.5	0.6	2.2	2.3	-	-	120 ± 5%	TBD	1, 2
K	60.0	60.1	0.4	1.2	1.2	1.9	1.0	1.1	-	-	120 ± 5%	TBD	1,2
N	46.7	46.8	10.1	10.2	0.5	0.6	1.5	1.6	-	-	120 ± 5%	TBD	1,2
P	55.0	55.1	19.9	20.0	0.4	0.5	4.0	4.1	1.0	1.0	240 ± 5%	TBD	1,2

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.
2. All capacitances are given in pF and should be kept within a tolerance of ± TBD%.

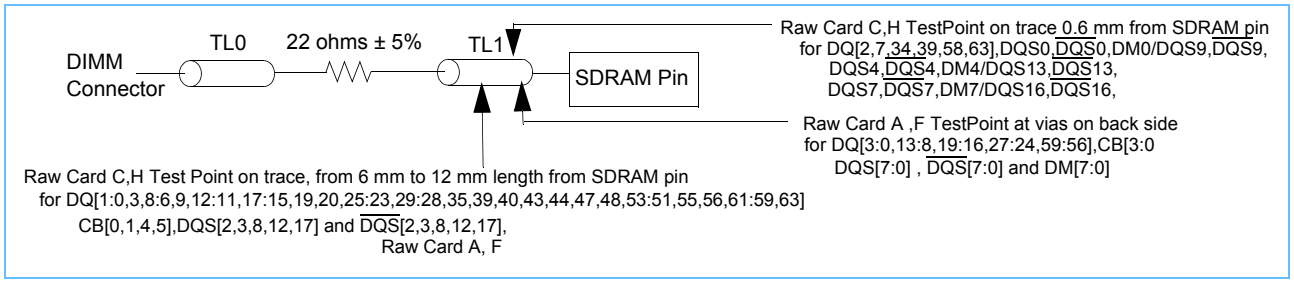
Petitioners
Ex. 1066, p. 61

Data Net Structures

DQ[63:0], CB[7:0], DQS[8:0], $\overline{\text{DQS}}$[8:0], DM[8:0]/RDQS[17:9],$\overline{\text{RDQS}}$[17:9]

Special attention has been paid to balancing data nets (including Check Bits) within a DDR SDRAM, within a particular DIMM, and across the DIMM family. Data nets have been placed in order to bound the data strobe nets. Because data travels with the data strobe, the placement of the strobe in the middle of the narrow window aids in data timing. Although it is not necessary to ensure consistent delays between SDRAMs and/or card types, doing so facilitates system design, system simulation, and DIMM specifications. We recommend consistent delays for all nets, as described in the following tables.

Net Structure Routing for DQ, DQS, DM (Raw Card A, F), for DQ, DQS (Raw Card C, H)



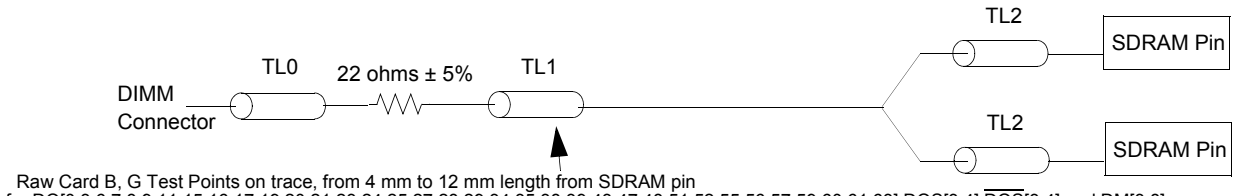
Trace Lengths for DQ, DQS, DM Net Structure (Raw Cards A, C, F, H)

Raw Card	TL0		TL1		TL0 + TL1 (2 via in trace)		TL0 + TL1 (1 via in trace)		TL0 + TL1 (no via in trace)		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
A, F	3.8	3.9	17.1	19.9	20.9	21.2	22.2	22.5	23.5	23.8	1, 2, 3
C, H	3.6	3.7	18.4	18.6	-	-	-	-	22.1	22.2	1, 2

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.
2. Total Min and Total Max refer to the min and max respectively of L0 + L1.
3. TL1 of Raw Card A is adjusted to compensate for the delay caused by via on DQ nets.

Petitioners
Ex. 1066, p. 62

Net Structure Routing for DQ, DQS, DM (Raw Card B, G), for DQ,DQS (Raw Card J, K)



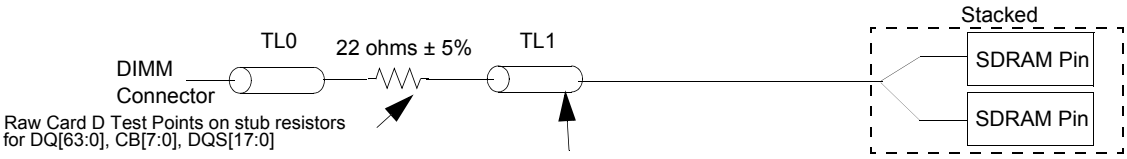
Raw Card B, G Test Points on trace, from 4 mm to 12 mm length from SDRAM pin
for DQ[0,3,6,7,8,9,11,15,16,17,19,20,21,23,24,25,27,28,29,34,35,38,39,43,47,48,51,52,55,56,57,59,60,61,63],DQS[3,4],$\overline{\text{DQS}}$[3,4] and DM[3,8]

Trace Lengths for DQ, DQS, DM Net Structure (Raw Card B, G), for DQ, DQS Net Structure(Raw Card J)

Raw Card	TL0		TL1		TL2		Total		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	
B, G	3.5	3.6	17.9	18.0	0.5	0.6	22.0	22.1	1, 2, 3
	3.5	3.6	14.7	15.4	3.1	3.8	22.0	22.1	1, 2, 4
J	3.4	4.7	20.2	23.1	4.1	6.3	29.6	29.8	1, 2

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.
2. Total Min and Total Max refer to the min and max respectively of L0 + L1 + L2
3. DQ
4. DQS, DM

Net Structure Routingfor DQ,DQS (Raw Card D, E, K, P)



Raw Card D Test Points on stub resistors
for DQ[63:0], CB[7:0], DQS[17:0]

Raw Card E Test Points on trace, from 4 mm to 6 mm length from SDRAM pin for CB[1,2,4,5]
DQ[2,3,7,8,12,13,17:15,21:19,24,2528,29,34,35,38,39,42,43,48:46,52:50,56:54,60,63], DQS[4:2,8,9,12,13,16,17]
Raw Card K Test Points on trace, from 5 mm to 12 mm length from SDRAM pin for
DQ[0,1,3,4,5,11,12,15,16,17,20,21,24,25,28,29,34,35,38,39,43,47,48,51,52,56,59,60,61,63], CB[1,4,5], DQS[3,8,12,17], $\overline{\text{DQS}}$[3,8,12,17]

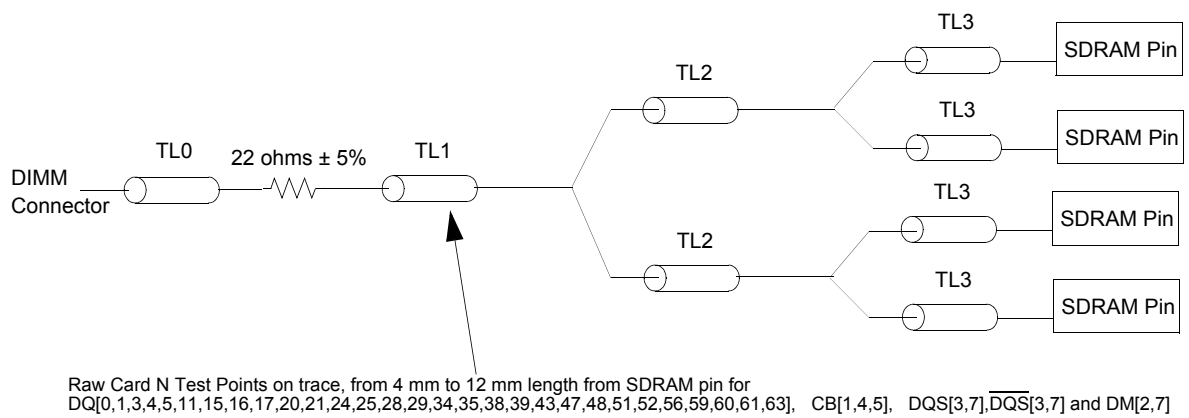
Trace Lengths for DQ, DQS, Net Structure (Raw Card D, E, K, P)

Raw Card	TL0		TL1		Total		Notes
	Min	Max	Min	Max	Min	Max	
D	8.0	8.1	23.0	23.1	31.0	31.1	1, 2
E	3.6	5.8	23.8	26.0	29.6	29.7	1, 2, 3
K	3.6	3.7	18.4	18.6	22.1	22.2	1, 2
P	3.6	5.8	28.8	30.9	34.5	34.6	1, 2

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.
2. Total Min and Total Max refer to the min and max respectively of L0 + L1 + L2
3. DQ58,59 has 2 vias on its line and via compensation (2.1mm per via) is applied on TL1

Petitioners
Ex. 1066, p. 63

Net Structure Routing for DQ, DQS, DM (Raw Card N)



Trace Lengths for DQ, DQS, DM Net Structure (Raw Card N)

Raw Card	TL0		TL1		TL2		TL3		Total		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
N	3.3	3.4	19.0	19.1	7.6	7.7	0.5	0.6	30.5	31.0	1, 2, 3
	3.3	3.4	16.7	16.8	7.6	7.7	2.8	2.9	30.5	31.0	1, 2, 4

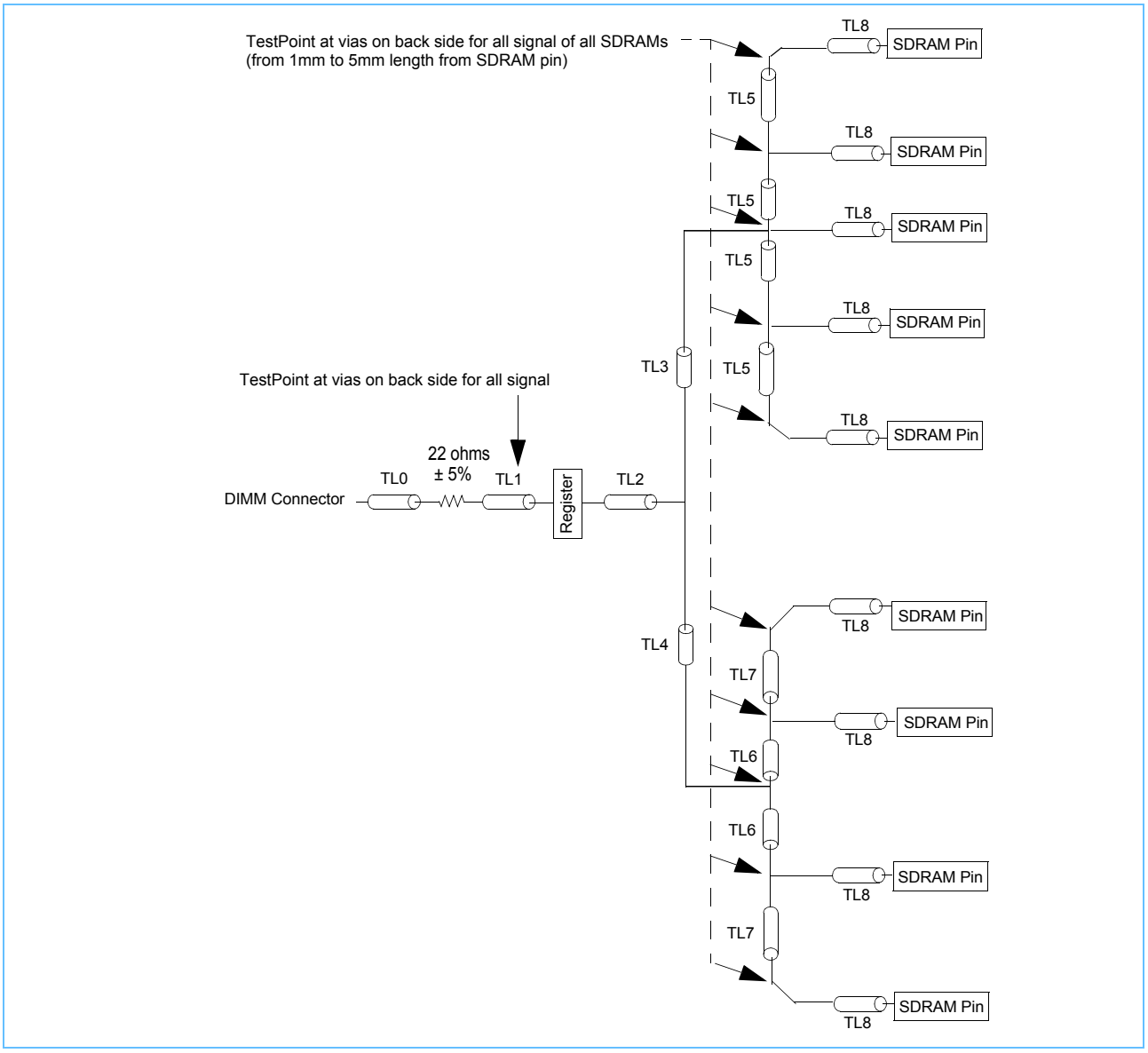
1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.
2. Total Min and Total Max refer to the min and max respectively of L0 + L1 + L2 + L3
3. DQ
4. DQS, DM

Petitioners
Ex. 1066, p. 64

Address/Command/Control Net Structures

Net Structure Routing for Address, Command and Control (Raw Card A, F)

A[15:0], BA[2:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{S0}$, CKE0, ODT0



Trace Lengths for Address, Command and Control (Raw Card A, F)

A[15:0], BA[2:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{S0}$, CKE0, ODT0

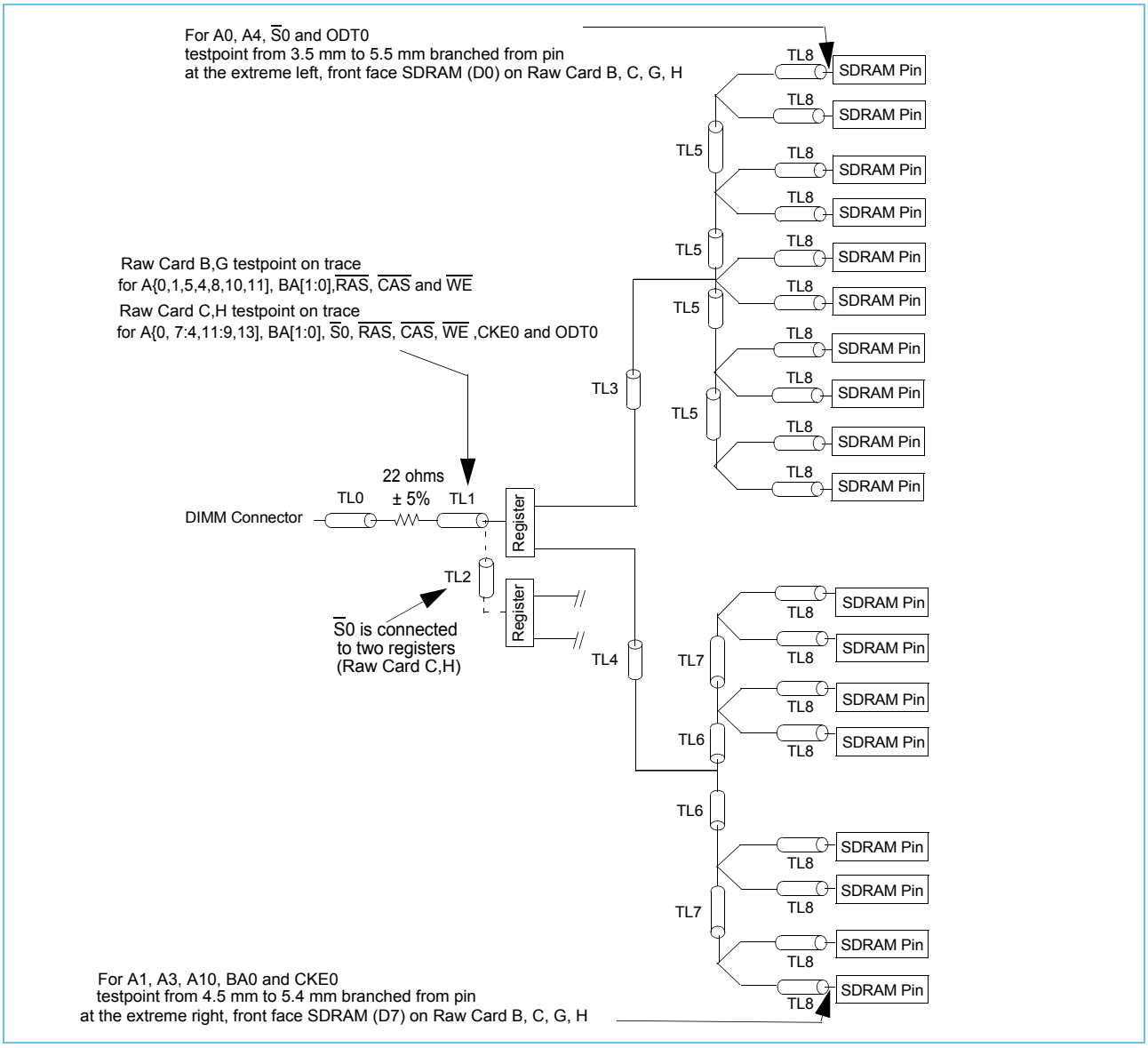
Raw Card	TL0		TL1		TL1 + TL2		TL2		TL3		TL4		TL5		TL6		TL7		TL8		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
A, F	3.1	4.6	28.8	30.2	33.4	33.6	0.5	0.6	37.6	37.8	46.4	46.5	13.9	14.0	6.9	7.1	13.9	14.0	1.3	5.4	1

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.

Petitioners
Ex. 1066, p. 65

Net Structure Routing for Address, Command and Control (Raw Cards B, C, G, H)

A[15:0], BA[2:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$,: Raw Card B, G
A[15:0], BA[2:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{S}$0, CKE0, ODT0: Raw Card C, H



Trace Lengths for Address, Command and Control Net Structure (Raw Cards B, C, G, H)

A[15:0], BA[2:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$,: Raw Card B, G
A[15:0], BA[2:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{S}$0, CKE0, ODT0: Raw Card C, H

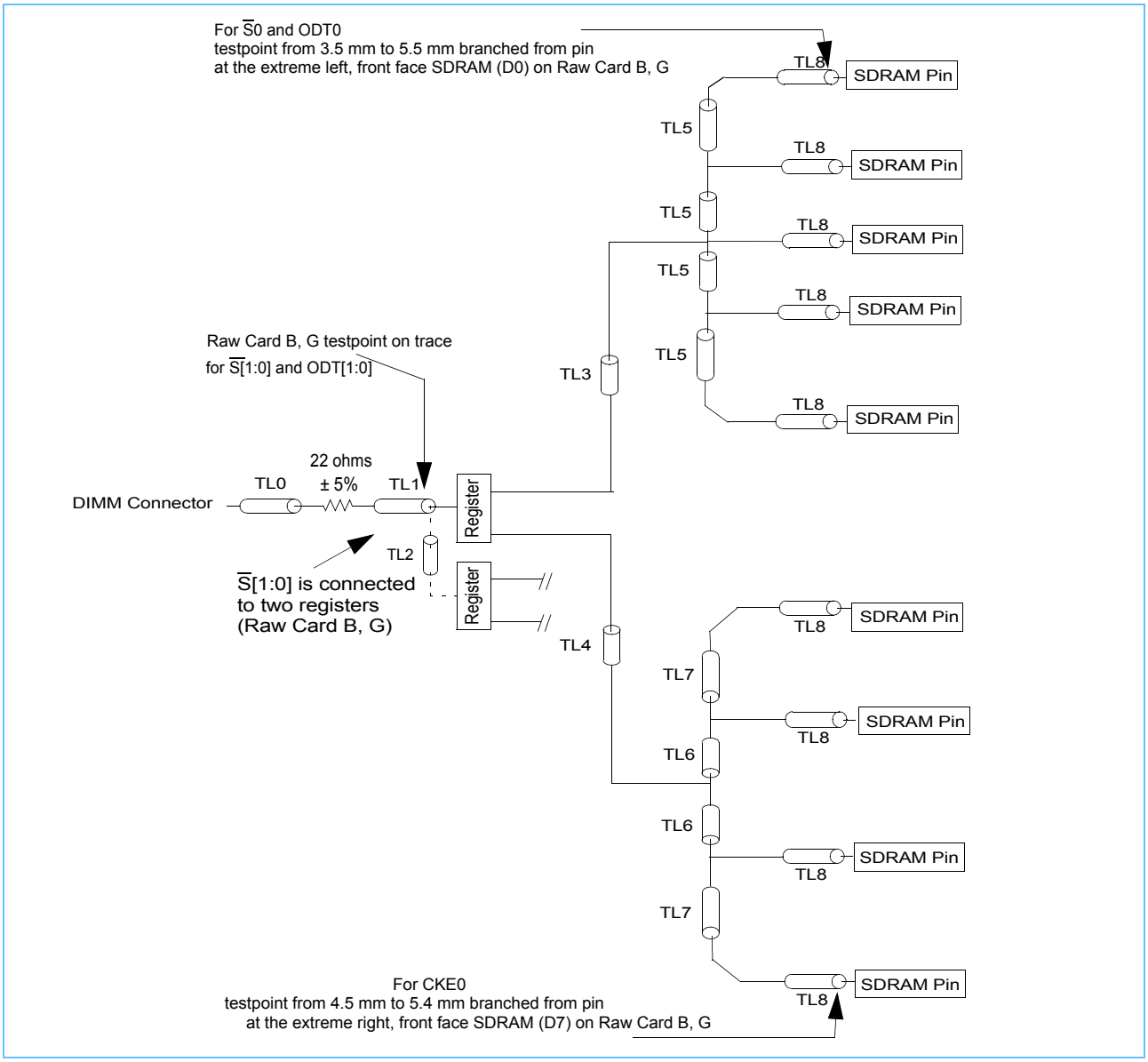
Raw Card	TL0		TL1		TL0 + TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
B, G	3.1	4.5	30.1	32.7	33.6	36.0	-	-	37.6	37.8	46.9	47.1	13.9	14.0	6.9	7.1	13.9	14.0	2.0	7.6	1,2
C, H	3.6	3.7	30.5	33.3	34.2	37.0	0.5	0.6	37.4	37.6	49.5	49.6	13.9	14.0	6.9	7.1	13.9	14.0	1.3	6.6	1,2

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.
2. TL2 is used only for $\overline{S}$0 of Raw Card C, H

Petitioners
Ex. 1066, p. 66

Net Structure Routing for Control (Raw Card B, G)

$\overline{S}$ [1:0], CKE [1:0], ODT[1:0]



Trace Lengths for Control (Raw Card B, G)

$\overline{S}$ [1:0], CKE [1:0], ODT[1:0]

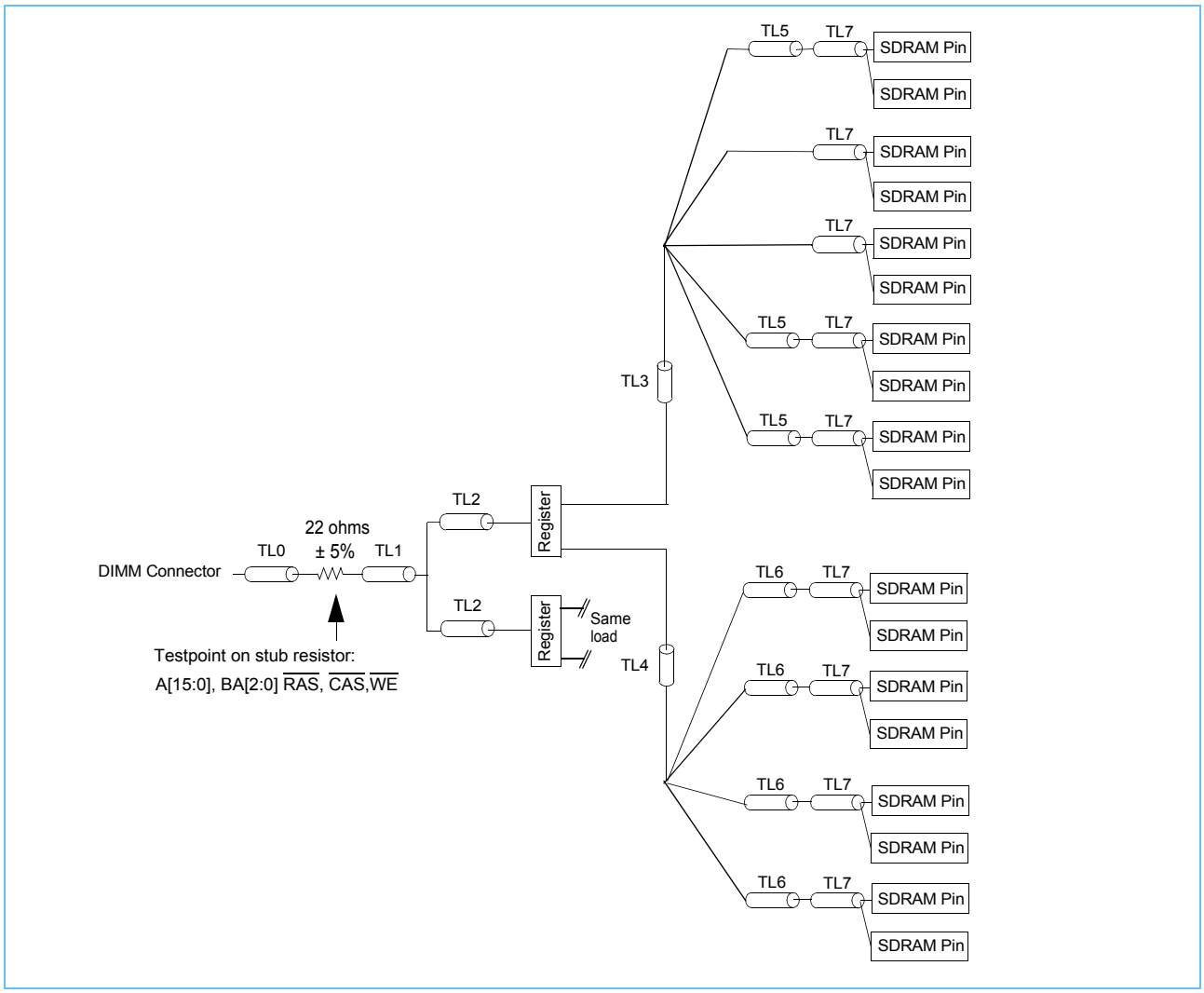
Raw Card	TL0		TL1		TL0+TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
B, G	3.5	3.6	29.9	31.3	33.4	34.9	0.5	0.6	37.6	37.8	46.9	47.1	13.9	14.0	6.9	7.1	13.9	14.0	2.0	7.6	1, 2

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.
2. TL2 is used only for S[1:0] of Raw Card B, G

Petitioners
Ex. 1066, p. 67

Net Structure Routing for Address and Command (Raw Cards D)

A[15:0], BA[2:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$



Trace Lengths for Address and Command Net Structure (Raw Cards D)

A[15:0], BA[2:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$,: Raw Card D

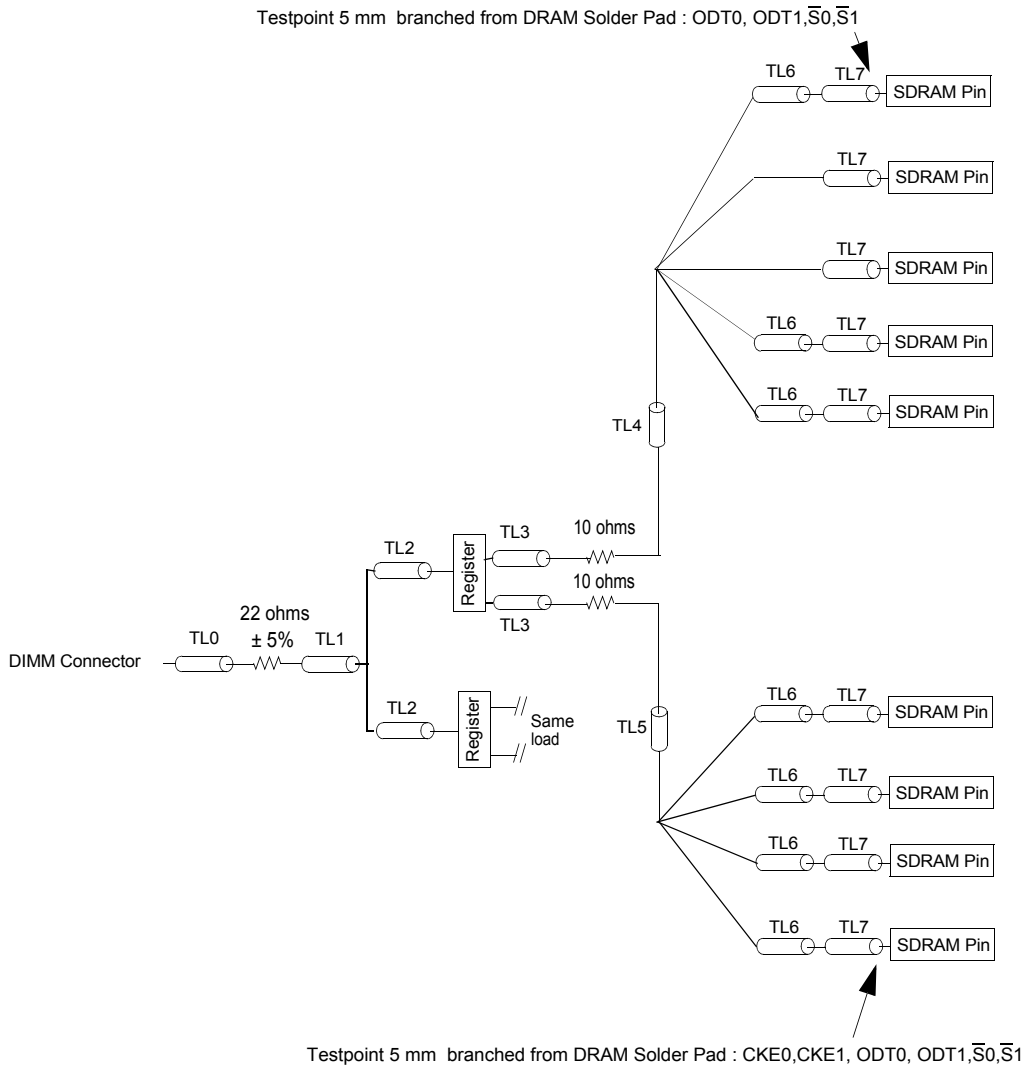
Raw Card	TL0		TL1		TL2		TL0+TL1+TL2		TL3		TL4		TL5		TL6		TL7		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
D	4.5	4.6	31.0	33.5	4.5	7.0	42.5	42.5	25.0	25.5	42.0	45.5	12.7	15.5	6.6	7.6	8.0	13.6	1

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter

Petitioners
Ex. 1066, p. 68

Net Structure Routing for Control (Raw Cards D)

$\overline{S}$ [1:0], CKE [1:0], ODT[1:0],



Trace Lengths for Control Net Structure (Raw Cards D)

$\overline{S}$ [1:0], CKE [1:0], ODT[1:0],: Raw Card D

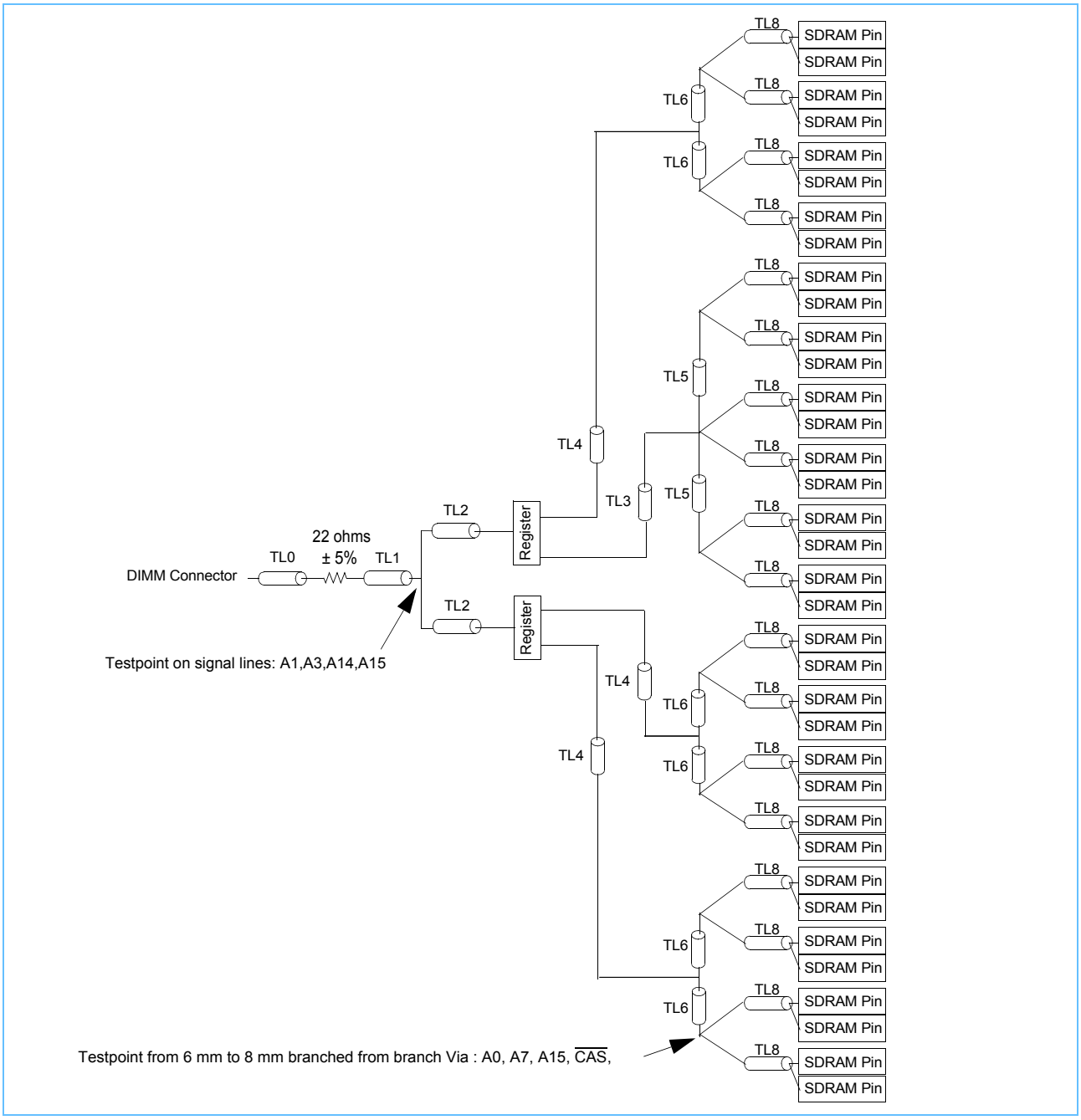
Raw Card	TL0		TL1		TL2		TL0 + TL1 + TL2		TL3		TL3 + TL4		TL3 + TL5		TL6		TL7		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
D	4.5	4.6	31.0	33.5	4.5	7.0	42.5	42.5	12.7	15.3	25.0	25.5	42.0	45.5	12.7	15.5	3.6	7.3	1, 2

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter
2. TL0 + TL1 + TL2 = 42.5 mm

Petitioners
Ex. 1066, p. 69

Net Structure Routing for Address and Command (Raw Card E)

A[15:0], BA[2:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$



Trace Lengths for Address and Command Net Structure (Raw Card E)

A[15:0], BA[2:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$

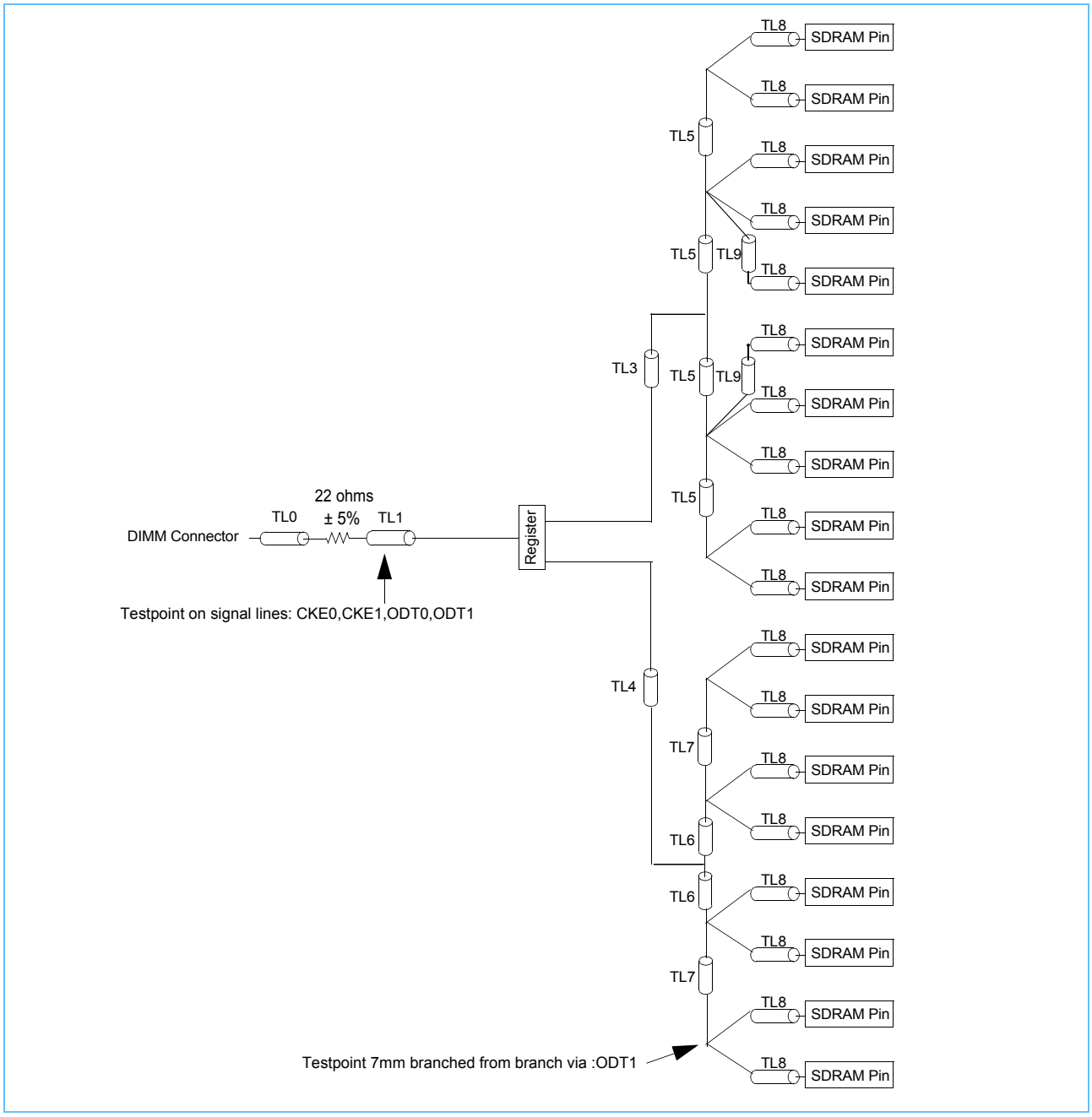
Raw Card	TL0		TL1		TL2		TL0 + TL1 + TL2		TL3		TL4		TL5		TL6		TL8		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
E	3.8	3.9	9.9	10.4	0.0	3.3	13.8	17.1	44.9	45.0	79.9	80.0	14.5	14.6	7.5	7.6	2.0	9.0	1

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.

Petitioners
Ex. 1066, p. 70

Net Structure Routing for Control (Raw Card E)

CKE [1:0], ODT[1:0]



Trace Lengths for Control Net Structure (Raw Card E)

CKE [1:0], ODT[1:0]

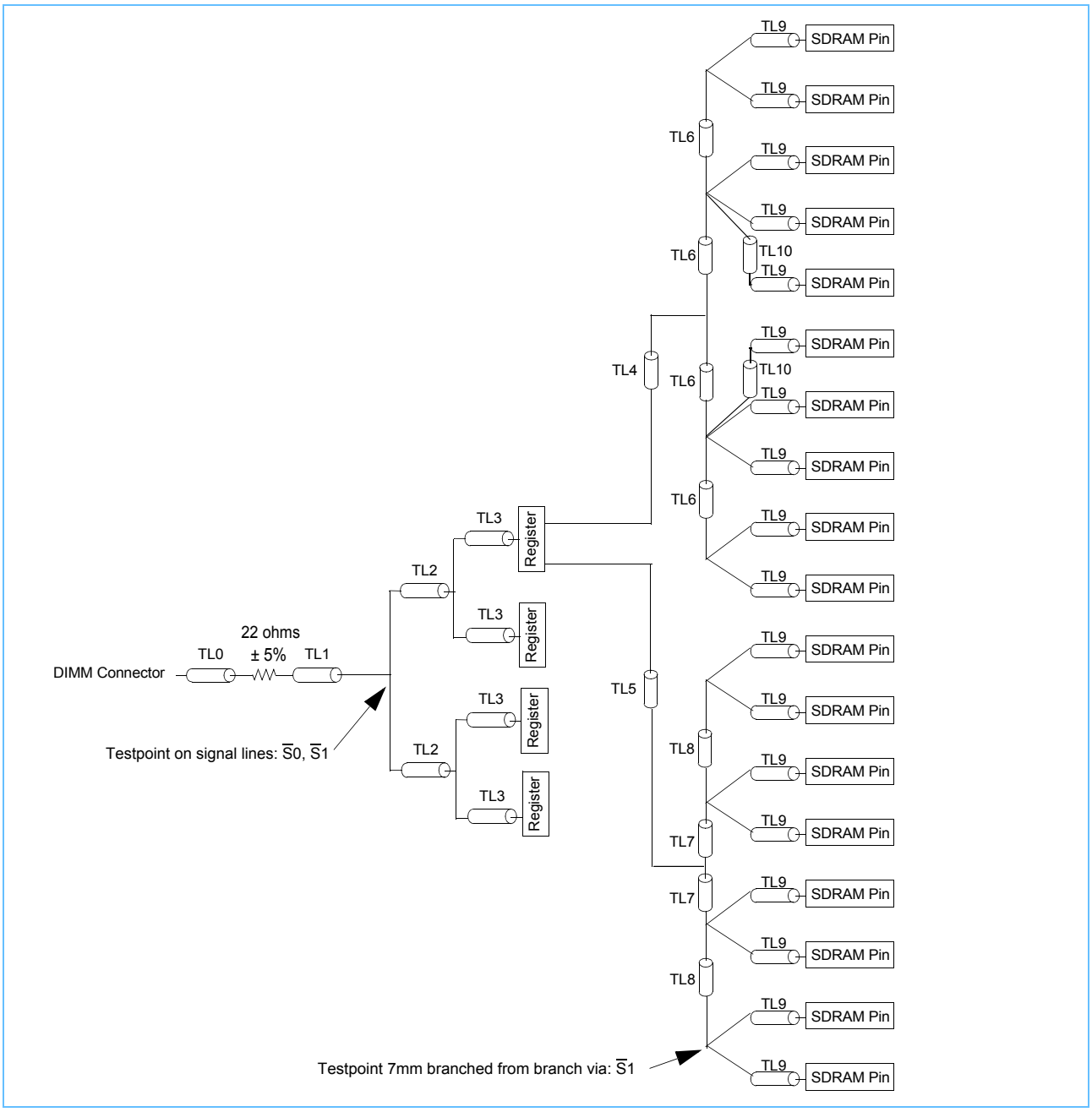
Raw Card	TL0		TL1		TL0 + TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		TL9		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
E	3.8	3.9	29.9	30.0	33.8	33.9	-	-	42.9	43.0	49.4	49.5	14.5	14.6	8.7	8.8	14.7	14.8	2.0	8.0	9.7	12.9	1

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.

Petitioners
Ex. 1066, p. 71

Net Structure Routing for Control (Raw Card E)

$\overline{S}$ [1:0]



Trace Lengths for Control Net Structure (Raw Card E)

$\overline{S}$ [1:0]

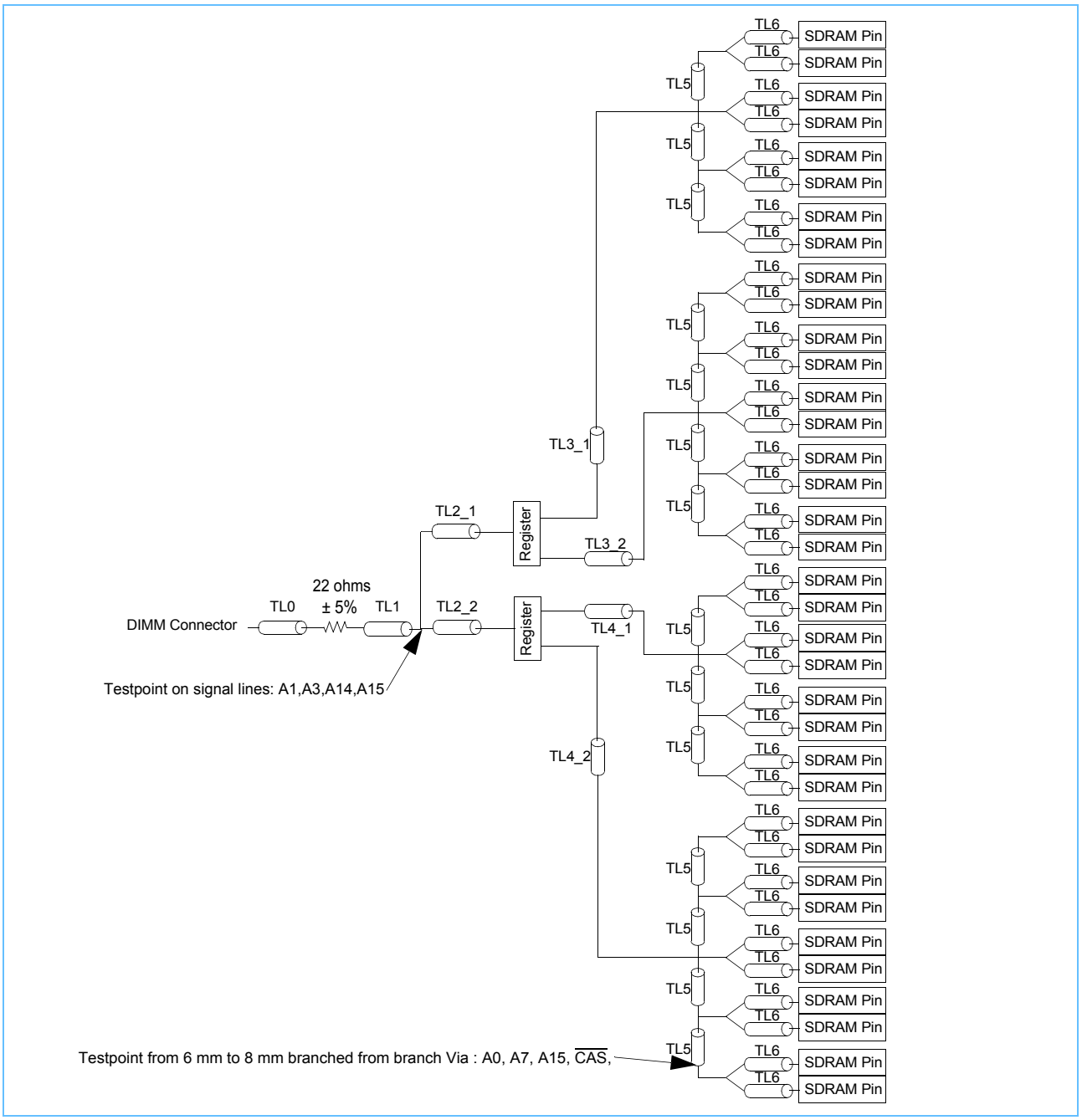
Raw Card	TL0		TL1		TL2		TL3		TL0+TL1+TL2+TL3		TL4		TL5		TL6		TL7		TL8		TL9		TL10		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
E	3.8	3.9	16.0	16.0	11.9	11.9	0.5	0.6	32.2	32.4	42.9	43.0	49.4	49.5	14.5	14.6	8.7	8.8	14.7	14.8	2.0	8.0	9.7	9.8	1

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.

Petitioners
Ex. 1066, p. 72

Net Structure Routing for Address and Command (Raw Cards J)

A[15:0], BA[2:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$



Trace Lengths for Address and Command Net Structure (Raw Cards J)

A[15:0], BA[2:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$

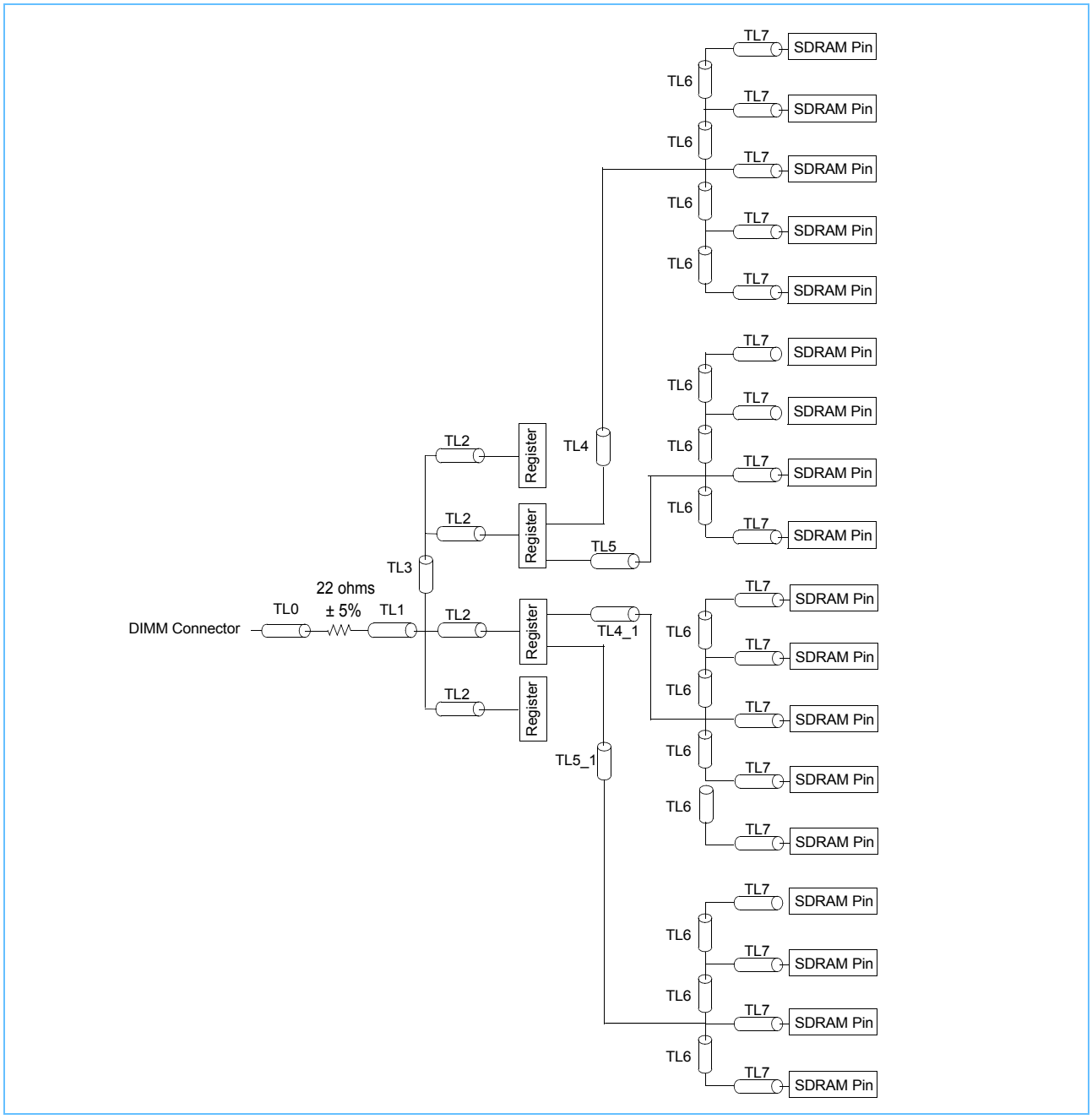
Raw Card	TL0		TL1		TL2_1		TL2_2		TL0+TL1+TL2_1, TL0+TL1+TL2_2		TL3_1		TL3_2		TL4_1		TL4_2		TL5		TL6		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
J	3.1	6.0	19.4	33.2	0.0	13.6	0.0	2.1	24.9	39.4	56.4	58.6	39.6	41.8	43.4	45.6	58.2	60.4	12.0	14.0	0.9	6.2	1

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter

Petitioners
Ex. 1066, p. 73

Net Structure Routing for Control (Raw Cards J)

S0



Trace Lengths for Control Net Structure (Raw Cards J)

S0:Raw Card J

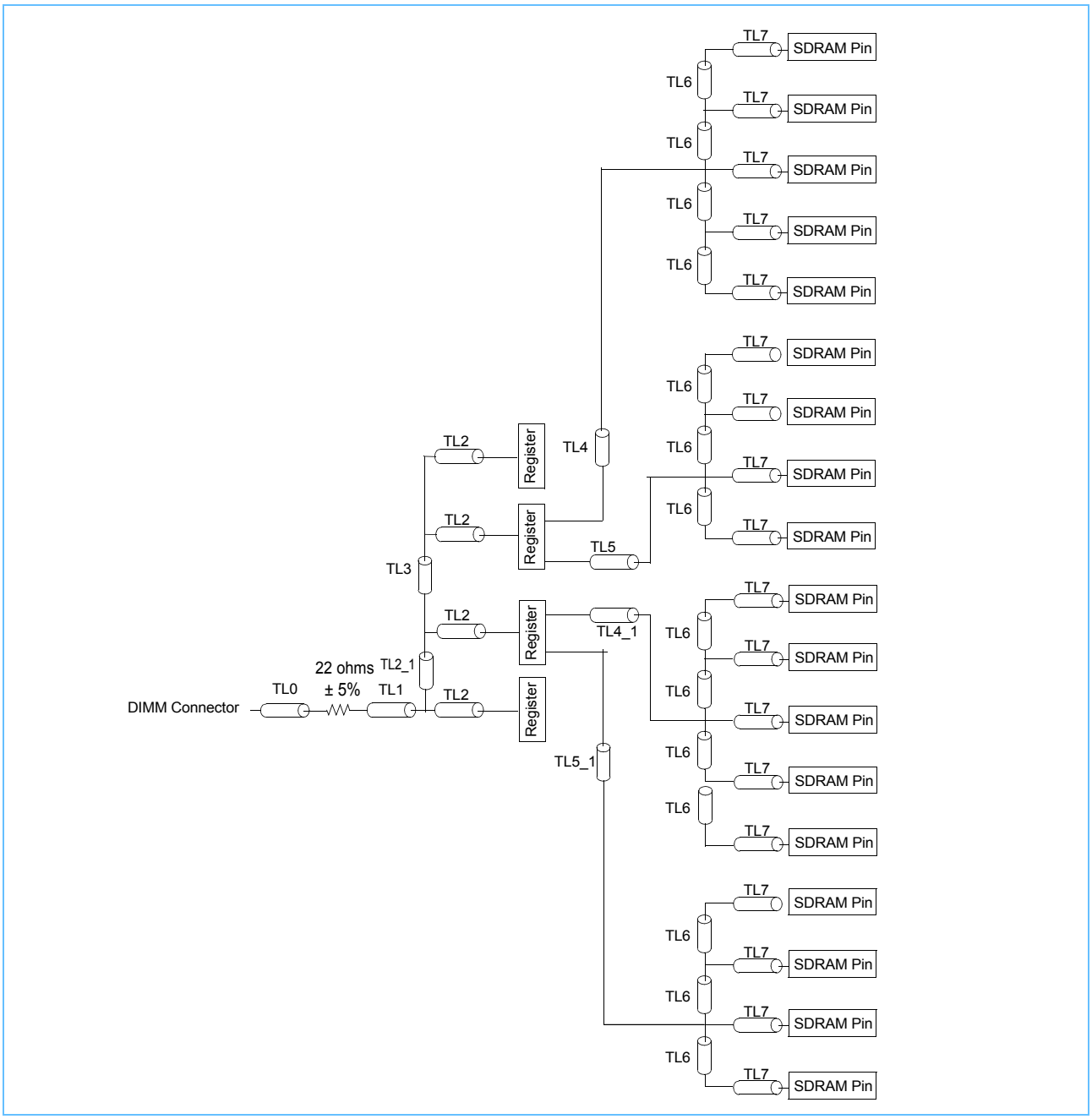
Raw Card	TL0		TL1		TL2		TL3		TL0+TL1+ TL2+TL3		TL4		TL4_1		TL5		TL5_1		TL6		TL7		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
J	3.4	3.4	20.3	20.3	0.5	2.0	11.1	11.1	35.3	36.8	40.8	42.3	56.4	57.3	56.6	57.7	45.9	46.5	11.9	13.2	1.3	2.6	1

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimete

Petitioners
Ex. 1066, p. 74

Net Structure Routing for Control (Raw Cards J)

$\overline{S1}$



Trace Lengths for Control Net Structure (Raw Cards J)

$\overline{S1}$: Raw Card J

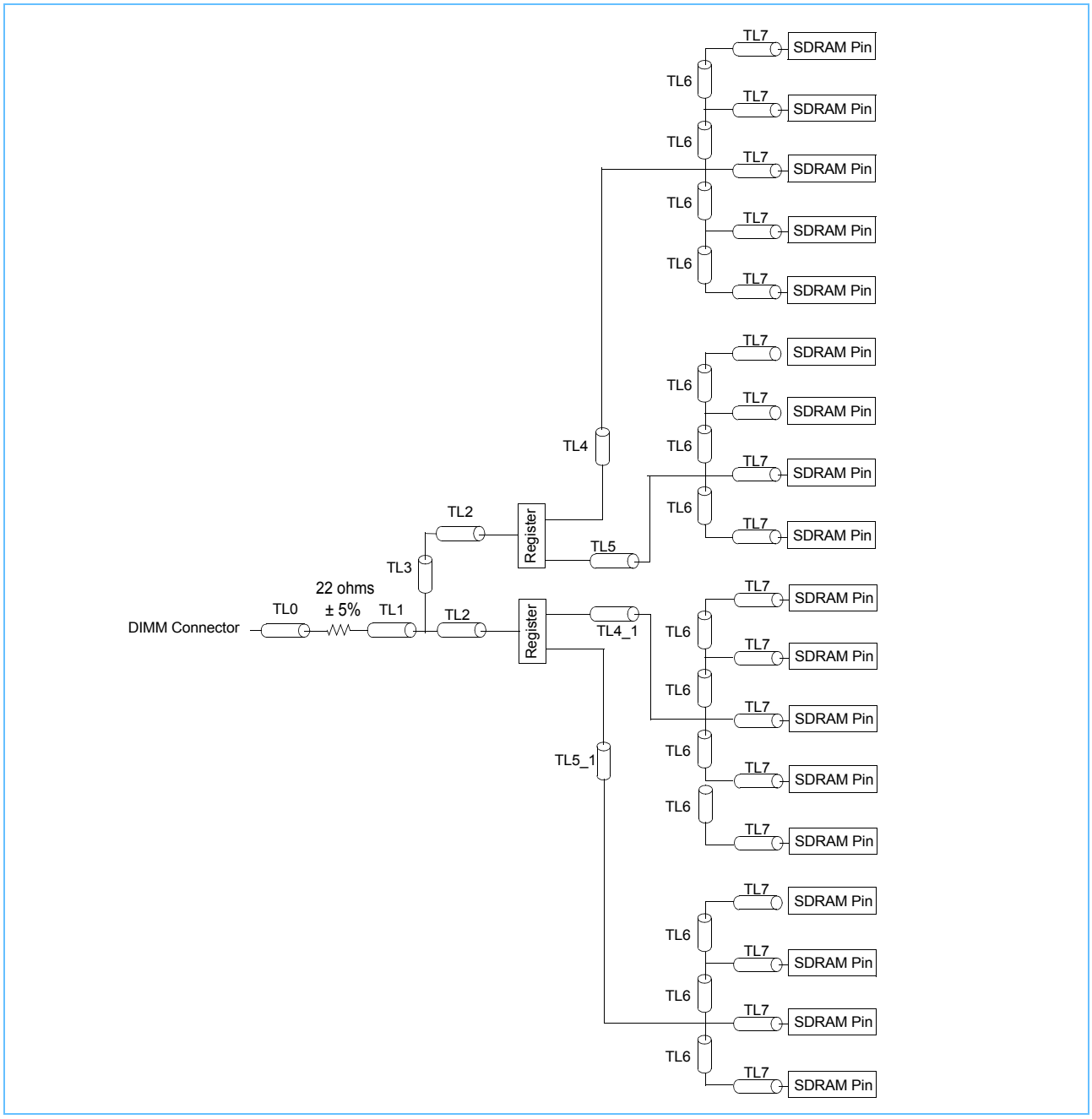
Raw Card	TL0		TL1		TL2		TL2_1		TL3		TL0+TL1+TL2 +TL2_1+TL3		TL4		TL4_1		TL5		TL5_1		TL6		TL7		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
J	3.1	3.1	19.5	19.5	0	2.2	2.1	2.1	12.4	12.4	37.1	39.3	40.8	42.3	56.4	57.3	56.6	57.7	45.9	46.5	11.9	13.2	1.3	2.6	1

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimete

Petitioners
Ex. 1066, p. 75

Net Structure Routing for Control (Raw Card J)

CKE [1:0], ODT[1:0],



Trace Lengths for Control Net Structure (Raw Card J)

CKE [1:0], ODT[1:0],: Raw Card J

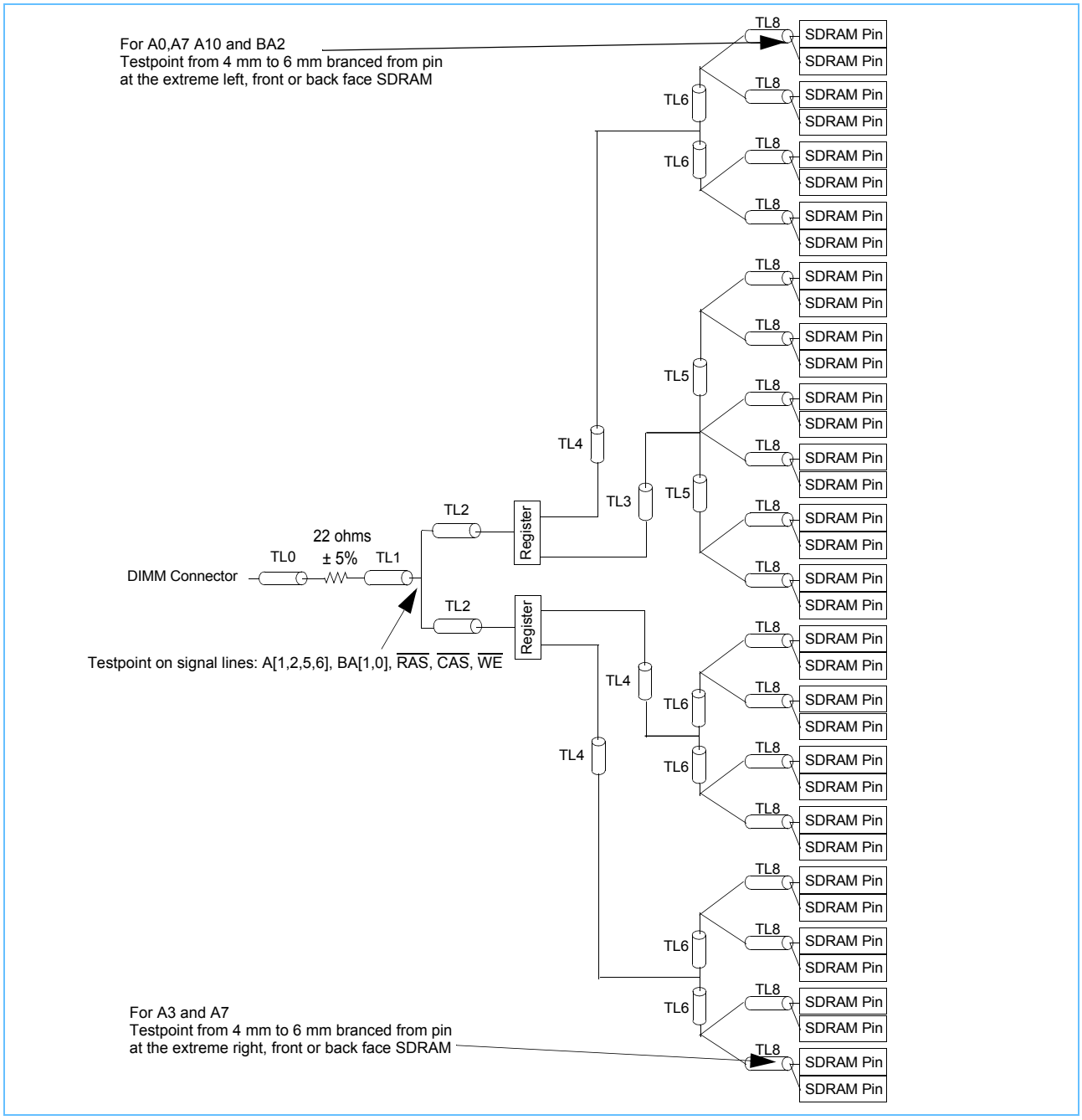
Signal	TL0		TL1		TL2		TL3		TL0+TL1+TL2+TL3		TL4		TL4_1		TL5		TL5_1		TL6		TL7		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
CKE[1:0]	4.1	4.6	20.7	21.3	0.0	0.8	11.4	11.8	36.2	38.5	41.4	42.0	56.7	56.9	56.6	57.2	46.0	47.0	12.5	13.4	1.6	3.6	1
ODT[1:0]	3.1	3.4	20.1	21.5	0.5	1.7	11.6	12.0	35.3	38.6	41.1	41.8	56.7	57.0	56.3	56.7	46.3	46.5	12.8	13.4	0.8	1.9	1

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimete

Petitioners
Ex. 1066, p. 76

Net Structure Routing for Address and Command (Raw Card K)

A[15:0], BA[2:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$



Trace Lengths for Address and Command Net Structure (Raw Card K)

A[15:0], BA[2:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$

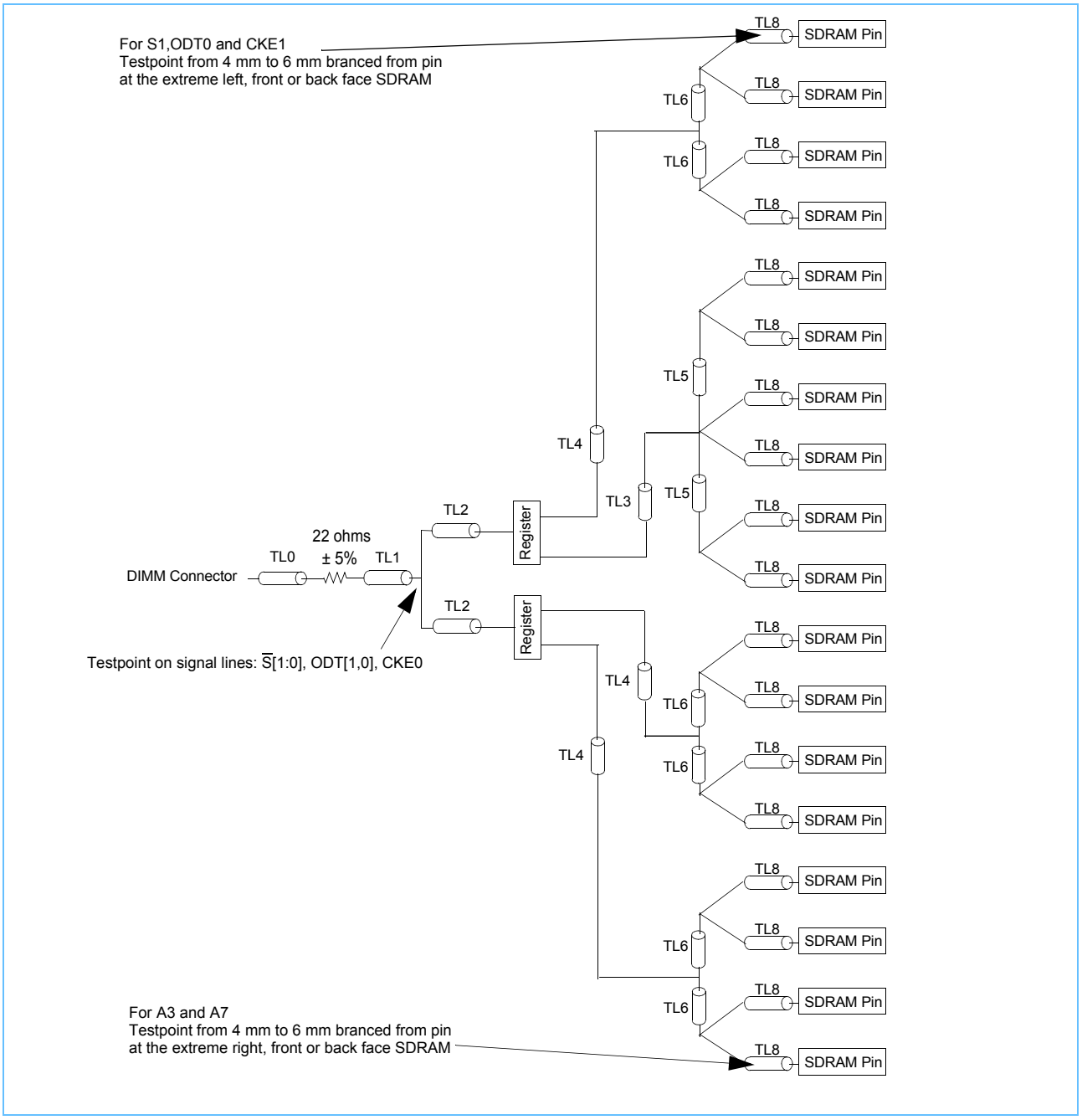
Raw Card	TL0		TL1		TL2		TL0 + TL1 + TL2		TL3		TL4		TL5		TL6		TL7		TL8		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
K	3.6	3.7	29.5	34.6	0.4	4.0	36.0	38.7	24.9	25.0	59.9	60.0	13.9	14.0	6.9	7.0	-	-	1.4	9.3	1

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.

Petitioners
Ex. 1066, p. 77

Net Structure Routing for Control (Raw Card K)

$\overline{S}$[1:0], CKE[1:0], ODT[1:0]



Trace Lengths for Control Net Structure (Raw Card K)

$\overline{S}$[1:0], CKE[1:0], ODT[1:0]

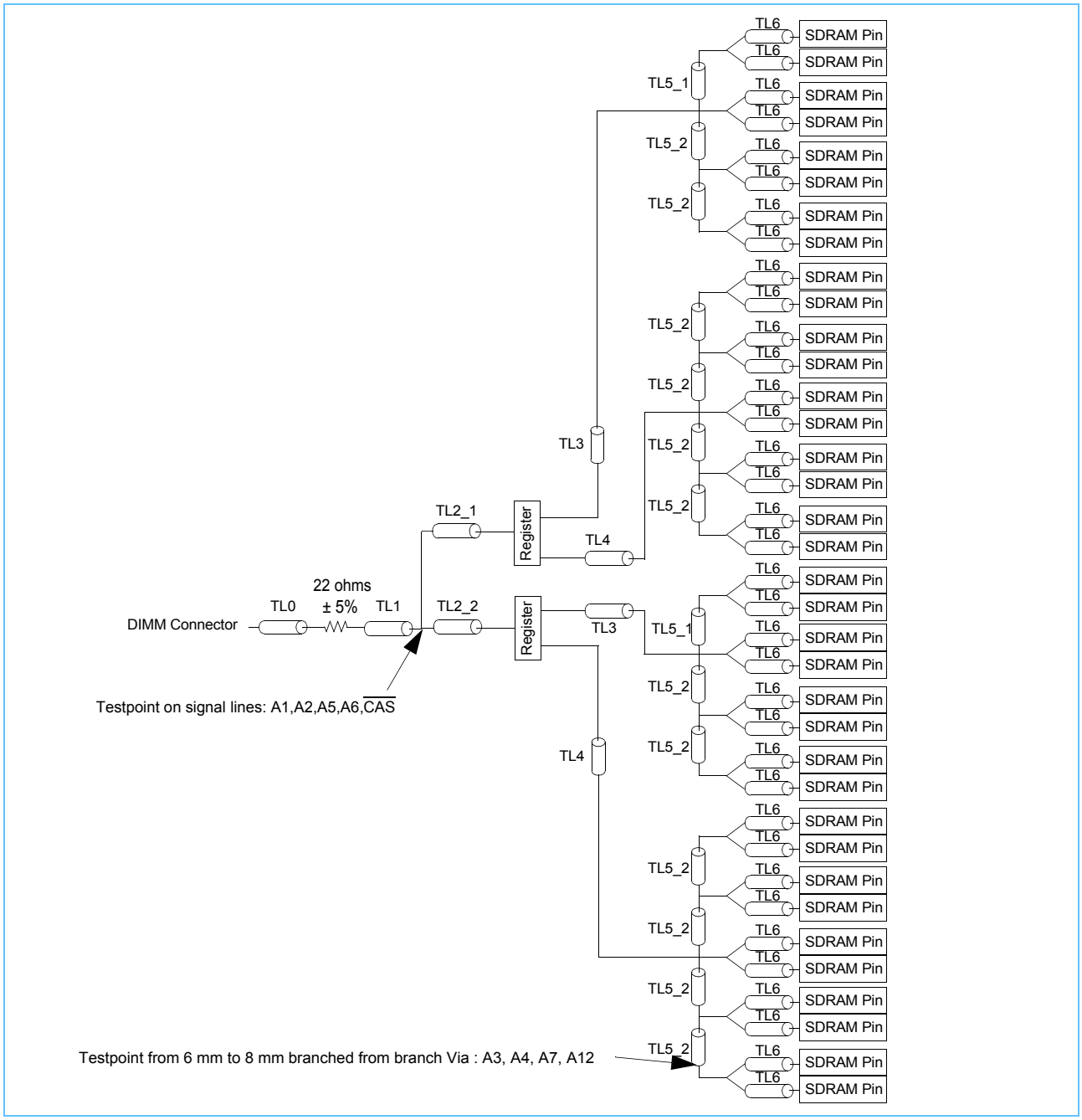
Raw Card	TL0		TL1		TL2		TL0 + TL1 + TL2		TL3		TL4		TL5		TL6		TL7		TL8		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
K	3.6	3.7	28.8	31.8	1.2	4.1	36.1	37.2	44.9	45.0	79.9	80.0	13.9	14.0	6.9	7.0	-	-	2.0	6.6	1

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.

Petitioners
Ex. 1066, p. 78

Net Structure Routing for Address and Command (Raw Cards N)

A[15:0], BA[2:0], RAS, CAS, WE



Trace Lengths for Address and Command Net Structure (Raw Cards N)

A[15:0], BA[2:0], RAS, CAS, WE

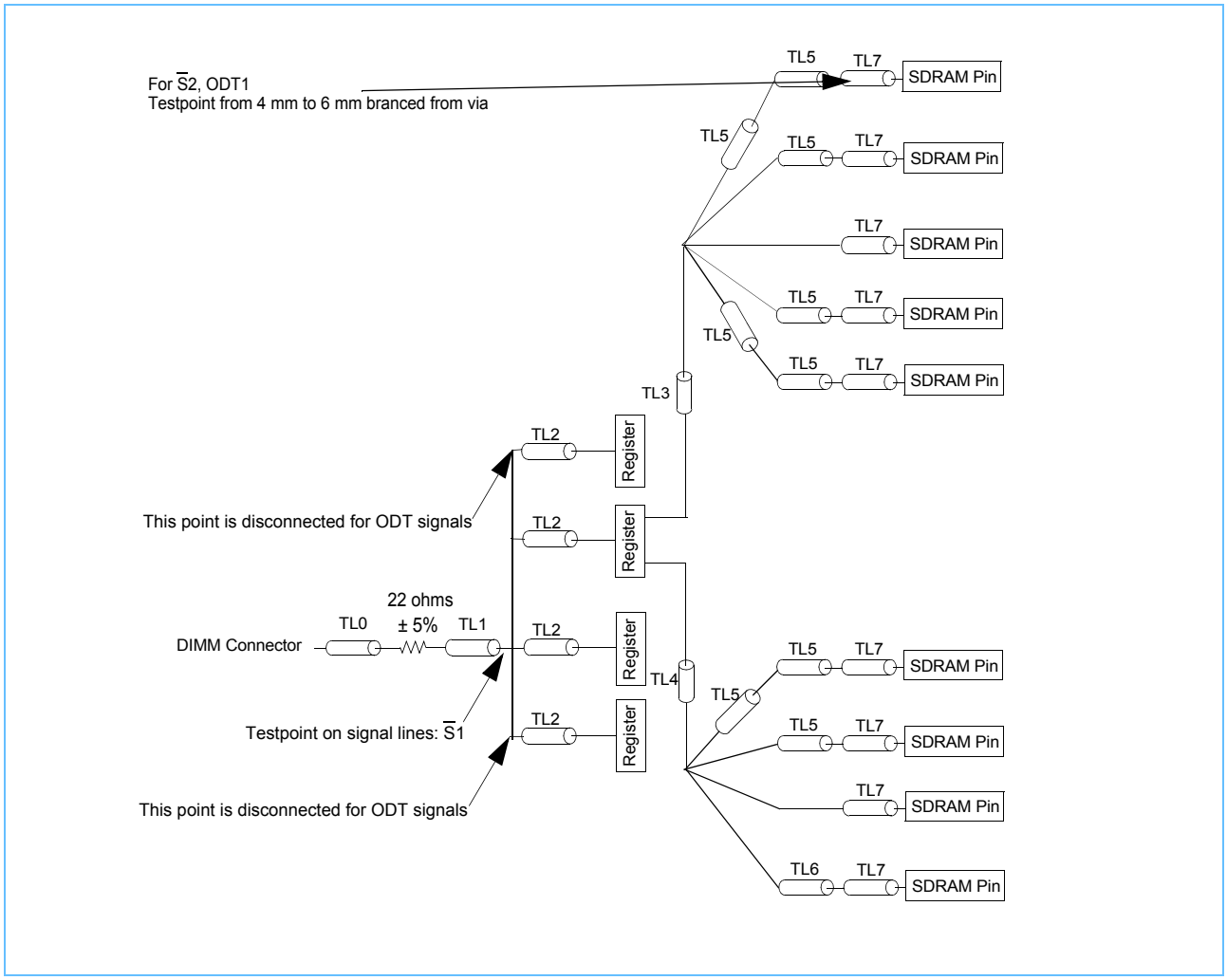
Raw Card	TL0		TL1		TL2_1		TL2_2		TL0+TL1+TL2_1, TL0+TL1+TL2_2		TL3		TL4		TL5_1		TL5_2		TL6		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
N	3.0	6.2	18.0	24.0	18.5	23.5	0.0	2.2	22.0	49.7	48.0	50.5	48.0	52.0	33.9	34.1	13.0	13.2	1.5	4.8	1

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter

Petitioners
Ex. 1066, p. 79

Net Structure Routing for Control (Raw Cards N)

$\overline{S}$ [3:0], ODT[1:0]



Trace Lengths for Control Net Structure (Raw Cards N)

$\overline{S}$ [3:0], ODT[1:0],: Raw Card N

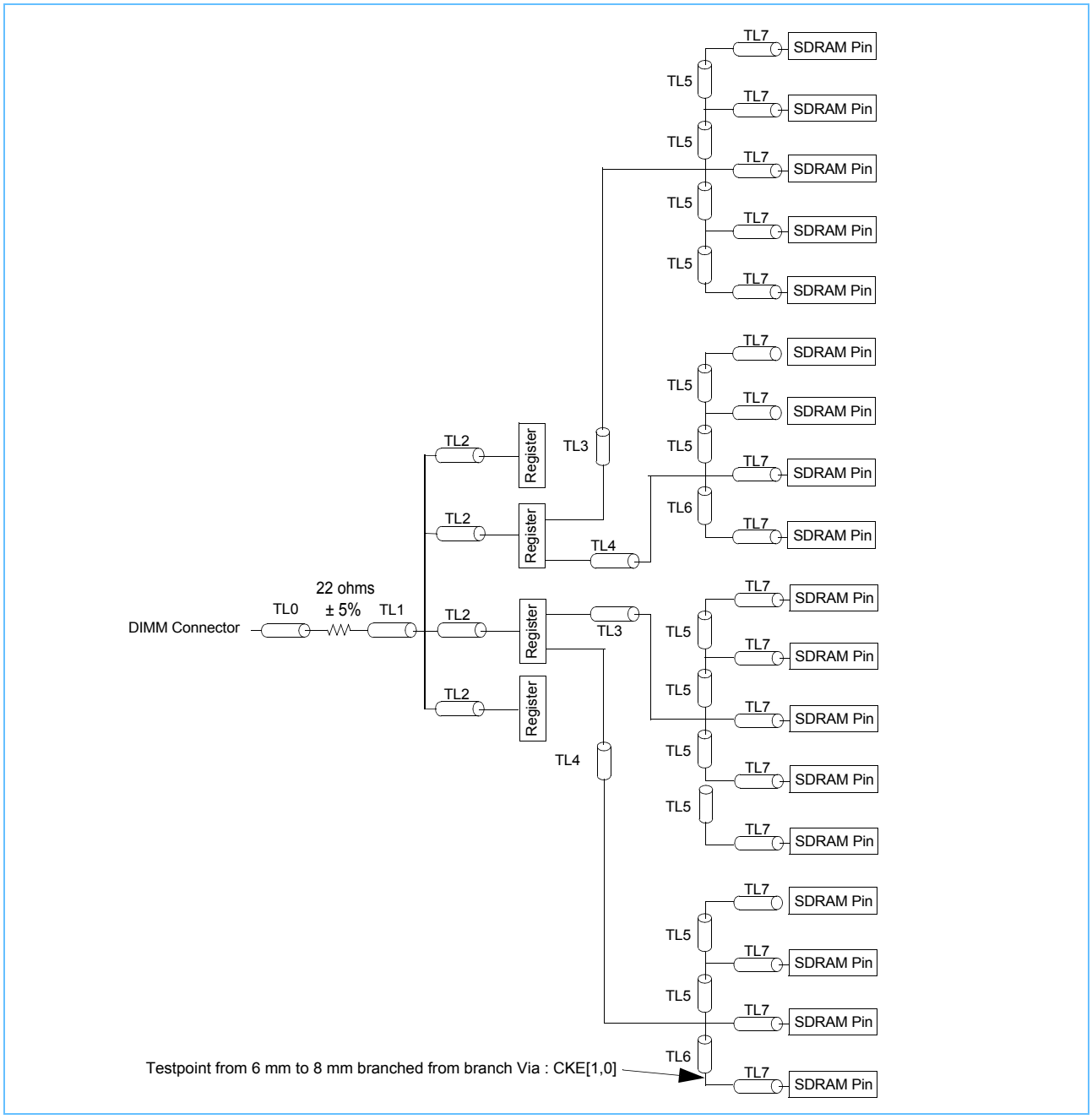
Raw Card	TL0		TL1		TL2		TL0 + TL1 + TL2		TL3		TL4		TL5		TL6		TL7		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
N	3.1	4.1	20.0	28.0	0	2.2	24.0	34.0	54.0	58.0	58.0	62.0	13.0	13.2	33.9	34.1	1.5	3.5	1, 2
	3.1	4.1	19.5	21.3	0	2.2	28.0	34.0	54.0	58.0	58.0	62.0	13.0	13.2	33.9	34.1	1.5	3.5	1, 3
	3.1	4.1	56.5	56.6	0	2.2	65.0	71.0	54.0	58.0	58.0	62.0	13.0	13.2	33.9	34.1	1.5	3.5	1, 4

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimete
2. ODT
3. $\overline{S}$0, $\overline{S}$1
4. $\overline{S}$2, $\overline{S}$3

Petitioners
Ex. 1066, p. 80

Net Structure Routing for Control (Raw Cards N)

CKE [1:0]



Trace Lengths for Control Net Structure (Raw Cards N)

CKE [1:0]: Raw Card N

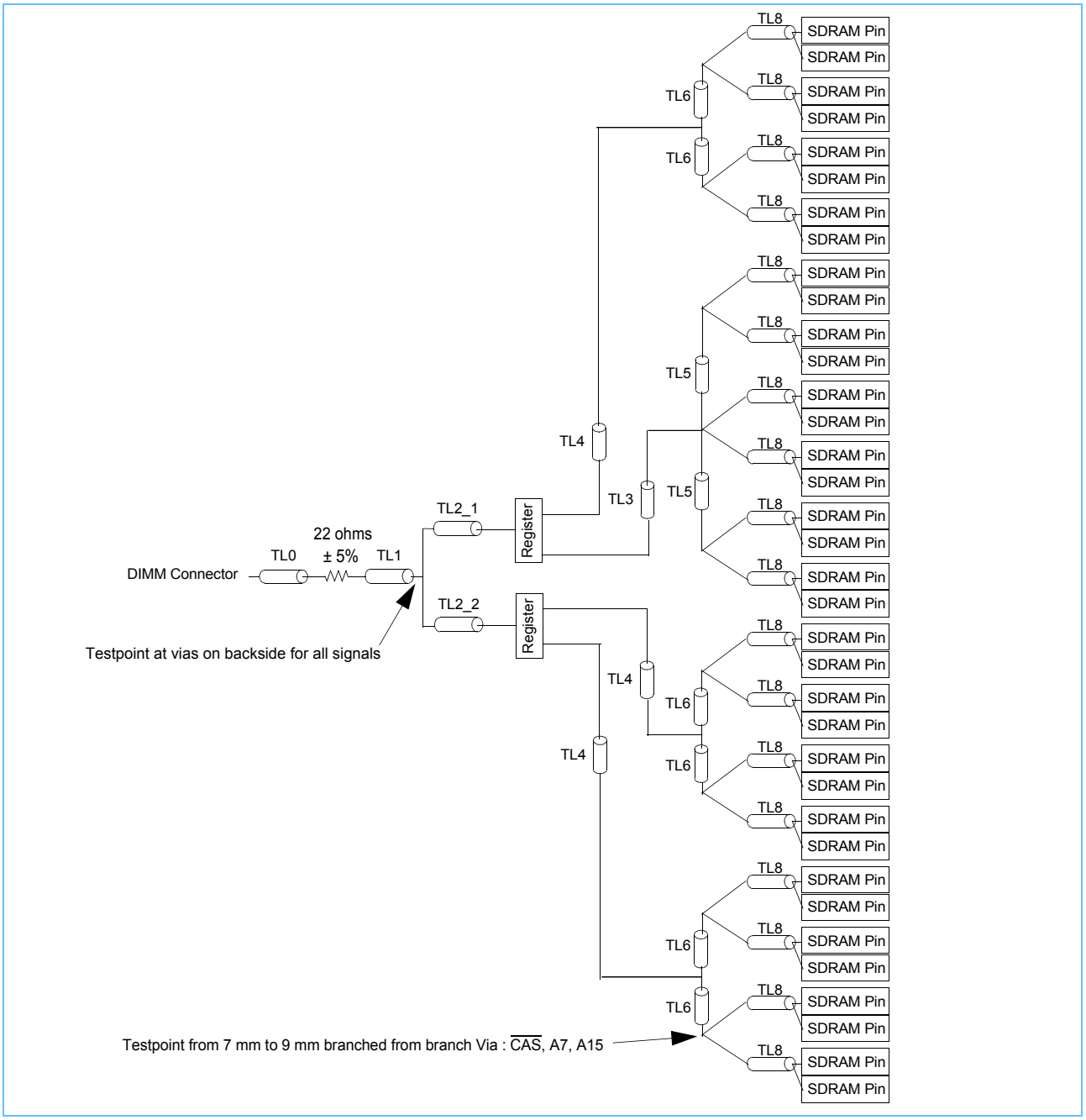
Raw Card	TL0		TL1		TL2		TL0 + TL1 + TL2		TL3		TL4		TL5		TL6		TL7		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
N	3.1	4.1	20.0	28.0	0	2.2	24.0	34.0	54.0	58.0	58.0	62.0	13.0	13.2	33.9	34.1	1.5	3.5	1

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimete

Petitioners
Ex. 1066, p. 81

Net Structure Routing for Address and Command (Raw Card P)

A[15:0], BA[2:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$



Trace Lengths for Address and Command Net Structure (Raw Card P)

A[15:0], BA[2:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$

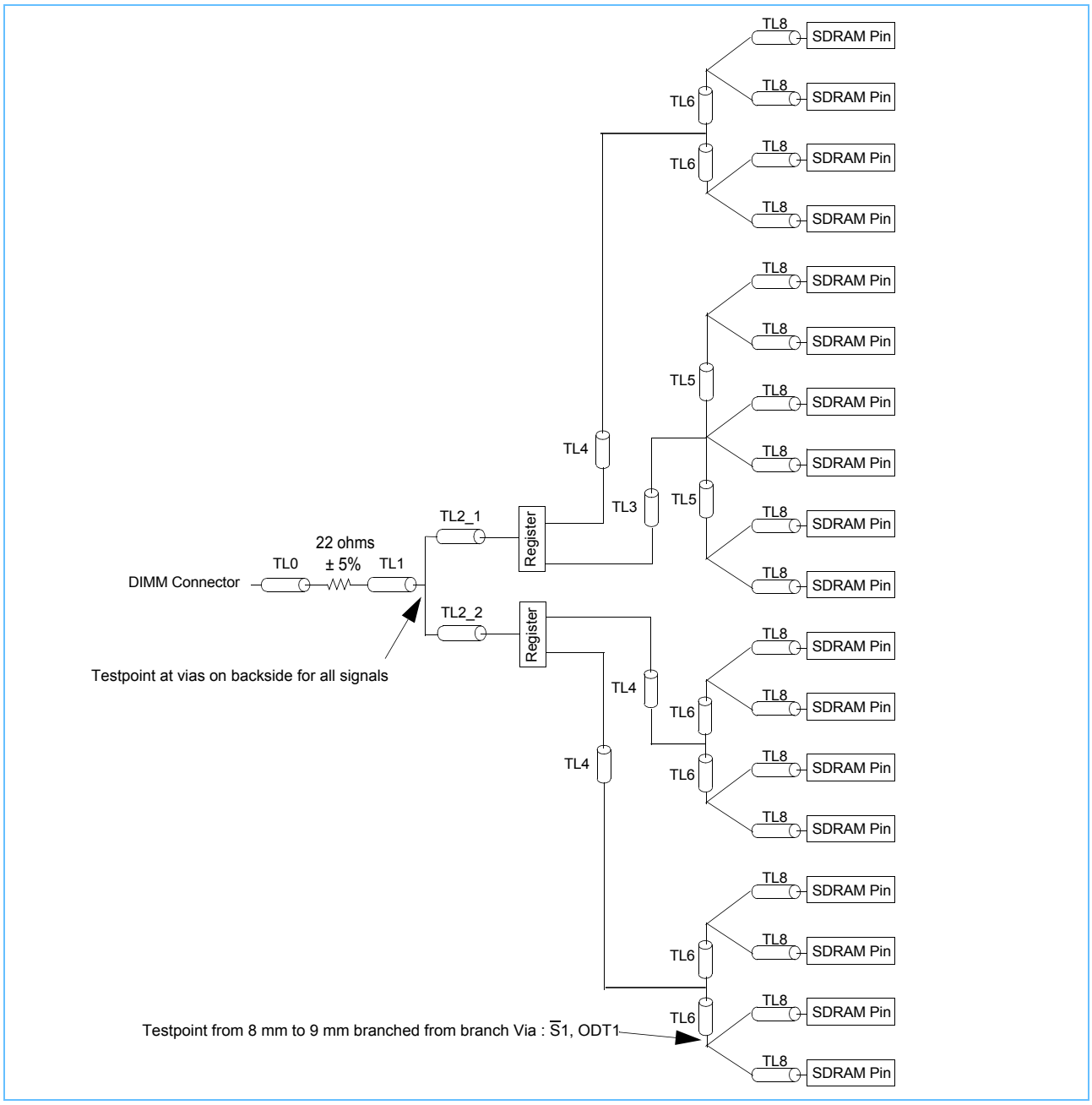
Raw Card	TL0		TL1		TL0+TL1		TL2_1		TL2_2		TL0+TL1+ TL2(_1 or_2)		TL3		TL4		TL5		TL6		TL8		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
P	3.6	4.4	9.3	10.1	13.6	13.7	0.4	42.1	0.4	42.1	14.0	55.8	24.9	25.0	59.9	60.0	14.9	15.0	7.9	8.0	0.9	8.7	1
	3.6	3.7	20.0	20.1	23.6	23.7	32.0	32.1	32.0	32.1	55.6	55.8	24.9	25.0	59.9	60.0	14.9	15.0	7.9	8.0	0.9	8.7	1,2

1. All distances are given in millimeters and must be kept within a toleranc
2. Applied only for A8,A9,A12,A14 and A15

Petitioners
Ex. 1066, p. 82

Net Structure Routing for Control (Raw Card P)

$\overline{S}$[1:0], CKE[1:0], ODT[1:0]



Trace Lengths for Control Net Structure (Raw Card P)

$\overline{S}$[1:0], CKE[1:0], ODT[1:0]

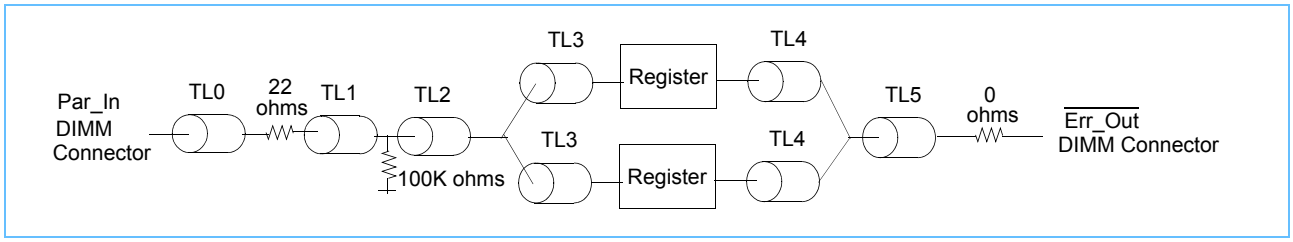
Raw Card	TL0		TL1		TL0+TL1		TL2_1		TL2_2		TL0 + TL1 + TL2(_1 or_2)		TL3		TL4		TL5		TL6		TL8		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
P	3.6	4.4	8.6	9.5	13.1	13.2	0.4	42.1	0.4	42.1	13.5	55.3	44.9	45.0	79.9	80.0	14.9	15.0	7.9	8.0	2.7	7.5	1

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.

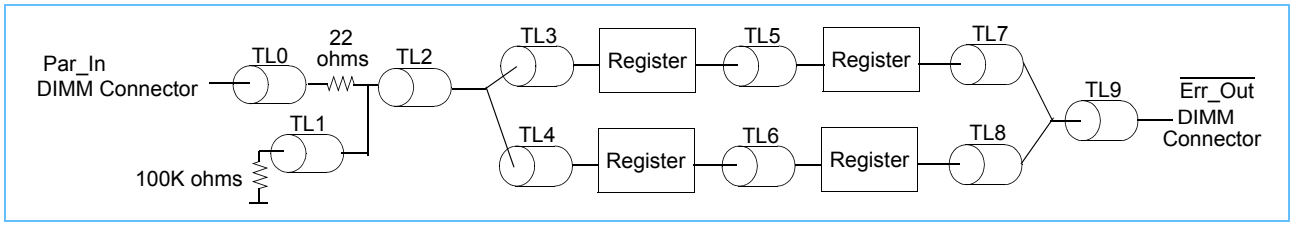
Petitioners
Ex. 1066, p. 83

Address and Command Parity Net Structures

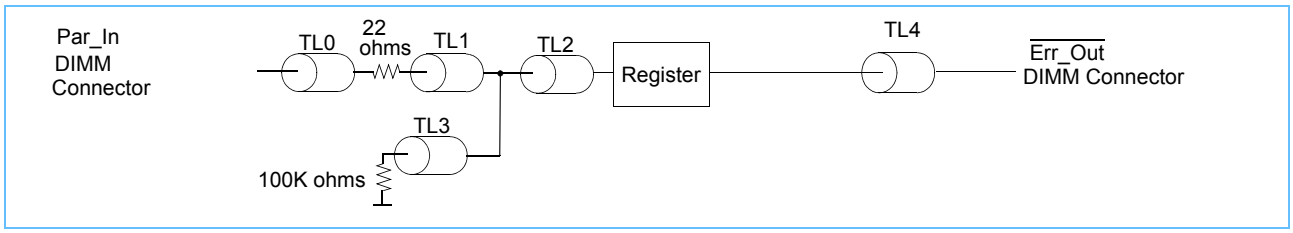
Net Structure Routing for Address and Command Parity (Raw Card D)



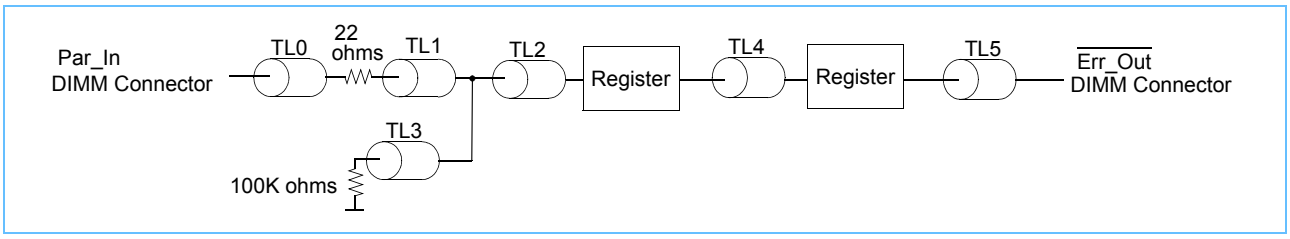
Net Structure Routing for Address and Command Parity (Raw Card E, N)



Net Structure Routing for Address and Command Parity (Raw Card F)

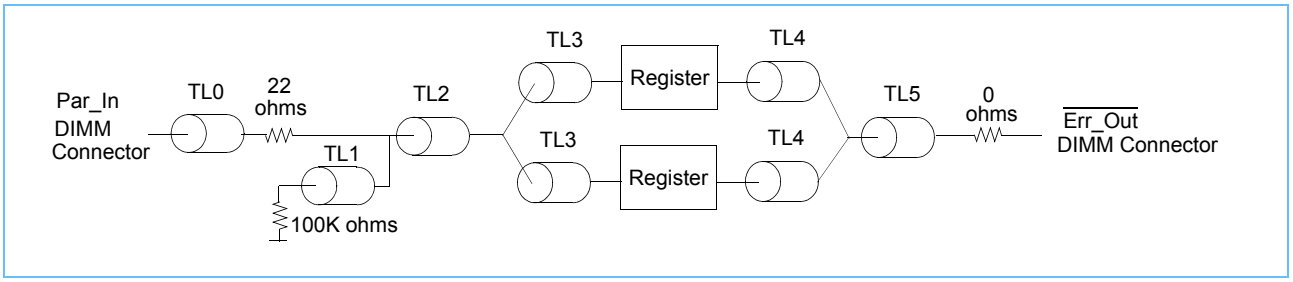


Net Structure Routing for Address and Command Parity (Raw Card G,H, J)

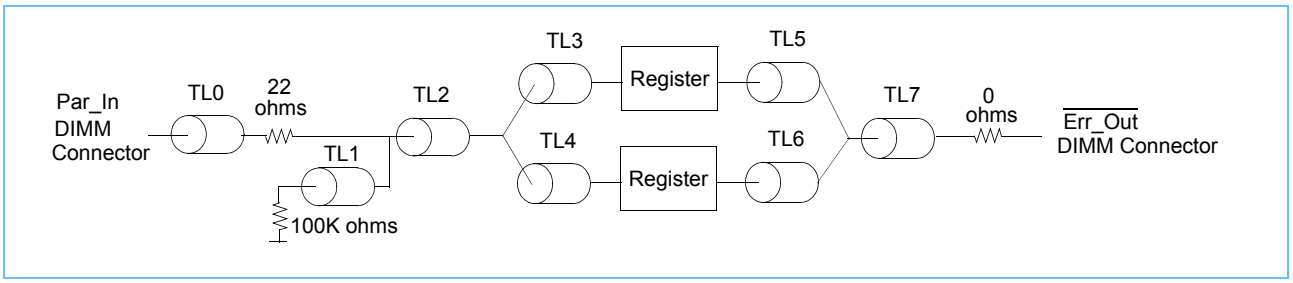


Petitioners
Ex. 1066, p. 84

Net Structure Routing for Address and Command Parity (Raw Card K)



Net Structure Routing for Address and Command Parity (Raw Card P)



Trace Lengths for Address and Command Parity Net Structure

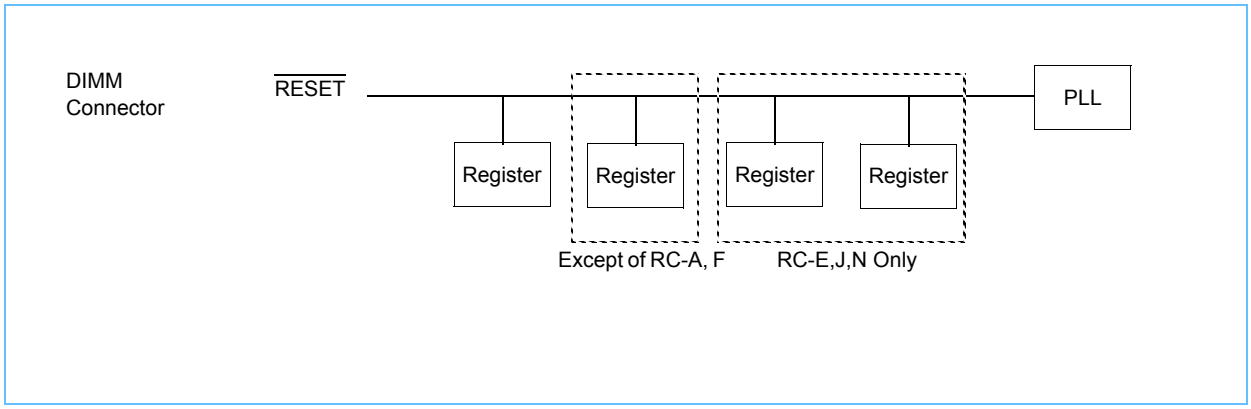
(Raw Cards D, E, F, G, H, J, K, N and P)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		TL9		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
D	10.5	10.6	1.0	1.1	19.5	19.6	12.1	12.2	12.1	12.2	31.0	31.1	-	-	-	-	-	-	-	-	1
E	4.1	4.2	1.5	1.6	1.4	1.5	4.3	4.4	9.9	10.0	15.7	15.8	34.4	34.5	4.4	4.5	13.5	13.6	4.0	4.1	1
F	3.7	3.8	1.2	1.3	13.9	14.0	2.2	2.3	30.3	30.4	-	-	-	-	-	-	-	-	-	-	1
G	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	8.8	8.9	39.1	39.2	-	-	-	-	-	-	-	-	1
H	6.7	6.8	19.8	19.9	13.0	13.1	2.0	2.1	9.0	9.1	36.7	36.8	-	-	-	-	-	-	-	-	1
J	6.2	6.3	1.5	1.6	24.0	24.1	2.1	2.2	15.0	15.1	16.5	16.6	38.0	38.1	4.4	4.5	13.5	13.6	4.0	4.1	1
K	3.6	3.7	1.0	1.1	33.0	33.1	0.4	0.5	0.4	0.5	33.0	33.1	3.7	3.8	-	-	-	-	-	-	1
N	3.5	3.6	3.8	3.9	8.6	8.7	2.5	2.6	11.4	11.5	23.5	23.6	8.4	8.5	0.6	0.7	15.3	15.4	29.2	29.3	1
P	3.6	3.7	1.0	1.1	7.6	7.7	0.4	0.5	40.4	40.5	28.8	28.9	10.4	10.5	0.7	0.8	-	-	-	-	1

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.

Petitioners
Ex. 1066, p. 85

$\overline{\text{RESET}}$ Net Structures



$\overline{\text{RESET}}$ Net Total Length

Raw Card	Total Net Length	Raw Card	Total Net Length
A,F	82	J	108
B, G	91	K	99
C, H	93	N	tbd
D	98	P	80
E	85		
Note: Net is wired with 100um width; only the total length all traces together (in millimeters) is specified and must be kept within a tolerance of ± 10%			

Petitioners
Ex. 1066, p. 86

Cross Section Recommendations

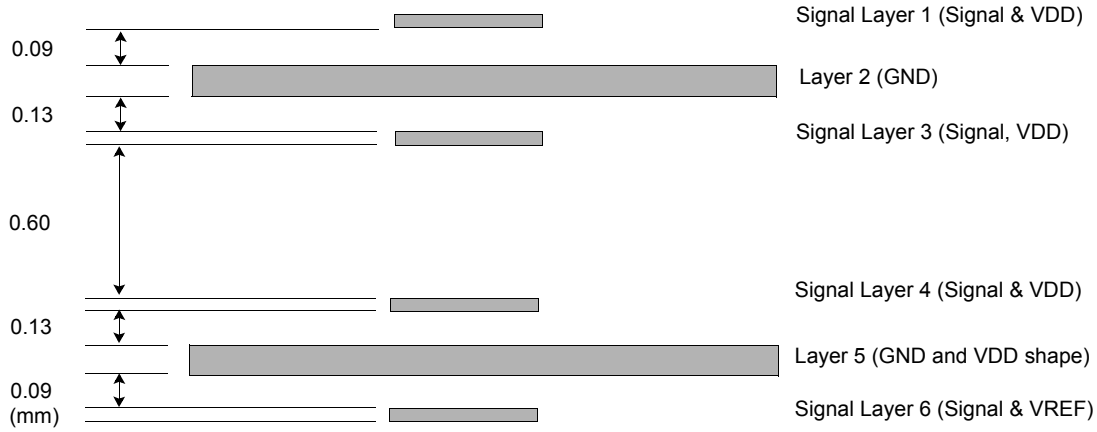
The DIMM printed circuit board design uses six layers of glass epoxy material. PCBs should contain solid ground plane and power plane layers as far as possible. The PCB stackup must be designed with 0.10 mm wide traces. Layer 2 and 4 are divided for the plane referencing (the signals on the signal layer and its referencing plane on GND/VDD layer are facing each other).

Note: The PCB edge connector contacts shall be gold-plated and not chamfered.

PCB Electrical Specifications

Parameter	Min	Max	Units
Trace velocity: S0 (outer layers, 0.10 mm wide single trace)	5.5	6.7	ps/mm
Trace velocity: S0 (inner layers, 0.10 mm wide single trace)	6.5	7.6	ps/mm
Trace impedance: Z_0 (all layers, 0.10 mm wide single trace)	54	66	Ohms

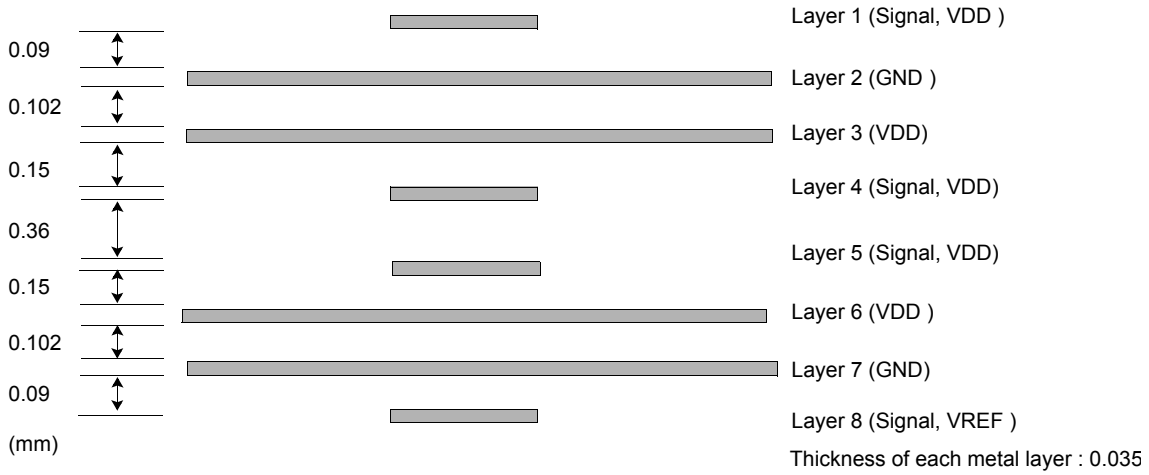
Example Six Layer Stackup for Raw Card A, B, C, F, G and H



Note: This diagram is intended as an example only. Each DIMM manufacturer can determine the thickness of their layers based on their own impedance calculations.

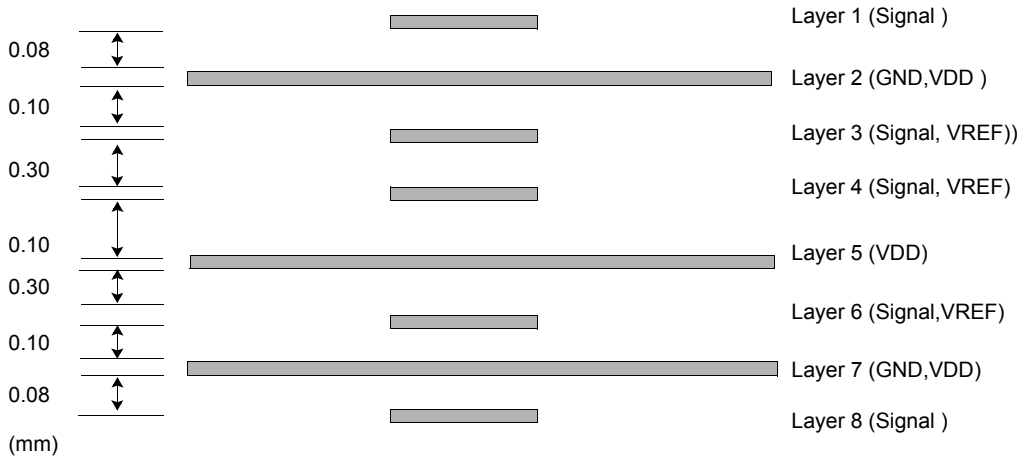
Petitioners
Ex. 1066, p. 87

Example Eight Layer Stackup for Raw Card D



Note: This diagram is intended as an example only. Each DIMM manufacturer can determine the thickness of their layers based on their own impedance calculations.

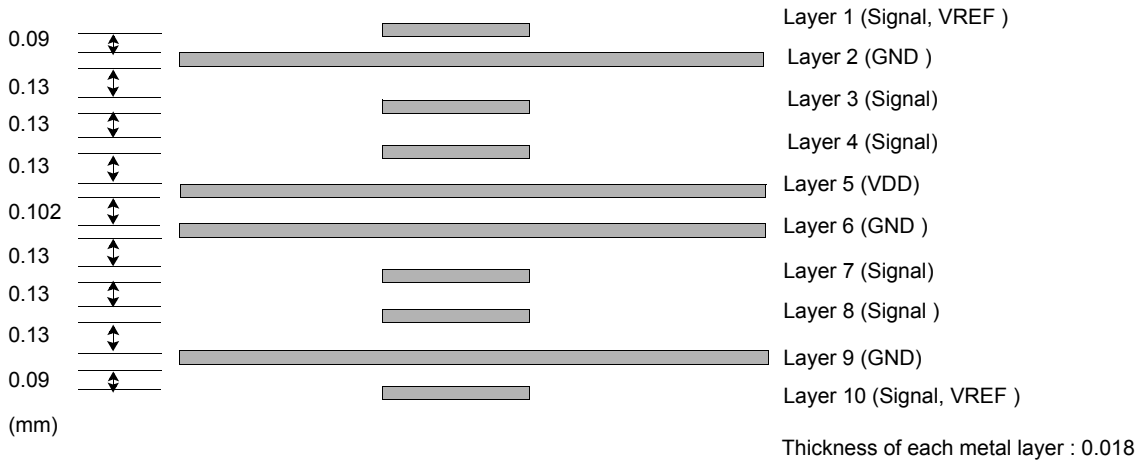
Example Eight Layer Stackup for Raw Card E and K



Note: This diagram is intended as an example only. Each DIMM manufacturer can determine the thickness of their layers based on their own impedance calculations.

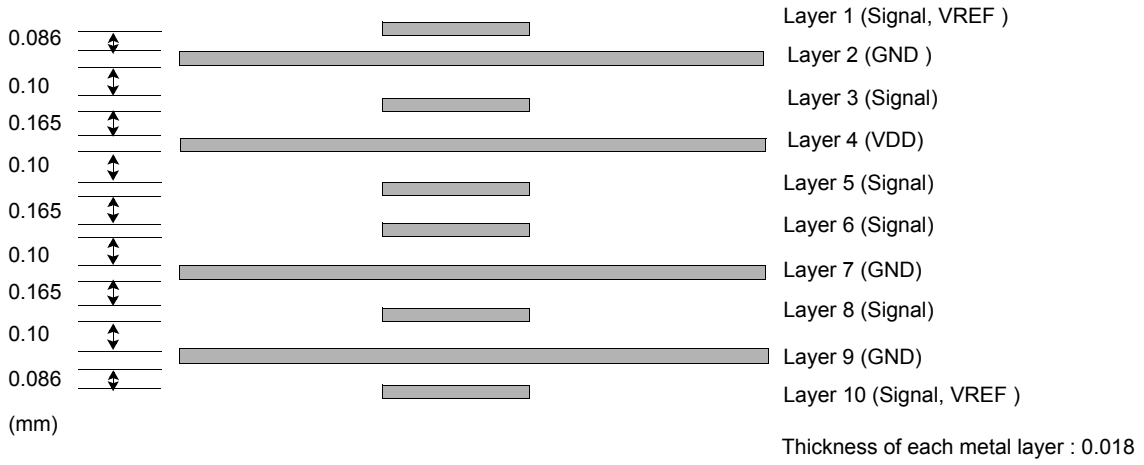
Petitioners
Ex. 1066, p. 88

Example Ten Layer Stackup for Raw Card J, M, N



Note: This diagram is intended as an example only. Each DIMM manufacturer can determine the thickness of their layers based on their own impedance calculations.

Example Ten Layer Stackup for Raw Card P



Note: This diagram is intended as an example only. Each DIMM manufacturer can determine the thickness of their layers based on their own impedance calculations.

Impedance Measurement Coupons

In order to allow DIMM card manufacturers to verify and monitor the trace impedance (Zo) listed above, measurement coupons have been added to the panels only (not the DIMM raw cards). A Time Domain Reflectometer (T.D.R.) should be used to perform these measurements before DIMM assembly.

Petitioners
Ex. 1066, p. 89

Timing Budget

The post-register timings on the Registered DIMMs are critical. The following table describes a preliminary post-register timing budget for a typical DDR2 PC2-3200/PC2-4200 Registered DIMM. This method is 'Time to Vm' that uses the register timing into its specified test load (instead of tCO, open circuit) and adds or subtracts the timing into the SDRAM net and loads.

Example DIMM Post-Register Timing (PC2-3200/PC2-4200, assumptions: 10/8 loads)

Parameter	Definition	Time (ns) Setup PC2-3200	Time (ns) Hold PC2-3200	Time (ns) Setup PC2-4200	Time (ns) Hold PC2-4200	Notes
tCLK (Clock Cycle Time)	Design point	5.000	NA	3.750	NA	
tPDM (Register Clk -> Y)	Register spec value for the delay from the register input rising clock edge (crossover of CK and /CK) to the output crossing Vtt at the Test Load (350ps transmission line delay, 30 pF to Gnd, 1K ohms pullup/pulldown to Gnd/Vdd)	-2.150	1.410	-2.150	1.410	1,2
tSS (S.S.adder)	Register spec value: tPDMSS-tPDM	-0.200	NA	-0.200	NA	1,2
tNETDELAY (Flight Time)	Delta between the time signal register drives reaches the SDRAM input via actual DIMM net structure and the time signal register drives reaches the test point of test load via test net structure. The measuremet points are as follow. Setup : Time delta between the time the signal reaches the AC level on net structure and the Vref level on test load. Hold : Time delta between the time the signal reaches the DC level on net structure and the Vref level on test load. tNETDELAY includes ISI.	-0.460	-0.360	-0.460	-0.360	1,2,3
tREG (Reg Clock Shift)	Accounts for the clock shift across the clocks to the registers due to wiring and register input cap deltas	-0.100	-0.100	-0.100	-0.100	1
tIS/IH (DRAM Setup/Hold)	DRAM spec for basic setup and hold at the SDRAM inputs.	-0.350	-0.475	-0.250	-0.375	1,4
Derating	Compensation value of delta tIS/tIH for various slew rate of SDRAM inputs related to CK, $\overline{CK}$ differential Slew Rate	-0.067	-0.045	-0.067	-0.045	7
tSKEW (Clock jitter/skew)	PLL spec for Period jitter and output clock skew plus the delta across the card due to wiring & SDRAM cap deltas	-0.200	-0.160	-0.200	-0.160	1,5
tXTALK (Crosstalk Adder)	Derived from simulation of address/control nets	0	0	0	0	6
Register Clock Offset	Adjusted clock arrival to register(s) to help setup or hold	0	0	0	0	
Margin	The clock cycle time (tCLK) minus the contributors above	1.473	0.270	0.323	0.370	

1. The timing values shown are consistent with registers, PLLs and DRAMs available at the time this specification was written. All devices must meet the combined delay values and ensure positive margin, although the specific delay value for each term can vary.
2. The timing values for tNETDELAY, tPDM, and tSS, when added together, define the overall delay from clock at the register to the time when the last re-driven signal arrives at the SDRAM (setup time), or earliest re-driven signal changes state after clock (hold time).
3. Maximum netdelay is simulated with slow register parameters and measured to the last DRAM reaching derating values. Minimum netdelay is simulated with fast register parameters and measured to the first SDRAM input signal approaching derating values. Each simulation has to assume the respective worst case PCB, net length and SDRAM package parasitics and the input capacitance parameters.
4. Assumed value for fast slew rate (T.B.D now)
5. See the tables below.
6. Crosstalk adder is included in tNETDELAY simulation number
7. Derating number should be referred to derating table. This Setup derating example of 67 is for 1.5V/ns for input, 2V/ns for Differntial Clock case. This Hold derating example of 45 is for 2.0V/ns for input, 2V/ns for Differntial Clock case.

Petitioners
Ex. 1066, p. 90

Example DIMM Post-Register Timing (PC2-5300, assumptions: 10/8 loads)

Parameter	Definition	Time (ns) Setup PC2-5300	Time (ns) Hold PC2-5300	Time (ns) Hold PC2-3200 Backward Compatibility	Notes
tCLK (Clock Cycle Time)	Design point	3.000	NA	NA	
tPDM (Register Clk -> Y)	Register spec value for the delay from the register input rising clock edge (crossover of CK and /CK) to the output crossing Vtt at the Test Load (350ps transmission line delay, 30 pF to Gnd, 1K ohms pullup/pulldown to Gnd/Vdd)	-1.900	1.200	1.200	1,2
tSS (S.S.adder)	Register spec value: tPDMSS-tPDM	-0.100	NA	NA	1,2
tNETDELAY (Flight Time)	Delta between the time signal register drives reaches the SDRAM input via actual DIMM net structure and the time signal register drives reaches the test point of test load via test net structure. The measuremet points are as follow. Setup : Time delta between the time the signal reaches the AC level on net structure and the Vref level on test load. Hold : Time delta between the time the signal reaches the DC level on net structure and the Vref level on test load. tNETDELAY includes ISI.	-0.460	-0.360	-0.360	1,2,3
tREG (Reg Clock Shift)	Accounts for the clock shift across the clocks to the registers due to wiring and register input cap deltas	-0.100	-0.100	-0.100	1
tIS/IH (DRAM Setup/Hold)	DRAM spec for basic setup and hold at the SDRAM inputs.	-0.200	-0.275	-0.475	1,4
Derating	Compensation value of delta tIS/tIH for various slew rate of SDRAM inputs related to CK, $\overline{CK}$ differential Slew Rate	-0.067	-0.045	-0.045	7
tSKEW (Clock jitter/skew)	PLL spec for Period jitter and output clock skew plus the delta across the card due to wiring & SDRAM cap deltas	-0.150	-0.130	-0.130	1,5
tXTALK (Crosstalk Adder)	Derived from simulation of address/control nets	0	0	0	6
Register Clock Offset	Adjusted clock arrival to register(s) to help setup or hold	0	0	0	
Margin	The clock cycle time (tCLK) minus the contributors above	0.023	0.290	0.090	

1. The timing values shown are consistent with registers, PLLs and DRAMs available at the time this specification was written. All devices must meet the combined delay values and ensure positive margin, although the specific delay value for each term can vary.
2. The timing values for tNETDELAY, tPDM, and tSS, when added together, define the overall delay from clock at the register to the time when the last re-driven signal arrives at the SDRAM (setup time), or earliest re-driven signal changes state after clock (hold time).
3. Maximum netdelay is simulated with slow register parameters and measured to the last DRAM reaching derating values. Minimum netdelay is simulated with fast register parameters and measured to the first SDRAM input signal approaching derating values. Each simulation has to assume the respective worst case PCB, net length and SDRAM package parasitics and the input capacitance parameters.
4. Assumed value for fast slew rate (T.B.D now)
5. See the tables below.
6. Crosstalk adder is included in tNETDELAY simulation number
7. Derating number should be referred to derating table. This Setup derating example of 67 is for 1.5V/ns for input, 2V/ns for Differntial Clock case. This Hold derating example of 45 is for 2.0V/ns for input, 2V/ns for Differntial Clock case.

Petitioners
Ex. 1066, p. 91

Example DIMM Post-Register Timing (PC2-6400, assumptions: 10/8 loads)

Parameter	Definition	Time (ns) Setup PC2-6400	Time (ns) Hold PC2-6400	Time (ns) Hold PC2-3200 Backward Compatibility	Notes
tCLK (Clock Cycle Time)	Design point	2.500	NA	NA	
tPDM (Register Clk -> Y)	Register spec value for the delay from the register input rising clock edge (crossover of CK and /CK) to the output crossing Vtt at the Test Load (350ps transmission line delay, 30 pF to Gnd, 1K ohms pullup/pulldown to Gnd/Vdd)	-1.500	1.100	1.200	1,2
tSS (S.S.adder)	Register spec value: tPDMSS-tPDM	-0.100	NA	NA	1,2
tNETDELAY (Flight Time)	Delta between the time signal register drives reaches the SDRAM input via actual DIMM net structure and the time signal register drives reaches the test point of test load via test net structure. The measuremet points are as follow. Setup : Time delta between the time the signal reaches the AC level on net structure and the Vref level on test load. Hold : Time delta between the time the signal reaches the DC level on net structure and the Vref level on test load. tNETDELAY includes ISI.	-0.432	-0.336	-0.360	1,2,3
tREG (Reg Clock Shift)	Accounts for the clock shift across the clocks to the registers due to wiring and register input cap deltas	-0.100	-0.100	-0.100	1
tIS/IH (DRAM Setup/Hold)	DRAM spec for basic setup and hold at the SDRAM inputs.	-0.150	-0.250	-0.475	1,4
Derating	Compensation value of delta tIS/tIH for various slew rate of SDRAM inputs related to CK, $\overline{CK}$ differential Slew Rate	-0.027	+0.125	-0.045	7
tSKEW (Clock jitter/skew)	PLL spec for Period jitter and output clock skew plus the delta across the card due to wiring & SDRAM cap deltas	-0.150	-0.130	-0.130	1,5
tXTALK (Crosstalk Adder)	Derived from simulation of address/control nets	0	0	0	6
Register Clock Offset	Adjusted clock arrival to register(s) to help setup or hold	0	0	0	
Margin	The clock cycle time (tCLK) minus the contributors above	0.041	0.359	0.090	

1. The timing values shown are consistent with registers, PLLs and DRAMs available at the time this specification was written. All devices must meet the combined delay values and ensure positive margin, although the specific delay value for each term can vary.
2. The timing values for tNETDELAY, tPDM, and tSS, when added together, define the overall delay from clock at the register to the time when the last re-driven signal arrives at the SDRAM (setup time), or earliest re-driven signal changes state after clock (hold time).
3. Maximum netdelay is simulated with slow register parameters and measured to the last DRAM reaching derating values. Minimum netdelay is simulated with fast register parameters and measured to the first SDRAM input signal approaching derating values. Each simulation has to assume the respective worst case PCB, net length and SDRAM package parasitics and the input capacitance parameters.
4. Assumed value for fast slew rate (T.B.D now)
5. See the tables below.
6. Crosstalk adder is included in tNETDELAY simulation number
7. Derating number should be referred to derating table. This Setup derating example of 67 is for 1.5V/ns for input, 2V/ns for Differntial Clock case. This Hold derating example of 45 is for 2.0V/ns for input, 2V/ns for Differntial Clock case.

Petitioners
Ex. 1066, p. 92

DIMM Clock Jitter and Skew (tSKEW) for PC2-4200/PC2-3200

Parameter	tSKEW for Setup	tSKEW for Hold	Units	Note
DIMM PLL Period Jitter: tjit (per)	0.040	N/A	ns	
DIMM PLL Output Clock Skew: tsk (o)	0.040	0.040	ns	
DIMM PLL Dynamic Phase Offset	0.050	0.050	ns	
DIMM Clock Net Skew	0.070	0.070	ns	1
Total tSKEW	0.200	0.160	ns	
1. Accounts for the clock shift across the SDRAMs due to wiring & SDRAM capacitance deltas.				

DIMM Clock Jitter and Skew (tSKEW) for PC2-5300

Parameter	tSKEW for Setup	tSKEW for Hold	Units	Note
tjit(per) + t(DPO) + tSK(o)	0.080	N/A	ns	
t(DPO) + tSK(o)	N/A	0.060	ns	
DIMM Clock Net Skew	0.070	0.070	ns	1
Total PLL SKEW	0.150	0.130	ns	
1. Accounts for the clock shift across the SDRAMs due to wiring & SDRAM capacitance deltas.				

DIMM Clock Jitter and Skew (tSKEW) for PC2-6400

Parameter	tSKEW for Setup	tSKEW for Hold	Units	Note
tjit(per) + t(DPO) + tSK(o)	0.080	N/A	ns	
t(DPO) + tSK(o)	N/A	0.060	ns	
DIMM Clock Net Skew	0.070	0.070	ns	1
Total PLL SKEW	0.150	0.130	ns	
1. Accounts for the clock shift across the SDRAMs due to wiring & SDRAM capacitance deltas.				

Petitioners
Ex. 1066, p. 93

Serial Presence Detect Definition

The Serial Presence Detect (SPD) function MUST be implemented on the PC2-6400 DDR2 SDRAM R-DIMM. The component used and the data contents must adhere to the most recent version of the JEDEC DDR2 SDRAM SPD Specifications. Please refer to this document for all technical specifications and requirements of the serial presence detect devices. Please refer to this document for all technical specifications and requirements of the Serial Presence Detect devices (Refer to JEDEC ballot JC-42.5-99-129 item 894A for SPD field definitions)

The following table is intended to be an **example** of a typical PC2-6400 RDIMM. SPD values indicating different Min-DIMM performance characteristics will be utilized based on specific characteristics of the SDRAMs or DIMMs. This example assumes:

- Module Organization: 512MB (64Mx72)
- Device Composition: 64Mx8
- Device Package: FBGA
- Module Physical Ranks: 1
- CAS latency: 6(DDR2-800)

Serial Presence Detect Example Raw Card Version A (1 of 3)

64M x 72 DDR2

Byte #	Function Described	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
0	Number of Serial PD Bytes written during module production	128	80	1
1	Total number of Bytes in Serial PD device	256	08	2
2	Fundamental Memory Type (FPM, EDO, SDRAM, DDR, DDR2,....)	DDR2 SDRAM	08	
3	Number of Row Addresses on this assembly	14	0E	
4	Number of Column Addresses on this assembly	10	0A	
5	Number of DIMM Ranks	Module height: 30mm Planar, Card on Card: no 1 rank	60	
6	Data Width of this assembly	x72	48	
7	Reserved	Undefined	00	
8	Voltage Interface Level of this assembly	SSTL 1.8V	05	
9	SDRAM Cycle time at Maximum Supported $\overline{\text{CAS}}$ Latency (CL), CL=X	2.5ns	25	3
10	SDRAM Access from Clock	±0.40ns	45	
11	DIMM configuration type (Non-parity, Parity or ECC)	ECC	02	
12	Refresh Rate/Type	7.8µs	82	3,4
13	Primary SDRAM Width	x8	08	
14	Error Checking SDRAM Width	x8	08	
15	Reserved	Undefined	00	
16	SDRAM Device Attributes: Burst Lengths Supported	4, 8	0C	
17	SDRAM Device Attributes: Number of Banks on SDRAM Device	4	04	3

Petitioners
Ex. 1066, p. 94

Serial Presence Detect Example Raw Card Version A (2 of 3)

64M x 72 DDR2

Byte #	Function Described	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
18	SDRAM Device Attributes: $\overline{CAS}$ Latency	6,5	60	3
19	DIMM Mechanical Characteristics	Less than 4.1 mm	01	3
20	DIMM Type Information	Regular RDIMM (133.35mm)	01	3
21	SDRAM Module Attributes	normal DIMM	00	
22	SDRAM Device Attributes: General	Support 50 ohms ODT	02	3
23	Minimum Clock Cycle at CLX-1	2.5ns	25	3
24	Maximum Data Access Time (tAC) from Clock at CLX-1	±0.40ns	40	3
25	Minimum Clock Cycle at CLX-2	3.0ns	30	3
26	Maximum Data Access Time (tAC) from Clock at CLX-2	±0.45ns	45	3
27	Minimum Row Precharge Time (tRP)	12.5ns	32	3
28	Minimum Row Active to Row Active delay (tRRD)	7.5ns	1E	3
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay (tRCD)	12.5ns	32	3
30	Minimum Active to Precharge Time (tRAS)	45.0ns	2D	3
31	Module Rank Density	512MB	80	
32	Address and Command Input Setup Time Before Clock (tIS)	0.15ns	15	3
33	Address and Command Input Hold Time After Clock (tIH)	0.25ns	25	3
34	Data Input Setup Time Before Clock (tDS)	0.10ns	10	3
35	Data Input Hold Time After Clock (tDH)	0.15ns	15	3
36	Write recovery time (tWR)	15.0ns	3C	3
37	Internal write to read command delay (tWTR)	7.5ns	1E	3
38	Internal read to precharge command delay (tRTP)	7.5ns	1E	3
39	Memory Analysis Probe Characteristics	Undefined	00	
40	Extention of Byte 41 tRC and Byte 42 tRFC	The number below a decimal point of tRC and tRFC are 0, tRFC is less than 256ns	00	3
41	SDRAM Device Minimum Active to Active/Auto Refresh Time (tRC)	57.0ns	39	3
42	SDRAM Device Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC)	105.0ns	69	3
43	SDRAM Device Maximum device cycle time (tCKmax)	8.0ns	80	3
44	SDRAM Device Maximum skew between DQS and DQ signals	0.240ns	18	3
45	SDRAM Device Maximum Read Data Hold Skew Factor (tQHS)	0.340ns	22	3
46	PLL Relock Time	6.0µs	06	

Petitioners
Ex. 1066, p. 95

Serial Presence Detect Example Raw Card Version 'A' (3 of 3)

64M x 72 DDR2

Byte #	Function Described	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
47-xx	IDD in SPD(IDD in SPD TG is working to defiene this standard, and a discussion result will be added later)	Undefined	00	
xx-61	Reserved	Undefined	00	
62	SPD Revision	1.2	12	
63	Checksum for Bytes 0-62	Checksum Data	cc	
64-71	Manufacturer's JEDEC ID Code			
72	Module Manufacturing Location			
73 - 90	Module Part Number			5
91 - 92	Module Revision Code			5
93 - 94	Module Manufacturing Date	Year/Week Code	yyww	5
95 - 98	Module Serial Number	Serial Number	ssssssss	
99 - 127	Manufacturer's Specific Data	Undefined	00	5
128 - 255	Open for Customer Use	Undefined		

1. This will typically be programmed as 128 Bytes.
2. This will typically be programmed as 256 Bytes.
3. From Datasheet.
4. High order bit is Self Refresh "flag". If set to "1", the assembly supports self refresh.
5. These are optional, in accordance with the JEDEC spec.

Serial Presence Detect Component Specification

The DIMM vendor should ensure that the lower 128 bytes are software write protectable. A write to the SPD with address "0 1 1 0 SA2 SA1 SA0 0", where SA(2:0) are the SPD addresses on the DIMM connector, will prevent all future writes to the lower 128 bytes of the SPD. The software write protect feature is "write once", but should be done by the BIOS at each power up, to prevent corruption of the lower 128 bytes of the SPD.

Petitioners
Ex. 1066, p. 96

DDR2 DIMM Label Format:

The following label shall be applied to all DDR2 memory modules to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A minimum font size of 8 points should be used, and the number can be printed in one or more rows on the label. Hyphens may be dropped when lines are split, or when font changes sufficiently separate fields.

ggggg eRxff PC2-wwwwm-abc-dd-ef

Where:

ggggg = Module total capacity, in bytes
- 256MB, 512MB, 1GB, 2GB, 4GB, etc.

eR = Number of ranks of memory installed
- 1R = 1 rank of DDR2 SDRAM installed
- 2R = 2 ranks
- 4R = 4 ranks

xff = Device organization (bit width) of DDR2 SDRAMs used on this assembly
- x4 = x4 organization (4 DQ lines per SDRAM)
- x8 = x8 organization
- x16 = x16 organization

wwww = Module bandwidth in MB/s
- 3200 = 3.20 GB/s
- 4200 = 4.26 GB/s
- 5300 = 5.33 GB/s
- 6400 = 6.40 GB/s

m = Module Type
- E = Unbuffered DIMM ("UDIMM"), with ECC (x72 bit module data bus)
- F = Fully Buffered DIMM ("FB-DIMM")
- M = Micro-DIMM
- N = Mini-Registered DIMM ("Mini-RDIMM"), no address/command parity function
- P = Registered DIMM ("RDIMM"), with address/command parity function
- R = RDIMM, no address/command parity function
- S = Small Outline DIMM ("SO-DIMM")
- U = Unbuffered DIMM ("UDIMM"), no ECC (x64 bit module data bus)

a = DDR2 SDRAM CAS Latency, in clocks at maximum operating frequency

b = DDR2 SDRAM minimum tRCD specification, in clocks at maximum operating frequency

c = DDR2 SDRAM minimum tRP specification, in clocks at maximum operating frequency

dd = JEDEC SPD Revision Encoding and Additions level used on this DIMM

e = Reference design file used for this design (if applicable)
- A = Reference design for raw card ’A’ is used for this assembly
- B = Reference design for raw card ’B’ is used for this assembly
- Z = None of the reference designs were used for this assembly

f = Revision number of the reference design used
- 0 = Initial release
- 1 = First revision
- 2 = Second revision
- P = Pre-release or Engineering sample
- Z = To be used when field e = Z

Petitioners
Ex. 1066, p. 97

Example:

1GB 2Rx4 PC2-3200R-333-11-E2

is a 1GB DDR2 Registered DIMM, without address/command parity function, using 2 ranks of x4 SDRAMs operational to PC2-3200 performance with CAS Latency = 3, t_{RCD} = 3, t_{RP} = 3, using JEDEC SPD revision 1.1, raw card reference design file E revision 2 used for the assembly

4GB 4Rx4 PC2-4200P-444-12-M1

is a 4GB DDR2 Registered DIMM, with address/command parity function, using 4 ranks of x4 SDRAMs operational to PC2-4200 performance with CAS Latency = 4, t_{RCD} = 4, t_{RP} = 4, using JEDEC SPD revision 1.2, raw card reference design file M revision 1 used for the assembly

Petitioners
Ex. 1066, p. 98

DIMM Mechanical Specifications

JEDEC has standardized detailed mechanical information for the 240Pin DIMM family. This information can be accessed on the worldwide web as follows:

1. Go to JEDEC official site; http://www.jedec.org.
2. Click on 'Free Standards ' and enter the free download area.
3. Search by document number: 'MO-237' and download the PDF for this product family.
4. Or search by 'JEP95';'JEDEC Publication 95.' and open entire document,scroll down and select 'MO-237' to download the PDF for this product family.

Within MO-237, several DIMM thickness variations are defined. These variations are summarized in the table below, in conjunction with examples of the types of RDIMM components and assemblies that may be associated with each DIMM thickness range:

Maximum RDIMM Thickness	Comments
Less than or equal to 4.00 mm	Generally associated with DIMMs produced with devices that are 1.35 mm thick or less
> 4.00 mm and less than or equal to 6.75 mm	Generally associated with DIMMs produced with devices that are greater than 1.35 mm and less than or equal to 2.70 mm thick
> 6.75 mm and less than or equal to 7.55 mm	Generally associated with DIMMs produced with devices that are greater than 2.70 mm and less than or equal to 3.10 mm thick
> 7.55 mm	Intended to cover DIMMs produced with non-standard package thicknesses, card-on-card structures or alternate solutions

Note: Maximum DIMM thickness can be a measured maximum value, or can be calculated using the maximum component, card, label, and assembly process adders.

To enable systems to electronically detect DIMM thickness, SPD byte 19 is encoded with the RIDMM thickness value ranges in the table above. When used in conjunction with bytes 20-21 and 47-61, system operating conditions can be adjusted based on installed modules and projected power consumption.

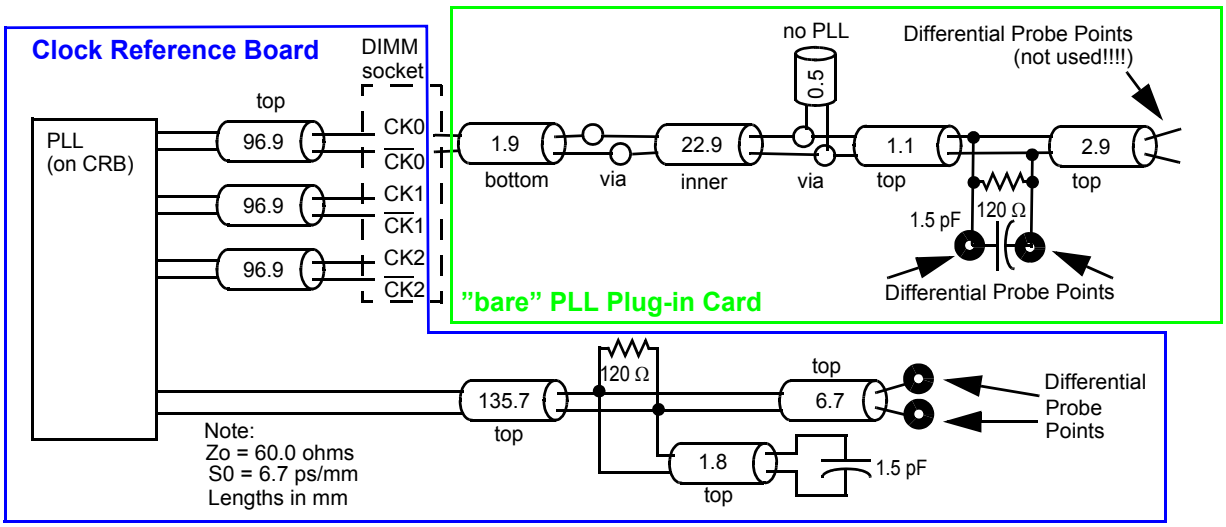
Petitioners
Ex. 1066, p. 99

Application Notes:

Clock Timing Methodology

Clock Reference Board

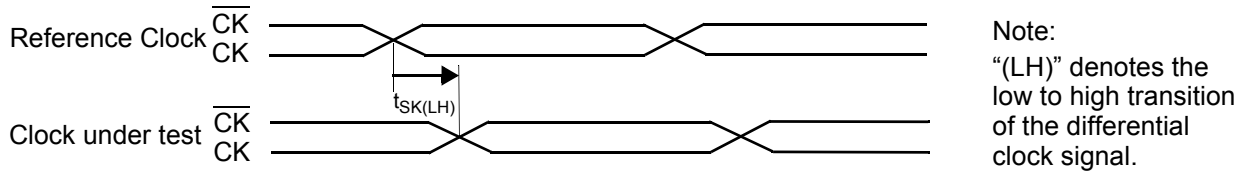
The clock net from the edge connector pins CK/$\overline{CK}$ to the PLL input balls of each RDIMM raw card is typically 25.4 mm. The Clock Reference Board ("CRB") (How can we refer to this board without it being formally standardized?) has three equal clock nets from its PLL outputs to the DIMM socket (CK0, CK1, CK2) and one "reference" clock net, which is longer and resembles the flight time of the above mentioned clock nets, the edge connector and the DIMM clock lead-in net. This net ends in a test point (through hole via); all measurements are done with respect to this test point..



One advantage of measuring all clocks on a DIMM with respect to the test point at the clock reference net is, that the disturbance of the skew by the probe does not shift the reference timing. (see DDR2 DIMM clock skew measurement procedure - see item JC45.1 #1394)

Skew Definition

Timing phase shift (skew) in two different DDR differential clock signals is always measured between the two crossing points of the two-clock pairs. If the clock crossing of the clock under test is later than the clock crossing of the reference clock, the skew t_{SK} is considered positive; if it is earlier, the skew is negative:



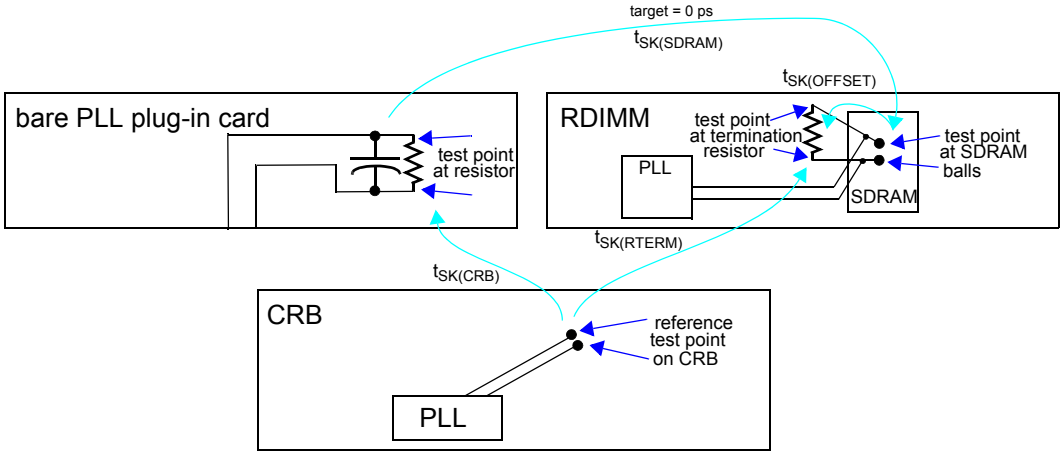
The clock nets on the RDIMM are designed so that the skew of the clock at the SDRAM balls with respect to the reference is nominally 0 ns. Under the assumption that the reference net on the CRB matches the delay of the clock lead-in length to the PLL, the clock at the PLL input balls and the clock at the SDRAM balls are

Petitioners
Ex. 1066, p. 100

also aligned. (Note however that the first condition is the overriding design objective.)
The clock arrival time at the PLL might vary slightly (sources of timing variation include PLL input capacitance, padding capacitor and termination resistor tolerances, and DIMM impedance variations), however the PLL feedback path may be adjusted such that the SDRAM input clock still aligns with the clock reference.
Due to these variations, it is possible that there will be a difference between the input of the PLL and the input of any of the SDRAMs on the card. The most important factor in clock measurements is to ensure consistent clock arrival times at the SDRAM.
The clock to the register should also be in phase with the SDRAM clock. The actual delay may vary as a result of the input capacitance of the SDRAMs, the register clock input capacitance, PLL output skew variations of the PCB parasitics. In the case when the register clocks arrive prior to the SDRAM input clock, this relationship may be adjusted by increasing the value of the register clock padding capacitor.

PLL plug-in card and "Normalized Skew"

Ideally one would use the CRB test point as reference for all timing measurements. However the variation between different reference boards seems to be substantial (+/- 30ps). It is therefor recommended that each board be measured/normalized using the "bare PLL plug-in card" supplied with each CRB. This card has a clock net that is very close in topology to the actual RDIMMs. It has only two passive components: the termination resistor at the end of the CK lead-in nets and a capacitor across it to resemble the input capacitance of the PLL. This card inherently is less subjective to variations. It is believed that the delay of the clock net on these cards is within +/- 5ps across one batch. To determine the skew of the CRB one would first measure the skew $t_{SK(CRB)}$ between the plug-in card (at the termination resistor) and the clock reference test point on the CRB.
The clock at the SDRAM balls should then have the same skew value $t_{SK(SDRAM)} = t_{SK(CRB)}$ to be considered to have a "normalized skew" of 0 ns.



Measuring the SDRAM skew at the termination resistor:

Unfortunately on most RDIMMs the balls of the SDRAM are not accessible for direct measurement. The closest feasible test point is at the termination resistor of that particular clock net, which is typically several millimeters away from the SDRAM balls. The skew $t_{SK(OFFSET)}$ between the SDRAM balls and the test point at the termination resistor can typically only be estimated by simulation. Each Raw Card should be provided with a set of estimated skew values $t_{SK(OFFSET)}$ for each termination resistor. (The skew values might be different for register, PLL and potentially for each DRAM). The procedure to determine the estimated skew is (I.E. WILL BE) outlined in the "DDR2 RDIMM clock skew measurement procedure" (JEP-TBD #1394). The target for the measured "normalized skew" $t_{SK(SDRAM)}$ between the test point on the plug-in card and the

Petitioners
Ex. 1066, p. 101

SDRAM is 0 ns. Expressed in measurable entities this becomes:

$$t_{SK(SDRAM)} = t_{SK(RTERM)} - t_{SK(OFFSET)} - t_{SK(CRB)} = 0 \text{ ns (Target)}$$

with:
tSK(SDRAM): “normalized skew”: skew between SDRAM balls and test point at bare PLL plug-in card ()
tSK(CRB): skew between bare PLL plug-in card and reference test point at CRB. (This is a charcteristric number for each CRB)
tSK(OFFSET): skew between test point at termination resistor and SDRAM balls (obtained by simulation; see table below)
tSK(RTERM): skew between termination resistor at DRAM and reference test point of CRB (this is the actually measured value, when evaluating a DIMM)

Skew Table (test point at termination resistor to device ball)

Table 1:

Raw Card	$t_{SK(OFFSET)}$			Notes
	SDRAMs	**Registers**	**PLL**	
A, F	110	0	0	1, 2
B, G	125	0	0	1, 2
C, H	80	0	0	1, 2
D	85	70	0	1, 2
E	100	0	0	1, 2
J	100	85	0	1, 2
K	90	0	0	1, 2
M	tbd	tbd	tbd	tbd
N	tbd	tbd	tbd	tbd
P	100	0	0	1, 2
.....				

1. Values in ps
2. These numbers were obtained by simulation assuming a diffrential probe with:1pF and 20 kohms at termination resistor and at test point of CRB

Petitioners
Ex. 1066, p. 102

Clock Timing Accuracy

There are several key contributors to the DRAM clock timing error:

Contributor to error	Δt	Notes
Variation of clock arrival time between individual DRAMs of a module (PLL output skew and clock net skew)	70 + 40	1, 2
Clock arrival time at the DRAMs (mean across all DRAMs on a card) with respect to the test point of the “bare PLL plug-in card”	tuning error tbd	1, 2
Half of total Jitter Envelope measured at any of the DRAMs on a card (PLL jitter plus crosstalk on card)	(40 + tbd) / 2	1
Error in simulating $t_{SK(OFFSET)}$	30	1
error margin of state-of-the-art equipment.	50	1
1. Values in ps 2. measured as mean value to eliminate jitter		

These three contributors shall be measured independently and on a reasonable amount of qualification samples. The worst-case timing error relevant for sage system operation can be expected to be the sum of all contributors.

Petitioners
Ex. 1066, p. 103

Reset usage

The $\overline{\text{RESET}}$ signal, wired to the Registered DIMM $\overline{\text{RESET}}$ pin, is tied to both the $\overline{\text{RST}}$ pin of Register(s) and OE pin of PLL.
Upon receipt of a low level on the $\overline{\text{RST}}$ pin of Register(s), the register(s) will do the following:
-Differential clock and data input receivers are disabled
-All internal registers will be cleared with the outputs of the registers forced low
Upon receipt of a low level on the OE pin of PLL, the PLL will enter a low power state, from which it can return to normal operation in only a few clock cycles. In this state, the primary power reduction results from the output clocks being held at a stable (low) level, with the PLL input receivers (clock input and feedback input) and feedback outputs remaining operational. Since the internal oscillator continues to operate, with a valid clock input and feedback path, the PLL will retain a lock to the input clock. The PLL is expected to draw tbd mA of current in this state, and 10 of the 11 clock terminators on the clock outputs, on a typical memory module, will also see no current flow.

The $\overline{\text{RESET}}$ is used in power up & initialization sequence and self refresh entry/exit sequence.
In power up & initialization sequence, $\overline{\text{RESET}}$ is used to ensure defined outputs from the register before a stable clock has been supplied. The detail sequence is as follows.
1. The system sets $\overline{\text{RESET}}$ at a valid low level.
2. The memory power supplies should be initialized according to the JEDEC-approved initialization sequence for DDRII SDRAMs.
3. The system should apply valid logic levels to all of the data inputs of the register (address and controls at the DIMM connector).
4. Stabilization of clocks to the PLL input
5. The system drives $\overline{\text{RESET}}$ to a valid high level
6. SDRAM preconditioning
In self refresh entry/exit sequence, $\overline{\text{RESET}}$ is used for the lowest possible power dissipation as follows.
Self Refresh Entry:
1. The system applies the Self Refresh Entry Command.
(CKE to Low, $\overline{\text{CS}}$ to Low, $\overline{\text{RAS}}$ to Low, $\overline{\text{CAS}}$ to Low, $\overline{\text{WE}}$ to High)
2. The system applies low levels to the input of the register (preferred state)
3. The system sets $\overline{\text{RESET}}$ to a logic 'low' level
4. The system clock is halted
5. The system may release all inputs to the memory module except of $\overline{\text{RESET}}$
Self Refresh Exit:
6. The system will re-start the clock
7. The system should apply valid logic levels to all of the data inputs of the register
8. Stabilization of clocks to the PLL input
9. The system drives $\overline{\text{RESET}}$ to a valid high level
10. SDRAM Self Refresh Exit
The 4, 6 and 8 can be omitted in case that the system clock is running through self refresh operation.

Petitioners
Ex. 1066, p. 104

4 Rank RDIMMs:

DDR2 Registered DIMMs with 4 ranks of memory per RDIMM (raw cards M and N) are a recent addition to the DDR2 RDIMM family. As such, system designers and users need to be aware of some distinguishing characteristics of these designs.

Product Label:

The 4 rank DDR2 RDIMMs are distinguished on the module label in the “eRxff” field, where e=4. For example, a 4GB 4 rank RDIMM built using x4 SDRAMs would be labeled:

- **4GB 4Rx4 PC2-...**

In addition, the raw card reference design letter field “-ef” will indicate the standard design used, if any. For example, a complete label example for such an RDIMM based on raw card M revision 0 with address parity and SPD version 1.2 using DDR2-533 SDRAMs with CAS latency, tRCD, and tRP of 4 clocks each would be:

- **4GB 4Rx4 PC2-4200P-444-12-M0**

Bus Loading:

Loading on the address and command bus for 4 rank RDIMMs is similar to other raw cards: 1 or 2 loads per signal compared to 1 to 4 loads on other raw cards. Additional pre-register flight time must be accounted for on the $\overline{S}2$ and $\overline{S}3$ signals which require an additional 37 mm of routing on the RDIMM.

DDR2 RDIMMs with 4 ranks place 4 loads on the data bus. For raw card M these are all DQ, CB, DQS, and $\overline{DQS}$ signals. For raw card N these are all DQ, CB, DM, DQS, and $\overline{DQS}$ signals. System simulation must be done to ensure proper operation, especially with systems supporting more than one slot which must verify proper interaction of 4 rank RDIMMs with empty slots or slots containing RDIMMs with 1, 2, or 4 ranks per slot.

Rank Selects, Clock Enables, On-Die Termination:

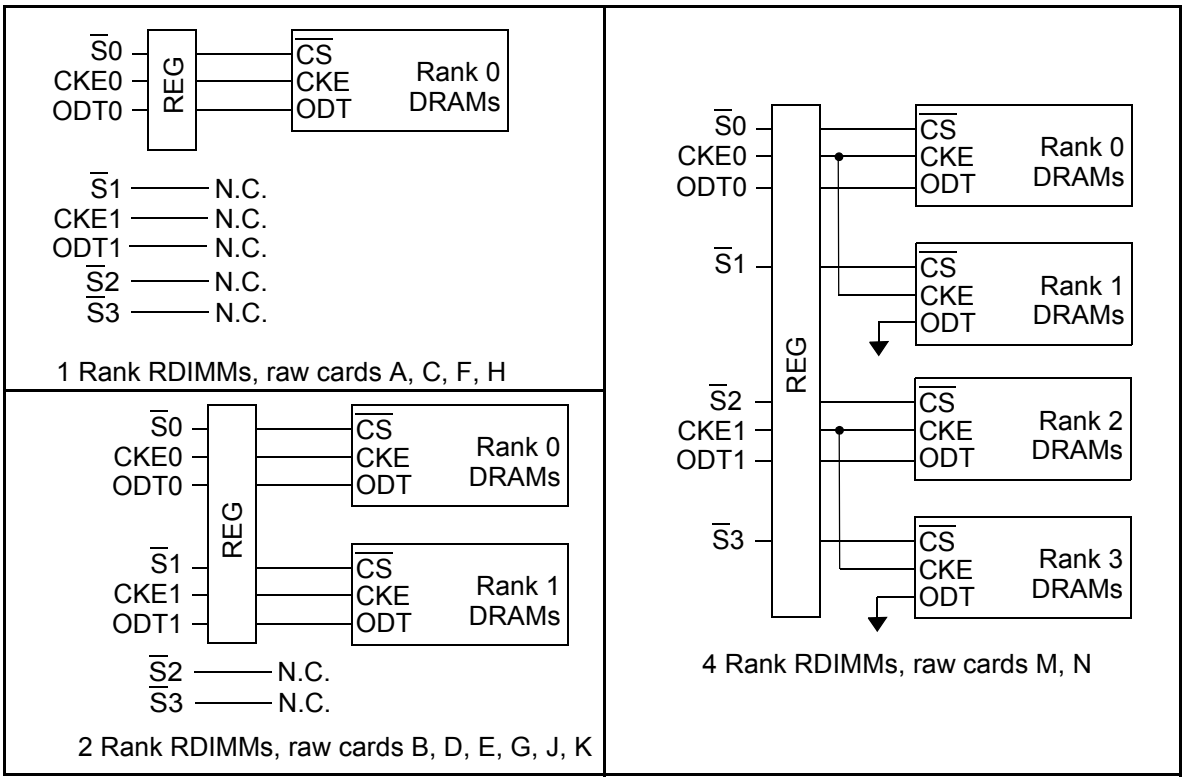
The addition of rank select signals $\overline{S}2$ and $\overline{S}3$ on the motherboard are required in order to support 4 rank RDIMMs. Consistent with the rest of the command and address bus and rank selects $\overline{S}0$ and $\overline{S}1$, it is recommended that routing of rank selects $\overline{S}2$ and $\overline{S}3$ is done referenced to VDD for best signal integrity. All DDR2 RDIMMs (1, 2, and 4 rank versions) reference the data bus, masks, strobes, and clocks to VSS.

Only two clock enable signals, CKE0 and CKE1, and two on-die termination signals, ODT0 and ODT1, are provided at the DDR2 RDIMM edge connector. Controllers must be programmed as appropriate for the following association between signals:

- **$\overline{S}0$ and $\overline{S}1$ associated with CKE0 and ODT0**
- **$\overline{S}2$ and $\overline{S}3$ associated with CKE1 and ODT1**

These associations between control signals are shown graphically in the following block diagrams.

Petitioners
Ex. 1066, p. 105



Simulation and testing indicate that best signal integrity on the data, mask, and strobe bus is obtained when ODT is programmed for 75 Ω for ranks 0 and 2 of DDR2 SDRAMs via the mode register set command EMRS(1) and both ODT0 and ODT1 RDIMM signals are asserted during cycles requiring termination from the slot containing the 4 rank RDIMM, providing an effective 37.5 Ω termination impedance during these cycles. Since ODT for ranks 1 and 3 are disabled via the ODT pins on these ranks, programming via EMRS(1) is a don't-care for these ranks.

Serial Presence Detect:

Byte 5 of the standard serial presence detect (SPD) describes the number of ranks of memory installed on the RDIMM. A rank of memory is defined as the collection of SDRAMs driven by a given rank select signal, $\overline{S0}$ through $\overline{S3}$. SPD byte 5 of a 4 rank RDIMM will contain the value 0x04.

Petitioners
Ex. 1066, p. 106

Revision Log

Revision Info	Page of Revision	Description of Change
Revision 0.50	ALL	Sponsors version submitted to 42.5 chair including all edits after committee ballot review. (note that the ballots JC42.5-03-29, JC42.5-03-30, JC42.5-03-31 were labeled revision 1.0
Revision 0.51	Version variable	Version 0.51 contains the edits by the 42.5 co-chair before BoD ballot submission
	43	changed “floaring” to “floating”
	4, 22	changed variation number from “A” to “AB” indicating the 1.8 volt key
	41	changed “serch” to “search”
	8	changed “NC/ $\overline{\text{Err_Out}}$” to “NC, $\overline{\text{Err_Out}}$”, “NC/ Par_In” “NC, Par_In” and “NC/ $\overline{\text{DQSn}}$” to “NC, $\overline{\text{DQSn}}$”
	22	added: “The minimum center-to-center spacing of DRAMs is 12.8 mm and the height of the DRAM outline is 21.9 mm for raw card A, B and C reference designs.”
Revision 0.52	7	changed pin# of DQ15 from 144 to 141
	11,12,15,17,19, 22,24-27, 30-33,35-40, 44-47,49	Added tentative specification of Raw Card D and Raw Card E
Revision 0.53	8-10,26-31,34-35 37-45	Added specification of Raw Card F,G,H
	22-23	Added pin-assignment of Register with address and command parity function
	46-50	Changed Raw Card D and E routing information
Revision 0.54	14	Added SDRAM package maximum size
	19,20	Change the landing pattern
	30	Changed DIMM Design File Releases
	38-40, 42,44-46	Changed Net structure Routing of Raw Card F and G
	52	Added Address and Command Parity Net Structures
	54	Added Layer stackup for Raw Card D
Revision 0.55	14	Changed support DRAM outline max. of Raw Card D
	30	Changed DIMM Design File Releases
	38,39	Changed R/C-E Clock net length
	50,51	Changed TL5 of CKE,ODT and TL6 of $\overline{\text{S}}$ of Raw Card E
	54	Added the thickness of layer stackup
	55	Deleted column of derating and added row of derating on post-Register Timing table
Revision 0.56	7	Changed DIMM Pinout of 54pin from BA2 to BA2, NC
	8-12	Added stub resistor and changed topology of Signals for Address and Command Parity function
	25	Added Note 3 for CSGateEN
	27	Added options of No support Address and Command Parity Function on Raw Card E,F,G and H
	30	Changed DIMM Design File Releases
	39	Changed PLL feedback path net length of Raw Card C, D, E and H
	40	Changed PLL output to SDRAM net length of Raw Card D
	41,42	Changed PLL output to Register net length and topology of Raw Card D

Petitioners
Ex. 1066, p. 107

Revision Log

Revision Info	Page of Revision	Description of Change
Revision 0.56	47,48	Changed Address and Command Net length and topology of Raw Card D
	49-51	Changed Address and Command Net length and topology of Raw Card E
	52	Changed Address and Command Parity Net Structures of Raw Card D and E
	54	Changed thickness of Eight layer Stackup for Raw Card D
	60	Added Module type of R on module type of Product Label
Revision 0.57	5	Replaced the operating temperature with note 3
	11	Added resistor on Err_Out of Raw Card D
	19,20	Added notes 2 and 3
	28, 29	Added Stub resistor and pull down resistor table and DIMM applicable table for non parity DIMM and parity DIMM
	32	Changed DIMM Design File Releases
	38	Added test point information of Raw Card D and E
	45,54	Changed Net length of Raw Card E
Revision 0.58	12	Deleted the note " $\overline{S}$1, CKE1 and ODT1 are NC"
	14	Added Block Diagram for Raw Card K
	16	Added Raw Card J and K and note 2 in table of Component Details
	22	Added Note 2 and 3
	23-26	Changed some NC to DNU, added Note 1 and 2
	27	Changed MTL to MCL, MTH to MCH, added notes, Correct MO number from MO-225B to MO-246A, Deleted "/ 1:1 "from the title of SSTU32865
	28, 29	Added Pin Assignments for SSTU32868
	31	Added Raw Card J and K column in Table of DIMM Register Use, Changed the value of tACT and tINACT from TBD to 10ns and15ns
	32	Updated optional resistor information for 4Gb, A15 on table of Register Options for Unused Address inputs, Added Raw Card K on this table
	33	Added Raw Card K on Rzero of $\overline{\text{Err_Out}}$ drawing and table of Applicable DIMM types in Systems
	35	Updated addressing of DIMM used 4Gb DRAM
	36	Added Raw Card J and K column in both tables
	40	Added Raw Card J and K drawing of Example Component Placement
	41	Added Parity Function Signal Group and Raw Card K on table
	41,43	Added Raw Card K testpoint information
	45-47, 49, 50, 52, 61-62, 64	Added Raw Card K net structure information
	66	Added Raw Card K layer stackup
	72	Updated Product Label

Petitioners
Ex. 1066, p. 108

Revision Log

Revision Info	Page of Revision	Description of Change
Revision 1.01	4, 36, 70, 72	Changed from PC2-4300 to PC2-4200
	13	Added RC-J Block Diagram
	16	Added RC-J Component Detail
	21	Corrected typo: VSSQ changed to VSS onSDRAM Landing Pattern
	31	Added footnotes for requirement of faster register for PC2-4200 RC J
	31-36	Added RC-J information
	36	Updated Applicable Design File and BOM
	40	Added Component Types and Placement of RC-J
	41	Updated page of signal group
	61-62	Added Net structure Routing of Address and Command of RC-J
	65-66	Added Net structure Routing of Address and Command Parity of RC-J
	69	Added Layer Stackup Example of RC-J
	74	Deleted “00” from SPD data entry for byte 128-255 on Serial Presence Detect Example table,
	75-76	Updated product label
	77	Added a table of DIMM thickness variations on DIMM mechanical Specifications
Revision 1.1	4	Added DIMM configuration table, DIMM thickness variation on Product family attributes
	11	RS0 connected to D8 and D26
	21	Corrected typo : VSSQ to VSS
	33	Removed "Plugging parity DIMM ..... therefore not allowed"
	36	Updated Applicable Design File and BOM
	53	Separated DQ/DQS/DM topology of RC-D,E and K from DQ/DQS/DM topology of RC-B and J
	54-65	Added cell for total length of pre-register
	62,63	Corrected RC-J Pre-Register topology
	71	note3: Corrected netdelay measurement points from Vref timing methodology to derating values timing methodology
	73	Corrected SPD byte 12 from 02 to 82
	74	Applied SPD byte 19 the DIMM thickness code
	78	Corrected DIMM thickness from 4.1mm to 4.0 mm
	80	Changed reset usage
Revision 1.21	All	Added PC2-5300 RDIMM speed grade support
Revision 1.22	4	Added DRAM size column; added parity function support column; deleted redudant notes
	11	Moved DQS2 at proper location
	31	Re-labeled PC2-4200 to PC2-4200/PC2-3200; Deleted SSUTA32864 register from R/C J
	32	Added note 3: Refers to appropriate register datasheet for exact detailed register specification.
	73	Corrected tPDM, tSKEW, tSS numbers and re-did the math
	74	Added PLL Skew table for PC2-5300 speed grade

Petitioners
Ex. 1066, p. 109

Revision Log

Revision Info	Page of Revision	Description of Change
Revision 1.23	4	Added Note for R/C D and K; Added note for PC2-5300 specification status; Deleted third paragraph statement about which cards supports what speed bin.
	33	Deleted R/C J from Non-parity DIMM option with SSTU32864 register
Revision 2.0	4	PC2-5300 is applied only for RC-D,F,G,H,K in Table of Module Configurations; Deleted RC-E and J
	13	Correct typo in RC-J Block Diagram;Correct the four Registers parity check to two Registers parity check. and this “typo” was then reversed again (in RED) as the RDIMM TG was not sure if this is editorial
	38	Correct file name of RC-D0 (Design File and BOM) and RC-H0(BOM) in DDR2 Registered DIMM Design File Release table to correct of typo. Deleted the BOM for Non-Parity RC-D0.
Revision 2.1 (Revision 3.0 after Comittee ballot pass)	4	PC2-6400 is applied (tentatively) for RC-D,F,G,H,J and K in Table of Module Configurations
	25	Added SSTUB32866 on title of table
	27	Changed from SSTUA32865 to SSTUA32S865/SSTUA32D865, Added SSTUB32S865/SSTUB32D865
	28	Changed from SSTUA32868 to SSTUA32S868/SSTUA32D868, Added SSTUB32S868/SSTUB32D868
	31	Added the row of PC2-6400 in the table of DIMM Register Use, Added registers for backward compativility
	33	Added Critical Register Specification for PC2-6400, Added Cin for Dual-die PC2-5300
	36	Added tsk(o) on PLL spec for PC2-4200/PC2-3200, Added PLLs for backward compatibility
	37	Added PC2-6400 to Critical PLLSpecification for PC2-5300, Added tsk(o),Σt(su) and Σt(h) on PLL spec for PC2-6400/PC2-5300
	39	Added BOM file name of RC-DO non address and command parity
	72-73	Changed the spacing between inner planes of RC-D and RC-J
	75	Corrected tPDM, tIS and Margin of PC2-5300 in Example DIMM Post Register Timing
	76	Added Example DIMM Post Register Timing for PC2-6400
	77	Added DIMM Clock jitter and Skew for PC2-6400
	78-80	Changed the example of SPD for PC2-6400
Revision 3.0	4-6, 8, 16, 17, 19, 34, 37-39, 41-42, 47-48, 50, 52-55, 58, 61, 74-78, 81, 89, 90	Added Pinouts & Other reference of Raw Card M and N as ballot material Item# 1520.05, net topologies and net length of Raw Card N as ballot material Item# 1520.06.
	18	Replaced section “Differential Clock Wiring” by respective section of ballot material on normalized clockskew Item #1394.04
	34	Deleted SSTUB32S865,SSTUB32D865,SSTUB32866,SSTUB32S868,SSTUB32D868 from row of Register Speed Grade PC2-4200/PC2-3200 in table of DIMM Register Use
	37	Added SSTUA32S865/SSTUA32D865/SSTUB32S865/SSTUB32D865 and SSTUA32S868/SSTUA32D868/SSTUB32S868/SSTUB32D868 on the note in table of Register Options for Unused Address inputs
	71-73	Raw Card J net topology changed
	94-97	Replaced the old text on clock timing methodology and clock reference board with respective section of ballot material Item #1394.04

Petitioners
Ex. 1066, p. 110

Revision Log

Revision Info	Page of Revision	Description of Change
3.1	5	Added x mark on RC-J PC2-5300
	5,18,20,35,38,39,40,42,43,48,49,52,54-57,61,63,82,83,85,89	Added RC-P information
	14	Deleted the note about Parity In net topology for RC-J0 design from RC-J Block Diagram
	20,22-24	Added MO-242 for Stacked Package on table of Component Details. MO in title corrected
	42	Corrected the ball number of SDRAM package type
	43	Updated Applicable Design File and Applicable BOM of RC-N0, RC-P0 and RC-J1
	49, 86	Added $\overline{\text{RESET}}$ net topology
	102	Added RC-E, K and P information on the skew table
3.2	16	Updated RC-M Block Diagram (After BOD, typo(D32 --> D31)corrected)
	21-24	Added Note for NC and NU, indicate the apge numbers to be referred note 2 and note 3
	35	Added SSTUB register series on RC-D,H,J,K and P, Added SSTUB series on RC-J PC2-5300 speed bin. (After BOD, typo corrected ;SSTUA series has deleted for RC-J PC2-5300)
	59-61	Correct PLL output to Register net topology of RC-J like the topology of RC-N Correct clock termination resistor: R1 of RC-J from 240 ohms to 120 ohms
	74-76	(After BOD, Deleted the Note about RC-J0 placed in topology pictures area since current J1 design meets this topology pictures and this note is not necessary)
	102	Defined the skew values for RC-D and RC-J, and added RC-M and RC-N in Skew t able
	105-106	Added application notes for 4 rank DIMMs

Petitioners
Ex. 1066, p. 111