Paper No. 2

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,

Petitioners,

v.

NETLIST, INC.,

Patent Owner.

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Case IPR2023-01141
Patent 11,093,417

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**PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 11,093,417**

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## Regulations

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## EXHIBIT LIST

| Exhibit # | Description |
|---|---|
| 1001 | U.S. Patent No. 11,093,417 (issued Aug. 17, 2021) |
| 1002 | File History of U.S. Patent No. 11,093,417 (filed Nov. 25, 2019) |
| 1003 | Declaration of Dr. Andrew Wolfe |
| 1004 | Curriculum Vitae of Dr. Andrew Wolfe |
| 1005 | U.S. Provisional Application No. 60/645,087 (filed Jan. 19, 2005) |
| 1006 | U.S. Provisional Application No. 60/588,244 (filed July 15, 2004) |
| 1007 | U.S. Provisional Application No. 60/550,668 (filed March 5, 2004) |
| 1008 | U.S. Provisional Application No. 60/575,595 (filed May 28, 2004) |
| 1009 | U.S. Provisional Application No. 60/590,038 (filed July 21, 2004) |
| 1010 | File History of U.S. Patent No. 7,286,436 (filed March 7, 2005) |
| 1011 | U.S. Patent No. 7,286,436 (issued Oct. 23, 2007) |
| 1012 | U.S. Patent No. 7,289,386 (issued Oct. 30, 2007) |
| 1013 | Affirmance of the Examiner's Decision on Reexamination of '386 Patent (Feb. 25, 2015) |
| 1014 | Reexamination Certificate for '386 Patent (Aug. 19, 2016) |
| 1015 | U.S. Patent No. 7,619,912 (issued Nov. 17, 2009) |
| 1016 | Decision on Reexamination of '912 Patent (June 6, 2016); Decision Under 37 C.F.R. § 41.77(f) (July 27, 2018); and Decision on Rehearing (Jan. 31, 2019) |
| 1017 | Reexamination Certificate for '912 Patent (Feb. 8, 2021) |
| 1018 | Petition for *Inter Partes* Review of U.S. Patent No. 7,619,912 (Feb. 17, 2022) |
| 1019 | Patent Owner Preliminary Response to Petition for *Inter Partes* Review of U.S. Patent No. 7,619,912 (July 21, 2022) |

| Exhibit # | Description |
|---|---|
| 1020 | Declaration of Michael C. Brogioli, Ph.D. in Support of Patent Owner Preliminary Response to Petition for *Inter Partes* Review of U.S. Patent No. 7,619,912 (July 21, 2022) |
| 1021 | Reply to Patent Owner Preliminary Response to Petition for *Inter Partes* Review of U.S. Patent No. 7,619,912 (Aug. 26, 2022) |
| 1022 | Sur-Reply to Patent Owner Preliminary Response to Petition for *Inter Partes* Review of U.S. Patent No. 7,619,912 (Sept. 9, 2022) |
| 1023 | Decision Granting Institution of *Inter Partes* Review of U.S. Patent No. 7,619,912 (Oct. 19, 2022) |
| 1024 | Patent Owner's Request for Rehearing of Decision Granting Institution of *Inter Partes* Review of U.S. Patent No. 7,619,912 (Nov. 2, 2022) |
| 1025 | Order of Sua Sponte Director Review of Decision Granting Institution of *Inter Partes* Review of U.S. Patent No. 7,619,912 (Jan. 5, 2023) |
| 1026 | U.S. Patent No. 7,864,627 (issued Jan. 4, 2011) |
| 1027 | Decision on Appeal of Reexamination of '627 Patent (May 30, 2016); Decision Under 37 C.F.R. § 41.77(f) (May 31, 2018) |
| 1028 | Reexamination Certificate for '627 Patent (Nov. 5, 2018) |
| 1029 | U.S. Patent No. 8,756,364 (issued June 17, 2014) |
| 1030 | IPR2017-00549 Final Written Decision ('364 Patent) (May 3, 2018) |
| 1031 | IPR Certificate for '364 Patent (May 26, 2020) |
| 1032 | U.S. Patent No. 7,532,537 (issued May 12, 2009) |
| 1033 | IPR2017-00667 Final Written Decision ('537 Patent) (July 18, 2018) |
| 1034 | IPR2017-00668 Final Written Decision ('537 Patent) (July 18, 2018) |
| 1035 | IPR Certificate for '537 Patent (Apr. 27, 2020) |

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| 1036 | U.S. Patent No. 7,636,274 (issued Dec. 22, 2009) |
| 1037 | Decision on Appeal of Reexamination of ’274 Patent (May 9, 2017) |
| 1038 | Reexamination Certificate for ’274 Patent (Nov. 5, 2018) |
| 1039 | U.S. Patent No. 7,881,150 (issued Feb. 1, 2011) |
| 1040 | IPR2014-00882 Final Written Decision on Remand (’150 Patent) (March 29, 2018) |
| 1041 | IPR2014-01011 Final Written Decision on Remand (’150 Patent) (March 29, 2018) |
| 1042 | IPR2015-01020 Final Written Decision (’150 Patent) (Sept. 28, 2016) |
| 1043 | IPR Certificate for ’150 Patent (Mar. 6, 2019) |
| 1044 | File History of U.S. Patent No. 7,916,574 (filed Nov. 29, 2010) |
| 1045 | U.S. Patent No. 7,916,574 (issued Mar. 29, 2011) |
| 1046 | U.S. Patent No. 8,081,536 (issued Dec. 20, 2011) |
| 1047 | IPR2014-00883 Final Written Decision on Remand (’536 Patent) (March 29, 2018) |
| 1048 | IPR2015-01021 Final Written Decision (’536 Patent) (Sept. 28, 2016) |
| 1049 | IPR Certificate for ’536 Patent (Mar. 11, 2019) |
| 1050 | File History of U.S. Patent No. 8,516,188 (filed Nov. 1, 2011) |
| 1051 | U.S. Patent No. 8,516,188 (issued Aug. 20, 2013) |
| 1052 | File History of U.S. Patent No. 9,037,774 (filed Aug. 20, 2013) |
| 1053 | U.S. Patent No. 9,037,774 (issued May 19, 2015) |
| 1054 | File History of U.S. Patent No. 10,489,314 (filed Dec. 28, 2017) |
| 1055 | U.S. Patent No. 10,489,314 (issued Nov. 26, 2019) |

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|---|---|
| 1056 | Decisions Granting Institution of *Inter Partes* Reviews of U.S. Patent No. 10,489,314 (Nov. 1, 2022) |
| 1057 | File History of U.S. Patent No. 9,858,215 (filed May 18, 2015) |
| 1058 | U.S. Patent No. 9,858,215 (issued January 2, 2018) |
| 1059 | File History of U.S. Patent Application No. 17/403,832 (filed Aug. 16, 2021) |
| 1060 | JEDEC JESD79 standard for DDR SDRAM (June 2000) |
| 1061 | [intentionally omitted] |
| 1062 | JEDEC JESD21-C design specification for DDR SDRAM Registered DIMM (January 2002) |
| 1063 | [intentionally omitted] |
| 1064 | JEDEC JESD79-2 standard for DDR2 SDRAM (Sept. 2003) |
| 1065 | Declaration of Julie Carlson (JESD79-2) |
| 1066 | JEDEC JESD21-C design specification for DDR2 SDRAM Registered DIMM, Rev. 3.2 (Oct. 4, 2005) |
| 1067 | [intentionally omitted] |
| 1068 | Harold S. Stone, Microcomputer Interfacing (1982) |
| 1069 | Bruce Jacob, *Synchronous DRAM Architectures, Organizations, and Alternative Technologies* (Dec. 10, 2002) |
| 1070 | Bruce Jacob et al., Memory Systems: Cache, DRAM, Disk (2008) |
| 1071 | U.S. Patent No. 7,363,422 to Perego et al. (filed Jan. 28, 2004) |
| 1072 | U.S. Patent No. 7,155,627 to Matsui (filed Aug. 22, 2003) |
| 1073 | U.S. Patent Application Publication No. 2006/0277355 to Ellsberry et al. (filed June 1, 2005) |
| 1074 | IPR2018-00362 Final Written Decision (June 27, 2019) ('907 Patent) |

| Exhibit # | Description |
|---|---|
| 1075 | U.S. Patent No. 9,606,907 (all claims cancelled) |
| 1076 | Decision Granting Institution of *Inter Partes* Review of U.S. Patent No. 10,949,339 (Oct. 19, 2022) (child of U.S. Patent No. 9,606,907, Exhibit 1075) |
| 1077 | U.S. Patent Application Publication No. 2002/0112119 to Halbert et al. (published Aug. 15, 2002) |
| 1078 | U.S. Patent No. 7,024,518 to Halbert et al. (filed Mar. 13, 2002) |
| 1079 | U.S. Patent Application Publication No. 2006/0117152 to Amidi et al. (filed Jan. 5, 2004) |
| 1080 | U.S. Patent No, 8,250,295 to Amidi et al. (filed Jan. 5, 2004) |
| 1081 | U.S. Patent. No. 5,513,135 to Dell et al. (issued Apr. 30, 1996) |
| 1082 | U.S. Patent Application Publication No. 2003/0039151 to Matsui (published Feb. 27, 2003) |
| 1083 | [intentionally omitted] |
| 1084 | [intentionally omitted] |
| 1085 | Amended Complaint in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al*., No. 2:22-cv-00293 (E.D. Tex. filed Aug. 15, 2022) |
| 1086 | Waiver of Service in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al*., No. 2:22-cv-00293 (E.D. Tex. filed Aug. 31, 2022) |
| 1087 | [intentionally omitted] |
| 1088 | Amended Complaint in *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:22-cv-00294 (E.D. Tex. filed Aug. 15, 2022) |
| 1089 | Micron's Answer in *Netlist, Inc. v. Micron Technology, Inc. et al*., No. 2:22-cv-00294 (E.D. Tex. filed Sept. 7, 2022) |
| 1090 | [intentionally omitted] |
| 1091 | *Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation* (June 21, 2022) |

| Exhibit # | Description |
|---|---|
| 1092 | Federal Court Management Statistics (Mar. 31, 2022), *available at* https://www.uscourts.gov/statistics/table/na/federal-court-management-statistics/2022/03/31-1 |

## CLAIM LISTING

| Ref. # | Listing of Challenged Claims |
|---|---|
| **1.a.1** | 1. A memory module |
| **1.a.2** | operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, |
| **1.a.3** | the memory bus including address and control signal lines and data signal lines, |
| **1.a.4** | the memory module comprising: |
| **1.b** | a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system; |
| **1.c.1** | logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals, |
| **1.c.2** | the set of input address and control signals including a plurality of input chip select signals and other input address and control signals, the plurality of input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value, |
| **1.c.3** | the set of registered address and control signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals, the plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value, |
| **1.c.4** | wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command; |
| **1.d.1** | memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, |

| Ref. # | Listing of Challenged Claims |
|---|---|
| **1.d.2** | wherein the plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices one respective N-bit wide rank of the plurality of N-bit-wide ranks, |
| **1.d.3** | wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command; and |
| **1.e** | circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module; |
| **1.f** | wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices. |
| **2** | The memory module of claim 1, wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus. |
| **3** | The memory module of claim 1, wherein the burst of N-bit wide data signals includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein the set of consecutively transmitted data bits are successively transferred through the circuitry in response to the data buffer control signals. |
| **4** | The memory module of claim 1, wherein each of the memory devices is 4-bits wide, and wherein each of the plurality of ranks is 64-bits or 72-bits wide and includes 16 or 18 memory devices configured in pairs. |

| Ref. # | Listing of Challenged Claims |
|---|---|
| **5** | The memory module of claim 1, wherein the memory devices are organized in four ranks and the set of input address and control signals include four chip select signals, one for each of the four ranks. |
| **6** | The memory module of claim 1, wherein the circuitry includes logic pipelines configurable to enable the data transfers between the memory devices and the memory bus through the circuitry. |
| **7** | The memory module of claim 1, wherein the logic is further configured to report the overall CAS latency to the memory controller in response to a mode register set command received from the memory controller. |
| **8** | The memory module of claim 1, wherein the memory module has a specified data rate, and wherein the burst of N-bit wide data signals are transferred between the one of the plurality of N-bit wide ranks and the memory controller at the specified data rate. |
| **9** | The memory module of claim 1, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay. |
| **10** | The memory module of claim 9, wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the one of the plurality of N-bit wide ranks is configured to receive or output a respective set of bits of the burst of N-bit wide data signals on both edges of each of a respective set of data strobes. |
| **11** | The memory module of claim 1, wherein the circuitry includes data paths, and wherein the circuitry is configurable to enable the data paths in response to the data buffer control signals so that the burst of N-bit wide data signals are transferred via the data paths. |
| **12** | The memory module of claim 11, wherein the data paths are disabled when no data signals associated with any memory command are being transferred through the circuitry. |
| **13** | The memory module of claim 12, wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus. |

| Ref. # | Listing of Challenged Claims |
|---|---|
| **14** | The memory module of claim 12, wherein the memory module has a specified data rate, and wherein the burst of N-bit wide data signals are transferred through the data paths at the specified data rate. |
| **15** | The memory module of claim 12, wherein the read or write command is a write memory command, wherein the burst of N-bit wide data signals include a respective series of write data bits received by the circuitry from a respective one of the data signal lines, and wherein the respective series of write data bits are successively transferred via a respective one of the data paths |

# I. PETITIONERS' MANDATORY NOTICES

## A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

The real parties in interest are the Petitioners Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC.

## B. Related Matters (37 C.F.R. § 42.8(b)(2))

The following judicial or administrative matters would affect, or be affected by, a decision in this proceeding concerning U.S. Patent No. 11,093,417.

The following proceedings are currently pending:

- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al*., No. 2:22-cv-00293 (E.D. Tex. amended complaint filed Aug. 15, 2022)
- *Netlist, Inc. v. Micron Technology, Inc. et al*., No. 2:22-cv-00294 (E.D. Tex. amended complaint filed Aug. 15, 2022)
- *Samsung Electronics Co., Ltd. v. Netlist, Inc*., IPR2022-00615 (U.S. Patent No. 7,619,912)
- *Micron Technology, Inc. et al. v. Netlist, Inc*., IPR2023-00203 (U.S. Patent No. 7,619,912)
- *Samsung Electronics Co., Ltd. v. Netlist, Inc*., IPR2022-00639 (U.S. Patent No. 10,949,339)
- *Micron Technology, Inc. et al. v. Netlist, Inc*., IPR2022-00744 (U.S. Patent No. 10,489,314)

- *Micron Technology, Inc. et al. v. Netlist, Inc*., IPR2022-00745 (U.S. Patent No. 10,489,314)
- *Samsung Electronics Co., Ltd. v. Netlist, Inc*., IPR2023-00455 (U.S. Patent No. 9,858,215)
- U.S. Application No. 17/403,832

The following proceedings have concluded:

- *Inter partes* Reexamination Nos. 95/000,578; 95/000,579; and 95/001,339 of U.S. Patent No. 7,619,912
- *Inter partes* Reexamination Nos. 95/000,546 and 95/000,577 of U.S. Patent No. 7,289,386
- *Inter partes* Reexamination No. 95/001,758 of U.S. Patent No. 7,864,627
- *Inter partes* Reexamination No. 95/001,337 of U.S. Patent No. 7,636,274
- *SK hynix Inc. et al. v. Netlist, Inc*., IPR2017-00549 (U.S. Patent No. 8,756,364)
- *SK hynix Inc. et al. v. Netlist, Inc*., IPR2017-00667 (U.S. Patent No. 7,532,537)
- *SK hynix Inc. et al. v. Netlist, Inc*., IPR2017-00668 (U.S. Patent No. 7,532,537)

- *Diablo Technologies, Inc. v. Netlist, Inc.*, IPR2014-00882 (U.S. Patent No. 7,881,150)
- *Diablo Technologies, Inc. v. Netlist, Inc.*, IPR2014-01011 (U.S. Patent No. 7,881,150)
- *SanDisk Corp. v. Netlist, Inc.*, IPR2015-01020 (U.S. Patent No. 7,881,150)
- *Diablo Technologies, Inc. v. Netlist, Inc.*, IPR2014-00883 (U.S. Patent No. 8,081,536)
- *SanDisk Corp. v. Netlist, Inc.*, IPR2015-01021 (U.S. Patent No. 8,081,536)
- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2018-00362 (U.S. Patent No. 9,606,907)
- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2018-00363 (U.S. Patent No. 9,606,907)

### C. Lead and Back-up Counsel (37 C.F.R. § 42.8(b)(3))

Lead Counsel is Juan C. Yaquian (Reg. No. 70,755), Winston-IPR-NetList@winston.com, (713) 651-2600, Winston & Strawn LLP, 800 Capital Street, Suite 2400, Houston, TX 77002.

Backup Lead Counsel are:

- Michael Rueckheim (*pro hac vice* to be filed),

Winston-IPR-NetList@winston.com, (650) 858-6500, Winston & Strawn LLP, 255 Shoreline Dr., Suite 520, Redwood Shores, CA 94065.

- James C. Lin (*pro hac vice* to be filed), Winston-IPR-NetList@winston.com, (650) 858-6500, Winston & Strawn LLP, 255 Shoreline Dr., Suite 520, Redwood Shores, CA 94065.

The fax number for lead and backup counsel is (713) 651-2700 .

### D. Service Information (37 C.F.R. § 42.8(b)(4))

Service information is provided in the designation of counsel above. Petitioner consents to service of all documents via electronic mail to Winston-IPR-NetList@winston.com.

## II. INTRODUCTION

Petitioners respectfully request trial on claims 1-15 of U.S. Patent 11,093,417 ("417 Patent") (EX1001) based on grounds not considered during prosecution.

## III. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW

### A. Standing (§42.104(a))

The 417 Patent is available for IPR and Petitioners are not barred or estopped from requesting IPR on the grounds identified below.

### B. Identification of Challenge (§42.104(b))

Petitioner challenges claims 1-15 of the 417 Patent as follows:

| Ground | Claims Challenged | 35 U.S.C. | References |
|---|---|---|---|
| 1 | 1-15 | §103(a) | Perego + JESD79-2 |
| 2 | 1-15 | | Ground 1 + Ellsberry |
| 3 | 1-15 | | Ground 1 + Halbert |

Petitioners' proposed claim constructions and the precise reasons why the claims are unpatentable are provided below. The evidence relied upon is listed above, beginning on page vii.

## IV. RELEVANT INFORMATION CONCERNING THE CONTESTED PATENT

### A. Effective Filing Date of the 417 Patent: No Earlier Than July 1, 2005

The prior art in Grounds 1 and 3 (Perego, JESD79-2, and Halbert) all predate March 5, 2004, the filing date of the 417 Patent's earliest provisional application. But Ellsberry (Ground 2 only) is also prior art because the 417 Patent's claims lack §112 support from any application filed before July 1, 2005,

the filing date of the continuation-in-part application that resulted in U.S. Patent No. 7,289,386 ("386 Patent") (EX1012). EX1003, ¶¶51-67.

Independent claim 1 (and thus every claim) requires "logic...configurable to output ***data buffer control signals*** in response to the read or write memory command" and "circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the ***circuitry*** being configurable to ***transfer the burst of N-bit wide data signals*** between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks ***in response to the data buffer control signals*** [.]"[1]EX1001, 42:38-40, 42:54-61. However, no application filed prior to July 1, 2005 provided §112 support for these limitations. EX1003, ¶¶59-67.

Of the five provisional applications and the one non-provisional application filed prior to July 1, 2005, only one provisional application (U.S. Provisional Application No. 60/645,087 ("087 Provisional") (EX1005)) discloses any circuitry or "Buffer" (RBDL) through which data (DQ0-DQ63) is communicated:

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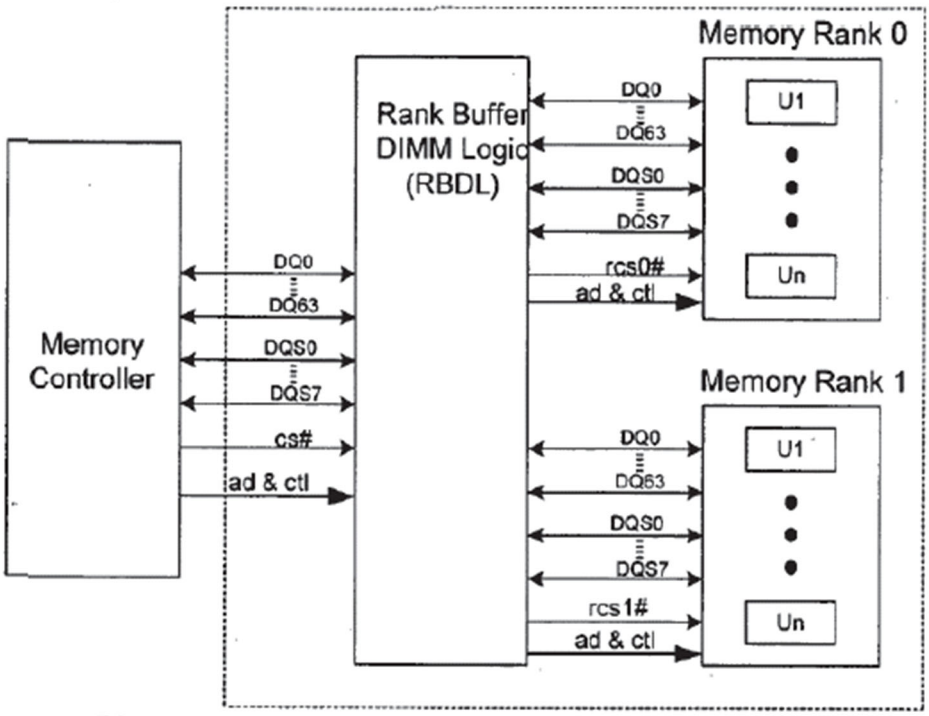
[1] All emphasis in quotes, and color highlighting in figures, has been added unless otherwise noted.

FIGURE 1:




**Block Diagram: Rank Buffered DIMM Memory Sub-system**

EX1005, Fig.1; EX1003, ¶¶58-60. But the 087 Provisional fails to disclose data buffer control signals for enabling the transfer of data bursts through the buffer in response to read or write memory commands. EX1003, ¶61. The 087 Provisional does not mention any "burst of N-bit wide data signals" or "control signals," much less the specific "data buffer control signals" required by the claims. *Id*. The 087 Provisional also does not name all the inventors listed on the 417 Patent. EX1005, p.1.

Although the 087 Provisional refers to "a data path multiplexer/demultiplexer" that provides separate DQ/DQS paths for each rank, it fails to disclose how the multiplexer/demultiplexer specifically transfers data

bursts through the data buffer in response to read or write memory commands or what its control signals are. EX1005, [0005], [0008], [0017]; EX1003, ¶62. And a POSITA would have recognized that the buffer (or "circuitry") need not use "data buffer control signals" to direct a data burst to one of the ranks, even if a memory write command is directed to that one rank, because, for example, the data could be sent to both of the ranks, and a chip-select signal (e.g., rcs0#, rcs1#) could be used to target one of those ranks. EX1003, ¶¶63-64 (citing EX1005, [0009], [0012], Fig.1; EX1064, p.6). A POSITA would have also recognized that data transfer through the buffer does not necessarily happen in response to memory commands as required by the 417 Patent claims and instead could be controlled by other means, such as the "preamble" on the DQS strobe lines. EX1003, ¶65 (citing EX1064, pp.26 ($t_{RPRE}$), 30 ($t_{WPRE}$), 65).

Although the claims of the 417 Patent are obvious in light of the prior art, as explained below, that does not mean the 087 Provisional in light of that prior art provides §112 support for the claims of the 417 Patent: "[A] description that merely renders the invention ***obvious*** does not satisfy the [written description] requirement[.]" *Ariad Pharms., Inc. v. Eli Lilly & Co*., 598 F.3d 1336, 1352 (Fed. Cir. 2010) (en banc). "[T]he written description inquiry looks to the 'four corners of the specification'....The knowledge of ordinary artisans may be used to inform what is actually in the specification, ***but not to teach limitations that are not in the***

***specification, even if those limitations would be rendered obvious by the disclosure in the specification.***" *Rivera v. ITC*, 857 F.3d 1315, 1322 (Fed. Cir. 2017) (citations omitted).

Accordingly, the claims of the 417 Patent are not entitled to a priority date before July 1, 2005, making Ellsberry prior art for Ground 2.

### B. Person of Ordinary Skill in the Art ("POSITA")

A POSITA in the field of the 417 Patent in 2004 or 2005 would have had an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field. EX1003, ¶48. Additional training can substitute for educational or research experience, and vice versa. *Id*. A POSITA would have been familiar with various standards of the day including the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with the memory controller of a computer system. *Id*. Specifically, he or she would have been knowledgeable about the JEDEC DDR and DDR2 SDRAM standards used to standardize the functioning of memory devices, and the JEDEC 21-C standard used to standardize different possibilities for the physical layout of memory devices on a module as well as different possibilities for density and organization of the memory devices to achieve a given memory capacity. *Id*.;

*see also id*. ¶¶49-50 (citing EX1001, 6:43-58, 23:23-24:22, 39:21-28 (referring to JEDEC standards); EX1060, EX1062, EX1064, EX1066). He or she would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs (Application-Specific Integrated Circuits) and CPLDs (Complex Programmable Logic Devices) and more low-level circuits such as tri-state buffers, flip flops and registers. *Id*. ¶48.

### C. Background Technology

#### 1. JEDEC Standards

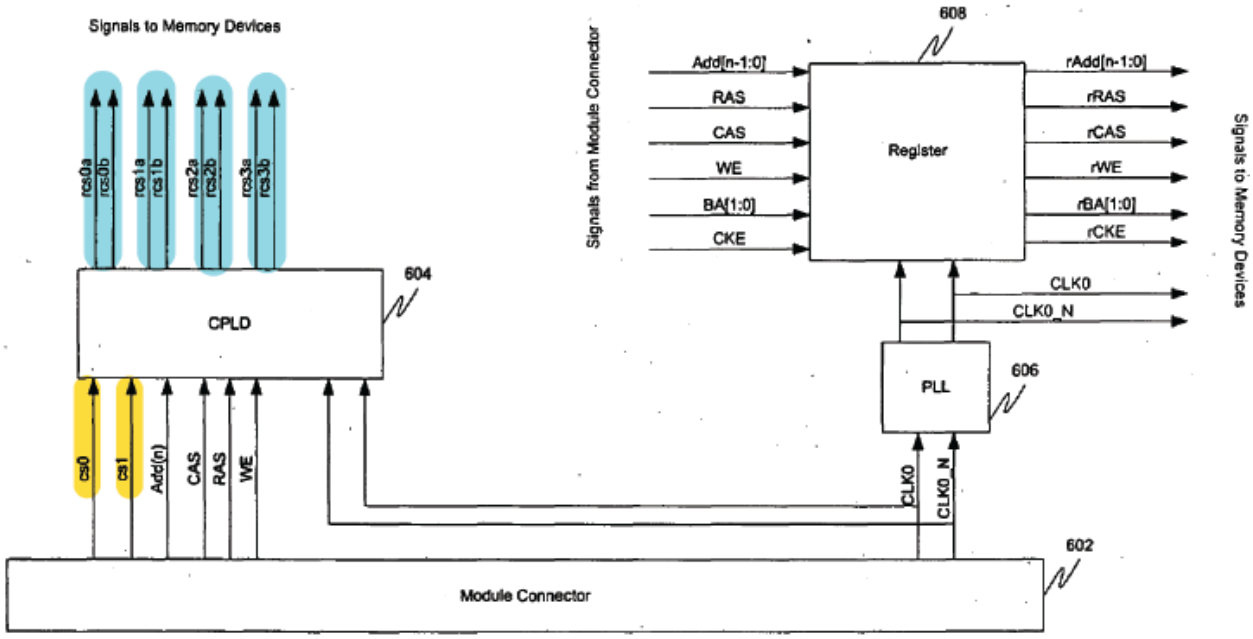
"For over 50 years, JEDEC has been the global leader in developing and publishing open standards for the microelectronics industry." EX1065, ¶4. The 417 Patent refers to various JEDEC standards, including for RDIMM memory modules and DDR SDRAM memory devices. EX1001, 6:43-58, 23:23-24:22, 39:21-28. A POSITA would have been familiar with these JEDEC standards. EX1003, ¶¶165-166; EX1060 (DDR); EX1062 (RDIMM for DDR); EX1064 (DDR2); EX1066 (RDIMM for DDR2). The prior art also refers to these JEDEC standards. *Id*. (citing EX1071, 3:67-4:3, 8:1-9, 10:54-59; EX1073, [0046], [0050]).

#### 2. Rank Multiplication

A POSITA also would have been familiar with "rank multiplication," which permitted replacing one rank of expensive high-density memory with two or more

ranks of less expensive low-density memory without any change to the overall performance or memory capacity of the memory module — thus enabling significant cost savings. EX1003, ¶¶167-170; EX1079, ¶[0008]; EX1001, 13:51-14:4 ("cost savings can be significant").

A POSITA would have understood how to implement rank multiplication. EX1003, ¶168. For example, Amidi (EX1079), which is prior art, teaches that rank multiplication involves mapping address signals (e.g., Add(n)) and chip-select signals (e.g., cs0 and cs1, yellow, for two ranks of high-density memory devices) received from a system memory controller complying with the JEDEC standard into ***more*** chip-select signals (e.g., rcs0 to rcs3, blue) to control the higher number of ranks (e.g., four ranks) of less expensive, lower density memory devices on the memory module:




Row Address Decoding
FIG.6A

EX1079, [0041], [0050]-[0052], FIG. 6A; EX1003, ¶168. Another example of prior art that teaches rank multiplication is Ellsberry, discussed below (pp.20-22). EX1003, ¶169.

Given the significant cost savings from rank multiplication, POSITAs were motivated to implement the technique in a wide range of memory modules. EX1003, ¶¶167, 170.

### D. The 417 Patent

#### 1. Technical Overview

The 417 Patent concerns "rank multiplication," discussed directly above. EX1003, ¶¶68-73. The 417 Patent purports to describe "devices and methods for improving the performance, the memory capacity, or both, of memory modules."

EX1001, 1:47-50. As shown below, a memory module (10) includes "a circuit 40 [red] electrically coupled to the plurality of memory devices 30 [green, blue] and configured to be electrically coupled to the memory controller 20 of the computer system." *Id*., 6:4-7, Fig.1 (below).

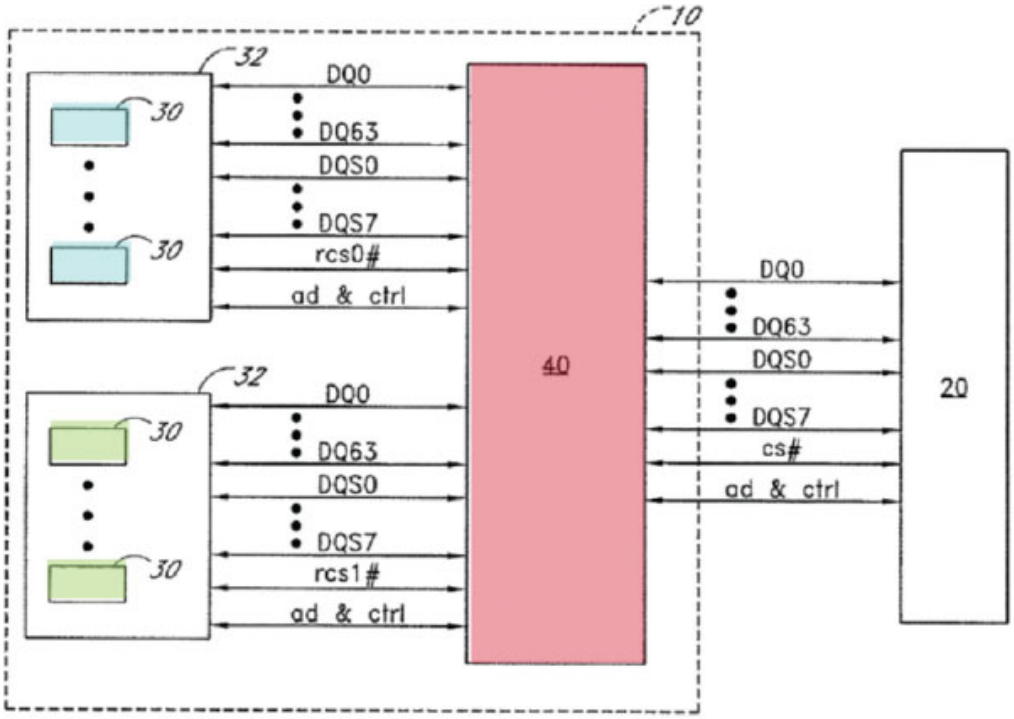



FIG. 1

"DRAM devices of a memory module are generally arranged as ranks or rows of memory" (e.g., the two ranks 32, green and blue, in Figure 1 above). *Id*., 2:47-51, 7:10-13, 14:24-29, Fig.1. "[T]he ranks...are selected or activated by address and command signals," including "rank-select signals [(cs#)], also called chip-select signals," *id*., 2:65-3:2, which are JEDEC-standard signals for DDR

(sometimes called DDR-1) and DDR-2 memory devices, EX1003, ¶69; EX1060, p.7; EX1064, p.6. The 417 Patent's embodiments are compatible with such memory devices. EX1001, 6:51-55; 22:56-60.

The 417 Patent purportedly improves a memory module's capacity because the "circuit 40 selectively isolates one or more of the loads of the memory devices from the computer system...[and] comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module 10." EX1001, 6:7-12, Fig.1 (above); *see also id*., 10:5-46. The computer system sees a memory module with higher-density memory devices (a system memory domain), while the physical configuration of the module (a physical memory domain) is different. EX1003, ¶71; EX1001, 17:56-60. As shown above in Figure 1, the memory controller (20) issues commands to a single "virtual" rank using a single chip-select signal ("cs#"), while the module actually has two ranks, each having its own chip-select signals ("rcs0#" and "rcs1#"). EX1003, ¶71. Signal collision is prevented by selectively connecting the system data bus to only one of the ranks that form the "virtual" higher density memory device. *Id*., ¶72; EX1001, 13:60-14:55, Fig.7.

When the buffer circuit (40) registers the data transfers, an extra clock cycle is added to the natural CAS latency of the individual memory devices ("equivalent to a registered DIMM") and "advantageously provides sufficient time budget to

add a buffer which electrically isolates the ranks of memory devices 30 from the memory controller 20." EX1001, 22:36-60; EX1003, ¶73.

#### 2. Prosecution History

During prosecution of the 417 Patent, the Examiner never issued a rejection and simply allowed the claims. EX1003, ¶¶118-119; EX1002, pp.224-31, 298-303, 311-13.

The 417 Patent is related to a number of earlier applications. EX1003, ¶¶74-120. Hundreds of claims from those earlier applications, all related to "rank multiplication," have been canceled in recent years as a result of reexaminations and IPRs. *Id*. ¶¶89-95, 99, 167 (citing EX1012-EX1017, EX1026-EX1043, EX1046-EX1049). In addition, IPRs were recently instituted against the 912 and 314 patents, which are in the same family as the 417 Patent. *See* EX1023;[2] EX1056, pp.22, 50.

## V. OVERVIEW OF THE PRIOR ART

### A. Perego (EX1071)

U.S. Patent No. 7,363,422 ("Perego"), filed January 28, 2004, and published September 23, 2004, is prior art under §102(a), (e). EX1071; EX1003, ¶135. Perego teaches a memory system 305 including a memory controller 310

[2] This decision is being reviewed. EX1024-EX1025.

connected to multiple buffered memory modules 330a-330n, such as memory module 340, which includes a buffer device (350, red) and multiple groups of memory devices (360, green and blue). EX1071, Abstract, Fig.3B, 4:63-5:15; EX1003, ¶137.

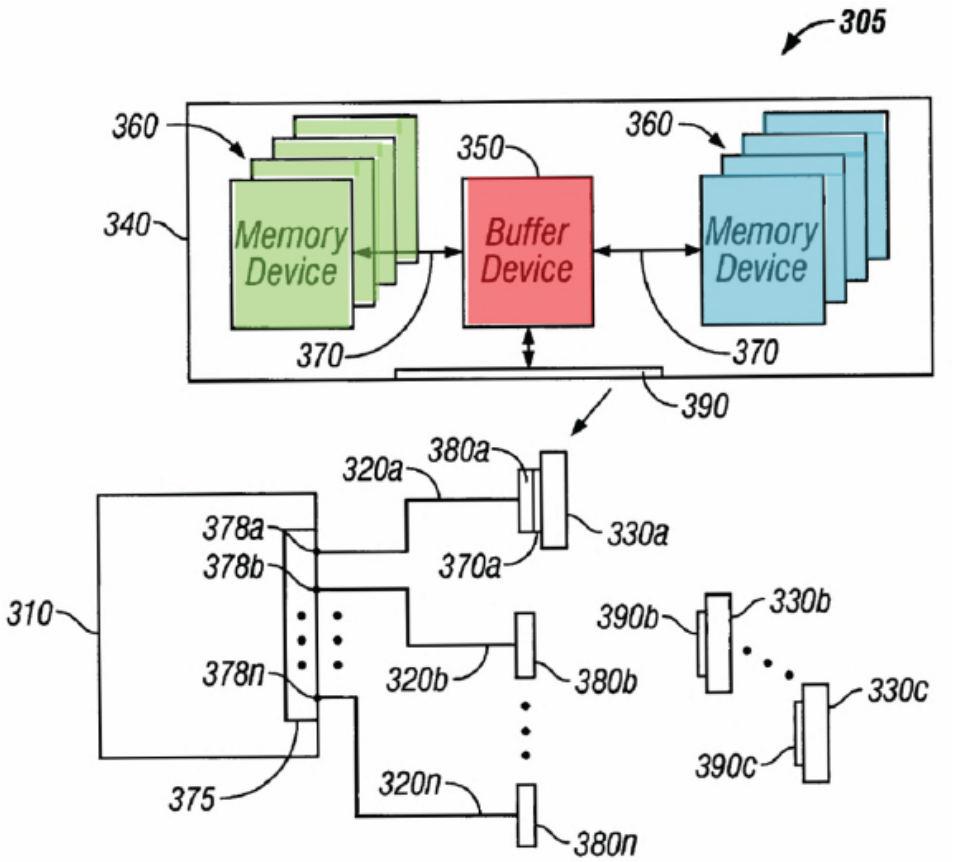



FIG. 3B

EX1071, Fig.3B. "Buffer device 350 provides a high degree of system flexibility. New generations of memory devices may be phased in with controller 310.... Similarly, new generations of controllers may be phased in...while retaining backward compatibility with existing generations of memory devices." *Id.*, 6:34-

43; *see also id*. Fig.3C (below, showing configurable width buffered module 395); EX1003, ¶¶138-139.

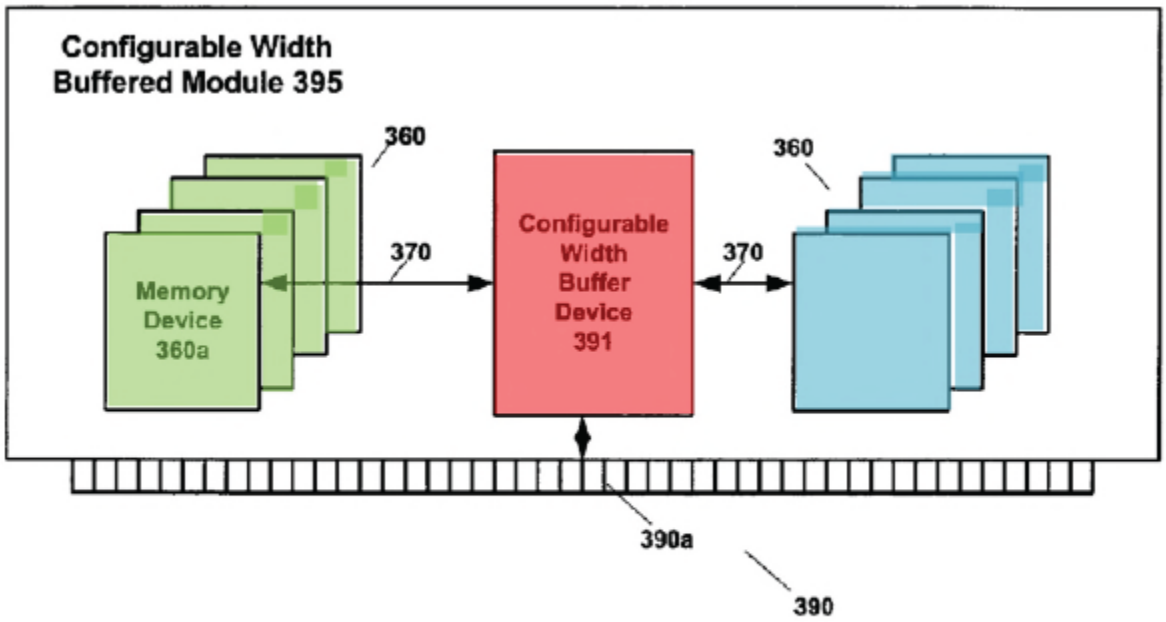



Fig. 3C

The buffer device (red, above and below) includes programmable interfaces 520a and 520b, which accommodate different numbers and types of memory devices, while configurable width interface 590 communicates with the memory controller. *Id*., 13:6-10, 13:60-14:15; EX1003, ¶140.

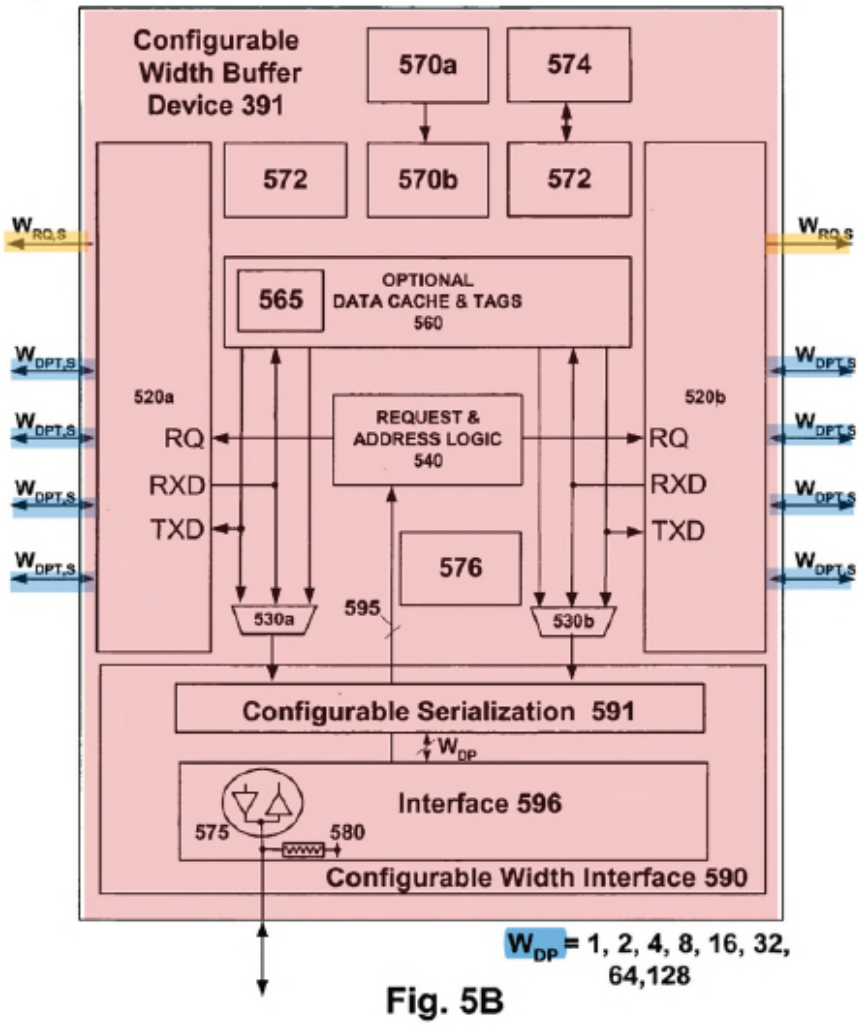



Fig. 5B

EX1071, Fig.5B. Configurable width interface 590 can include two input and output latches 597f-m (blue, below) for each data connection. *Id*., 17:22-26, 17:61-67; EX1003, ¶141.

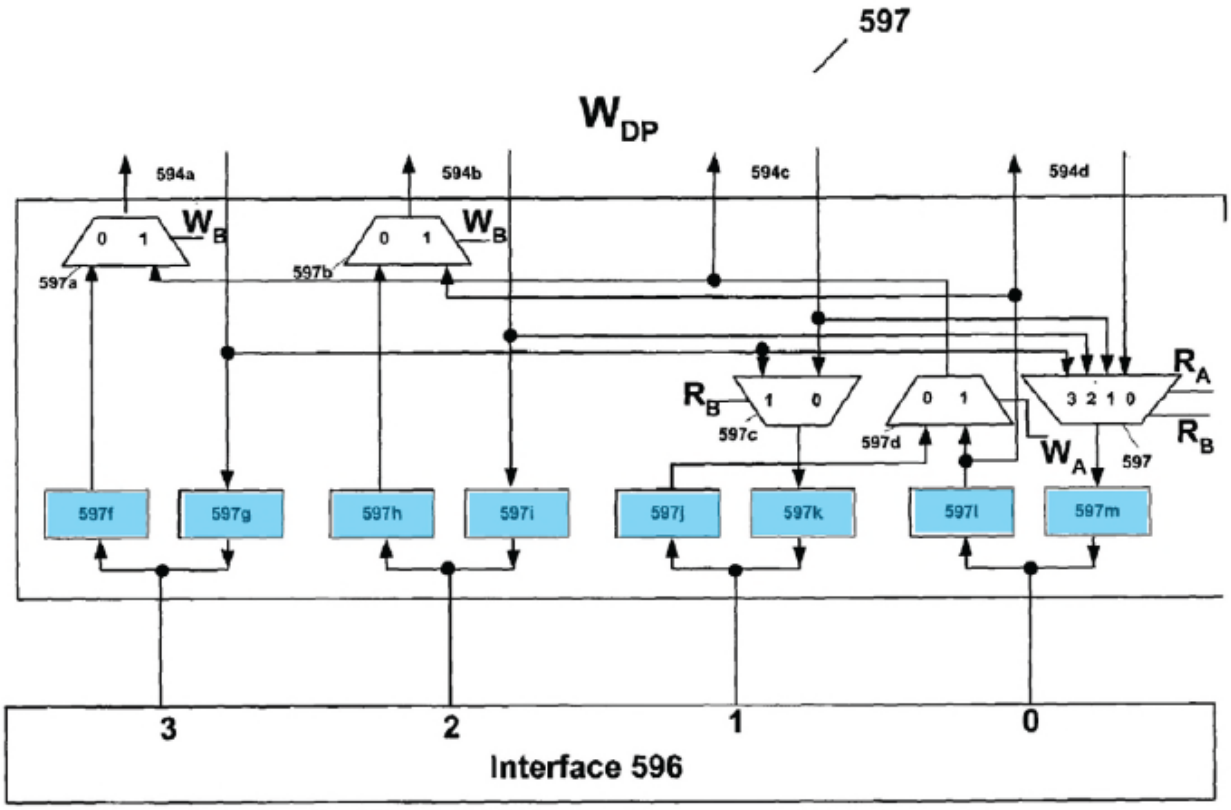



Fig. 5C

EX1071, Fig.5C. Perego's buffer device (red, above) also includes a serial interface 574 and operations circuit 572 to provide information to the system memory controller for initialization and proper configuration and operation of the system, including access latency values. *Id*., 12:20-34, Figs.5A-5B; EX1003, ¶142.

### B. JESD79-2 (EX1064)

The DDR2 SDRAM Specification (JESD79-2), published in September 2003, is prior art under §102(a), (b). EX1064; EX1065, ¶¶6-11; EX1003, ¶143. It is a JEDEC standard for second generation double data rate (DDR2) memory

devices. EX1064, p.Cover-1; EX1003, ¶144. JESD79-2 describes, for example, the signals used to execute read and write commands in ranks of memory devices. EX1064, pp.6, 24-33, 49; EX1003, ¶145. JESD79-2 also describes CAS latencies and adding additional clock cycles of latency when executing read and write commands. EX1064, pp.24-25; EX1003, ¶145.

### C. Ellsberry (EX1073)

U.S. Patent Publication No. 2006/0277355 ("Ellsberry"), filed June 1, 2005, is prior art at least under §102(e) as explained above (pp.5-9). EX1073; EX1003, ¶146; *see also* EX1023, pp.24-26 (recognizing Ellsberry as prior art in proceeding against family member of 417 Patent). The Board analyzed Ellsberry extensively in a Final Written Decision against Netlist, *see* EX1074, and thus the issues decided against Netlist in that Decision are now binding against Netlist, *see, e.g., VirnetX Inc. v. Apple, Inc.*, 909 F.3d 1375, 1377-78 (Fed. Cir. 2018); *MaxLinear, Inc. v. CF CRESPE LLC*, 880 F.3d 1373, 1376-77 (Fed. Cir. 2018).

Ellsberry implements "rank multiplication" (discussed above, pp.10-12) by "making two smaller-capacity memory devices emulate a single higher-capacity memory device." EX1073, Abstract; EX1003, ¶149. In particular, Ellsberry's memory module has "[a] control unit [red, below] and memory bank switch [purple, below]...to selectively control write and/or read operations...[and] selectively rout[e] data to and from the memory devices," thus allowing "a

plurality of memory devices [blue and green, below] [to] appear as a single memory device to the operating system." *Id.*

Figures 10-13 of Ellsberry illustrate different memory module configurations "that can be built using combinations of the control unit and bank switch." EX1073, ¶[0052]; *see also* EX1074, pp.77-81 (Final Written Decision discussing relationship of Figures 2, 5-6, and 10-13).

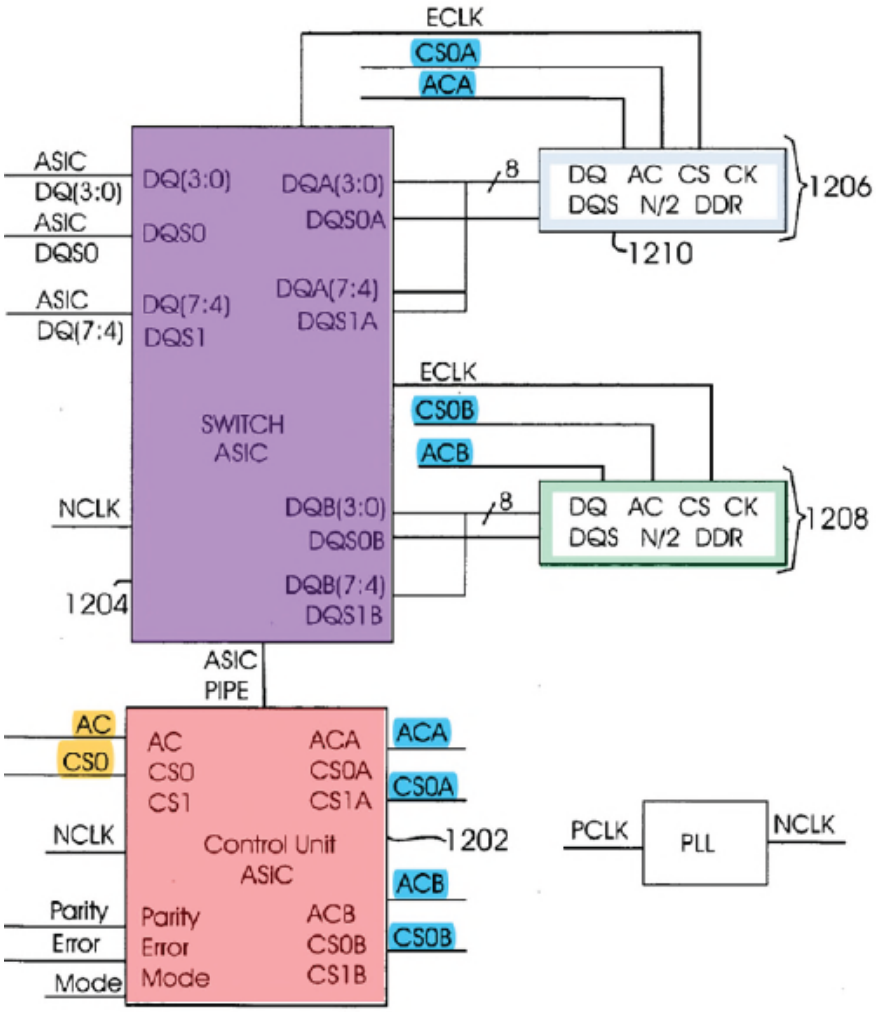



Fig. 12

EX1073, Fig.12. For example, "FIG. 12 illustrates...one control unit 1202 [(red)] and one bank switch 1204 [(purple)]...to control two memory banks 1206 [(light blue frame)] & 1208 [(light green frame)], each memory bank having one memory device 1210." *Id*. ¶[0055], Fig.12; EX1003, ¶150. The control unit (1202, red) receives a single chip-select signal (CS0, orange) to control a single memory rank, and generates two chip-select signals (CS0A and CS0B, blue) for two memory ranks. *Id*.

### D. Halbert (EX1078)

U.S. Patent No. 7,024,518 ("Halbert"), filed March 13, 2002, is prior art at least under §102(e). EX1078; EX1003, ¶151. Halbert discloses "a new memory module architecture" that can be used in "a typical memory system" such as Figure 1 below. EX1078, Abstract, 1:31-2:46, Fig.1 (below); EX1003, ¶¶153-156.

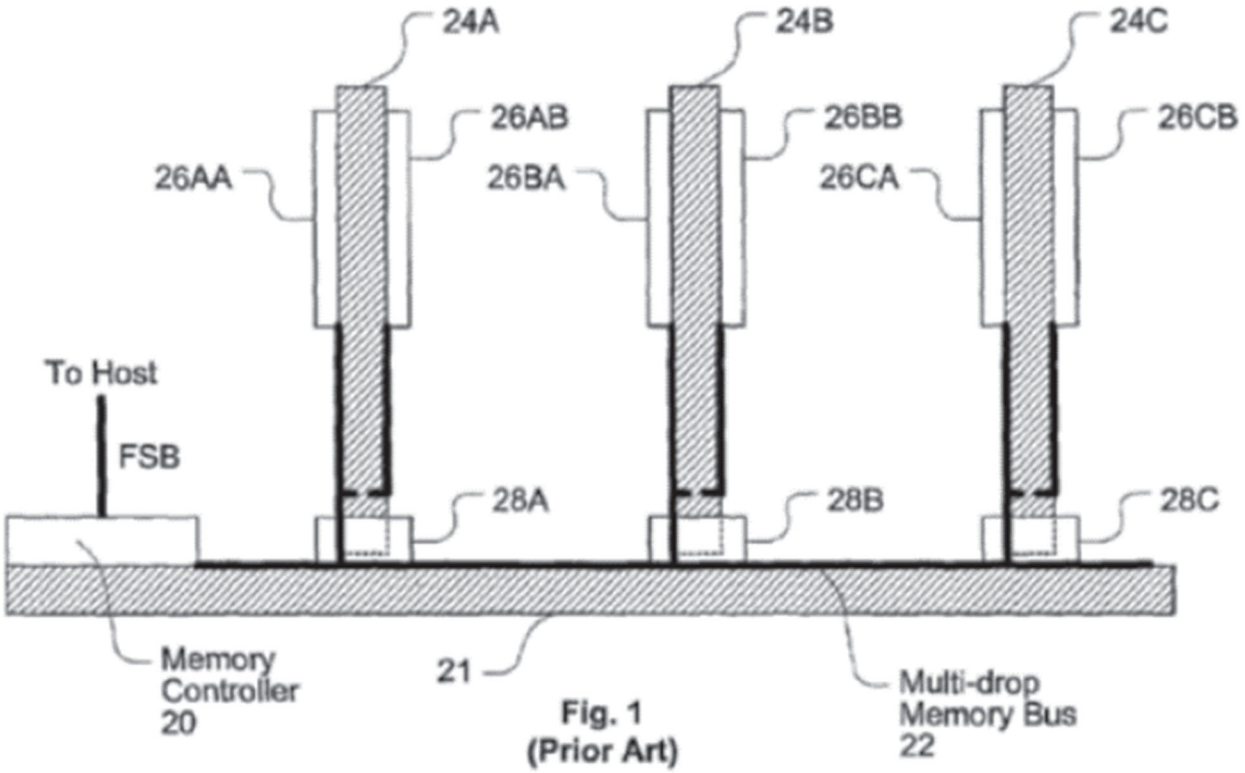
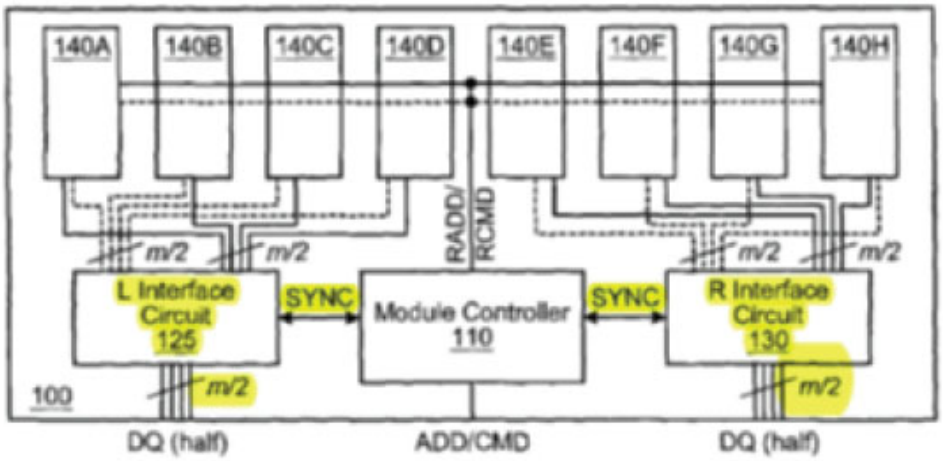



Fig. 1
(Prior Art)

Halbert's proposed memory module (below) can "allow the memory devices to be isolated from the full capacitive loading effects of the system memory data bus," EX1078, 3:60-4:2, while being "compatible with an existing memory controller/bus and with existing memory devices," *id*., 3:48-57; *see also id*., 3:42-4:35, 6:1-4.

Fig. 7



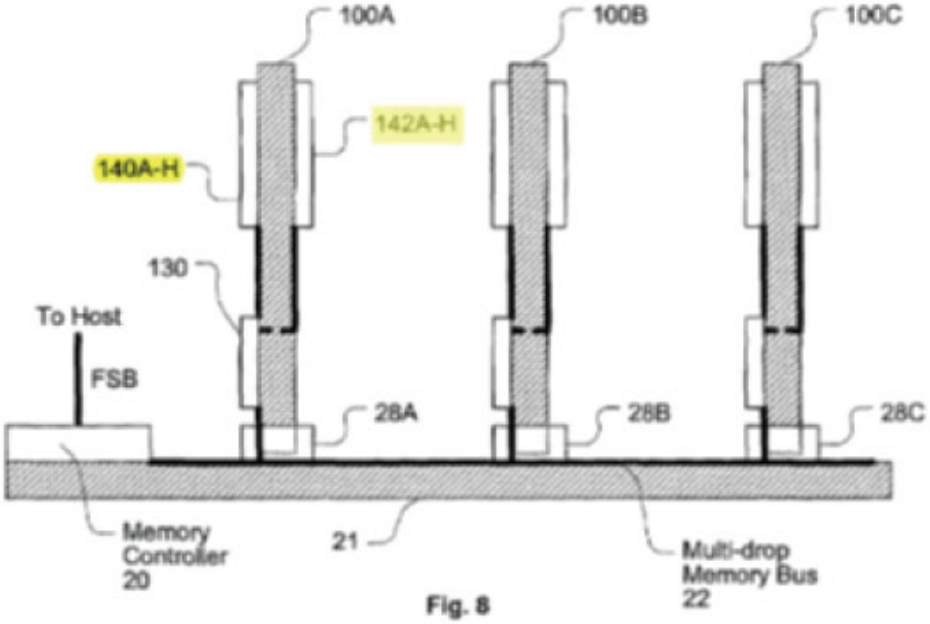
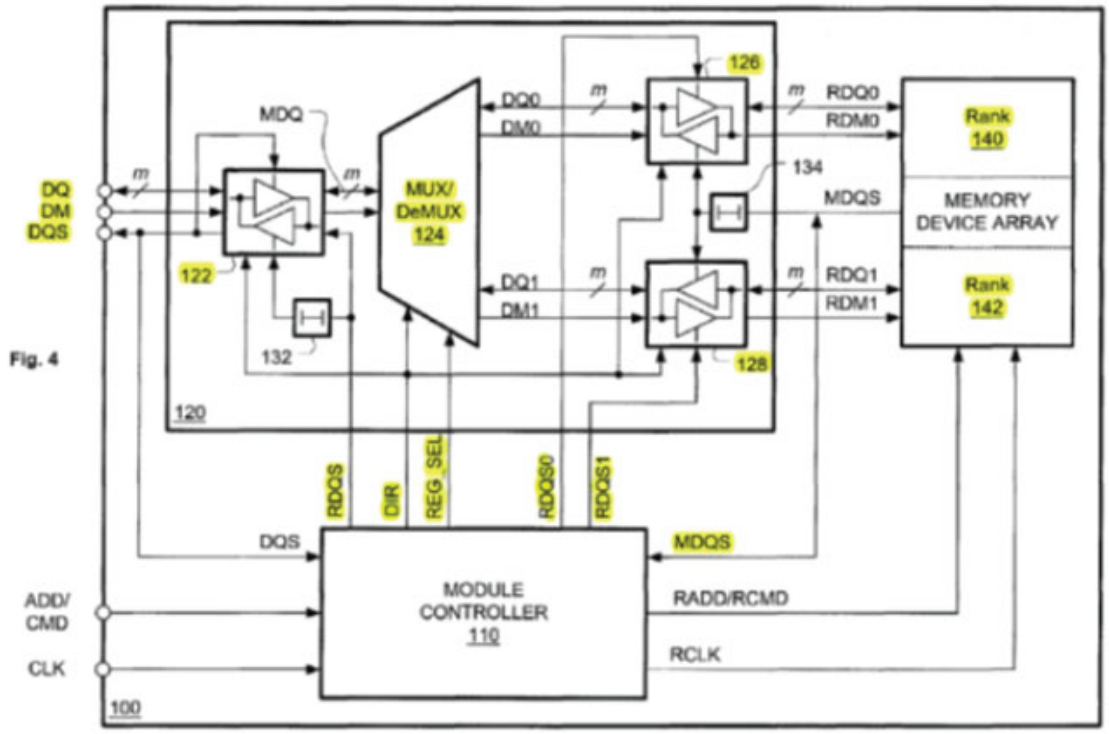




Fig. 8

*Id*., 7:31-61, Figs.7-8; EX1003, ¶¶157-158.

Halbert's module 100 (above and below) includes a module controller 110 that registers the address and command signals (ADD/CMD), and controls data interface circuits 125 and 130 (above) that communicate data between the system memory bus 22 and memory devices in ranks 140 and 142. EX1078, 4:36-5:65, 7:31-61, Fig.4; EX1003, ¶159. Interface circuits 125 and 130 (above) can each be

implemented as data interface circuit 120 in Figure 4 (below), except with half the number of data signal lines. *Id*., 7:37-40; EX1003, ¶160.




EX1078, Fig.4. Interface circuit 120 has a multiplexer/demultiplexer 124 that selectively directs data signals through registers 126 or 128 to or from rank 140 or 142, respectively. *Id*., 5:6-22; EX1003, ¶¶161-164.

## VI. CLAIM CONSTRUCTION

Except for the term "rank," discussed below, Petitioner contends for purposes of this proceeding that no further construction is needed. While Netlist appears to have interpreted some of the other claim terms unduly broadly for purposes of infringement, *see*, *e.g*., EX1085, pp.31-45; EX1088, pp.30-43, even

though a narrower interpretation may be more reasonable, the claims are obvious under either interpretation, so no further construction is needed. EX1003, ¶133.

### A. "rank"

A POSITA would have understood that "rank" refers to "an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module." EX1003, ¶126. This is consistent with the claim language (e.g., claim 1's "including at least one [first/second] memory integrated circuit in the [first/second] rank[,]" EX1001, 37:32-38); the specification (e.g., "The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width....[T]he ranks of a memory module are selected or activated by....rank-select signals, also called chip-select signals," *id*., 2:59-62); and the JEDEC standard, EX1064, p.6 ("Chip Select:…. $\overline{CS}$ provides for external ***Rank*** selection on systems with multiple ***Ranks***."). EX1003, ¶¶124-128.

As already recognized by the Board, the term "bank" (or "physical bank") was also sometimes used to refer to what is now typically called a "rank." EX1003, ¶129; EX1048, pp.13-14, 20, 28 (invalidating claims to "ranks" based on prior-art "banks"); *compare* EX1060, p.7 (chip-select for "bank"), *with* EX1064, p.6 (chip-select for "[r]ank"); *see also* EX1062, pp.6, 10-16 (chip-selects for

"physical banks"). Thus a POSITA would understand that "bank" and "physical bank" could mean the same thing as "rank" (given the "chip-select signal"):

**10.2.2 Rank**

Figure 10.5 shows a memory system populated with 2 ranks of DRAM devices. Essentially, a *rank* of memory is a *"bank"* of one or more DRAM devices that operate in lockstep in response to a given command. However, the word *bank* has already been used to describe the number of independent DRAM arrays within a DRAM device. To lessen the confusion associated with overloading the nomenclature, the word *rank* is now used to denote a set of DRAM devices that operate in lockstep to respond to a given command in a memory system.

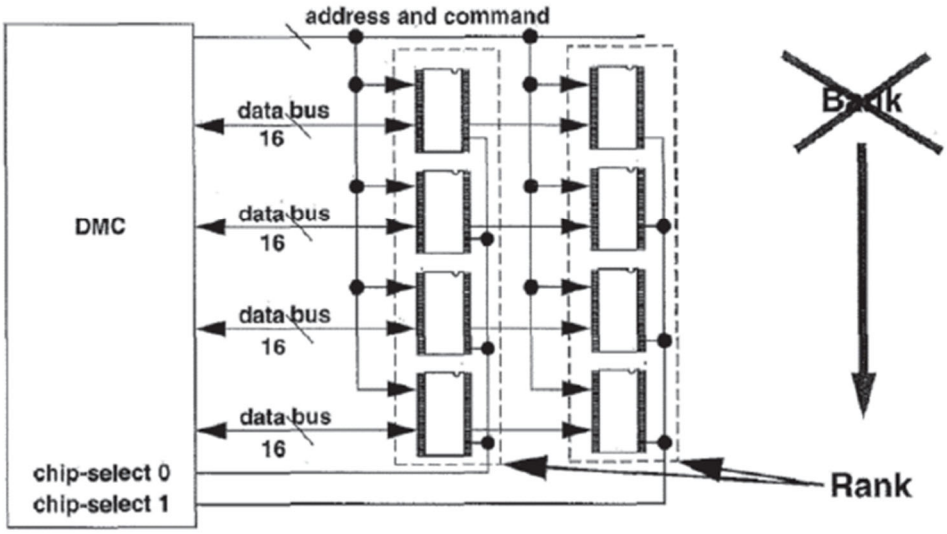



FIGURE 10.5: Memory system with 2 ranks of DRAM devices.

EX1070, p.413; *see also* EX1069, pp.4 n.3, 9; EX1003, ¶129.

A "rank" comprises "one or more DRAM devices." EX1003, ¶¶127, 130¬131; EX1070, p.413; EX1058, 37:32-38 ("at least one"); EX1023, pp.28-33 (rejecting Netlist's argument to the contrary). The 417 Patent describes an

embodiment with one memory device in each "rank." EX1003, ¶130; EX1001, 19:13-23 (disclosing that "[i]n certain embodiments, the command signal is passed through to the ***selected rank only***" and "sent to ***only one memory device*** or the other memory device so that data is supplied from one ***memory device*** at a time"). In this embodiment, the bit width of the "rank" would be the same as the bit width of the memory device, for example 16 bits. EX1003, ¶130. The 417 Patent explains that "memory devices...having bit widths of 4, 8, 16, 32, as well as other bit widths[] are compatible." EX1001, 6:56-58.

## VII. ARGUMENT

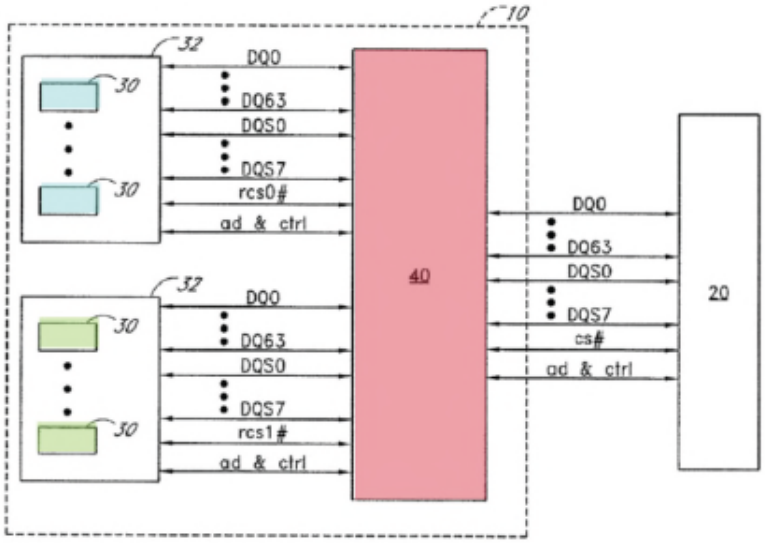
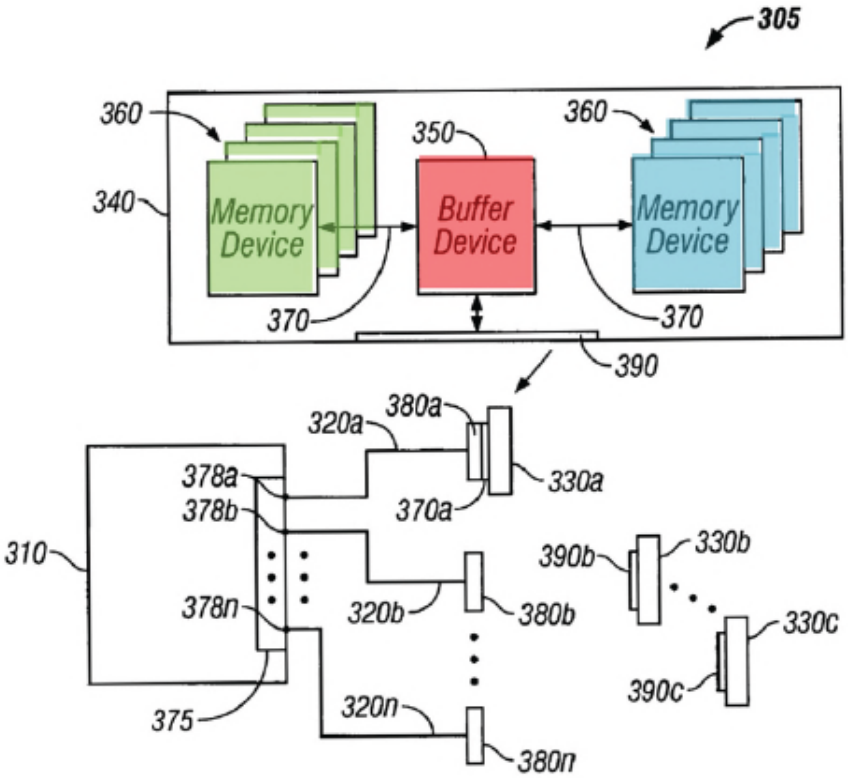
### A. Ground 1

Ground 1 renders obvious claims 1-15.

#### 1. Ground 1 combination: Perego (EX1071) and JESD79-2 (EX1064)

Ground 1 combines Perego (EX1071) with JESD79-2 (EX1064). EX1003, ¶¶177-187.

As shown below, Perego is similar to the 417 Patent, which discloses a "circuit 40" (red) that "selectively ***isolates*** the loads of some (e.g., one or more) of the ranks" (blue and green) "of the memory module 10 from the computer system." EX1001, 7:61-8:4. Perego similarly discloses a "buffer device 350" (red) that "transceives and ***provides isolation*** between...signals interfacing to the plurality of memory devices 360[]" (blue and green). EX1071, 6:12-15.

| | |
|---|---|
| 417 Patent |  <br>FIG. 1 |
| Perego |  <br>FIG. 3B |

The 417 Patent explains that its circuit 40 can be part of the same component as a register 230, EX1001, 16:64-17:3, that "receives and buffers a plurality of command signals and address signals...and transmits corresponding signals to the appropriate memory devices 30," *id*., 16:58-63. As explained below, Perego similarly explains that its buffer device 350 can perform these functions. *See, e.g*., EX1071, 5:6-15, 6:12-33, 13:18-24, Figs.5A-5B; *see also* claim elements [1.c.1]-[1.c.4] (pp.43-63), [1.e.1]-[1.e.3] (pp.85-94); EX1003, ¶¶234-273, 324-353.

Both Perego and the 417 Patent disclose that their memory modules can use DDR2 memory devices. EX1071, 3:62-4:12, 8:1-4 ("DDR"), 10:54-67 ("DDR2"); EX1001, 6:51-:55 ("DDR-1, DDR-2"), 23:22-25 ("DDR1, DDR2"). As discussed above (pp.9-10), the JEDEC standard for DDR2 memory devices is JESD79-2 (EX1064).

Accordingly, a POSITA would have been motivated to combine the teachings of JESD79-2 with the memory module described in Perego. EX1003, ¶178. A POSITA would have known about and been familiar with the JEDEC standards, including JESD79-2 as discussed above (pp.9-10), and would have recognized the relevance of these standards given Perego's references to using DDR2 memory devices. *Id*. For example, JESD79-2 discloses specific ways to issue read and write commands to DDR2 memory devices, including using "row address strobe, column address strobe, etc., and address lines" as referenced in

Perego, EX1071, 9:58-:60. *See, e.g.*, EX1064, pp.6, 24-33, 49. Accordingly, a POSITA would have been motivated to consult JESD79-2—including its details regarding memory transactions, such as read and write operations, for JEDEC-compliant memory devices—to implement Perego's system with JEDEC-compatible memory devices. EX1003, ¶178.

Furthermore, Perego discloses "exploit[ing] features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices," EX1071, 6:34-43, which would have motivated a POSITA to turn to JESD79-2 to implement Perego's system in a way that is compatible with existing generations of memory devices (specifically DDR2 memory devices). EX1003, ¶179. A POSITA would have also recognized that applying JESD79-2's teachings to Perego would have resulted in a predictable variation of Perego, which would improve similar devices in the same way and not yield unexpected results or challenges in implementation. *Id*. Indeed, the very purpose of the JEDEC standards is "to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products." EX1064, p.Cover-2.

In applying the teachings of JESD79-2 to Perego, a POSITA would have been knowledgeable about other JEDEC standards, as noted above (pp.9-10). These standards would have included, for example, JESD21-C, which had

standardized a registered DIMM format for DDR memory devices, specifying the input and output signals and their functions on the memory module, and the corresponding assignments for socket/connector pins. EX1003, ¶¶180-183; EX1062, pp.1, 5-9; EX1066, pp.1, 4-8. Indeed, Perego discloses an upgradeable memory system that includes interfaces for DIMM and other removable memory modules, EX1071, 1:58-2:6 (discussing DIMM format disclosed by U.S. Patent No. 5,513,135, EX1081), along with a need for "flexible and cost effective upgrade capabilities," EX1071, 2:26-29, 6:34-43. *See* EX1003, ¶180. A POSITA would have therefore been motivated to implement Perego's memory modules in a registered DIMM format with DDR memory devices that fits into DIMM connectors and uses DIMM module input signals, according to JEDEC standards, including JESD21-C and JESD79-2. EX1003, ¶¶180-183. Perego also discloses that its module includes the functionality of a serial presence detect (SPD) consistent with "conventional DIMM modules" to store information used to configure memory devices upon system startup, EX1071, 12:20-34, and which "provides the configurable width buffer and/or module capabilities to the memory system," *id*., Abstract. A POSITA would therefore have understood that Perego's module would be compatible with JEDEC's SPD requirements, e.g., EX1062, pp.68-70; EX1066, pp.94-96, to allow the system memory controller to read, understand, and properly initialize and use Perego's module. EX1003, ¶184.

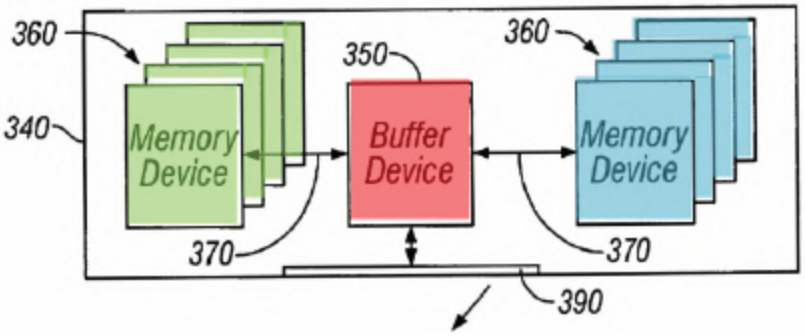
For at least these reasons, a POSITA would have been aware of JESD79-2 and related JEDEC standards and understood their disclosure, and would have been motivated to combine JESD79-2 with Perego in order to implement Perego's modules using JEDEC-compliant memory devices, such as DDR2 memory devices, to allow these modules to be used in JEDEC-compliant memory systems, such as those using DIMM modules of the format described by JESD21-C. EX1003, ¶185. A POSITA would have understood that the combination of Perego and JESD79-2 merely used familiar elements according to known methods described in Perego and the JEDEC standards, including JESD79-2, yielding predictable results, namely memory modules like Perego's including memory devices operating according to the familiar JEDEC standards. EX1003, ¶186.

### 2. Independent Claim 1

#### *a) [1.a] Preamble*

##### *(1) [1.a.1] Memory Module*

To the extent the preamble is limiting, Ground 1 teaches "[a] *memory module*," e.g., Perego's memory subsystem 340, buffered module 395, and memory modules 400, 450, and 470, as shown in Figures 3B (partially below) and 3C-4C (below). EX1071, 1:21-23, 6:57-60, 7:30-33, 9:26-33, Title, Abstract; EX1003, ¶¶203-207.


360
340
Memory Device
350
Buffer Device
360
Memory Device
370
370
390

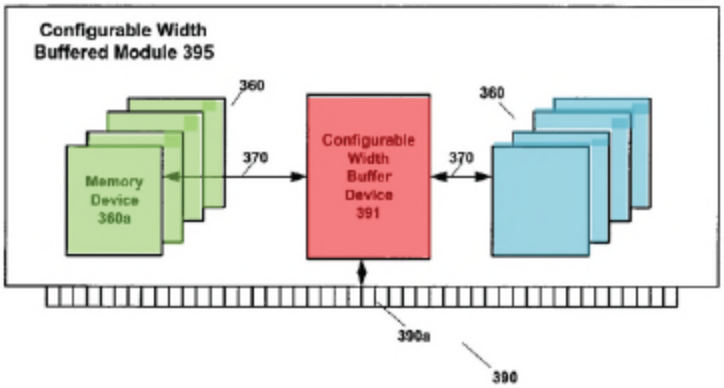

Configurable Width Buffered Module 395
360
Memory Device 360a
370
Configurable Width Buffer Device 391
370
360
390a
390

Fig. 3C

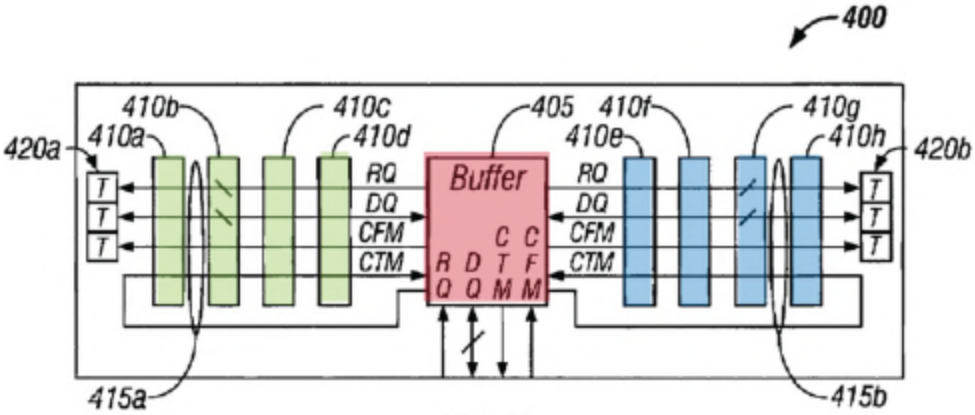

400
420a
410a
410b
410c
410d
405
410e
410f
410g
410h
420b
Buffer
RQ
DQ
CFM
CTM
RQ
DQ
CFM
CTM
R Q
D Q
C T M
C F M
T
T
T
T
T
T
415a
415b

FIG. 4A

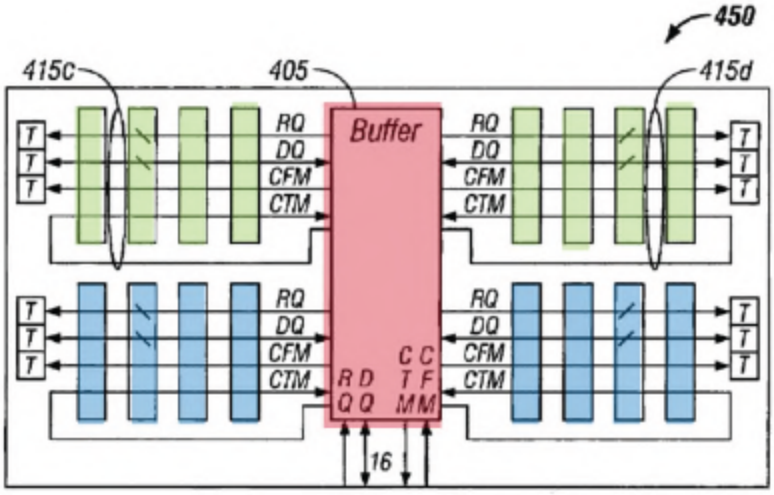



FIG. 4B

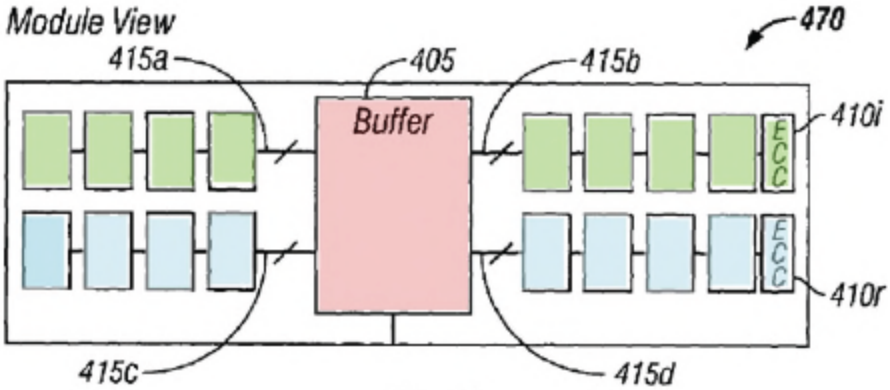



FIG. 4C

As demonstrated by comparing Figures 3B-4C of Perego (above) with Figure 1 of the 417 Patent (below), Perego's buffered module has substantially the same structure as that of the 417 Patent: a buffer device (red) communicates with a system memory controller on a system memory bus and also with different sets of memory devices (green, blue) on the module using a respective data bus for each set of memory devices. EX1003, ¶206.

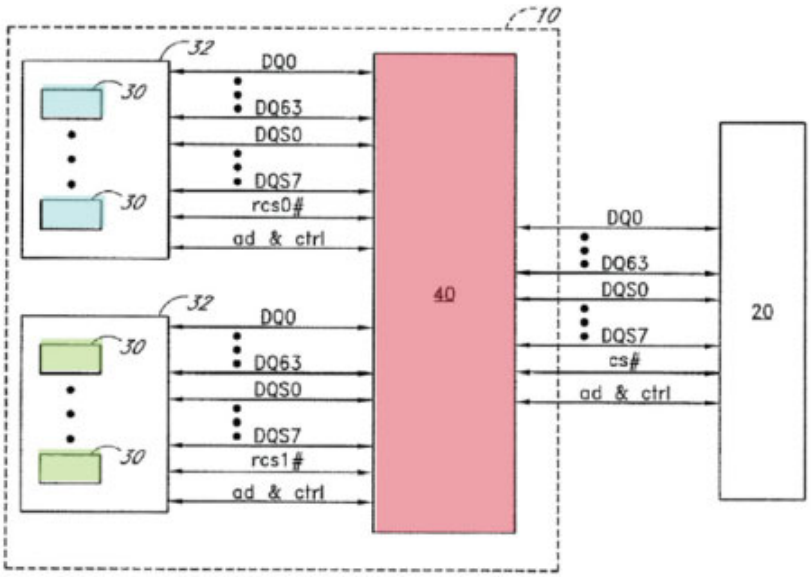



**FIG. 1**

EX1001, Fig. 1.

### *(2) [1.a.2] Operable in a Computer System*

Ground 1 teaches that the memory module is "*operable in a computer system*," e.g., Perego's teachings of a "personal computer or server" including memory system 305 (below). EX1071, 3:13-22, 4:65-5:15; EX1003, ¶¶210-211. Perego's module provides "upgrade flexibility," EX1071, 3:23-28, 6:34-37, and thus is compatible with prior-art computers using a traditional bus for data, address, and control signals consistent with the JEDEC standards, *id*., 1:34-40, 2:22-25 ("bussed approaches...permit[]...upgradeability"), Figs.1, 2A-2B; EX1064, p.6; EX1062, p.6; EX1066, p.6. EX1003, ¶¶212-213.

Ground 1 also teaches "*to communicate data* [through a respective link, e.g., 320a] *with a memory controller* [e.g., memory controller 310] *of the computer system via a N-bit wide* [N=data width=$W_{DP}$=e.g., 64 bits] *memory bus* [e.g., in link 320a, which communicates "data, addressing and control information" between memory controller 310 and memory module 340] *in response to read or write memory commands* [e.g., read or write commands that comply with JESD79-2, EX1064, pp.24-33, 49] *received from the memory controller* [e.g., from memory controller 310 through the link 320a]." *See, e.g.*, EX1071, Fig.3B (below), 3:12-22, 3:62-4:12, 4:65-5:15, 6:15-25, 9:50-60, 14:16-51; EX1003, ¶¶208-219.

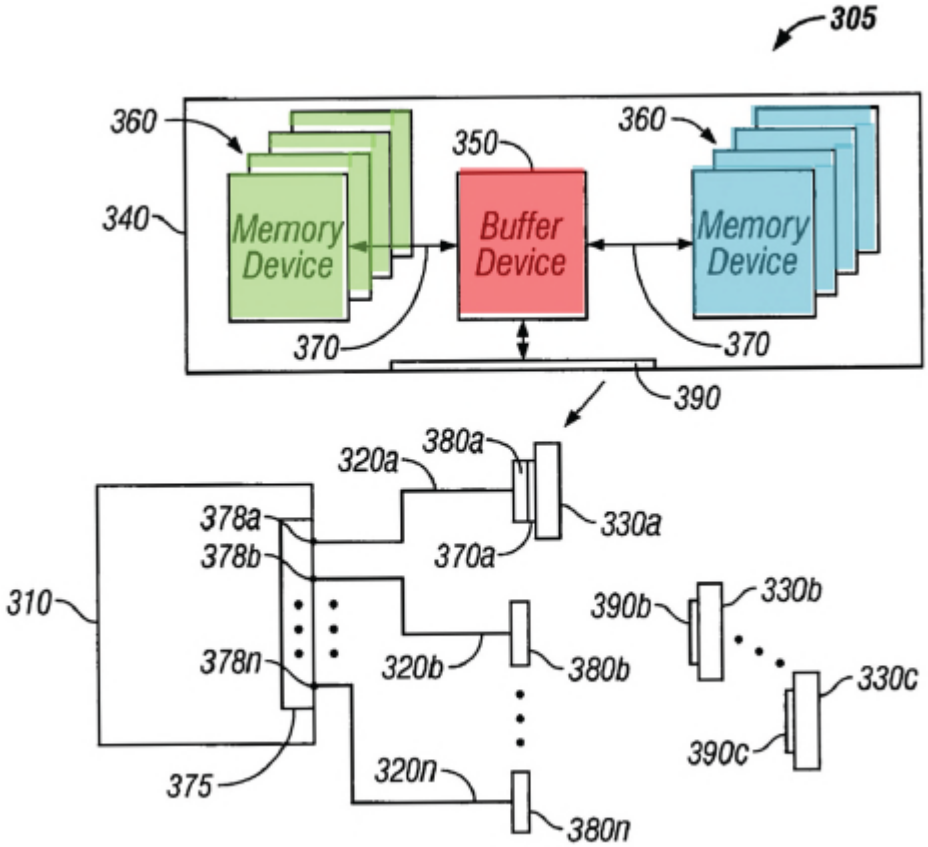



FIG. 3B

More specifically, Perego discloses that its "*memory bus*" (e.g., in link 320a) can have a data width of $W_{DP}$=16, 32, 64, or 128 bits "*to communicate data with a memory controller* [310] *of the computer system*." EX1071, Figs.4A-4B ("DQ" data lines), Figs.5A-5B (below), 3:41-47 ("one or more busses"), 5:6-24 ("bus"), 11:8-12, 14:16-51; EX1003, ¶¶211-215. A POSITA would have understood that a data width of $W_{DP}$=64 corresponds to the 64-bit data width of a JEDEC-compliant registered DIMM module. EX1062, p.5; EX1003, ¶215.

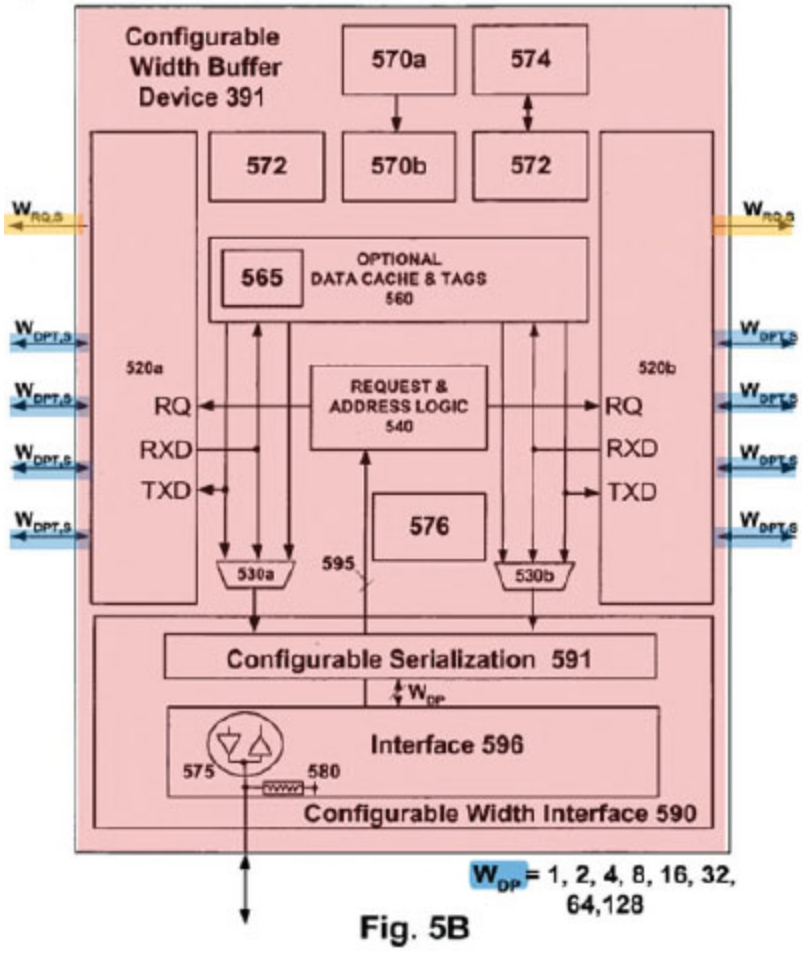


Fig. 5B

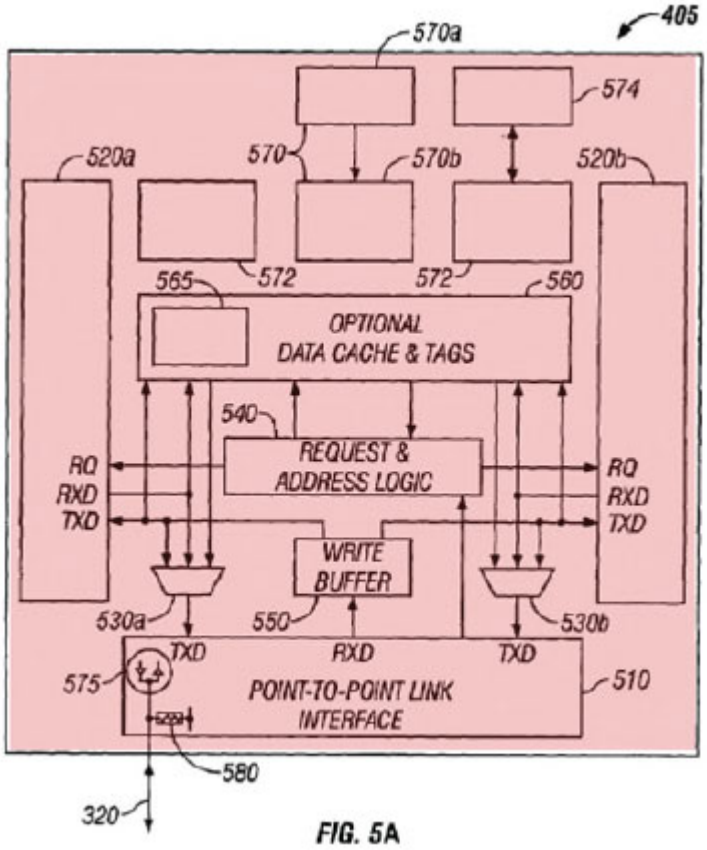



FIG. 5A

Further, a POSITA would have understood that Perego's module and corresponding memory devices communicate data "*in response to memory commands received from the memory controller*." EX1003, ¶¶216-218. For example, Perego discloses that "[i]n a normal memory read operation" memory devices 360 transmit data in response to controller 310 "transmit[ting]...signals to one or more, or all of memory devices 360." EX1071, 6:15-25, Fig.3B; *see also id*., 3:62-4:12 (describing memory devices storing and retrieving data "as part of a write or read command"). Perego's disclosure of "control lines (RQ) transport[ing] control (e.g., read, write, precharge...) information," EX1071, 9:50¬60, and the use of "row address strobe [RAS], column address strobe [CAS], etc.," *id*., 9:58-60

also teaches that such control information includes read and write commands from the memory controller. EX1003, ¶217. A POSITA would also have understood from their own knowledge of JEDEC standards, including JESD79-2, the specific ways to issue read and write commands to Perego's DDR2 memory devices, and would have been motivated to apply those teachings. EX1003, ¶218; EX1064, pp. 24-33 (Section 2.2.4, "Read and Write Access Modes"); *id*., pp.6, 49 & n.1 (showing Chip Select "CS," Row Address Strobe "$\overline{RAS}$," and Column Address Strobe "$\overline{CAS}$" signals used to convey memory read and write commands).

### *(3) [1.a.3] Signal Lines*

Ground 1 teaches "*the memory bus* [e.g., in link 320a, which communicates "data, addressing and control information" between memory controller 310 and memory module 340] *including address and control signal lines and data signal lines*." EX1003, ¶¶220-224; EX1071, 5:12-15 ("One of memory subsystem ports 378a-378n includes I/Os, for sending and receiving data, addressing and control information over one of point-to-point links 320a-320n"), 5:21-24 ("memory subsystems are connected to a memory subsystem port via a bus (i.e., a plurality of signal lines)"), Fig.3B (below).

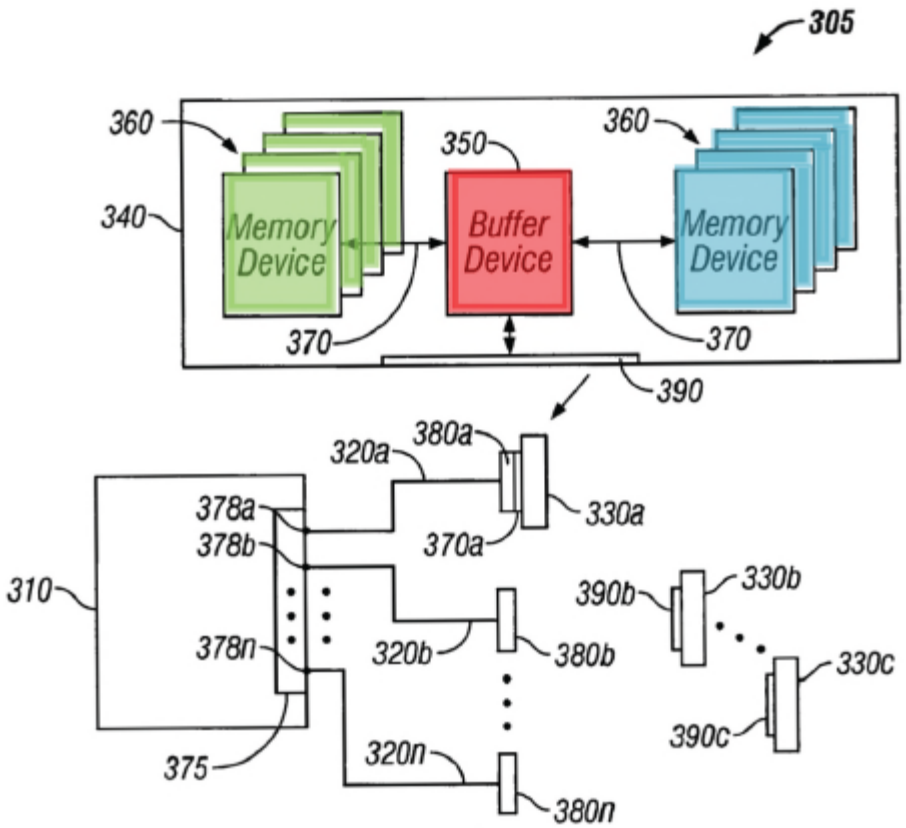



FIG. 3B

*See also* EX1071, Figs.4A-4B (showing RQ and DQ lines connecting to the memory bus); 9:43-45, 9:58-60 ("Signal lines of channels 415a and 415b include control lines (RQ), data lines (DQ) and clock lines (CFM, CTM)....[C]ontrol lines (RQ) may comprise individual control lines, for example...address lines."). EX1003, ¶222.

### *(4) [1.a.4] Comprising*

Ground 1 teaches "*the memory module* [above, pp.33-36] *comprising*" [below, pp.42-96].

### *b) [1.b] Printed Circuit Board*

Ground 1 teaches "*a printed circuit board* [PCB] *having a plurality of edge connections* [edge connectors 390] *configured to be electrically coupled to a corresponding plurality of contacts of a module slot* [e.g., mating connectors or sockets 380] *of the computer system*." EX1003, ¶¶228-233. For example, Perego's memory modules "are incorporated onto individual substrates (e.g., ***PCBs***)...that include connectors 390a-390c" with "a plurality of contacts, conducting elements or pins," EX1071, 5:56-6:11, 7:39-41, as shown below:

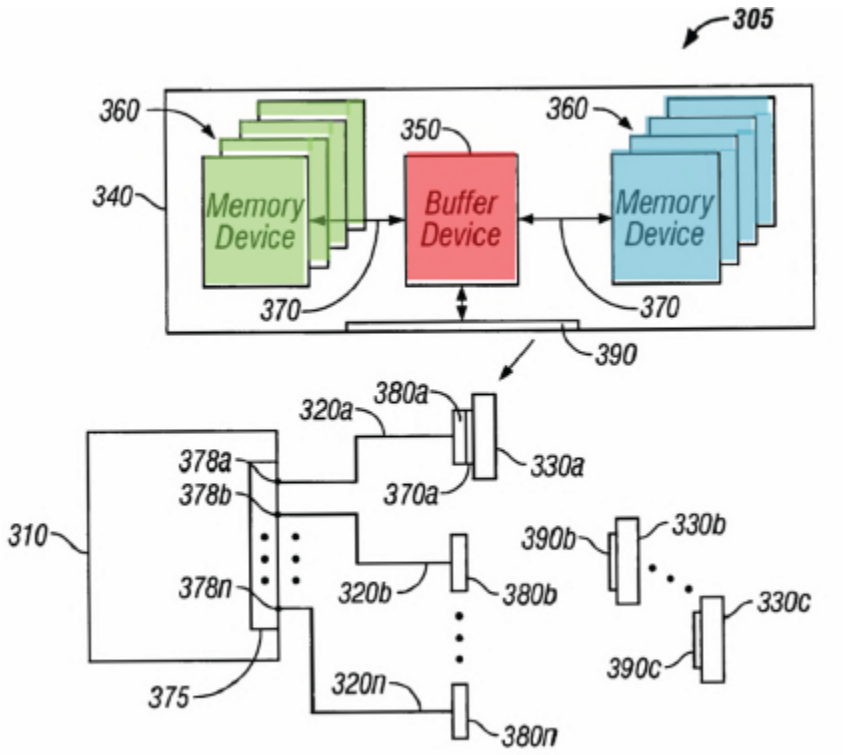



FIG. 3B

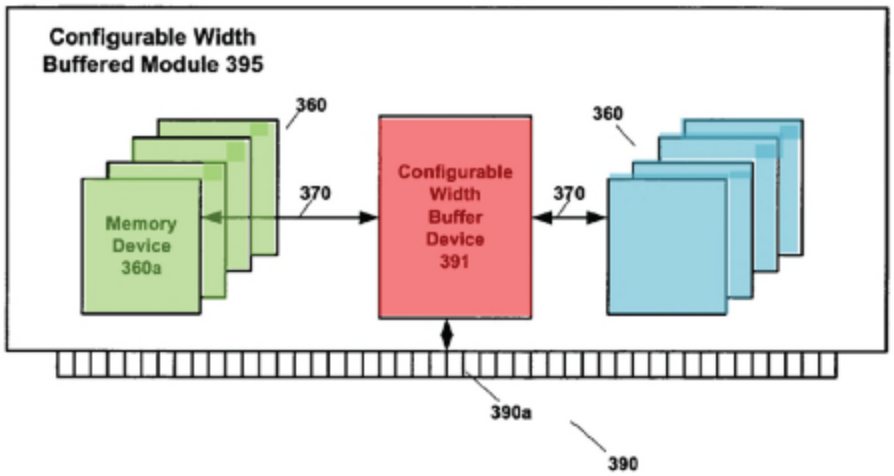



**Fig. 3C**

*Id*., Figs.3B-3C. Moreover, a POSITA would have understood from Perego that its module can be implemented in a standard DIMM format, EX1003, ¶232; EX1071, 6:34-43, 3:25-28; EX1069, p.2, and that such a DIMM format also uses a "*printed circuit board*" (PCB) with "*edge connections*" to couple to the socket of the memory system, EX1003, ¶232; EX1062, pp.29 (describing mounting on "PCB"), 66 (describing "DIMM printed circuit board" with "PCB edge connector contacts").

### *c) [1.c] Logic*

#### *(1) [1.c.1] Receive Input Address and Control Signals*

Ground 1 teaches "*logic* [e.g., in the buffer device (red, below), specifically in interface 510 and write buffer 550 (in Figure 5A's implementation, below) or in interface 590 (in Figure 5B's implementation, second below) as well as in

interfaces 520a and 520b, Request & Address Logic 540, and computation block 565] *coupled to the printed circuit board* [from [1.b] (pp.42-43), because the buffer device is coupled to the printed circuit board] *and configurable to receive a set of input address and control signals associated with a read or write memory command* [e.g., read or write commands from the memory controller that comply with JESD79-2, EX1064, pp.6, 24-33, 49] *via the address and control signal lines* [from [1.a.3] (pp.40-41), e.g., the vertical RQ lines coupled to the edge of the module in Figures 4A-4B (third below), *see* EX1071, 9:43-53] *and to output a set of registered address and control signals* [e.g., on the horizontal RQ lines in Figures 4A-4B (third below) in one or more selected channels 415 coupled to the memory devices in [1.d.1]-[1.d.3] (pp.64-84), *see* EX1071, 9:43-53] *in response to the set of input address and control signals*." EX1003, ¶¶234-243.

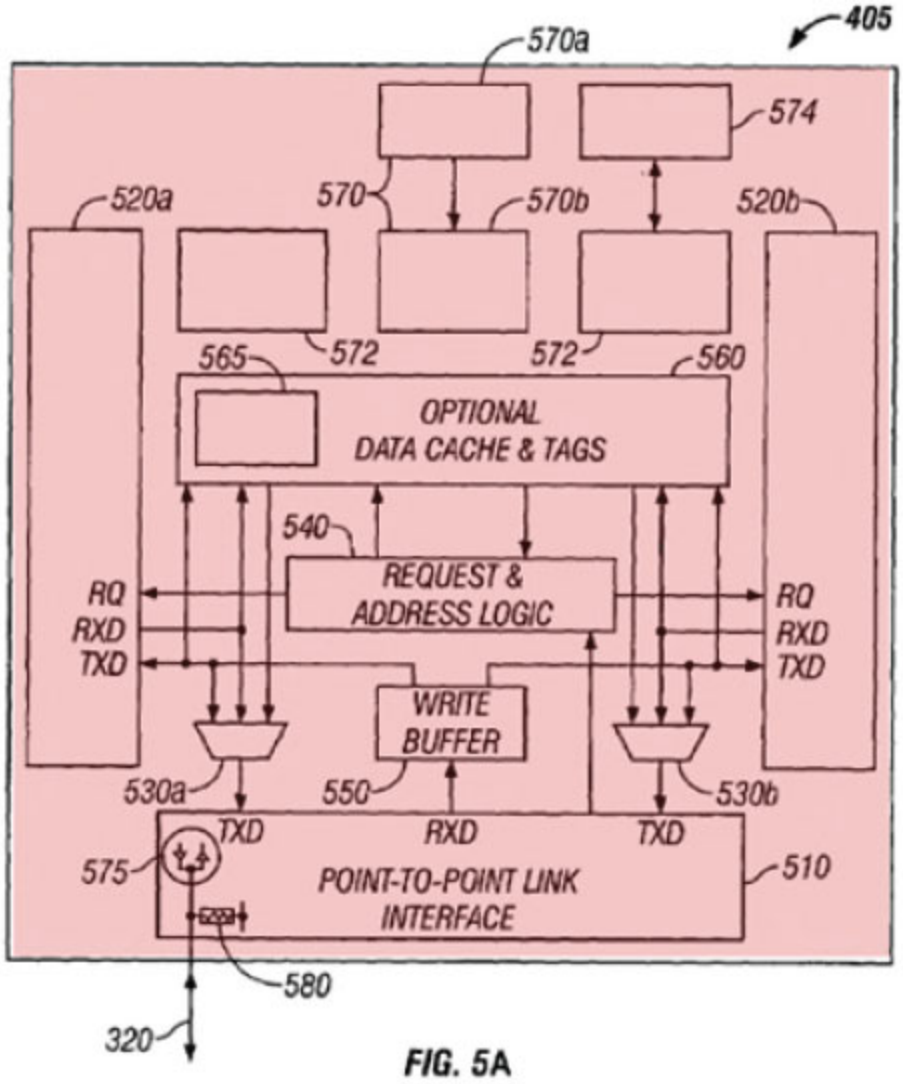

405
570a
574
520a
570
570b
520b
565
572
572
560
OPTIONAL
DATA CACHE & TAGS
540
REQUEST &
ADDRESS LOGIC
RQ
RXD
TXD
RQ
RXD
TXD
WRITE
BUFFER
530a
550
530b
TXD
RXD
TXD
575
POINT-TO-POINT LINK
INTERFACE
510
580
320

FIG. 5A

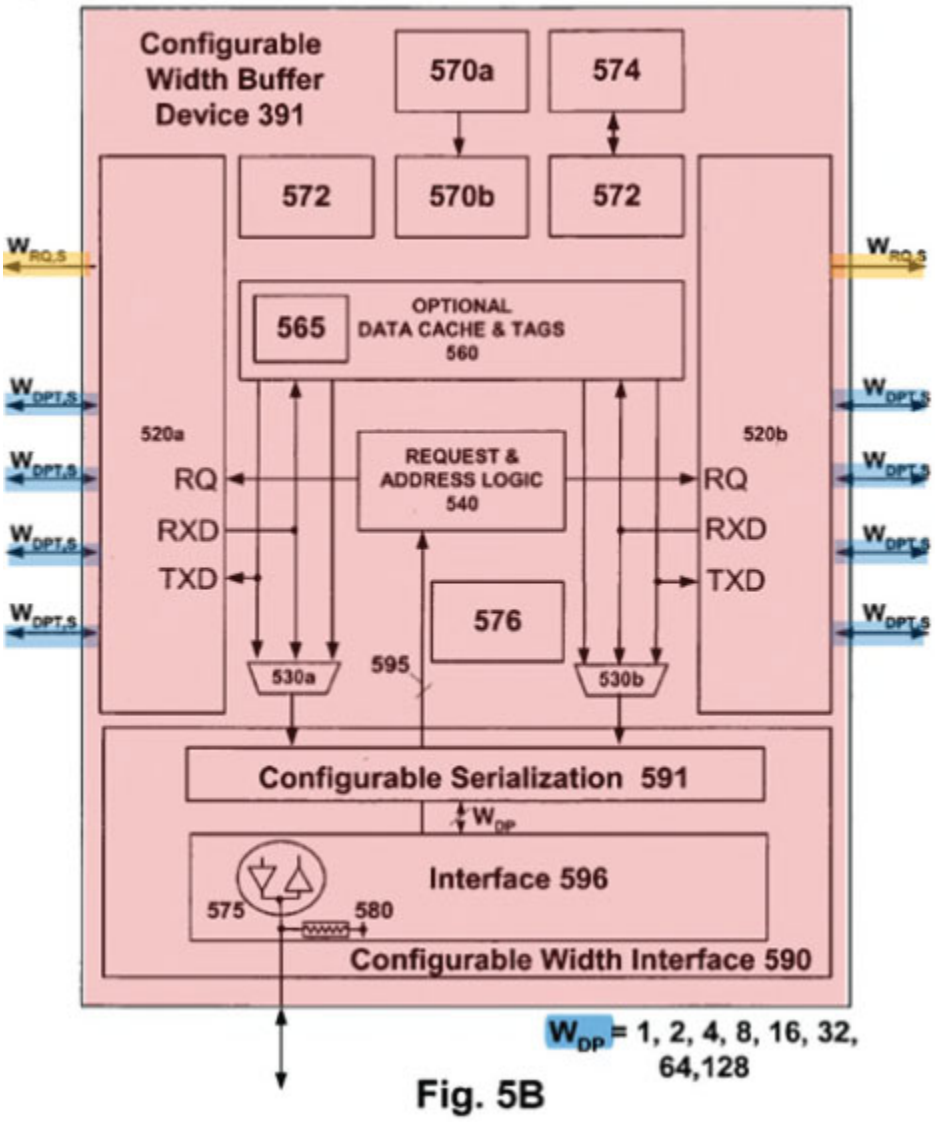

Configurable Width Buffer Device 391
570a
574
572
570b
572
565
OPTIONAL DATA CACHE & TAGS 560
520a
520b
REQUEST & ADDRESS LOGIC 540
RQ
RXD
TXD
RQ
RXD
TXD
576
530a
595
530b
Configurable Serialization 591
Interface 596
575
580
Configurable Width Interface 590
= 1, 2, 4, 8, 16, 32, 64,128

Fig. 5B

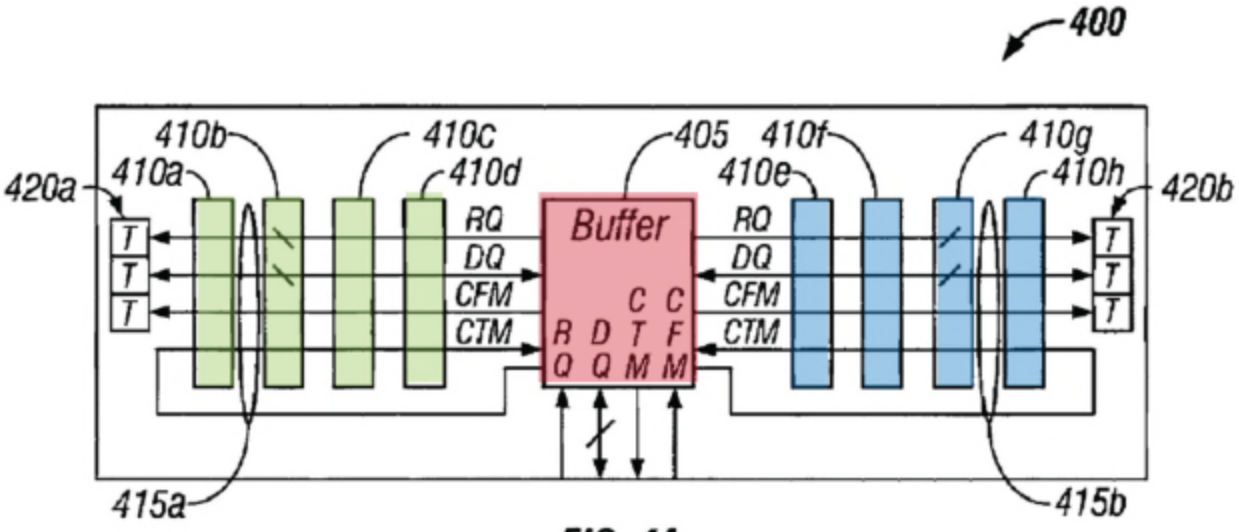

400
410b
410c
405
410f
410g
420a
410a
410d
410e
410h
420b
Buffer
RQ
DQ
CFM
CTM
RQ
DQ
CFM
CTM
C C
R D T F
Q Q M M
T
T
T
415a
415b

FIG. 4A

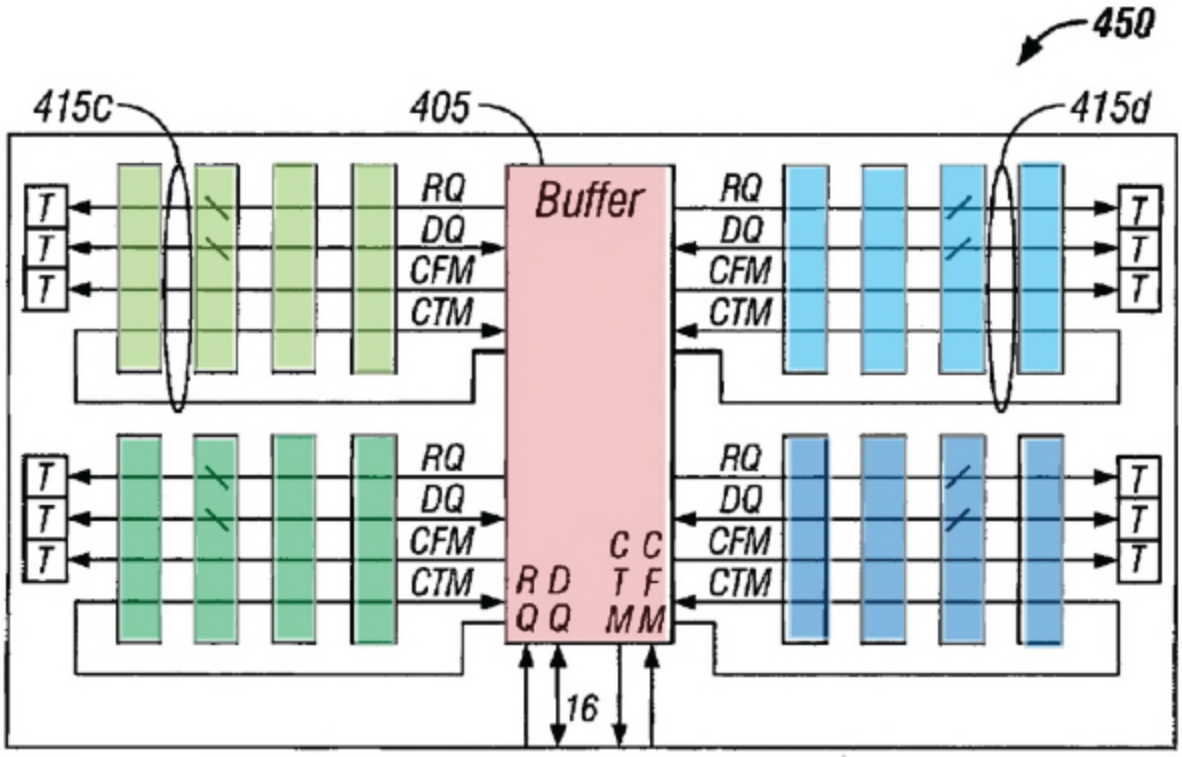

450
415c
405
415d
Buffer
RQ
DQ
CFM
CTM
RQ
DQ
CFM
CTM
C C
R D T F
Q Q M M
16
T
T
T

FIG. 4B

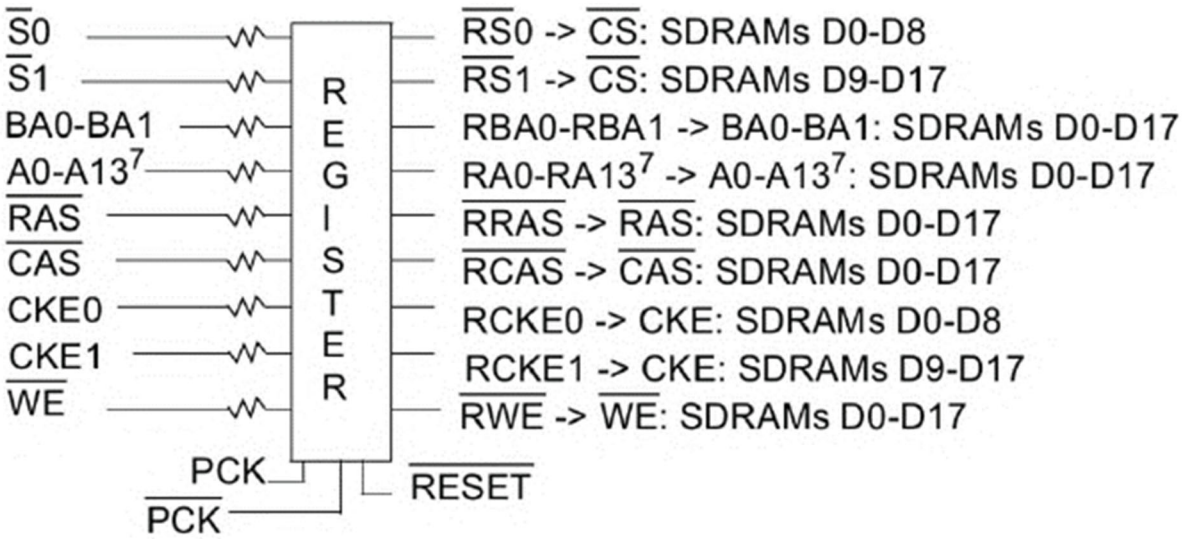
A POSITA would have understood from Perego's disclosure that "logic" is configured to receive from the memory controller "*a set of input address and control signals associated with a read or write memory command*," including "request and address information," EX1071, 4:3-6, sent on "control lines (RQ)" that include "read,write" and "address (e.g., row and column) information," *id.*, 9:50-60; EX1003, ¶238. As shown by the JESD79-2 standard below, read and write commands include both address signals (e.g., BA0-BA2, A0-A15) and control signals (e.g., CS chip select, RAS, CAS, WE). EX1064, pp.6, 49 (below); EX1003, ¶238.

**Table 10 — Command truth table.**

| Function | CKE | | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | BA0 BA1 BA2 | A15-A11 | A10 | A9 - A0 | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Previous Cycle | Current Cycle | | | | | | | | | |
| (Extended) Mode Register Set | H | H | L | L | L | L | BA | OP Code | | | 1,2 |
| Refresh (REF) | H | H | L | L | L | H | X | X | X | X | 1 |
| Self Refresh Entry | H | L | L | L | L | H | X | X | X | X | 1 |
| Self Refresh Exit | L | H | H | X | X | X | X | X | X | X | 1,7 |
| | | | L | H | H | H | | | | | |
| Single Bank Precharge | H | H | L | L | H | L | BA | X | L | X | 1,2 |
| Precharge all Banks | H | H | L | L | H | L | X | X | H | X | 1 |
| Bank Activate | H | H | L | L | H | H | BA | Row Address | | | 1,2 |
| Write | H | H | L | H | L | L | BA | Column | L | Column | 1,2,3, |
| Write with Auto Precharge | H | H | L | H | L | L | BA | Column | H | Column | 1,2,3, |
| Read | H | H | L | H | L | H | BA | Column | L | Column | 1,2,3 |
| Read with Auto-Precharge | H | H | L | H | L | H | BA | Column | H | Column | 1,2,3 |
| No Operation | H | X | L | H | H | H | X | X | X | X | 1 |
| Device Deselect | H | X | H | X | X | X | X | X | X | X | 1 |
| Power Down Entry | H | L | H | X | X | X | X | X | X | X | 1,4 |
| | | | L | H | H | H | | | | | |
| Power Down Exit | L | H | H | X | X | X | X | X | X | X | 1,4 |
| | | | L | H | H | H | | | | | |

A POSITA would have also understood from Perego's disclosure of how buffer device 350, memory devices 360, and controller 310 receive and respond to data, including address and control signals, that Perego's buffer device "*register[s]*" address and control signals similar to a JEDEC-compliant conventional registered DIMM (below, showing the Register on the module receiving on the left side input signals from the memory controller, including address signals (e.g., BA0-BA1, A0-A13) and control signals (e.g., S0-S1 chip select and RAS, CAS, and WE), and outputting on the right side registered address

signals (e.g., RBA0-RBA1, RA0-RA13) and registered control signals (e.g., RS0-RS1 registered chip select and RRAS, RRCAS, and RWE) that are transmitted to the SDRAM memory devices). EX1003, ¶¶239-240; EX1071, 6:15-30; EX1062, p.12; *see also* EX1071, 13:54-59, Fig.5C (showing that interface 596 includes registers, similar to latches 597f-m, for interfacing with the system memory bus).




Furthermore, Perego teaches that the "*logic*" in the buffer device can perform "rank multiplication" (discussed above, pp.10-12) when "*output[ting] a set of registered address and control signals in response to the set of input address and control signals*." *See, e.g.*, EX1071 (Perego) at 14:63-65 ("The address of the transaction will determine which target subset of channels 370 will be utilized for the data transfer portion of the transaction."), 15:34-40 ("configurable width buffer device 391 may employ a configurable datapath router within interface 591 to route requests between the primary channel and the target subset of secondary

channel signal lines for each transaction… the target subset of secondary channel signal lines may be selected via address bits provided as part of the primary channel request"). Thus, for example, if the "*input address and control signals*" include two chip-select signals from the memory controller (corresponding to two ranks of higher-density memory devices), then the "*logic*" in Perego's buffer device may use those chip-select signals along with the address information from the "*input address and control signals*" to produce four chip-select signals (corresponding to four ranks of lower-density memory devices actually on the module) that are included in the "*set of registered address and control signals*" sent to the memory devices on the module. *Id*.; EX1003, ¶241. Furthermore, a POSITA would have been motivated to implement "rank multiplication" given the significant cost savings (discussed above, pp.10-12). EX1003, ¶241.

#### ***(2) [1.c.2] Input Address and Control Signals***

Ground 1 teaches "*the set of input address and control signals* [from [1.c.1] (pp.43-51)] *including a plurality of input chip select signals* [e.g., "CS" signals as part of the input read or write command from the memory controller, as required by JESD79-2, EX1064, pp.6 (first below), 24-33, 49 (second below)] *and other input address and control signals* [e.g., bank and row/column address signals (e.g., BA0-BA2, A0-A15), and RAS, CAS and WE control signals, as part of the input read or write command from the memory controller, as required by JESD79-2,

EX1064, pp.6 (first below), 24-33, 49 (second below)], *the plurality of input chip select signals including one chip select signal having an active signal value* [e.g., "L" or "Low," identifying the target rank of memory devices as seen by the memory controller for the read or write operation, *see* JESD79-2, EX1064, pp.6 (first below), 49 (second below)] *and one or more other input chip select signals each having a non-active signal value* [e.g., "H" or "High," so the other rank(s) of memory devices are "Deselected" and do not participate in the read or write operation, i.e., perform "No Operation" (or NOP), *see* JESD79-2, EX1064, pp.6 (first below), 48 ("Deselect command performs the same function as a No Operation [NOP] command."), 49 (second below)]." EX1003, ¶¶244-254; *see also* EX1069, pp.2-3 (discussing "chip-select" signals).

## 1.2 Input/Output Functional Description

| Symbol | Type | Function |
|---|---|---|
| CK, $\overline{CK}$ | Input | **Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK. Output (read) data is referenced to the crossings of CK and CK (both directions of crossing). |
| CKE | Input | **Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh. |
| $\overline{CS}$ | Input | **Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code. |
| ODT | Input | On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS, RDQS, RDQS, and DM signal for x4x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/UDQS, LDQS/LDQS, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT. |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | Input | **Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered. |
| DM (UDM), (LDM) | Input | **Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/RDQS is enabled by EMRS command. |
| BA0 - BA2 | Input | **Bank Address Inputs:** BA0 and BA1 for 256 and 512Mb, BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle. |
| A0 - A15 | Input | **Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands. |
| DQ | Input/Output | **Data Input/ Output:** Bi-directional data bus. |
| DQS, ($\overline{DQS}$) (UDQS), ($\overline{UDQS}$) (LDQS), ($\overline{LDQS}$) (RDQS), ($\overline{RDQS}$) | Input/Output | **Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15. For the x8, an RDQS option using DM pin can be enabled via the EMRS(1) to simplify read timing. The data strobes DQS, LDQS, UDQS, and RDQS may be used in single ended mode or paired with optional complementary signals DQS, LDQS, UDQS, and RDQS to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables all complementary data strobe signals. |

**Table 10 — Command truth table.**

| Function | CKE | | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | BA0 BA1 BA2 | A15-A11 | A10 | A9 - A0 | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Previous Cycle | Current Cycle | | | | | | | | | |
| (Extended) Mode Register Set | H | H | L | L | L | L | BA | OP Code | | | 1,2 |
| Refresh (REF) | H | H | L | L | L | H | X | X | X | X | 1 |
| Self Refresh Entry | H | L | L | L | L | H | X | X | X | X | 1 |
| Self Refresh Exit | L | H | H | X | X | X | X | X | X | X | 1,7 |
| | | | L | H | H | H | | | | | |
| Single Bank Precharge | H | H | L | L | H | L | BA | X | L | X | 1,2 |
| Precharge all Banks | H | H | L | L | H | L | X | X | H | X | 1 |
| Bank Activate | H | H | L | L | H | H | BA | Row Address | | | 1,2 |
| Write | H | H | L | H | L | L | BA | Column | L | Column | 1,2,3, |
| Write with Auto Precharge | H | H | L | H | L | L | BA | Column | H | Column | 1,2,3, |
| Read | H | H | L | H | L | H | BA | Column | L | Column | 1,2,3 |
| Read with Auto-Precharge | H | H | L | H | L | H | BA | Column | H | Column | 1,2,3 |
| No Operation | H | X | L | H | H | H | X | X | X | X | 1 |
| Device Deselect | H | X | H | X | X | X | X | X | X | X | 1 |
| Power Down Entry | H | L | H | X | X | X | X | X | X | X | 1,4 |
| | | | L | H | H | H | | | | | |
| Power Down Exit | L | H | H | X | X | X | X | X | X | X | 1,4 |
| | | | L | H | H | H | | | | | |

EX1064, pp.6, 49; EX1003, ¶248.

Consistent with the JESD79-2 standard above, Perego discloses that its module includes multiple sets of memory devices (e.g., "*ranks*," as discussed below for [1.d.1] (pp.64-73)), each of which can be a target of a memory read or write command, and each of which acts together in response to a memory read or write command. EX1003, ¶¶249-250; EX1071, 15:37-45 (disclosing "grouping memory devices into multiple independent target subsets (i.e. more independent

banks)"), 6:12-24 ("buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to ***one or more***, or all of ***memory devices 360*** via channels 370. ***One or more of memory devices 360*** may respond by transmitting data to Buffer device 350 which receives the data via ***<u>one</u> or more of channels 370*** and in response, transmits corresponding signals to controller 310 via point-to-point link 320a."), Figs.3C, 4A-4C (below).

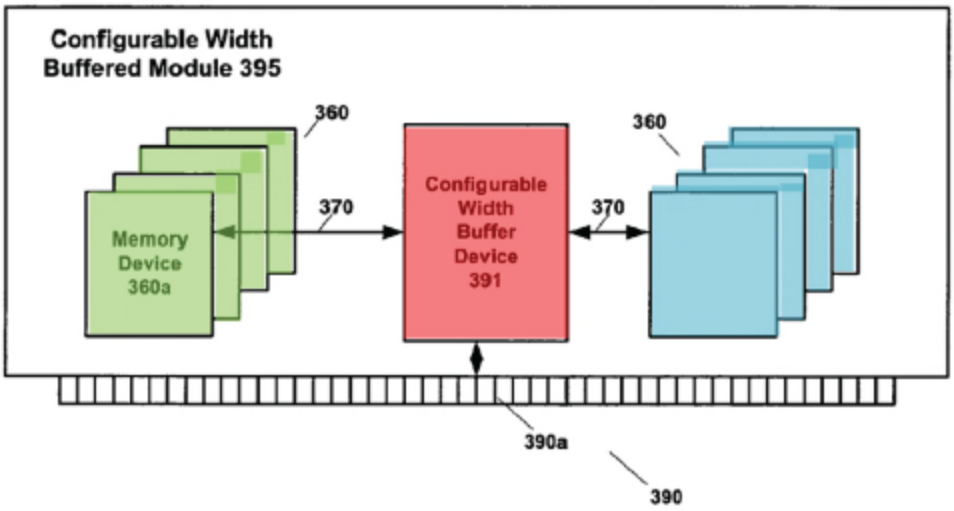



**Fig. 3C**

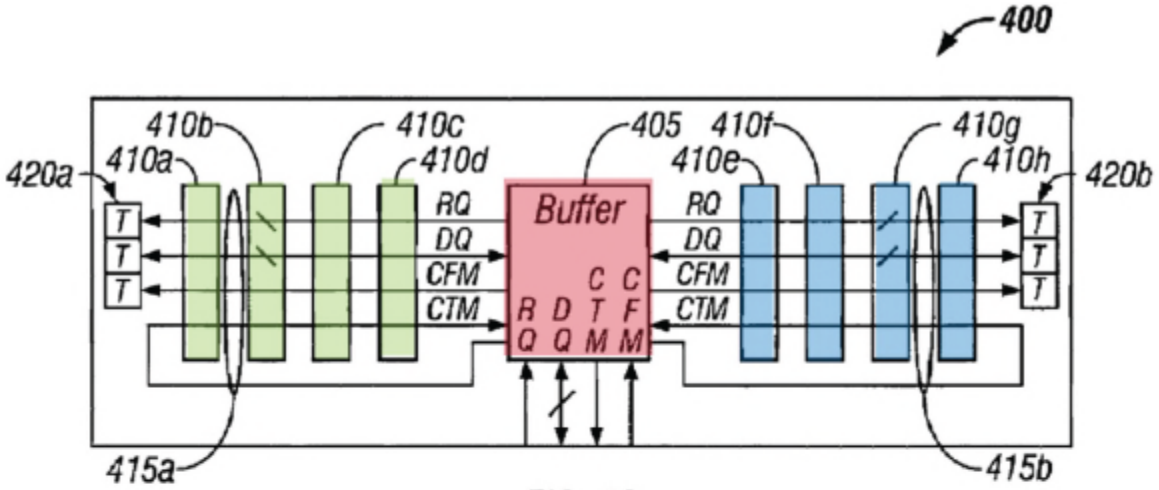

400
410b
410c
405
410f
410g
420a
410a
410d
410e
410h
420b
Buffer
RQ
DQ
CFM
CTM
RQ
DQ
CFM
CTM
T
T
T
T
T
T
415a
415b

FIG. 4A

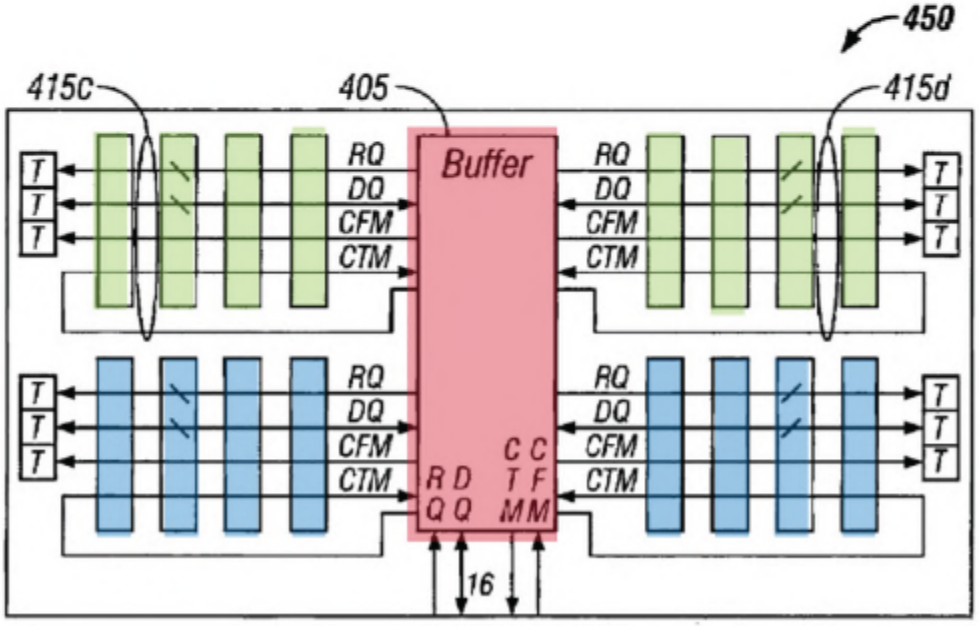

450
415c
405
415d
Buffer
RQ
DQ
CFM
CTM
RQ
DQ
CFM
CTM
T
T
T
16

FIG. 4B

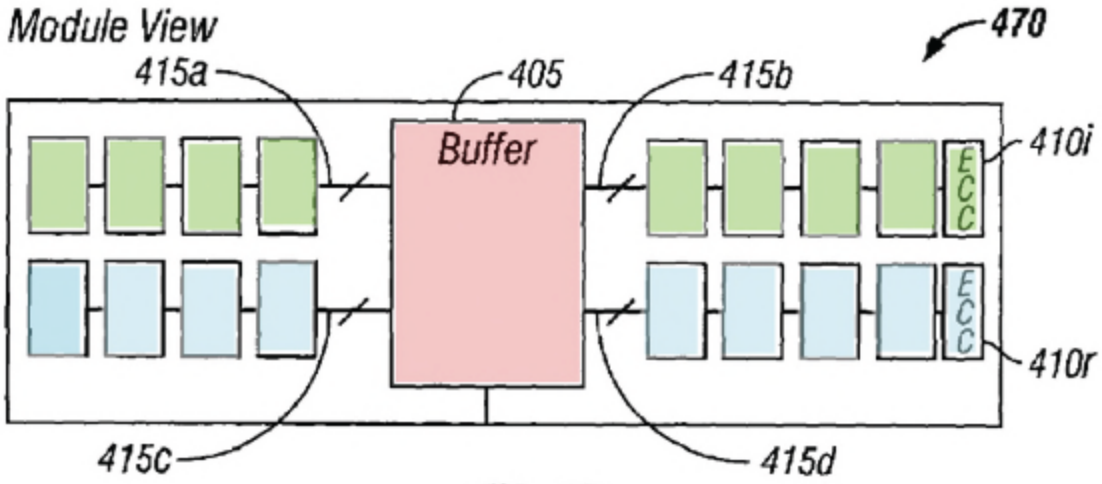



FIG. 4C

It also would have been obvious to a POSITA in light of JESD79-2 and knowledge of the JEDEC standards that the memory controller would provide multiple chip-select signals to the memory module (e.g., "S0-S3" below), corresponding to multiple "*ranks*" of memory devices (called "physical banks" below, *see* pp.26-28), where one of those chip-select signals is active to select the target rank of memory devices for the read or write operation, and the other chip-select signal(s) are inactive so that the other rank(s) of memory devices do not participate in the read or write operation. EX1003, ¶¶251-252; EX1064, p.6 ("CS provides for external Rank selection on systems with multiple Ranks."); EX1062, p.6 (below); EX1066, pp.6-7 (similar).

**Pin Description**

| Pin Name | Description | Pin Name | Description |
|---|---|---|---|
| A0 - A15 | SDRAM address bus | CK0 | SDRAM clock (positive line of differential pair) |
| BA0 - BA1 | SDRAM bank select | $\overline{CK0}$ | SDRAM clock (negative line of differential pair) |
| DQ0 - DQ63 | DIMM memory data bus | SCL | IIC serial bus clock for EEPROM |
| CB0 - CB7 | DIMM ECC check bits | SDA | IIC serial bus data line for EEPROM |
| $\overline{RAS}$ | SDRAM row address strobe | SA0 - SA2 | IIC slave address select for EEPROM |
| $\overline{CAS}$ | SDRAM column address strobe | $V_{DD}$ | SDRAM positive power supply |
| $\overline{WE}$ | SDRAM write strobe | $V_{DDQ}$ | SDRAM I/O Driver positive power supply |
| $\overline{S0}$ - $\overline{S3}$ | SDRAM chip select lines (Physical. banks 0, 1, 2, and 3) | $V_{REF}$ | SDRAM I/O reference supply |
| CKE0 - CKE1 | SDRAM clock enable lines | $V_{SS}$ | Power supply return (ground) |
| DQS0 - DQS8 | SDRAM low data strobes | $V_{DDSPD}$ | Serial EEPROM positive power supply (Supports both 2.5 Volt and 3.3 Volt operation) |
| DM(0-8)/DQS(9-17) | SDRAM low data masks/high data strobes (x4, x8-based x72 DIMMs) | NC | Spare Pins (no connect) |
| $V_{DDID}$ | $V_{DD}$ Identification Flag | $\overline{RESET}$ | Reset pin (forces register inputs low) |
| Test | Used by memory bus analysis tools (unused on memory DIMMs) | | |

### *(3) [1.c.3] Registered Address and Control Signals*

Ground 1 teaches "*the set of registered address and control signals* [from [1.c.1] (pp.43-51), e.g., output by the buffer devices on the horizontal RQ lines to the memory devices] *including a plurality of registered chip select signals* [e.g., "CS" signals as part of the read or write command to the memory devices, as required by JESD79-2, EX1064, pp.6, 24-33, 49] *corresponding to respective ones of the plurality of input chip select signals* [from the memory controller, *see* [1.c.2] (pp.51-58)] *and other registered address and control signals* [e.g., bank and row/column address signals (e.g., BA0-BA2, A0-A15), and RAS, CAS and WE control signals, as part of the read or write command to the memory devices, as

required by JESD79-2, EX1064, pp.6, 24-33, 49] *corresponding to respective ones of the other input address and control signals* [from the memory controller, see [1.c.2] (pp.51-58)], *the plurality of registered chip select signals including one registered chip select signal having an active signal value* [e.g., "L" or "Low," identifying the rank of memory devices being targeted by the buffer device for the read or write operation, *see* JESD79-2, EX1064, pp.6, 49] *and one or more other registered chip select signals each having a non-active signal value* [e.g., "H" or "High," so the other rank(s) of memory devices are "Deselected" and do not participate in the read or write operation, i.e., perform "No Operation" (or NOP), *see* JESD79-2, EX1064, pp.6, 48 ("Deselect command performs the same function as a No Operation [NOP] command."), 49]." EX1003, ¶¶255-263.

Consistent with JESD79-2's disclosure of chip-select signals to target one rank of memory devices for a read or write operation, discussed immediately above, Perego also teaches that only the targeted rank of memory devices would participate in the read or write operation, while the other memory devices would "remain in a ready or standby state until called upon to perform memory access operations." EX1071, 21:16-20; *see also id*. 15:40-45 ("By accessing a subset of secondary channel signal lines per transaction,…One of these benefits is reduced power consumption. Another benefit is higher performance by grouping memory

devices into multiple independent target subsets (i.e. more independent banks)."); EX1003, ¶¶257-260.

A POSITA also would have known that under the JEDEC standards it was standard for a memory module to use registered chip-select signals to target one rank of memory devices for a read or write operation. EX1064, p.6 ("CS provides for external Rank selection on systems with multiple Ranks."); EX1062, pp.12-13 (showing two-rank modules with a register outputting a registered chip-select signal RS0 to one rank of memory devices, and another registered chip-select signal RS1 to the other rank of memory devices); EX1066, pp.10, 12-13 (similar); EX1069, pp.2-3 ("[T]he chip-select bus[] is essential in a JEDEC-style memory system, as it enables the intended recipient of a memory request....Even though all DRAMs in the system are connected to the same address and control busses and could, in theory, all respond to the same request at the same time, the chip-select bus prevents this from happening."); EX1003, ¶259.

Finally, as discussed above for [1.c.1] (pp.50-51), Perego teaches that the "*logic*" in the buffer device can perform "rank multiplication" (discussed above, pp.10-12) so that, for example, if the "*input address and control signals*" from the memory controller includes two chip-select signals in the "*plurality of input chip select signals*" (corresponding to two ranks of higher-density memory devices), then the "logic" in Perego's buffer device may use those chip-select signals along

with the address information from the "*input address and control signals*" to produce four chip-select signals (corresponding to four ranks of lower-density memory devices actually on the module) that are included in the "*plurality of registered chip select signals*" sent to the memory devices on the module. EX1003, ¶¶241, 261.

#### *(4) [1.c.4] Output Data Buffer Control Signals*

Ground 1 teaches "*wherein the logic* [from [1.c.1] (pp.43-51), e.g., in the buffer device (red below), coupled to a data buffer which buffers and/or routes data signals through interfaces 520a, 520b, multiplexers 530a and 530b, and interface 510 and 590, EX1071, Figs. 5A-5B] *is further configurable to output data buffer control signals* [to the data buffer, to enable data communication through the data buffer and between (i) the rank of memory devices targeted to perform the read or write operation and (ii) the memory controller (310)] *in response to the read or write memory command* [from [1.c.1] (pp.43-51)]." EX1003, ¶¶264-273.

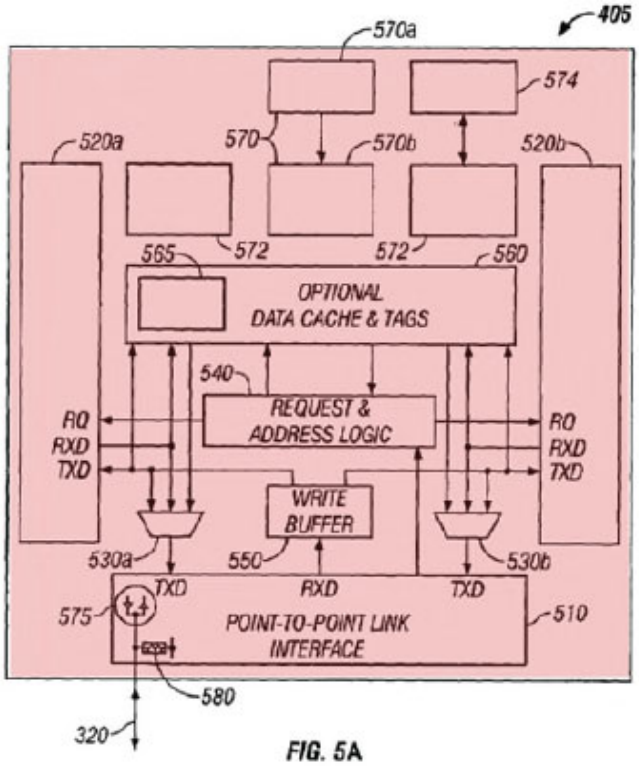

405
570a
574
520a
570
570b
520b
565
572
572
560
OPTIONAL
DATA CACHE & TAGS
540
REQUEST &
ADDRESS LOGIC
RQ
RXD
TXD
RQ
RXD
TXD
WRITE
BUFFER
530a
550
530b
TXD
RXD
TXD
575
POINT-TO-POINT LINK
INTERFACE
510
580
320

FIG. 5A

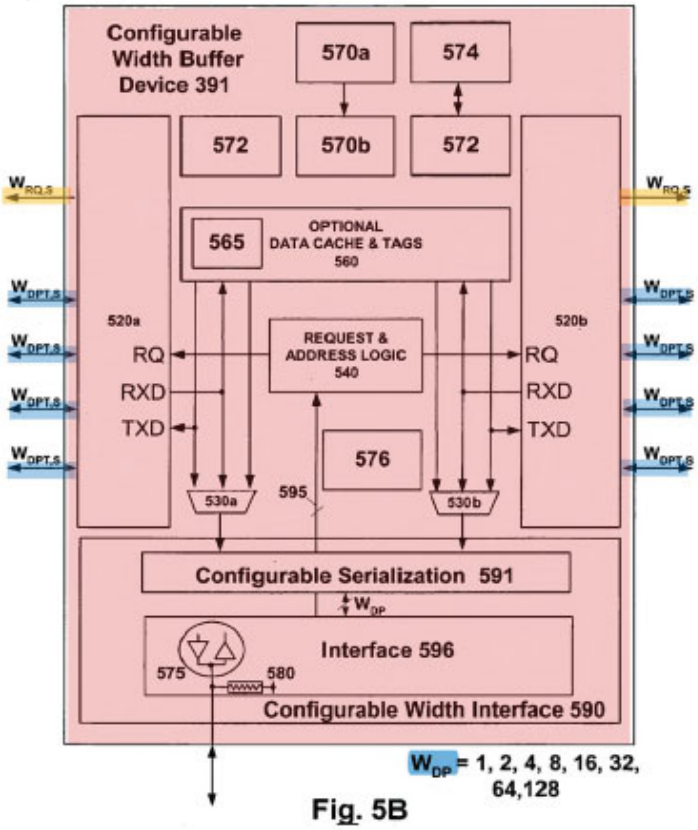

Configurable
Width Buffer
Device 391
570a
574
572
570b
572
565
OPTIONAL
DATA CACHE & TAGS
560
520a
520b
REQUEST &
ADDRESS LOGIC
540
RQ
RXD
TXD
RQ
RXD
TXD
576
530a
595
530b
Configurable Serialization 591
Interface 596
575
580
Configurable Width Interface 590
$W_{DP}$ = 1, 2, 4, 8, 16, 32,
64,128

Fig. 5B

A POSITA would have understood from Perego's descriptions of "control information and address information [being] decoded and separated from multiplexed data and provided on lines 595 to request & address logic 540 from interface 596," and from Perego's description of data signals being selectively routed to and from a subset of memory devices and the memory controller through the buffer device, that Perego's buffer device includes logic configured to output data buffer control signals to activate only the channel that transfers the data between the memory controller and the targeted rank, keeping the other channels in a "ready or standby state" thus providing "reduced power consumption." EX1071, 13:54-59, 12:9-12, 11:56-61, 6:15-25, 21:16-20, 15:40-45; EX1003, ¶¶267-269.

Furthermore, a POSITA would have understood that Perego's buffer device includes logic that outputs data buffer control signals to transceivers (e.g., 575, included in interface 520a, 520b, 510, and 590), multiplexing/demultiplexing circuits 597, and to input/output latches 597f-m, to selectively activate these circuit elements of the "buffer" according to the targeted rank and direction of the read and write operation. EX1071, 14:62-15:6, 15:34-37, 17:41-44, 17:61-62, Figs.5A-5B; EX1003, ¶¶270-271.

### *d) [1.d] Memory Devices*

#### *(1) [1.d.1] Ranks*

Ground 1 teaches "*memory devices* [e.g., 360, 410, below] *mounted on the printed circuit board* [from [1.b] (pp.42-43)] *and arranged in a plurality of N-bit wide* [e.g., 64-bit wide] *ranks* [e.g., green, blue]." EX1003, ¶¶274-296.

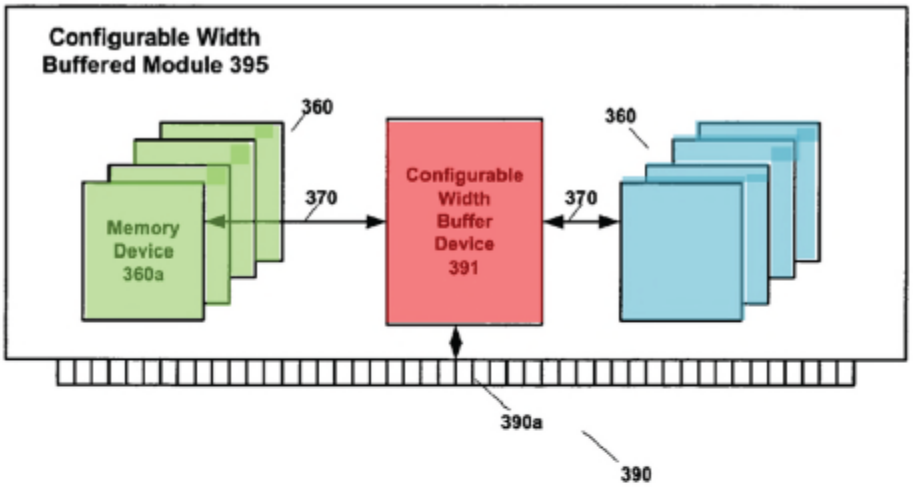



**Fig. 3C**

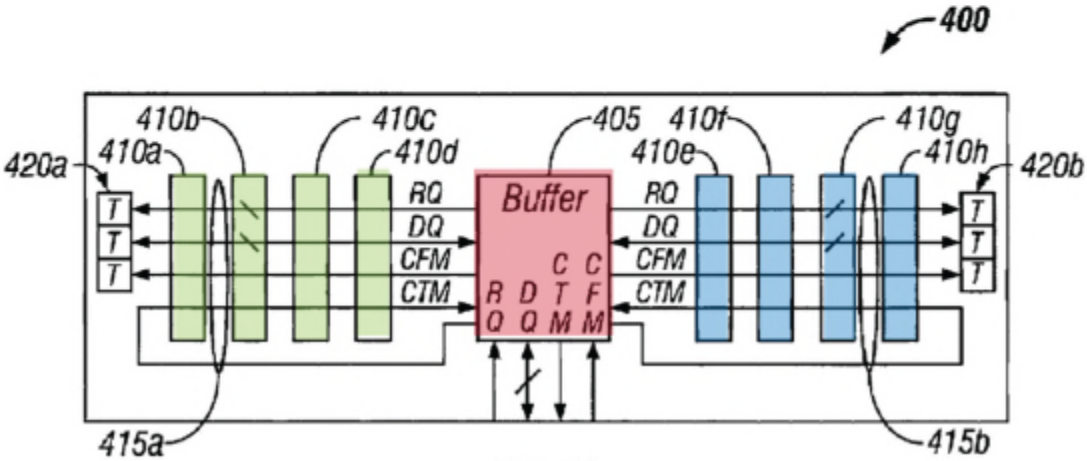



**FIG. 4A**

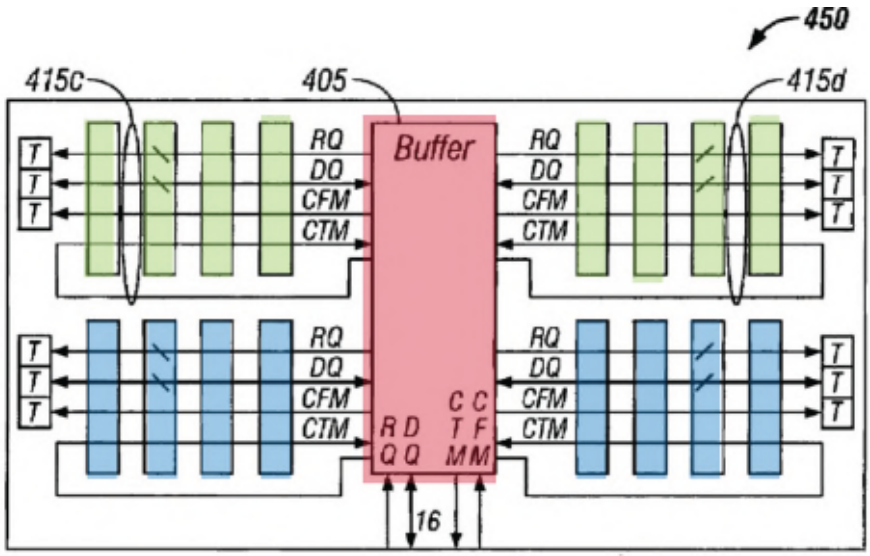



FIG. 4B

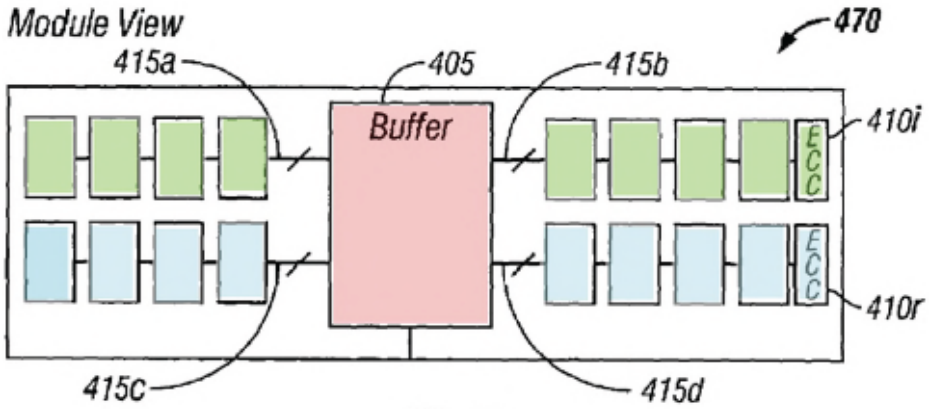



FIG. 4C

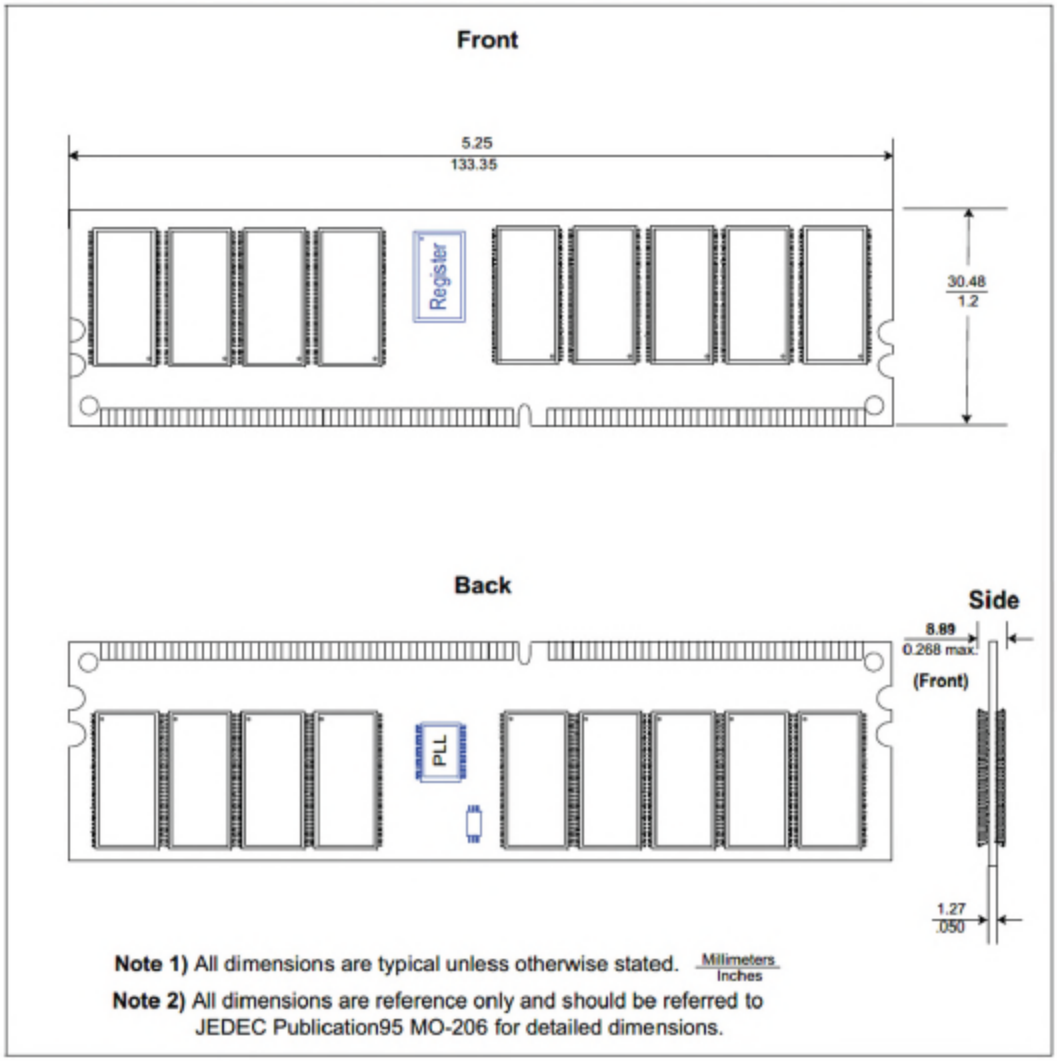
EX1071, Figs.3C, 4A-4C.

Perego's "*memory devices*" 360 and 410, which can include DDR or DDR2 SDRAM devices, are shown above. EX1071, 3:62-4:3, 8:1-4, 10:56-58; EX1003, ¶277.

As explained above for [1.b] (pp.42-43), Perego's "memory module" includes a "*printed circuit board*" (PCB), which Perego explains is a "a substrate

package housing or structure having a plurality of memory devices employed with a connector interface," EX1071, 4:19-22, consistent with the standard DIMM format (below) that includes "*memory devices mounted on the printed circuit board*," EX1062, pp.29, 35 (below, illustrating DDR SDRAM devices "surface mounted" on both sides of a PCB in a DIMM format); EX1071, 2:4-6 ("DIMM"). EX1003, ¶278.

**Example Raw Card Versions N (2 Physical Banks) Component Placement**



Perego discloses "grouping memory devices into multiple independent target subsets (i.e. more ***independent banks***)," EX1071, 15:37-45, which renders obvious the claim limitation "*ranks*" as properly construed (pp.26-28). EX1003, ¶276. Perego also teaches that the "*ranks*" are each "*N-bit wide*" (e.g., 64-bits wide): For example, Perego teaches that "interfaces 520a and 520b [below] may be programmed to connect to 16'x4' width memory devices, 8'x8' width memory devices or 4'x16' width memory devices," EX1071, 14:10-15, Figs.5A-5B, resulting in a "*rank*" with a bit-width of 64 bits, consistent with the standard DIMM layout shown above, *see, e.g.*, EX1062, p.13 (describing a "x64 DIMM, populated as two physical banks [i.e., "*ranks*," *see* pp.26-28] of [eight] x8 DDR SDRAMs [i.e., D0-D7, and D8-D15]"). The terms 'x4', 'x8' and 'x16'—pronounced "by four," "by eight," and "by sixteen"—refer to the data width of a single memory device, EX1069, p.1, so eight 'x8' memory devices results in a total bit-width of 64 bits. EX1003, ¶¶279-280.

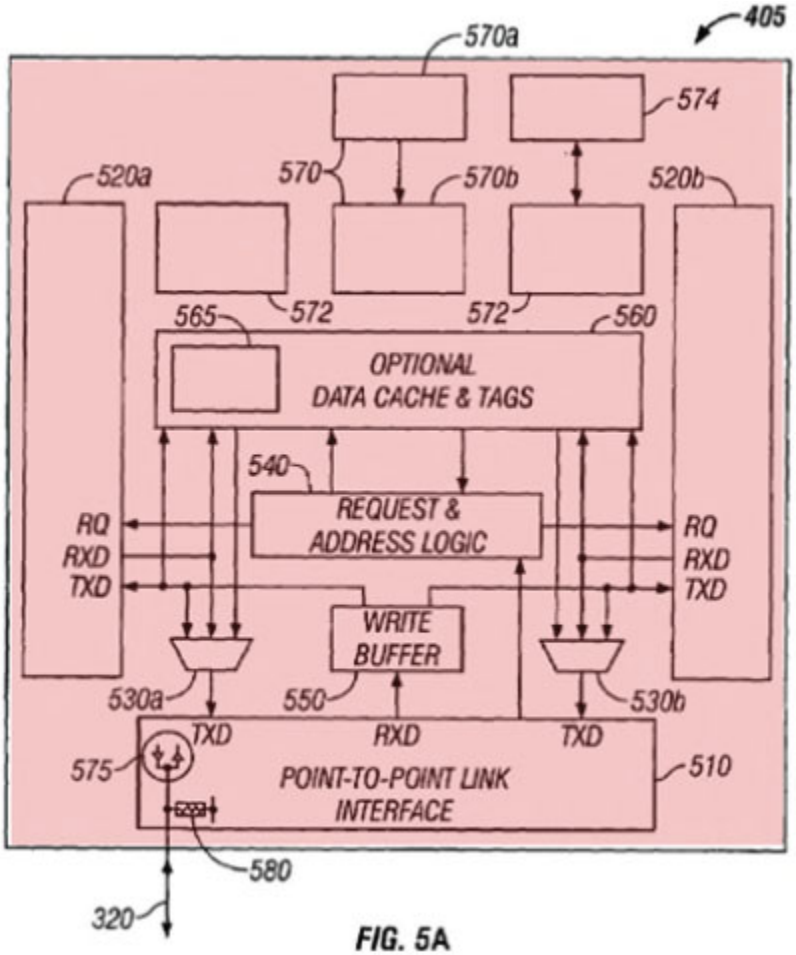

405
570a
574
520a
570
570b
520b
565
572
572
560
OPTIONAL
DATA CACHE & TAGS
540
REQUEST &
ADDRESS LOGIC
RQ
RXD
TXD
RQ
RXD
TXD
WRITE
BUFFER
530a
550
530b
TXD
RXD
TXD
575
POINT-TO-POINT LINK
INTERFACE
510
580
320

FIG. 5A

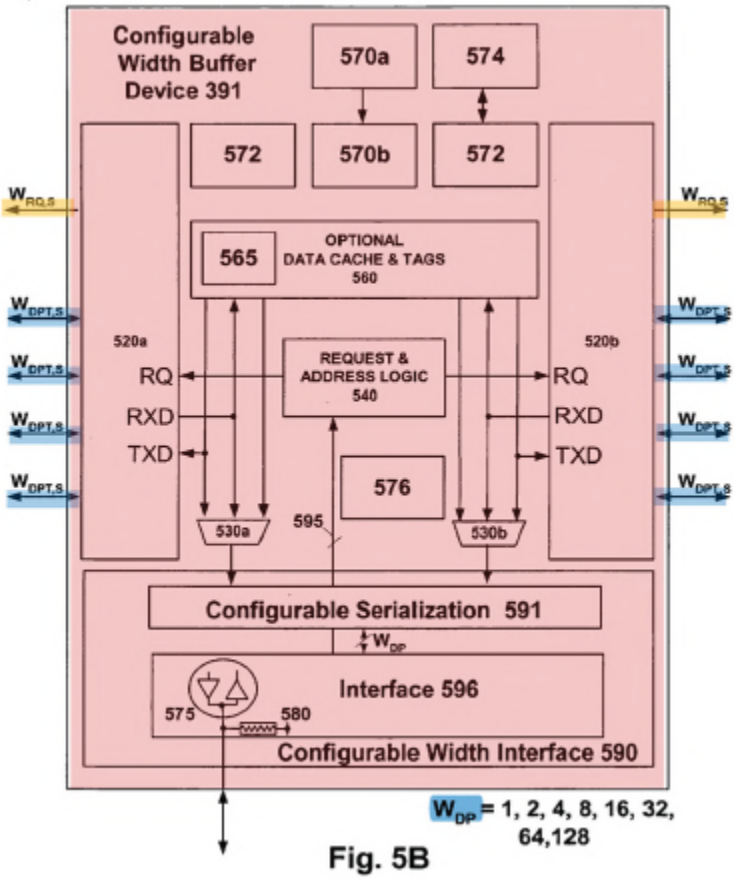



Fig. 5B

Perego teaches that the data width accessed in a memory transaction ($W_A$), and the data width of the buffer interfacing with the memory controller ($W_{DP}$), can both be the same (e.g., both 64 bits), such that the ratio $W_A/W_{DP}$=1:1. EX1071, 14:16-40, 17:22-28 ("1:1"), Fig.5C; EX1003, ¶281. A POSITA would understand that $W_A$ refers to the bit-width of each "*rank*" of memory devices (e.g., 64 bits can be read or written at a time) when only "***one***" of the "one or more channels 370" (shown below) is used for a read or write operation. EX1071, 6:12-24, 14:23-27, Fig.3C; EX1003, ¶¶282-283. Accordingly, when Perego's buffer device has two

channels, and each channel is connected to one rank, Perego's module includes two ranks of memory devices (green and blue below). EX1003, ¶283.

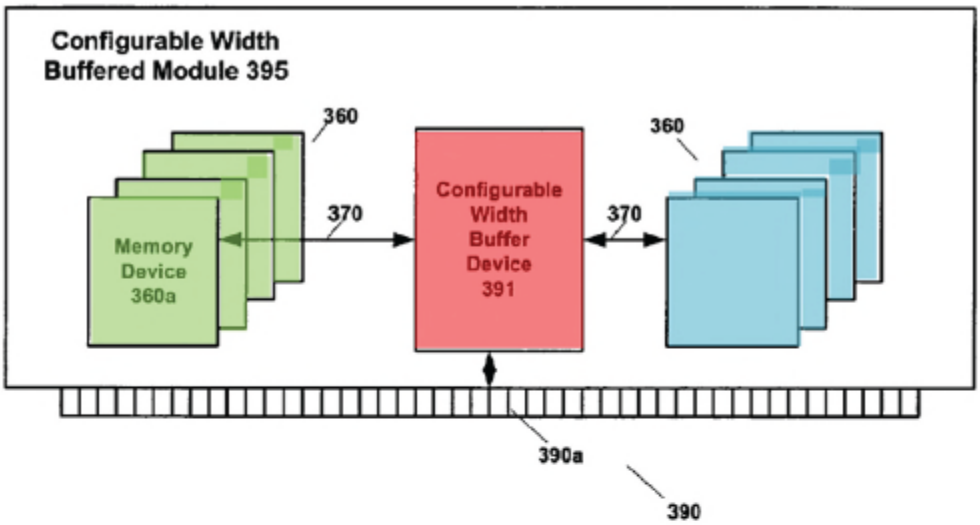



Fig. 3C

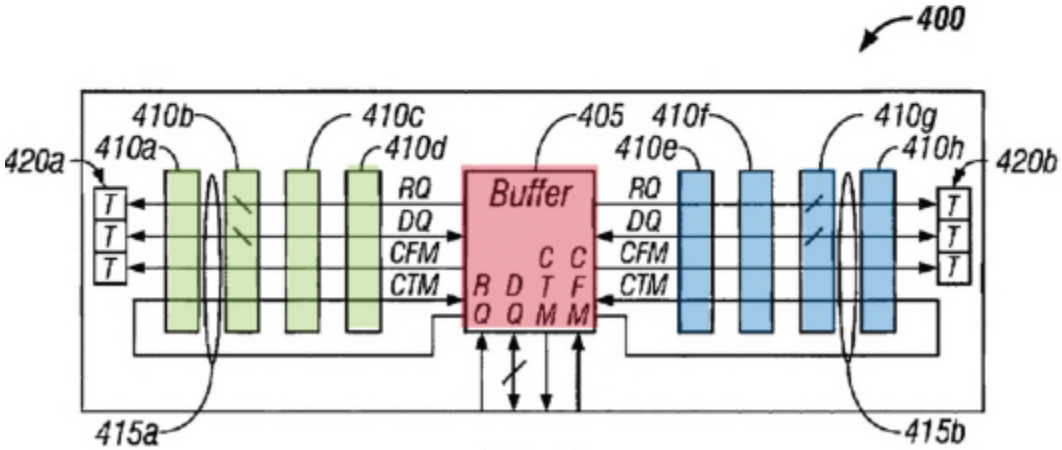



FIG. 4A

EX1071, Figs.3C, 4A.

Furthermore, Perego discloses that "[a]ny number of channels 415a-415d, for example[] two channels 415c and 415d may transfer information

simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations." *Id*., 21:16-20. In such an implementation, shown below, a POSITA would understand that the memory devices coupled to channels 415c/d form one "*rank[]*" (green), and the memory devices coupled to channels 415a/b form another "*rank[]*" (blue). EX1003, ¶284; EX1071, Fig.4B (below); *see also id*. Fig.4C (further below, using different channel numbering, with 415a/b referring to the top channels and 415c/d referring to the bottom channels). Indeed, Netlist has previously conceded that Perego discloses two such "*ranks*" (e.g., 415a/b and 415c/d, shown below). EX1019, p.43; EX1020, ¶¶93-94; EX1003, ¶285.

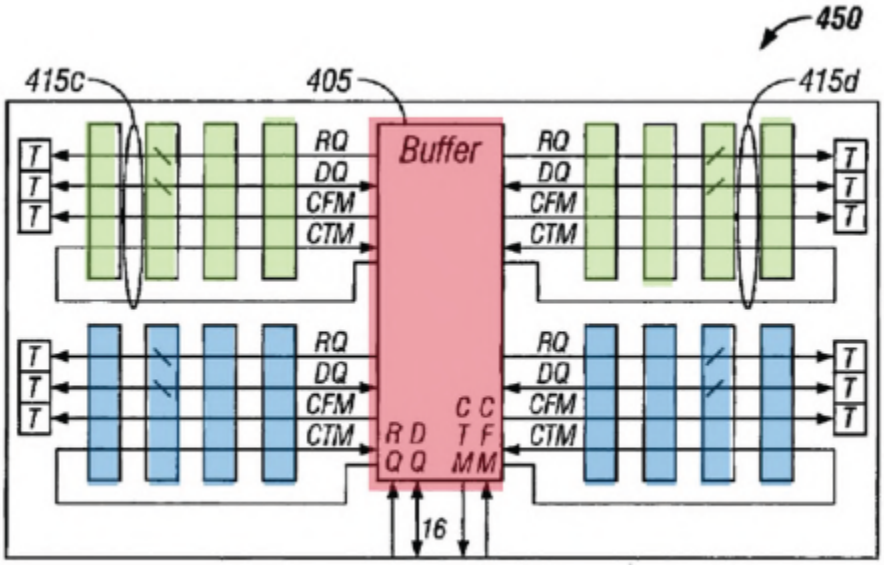



FIG. 4B

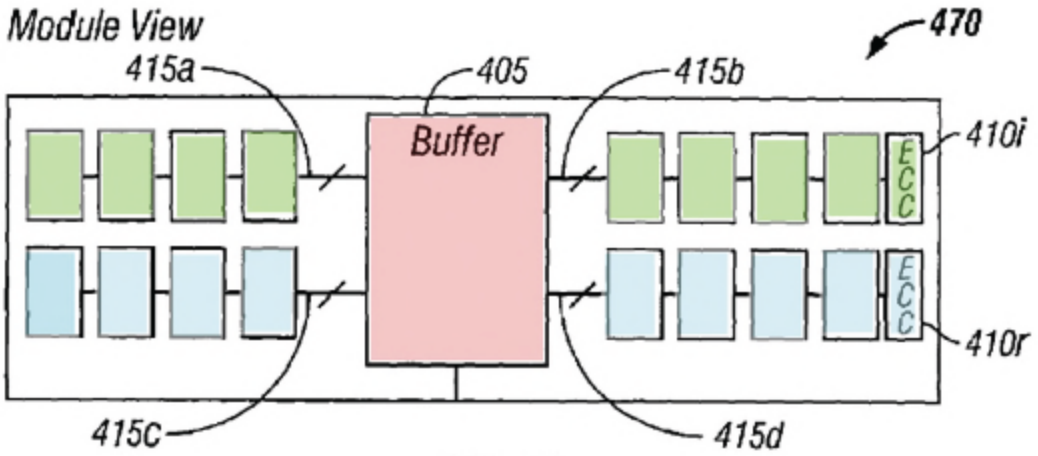



FIG. 4C

EX1071, Figs.4B-4C.

As shown above, Perego discloses multiple "*memory devices*" on the "*printed circuit board*," including at least one memory device for each "*rank*." EX1071, 15:37-45, Figs.3B (memory devices 360), 4A-4C (memory devices 410); EX1003, ¶286.

Finally, it would have been obvious to a POSITA to arrange Perego's DDR memory devices into "*ranks*," and a POSITA would have been motivated to do so, in light of the JEDEC standards. EX1003, ¶¶287-289; EX1064, p.6 ("Chip Select...provides for external ***Rank*** selection on systems with multiple ***Ranks***"); EX1062, p.13 (showing "x64 DIMM" with two "*ranks*," referred to as "physical banks," *see* pp.26-28, each with eight x8 memory devices, and each with its own chip-select signal, RS0 and RS1). Implementing such ranks in Perego's module would have been well within the level of ordinary skill. EX1003, ¶288 (citing, e.g.,

EX1072, Fig.1 (Matsui1, below, showing details of wiring DDR SDRAMs to a central buffer in DIMM format)).

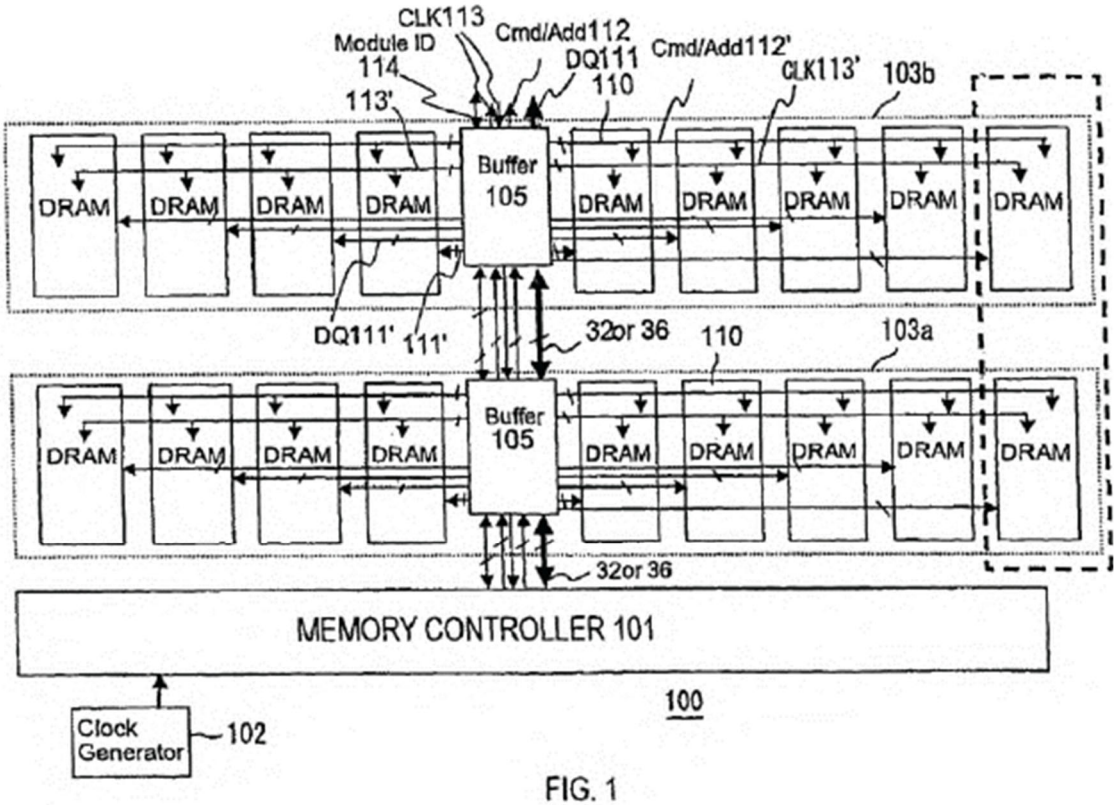



FIG. 1

### *(2) [1.d.2] Registered Chip Select Signals*

Ground 1 teaches "*wherein the plurality of N-bit wide ranks* [from [1.d.1] (pp.64-73)] *correspond to respective ones of the plurality of registered chip select signals* [from [1.c.3] (pp.58-61)] *such that each of the plurality of registered chip*

*select signals is received by memory devices [in]*[3] *one respective N-bit wide rank of the plurality of N-bit-wide ranks*," consistent with the JEDEC standards as discussed for [1.c.2]-[1.c.3] (pp.51-61). *See, e.g.*, EX1064, p.6 ("CS provides for external Rank selection on systems with multiple Ranks."); EX1069, pp.2-3 ("chip-select bus contains a separate wire for every rank of DRAM in the system."), 9. EX1003, ¶¶297-301.

***(3) [1.d.3] One N-bit Wide Rank***

Ground 1 teaches "*wherein one* [e.g., green, below] *of the plurality of N-bit wide ranks* [from [1.d.1] (pp.64-73)] *including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals* [from [1.c.3] (pp.58-61), e.g., in response to a read or write command from the buffer device targeting that rank] *is configured to receive* [for a write command] *or output* [for a read command] *a burst of N-bit wide data signals* [e.g., according to the JESD79-2 standard, EX1064, pp.25-32 ("Burst" read

[3] The claim language as written (without "*[in]*") is, at a minimum, grammatically incorrect. The prosecution history indicates that "*[in]*" was intended to be included. EX1002, p.299; EX1003, ¶298.

and write operations)] *in response to the*[4] *read or write command* [from [1.c.1] (pp.43-51)]." EX1003, ¶¶302-323.

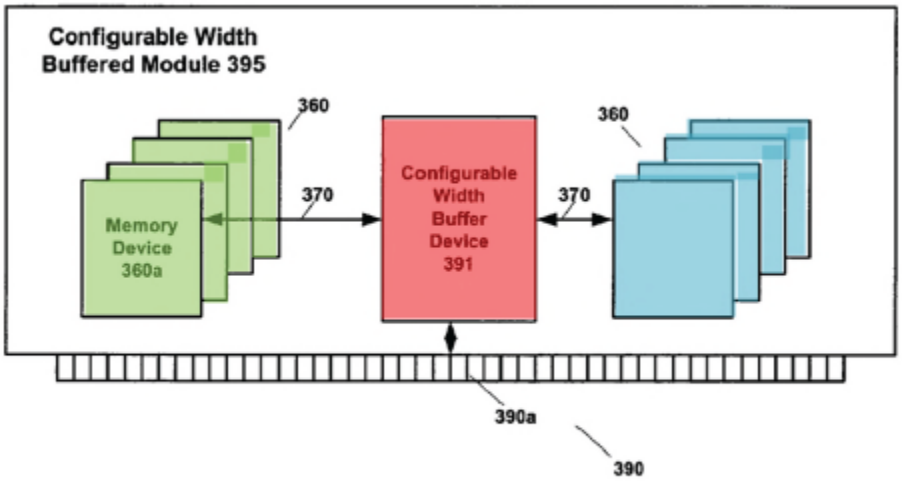



**Fig. 3C**

[4] There is no antecedent basis for "*read or write command*," but [1.c.1] provides antecedent basis for "*read or write memory command*." EX1003, ¶303.

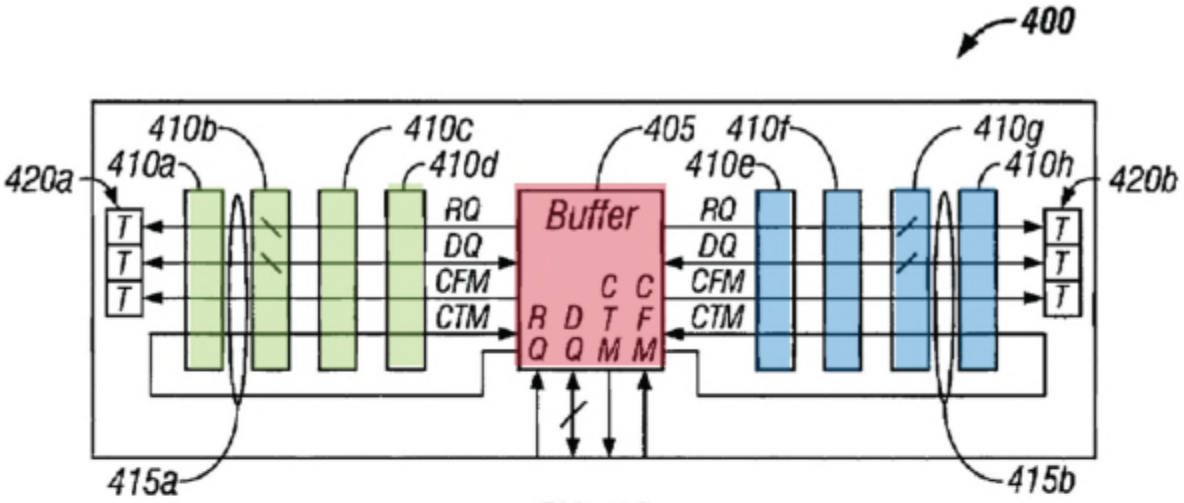

400
410b
410c
405
410f
410g
420a
410a
410d
410e
410h
420b
Buffer
RQ
DQ
CFM
CTM
RQ
DQ
CFM
CTM
T
T
T
T
T
T
415a
415b

FIG. 4A

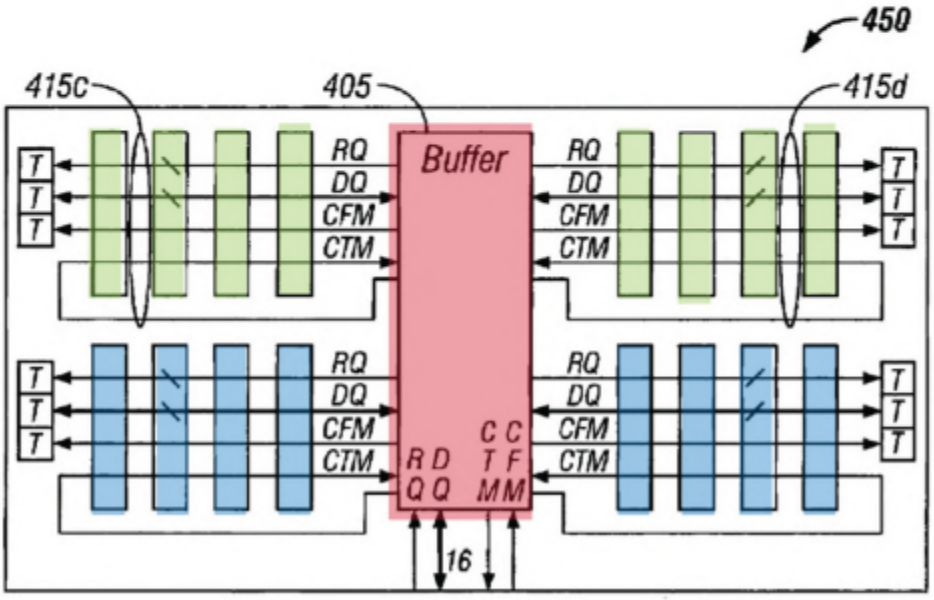

450
415c
405
415d
Buffer
RQ
DQ
CFM
CTM
RQ
DQ
CFM
CTM
T
T
T
16

FIG. 4B

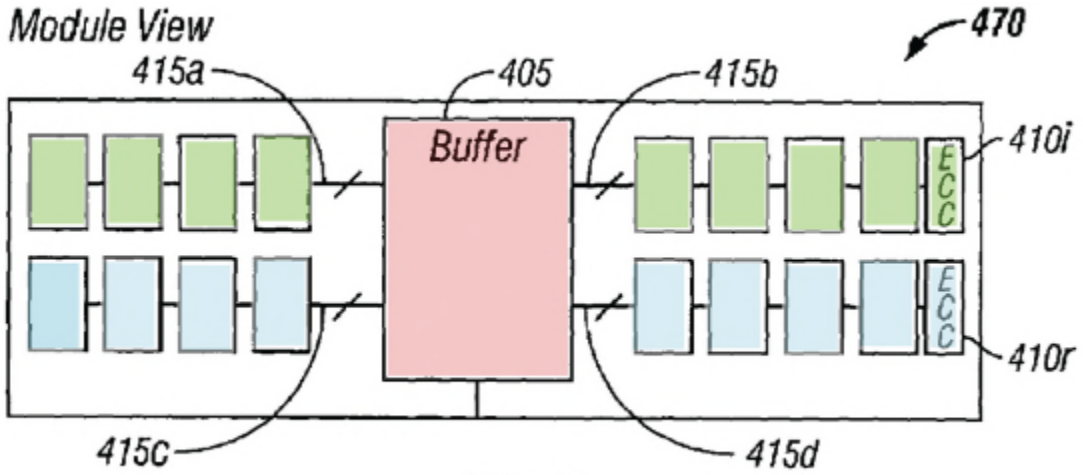



FIG. 4C

EX1071, Figs.3C, 4A-4C.

Perego's buffer device (red, above and below) responds to a read or write command by selecting a target subset of memory devices, e.g., a "*rank*," and routes the data through a corresponding "datapath" to that rank of memory devices (e.g., green above) and not the other rank(s) of memory devices. EX1003, ¶¶306-307, 319-321; EX1071, 6:21-22 ("Buffer device 350...receives the data via ***one***...of channels 370."), 11:56-61 ("route data"), 15:31-45 ("datapath" to "target subset" of memory devices), 21:16-20 (other memory devices "remain in a ready or standby state until called upon to perform memory access operations"), Figs.5A-5B.

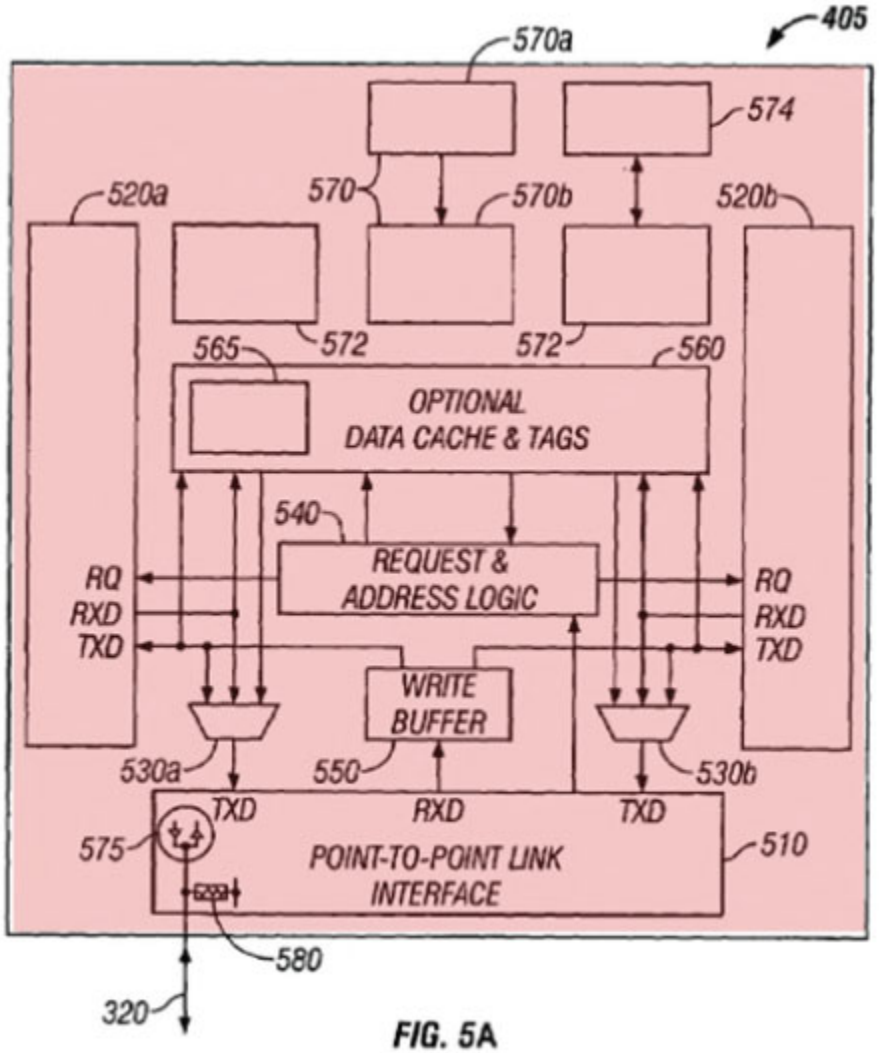

405
570a
574
520a
570
570b
520b
565
572
572
560
OPTIONAL
DATA CACHE & TAGS
540
REQUEST &
ADDRESS LOGIC
RQ
RXD
TXD
RQ
RXD
TXD
WRITE
BUFFER
530a
550
530b
TXD
RXD
TXD
575
POINT-TO-POINT LINK
INTERFACE
510
580
320

FIG. 5A

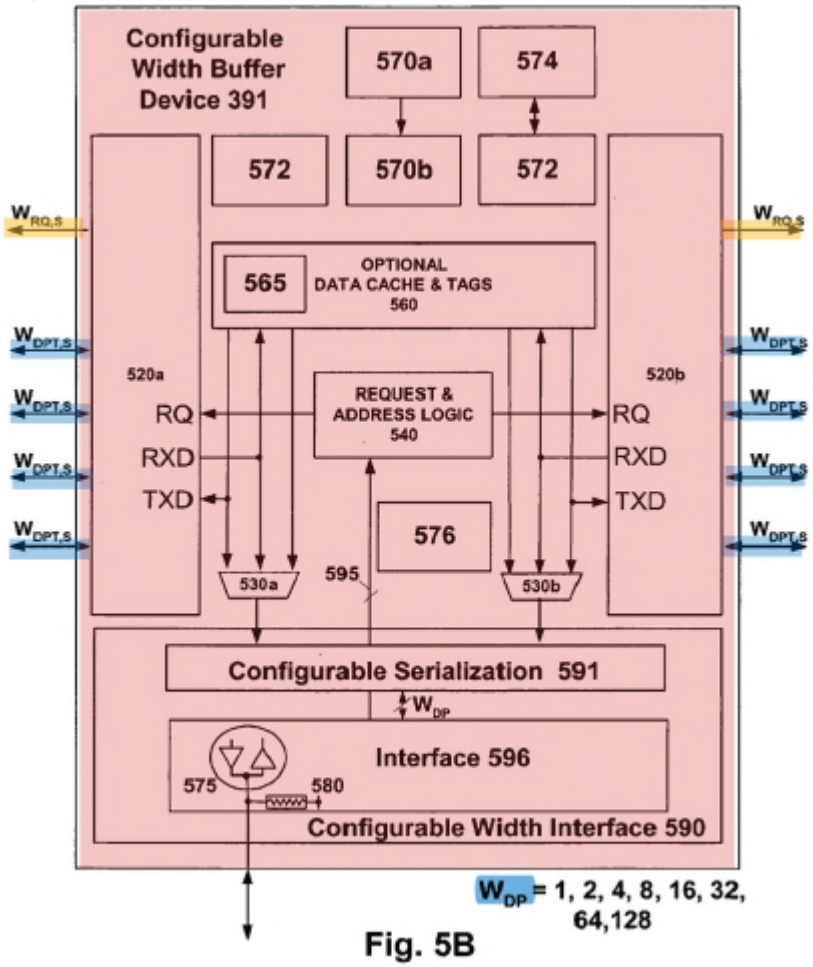
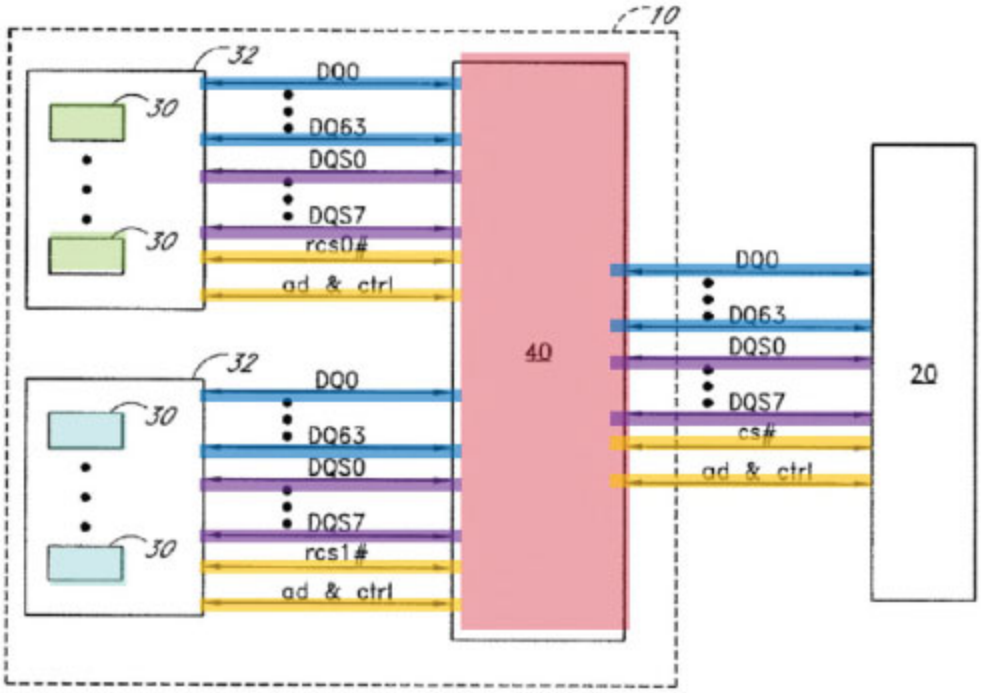



Fig. 5B

EX1071, Figs.5A-5B.

Perego's disclosure above is consistent with the claim language and the 417 Patent's disclosure that different ranks (green and blue, below) are on different "forks" of the data path (blue DQ data lines, and purple DQS strobe lines, below, from buffer 40, red), *see* EX1003, ¶¶316-317.




EX1001, Fig.1. As shown above and below, the 417 Patent discloses that data and strobe signals output or received by one rank are ***not*** received or output by the other rank because they are on separate data paths, thus avoiding collisions. EX1003, ¶318; EX1001, 15:48-61; *see also id*. Fig.8C (below).

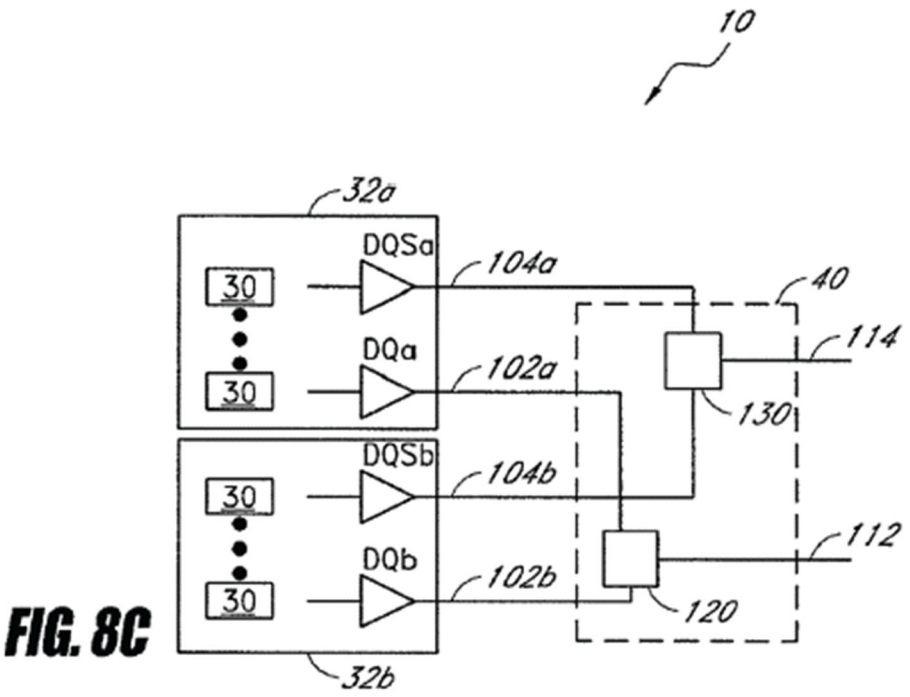
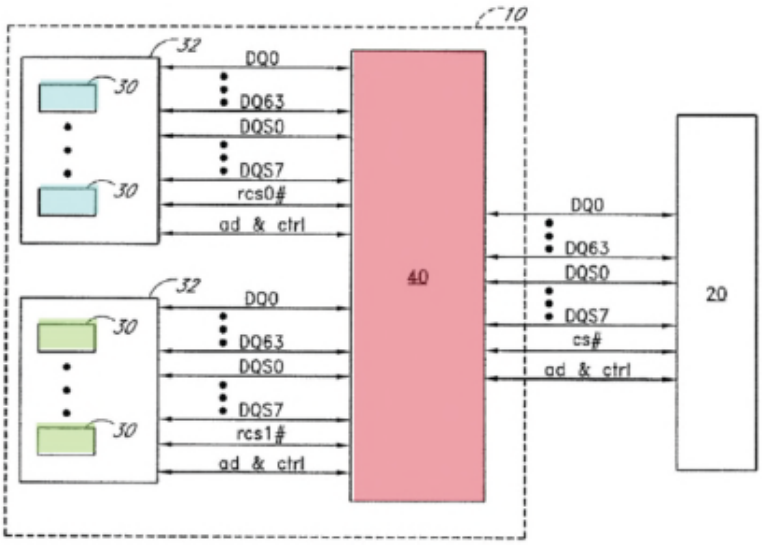


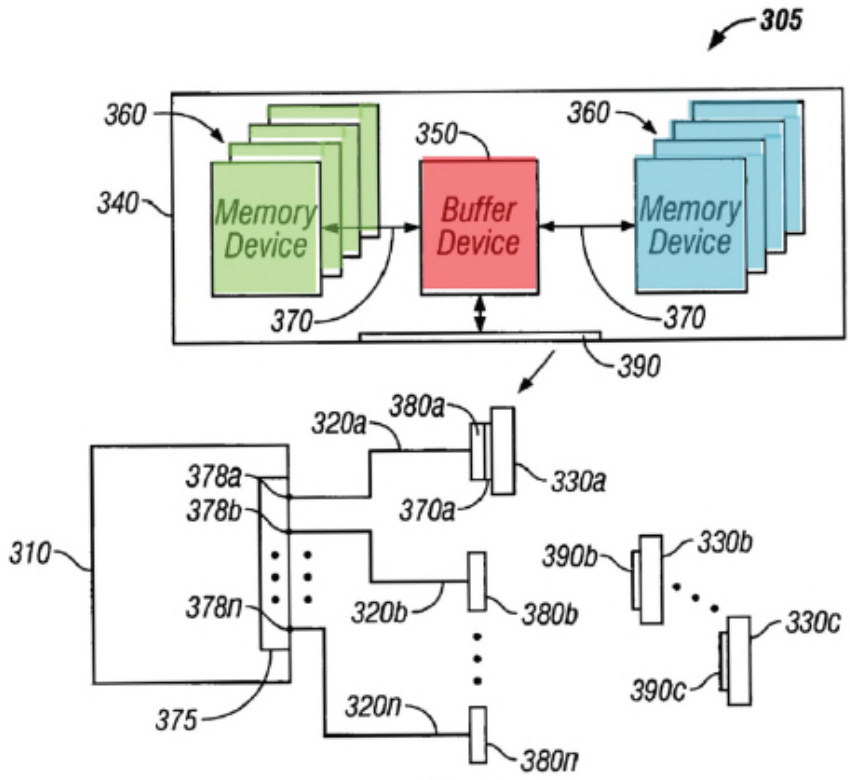
FIG. 8C

Like the 417 Patent, Perego teaches a separate data path for each rank (e.g., green, blue) as discussed above (pp.75-79).

In district court, Netlist appears to advance an unduly broad construction permitting the two ranks to ***share*** the same data lines on the module (rather than being on separate "forks"). *See* EX1085, pp.22-25; EX1003, ¶310. This arrangement was also well known and is similar to the arrangement disclosed in the prior-art JEDEC standards. *See, e.g.*, EX1062, p.16 (showing two ranks connected to chip-select signals RS0 and RS1, respectively, where the memory devices in the two ranks, e.g., D0 and D18, are connected to the same DQS data strobes and the same DQ data signals); EX1064, pp.4-5 (similar, for stacked memory device, with chip-select signals CS0 and CS1); EX1003, ¶311. A POSITA

would have recognized that Perego also renders obvious this limitation under Netlist's broader construction. EX1003, ¶312. Indeed, Perego discloses the same memory module structure as the 417 Patent:

| | |
|---|---|
| 417 Patent (EX1001, Fig.1) |  <br>FIG. 1 |

| | |
|---|---|
| Perego (EX1071, Fig.3B) |  <br>FIG. 3B |

Thus, if the primary embodiment shown in Figure 1 of the 417 Patent (above) is not excluded from the scope of the claim, Perego satisfies the claim because Perego similarly discloses a separate data channel to each rank (e.g., 370 above) and that one rank is selected to communicate data while the other rank(s) are not, as discussed above (pp.75-79). EX1003, ¶¶312-313.

If Netlist argues that the claim requires a single data channel to both ranks (as in the prior-art JESD21-C standard, *see, e.g.*, EX1062, p.16), Perego discloses that implementation as well, where a single channel is used to access two memory devices (e.g., 652 and 653, below) in two different ranks (green and blue, below)

coupled to the same data lines (e.g., DQ3 and DQ4). EX1003, ¶¶314-315; EX1071, 10:14-15, Fig.5E.

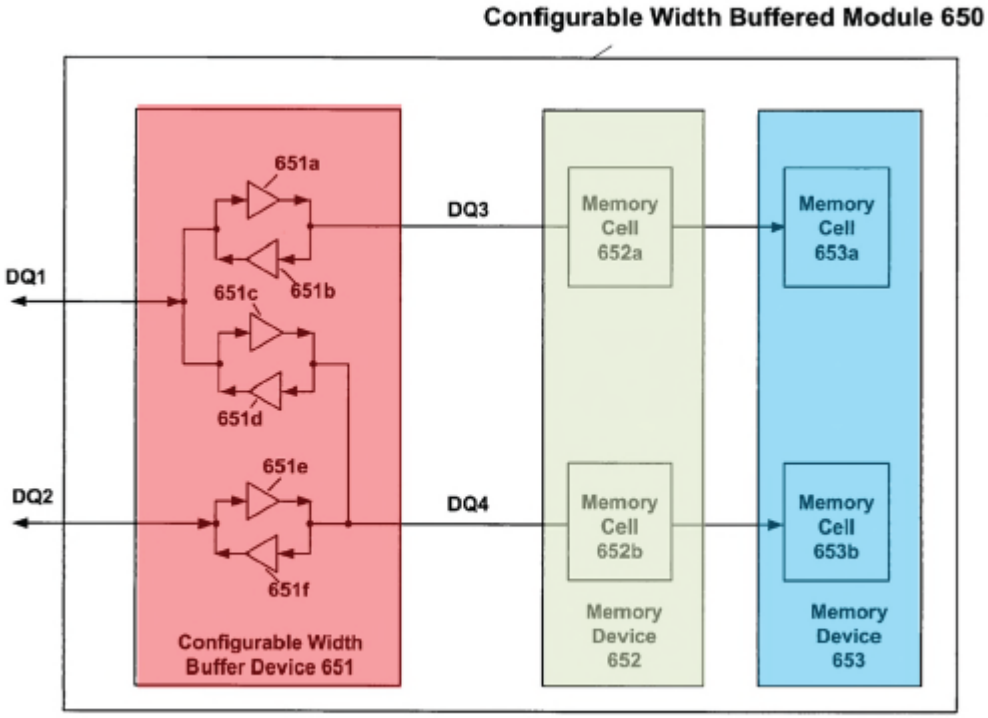



Fig. 5E

EX1071, Fig.5E. In this arrangement, a POSITA would have understood that, because the data lines are shared by multiple SDRAM memory devices, each rank of memory devices would receive a separate chip-select signal that selects the memory devices in that rank, similar to the prior-art JEDEC standard. EX1062, p.16 (showing a two-rank module having two chip-select signals, RS0 and RS1, each coupled to a respective rank of memory devices); EX1069, pp.2-3 (similar); EX1003, ¶315.

### *e) [1.e] Circuitry*

#### *(1) [1.e.1] Coupled between Data Signal Lines and Corresponding Data Pins*

Ground 1 teaches "*circuitry*[5] [red, below, including circuitry in Perego's buffer device (e.g., buffer device 391 in Figures 3C/5B, and buffer device 405 in Figures 4A-4B, 5A) for buffering and/or routing data signals in interfaces 520a and 520b, multiplexers 530a and 530b, and interfaces 510 or 590] *coupled between the data signal lines in the N-bit wide memory bus* [from [1.a.2]-[1.a.3] (pp.36-41), e.g., coupled to interface 510 or 590] *and corresponding data pins of memory*

---

[5] The intrinsic evidence shows that the "*circuitry*" (which as explained above can buffer data signals) does not need to be a physically separate component from the "*logic*" in [1.c.1] (pp.43-51) that registers address and control signals. EX1003, ¶328; EX1001, Fig.1 (showing circuit 40 in memory module 10 buffers both address/control ("ad & ctrl") and data (DQ0-DQ63)), 16:58-63 ("register 230 receives and buffers...command signals and address signals"), 18:26-29 (similar), 16:64-17:2 (register 230 for address and control signals, and circuit 40, can be "portions of a single component"); *see also id*. 6:18-23 ("'circuit'" is a broad term"), 7:28-31 ("…the logic element comprises various discrete electrical elements,…the logic element comprises one or more integrated circuits.").

*devices in each of the plurality of N-bit wide ranks* [from [1.d.1] (pp.64-73), e.g., coupled to interfaces 520a and 520b]." EX1003, ¶¶324-333.

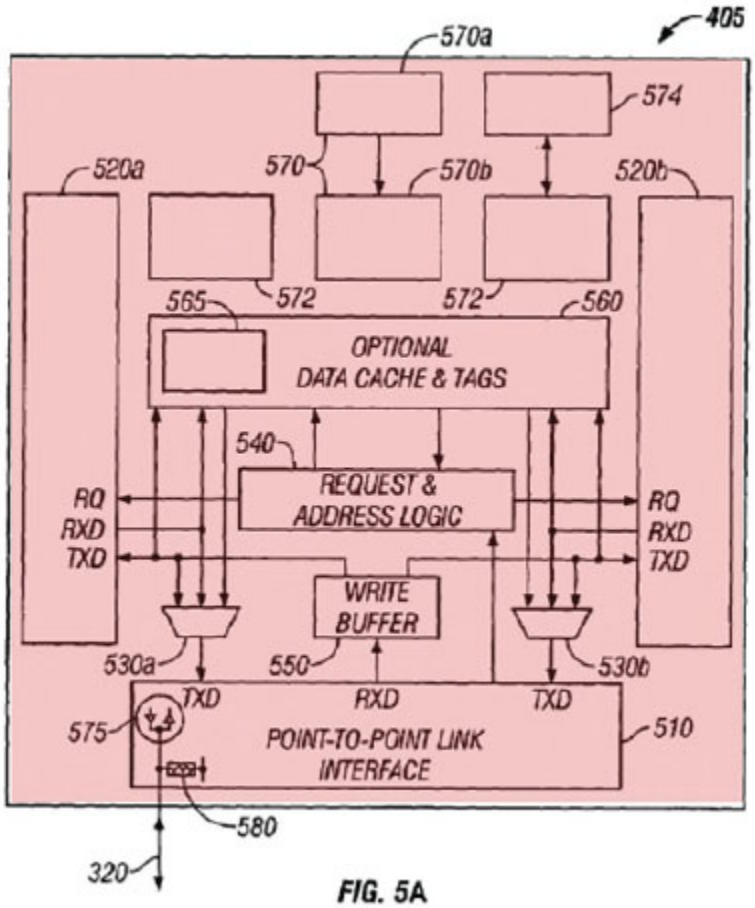



FIG. 5A

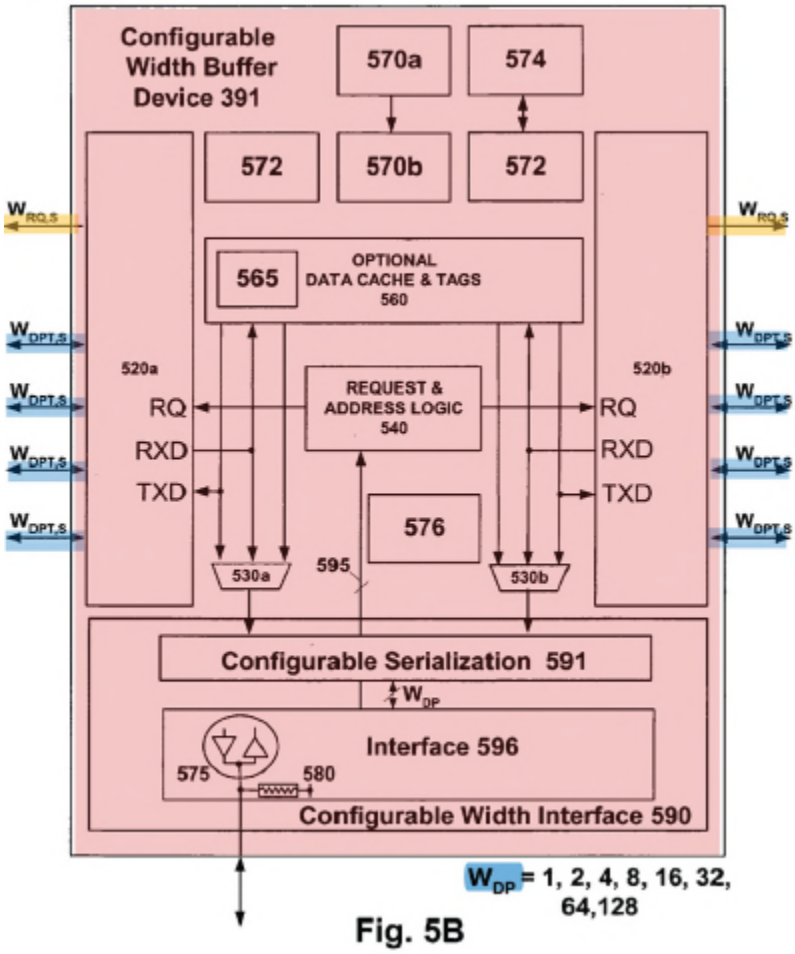



Fig. 5B

A POSITA would have understood that DDR "*memory devices*" have DQ "*data pins*" to output or receive data signals. EX1064, pp.1-6; EX1003, ¶327. Furthermore, Perego's "*circuitry*" (red, above) "isolate[es]" signals, including data signals, thus isolating the memory controller from signals interfacing with the "*data pins of memory devices*." *See, e.g.*, EX1071, Figs. 5A-5B (above), 4:38-42 ("buffer device...isolating data...signals"), 6:12-15 (buffer device 350 in Figs.3A-3B), 11:1-7 (buffer device 405 in Fig.5A), 13:6-10 (buffer device 391 in Fig.5B);

*see also id*., 7:30-34, 10:59-67 (buffer device 391/405 from Figs.5A-5B can be the buffer device in memory systems 300/305 in Figs.3A-3B); EX1003, ¶¶330-331.

Furthermore, a POSITA would have understood that the circuitry for handling data signals in interfaces 520a/b, multiplexers 530a/b, and interface 510 or 590 include data buffers, e.g., transceivers 575 in interface 510 or 590, and transceivers in interfaces 520a/b, which can include latches (e.g., blue, below) that buffer the data signals. EX1071, 13:18-24, 14:65-15:2, Fig.5C (below, showing input/output latches 597f-m for data signals), 17:61-63, 18:65-19:3; EX1003, ¶332.

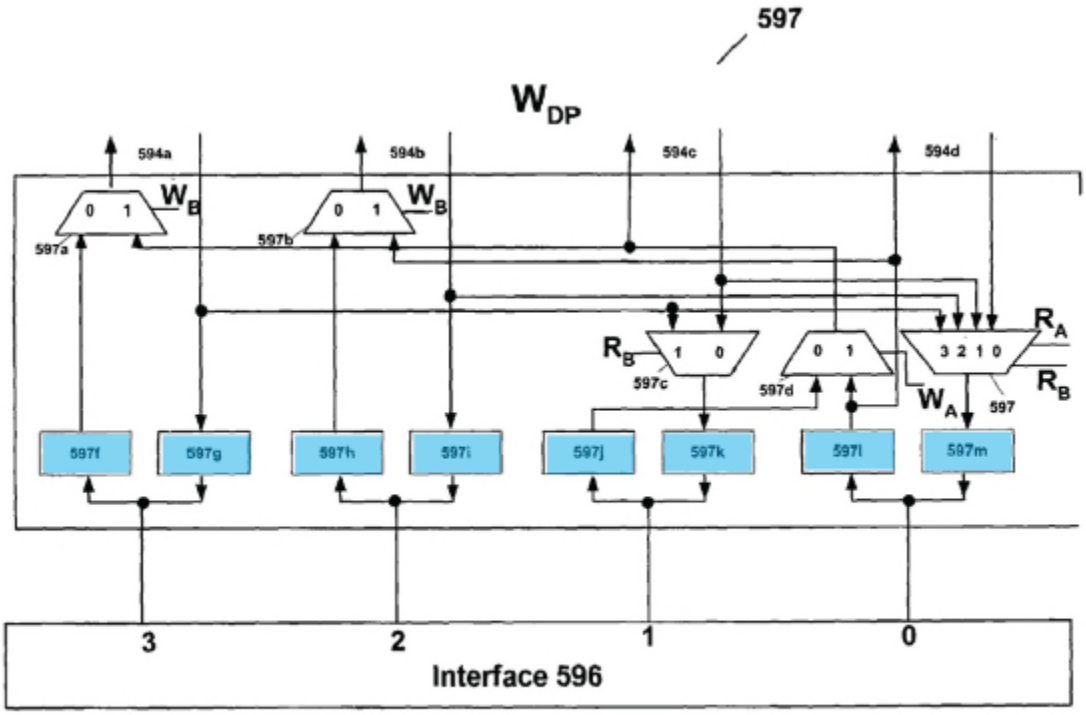



Fig. 5C

#### *(2) [1.e.2] Configurable to Transfer Bursts of Data Signals Between Memory Bus and Memory Devices*

Ground 1 teaches "*the circuitry* [from [1.e.1] (pp.85-88), red below, e.g., for buffering and/or routing data signals] *being configurable to transfer the burst of N-bit wide data signals* [from [1.d.3] (pp.74-84)] *between the N-bit wide memory bus* [from [1.a.2] (pp.36-40)] *and the memory devices in the one of the plurality of N-bit wide ranks* [from [1.d.3] (pp.74-84), e.g., the target rank of the read or write command from the buffer device] *in response to the data buffer control signals* [from [1.c.4] (pp.61-63)]." EX1003, ¶¶334-343.

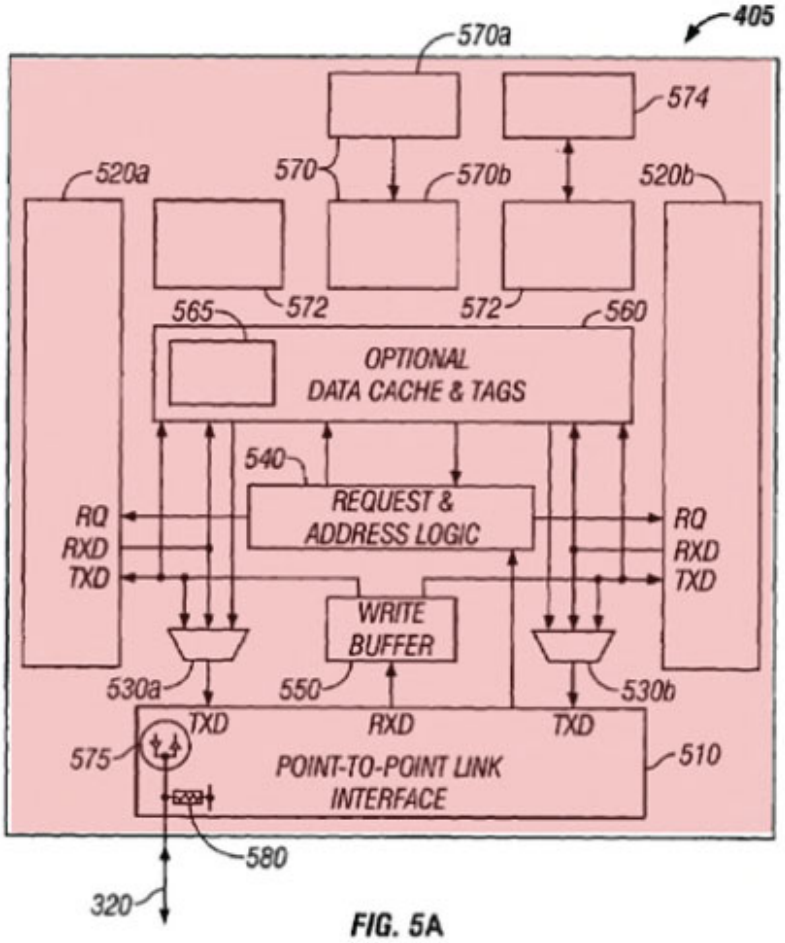



FIG. 5A

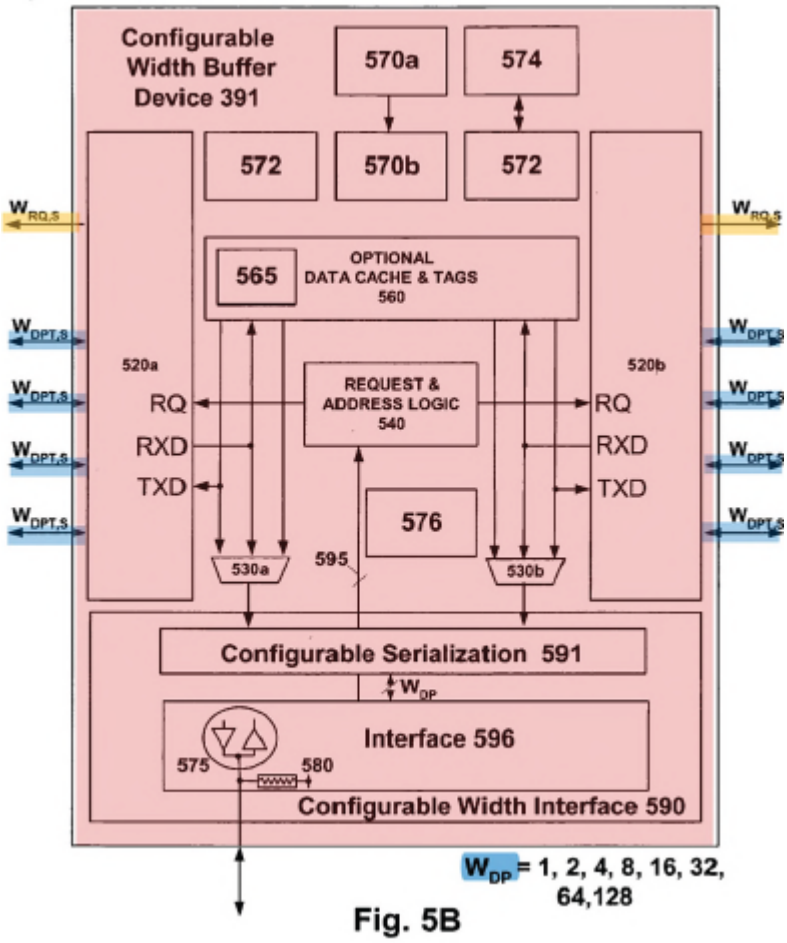



Fig. 5B

As explained for [1.a.2]-[1.a.3] (pp.36-41), [1.c.4] (pp.61-63), and [1.d.3] (pp.74-84), Perego's data bursts are selectively routed through the buffer device to/from the targeted "*rank*" of memory devices and to/from the memory controller, and a POSITA would have understood that the buffer device's logic sends "*data buffer control signals*" to interfaces 520a/b to activate only the channel transferring the data burst between the memory controller and the targeted rank. EX1003, ¶¶338-340; EX1071, 11:56-61 ("route data"), 6:15-25 ("data via one or more of channels 370"), 12:9-12 (computation block 565), 13:54-59 (request & address

logic 540), 21:16-20 (other channels "remain in a ready or standby state"), 15:40-45 (not using all channels "reduce[s] power consumption").

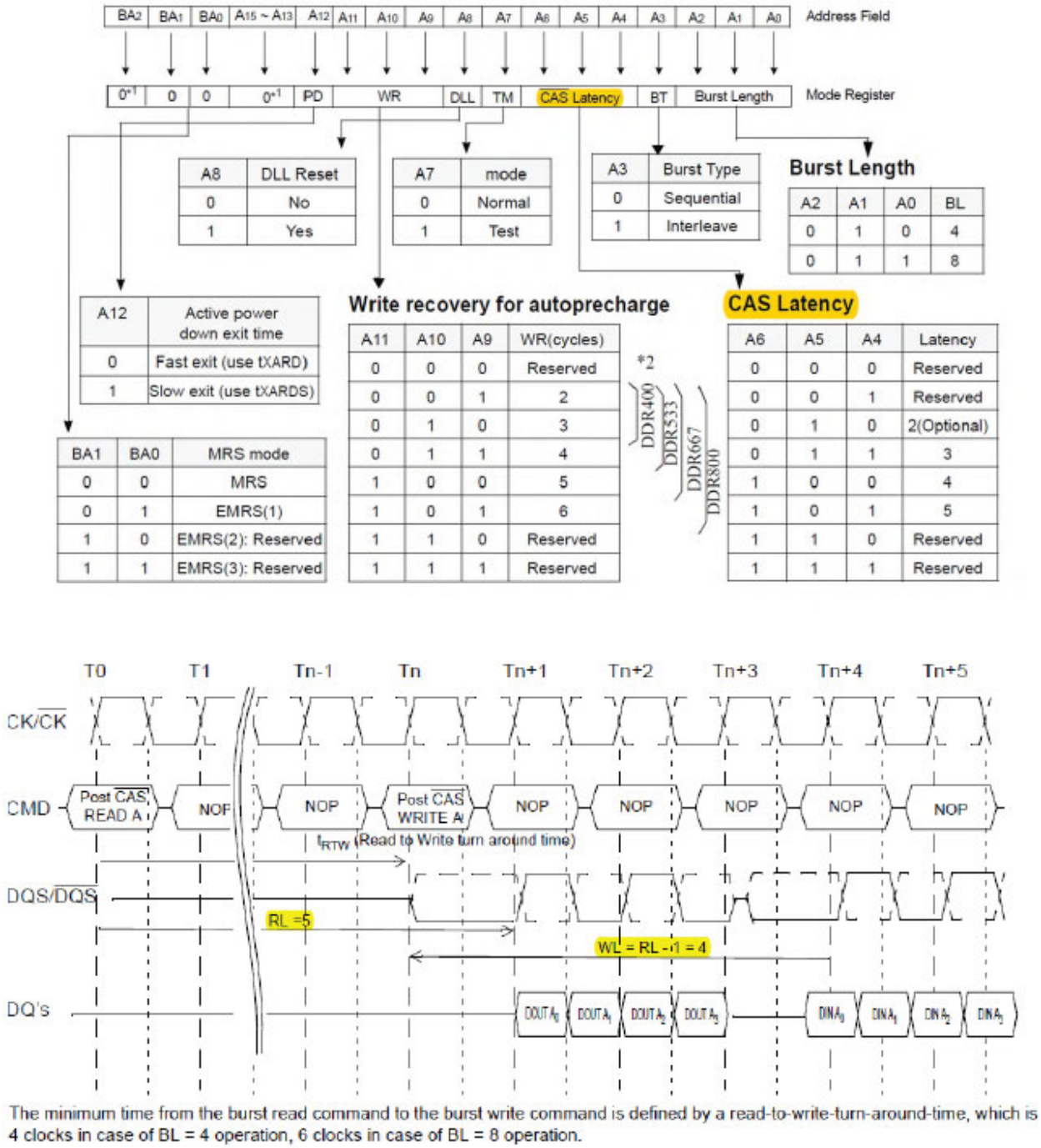
Furthermore, a POSITA would have understood that, because interfaces 520a/b, 510, and 590 include transceivers (e.g., 575), and because multiplexer/demultiplexer circuit 597 (e.g., in 591) contains "multiplexing logic and demultiplexing logic," Perego's buffer device includes logic that sends "*data buffer control signals*" to the transceivers, multiplexing/demultiplexing circuits, and to the input and output latches to selectively activate those circuit elements of the buffer according to the targeted rank and direction of the read and write operations. EX1003, ¶¶341-342; EX1071, 14:62-15:6 ("The address…will determine which target subset of channels 370 will be utilized for the data transfer…"), 17:41-44 ("multiplexing logic is used during read operations, and the demultiplexing logic is used during write operations"), 17:61-62, Figs.5A-5B. For example, the targeted rank can be determined by the logic using the address information, in addition to the input chip-select signals, when Perego's module implements rank multiplication (as discussed above for [1.c.1] (pp.50-51)). EX1003, ¶340; EX1071, 14:63-65, 15:34-40.

#### *(3) [1.e.3] In Accordance with an Overall CAS Latency*

Ground 1 teaches that the "*transfer*" of the "*burst of N-bit wide data signals*" from [1.e.2] (pp.89-91) is done "*in accordance with an overall CAS latency of the*

*memory module* [e.g., per the JESD79-2 standard, as discussed below]." EX1003, ¶¶344-353.

Perego discloses providing "access latency values" to the memory controller during initialization, EX1071, 12:20-34, Fig.5B, and a POSITA would have known from the JEDEC standards (including JESD79-2, shown below) that the data transfers in Perego's memory module are enabled in accordance with these "access latency values," including CAS latency (expressed in terms of an integer number of clock cycles), which are programmed during initialization by the memory controller and used to properly time burst operations to comply with the JEDEC standards, see EX1064, pp.12 (first below, showing "CAS Latency" of 2, 3, 4, or 5 clock cycles), 14 (permitting additional "Additive Latency" of 1 clock cycle), 26 (Read Latency (RL)=Additive Latency (AL), if any, plus CAS Latency (CL)), 28 (second below, showing timing of burst in accordance with latency values). EX1003, ¶¶347-349.




The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation.

**Figure 26 — Burst Read Followed by Burst Write: RL = 5, WL = (RL-1) = 4, BL = 4**

The Board has previously concluded, in finding claims unpatentable from a family member of the 417 Patent, that it would have been obvious to a POSITA to enable data communications in accordance with a CAS latency value to ensure

proper data transfer. *See* EX1030, pp.3 (last limitation), 7-14. That finding is now binding against Netlist, as explained above (p.20).

Furthermore, a POSITA would have understood that any scheduled data transfer to or from the memory module must account for the latency of the ***entire*** module ("*overall CAS latency of the memory module*"), including the latency of the memory devices (e.g., 3 clock cycles for the memory devices, 360 below) combined with the latency added by the buffer device (e.g., 1 clock cycle for the buffer device, red below, which sits between the memory devices and the memory controller). EX1003, ¶¶350-351; EX1062, p.68 n.1 (adding "an additional clock cycle" to the "CAS latency" of the memory devices to leave enough time for the register on the DIMM to perform its functions).

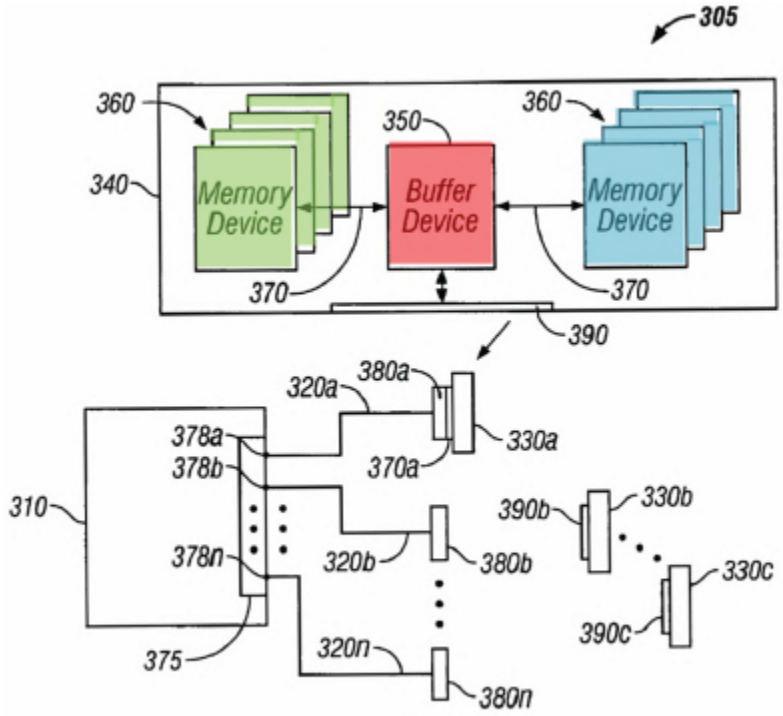



FIG. 3B

#### *f) [1.f] CAS Latency*

Ground 1 teaches "*wherein data transfers through the circuitry* [from [1.e.2] (pp.89-91)] *are registered for an amount of time delay* [e.g., 1 clock cycle, similar to registering address and command signals in a Registered DIMM (RDIMM), *see* EX1062, p.68 n.1] *such that the overall CAS latency of the memory module* [from [1.e.3] (pp.92-94), e.g., 4 clock cycles] *is greater than an actual operational CAS latency of each of the memory devices* [e.g., 3 clock cycles, *see* EX1064, p.12]." EX1003, ¶¶354-378.

Under the JEDEC standards, "an additional clock cycle" is added to the "CAS latency" of the memory devices to leave enough time for the register on the memory module to perform its functions. *See* EX1062, p.68 n.1; EX1064, pp.12 ("CAS Latency" of 2, 3, 4, or 5 clock cycles), 14 (permitting additional "Additive Latency" of 1 clock cycle); EX1003, ¶¶359-362. It would have been obvious to add one additional clock cycle to Perego for the same reason, i.e., so that the memory module complies with the timing of the JEDEC standards, and so the "circuitry" has enough time to perform its functions (including "*register[ing]*" the data signals for interfaces 520a/b with latches 597f-m, blue, below) using "internal" clock circuit 570a-b (purple, below). EX1003, ¶¶359-362; EX1071, 18:65-19:3, 17:61-63, 12:65-13:5, Figs.5B-5C.

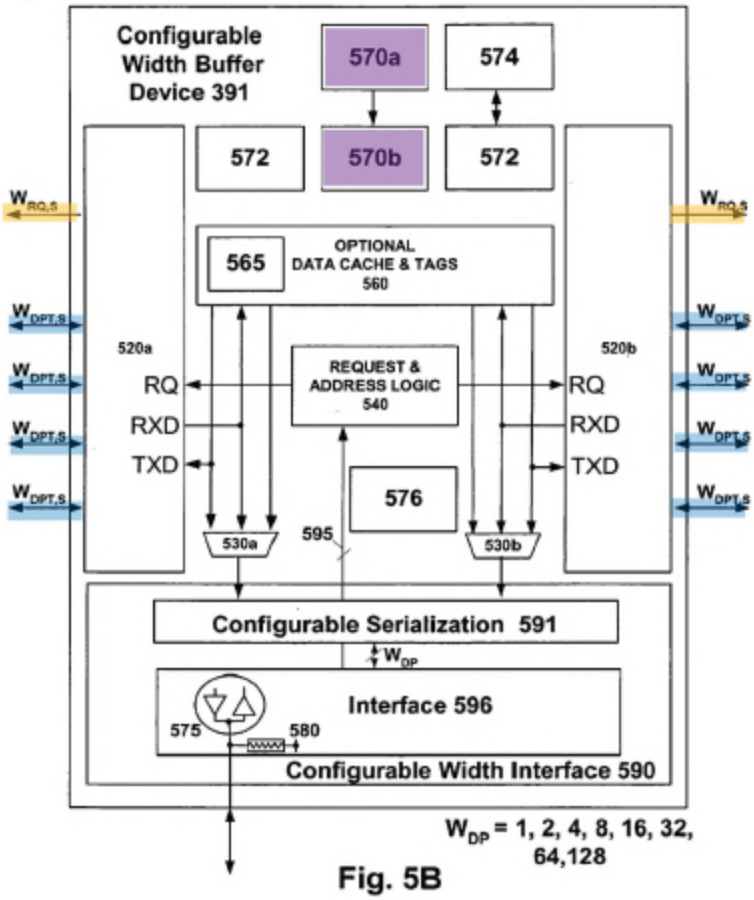

Configurable Width Buffer Device 391
570a
574
572
570b
572
565
OPTIONAL DATA CACHE & TAGS 560
520a
520b
REQUEST & ADDRESS LOGIC 540
RQ
RXD
TXD
576
530a
595
530b
Configurable Serialization 591
Interface 596
575
580
Configurable Width Interface 590
$W_{DP}$ = 1, 2, 4, 8, 16, 32, 64,128

Fig. 5B

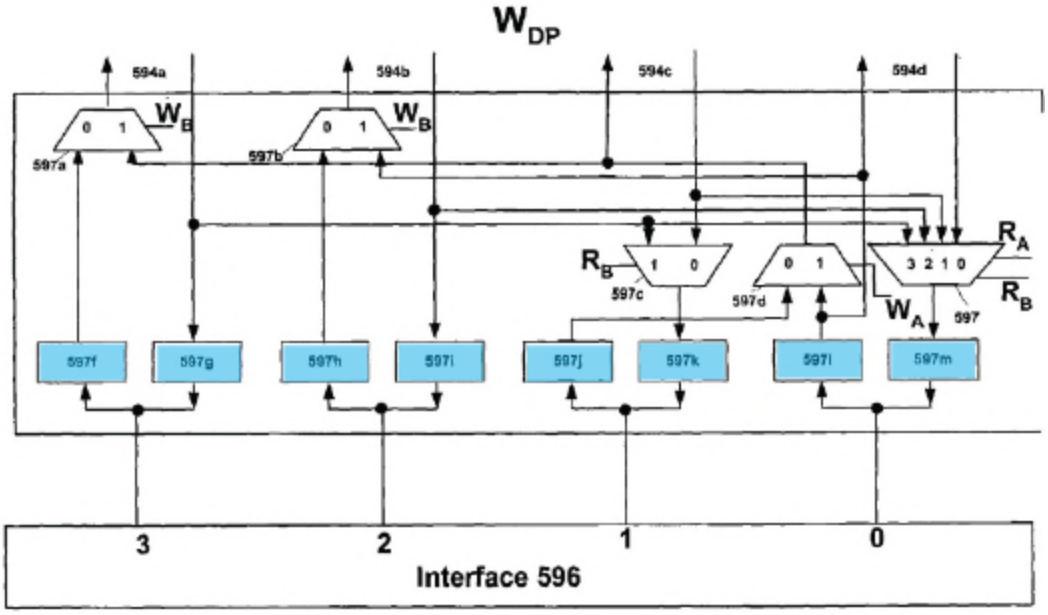

$W_{DP}$
594a
594b
594c
594d
$W_B$
597a
597b
$R_B$
597c
597d
$R_A$
$W_A$
597
597f
597g
597h
597i
597j
597k
597l
597m
3
2
1
0
Interface 596

Fig. 5C

### 3. Claim 2

Ground 1 teaches *"[t]he memory module of claim 1, wherein each of the memory devices has a corresponding load, and the circuitry* [from [1.e.1] (pp.85-88) including, e.g., input-output latches 597f-m] *is configured to isolate the loads of the memory devices from the memory bus* [from [1.a.2] (pp.36-40)]." EX1003, ¶¶379-385. For example, Perego teaches that its buffer device "effectively reduces the number of loading permutations on the corresponding point-to-point link to one." EX1071, 6:44-46; *see also id*., 4:38-45 ("buffer device...isolating data...signals"), 6:12-15 ("buffer device…provides isolation between…controller 310 and…memory devices 360."), 17:61-63 ("latches 597f-m…for…buffer device"). A POSITA would have understood the input and output latches 597f-m isolate the load of the "*memory devices*" from the memory controller (on the "*memory bus*") since the memory controller only sees the load of the latches 597f-m. EX1003, ¶383.

### 4. Claim 3

Ground 1 teaches "*[t]he memory module of claim 1, wherein the burst of N-bit wide data signals* [from [1.d.3] (pp.74-84) and [1.e.2] (pp.89-91), e.g., for DDR2 memory devices complying with JESD79-2] *includes a set of consecutively transmitted data bits for each data signal line in the memory bus* [e.g., a "Burst" of read or write data on the "DQ" lines under the JESD79-2 standard, below, to/from

the rank of memory devices targeted by the buffer device], *and wherein the set of consecutively transmitted data bits are successively transferred through the circuitry* [from [1.e.1] (pp.85-88)] *in response to the data buffer control signals* [from [1.c.4] (pp.61-63), e.g., to control the routing and timing of the transfer]." EX1003, ¶¶386-394.

A POSITA would have understood from JESD79-2 that DDR2 memory devices transmit or receive data in "bursts," as shown below (Figures 25, 31). EX1064, pp.25-32. EX1003, ¶¶389-390. Those "bursts" are timed in accordance with latencies (e.g., CL=CAS Latency, RL=Read Latency, WL=Write Latency, AL=Additive Latency) and burst lengths (e.g., BL=4 or 8), *see id*. p.24, programmed by mode register commands (e.g., third below), so that the data communication between the memory controller and the memory module is properly synchronized, *see id*. pp.12-14. EX1003, ¶391. Accordingly, it would have been obvious for the "*data buffer control signals*" to control the routing (e.g., write vs. read to/from the targeted rank) and timing of the "*set of consecutively transmitted data bits...successively transferred through the circuitry*" to comply with the timing of the JESD79-2 standard. *Id*.

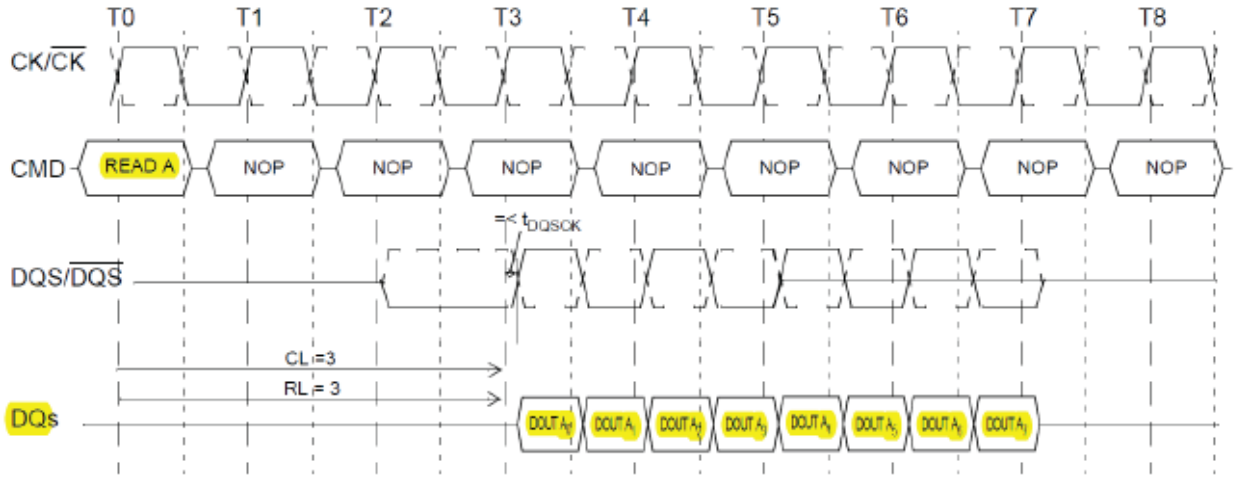



**Figure 25 — Burst Read Operation: RL = 3 (AL = 0 and CL = 3, BL = 8)**

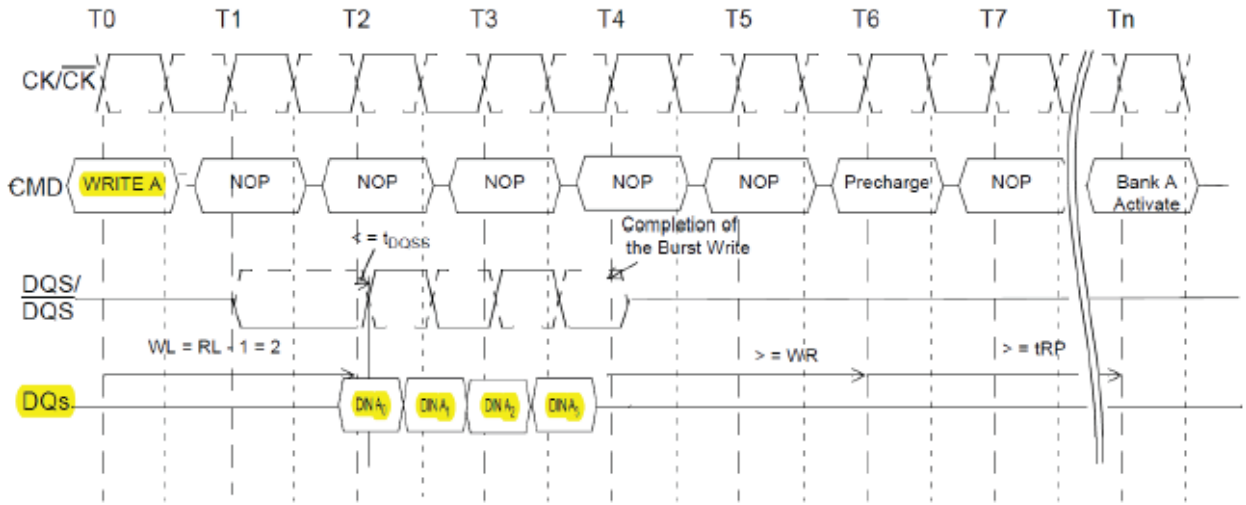
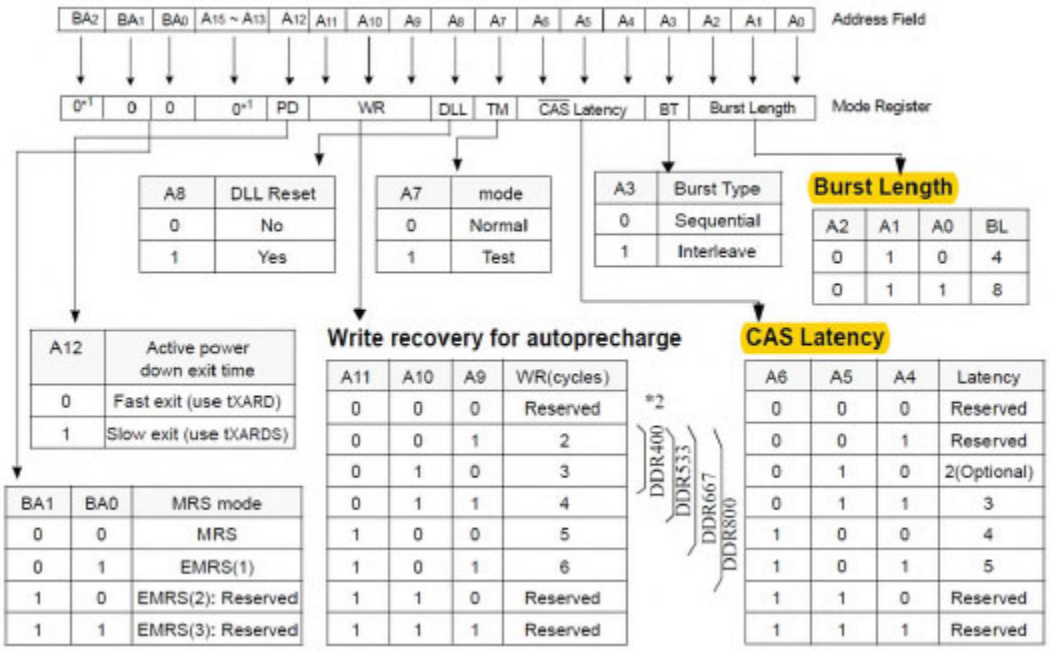



**Figure 31 — Burst Write Operation: RL = 3, WL = 2, tWR = 2 (AL=0, CL=3), BL = 4**




### 5. <u>Claim 4</u>

Ground 1 teaches "*[t]he memory module of claim 1, wherein each of the memory devices is 4-bits wide* [e.g., "x4" DDR2 memory devices, see EX1064, pp.7-8], *and wherein each of the plurality of ranks is 64-bits or 72-bits wide* [from [1.d.1] (pp.64-73), where 72-bits is when 8 bits, CB0-CB7, are added for error correction ("ECC"), EX1071, 10:48-53; EX1062, pp.5, 6; EX1066, pp.4, 6] *and includes 16 or 18 memory devices* [for 64 or 72 bits, respectively] *configured in pairs* [e.g., pairs of "x4" memory devices, consistent with the JEDEC standards, e.g., EX1062, pp.15-16 (showing two 72-bit-wide ranks, each with 9 pairs of x4 memory devices, such as the pair D0 and D9 both connected to the same chip-select signal RS0, where D0 is for the lower nibble DQ0-DQ3 and D9 is for the upper nibble DQ4-DQ7); EX1066, pp.12-15 (similar)]." EX1003, ¶¶395-400.

### 6. Claim 5

Ground 1 teaches "*[t]he memory module of claim 1, wherein the memory devices are organized in four ranks* [e.g., light and dark blue, and light and dark green, in Perego's Figure 4B (below), since each memory interface 415a-415d can correspond to a single rank, *see* [1.d.1] (pp.64-73)] *and the set of input address and control signals include four chip select signals* [from [1.c.2] (pp.51-58)], *one for each of the four ranks* [consistent with the JEDEC standards, e.g., EX1062, p.6 ("Physical banks"); EX1066, pp.6-7, 16-17]." EX1003, ¶¶401-406.

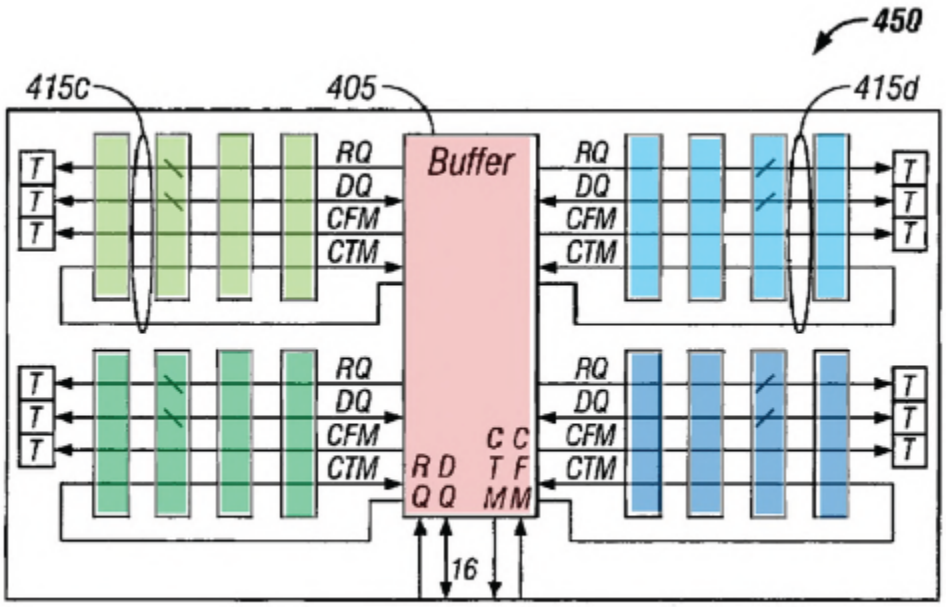



FIG. 4B

### 7. Claim 6

Ground 1 teaches "*[t]he memory module of claim 1, wherein the circuitry* [from [1.e.1] (pp.85-88)] *includes logic pipelines* [e.g., to handle the sequence of commands and corresponding latencies associated with data transfers, EX1064,

pp.23-25, 49] *configurable to enable the data transfers* [from [1.f] (pp.95-96) and [1.e.2] (pp.89-91)] *between the memory devices and the memory bus through the circuitry* [from [1.e.2] (pp.89-91)]." EX1003, ¶¶407-415.

Perego teaches using a "scheme that could potentially route any single data bit signal to any data pair line or to any of the interface 596 data connections," including multiplexer/demultiplexer circuit 597, which routing a POSITA would have understood to include "*logic pipelines*" to enable the "*data transfers*" through the "*circuitry*," all in response to control signals that enable the data transfer. EX1071, 18:48-54, Figs.5B-5C, 17:22-18:9 ("logic"), 13:49-59 ("request & address logic 540"); EX1003, ¶¶412-413.

A POSITA would understand that to properly route the data through the "*circuitry*" (whether or not implementing "rank multiplication"), "*logic pipelines*" would be required, because the JEDEC standards specify that a read or write operation includes at least two steps: a Bank Activate command (with bank and row addresses), EX1064, pp.23, 49, and then a Read or Write command (with bank and column addresses) followed by the actual transfer of data with pre-defined latencies, *id*. pp.24-25 (below), 49. EX1003, ¶¶411, 414.

#### 2.2.4.1 Posted $\overline{\text{CAS}}$

Posted $\overline{\text{CAS}}$ operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a $\overline{\text{CAS}}$ read or write command to be issued immediately after the $\overline{\text{RAS}}$ bank activate command (or any time during the $\overline{\text{RAS}}$-$\overline{\text{CAS}}$-delay time, tRCD, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the $\overline{\text{CAS}}$ latency (CL). Therefore if a user chooses to issue a R/W command before the tRCDmin, then AL (greater than 0) must be written into the EMRS(1). The Write Latency (WL) is always defined as RL - 1 (read latency -1) where read latency is defined as the sum of additive latency plus $\overline{\text{CAS}}$ latency (RL=AL+CL). Read or Write operations using AL allow seamless bursts (refer to seamless operation timing diagram examples in Read burst and Write burst section).

**Examples of posted $\overline{\text{CAS}}$ operation**

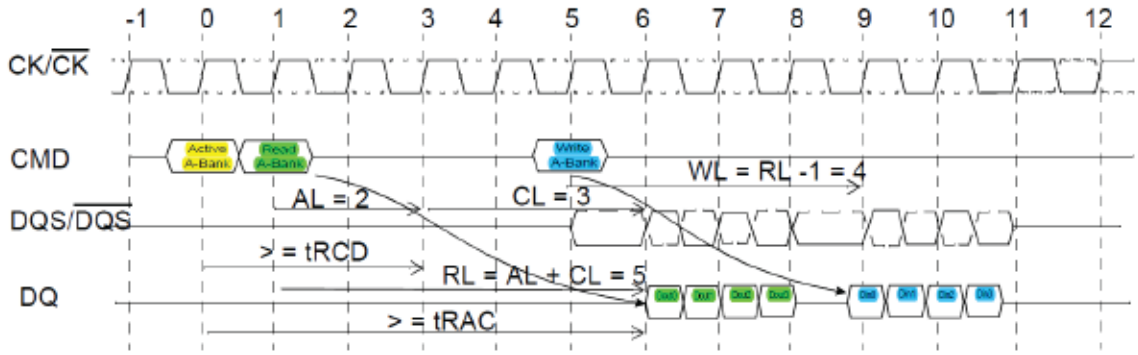



**Figure 21 — Example 1: Read Followed by a Write to the Same Bank [AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4]**

### 8. <u>Claim 7</u>

Ground 1 teaches "*[t]he memory module of claim 1, wherein the logic* [from [1.c.1] (pp.43-51) and [1.c.4] (pp.61-63)] *is further configured to report the overall CAS latency* [from [1.e.3]-[1.f] (pp.92-96)] *to the memory controller* [from [1.a.2] (pp.36-40)] *in response to a mode register set command* [MRS, a standard command in <u>JESD79-2</u>, EX1064, pp.10-14, 49] *received from the memory controller*." EX1003, ¶¶416-424.

A POSITA would have understood from JESD79-2 and Perego that "*mode register set command[s]*" and the module's reporting functionality are used by the "*memory controller*" to initialize the memory module. EX1064, pp.10-14 (below), 49; EX1003, ¶421.

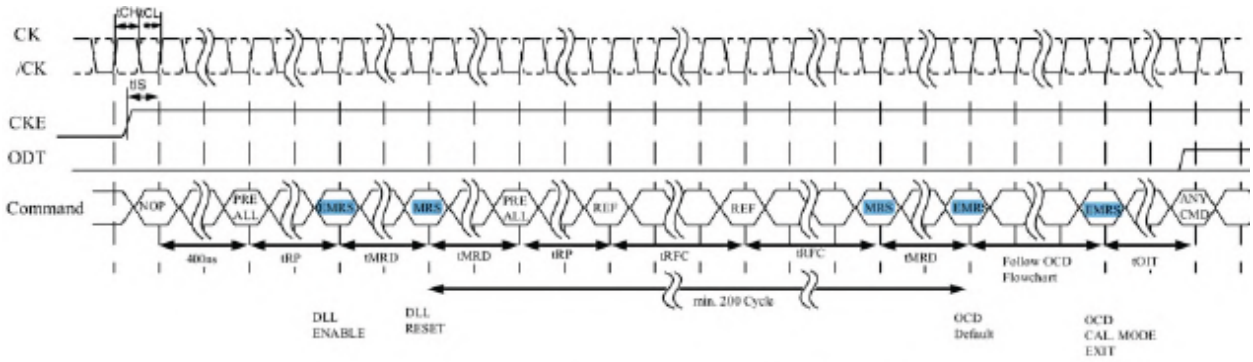



**Figure 7 — Initialization Sequence after Power Up**

A POSITA would have been motivated to report latency parameters during initialization, including reporting "*the overall CAS latency*" of the module, "to properly configure the memory devices upon boot of the system" and to ensure proper timing of commands from the memory controller. EX1071, 12:20-27, 12:32-34, 12:35-42, 12:45-50; EX1003, ¶¶419-420, 422.

### 9. Claim 8

Ground 1 teaches "*[t]he memory module of claim 1, wherein the memory module has a specified data rate* [e.g., indicated by clock signals CFM and CTM, shown in Figures 4A-4B below, used for transferring data to/from the memory controller (vertical lines) and used on the module between the buffer device and memory devices (horizontal lines)], *and wherein the burst of N-bit wide data*

*signals are transferred between the one of the plurality of N-bit wide ranks* [e.g., green or blue] *and the memory controller* [from [1.a.2] (pp.36-40)] *at the specified data rate*." EX1003, ¶¶425-430. Perego teaches that the same clocks (CFM, CTM) are used to transmit data on the system bus (320) and on the bus (415) between the buffer and the memory devices, and that the data width of the module and the rank can be the same (e.g., both 64 bits wide when $W_A/W_{DP}$=1:1, *see* [1.d.1] (pp.64-73)), causing a POSITA to understand that the same "*specified data rate*" is used on the system bus (320) and on the bus (415) between the buffer and the memory devices. EX1071, 9:43-49, 10:5-13, Figs.4A-4B (below); EX1003, ¶¶428-429.

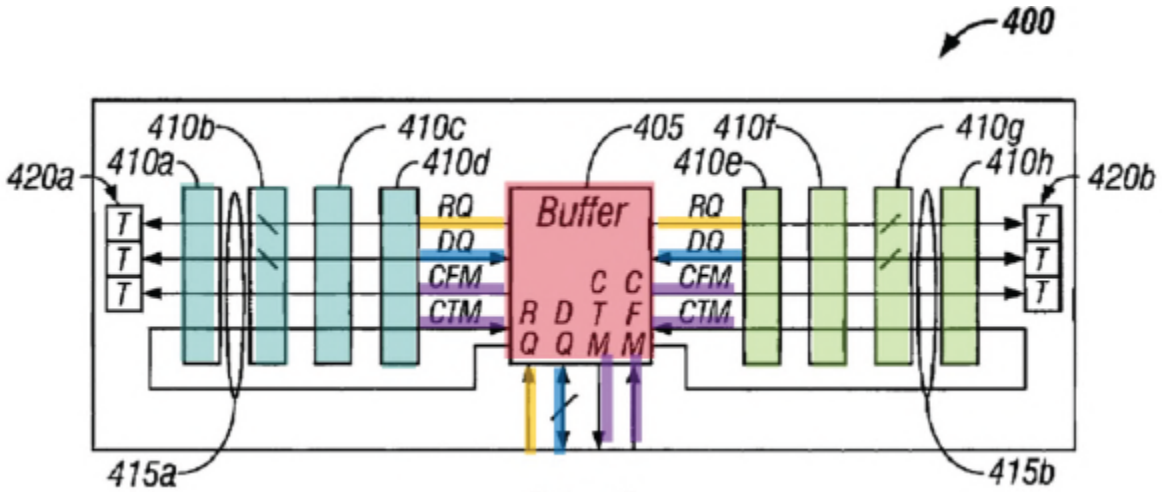



FIG. 4A

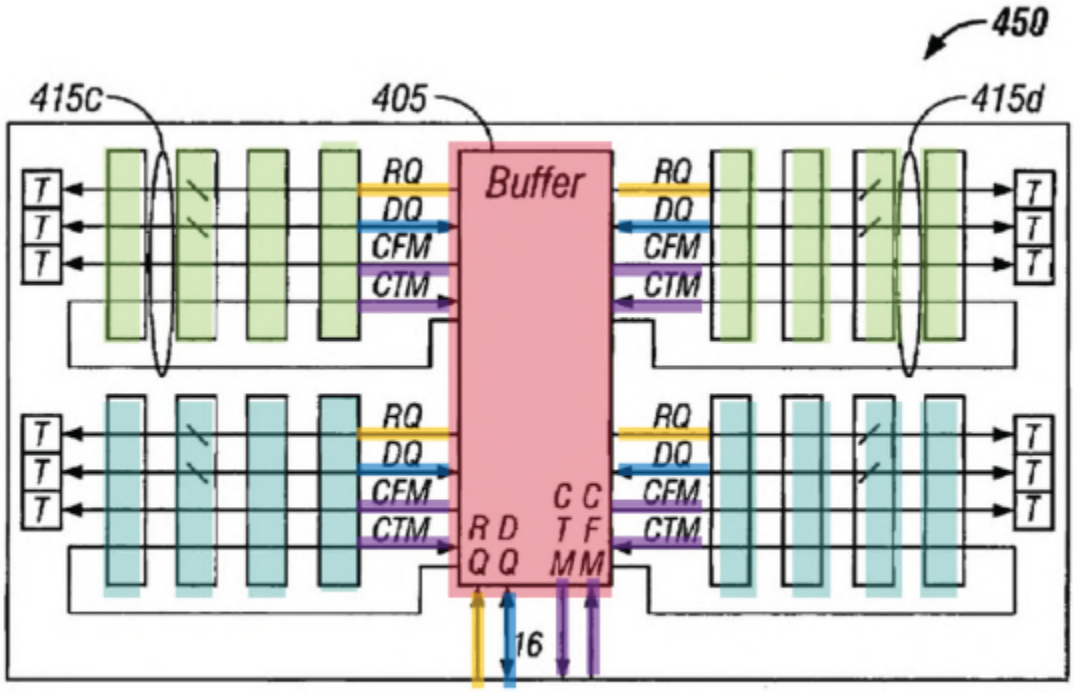



FIG. 4B

**10. <u>Claim 9</u>**

Ground 1 teaches "*[t]he memory module of claim 1, further comprising a phase locked loop* [PLL] *clock driver configured to output a clock signal in response to one or more signals received from the memory controller* [e.g., <u>Perego</u>'s clock circuit 570a-b in the buffer device, which "may include [a] clock generator circuit," implements the functionality of a "PLL" driver to generate clock signals for the module, phase aligned with the clock signals received from the memory controller, EX1071, 12:52-64; *see also* EX1069, p.11 ("PLL");

EX1073, [0030], [0048], Figs.2-6, 10-13 ("PLL")], *wherein the*[6] *predetermined amount of time delay is at least one clock cycle time delay* [e.g., 1 clock cycle, as explained for [1.f] (pp.95-96)]." EX1003, ¶¶431-437.

**11. <u>Claim 10</u>**

Ground 1 teaches "*[t]he memory module of claim 9, wherein the memory devices are dynamic random access memory* [DRAM] *devices* [e.g., double data rate (DDR or DDR2) synchronous dynamic random-access memory (SDRAM) devices, *see* EX1060, EX1064, as explained for [1.d.1] (pp.64-73)] *configured to operate synchronously* [e.g., the "S" in SDRAM, *see* EX1069, p.5; EX1060; EX1064; *see also* EX1071, 4:6-12, 10:58-59 ("DDR2...Synchronous DRAM")] *with the clock signal* [from claim 9 (pp.106-107)], *and wherein each memory device in the one of the plurality of N-bit wide ranks is configured to receive or output a respective set of bits of the burst of N-bit wide data signals on both edges of each of a respective set of data strobes* [consistent with <u>JESD79-2</u>, e.g., EX1064, pp.24-32 (showing bits of data burst on both edges of complementary set of $DQS/\overline{DQS}$ data strobes, EX1064, p.6); *see also* EX1069, p.7 (DDR "transfer[s]

---

[6] There is no antecedent basis for "*the <u>predetermined</u> amount of time delay*," but [1.f] (pp.95-96) refers to "*an amount of time delay*." EX1003, ¶433.

data at both edges of the clock (i.e., both the rising edge and the falling edge)"; EX1071, 4:6¬12]." EX1003, ¶¶438-441.

**12. <u>Claim 11</u>**

Ground 1 teaches "*[t]he memory module of claim 1, wherein the circuitry* [from [1.e.1] (pp.85-88), red below, including multiplexers 530a/b, and interfaces 520a/b and 510 or 590 (and respective transceivers in those interfaces)] *includes data paths* [e.g., 64-bit-wide "configurable datapath router," EX1071, 15:34-37, for selectively coupling the memory bus, on one hand, to the rank of memory devices targeted by the buffer device for a read or write command, on the other hand, as explained for [1.c.4] (pp.61-63)], *and wherein the circuitry is configurable to enable the data paths in response to the data buffer control signals* [from [1.c.4] (pp.61-63) and [1.e.2] (pp.89-91)] *so that the burst of N-bit wide data signals* [from [1.d.3] (pp.74-84) and [1.e.2] (pp.89-91)] *are transferred via the data paths*." EX1003, ¶¶442-448.

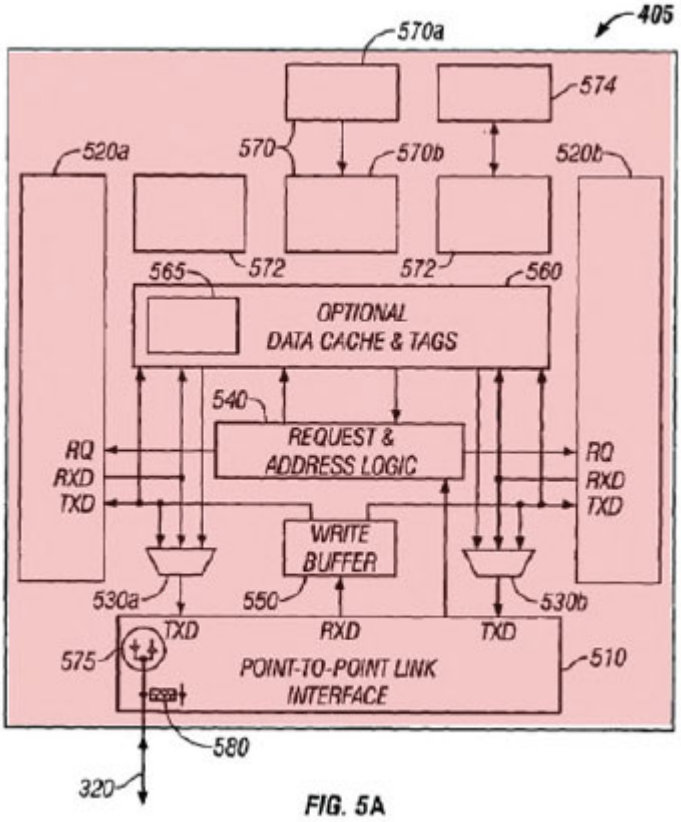

405
570a
574
520a
570
570b
520b
565
572
572
560
OPTIONAL
DATA CACHE & TAGS
540
REQUEST &
ADDRESS LOGIC
RQ
RXD
TXD
RQ
RXD
TXD
WRITE
BUFFER
530a
550
530b
TXD
RXD
TXD
575
POINT-TO-POINT LINK
INTERFACE
510
580
320

FIG. 5A

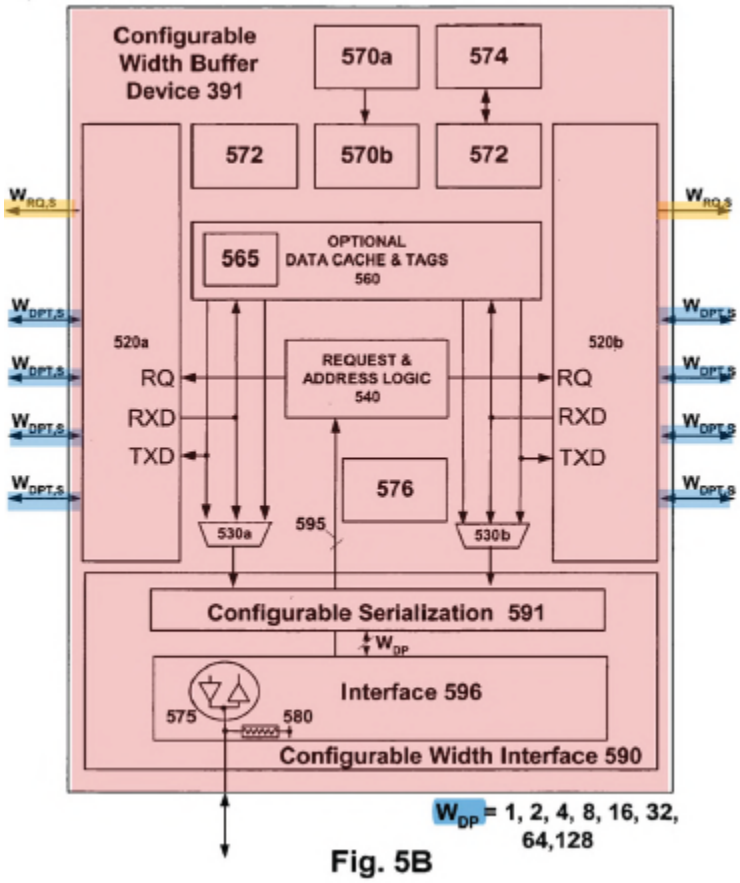



Fig. 5B

### 13. <u>Claim 12</u>

Ground 1 teaches "*[t]he memory module of claim 11, wherein the data paths* [from claim 11 (pp.108-110)] *are disabled when no data signals associated with any memory command are being transferred through the circuitry* [e.g., to avoid collisions and save power, and because there is no reason to enable them]." EX1003, ¶¶449-452; EX1071, 15:40-43 ("reduced power consumption"), 21:16¬28; EX1068, pp.89-90, 132-33 (disabling data paths to avoid collisions on the data bus).

### 14. Claims 13-15

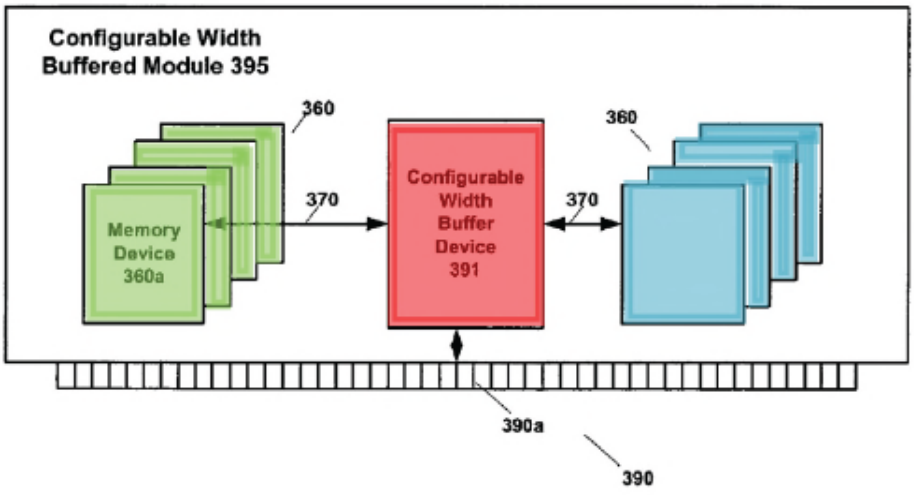
Claims 13-15 are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Ground 1 for at least the same reasons discussed above:

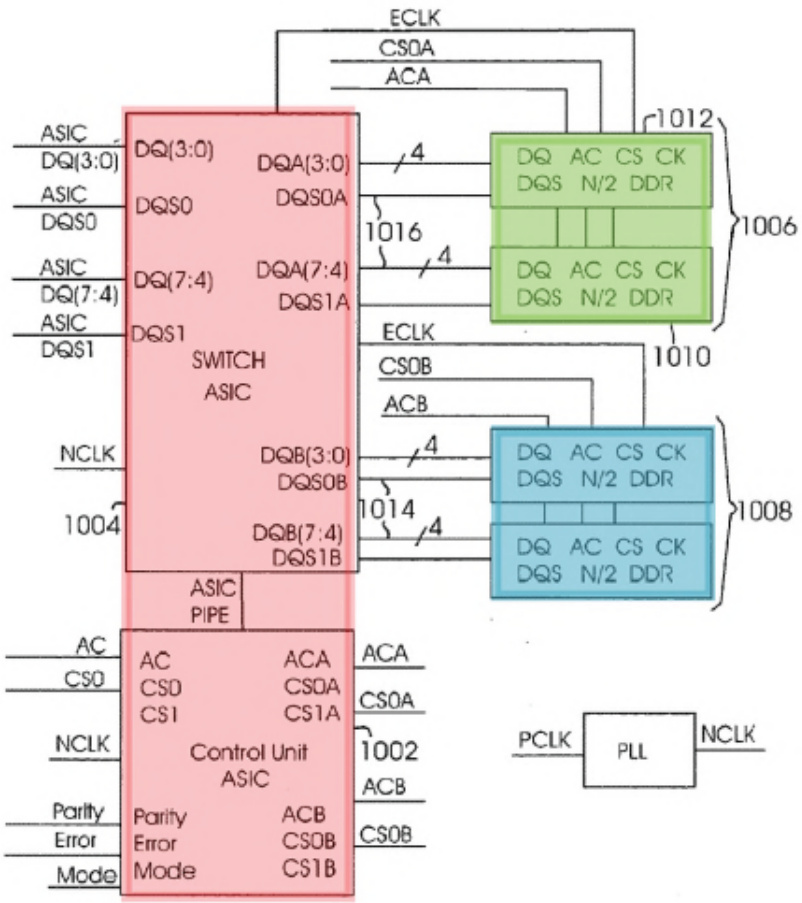
| This limitation... | ...is substantially similar to this limitation... | ...and thus obvious for at least the same reasons above and as discussed in EX1003: |
|---|---|---|
| [13] | [2] | ¶¶453-457 (¶¶379-385) |
| [14] | [8] | ¶¶458-462 (¶¶425-430) |
| [15] | [3] | ¶¶463-467 (¶¶386-394) |

## B. Ground 2

### 1. Ground 2 combination: Ground 1 + Ellsberry (EX1073)

Ground 2 combines Ground 1 (Perego + JESD79-2) with the teachings of Ellsberry (EX1073). EX1003, ¶¶188-195. As shown below, Perego and Ellsberry disclose memory modules with a similar structure:

| | |
|---|---|
| EX1071, Fig.3C (Perego) |  <br>Fig. 3C |

| | |
|---|---|
| EX1073, Fig.10 (Ellsberry) |   |

Ellsberry (introduced above, pp.20-22) is analogous art because it is directed to efficiently organizing and using memory systems, including expanding memory module capacity "without the need for additional chip select lines on the main memory bus." EX1073, Abstract, [0026]; EX1003, ¶188. Ellsberry also uses DDR and DDR2 SDRAM memory devices with memory modules in a DIMM format, like Perego and the 417 Patent, and expressly incorporates by reference the corresponding JEDEC standards, including JESD79-2 (EX1064). EX1073, [0023],

[0046], [0053], Claim 10; EX1003, ¶¶189, 191. Ellsberry also teaches "rank multiplication" (discussed above, pp.10-12), like Perego (as discussed for [1.c.3] (pp.58-61)) and the 417 Patent (pp.12-15). EX1003, ¶191; EX1073, [0026] ("two separate SDRAM DDR devices...emulate a single, two-times capacity, SDRAM DDR device" "without the need for additional chip select lines on the main memory bus"), Figs.7A-7F.

A POSITA would have been motivated to combine Ground 1 with Ellsberry because they would have recognized the relevance of the JEDEC standards, including JESD79-2, to both Perego and Ellsberry. EX1003, ¶190. A POSITA also would have been motivated to make the combination given Ellsberry's detailed description of how to implement "rank multiplication" using JEDEC-compliant memory devices, thus providing significant cost savings (discussed above, pp.10-12) that could be applied to Perego's module. EX1003, ¶191.

A POSITA would have recognized that both Ellsberry and Perego buffer the data signals on the module, advantageously reducing the load on the data lines. EX1003, ¶193. Perego discloses a centralized buffer for the data signals, like the preferred embodiment of the 417 Patent, while Ellsberry discloses distributed data buffers, and a POSITA would have understood that these implementations were known alternatives for data buffering. *Id.*; EX1078, 10:1-6 (recognizing these alternatives). Therefore, a POSITA would have been motivated to look at

analogous art like Ellsberry for details about implementing memory modules with data buffering, such as Perego. EX1003, ¶193.

A POSITA would have recognized that applying Ellsberry's teachings to Ground 1 (Perego+JESD79-2) would have resulted in a predictable variation, improving similar devices in the same way and not yielding unexpected results or challenges. EX1003, ¶¶192, 194. Furthermore, a POSITA would have recognized that, because both Perego and Ellsberry disclose buffering data signals and using JEDEC-compliant memory devices, they provide alternative, predictable solutions for operating memory modules with data buffering capabilities in accordance with the JEDEC standards. EX1003, ¶194. Therefore, it would have been at least obvious to a POSITA to try the proposed combination. *Id*.

**2. Claims 1-15**

Ground 2 renders obvious claims 1-15 for at least the same reasons provided above for Ground 1 (pp.28-111), since Ground 2 incorporates Ground 1.

**3. Claims 1-3, 6, 8, 10-11**

Ground 2 further renders obvious claims 1 (pp.33-96), 2 (pp.97-97), 3 (pp.97-100), 6 (pp.101-103), 8 (pp.104-106), 10 (pp.107-108), and 11 (pp.108-110).

Ellsberry teaches "rank multiplication," just like the 417 Patent, where two "*N-bit wide ranks*" of DDR2 SDRAM "*memory devices*" on the "*printed circuit*

*board*" (e.g., 72-bit-wide ranks, green and blue, below, which Ellsberry calls "banks") emulate a single, higher-density rank. EX1073, Abstract, [0047], [0049]-[0051], Figs.2, 5-6, 8B n.3, 10-13, claim 10; EX1076, pp.21-22; EX1003, ¶¶242, 294.

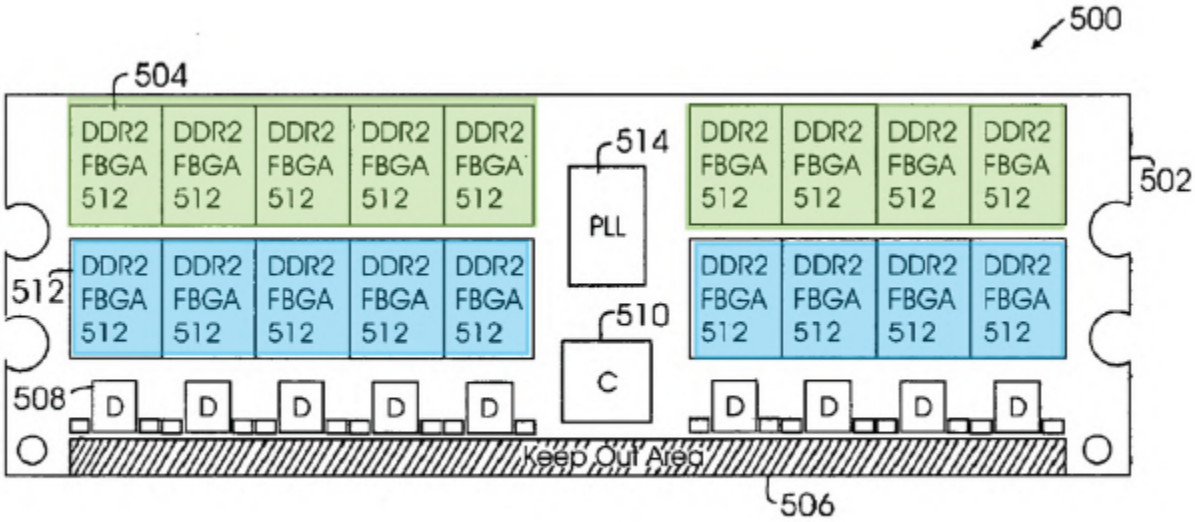
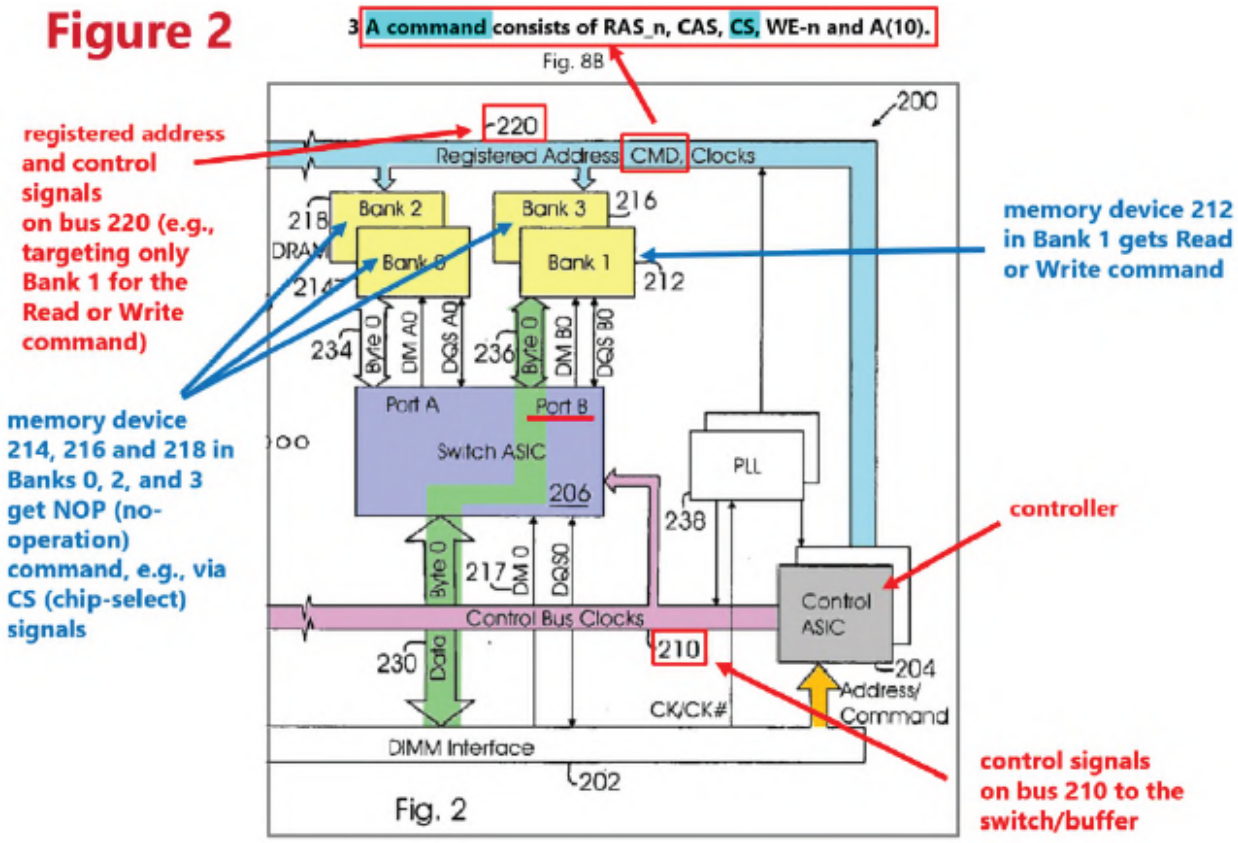



Fig. 5

As shown below, "Bank 0" and "Bank 1" are two different "*memory devices*" in two different "*ranks*" connected to two different "*data paths*" (234 to Port A vs. 236 to Port B) together emulating a single, higher-density memory device in a single rank. EX1073, Abstract, [0011], [0036], claim 1, Figs.2, 4, 7A-7F, 8A-8B, 10-13. EX1003, ¶¶242, 253, 262.




As shown above, Ellsberry's "Control ASIC" (204, grey) includes "*logic*" to "*receive a set of input address and control signals associated with a read or write memory command* [orange above] *via the address and control signal lines and to output a set of registered address and control signals* [on 220, blue, "Registered"] *in response to the set of input address and control signals*." *Id*.

The "*logic*" also provides "*data buffer control signals*" on 210 (purple) to the "*circuitry*" (Switch ASICs, blue), which "*isolate[s] the load of the memory devices*," where the "*logic*" uses the received address information and chip-select signals associated with a read or write "*memory command*" (as shown in Figures 7A-7F) to (i) cause the "*circuitry*" to choose either one "*data path*" (e.g., Port A

connected to one rank) or another "*data path*" (e.g., Port B connected to another rank) to "*transfer the burst of N-bit wide data signals*" at a "*specified data rate*" (in accordance with the JESD79-2 standard, incorporated by reference) as shown in Figures 2 and 8A, and to (ii) generate additional "*registered chip select signals*" (as shown in Figures 10-13, e.g., CS0A and CS0B) so that only the targeted rank (e.g., Bank 1) gets an "*active*" "*registered chip select signal*" on 220 (as part of the read or write command) while all the other ranks get a "*non-active*" "*registered chip select signals*" on 220 (i.e., a NOP or "Deselect" command). EX1003, ¶¶242, 253, 262, 272, 312-313, 340, 384, 392-393, 411, 444; EX1073, [0010], [0012], [0036], [0046], Figs.2-4, 7A-7F, 8A-8B, 10-13, Claim 1; EX1060, p.13, n.9 ("DESELECT and NOP are functionally interchangeable"); EX1064, p.48 (similar); EX1074, pp.31-37 (Final Written Decision finding that Ellsberry discloses sending NOP commands to the non-targeted ranks), 52-56 (finding that each Switch ASIC presents a single load to both the memory controller and to each memory device).

#### 4. [1.e.3]-[1.f] and [9]

Ground 2 further renders obvious [1.e.3]-[1.f] (pp.92-96) and [9] (pp.106-107), concerning "*overall CAS latency of the memory module*" that is "*greater than an actual operational CAS latency of each of the memory devices*" by "*at least one clock cycle*." EX1003, ¶¶374-378, 434-436. Ellsberry teaches that the command

from the memory controller setting the CAS latency for the DDR memory devices should be modified so that it is one clock cycle less than specified by the memory controller:

| Command | Mode | Addr | P Bank | DDR A | | DDR B | |
|---|---|---|---|---|---|---|---|
| | | | | Command | Addr | Command | Addr |
| MRS | X | X | X | MRS | 1 | MRS | 1 |
| EMRS | X | X | X | EMRS | 2 | EMRS | 2 |

NOTES: 1. if cl_mode. = subtract; cl = cl - 1 to DDRs
2. ods squelch-based on ODS setting, rtt squelch-based on REFF setting, ocd squelch-default, dqs_n enable, rdqs disable, out squelch - enable

EX1073, [0044], Figs.8A-8B; EX1003, ¶¶376-377. The result is that the "*overall CAS latency of the memory module*" is "*one clock cycle*" more than the "*actual operational CAS latency of each of the memory devices*." *Id*.

Ellsberry also teaches the use of a "*phase locked loop [PLL] clock driver configured to output a clock signal in response to one or more signals received from the memory controller* [e.g., input clock signals]." *See* EX1073, [0030], [0048], Figs.2-6, 10-13 ("PLL"). EX1003, ¶¶435-436.

**5. Claim 4**

Ground 2 further renders obvious claim 4 (pp.100-100) because Ellsberry discloses 18 4-bit-wide (i.e., "x4") "*memory devices configured in pairs*" resulting in 72-bit-wide "*ranks*." EX1003, ¶399; EX1073, [0051], Figs.6 (showing each rank

has 9 pairs of stacked x4 memory devices, corresponding to Figure 11), 11 (showing, e.g., a pair of x4 memory devices connected to chip-select signal CS0A, with DQA(3:0) for the lower nibble and DQA(7:4) for the upper nibble); EX1074, pp.66-68, 76-81 (Final Written Decision finding that Ellsberry's Figures 6 and 11 disclose pairs of x4 memory devices); *id*., pp.17, 25 (finding that Ellsberry discloses a total bit-width of N=Mxn, where M is 9 and n is 8).

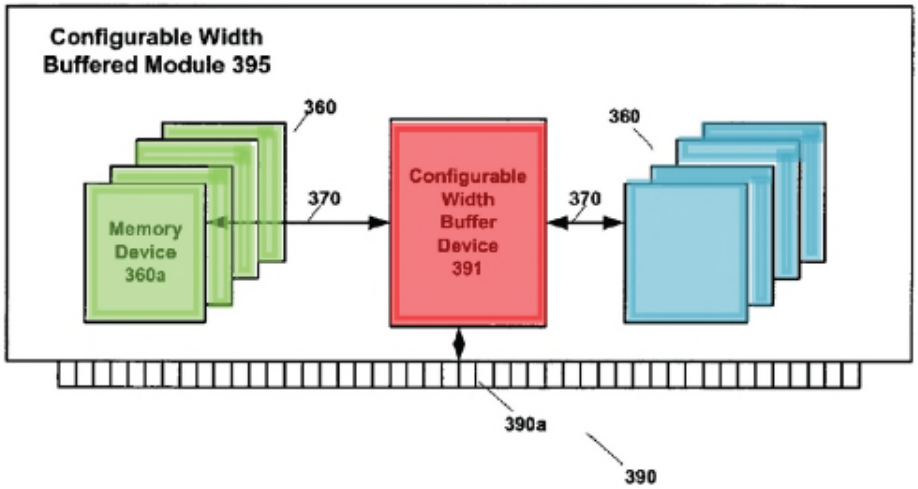
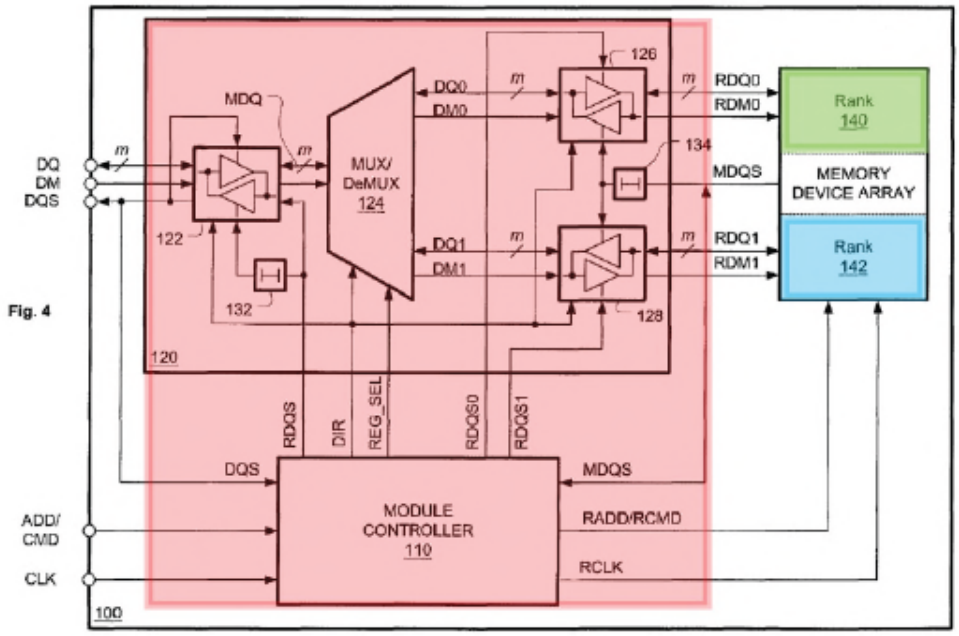
#### 6. Claims 13-15

The limitations of claims 13-15 are substantially identical to earlier limitations, as shown in the table above (p.111-111), and thus they are obvious in light of Ground 2 for at least the same reasons discussed above.

### C. Ground 3

#### 1. Ground 3 Combination: Ground 1 + Halbert (EX1078)

Ground 3 combines Ground 1 (Perego + JESD79-2) with the teachings of Halbert (EX1078). EX1003, ¶¶196-200. As shown below, Perego and Halbert disclose memory modules with a similar structure:

| | |
|---|---|
| EX1071, Fig.3C (Perego) |  <br>Fig. 3C |
| EX1078, Fig.4 (Halbert) |  <br>Fig. 4 |

Halbert (introduced above, pp.22-25) is analogous art because it is directed to efficiently organizing and using memory systems, including expanding DIMM-formatted memory modules by using one or more buffers (red) to isolate the

memory devices (green, blue) from the memory controller. EX1078, 1:16-19, 3:58-4:8; EX1003, ¶196. Halbert also discloses using DDR memory devices, EX1078, 9:55-59, similar to the DDR2 memory devices standardized by JESD79-2. EX1003, ¶196.

A POSITA would have been motivated to look at analogous art like Halbert for details about implementing memory modules with data buffering like Perego. EX1003, ¶197. For example, a POSITA would have been motivated to use Halbert's rank-based arrangements in Perego's module (by itself or as modified in view of JESD79-2) since they "allow the memory devices to be isolated from the full capacitive loading effects of the system memory data bus...[and] avoid arrangements of competing memory banks that load each other, as is the case with a dual-bank DIMM." EX1078, 3:67-4:5; EX1003, ¶295. A POSITA also would have been motivated to combine Halbert's teaching about the timing of subsequent read commands and the corresponding delays of the read data through the data buffer with the JEDEC requirements for latencies of memory devices and memory modules in order to be "compatible with an existing memory controller/bus and with existing memory devices." EX1078, 3:48-57; EX1003, ¶¶197-198.

A POSITA would have recognized that the combination would have resulted in a predictable variation, which would improve similar devices like Perego in the same way and not yield unexpected results or challenges. EX1003, ¶198. For

example, a POSITA would have understood that buffering both address/command and data signals on the module allows advantageously operating multiple memory ranks, and permits "rank multiplication" (discussed above, pp.10-12) to enable significant cost savings. EX1003, ¶199.

### 2. Claims 1-15

Ground 3 renders obvious claims 1-15 for at least the same reasons provided above for Ground 1 (pp.28-111), since Ground 3 incorporates Ground 1.

### 3. [1.d.1]

Ground 3 further renders obvious [1.d.1] (pp.64-73), concerning "*N-bit wide ranks*," given Halbert's disclosure of m-bit wide ranks in Figure 4, below (green and blue), where "m" can be 64 bits. EX1078, Abstract, Fig.4 (below). EX1003, ¶¶291-295. Specifically, as shown below, Halbert teaches a memory module including two memory ranks 140 (green) and 142 (blue) on separate data paths, and buffering circuitry (red) (which includes a module controller 110 and a data interface circuit 120) that interfaces with the two ranks on one side (right), and with the system memory bus on the other side (left), thus teaching the claimed "*N-bit wide ranks*" limitations. EX1078, 4:36-39, 4:49-59, 5:6-11, Fig.4 (below); EX1003, ¶¶291-292.

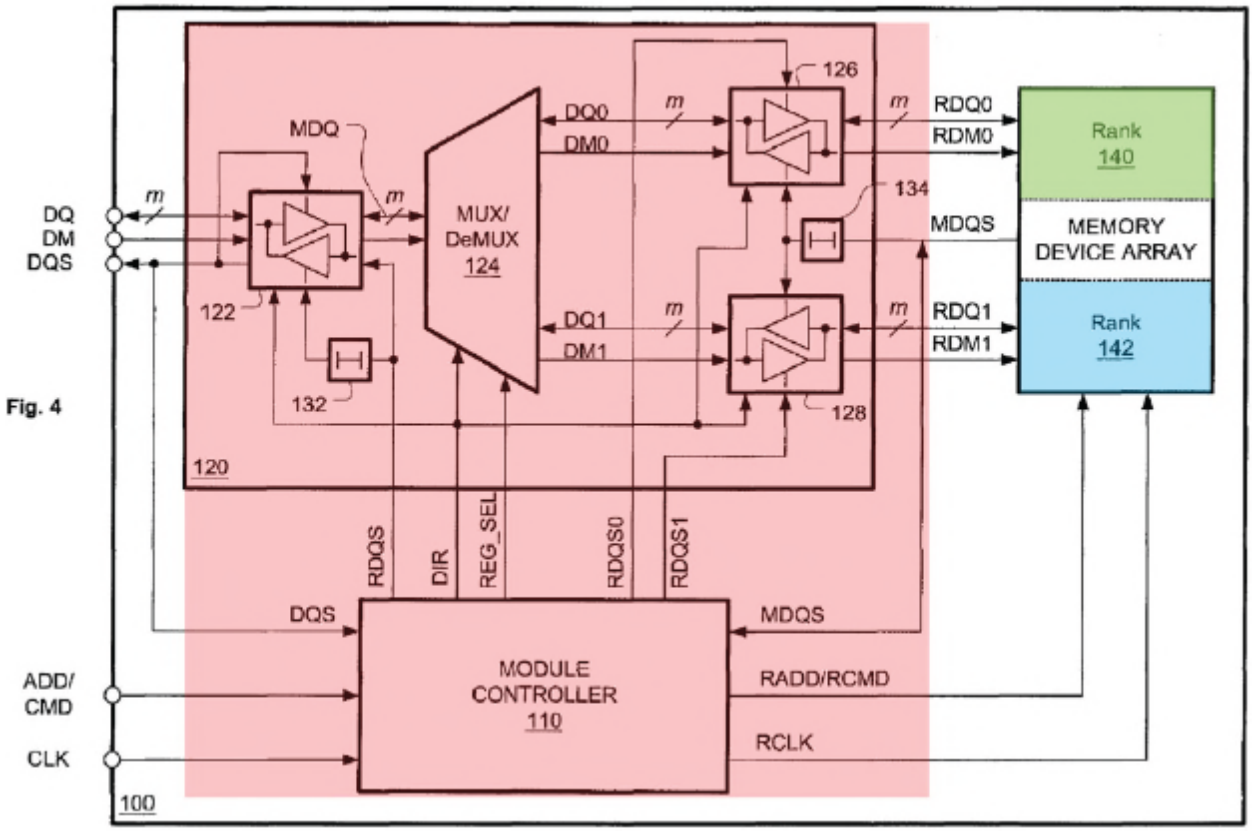



Fig. 4

### 4. [1.e.3]-[1.f] and [9]

Ground 3 further renders obvious [1.e.3]-[1.f] (pp.92-96) and [9] (pp.106-107), concerning "*overall CAS latency of the memory module*" that is "*greater than an actual operational CAS latency of each of the memory devices*" by "*at least one clock cycle*," as shown by Figures 3 and 5 of Halbert below. EX1003, ¶¶364-373; EX1078, 2:46-58 ("one-clock cycle delay"), Fig.3 (first below), 4:60-62, 5:6-11, Fig.4 (above), 5:66-6:65, Fig.5 (second below); *see also* EX1060, p.10 ("Read Latency").

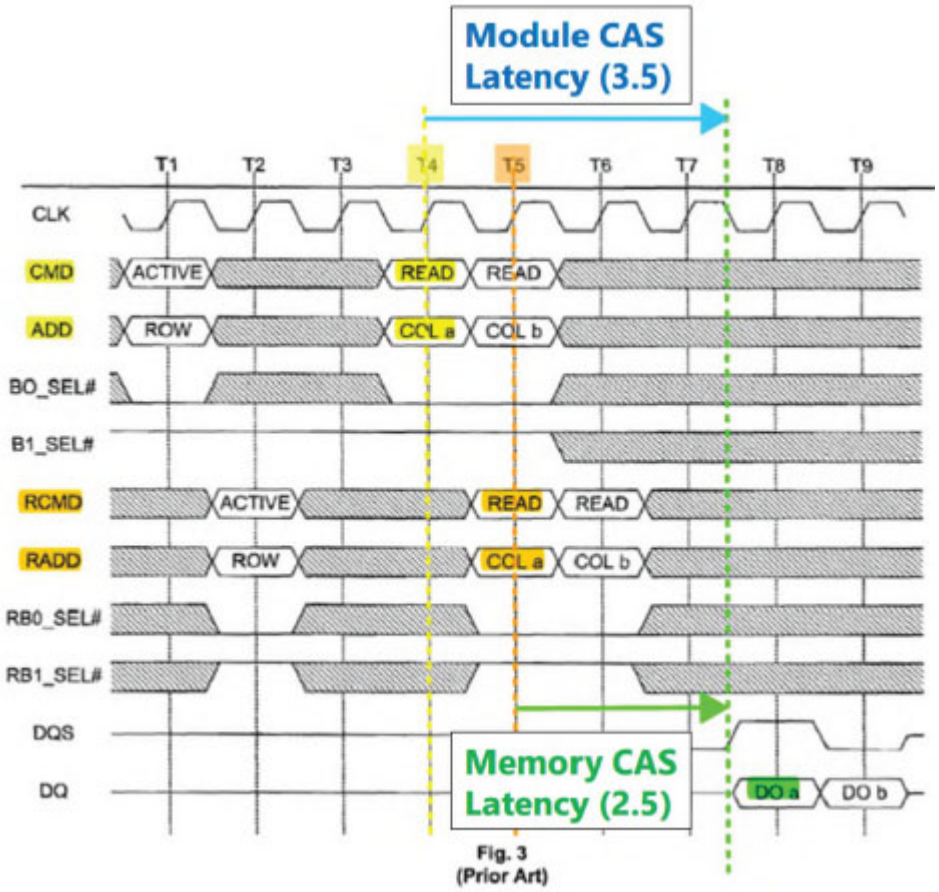
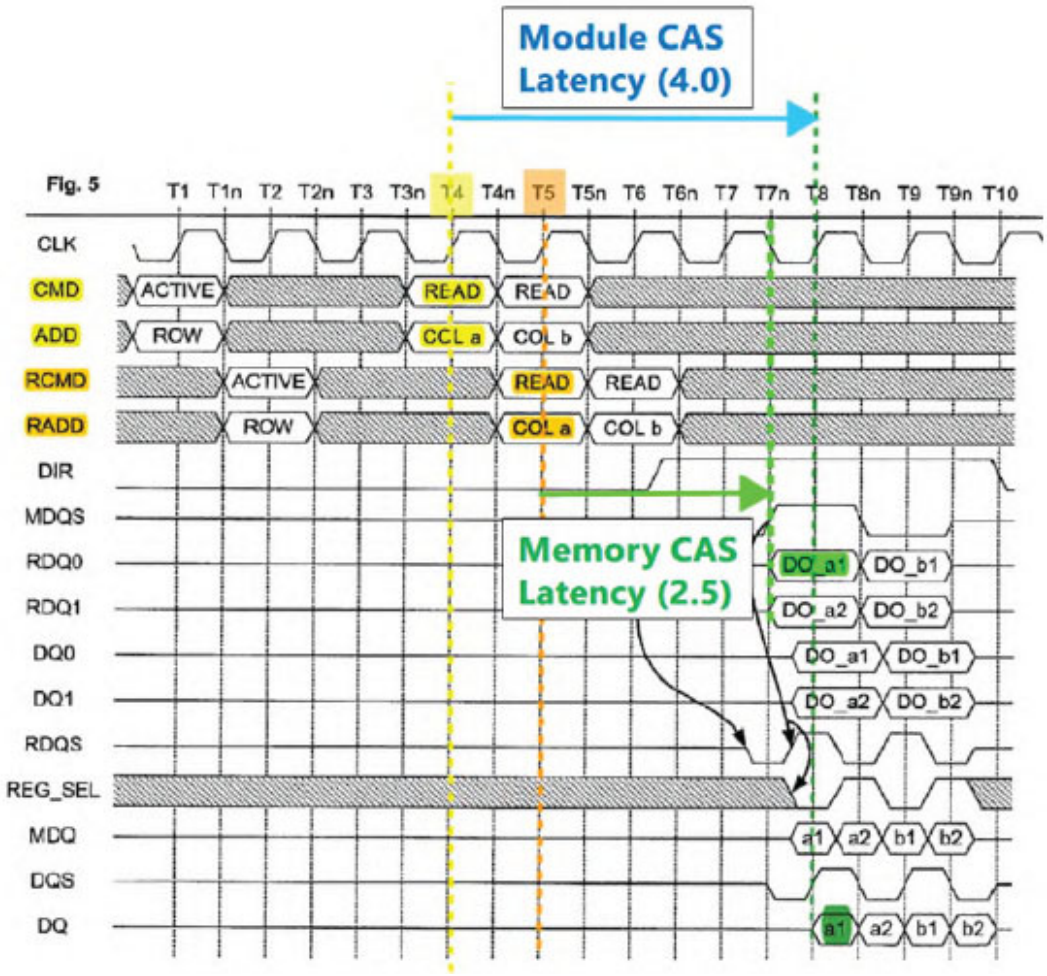



Fig. 3
(Prior Art)




### 5. Claim 2

Ground 3 further renders obvious claim 2 (pp.97-97), concerning "*isolat[ing] the loads of the memory devices from the memory bus*." EX1003, ¶384; EX1078, 3:67-4:2, 4:18-26 ("The…modules…isolate[e] the memory devices…from the bus").

## VIII. SECONDARY CONSIDERATIONS

As discussed above (pp.10-15), the 417 Patent discloses and claims "rank multiplication" as the solution to expensive, high-density memory devices. But others also immediately recognized and solved the same problem. As shown

above, the 417 Patent is remarkably similar to Ellsberry (EX1073), and both were filed within one month of each other. Amidi (EX1079) and Perego (EX1071) also recognized and solved the same problem in the 18 months before the 417 Patent, as discussed above. Such "simultaneous invention" is a secondary consideration of obviousness. EX1003, ¶¶468-469; EX1023, pp.39-40. Indeed, hundreds of claims from this family of patents — all directed to "rank multiplication" — have been found invalid, providing ample evidence of widespread "simultaneous invention" of the subject matter and claims of the 417 Patent. *Id*. ¶¶89-95, 99, 167 (citing EX1012-EX1017, EX1026-EX1043, EX1046-EX1049).

## IX. OTHER CONSIDERATIONS

### A. §325(d)

*Advanced Bionics* and §325(d) do not support discretionary denial because the Examiner did not consider the Grounds discussed above. Although Ellsberry, Halbert, and family members of Perego were disclosed by Netlist during prosecution, they were buried in an IDS with nearly 900 other references, and there is no evidence that the Examiner substantively considered those references either alone or as part of the Grounds presented here. EX1002, pp.171-217, 240-86, 315¬19. Denial under §325(d) is thus unwarranted. *E.g.*, *HTC Corp. v. Motiva Patents, LLC*, IPR2019-01666, Paper 9 at 6-10 (PTAB Apr. 3, 2020). Denial is also unwarranted because to the extent the Examiner considered Ellsberry, Halbert,

or the family members of Perego, the Examiner materially erred for the reasons explained above. Indeed, the Board has instituted *inter partes* reviews against family members of the 417 Patent based on grounds applying Perego and Ellsberry (*see* EX1023) and Halbert's publication (*see* EX1030, EX1056).

### B. *Fintiv*

The *Fintiv* factors and the Interim *Fintiv* Guidance (EX1091) favor institution. The Board should not exercise its discretion because, as shown above, the merits of this petition are compelling. EX1091, pp.4-5. Furthermore, Samsung Electronics Co., Ltd. ("Samsung") filed a petition against the 417 Patent (IPR2023-00454 ("Samsung IPR")) within five months of Netlist's complaint asserting the 417 Patent against Samsung and Petitioners in the Eastern District of Texas. EX1085; EX1088. Petitioners have filed this copycat petition and a motion for joinder to the Samsung IPR within the one-year statutory bar. Both Netlist's litigations are still in their early stages, with the Claim Construction hearing scheduled for October 5, 2023—almost three months after an Institution Decision will have issued in the Samsung IPR. Thus, the *Fintiv* factors favor institution. EX1091, pp.3, 8-9; EX1092, p.35 (showing a median 24.2-month time-to-trial); *Samsung Elecs. Co. v. Staton Techiya*, LLC, IPR2022-00324, Paper 13, at 12 (PTAB July 11, 2022) (applying the median). Moreover, should the Board grant institution of the Samsung IPR, the Board should not discretionarily deny

institution of this petition because it will have been determined that the unpatentability challenge presented in this petition is compelling. EX1091, pp.4-5.

### C. Discretionary Denial Under *General Plastic* Is Unwarranted

*General Plastic* does not support denying institution. This petition will not tax the Board's resources or ability to meet the statutory deadline for a final determination because Petitioners filed this petition and motion for joinder timely, advancing the same grounds and relying upon the same evidence and expert declaration as the Samsung IPR; Petitioners agree to be subject to the Samsung IPR schedule and take an understudy role only.

## X. CONCLUSION

Petitioners therefore respectfully request that Trial be instituted and that claims 1-15 be canceled as unpatentable.

Dated: July 28, 2023

/ *Juan C. Yaquian* /
Juan C. Yaquian
Reg. No. 70,755
Winston & Strawn LLP
800 Capital Street, Suite 2400
Houston, TX 77002
JYaquian@winston.com
T: (713) 651-2600
F: (713) 651-2700

*Lead Counsel for Petitioners*

## CERTIFICATE OF COMPLIANCE

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. § 42.24 because it contains 13,998 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. § 42.24.

Dated: July 28, 2023

*/ Juan C. Yaquian /*
Juan C. Yaquian
Reg. No. 70,755
Winston & Strawn LLP
800 Capital Street, Suite 2400
Houston, TX 77002
JYaquian@winston.com
T: (713) 651-2600
F: (713) 651-2700

*Lead Counsel for Petitioners*

## CERTIFICATE OF SERVICE

I hereby certify that on this 28th day of July, 2023, a copy of this Petition, including all exhibits, has been served in its entirety by FedEx Express on the following counsel of record for Patent Owner:

Jamie J. Zheng, Ph.D., Esq.
USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94306-3314

A courtesy copy was also served upon litigation counsel for Patent Owner via email, as follows:

Samuel F. Baxter (sbaxter@mckoolsmith.com)
Jennifer L. Truelove (jtruelove@mckoolsmith.com)
MCKOOL SMITH, P.C.

Jason Sheasby (jsheasby@irell.com)
Annita Zhong (hzhong@irell.com)
IRELL & MANELLA LLP

Dated: July 28, 2023

*/ Juan C. Yaquian /*
Juan C. Yaquian
Reg. No. 70,755
Winston & Strawn LLP
800 Capital Street, Suite 2400
Houston, TX 77002
JYaquian@winston.com
T: (713) 651-2600
F: (713) 651-2700

*Lead Counsel for Petitioners*