UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

Case IPR2023-00455
Patent 9,858,215

DECLARATION OF DR. ANDREW WOLFE
REGARDING U.S. PATENT NO. 9,858,215

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I. INTRODUCTION

A. Engagement

1. I have been retained by counsel for Samsung Electronics Co., Ltd. ("Samsung") as an expert witness in the above-captioned proceeding. I have been asked to provide my opinion about the state of the art of the technology described in U.S. Patent No. 9,858,215 ("the 215 Patent") (EX1001) and on the patentability of the claims of this patent. The following is my written declaration on these topics.

B. Background and Qualifications

2. My professional qualifications, experience, publications and presentations, and a listing of previous cases in which I have provided expert testimony are set forth in my CV, attached as Exhibit 1004.

3. I am the founder and sole employee of Wolfe Consulting. Through Wolfe Consulting, I provide technical and business analytics to businesses on processor technology, computer systems, consumer electronics, software, design tools, data security, cryptography and intellectual property issues. I have more than thirty years' experience developing products, researching, consulting, and teaching in those fields. In that time, I have worked as a computer architect, computer system designer, and as an executive in the PC and electronics business. I have also taught at some of the world's leading institutions in those fields,

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including Stanford University, Princeton University, Carnegie Mellon University, and Santa Clara University.

4. In 1985, I earned the B.S.E.E. degree in Electrical Engineering and Computer Science from the Johns Hopkins University. In 1987, I received the M.S. degree in Electrical and Computer Engineering from Carnegie Mellon University and in 1992, I received the Ph.D. degree in Computer Engineering from Carnegie Mellon University. My doctoral dissertation proposed a new approach for the architecture of a computer processor.

5. I have more than 35 years of experience as a computer architect, computer system designer, personal computer graphics designer, educator, and executive in the electronics industry.

6. In 1983, I began designing touch sensors, microprocessor-based computer systems, and I/O (input/output) cards for personal computers as a senior design engineer for Touch Technology, Inc. During the course of my design projects with Touch Technology, I designed I/O cards for PC-compatible computer systems, including the IBM PC-AT, to interface with interactive touch-based computer terminals that I designed for use in public information systems. I continued designing and developing related technology as a consultant to the Carroll Touch division of AMP, Inc., where in 1986 I designed one of the first custom touch-screen integrated circuits. I designed the touch/pen input system for

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the Linus WriteTop, which many believe to be the first commercial tablet computer.

7. From 1986 through 1987, I designed and built a high-performance computer system as a student at Carnegie Mellon University. From 1986 through early 1988, I also developed the curriculum, and supervised the teaching laboratory, for processor design courses.

8. In the latter part of 1989, I worked as a senior design engineer for ESL-TRW Advanced Technology Division. While at ESL-TRW, I designed and built a bus interface and memory controller for a workstation-based computer system, and also worked on the design of a multiprocessor system.

9. At the end of 1989, I (along with some partners) reacquired the rights to the technology I had developed at Touch Technology and at AMP, and founded The Graphics Technology Company. Over the next seven years, as an officer and a consultant for The Graphics Technology Company, I managed the company's engineering development activities and personally developed dozens of touch screen sensors, controllers, and interactive touch-based computer systems.

10. I have consulted, formally and informally, for a number of fabless semiconductor companies. In particular, I have served on the technology advisory boards for two processor design companies: BOPS, Inc., where I chaired the board, and Siroyan Ltd., where I served in a similar role for three networking chip

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companies — Intellon, Inc., Comsilica, Inc., and Entridia, Inc. — and one 3D game accelerator company, Ageria, Inc.

11. I have also served as a technology advisor to Motorola and to several venture capital funds in the United States and Europe. Currently, I am a director at Turtle Beach Corporation, providing guidance in its development of premium audio peripheral devices for a variety of commercial electronic products.

12. From 1991 through 1997, I served on the Faculty of Princeton University as an Assistant Professor of Electrical Engineering. At Princeton, I taught undergraduate and graduate-level courses in Computer Architecture, Advanced Computer Architecture, Display Technology, and Microprocessor Systems, and conducted sponsored research in the area of computer systems and related topics. From 1999 through 2002, I taught a Computer Architecture course to both undergraduate and graduate students at Stanford University multiple times as a Consulting Professor. At Princeton, I received several teaching awards, both from students and from the School of Engineering. I have also taught advanced microprocessor architecture to industry professionals in IEEE- and ACM-sponsored seminars. I am currently a lecturer at Santa Clara University teaching courses on Microprocessor Systems, Advanced Logic Design, Real-Time Computing, and Mechatronics. I teach about memory — including DDR (Double Data Rate) SDRAM (Synchronous Dynamic Random Access Memory) and flash

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memory — in several of my classes, and I rely on the standards published by JEDEC.[8]

13. From 1997 through 2002, I held a variety of executive positions at a publicly held fabless semiconductor company originally called S3, Inc. and later called Sonicblue Inc. I held the positions of Chief Technology Officer, Vice President of System Integration Products, Senior Vice President of Business Development, and Director of Technology, among others.

14. In the roles listed above, I worked with and managed architecture and design teams responsible for the development of SRAM (Static Random-Access Memory) and DRAM (Dynamic Random-Access Memory) memories, graphics chip memory controllers, and CPU memory controllers. I also worked with memory vendors and memory standards bodies, directly and through my staff, on the development of memory technology and standards. I have been involved with interpreting and understanding JEDEC memory standards since at least 1997. For many years, I had a direct-report staff member who would attend JEDEC meetings and bring me both proposed and final standards for review and comment. I also

[8] JEDEC standards have been adopted worldwide and are widely adhered to by those in the business of creating memory devices and modules. *See infra* ¶¶143-145, 169-170.

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have used proposed and final JEDEC standards for chips, modules, and protocols to guide product decisions and to facilitate technical discussions with corporate partners and with consulting clients. I supervised design teams that implemented memory controllers for successful commercial products that interoperated with JEDEC-compliant DDR memory chips and memory modules.

15. My teams also developed the Rio MP3 players and a music delivery platform and webstore backend service for selling music. In 1999, this music delivery system was spun out as a separate company called RioPort.com. I served on the RioPort.com board of directors and became involved in its product and technology strategy. I also managed engineering and marketing for the Rio product line for a period of time as an interim general manager. The Rio MP3 players were among the first consumer products to incorporate large quantities of NAND flash memory. I worked with CEOs and general managers at several leading flash memory suppliers on strategic planning for the flash market. I also worked with my engineering teams to evaluate and implement flash memory protocols and select flash memory form factors. During my time at SonicBlue we launched more than 30 new consumer electronics products.

16. I served as a board member and technical advisor at KBGear Inc. from 1999-2001. KBGear Inc. designed and produced digital cameras and music players.

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17. I have published more than fifty peer-reviewed papers in computer architecture and computer systems and IC (integrated circuit) design. My CV, attached as Exhibit 1004, lists all publications that I have authored in the previous 10 years.

18. I have also chaired IEEE and ACM conferences in microarchitecture and IC design and served as an associate editor for IEEE and ACM journals. I served on the IEEE Computer Society Awards committee. I am an IEEE Fellow and a Member of ACM. I am a named inventor on at least fifty-seven U.S. patents and thirty-seven foreign patents.

19. I have been the invited keynote speaker at the ACM/IEEE International Symposium on Microarchitecture and at the International Conference on Multimedia. I have also been an invited speaker on various aspects of technology or the PC industry at numerous industry events including the Intel Developer's Forum, Microsoft Windows Hardware Engineering Conference, Microprocessor Forum, Embedded Systems Conference, Comdex, and Consumer Electronics Show as well as at the Harvard Business School and the University of Illinois Law School. I have been interviewed on subjects related to technology and the electronics industry by publications such as the Wall Street Journal, New York Times, LA Times, Time, Newsweek, Forbes, and Fortune as well as CNN, NPR, and the BBC. I have also spoken at dozens of universities including MIT,

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Stanford, University of Texas, Carnegie Mellon, UCLA, University of Michigan, Rice University, and Duke University.

C. Compensation and Prior Testimony

20. I am being compensated at a rate of $600.00 per hour for my study and testimony in this matter. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

21. My CV, attached as Exhibit 1004, lists all other cases in which, during the previous 4 years, I have testified as an expert at trial or by deposition.

D. Information Considered

22. My opinions are based on my years of education, research and experience, as well as my investigation and study of relevant materials. In forming my opinions, I have considered the materials I identify in this declaration and those listed in the Exhibit List at the end of this declaration.

23. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional documents and information in forming any necessary opinions — including documents that may not yet have been provided to me.

24. My analysis of the materials produced in this matter is ongoing and I will continue to review any new materials as it is provided. This declaration represents only those opinions I have formed to date.

II. LEGAL STANDARDS FOR PATENTABILITY

25. In expressing my opinions and considering the subject matter of the claims of the 215 Patent, I am relying upon certain basic legal principles that have been explained to me.

26. First, I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious in view of what was known before the invention was made.

27. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as "prior art" and generally includes patents and printed publications (e.g., books, journal publications, articles on websites, product manuals, etc.).

28. I understand that in this proceeding the Petitioner has the burden of proving that the claims of the 215 Patent are anticipated by or obvious in view of the prior art by a preponderance of the evidence. I understand that "a preponderance of the evidence" is evidence sufficient to show that a fact is more likely true than it is not.

29. I understand that in this proceeding the claims should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. The claims after being construed in this manner are then to be compared to the information in the prior art.

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30. I understand that in this proceeding the information that may be evaluated is limited to patents and printed publications. My analysis below compares the claims to patents and printed publications that are prior art to the claims.

31. I understand that there are two ways in which prior art may render a patent claim unpatentable. First, the prior art can be shown to "anticipate" the claim. Second, the prior art can be shown to have made the claim "obvious" to a person of ordinary skill in the art. In this declaration I focus on "obviousness." My understanding of the legal standard for "obviousness" is set forth below.

32. I understand that a claimed invention is not patentable if it would have been obvious to a person of ordinary skill in the field of the invention at the time the invention was made.

33. I understand that the obviousness standard is defined in the patent statute (35 U.S.C. § 103(a)) as follows:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

34. I understand that the following standards govern the determination of whether a claim in a patent is obvious. I have applied these standards in my

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evaluation of whether the claims of the 215 Patent would have been considered obvious as of the priority date of the patent.

35. I understand that to find a claim in a patent obvious, one must make certain findings regarding the claimed invention and the prior art. Specifically, I understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non-obviousness may be present in any particular case.

36. In addition, I understand that the obviousness inquiry should not be done in hindsight, but must be done using the perspective of a person of ordinary skill in the relevant art as of the effective filing date of the patent claim.

37. I understand the objective factors indicating obviousness or non-obviousness may include the following: (1) commercial success of products covered by the patent claims; (2) a long-felt need for the invention; (3) failed attempts by others to make the invention; (4) copying of the invention by others in the field; (5) unexpected results achieved by the invention; (6) praise of the invention by those in the field; (7) the taking of licenses under the patent by others; (8) expressions of surprise by experts and those skilled in the art at the making of

the invention; and (9) the patentee proceeded contrary to the accepted wisdom of the prior art. I also understand that any of this evidence must be specifically connected to the invention rather than being associated with the prior art or with marketing or other efforts to promote an invention. I am not presently aware of any evidence of "objective factors" suggesting the claims are not obvious, and I reserve my right to address any such evidence if it is identified in the future.

38. I understand the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand that an example of a solution in one field of endeavor may make that solution obvious in another related field. I also understand that market demands or design considerations may prompt variations of a prior art system or process, either in the same field or a different one, and that these variations will ordinarily be considered obvious variations of what has been described in the prior art.

39. I also understand that if a person of ordinary skill can implement a predictable variation, that variation would have been considered obvious. I understand that for similar reasons, if a technique has been used to improve one device, and a Skilled Artisan would recognize that it would improve similar devices in the same way, using that technique to improve the other device would

have been obvious unless its actual application yields unexpected results or challenges in implementation.

40. I understand that the obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, but instead can take account of the "ordinary innovation" and experimentation that does no more than yield predictable results, which are inferences and creative steps that a Skilled Artisan would employ.

41. I understand that sometimes it will be necessary to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art. I understand that all these issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

42. I understand that the obviousness analysis cannot be confined by a formalistic conception of the words "teaching, suggestion, and motivation." I understand that in 2007, the Supreme Court issued its decision in *KSR Int'l Co. v. Teleflex, Inc.,* 550 U.S. 398 (2007), where the Court rejected the previous requirement of a "teaching, suggestion, or motivation to combine" known elements of prior art for purposes of an obviousness analysis as a precondition for finding obviousness. It is my understanding that *KSR* confirms that any motivation that

would have been known to a person of skill in the art, including common sense, or any motivation derived from the nature of the problem to be solved, is sufficient to explain why references would have been combined.

43. I understand that a person of ordinary skill in the art attempting to solve a problem will not be led only to those elements of prior art designed to solve the same problem. I understand that under the *KSR* standard, steps suggested by common sense are important and should be considered. Common sense teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. As such, the prior art considered can be directed to any need or problem known in the field of endeavor as of the priority date of the patent and can provide a reason for combining the elements of the prior art in the manner claimed. In other words, the prior art does not need to be directed towards solving the same problem that is addressed in the patent. Further, the individual prior art references themselves need not all be directed towards solving the same problem.

44. I understand that obviousness does not require that the features of a secondary reference be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of those references would have suggested to a Skilled Artisan. The disclosures of the prior art

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references need not be physically combinable. Combining the teachings of the references should be the focus of the analysis.

45. I understand that an invention that might be considered an obvious variation or modification of the prior art may be considered non-obvious if one or more prior art references discourages or lead away from the line of inquiry disclosed in the reference(s). A reference does not "teach away" from an invention simply because the reference suggests that another embodiment of the invention is better or preferred. My understanding of the doctrine of teaching away requires a clear indication that the combination should not be attempted (*e.g.*, because it would not work or explicit statements saying the combination should not be made).

46. I understand that a person of ordinary skill is also a person of ordinary creativity.

47. I further understand that in many fields, there may be little discussion of obvious techniques or combination, and it often may be the case that market demand, rather than scientific literature or knowledge, will drive design trends. When there is such a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within their technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was

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obvious to try might show that it was obvious. The fact that a particular combination of prior art elements was "obvious to try" may indicate that the combination was obvious even if no one attempted the combination. If the combination was obvious to try (regardless of whether it was actually tried) or leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than innovation.

III. THE 215 PATENT

A. Person of Ordinary Skill in the Art ("Skilled Artisan")

48. The 215 Patent identifies the relevant field of art as follows: "The present invention relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules." EX1001 at 1:40-45. Based on that description of the field of art, my experience, and the information I have reviewed for purposes of this proceeding, I believe a person of ordinary skill in the art in the field of the 215 Patent in 2004 or 2005 ("Skilled Artisan" or "POSITA") would have been someone with an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Additional training can substitute for educational or research experience, and vice versa. Such a hypothetical person would have been familiar with various standards

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of the day including the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with the memory controller of a computer system. Specifically, he or she would have been knowledgeable about the JEDEC DDR and DDR2 SDRAM standards used to standardize the functioning of memory devices, and the JEDEC 21-C standard used to standardize different possibilities for the physical layout of memory devices on a module as well as different possibilities for density and organization of the memory devices to achieve a given memory capacity. He or she would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs (Application-Specific Integrated Circuits) and CPLDs (Complex Programmable Logic Devices) and more low-level circuits such as tri-state buffers, flip flops and registers.

49. I have attached as exhibits some of the JEDEC standards that in my opinion a Skilled Artisan would have been familiar with as discussed above, including:

- DDR SDRAM standard (JESD79). *See* EX1060.
- DDR2 SDRAM standard (JESD79-2). *See* EX1064.
- JEDEC 21-C design specification (JESD21-C) for DDR RDIMM memory modules. *See* EX1062.

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- JEDEC 21-C design specification for DDR2 RDIMM. *See* EX1066.

50. JEDEC's standards were and still are widely known and adhered to by those in the business of creating memory devices and modules. In fact, the 215 Patent incorporates by reference one of the JEDEC standards to illustrate possible configurations of memory devices, and refers (for example) to standardized DDR2 memories and RDIMM memory modules. EX1001 at 5:63-6:11, 21:7-22:7, 34:26-33.

B. Effective Filing Date of the 215 Patent: No Earlier Than July 1, 2005

51. The application that resulted in the 215 Patent (EX1001) is U.S. Patent Application Serial No. 14/715,486, filed May 18, 2015. *See* EX1002. The 215 Patent resulted from:

- a continuation application of U.S. Patent Application No. 13/971,231, now U.S. Patent No. 9,037,774 ("774 Patent") (EX1053), filed August 20,2013, which is
- a continuation of U.S. Patent Application No. 13/287,081, now U.S. Patent No. 8,516,188 ("188 Patent") (EX1051), filed November 1, 2011, which is
- a continuation of U.S. Patent Application No. 13/032,470, now U.S. Patent No. 8,081,536 ("536 Patent") (EX1046), filed February 22, 2011, which is

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- a continuation of U.S. Patent Application No. 12/955,711, now U.S. Patent No. 7,916,574 ("574 Patent") (EX1045), filed on November 29, 2010, which is
- a continuation of U.S. Patent Application No. 12/629,827, now U.S. Patent No. 7,881,150 ("150 Patent") (EX1039), filed on December 2, 2009, which is
- a continuation of U.S. Patent Application No. 12/408,652, now U.S. Patent No. 7,636,274 ("274 Patent) (EX1036), filed on March 20, 2009, which is
- a continuation of U.S. Patent Application No. 11/335,875, now U.S. Patent No. 7,532,537 ("537 Patent") (EX1032), filed January 19, 2006, which is
- a continuation-***in-part*** of U.S. Patent Application No. 11/173,175, now U.S. Patent No. 7,289,386 ("386 Patent") (EX1012), filed July 1, 2005, which is
- a continuation-***in-part*** of U.S. Patent Application No. 11/075,395 ("395 Application"), now U.S. Patent No. 7,286,436 ("436 Patent") (EX1011), filed March 7, 2005, which claims priority to
- U.S. Provisional Application No. 60/645,087 ("087 Provisional Application" or "087 Provisional") (EX1005), filed January 19, 2005,

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- U.S. Provisional Application No. 60/588,244 ("244 Provisional Application" or "244 Provisional") (EX1006), filed July 15, 2004,
- U.S. Provisional Application No. 60/550,668 ("668 Provisional Application" or "668 Provisional") (EX1007), filed March 5, 2004,
- U.S. Provisional Application No. 60/575,595 ("595 Provisional Application" or "595 Provisional") (EX1008), filed May 28, 2004, and
- U.S. Provisional Application No. 60/590,038 ("038 Provisional Application" or "038 Provisional") (EX1009), filed July 21, 2004.

See EX1001 (215 Patent) at (63) and (60).

52. In my opinion, as explained below, the effective filing date for the claims of the 215 Patent is no earlier than July 1, 2005, which is the filing date of the 386 Patent (EX1012).

53. I understand that, in order for a claim of the 215 Patent to be entitled to the benefit of the filing date of an earlier application, the disclosure of that application must include, among other things, "a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same." 35 U.S.C. § 112, ¶ 1. I further understand that a continuation-in-part application is an

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application filed during the lifetime of an earlier nonprovisional application, repeating some substantial portion or all of the earlier nonprovisional application, and adding matter not disclosed in the earlier nonprovisional application (or applications).

54. As discussed below, three of the five prior art references I have considered (Perego, Halbert, and Matsui2) were filed before the earliest provisional application for the 215 Patent, which was filed on March 5, 2004, and a fourth reference (JESD79-2) was publicly available before this date. Thus, it is my understanding that those four references are prior art to the claims of the 215 Patent. However, another reference I have considered (Ellsberry) was filed June 1, 2005. Thus, it is my understanding that the Ellsberry reference would be prior art to a given claim of the 215 Patent if no application filed before June 1, 2005, to which the 215 Patent claims priority provided an enabling written description for the full scope of that claim.

55. For the reasons discussed below, it is my opinion that the claims of the 215 Patent (EX1001) are not entitled to a priority date before the July 1, 2005, continuation-in-part application that resulted in the 386 Patent (EX1012). Therefore, it is my opinion that Ellsberry (EX1073) is also prior art to the claims of the 215 Patent. In any event, the references in Grounds 1, 3, and 4 that I have considered (Perego in combination with JESD79-2, in further combination with

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Halbert, and Matsui2, respectively) were prior art even before March 5, 2004. Accordingly, my analysis for those Grounds does not depend on which priority date applies to the claims of the 215 Patent.

56. As discussed above, the 215 Patent is a continuation of the 537 Patent through a series of applications, and the 537 Patent is a continuation-in-part of the 386 Patent, filed on July 1, 2005, which itself is a continuation-in-part of the 436 Patent. The 215 Patent also claims priority to five provisional applications filed before July of 2005. I have been asked to give my opinion as to whether, from the perspective of a Skilled Artisan, the applications before the 386 Patent show that the inventors actually invented what is claimed in each of the claims of the 215 Patent, and possessed the claimed subject matter, prior to July 1, 2005, the filing date of the 386 Patent. I have considered that question on a claim-by-claim basis and analyzed whether the application for the 436 Patent and the provisional applications explicitly or inherently disclose all of the elements of the respective claim. To determine whether the application for the 436 Patent and the provisional applications inherently disclose an element, I considered whether a Skilled Artisan would have understood that any element not explicitly disclosed is, nevertheless, necessarily present and thus inherent. I understand that an element is not necessarily present if, in view of the disclosure, it is merely probable or possible that the element is present. I understand that the knowledge of a Skilled Artisan

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may be used to inform what is actually in the patent or application, but not to teach limitations that are not explicitly or inherently disclosed by the patent or application, even if those limitations would be rendered obvious by the disclosure in the patent or application.

57. I note that, in at least one other proceeding, the PTAB has found that the Patent Owner claimed subject matter in other patents in this family that was unsupported by the application for the 436 Patent and the provisional applications. *See* EX1023 (Institution Decision against U.S. Patent No. 7,619,912) at pp. 24–26; *see also infra* ¶90.

58. Each of the two independent claims 1 and 21 of the 215 Patent, and thus all dependent claims, requires responding to a first memory command by "providing first control signals to the ***buffer*** to enable communication of the first data burst between the at least one first memory integrated circuit [in the first rank] and the memory controller through the ***buffer***," and responding to a second memory command by "providing second control signals to the ***buffer*** to enable communication of the second data burst between the at least one second memory integrated circuit [in the second rank] and the memory controller through the ***buffer***, the second control signals being different from the first control signals." EX1001 at independent claims 1 and 21. Netlist added these limitations by amendment to replace parts of an earlier Examiner's amendment that put the

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claims "in condition for allowance" and required different first and second data paths for the first and second data bursts. EX1002 at 280 (Interview Summary), 284 (Examiner's Amendment to Claim 1), 389-91, 393 (Amendment in response to Notice of Allowance), 513 (showing application claim 11 issued as claim 21).

59. I have reviewed the application for the 436 Patent and found no disclosure of a buffer for enabling data bursts through the buffer. EX1010 at 4-46. In fact, the application for the 436 Patent lacks any buffers on the data lines. I have also reviewed the five provisional applications and found that four of them also lack any buffers for data signals, similar to the application for the 436 Patent. EX1006-1009. Thus, a Skilled Artisan would have understood that neither the application for the 436 Patent nor those four Provisional applications support the "control signal" limitations for the claimed "buffer."

60. Out of the priority applications, only the 087 Provisional discloses any "buffer" (Rank Buffer DIMM Logic, RBDL, below) through which data is communicated. EX1005 at Fig. 1 (reproduced below showing DQ/DQS data/strobe lines coupled to a block labeled RBDL).

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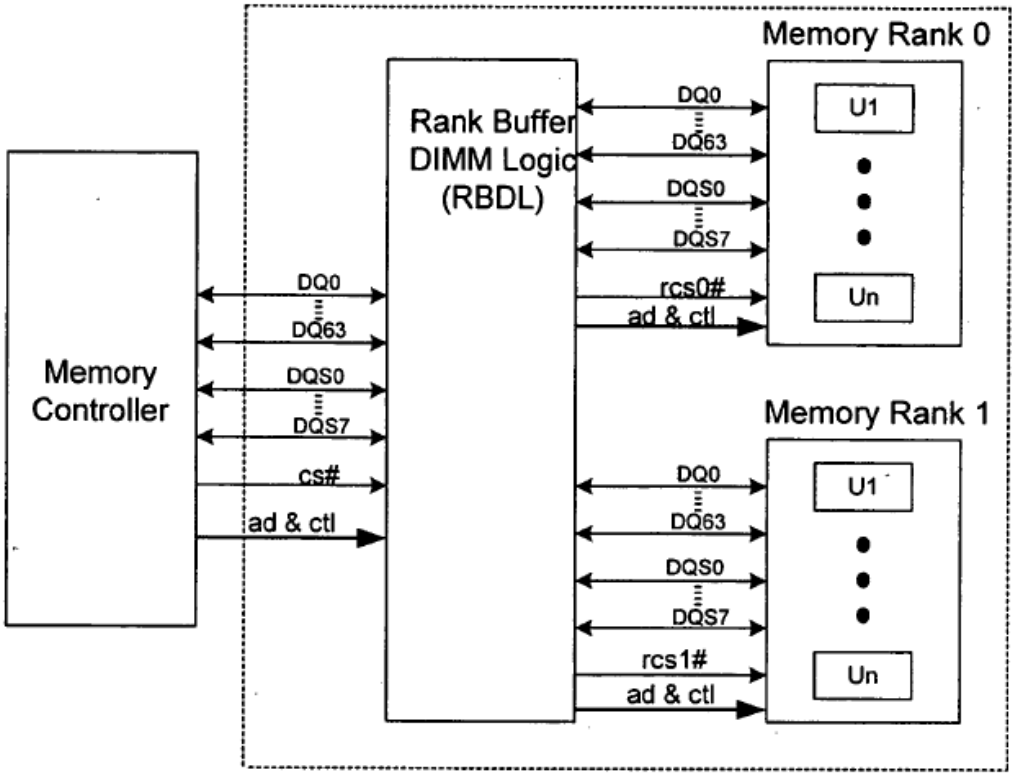
FIGURE 1:



Block Diagram: Rank Buffered DIMM Memory Sub-system

61. The 087 Provisional, however, still lacks any disclosure of the different first and second control signals for enabling the communication of data bursts through the buffer in response to memory commands as required by the claims. In fact, the 087 Provisional does not even mention any "data burst" or "control signals," much less any specific control signals to enable these data bursts through the buffer in any particular way in response to memory commands.

62. For example, the 087 Provisional discloses "a data path multiplexer/demultiplexer" which provides separate DQ/DQS paths for each rank (essentially as shown for the RBDL block in Fig. 1, reproduced above), but it is

silent about how that multiplexer/demultiplexer operates specifically for enabling data bursts through the data buffer in response to memory commands, what are its control signals, and how those control signals differ for the "first" and "second" memory commands. EX1005 at [0005], [0008], [0017].

63. A Skilled Artisan would have also understood that it was not necessary for the buffer to use different first and second control signals even if the first and second memory commands are directed to different ranks. For example, the 087 Provisional describes that a "transition bit … selects which rank of memory devices is enabled for a read or write operation." EX1005 at [0012] (pp.5-6). A Skilled Artisan would have understood that one out of multiple ranks can be enabled for, say, a write operation by chip select signals. EX1064 at p. 6 (explaining that "Chip Select … provides for external Rank Selection on systems with multiple Ranks"). Thus, even if the Rank Buffer DIMM Logic (RBDL) sends data from the memory controller to both Memory Rank 0 and Memory Rank 1 shown in Fig. 1 of the 087 Provisional, the ranks' respective chip select signals rcs0# and rcs1# can select the rank which is enabled for the write operation. EX1005 at Fig. 1 (reproduced above). In such a case, the data from the memory controller would go through the RBDL block to both Rank 0 and Rank 1 independent of the "transition bit" and independent of which rank was selected for the write operation. The 087 Provisional has no description of using different

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"first" and "second" control signals for enabling data transactions through the buffer.

64. Similarly, the 087 Provisional discloses that the buffer can include "combinatorial logic, registers, and logical pipelines" but is silent about how those elements are related to the control of enabling data bursts through the buffer in response to memory commands as claimed. EX1005 at [0009].

65. A Skilled Artisan would have also understood that data transfer through the 087 Provisional's buffer does not necessarily happen in response to the memory commands as required by the 215 Patent claims. For example, a Skilled Artisan would have understood that, for DDR SDRAM devices, a data transfer is preceded by a "preamble" on the DQS strobe lines, and the data transfer through the buffer can be controlled in response to such preambles. *See, e.g.*, EX1064 at pp. 26 (Fig. 23 showing preamble time t_{RPRE} for read operations), 30 (Fig. 29 showing preamble time t_{WPRE} for write operations), and 65 (timing parameters for read and write preambles). The 087 Provisional has no description of using different "first" and "second" control signals for enabling data transactions through the buffer in response to memory commands.

66. In short, I have not seen any disclosure in the 087 Provisional that would convey to a Skilled Artisan that the inventors of the 215 Patent actually invented what is claimed by these "control signals" limitations. To be clear, in my

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opinion a Skilled Artisan would have found obvious the claimed different "control signals" at the time as evidenced by the prior art discussed below. But as discussed above, none of the priority applications before the 386 Patent application filed July 1, 2005, has a disclosure that would convey to a Skilled Artisan that the claimed different control signals were necessarily present in a buffer for data signals.

67. Thus, a Skilled Artisan would have understood that the application for the 436 Patent and the five provisional applications before the 386 Patent filed July 1, 2005, failed to describe the limitations related to the different "first control signals" and "second control signals" in the claims of the 215 Patent.

C. Overview of the 215 Patent

68. The 215 Patent concerns "rank multiplication" (a prior-art technique discussed below, ¶¶171-174). The 215 Patent states that it "relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules." EX1001 (215 Patent) at 1:42-45. The 215 Patent discloses a memory module (10) that includes "a circuit 40 electrically coupled to the plurality of memory devices 30 and configured to be electrically coupled to the memory controller 20 of the computer system." *Id.* at 5:24-27, Fig. 1 (reproduced below).

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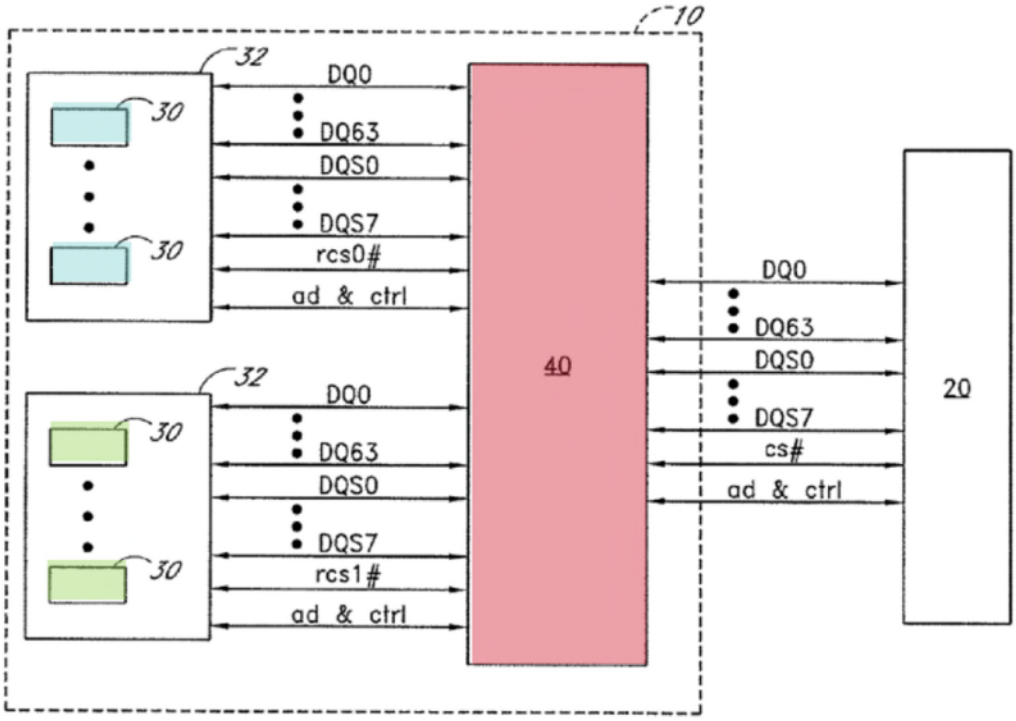

FIG. 1

69. The 215 Patent explains that "DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width," such as the module 10 in Figure 1 has two ranks (32), each having a bit width of 64 bits (DQ0-DQ63). EX1001 at 2:41-45, 6:30-34, 12:13-17, Fig. 1 (reproduced above). The 215 Patent further explains that "the ranks of a memory module are selected or activated by address and command signals," including "rank-select signals [(e.g., cs#)], also called chip-select signals." *Id.* at 2:59-63. Chip-select signals are standard signals in the JEDEC standards for DDR (sometimes called DDR-1) and DDR-2 memory devices, EX1060, p.7; EX1064,

p.6, which the 215 Patent specifically indicates are examples of memory devices compatible with the invention of the 215 Patent, EX1001 at 6:4-8; 21:7-10.

70. The 215 Patent purportedly improves the capacity of a memory module because the "circuit 40 selectively isolates one or more of the loads of the memory devices from the computer system…[and] comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module 10." EX1001 at 5:24-32 and Fig. 1 (reproduced above); *see also id.* at 9:17-64 ("the load isolation provided by the circuit 40 advantageously allows the memory module 10 to present a reduced load (e.g., electrical load, such as capacitive load, inductive load, or impedance load) to the computer system by selectively switching between the two ranks of memory devices 30 to which it is coupled … the load isolation advantageously diminishes the effects of capacitive loading, jitter and other sources of noise … load isolation advantageously increases the size of the memory array supported by the memory controller 20 of the computer system").

71. In particular, the 215 Patent's memory module appears to the computer system as if it had higher-density memory devices (a system memory domain), while the physical configuration of the module (a physical memory domain) is different from what the computer system sees. EX1001, 15:42-46 ("even though the memory module 10 actually has the first number of ranks of

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memory devices 30, the memory module 10 simulates a virtual memory module by operating as having the second number of ranks of memory devices 30"). In the examples shown in FIG. 1 (reproduced above), the memory controller (20) issues commands to a single "virtual" rank using a single chip select signal ("cs#"), while the module actually has two ranks (both labeled 32), each having its own chip select signals ("rcs0#" and "rcs1#").

72. The 215 Patent also teaches that signals from the two memory devices forming a single virtual memory device of higher capacity may collide "between back-to-back adjacent read commands which cross memory device boundaries," because the memory controller is not aware of those device boundaries. *Id*. at 12:5-24, FIG. 7. The 215 Patent teaches preventing such collisions by selectively connecting the system data bus to only one of the ranks that form the "virtual" higher density memory device. *Id*. at 12:37-43 ("collisions are avoided by a mechanism which electrically isolates the DQS data strobe signal lines 104a, 104b from one another").

73. The 215 Patent also discloses that, when the buffer circuit (40) registers the data transfers, an extra clock cycle of time is added to the natural CAS latency of the individual memory devices "which is equivalent to a registered DIMM" and "advantageously provides sufficient time budget to add a buffer which

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electrically isolates the ranks of memory devices 30 from the memory controller 20." *Id.* at 20:22-46.

D. The Prosecution History of the 215 Patent

74. The prosecution histories of the 215 Patent and the other patent applications in the family of the 215 Patent are discussed below, starting with the earliest filed application, the 668 Provisional Application.

1. Provisional Application No. 60/550,668 (Mar. 5, 2004)

75. The applicants filed Provisional Application No. 60/550,668 ("668 Provisional Application"), titled "Unbuffered Memory Module Using Shared DQS Pins," on March 5, 2004. EX1007 at p. 1. No inventors are named on this provisional application. *Id*. at p. 1. The three-page specification describes the application's embodiments as including "an unbuffered memory module [that] comprises a plurality of pairs of lower-density memory components, each pair connected together with shared DQS pins to simulate a higher density memory component." *Id*. at [0003]. FIGs. 1 and 2 are said to illustrate "the problem arising from tying together two signal pins." *Id*. at [0014]. FIGs. 3 and 4 illustrate current limiting resistors. *Id.* at [0016-0017].

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Figure 1:

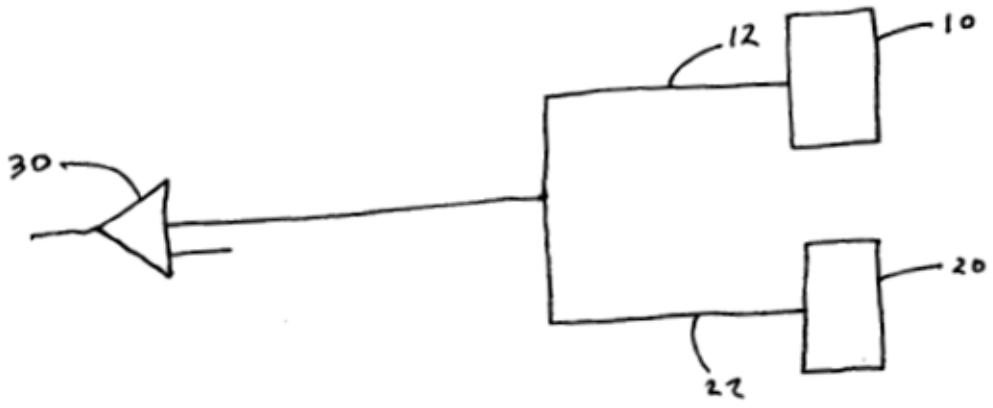
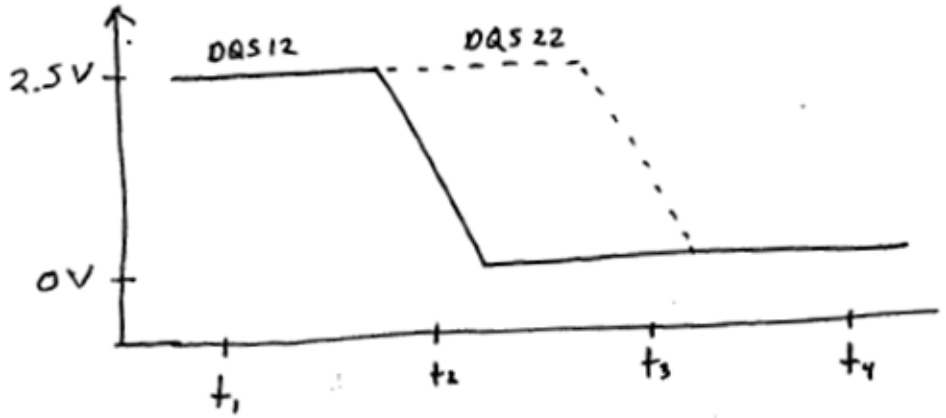


Figure 2:



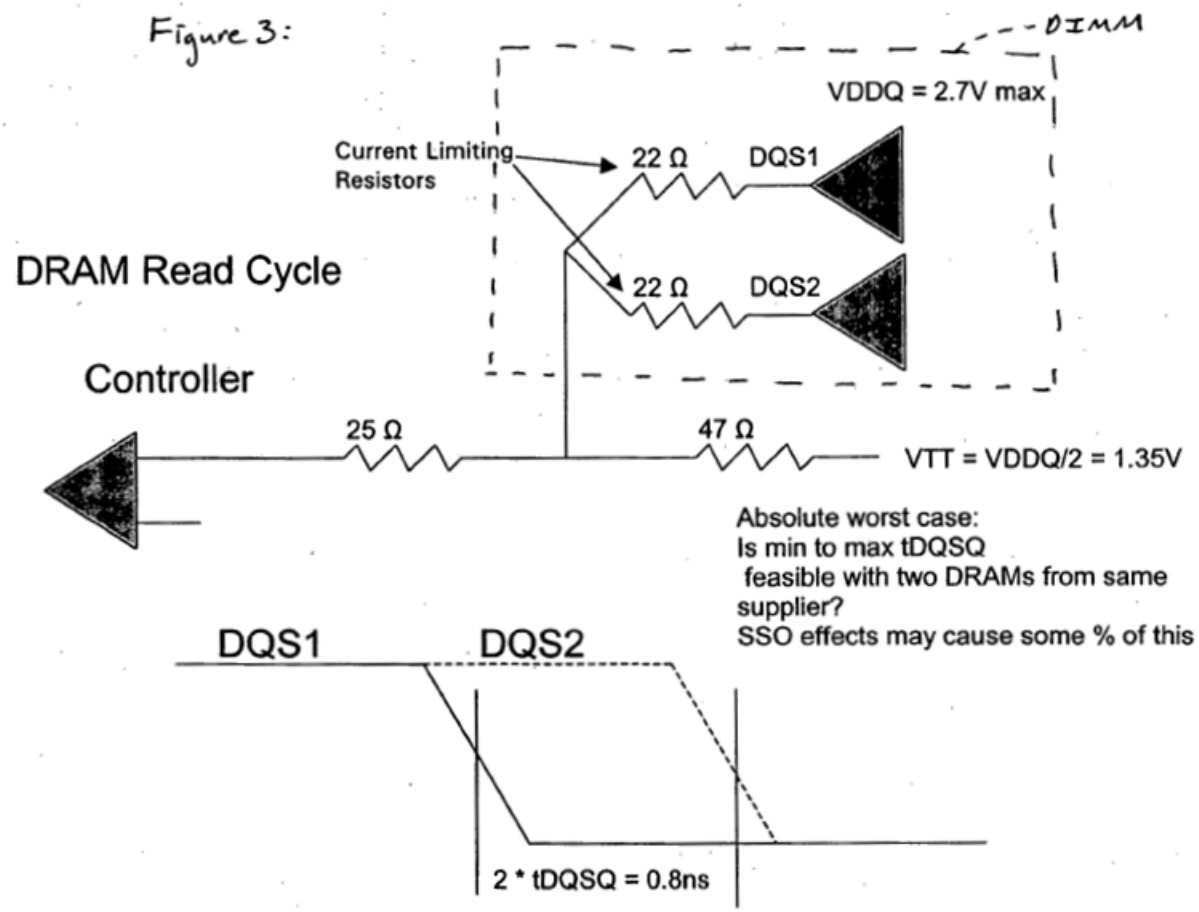
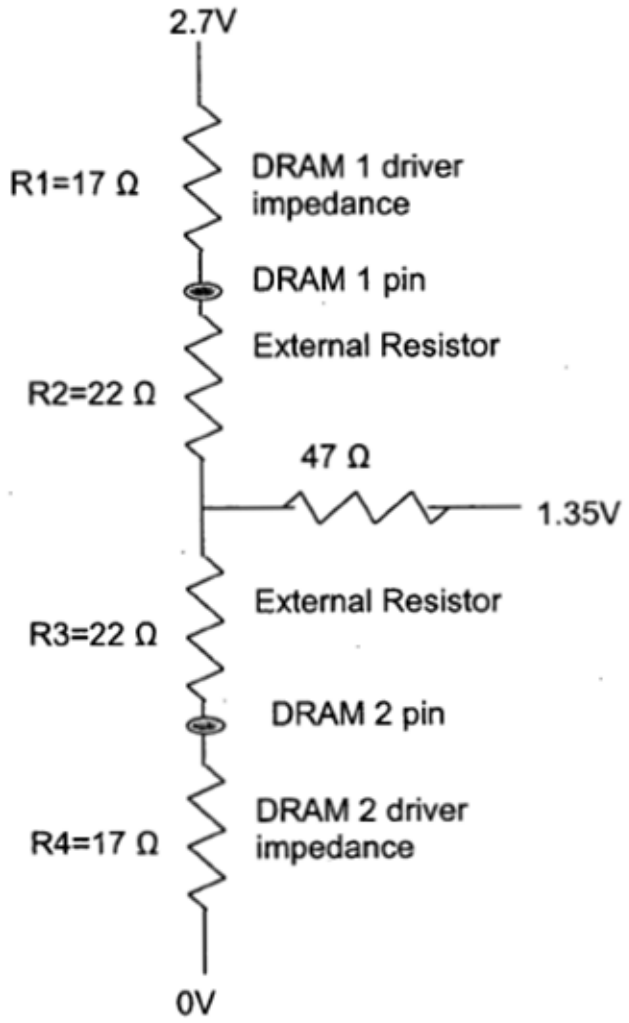


Figure 3:
DIMM
VDDQ = 2.7V max
Current Limiting Resistors
22 Ω
DQS1
22 Ω
DQS2
DRAM Read Cycle
Controller
25 Ω
47 Ω
VTT = VDDQ/2 = 1.35V
Absolute worst case:
Is min to max tDQSQ
feasible with two DRAMs from same supplier?
SSO effects may cause some % of this
DQS1
DQS2
2 * tDQSQ = 0.8ns

Figure 4:



2. Provisional Application No. 60/575,595 (May 28, 2004)

76. The applicants filed Provisional Application No. 60/575,595 ("595 Provisional Application"), titled "Method of Forming a Memory Module Having x8 Organization Using DRAM Devices Having x4 Organization," on May 28, 2004. EX1008 at p. 1. The named inventors on this provisional application are William M. Gervasi (who is not a named inventor on the 215 Patent) and Jeff Solomon. *Id*. at p. 1. In the application, "two lower-density devices are used to

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simulate one higher-density memory device…. [T]he SPD device of the memory module is programmed to describe the combined pair of lower-density memory devices as one pseudo-higher-density memory device." *Id.* at [0011]. Further, the application presents the table of possible configurations for different sizes of memory devices specified by the JEDEC standard JESD79D and gives examples of these configurations. *Id*. at [0006].

3. Provisional Application No. 60/588,244 (Jul. 15, 2004)

77. The applicants filed Provisional Application No. 60/588,244 ("244 Provisional Application"), titled "Memory Module Decoder for Simulating a Memory Module Having Fewer Ranks," on July 15, 2004. EX1006 at p. 1. The named inventors on this provisional application are Robert S. Pauley (who is not a named inventor on the 215 Patent), Jayesh R. Bhakta, William M. Gervasi (who is not a named inventor on the 215 Patent), Chi She Chen (who is not a named inventor on the 215 Patent), Jeffrey C. Solomon, and Yu Hui Zhang (who is not a named inventor on the 215 Patent). *Id*. at p. 1. FIG. 1 of this application describes a memory module with a phase-locked loop ("PLL") device, a register that buffers address signals from a processor and sends them to appropriate ranks of memory, and an ASIC that uses two chip-select signals provided by the processor. *Id*. at [0009], FIG. 1 (below). The application further provides a logic table for selection of ranks. *Id*. at Table 1 (below).

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Figure 1:

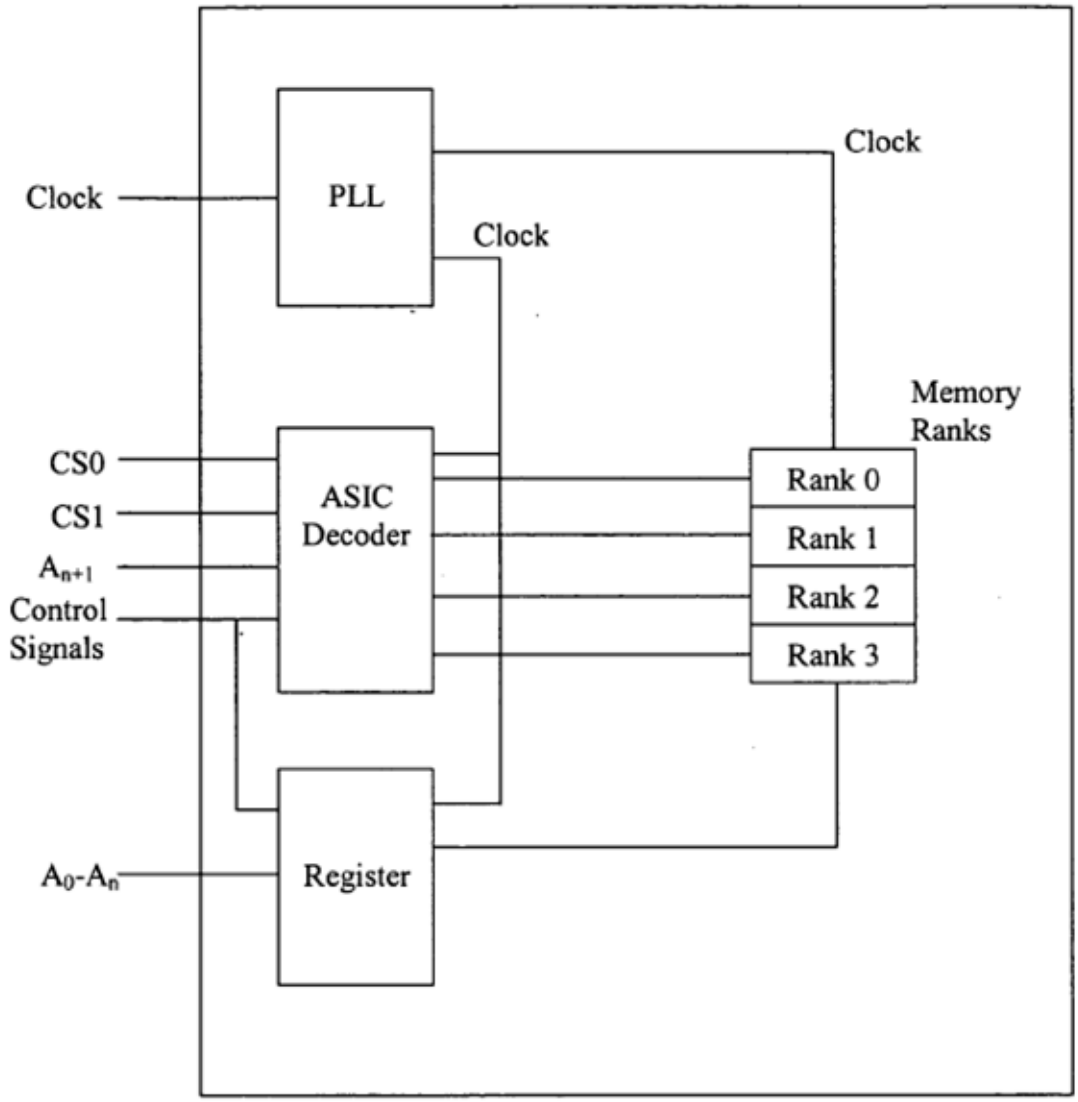
Clock
PLL
Clock
Clock
Memory
Ranks
CS0
CS1
A_{n+1}
Control
Signals
ASIC
Decoder
Rank 0
Rank 1
Rank 2
Rank 3
A_0-A_n
Register

Table 1:

State	CS0	CS1	A_{n+1}	Control	RS0	RS1	RS2	RS3
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

4. Provisional Application No. 60/590,038 (Jul. 21, 2004)

78. The applicants filed Provisional Application No. 60/590,038 ("038 Provisional Application"), titled "Memory Module with Tied DQS Pins," on July 21, 2004. EX1009 at p. 1. The named inventors on this provisional application are William M. Gervasi (who is not a named inventor on the 215 Patent), Jeffrey Solomon, and Jayesh R. Bhakta. EX1009 at p. 1. This application purports to present "a memory module us[ing] two lower-density DDR2 synchronous dynamic random access memory ('SDRAM') integrated circuits with shared data strobe signal ('DQS') pins to simulate one higher-density DDR2 SDRAM integrated circuit." *Id*. at [0001]; FIGs. 1-2 (below).

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FIGURE 1:

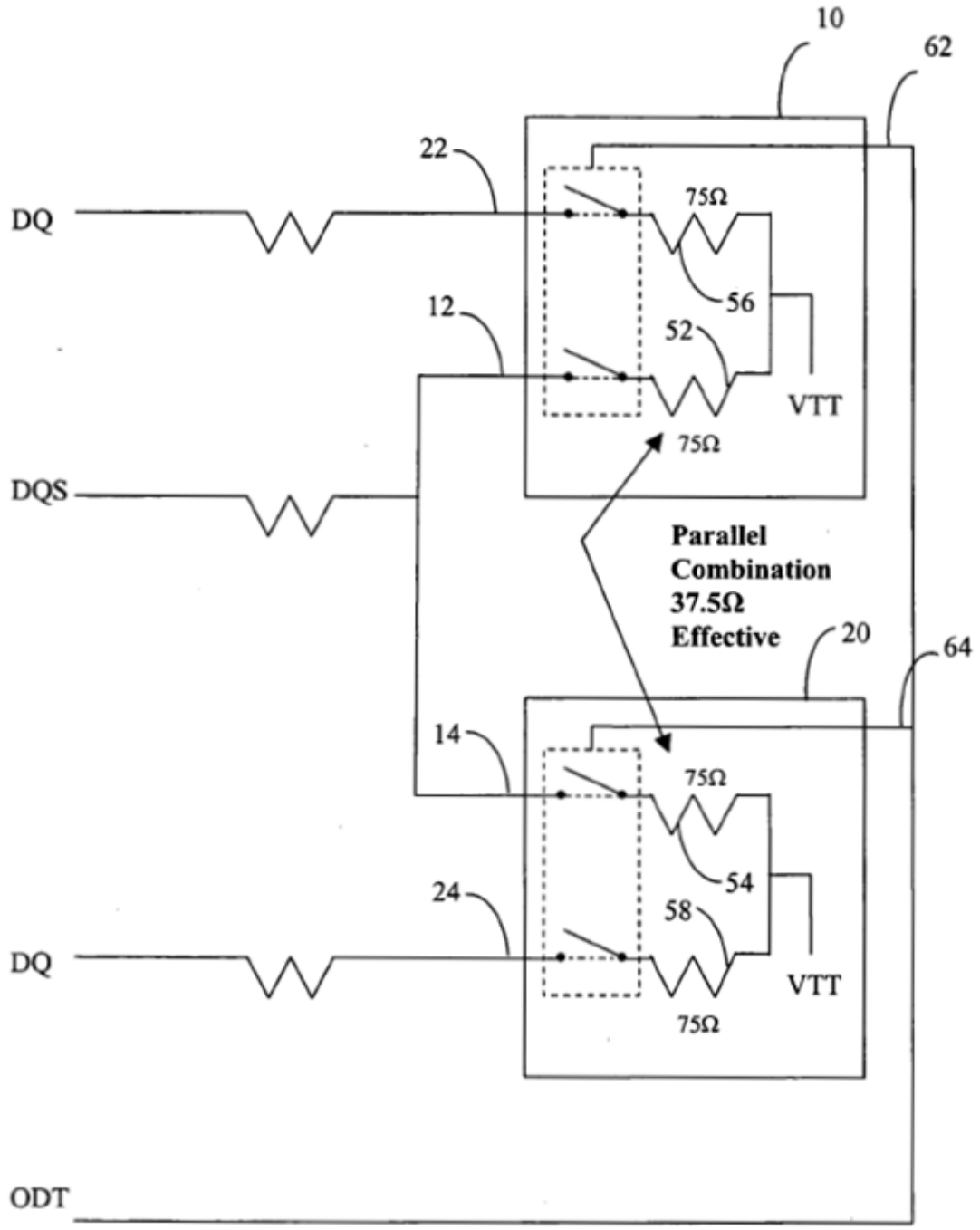
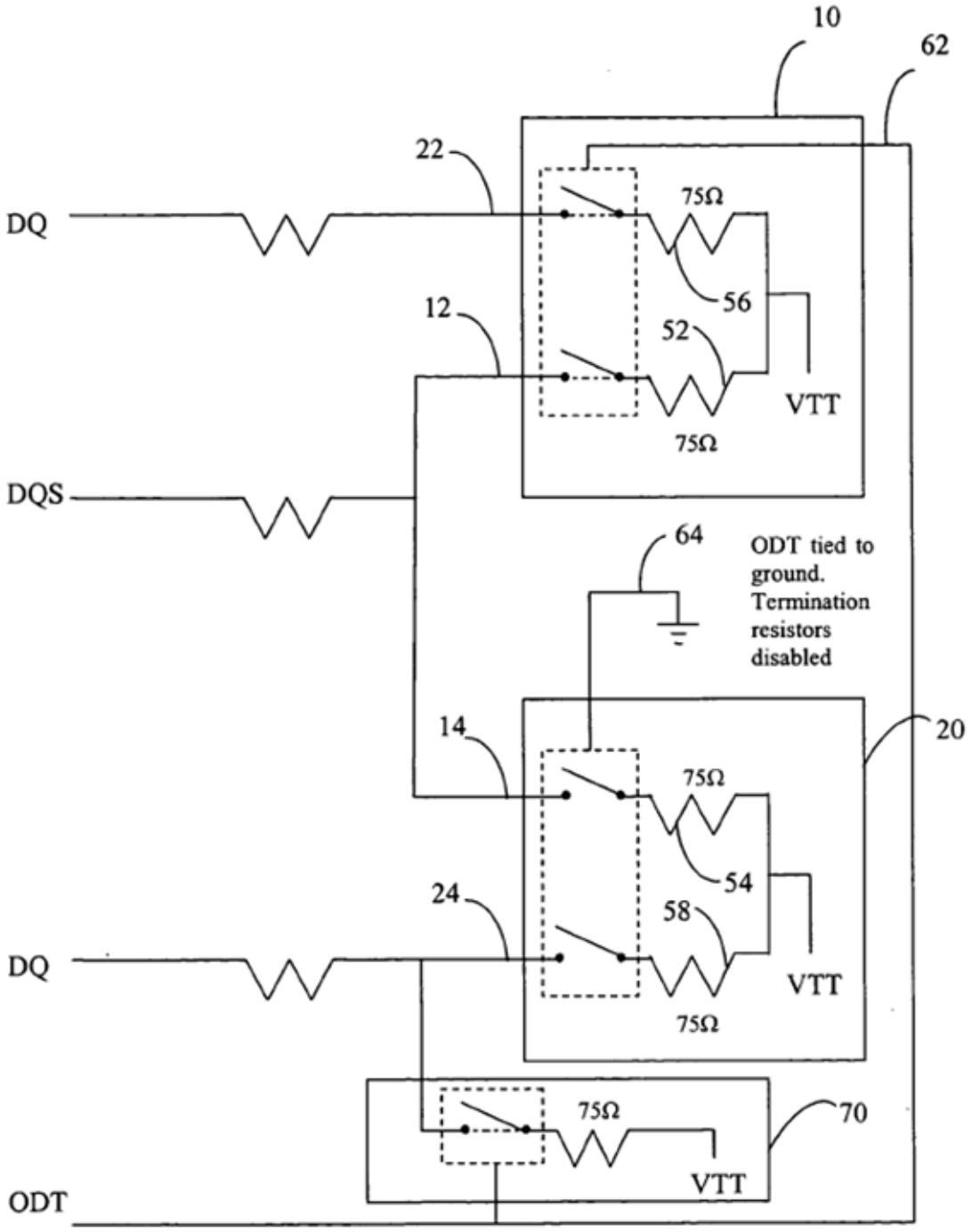

10
62
22
DQ
75Ω
56
12
52
VTT
75Ω
DQS
Parallel
Combination
37.5Ω
Effective
20
64
14
75Ω
54
24
58
DQ
VTT
75Ω
ODT

FIGURE 2:


10
62
22
DQ
75Ω
56
12
52
VTT
75Ω
DQS
64
ODT tied to ground. Termination resistors disabled
14
20
75Ω
54
24
58
DQ
VTT
75Ω
75Ω
70
VTT
ODT

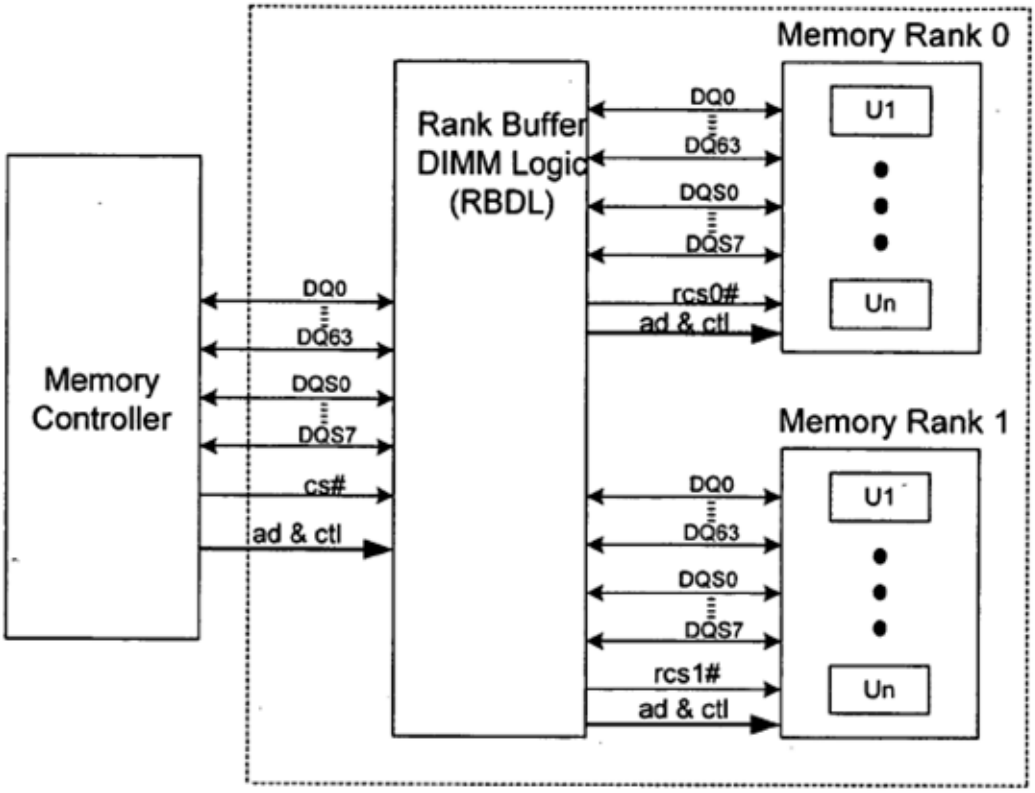
5. Provisional Application No. 60/645,087 (Jan. 19, 2005)

79. The applicants filed Provisional Application No. 60/645,087 ("087 Provisional Application"), titled "Rank Buffered Dual Inline Memory Module," on January 19, 2005. EX1005 at p. 1. The only inventor listed on this provisional application is Jeffrey Solomon. EX1005 at p. 1. As discussed above, this provisional application does not provide support for the claims of the 215 Patent. *See supra* ¶¶51-67. The application states the following:

> "The DIMM of certain embodiments utilizes a transition bit to select which rank of memory device is enabled for a read or write transfer operation. In certain embodiments, the logic translation element further comprises a data path multiplexer/demultiplexer which logically isolate the ranks of memory devices from one another. In certain embodiments, the logic translation element further comprises a serial-presence-detect (SPD) element which reports the CAS latency (CL) to the memory controller. The SPD element of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array."

Id. at [0005].

FIGURE 1:



Block Diagram: Rank Buffered DIMM Memory Sub-system

6. Application No. 11/075,395 (436 Patent) (Mar. 7, 2005)

80. The applicants filed U.S. Patent Application No. 11/075,395 ("395 Application"), titled "High-Density Memory Module Utilizing Low-Density Memory Components," on March 7, 2005. EX1001 at p. 2. The 395 Application claims the benefit of the 668 Provisional Application, filed March 5, 2004, the 595 Provisional Application, filed May 28, 2004, and the 038 Provisional Application, filed July 21, 2004. EX1010 p. 4. The 395 Application does not claim priority to the 087 Provisional Application filed January 19, 2005. *Id.* The 395 Application presented claims 1-27 at the time of filing. *Id.* at pp. 30-34.

81. On September 14, 2006, in an Office Action, Claims 1-27 were subject to restriction requirements. *Id.* at p. 96-99.

82. On October 10, 2006, applicants filed an amendment to cancel claims 1-25, and 27, to amend claim 26, and presented new claims 28-46. *Id.* at pp. 102-106.

83. On January 2, 2007 in a non-final Office Action, Claims 26, 28-30, and 33 were rejected as anticipated by Patent No. 6,944,694 ("Pax"). *Id.* at 115-116. Claims 31 and 32 were rejected as obvious in view of Pax. *Id.* at 116-117. Claims 34-45 were objected to for being dependent upon a rejected base claim. *Id.* at pp. 117-118.

84. On February 21, 2007, applicants amended Claims 26, 34, 40, and 46. *Id.* at p. 124-129. The applicants argued that the prior art, Pax, "does not disclose or suggest that the address signals are modified (e.g., by changing a row address into a column address) to be compatible with a different memory capacity. Therefore, Pax does not disclose or suggest 'a logic element' as recited by Claim 26." EX1010 at p. 132.

85. On April 3, 2007, in a final Office Action, Claims 26, 28-30, and 33 were rejected again as anticipated by Pax, and Claims 31 and 32 were rejected as obvious in view of Pax. EX1010 at pp. 138-144.

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86. On June 1, 2007, applicants cancelled claims 26, 28-33, and 46, and added Claims 47-54. EX1010 at 146-150.

87. On June 19, 2007, the Office mailed a Notice of Allowance to applicants with no reason given for allowance. EX1010 pp. 158-161.

88. Application 11/075,395 was issued on October 23, 2007, as U.S. Patent No. 7,286,436 with 20 claims. EX1010 at p. 172; EX1011.

7. Application No. 11/173,175 (386 Patent) (July 1, 2005)

89. While the 436 Patent (discussed above) was pending, the applicants filed a continuation-in-part application (No. 11/173,175) on July 1, 2005, which resulted in U.S. Patent No. 7,289,386 on October 30, 2007. EX1001 at p. 2; EX1012. The 386 Patent was then reexamined, and all the issued claims (1-13) were cancelled. EX1013; EX1014. Claims 1-13 are reproduced below:

> 1. A memory module connectable to a computer system, the memory module comprising:
>
> a printed circuit board;
>
> a plurality of memory devices coupled to the printed circuit board, the plurality of memory devices having a first number of memory devices; and
>
> a logic element coupled to the printed circuit board, the logic element receiving a set of input control signals from the computer system, the set of input control signals corresponding to a second number of memory devices smaller than the first number of memory devices, the logic element generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of memory devices, wherein the plurality of memory devices are arranged in a first number of ranks,

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and the set of input control signals corresponds to a second number of ranks of memory modules, the second number of ranks less than the first number of ranks, wherein the logic element further responds to a first command signal from the computer system by generating a second command signal transmitted to the plurality of memory devices, the first command signal corresponding to the second number of ranks and the second command signal corresponding to the first number of ranks.

2. The memory module of claim 1, wherein the first command signal is a refresh signal or a precharge signal.

3. The memory module of claim 1, wherein the memory devices comprise dynamic random-access memory (DRAM) devices.

4. The memory module of claim 1, wherein the set of input control signals comprises a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals, wherein the first number of chip-select signals is less than the second number of chip-select signals, the memory module simulating a virtual memory module having the second number of memory devices.

5. The memory module of claim 1, wherein the logic element comprises an application-specific integrated circuit.

6. The memory module of claim 1, wherein the logic element comprises a field-programmable gate array.

7. The memory module of claim 1, wherein the logic element comprises a custom-designed semiconductor device.

8. The memory module of claim 1, wherein the logic element comprises a complex programmable-logic device.

9. The memory module of claim 1, wherein the first number of ranks is four, and the second number of ranks is two.

10. The memory module of claim 1, wherein the first number of ranks is two, and the second number of ranks is one.

11. The memory module of claim 1, wherein the set of input control signals comprises two chip-select signals and an address signal and the set of output control signals comprises four chip-select signals.

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12. The memory module of claim 1, wherein the printed circuit board is mountable in a module slot of the computer system, the printed circuit board having a plurality of edge connections electrically coupled to corresponding contacts of the module slot.

13. The memory module of claim 1, wherein the plurality of memory devices are arranged to provide a first memory density per rank, and the set of output control signals corresponds to a second memory density per rank, the second memory density greater than the first memory density per rank.

8. U.S. Patent No. 7,619,912 (continuation of 386 Patent)

90. While the 386 Patent (discussed above) was pending, the applicants filed a continuation application (No. 11/862,931) on September 27, 2007, which resulted in U.S. Patent No. 7,619,912 on November 17, 2009. EX1015. The 912 Patent was then reexamined, and all claims were either cancelled or amended. EX1015 at pp. 42-49; EX1016; EX1017. Claim 16 (as amended) is currently the subject of an *inter partes* review. EX1018-EX1023. I understand that the decision instituting this *inter partes* review is being reviewed, but that the review concerns issues unrelated to the technical merits of whether or not claim 16 is obvious in light of the prior art. EX1024-EX1025. Original claims 1-51 of the 912 Patent are reproduced below:

1. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register.

2. The memory module of claim 1, wherein the circuit is configured to store an input control signal of the set of input control signals during a row access procedure and to transmit the stored input control signal as an output control signal of the set of output control signals during a column access procedure.

3. The memory module of claim 1, wherein the set of input control signals comprises a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals greater than the first number of chip-select signals.

4. The memory module of claim 3, wherein the first number of chip-select signals is two and the second number of chip-select signals is four.

5. The memory module of claim 1, wherein the circuit receives and buffers a plurality of row/column address signals of the input control signals

during a row access procedure and sends the buffered plurality of row/column address signals to the plurality of DDR memory devices during a subsequent column access procedure.

6. The memory module of claim 1, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.

7. The memory module of claim 1, wherein the bank address signals of the set of input control signals are received by both the logic element and the register.

8. The memory module of claim 1, wherein two or more of the phase-lock loop device, the register, and the logic element are portions of a single component.

9. The memory module of claim 1, wherein the register comprises a plurality of register devices.

10. The memory module of claim 1, wherein the plurality of DDR memory devices is arranged as a first set of DDR memory devices on a first side of the printed circuit board, a second set of DDR memory devices on the first side of the printed circuit board, a third set of DDR memory devices on a second side of the printed circuit board, and a fourth set of DDR memory devices on the second side of the printed circuit board, the DDR memory devices of the second set spaced from the DDR memory devices of the first set, the DDR memory devices of the fourth set spaced from the DDR memory devices of the third set.

11. The memory module of claim 10, wherein the DDR memory devices of the second set are spaced from the DDR memory devices of the first set in a direction along the first side and the memory devices of the fourth set are spaced from the memory devices of the third set in a direction along the second side.

12. The memory module of claim 1, wherein the plurality of DDR memory devices comprises a plurality of DDR2 memory devices arranged in a first rank, a second rank, a third rank, and a fourth rank, the first rank and the second rank on a first side of the printed circuit board, the third rank and the fourth rank on a second side of the printed circuit board, the second side different from the first side.

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13. The memory module of claim 12, wherein the first rank is spaced from the second rank and the third rank is spaced from the fourth rank.

14. The memory module of claim 1, wherein the set of input control signals corresponds to a first memory density, and the set of output control signals corresponds to a second memory density, the second memory density greater than the first memory density.

15. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register.

16. The memory module of claim 15, wherein the command signal is transmitted to only one DDR memory device at a time.

17. The memory module of claim 16, wherein the command signal comprises a read command signal.

18. The memory module of claim 15, wherein the command signal is transmitted to two ranks of the first number of ranks at a time.

19. The memory module of claim 18, wherein the command signal comprises a refresh command signal.

20. The memory module of claim 18, wherein the command signal is transmitted to the two ranks of the first number of ranks concurrently.

21. The memory module of claim 15, wherein the circuit is configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure.

22. The memory module of claim 15, wherein the command signal comprises a read command signal or a write command signal, the set of input signals comprises a density bit which is a row address bit, and the circuit is configured to store the row address bit during an activate command for a selected bank.

23. The memory module of claim 15, wherein the circuit is configured to store an input signal of the set of input signals during a row access procedure and to transmit the stored input signal as an output signal of the set of output signals during a subsequent column access procedure.

24. The memory module of claim 15, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.

25. The memory module of claim 15, wherein the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices.

26. The memory module of claim 25, wherein the logic element receives the bank address signals and the command signal from the computer system and the register receives the bank address signals and the command signal from the computer system.

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27. The memory module of claim 15, wherein two or more of the phase-lock loop device, the register, and the logic element are portions of a single component.

28. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register.

29. The memory module of claim 28, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.

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30. The memory module of claim 29, wherein the circuit is configured to store an input control signal of the set of input control signals during a row access procedure and to transmit the stored input control signal as an output control signal of the set of output control signals during a column access procedure.

31. The memory module of claim 28, wherein the set of input control signals comprises fewer chip-select signals than does the set of output control signals.

32. The memory module of claim 31, wherein the set of input control signals comprises two chip-select signals and the set of output control signals comprises four chip-select signals.

33. The memory module of claim 28, wherein the register receives the bank address signals and the input command signal of the set of input control signals.

34. The memory module of claim 28, wherein the first number of ranks is four and the second number of ranks is two.

35. The memory module of claim 28, wherein the first number of ranks is two and the second number of ranks is one.

36. The memory module of claim 28, wherein the input command signal is a refresh signal and the output command signal is a refresh signal.

37. The memory module of claim 28, wherein the input command signal is a precharge signal and the output command signal is a precharge signal.

38. The memory module of claim 28, wherein the input command signal is a read signal or a write signal and the output command signal is a read signal or a write signal.

39. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board having a first side and a second side;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or

more ranks which are selectable by a first number of chip-select signals; and

at least one integrated circuit element mounted to the printed circuit board, the at least one integrated circuit element comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the at least one integrated circuit element receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives the bank address signals and at least one command signal of the plurality of input signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals, the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank.

40. The memory module of claim 39, wherein the plurality of output signals corresponds to a first number of DDR memory devices arranged in the two or more ranks which are selectable by the first number of chip-select signals and wherein the plurality of input signals corresponds to a second number of DDR memory devices arranged in ranks which are selectable by the second number of chip-select signals, wherein the memory module simulates a virtual memory module having the second number of DDR memory devices.

41. The memory module of claim 39, wherein the at least one integrated circuit element comprises one or more integrated circuit elements selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device.

42. The memory module of claim 39, wherein the row address signals and the column address signals of the plurality of input signals are received and

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buffered by the register and are sent from the register to the plurality of DDR memory devices.

43. The memory module of claim 42, wherein the logic element receives the second number of chip-select signals.

44. The memory module of claim 43, wherein both the register and the logic element receive the bank address signals and at least one command signal of the plurality of input signals.

45. The memory module of claim 39, wherein two or more of the logic element, the register, and the phase-lock loop device are portions of a single component.

46. The memory module of claim 39, wherein the plurality of DDR memory devices is arranged as the first rank of DDR memory devices on the first side of the printed circuit board, the second rank of DDR memory devices on the first side of the printed circuit board, a third rank of DDR memory devices on the second side of the printed circuit board, and a fourth rank of DDR memory devices on the second side of the printed circuit board, the DDR memory devices of the fourth rank spaced from the DDR memory devices of the third rank.

47. The memory module of claim 39, wherein the DDR memory devices of the second rank are spaced from the DDR memory devices of the first rank in a direction along the first side.

48. The memory module of claim 39, wherein the plurality of DDR memory devices comprises a plurality of DDR2 memory devices arranged in the first rank, the second rank, a third rank, and a fourth rank, the third rank and the fourth rank on the second side of the printed circuit board.

49. The memory module of claim 39, wherein the plurality of input signals corresponds to a first memory density, and the plurality of output signals corresponds to a second memory density, the second memory density greater than the first memory density.

50. The memory module of claim 39, wherein the at least one integrated circuit element is configured to respond to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting a command signal to at least one DDR memory device of the selected at least one rank.

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51. The memory module of claim 39, wherein the at least one integrated circuit element is configured to store a signal of the plurality of input signals during a row access procedure and to transmit the stored signal as an output signal of the plurality of output signals during a column access procedure.

9. U.S. Patent No. 7,864,627 (continuation of 912 Patent)

91. While the 912 Patent (discussed above) was pending, the applicants filed a continuation application (No. 12/577,682) on October 12, 2009, which resulted in U.S. Patent No. 7,864,627 on January 4, 2011. EX1026. The 627 Patent was then reexamined, and all claims were either cancelled or amended. EX1027-EX1028. Original claims 1-20 of the 627 Patent are reproduced below:

1. A circuit configured to be mounted on a memory module so as to be electrically coupled to a first number of double-data-rate (DDR) memory devices arranged in a first number of ranks on the memory module, the memory module configured to be electrically coupled to a memory controller of a computer system so as to receive a set of input signals from the computer system, the set of input signals comprising row/column address signals, bank address signals, and chip-select signals, the set of input signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit comprising:

a logic element configurable to receive the set of input signals;

a register; and

a phase-lock loop circuit configurable to be operatively coupled to the first number of DDR memory devices, the logic element, and the register,

wherein the circuit is configurable to generate a set of output signals in response to the set of input signals, the set of output signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit is configurable to further

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respond to the set of input signals from the computer system by generating and transmitting the set of output signals to the first number of DDR memory devices.

2. The circuit of claim 1, wherein the set of input signals comprises a first number of chip-select signals and wherein the set of output signals comprises a second number of chip-select signals greater than the first number of chip-select signals.

3. The circuit of claim 2, wherein the first number of chip-select signals is two.

4. The circuit of claim 1, wherein the circuit is configurable to receive and buffer a plurality of row/column address signals of the input signals during a row access procedure and to use the buffered plurality of row/column address signals during a subsequent column access procedure.

5. The circuit of claim 1, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.

6. The circuit of claim 1, wherein the bank address signals of the set of input signals are received by both the logic element and the register.

7. The circuit of claim 1, wherein two or more of the phase-lock loop circuit, the register, and the logic element are portions of a single component.

8. The circuit of claim 1, wherein the register comprises a plurality of register circuits.

9. The circuit of claim 1, wherein the plurality of DDR memory devices comprises a plurality of DDR3 memory devices.

10. The circuit of claim 1, wherein the set of input signals corresponds to a first memory density per rank, and the set of output signals corresponds to a second memory density per rank, the second memory density per rank less than the first memory density per rank.

11. The circuit of claim 1, wherein the circuit is configurable to further respond to the set of input signals from the computer system by selecting at

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least one rank of the first number of ranks and transmitting the set of output signals to at least one DDR memory device of the selected at least one rank of the first number of ranks.

12. The circuit of claim 1, wherein the circuit is configurable to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure.

13. A circuit configured to be mounted on a memory module so as to be electrically coupled to a first number of double-data-rate (DDR) memory devices arranged in a first number of ranks on the memory module, the memory module configured to be electrically coupled to a memory controller of a computer system so as to receive a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit comprising:

a logic element configurable to receive the set of input signals;

a register; and

a phase-lock loop circuit configurable to be operatively coupled to the first number of DDR memory devices, the logic element, and the register,

wherein the circuit is configurable to generate a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit is configurable to transmit the set of output signals to the first number of DDR memory devices.

14. The circuit of claim 13, wherein the set of input signals comprises a number of chip-select signals and wherein the set of output signals comprises more chip-select signals than the number of chip-select signals.

15. The circuit of claim 13, wherein the circuit is configurable to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure.

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16. The circuit of claim 13, wherein the circuit is configurable to select at least one rank of the first number of ranks and to transmit the set of output signals to at least one DDR memory device of the selected at least one rank of the first number of ranks.

17. The circuit of claim 13, wherein two or more of the phase-lock loop circuit, the register, and the logic element are portions of a single component.

18. The circuit of claim 13, wherein the set of input signals corresponds to a first memory density per rank, and the set of output signals corresponds to a second memory density per rank, the second memory density per rank less than the first memory density per rank.

19. A circuit configured to be mounted on a memory module so as to be electrically coupled to a first number of double-data-rate (DDR) memory devices arranged in a first number of ranks on the memory module, the first number of ranks selectable by a first number of chip-select signals, the memory module configured to be electrically coupled to a memory controller of a computer system so as to receive a set of input signals from the computer system, the set of input signals comprising row address signals, column address signals, bank address signals, and a second number of chip-select signals less than the first number of chip-select signals, the set of input signals configured to utilize a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit comprising:

a logic element configurable to receive the set of input signals;

a register; and

a phase-lock loop circuit configurable to be operatively coupled to the first number of DDR memory devices, the logic element, and the register,

wherein the circuit is configurable to generate a set of output signals in response to the set of input signals, the set of output signals comprising the first number of chip-select signals and configured to utilize the first number of DDR memory devices arranged in the first number of ranks.

20. The circuit of claim 19, wherein two or more of the phase-lock loop circuit, the register, and the logic element are portions of a single component.

10. U.S. Patent No. 8,756,364 (continuation of continuation of continuation of 627 Patent)

92. While the 627 Patent (discussed above) was pending, the applicants filed a continuation application (No. 12/954,492) on November 24, 2010, which resulted in U.S. Patent No. No. 8,081,535 on December 20, 2011. While the 535 Patent was pending, the applicants filed a continuation application (No. 13/154,172) on June 6, 2011, which resulted in U.S. Patent No. 8,081,537 on December 20, 2011. While the 537 Patent was pending, the applicants filed a continuation application (No. 13/287,042) on November 1, 2011, which resulted in U.S. Patent No. 8,756,364 on June 17, 2004. EX1029. Claims 1-4, 6-7, 10, 13, 17, and 23 of the 364 Patent, reproduced below, were then subject to *inter partes* review and cancelled. EX1030-EX1031.

1. A memory module to be coupled to a memory controller via a plurality of signal lines, including input control signal lines, DQ data signal lines and DQS data strobe signal lines, the memory module comprising:

a first logic element to receive input control signals associated with a first memory command from the memory controller via the input control signal lines, and to generate output control signals in response to the input control signals;

memory devices organized in a number of ranks including a first rank receiving a first set of one or more of the output control signals and at least one second rank receiving at least one second set of one or more of the output control signals, wherein a first memory device in the first rank and at least one second memory device in the at least one second

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rank communicate with the memory controller via a common set of the DQ and DQS signal lines among the plurality of signal lines; and

a second logic element to selectively enable data communication between the first memory device and the memory controller via the common set of the DQ and DQS signal lines in response to the first memory command while isolating a load associated with the at least one second memory device from the common set of the DQ and DQS signal lines;

wherein the first logic element is configured to determine a latency value based on a previous memory command received by the memory module from the memory controller, and wherein the first logic element controls the second logic element to selectively enable the data communication according to the latency value.

2. The memory module of claim 1, wherein one or both of the first logic element and the second logic element are included in an integrated circuit.

3. The memory module of claim 1, wherein the first logic element and the second logic element are in separate respective integrated circuits.

4. The memory module of claim 1, wherein the first memory command is a read command or write command.

6. The memory module of claim 1, wherein the at least one second memory device does not receive or output data in response to the first memory command.

7. The memory module of claim 1, wherein the first set of one or more of the output control signals include a first chip select signal and the second set of one or more of the output control signals include at least one second chip select signal, the first chip select signal and the at least one second chip select signals select the first rank to output or receive data and do not select the at least one second rank to output or receive data.

10. The memory module of claim 1, wherein the second logic element is coupled between memory devices including the first memory device and the at least one second memory device and the common set of the DQ and DQS signal lines.

13. The memory module of claim 1, wherein the output control signals include a first number of chip select signals while the input control signals

include a smaller number of chip select signals than the first number of chip select signals.

17. A method of operating a memory module coupled to a memory controller via a plurality of signal lines, including input control signal lines, DQ data signal lines and DQS data strobe signal lines, the method comprising:

receiving input control signals associated with a first memory command from the memory controller via the input control signal lines;

generating output control signals in response to the input control signals;

transmitting the output control signals to a plurality of memory devices, the plurality of memory devices being organized in a number of ranks including a first rank receiving a first set of one or more of the output control signals and at least one second rank receiving at least one second set of one or more of the output control signals, wherein a first memory device in the first rank and a second memory device in the at least one second rank communicate data with the memory controller via a common set of the DQ and DQS signal lines among the plurality of signal lines; and

selectively enabling data communication between the first memory device and the memory controller in response to the first memory command while isolating a load associated with the at least one second memory device from the common set of the DQ and DQS signal lines;

wherein the method further comprises determining a latency value based on a previous memory command received from the memory controller and controlling the selective enabling of the data communication in accordance with the latency value.

23. The memory module of claim 17, wherein the at least one second memory device does not receive or output data in response to the first memory command.

11. Application No. 11/335,875 (537 Patent) (Jan. 19, 2006)

93. While the 386 Patent (discussed above) was pending, the applicants filed a continuation-in-part application on January 19, 2006, which resulted in U.S.

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Patent No. 7,532,537. EX1001 p. 2. The 537 Patent was then reexamined, resulting in 60 claims. EX1032 at pp. 49-52. All 60 claims of the 537 Patent, reproduced below, were then subject to *inter partes* review and cancelled. EX1033 at pp. 1-44; EX1034 at pp. 1-46; EX1035.

1. A memory module comprising:

a plurality of memory devices, each memory device having a corresponding load; and

a circuit electrically coupled to the plurality of memory devices and configured to be electrically coupled to a memory controller of a computer system, the circuit selectively isolating one or more of the loads of the memory devices from the computer system, the circuit comprising logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module, wherein the system memory domain is compatible with a first number of chip selects, and the physical memory domain is compatible with a second number of chip selects equal to twice the first number of chip selects, wherein the plurality of memory devices comprises double-data rate (DDR) dynamic random-access memory (DRAM) devices and the chip selects of the first and second number of chip selects are DDR chip selects that are not CAS, RAS, or bank address signals.

2. The memory module of claim1, wherein the circuit comprises a logic element selected from a group consisting of: a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, and a complex programmable logic device (CPLD).

3. The memory module of claim 2, wherein the circuit further comprises one or more switches operatively coupled to the logic element to receive control signals from the logic element.

4. The memory module of claim 1, wherein the plurality of memory devices has a first number of memory devices, and the circuit selectively

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isolates the loads of a second number of the memory devices from the computer system, the second number less than the first number.

5. The memory module of claim 4, wherein the first number of memory devices are configured in a plurality of ranks, and wherein the second number of memory devices are configured as one rank of the plurality of ranks.

6. The memory module of claim 1, wherein the logic translates address signals in the system memory domain to address signals in the physical memory domain.

7. The memory module of claim 1, wherein the plurality of memory devices are arranged in one or more ranks and the system memory domain is compatible to a first memory density per rank, and the physical memory domain is compatible with a second memory density per rank equal to half the first memory density per rank.

8. The memory module of claim 1, wherein the plurality of memory devices comprises a pair of memory devices, each memory device of the pair having a first memory capacity, the pair of memory devices configured to simulate a memory device having a second memory capacity equal to twice the first memory capacity.

9. The memory module of claim 1, wherein the memory module comprises a dual inline memory module.

10. The memory module of claim 9, wherein the memory module comprises a rank-buffered dual inline memory module.

11. The memory module of claim 1, wherein the memory module comprises a DDR2 SDRAM memory array.

12. The memory module of claim 1, wherein the circuit selectively isolates the loads of the memory devices from the computer system in response to a command or address signal received from the computer system.

13. A method of using a memory module with a computer system, the method comprising:

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providing a memory module having a plurality of memory devices and a circuit comprising logic and electrically coupled to the plurality of memory devices, the circuit configured to be electrically coupled to a computer system, each memory device having a corresponding load;

electrically coupling the memory module to the computer system; and

activating the circuit to selectively isolate at least one of the loads of the memory devices from the computer system and to translate between a system memory domain of the computer system and a physical memory domain of the memory module, wherein the system memory domain is compatible with a first number of chip selects, and the physical memory domain is compatible with a second number of chip selects equal to twice the first number of chip selects, wherein the plurality of memory devices comprises double- data rate (DDR) dynamic random-access memory (DRAM) devices and the chip selects of the first and second number of chip selects are DDR chip selects that are not CAS, RAS, or bank address signals.

14. The method of claim 13, wherein the plurality of memory devices comprises a pair of memory devices, each memory device of the pair having a first memory capacity, the is pair of memory devices configured to simulate a memory device having a second memory capacity equal to twice the first memory capacity.

15. The method of claim 13, wherein the logic translates address signals in the system memory domain to address signals in the physical memory domain.

16. The method of claim 13, wherein the plurality of memory devices are arranged in one or more ranks and the system memory domain is compatible to a first memory density per rank, and the physical memory domain is compatible with a second memory density per rank equal to half the first memory density per rank.

17. The method of claim 13, wherein the memory module comprises a dual inline memory module.

18. A memory module connectable to a computer system, the memory module comprising:

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a first memory device having a first data signal line and a first data strobe signal line;

a second memory device having a second data signal line and a second data strobe signal line;

a common data signal line connectable to the computer system; and

a device electrically coupled to the first data signal line, to the second data signal line, and to the common data signal line, the device selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line, the device comprising logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module, wherein the system memory domain is compatible with a first number of chip selects, and the physical memory domain is compatible with a second number of chip selects equal to twice the first number of chip selects, wherein the first memory device and the second memory device are double-data rate (DDR) dynamic random-access memory (DRAM) devices and the chip selects of the first and second number of chip selects are DDR chip selects that are not CAS, RAS, or bank address signals.

19. The memory module of claim 18, wherein the device comprises a logic element.

20. The memory module of claim 19, wherein the logic element is selected from the group consisting of: an application-specific integrated circuit, a custom-programmable logic device, and a field-programmable gate array.

21. The memory module of claim 18, wherein the device comprises at least one switch which selectively electrically couples the first data signal line to the common data signal line and selectively electrically couples the second data signal line to the common data signal line.

22. The memory module of claim 18, wherein the memory module further comprises a common data strobe signal line connectable to the computer system, the device electrically coupled to the first data strobe signal line, to the second data strobe signal line, and to the common data strobe signal line, the device selectively electrically coupling the first data strobe signal line to

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the common data strobe signal line and selectively electrically coupling the second data strobe signal line to the common data strobe signal line.

23. The memory module of claim 18, wherein the device selectively electrically couples the first data strobe signal line to a common data strobe signal line and selectively electrically couples the second data strobe signal line to the common data strobe signal line.

24. A memory module comprising:

a plurality of memory devices arranged in one or more ranks, each memory device having a corresponding load; and

a circuit electrically coupled to the plurality of memory devices and configured to be electrically coupled to a memory controller of a computer system, the circuit selectively isolating one or more of the loads of the memory devices from the computer system, the circuit comprising logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module, wherein the system memory domain is compatible with a first number of chip selects and a first memory density per rank, and the physical memory domain is compatible with a second number of chip selects equal to twice the first number of chip selects and a second memory density per rank less than the first memory density per rank.

25. The memory module of claim 24, wherein the circuit comprises a logic element selected from a group consisting of: a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, and a complex programmable-logic device (CPLD).

26. The memory module of claim 25, wherein the circuit further comprises one or more switches operatively coupled to the logic element to receive control signals from the logic element.

27. The memory module of claim 24, wherein the plurality of memory devices has a first number of memory devices, and the circuit selectively isolates the loads of a second number of the memory devices from the computer system, the second number less than the first number.

28. The memory module of claim 27, wherein the first number of memory devices are configured in a plurality of ranks, and wherein the second

number of memory devices are configured as one rank of the plurality of ranks.

29. The memory module of claim 24, wherein the logic translates address signals in the system memory domain to address signals in the physical memory domain.

30. The memory module of claim 24, wherein the plurality of memory devices comprises a pair of memory devices, each memory device of the pair having a first memory capacity, the pair of memory devices configured to simulate a memory device having a second memory capacity equal to twice the first memory capacity.

31. The memory module of claim 24, wherein the memory module comprises a dual inline memory module.

32. The memory module of claim 31, wherein the memory module comprises a rank-buffered dual inline memory module.

33. The memory module of claim 24, wherein the memory module comprises a DDR2 SDRAM memory array.

34. The memory module of claim 24, wherein the circuit selectively isolates the loads of the memory devices from the computer system in response to a command or address signal received from the computer system.

35. A method of using a memory module with a computer system, the method comprising:

providing a memory module having a plurality of memory devices arranged in one or more ranks and a circuit electrically coupled to the plurality of memory devices, the circuit configured to be electrically coupled to a computer system, each memory device having a corresponding load;

electrically coupling the memory module to the computer system; and

activating the circuit to selectively isolate at least one of the loads of the memory devices from the computer system and to translate between a system memory domain of the computer system and a physical memory domain of the memory module, wherein the system memory domain is

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compatible with a first number of chip selects and a first memory density per rank, and the physical memory domain is compatible with a second number of chip selects equal to twice the first number of chip selects and a second memory density per rank less than the first memory density per rank.

36. The method of claim 35, wherein the plurality of memory devices comprises a pair of memory devices, each memory device of the pair having a first memory capacity, the pair of memory devices configured to simulate a memory device having a second memory capacity equal to twice the first memory capacity.

37. The method of claim 35, wherein the logic translates address signals in the system memory domain to address signals in the physical memory domain.

38. The method of claim 35, wherein the memory module comprises a dual inline memory module.

39. A memory module connectable to a computer system, the memory module comprising:

a first memory device having a first data signal line and a first data strobe signal line;

a second memory device having a second data signal line and a second data strobe signal line;

a common data signal line connectable to the computer system; and

a device electrically coupled to the first data signal line, to the second data signal line, and to the common data signal line, the device selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line, the device comprising logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module, wherein the system memory domain is compatible with a first number of chip selects and a first memory density per memory device, and the physical memory domain is compatible with a second number of chip selects equal to twice the first number of chip selects and a second memory

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density per memory device less than the first memory density per memory device.

40. The memory module of claim 39, wherein the device comprises a logic element.

41. The memory module of claim 39, wherein the device comprises at least one switch which selectively electrically couples the first data signal line to the common data signal line and selectively electrically couples the second data signal line to the common data signal line.

42. The memory module of claim 41, wherein the logic element is selected from the group consisting of: an application-specific integrated circuit, a custom-programmable logic device, and a field-programmable gate array.

43. The memory module of claim 39, wherein the memory module further comprises a common data strobe signal line connectable to the computer system, the device electrically coupled to the first data strobe signal line, to the second data strobe signal line, and to the common data strobe signal line, the device selectively electrically coupling the first data strobe signal line to the common data strobe signal line and selectively electrically coupling the second data strobe signal line to the common data strobe signal line.

44. The memory module of claim 39, wherein the device selectively electrically couples the first data strobe signal line to a common data strobe signal line and selectively electrically couples the second data strobe signal line to the common data strobe signal line.

45. The memory module of claim 1, wherein the circuit has a load and selectively isolating one or more of the loads of the memory devices from the computer system comprises presenting the load of the circuit to the computer system.

46. The memory module of claim 1, wherein the plurality of memory devices are arranged in a plurality of ranks and the circuit comprises a data path rank buffer which selectively electrically couples the ranks of memory devices to the computer system and isolates the ranks of memory devices of the memory module from one another and from the computer system.

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47. The memory module of claim 46, wherein the data path rank buffer provides data paths for each rank of memo devices wherein the data paths are separate from one another.

48. The memory module of claim 46, wherein the data path rank buffer provides data paths for each rank of memory devices, wherein the data paths are separate from the computer system.

49. The memory module of claim 1, wherein the logic 10 translates between the system memory domain and the physical memory domain by receiving a set of control signals corresponding to the system memory domain from the memory controller of the computer system and generating a set of control signals corresponding to the physical memory domain.

50. The memory module of claim 1, wherein the plurality of memory modules are arranged in four ranks and the memory module is configured to receive from the memory controller a set of control signals that corresponds to two 20 ranks.

51. The memory module of claim 50, wherein each memory device comprises memory locations arranged in a plurality of banks and the set of control signals comprise row/column address signals and bank address signals.

52. The method of claim 13, wherein the circuit has a load and selectively isolating at least one of the loads of the memory devices from the computer system comprises presenting the load of the circuit to the computer system.

53. The method of claim 13, wherein the plurality of memory devices are arranged in a plurality of ranks and the circuit comprises a data path rank buffer which selectively electrically couples the ranks of memory devices to the computer system and isolates the ranks of memory devices of the memory module from one another and from the computer system.

54. The method of claim 13, wherein the logic translates between the system memory domain and the physical memory domain by receiving a set of control signals corresponding to the system memory domain from the memory 40 controller of the computer system and generating a set of control signals corresponding to the physical memory domain.

55. The method of claim 13, wherein the plurality of memory modules are arranged in four ranks, the memory module is configured to receive from the memory controller a set of control signals, wherein each memory device comprises memory locations arranged in a plurality of banks and the set of control signals comprise row/column address signals and bank address signals.

56. The memory module of claim 18, wherein the first memory device is in a first rank of memory devices and the second memory device is in a second rank of memory devices, wherein the logic translates an address bit to a rank selection between the first rank and the second rank

57. The memory module of claim 18, wherein the device has a load and selectively isolating at least one of the loads of the memory devices from the computer system comprises presenting the load of the device to the computer system.

58. The memory module of claim 18, wherein the device comprises a data path rank buffer which selectively electrically couples the first memory device to the computer system, selectively electrically couples the second memory device to the computer system, and isolates the first memory device and the second memory device from one another and from the computer system.

59. The memory module of claim 18, wherein the logic translates between the system memory domain and the physical memory domain by receiving a set of control signals corresponding to the system memory domain from the memory controller of the computer system and generating a set of control signals corresponding to the physical memory domain.

60. The memory module of claim 18, wherein each of the first memory device and the second memory device comprises memory locations arranged in a plurality of banks.

12. Application No. 12/408,652 (274 Patent)

94. While the 537 Patent (discussed above) was pending, the applicants filed a continuation application (No. 12/408,652) on March 20, 2009, which resulted in U.S. Patent No. 7,636,274. EX1001 at p. 2; EX1036. The 274 Patent

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was then subject to reexamination. EX1037; EX1038. Claims 1-97 were cancelled, which are reproduced below:

1. A memory module comprising:

a plurality of double-data-rate (DDR) memory devices arranged in one or more ranks, each DDR memory device having a corresponding load;

a circuit comprising a logic element and a register, the circuit electrically coupled to the plurality of DDR memory devices and configured to be electrically coupled to a memory controller of a computer system to receive a set of input signals from the computer system, the set of input signals comprising row/column address signals, bank address signals, and chip-select signals, the set of input signals compatible with a system memory domain of the computer system, the circuit configurable to be responsive to the set of input signals by selectively isolating one or more of the loads of the DDR memory devices from the computer system, the circuit configurable to translate between the system memory domain of the computer system and a physical memory domain of the memory module, wherein the system memory domain has a first memory density per rank, and the physical memory domain has a second memory density per rank less than the first memory density per rank; and

a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register.

2. The memory module of claim 1, wherein the logic element is selected from a group consisting of: a programmable logic device, an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device.

3. The memory module of claim 2, wherein the circuit further comprises one or more switches operatively coupled to the logic element to receive control signals from the logic element.

4. The memory module of claim 1, wherein the plurality of DDR memory devices has a first number of DDR memory devices, and the circuit is configurable to selectively isolate the loads of a second number of the

DDR memory devices from the computer system, the second number less than the first number.

5. The memory module of claim 4, wherein the first number of DDR memory devices are configured in a plurality of ranks, and wherein the second number of DDR memory devices are configured as one rank of the plurality of ranks.

6. The memory module of claim 1, wherein the circuit is configurable to translate address signals in the system memory domain to address signals in the physical memory domain.

7. The memory module of claim 1, wherein the system memory domain is compatible with a first number of chip selects, and the physical memory domain is compatible with a second number of chip selects equal to twice the first number of chip selects.

8. The memory module of claim 1, wherein the first memory density per rank is equal to twice the second memory density per rank.

9. The memory module of claim 1, wherein the plurality of DDR memory devices are arranged in two or more ranks of memory devices.

10. The memory module of claim 9, wherein the circuit comprises a data path multiplexer/demultiplexer which isolates the ranks of DDR memory devices from one another.

11. The memory module of claim 1, wherein the plurality of DDR memory devices comprises a pair of DDR memory devices, each DDR memory device of the pair having a first memory capacity, the pair of DDR memory devices configured to simulate a DDR memory device having a second memory capacity greater than the first memory capacity.

12. The memory module of claim 11, wherein the second memory capacity is twice the first memory capacity.

13. The memory module of claim 1, wherein two or more of the phase-lock loop device, the logic element, and the register are portions of a single component.

14. The memory module of claim 1, wherein the memory module comprises a registered dual inline memory module.

15. The memory module of claim 14, wherein the plurality of DDR memory devices comprises DDR3 synchronous dynamic random-access memory (SDRAM) devices.

16. The memory module of claim 1, wherein the circuit is configurable to selectively isolate the loads of the DDR memory devices from the computer system in response to a command or address signal of the set of input signals.

17. The memory module of claim 1, further comprising a printed circuit board configured to be electrically coupled to the memory controller, the circuit mounted on the printed circuit board, the plurality of DDR memory devices mounted on the printed circuit board as a first set of DDR memory devices on a first side of the printed circuit board, a second set of DDR memory devices on the first side of the printed circuit board, a third set of DDR memory devices on a second side of the printed circuit board, and a fourth set of DDR memory devices on the second side of the printed circuit board, the DDR memory devices of the second set spaced from the DDR memory devices of the first set, the DDR memory devices of the fourth set spaced from the DDR memory devices of the third set.

18. The memory module of claim 1, wherein the circuit is configurable to transmit a set of output signals to the plurality of DDR memory devices, the set of output signals compatible with the physical memory domain.

19. The memory module of claim 18, wherein the set of input signals comprises a command signal and the set of output signals comprises the command signal.

20. The memory module of claim 18, wherein the circuit is configurable to receive a command signal from the computer system, select at least one rank of the one or more ranks, and transmit the command signal to at least one DDR memory device of the selected rank of DDR memory devices.

21. The memory module of claim 18, wherein the set of input signals comprises a first set of address and command signals and the set of output signals comprises a second set of address and command signals.

22. The memory module of claim 21, wherein the circuit is configurable to store an address signal of the set of input signals during a row access procedure and pass the stored address signal as an address signal of the set of output signals during a subsequent column address procedure.

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23. The memory module of claim 1, wherein the circuit is configurable to selectively isolate a data signal line of a DDR memory device of the plurality of DDR memory devices from the computer system.

24. The memory module of claim 1, wherein the circuit is configurable to receive a row/column address signal of the set of input signals and to use the row/column address signal to translate between the system memory domain and the physical memory domain.

25. The memory module of claim 24, wherein the row/ column address signal is a row address bit and the circuit is configurable to latch the row address bit.

26. The memory module of claim 24, wherein the row/ column address signal is a row address bit and the circuit is configurable to use the row address bit and a first number of chip-select signals of the set of input signals to generate a second number of chip-select signals greater than the first number of chip-select signals.

27. The memory module of claim 24, wherein the row/ column address signal is a row address bit and the circuit is configurable to use the row address bit and a first number of column address strobe (CAS) signals to generate a second number of CAS signals greater than the first number of CAS signals.

28. A method of using a memory module with a computer system, the method comprising:

providing a memory module having a plurality of dual data-rate (DDR) memory devices arranged in one or more ranks and a circuit electrically coupled to the plurality of DDR memory devices, the circuit comprising a logic element, a register, and a phase-lock loop device, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register, the circuit configured to be electrically coupled to a computer system to receive a set of input signals from the computer system, the set of input signals comprising row/column address signals, bank address signals, and chip-select signals, the set of input signals compatible with a system memory domain of the computer system, each DDR memory device having a corresponding load;

electrically coupling the memory module to the computer system; and

activating the circuit in response to the set of input signals to selectively isolate at least one of the loads of the DDR memory devices from the computer system and to translate between the system memory domain of the computer system and a physical memory domain of the memory module, wherein the system memory domain has a first memory density per rank, and the physical memory domain has a second memory density per rank less than the first memory density per rank.

29. The method of claim 28, wherein the plurality of DDR memory devices comprises a first number of DDR memory devices and activating the circuit selectively isolates the loads of a second number of DDR memory devices from the computer system, the second number less than the first number.

30. The method of claim 29, wherein the first number of DDR memory devices are arranged in two or more ranks of DDR memory devices, and wherein the second number of DDR memory devices are arranged as one rank of the two or more ranks.

31. The method of claim 28, further comprising storing an address signal of the set of input signals during a row access procedure and passing the stored address signal as an address signal of a set of output signals during a subsequent column address procedure.

32. The method of claim 28, wherein the plurality of DDR memory devices comprises a pair of DDR memory devices, each DDR memory device of the pair having a first memory capacity, the pair of DDR memory devices configured to simulate a DDR memory device having a second memory capacity equal to twice the first memory capacity.

33. The method of claim 28, wherein two or more of the logic element, the register, and the phase-lock loop device are portions of a single component.

34. The method of claim 28, wherein upon said activation, the circuit is responsive to the set of input signals to selectively isolate a data signal line of a DDR memory device of the plurality of DDR memory devices from the computer system. 44

35. The method of claim 28, wherein upon said activation, the circuit uses a row/column address signal of the set of input signals to translate between the system memory domain and the physical memory domain.

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36. The method of claim 35, wherein the row/column address signal is a row address bit and the circuit latches the row address bit.

37. The method of claim 35, wherein the row/column address signal is a row address bit and the circuit uses the row address bit and a first number of chip-select signals of the set of input signals to generate a second number of chip-select signals greater than the first number of chip-select signals.

38. The method of claim 35, wherein the row/column address signal is a row address bit and the circuit uses the row address bit and a first number of column address strobe (CAS) signals to generate a second number of CAS signals greater than the first number of CAS signals.

39. A memory module connectable to a computer system, the memory module comprising:

a first dual-data-rate (DDR) memory device having a first data signal line and a first data strobe signal line;

a second DDR memory device having a second data signal line and a second data strobe signal line;

a common data signal line connectable to the computer system; and

a circuit comprising a logic element, a register, and a phaselock loop device operationally coupled to the first DDR memory device, the second DDR memory device, the logic element, and the register, the circuit configured to be electrically coupled to a memory controller of a computer system to receive a set of input signals from the computer system, the set of input signals comprising row address signals, column address signals, bank address signals, and chip-select signals, the set of input signals compatible with a system memory domain of the computer system, the circuit electrically coupled to the first data signal line, to the second data signal line, and to the common data signal line, the circuit configurable to be responsive to the set of input signals by selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line, the circuit configurable to translate between the system memory domain of the computer system and a physical memory domain of the memory module, wherein the system memory domain has a first memory density per memory device,

and the physical memory domain has a second memory density per memory device less than the first memory density per memory device.

40. The memory module of claim 39, wherein the two or more of the logic element, the register, and the phase-lock loop device are portions of a single component.

41. The memory module of claim 40, wherein the circuit further comprises one or more switches selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line, the one or more switches operatively coupled to the logic element to receive control signals from the logic element.

42. The memory module of claim 39, wherein the logic element is selected from the group consisting of: an application-specific integrated circuit, a custom-programmable logic device, and a field-programmable gate array.

43. The memory module of claim 39, wherein the register comprises a plurality of register devices.

44. The memory module of claim 39, wherein the circuit is configurable to translate address signals in the system memory domain to address signals in the physical memory domain.

45. The memory module of claim 39, wherein the system memory domain is compatible with a first number of chip select signals, and the physical memory domain is compatible with a second number of chip select signals greater than the first number of chip select signals.

46. The memory module of claim 45, wherein the second number of chip select signals is equal to twice the first number of chip select signals.

47. The memory module of claim 39, wherein the memory module further comprises a third data strobe signal line connectable to the computer system, the circuit electrically coupled to the first data strobe signal line, to the second data strobe signal line, and to the third data strobe signal line, the circuit selectively electrically coupling the first data strobe signal line to the third data strobe signal line and selectively electrically coupling the second data strobe signal line to the third data strobe signal line.

48. The memory module of claim 39, wherein the circuit is configurable to transmit a set of output signals to at least one of the first and second DDR memory devices, the set of output signals compatible with the physical memory domain.

49. The memory module of claim 48, wherein the set of input signals comprises a command signal and the set of output signals comprises the command signal.

50. The memory module of claim 48, wherein the circuit is configurable to receive a command signal from the computer system and transmit the command signal to the at least one of the first and second DDR memory devices.

51. The memory module of claim 48, wherein the set of output signals comprises row address signals, column address signals, bank address signals, and chip-select signals.

52. The memory module of claim 48, wherein the set of input signals comprises a first set of address and command signals and the set of output signals comprises a second set of address and command signals.

53. The memory module of claim 52, wherein the circuit is configurable to save an address signal of the set of input signals during a row access procedure and pass the saved address signal as an address signal of the set of output signals during a subsequent column address procedure.

54. The memory module of claim 39, wherein the circuit is configurable to be responsive to the set of input signals by selectively electrically coupling both the first data signal line and the second data signal line to the computer system.

55. The memory module of claim 39, wherein the circuit is configurable to selectively isolate both the first data signal line and the second data signal line from the computer system.

56. A memory module comprising:

a plurality of double-data-rate (DDR) memory devices arranged in one or more ranks, each DDR memory device having a corresponding load; and

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a circuit comprising a logic element, a register, and a phase lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the circuit electrically coupled to the plurality of DDR memory devices and configured to be electrically coupled to a memory controller of a computer system to receive a set of input signals from the computer system, the set of input signals comprising row/column address signals, bank address signals, and chip-select signals, the set of input signals compatible with a system memory domain of the computer system, the circuit configurable to be responsive to the set of input signals by selectively isolating one or more of the loads of the DDR memory devices from the computer system, the circuit configurable to translate between the system memory domain of the computer system and a physical memory domain of the memory module, wherein the system memory domain is compatible with a first number of chip-select signals, and the physical memory domain is compatible with a second number of chip select signals greater than the first number of chip-select signals.

57. The memory module of claim 56, wherein the circuit comprises one or more switches operatively coupled to the logic element to receive control signals from the logic element.

58. The memory module of claim 56, wherein the plurality of DDR memory devices has a first number of DDR memory devices, and the circuit is configurable to selectively isolate the loads of a second number of the DDR memory devices from the computer system, the second number less than the first number.

59. The memory module of claim 58, wherein the first number of DDR memory devices are configured in a plurality of ranks, and wherein the second number of DDR memory devices are configured as one rank of the plurality of ranks.

60. The memory module of claim 56, wherein the second number of chip-select signals is equal to twice the first number of chip-select signals. The memory module of claim 56, wherein the circuit comprises a data path multiplexer/demultiplexer which isolates the ranks of DDR memory devices from one another.

61. The memory module of claim 56, wherein the circuit comprises a data path multiplexer/demultiplexer which isolates the ranks of DDR memory devices from one another.

62. The memory module of claim 56, wherein the plurality of DDR memory devices comprises a pair of DDR memory devices, each DDR memory device of the pair having a first memory capacity, the pair of DDR memory devices configured to simulate a DDR memory device having a second memory capacity greater than the first memory capacity.

63. The memory module of claim 56, wherein two or more of the logic element, the register, and the phase-lock loop device are portions of a single component.

64. The memory module of claim 56, wherein the memory module comprises a registered dual inline memory module.

65. The memory module of claim 56, wherein the plurality of DDR memory devices comprises DDR3 synchronous dynamic random-access memory (SDRAM) devices.

66. The memory module of claim 56, further comprising a printed circuit board configured to be electrically coupled to the memory controller, the circuit mounted on the printed circuit board, the plurality of DDR memory devices mounted on the printed circuit board as a first set of DDR memory so devices on a first side of the printed circuit board, a second set of DDR memory devices on the first side of the printed circuit board, a third set of DDR memory devices on a second side of the printed circuit board, and a fourth set of DDR memory devices on the second side of the printed circuit board, the DDR memory devices of the second set spaced from the DDR memory devices of the first set, the DDR memory devices of the fourth set spaced from the DDR memory devices of the third set.

67. The memory module of claim 56, wherein the circuit is configurable to receive a command signal from the computer system, select at least one rank of the one or more ranks, and transmit the command signal to at least one DDR memory device of the selected rank of DDR memory devices.

68. The memory module of claim 56, wherein the set of input signals comprises a first set of address and command signals and the set of output signals comprises a second set of address and command signals, wherein the circuit is configurable to store an address signal of the set of input signals

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during a row access procedure and pass the stored address signal as an address signal of the set of output signals during a subsequent column address procedure.

69. The memory module of claim 56, wherein the circuit is configurable to selectively isolate a data signal line of a DDR memory device of the plurality of DDR memory devices from the computer system.

70. The memory module of claim 56, wherein the circuit is configurable to receive a row/column address signal of the set of input signals and to use the row/column address signal to translate between the system memory domain and the physical memory domain.

71. The memory module of claim 70, wherein the row/ column address signal is a row address bit and the circuit is configurable to latch the row address bit.

72. The memory module of claim 70, wherein the row/ column address signal is a row address bit and the circuit is configurable to use the row address bit and a first number of chip-select signals of the set of input signals to generate a second number of chip-select signals greater than the first number of chip-select signals.

73. The memory module of claim 70, wherein the row/ column address signal is a row address bit and the circuit is configurable to use the row address bit and a first number of column address strobe (CAS) signals to generate a second number of CAS signals greater than the first number of CAS signals.

74. A method of using a memory module with a computer system, the method comprising:

providing a memory module having a plurality of dual data-rate (DDR) memory devices arranged in one or more ranks and a circuit electrically coupled to the plurality of DDR memory devices, the circuit comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the circuit configured to be electrically coupled to a computer system to receive a set of input signals from the computer system, the set of input signals comprising row/column address signals, bank address signals, and chip-select signals, the set of input signals compatible with a system memory domain of the

computer system, each DDR memory device having a corresponding load;

electrically coupling the memory module to the computer system; and

activating the circuit in response to the set of input signals to selectively isolate at least one of the loads of the DDR memory devices from the computer system and to translate between the system memory domain of the computer system and a physical memory domain of the memory module, wherein the system memory domain is compatible with a first number of chip-select signals, and the physical memory domain is compatible with a second number of chip-select signals greater than the first number of chip-select signals.

75. The method of claim 74, wherein the plurality of DDR memory devices comprises a first number of DDR memory devices and activating the circuit selectively isolates the loads of a second number of DDR memory devices from the computer system, the second number less than the first number.

76. The method of claim 75, wherein the first number of DDR memory devices are arranged in two or more ranks of DDR memory devices, and wherein the second number of DDR memory devices are arranged as one rank of the two or more ranks.

77. The method of claim 74, further comprising storing an address signal of the set of input signals during a row access procedure and passing the stored address signal as an address signal of a set of output signals during a subsequent column address procedure.

78. The method of claim 74, wherein two or more of the logic element, the register, and the phase-lock loop device are portions of a single component.

79. The method of claim 70, wherein upon said activation, the circuit is responsive to the set of input signals to selectively isolate a data signal line of a DDR memory device of the plurality of DDR memory devices from the computer system.

80. The method of claim 74, wherein upon said activation, the circuit uses a row/column address signal of the set of input signals to translate between the system memory domain and the physical memory domain.

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81. The method of claim 80, wherein the row/column address signal is a row address bit and the circuit latches the row address bit.

82. The method of claim 80, wherein the row/column address signal is a row address bit and the circuit uses the row address bit and a first number of chip-select signals of the set of input signals to generate a second number of chip-select signals greater than the first number of chip-select signals.

83. The method of claim 80, wherein the row/column address signal is a row address bit and the circuit uses the row address bit and a first number of column address strobe (CAS) signals to generate a second number of CAS signals greater than the first number of CAS signals.

84. A memory module connectable to a computer system, the memory module comprising:

a first dual-data-rate (DDR) memory device having a first data signal line and a first data strobe signal line; a second DDR memory device having a second data signal line and a second data strobe signal line;

a common data signal line connectable to the computer system; and

a circuit comprising a logic element, a register, and a phase lock loop device operationally coupled to the first DDR memory device, the second DDR memory device, the logic element, and the register, the circuit configured to be electrically coupled to a memory controller of a computer system to receive a set of input signals from the computer system, the set of input signals comprising row/column address signals, bank address signals, and a first number of chip-select signals, the set of input signals compatible with a system memory domain of the computer system, the circuit electrically coupled to the first data signal line, to the second data signal line, and to the common data signal line, the circuit configurable to be responsive to the set of input signals by selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line, the circuit configurable to translate between the system memory domain of the computer system and a physical memory domain of the memory module, wherein the system memory domain is compatible with the first number of chip-select signals, and the physical memory domain is compatible with a

second number of chip-select signals greater than the first number of chip select signals.

85. The memory module of claim 84, wherein two or more of the logic element, the register, and the phase-lock loop device are portions of a single component.

86. The memory module of claim 84, wherein the circuit further comprises one or more switches selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line, the one or more switches operatively coupled to the logic element to receive control signals from the logic element.

87. The memory module of claim 84, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, or a programmable-logic device.

88. The memory module of claim 84, wherein the second number of chip-select signals is equal to twice the first number of chip-select signals.

89. The memory module of claim 84, wherein the memory module further comprises a third data strobe signal line connectable to the computer system, the circuit electrically coupled to the first data strobe signal line, to the second data strobe signal line, and to the third data strobe signal line, the circuit selectively electrically coupling the first data strobe signal line to the third data strobe signal line and selectively electrically coupling the second data strobe signal line to the third data strobe signal line.

90. The memory module of claim 84, wherein the circuit is configurable to transmit a set of output signals to at least one of the first and second DDR memory devices, the set of output signals comprising row/column address signals, bank address signals, and the second number chip-select signals, the set of output signals compatible with the physical memory domain.

91. The memory module of claim 90, wherein the set of input signals comprises a command signal and the set of output signals comprises the command signal.

92. The memory module of claim 90, wherein the circuit is configurable to receive a command signal from the computer system and transmit the

command signal to the at least one of the first and second DDR memory devices.

93. The memory module of claim 90, wherein the circuit is configurable to save an address signal of the set of input signals during a row access procedure and pass the saved address signal as an address signal of the set of output signals during a subsequent column address procedure.

94. The memory module of claim 84, wherein the circuit is configurable to be responsive to the set of input signals by selectively electrically coupling both the first data signal line and the second data signal line to the computer system.

95. The memory module of claim 84, wherein the circuit is configurable to selectively isolate both the first data signal line and the second data signal line from the computer system.

96. A circuit configured to be mounted on a memory module so as to be electrically coupled to a plurality of double data-rate (DDR) memory devices arranged in one or more ranks on the memory module, the memory module configured to be electrically coupled to a memory controller of a computer system so as to receive a set of input signals from the computer system, the set of input signals comprising row/ column address signals, bank address signals, and chip-select signals, the set of input signals compatible with a system memory domain of the computer system, the circuit comprising:

a logic element;

a register;

a phase-lock loop device configured to be operationally coupled to the plurality of DDR memory devices, the logic element and the register,

wherein the circuit is configurable to be responsive to the set of input signals by selectively isolating one or more loads of the DDR memory devices from the computer system, the circuit configurable to translate between the system memory domain of the computer system and a physical memory domain of the plurality of DDR memory devices, wherein the system memory domain has a first memory density per rank and the physical memory domain has a second memory density per rank less than the first memory density per rank.

97. The circuit of claim 96, wherein two or more of the phase-lock loop device, the logic element, and the register are portions of a single component.

13. Application No. 12/629,827 (150 Patent)

95. While the 274 Patent (discussed above) was pending, the applicants filed a continuation application (No. 12/629,827) on December 2, 2009, which resulted in U.S. Patent No. 7,881,150. EX1001 at p. 2; EX1039. Claims 15-17, 22, 24, 26, and 31-33 of the 150 Patent, reproduced below, were then subject to *inter partes* review and cancelled. EX1040-EX1043.

15. A circuit configured to be mounted on a memory module so as to be electrically coupled to a first double-data-rate (DDR) memory device having a first data signal line and a first data strobe line, to a second DDR memory device having a second data signal line and a second data strobe line, and to a common data signal line, the memory module configured to be electrically coupled to a memory controller of a computer system so as to receive a set of input signals comprising row address signals, column address signals, bank address signals, and chip-select signals, the set of input signals compatible with a system memory domain of the computer system, the circuit comprising:

a logic element;

a register;

a phase-lock loop device configured to be operationally coupled to the first DDR memory device, the second DDR memory device, the logic element, and the register,

wherein the circuit is configurable to be responsive to the set of input signals by selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line, the circuit configurable to translate between the system memory domain of the computer system and a physical memory domain of the memory module, wherein the system

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memory domain has a first memory density per memory device, and the physical memory domain has a second memory density per memory device less than the first memory density per memory device.

16. The circuit of claim 15, wherein the two or more of the logic element, the register, and the phase-lock loop device are portions of a single component.

17. The circuit of claim 16, further comprising one or more switches selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line, the one or more switches operatively coupled to the logic element to receive control signals from the logic element.

…

22. A circuit configured to be mounted on a memory module so as to be electrically coupled to a plurality of double-data-rate (DDR) memory devices arranged in one or more ranks on the memory module, the memory module configured to be electrically coupled to a memory controller of a computer system so as to receive a set of input signals, comprising row address signals, column address signals, bank address signals, and chip-select signals, the set of input signals compatible with a system memory domain of the computer system, the circuit comprising:

a logic element;

a register;

a phase-lock loop device configured to be operationally coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the circuit is configurable to be responsive to the set of input signals by selectively isolating one or more loads of the DDR memory devices from the computer system, the circuit configurable to translate between the system memory domain of the computer system and a physical memory domain of the plurality of DDR memory devices, wherein the system memory domain is compatible with a first number of chip-select signals, and the physical memory domain is compatible with a second number of chip-select signals greater than the first number of chip-select signals.

…

24. The circuit of claim 22, wherein two or more of the logic element, the register, and the phase-lock loop device are portions of a single component.

…

26. The circuit of claim 22, further configurable to selectively isolate a data signal line of a DDR memory device of the plurality of DDR memory devices from the computer system.

…

31. A circuit configured to be mounted on a memory module so as to be electrically coupled to a first double-data-rate (DDR) memory device having a first data signal line and a first data strobe line, to a second DDR memory device having a second data signal line and a second data strobe line, and to a common data signal line, the memory module configured to be electrically coupled to a memory controller of a computer system so as to receive a set of input signals comprising row address signals, column address signals, bank address signals, and chip-select signals, the set of input signals compatible with a system memory domain of the computer system, the circuit comprising:

a logic element;

a register;

a phase-lock loop device configured to be operationally coupled to the first DDR memory device, the second DDR memory device, the logic element, and the register,

wherein the circuit is configurable to be responsive to the set of input signals by selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line, the circuit configurable to translate between the system memory domain of the computer system and a physical memory domain of the memory module, wherein the system memory domain is compatible with a first number of chip-select signals, and the physical memory domain is compatible with a second number of chip-select signals greater than the first number of chip-select signals.

32. The circuit of claim 31, wherein two or more of the logic element, the register, and the phase-lock loop device are portions of a single component.

33. The circuit of claim 31, further comprising one or more switches configurable to selectively electrically couple the first data signal line to the common data signal line and to selectively electrically couple the second data signal line to the common data signal line, the one or more switches operatively coupled to the logic element to receive control signals from the logic element.

14. Application No. 12/955,711 (574 Patent)

96. While the 150 Patent (discussed above) was pending, the applicants filed continuation application 12/955,711 on November 29, 2010, which resulted in U.S. Patent No. 7,916,574. EX1001 at p. 2; EX1045.

97. On February 2, 2011, the Office issued a Notice of Allowance for the application for the 574 Patent. EX1044 at pp. 128-131. The Examiner made two minor corrections in an Examiner's Amendment but made no statement of reasons for allowance. EX1044 at pp. 135-146.

98. U.S. Patent No. 7,916,574 was issued from the 711 Application on March 29, 2011. EX1044 at pp. 199; EX1045.

15. Application No. 13/032,470 (536 Patent)

99. While the 574 Patent (discussed above) was pending, the applicants filed continuation application 13/032,470 on February 22, 2011, which resulted in U.S. Patent No. 8,081,536. EX1001 at p. 2; EX1046. Claims 1, 16, 17, 24, 30, and 31 of the 536 Patent, reproduced below, were then subject to *inter partes* review and cancelled. EX1047-EX1049.

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1. A circuit configured to be mounted on a memory module configured to be operationally coupled to a computer system, the memory module having a first number of ranks, each rank of the first number of ranks comprising a plurality of double data-rate (DDR) memory circuits that are configured to be activated concurrently with one another for receiving and transmitting data having a bit width of the rank in response at least in part to a first number of DDR chip-select signals, the circuit including at least one configuration in which the circuit is configured to:

receive a set of signals comprising address signals and a second number of DDR chip-select signals smaller than the first number of DDR chip-select signals:

generate phase-locked clock signals and transmit the phase-locked clock signals to the DDR memory circuits of the first number of ranks;

selectively isolate a load of the DDR memory circuits of at least one rank of the first number of ranks from the computer system in response at least in part to the set of signals; and

generate the first number of DDR chip-select signals in response at least in part to the phase-locked clock signals, the address signals, and the second number of DDR chip-select signals.

…

16. The circuit of claim 1, wherein the memory module has attributes and the circuit in the at least one configuration is further configured to store data accessible to the computer system, wherein the data characterizes the memory module as having attributes that are different from the attributes of the memory module.

17. The circuit of claim 16, wherein the attributes are selected from a group consisting of a number of row addresses, a number of column addresses, a number of DDR memory circuits, a data width of the DDR memory circuits, a memory density per DDR memory circuit, a number of ranks, and a memory density per rank.

…

24. A method of operating a memory module configured to be operationally coupled to a computer system, the memory module having a

first number of ranks, each rank of the first number of ranks comprising a plurality of double-data-rate (DDR) memory circuits that are configured to be activated concurrently with one another for receiving and transmitting data having a bit width of the rank in response at least in part to a first number of DDR chip-select signals, the method comprising:

receiving a set of signals comprising address signals and a second number of DDR chip-select signals smaller than the first number of DDR chip-select signals:

using the memory module to generate phase-locked clock signals and transmitting the phase-locked clock signals to the DDR memory circuits of the first number of ranks:

selectively isolating a load of the DDR memory circuits of at least one rank of the first number of ranks from the computer system in response at least in part to the set of signals; and

generating the first number of DDR chip-select signals in response at least in part to the phase-locked clock signals, the address signals, and the second number of DDR chip-select signals.

…

30. The method of claim 24, wherein the memory module has attributes and the method further comprises storing data accessible to the computer system, wherein the data characterizes the memory module as having attributes that are different from the attributes of the memory module.

31. The method of claim 30, wherein the attributes are selected from a group consisting of a number of row addresses, a number of column addresses, a number of DDR memory circuits, a data width of the DDR memory circuits, a memory density per DDR memory circuit, a number of ranks, and a memory density per rank.

16. Application No. 13/287,081 (188 Patent)

100. While the 536 Patent (discussed above) was pending, the applicants filed continuation application 13/287,081 on November 1, 2011. EX1001 at p. 2.

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101. On April 8, 2013, the Office issued a Notice of Allowance for the 13/287,081 application. EX1050 at pp. 139-154. The Examiner allowed Claims 2-21 with minor amendments made to Claim 7, Claim 18, Claim 19, and Claim 21. *Id.* at p. 145. Claim 1 had previously been cancelled. *Id.*

102. On April 16, 2013, the Applicant and the Examiner engaged in an Applicant-Initiated Interview to correct the paperwork to reflect the correct Examiner's Amendment, the corresponding allowable subject matter, and the closest art of record. *Id.* at p. 185.

103. On April 25, 2013, the Office issued a Supplemental Notice of Allowability. *Id.* at pp. 184, 187.

104. On August 20, 2013, U.S. Patent No. 8,516,188 issued from the 081 Application. *Id.* at p. 207; EX1050.

17. Application No. 13/971,231 (774 Patent)

105. While the 188 Patent (discussed above) was pending, the applicants filed continuation application 13/971,231 on August 20, 2013, which resulted in U.S. Patent No. 9,037,774. EX1001 at p. 1; EX1053.

106. A non-final office action was mailed May 20, 2014, rejecting Claims 1-10 on the ground of nonstatutory double patenting as being unpatentable over Claim 1, Claim 6, and Claim 8 of copending Application No. 13/287,042. EX1052 at pp. 175-179. Claims 1-10 were also rejected as obvious in view of U.S. Patent

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Application Publication Nos. 2003/0070052 ("Lai") and 2004/0098528 ("Janzen"). *Id.* at pp. 179-182.

107. Applicants filed an amendment on November 20, 2014, cancelling Claims 1-10 and adding new claims 11-30. *Id.* at pp. 211-220. The applicants distinguished the prior art with the arguments below. *Id.* at pp. 221-24.

IV. REJECTION OF CLAIMS 1-10 UNDER PRE-AIA 35 U.S.C. 103(A) AS BEING UNPATENTABLE OVER LAI, IN VIEW OF JANZEN

New claims 11-30 are presented to replace original claims 1-10, which are cancelled. New claim 11 recites a memory module comprising a plurality of memory devices including a first set of memory devices and a second set of memory devices and a register device to

receive from the memory controller a first set of input C/A signals associated with a first memory command via the C/A bus and subsequently a second set of input control/address signals associated with a second memory command via the C/A bus, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst.

New claim 11 then requires the register to generate a first set of output C/A signals in response to the first set of input C/A signals and a second set of output C/A signals in response to the second set of input C/A signals, the first set of output C/A signals causing the first set of memory devices to receive or output the first data burst, the second set of output C/A signals causing the second set of memory devices to receive or output the second data burst.

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New claim 11 further requires a circuit coupled between the data bus and the plurality of memory devices. The circuit is coupled to the first set of memory devices via a first set of module DQ and DQS signal lines and to the second set of memory devices via a second set of module DQ and DQS signal lines. New claim 11 further requires the circuit to respond to the first memory command by coupling the first set of module DQ and DQS signal lines to respective DQ and DQS signal lines of the data bus and by isolating the second set of module DQ and DQS signal lines from the data bus as the memory module is receiving or outputting the first data burst in response to the first memory command (*emphasis added*). New claim 11 then requires the circuit to respond to the second memory command by coupling the second set of module DQ and DQS signal lines to respective DQ and DQS signal lines of the data bus and by isolating the first set of module DQ and DQS signal lines from the data bus as the memory module is receiving or outputting the second data burst in response to the second memory command (*emphasis added*).

The above features of new claim 11 are not disclosed or taught by Lai in view of Janzen. In Lai, the buffer chip 108 or FET switch circuit 118 does not isolate either one of the two memory banks 104 and 106 from the data bus in response to a memory command. Instead, the buffer chip 108 comprises "a plurality of first-in first-out (FIFO) buffers" to "double the data rate for reading and writing" of each of the two memory banks 104 and 106, which are of DDR SDRAM structure (Lai, paragraph [0035]). Similarly, the FET switches 118 is "to double the transmission rate of the first data selection signal (DQSA) and the data selection (*sic*) signal (MDA) of the first memory bank 114" and the second memory bank 116 (Lai, paragraph [0039]).

Nowhere in Lai it is mentioned that the buffer chip 108 or FET switch circuit 118 chooses which of the two memory banks 104 and 106 to connect to the memory bus, or which of the two memory banks 104 and 106 to isolate from the memory bus, based on a memory command. Instead, the buffer chip may lock data of the memory data signal MD and transmit the respective data units in the data signal MD to the two memory banks 104, 106 respectively according to data selection signal (DQS) and the data mask signal (DQM)" (Lai, FIG. 5; paragraph [0038]). Neither of the data selection signal (DQS) and the data mask signal (DQM) constitutes a memory command, which, according to the Specification of the instant application and to the common understanding of DDR memory operations, involves a number of command signals that define memory operations such as read, write, refresh, precharge, and other operations (Specification, Table 1 and Table 2).

Lai also does not isolate either one of the two memory banks 104 and 106 as the memory module is receiving or outputting a data burst in response a memory command. In fact, to make the memory module of Lai receive or output data units at quad data rate, Lai requires both memory banks be activated by the chip select signal (0,1) at the same time (Lai, FIGS. 4, 5, 7, and 8, showing chip select signal (0,1) being pulled low). Thus, for each memory command, Lai requires both of the two memory banks 104 and 106 to receive or output units of data, because otherwise the memory module in Lai with the double data rate memory banks 104, 106 would not be able to receive or output a quad data rate data signal (MD).

Thus, during a read operation, the buffer chip 108 or FET switch circuit 118 interleaves units of data from the two memory banks 104, 106 and outputs the read data MD onto the data bus at twice the frequency as each of the two memory banks 104 and 106 outputs read data MDA and MDB, respectively (Lai, FIGS. 4 and 7; paragraphs [0037] and [0039]). As stated in Lai, the "signals between the memory controller 102 and buffer chip 108 operate and *(sic)* four times faster than a baseline rate." "Therefore, four units of data are capable of being transmitted within one memory clock cycle" (Lai, paragraph [0036]). Note that the memory banks 104, 106 are of the DDR SDRAM structure (paragraph [0035]), so each of the memory banks 104, 106 can only transmit two units of data per memory clock cycle. Therefore, for each read command, both of the two memory banks 104, 106 need to

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feed data units to the buffer chip 108 or FET switch circuit 118. Thus, unlike what is claimed in new claim 11, neither of the memory banks 104, 106 can be isolated from the memory bus as the memory module of Lai is outputting read data MD onto the data bus.

During a write operation, the buffer chip may lock data of the memory data signal MD and transmit the respective data units in the data signal MD to the two memory banks 104, 106 respectively according to data selection signal (DQS) and the data mask signal (DQM" (Lai, FIG. 5; paragraph [0038]). As discussed above, the memory data signal has four units of data per memory cycle while each of the memory banks 104, 106 can only receive two units of data per memory cycle. Thus, if only one of the memory banks 104, 106 is receiving the memory data signal MD, half of the data units in the memory data signal would be lost. Therefore, unlike what is claimed in claim 11, neither of the memory banks 104, 106 can be isolated from the memory bus as the memory module in Lai is receiving the memory data signal MD.

Since Janzen does not make up for the above deficiencies of Lai, new claim 11 is patentable over Lai in view of Janzen.

New claims 12-20 depend from new claim 11 and include further limitations in addition to the limitations in new claim 11. Therefore, new claims 12-20 are patentable for at least the same reasons new claim 11 is patentable.

The above arguments with regard to new claim 11 apply to new claim 21. Therefore, new claim 21 is also patentable.

New claims 22-30 depend from new claim 21 and include further limitations in addition to the limitations in new claim 21. Therefore, new claims 22-30 are patentable for at least the same reasons new claim 21 is patentable.

108. A notice of allowance was mailed on January 9, 2015. *Id.* at pp. 250-254.

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109. Applicants filed a request for continued examination on March 23, 2015. *Id.* at pp. 275-276. Applicants amended the specification and amended draft claims 11, 13, and 23. *Id.* at 278-288.

110. A notice of allowance was mailed on April 2, 2015. *Id.* at pp. 306-310.

111. On May 19, 2015, U.S. Patent No. 9,037,774 was issued from the 231 Application. *Id.* at p. 353; EX1053.

18. Application No. 14/715,486 (215 Patent)

112. While the 774 Patent (discussed above) was pending, the applicants filed continuation application 14/715,486 on May 18, 2015, which resulted in the 215 Patent. EX1001 at p. 1. The Applicants originally filed 21 claims. EX1002 at pp. 60-65.

113. A notice of allowance was mailed on May 11, 2017 following an examiner's interview and examiner's amendments. *Id.* at pp. 275-295. The examiner's amendments altered several claims, cancelled Claims 19-21 and added new Claims 22-29. EX1002 at pp. 283-292.

114. On August 11, 2017, the applicants filed a Request for Continued Examination, amending several claims, cancelling claims 10 and 18 and adding five new claims, Claims 30-34. EX1002 at pp. 385-398.

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115. A second Notice of Allowance was mailed on August 22, 2017, including another examiner's amendment further amending the specification and claims following another examiner's interview. EX1002 at pp. 412-436.

116. On November 22, 2017, a Corrected Notice of Allowability was mailed. EX1002 at p. 515. The patent issued as U.S. Patent No. 9,858,215 on December 13, 2017. EX1002 at p. 530; EX1001. At time of issuance, the patent included 29 claims. EX1002 at p. 515. As explained below, in my opinion the claims of the 215 Patent are obvious in light of the prior art.

19. Application No. 15/857,519 (314 Patent)

117. While the 215 Patent (discussed above) was pending, the applicants filed continuation application 15/857,519 on December 28, 2017, which resulted in U.S. Patent No. 10,489,314 on November 26, 2019. EX1054-EX1055. All claims of the 314 Patent are currently the subject of *inter partes* review. EX1056 at pp. 22, 50.

20. Application No. 16/695,020 (417 Patent)

118. While the 314 Patent (discussed above) was pending, the applicants filed continuation application 16/695,020 on November 25, 2019, which resulted in U.S. Patent No. 11,093,417 on August 17, 2021. EX1057-EX1058.

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119. In my opinion, the claims of the 417 Patent are obvious for substantially the same reasons that the claims of the 215 Patent are obvious, as discussed in a separate declaration by me addressing the claims of the 417 Patent.

21. Application No. 17/403,832

120. While the 417 Patent (discussed above) was pending, the applicants filed continuation application 17/403,832 on August 16, 2021. EX1059. A non-final rejection of all pending claims was issued on September 2, 2022, based on anticipation in light of Matsui (EX1072) ("Matsui1"). EX1059 at pp. 245-53.

E. Construction of Terms Used in the 215 Patent Claims

121. I understand that in an *inter partes* review proceeding the claims of the patent are to be given their ordinary and customary meaning in view of the specification and file history (i.e., the meaning that the term in question would have to a Skilled Artisan).

122. I also understand that where a patent application provides an explicit definition of a claim term in the specification that definition may control the interpretation of that term in the claim.

123. I also understand that if no explicit definition is given to a term in the patent specification, the claim terms must be evaluated using the ordinary meaning of the words being used in those claims, evaluated from the perspective of a Skilled Artisan.

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1. "rank"

124. The term "rank" appears in claims 1, 14, 21, and 26 of the 215 Patent. Claims 1 and 14 are reproduced below as an example, with the term "rank" emphasized:

> 1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising:
>
> a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;
>
> a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command;
>
> a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of **ranks** including a first **rank** and a second **rank**, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first **rank** and at least one second memory integrated circuit in the second **rank**, wherein the first **rank** is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second **rank** is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command;

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> a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus; and
>
> logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.
>
> …
>
> 14. The memory module of claim 1, wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first **rank** or the second **rank** is selected to communicate data with the memory controller.

EX1001 at 37:13-62, 39:24-28 (emphasis added).

125. The 215 Patent states, "DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width." EX1001 at 2:41-43. "During operation, the ranks of a memory module are selected or activated by address and command signals that are received from the processor. Examples of such address and command signals include, but are not limited to, rank-select signals, also called chip-select signals." *Id.* at 2:59-63.

126. In my opinion, a Skilled Artisan would have understood that the term "rank" refers to an independent set of one or more memory devices on a memory

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module that act together in response to command signals, including chip select signals, to read or write the full bit-width of the memory module.

127. This construction of the term "rank" is consistent with the 215 Patent's disclosure, including the above-discussed claim language (e.g., "including **at least one first memory integrated circuit in the first rank** and **at least one second memory integrated circuit in the second rank**"), and the specification (e.g., "… **each rank** of memory generally **having a bit width**," EX1001 at 2:41-43, "the ranks of a memory module are selected or **activated by …** rank-select signals, also called **chip-select signals**," *id.* at 2:59-63.").

128. This construction is also consistent with how a Skilled Artisan would have understood the ordinary and customary meaning of the term "rank." *See, e.g.*, EX1070 (Memory Systems textbook) at p. 413 ("Essentially, a *rank* of memory is a '*bank*' of one or more DRAM devices that operate in lockstep in response to a given command." (emphases in original)); EX1064 (JESD79-2) at p. 6 ("**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code."); EX1062 (JESD21-C) at pp. 10-16 (showing modules with one or two ranks, called "physical banks" as discussed below, each rank receiving a respective chip select signal and having the full bit-width of the memory module).

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129. I note that, at the time of the 215 Patent, the terms "physical bank" and "bank" were more general terms that, depending on the context, could be used to refer to what is now more typically described as a "rank." For example, the term "bank" was used not only to refer to a memory array *within* a single memory device, but also to one or more memory devices on a memory module that act together in response to command signals, including chip select signals, to read or write the full bit-width of the memory module. Indeed, while the JESD79-2 standard dated September 2003 explained that a chip-select signal selects a "rank" as quoted above, the JESD79 standard originally published in June 2000 — which was still in use as of 2005 — used the term "bank" to mean exactly the same thing. *See* EX1060 (JESD79) at p. 7 ("Chip Select: All commands are masked when $\overline{S}$ is registered high. $\overline{S}$ provides for external bank selection on systems with multiple banks. $\overline{S}$ is considered part of the command code."). Similarly, the JESD21-C standard in 2002 used the term "physical bank" to refer to what is now more typically described as a "rank." *See, e.g.*, EX1062 (JESD21-C) at pp. 6 (describing "$\overline{S}$0-$\overline{S}$3 SDRAM chip select lines" to select "Physical. [sic] banks 0, 1, 2, and 3"), 10-16 (describing modules with one or two "physical banks" with a bit-width of 64 or 72 bits, each "physical bank" having a respective set of memory devices activated by a corresponding (registered) chip select signal $\overline{RS}$0 or $\overline{RS}$1). Similarly, in previous Final Written Decisions invalidating claims in the same

family as the 215 Patent, the Board has agreed that the "banks" in various prior art references correspond to the "ranks" claimed by Netlist. *See, e.g.*, EX1048 at pp. 13-14, 20, 28 (Final Written Decision invalidating claims of U.S. Patent No. 8,081,536, EX1046). Over time, the term "rank" became preferred over the more general term "bank," as explained by the following textbook on memory systems. But at the time of the 215 Patent, a Skilled Artisan would have understood that "bank" and "physical bank" could be used to mean the same thing as "rank" (given the "chip-select signal"):

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10.2.2 Rank

Figure 10.5 shows a memory system populated with 2 ranks of DRAM devices. Essentially, a *rank* of memory is a *"bank"* of one or more DRAM devices that operate in lockstep in response to a given command. However, the word *bank* has already been used to describe the number of independent DRAM arrays within a DRAM device. To lessen the confusion associated with overloading the nomenclature, the word *rank* is now used to denote a set of DRAM devices that operate in lockstep to respond to a given command in a memory system.

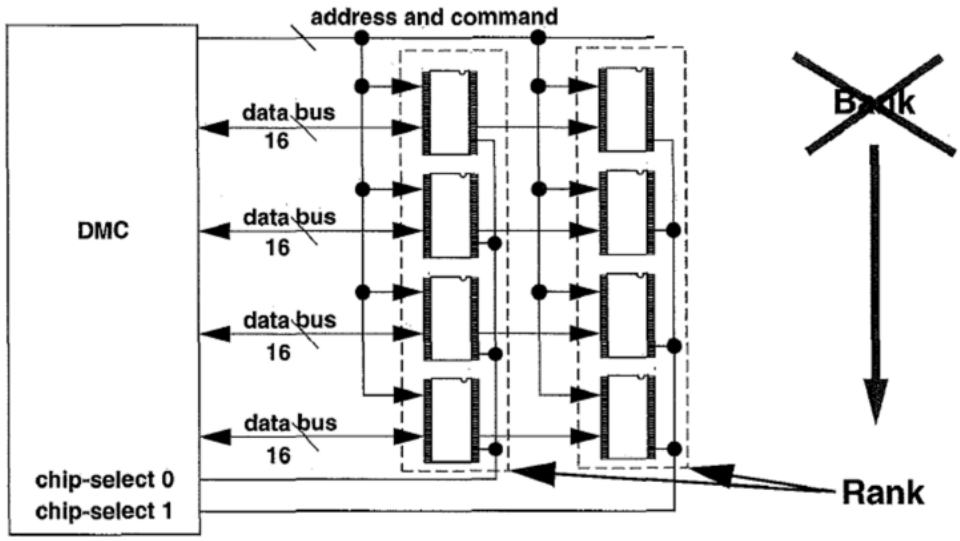

FIGURE 10.5: Memory system with 2 ranks of DRAM devices.

EX1070 (Memory Systems textbook) at p. 413; *see also* EX1069 (Synchronous DRAM Architectures paper) at pp. 4 n.3 (distinguishing between "rank" and a "bank" within a single DRAM), 9 ("Chip-select is used to enable ranks of DRAMs

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and thereby allow them to read commands off the bus and read/write data off/onto the bus.”).

130. As discussed above, a “rank” can be formed by “one or more DRAM devices.” EX1070 (Memory Systems textbook) at p. 413. For example, the 215 Patent describes an embodiment of a “rank” with one memory device:

> “[i]n certain embodiments, the command signal is passed through to the ***selected rank only*** (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to ***only one memory device*** or the other memory device so that data is supplied from ***one memory device*** at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices….”

EX1001 at 16:66-17:8 (emphasis added). A Skilled Artisan would have understood from this disclosure that, in such embodiments, each rank has only one memory device, because the command signal (e.g., read) is passed to the selected rank only, and this command signal is sent to only one memory device. In this embodiment, where there is only one memory device in the “rank,” the bit width of the “rank” would be the same as the bit width of the memory device, for example 16 bits. The 215 Patent explains that “memory devices…having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein.” *Id.* at 6:9-11.

131. I note that the Board has recently rejected an attempt by Netlist to construe “rank” in another member of the 215 Patent’s family to require multiple

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memory devices, concluding instead that the term "rank" may refer to only one memory device. *See* EX1023 at pp. 28-33; *see also supra* ¶90. I also note that the Board relied on the 215 Patent's disclosures in reaching this conclusion. *See* EX1023 at pp. 32-33. The Board's construction is consistent with the ordinary and customary meaning of the term "rank."

132. I also note that, in a Final Written Decision that the Board issued for the 536 Patent (a patent in the same family as the 215 Patent and to which the 215 Patent claims priority), the Board construed "rank" as "a block or area that is created using some or all of the memory chips on a memory module." EX1048 at p. 8 (internal quotation marks and citations omitted). I also understand that, in that proceeding the Board interpreted the claims "according to their broadest reasonable construction in light of the specification of the patent in which they appear[.]" *Id.* at p.7 (citations omitted). (I understand that the Board no longer applies the broadest reasonable construction, and instead construes the claims using the same claim construction standard that would be used in district court, including construing the claims in accordance with the ordinary and customary meaning of such claims as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.) I have been informed by counsel that the broadest reasonable interpretation of a claim is often — but is not necessarily — broader than the ordinary meaning. The ordinary meaning of "rank" (an

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independent set of one or more memory devices on a memory module that act together in response to command signals, including chip select signals, to read or write the full bit-width of the memory module) is narrower than what the Board previously found is the broadest reasonable interpretation of "rank" ("a block or area that is created using some or all of the memory chips on a memory module"). Accordingly, the ordinary meaning of "rank" is not inconsistent with the Board's previous construction of "rank" that applied the broadest reasonable interpretation. Regardless, as noted below, even if the Board were to apply its previous finding as to the broadest reasonable interpretation of "rank," the claims of the 215 Patent are still obvious in view of the prior art.

133. For purposes of my analysis below, I do not believe that any other terms contained in the claims of the 215 Patent require an explicit claim construction. While I understand that Patent Owner appears to have interpreted some of the claim terms broadly for purposes of infringement, *see, e.g.*, EX1085 at pp. 31-45; EX1088 at pp. 30-43, and that a narrower interpretation may be more reasonable, in my opinion the claims are obvious under either interpretation, as shown by my analysis below.

IV. OVERVIEW OF THE PRIOR ART

134. Below is an overview of the primary prior art references that I considered when analyzing the validity of the claims of the 215 Patent.

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A. Prior Art

1. U.S. Patent No. 7,363,422 to Perego ("Perego") (EX1071)

135. United States Patent No. 7,363,422 to Perego ("Perego") was filed January 28, 2004, published on September 23, 2004, and issued as a patent on April 22, 2008. EX1071. I therefore understand that Perego is prior art to the 215 Patent pursuant to at least 35 U.S.C. § 102(e) since it was filed before the earliest priority application. Since Perego was published in September of 2004, it is also prior art pursuant to § 102(a) assuming the 215 Patent is not entitled to a priority date earlier than July 1, 2005, which I believe to be the case, as discussed above. *See supra* ¶¶51-67.

136. Perego was not discussed during prosecution of the 215 Patent (*see generally* EX1002) and is not a reference cited in the 215 Patent (*see* EX1001 at pp. 1-3 (56)). Other patents related to Perego were listed with nearly 400 other references in an IDS filed by the Patent Owner (*see* EX1002 at pp. 120-136), but these were also not discussed during prosecution of the 215 Patent (*see* EX1001 at pp. 1-3 (56); *see also generally* EX1002).

137. Perego discloses a memory system, such as memory system 305, that includes a memory controller 310 connected to multiple buffered memory modules 330a-330n, such as memory module 340 (representing memory module 330a) that includes a buffer device (350, red) and multiple groups of memory devices (360,

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green and blue). *E.g.*, EX1071 at Abstract, FIG. 3B (reproduced below with annotations), 4:63-5:15.

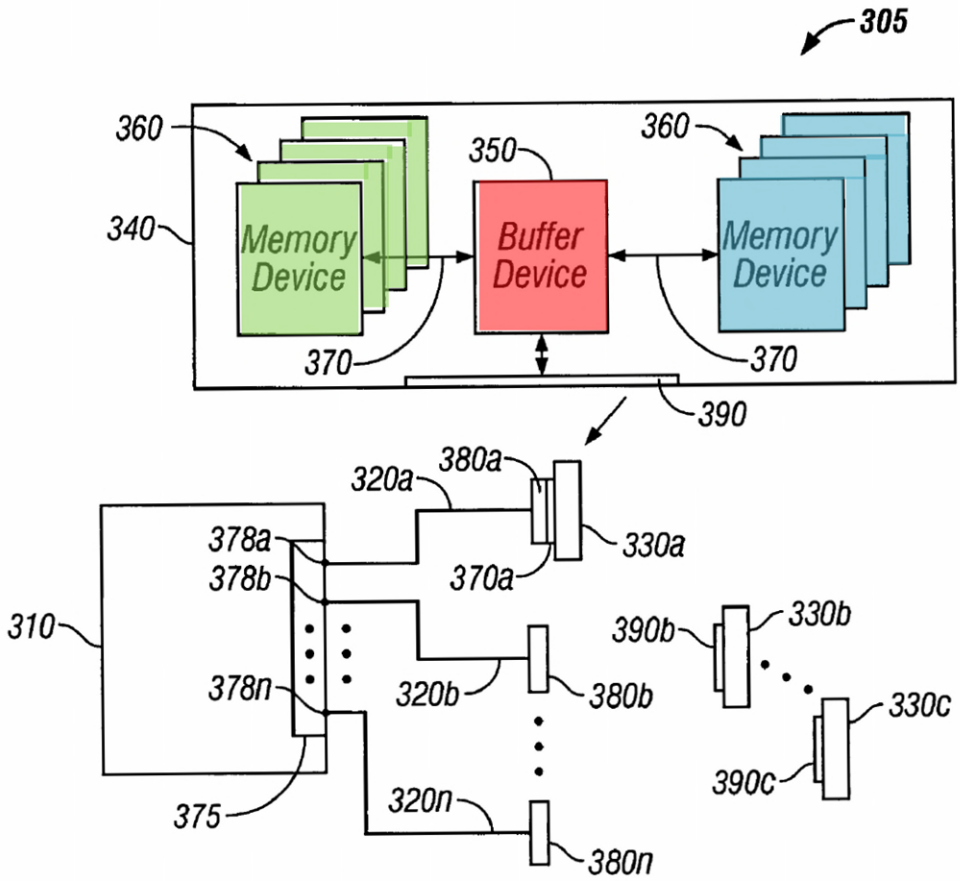

FIG. 3B

138. Furthermore, Perego's FIG. 3C shows an example of a configurable width buffered module 395 that includes a configurable width buffer device 391 (red) and memory devices 360 organized in groups (green, blue), and can be used in conjunction with the system described above. *Id.* at FIG. 3C (reproduced below with annotations).

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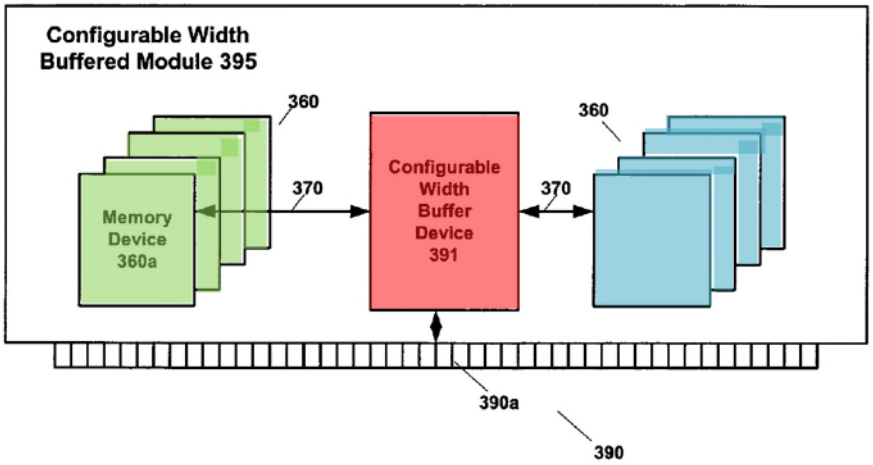

Fig. 3C

139. The purpose of Perego's invention was to fill the "need for memory system architectures or interconnect topologies that provide flexible and cost-effective upgrade capabilities while providing high bandwidth to keep pace with microprocessor operating frequencies." *Id.* at 2:26-29. Accordingly, Perego's

> "[b]uffer device 350 provides a high degree of system flexibility. New generations of memory devices may be phased in with controller 310 or into memory system 300 by modifying buffer device 350. Backward compatibility with existing generations of memory devices (i.e., memory devices 360) may also be preserved. Similarly, new generations of controllers may be phased in which exploit features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices."

Id. at 6:34-43.

140. Perego's FIG. 5B illustrates an implementation of "a configurable width buffer device 391 as seen in FIG. 3C[,]" which was shown above. *Id.* at 13:6-10, FIG. 5B (reproduced below with annotations). For example, the buffer

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device 391 includes interfaces 520a and 520b that are programmable to accommodate different numbers and types of memory devices, and also includes a configurable width interface 590 to communicate with the memory controller. *Id.* at 13:60-14:15.

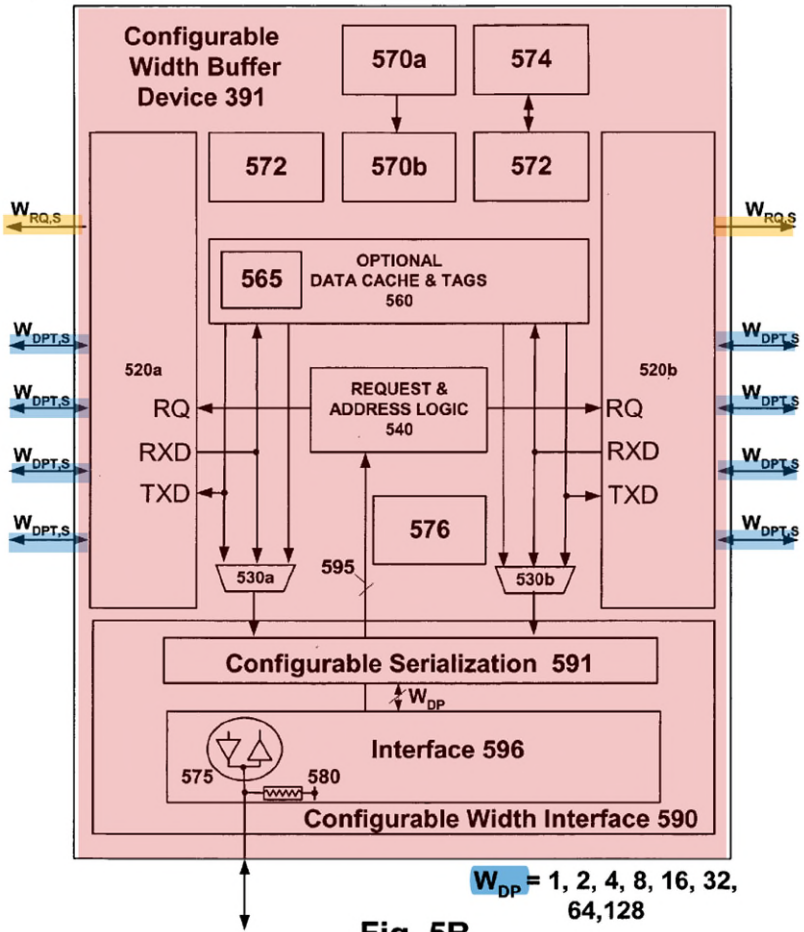

Fig. 5B

141. Perego also discloses an embodiment of the configurable width interface 590 that includes input and output latches 597f-m (blue). *Id.* at FIG. 5C (reproduced below with annotations), 17:22-26, 17:61-67. Perego discloses that

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there are two of these latches for each data connection of the configurable width buffer device. *Id.* at FIG. 5C, 17:22-26, 17:61-67.

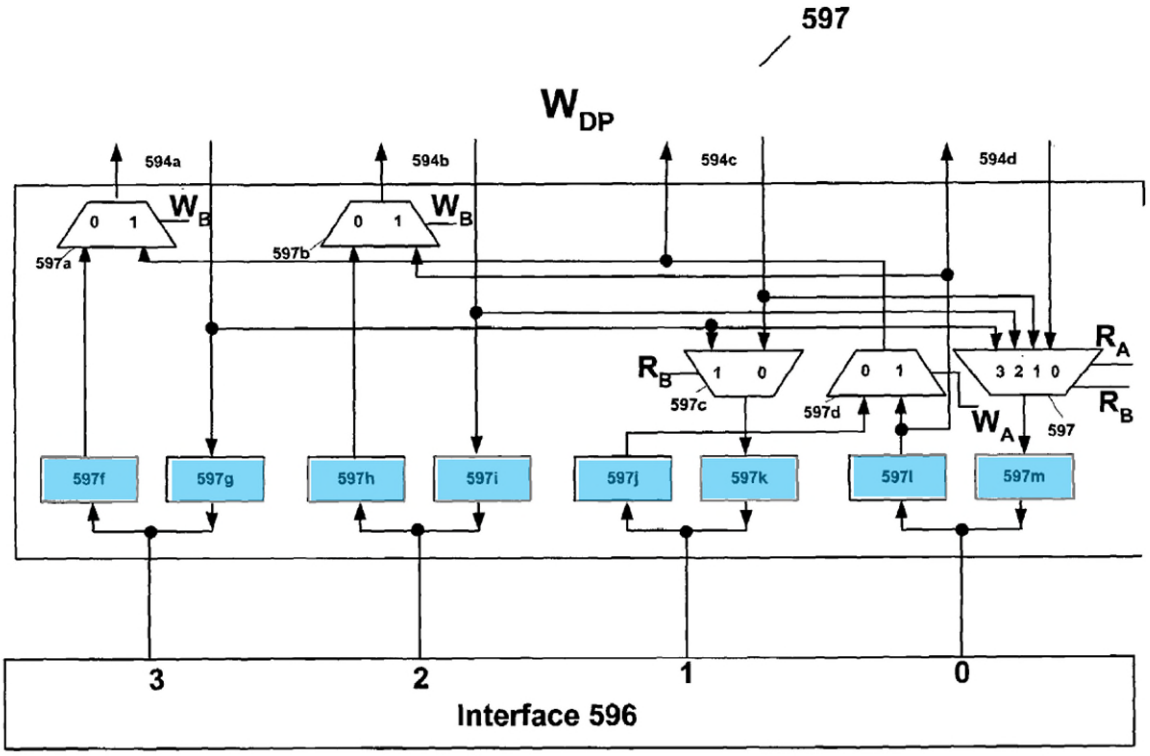

Fig. 5C

142. Perego further discloses that its buffer device includes a serial interface 574 and operations circuit 572 which may provide information to the memory controller that can be used, for example "in initialization of module or memory device identification values, test function, set/reset, access latency values, vendor specific functions or calibration." EX1071 at 12:20-34, FIGS. 5A and 5B.

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2. JEDEC Standard, DDR2 SDRAM Specification ("JESD79-2") (EX1064)

143. "JESD79-2" is the "JEDEC STANDARD, DDR2 SDRAM Specification." EX1064. It is my understanding that JESD79-2 was published in September of 2003. EX1065 at ¶¶ 6-11. I therefore understand that JESD79-2 is prior art to the 215 Patent pursuant to 35 U.S.C. § 102(a), at least because of its publication date. I also understand that JESD79-2 is prior art to the 215 Patent pursuant to at least 35 U.S.C. § 102(b) assuming the 215 Patent is not entitled to a priority date earlier than July 1, 2005, which I believe to be the case, as discussed above. *See supra* ¶¶51-67.

144. JESD79-2 was not discussed during prosecution of the 215 Patent (*see generally* EX1002) and is not a reference cited in the 215 Patent (*see* EX1001 at pp. 1-3 (56)). JESD79-2 is a standard by JEDEC for second generation double data rate (DDR2) SDRAM devices. EX1064 at Cover-1.

145. "For over 50 years, JEDEC has been the global leader in developing and publishing open standards for the microelectronics industry. JEDEC's membership consists of more than 3,000 volunteers representing nearly 300 member companies, and includes key technical individuals from most device, assembly, system and testing companies. JEDEC publications and standards are adopted worldwide." EX1065 at ¶ 4. JEDEC's standards were and are widely known and adhered to by those in the business of creating memory devices and

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modules. In fact, the 215 Patent incorporated another of the JEDEC standards for an earlier generation of DDR SDRAM devices, JESD79D, "Double Data Rate (DDR) SDRAM Specification," published February 2004, by reference to illustrate possible configurations of memory devices. *See* EX1001 at 21:36-40. Among other things, the JEDEC Standards, specifically JESD79-2, describe the process of executing read and write functions by memory devices, including receiving control signals from a memory controller and sending data signals to and from ranks of memory devices. *See* EX1064 at pp. 6, 24-33 (Section 2.2.4), 49. JESD79-2 also describes CAS latencies and a method of adding additional clock cycles to the CAS latency when executing read and write commands from a memory controller. *See id*. at pp. 24-25 (Section 2.2.4.1).

3. U.S. Patent Publication No. 2006/0277355 to Ellsberry et al. ("Ellsberry") (EX1073)

146. U.S. Patent Publ. No. 2006/0277355 to Ellsberry et al. ("Ellsberry"), titled "Capacity-Expanding Memory Device," was filed on June 1, 2005 as U.S. Patent Application No. 11/142,989, and was published as on December 7, 2006. EX1073 (Ellsberry) at p. 1. I understand that Ellsberry is prior art to the 215 Patent pursuant to at least 35 U.S.C. § 102(e) assuming the 215 Patent is not entitled to a priority date earlier than July 1, 2005, which I believe to be the case, as discussed above. *See supra* ¶¶51-67. I note that, in at least one other proceeding, the PTAB has found that the Patent Owner claimed subject matter in

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other patents in this family that was unsupported by the application for the 436 Patent and the provisional applications, meaning that Ellsberry was prior art. *See* EX1023 (Institution Decision against U.S. Patent No. 7,619,912) at pp. 24-26; *see also supra* ¶90.

147. During the original prosecution of the 215 Patent, Ellsberry was listed in an IDS with nearly 400 other references filed by Netlist (*see* EX1002 at pp. 120-136), but Ellsberry was not discussed during prosecution of the 215 Patent (*see* EX1001 at pp. 1-3 (56); *see also generally* EX1002).

148. In a Final Written Decision in an IPR against another patent owned by Netlist, the Board made numerous findings about what Ellsberry discloses. *See* EX1074.

149. Ellsberry discloses that the "term 'memory module' refers to any package in which one or more memory devices are mounted (e.g., DIMM, SIMM, etc.)." EX1073 at ¶[0023]. Ellsberry's Abstract explains that:

> "A control unit and memory bank switch are mounted on a memory module to selectively control write and/or read operations to/from memory devices communicatively coupled to the memory bank switch. By selectively routing data to and from the memory devices, a plurality of memory devices may appear as a single memory device to the operating system. That is, the invention expands the addressable memory banks on a module by making two smaller-capacity memory devices emulate a single higher-capacity memory device."

Id. at Abstract.

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150. For example, Figure 12 illustrates a configuration of a memory module "that can be built using combinations of the control unit and bank switch according to various embodiments of the invention." *Id.* at ¶[0052], FIG. 12 (reproduced below with annotations).

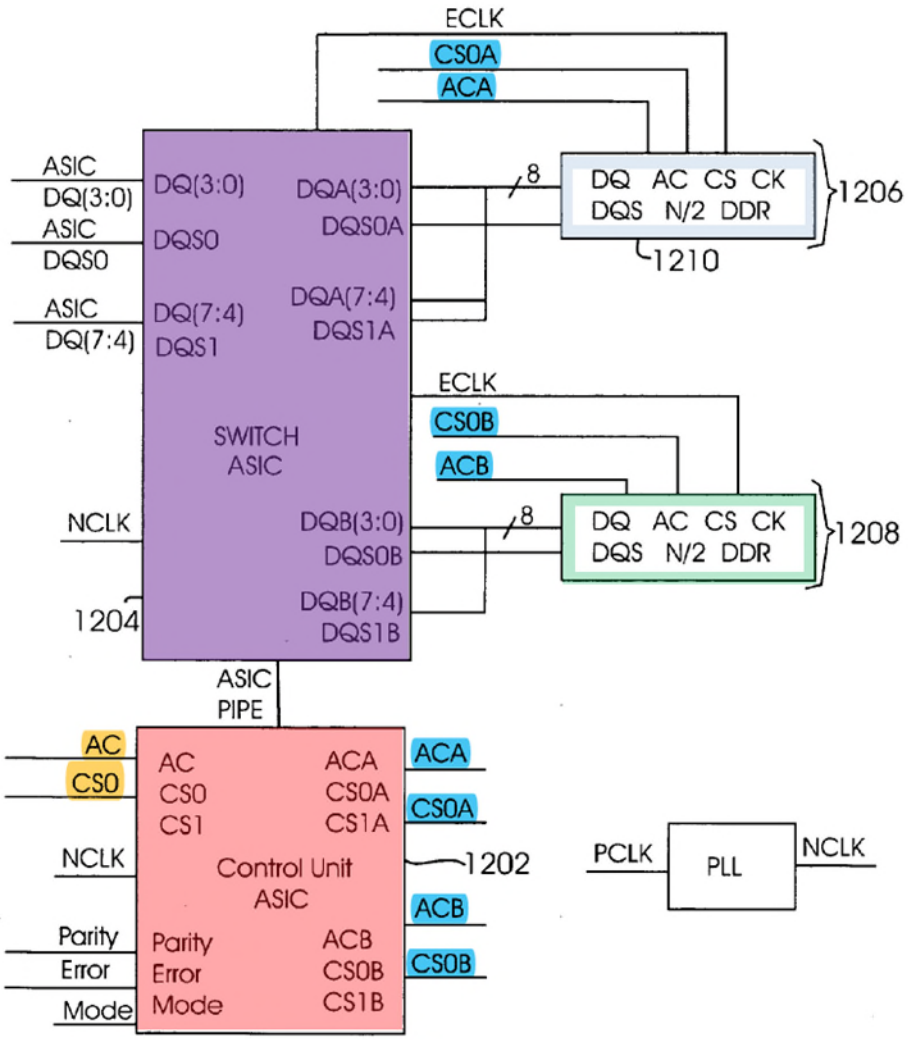

Fig. 12

In particular, "FIG. 12 illustrates a single chip-select memory configuration in which one control unit 1202 [(red)] and one bank switch 1204 [(purple)] are used

to control two memory banks 1206 [(light blue frame)] & 1208 [(light green frame)], each memory bank having one memory device 1210." *Id.* at ¶[0055]. As also shown in Figure 12, the control unit (1202, red) receives a single chip select signal (CS0, orange) to control a single memory rank and generates two chip select signals (CS0A and CS0B, blue) for two memory ranks. *See also* EX1023 at pp. 51-52 (Institution Decision agreeing Ellsberry discloses "ranks"); EX1076 at pp. 21-22 (same).

4. U.S. Patent No. 7,024,518 to Halbert et al. ("Halbert") (EX1078)

151. U.S. Patent No. 7,024,518 to Halbert et al. ("Halbert"), titled "Dual-Port Buffer-to-Memory Interface," was filed on March 13, 2002, published as U.S. Patent Publication No. 2002/0112119 on August 15, 2002, and issued as a patent on April 4, 2006. EX1078 at p. 1. I understand that Halbert is prior art to the 215 Patent pursuant to at least 35 U.S.C. § 102(a), (b), and (e).

152. During the original prosecution of the 215 Patent, Halbert's publication was listed with dozens of other references in an IDS filed by the Patent Owner (*see* EX1002 at pp. 252-253), but neither Halbert nor its publication were discussed during prosecution of the 215 Patent (*see* EX1001 at pp. 1-3 (56); *see also generally* EX1002).

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153. Halbert discloses "a new memory module architecture" (EX1078 at Abstract) which can be used in "a typical memory system configuration" (*id.* at 1:31-39), such as that shown in FIG. 1 (reproduced below).

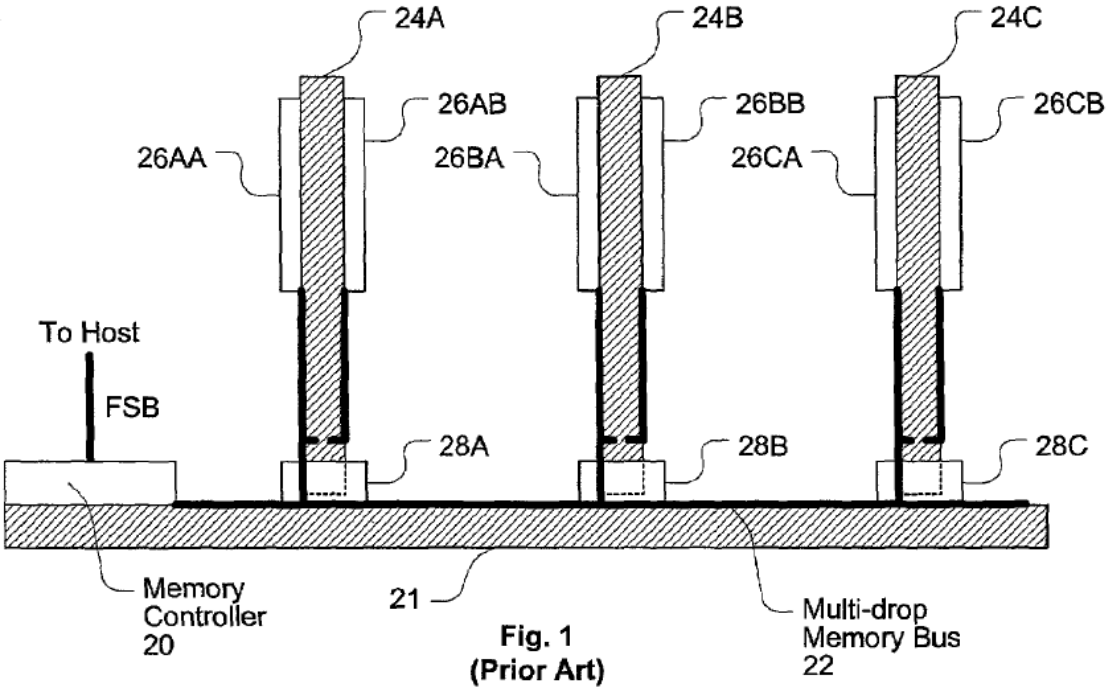

Fig. 1 (Prior Art)

154. This prior-art memory system includes a memory controller 20 coupled to a multi-drop "[m]emory bus 22 [which] carries memory signals on a collection of signal lines … including clock and control signals, address signals, command signals, and data signals." *Id.* at 1:31-2:23. The memory bus 22 is coupled to three memory sockets 28A-C, each holding a respective prior-art Dual In-Line Memory Module (DIMM) 24A-C, which was "a popular type of memory module" at the time. *Id.*

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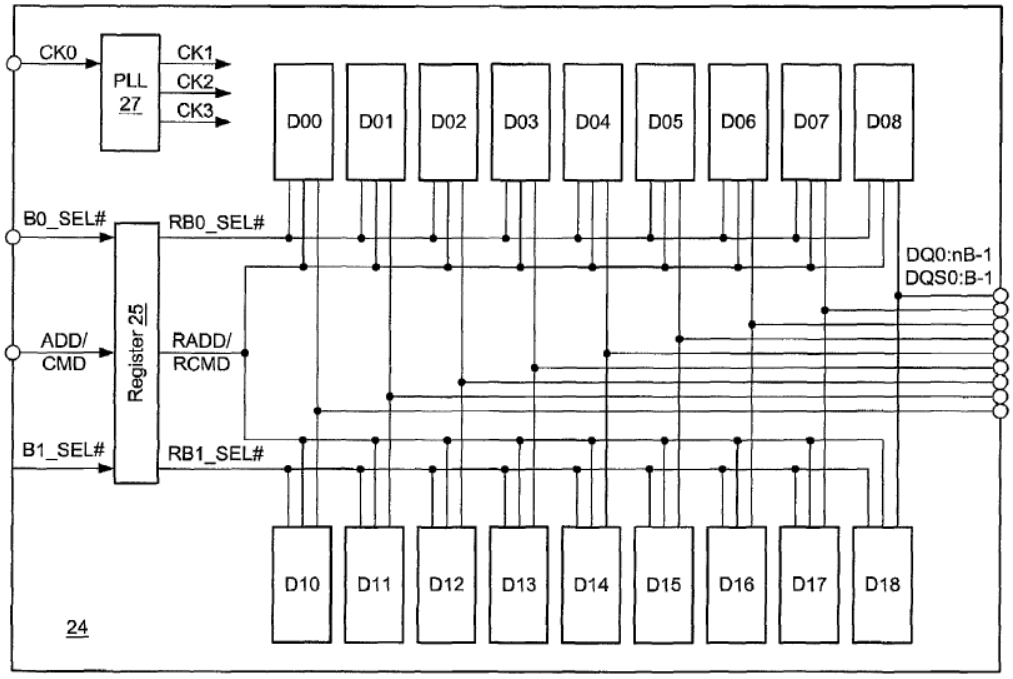
155. In general, a DIMM is built on a "rectangular low-profile circuit board" with electronic contacts along an edge to be inserted into a memory socket 28A-C. *Id.* at 2:6-14. The memory devices on the module are organized into one or more groups, called banks or ranks of memory devices. *Id.* at 2:15-24; 4:55-57. (As discussed above, the term "bank" could be used to mean the same thing as "rank." *See supra* ¶ 129.) Each such rank comprises enough memory devices to form a data path that has the full bit width of the module, and which "work in parallel to perform memory functions." *Id.* at 2:16-17. Halbert specifically discloses an exemplary prior art "registered DIMM 24 containing eighteen memory devices arranged in two banks, one containing devices D00-D08 and the other containing devices D10-D18." *Id.* at 2:23-46, FIG. 2 (reproduced below).

Fig. 2
(Prior Art)



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156. The prior-art DIMM 24 is a "registered DIMM," in which a register 25 latches on the address and command signals ADD/CMD received from the memory controller 20 through the memory bus 22, and re-drives the registered signals onto the module's address/command bus RADD/RCMD connected to the memory devices D00-D18 in both ranks. *Id.* The memory controller 20 also uses bank select signals B0_SEL# and B1_SEL# in the memory bus 22 to select the first bank of memory devices (D00-D08) or the second bank of memory devices (D10-D18), respectively, for a specific memory access. *Id.*; *see also* FIG. 3, 2:46-60 (describing how the memory controller 20 uses the ADD/CMD and B0_SEL# signals for "two consecutive random reads to memory bank D00-D08"). Halbert further explains that each of the registered B0-SEL# and B1_SEL# signals is a chip select signal which is connected to the chip select pins of the memory devices in their respective bank (i.e., rank). *Id*. at 2:23-46. In the prior art module, the data lines from both banks of memory devices are connected to a common set of DQ lines that are directly coupled to the edge connector and, in turn, to the system data bus 22 and the memory controller 20. *Id.*

157. The module architecture proposed by Halbert improved on the prior art modules "in several respects." *Id.* at 3:60; *see also id.* at 3:42-4:35. For example, Halbert's modules can "provide twice the data rate of the registered DIMM[]" (*id.* at 3:60-64) and "also allow the memory devices to be isolated from

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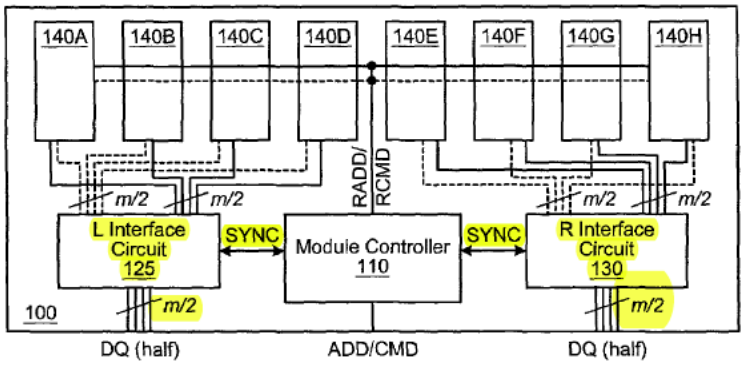
the full capacitive loading effects of the system memory data bus[]" (*id.* at 3:67-4:2). *Id.* Halbert explains that this isolation of the capacitive load from the memories is important because "at higher frequencies, this capacitance may make it infeasible to drive signals reliably on the bus." *Id.* at 4:21-22.

158. Halbert's proposed module 100 can be implemented to be "transparent to the memory system and to the memory devices … [which] allows for an embodiment that is compatible with an existing memory controller/bus and with existing memory devices[]" (*id.* at 3:48-57; *see also id.* at 3:42-4:35), as shown in FIGS. 7 and 8 (*see id.* at 7:31-61), which are reproduced with annotations below.

Fig. 7



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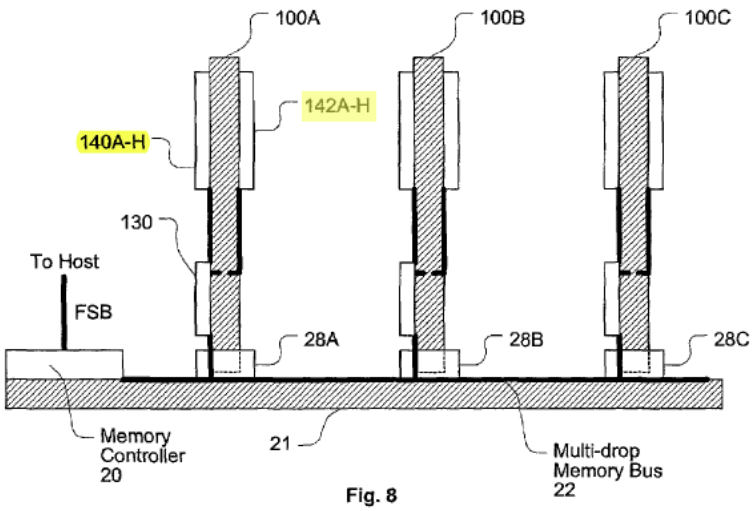

In this memory system, Halbert's proposed modules 100A-C are inserted into the prior-art memory system's bus sockets 28A-C instead of the prior-art modules 24A-C. *Id.* at 7:31-61. Thus, the modules 100A-C are coupled through the same memory bus 22 to the same memory controller 20. *Id.* Halbert specifically notes that the memory controller 20 "initiates READ operations just like it would for a [prior art] registered DIMM" described with reference to Halbert's FIG. 3. *Id.* at 6:1-4.

159. Halbert's proposed module 100 includes a module controller 110 that, like the register 25 in the prior-art module, receives the address and command signals from the system controller and provides registered versions of those signals to two ranks of memory devices, 140A-H and 142A-H. *Id.* at 4:36-48, 7:31-37. The module 100, unlike the prior-art module, also includes left and right data interface circuits 125 and 130, the details of which are described with reference to

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FIG. 4. *Id.* at 7:31-61, FIG. 4, 4:36-5:65. These circuits provide an interface for data communication between the system memory bus 22, at one side, and corresponding memory devices in ranks 140 and 142, on the other side. *Id.* This data communication is controlled by the module controller 110, which "provides timing and synchronization signals to the data interface circuit" through control lines (*id.* at 4:45-47; *see also id.* at 7:31-61, FIG. 4, 4:36-5:65), which in FIG. 7 are labeled as 'SYNC').

160. Each of the interface circuits 125 and 130 can be implemented as a circuit which is almost identical to the data interface circuit 120 of Halbert's FIG. 4 (reproduced below with annotations), except that the number of data signal lines is split in half. *Id.* at 7:37-40. In other words, interface circuit 120 has 'm' DQ lines connecting to the data bus, and each of the left and right interface circuits 125 and 130 has only half of those data signal lines, 'm/2.' *Id.*

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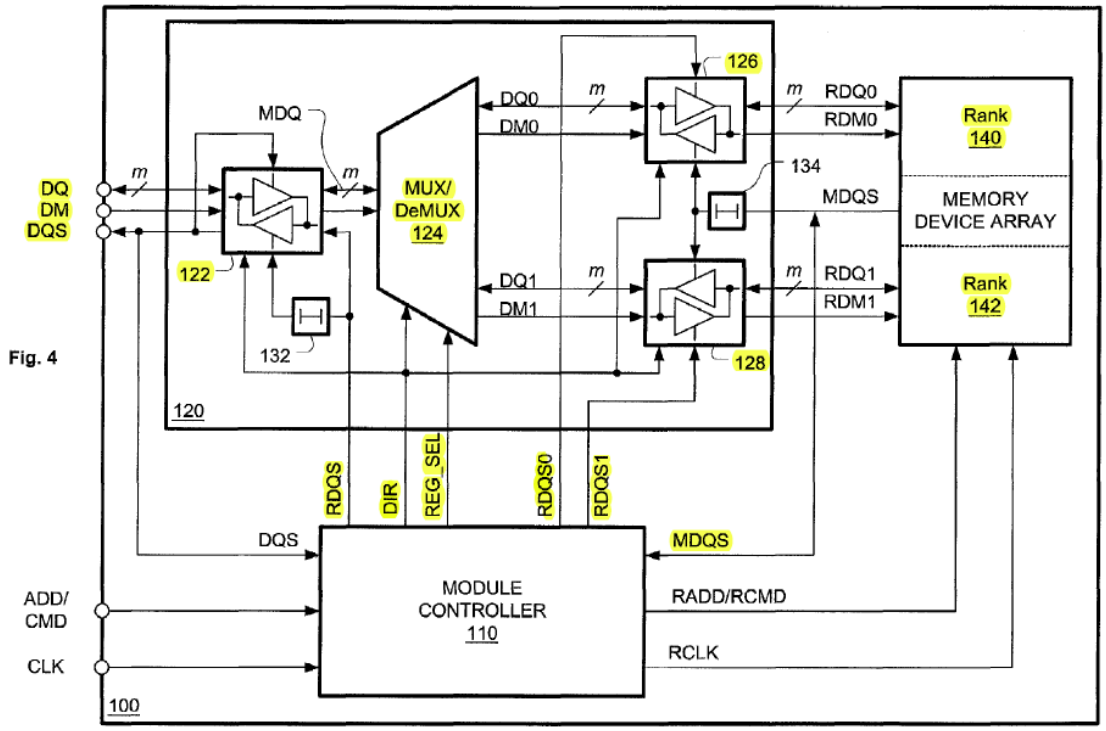

Fig. 4

161. On the memory data bus side, the interface circuit 120 has a bi-directional buffer 122 that "receives and drives data signals DQ on the system memory data bus." *Id.* at 4:60-5:5. The bidirectional buffer 122 can also drive data strobe signals DQS "onto the memory data bus." *Id.* at 5:4-5. On the memory rank side, the interface circuit 120 has two bi-directional registers 126 and 128 to connect to the memory ranks 140 and 142, respectively. *Id.* at 5:6-14. The interface circuit also has a multiplexer/demultiplexer 124 that selectively directs data signals through register 126 or register 128. *Id.* at 5:15-22, FIG. 4.

162. The module controller 110 controls the interface circuits with signals, such as DIR, REG_SEL, RDQS0 and RDQS1. *Id.* at 5:23-65, 7:51-53. "For

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instance, direction signal DIR specifies whether data flow is towards the memory array (TO) or away from the memory array (AWAY)." *Id.* at 5:25-28. "The register select signal REG_SEL, in the AWAY mode, determines whether DQ0 [from rank 140] or DQ1 [from rank 142] will be supplied to buffer 122 … [which] drives that data onto the memory data bus." *Id.* at 5:40-50. "In the TO mode, REG_SEL determines which of registers 126 and 128 will receive DQ at each memory bus clock cycle…. When RDQS0 transitions, register 126 latches data from DQ0 (and DM0) [and w]hen RDQS1 transitions, register 128 latches data from DQ1 (and DM1)." *Id.* at 5:51-65.

163. In operation, the module controller 110 determines the current value of the control signals, such as DIR, "by snooping CMD signals as they pass through the controller 110." *Id.* at 5:23-39. For example, the "controller 110 scans the command bus for READ or WRITE commands … [and] counts the number of pending READ operations (including each operation's burst length if the devices support burst mode access) in order to track how long to stay in the READ state." *Id.* at 6:5-14.

164. Halbert also discloses alternative implementations. For example, Halbert explains that its "illustrated examples … show two ranks of memory, but other numbers of ranks are also possible, e.g., a 4:1 multiplexer and four ranks of memory." *Id.* at 9:20-35. Halbert also discloses that "an embodiment can also

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have the capability to respond to a write that requests to write less than N=Rxm bits … [so that] when a write to the ranks is performed, only the one word requested by the external memory controller will actually be written[.]" *Id.* at 9:46-54. Halbert further explains that the "types, sizes, or numbers of memory devices selected for use with the present invention are not critical[]" and that "although the illustrated embodiments use one or two interface circuits and a separate module controller, all of these devices could be integrated in a single device, or in some other number of packages with some other division of tasks to be performed by the module." *Id.* at 9:55-10:6.

5. U.S. Patent Publication No. 2003/0039151 to Matsui ("Matsui2") (EX1082)

165. U.S. Patent Publication No. 2003/0039151 to Matsui ("Matsui2"), titled "Memory Device and Memory System," was filed on August 23, 2002, as U.S. Patent Application No. 10/227,647, and published on February 27, 2003. EX1082 (Matsui2) at p.1. I understand that Matsui2 is prior art to the 215 Patent pursuant to at least 35 U.S.C. § 102(a), (b), & I.

166. Matsui2 was not cited during prosecution of the 215 Patent. *See* EX1001 at pp. 1-3 (56); *see also generally* EX1002. Another patent (U.S. Patent No. 5,953,280) naming the same inventor was listed in an IDS during prosecution of the 215 Patent (*see, e.g.*, EX1002 at p. 164), but this listed patent contains

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different disclosure than Matsui2 and stems from an application that was filed more than five years earlier.

167. Matsui2 discloses a termination circuit 213 that interfaces with memory devices and provides external termination for data signals received on data bus 22 from the memory devices. *E.g.*, EX1082 (Matsui2) at [0037]. For example, as illustrated in its Fig. 2, Matsui2 teaches "…a termination circuit 213 to be put into an operating state in case [sic] where the data are read from the DRAM1, the DRAM2, the DRAM3, and the DRAM4." *Id.* at [0037] & Fig. 2 (reproduced below with annotations). Furthermore, Matsui2 teaches, as illustrated in several figures, that termination circuit 213 is turned off and on to perform read and write operations. *See id*. at Figs. 5-7, & 9.

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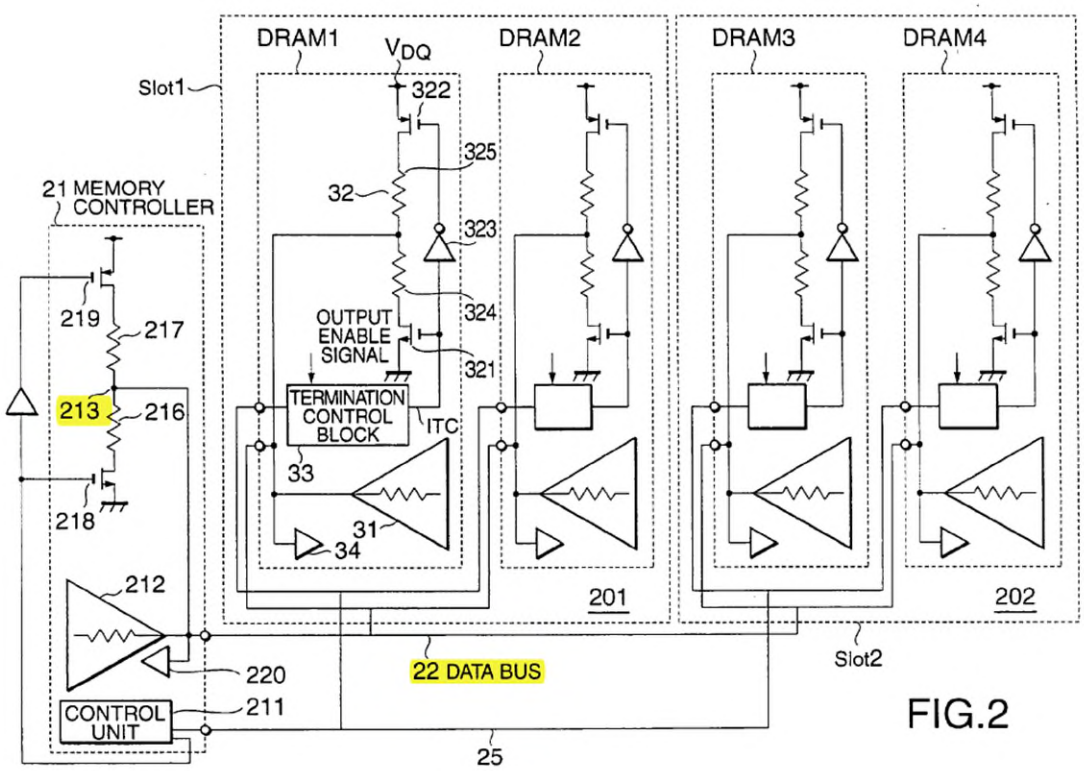
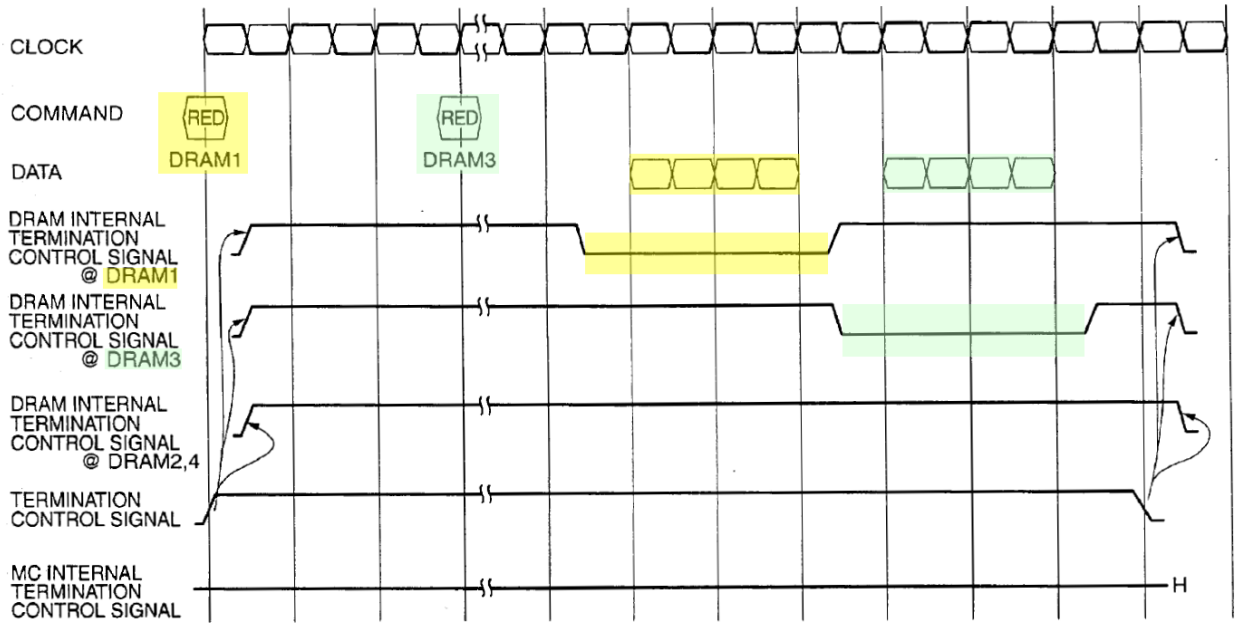


FIG.2

168. Specifically, Figure 5 in Matsui2 (reproduced below) illustrates the process of turning on and off the termination of DRAM devices for termination control for a read operation.



TERMINATION CONTROL UPON READ OPERATION OF DRAM1/3

FIG.5

Id. at FIG. 5.

B. Background Technology

1. JEDEC Standards

169. In my opinion, a Skilled Artisan would have been familiar with memory systems and corresponding standards, including the JEDEC standards for memory devices and memory modules at the time. *See supra* ¶¶49-50; EX1069, p. 9 & Fig. 16; EX1070, pp. 332-35, 318-20. For example, Perego discloses Double Data Rate (DDR) SDRAM memory devices. *See* EX1071 at 3:67-4:3, 8:1-9, 10:54-59. A Skilled Artisan would have readily understood that DDR memories were already standardized by JEDEC and that these standards were available and well-known. *See, e.g.*, EX1073 (Ellsberry) at [0046] (incorporating by reference

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DDR1 and DDR2 standards), [0050] ("As a result of this architecture, the memory module presents a single electrical load to the system and is compatible with existing standards (e.g., JEDEC compatible, etc.). The Joint Electron Device Engineering Council (JEDEC) standards, used in many memory applications, are incorporated herein by reference."). A Skilled Artisan would have also understood that JEDEC also standardized memory modules and corresponding interface circuits. *See, e.g.*, EX1001 at 6:1, 21:17 (referring to "RDIMM," a memory module configuration standardized by JEDEC); EX1062, EX1066 (JEDEC standards for "RDIMM"). Furthermore, a Skilled Artisan would have also been familiar with the standards developing process at JEDEC, including proposals for the standards that were being developed at the time.

170. Therefore, in my opinion, a Skilled Artisan would have been familiar with the technology described in the JEDEC standards that existed and were being developed at the time. Examples of such standards include the JEDEC standard for DDR memory devices (*see* EX1060 & EX1062) and the JEDEC standard for DDR2 memory devices (*see* EX1064 & EX1066).

2. Rank multiplication

171. In my opinion, a Skilled Artisan also would have been familiar with rank multiplication at the time. Indeed, as shown above, hundreds of claims from this family of patents have been found invalid, and those invalid claims were

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predominantly directed to rank multiplication. *See, e.g.*, *supra* ¶¶ 89-95, 99. Rank multiplication was well known in the prior art because it permitted replacing one rank of expensive high-density memory with two or more ranks of less expensive low-density memory without any change to the overall performance or memory capacity of the memory module — thus enabling significant cost savings. *See, e.g.*, EX1079, ¶ [0008] ("lower densities are cheaper"); EX1001 at 13:51-14:4 ("cost savings can be significant"). For example, U.S. Patent Application Publication No. 2006/0117152 to Amidi et al. (Amidi), which was filed January 5, 2004, and is prior art to the 215 Patent under 35 U.S.C. § 102, discloses a four rank memory module for standard two rank sub-systems. EX1079 at Title. Amidi explains that prior-art memory modules typically had one or two ranks of memory devices, and were configured to be inserted into sockets on the computer's main board. *Id.* at [0002]-[0007]. "Common system implementations 100 have typically two memory chip selects routed per socket … [where t]he system chip select signals control individual memory modules ranks." *Id.* at [0003]. "Because memory devices with lower densities are cheaper and more readily available, it may be advantageous to build the above same density memory module using lower densities devices. However, in order to achieve a [higher] density . . . the memory module needs four ranks." *Id*. at [0008]. "A need therefore exists for a transparent four rank memory module fitting into a memory socket having two chip select

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signals routed." *Id.* at [0011]. This need for having modules with more ranks than available chip selects in a given system was commonly referred to as "rank multiplication."

172. A Skilled Artisan would have understood such rank multiplication was an available and predictable technology at the time. For example, Amidi teaches that rank multiplication can be implemented on a memory module by a "[Complex Programmable Logic Device] CPLD 410 [which] emulates a two rank memory module on the four rank memory module 400. CPLD 410 allows a system having a memory socket with only two chip select signals routed to interface with a four rank memory module . . . . The CPLD 410 determines which rank from the four ranks to activate based upon the address and command signals from a memory controller coupled to the memory module 410." *See* EX1079 at [0041]. Amidi also teaches that its CPLD uses command signals such as CAS, RAS, and WE in addition to the chip select signals cs0 and cs1 and the row address, and generates four chip select signals rcs0, rcs1, rcs2, and rcs3 (one for each rank) as shown in Amidi's FIG. 6A (reproduced below with annotations highlighting the two received chip selects in yellow and the generated four chip selects in light blue). *Id.* [0050]-[0052].

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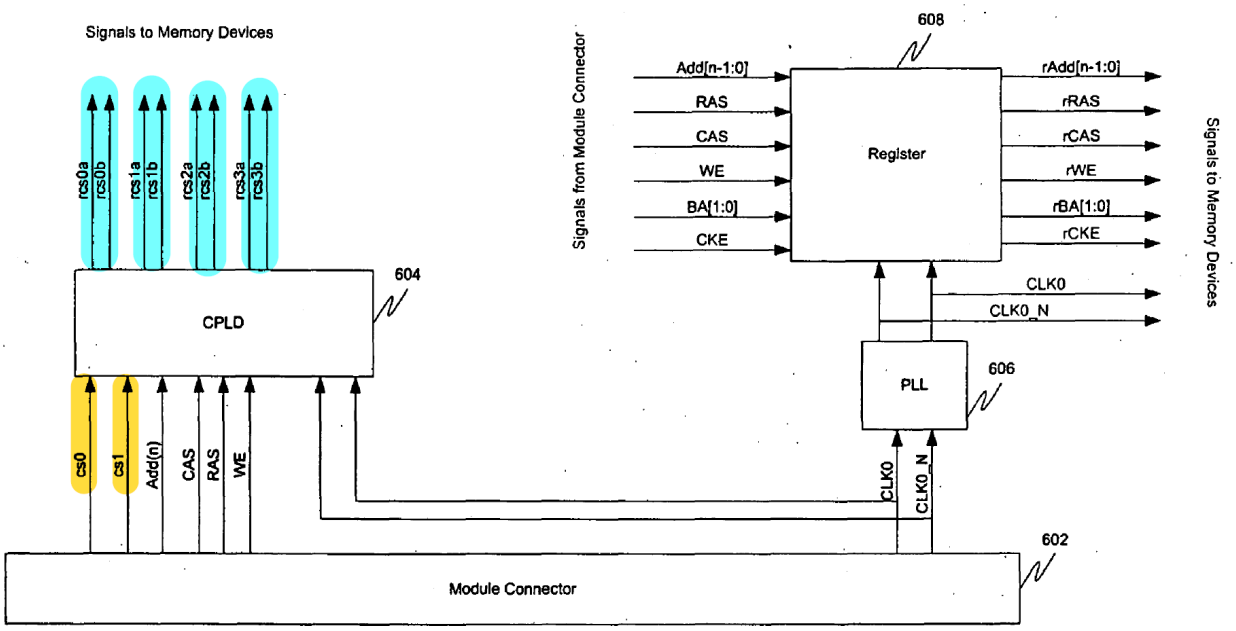

Row Address Decoding
FIG.6A

173. Another example of prior art that teaches rank multiplication is Ellsberry (EX1073), discussed above. *Supra* at ¶¶146-150; EX1073, Abstract, ¶¶ [0010], [0011], [0026], [0034], [0037], [0046], Figs. 7A-F.

174. Therefore, a Skilled Artisan would have been familiar with rank multiplication, its advantages, and understood that it was an available and predictable technology at the time. A Skilled Artisan would have also understood that rank multiplication is a broadly adaptable technique that can be implemented in a variety of ways using only ordinary engineering effort.

C. **The Combinations Relied on Here**

175. The combinations analyzed here were obvious to a Skilled Artisan at the time and are straightforward applications of the teaching of the prior art to

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achieve predictable advantageous results. Each of the Grounds discussed below involves the combination of prior-art references in view of the knowledge of a Skilled Artisan.

176. Ground 1 involves Perego in view of JESD79-2

177. Ground 2 involves Ground 1 in further view of Ellsberry.

178. Ground 3 involves Ground 1 in further view of Halbert.

179. Ground 4 involves Ground 1 in further view of Matsui2.

V. COMPARISON OF THE PRIOR ART TO THE CLAIMS OF THE 215 PATENT

180. My analysis below is based on my understanding of the law and the other information discussed above, including the four Grounds discussed above.

A. Reasons to Combine

181. A Skilled Artisan would have been motivated to make the combinations in Grounds 1-4 for at least the following reasons.

1. Ground 1: Perego (EX1071) and JESD79-2 (EX1064)

182. As mentioned above, Ground 1 involves Perego and JESD79-2. *See supra* ¶176. Perego and JESD79-2 are analogous art to the 215 Patent as each is directed to solving the problem of efficiently organizing and using memory systems as required in computer systems at the time, including achieving increased speed, capacity, and flexibility. EX1071 (Perego) at 1:14-17 ("More specifically, this invention is directed toward memory system architectures that may include

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integrated circuit devices such as one or more controllers and a plurality of memory devices."), 2:26-30 ("There is a need for memory system architectures or interconnect topologies that provide flexible and cost effective upgrade capabilities while providing high bandwidth to keep pace with microprocessor operating frequencies."); EX1064 (JESD79-2) at Cover-1 (DDR2 SDRAM Specification), Cover-2 ("JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, …"); EX1001 at 1:42-45 ("The present invention relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules.").

183. A Skilled Artisan would have been motivated to combine the teachings of JESD79-2 with the memory module described in Perego. As discussed above in ¶¶169-170, a Skilled Artisan would have known about and been familiar with the JEDEC Standards, including JESD79-2, and would have recognized the relevance of these standards in the disclosure of Perego. For example, Perego discloses that examples of memory devices include double data rate (DDR), e.g., DDR2 Synchronous DRAM (SDRAM) memory devices. EX1071 at 3:62-4:12, 10:54-67. A Skilled Artisan would have understood that Perego's disclosure of DDR2 memory devices refers to memory devices that

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follow the JEDEC Standards for double data rate memory devices, including JESD79-2 for DDR2 memory devices. EX1064 at Cover Page ("DDR2 SDRAM Specification"). Accordingly, a Skilled Artisan would have been motivated to consult the relevant JEDEC Standards, including JESD79-2, in order to implement Perego's system with JEDEC-compatible memory devices.

184. Perego also teaches the following:

> "Buffer device 350 provides a high degree of system flexibility. New generations of memory devices may be phased in with controller 310 or into memory system 300 by modifying buffer device 350. Backward compatibility with existing generations of memory devices (i.e., memory devices 360) may also be preserved. Similarly, new generations of controllers may be phased in which exploit features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices."

EX1071 at 6:34-43. A Skilled Artisan would have understood from this disclosure that Perego's system can be compatible with memory standards existing at the time for memory devices ("retaining backward compatibility with existing generations of memory devices"). As discussed above, standards for memory devices at the time included the JEDEC Standards, such as JESD79-2 for DDR2 memory devices. Accordingly, a Skilled Artisan would have been motivated to turn to the standards for memory devices that existed at the time in order to implement Perego's system in a way that is compatible with existing generations of memory devices, including DDR2 memory devices following the JEDEC standard JESD79-2. A Skilled Artisan would have also recognized that applying JESD79-2's

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teachings to Perego would have resulted in a predictable variation of Perego, which would improve similar devices in the same way and not yield unexpected results or challenges in implementation. Indeed, the very purpose of the JEDEC standards is "to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, …" EX1064 at Cover-2.

185. Perego discloses that a "memory module" or "module" "denotes a substrate package housing or structure having a plurality of memory devices employed with a connector interface." EX1071 at 4:13-37. Perego also discloses that an upgradeable memory system can include socket and connector interfaces for removable memory modules, such as dual inline memory modules (DIMM). EX1071 at 1:21-23 ("Memory capacity is commonly upgraded via memory modules or cards featuring a connector/socket interface."), 1:58-2:6 ("A socket and connector interface may be employed which allows each module to be removed and replaced by a memory module that is faster or includes a higher capacity. … U.S. Pat. No. 5,513,135 [(EX1081)] discloses a contemporary dual inline memory module (DIMM) having one or more discrete buffer devices."). Perego also discloses that there was a need for "flexible and cost effective upgrade capabilities[.]" *Id.* at 2:26-29. As discussed above, Perego teaches to use DDR

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SDRAM devices, and a Skilled Artisan would have understood that those memory devices were standardized by JEDEC. EX1071 (Perego) at 3:62-4:12, 10:56-59.

186. A Skilled Artisan would have understood from this disclosure that it was desirable to use the DIMM format for Perego's memory modules according to the JEDEC standards, including JEDEC compliant memory devices, because it allowed "flexible and cost effective upgrade capabilities." EX1071 at 2:26-29; EX1064 at Cov-2 ("JEDEC standards … are designed to serve the public interest through … facilitating interchangeability and improvement of products, …").

187. Perego's disclosure about upgrade capabilities and DIMM format was consistent with the knowledge of a Skilled Artisan, further motivating her to use JEDEC DIMM format and the JEDEC compliant memory devices, as discussed above. *Supra* at ¶184; EX1071 at 6:34-43.

188. A Skilled Artisan would have understood from Perego's disclosure and the JEDEC standards that Perego's module can be implemented in a registered DIMM format that could be used at the time to upgrade existing memory systems that used sockets/connectors for modules in a registered DIMM format. A Skilled Artisan would have also understood that such a DIMM format had been standardized by JEDEC, for example, in JESD21-C. EX1062 at p. 1 ("DDR SDRAM Registered DIMM Design Specification"); EX1066 at p. 1 (similar). In accordance with the general purpose of JEDEC, the JESD21-C standard specified

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the input and output signals and their functions on the module, as well as the corresponding pin assignments for the pins in the socket/connector for inter-operability. EX1062 at pp. 5-9 ("This specification defines the electrical and mechanical requirements for 184-pin, 2.5 Volt, PC1600/PC2100, 64/72 bit-wide, Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR SDRAM DIMMs)."); EX1066 at pp. 4-8 (similar). Accordingly, a Skilled Artisan would have been motivated to implement Perego's memory modules in a registered DIMM format that fits into the DIMM connectors of the time and uses the input and output signals of a DIMM module according to the relevant JEDEC standards, including JESD21-C.

189. Furthermore, Perego discloses that its module includes "a SPD [which] provides the configurable width buffer and/or module capabilities to the memory system." EX1071 at Abstract. Perego also discloses that "serial presence detect (SPD) [is] employed in some conventional DIMM modules" and the "SPD stores information used by the remainder system to properly configure the memory devices upon boot of the system." *Id*. at 12:20-34. A Skilled Artisan would have understood from this disclosure that Perego's module can be in a format of a conventional DIMM and include an SPD in order to upgrade the memory system and provide the upgrade information to the memory controller. A Skilled Artisan would have also understood that JEDEC standards, such as JESD21-C, describe

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details of the information that can be provided by an SPD. *See* EX1062 at pp. 68-70 ("The Serial Presence Detect function MUST be implemented on the PC DDR SDRAM Registered DIMM. The component used and the data contents must adhere to the most recent version of the JEDEC DDR SDRAM Serial Presence Detect Specifications."); EX1066 at pp. 94-96 (similar). A Skilled Artisan would have understood that, in order to upgrade such a JEDEC-compatible system, Perego's module would also need to be compatible with SPD requirements of the specific system at the time in order to allow the memory controller to read, understand, and properly initialize and use that upgrade module.

190. In addition, a Skilled Artisan would have further understood that the JEDEC standards, including the JESD21-C and JESD79-2 standards, describe useful designs for implementing memory modules. For example, JESD21-C discloses electrical connection and physical layouts for registered memory modules with one or more ranks of memory devices. EX1062 at pp. 10-16 & 29-35. For example, these designs describe memory modules with DDR memory devices of different types and numbers. *See, e.g.*, *id*. at p. 13 (x64 DIMM of two ranks with x8 DDR SDRAMs) & 15 (x72 DIMM of two ranks with x4 DDR SDRAMs). Similarly, JESD79-2 describes the details of memory transactions, including read and write operations, for JEDEC-compliant memory devices. *See, e.g.,* EX1064 at pp. 24-33 (Section 2.2.4). A Skilled Artisan would have been aware of these

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standards and understood their disclosure, thus motivating her to look at these standards based on the disclosure of Perego in order to implement Perego's modules using JEDEC-compliant memory devices, such as DDR2 SDRAMs, and to allow these modules to be used in JEDEC-compliant memory systems, such as those using DIMM modules of the format described by JESD21-C.

191. Accordingly, a Skilled Artisan would have understood that the combination of Perego and JESD79-2 includes elements that were familiar to a Skilled Artisan since she was familiar with the prior art memory modules, including Perego's, as well as the JEDEC standards, including JESD79-2. The proposed combination uses those familiar elements according to known methods described in Perego and the JEDEC standards, including JESD79-2, and yielded predictable results, namely memory modules like Perego's including memory devices operating according to the familiar JEDEC standards.

192. Details of the combination of Perego and JESD79-2 and further motivations to make the specific combination will be discussed below with reference to specific claim limitations.

2. Ground 2: Ground 1 and Ellsberry (EX1073)

193. As mentioned above, Ground 2 involves Ground 1 (Perego in view of JESD79-2) in further view of Ellsberry. *See supra* ¶177. Ellsberry is analogous art to Perego, JESD79-2, and the 215 Patent, because Ellsberry is also directed to

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solving the problem of efficiently organizing and using memory systems, including expanding the capacity of memory modules that can be used in the memory systems at the time. EX1073 at Abstract ("The invention relates to a device, system, and method for expanding the memory capacity of a memory module."), [0026] ("One embodiment of the invention relates to a system that expands the memory capacity of a memory module without increasing the bus size. A controller and memory bank switch allow the use of separate smaller-capacity memory devices to emulate a single higher-capacity memory device to a host system. This effectively expands the number of addressable banks per memory module without the need for additional chip select lines on the main memory bus.").

194. Furthermore, Ellsberry uses DDR SDRAM devices with memory modules in a DIMM format like Perego and the 215 Patent, and expressly incorporates the corresponding JEDEC standards, like JESD79-2. EX1073 at [0046] ("In various embodiments of the invention, the control unit and bank switch combination may support SDRAM DDR1 and DDR2 specifications (incorporated herein by reference)"), [0023] ("The term "memory module" refers to any package in which one or more memory devices are mounted (e.g., DIMM, SIMM, etc.)."), [0050] ("the memory module ... is compatible with existing standards (e.g., JEDEC compatible, etc.). The Joint Electron Device Engineering Council (JEDEC)

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standards, used in many memory applications, are incorporated herein by reference."); [0053] ("FIGS. 10, 11, 12 and 13 illustrate different configurations of memory modules (e.g., DIMMs) that can be built using combinations of the control unit and bank switch according to various embodiments of the invention.").

195. A Skilled Artisan would have been motivated to combine the Perego-JESD79-2 combination with the teaching in Ellsberry. As discussed above in ¶¶182-190, a Skilled Artisan would have known about and been familiar with the JEDEC standards, including JESD79-2, and would have recognized the relevance of these standards in the disclosure of Perego. Similarly, a Skilled Artisan would have recognized the relevance of these standards in the disclosure of Ellsberry as discussed above and below.

196. Ellsberry describes an implementation with a "memory module [that] presents a single electrical load to the system and is compatible with existing standards (e.g., JEDEC compatible, etc.)[.]" EX1073 (Ellsberry) at [0050]. For example, Ellsberry discloses an implementation where its memory bank switch presents a single load to the memory bus. *Id*. at [0012], Fig. 4. A Skilled Artisan would have understood that, although not expressly shown in Ellsberry's Fig. 4, such a single electrical load can be implemented in the memory bank switch by tristate pin drivers, which was a standard way for a chip to drive and receive signals on bidirectional lines that go beyond the chip boundary. EX1068 (Stone) at

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131-133 (explaining that memory chips use tristate output drivers on the chip which have to be turned on and off such that bus conflicts are avoided). Therefore, Ellsberry teaches a load reduced memory module like Perego and the 215 Patent. Ellsberry also incorporates the JEDEC standards by reference. EX1073 at [0050]. In fact, one of Ellsberry's claims recites that "the memory module is a dual inline memory module compl[ia]nt with a Joint Electron Device Engineering Counsel (JEDEC) standard." *Id*. at Claim 10. Furthermore, Ellsberry teaches using "two separate SDRAM DDR devices to emulate a single, two-times capacity, SDRAM DDR device[.]" EX1073 at [0026]; *see also id.* Figs. 7A-7F. Therefore, Ellsberry also teaches rank multiplication like the 215 Patent. Ellsberry further teaches that, to implement such rank multiplication, "the control unit and bank switch combination may support SDRAM DDR1 and DDR2 specifications (incorporated herein by reference) with memory capacities of 256 Mb, 512 Mb, and 1 Gb…." *Id*. at [0046].

197. Accordingly, as for Perego, when looking at Ellsberry, a Skilled Artisan would have been motivated to consult the relevant JEDEC standards, such as JESD79-2, in order to implement Ellsberry's system with JEDEC compatible memory devices. A Skilled Artisan would have also recognized that applying Ellsberry's teachings to the Perego-JESD79-2 combination would have resulted in a predictable variation of the Perego-JESD79-2 combination, which would

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improve similar devices in the same way and not yield unexpected results or challenges in implementation.

198. For example, Ellsberry discloses that, like Perego, its memory module buffers the data signals which advantageously reduces the load on the data lines. EX1073, e.g., at Fig. 2 (reproduced below, showing switch ASICs 206 and 208 coupled to respective data busses 230 and 232 on the system side, and each having Port A and Port B with respective data busses to Banks 0-3 of memory devices) and Fig. 4 (showing bidirectional drivers on the data lines), [0031] ("Additionally, each memory bank switch 206 and 208 includes signal drivers to drive data signals to and from the memory banks and to and from the DIMM interface 202. This reduces resistive and/or capacitive loading of the data bus coupled to the DIMM interface and the bus 110 while emulating a standard memory device interface."). A Skilled Artisan would have understood that data buffering advantageously reduces the load on the data lines independent of the details of the data buffer implementations. For example, Perego, like the 215 Patent, uses a central buffer that buffers, among other signals, the data signals, and Ellsberry uses distributed data buffers, and a Skilled Artisan would have understood that these implementations were known alternatives to implement data buffering at the time. EX1078 (Halbert) at 10:1-6 ("For instance, although the illustrated embodiments use one or two interface circuits and a separate module controller, all of these

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devices could be integrated in a single device, or in some other number of packages with some other division of the tasks to be performed by the module."). Therefore, a Skilled Artisan would have been motivated to look at analogous art like Ellsberry for details of implementing memory modules with data buffering.

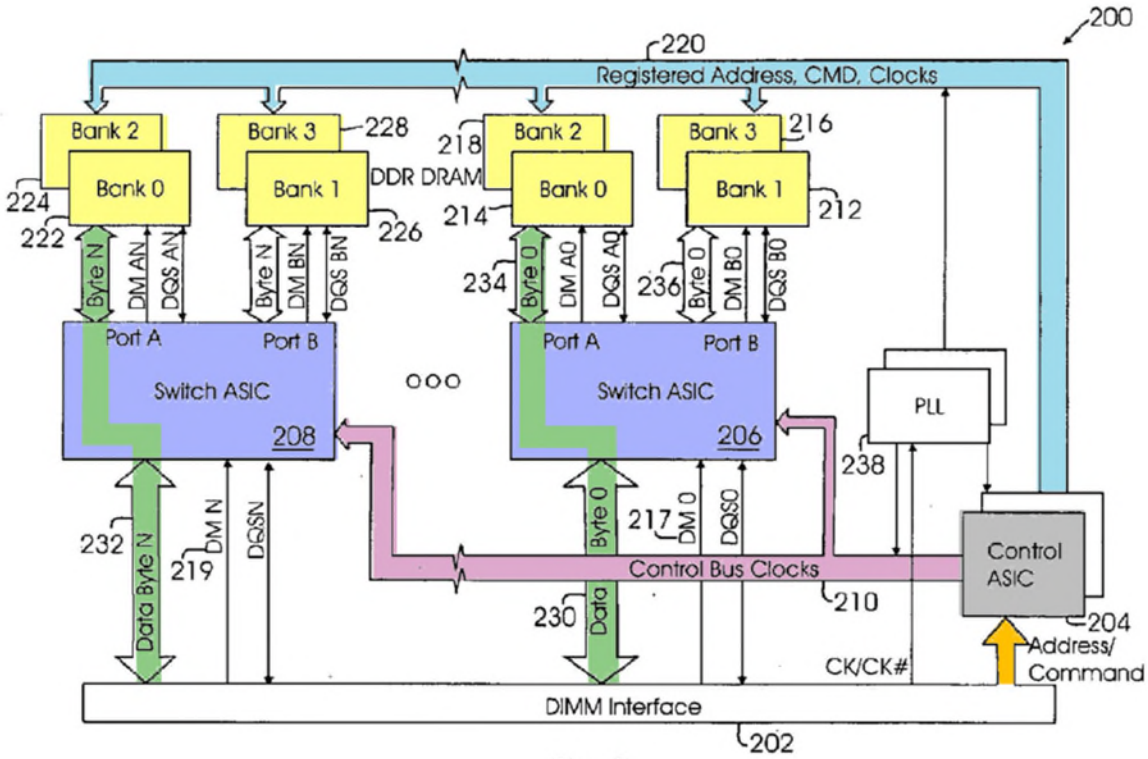

Fig. 2

199. Accordingly, the proposed combination of Perego, Ellsberry, and the JESD79-2 standard uses elements that were familiar to a Skilled Artisan, including Perego's and Ellsberry's memory modules with data buffering functionalities that advantageously reduced load on the data lines and used familiar DDR2 SDRAM devices that were already standardized, e.g., according to the JESD79-2 standard. Therefore, the proposed combination relies on known methods of interfacing with

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memory devices and memory controllers according to the familiar JEDEC standards, thereby yielding predictable results which would have further motivated a Skilled Artisan. The combination also uses techniques that improved one device, like Ellsberry's disclosure about operating two ranks of DDR SDRAM memory devices that are accessible through data buffering and can perform rank multiplication, to improve a similar device, like Perego's module that also buffers data signals and can use DDR SDRAM devices in a similar way. Therefore, the proposed combination provided predictable results, namely Perego's module with DDR SDRAM devices using Ellsberry's techniques to operate the module with multiple ranks and data buffering according to the JEDEC standards, thereby advantageously reducing the load on the data lines and allowing for rank multiplication. Furthermore, a Skilled Artisan would have recognized that, because both Perego and Ellsberry disclose buffering data signals and using JEDEC compliant memory devices, they provide alternative, predictable solutions for operating memory modules with data buffering capabilities in accordance with the JEDEC standards. Therefore, it would have been at least obvious to a Skilled Artisan to try the proposed combination.

200. Details of the combination of Ground 1 and Ellsberry and further motivations to make specific details of the combination will be discussed below with reference to specific claim limitations.

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3. Ground 3: Ground 1 and Halbert (EX1078)

201. As mentioned above, Ground 3 involves Ground 1 (Perego in view of JESD79-2) in further view of Halbert. *Supra* ¶178. Halbert is analogous art to Perego, JESD79-2, and the 215 Patent, because Halbert is also directed to solving the problem of efficiently organizing and using memory systems, including expanding the capacity of memory modules in DIMM format that can be used in the memory systems at the time. EX1078 at 1:16-19 ("This present invention relates generally to digital memory devices and systems, and more particularly to memory module architectures and methods for operating such devices and systems."). In particular, Halbert's "memory module configurations and access methods … can improve on the dual-bank registered DIMM in several respects. For instance, one embodiment describes a DIMM that can, with the same type of devices, number of devices, and data signal pins as the dual-bank registered DIMM, provide twice the data rate of the registered DIMM. This configuration can also allow the memory devices to operate at voltage levels independent of the voltage levels of the memory system that the module is attached to. The exemplary embodiments also allow the memory devices to be isolated from the full capacitive loading effects of the system memory data bus. Further, the memory devices of the embodiments avoid arrangements of competing memory banks that load each other, as is the case with a dual-bank DIMM. Finally, with the disclosed

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embodiments there is less need for complex logic, within the memory devices themselves, in order to increase the bandwidth of the memory system." EX1078 at 3:58-4:8. Halbert also discloses that the "types, sizes, or numbers of memory devices selected for use with the present invention are not critical. Some possible device types include dynamic random access memory (DRAM) devices, synchronous DRAM (SDRAM) devices including double-data-rate (DDR) SDRAM devices." *Id*. at 9:55-59. As discussed above, a Skilled Artisan would have understood that such memory devices were standardized by JEDEC, including the JESD79-2 standard for second generation DDR SDRAM devices. *See supra* ¶¶49-50, 169-170.

202. Furthermore, like Perego, Halbert uses a similarly-structured memory module including ranks of SDRAM devices and data buffering, and describes similar issues and solutions to operate such a module, including operations in response to consecutive memory commands. EX1078 (Halbert) at Fig. 4 (reproduced below annotated, red indicating buffering functionalities and green and blue indicating two ranks of memory devices.)

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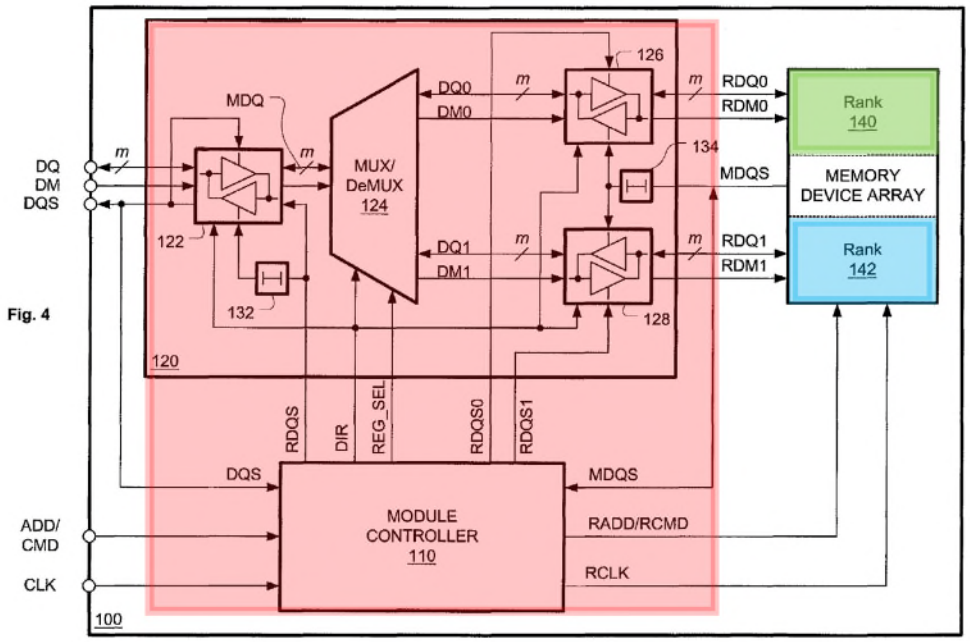

Specifically, Halbert describes memory modules having multiple ranks (like 140 and 142 in Fig. 4, sometimes also called "banks" of memory devices), a phase-locked-loop (PLL), and a register (in Module Controller 110 in Fig. 4) that buffers address and command signals. EX1078 at 2:23-46. Additionally, Halbert describes buffering data signals and data strobes (in data interface circuit 120 in Fig. 4) and shows timing diagrams illustrating consecutive signals and corresponding latencies. *Id.* at Figs. 3 and 5-6. Therefore, a Skilled Artisan would have been motivated to look at analogous art like Halbert for details of implementing memory modules with data buffering. For example, a Skilled Artisan would have been motivated to combine Halbert's teaching about the timing of subsequent read commands and the corresponding delays of the read data

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through the data buffer with the JEDEC requirements for latencies of memory devices and memory modules in order to implement JEDEC compliant memory systems.

203. For example, Halbert explains that its system seeks to be "compatible with an existing memory controller/bus and with existing memory devices." *Id.* at 3:48-57. A Skilled Artisan would have recognized that such components and devices would have included those described in various JEDEC standards, including JESD79-2, and would have also naturally considered purported improvements on those standards, such as those disclosed by Perego. Accordingly, a Skilled Artisan would have been motivated to combine Halbert's teachings with the teachings of the Perego-JESD79-2 combination. A Skilled Artisan would have also recognized that applying the Halbert's teachings to the teachings of the Perego-JESD79-2 combination would have resulted in a predictable variation of the Perego-JESD79-2 combination, which would improve similar devices in the same way and not yield unexpected results or challenges in implementation.

204. Accordingly, the proposed combination of Perego, Halbert, and the JESD79-2 standard uses elements that were familiar to a Skilled Artisan at the time. For example, both Perego's and Halbert's memory modules include known data buffering functionalities and known SDRAM devices according to the JEDEC standards, including the JESD79-2 standard at the time. As discussed above, a

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Skilled Artisan would have also known that data buffering advantageously provides load reduction, allowing to increase the capacity of memory modules. The proposed combination also relies on known methods of interfacing with memory devices and memory controllers according to the familiar JEDEC standards. For example, Halbert and JESD79-2 disclose timing requirements for organizing read and write operations according to preset latencies, such as CAS latencies, and a Skilled Artisan would have understood how to implement and adjust these standard timing requirements in the module of Perego. A Skilled Artisan would have understood that buffering both address/command and data signals on the module allows advantageously operating multiple memory ranks, including implementing the rank multiplication techniques. Thereby, the combination yields predictable results which would have further motivated a Skilled Artisan. The combination also relies on techniques that improve one device, like Halbert's disclosure about operating SDRAM memory devices in multiple ranks that are accessible through data buffering that delays the data signals, to improve a similar device, like Perego's module that also buffers data signals and can use SDRAM devices according to the JEDEC standards. Therefore, the proposed combination provided predictable results, namely Perego's module with DDR SDRAM devices using Halbert's techniques to operate the module, which has multiple ranks and uses data buffering, in accordance with the

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JEDEC standards. Furthermore, a Skilled Artisan would have recognized that, because both Perego and Halbert disclose buffering data signals and using JEDEC compliant memory devices, they provide predictable solutions for operating memory modules with multiple ranks and data buffering capabilities in accordance with the JEDEC standards. Therefore, it would have been at least obvious to a Skilled Artisan to try the proposed combination.

205. Details of the combination of Ground 1 and Halbert and further motivations to make the specific combination will be discussed below with reference to specific claim limitations.

4. Ground 4: Ground 1 and Matsui2 (EX1082)

206. As mentioned above, Ground 4 involves Ground 1 (Perego in view of JESD79-2) in further view of Matsui2. *See supra* ¶179. Matsui2 is analogous art to Perego, JESD79-2 and the 215 Patent, since Matsui2 is also directed to solving the problem of efficiently organizing and using memory systems, including high speed operations. EX1082 (Matsui2) at [0001] ("This invention relates to a memory device operable at a high speed and a memory system comprising a plurality of memory systems of the type."). Like Perego, JESD79-2 and the 215 Patent, Matsui2 also uses double data rate (DDR) SDRAM devices. *Id*. at [0002] ("In order to operate a DRAM (Dynamic Random Access Memory) as one of memory devices at a high speed, proposal is also made of a DDR (Double Data

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Rate) solution in which a data rate can be doubled by carrying out data input/output in synchronism with both of leading and trailing edges of each clock."). For example, Perego discloses examples of memory devices include double data rate (DDR), e.g., DDR2 Synchronous DRAM (SDRAM) memory devices (EX1071 at 3:62-4:12 & 10:54-67), which were standardized in by the JEDEC standards, including JESD79-2. Therefore, a Skilled Artisan would have been motivated to look at analogous art like Matsui2 to implement Perego's module with double data rate memory devices in accordance with the JEDEC standards, like JESD79-2.

207. In particular, Matsui2 is directed to "a memory system comprising a plurality of memory devices connected to a data bus in a branched arrangement, which is capable of reading data from the memory devices at a high speed by effectively preventing reflection between the data bus and each memory device" and "is capable of carrying out antireflection control adapted to a read state or a write state." EX1082 (Matsui2) at [0011-12]. Accordingly, a Skilled Artisan would have been motivated to look at Matsui2 in order to implement Perego's module with DDR memory devices which can prevent signal reflections during read and write operations at high speeds.

208. Accordingly, a Skilled Artisan would have been motivated to combine Matsui2's teachings with the teachings of the Perego-JESD79-2

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combination. A Skilled Artisan would have also recognized that applying the Matsui2's teachings to the teachings of the Perego-JESD79-2 combination would have resulted in a predictable variation of the Perego-JESD79-2 combination, which would improve similar devices in the same way and not yield unexpected results or challenges in implementation. In particular, the combination relies on familiar elements, including Perego's memory module with DDR2 SDRAM devices according to the JESD79-2 standard and Matsui2's termination circuits that operated according to known methods yielding the predictable result of preventing signal reflections during read and write operations.

209. Details of the combination of Ground 1 and Matsui2 and further motivations to make the specific combination will be discussed below with reference to specific claim limitations.

B. Claims 1-29 Are Unpatentable Over Ground 1, Ground 2, Ground 3, and/or Ground 4

210. As explained below, it is my opinion that claims 1-29 are unpatentable in view of (1) Ground 1 (Perego and JESD79-2), (2) Ground 2 (Perego, JESD79-2, and Ellsberry), (3) Ground 3 (Perego, JESD79-2, and Halbert), and/or (4) Ground 4 (Perego, JESD79-2, and Matsui2).

1. Claim 1 is Unpatentable

211. In my opinion, Claim 1 is unpatentable because it is obvious in view of Grounds 1-4.

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a) [1.a] Preamble

(1) [1.a.1] Memory Module

212. The preamble of Claim 1 requires "*[a] memory module*."

213. To the extent the preamble is limiting, the prior art references in Ground 1 (Perego by itself or in combination with JESD79-2) teach this limitation to a Skilled Artisan. This limitation is also taught by Grounds 2-4 at least because they include Ground 1.

214. Perego discloses a "*memory module*." EX1071 (Perego) at 1:21-23 ("Memory capacity is commonly upgraded via memory modules or cards featuring a connector/socket interface."). In particular, Perego discloses a "*memory module*," such as memory subsystem 340, buffered module 395, and memory modules 400, 450, and 470. *E.g.*, *id.* at Fig. 3B (annotated version reproduced below in part) and Figs. 3C and 4A-4C (annotated version reproduced below), 6:57-60 ("FIG. 3B [illustrates] an exemplary system that uses configurable width modules"), 7:30-33 ("FIG. 3C shows an example of a configurable width buffered module 395 that can be used in conjunction with the system described above"), 9:26-33 ("With reference to FIGS. 4A, 4B and 4C, buffered memory modules according to embodiments of the present invention are shown"); *see also id.* at Title ("Configurable width buffered module") and Abstract ("A memory system

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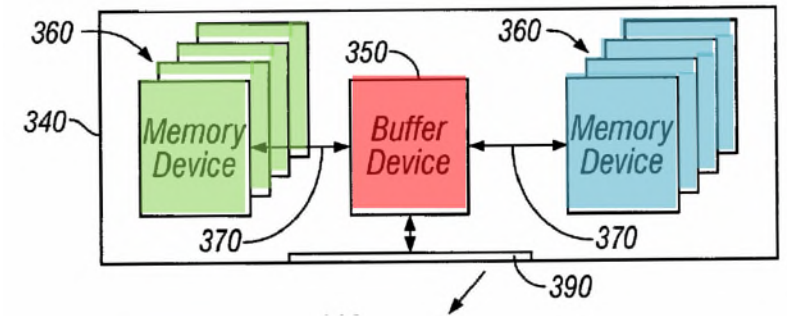
architecture/interconnect topology includes a configurable width buffered module having a configurable width buffer device.”).



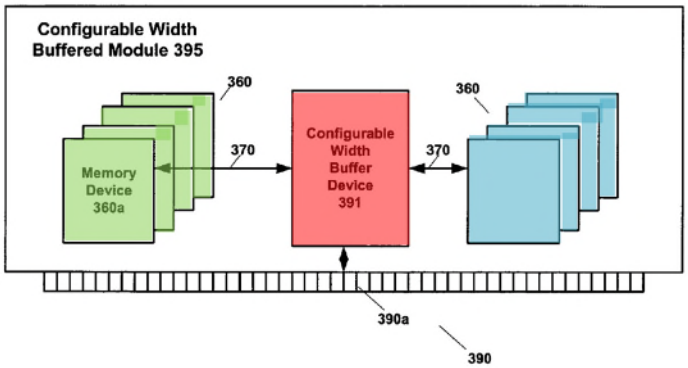


Fig. 3C

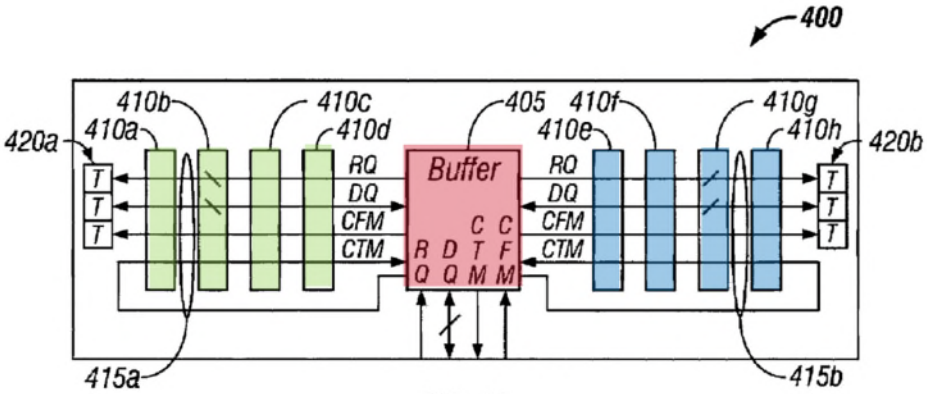


FIG. 4A

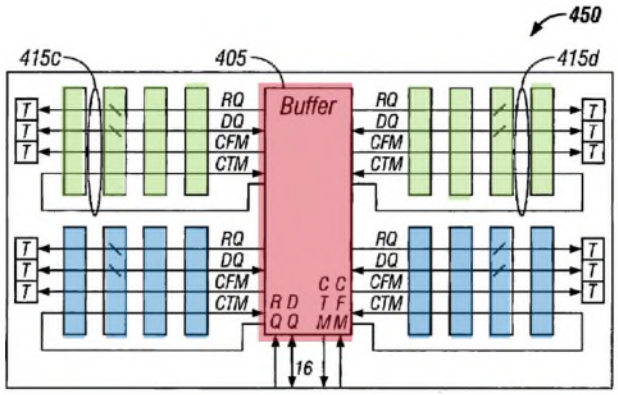


FIG. 4B

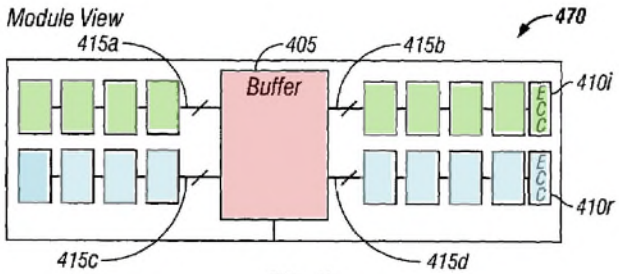


FIG. 4C

215. I note that Perego's buffered module has substantially the same structure as that of the 215 Patent: a buffer device (red) communicates, on one hand, with a system memory controller on a system memory bus and, on the other hand, with different sets of memory devices (green, blue) on the module using a respective data bus for each of those sets of memory devices. *Compare* EX1001 at FIG. 1, *with* EX1071 at FIG. 3B (both reproduced below with annotations).

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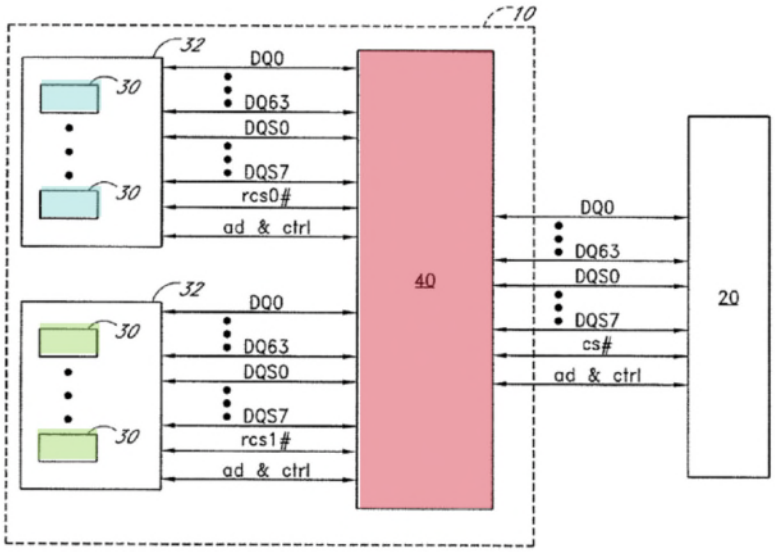
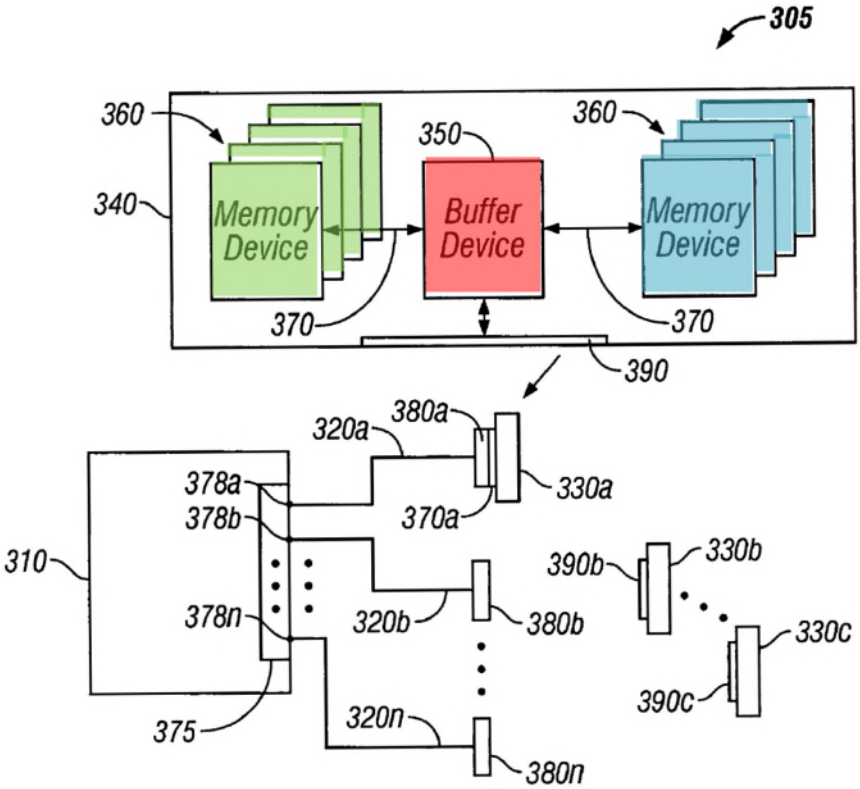
215 Patent	 FIG. 1
Perego	 FIG. 3B

216. Accordingly, to the extent the preamble of claim 1 is limiting, Perego discloses "*[a] memory module*" as recited by Claim 1.

(2) [1.a.2] Operable in a Computer System

217. The preamble of claim 1 requires that the memory module is "*operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller*."

218. To the extent the preamble is limiting, the prior art references in Ground 1 (Perego by itself or in combination with JESD79-2) teach this limitation to a Skilled Artisan. This limitation is also taught by Grounds 2-4 at least because they include Ground 1.

219. Perego discloses that its memory module is operable in a computer system (e.g., a personal computer or server including memory system 305) to communicate data (through a respective link, e.g., 320a) with a memory controller (e.g., memory controller 310) of the computer system via a memory bus (e.g., in link 320a) in response to memory commands (such as read and write commands) received from the memory controller 310 through the link 320a. *See, e.g.*, EX1071 (Perego) at FIG. 3B (annotated version reproduced below).

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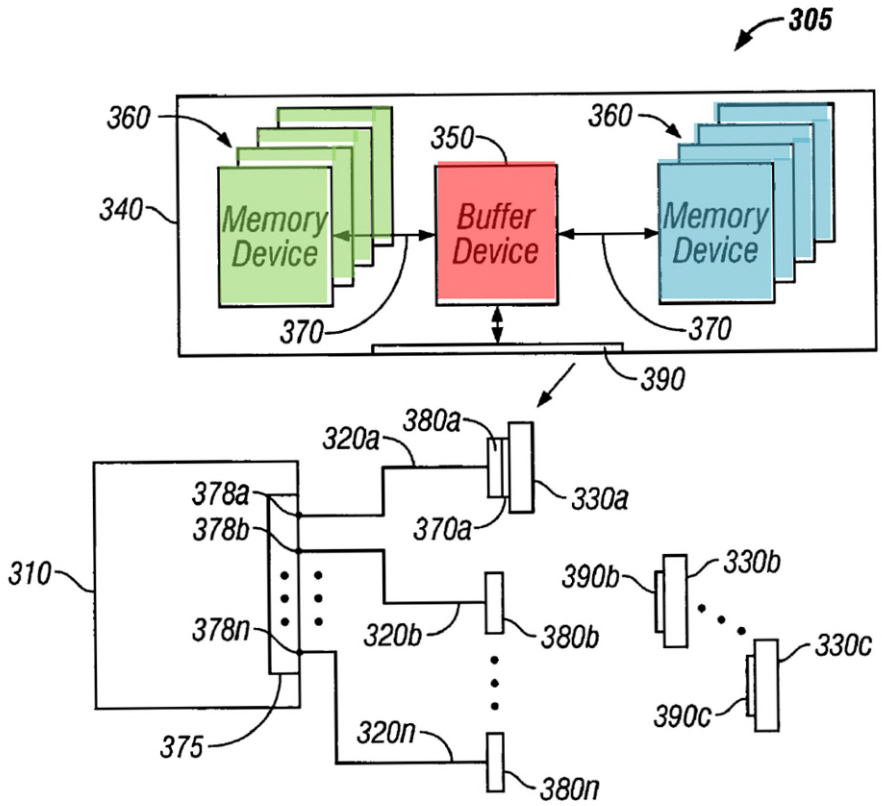

FIG. 3B

220. In particular, Perego discloses that its memory module is "*operable in a computer system,*" such as "a personal computer or server." *Id.* at 3:13-22. Perego further explains that, "[i]n several embodiments, one or more busses or a plurality of point-to-point links may be used to couple one or more buffer devices to a master." EX1071 (Perego) at 3:41-47. For example, "[m]emory systems 300 and 305 include a controller 310, a plurality of point-to-point links 320a-320n, and a plurality of memory subsystems 330a-330n. For simplicity, a more detailed embodiment of memory subsystem 330a is illustrated as memory subsystem 340." *Id*. at 4:65-5:4. "Interface 375 disposed on controller 310 includes a plurality of

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memory subsystem ports 378a–378n.… One of memory subsystem ports 378a–378n includes I/Os, for sending and receiving data, addressing and control information over one of point-to-point links 320a–320n. According to … embodiments, memory subsystems are connected to a memory subsystem port via a bus (i.e., a plurality of signal lines)." *Id.* at 5:6-24.

221. Perego discloses multiple examples of a bus between a system memory controller and one or more memory modules. EX1071 (Perego) at Figs. 1, 2A, and 2B. In the example of Fig. 1, the bus includes "control/address bus 130, data bus 140, and corresponding module control lines 150a-150c. Control/address bus 130 typically comprises a plurality of address lines and control signals (e.g., RAS, CAS and WE)." *Id*. at 1:34-40, Fig. 1 (reproduced below).

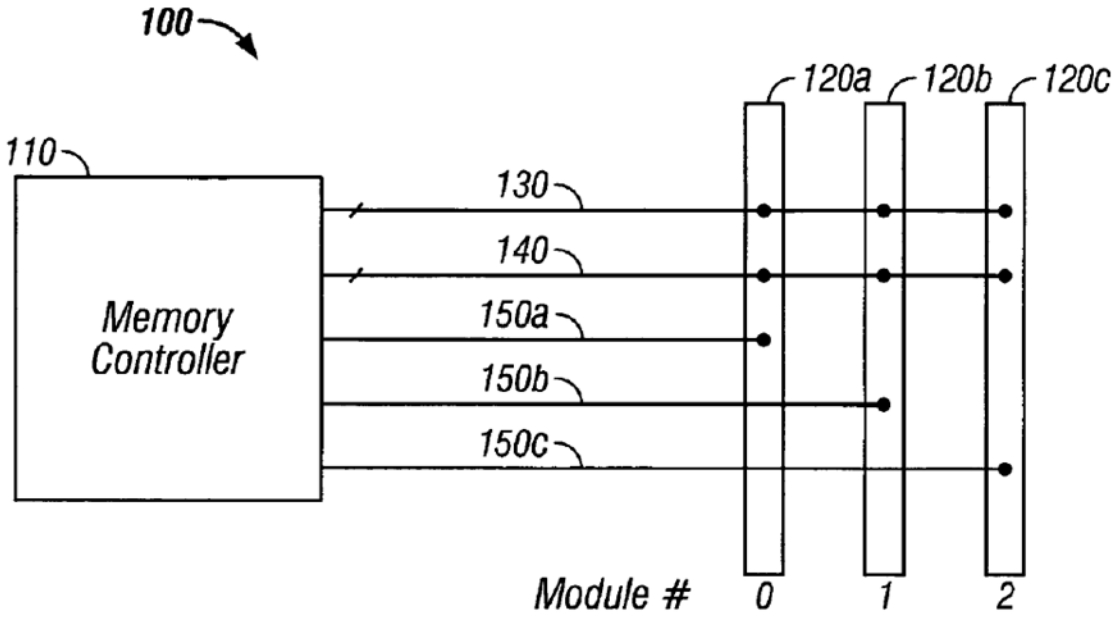

FIG. 1
(Prior Art)

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A Skilled Artisan would have understood from this disclosure that an example of the bus shown in Perego's Fig. 1 is a JEDEC-style bus where the control/address bus 130 correspond to DDR SDRAM command lines including RAS, CAS, and WE command lines, and the module control lines 150a-150c include chip select (CS) signals in accordance with the JEDEC standard for DDR SDRAM devices. *See, e.g.*, EX1064 (JESD79-2) at 6 (listing pin-out for RAS, CAS, and WE command inputs, and CS chip select "for external Rank selection"); *see also* EX1062 (JESD21-C) at 6 (Pin description for RDIMM modules listing pins for RAS, CAS, WE, and S0-S3, the latter corresponding to SDRAM chip selection lines); EX1066 at 6 (similar). Another example of a memory bus, called Synchronous Link, is also disclosed by Perego. EX1071 (Perego) at Fig. 2 (reproduced below). This bus architecture also includes Command Link lines and separate Data Link lines. *Id*.

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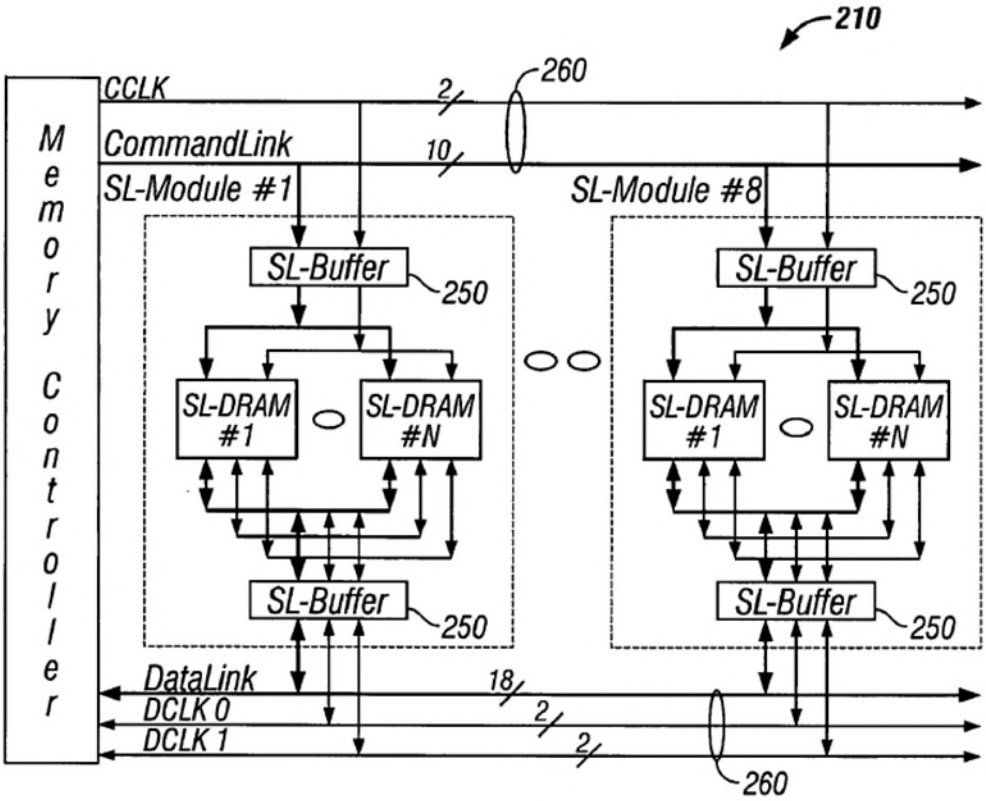

FIG. 2B
(Prior Art)

Perego further explains that "the bussed approaches lend efficiency towards resource utilization of a system and permits module interfacing for upgradeability." *Id*. at 2:22-25. Indeed, Perego's buffer device provides "upgrade flexibility … among a variety of possible module configurations in the system." *Id*. 3:23-28; *see also id*. at 6:34-40 ("Buffer device 350 provides a high degree of system flexibility. New generations of memory devices may be phased in with controller 310 or into memory system 300 by modifying buffer device 350. Similarly, new generations of controllers may be phased in….").

222. A Skilled Artisan would have understood from this disclosure that link 320a constitutes a "*memory bus*" because it is using a plurality of signal lines for communicating "data, addressing and control information" between controller 310 and memory module 340. EX1071 (Perego) at Fig. 3B and 5:6-24. A Skilled Artisan would have also understood that link 320a can include a JEDEC style or a Synchronous Link bus which has a number of data lines for communicating data and separate lines for control, for example, when Perego's module is configured to update a memory system similar to that shown in Figs. 1 and 2b of Perego, respectively. Perego references busses in numerous locations in the specification with respect to his invention. *See, e.g.*, EX1071 (Perego) at 3:41-47; 5:16-31; 8:27-50; 8:60-65; 9:9-12; 9:34-36; and 15:7-14. Therefore, Perego discloses that the "*memory bus*" includes data lines (DQ) "*to communicate data with a memory controller* [310] *of the computer system*." *Supra* at ¶221, EX1071 (Perego) at Figs, 4A and 4B (showing separate DQ and RQ lines for data communication and control signals of the system controller).

223. Perego also discloses that its system's "*memory bus*" can have a data width of W_{DP}=16, 32, 64, or 128 "*to communicate data with a memory controller* [310] *of the computer system*." EX1071 (Perego) at Fig. 5B (reproduced below with annotations), 14:16-51 ("Configurable width buffer device 391 has a maximum buffer device interface width equivalent to the number of data pins or

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contacts provided on the buffer device's package or interface 596. In an embodiment of the present invention, interface 596 includes 128 pins of which selectable subsets of 1, 2, 4, 8, 16, 32, 64 or all 128 pins (W_{DP}) may be used in order to configure the width of configurable width buffer device 391."); *see also id*. at Fig. 5A & 11:8-12 ("In an embodiment, interface 510 couples to external point-to-point link 320 (e.g., point-to-point links 320a–320n in FIGS. 3A and 3B). Interface 510 includes a port having transceiver 575 (i.e. transmit and receive circuit) that connects to a point-to-point link.").

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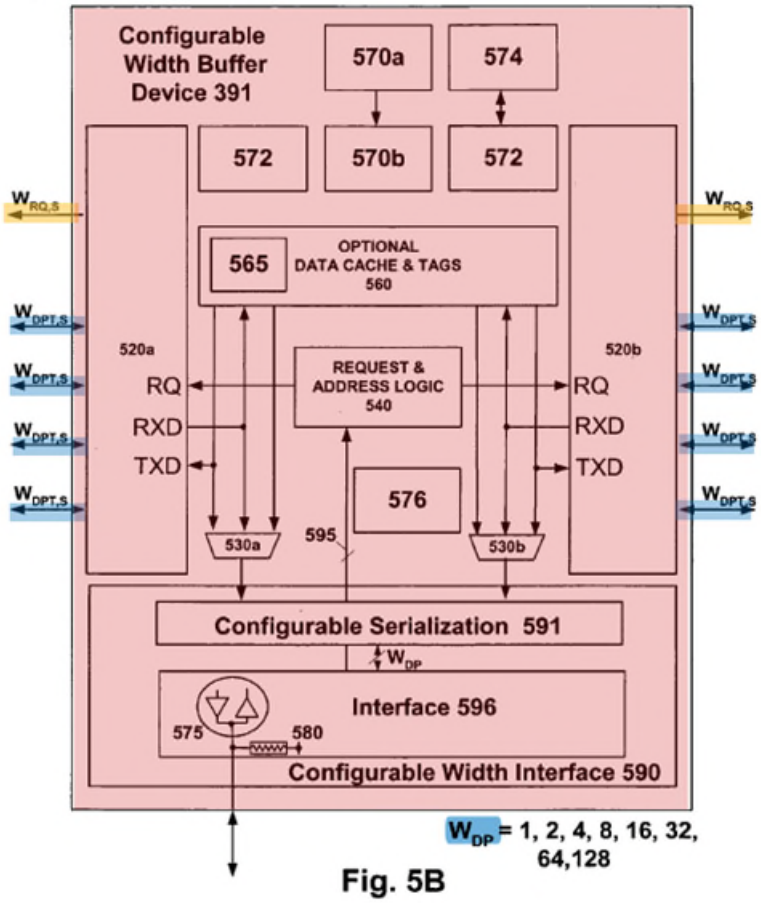
Configurable Width Buffer Device 391
570a
574
572
570b
572
OPTIONAL DATA CACHE & TAGS 560
565
520a
520b
REQUEST & ADDRESS LOGIC 540
RQ
RXD
TXD
RQ
RXD
TXD
576
530a
595
530b
Configurable Serialization 591
Interface 596
575
580
Configurable Width Interface 590
= 1, 2, 4, 8, 16, 32, 64,128

Fig. 5B

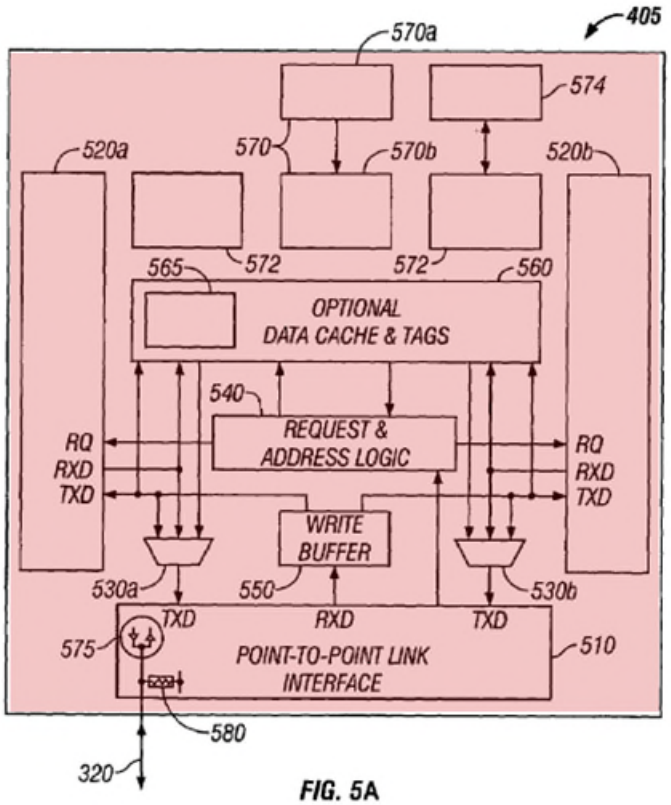

FIG. 5A

224. For example, Perego discloses a data width of W_{DP}=64, which a Skilled Artisan would have understood corresponds to a 64-bit data width of a JEDEC-compliant registered DIMM module, according to the JEDEC standard JESD21-C. *Id.* at 2:4-6 (disclosing "contemporary dual inline memory module (DIMM) having one or more discrete buffer devices"); EX1062 (JESD21-C) at p. 5 ("This specification defines the electrical and mechanical requirements for 184-pin, 2.5 Volt, PC1600/PC2100, 64/72 bit-wide, Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR SDRAM DIMMs). These SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations. PC1600/PC2100 refers to the JEDEC

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standard DIMM naming convention in which PC1600 indicates a 184-pin DIMM running at 100 MHz clock speed and offering 1600MB/s bandwidth.”).

225. Perego also discloses that its module and the memory devices in the module communicate data “*in response to memory commands received from the memory controller*” through control lines (RQ), e.g., when the link 320a includes control/address lines of a JEDEC style bus or the Command Link lines of a Synchronous Link bus. *Supra* at ¶221. In particular, Perego discloses that the data is communicated in response to read and write commands received from the memory controller through the control lines (RQ). EX1071 at 3:62-4:12 (“A memory device stores data (which may be retrieved) associated with a particular address provided, for example, as part of a write or read command.”), 9:50-60 (“control lines (RQ) transport control (e.g., read, write, precharge ...) information and address (e.g., row and column) information”); *see also, e.g.*, *id.* at FIG. 3B & 6:15-25 (“In a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370. One or more of memory devices 360 may respond by transmitting data to Buffer device 350 which receives the data via one or more of channels 370 and in response, transmits corresponding signals to controller 310 via

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point-to-point link 320a. Controller 310 receives the signals corresponding to the data at corresponding ports 378a–378n.”).

226. A Skilled Artisan would have understood from Perego’s disclosure of “control lines (RQ) transport[ing] control (e.g., read, write, precharge ...) information” that such control information includes read and write commands from the memory controller. *Id.* at 9:50-53, FIG. 5B. Perego further discloses that “control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines.” *Id*. at 9:58-60. In addition, Perego discloses using DDR2 SDRAM devices. *Id*. at 3:62-4:3, 8:1-4, 10:56-58. Perego explains that these devices can receive read and/or write commands. *Id*. at 3:62-4:3.

227. A Skilled Artisan would have also understood from this disclosure that DDR2 SDRAM devices have individual control lines, including “row address strobe” (RAS) and “column address strobe” (CAS) lines, as well as “address lines” (e.g., A0-A15), because they comply with JEDEC standards that describe the specific ways to issue read and write commands to those memory devices using individual “row address strobe, column address strobe, etc., and address lines.” EX1064 (JESD79-2) at pp. 24-33 (Section 2.2.4, “Read and Write Access Modes”) & 49 (showing Row Address Strobe “$\overline{\text{RAS}}$” and Column Address Strobe “$\overline{\text{CAS}}$” signals used to convey memory read and write commands for a DDR2 SDRAM).

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A Skilled Artisan would have also understood that chip-select signals are also part of the read and write commands for DDR SDRAM devices. *Id.*, *see also id.* at 6 ("CS is considered part of the command code."), 49 n.1 (similar).

Table 10 — Command truth table.

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1,2
Refresh (REF)	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1,7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.

NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

NOTE 3 Burst reads or writes at BL=4 cannot be terminated or interrupted. See sections "Reads interrupted by a Read" and "Writes interrupted by a Write" in section 2.2.4 for details.

NOTE 4 The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined in section 2.2.7.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See section 2.2.2.4.

NOTE 6 "X" means "H or L (but a defined logic level)".

NOTE 7 Self refresh exit is asynchronous.

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Id. at p. 49 (Table 10). Although this understanding would have been within a Skilled Artisan's knowledge, a Skilled Artisan would have alternatively been motivated to combine these teachings from JESD79-2 to Perego, given that by doing so the Skilled Artisan would have implemented predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results or challenges in implementation. Indeed, a Skilled Artisan would have understood that JESD79-2 provides details about operating DDR2 SDRAM devices, thus she would have been motivated to look to JESD79-2 to find out those details and to incorporate them when Perego's module is implemented with DDR2 SDRAM devices. EX1071 at 10:56-59 ("memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices"). *Supra* at ¶¶182-192.

228. Accordingly, Perego, either by itself or in combination with JESD79-2, discloses that its memory module is "*operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller*."

(3) [1.a.3] First and Second Memory Command

229. The preamble of Claim 1 requires "*the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data*

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burst and the second memory command to cause the memory module to receive or output a second data burst."

230. To the extent the preamble is limiting, the prior art references in Ground 1 (Perego by itself or in combination with JESD79-2) teach this limitation to a Skilled Artisan. This limitation is also taught by Grounds 2-4 at least because they include Ground 1.

231. Perego discloses to a Skilled Artisan that the memory commands include a first memory command (write or read) and a subsequent second memory command (subsequent write or read), the first memory command to cause the memory module to receive (for a write command) or output (for a read command) a first data burst (e.g., in accordance with the corresponding DDR standard) and the second memory command to cause the memory module to receive or output a second data burst (in accordance with the corresponding DDR standard).

232. For example, Perego discloses using DDR SDRAM devices that store or retrieve data in response to "a write or read command." EX1071 (Perego) at 3:64-4:12, 8:1-4, 10:56-58. A Skilled Artisan would have understood that, in accordance with corresponding standards for DDR SDRAM devices, a first read or write command is ordinarily followed by a second read or write command. *See, e.g.,* EX1064 (JESD79-2) at pp. 24-33 (DDR2 SDRAM Specification at Section 2.2.4 entitled Read and Write Access Modes). For example, Figure 26 of JESD79-

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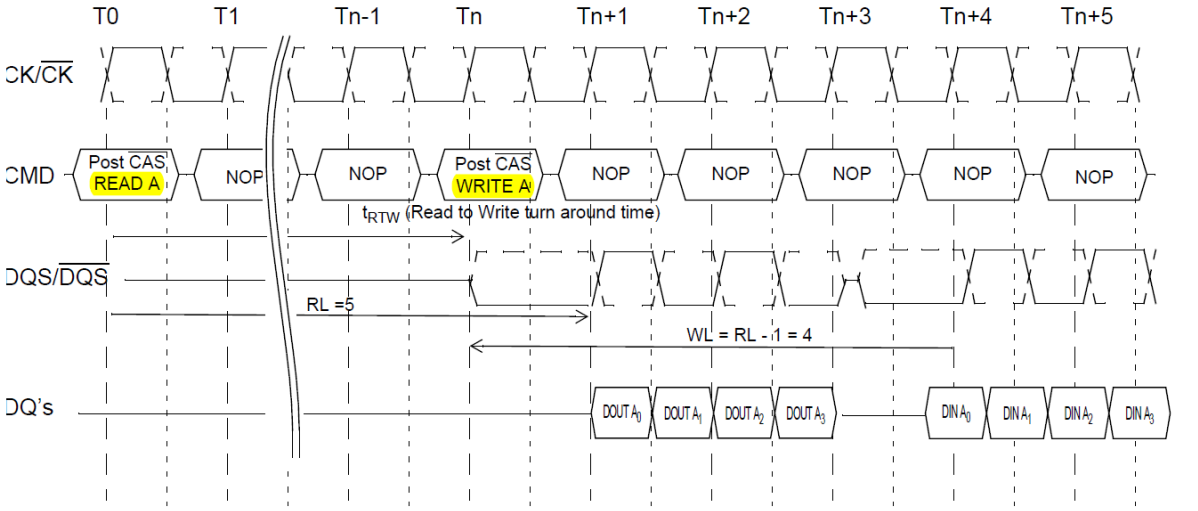
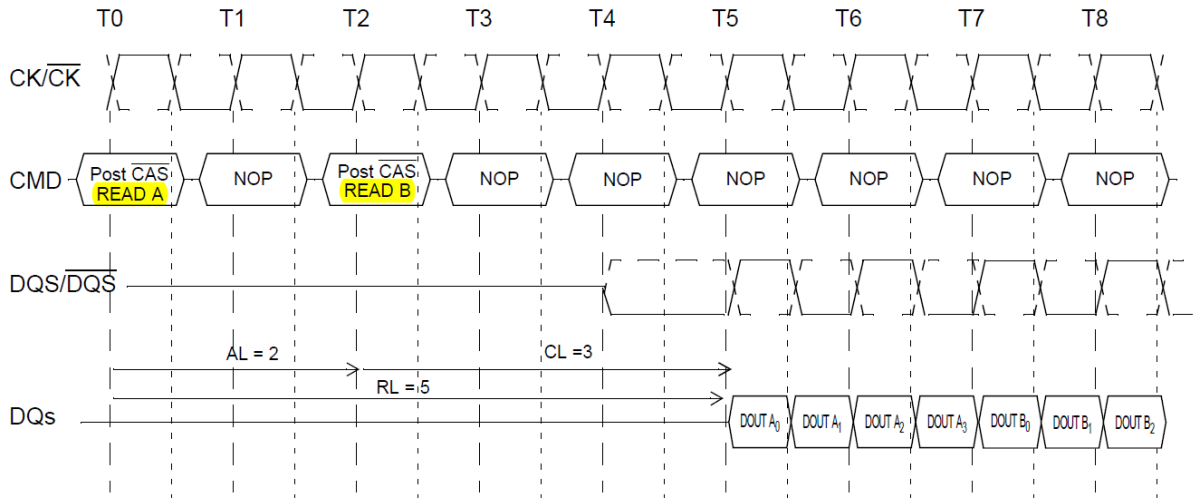
2 (reproduced below) shows an example of a read command followed by a write command:



The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation.

Figure 26 — Burst Read Followed by Burst Write: RL = 5, WL = (RL-1) = 4, BL = 4

Id. at p. 28. Figure 27 of JESD79-2 similarly shows an example of a read command followed by another read command in a "seamless burst read operation":



The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 27 — Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

Id.

233. A Skilled Artisan would have also understood that DDR SDRAM devices at the time of the invention transmitted or received the data in bursts. *See, e.g.*, EX1064 (JESD79-2) at pp. 25-32 (including Sections 2.2.4.2 (Burst Mode Operation), 2.2.4.3 (Burst Read Command), and 2.2.4.4 (Burst Write Operation)). A Skilled Artisan would have understood that, in the DDR SDRAM devices, the data is communicated according to a predefined schedule. For example, as shown in Figure 25 of JESD79-2 (reproduced below), a DDR2 SDRAM can be programmed to operate with a read latency (RL) of three and a burst length (BL) of eight, so that after a Read command is received at time T0, the memory starts at time T3 to transmit a burst of eight bits of data.

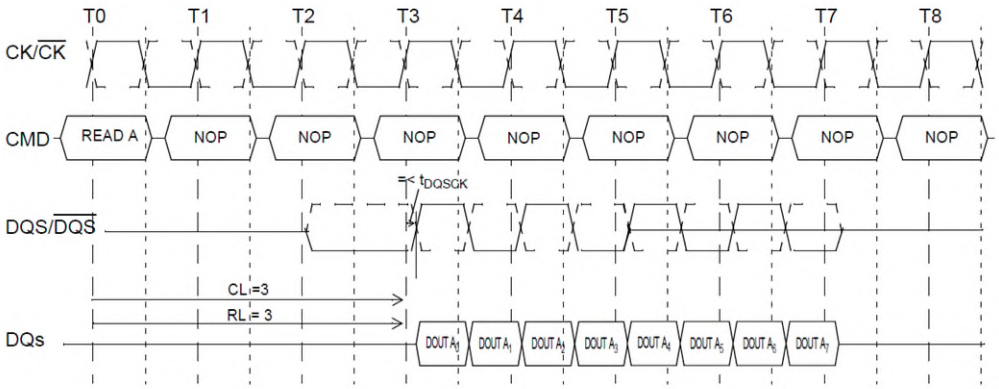


Figure 25 — Burst Read Operation: RL = 3 (AL = 0 and CL = 3, BL = 8)

Id. at p. 27.

234. Similarly, in a DDR2 SDRAM programmed to operate with a write latency (WL) of two and a burst length (BL) of four, after a Write command is

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received at time T0, a burst of four bits of data is received starting at T2, as shown in Figure 31 of JESD79-2 (reproduced below).

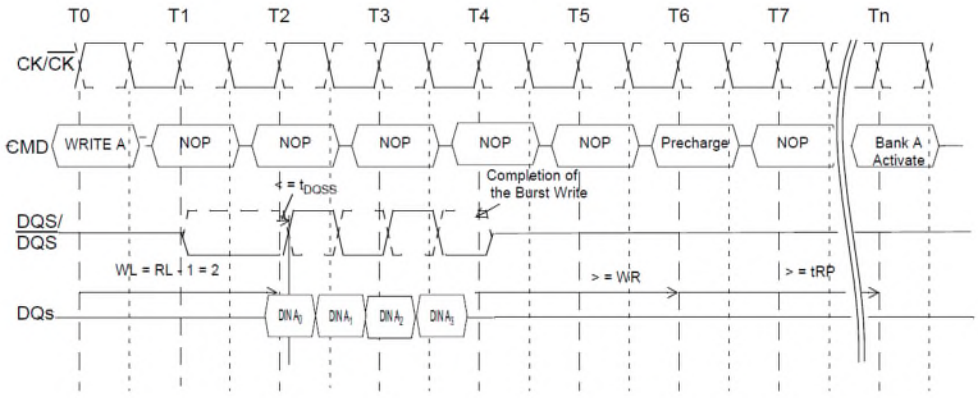

Figure 31 — Burst Write Operation: RL = 3, WL = 2, tWR = 2 (AL=0, CL=3), BL = 4

Id. at p. 30.

235. A Skilled Artisan would have understood that a memory controller can program these latencies and burst lengths by mode register commands, so that the data communication between the memory controller and the memory module is properly synchronized, as shown in Figure 8 of JESD79-2 (partially reproduced below with yellow highlighting).

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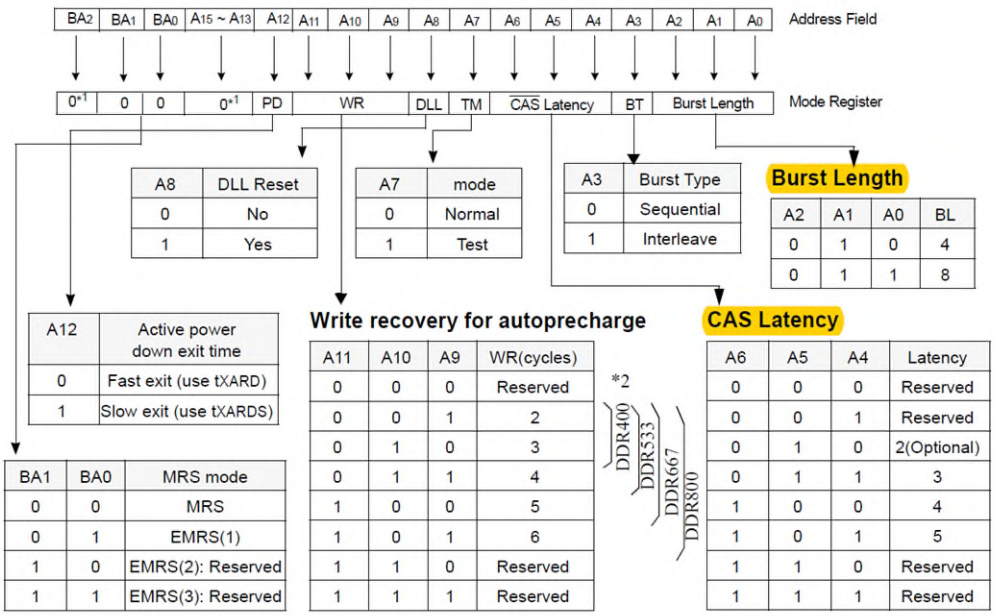

Id. at p. 12.

236. A Skilled Artisan would have also understood that Perego's modules were designed to perform multiple read and write operations over time and output or receive corresponding bursts of data signals, in accordance with the DDR2 standards. For example, Figure 26 of JESD79-2 illustrates subsequent read and write operations:

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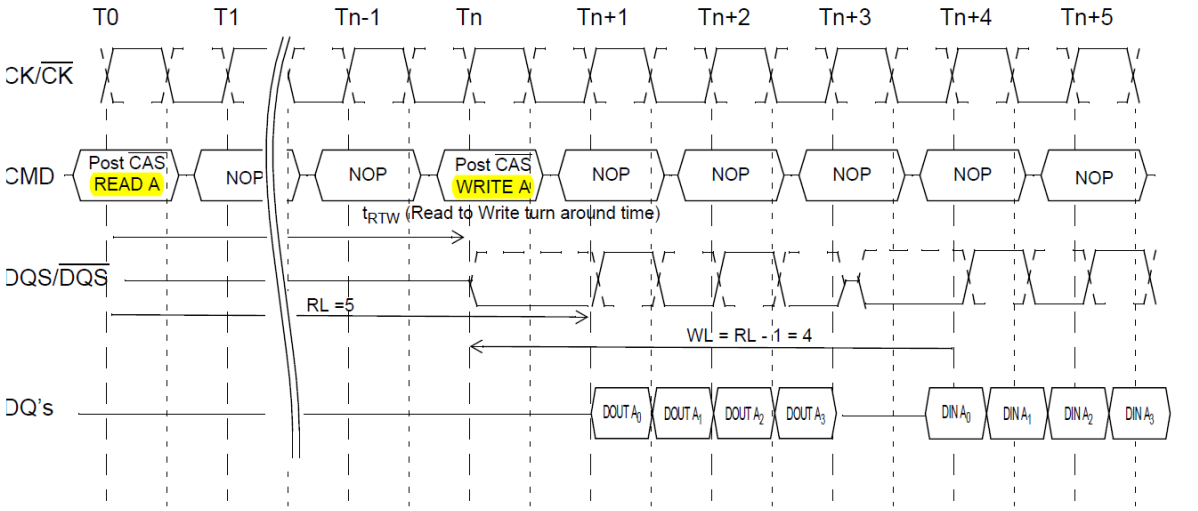

The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation.

Figure 26 — Burst Read Followed by Burst Write: RL = 5, WL = (RL-1) = 4, BL = 4

Id. at p. 28.

237. A Skilled Artisan would have also understood that, in Perego's module, the subsequent memory operations (such as read or write operations) can be directed to different subsets of the memory devices. EX1071 at 7:56-59 ("different subsets of memory devices and memory cells may be accessed through different sets of interface connections").

238. Although the above-described information from the JEDEC standards (including JESD79-2) would have been within a Skilled Artisan's knowledge when reading Perego, a POSITA would have alternatively been motivated to combine these teachings from JESD79-2 to Perego, given that by doing so the Skilled Artisan would have implemented predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results

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or challenges in implementation. Indeed, the Skilled Artisan would have understood that, when Perego's module is implemented by DDR2 SDRAM devices, *see, e.g.*, EX1071 at 10:56-59, the operation details for those memory devices can be found in JESD79-2. Accordingly, a Skilled Artisan would have been motivated to combine the teaching of Perego with that of JESD79-2 in order to operate Perego's DDR2 memory devices properly and efficiently in an optimal manner in accordance with the JESD79-2 standard. *Supra* at ¶¶182-192.

239. Accordingly, Perego, either by itself or in combination with JESD79-2, discloses "*the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst.*"

(4) [1.a.4] Comprising

240. Claim 1 requires "*the memory module comprising.*"

241. As discussed, above, the Grounds 1-4 teach "*[a] memory module*." *See supra* ¶¶212-216. Further, as discussed below, Grounds 1-4 similarly teach the limitations that the *memory module* must comprise. *See infra* ¶¶243-324.

242. Accordingly, the prior art references in Grounds 1-4 satisfy "*the memory module comprising*."

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b) [1.b] Printed Circuit Board

243. Claim 1 requires "*a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system*."

244. The prior art references in Ground 1 (specifically Perego) teach this limitation to a Skilled Artisan. This limitation is also taught by Grounds 2-4 at least because they include Ground 1.

245. Perego discloses that the memory module includes a printed circuit board having a plurality of edge connections (edge connectors 390) configured to be electrically coupled to a corresponding plurality of contacts of a module slot (mating connectors or sockets 380) of the computer system. *See* EX1071 (Perego) at FIGS. 3B and 3C (reproduced with annotations below).

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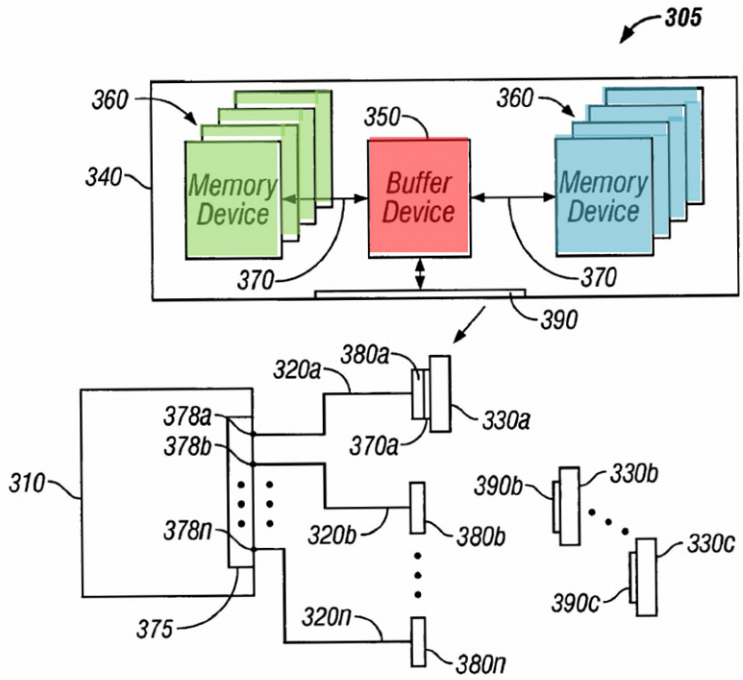

FIG. 3B

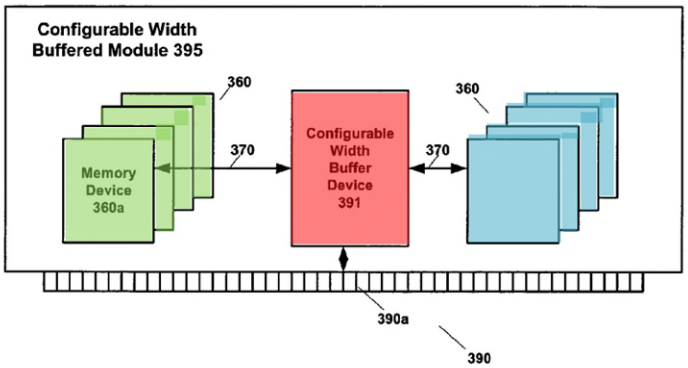

Fig. 3C

246. For example, Perego discloses that the memory modules (also called "memory subsystems" in Perego) "are incorporated onto individual substrates (e.g., ***PCBs***) … that include connectors 390a-390c … Corresponding mating connectors 380a-380n are connected to a connection point of each point-to-point

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link 320a-320n. Each of mating connectors 380a–380n interface with connectors 390a-390c to allow removal/inclusion of memory subsystems 330a-330c in memory system 305. In one embodiment, mating connectors 380a-380n are sockets and connectors 390a-390c are edge connectors disposed on an edge of each memory subsystems 330a-330c. Mating connectors 380a-380n, are attached to a common substrate shared with point-to-point links 320a-320n and controller 310." *Id.* at 5:56-6:11 (emphasis added). "PCB" is a well-known acronym for "printed circuit board." Perego also teaches that "interface connections 390a includes a plurality of contacts, conducting elements or pins." *Id*. at 7:39-41.

247. Furthermore, a Skilled Artisan would have understood from Perego's disclosure that its module can be implemented in a DIMM format, e.g., in order to upgrade a DIMM system with a memory module using a new generation of memory devices, or to use older generations of memory devices with new memory controllers:

> "Buffer device 350 provides a high degree of system flexibility. New generations of memory devices may be phased in with controller 310 or into memory system 300 by modifying buffer device 350. Backward compatibility with existing generations of memory devices (i.e., memory devices 360) may also be preserved. Similarly, new generations of controllers may be phased in which exploit features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices."

Id. at 6:34-43.

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> "For example, the buffer device may be a configurable width buffer device to provide upgrade flexibility and/or provide high bandwidth among a variety of possible module configurations in the system."), 5:64-6:1 ("In another alternate embodiment illustrated in FIG. 3B, memory subsystems 330a–330c are incorporated onto individual substrates that include connectors 390a–390c to support upgradeability in memory system 305."

Id. at 3:25-28. A Skilled Artisan would have understood based on their knowledge of JEDEC standards that such a DIMM format also uses a printed circuit board (PCB) with edge connections to couple to the socket of the memory system. EX1062 (JESD21-C) at p. 29 ("Components shall be surface mounted on both sides of the PCB and positioned on the PCB to meet the minimum and maximum trace lengths required for DDR SDRAM signals.") & p. 66 ("The DIMM printed circuit board design uses….PCB edge connector contacts [that] shall be gold-plated and not chamfered."); *see also* EX1069, p. 2 ("a typical memory module (often called a 'DIMM' for *dual in-line memory module*)").

248. Accordingly, Perego discloses "*a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system*."

c) [1.c] Register

249. Claim 1 requires "*a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command.*"

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250. The prior art references in Ground 1 (Perego by itself or in combination with JESD79-2) teach this limitation to a Skilled Artisan. This limitation is also taught by Grounds 2-4 at least because they include Ground 1.

251. Perego discloses that a "*register*" in its buffer device (e.g., 350) is coupled to the printed circuit board, since the buffer device itself is coupled to the printed circuit board and is configured to receive and buffer (1) first command and address signals representing the first memory command (read or write command received on a link 320) and (2) second command and address signals representing the second memory command. *See, e.g.*, EX1071 (Perego) at FIG. 3B (reproduced with annotations below). For example:

> "Interface 375 disposed on controller 310 includes a plurality of memory subsystem ports 378a–378n. … One of memory subsystem ports 378a–378n includes I/Os, for sending and receiving data, addressing and control information over one of point-to-point links 320a–320n."

Id. at 5:6-15.

> "With further reference to FIGS. 3A and 3B, buffer device 350 transceives and provides isolation between signals interfacing to controller 310 and signals interfacing to the plurality of memory devices 360…. In this embodiment, memory subsystems 330a–330n are buffered modules. By way of comparison, buffers disposed on the conventional DIMM module in U.S. Pat. No. 5,513,135 are employed to buffer or register control signals such as RAS, and CAS, etc., and address signals. Data I/Os of the memory devices disposed on the DIMM are connected directly to the DIMM connector (and ultimately to data lines on an external bus when the DIMM is employed in memory system 100)."

6:12-33.

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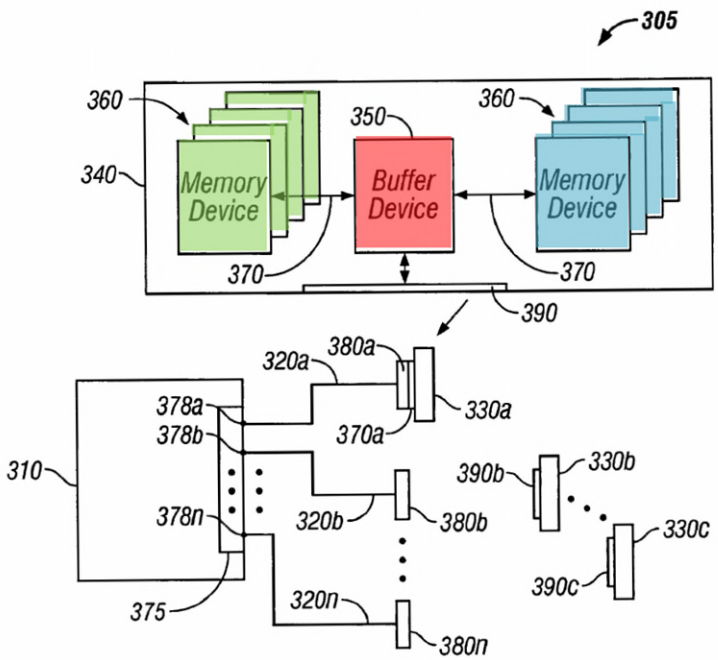

FIG. 3B

252. Perego also discloses that the buffer device includes a "*register*" that is configured to receive and buffer the first and second command and address signals representing the first and second memory commands, respectively. EX1071 at Figs. 5A & 5B (reproduced below with annotations).

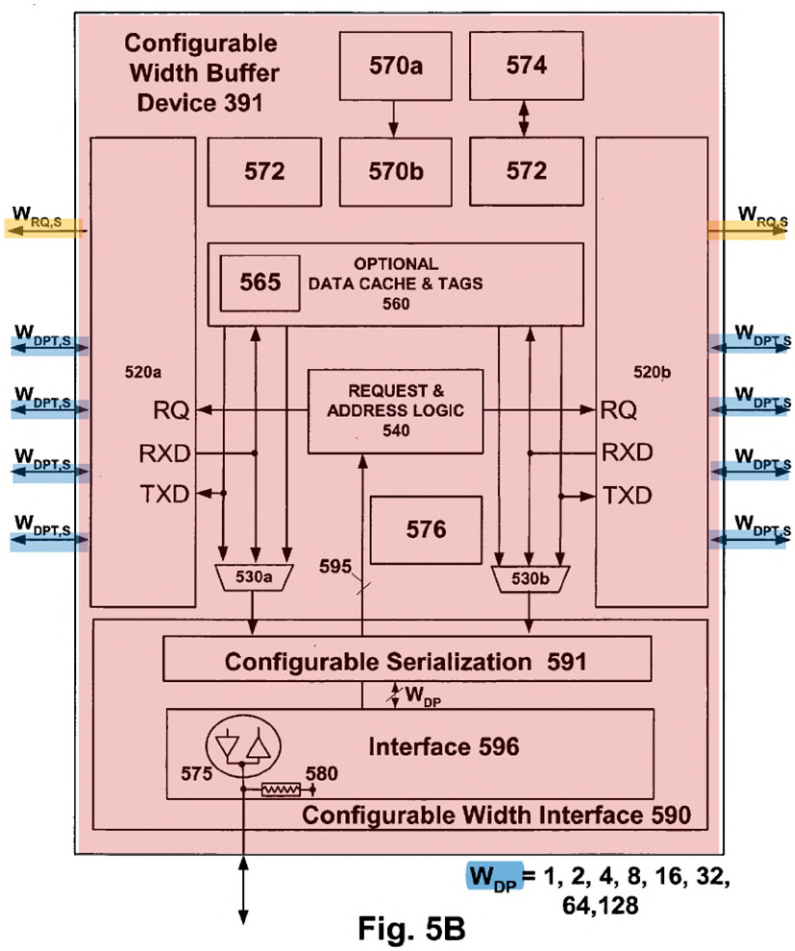
Configurable Width Buffer Device 391
570a
574
572
570b
572
OPTIONAL DATA CACHE & TAGS 560
565
520a
520b
REQUEST & ADDRESS LOGIC 540
RQ
RXD
TXD
576
530a
595
530b
Configurable Serialization 591
Interface 596
575
580
Configurable Width Interface 590
= 1, 2, 4, 8, 16, 32, 64,128

Fig. 5B

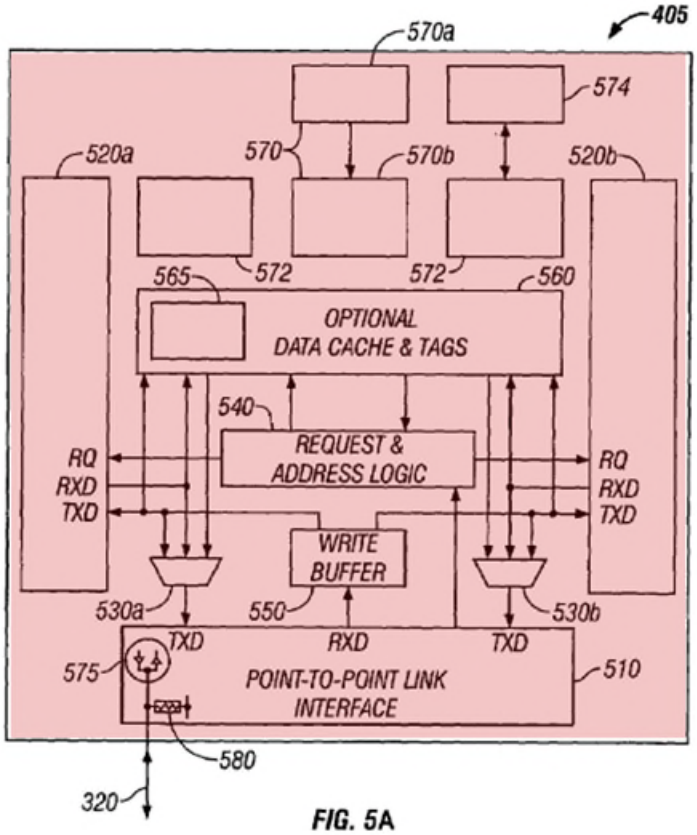

FIG. 5A

253. For example, Perego's disclosure that its "buffer device 350 transceives and provides isolation between signals interfacing to controller 310 and signals interfacing to the plurality of memory devices 360," *id*. at 6:12-15, discloses to a Skilled Artisan that such "transceiv[ing] and providing isolation" includes receiving and buffering the address and command signals in link 320. *See also id*. at 11:8-12 ("Interface 510 includes a port having transceiver 575 (i.e. transmit and receive circuit)"). Perego further discloses request and address logic 540 for decoding "control information and address information," among other tasks. *Id*. at 13:54-59 ("control information and address information may be decoded and separated from multiplexed data and provided on lines 595 to request

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& address logic 540 from interface 596."). A Skilled Artisan would have understood that this "control information and address information" would be registered in at least some disclosed embodiments and represent a corresponding memory command as the receiving of request and address information is naturally associated with a memory command. For example, Perego discloses that its module can include DDR SDRAM devices. EX1071 at 8:1-4 & 10:56-59. A Skilled Artisan would have understood that DDR SDRAM devices respond to read and write commands and corresponding address information. EX1064 at pp. 26 ("The Burst Read command is initiated by having CS and CAS low while holding RAS and WE high at the rising edge of the clock. The address inputs determine the starting column address for the burst."), 29 ("The Burst Write command is initiated by having CS, CAS and WE low while holding RAS high at the rising edge of the clock. The address inputs determine the starting column address."), 49 (Command truth table showing "Write" and "Read" commands include address signals BA0-BA3 and A0-A15).

254. Perego also discloses the following:

> "In a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370. One or more of memory devices 360 may respond by transmitting data to Buffer device 350 which receives the data via one or more of channels 370 and in response, transmits corresponding signals to controller 310 via point-to-point link 320a. Controller 310 receives the signals corresponding to the data at corresponding ports 378a–

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> 378n. In this embodiment, memory subsystems 330a–330n are buffered modules. By way of comparison, buffers disposed on the conventional DIMM module in U.S. Pat. No. 5,513,135 are employed to buffer or register control signals such as RAS, and CAS, etc., and address signals."

EX1071 at 6:15-30.

255. A Skilled Artisan would have understood from this disclosure that the buffer device in Perego includes a "*register*" that receives and registers (and thus buffers) the command and address signals, and thereafter provides registered address and control signals to the memory devices in at least some disclosed embodiments. *See also id*. at 13:54-59 ("For example, control information and address information may be decoded and separated from multiplexed data and provided on lines 595 to request & address logic 540 from interface 596.") and Fig. 5C (showing that interface 596 includes registers, similar to latches 597f-m, for interfacing with the system memory bus). Such registering of the address and command signals was well known at the time. For example, Perego's buffer device can register the command and address signals similar to the conventional registered DIMM, which would have been within a Skilled Artisan's knowledge via the JEDEC standards. For example, a block diagram provided by JESD21-C (reproduced below in part) showed the Register on the module registering address signal (*e.g.*, BA0-BA1, A0-A13) and control signals (*e.g.*, S0-S1 chip select and RAS, CAS, and WE), and providing the registered address signals (*e.g.*, RBA0-

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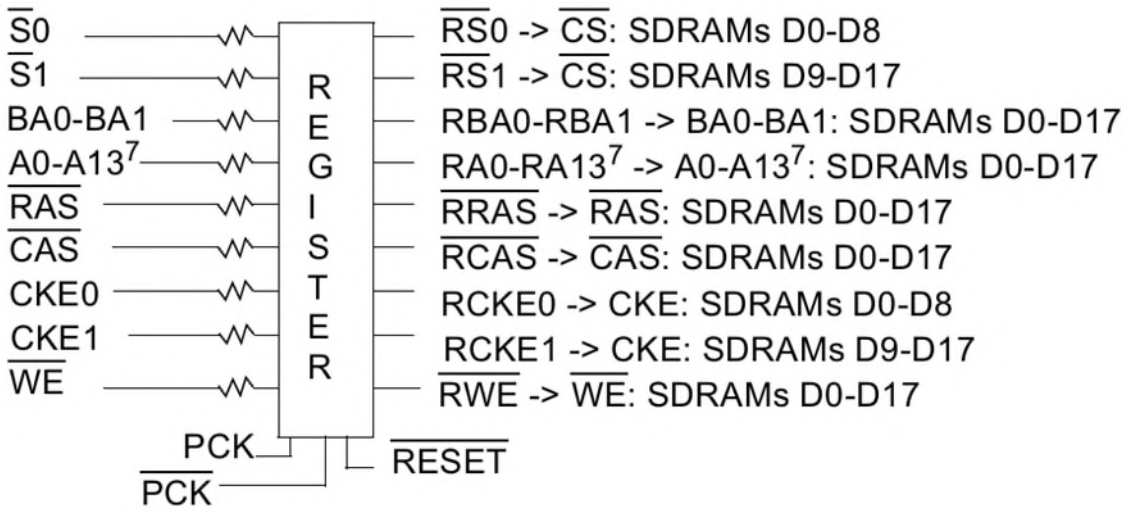
RBA1, RA0-RA13) and registered control signals (*e.g.*, RS0-RS1 registered chip select and RRAS, RRCAS, and RWE) to SDRAM memory devices.



EX1062 at p. 12.

256. Perego also discloses that the link between the system controller and the memory module includes control lines (RQ) to send read and write commands and corresponding address signals. *Id*. at 4A & 4B (reproduced with annotations below) & 9:50-60 ("In accordance with an embodiment of the present invention, control lines (RQ) transport control (e.g., read, write, precharge ...) information and address (e.g., row and column) information contained in packets. … In alternate embodiments, control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines.").

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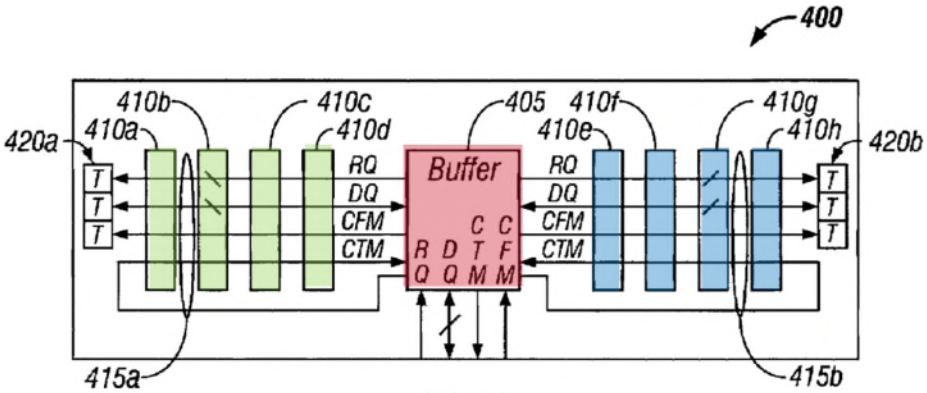

FIG. 4A

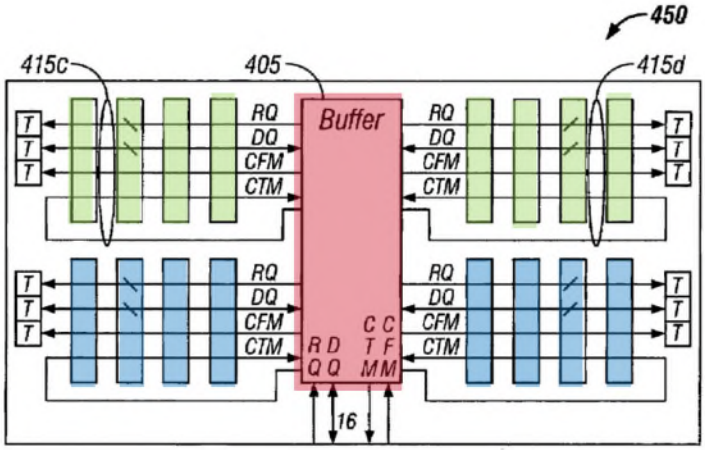

FIG. 4B

257. A Skilled Artisan would have understood from this disclosure that "*command and address signals*" would be received from the memory controller and would be representing a respective memory command because the receiving of command and address information is naturally associated with a memory command. For example, Perego discloses that its module can include DDR SDRAM devices. *Id.* at 8:1-4 & 10:56-59. A Skilled Artisan would have understood based on their knowledge of JEDEC standards (including JESD79-2)

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that DDR SDRAM devices respond to read and write commands and corresponding address information. EX1064 (JESD79-2) at pp. 26 ("The Burst Read command is initiated by having CS and CAS low while holding RAS and WE high at the rising edge of the clock. The address inputs determine the starting column address for the burst.") & 29 ("The Burst Write command is initiated by having CS, CAS and WE low while holding RAS high at the rising edge of the clock. The address inputs determine the starting column address.").

258. For the reasons discussed above with reference to claim element [1.a.3] (*see supra* ¶¶229-239), Perego discloses subsequent command and address signals representing subsequent read and/or write commands. A Skilled Artisan would have known and understood that multiple memory commands would follow each other in a memory system during normal operation. In fact, as discussed above, the JEDEC standards (including JESD79-2) expressly disclose subsequent bursts of data in response to memory commands following each other. *See, e.g.,* EX1064 (JESD79-2) at p. 28 (FIG. 26, reproduced below, showing a read command followed by a write command). As further discussed above, each of those commands is represented by respective command and address signals that would be received and buffered in a register of Perego's buffer.

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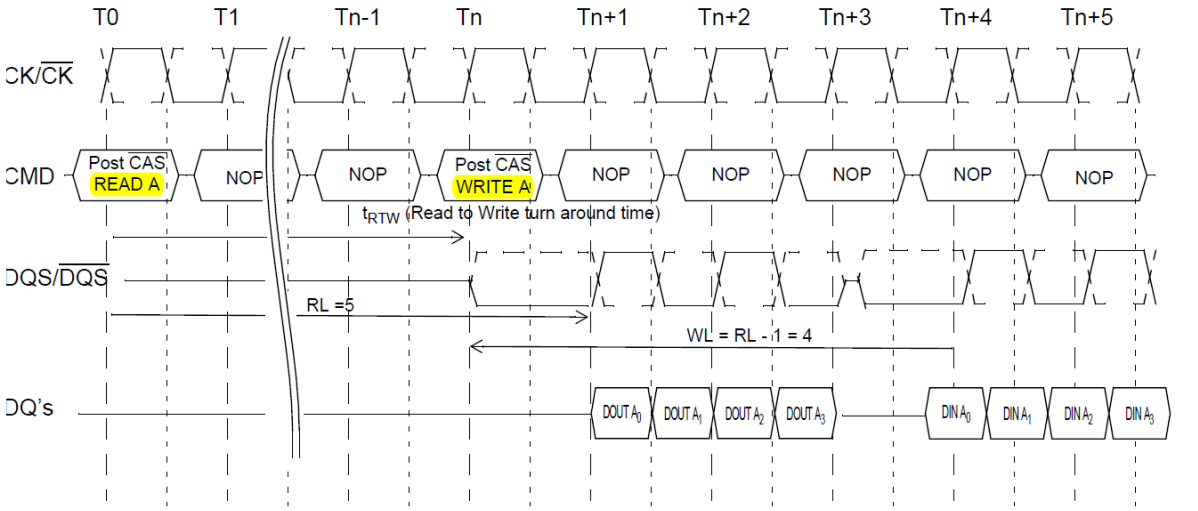

The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation.

Figure 26 — Burst Read Followed by Burst Write: RL = 5, WL = (RL-1) = 4, BL = 4

259. Although this understanding would have been within a Skilled Artisan's knowledge, a POSITA would have alternatively been motivated to combine these teachings from JESD79-2 with Perego, given that by doing so the Skilled Artisan would have implemented a predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results or challenges in implementation. *Supra* at ¶¶182-192. A Skilled Artisan would have been particularly motivated to make the combination in light of the importance of JEDEC compliance in the field of memory devices and memory modules. *Id.*

260. Accordingly, Perego, either by itself or in combination with JESD79-2, discloses "*a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first*

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memory command, and to receive and buffer second command and address signals representing the second memory command."

d) [1.d] Memory Integrated Circuits

(1) [1.d.1] Ranks

261. Claim 1 requires "*a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank.*"

262. The prior art references in Ground 1 (Perego by itself or in combination with JESD79-2) and/or Ground 3 (Ground 1 in combination with Halbert) teach this limitation to a Skilled Artisan. This limitation is also taught by Grounds 2 and 4 at least because they include Ground 1.

263. Perego discloses a plurality of memory integrated circuits (360, 410) mounted on the printed circuit board and arranged in a plurality of ranks including a first rank (green) and a second rank (blue), the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank. *E.g.*, EX1071 (Perego) at Figs. 3C, & 4A-4C (reproduced with annotations below) & 15:37-45

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(disclosing "grouping memory devices into multiple independent target subsets (i.e. more independent banks)").

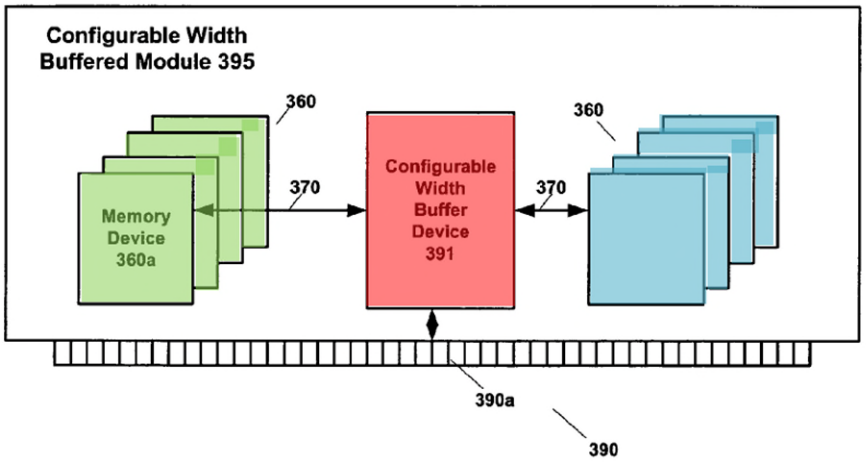

Fig. 3C

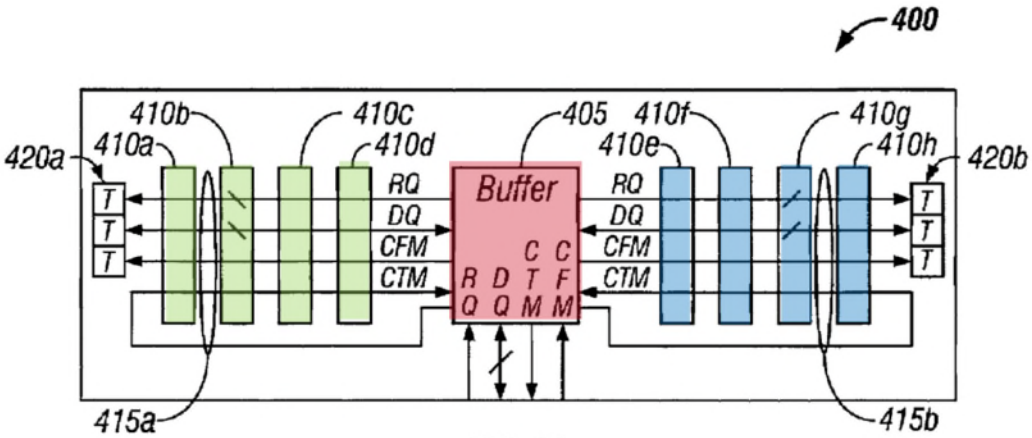

FIG. 4A

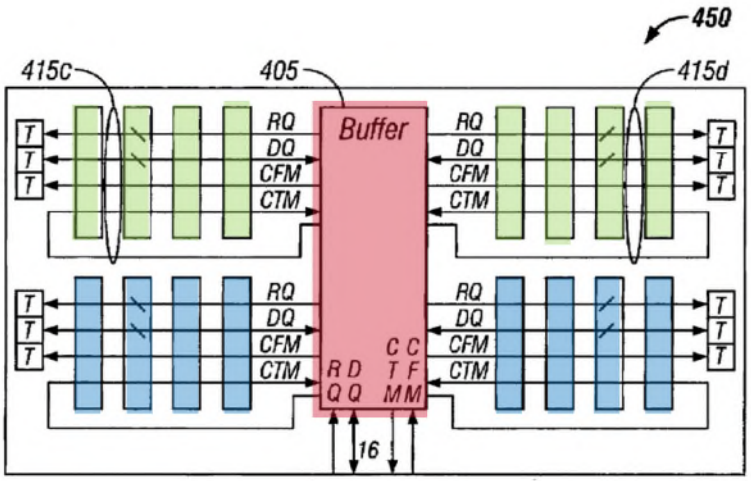

FIG. 4B

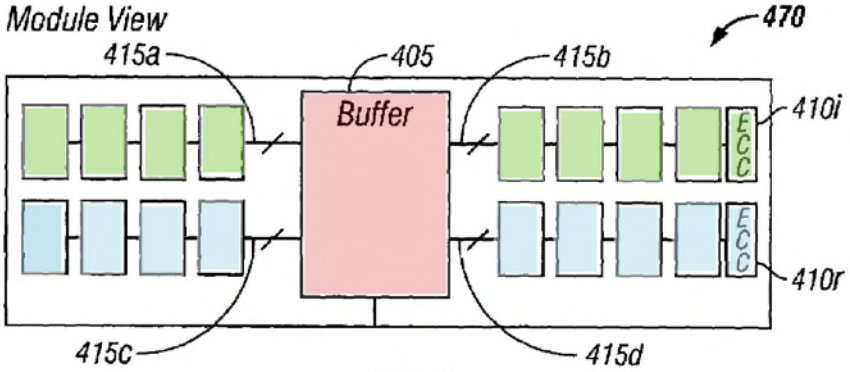

FIG. 4C

264. For example, Perego discloses the following:

"'Memory devices' are a common class of integrated circuit devices that have a plurality of storage cells, collectively referred to as a memory array. A memory device stores data (which may be retrieved) associated with a particular address provided, for example, as part of a write or read command. Examples of types of memory devices include dynamic random access memory (DRAM), static random access memory (SRAM), and double data rate SDRAM (DDR)."

Id. at 3:62-4:3. Perego also expressly discloses that its modules can include such DDR SDRAM devices. *Id.* at 8:1-4 & 10:56-58.

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265. Perego also explains that a "'memory module' or simply just 'module' denotes a substrate package housing or structure having a plurality of memory devices employed with a connector interface." *Id.* at 4:19-22. As discussed above with reference to claim element [1.b] (*see supra* ¶¶243-248), Perego discloses that the module's substrate on which the memory devices are mounted is a PCB. *See, e.g.*, EX1071 at 5:56-6:11. Perego further discloses modules in a DIMM format (*id*. at 2:4-6), and a Skilled Artisan would have understood that Perego's modules can also be implemented in such a DIMM format in order to "provide flexible and cost effective upgrade capabilities[.]" (*id*. at 2:26-30). A Skilled Artisan would have also understood, including from their knowledge of JEDEC standards, that DIMM modules include memory devices mounted on a PCB. *E.g.*, EX1062 at pp. 29 ("Components shall be surface mounted on both sides of the PCB and positioned on the PCB to meet the minimum and maximum trace lengths required for DDR SDRAM signals. Bypass capacitors for DDR SDRAM devices must be located near the device power pins. In two-bank, x4 based DDR SDRAM designs, the second DDR SDRAM bank devices will be stacked on the first DDR SDRAM bank devices.") & 35 (reproduced below, showing DDR SDRAM devices mounted on both sides on a PCB in a DIMM format).

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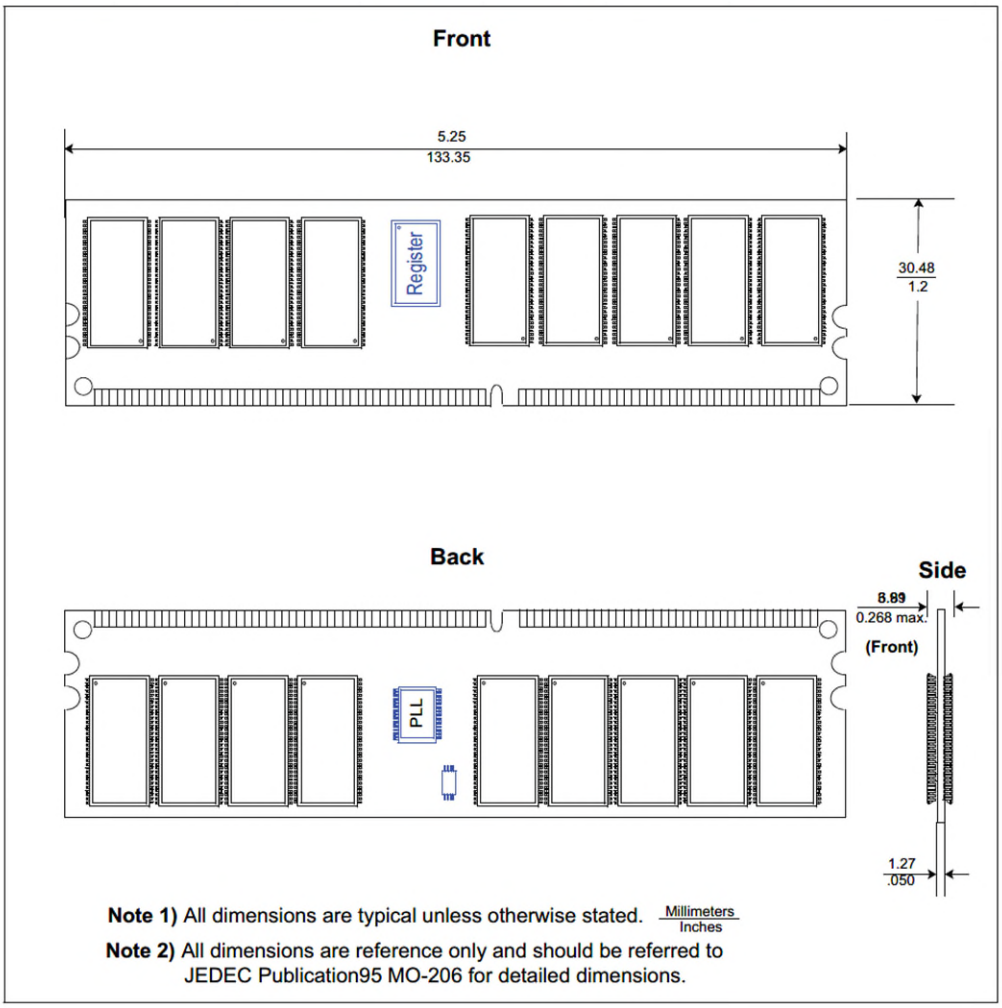
Example Raw Card Versions N (2 Physical Banks) Component Placement



266. Furthermore, Perego discloses that, in its buffer device, "interfaces 520a and 520b may be programmed to connect to 16'x4' width memory devices, 8'x8' width memory devices or 4'x16' width memory devices." EX1071 at 14:10-15, Figs. 5A & 5B (reproduced below with annotations).

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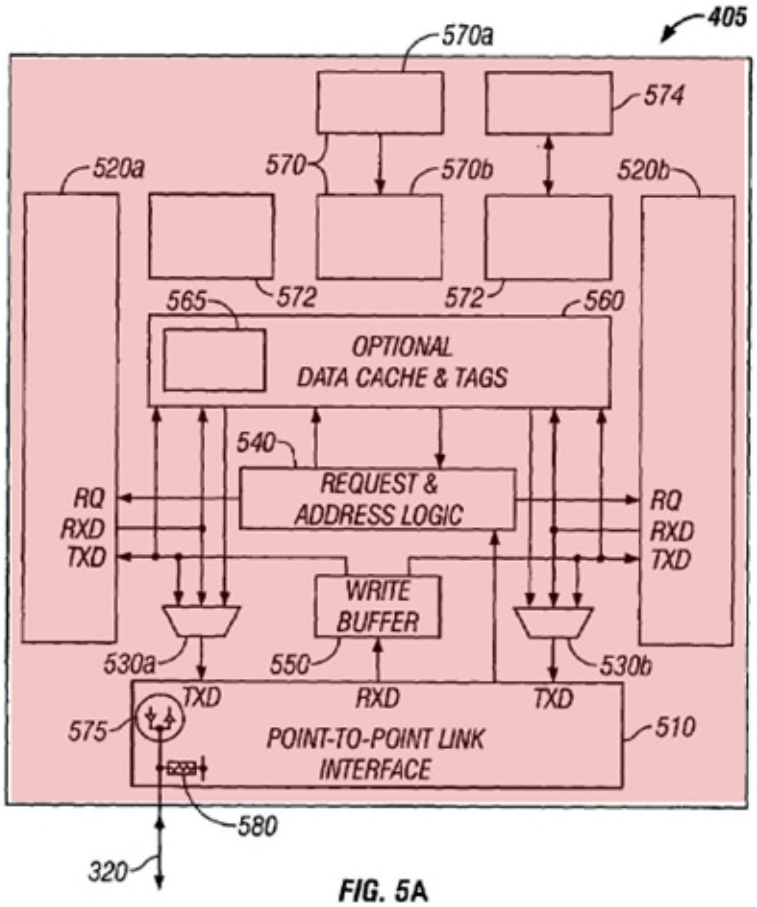
405
570a
574
520a
570
570b
520b
565
572
572
560
OPTIONAL
DATA CACHE & TAGS
540
REQUEST &
ADDRESS LOGIC
RQ
RXD
TXD
RQ
RXD
TXD
WRITE
BUFFER
530a
550
530b
TXD
RXD
TXD
575
POINT-TO-POINT LINK
INTERFACE
510
580
320

FIG. 5A

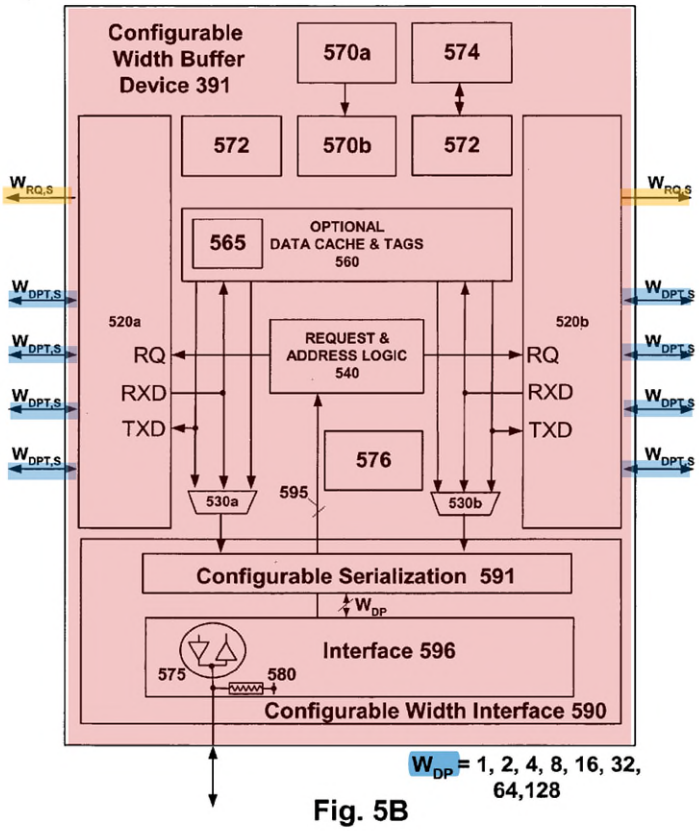

Fig. 5B

A Skilled Artisan would have understood from this disclosure that 'x4', 'x8' and 'x16' (pronounced "by four," "by eight," and "by sixteen") refer to the data width of a single memory device. *See, e.g.*, EX1069 (Synchronous DRAM Architectures paper) at 1 ("For example, … a x4 DRAM (pronounced 'by four') indicates that the DRAM has … a column width [which] is 4 bits (each column read or write transmits 4 bits of data). Likewise, a x8 DRAM indicates that the DRAM has … a column width [which] is 8 bits."). Accordingly, Perego's "16'x4' width memory devices" have a total data width of 64 bits, just like "8'x8' width memory devices or 4'x16' width memory devices." EX1071 at 14:10-15. A Skilled Artisan would

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have understood that such groups of memory devices correspond to 64-bit wide ranks on a standard DIMM module based on, for example, their knowledge of JEDEC standards. *See, e.g.*, EX1062 at p. 13 (describing a "x64 DIMM, populated as two physical banks [i.e., "*ranks*"] of [eight] x8 DDR SDRAMs [i.e., D0-D7, and D8-D15]").

267. Indeed, Perego discloses that the data width that is accessed in a memory transaction (W_A, Configured Buffer Device Interface Width) can be the same as the data width of the buffer interfacing with the memory controller (W_{DP}, Configured Buffer Device Interface Width), such that the ratio W_A/W_{DP} is 1:1:

> "Configurable width buffer device 391 has a maximum buffer device interface width equivalent to the number of data pins or contacts provided on the buffer device's package or interface 596. In an embodiment of the present invention, interface 596 includes 128 pins of which selectable subsets of 1, 2, 4, 8, 16, 32, 64 or all 128 pins (W_{DP}) may be used in order to configure the width of configurable width buffer device 391. Configurable width buffer device 391 also has a maximum memory device access width defined as the largest number of bits that can be accessed in a single memory device transfer operation to or from configurable width buffer device 391."

EX1071 at 14:16-40; *see also id.* at 17:22-28 & FIG. 5C (showing an implementation of an interface having a variable width of 4, 2, or 1, and a serialization ratio of 1:1).

268. Although Perego does not expressly use the word "rank," it clearly discloses the concept and structure to a Skilled Artisan. As I explained above, a Skilled Artisan would have understood that "rank" refers to an independent set of

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one or more memory devices on a memory module that act together in response to command signals, including chip select signals, to read or write the full bit-width of the memory module. *See supra* ¶¶124-133. As I also noted above, in a Final Written Decision issued for a patent to which the 215 Patent claims priority, the Board construed "rank" as "a block or area that is created using some or all of the memory chips on a memory module." *See supra* ¶132 (citing EX1048 at p. 8 (internal quotation marks and citations omitted)). For the reasons explained below, Perego clearly discloses the concept and structure of a "rank," both to a Skilled Artisan and also under the Board's previous finding of the broadest reasonable interpretation of the term.

269. A Skilled Artisan would have understood that Perego's disclosure of the memory device access width (W_A) as "the largest number of bits that can be accessed in a single memory device transfer operation" (EX1071 at 14:23-27) refers to the number of data bits a rank of memory can access at a time, in other words, the width of the memory rank. Thus, when the memory device access width (W_A) is the same as the data width (W_{DP}) of the buffer, the width of the rank (W_A) is the same as the data width (W_{DP}) of the data bus to the system controller. Furthermore, Perego discloses that, in case of a read operation, the buffer device can receive the corresponding read data "via one or more of channels 370":

> "In a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in

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> response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370. One or more of memory devices 360 may respond by transmitting data to Buffer device 350 which receives the data via one or more of channels 370 and in response, transmits corresponding signals to controller 310 via point-to-point link 320a."

Id. at 6:12-24; *see also id.* at FIG. 3C. A Skilled Artisan would have understood from this disclosure, that, when the read data is received "via *one* … of channels 370" in response to a read command, the memory device access width (W_A) is the same as the width of one channel (e.g., from interface 520a, Figs. 5A and 5B). Thus, in this implementation of Perego, each channel is connected to a rank of memory devices. Accordingly, when the buffer device has two channels, as shown in Figs. 3C and 4A, and each channel is connected to one rank of memory devices, Perego's module includes two ranks of memory devices (shown below as light green and light blue in annotated versions of Perego's Figures 3C and 4A).

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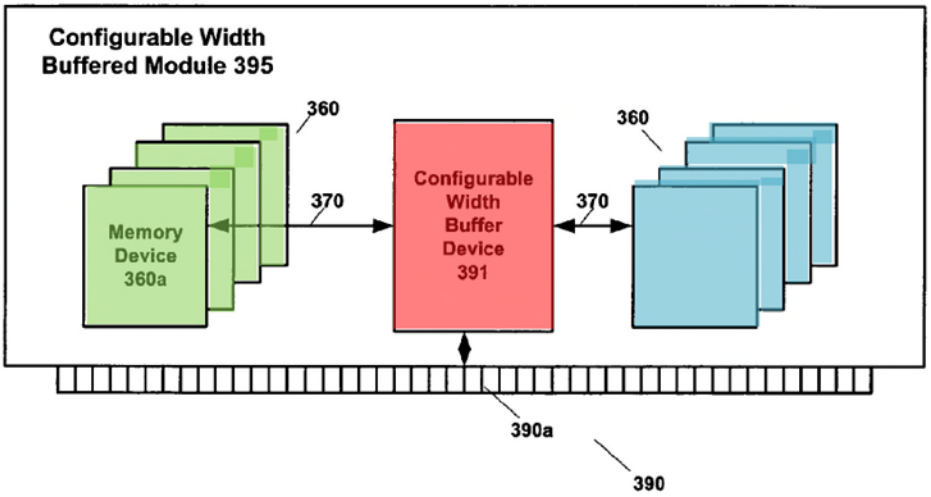

Fig. 3C

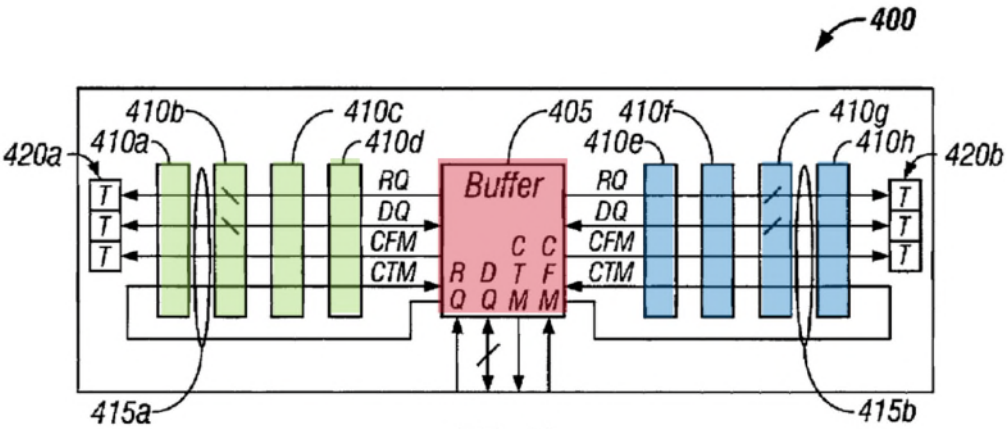

FIG. 4A

270. Furthermore, Perego discloses that "[a]ny number of channels 415a-415d, for example[] two channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations." *Id.* at 21:16-20. A Skilled Artisan would have understood that, in

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such an implementation, the memory devices coupled to channels 415c and 415d form one rank (green, "*first rank*"), and the memory devices coupled to channels 415a and 415b form another rank (blue, "*second rank*"). *Id*. at Fig. 4B (annotated version reproduced below); *see also* Fig. 4C (annotated version reproduced below) (using different channel numbering, with 415a/b referring to the top and 415c/d referring to the bottom channels).

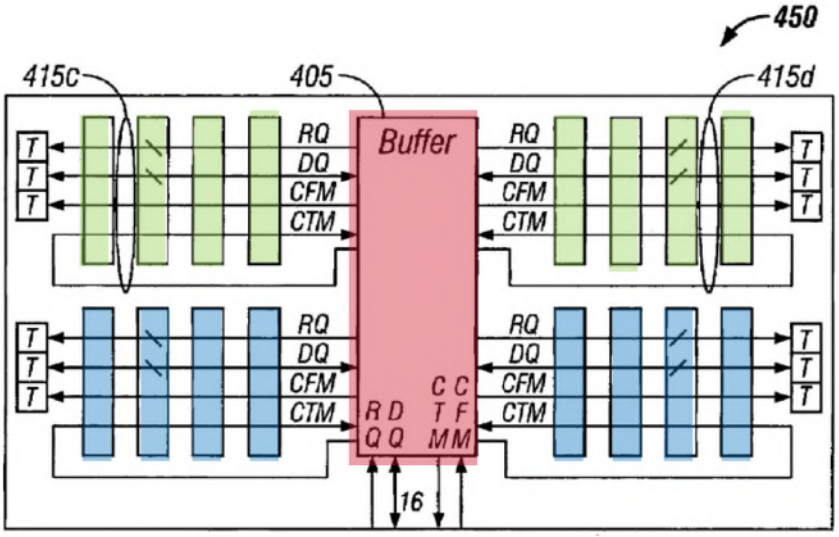

FIG. 4B

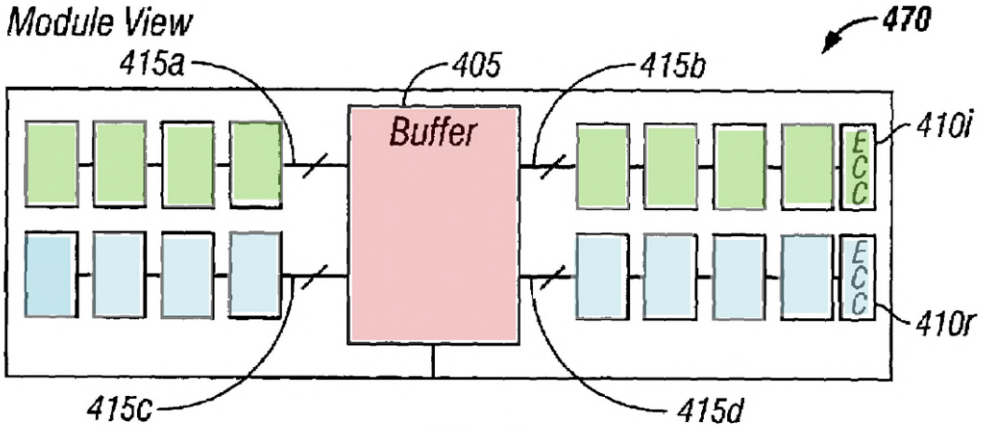

FIG. 4C

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271. I understand that Patent Owner and its expert have previously agreed that Perego discloses two such ranks, in *inter partes* review proceedings before the Board against a member of the 215 Patent's family:

> Petitioner provides no explanation why either arrangement describes single-device ranks, even under Petitioner's construction. Pet., 12, (contending "rank" means "an independent set of one or more memory devices on a memory module that act together in response to command signals"). To the contrary, **a POSITA would understand that in the paired arrangement, the devices connected to channels 415c/d correspond to one "rank" because they are "routed in parallel," i.e., "act together in response to command signals."** Brogioli, ¶¶93-94. Likewise, the devices connected to 415a/b correspond to another "rank." *Id.*

EX1019 (912 POPR) at p.43 (emphasis removed from and added the original); *see also* EX1020 (912 Petitioner Expert Declaration) at ¶¶93-94 (similar).

272. Furthermore, as illustrated in the above figures, each of Perego's ranks includes at least one "*memory integrated circuit*." EX1071 at Figs. 3B (showing memory devices 360 in each rank) & 4A-4C (showing memory devices 410 in each rank), 15:37-45 (disclosing "grouping memory devices into multiple independent target subsets (i.e. more independent banks)").

273. To the extent one might argue that Perego does not sufficiently disclose multiple ranks, this would have been within the knowledge of a Skilled Artisan at the time or otherwise obvious. As discussed above, Perego discloses using DDR SDRAM devices and systems that use memory modules in DIMM format. EX1071 at 6:25-33, 8:1-4, 10:56-58. Perego also discloses an inventive

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"configurable width buffer device to provide upgrade flexibility and/or provide high bandwidth among a variety of possible module configurations in the system." *Id.* at 3:23-28. A Skilled Artisan would have understood from this disclosure that Perego's modules can be used to upgrade memory systems using memory modules in a DIMM format in accordance with the corresponding JEDEC standard describing DDR SDRAM memory systems, including JESD79-2. *See, e.g.,* EX1064 (JESD79-2) and EX1062 (JESD21-C). According to these JEDEC standards, the memory devices are organized into ranks (also called "physical banks" in JESD21-C). *E.g.*, EX1062 at p. 13; *see also supra* ¶129 (discussing the relationship between "rank" and "physical bank"). To upgrade the memory modules in such a JEDEC-style system as taught by Perego, a Skilled Artisan would have known or otherwise been motivated to follow the rank-based organization of the memory devices in the JEDEC standards because the memory controllers in those systems are configured to communicate with such ranks, e.g., through the use of chip select signals. *See, e.g.*, EX1064 at p. 6 ("Chip Select: All commands are masked when CS is registered HIGH. CS provides for external Rank selection on systems with multiple Ranks. CS is considered part of the command code.").

274. Implementing such ranks in Perego's module would have been well within the level of ordinary skill, since both the JEDEC standards and Perego teach

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how to select and communicate with groups of memory devices. For example, Perego teaches that a single channel 370 or a pair of channels 415a/b or 415c/d can provide read data in response to a read command, and a Skilled Artisan would have understood that, in a JEDEC module, a single rank provides read data in response to a read command. *See, e.g.*, EX1071 at 6:15-25; EX1062 at p.3 (showing a two rank ("two physical bank[]") module, each rank receiving a separate chip select signal); *see also* EX1072 (Matsui1, US7,155,627) at FIG. 1 (reproduced below, showing details of wiring DDR SDRAMs to a central buffer in a DIMM format).

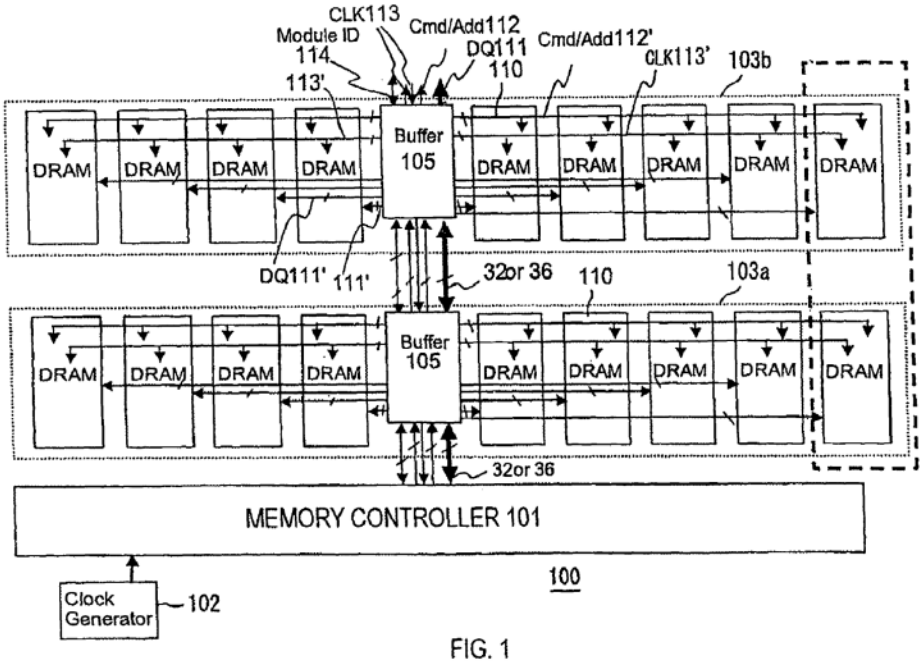

FIG. 1

275. Accordingly, a Skilled Artisan would have known and it would have been at least obvious to a Skilled Artisan to connect a rank of DDR SDRAMs to each channel 370 or to a pair of channels 415a/b or 415c/d in order to provide an upgrade module for a JEDEC style memory system. A Skilled Artisan would have

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been further motivated to do so because it would have produced a predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results or challenges in implementation.

276. Accordingly, the prior art references in Ground 1 (Perego, either by itself or in combination with JESD79-2) satisfy "*a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank*."

277. To the extent one might argue that Perego or the Perego-JESD79-2 combination does not sufficiently disclose the claimed ranks, it would have been obvious in further view of Halbert or Ellsberry. EX1078 (Halbert), EX1073 (Ellsberry). As discussed above, Halbert and Ellsberry are analogous art to the 215 Patent and Perego, as each is directed to improved memory modules that buffer the data signals and isolate the memories from the system bus. *Supra* at ¶¶193-205. For example, the 215 Patent is titled "Memory module with data buffering" and discloses the following:

> "In certain embodiments, the memory module 10 operates as having a data path rank buffer which advantageously isolates the ranks of memory devices 30 of the memory module 10 from one another, from the ranks on other memory modules, and from the computer system."

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EX1001 at 9:26-42. Similarly, Perego is titled "Configurable width buffered module" and discloses the following:

> "It follows from these definitions that a memory module having a buffer device (e.g., having a configurable width) isolating data, control, and address signals of the memory devices from the connector interface may be a memory subsystem."

EX1071 (Perego) 4:38-42.

> "With further reference to FIGS. 3A and 3B, buffer device 350 transceives and provides isolation between signals interfacing to controller 310 and signals interfacing to the plurality of memory devices 360. In a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370. One or more of memory devices 360 may respond by transmitting data to Buffer device 350 which receives the data via one or more of channels 370 and in response, transmits corresponding signals to controller 310 via point-to-point link 320a."

Id. at 6:12-24. Ellsberry is also directed to a memory module which buffers data signals to reduce loading on the data lines and to perform rank multiplication. EX1073 at [0031] ("Additionally, each memory bank switch 206 and 208 includes signal drivers to drive data signals to and from the memory banks and to and from the DIMM interface 202. This reduces resistive and/or capacitive loading of the data bus coupled to the DIMM interface and the bus 110 while emulating a standard memory device interface."), *supra* at ¶¶193-200. And Halbert is similarly titled "Dual -port buffer-to-memory interface" and discloses the following:

> "The exemplary embodiments also allow the memory devices to be isolated from the full capacitive loading effects of the system memory data bus.

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> Further, the memory devices of the embodiments avoid arrangements of competing memory banks that load each other, as is the case with a dual-bank DIMM."

EX1078 (Halbert) 3:67-4:5.

278. In particular, Halbert discloses a memory module that includes two memory ranks 140 (green) and 142 (blue), and buffering circuitry (red) that interfaces with the two ranks 140 and 142 on one side and with the system memory bus on the other side (to the left of Fig. 4). EX1078 (Halbert) at 4:36-39, 4:49-59, FIG. 4 (reproduced below with annotations). Halbert's buffering circuitry includes a module controller 110 and a data interface circuit 120 (*id*. at 4:36-39 & FIG. 4):

> "Data interface circuit 120 provides for m-bit-wide data transfers between the module and the system memory data bus, and for R×m-bit-wide data transfers between the interface circuit and the memory device array. In FIG. 4, R=2, i.e., the memory device array comprises two memory device ranks 140 [(green)] and 142 [(blue)], each capable of performing m-bit-wide data transfers. As used herein, a rank of memory comprises enough memory devices to form a data path that is m bits wide."

Id. at 4:49-57. In particular, "bi-directional data registers 126 and 128 connect, respectively, to memory device array ranks 140 and 142. Each data register can receive an m-bit-wide word from its corresponding memory device rank, or drive an m-bit-wide word to that rank, over a dedicated point-to-point module data bus." *Id*. at 5:6-11.

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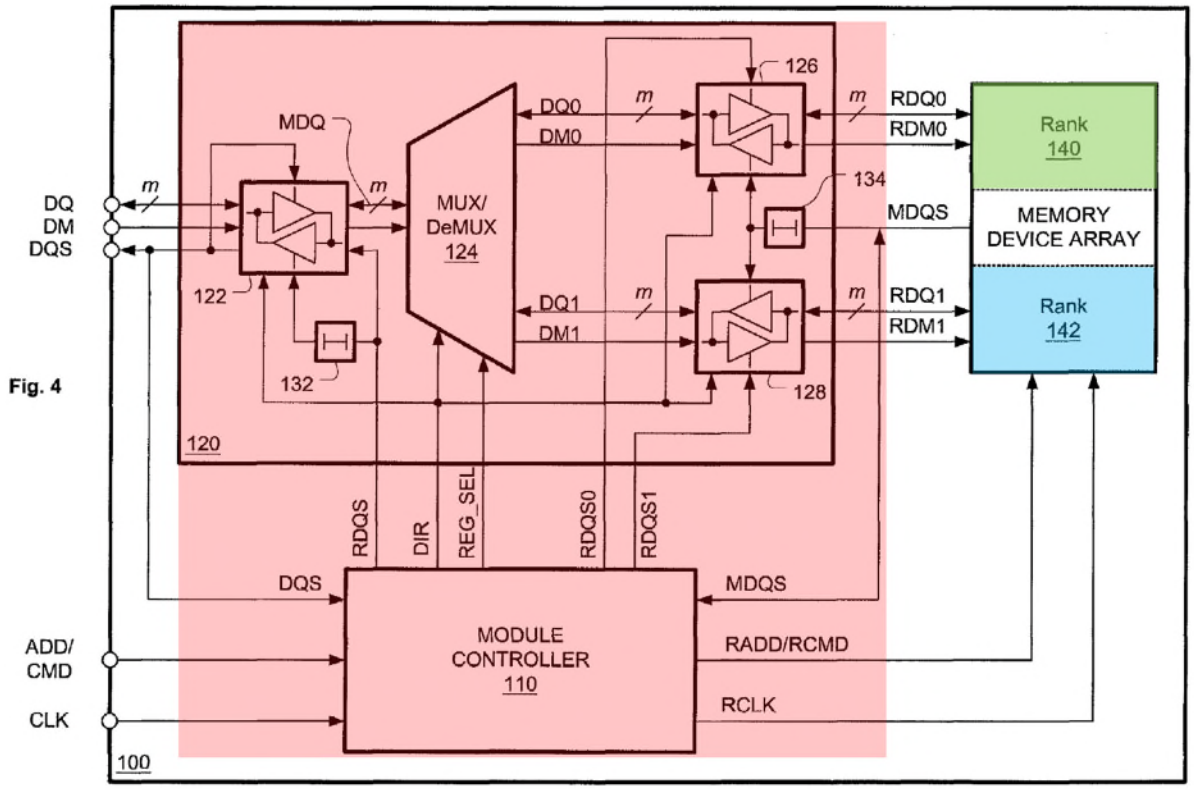

279. Therefore, Halbert discloses "a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank" as required by the claim.

280. Ellsberry also discloses the claimed ranks of memory devices. EX1073 (Ellsberry), e.g., at Abstract ("the invention expands the addressable memory banks on a module") and Fig. 5 (reproduced below, annotated to indicate two ranks, green and blue).

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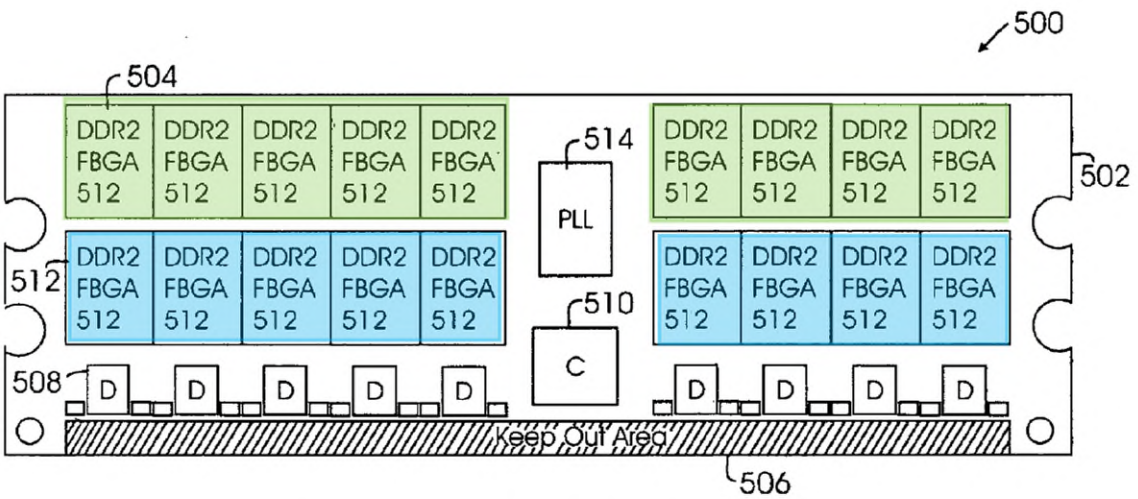

Fig. 5

Although Ellsberry uses the terms "memory bank" and "physical memory bank," a Skilled Artisan would have understood at the time that these "memory banks" and "physical memory banks" refer to ranks of memory devices (under the proper construction of "rank"), such as ranks of DDR2 memory devices shown in Fig. 5 of Ellsberry. *Supra* at ¶¶124-133 (discussing claim construction for "rank"); *see also* EX1073 (Ellsberry) at Fig. 2 (showing memory devices organized in four "Banks", each "Bank" corresponding to one rank), Fig. 8B (Note 3 explaining that chip select is part of commands), and Figs. 10-13 (showing that each "rank" of memory devices receives a separate chip select signal). Ellsberry's terminology is consistent with how the JEDEC standards, incorporated by reference in Ellsberry, also referred to "ranks" at the time. EX1073 at [0046] and [0050], EX1060 (JESD79) at p. 7 ("Chip Select: … for external bank selection on systems with multiple banks. $\overline{S}$ is considered part of the command code."), EX1062 (JESD21-

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C) at pp. 6 (describing "$\overline{S}$0-$\overline{S}$3 SDRAM chip select lines" to select "Physical. [sic] banks 0, 1, 2, and 3"), 10-16 (describing modules with one or two "physical banks" with a bit-width of 64 or 72 bits, each "physical bank" having a respective set of memory devices activated by a corresponding (registered) chip select signal $\overline{RS}$0 or $\overline{RS}$1). Furthermore, Ellsberry discloses the same "rank multiplication" as the 215 Patent. EX1073 at [0011] ("The memory bank switch is designed to receive data information from the bus and direct the data information to a plurality of physical memory banks according to control signals from the control unit that maps one logical memory bank to a plurality of physical memory banks."), and Figs. 10-13 (each showing a control unit ASIC producing more chip select signals than received, each produced chip select controlling a respective rank of one or more memory devices). I understand that the Board has also found that Ellsberry discloses "ranks" of memory devices. *See, e.g.,* EX1023 at 51-52 (Board agreeing that Ellsberry discloses "memory devices arranged in a first number of ranks"); EX1074 at 20-21 (Board finding that Ellsberry discloses groups of memory devices simultaneously providing the full bit width of the memory module); EX1076 at 21-22 (Board finding that Ellsberry discloses "double data rate dynamic random access memory (DDR DRAM) devices … arranged in multiple N-bit-wide ranks").

281. Because Perego discloses embodiments which a Skilled Artisan would have understood correspond to rank-based organization of memory devices in Halbert and Ellsberry, a Skilled Artisan would have been motivated to organize the memory devices of Perego (as taught by Perego or the Perego-JESD79-2 combination) into ranks, where each rank is coupled to the data buffer by a corresponding data bus, as taught by Halbert and Ellsberry. For example, as discussed above, Perego discloses that data is communicated "via *one* … of channels 370" in response to a memory command, and the memory device access width (W_A) is the same as the width of the memory module (W_{DP}). *Supra* ¶269. A Skilled Artisan would have understood from this disclosure that, in such an arrangement, each of Perego's channel interfaces with a respective rank, as taught by Halbert (and in 2-rank implementations of Ellsberry, like in Figs. 10 and 12) because the full bit width of the module is transmitted in one channel, as required for a rank. A Skilled Artisan would have been motivated to use such a rank-based arrangements of Halbert and Ellsberry in Perego's module (by itself or as modified in view of JESD79-2's teachings) because they "allow the memory devices to be isolated from the full capacitive loading effects of the system memory data bus … [and] avoid arrangements of competing memory banks that load each other, as is the case with a dual-bank DIMM." EX1078 (Halbert) at 3:67-4:5. A Skilled Artisan would have also understood that a rank responds to a memory command by

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transferring the full bit width of the memory module and is connected to the data buffer by a corresponding data bus that is not connected to other rank(s) on the module, meaning that this arrangement beneficially provides "reduced power consumption" by accessing only a subset of the data lines and allows "higher performance by grouping memory devices into multiple independent target subsets (i.e. more independent banks)." EX1071 (Perego) at 15:40-45. As discussed above, this rank based organization was well known, widely used, and standardized by JEDEC, thus providing predictable results of timely and efficient data transfers between the data buffer and the memory devices. Additionally, a POSITA would have alternatively been motivated to combine these teachings from Halbert or Ellsberry with Perego or the Perego- JESD79-2 combination, given that by doing so the Skilled Artisan would have implemented a predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results or challenges in implementation.

282. Therefore, Perego or the Perego-JESD79-2 combination in view of Halbert or Ellsberry renders obvious to a Skilled Artisan "*a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank*."

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(2) [1.d.2]-[1.d.3] First and Second Ranks

283. Claim 1 requires (1) "*wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and*" (2) "*wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command*."

284. The prior art references in Ground 1 (specifically, Perego) teach these limitations to a Skilled Artisan. This limitation is also taught by Grounds 2-4 at least because they include Ground 1. Furthermore, Ellsberry also discloses this limitation and a Skilled Artisan would have been motivated to include it in Perego's module for the reasons discussed below.

285. Perego discloses to a Skilled Artisan that the first rank (green) is selected to receive (in response to a write command) or output (in response to read command) the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and the second rank (blue) is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory

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command. *E.g.*, EX1071 (Perego) at Figs. 3C, 4A-4B (annotated versions reproduced below), 6:21-22 ("Buffer device 350 … receives the data via **one** … of channels 370."), & 21:16-20 ("Any number of channels … may transfer information simultaneously and the memory devices on the other … channels … remain in a ready or standby state until called upon to perform memory access operations.").

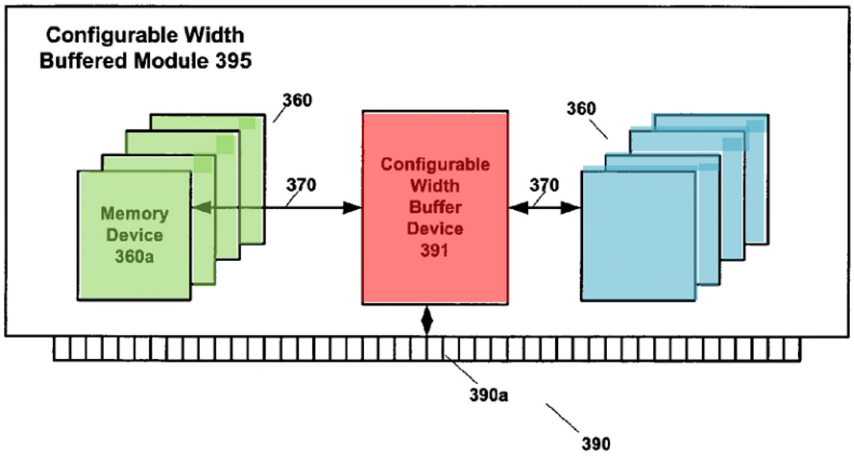

Fig. 3C

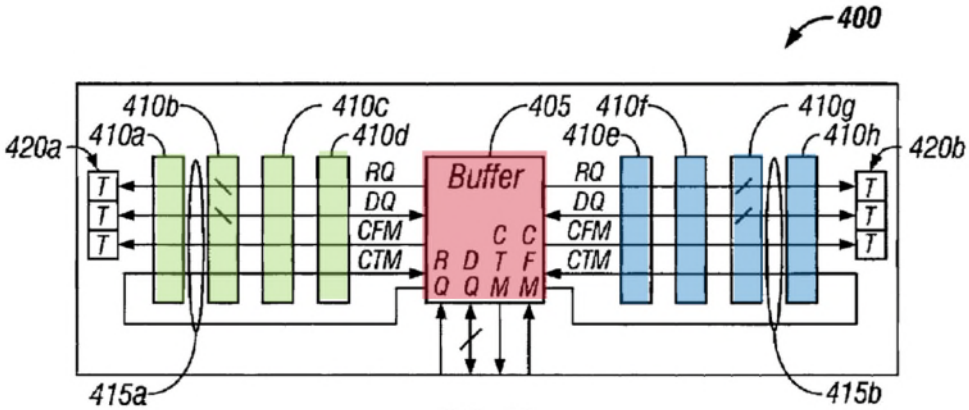

FIG. 4A

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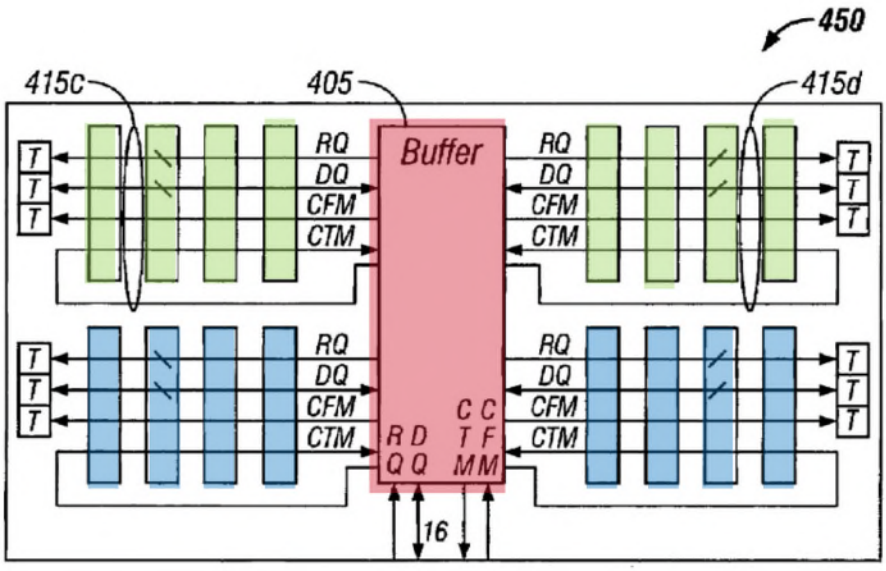

FIG. 4B

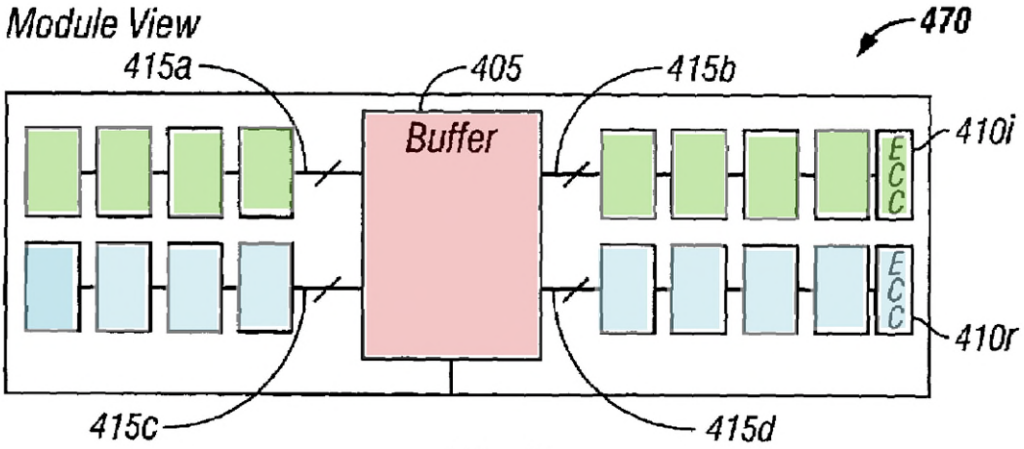

FIG. 4C

286. For example, Perego discloses that its buffer device selects a target subset of memory devices, such as a rank, and routes data through a corresponding "datapath" in response to a read or write requests:

> "… [C]onfigurable width buffer device 391 may employ a configurable datapath router within interface 591 to route requests between the primary channel and the target subset of secondary channel signal lines for each transaction. … By accessing a subset of secondary channel signal lines per

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> transaction, a number of benefits may be derived. One of these benefits is reduced power consumption. Another benefit is higher performance by grouping memory devices into multiple independent target subsets (i.e. more independent banks)."

Id. at 15:31-45.

> "According to an embodiment of the present invention, multiplexers 530a and 530b perform bandwidth-concentrating operations, between interface 510 and interfaces 520a and 520b, as well as route data from an appropriate source (i.e. target a subset of channels, internal data, cache or write buffer)."

Id. at 11:56-61; *see also id*. at FIGS. 5A & 5B (annotated versions reproduced below).

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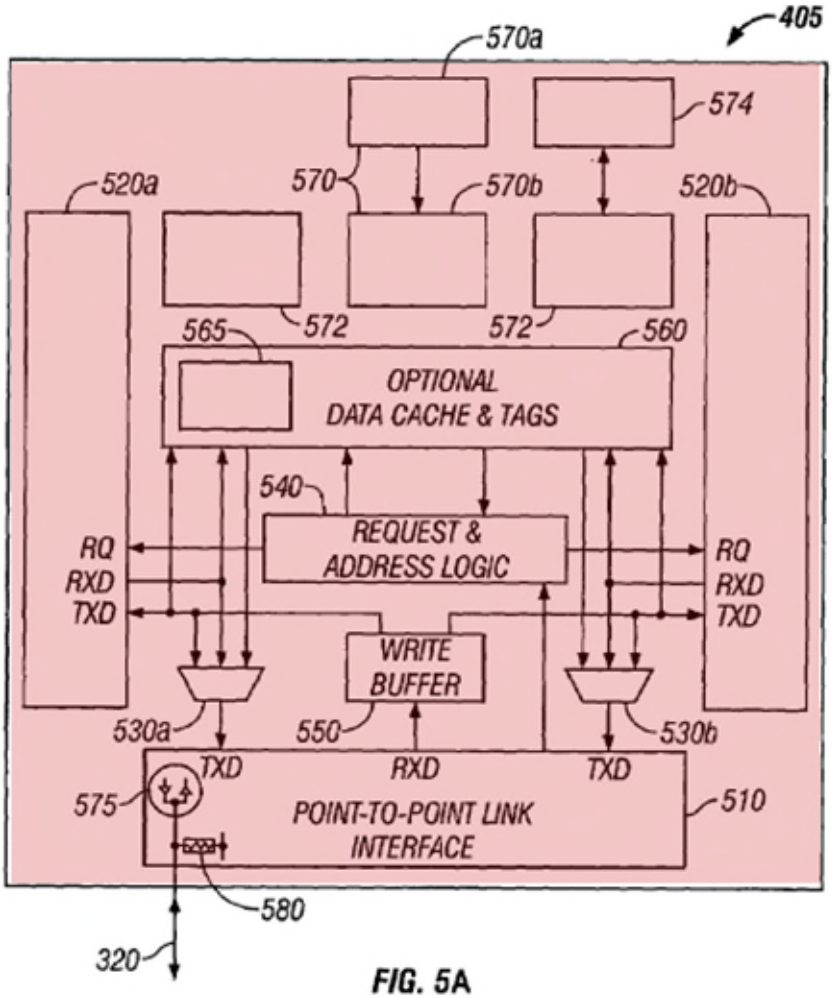
405
570a
574
520a
570
570b
520b
565
572
572
560
OPTIONAL
DATA CACHE & TAGS
540
REQUEST &
ADDRESS LOGIC
RQ
RXD
TXD
RQ
RXD
TXD
WRITE
BUFFER
530a
550
530b
TXD
RXD
TXD
575
POINT-TO-POINT LINK
INTERFACE
510
580
320

FIG. 5A

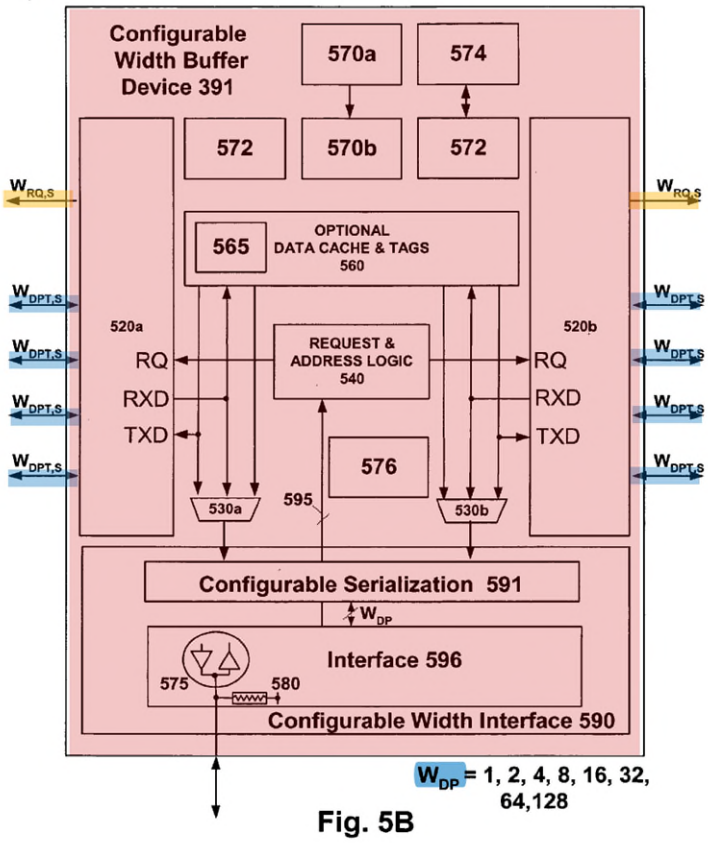

Fig. 5B

287. As discussed above with reference to claim elements [1.a.1], [1.a.2], and [1.a.3], Perego discloses to a Skilled Artisan the claimed first and second ranks and first and second commands and corresponding first and second data bursts. *See supra* ¶¶212-239. A Skilled Artisan would have understood these disclosures in view of, for example, their knowledge of JEDEC standards, including JESD79-2. EX1064 at pp. 24-33 (describing in Section 2.2.4 the standard memory access operations, including read and write operations of DDR SDRAM devices which were well known at the time). Although this understanding would have been within a Skilled Artisan's knowledge, a POSITA would have alternatively been

motivated to combine these teachings from JESD79-2 to Perego, given that by doing so the Skilled Artisan would have implemented a predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results or challenges in implementation. *Supra* at ¶¶182-192.

288. Furthermore, the claim language expressly requires that the second rank is not selected to communicate data with the memory controller in response to the first memory command while the first rank is receiving or outputting the data signals (and vice versa). Based on its First Amended Complaint filed against Samsung in district court, Netlist appears to be advancing an interpretation of the claim that is broader than the claim's plain meaning. My analysis below addresses Netlist's broader interpretation and the narrower interpretation that is consistent with the claim's plain meaning. Under either interpretation, I conclude that Perego discloses or renders obvious this claim language alone or in combination with Ellsberry.

(1) Netlist's Broader Interpretation

289. I understand that Netlist has asserted that this claim limitation is satisfied when two ranks share the same data lines on the module, as shown in the following figure reproduced from Netlist's First Amended Complaint against Petitioner:

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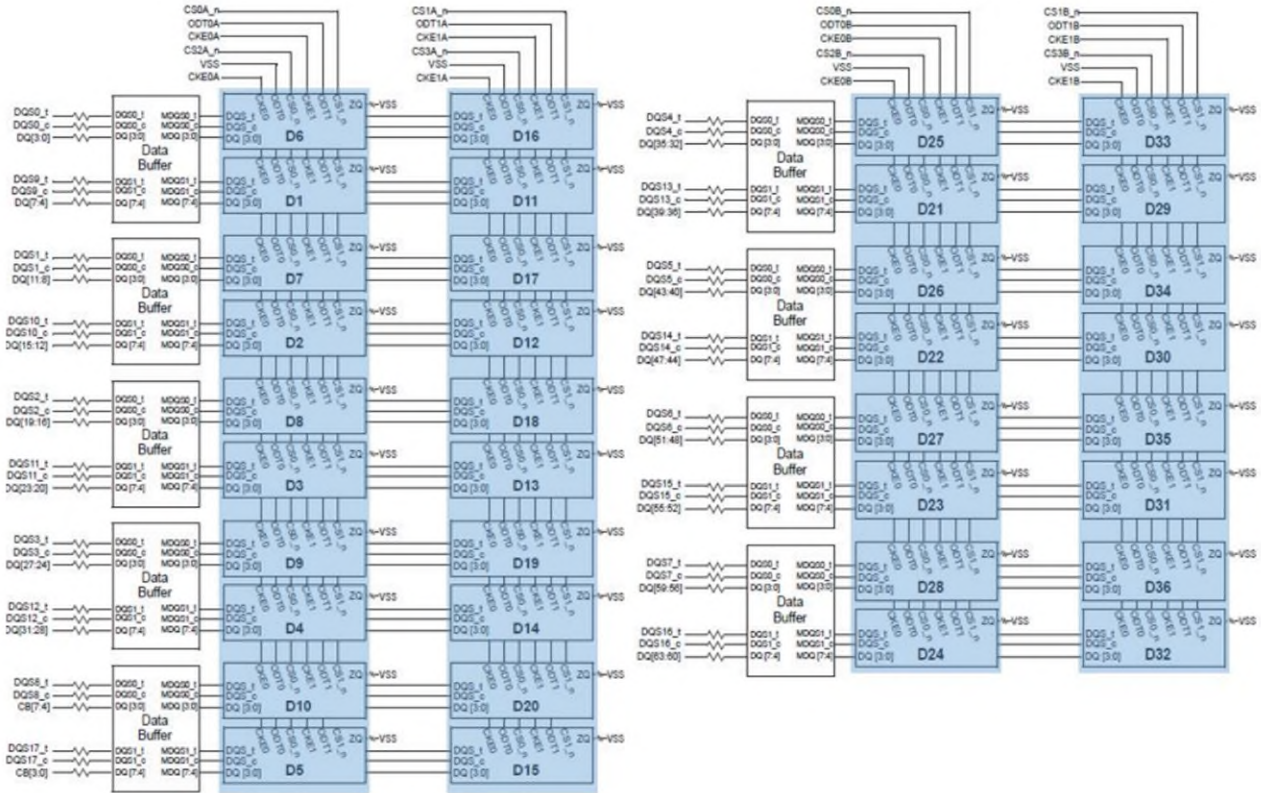

EX1085 (Samsung Complaint) at pp.39-41 (blue annotation by Netlist). Here, the memory devices are stacked (so each of D1-D32 has two memory devices) and there are four ranks that can be distinguished because each rank receives a respective one of chip select signals CS0, CS1, CS2, and CS3.

290. This arrangement of multiple ranks using shared data lines was well known at the time. For example, this arrangement is similar to arrangements disclosed in the JEDEC standards, including the following block diagram from the JESD21-C specification for memory modules:

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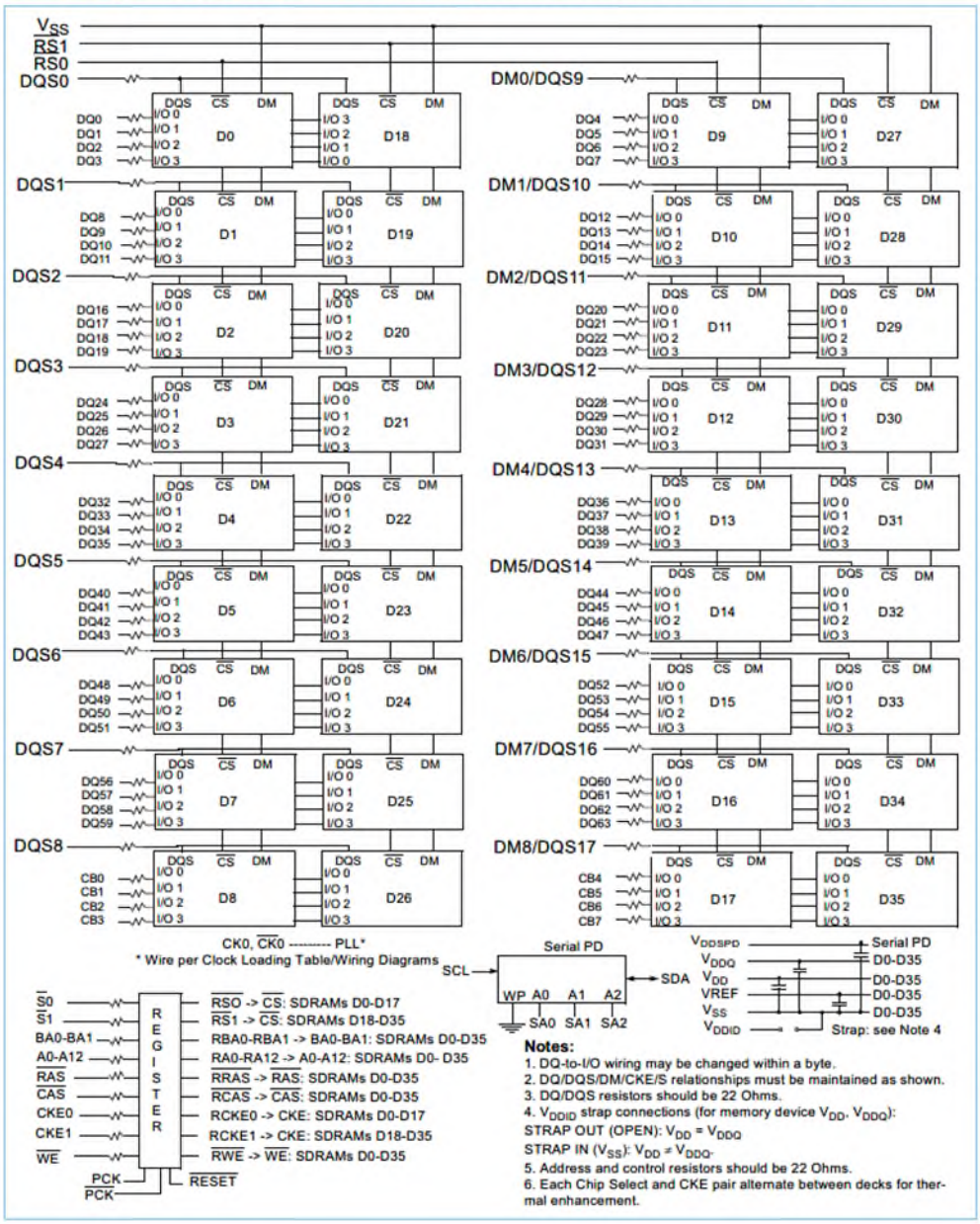
Block Diagram: Raw Card Version C/E (Populated as two physical banks of x4 DDR SDRAMs)



EX1062 at p. 16 (showing two ranks connected to registered chip select signals RS0 and RS1, respectively, where the memory devices in the two ranks, e.g., D0 and D18, are connected to the same DQS data strobes and the same DQ data signals); *see also* EX1064 at 4-5 (showing pin-out of stacked memory device packages, each having two chip-select inputs).

291. Regardless of how this part of the claim is construed, however, a Skilled Artisan would have understood that Perego discloses or renders it obvious alone or in combination with Ellsberry. For example, Perego discloses the same structure for the memory module as the 215 Patent: a buffer circuit interfaces with the memory controller on the system side and uses a respective separate bus to interface with each rank on the module. *Compare* EX1001 (215 Patent) at FIG. 1 (reproduced below with annotations showing the buffer circuit (red) having a separate bus to each rank (light green or light blue) on the module and a common interface to the system memory bus to the memory controller, *with, e.g.*, EX1071 (Perego) at FIG. 3B (same). Accordingly, Perego discloses what is described and claimed in the 215 Patent under any reasonable claim interpretation that does not exclude the 215 Patent's primary embodiment (shown in FIG. 1).

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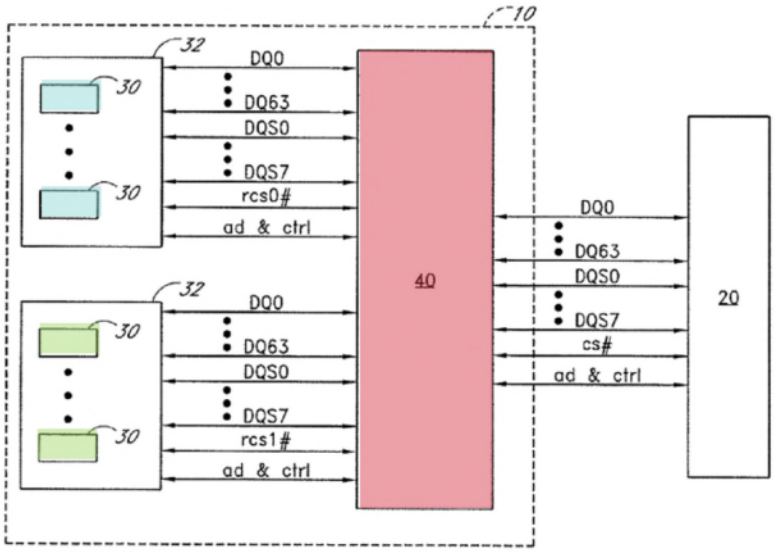
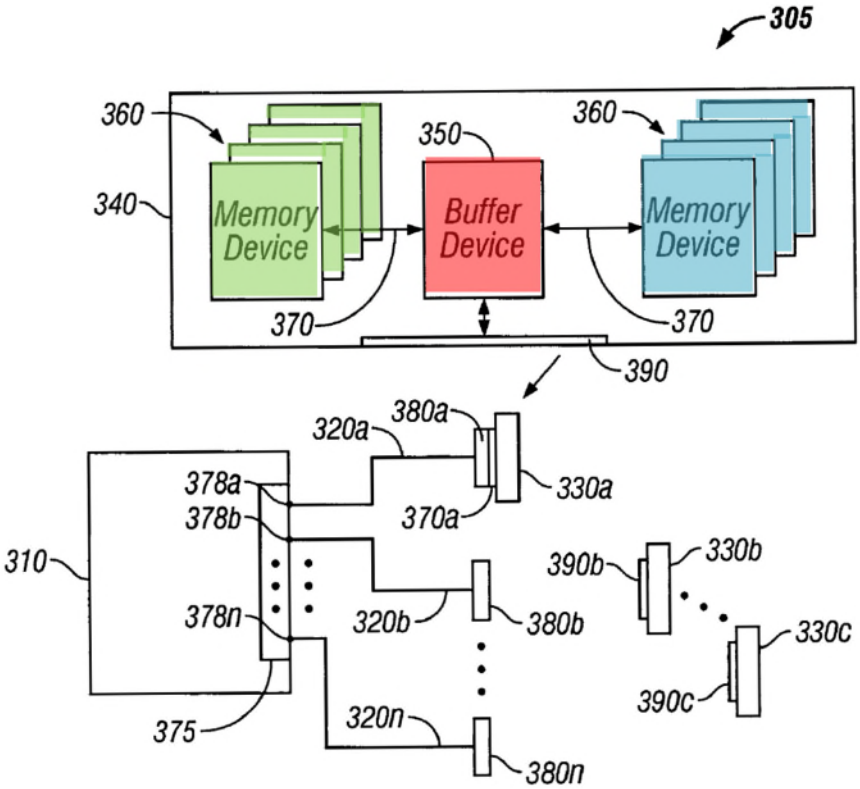
215 Patent	 FIG. 1
Perego	 FIG. 3B

Ellsberry also discloses a similar structure with a buffer device (red) including data buffering functionality (in Switch ASIC) and a separate data bus to each rank of memory devices (green and blue). *See*, *e.g.*, EX1073 at Fig. 10 (reproduced below, annotated).

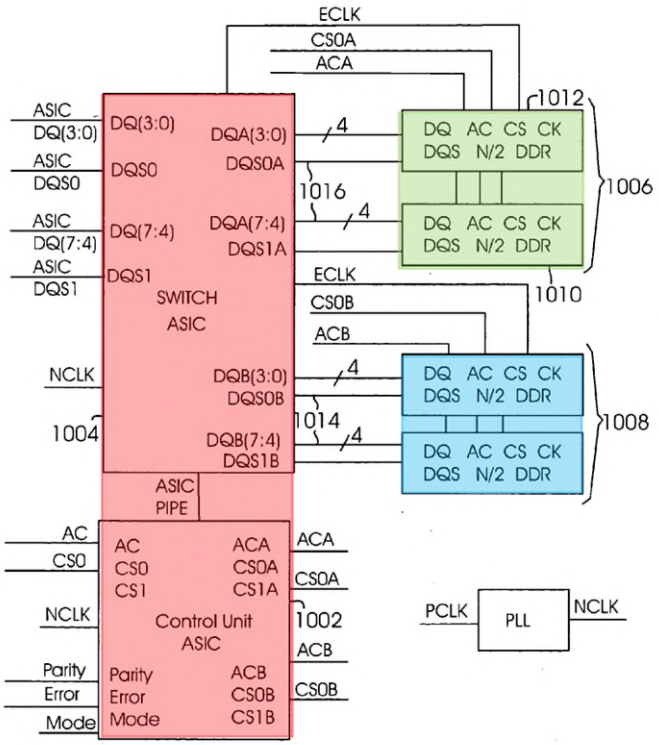


Fig. 10

292. If the primary embodiment shown in FIG. 1 of the 215 Patent is not excluded from the scope of the claim, Perego discloses, just like the 215 Patent, a separate data channel to each rank (e.g., in separate channels 370 in FIGS. 3B-3C; separate channels 415a and 415b in Fig. 4A; and separate pairs of channels 415a/b and 415c/d in Figs. 4B and 4C). For example, Perego discloses that, in response to a read or write command, the data is transmitted in only one channel coupled to

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only one rank of memory devices, while the other channel(s) coupled to other rank(s) of memory devices are not used. *See, e.g.*, EX.1071 at Figs. 3C & 4A-4B (annotated versions reproduced above), 9:26-33 ("Buffer device 350 … receives the data via **one** … of channels 370."), & 21:16-20 ("Any number of channels … may transfer information simultaneously and the memory devices on the other … channels … remain in a ready or standby state until called upon to perform memory access operations."). Thus, the other rank(s) are not selected to communicate data with the memory. To the extent one might argue that Perego alone does not disclose or render obvious this limitation, it would have been obvious in light of Ellsberry's disclosure that only memory devices in the selected rank participate in the data transaction in response to a memory command. EX1073, e.g., at [0036] ("The state machine implemented by the control unit 204 directs data to a particular memory bank based on the memory configuration of memory banks and the address received.") and Claim 1 ("a control unit to receive memory address and command information, … and a memory bank switch … to receive data information and direct the data information to one of a plurality of physical memory banks in real-time according to control signals from the control unit"). As discussed above, ¶¶193-200, it would have been obvious to a Skilled Artisan to combine the teachings of Ellsberry and Perego, including Ellsberry's teaching of directing data to only one of the memory ranks, namely the one which

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is the target of a read or write command. A Skilled Artisan would have been motivated to make the combination in order to reduce power consumption and increase performance. EX1071 at 15:40-45 ("By accessing a subset of secondary channel signal lines per transaction, a number of benefits may be derived. One of these benefits is reduced power consumption. Another benefit is higher performance by grouping memory devices into multiple independent target subsets (i.e. more independent banks).").

293. If Netlist were to argue that the claim requires a single data channel to both ranks, just like in the JESD21-C standard, Perego also teaches such an embodiment. For example, Perego discloses that a single channel is used to access two memory devices (652 and 653) coupled to the same data lines (DQ3 and DQ4), similar to the JESD21-C standard. *Compare, e.g.*, EX1071 at FIG. 5E (reproduced below with annotations), *with* EX1062 at p. 16.

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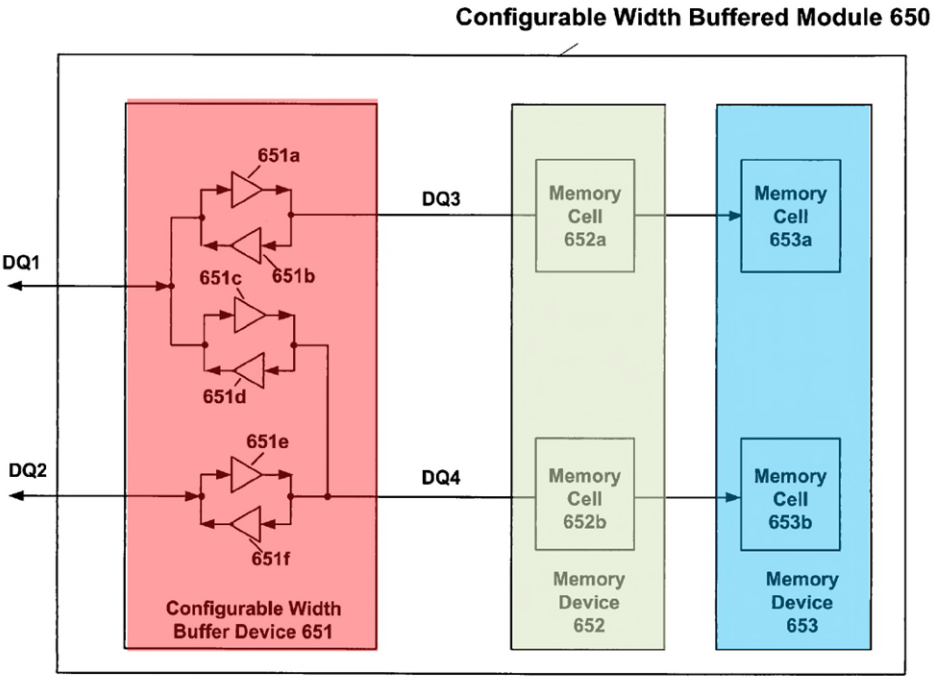

Fig. 5E

294. Perego also discloses that its module can be implemented with a single channel. *Id.* at 10:14-15 ("Although two channels 415a and 415b are shown in FIG. 4A, a single channel is also feasible."). A Skilled Artisan would have understood from Perego's disclosure that such a single channel to two ranks of DDR SDRAMs can be implemented in the way showed in FIG. 5E of Perego and also described in the JESD21-C standard. *See* EX1062 at p. 16. A Skilled Artisan would have also understood that, because the data lines are shared by multiple SDRAM memories, each of those memories receives a respective chip select signal, which selects the memory that outputs the data in response to a read command or writes the data into memory in response to a write command, similar

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to the JEDEC standard. *Id*. (showing that a two-rank module having two chip selects RS0 and RS1, each coupled to respective rank); *see also* EX1069, pp. 2-3 (similar). Accordingly, Perego discloses and it renders obvious to a Skilled Artisan this limitation, even if it requires such a "straight-line" arrangement of the memory devices.

(2) The Narrower Interpretation Consistent with the Plain Meaning

295. Perego also discloses, and at least renders obvious alone or in combination with Ellsberry, to a Skilled Artisan a narrower interpretation of the terms (1) "*the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and*" (2) "*wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command*" where those terms require **selective access** to either the "first" or "second" rank. That is, when the "first rank … receive[s] or output[s]the first data burst in response to the first memory command," the "second rank" does not receive or output those "first" data signals. Similarly, when the "second rank … receive[s] or output[s] the second data burst in response to the second memory command," the "first rank" does not receive or output those "second" data signals. This narrower

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interpretation is supported by the claim language which expressly requires that the reception or output of the data in a specific rank has to happen in response to a corresponding command, while the other rank is not selected to communicate data in response to that command. Thus, under this narrower interpretation, a rank which is not selected in response to that command should not receive or output any data.

296. Similarly, claim elements [1.f.1] and [1.f.2] (*see infra* ¶¶312-324) require that logic be configured, in response to the first command, "*to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer*" and, in response to the second command, "*to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer*." This claim language differentiates enabling access to the first rank from enabling access to the second rank, further supporting an interpretation where the "buffer" selectively transfers the "first" data burst between the "first" rank and the system memory controller, and the "second" data burst between the "second" rank and the system memory controller. Under this interpretation, the buffer does <u>not</u> transfer (1) the "first" data burst to or from the "second" rank in response to the "first" command or (2) the "second" data burst to or from the "first" rank in response to the "second" command.

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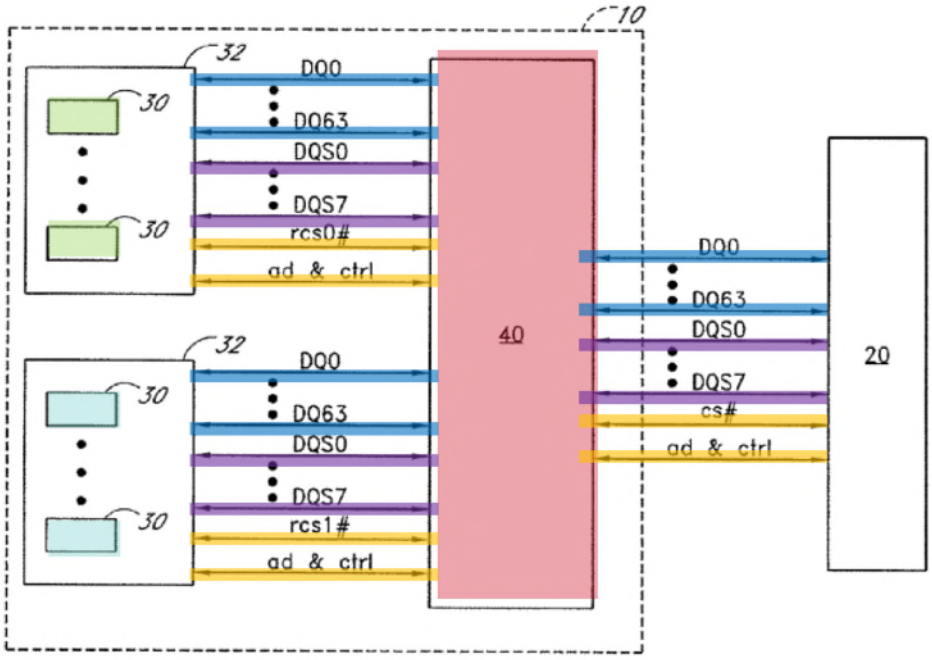
297. This narrower interpretation is also supported by the specification of the 215 Patent which explains that the different ranks are on different "forks" of the data paths, that is, each rank (light green or blue) has its own data (DQ, blue) and strobe (DQS, purple) lines from the buffer 40, while the buffer 40 communicates with the system through a single set of data and strobe lines, resulting in a "fork" in the data path at the buffer 40. *See, e.g.*, EX1001 (215 Patent) at FIG. 1 (reproduced with annotations below).



298. In the arrangement shown in Figure 1 of the 215 Patent above, the data and strobe signals output or received by one rank (light green) are not received or output by the other rank (light blue) because they are on separate data paths:

> "The circuit 40 of certain embodiments controls the isolation of the DQS data strobe signal lines 104a, 104b by monitoring commands received by the memory module 10 from the computer system and producing "windows" of operation whereby the appropriate switches 130 are activated or deactivated to enable and disable the DQS data strobe signal lines 104a, 104b to mitigate BBARX collisions. In certain other embodiments, the circuit 40 monitors the commands received by the memory module 10 from the computer system and selectively activates or deactivates the switches 120 to enable and disable the DQ data signal lines 102a, 102b to reduce the load of the memory module 10 on the computer system. In still other embodiments, the circuit 40 performs both of these functions together."

Id. at 13:36-49; *see also id.* at FIG. 8C (reproduced below).

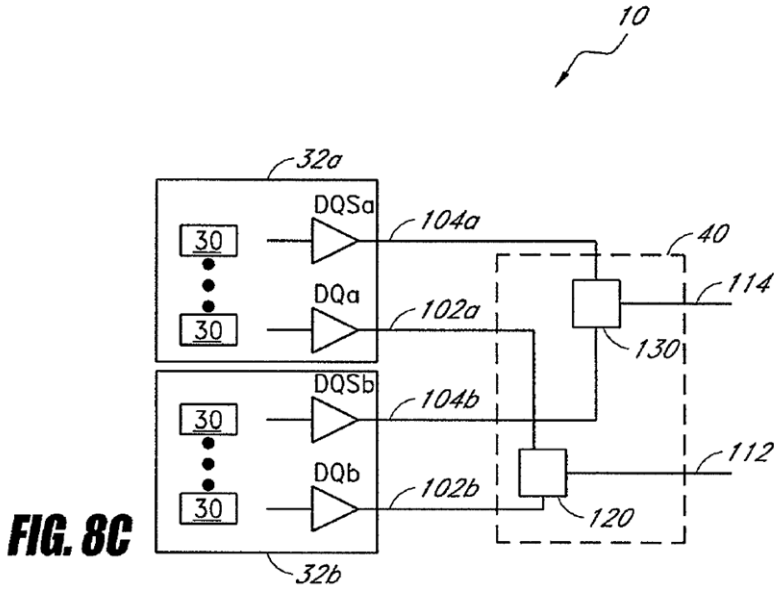


FIG. 8C

299. Perego, like the 215 Patent, discloses a separate data bus, for example, in channel 370 for one rank on the left, and another data bus in channel 370 for one rank on the right, thus satisfying this limitation even under the narrower claim interpretation discussed above. *See*, *e.g.*, EX1071 at FIG. 3C (reproduced with annotations below). For example, Perego explains that "Buffer device 350 …

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receives the data via **one** … of channels 370." *Id.* at 6:21-22; *see also id.* at 21:16-20 ("Any number of channels … may transfer information simultaneously and the memory devices on the other … channels … remain in a ready or standby state until called upon to perform memory access operations.").

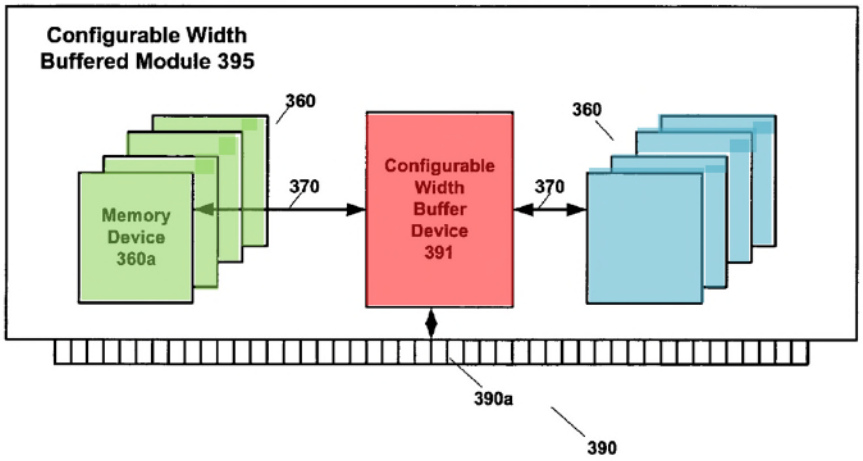

Fig. 3C

300. Similarly, Perego discloses that one pair of channels, e.g., 415c/d coupled to the "*first*" rank (green), is used for one data transaction while the other pair of channels, e.g., 415a/b coupled to the "*second*" rank (blue), is not used for that data transaction. *Id.* at FIG. 4B & 21:16-20 ("… for example[,] two channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations.").

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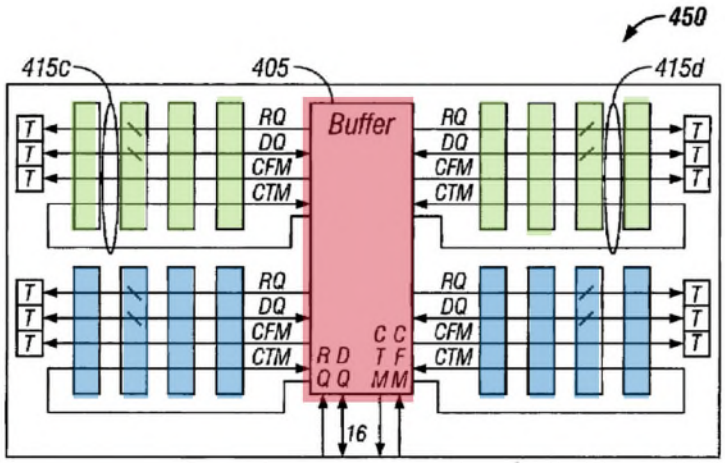

FIG. 4B

301. Perego teaches that the selective access of the different ranks can be achieved by "employ[ing] a configurable datapath router within interface 591 to route requests between the primary channel and the target subset of secondary channel signal lines for each transaction." *Id.* at 15:31-37. Perego also explains the benefits of accessing only an independent target subset, such as a rank, thus providing express motivation to a Skilled Artisan for accessing only a target rank of the memory devices while not accessing the other ranks. *Id.* at 15:40-45 ("By accessing a subset of secondary channel signal lines per transaction, a number of benefits may be derived. One of these benefits is reduced power consumption. Another benefit is higher performance by grouping memory devices into multiple independent target subsets (i.e. more independent banks)."). Furthermore, a Skilled Artisan would have understood that, when a single channel or a pair of channels provides the requested data, there is no need to access the other channels.

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Id. at 14:10-31 ("Configurable width buffer device 391 also has a maximum memory device access width defined as the largest number of bits that can be accessed in a single memory device transfer operation."). As discussed above, *supra* at ¶292, Ellsberry also teaches such a selective access to the first or second rank, and it would have been obvious to a Skilled Artisan to implement Ellsberry's selective access functionality in the module of Perego.

302. Thus, Perego discloses and renders obvious alone or in combination with Ellsberry to a Skilled Artisan that, when data is transferred between a specific rank and the buffer device on the module, the other ranks on the module do not receive or output any data and no data is transferred to or from those other ranks.

(3) Conclusion for These Claim Limitations

303. Therefore, regardless of the disputed claim interpretation, Grounds 1-4 disclose or render obvious to a Skilled Artisan that (1) "*the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and*" (2) "*wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command.*"

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e) [1.e] Buffer

304. Claim 1 requires "*a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus; and*."

305. The prior art references in Ground 1 (specifically, Perego) teach this limitation to a Skilled Artisan. This limitation is also taught by Grounds 2-4 at least because they include Ground 1.

306. As an initial matter, in my opinion, nothing in the claims, specification, or prosecution history of the 215 Patent would suggest to a Skilled Artisan that the recited "buffer" must be a physically separate component from the earlier-recited "register," and instead suggest the opposite. Indeed, the dependent claims (such as dependent claim 8) explicitly inform a Skilled Artisan that a buffer can comprise "registers." EX1001 at 38:35-39. The claim language also informs a Skilled Artisan that a register can incorporate a buffer and act as a buffer. *Id.* at 37:27-31 ("a register coupled to the printed circuit board and configured to receive and buffer…."). The specification similarly informs a Skilled Artisan that the register can incorporate a buffer and act as a buffer. *Id.* at 14:46-51 ("The register 230 receives and buffers …."); 16:12-14 ("The A_0-A_n row/column address signals are received by the register 230, which buffers these address signals …."). The specification similarly informs a Skilled Artisan that "memory module 10" can

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"operate[] as having a data path rank buffer" (*id.* at 9:26-31) and comprise a "register" (*id.* at 14:37-43), and also informs a Skilled Artisan that elements comprising "memory module 10" (a "lock loop device 220" and a "register 230") along with a "circuit 40" can be "portions of a single component" (*id.* at 14:37-40 & 14:53-57). Figure 1 of the 215 Patent specification also shows a Skilled Artisan that the same circuit 40 in memory module 10 can buffer both address/control ("ad & ctrl") and data (DQ0-DQ63) lines:

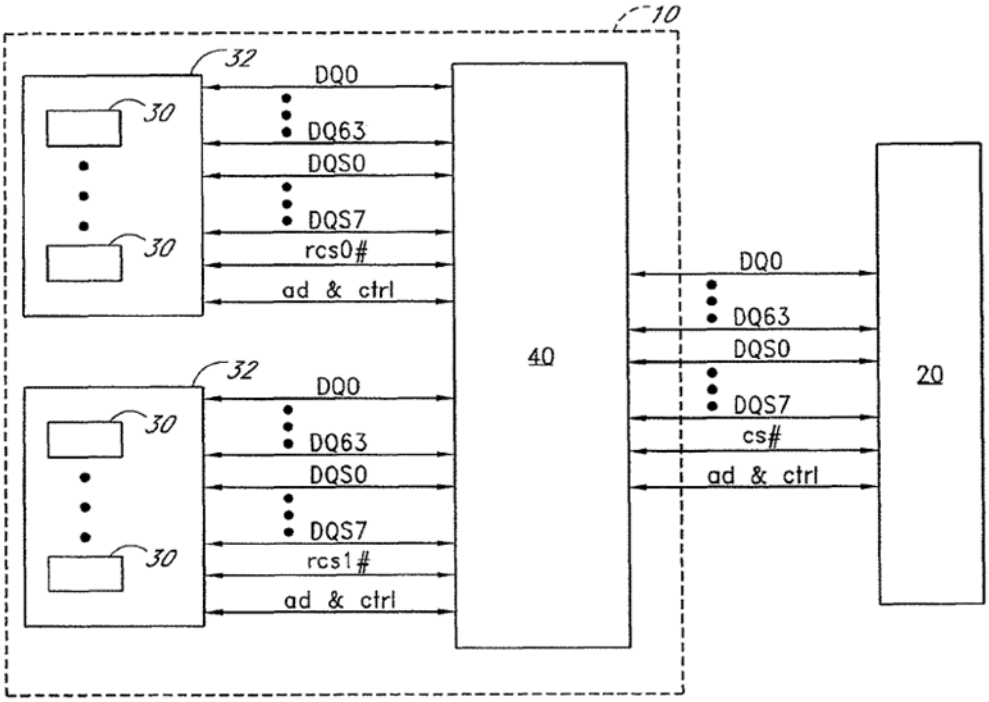

FIG. 1

Id. at FIG 1, *see also id*. at 5:38-43 ("As used herein, the term "circuit" is a broad term which includes, without limitation, an electrical component or device, or a configuration of electrical components or devices which are electrically or

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electromagnetically coupled together (e.g., integrated circuits), to perform specific functions."), 6:48-51 ("In certain embodiments, the logic element comprises various discrete electrical elements, while in certain other embodiments, the logic element comprises one or more integrated circuits.").

307. Perego discloses a "*buffer*," including circuitry in its buffer device (e.g., buffer device 391 in FIGS. 3C and 5B and buffer device 405 in FIGS. 4A, 4B and 5A) for buffering and/or routing data signals in interfaces 520a and 520b, multiplexers 530a and 530b, and interface 510 or 590. This circuitry is between the memory bus coupled to interface 510 or 590 and (1) the at least one first memory integrated circuit in the "*first*" rank (e.g., a rank coupled to interface 520a), and (2) the at least one second memory integrated circuit in the "*second*" rank (e.g., a rank coupled to interface 520b). *See, e.g.,* EX1071 (Perego) at FIGS. 5A and 5B (reproduced below with annotations).

308. For example, Perego discloses that its buffer device isolates signals of the memory devices, including data signals, from signals interfacing the memory controller. *Id.* at 4:38-42 ("It follows from these definitions that a memory module having a buffer device (e.g., having a configurable width) isolating data, control, and address signals of the memory devices from the connector interface may be a memory subsystem."), 6:12-15 ("With further reference to FIGS. 3A and 3B,

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buffer device 350 transceives and provides isolation between signals interfacing to controller 310 and signals interfacing to the plurality of memory devices 360.”).

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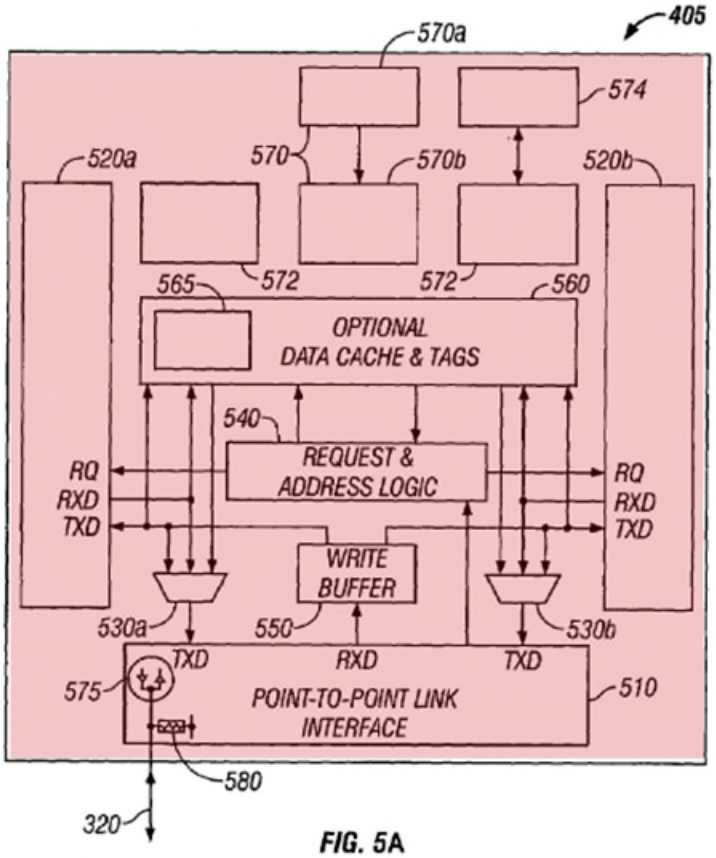
405
570a
574
520a
570
570b
520b
565
572
572
560
OPTIONAL
DATA CACHE & TAGS
540
REQUEST &
ADDRESS LOGIC
RQ
RXD
TXD
RQ
RXD
TXD
WRITE
BUFFER
530a
550
530b
TXD
RXD
TXD
575
POINT-TO-POINT LINK
INTERFACE
510
580
320

FIG. 5A

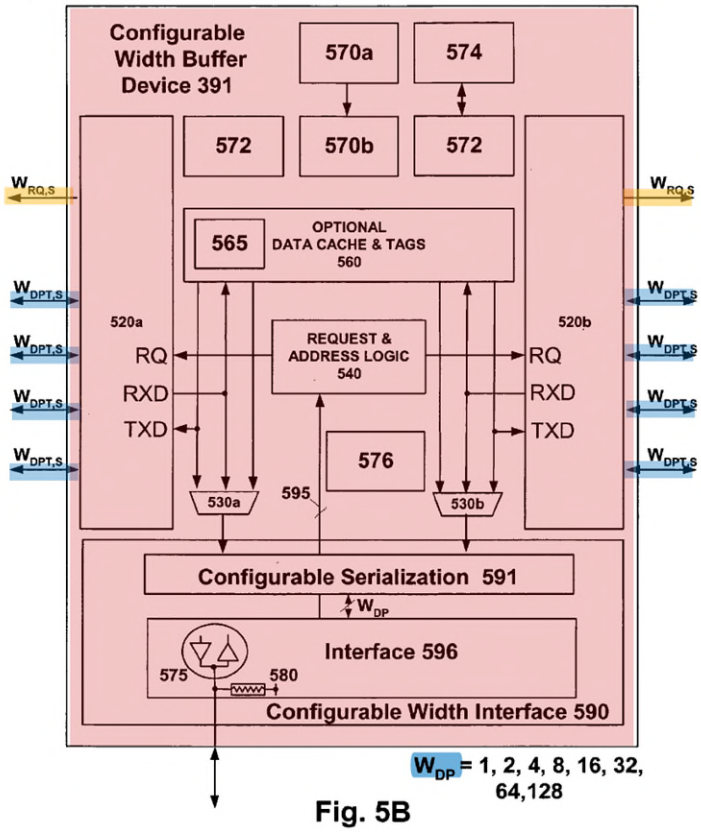

Fig. 5B

309. In particular, Perego's Figs. 5A and 5B illustrate such data buffering circuitry in an implementation of Perego's buffer device, such as buffer device 405 in Figs. 4A and 4B and buffer device 391 in FIG. 3C. *Id.* at 11:1-7, 13:6-10. Perego also discloses that buffer device 391 and 405 can be used in memory systems such as memory systems 300 and 305 in Figures 3A and 3B. *Id.* at 7:30-34, 10:59-67.

310. A Skilled Artisan would have understood that the circuitry for handling data signals in interfaces 520a and 520b, multiplexers 530a and 530b, and interface 510 or 590 is a "*buffer*" because it includes data buffers, such as

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transceivers 575 in interface 510 or 590 and transceivers in interfaces 520a and 520b:

> "Also, in an embodiment of the present invention, one or more transceiver 575 (FIG. 5B) and termination 580 are associated with each port in interface 596. In this specific embodiment, transceiver 575 includes a transmit circuit to transmit data onto a signal line (external to configurable width buffer device 391) and a receiver circuit to receive a data signal on the same signal line."

Id. at 13:18-24.

> "In addition, the number of transceiver circuits included in interface 520a and 520b that are employed to communicate with one or more memory devices"

Id. at 14:65-15:2. Furthermore, Perego discloses that each of interfaces 510, 590 and 520a and 520b can include latches, which a Skilled Artisan would have understood also buffers the data signals. *Id.* at FIG. 5C (reproduced below with annotations, showing input/output latches 597f-m for latching data signals), and 17:61-63 ("Multiplexer/demultiplexer circuit 597 includes input and output latches 597f–m, two for each configurable width buffer device data connection in interface 596."), and 18:65-19:3 ("In embodiments of the present invention, interfaces 520a and 520b include multiplexer/demultiplexer circuit 597, also known as a type of partial crossbar circuit, for transferring signals between configurable width buffer device 391 and memory devices on configurable width buffered module 395.").

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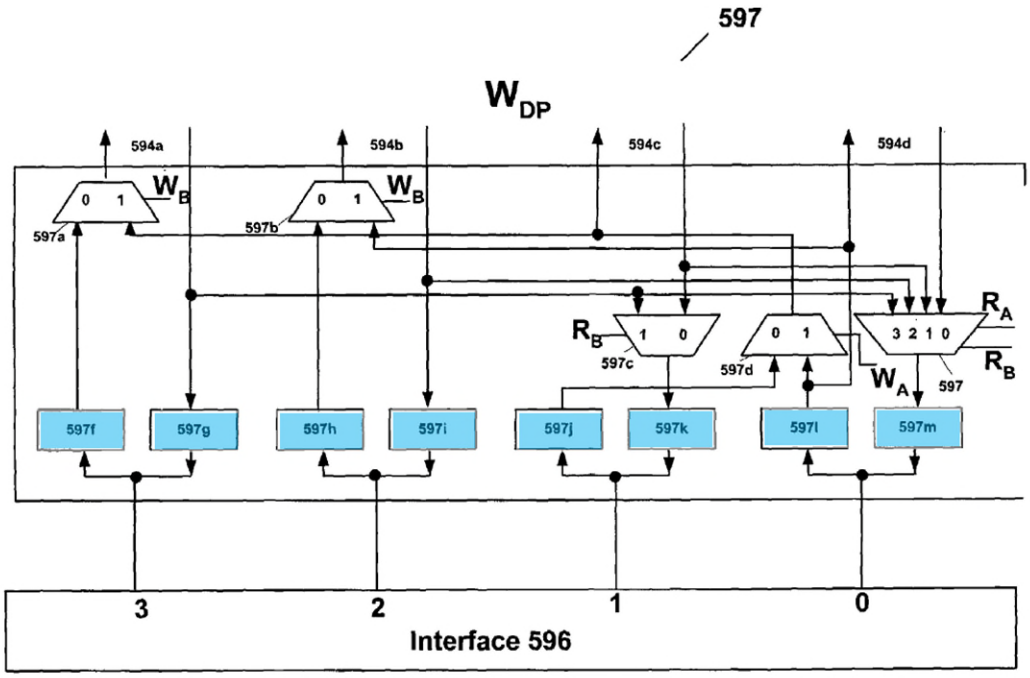

Fig. 5C

311. Accordingly, Perego discloses to a Skilled Artisan "*a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus; and*."

f) [1.f.1]-[1.f.2] Logic

312. Claim 1 requires (1) "*logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer,*" and (2) "*wherein the logic is further configured to respond to the second memory*

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command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different than the first control signals."

313. The prior art references in Ground 1 (specifically, Perego) teach this limitation to a Skilled Artisan. This limitation is also taught by Grounds 2-4 at least because they include Ground 1. For example, Ellsberry also discloses this limitation.

314. Perego discloses "*logic*" in its buffer device (e.g., buffer device 391 in FIGS. 3C and 5B and buffer device 405 in FIGS. 4A, 4B and 5A), including logic in the interface to the system memory controller (interface 590 or 510), interfaces 520a and 520b to the memory devices, Request & Address Logic 540, and computation block 565. EX1071 (Perego) at FIGS. 5A & 5B. This "*logic*" is coupled to the "*buffer*" which buffers and/or routes data signals through interfaces 520a, 520b, multiplexers 530a and 530b, and interface 510 or 590. *Id.* Perego also discloses that its "*logic*" is configured to respond to the first memory command (read or write) by providing first control signals to the "*buffer*" to enable communication of the first data burst between the at least one first memory integrated circuit in the "first" rank and the memory controller (310) through the

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"*buffer*," as discussed above with reference to claim element [1.e]. *See supra* ¶¶304-311.

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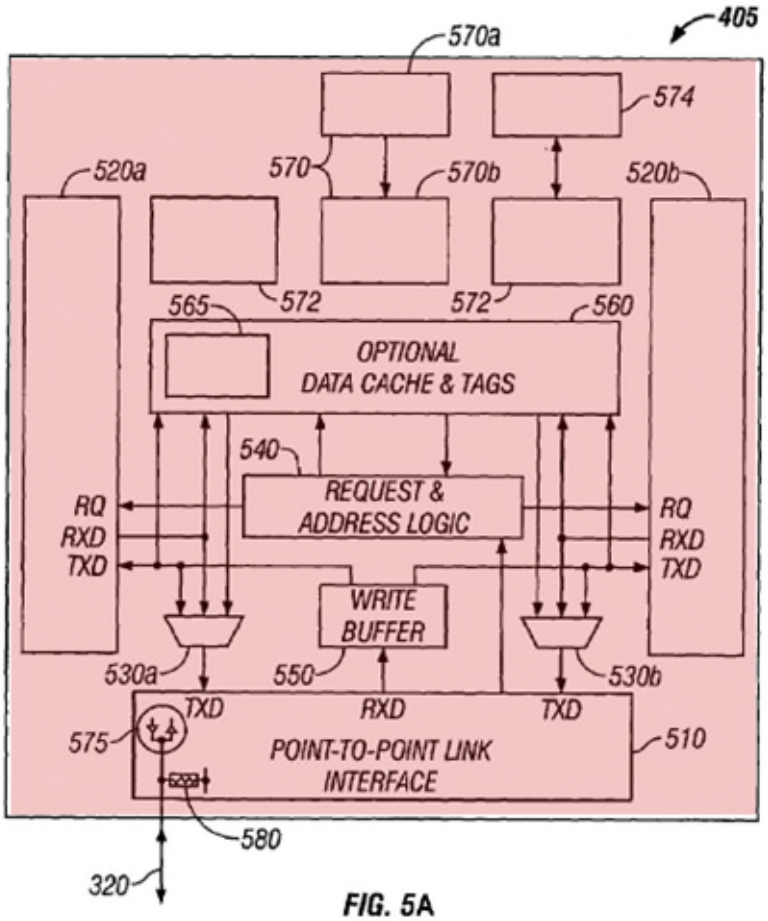

FIG. 5A

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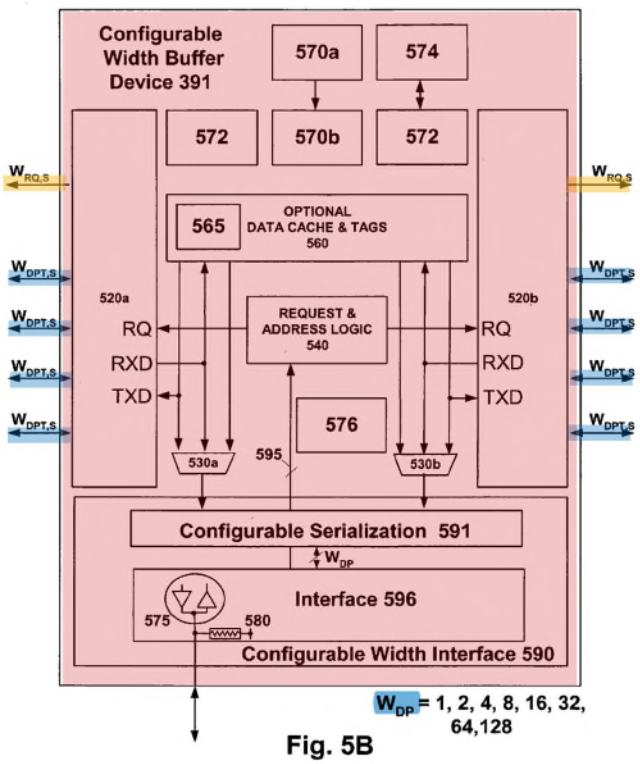

Fig. 5B

315. For example, Perego explains that "control information and address information may be decoded and separated from multiplexed data and provided on lines 595 to request & address logic 540 from interface 596. The data may then be provided to configurable serialization circuit 591." EX1071 at 13:54-59. "Computation block 565 may include a processor or controller unit, a compression/decompression engine, etc., to further enhance the performance and/or functionality of the buffer device." *Id*. at 12:9-12.

316. As discussed above with reference to claim elements [1.a.2], [1.a.3], and [1.d.2]-[1.d.3] (*see supra* ¶¶217-239 & 283-303), Perego discloses that commands and corresponding data bursts are selectively routed to and from a

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subset of the memory devices and the memory controller through the buffer device, for example:

> "According to an embodiment of the present invention, multiplexers 530a and 530b perform bandwidth-concentrating operations, between interface 510 and interfaces 520a and 520b, as well as route data from an appropriate source (i.e. target a subset of channels, internal data, cache or write buffer)."

EX1071 at 11:56-61.

> "In a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370. One or more of memory devices 360 may respond by transmitting data to Buffer device 350 which receives the data via one or more of channels 370 and in response, transmits corresponding signals to controller 310 via point-to-point link 320a."

Id. at 6:15-25; *see also id*. at 21:16-20 ("Any number of channels 415a–415d, for example[,] two channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations.") and 15:40-45 ("By accessing a subset of secondary channel signal lines per transaction, a number of benefits may be derived. One of these benefits is reduced power consumption.").

317. A Skilled Artisan would have understood from these disclosures that Perego's buffer device includes logic that sends control signals to the interfaces 520a and 520b to activate only the channel that transfers the data burst between the memory controller (coupled to interface 510 or 590) and the targeted rank (thus to

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or from the memory devices in the targeted rank), keeping the other channels in a ready or standby state.

318. As discussed above with reference to claim element [1.c] (*see supra* ¶¶249-260), Perego further teaches that interfaces 520a, 520b, 510 and 590 include transceivers, such as transceivers 575, that are controlled in accordance with the received memory command:

> "Channels 370 (FIG. 3C) may be subdivided into several addressable subsets. The address of the transaction will determine which target subset of channels 370 will be utilized for the data transfer portion of the transaction. … Typically, configuration of the transceivers may be effectuated by enabling or disabling how many transceivers are active in a given transfer between one or more memory devices and configurable width buffer device 391."

EX1070 at 14:62-15:6; *see also id.* at Figs. 5A and 5B. Perego further teaches that "multiplexer/demultiplexer circuit 597 contains multiplexing logic and demultiplexing logic. The multiplexing logic is used during read operations, and the demultiplexing logic is used during write operations[]" (*id.* at 17:41-44) and that "[m]ultiplexer/demultiplexer circuit 597 includes input and output latches 597f–m[]" (*id*. at 17:61-62).

319. A Skilled Artisan would have understood from these disclosures that Perego's buffer device includes logic that sends control signals to the transceivers, multiplexing/demultiplexing circuits, and to the input and output latches to selectively activate these circuit elements of the "buffer" in accordance with the

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targeted rank and direction of the read and write operations. As discussed above, the targeted rank can be determined from an address when Perego's module implements rank multiplication. *Supra* at ¶¶171-174; *see also* EX1071 (Perego) at 14:63-65 ("The address of the transaction will determine which target subset of channels 370 will be utilized for the data transfer portion of the transaction."), 15:34-40 ("configurable width buffer device 391 may employ a configurable datapath router within interface 591 to route requests between the primary channel and the target subset of secondary channel signal lines for each transaction. According to a preferred embodiment, the target subset of secondary channel signal lines may be selected via address bits provided as part of the primary channel request"). Furthermore, Ellsberry also discloses logic in its Control ASIC that responds to a read or write command by controlling the Switch ASICs to direct the corresponding data communication to the target memory rank that is selected based on an address signal to implement rank multiplication:

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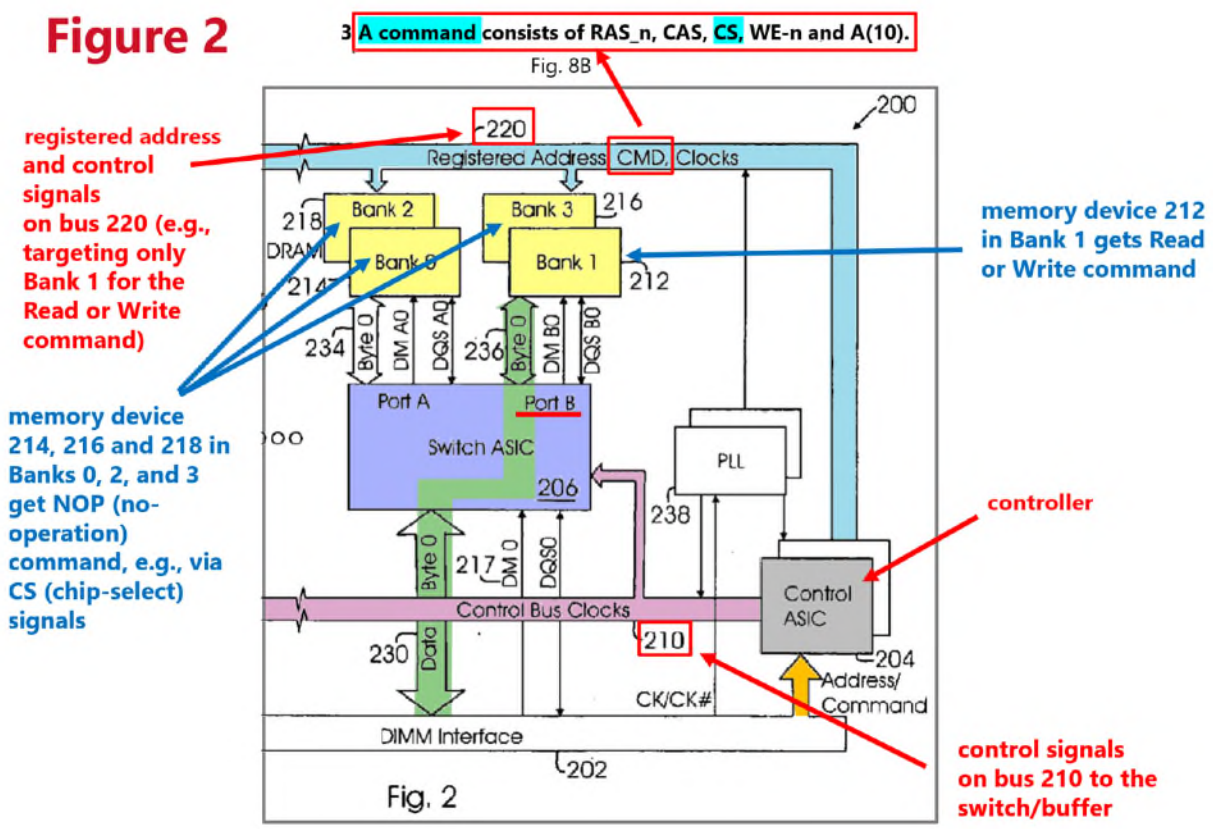

EX1073 (Ellsberry) at [0010] ("A state machine is used to send Read/Write commands to the intended memory bank while sending no-operation commands to the other memory bank."), [0036] ("The state machine implemented by the control unit 204 directs data to a particular memory bank based on the memory configuration of memory banks and the address received. For example, one or more of the address bits (e.g., in a column and/or row address bits) may be used to direct data to a particular memory bank."), Figs.2-4, 7-8, and Claim 1 ("the memory bank switch to receive data information and direct the data information to one of a plurality of physical memory banks in real-time according to control signals from the control unit"). As discussed above, it would have been obvious to

a Skilled Artisan to combine the teachings of Perego and Ellsberry, and she would have been motivated to make that combination, for example, to implement Ellsberry's rank multiplication in the buffered module of Perego. *Supra* at ¶¶193-200.

320. Thus, Perego discloses and renders obvious alone or in combination with Ellsberry to a Skilled Artisan "*logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer*."

321. Additionally, because Perego's (and Ellsberry's) logic responds to the subsequent second memory command by providing control signals to the "*buffer*" in accordance with that second command for the reasons discussed above with reference to claim element [1.f.1] (*see supra* ¶¶312-320), Perego also discloses and renders obvious alone or in combination with Ellsberry to a Skilled Artisan that "*the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer*."

322. Finally, Perego also discloses "*the second control signals being different from the first control signals.*" Ellsberry also discloses this limitation.

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323. For example, as discussed above, the "*first*" rank is selected to receive or output the "*first*" data burst and the "*second*" rank is selected to receive or output the "*second*" data burst, and the "*first*" and "*second*" ranks are coupled to different channels of Perego's buffer device. *See supra* at ¶¶261-303 (claim elements [1.d.1] and [1.d.2]-[1.d.3]). Thus, the "*second control signals*" for routing the second data burst select one or more different channels than the "*first control signals*" for routing the first data burst. Accordingly, a Skilled Artisan would have understood from Perego's disclosure that the "*second control signals*" are different from the "*first control signals.*" A Skilled Artisan would have also understood that, to the extent the first and second data bursts are transmitted in different directions, the "*first*" and "*second*" control signals also differ in order to control the difference in the direction. Similarly, Ellsberry discloses directing the data to a rank of memory devices that is coupled to either Port A or Port B, which a Skilled Artisan would have understood can be implemented in an ordinary manner by using different control signals from the Control ASIC to the Switch ASICs. *Supra* at ¶319.

324. Accordingly, Perego discloses and renders obvious alone or in combination with Ellsberry "*logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory*

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integrated circuit and the memory controller through the buffer," and "*wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different than the first control signals*."

2. Claim 2 is Unpatentable

325. In my opinion, Claim 2 is unpatentable because it is obvious in view of Grounds 1-4.

326. Claim 2 requires "*[t]he memory module of claim 1, wherein the buffer is configured to isolate both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory controller*."

327. Perego discloses to a Skilled Artisan that the buffer, as discussed above with reference to claim element [1.e] (*see supra* ¶¶304-311), is configured to, when the memory module is not being accessed by the memory controller, isolate from the memory bus both (1) the at least one first memory integrated circuit in the first rank and (2) the at least one second memory integrated circuit in the second rank.

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328. For example, Perego teaches that its buffer device isolates the signals interfacing the memory devices from the signals interfacing the memory controller. EX1071 (Perego) at 6:12-15 ("With further reference to FIGS. 3A and 3B, buffer device 350 transceives and provides isolation between signals interfacing to controller 310 and signals interfacing to the plurality of memory devices 360.").

329. Perego further teaches that, advantageously, only the targeted rank of its memory module is accessed, for example:

> "… [C]onfigurable width buffer device 391 may employ a configurable datapath router within interface 591 to route requests between the primary channel and the target subset of secondary channel signal lines for each transaction. By accessing a subset of secondary channel signal lines per transaction, a number of benefits may be derived. One of these benefits is reduced power consumption. Another benefit is higher performance by grouping memory devices into multiple independent target subsets (i.e. more independent banks)."

Id. at 15:31-45. The ranks that are not being accessed are in a ready or standby state "until called upon to perform memory access operations." *Id.* at 21:16-20 ("Any number of channels 415a–415d, for example; two channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations.").

330. A Skilled Artisan would have understood from this disclosure that, when the memory module is not accessed by the memory controller, each of its ranks is isolated and remains in a ready or standby state. To the extent one might

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argue that Perego does not disclose the claimed isolation, it would have been obvious to a Skilled Artisan in view of Perego's disclosures because Perego expressly teaches the advantages of such isolation, including power savings. *Id.* at 20:42-47 ("According to embodiments of the present invention, subsets of available memory devices on configurable width buffered module 395 are activated or powered-on during various modes of operation. Thus, configurable width buffered module 395 is able to achieve power savings by only powering particular memory devices."). The advantages of isolating the memory devices from the memory bus were well known at the time. *See, e.g.,* EX1078 (Halbert) at 4:23-26 ("The memory systems and modules described herein generally improve upon the multi-drop memory bus architecture by isolating the memory devices on each module from the bus…"); EX1073 (Ellsberry) at [0031] ("Additionally, each memory bank switch 206 and 208 includes signal drivers to drive data signals to and from the memory banks and to and from the DIMM interface 202. This reduces resistive and/or capacitive loading of the data bus coupled to the DIMM interface and the bus 110 while emulating a standard memory device interface.").

331. Accordingly, Perego discloses to a Skilled Artisan that "*the buffer is configured to isolate both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory controller.*"

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3. Claim 3 is Unpatentable

332. In my opinion, Claim 3 is unpatentable because it is obvious in view of Grounds 1-4.

333. Claim 3 requires "*[t]he memory module of claim 1, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits*."

a) Perego's Disclosures

334. Perego discloses to a Skilled Artisan that its memory module has an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits. For example, as discussed above with reference to claim element [1.c] (*see supra* ¶¶249-260), Perego discloses to a Skilled Artisan that its buffer device includes a register to receive and buffer command and address signals, similar to the traditional registered DIMMs. Thus, a Skilled Artisan would have understood based on, for example, their understanding of JEDEC standards, that an overall CAS latency of Perego's memory module has an additional latency of one clock cycle due to registering the address and command signals similar to a registered DIMM. EX1062 (JESD21-C) at p. 68 n.1 ("In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM $\overline{\text{CAS}}$ latency)").

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335. Perego also discloses that its interfaces include circuitry, such as input and output latches 597f–m, which latch the data signals for both read and write data transactions. *See* EX1071 at Fig. 5C & 17:61-63 ("Multiplexer/demultiplexer circuit 597 includes input and output latches 597f–m, two for each configurable width buffer device data connection in interface 596."). Perego's buffer circuit includes "clock circuit 570a-b … to generate internal synchronizing clock signals having a predetermined temporal relationship." *Id.* at 12:65-13:5. A Skilled Artisan would have understood from these disclosures that Perego's latching of the data signals and the use of internal synchronizing clock signals adds a predetermined amount of time delay for each data transfer through the buffer because the output of the latch needs to be in synchronization with an internal clock. A Skilled Artisan would have understood that such registering of the data signals would require the addition of a fixed time delay, such as one clock cycle, for each registered data transfer through the circuitry with respect to the actual operational CAS latency of each of the plurality of memory integrated circuits.

336. A Skilled Artisan would have understood that latencies like the CAS latency of the memory devices are set to a selected value from among a set of predetermined values according to respective standards. For example, the first generation of DDR memory devices could be programmed to have a CAS latency of 1.5, 2, 2.5, or 3 clock cycles. EX1060 (JESD79) at 9-10. Perego expressly

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discloses using DDR2 SDRAM devices, EX1071 at 10:54-59, and a Skilled Artisan would have understood that DDR2 memory devices had latency parameters like CAS latency and Additive Latency that could take values of integer clock cycles only. EX1064 (JESD79-2) at 12 ("The DDR2 doesn't support half clock latency mode."), Fig. 8 (showing CAS Latency of 2, 3, 4, 5), 14 (Fig. 9 showing Additive Latency of 0, 1, 2, 3, 4). Therefore, a Skilled Artisan would have been motivated to implement a whole-clock-cycle latency for registering the data signals in order to be compatible with the corresponding JEDEC standard. A Skilled Artisan would have also understood that a full clock cycle would have provided more time budget for the data registration thereby avoiding synchronization issues and resulting in more stable, reliable operation.

337. A Skilled Artisan would have also understood that interfaces 520a and 520b also use input-output latches in order to synchronize their input-output signals using clock alignment circuits:

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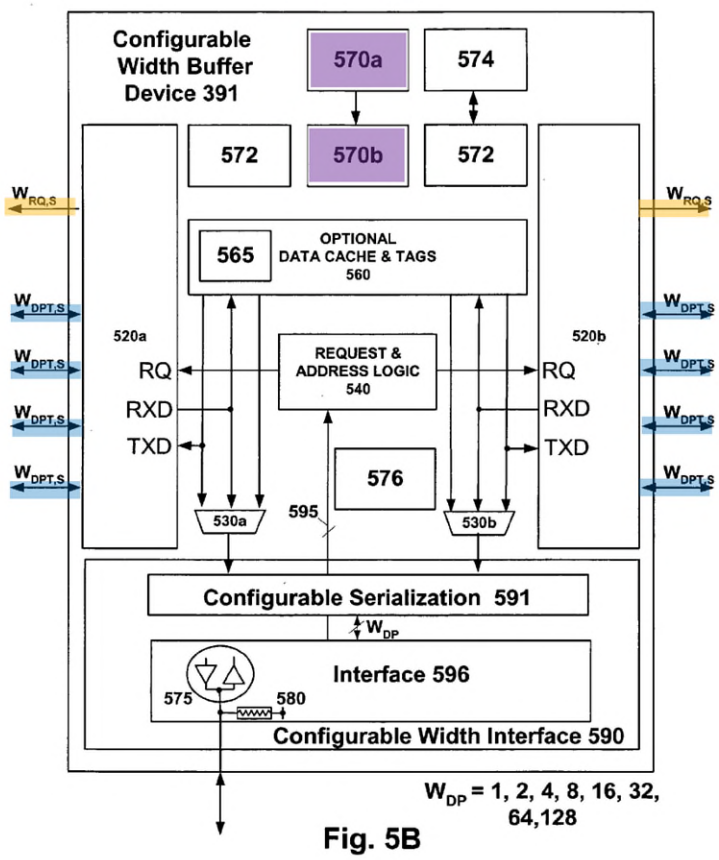

Fig. 5B

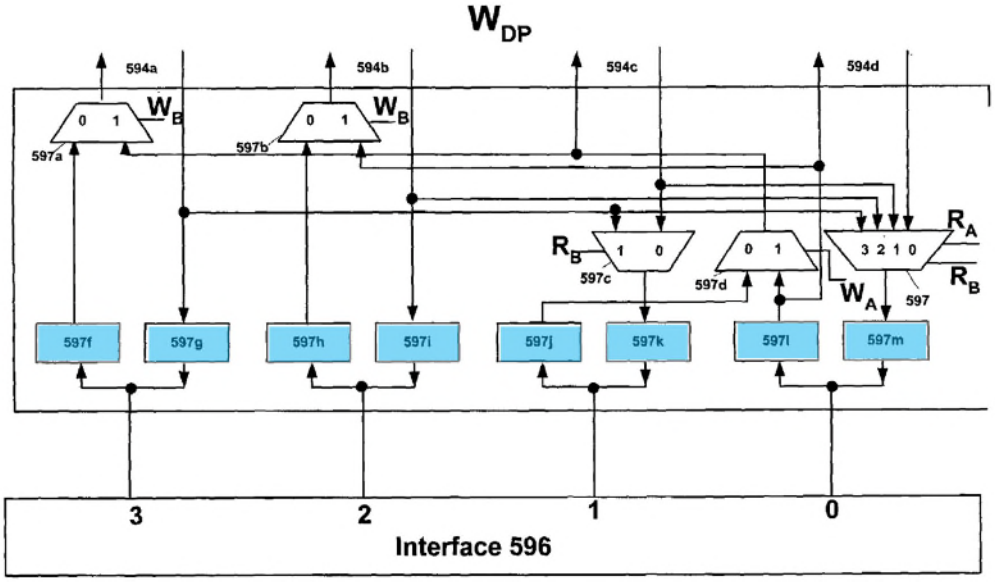

Fig. 5C

Id. at FIGs. 5B and 5C (annotated versions reproduced above).

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> "In embodiments of the present invention, interfaces 520a and 520b include multiplexer/demultiplexer circuit 597, also known as a type of partial crossbar circuit, for transferring signals between configurable width buffer device 391 and memory devices on configurable width buffered module 395."

Id. at 18:65-19:3.

> "[C]lock circuit 570a–b includes one or more clock alignment circuits for phase or delay adjusting internal clock signals with respect to an external clock[.]"

Id. at 12:65-13:5. Thus, a Skilled Artisan would have understood that such latching delays in the buffer device of Perego increase the overall CAS latency of the memory module compared to the CAS latency of the memory devices. As discussed above, the system memory controller needs to adjust the schedule of the data flow and its operation timing according to the overall CAS latency of the read operation, not just the operational CAS latency of the memory circuit. Accordingly, a Skilled Artisan would have understood that, due to the input-output latches in Perego, the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.

338. Thus, Perego discloses to a Skilled Artisan that "*the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits*."

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b) Halbert's Disclosures

339. To the extent one might argue that Perego does not sufficiently disclose that the module's overall latency is greater than an actual operational CAS latency of the memory devices, it would have been obvious in light of Halbert (EX1078, U.S. Patent No. 7,024,518).

340. As discussed above, Halbert is analogous art to the 215 Patent, Perego, and JESD79-2, and discloses a memory module that registers control and address signals, as well as data signals. *See supra* ¶¶261-282 (claim element [1.d.1]). Halbert discloses to a Skilled Artisan that its memory module has an overall CAS latency that is greater than an actual operational CAS latency of each of the plurality of memory integrated circuits due to this registration.

341. For example, Halbert discloses that, by registering the address and command signals (ADD/CMD, yellow) from the system memory controller, the registered address and command signals (RADD/RCMD, orange) are provided to the memory ranks with a delay of one clock cycle due to the registration. EX1078 (Halbert) at 2:46-55 ("After a known RAS (row address strobe) latency, the controller transmits a READ command along with a COL 'a' address. These signals also pass through register 25 with a one-clock cycle delay.") & FIG. 3 (annotated version reproduced below).

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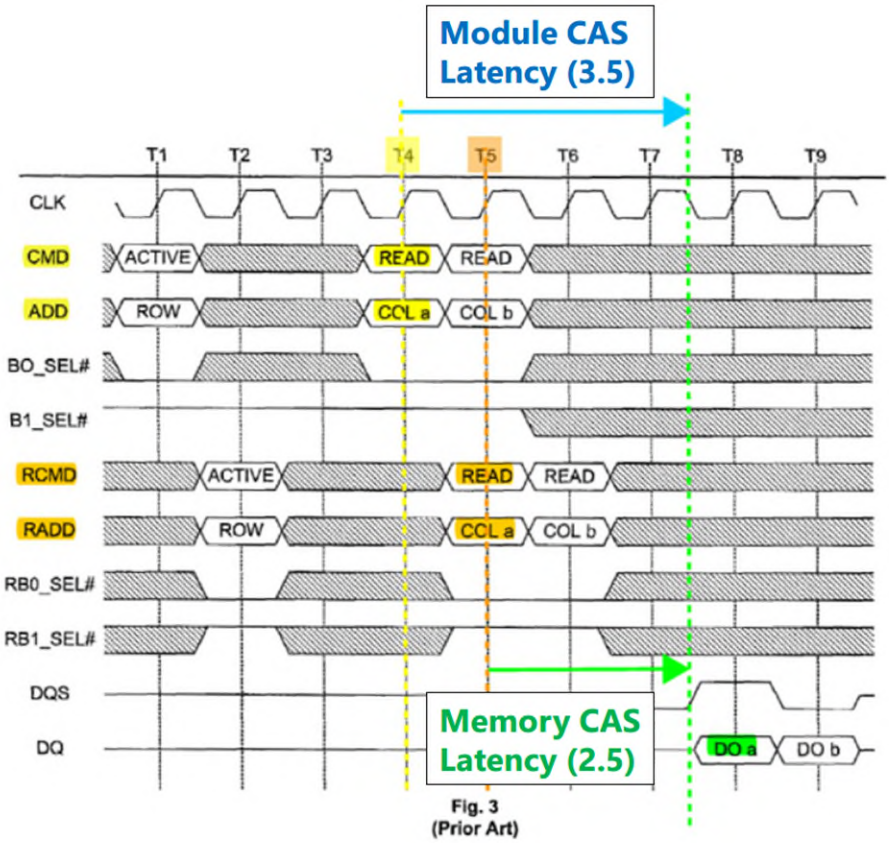

Fig. 3
(Prior Art)

342. In the example of FIG. 3 of Halbert, a read command (CMD/ADD, yellow) for column 'a' is registered at time T4 (yellow), and the registered read command (RCMD/RADD, orange) is transmitted to the memories at time T5 (orange) with one clock-cycle delay. *Id*. "After a known CAS (column address strobe) latency [green arrow], the memory bank places data (DQ a) from ROW and COL 'a' onto bus lines DQ, and DQS is driven as well." *Id*. at 2:55-58. A Skilled Artisan would have understood, for example, based on their knowledge of JEDEC standards, that such a CAS latency (CL) is "the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data." EX1060 (JESD79) at p. 10. In Halbert's example, DDR1 memory devices

were used with an actual operational CAS latency of CL=2.5 (green arrow) from T5 to T7.5, and the CAS latency of the module is CL=3.5 (blue arrow) from T4 to T7.5 due to the delay caused by the module registering the command before it reaches the memory devices. EX1078 (Halbert) at FIG. 3 (annotated version reproduced above). This added CAS latency is consistent with the JEDEC standards for DDR1 memory devices at the time. EX1062 (JESD21-C) at p. 68 n.1 ("In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM CAS latency)"). This is unsurprising, given that FIG. 3 of Halbert is labeled as prior art. *See* EX1078 at FIG. 3.

343. Halbert also discloses that its data interface 120 includes bi-directional data registers 126 and 128 connected, respectively, to memory device array ranks 140 and 142, and data register 122 connected to the system memory data bus (DQ). *Id.* at 5:6-11, 4:60-62; *see also id*. at FIG. 4 (annotated version reproduced below).

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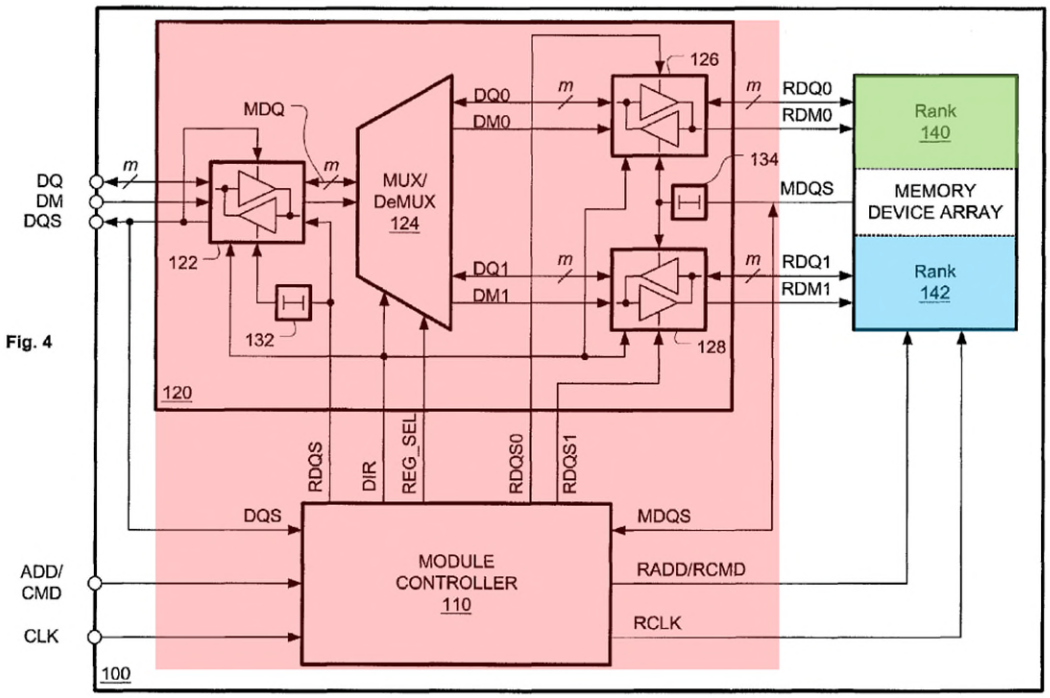

Fig. 4

344. As illustrated in Halbert's FIG. 5 (annotated version reproduced below), its module controller 110 delays the address and command signals (ADD/CMD) transmitted to the memory devices and the registers 122, 126 and 128 delay the data signals from the memory devices, further increasing the CAS latency of the module. EX1078 at 5:66-6:65. Here, as in FIG. 3 of Halbert, the DDR1 memory devices have an actual operational CAS latency of CL=2.5 (green arrow) from T5 to T7n (where 'n' represents a half cycle). The data from rank 140 output at T7n is further delayed by registering them in registers 126 and 122, so that the module starts driving the read data to the memory controller at T8, CL=4 cycles after the read command was registered at T4.

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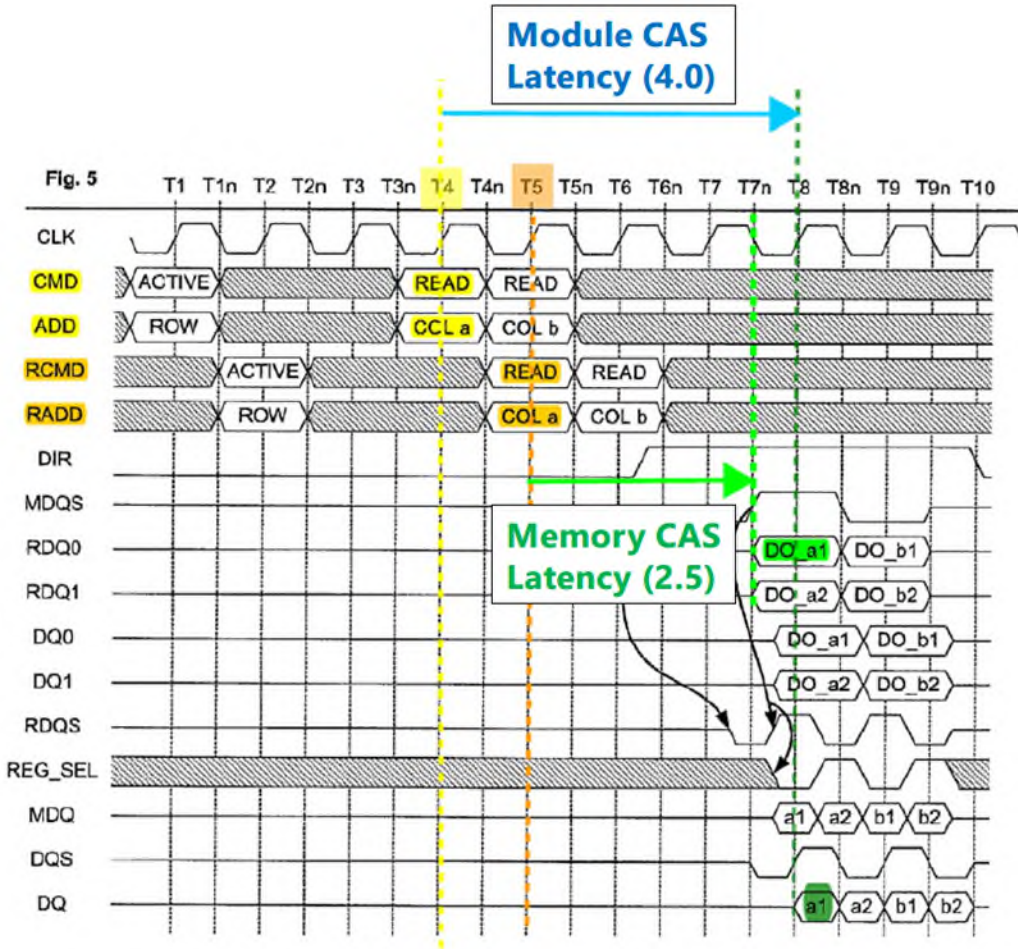

345. As discussed above, for example with reference to claim element [1.c], Perego's module includes a register to receive and buffer the command and address signals of a, say, read command by registering those signals. *See supra* ¶¶249-260. Perego also discloses using DDR2 memory devices, EX1071 at 10:54-59, whose latencies are defined only in terms of integer clock cycles, EX1064 at 12-14. A Skilled Artisan would have understood from Perego's disclosure, in view of Halbert's teaching about CAS latency, that such a registering of a read command increases the CAS latency of the module because the registered address

and command signals for the read operation are transmitted to the memory devices with a delay of one clock cycle due to this registration.

346. Furthermore, as discussed above (for example with reference to claim element [1.e]), Perego's module includes a buffer device that buffers read data from the memory devices, including registering the data signals by latches, such as latches 597f-m shown in Fig. 5C. *See supra* ¶¶304-311. A Skilled Artisan would have understood from Perego's disclosure, in view of Halbert's teaching about CAS latency, that such a registering of the data signals further increases the CAS latency of the module because the registered data signals of the read operation are transmitted from the module to the system memory controller with an additional delay due to this registration, just as in Halbert. Furthermore, a Skilled Artisan would have understood that Perego uses DDR2 memory devices which utilized integer values for CAS latency and Additional latency, and thus would have been motivated to implement the data registering with a full clock cycle latency, as discussed above. *Supra* at ¶336.

347. Additionally, a POSITA would have alternatively been motivated to combine these teachings from Halbert with Perego or the Perego- JESD79-2 combination, given that by doing so the Skilled Artisan would have implemented a predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results or challenges in implementation.

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348. Therefore, Perego in view of Halbert discloses to a Skilled Artisan that "*the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits*."

c) Ellsberry's Disclosures

349. Alternatively, this limitation would have also been obvious in light of Ellsberry.

350. Ellsberry is analogous art to the 215 Patent, Perego, and the JESD79-2 standard. *Supra* at ¶¶193-199. For example, the 215 Patent, Perego, and Ellsberry each is directed to improving memory modules that include DDR2 memory devices described by the JESD79-2 standard and they buffer data signals. For example, the 215 Patent is titled "Memory module with data buffering" and discloses the following:

> "The present invention relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules."

Id. at 1:42-45. Similarly, Perego is titled "Configurable width buffered module" and discloses the following:

> "The present invention relates to a memory system which includes one or more semiconductor memory devices coupled to a buffer device. The buffer device may be disposed on a memory module … [and] provides for flexible system configurations, and several performance benefits. For example, the buffer device may be a configurable width buffer device to provide upgrade flexibility and/or provide high bandwidth among a variety of possible module configurations in the system. A plurality of buffer devices,

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> configurable or otherwise, may be utilized in the memory system to provide high capacity, without compromising performance."

EX1071 (Perego) at 3:13-28. And Ellsberry is similarly titled "Capacity-Expanding Memory Device" and discloses the following:

> "The invention relates to a device, system, and method for expanding the memory capacity of a memory module. A control unit and memory bank switch are mounted on a memory module or, alternately, on a system motherboard to selectively control write and read operations to/from memory devices communicatively coupled to the memory bank switch."

EX1073 (Ellsberry) at [0010]. Additionally, both Perego and Ellsberry disclose a memory module including a buffer device (red) that buffers command, address, and data signals communicated on a system memory bus, on one hand, and two memory ranks (green and blue), on the other hand, where each rank is coupled to the buffer device with a respective data bus on the memory module. *Compare, e.g.*, EX1071 (Perego) at FIG. 3C (annotated version reproduced below), *with* EX1073 (Ellsberry) at FIG. 10 (annotated and rotated version reproduced below). Therefore, a Skilled Artisan would have been motivated to look at Ellsberry for details about implementing certain functionalities in Perego's module as discussed below in more detail.

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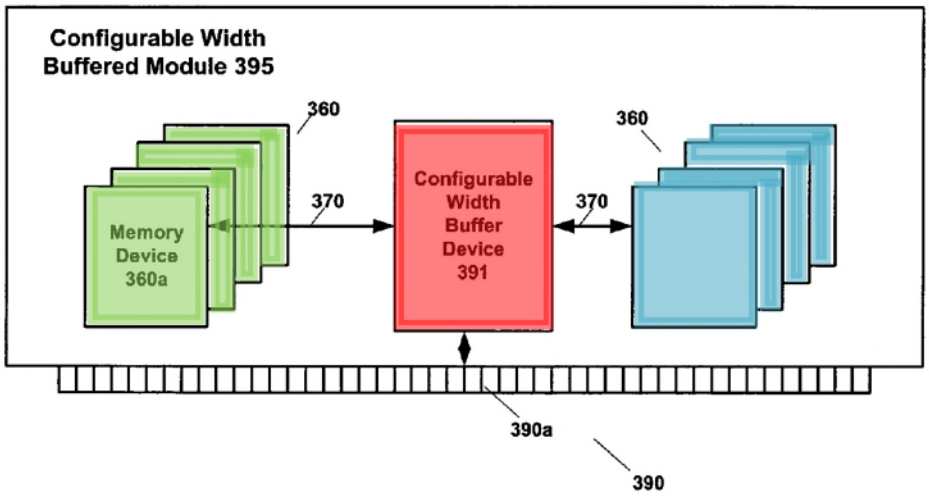
Perego	 Fig. 3C

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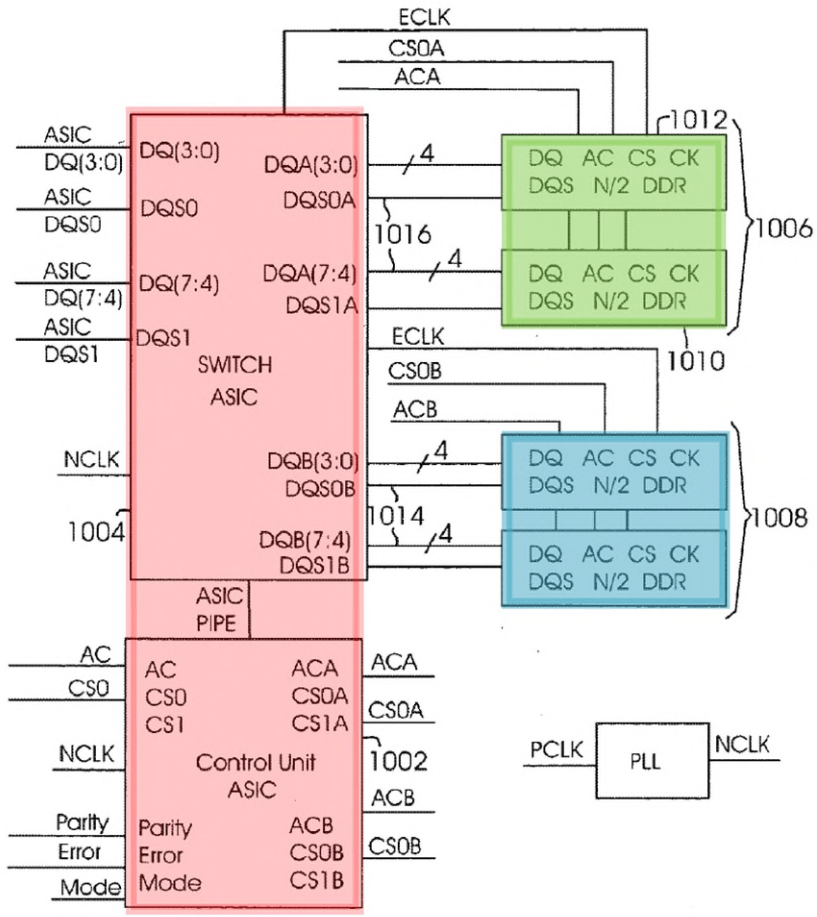
Ellsberry	

351. For example, Ellsberry teaches that its "invention squelches or suppresses extended mode register set (EMRS) commands from being passed to the SDRAMs. Instead of passing these commands directly to the memory devices, the control unit passes the command to the memory bank switch where the values are stored and one or more of the EMRS commands are squelched, modified, or suppressed." EX1073 (Ellsberry) at [0044]. Ellsberry also teaches modifying the CAS latency mode register setting command from the memory controller such that

the memory device has a CAS latency that is one clock cycle less than what is set by the memory controller. *Id*. at Figs. 8A and 8B (annotated versions reproduced below in part).

Command	Mode	Addr	P Bank	DDR A		DDR B	
				Command	Addr	Command	Addr
MRS	X	X	X	MRS	1	MRS	1
EMRS	X	X	X	EMRS	2	EMRS	2

NOTES: 1. if cl_mode = subtract; cl = cl - 1 to DDRs

2. ods squelch-based on ODS setting, rtt squelch-based on REFF setting, ocd squelch-default, dqs_n enable, rdqs disable, out squelch - enable

352. A Skilled Artisan would have understood from these disclosures of Ellsberry that the CAS latency of the memory device is set to be one clock cycle shorter than a CAS latency setting received from the memory controller, in order to allow time for the data to pass through the data buffer. As discussed above, Perego also has a buffer that delays the data signals. *See supra* ¶¶304-311. Thus, a Skilled Artisan would have been motivated to set the CAS latency of the memory devices to be one clock cycle shorter as taught by Ellsberry, in order to allow for the delay caused by the data buffer in the memory module of Perego. A Skilled Artisan would have understood that, by implementing Ellsberry's CAS latency setting functionality in Perego, the memory devices' actual operational CAS

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latency would be less than an overall CAS latency of the module. Implementing such a functionality was well within the level of skill as evidenced by Ellsberry. Additionally, a POSITA would have alternatively been motivated to combine these teachings from Ellsberry with Perego or the Perego- JESD79-2 combination, given that by doing so the Skilled Artisan would have implemented a predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results or challenges in implementation.

353. Accordingly, Perego in light of Ellsberry discloses to a Skilled Artisan that "*the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits*."

4. Claim 4 is Unpatentable

354. In my opinion, Claim 4 is unpatentable because it is obvious in view of Grounds 1-4.

355. Claim 4 requires "*[t]he memory module of claim 1, further comprising an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits*."

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a) Perego's Disclosures

356. As discussed above with reference to Claim 3, Perego, alone or in combination with Halbert, discloses to a Skilled Artisan that the overall CAS latency has one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits. *See supra* ¶¶334-348.

357. Perego also discloses to a Skilled Artisan that its module includes an SPD device that reports an overall CAS latency of the memory module to the memory controller during initialization, by, for example, describing "access latency values" that are stored in a serial presence detect device (SPD):

> "A serial interface 574 may be employed to couple signals utilized in initialization of module or memory device identification values, test function, set/reset, access latency values, vendor specific functions or calibration. … "

EX1071 at 12:20-23.

> "Alternatively the information may be stored in a serial presence detect device (SPD)."

Id. at 15:52-53; *see also* Abstract ("A state storage provides a data width for the configurable width buffer and a SPD provides the configurable width buffer and/or module capabilities to the memory system."), 16:1-5. A Skilled Artisan would have understood that an SPD device must report the latency information on what is happening within the system, including the overall CAS latency, to the controller to allow for proper initialization of parameters and other processes associated with the running of the system. Indeed, Perego discloses that its module can include

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DDR memory devices. *See, e.g.,* EX1071 (Perego) at 8:1-4 ("In the described embodiment, memory devices 360 are discretely packaged Synchronous type DRAM integrated circuits (ICs), for example, DDR memory devices"). A Skilled Artisan would have also understood from their own knowledge, including from JEDEC standards, that DDR memory modules include SPD devices. EX1062 (JESD21-C) at p. 68 n.1 (providing in the standard for Serial Presence Detect (SPD) that "[i]n a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM $\overline{\text{CAS}}$ latency)").

358. Thus, Perego discloses to a Skilled Artisan "*an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits*."

b) Ellsberry's Disclosures

359. To the extent one might argue that Perego does not sufficiently disclose that its SPD device reports an overall latency of the module having one more clock cycle than an actual operational CAS latency of the memory devices, it would have been obvious in view of Ellsberry. As discussed above with reference to claim 3, Ellsberry is analogous art to the 215 Patent, Perego, and the JESD79-2 standard. *See supra* ¶¶193-199, 350. Ellsberry explains that, in its module:

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> "a Serial Presence Detect (SPD) feature is implemented to collect and store the memory module configuration. The memory control configuration is communicated to the host system and stored. The memory module reports the total module memory capacity and data width along with the individual emulated memory device capacity."

EX1073 (Ellsberry) at [0034]. Thus, as explained below in more detail, a Skilled Artisan would have been motivated to collect and report an "emulated" CAS latency that takes into account a clock cycle delay due to registering the data signals, as taught by Ellsberry.

360. As discussed above, Perego discloses that its module includes an SPD functionality to report "access latency values" to the memory controller during initialization. *See supra* ¶¶356-358; *see also* EX1071 (Perego) at 12:20-23 ("A serial interface 574 may be employed to couple signals utilized in initialization of module or memory device identification values … [and] access latency values…."). Thus, a Skilled Artisan would have been motivated to look at analogous art, such as Ellsberry, that further explains this SPD functionality and provides further details about it. In particular, Ellsberry explains the flowing:

> "[A] Serial Presence Detect (SPD) feature is implemented to collect and store the memory module configuration. The memory control configuration is communicated to the host system and stored. The memory module reports the total module memory capacity and data width along with the individual emulated memory device capacity."

EX1073 (Ellsberry) at [0034].

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361. A Skilled Artisan would have understood from Ellsberry's teaching that the SPD feature requires collecting and reporting the memory module configuration, including features that are "emulated." As discussed above, Perego discloses and renders obvious to a Skilled Artisan that the module's CAS latency is longer than the actual operational CAS latency of the memory devices due to the registration of the data signals in the buffer. Therefore, a Skilled Artisan would have been motivated to collect the memory module configuration, including the delay caused by the data registration, and report the additional delay as an "emulated" characteristic of the memory devices as suggested by Ellsberry.

362. Furthermore, as discussed above with reference to Claim 3, Ellsberry also teaches that the CAS latency of the memory device is set to be one clock cycle shorter in order to allow time for the data to pass through the data buffer. *See supra* at ¶¶351-352. Since Perego also has a buffer that delays the data signals, a Skilled Artisan would have been motivated to set the CAS latency of the memory devices to be one clock cycle shorter as taught by Ellsberry. *Id.* A Skilled Artisan would have also understood that, in order to allow for this subtraction, the SPD device would need to report a CAS latency that is one clock cycle more (e.g., 4 clock cycles) than an actual operational CAS latency of the memory devices (e.g., 3 clock cycles). Indeed, without increasing the reported CAS latency, the one-clock-cycle-shorter CAS latency may not be feasible for the memory devices (e.g.,

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2 clock cycles may not work). *See* EX1064 at p. 12 (CAS Latency of "2" is only "Optional," not required). Additionally, a POSITA would have alternatively been motivated to combine these teachings from Ellsberry with Perego and the Perego-JESD79-2 combination, given that by doing so the Skilled Artisan would have implemented a predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results or challenges in implementation. For example, JESD79-2 teaches that CAS and Additional latency values are integer multiples of a clock cycle, which would have motivated a Skilled Artisan to implement and report latencies, including an overall latency, as integer multiples of a clock cycle. *Supra* at ¶336.

363. Therefore, Perego in view of Ellsberry renders obvious to a Skilled Artisan "*an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits*."

5. Claim 5 is Unpatentable

364. In my opinion, Claim 5 is unpatentable because it is obvious in view of Grounds 1-4.

365. Claim 5 requires *"[t]he memory module of claim 1, wherein the memory module is a dual in-line memory module (DIMM), and wherein the*

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plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits."

366. As discussed above with reference to claim element [1.b] (*see supra* ¶¶243-248), a Skilled Artisan would have understood from Perego's disclosure that its module can be implemented in a DIMM format, e.g., in order to upgrade a DIMM system with a memory module using a new generation of memory devices, or to use older generations of memory devices with new memory controllers. For example, Perego disclosed the following:

> "Buffer device 350 provides a high degree of system flexibility. New generations of memory devices may be phased in with controller 310 or into memory system 300 by modifying buffer device 350. Backward compatibility with existing generations of memory devices (i.e., memory devices 360) may also be preserved. Similarly, new generations of controllers may be phased in which exploit features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices."

EX1071 (Perego) at 6:34-43.

> "For example, the buffer device may be a configurable width buffer device to provide upgrade flexibility and/or provide high bandwidth among a variety of possible module configurations in the system."), 5:64-6:1 ("In another alternate embodiment illustrated in FIG. 3B, memory subsystems 330a–330c are incorporated onto individual substrates that include connectors 390a–390c to support upgradeability in memory system 305."

Id. at 3:25-28; *see also* EX1069 (Synchronous DRAM Architectures paper) at FIG. 1 (illustrating a DIMM format for a memory module).

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367. Furthermore, as discussed above with reference to claim element [1.d.1] (*see supra* ¶¶261-282), Perego discloses that the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits. *E.g.*, EX1071 at 8:1-4 ("In the described embodiment, memory devices 360 are discretely packaged Synchronous type DRAM integrated circuits (ICs), for example, DDR memory devices[]") & 10:56-58 ("Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices"). Arranging DDR SDRAM devices in a DIMM as disclosed by Perego was a well-known, commonly used technology at the time, especially in view of the JEDEC standards. *See, e.g.*, EX1062 (JESD21-C) (DDR SDRAM Registered DIMM Specification); EX1064 (DDR2 SDRAM Registered DIMM Specification); EX1073 (Ellsberry) at [0046] ("In various embodiments of the invention, the control unit and bank switch combination may support SDRAM DDR1 and DDR2 specifications….") & [0052] ("FIGS. 10, 11, 12 and 13 illustrate different configurations of memory modules (e.g., DIMMs)…"); EX1078 (Halbert) at 2:8-9 ("One popular type of memory module is a Dual In-line Memory Module, or DIMM.") & 9:56-59 ("Some possible device types include dynamic random access memory (DRAM) devices, synchronous DRAM (SDRAM) devices including double-data-rate (DDR) SDRAM devices…").

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368. Accordingly, Perego discloses to a Skilled Artisan that "*the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits*."

6. Claim 6 is Unpatentable

369. In my opinion, Claim 6 is unpatentable because it is obvious in view of Grounds 1-4.

370. Claim 6 requires "*[t]he memory module of claim 1, further comprising determining a latency value, wherein the communication of the first data burst between the at least one first memory integrated circuit and the memory controller is enabled in accordance with the latency value*."

371. As an initial matter, as discussed above, Perego both discloses (and renders obvious in view of Ellsberry or Halbert) to a Skilled Artisan "*determining a latency value*" for the reasons discussed above with reference to Claims 3 and 4. *See supra* ¶¶332-363.

372. Perego also discloses to a Skilled Artisan that "*the communication of the first data burst between the at least one first memory integrated circuit and the memory controller is enabled in accordance with the latency value*."

373. For example, Perego discloses a serial interface 574 and operation circuit 572 including a ROM (both highlighted in purple below) that, during

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initialization of the module, provide identification information about the module, including "access latency values," that are used by the controller "to properly configure the memory devices upon boot of the system[]":

> "A serial interface 574 may be employed to couple signals utilized in initialization of module or memory device identification values, test function, set/reset, access latency values, vendor specific functions or calibration. Operations circuit 572 may include registers or a read-only memory (ROM) to store special information (e.g., vendor, memory device parameter or configuration information) that may be used by the controller. … An SPD device is a non-volatile memory device included on a memory module. The SPD stores information used by the remainder system to properly configure the memory devices upon boot of the system."

EX1071 at 12:20-34. As discussed above, Perego also discloses using DDR SDRAMs. *Id*. at 3:62-4:3.

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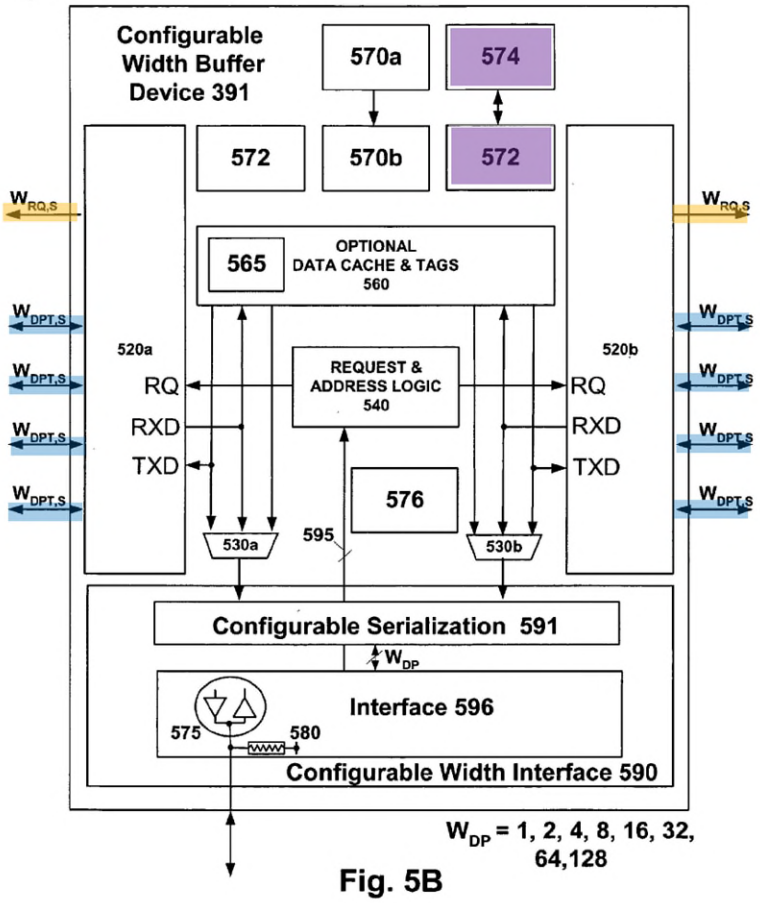

Fig. 5B

Id., FIG. 5B (annotated version reproduced above).

374. A Skilled Artisan would have understood from this disclosure based, for example, on their knowledge of the JEDEC standards (including JESD79-2), that the data transfers in Perego's memory module are scheduled according to "access latencies," including a CAS latency for DDR SDRAMs, which are programmed during initialization by the memory controller. EX1064 (JESD79-2) at p. 12 (Section 2.2.2.1) (DDR2 SDRAM Mode Register Set (MRS)).

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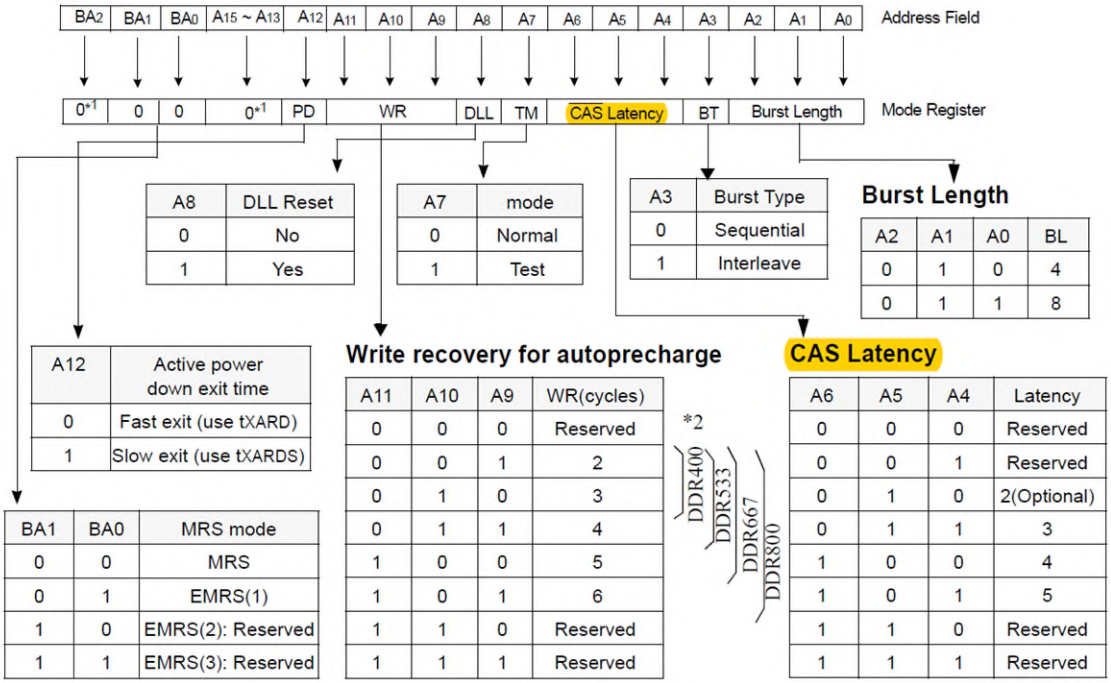

Id. at p. 12 FIG. 8 (partial annotated version reproduced above).

375. A Skilled Artisan would have also understood that such a CAS latency determines, in DDR2 SDRAM systems, the time between issuance of a read or write command and the availability of the corresponding read or write data burst. For example, the read latency (RL) is determined by the CAS latency (CL) and an additive latency (AL, which delays the read command by a set amount), and the write latency (WL) is one cycle less than the read latency (RL). *Id.* at p. 28 (FIG. 26, reproduced below).

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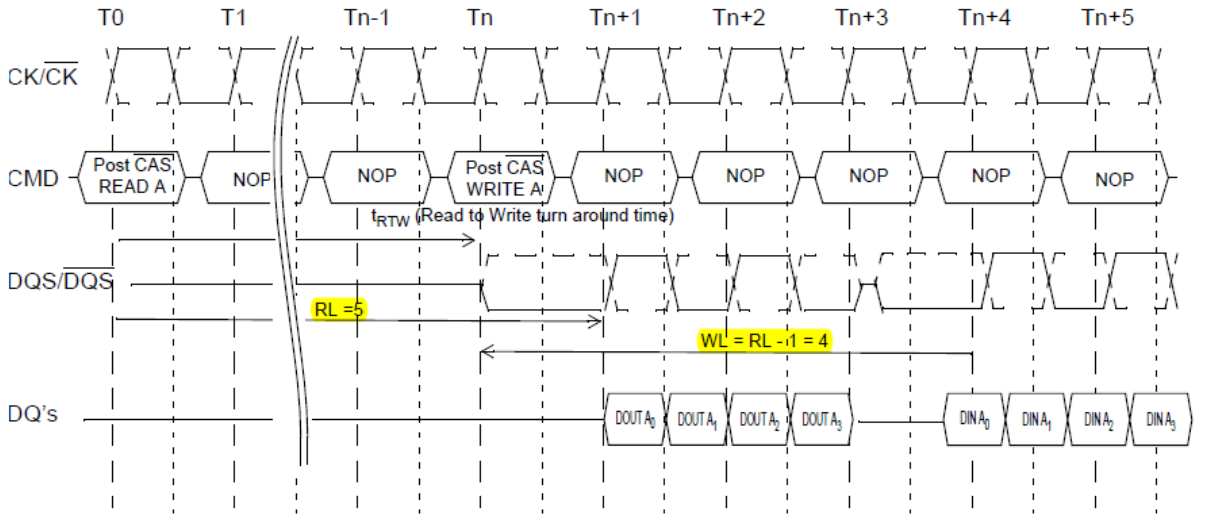

The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation.

Figure 26 — Burst Read Followed by Burst Write: RL = 5, WL = (RL-1) = 4, BL = 4

376. Further, a Skilled Artisan would have also understood that, at the time, the CAS latency was given in terms of an integer number of clock cycles for at least the most popular types of memory modules and devices. *Id.* at p. 12 (allowing CAS latency of 2, 3, 4, or 5 in a memory device). Although these disclosures would have been within a Skilled Artisan's knowledge, a POSITA would have alternatively been motivated to combine these teachings from JESD79-2 to Perego, given that by doing so the Skilled Artisan would have implemented a predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results or challenges in implementation.

377. It is my understanding that the Board has already concluded in a Final Written Decision invalidating claims in the same family as the 215 Patent that it would have been obvious to a Skilled Artisan to enable data transfers in

accordance with a CAS latency value to ensure that the data transfer works properly. *See* EX1030 at pp. 7-14 (Final Written Decision). I understand that this determination is now binding against Netlist, including in this proceeding. *See also* EX1076 at pp. 24-26 (Initial Determination finding similar limitation obvious in light of Ellsberry and Halbert).

378. Thus, a Skilled Artisan would have understood that the data transfers for read and write operations in Perego's buffer device are also enabled according to this schedule that is determined by the CAS latency because the memory controllers at the time were configured to set these scheduling latencies and expect the data transfers according to this schedule. A Skilled Artisan would have understood that, if the data transfers are not enabled according to this schedule, the memory system would not work properly because the system memory controller would follow this schedule and either the module, the memory controller, or both would miss or misinterpret data not scheduled in accordance with the CAS latency. For at least the same reasons, a Skilled Artisan would have understood that the CAS latency that matters for the communication between the memory controller and the memory module is an overall CAS latency of the memory module.

379. For example, a Skilled Artisan would have known based, for example, on the JEDEC standards, that registered DIMMs at the time registered the address and command signals that resulted in a longer CAS latency for the module

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("DIMM CAS latency") than for the memory devices alone ("Device CL"). EX1062 at p. 68 n.1 (noting in the standard for Serial Presence Detect (SPD) that "[i]n a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM $\overline{CAS}$ latency)"). Because it is Perego's buffer device (350, red) and not any of the memory devices (360, light green and blue) that interface with the system memory controller (310) directly, any delay caused by the buffer device due to registering the address, command and data signals should be reported to the memory controller to ensure compatibility, including proper scheduling of the data transfers according to the CAS latency, for example:

> "Buffer device 350 provides a high degree of system flexibility. New generations of memory devices may be phased in with controller 310 or into memory system 300 by modifying buffer device 350. Backward compatibility with existing generations of memory devices (i.e., memory devices 360) may also be preserved. Similarly, new generations of controllers may be phased in which exploit features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices."

EX1071 at 6:34-43; *see also id.* at FIG. 3B (annotated version reproduced below).

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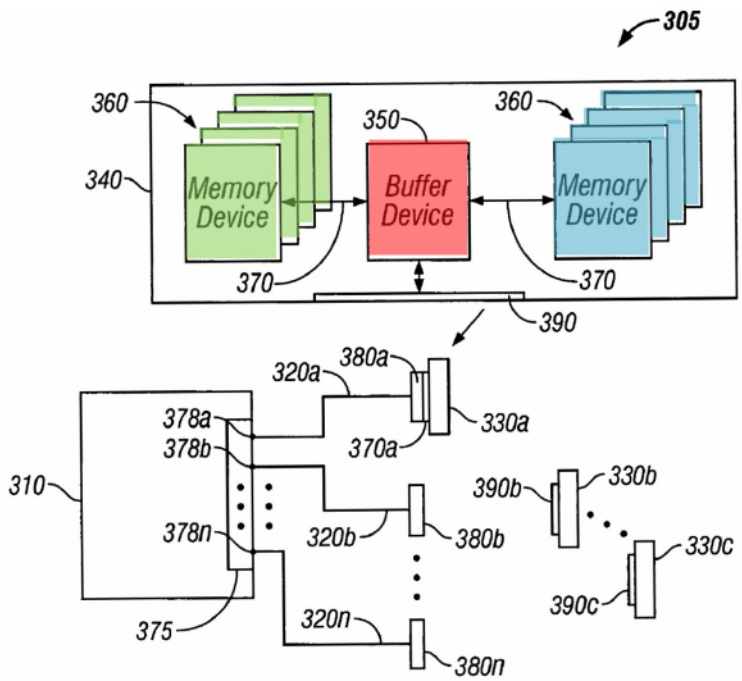

FIG. 3B

380. Thus, a Skilled Artisan would have understood that any scheduled data transfer to and from the memory module should respect the latency of the entire module, including the latency of the memory devices combined with the latency added by the buffer device, in order to perform memory operations efficiently and without errors. EX1062 at p. 68 n.1 ("In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM CAS latency)"); *see also supra* ¶¶359-362 (discussing with reference to Ellsberry (EX1073) that memory device CAS latency set to be one clock cycle shorter than in mode register command to allow time for the data to pass through the buffer).

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381. Accordingly, Perego, either by itself or in combination with Ellsberry or Halbert discloses the "*memory module of claim 1, further comprising determining a latency value, wherein the communication of the first data burst between the at least one first memory integrated circuit and the memory controller is enabled in accordance with the latency value*."

7. Claim 7 is Unpatentable

382. In my opinion, Claim 7 is unpatentable because it is obvious in view of Grounds 1-4.

a) [7.a] On-Die-Termination (ODT) Bus

383. Claim 7 requires *"[t]he memory module of claim 1, wherein the memory module is further coupled to the memory controller using an on-die-termination (ODT) bus*."

384. Perego discloses to a Skilled Artisan that the memory module is further coupled to the memory controller using an on-die-termination (ODT) bus, for example, when Perego's module is included in a DDR2 SDRAM system:

> "Configurable width buffered module 395 includes at least one memory device 360a, of memory devices 360, that receive and transmit data bit signals through channels 370 (e.g., a plurality of signal lines). In the described embodiment, memory devices 360 are discretely packaged Synchronous type DRAM integrated circuits (ICs), for example, DDR memory devices"

EX1071 (Perego) at 7:65-8:4; *see also id.* at 10:56-58 (expressly referring to DDR2 SDRAM devices).

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385. A Skilled Artisan would have understood from this disclosure that such an implementation of Perego's system includes a memory controller that is configured to work with DDR2 SDRAM devices and is coupled to an ODT bus that includes On Die Termination (ODT) signals in accordance with the corresponding JEDEC standards, including JESD79-2. *See* EX1064 at p. 6 (ODT pin on DDR2 SDRAM devices) (annotated text reproduced below in part); *see also id.* at pp. 18-22 (Section 2.2.2.4, describing detailed operation of On-Die Termination). Thus, a Skilled Artisan would have understood that On Die Termination (ODT) is a common feature of DDR2 SDRAM devices that turns on/off internal termination resistance for signals, including data (DQ) and strobe (DQS) signals in accordance with the JEDEC standards.

1.2 Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, and DM signal for x4x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.

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See also EX1066 (JESD21-C, Rev. 3.2) at p. 7 (describing JEDEC Registered DIMM design for DDR2 memories including coupling to an ODT bus including ODT[1:0] pins (text reproduced below in part)).

Registered DIMM Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0	IN	Positive Edge	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM PLL.
$\overline{CK0}$	IN	Negative Edge	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM PLL.
CKE[1:0]	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
$\overline{S}$[3:0]	IN	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. These input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When both $\overline{S}$[0:1] are high, all register outputs (except CKE, ODT and Chip select) remain in the previous state. For modules supporting 4 ranks, $\overline{S}$[2:3] operate similarly to $\overline{S}$[0:1] for a second set of register outputs.
ODT[1:0]	IN	Active High	On-Die Termination control signals
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	IN	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.

386. I also note that Perego itself describes the importance of proper signal termination, further motivating a Skilled Artisan to couple the memory module to an ODT bus of the memory bus of the system. EX1071 at 11:26-36 ("Termination 580 may dissipate signal energy reflected (i.e., a voltage reflection) from transceiver 575.") & 9:34-49 ("The plurality of signal lines may be controlled impedance transmission lines that are terminated using respective termination elements 420a and 420b.").

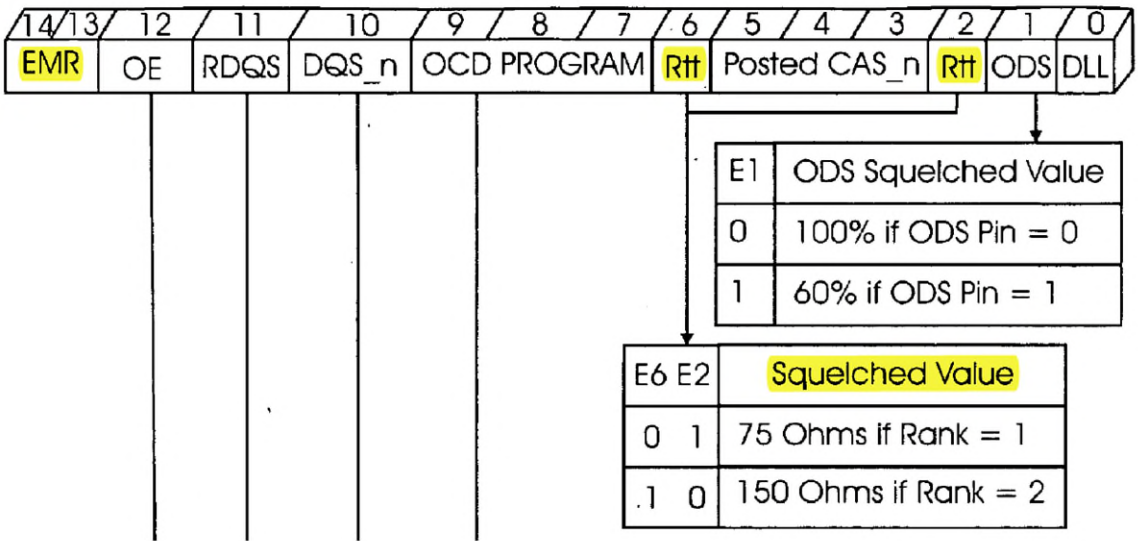
387. As another example, Ellsberry also confirms that a Skilled Artisan knew that DDR2 systems include an on-die-termination bus from the memory controller by disclosing that the extended mode register set (EMRS) command setting the termination resistance Rtt is squelched and the squelched value depends

on the number of ranks. EX1073 (Ellsberry) at Figs. 8A, 8B and 9 (annotated versions reproduced below in part).

Command	Mode	Addr	P Bank	DDR A		DDR B	
				Command	Addr	Command	Addr
MRS	X	X	X	MRS	1	MRS	1
EMRS	X	X	X	EMRS	2	EMRS	2

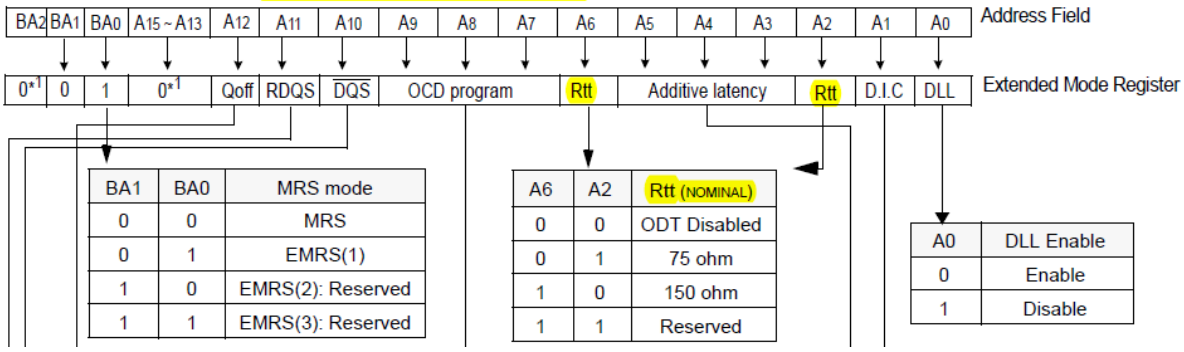
NOTES: 1. if cl_mode = subtract; cl = cl - 1 to DDRs

2. ods squelch-based on ODS setting, rtt squelch-based on REFF setting, ocd squelch-default, dqs_n enable, rdqs disable, out squelch - enable



See also EX1064 at p. 14 (showing "Rtt" is set by EMRS command), pp. 18-19 (showing "Rtt" affects ODT termination):

2.2.2.2 DDR2 SDRAM Extended Mode Register Set (cont'd)

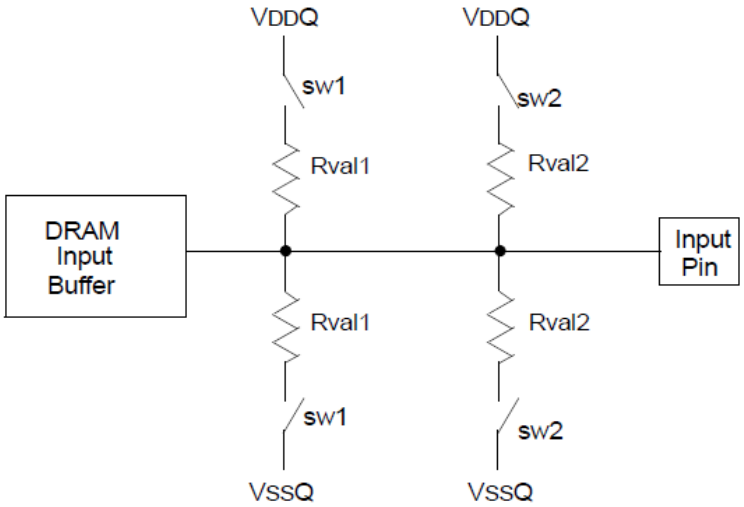


BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2): Reserved
1	1	EMRS(3): Reserved

A6	A2	Rtt (NOMINAL)
0	0	ODT Disabled
0	1	75 ohm
1	0	150 ohm
1	1	Reserved

A0	DLL Enable
0	Enable
1	Disable

2.2.2.4 ODT (On Die Termination) (cont'd)



Switch sw1 or sw2 is enabled by ODT pin.
Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.
Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

388. Accordingly, Perego, either by itself or in combination with JESD79-2 and/or Ellsberry, discloses "*the memory module is further coupled to the memory controller using an on-die-termination (ODT) bus*."

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b) [7.b] ODT Circuit

389. Claim 7 requires "*wherein each of the plurality of memory devices including an ODT circuit*."

390. Perego discloses using DDR2 SDRAM memory devices. *E.g.*, EX1071 at 10:56-59 ("Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices."). As discussed above, a Skilled Artisan would have understood that each of the DDR2 memory devices includes an ODT circuit. *Supra* at ¶385.

391. Therefore, Perego discloses to a Skilled Artisan that "*each of the plurality of memory devices includes an ODT circuit*."

c) [7.c] Termination Circuit

392. Claim 7 requires "*the memory module further comprising a termination circuit external to any of the plurality of memory devices, wherein the termination circuit is coupled to the ODT bus and to the ODT circuit of at least one of the plurality of memory devices*."

393. Perego discloses to a Skilled Artisan that (1) the memory module further comprises a termination circuit, including circuitry, logic and termination elements, such as termination 580, in the buffer device which is external to any of the plurality of memory devices (360), and (2) the termination circuit is coupled to

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the ODT bus including ODT signals from the memory controller and to the ODT circuit of at least one of the memory integrated circuits in order to set the termination state in DDR2 SDRAM memory devices. *See, e.g.*, EX1071 at FIG. 5B (annotated version reproduced below); *see also, e.g.*, EX1072 (Matsui1) at FIG. 19 (reproduced below, illustrating that a Skilled Artisan would have understood that the termination circuit for the signals from the memory chips would be in the buffer device when that is what is interfacing with the memory chips).

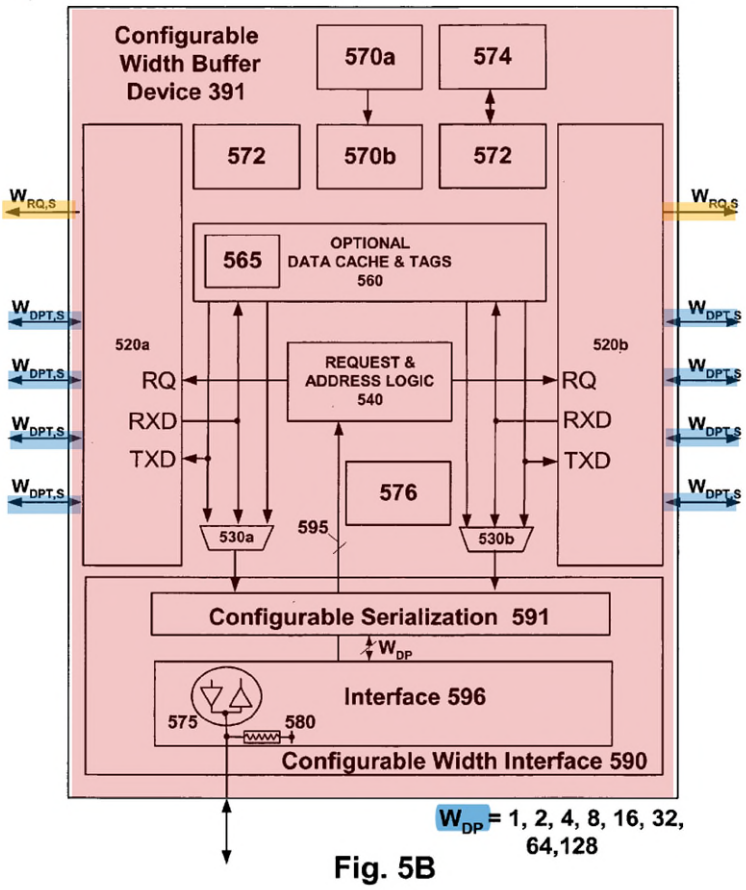

Fig. 5B

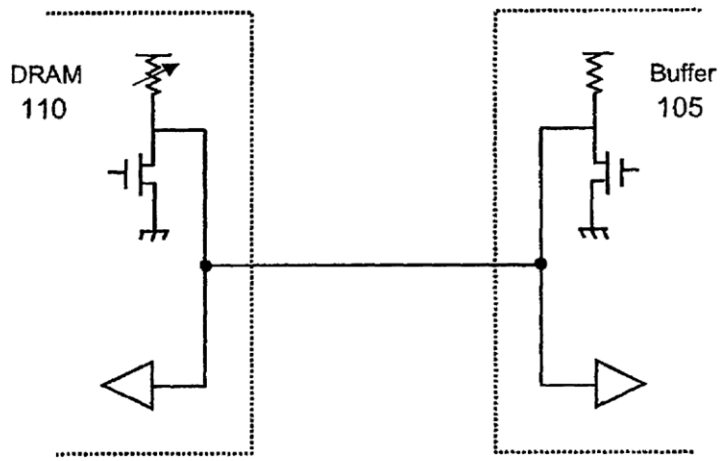

FIG. 19

394. For example, a Skilled Artisan would have understood that, in a memory system that includes DDR2 SDRAM devices, Perego's buffer device includes circuitry that is coupled to the ODT bus, including ODT signals from the memory controller. This is because a Skilled Artisan would have understood based, for example, on their knowledge of the JEDEC standards (including JESD79-2) that the DDR2 SDRAM devices have an ODT signal input which can be controlled by the memory controller in order to turn on or off the internal termination resistance of the DDR2 SDRAM devices. *See, e.g.*, EX1064 (JESD79-2) at p. 6 (identifying the ODT input and its function).

ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS, RDQS, RDQS, and DM signal for x4x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/UDQS, LDQS/LDQS, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.

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Although this understanding would have been within a Skilled Artisan's knowledge, a POSITA would have alternatively been motivated to combine these teachings from JESD79-2 to Perego, given that by doing so the Skilled Artisan would have implemented predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results or challenges in implementation.

395. For the same reasons, a Skilled Artisan would have also understood that the DDR2 SDRAM devices in Perego's module also receive an ODT signal from the buffer device to enable or disable the internal termination resistance of the DDR2 SDRAM devices. *Id.*; *see also* EX1066 (JESD21C, DDR2 RDIMM) at p. 6 (Pin Description including ODT inputs). Because the DDR2 SDRAM devices have ODT circuitry and require corresponding ODT signals for their operation, a Skilled Artisan would have understood that the termination circuit includes logic in Perego's buffer device and provides ODT signals to the DDR2 SDRAM devices for their proper operation.

396. Furthermore, a Skilled Artisan would have been motivated to use these ODT signals in order to avoid reflections that may degrade the quality of the signals. EX1071 at 9:6-12 ("The terminator may be matched to the impedance of each transmission line in point-to-point links 320a–320n, to help reduce voltage reflections. Signal lines of bussed topologies may also benefit from terminating

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end points or connection points where devices, such as buffer devices connect to those signal lines."); *see also* EX1068 (Stone) at p. viii ("The student is told about reflections on transmission lines and how terminations can remove or reduce reflections."), pp. 54-71 (Chapter 2.2, "Transmission-Line Techniques"). Indeed, as discussed above with reference to claim element [7.a] (*see supra* ¶¶383-388), Ellsberry sets the value of the termination resistance Rtt in the memory devices in accordance with the configuration on the module, and a Skilled Artisan would have understood from this disclosure that a termination circuit in the module controller is coupled to the ODT circuit of the memory devices in order to properly control the memories' ODT circuit. EX1073 (Ellsberry), e.g., at FIG. 9.

397. Accordingly, Perego, either by itself or in combination with JESD79-2, discloses to a Skilled Artisan "*the memory module further comprising a termination circuit external to any of the plurality of memory devices, wherein the termination circuit is coupled to the ODT bus and to the ODT circuit of at least one of the plurality of memory devices*."

d) [7.d] External Termination

398. Claim 7 requires "*wherein the termination circuit is configured to provide external termination of the at least one of the plurality of memory devices in response to an ODT signal on the ODT bus, and*."

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399. Perego discloses to a Skilled Artisan that the termination circuit includes termination elements in the buffer device, such as termination elements in the interfaces 520a and 520b, that are configured to provide external termination for at least one of the memory devices, such as DDR2 SDRAM devices coupled to the interfaces 520a and 520b. The termination elements are so configured in order to properly terminate at the interfaces 520a and 520b data signals transmitted by the memory devices, in response to the ODT signal on the ODT bus. *See, e.g.*, EX1071 (Perego) at FIG. 5B (annotated version reproduced below).

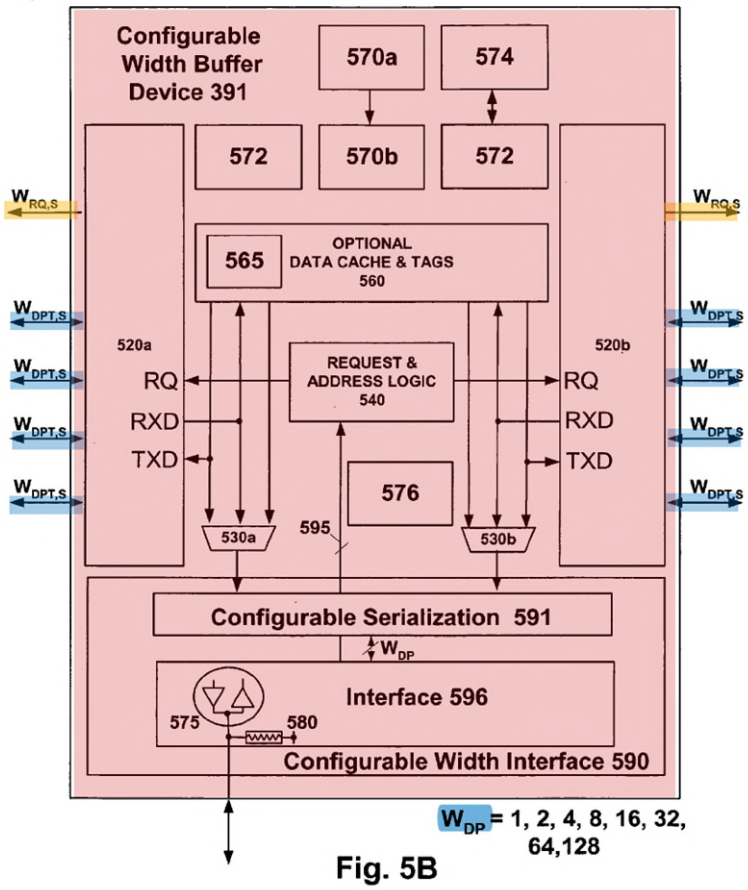

Fig. 5B

400. For example, Perego explains the following:

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> "One or more terminators (e.g., a resistive element) may terminate each signal line in point-to-point links 320a–320n. … The terminator(s) connect to a termination voltage, such as ground or a reference voltage. The terminator may be matched to the impedance of each transmission line in point-to-point links 320a–320n, to help reduce voltage reflections. Signal lines of bussed topologies may also benefit from terminating end points or connection points where devices, such as buffer devices connect to those signal lines."

EX1071 at 8:66-9:12. Perego also explains that "Buffer device 350 is coupled to the plurality of memory devices 360 via channels 370" (*id*. at 5:4-6), and that the interfaces 520a and 520b include signal lines to the memory devices with corresponding transceivers (*id*. at 16:17-21) ("In addition, the number of transceiver circuits included in interface 520a and 520b that are employed to communicate with one or more memory devices may be configured based on the desired serialization ratio."). *See also id.* at 8:51-65 (explaining the use transceivers in point-to-point links and bus arrangements).

401. A Skilled Artisan would have understood from these disclosures that Perego's interfaces 520a and 520b include transceivers to communicate with the memory chips and corresponding terminations to avoid reflections on the signal lines. A Skilled Artisan would have also understood that these terminations along the data path are controlled in response to the ODT signal in order to provide for proper termination of active signals on the corresponding channel. For example, when the ODT terminations in the DDR2 SDRAM devices are turned on or off in response to the ODT signal, the terminations in the corresponding interface 520a or

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520b are controlled accordingly, similar to other point-to-point or bussed links. EX1071 at 9:6-9 ("The terminator may be matched to the impedance of each transmission line in point-to-point links 320a-320n, to help reduce voltage reflections. Signal lines of bussed topologies may also benefit from terminating end points or connection points where devices, such as buffer devices connect to those signal lines.").

402. To the extent one might argue that Perego does not sufficiently discloses this limitation, it would have been obvious to a Skilled Artisan at the time. As discussed above (*see supra* ¶396), Perego discloses the importance of using terminations to reduce voltage reflections. *E.g.*, EX1071 at 9:6-9; *see also id*. at 11:29-31 (explaining how termination 580 reduces voltage reflections). For example, a Skilled Artisan would have been motivated to properly terminate data signals that are driven from the memory devices on a channel to one of the interfaces 520a or 520b, in order to avoid reflections. EX1068 (Stone) at pp. viii ("The student is told about reflections on transmission lines and how terminations can remove or reduce reflections. The student has to see this to appreciate the ideas fully.") & 57 ("A very interesting and important situation arises when the load impedance ZL is chosen to be equal to the wave impedance Z0 of the transmission line. In this case the reflection coefficient is 0, and there is no reflected wave at all."). Accordingly, a Skilled Artisan would have been motivated to use

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terminations in the interfaces 520a and 520b in order to reduce voltage reflections on signal lines in the channels connecting those interfaces to the memory devices.

403. A Skilled Artisan would have also understood that implementing such external termination in the interfaces 520a and 520b of Perego was well within the level of skill. For example, Matsui2 (US2003/0039151) discloses a termination circuit 213 that interfaces with memory devices and provides external termination for data signals received on data bus 22 from the memory devices. EX1082 (Matsui2) at FIG. 2 (annotated version reproduced below) & [0037] ("…a termination circuit 213 to be put into an operating state in case where the data are read from the DRAM1, the DRAM2, the DRAM3, and the DRAM4"); *see also id*. at FIGS. 5-7, and 9 (showing that the termination circuit 213 is turned on and off for performing read and write operations).

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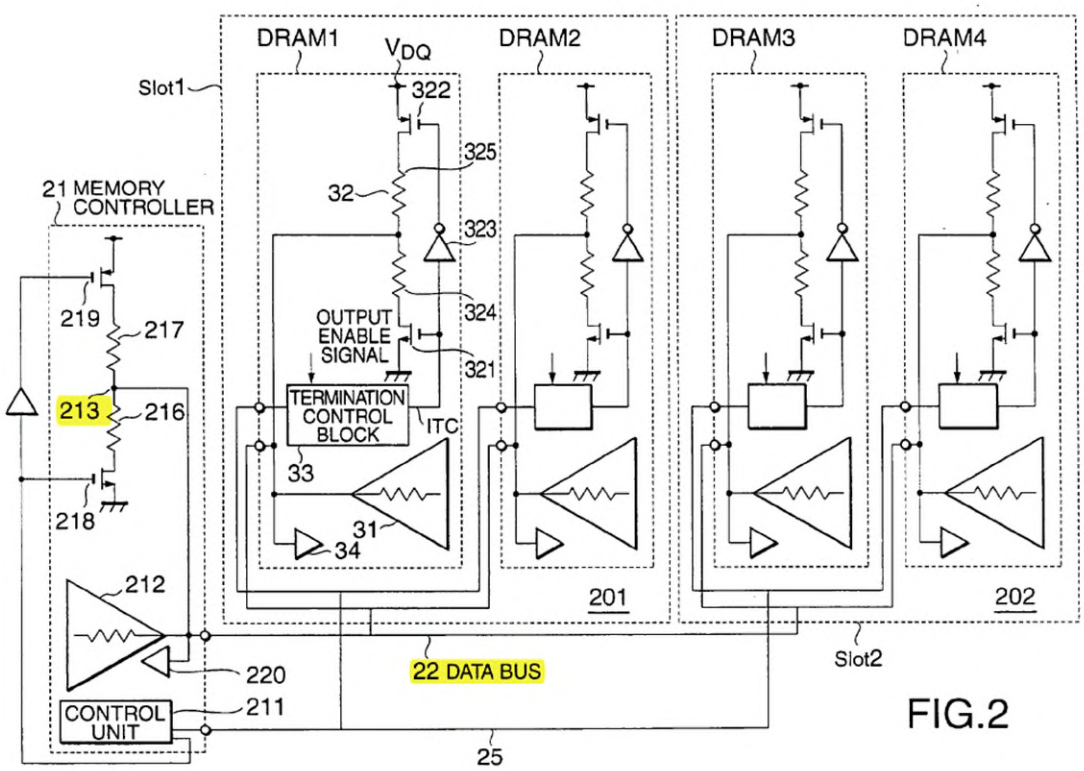

FIG.2

Although this understanding would have been within a Skilled Artisan's knowledge, a POSITA would have alternatively been motivated to combine these teachings from Matsui2 to Perego, given that by doing so the Skilled Artisan would have implemented predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results or challenges in implementation. *Supra* at ¶¶206-209.

404. Accordingly, Perego, either by itself or in combination with Matsui2, discloses "*the termination circuit is configured to provide external termination of the at least one of the plurality of memory devices in response to an ODT signal on the ODT bus*."

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e) [7.e] ODT Circuit Disabled

405. Claim 7 requires "*wherein the ODT circuit in the at least one of the plurality of memory devices is disabled*."

406. Perego discloses to a Skilled Artisan that the ODT circuit in the at least one of the plurality of memory devices is disabled.

407. As discussed above with reference to claim element [1.a.2] (*see supra* ¶¶226-227), Perego discloses using DDR2 SDRAMs. A Skilled Artisan would have also understood based, for example, on their knowledge of JEDEC standards (including JESD79-2), that, for DDR2 SDRAM devices, the "ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices." EX1064 (JESD79-2) at 18-19.

2.2.2.4 ODT (On Die Termination)

On Die Termination (ODT) is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQS/DQS, RDQS/RDQS, and DM signal for x4x8 configurations via the ODT control pin. For x16 configuration ODT is applied to each DQ, UDQS/UDQS, LDQS/LDQS, UDM, and LDM signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

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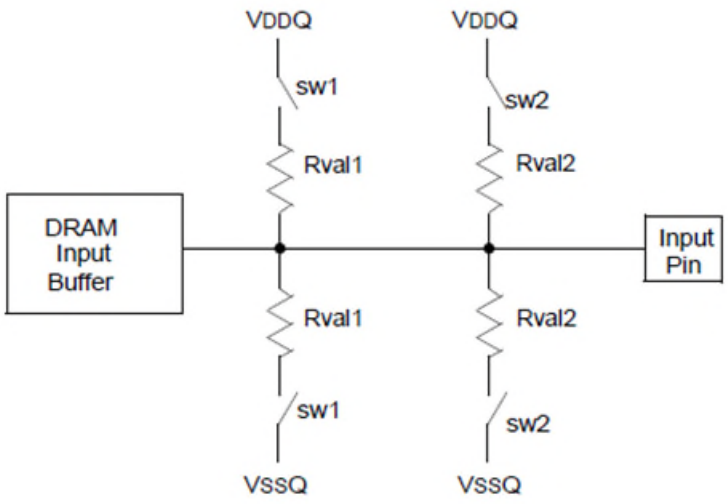

Switch sw1 or sw2 is enabled by ODT pin.
Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
Termination included on all DQs, DM, DQS, $\overline{DQS}$, RDQS, and $\overline{RDQS}$ pins.
Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

408. A Skilled Artisan would have also understood that the ODT circuit of a memory device may be turned off (disabled) when that memory device is driving the data signal line and that it is the termination element in the interface circuit 520 that is matched to the impedance of the transmission line in order to properly terminate the signal driven by the memory device:

> "The terminator may be matched to the impedance of each transmission line in point-to-point links 320a–320n, to help reduce voltage reflections. Signal lines of bussed topologies may also benefit from terminating end points or connection points where devices, such as buffer devices connect to those signal lines"

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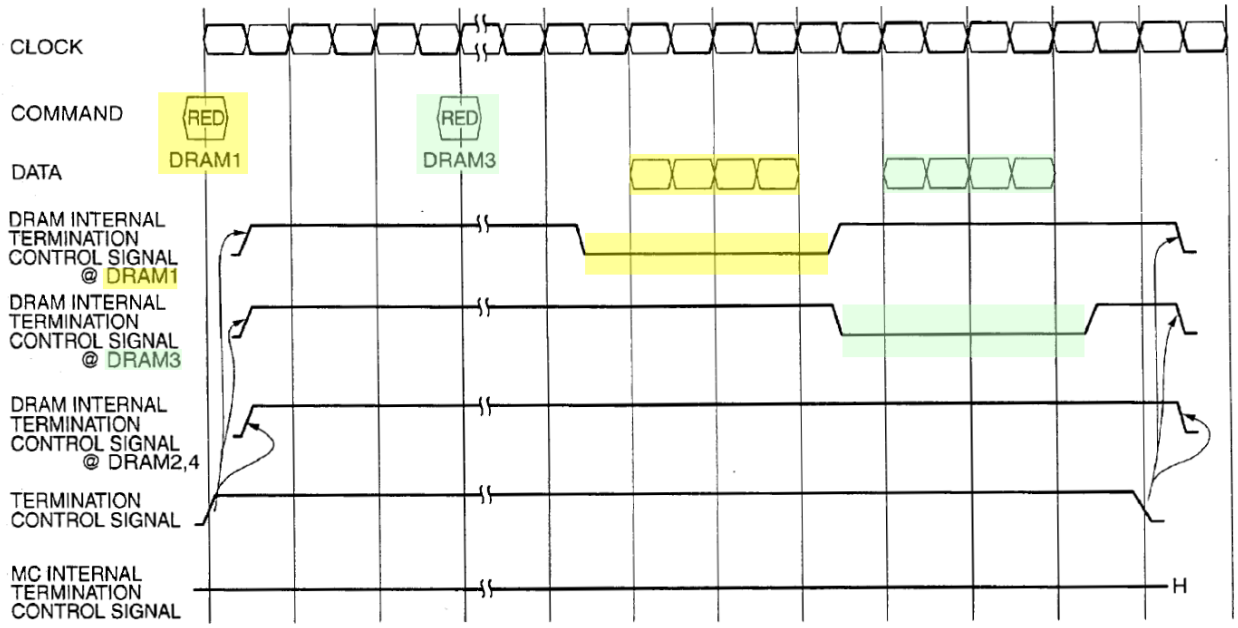
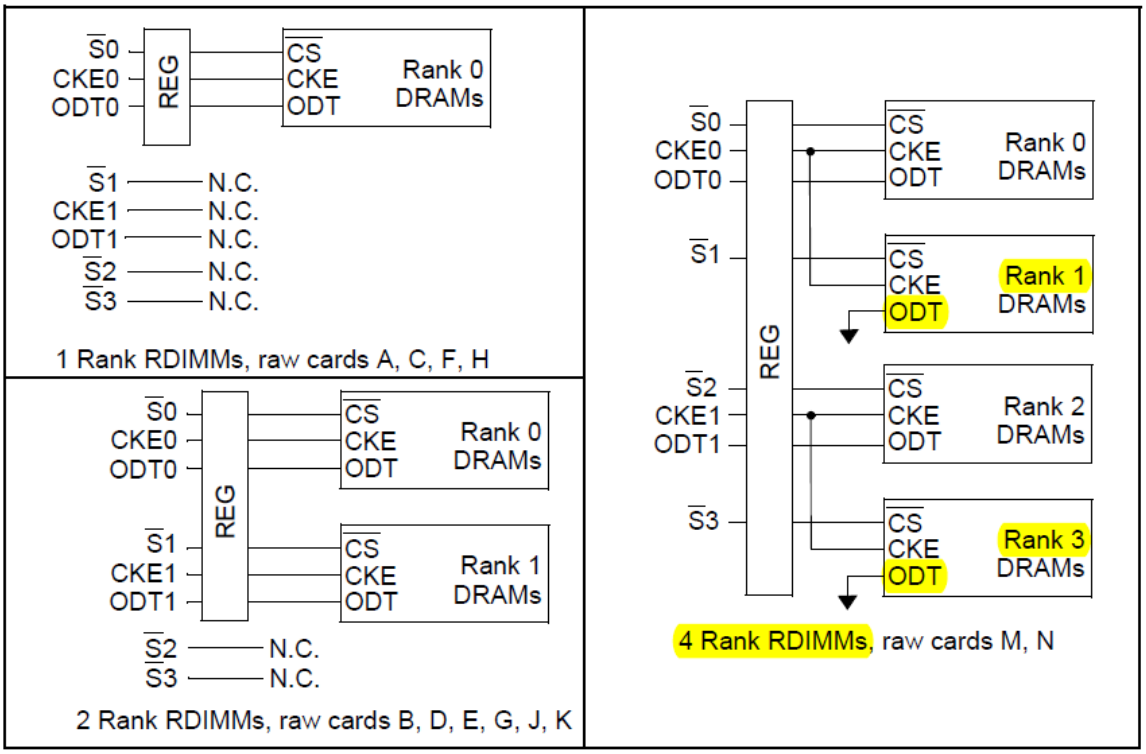
EX1071 at 9:5-12; *see also* EX1082 (Matsui2) at FIG. 5 (reproduced below, annotated, showing termination control for read operation, turning on and off the termination of DRAM devices).



TERMINATION CONTROL UPON READ OPERATION OF DRAM1/3

FIG.5

409. Furthermore, a Skilled Artisan would have understood that, in four-rank modules that are used in a system where the ODT bus has only two ODT signals, the ODT is disabled (grounded) for some of the memory devices to achieve optimal signal integrity. EX1066 (JESD21-C (Rev. 3.2)) at p. 106 (reproduced below in part).



Simulation and testing indicate that best signal integrity on the data, mask, and strobe bus is obtained when ODT is programmed for 75 Ω for ranks 0 and 2 of DDR2 SDRAMs via the mode register set command EMRS(1) and both ODT0 and ODT1 RDIMM signals are asserted during cycles requiring termination from the slot containing the 4 rank RDIMM, providing an effective 37.5 Ω termination impedance during these cycles. Since ODT for ranks 1 and 3 are disabled via the ODT pins on these ranks, programming via EMRS(1) is a don't-care for these ranks.

Although these understandings would have been within a Skilled Artisan's knowledge, a POSITA would have alternatively been motivated to combine the these teachings from JESD79-2 or Matsui2 to Perego, given that by doing so the Skilled Artisan would have implemented predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results or challenges in implementation. *Supra* at ¶¶206-209.

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410. Accordingly, Perego, either by itself or in combination with either JESD79-2 or Matsui2, discloses that "*the ODT circuit in the at least one of the plurality of memory devices is disabled*."

8. Claim 8 is Unpatentable

411. In my opinion, Claim 8 is unpatentable because it is obvious in view of Grounds 1-4.

412. Claim 8 requires "*[t]he memory module of claim 1, wherein the buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the first data burst or the second data burst through the buffer.*"

413. The 215 Patent provides little disclosure for this claim beyond the claim language itself. *See* EX1001 at 20:35-46 ("The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three."), 29:62-30:3 ("In

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certain embodiments, the PLD 42 uses sequential and combinatorial logic procedures to produce the gated CAS signals which are each transmitted to a corresponding one of the four ranks 32 a, 32 b, 32 c, 32 d. In certain other embodiments, the PLD 42 instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS0a, CS0b, CS1a, and CS1b) which are each transmitted to a corresponding one of the four ranks 32 a, 32 b, 32 c, 32 d."), Fig.11B.

414. Perego discloses to a Skilled Artisan that the buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the first data burst or the second data burst through the buffer, similar to the disclosure found in the 215 Patent.

415. For example, as discussed above with reference to claim elements [1.c] and [1.f.1]-[1.f.2] (*see supra* ¶¶249-260 & 312-324), Perego discloses that its buffer device includes logic and registers, which can be used, for example, to perform "rank multiplication," *see supra* ¶¶171-174, 319. For example, Perego's logic is configured to select the data path for memory access operations based on an address signal. EX1071, e.g., at 14:63-65 ("The address of the transaction will determine which target subset of channels 370 will be utilized for the data transfer portion of the transaction."), 15:34-40 ("configurable width buffer device 391 may employ a configurable datapath router within interface 591 to route requests

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between the primary channel and the target subset of secondary channel signal lines for each transaction. According to a preferred embodiment, the target subset of secondary channel signal lines may be selected via address bits provided as part of the primary channel request"). A Skilled Artisan would have understood that a logic for such data path routing operations based on address signals includes combinatorial logic and logic pipelines. For example, the JEDEC standards specify that a read or write operation includes a sequence of commands and corresponding addresses: First, a Bank Activate command with bank and row addresses is issued to activate the corresponding row in the corresponding bank. EX1064 at 23. Next, the Bank Activate command is followed by a Read or Write command with bank and column addresses, requesting data from or writing data to the previously activated bank and row. *Id*. at 24-25. The corresponding data transfer has pre-defined latencies. *Id*. Thus, a Skilled Artisan would have understood that Perego's "logic" to route data transactions based on the address signals is implemented by using combinatorial logic that recognizes the addresses of the Activate and Read or Write commands, and logic pipelines to handle the sequence of commands and the corresponding latencies. Ellsberry discloses the same thing. *See* EX1073, ¶[0037] & Figs. 3, 7 (similar, based on the address space of, e.g., JESD79-2, EX1064, p.7). As also discussed above with reference to Claim 3 (*see supra* ¶¶334-338), the buffer device of Perego and Ellsberry is

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configured to register (latch) the data signals, and a Skilled Artisan would have understood that such a data registering requires an additional clock cycle for transferring the data bursts through the buffer, similar to registering the address and command signals in a registered DIMM. *See also* EX1071 at 16:29-32 ("In an embodiment of the present invention as illustrated by FIG. 5B, state storage 576 is a programmable register comprising two programmable memory cells, latches, or other mechanisms for storing state information.").

416. In particular, Perego discloses using a "scheme that could potentially route any single data bit signal to any data pair line or to any of the interface 596 data connections," including multiplexers 530a and 530b and multiplexer/demultiplexer circuit 597:

> "According to an embodiment of the present invention, multiplexers 530a and 530b perform bandwidth-concentrating operations, between interface 510 and interfaces 520a and 520b, as well as route data from an appropriate source (i.e. target a subset of channels, internal data, cache or write buffer)."

EX1071 at 11:56-61.

> "The circuit of FIG. 5C is just one example out of many possible embodiments of the present invention. At the expense of increased logic and wiring complexity, an embodiment of the present invention uses a more elaborate crossbar-type scheme that could potentially route any single data bit signal to any data pair line or to any of the interface 596 data connections."

Id. at 18:48-54; *see also id.* at FIG. 5C, 17:22-18:9 ("Generally, multiplexer/demultiplexer circuit 597 contains multiplexing logic and

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demultiplexing logic. The multiplexing logic is used during read operations, and the demultiplexing logic is used during write operations.”).

417. As discussed above, ¶415, a Skilled Artisan would have understood that Perego’s routing scheme includes combinatorial logic and logic pipelines to handle the address-based routing of the command sequences that would be configured to enable data transfers, including the first and second data bursts, through the buffer:

> “In an embodiment of the present invention, any multiplexed combination of control, address information and data intended for memory devices coupled to configurable width buffer device 391 is received via configurable width interface 590, which may, for example extract the address and control information from the data. For example, control information and address information may be decoded and separated from multiplexed data and provided on lines 595 to request & address logic 540 from interface 596. The data may then be provided to configurable serialization circuit 591.”

Id. at 13:49-59; *see also id.* at FIGS. 5B & 5C. Indeed, Perego expressly explains that “one of ordinary skill in the art would appreciate that ma[n]y components used in a buffer device and memory devices are not shown, such as memory device access logic and transceivers as well as configurable width buffer device 651 logic.” *Id.* at 20:35-40.

418. In addition, JESD79-2 describes “Posted CAS” and “Additive Latency (AL)” and requires logic pipelines to enable the data transfers according to the added latency. EX1064 (JESD79-2) at 24 (shown below):

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2.2.4.1 Posted $\overline{\text{CAS}}$

Posted $\overline{\text{CAS}}$ operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a $\overline{\text{CAS}}$ read or write command to be issued immediately after the $\overline{\text{RAS}}$ bank activate command (or any time during the $\overline{\text{RAS}}$-$\overline{\text{CAS}}$-delay time, tRCD, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the $\overline{\text{CAS}}$ latency (CL). Therefore if a user chooses to issue a R/W command before the tRCDmin, then AL (greater than 0) must be written into the EMRS(1). The Write Latency (WL) is always defined as RL - 1 (read latency -1) where read latency is defined as the sum of additive latency plus $\overline{\text{CAS}}$ latency (RL=AL+CL). Read or Write operations using AL allow seamless bursts (refer to seamless operation timing diagram examples in Read burst and Write burst section).

Examples of posted $\overline{\text{CAS}}$ operation

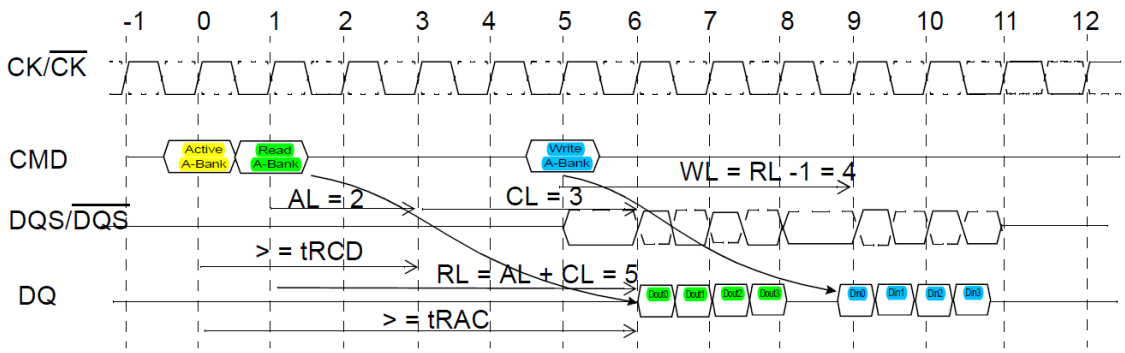

Figure 21 — Example 1: Read Followed by a Write to the Same Bank [AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4]

419. Accordingly, Perego alone or in combination with Ellsberry discloses that "*the buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the first data burst or the second data burst through the buffer*."

9. Claim 9 is Unpatentable

420. In my opinion, Claim 9 is unpatentable because it is obvious in view of Grounds 1-4.

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421. Claim 9 requires "*[t]he memory module of claim 1, wherein the first memory command includes at least one first chip select signal and the second memory command includes at least one second chip select signal.*"

422. Perego discloses to a Skilled Artisan that (1) the first memory command (read or write) includes at least one first chip select signal (in accordance with the JEDEC standards for DDR SDRAM devices) and (2) the second memory command (read or write) includes at least one second chip select signal (in accordance with the JEDEC standards for DDR SDRAM devices). *E.g.*, EX1071 (Perego) at 3:64-4:3 ("A memory device stores data (which may be retrieved) associated with a particular address provided, for example, as part of a write or read command. Examples of types of memory devices include dynamic random access memory (DRAM), static random access memory (SRAM), and double data rate SDRAM (DDR).").

423. As discussed above with reference to claim elements [1.a.2] and [1.a.3] (*see supra* ¶¶217-239), Perego discloses subsequent first and second memory commands, such as read and write commands. Perego also discloses that its system can include DDR SDRAM devices. EX1071 at 3:62-4:3, 8:1-4, 10:56-58. A Skilled Artisan would have understood from these disclosures, based, on for example, their knowledge of JEDEC standards (including JESD79-2) that, for DDR SDRAM devices, the read and write command information is carried not just

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on row address strobe (RAS) and column address strobe (CAS) lines, but also on chip select lines that carry a corresponding chip select signal that is considered part of the command signals for DDR SDRAMs. *See* EX1064 (JESD79-2) at pp. 6, 49 (annotated below):

1.2 Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, and $\overline{DM}$ signal for x4x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.

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Table 10 — Command truth table.

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1,2
Refresh (REF)	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1,7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.

NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

NOTE 3 Burst reads or writes at BL=4 cannot be terminated or interrupted. See sections "Reads interrupted by a Read" and "Writes interrupted by a Write" in section 2.2.4 for details.

NOTE 4 The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined in section 2.2.7.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See section 2.2.2.4.

NOTE 6 "X" means "H or L (but a defined logic level)".

NOTE 7 Self refresh exit is asynchronous.

424. A Skilled Artisan would have understood at the time that memory modules including DDR SDRAM devices are also controlled by command signals, including a set of input chip select signals corresponding to respective ranks (*e.g.*,

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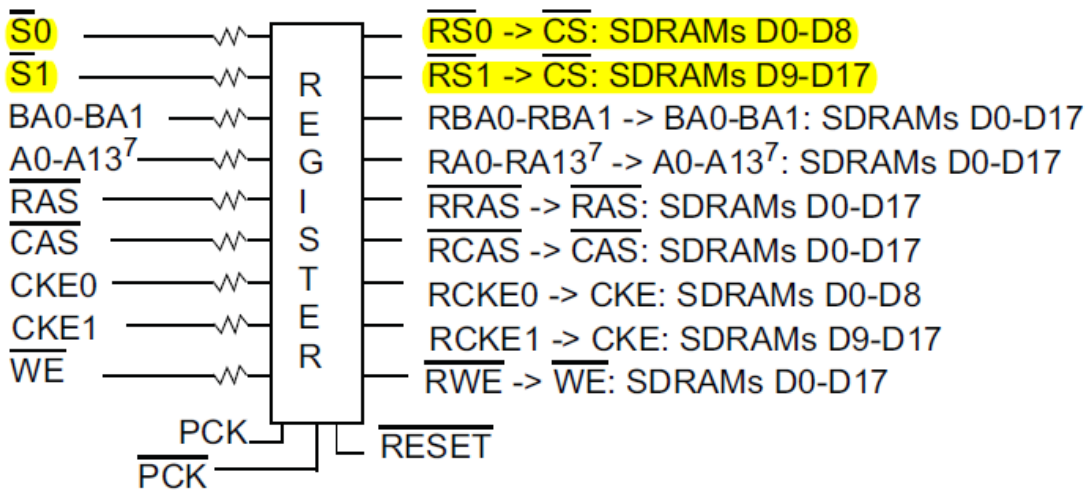
S0 and S1 for a two-rank module). *See, e.g.*, EX1062 at p. 12 (reproduced below in part); *see also, e.g.*, EX1069 at pp. 2-3 ("The chip-select bus contains a separate wire for every rank of DRAM in the system.").



This disclosure shows the register on the module (1) registering address signals (e.g., A0-A13) and control signals, including S0-S1 chip select signals and (2) providing the registered address signals (e.g., RA0-RA13) and registered control signals, including respective RS0-RS1 registered chip select signals. One of the registered address signals and registered control signals are provided to each rank of the SDRAM memory devices: RS0 to SDRAM memory devices D0-D8 (forming the first rank) and RS1 to SDRAM memory devices D9-D17 (forming the second rank). *See also* Ellsberry at Fig. 8B (Note 3 explaining that a command includes "CS" chip select signal) and Figs. 10-13 (showing Control ASIC registering address/control (AC) and chip select (CS) signals).

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425. Although these understandings would have been within a Skilled Artisan's knowledge, a POSITA would have alternatively been motivated to combine these teachings from JESD79-2 to Perego, given that by doing so the Skilled Artisan would have implemented predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results or challenges in implementation. *Supra* at ¶¶182-192.

426. Accordingly, Perego, either by itself or in combination with JESD79-2, discloses to a Skilled Artisan that "*the first memory command includes at least one first chip select signal and the second memory command includes at least one second chip select signal*."

10. Claim 10 is Unpatentable

427. In my opinion, Claim 10 is unpatentable because it is obvious in view of Grounds 1-4.

428. Claim 10 requires "*[t]he memory module of claim 9, wherein the memory module produces at least third and fourth chip select signals in response to the first memory command, the third chip select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the fourth chip-select signal being provided to the at least one second memory integrated circuit and having a non-*

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active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command."

429. Claim 10 is obvious in light of the "rank multiplication" feature disclosed by Perego and Ellsberry. *See supra* ¶¶171-174, 319.

430. For example, Perego discloses to a Skilled Artisan that its memory module includes a buffer device that produces, in response to the first memory command (write or read), at least a third chip select signal to control the first rank and a fourth chip select signal to control the second rank, the third chip select signal being provided to the at least one first memory integrated circuit in the first rank and having an active value to cause the at least one first memory integrated circuit to receive (in case of write command) or output (in case of a read command) data signals in response to the first memory command, the fourth chip-select signal being provided to the at least one second memory integrated circuit in the second rank and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.

431. For example, as discussed above with reference to claim elements [1.a.3.], [1.d.2]-[1.d.3], and [1.f.1]-[1.f.2] (*see supra* ¶¶229-239, 283-303, 312-324), Perego discloses to a Skilled Artisan that Perego's buffer device selects the target rank for a data burst in response to a read or write command. *See, e.g.,*

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EX1071 (Perego) at FIG. 3C (annotated version reproduced below) & 6:15-25 ("Buffer device 350 … receives the data via one or more of channels 370"); *see also id.* at 21:16-20 ("Any number of channels … may transfer information simultaneously and the memory devices on the other … channels …. remain in a ready or standby state until called upon to perform memory access operations.").

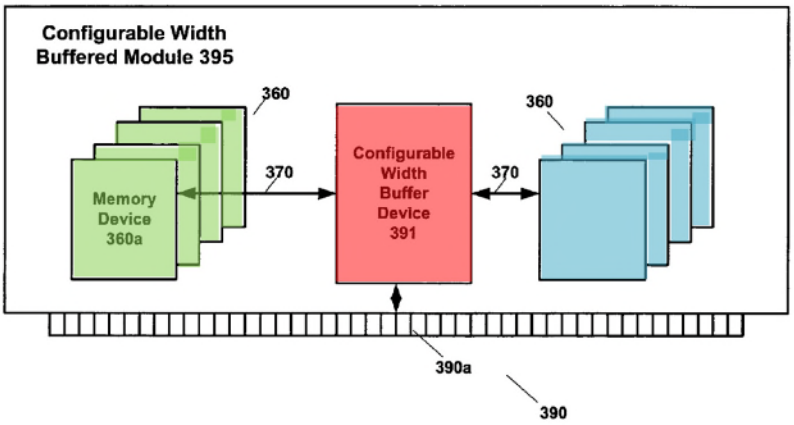

Fig. 3C

432. Perego also discloses that the target rank is selected based on an address signal, which was known at the time as "memory density multiplication" or "rank multiplication." *Id.* at 14:63-65 ("The address of the transaction will determine which target subset of channels 370 will be utilized for the data transfer portion of the transaction.") & 15:37-40 ("According to a preferred embodiment, the target subset of secondary channel signal lines may be selected via address bits provided as part of the primary channel request."); EX1001 (215 Patent) at 20:48-52 ("Memory Density Multiplication" where "an additional address bit is used to

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access the additional memory"); *supra* at ¶¶171-174. Another example of rank multiplication is disclosed by Ellsberry. EX1073 (Ellsberry) at Abstract ("By selectively routing data to and from the memory devices, a plurality of memory devices may appear as a single memory device").

433. A Skilled Artisan would have understood that, when Perego's buffer device selectively activates the ranks, e.g., based on the received address, it produces and provides a respective chip-select signal for each rank in accordance with the JEDEC standards for DDR SDRAM devices. In particular, a Skilled Artisan would have understood that, in a commonly-used JEDEC style bus, each rank has its own chip select signal which is asserted to select the corresponding rank. EX1069 (Jacob paper) at 9. Thus, a Skilled Artisan would have understood from Perego's disclosure of using the address signal to select which channel would be used for the read or write transaction that it is implementing rank multiplication, because the target channel, thus the corresponding rank, is not selected based solely on the chip select signal from the memory controller. EX1071 (Perego) at 14:63-65 ("The address of the transaction will determine which target subset of channels 370 will be utilized for the data transfer portion of the transaction.") & 15:37-40 ("According to a preferred embodiment, the target subset of secondary channel signal lines may be selected via address bits provided as part of the primary channel request."). The one or more memory devices coupled to the

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selected channel, however, would receive the standard read or write commands the standard way, including the chip select signal which is part of the command code for DDR SDRAM devices.

434. For example, Perego expressly discloses that its "buffer device may be a configurable width buffer device to provide upgrade flexibility and/or provide high bandwidth among a variety of possible module configurations in the system." EX1071 at 3:23-28. "New generations of memory devices may be phased in with controller 310 or into memory system 300 by modifying buffer device 350." *Id*. at 6:34-37. A Skilled Artisan would have understood from this disclosure that Perego's modules can be used to upgrade memory systems of the time, including JEDEC-compliant memory systems. A Skilled Artisan would have also understood that, in such systems, the memory controller uses chip select signals to select a rank on a module as the target of a memory operation:

> "This last bus, the chip-select bus, is essential in a JEDEC-style memory system, as it enables the intended recipient of a memory request. A value is asserted on the chip-select bus at the time of a request (e.g., read or write). The chip-select bus contains a separate wire for every rank of DRAM in the system. The chip-select signal thus passes over a wire unique to each small set of DRAMs and enables or disables the DRAMs in that rank so that they, respectively, either handle the request currently on the bus or ignore the request currently on the bus. Thus, only the DRAMs to which the request is directed handle the request."

EX1069 (Synchronous DRAM Architectures paper) at pp. 2-3. As discussed above, Perego also discloses that each channel 370 (or pairs of channels 415) on

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the module can be connected to a respective rank of memory devices, including DDR SDRAM devices that also use chip select signals.

435. Thus, Perego discloses to a Skilled Artisan using ranks of DDR SDRAM devices and providing control signals to those ranks of DDR SDRAM devices, including chip select signals to activate one of the ranks, which is the target of the memory request. A Skilled Artisan would have also understood, as illustrated in the JEDEC standards (including JESD79-2), that a chip select signal for a DDR SDRAM device has either an active (Low or "L") or non-active (High or "H") value (device deselect). EX1064 (JESD79-2) at p. 49, Table 10 (annotated partial version reproduced below):

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Table 10 — Command truth table.

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1,2
Refresh (REF)	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1,7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					

436. A Skilled Artisan would have also understood that the memory controller cannot issue a read command to more than one rank at the same time because, in that case, each rank would try to transmit the read data at the same time on the data bus shared by multiple ranks, which would lead to bus conflicts with devastating effects. *E.g.*, *id.* at p. 27 (showing that the DDR SDRAM devices output the read data after a pre-determined RL read latency); *see also* EX1068 (Stone) at pp. 89-90 (explaining the disastrous effects of bus conflicts).

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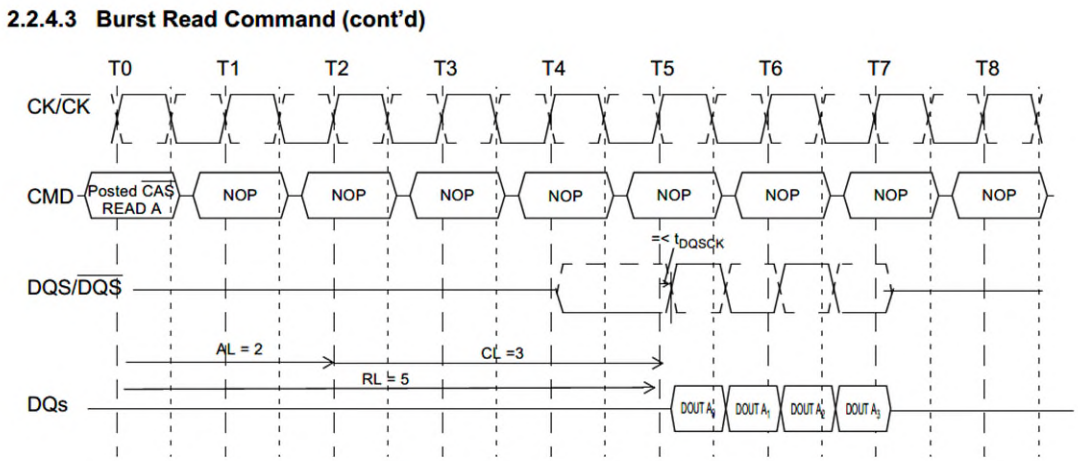

Figure 24 — Burst Read Operation: RL = 5 (AL = 2, CL = 3, BL = 4)

Id. at p. 27, Figure 24 (reproduced above); *see also* EX1062 at p.13 (showing two ranks communicating on the same data lines).

437. A Skilled Artisan would have also understood that it would have been unusual to try to write the same data to multiple ranks at the same time. Thus, a Skilled Artisan would have understood that, in a JEDEC-style DDR SDRAM system, only one rank reads or writes data in normal operations. Accordingly, only one of the chip select signals is active for each read or write operation. *See, e.g.*, EX1069 (Synchronous DRAM Architectures paper) at pp. 3 ("Even though all DRAMs in the system are connected to the same address and control busses and could, in theory, all respond to the same request at the same time, the chip-select bus prevents this from happening.") & 4 ("The rank number ends up causing a chip-select signal to be sent out over a single one of the separate chip-select lines.").

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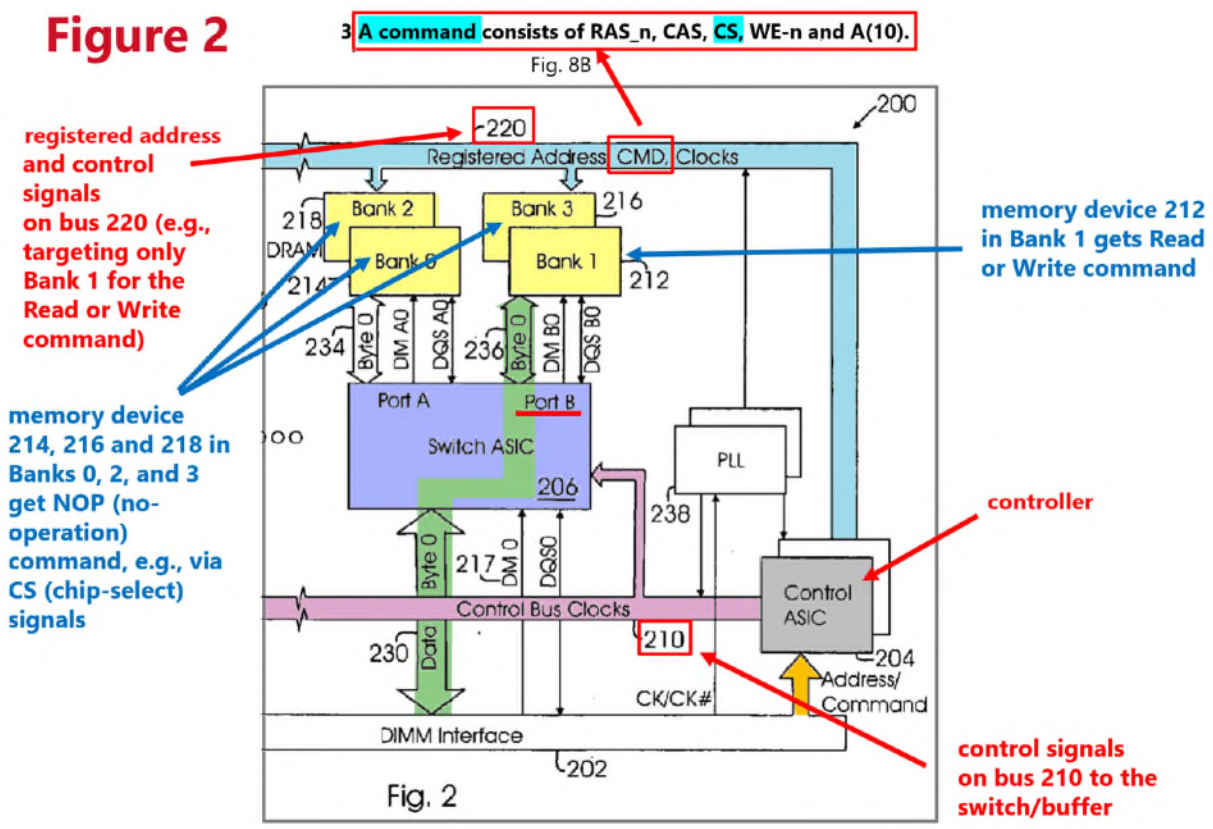
438. Ellsberry also confirms that regular read and write commands from the memory controller are sent only to the target rank while the other ranks receive a no-operation (NOP) command which can be implemented by not asserting the chip select signals, as shown below:



EX1073 (Ellsberry) at [0010] ("A state machine is used to send Read/Write commands to the intended memory bank while sending no-operation commands to the other memory bank."), and FIGS. 2, 8A & 8B (sending read and write commands from the memory controller only to the target rank while sending no-operation (NOP) command to the other ranks and explaining in Note 3 that chip select, CS, is part of the command); EX1060 at 13, n.9 ("DESELECT and NOP are

functionally interchangeable"); EX1064 at 48 (similar); EX1074 at 31-37 (Final Written Decision finding that Ellsberry discloses sending NOP commands to the non-targeted ranks).

439. Furthermore, Ellsberry discloses implementations where only the targeted ranks receives or outputs the data signals. EX1073, e.g., at Fig. 10 (reproduced below, annotated), and Claim 1 ("a memory bank switch communicatively coupled to the control unit, the memory bank switch to receive data information and direct the data information to one of a plurality of physical memory banks in real-time according to control signals from the control unit.").

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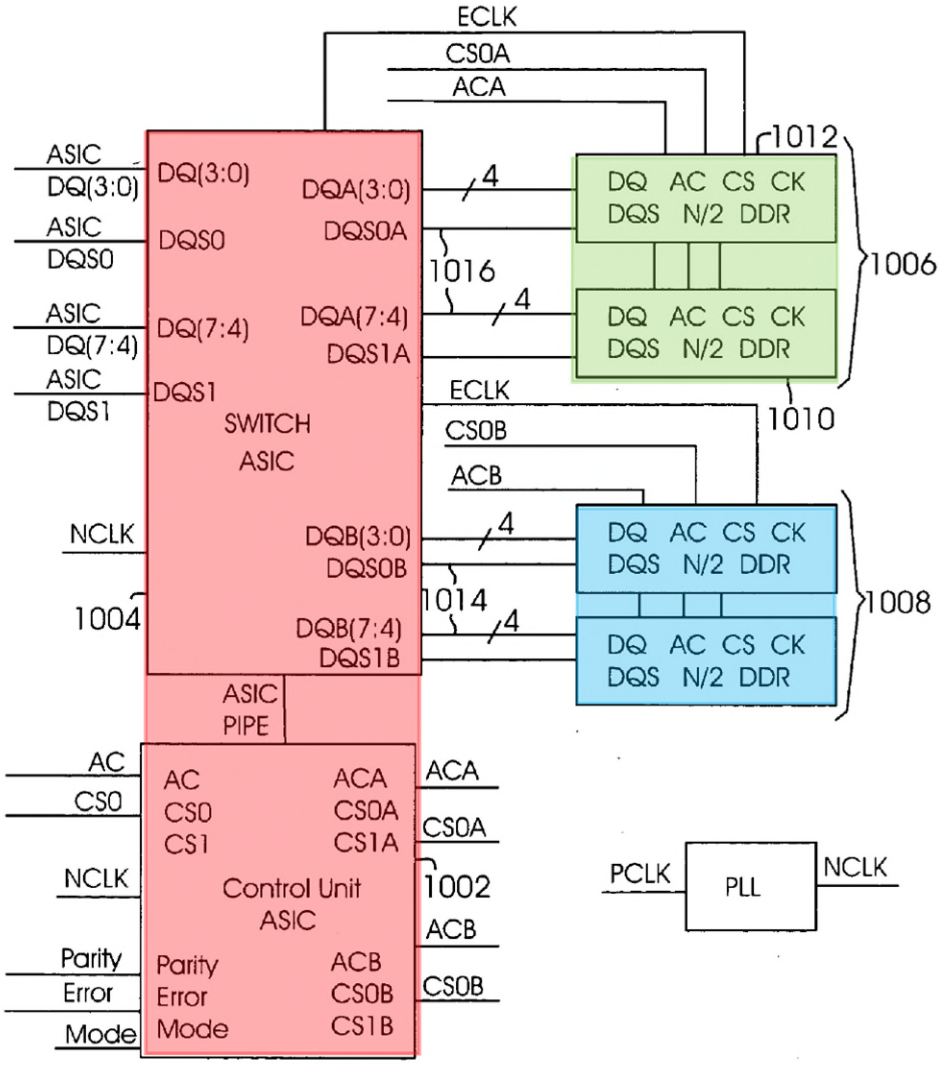

Fig. 10

440. Accordingly, a Skilled Artisan would have understood from Perego's disclosure in view of the JEDEC standards that Perego's buffer circuit produces the "*third*" and "*fourth*" chip-select signals, in response to the "*first memory command*," which are provided to the "*first*" and "*second*" memory ranks, respectively, to select the "*first*" rank with an active "*third*" chip select signal for receiving or outputting the first data burst, and to not select the "*second*" rank for

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the first memory access by an inactive "*fourth*" chip select signal. A Skilled Artisan would have understood that this operation is similar to that of the well-known registered DIMMs of the time. *See, e.g.*, EX1062 at p. 13 (showing two ranks, each having a respective chip select signal S0 and S1, which are registered as RS0 and RS1, and connected to the chip select "CS" input of the memory devices).

441. Although these understandings would have been within a Skilled Artisan's knowledge, a POSITA would have alternatively been motivated to combine the above teachings from JESD79-2 and/or Ellsberry to Perego, given that by doing so the Skilled Artisan would have implemented predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results or challenges in implementation. *Supra* at ¶¶182-192.

442. Therefore, Perego, either by itself or in combination with JESD79-2 or Ellsberry, discloses that "*the memory module produces at least third and fourth chip select signals in response to the first memory command, the third chip select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the fourth chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated*

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circuit from receiving or outputting data signals in response to the first memory command."

11. Claim 11 is Unpatentable

443. In my opinion, Claim 11 is unpatentable because it is obvious in view of Grounds 1-4.

444. Claim 11 requires "*[t]he memory module of claim 10, wherein the memory module produces at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first [sic: second] memory command, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an active value to cause the at least one second memory integrated circuit to receive or output data signals in response to the second memory command*."

445. A Skilled Artisan would have realized that claim 11, as written, is not operational, given that it says "*first [sic] memory command*" rather than "*second memory command*." In particular, claim 11 as written requires that the "*fifth chip select signal*" is produced in response to the "***second** memory command*," but the same signal is supposed to keep the first memory integrated circuit "*from receiving*

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or outputting data signals in response to the ***first*** *[sic] memory command*." Claim 11 depends from claim 1, which requires that the first memory integrated circuit in the first rank is selected to receive or output the first data burst in response to the first memory command, and that communication of the first data burst is enabled between the first memory integrated circuit and the memory controller. Thus, claim 11, as written, requires the signal produced in response to the subsequent *second* memory command to prevent the very operation that is required by claim 1 in response to the *first* memory command. In light of this contradiction, I have evaluated claim 11 as if it were written to refer to the "*second memory command*" (rather than the "*first [sic] memory command*"), making its subject matter similar to claim 10, with claims 10 and 11 being directed to the first and second memory command, respectively, consistent with claim 1.

446. As shown in the table below, claim 11 is very similar to claim 10:

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Claim 10	**Claim 11**
[10] The memory module of claim 9, wherein the memory module produces at least third and fourth chip select signals in response to the first memory command, the third chip select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the fourth chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.	[11] The memory module of claim 10, wherein the memory module produces at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first [sic: second] memory command, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an active value to cause the at least one second memory integrated circuit to receive or output data signals in response to the second memory command.

447. As discussed above with reference to Claim 10, the prior art references in Grounds 1-4 satisfy "*wherein the memory module produces at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first [sic: second] memory command, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an active value to cause*

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the at least one second memory integrated circuit to receive or output data signals in response to the second memory command." *See supra* ¶¶427-442.

448. For the reasons discussed above with reference to claim 10 (*see supra* ¶¶427-442), Perego, either by itself or in combination with JESD79-2 and/or Ellsberry, discloses to a Skilled Artisan that its memory module includes a buffer device that produces, in response to the second memory command, at least a fifth chip select signal to control the first rank and a sixth chip select signal to control the second rank, the fifth chip select signal being provided to the at least one first memory integrated circuit in the first rank and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first memory command, the sixth chip select signal being provided to the at least one second memory integrated circuit in the second rank and having an active value to cause the at least one second memory integrated circuit to receive or output data signals in response to the second memory command.

449. In particular, the "*second memory command*" is directed to access the second rank, so Perego's buffer device produces an active "*sixth*" chip select signal provided to the second rank which receives or outputs the second data burst, and a non-active "*fifth*" chip select signal to the first rank that does not participate in the data transaction of the second memory command.

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450. Therefore, Perego, either by itself or in combination with JESD79-2 and/or Ellsberry, discloses to a Skilled Artisan that "*the memory module produces at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first [sic: second] memory command, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an active value to cause the at least one second memory integrated circuit to receive or output data signals in response to the second memory command.*"

12. Claim 12 is Unpatentable

451. In my opinion, Claim 12 is unpatentable because it is obvious in view of Grounds 1-4.

a) [12.a] First Memory Command

452. Claim 12 requires "*[t]he memory module of claim 1, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and....*"

453. Perego discloses to a Skilled Artisan that the first memory command is a first read command (READ A, yellow) and the second memory command is a

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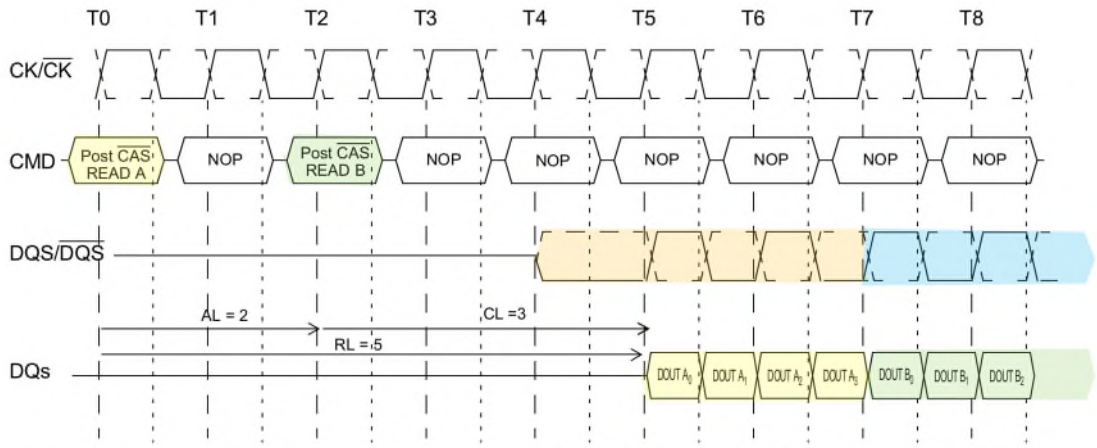
second read command (READ B, green), wherein the first read command and the second read command are back-to-back adjacent read commands. For example, Perego discloses using DDR SDRAM memory devices, which a Skilled Artisan would have understood respond to back-to-back adjacent read commands in accordance with the JEDEC standards (including JESD79-2). *See, e.g.*, EX1064 (JESD79-2) at pp. 24 ("Read or Write operations using AL allow seamless bursts.") & 28 (Fig. 27, an annotated version of which is reproduced below, showing a seamless burst read operation including READ commands at every other clock for a burst length of 4).



The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 27 — Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

In such a "seamless burst read operation" the data bursts follow each other without break, and back-to-back read commands can be issued at every other clock cycle for a burst length of 4 (since a burst of 4 data bits takes two clock cycles at double data rate) and every 4 clock cycles for a burst length of 8 (since a burst of 8 data

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bits takes 4 clock cycles at double data rate). *Id*. (Fig. 27 caption). That is, the back-to-back read commands are "adjacent" because the data burst corresponding to the second read command is output immediately after the first one without the preamble in the strobe signals. The JEDEC standards allow such back-to-back adjacent read commands on a module "regardless of same or different banks as long as the banks are activated." *Id*. (Fig. 27 caption).

454. As discussed above, e.g., with reference to Claims 5 and 10 (*see supra* ¶¶364-368, 427-442), Perego discloses a memory system that uses DDR SDRAM devices. *E.g.*, EX1071 (Perego) at 10:56-59 ("Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices."). A Skilled Artisan would have understood from this disclosure that Perego's module can operate in a JEDEC-style memory system that uses DDR SDRAM memories and follows the corresponding JEDEC standards. *Id.*; *see also* EX1069 (Jacob Paper) at pp. 9-11 (describing salient features of JEDEC's SDRAM technology, including Fig. 16 at p. 9, reproduced below).

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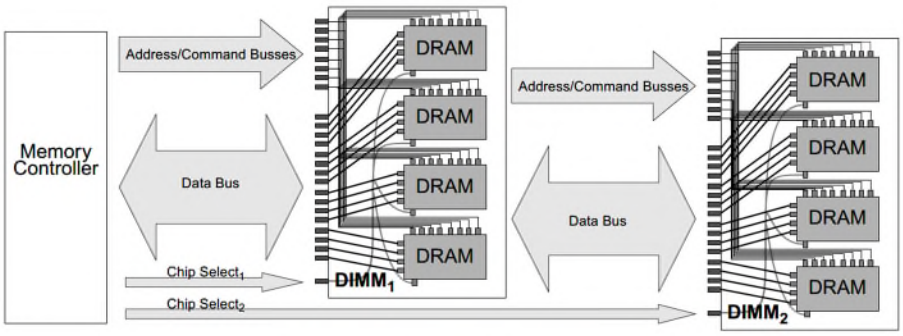

Figure 16: JEDEC-Style Memory Bus Organization
The figure shows a system of a memory controller and two memory modules with a 16-bit data bus and an 8-bit address and command bus.

455. As further discussed above, e.g., with reference to claim element [1.a.3] (*see supra* ¶¶229-239), Perego discloses to a Skilled Artisan that the first memory command is a first read command and the second memory command is a subsequent second read command. Therefore, a Skilled Artisan would have understood from the disclosure of Perego that, in a JEDEC-style memory system, the memory controller would issue commands in accordance with the JEDEC standards, including back-to-back adjacent read commands, and would have expected the module to respond with a seamless burst read operation also according to the JEDEC standards. *See, e.g.,* EX1064 (JESD79-2) at p. 28 (Fig. 27, reproduced above, showing a seamless burst read operation in response to back-to-back adjacent read commands). Because Perego discloses to a Skilled Artisan that its module can operate in such a JEDEC system, Perego also discloses to a Skilled Artisan that its module would respond to back-to-back adjacent read commands according to the JEDEC standards.

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456. Although the above-described information from the JEDEC standards (including JESD79-2) would have been within a Skilled Artisan's knowledge when reading Perego, a POSITA would have alternatively been motivated to combine these teachings from JESD79-2 to Perego, given that by doing so the Skilled Artisan would have implemented predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results or challenges in implementation. *Supra* at ¶¶182-192. For example, as discussed below in details with reference to claim element [12.c], ¶¶464-472, a Skilled Artisan would have understood that, in the case of back-to-back read commands directed to the same virtual memory device — implemented with two separate physical memory devices in two different ranks when Perego's module is implemented with rank multiplication (e.g., the first memory device corresponding to a first bank of the virtual memory device and the second memory device corresponding to a second bank of the same virtual memory device), *supra* at ¶¶171-174, 277, 319, 432 — the read data is driven to the memory controller either from one rank on one bus or from the other rank on a separate bus, but not from both, to avoid bus conflicts as disclosed, e.g., by Ellsberry. *See, e.g.,* EX1073 (Ellsberry) at FIG. 4 (reproduced below) & [0045], [0033] ("… the data from the selected target memory device is multiplexed onto the DIMM interface 202. That is, only the data read from the selected target memory device is sent to the DIMM

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interface 202."); EX1068 (Stone) at pp. 89-90 (explaining the dangers of bus conflicts).

457. Accordingly, Perego, either by itself or in combination with JESD79-2 or Ellsberry discloses that "*the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands*."

b) [12.b] First Burst of Data Strobe Signals

458. Claim 12 requires "*wherein the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory bus, and....*"

459. Perego discloses to a Skilled Artisan that its memory module is a JEDEC-style memory system using DDR SDRAM devices that outputs the first data burst (DOUT A_0-A_3, yellow) together with a first burst of data strobe signals (DQS T4-T7, orange) in response to the first read command (READ A, yellow) according to the JEDEC standards. Perego also discloses that the memory module outputs the second data burst (DOUT B_0, B_1, B_2, …, green) together with a second

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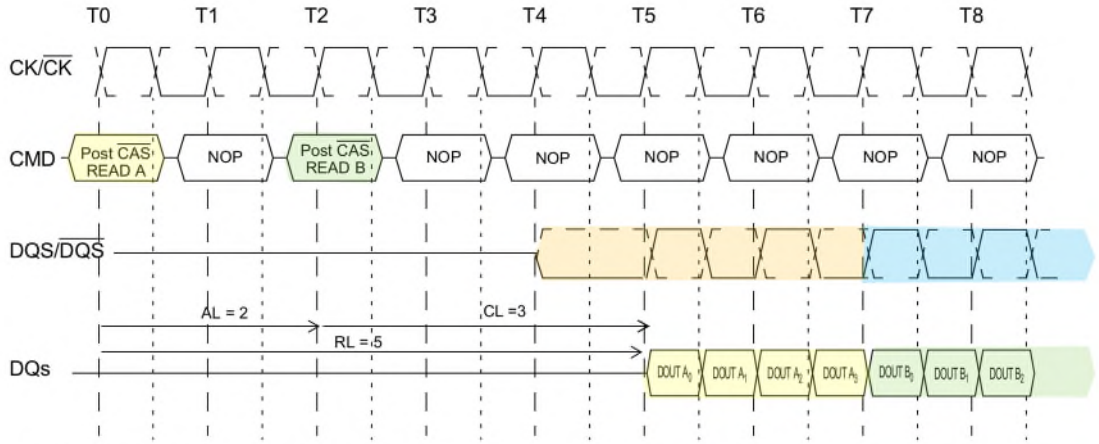
burst of data strobe signals (DQS T7-…, blue) in response to the second read command (READ B, green) according to the JEDEC standards, wherein the second data burst (DOUT B_0, B_1, B_2, …, green) follows the first data burst (DOUT A_0-A_3, yellow) on the memory bus. *See, e.g.,* EX1064 (JESD79-2) at p.28 (Fig. 27, reproduced below annotated, showing a seamless burst read operation including READ commands at every other clock for a burst length of 4). For example as discussed above, *supra* at ¶456, the first and second Read commands can be directed to the same virtual rank simulated by the first and second ranks on Perego's module according to the known rank multiplication technique, *supra* at ¶¶171-174, 277, 319, 432, so the first and second data bursts and the corresponding strobe signals are combined into a seamless burst read operation in accordance with the JEDEC standard. EX1064 (JESD79-2) at p.28 (Fig. 27).



The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 27 — Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

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460. Indeed, Perego expressly discloses an embodiment where "an additional complement data strobe signal for each byte of each memory device may be programmed at interfaces 520a and 520b to accommodate different types of memory devices on a configurable width memory module 395, such as legacy memory devices that require such a signal." EX1071 (Perego) at 14:4-10. Based on the JEDEC standards, a Skilled Artisan would have understood that DDR SDRAM memory devices require such "complement data strobe signal." For example, as discussed above with reference to claim element [12.a] (*see supra* ¶¶452-457), Perego discloses to a Skilled Artisan that its module operates in a JEDEC-style system, and a Skilled Artisan would have understood that, in response to a read command, each data burst is output on DQ lines together with a corresponding burst of data strobe signals on DQS lines in accordance with the JEDEC standards. *See, e.g.,* EX1064 (JESD79-2) at p.27 (Fig. 24 reproduced below); *see also* EX1069 at p. 2, n.2 ("A 'strobe' is a signal that indicates to the recipient that another signal— e.g., data or command—is present and valid.").

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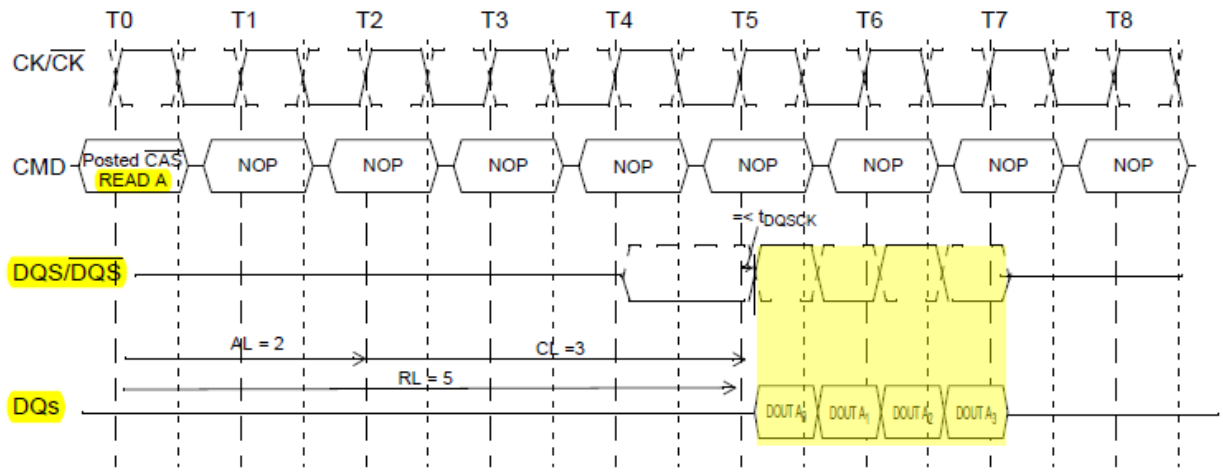

Figure 24 — Burst Read Operation: RL = 5 (AL = 2, CL = 3, BL = 4)

461. Furthermore, as also discussed above with reference to claim element [12.a] (*see supra* ¶¶452-457), a Skilled Artisan would have understood that the second data burst (blue) follows the first data burst (yellow) on the memory bus to the memory controller, in accordance with the timing of the first and second read commands and the corresponding latency parameters of the module. In the example of Fig. 27 of JESD79-2 (EX1064), the additional latency is 2 clock cycles and the CAS latency is 3 clock cycles, resulting in a total latency of 5. Thus, the first data burst in response to the first read command (READ A, yellow) at T0 starts five clock cycles later at T5, and the second data burst in response to the second read command (READ B, green) at T2 starts five clock cycles later at T7. EX1064 (JESD79-2) at p.28 (Fig. 27, reproduced above, annotated).

462. Although the above-described information from the JEDEC standards (including JESD79-2) would have been within a Skilled Artisan's knowledge when

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reading Perego, a POSITA would have alternatively been motivated to combine these teachings from JESD79-2 to Perego, given that by doing so the Skilled Artisan would have implemented predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results or challenges in implementation. *Supra* at ¶¶182-192.

463. Accordingly, Perego, either by itself or in combination with JESD79-2, discloses to a Skilled Artisan that "*the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory bus*."

c) [12.c] Buffer Configured to Prevent Collisions

464. Claim 12 requires "*wherein the buffer is configured to prevent the first burst of data strobe signals and the second burst of data strobe signals from colliding with each other*."

465. Perego discloses to a Skilled Artisan that its buffer is configured to prevent the first burst of data strobe signals of the first rank and the second burst of data strobe signals of the second rank from colliding with each other.

466. For example, because each of Perego's ranks has a separate interface, a Skilled Artisan would have understood that the first data strobe signals from the

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first rank are received with one interface of the buffer device (e.g., interface 520a) and the second data strobe signals from the second rank are received with another interface of the buffer device (e.g., interface 520b), and that they therefore do not collide with each other. *E.g.*, EX1071 (Perego) at 14:4-10 ("In another embodiment of the present invention, an additional complement data strobe signal for each byte of each memory device may be programmed at interfaces 520a and 520b to accommodate different types of memory devices on a configurable width memory module 395, such as legacy memory devices that require such a signal.").

467. Perego also discloses that its buffer "may employ a configurable datapath router within interface 591 to route requests between the primary channel and the target subset of secondary channel signal lines for each transaction." *Id.* at 15:34-37. A Skilled Artisan would have understood that such a data path router would also prevent the first and second data strobe signals from colliding with each other, because the data and the corresponding strobe signals are received only from the target rank at a time.

468. Furthermore, as discussed above with reference to claim element [1.e] and Claim 3 (*see supra* ¶¶304-311, 334-338), Perego discloses that the buffer's interface to the memory bus includes data latches and can use "source synchronous clocking (i.e., where data is transported alongside the clock from the source to destination such that the clock and data become skew tolerant)." EX1071 at 8:31-

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33. Thus, a Skilled Artisan would have understood from Perego's disclosure that the data strobe signals in the JEDEC standard are examples of such source synchronous clocking and are produced by the interface to reduce skew, thus achieving higher data rate on the memory bus. *See, e.g.,* EX1069 (Jacob Paper) at p. 7 (Fig. 13 reproduced below, explaining that DDR SDRAMs use "source synchronous data strobe (DQS) to achieve high data rates"); *see also id*. at p. 11 ("On DRAM reads, the data strobe is edge aligned with the data and system clock; the memory controller is responsible for providing its own mechanism for generating a center aligned edge. The strobe is called 'DQS.'").

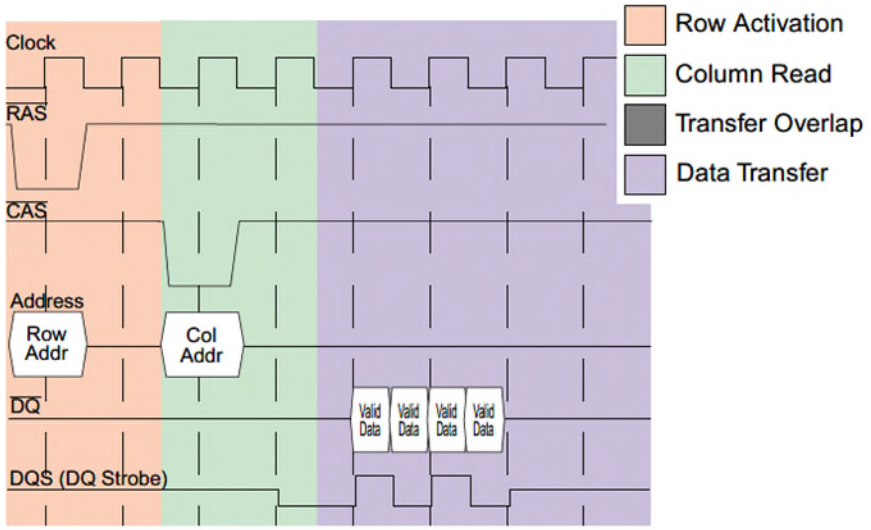

Figure 13: DDR SDRAM Read Timing (CAS-2)
DDR SDRAMs use both a clock and a source-synchronous data strobe (DQS) to achieve high data rates. DQS is used by the DRAM to sample incoming write data; it is typically ignored by the memory controller on DRAM reads.

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469. Perego further explains that its buffer device isolates signals, including data signals, interfacing the memory controller from signals interfacing the memory devices. EX1071 at 4:38-42 ("It follows from these definitions that a memory module having a buffer device (e.g., having a configurable width) isolating data, control, and address signals of the memory devices from the connector interface may be a memory subsystem."), 6:12-15 ("With further reference to FIGS. 3A and 3B, buffer device 350 transceives and provides isolation between signals interfacing to controller 310 and signals interfacing to the plurality of memory devices 360."). A Skilled Artisan would have understood that, for DDR SDRAMs, those data signals are accompanied by data strobe signals, so the buffer device also isolates the data strobe signals interfacing the memory controller from the data strobe signals interfacing the memory devices. A Skilled Artisan would have also understood that, because the first and second ranks are using separate channels, the data strobe signals on those different channels are also isolated from each other. Therefore, the buffer prevents data strobe signals from the first rank to collide with data strobe signals from the second rank when they are combined in the interface to the memory controller.

470. To the extent one might argue that Perego does not sufficiently disclose this limitation, it would have been obvious in light of Ellsberry. As discussed above, Ellsberry is analogous art to the 215 Patent, Perego, and JESD79-

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2, and discloses a memory module with a data buffer, similar to Perego. *See supra* ¶¶193-199, 350. Ellsberry discloses that its data buffer uses two bidirectional drivers 402 and 404 to transmit and receive data through respective data buses 234 and 236, each including corresponding data (DQ) and data strobe (DQS) signals. EX1073 (Ellsberry) at FIG. 4 (reproduced below) & [0045] ("Data is transmitted from the DIMM interface 202 via the data bus 230 to bidirectional signal drivers 402 & 404 that transmit and receive data over separate data busses 234 and 236 to the different sets of memory banks."). In particular, Ellsberry's data buffer selectively transmits data to and from memory devices on either Port A or Port B. *Id., see also* Abstract ("A control unit and memory bank switch are mounted on a memory module to selectively control write and/or read operations to/from memory devices communicatively coupled to the memory bank switch. By selectively routing data to and from the memory devices, a plurality of memory devices may appear as a single memory device to the operating system."), Claim 1 ("a memory bank switch communicatively coupled to the control unit, the memory bank switch to receive data information and direct the data information to one of a plurality of physical memory banks"), [0031] ("For example, if the control unit 204 determines that a particular address is associated with, or mapped to, Bank 1 212 coupled to memory bank switch 206, then it causes Port B to be activated and Port A to be disabled so that the data is written to the correct memory bank 212.");

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[0037] ("For example, where a DDR 1, 2×256 Megabyte (×4) configuration is used in the memory banks, the address bit corresponding to Column 12 is used to select a memory bank (banks on Port A or Port B). Also, where a DDR II, 2×1 Gigabyte (×8) configuration is used in the memory banks, the address bit corresponding to Row 14 is used to select a memory bank (banks on Port A or Port B)."); *see also* Ex1071 (Perego) at 5:8-9 (explaining that "[a] 'port' is a portion of an interface that serves a congruent I/O functionality.").

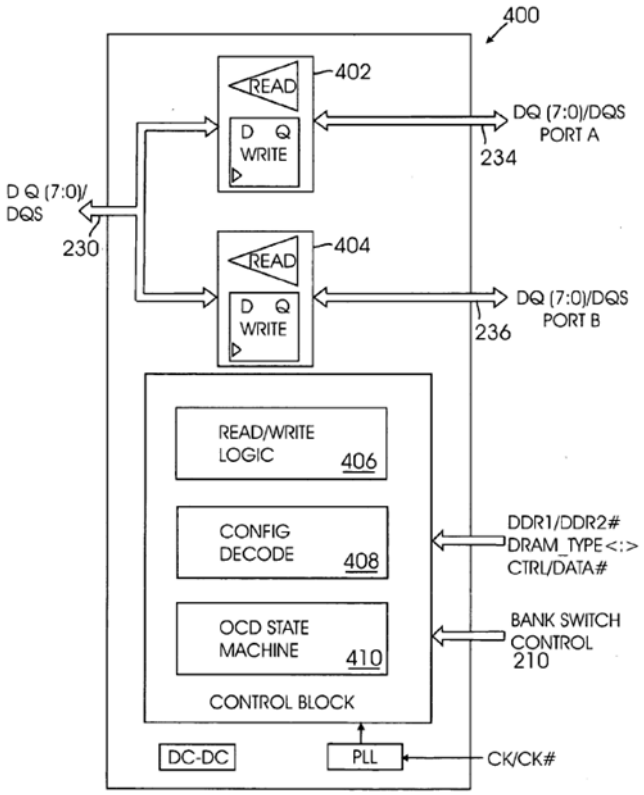

Fig. 4

471. Ellsberry also discloses to a Skilled Artisan that, in case of a read command, the data from the target rank is driven by either driver 402 or driver 404,

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but not both, on the data bus 230 to the memory controller. EX1073 (Ellsberry) at FIG. 4 (reproduced above) & [0045], *see also id*. at [0033] ("… the data from the selected target memory device is multiplexed onto the DIMM interface 202. That is, only the data read from the selected target memory device is sent to the DIMM interface 202."). Indeed, a Skilled Artisan would have understood that driving the bus 230 via only one of drivers 402 and 404, but not both, is required to avoid disastrous conflicts on the bus 230 that would result in loss of data and potentially burning out the drivers. *See, e.g.*, EX1068 (Stone) at pp. 89-90. Thus, a Skilled Artisan would have been motivated to follow the teaching of Ellsberry in the memory module of Perego and use separate drivers for the two ranks to prevent the signals, including the strobe signals, from colliding with each other on the data bus to the system controller. Thus, in the case of "*back to back adjacent read commands*" directed to two different actual ranks that correspond to a single emulated virtual rank, there would be no collisions because the driver connected to the first rank (e.g., 402) would stop driving the DQ data and DQS strobe signals onto bus 230 at T7 (in the example from JESD79-2 below), meaning the *post-amble* from the *first burst of data strobe signals* would not be driven onto bus 230, and the driver connected to the second rank (e.g., 404) would start driving the DQ and DQS signals onto bus 230 at T7, meaning the *pre-amble* of the *second burst of data strobe signals* would not be driven onto bus 230.

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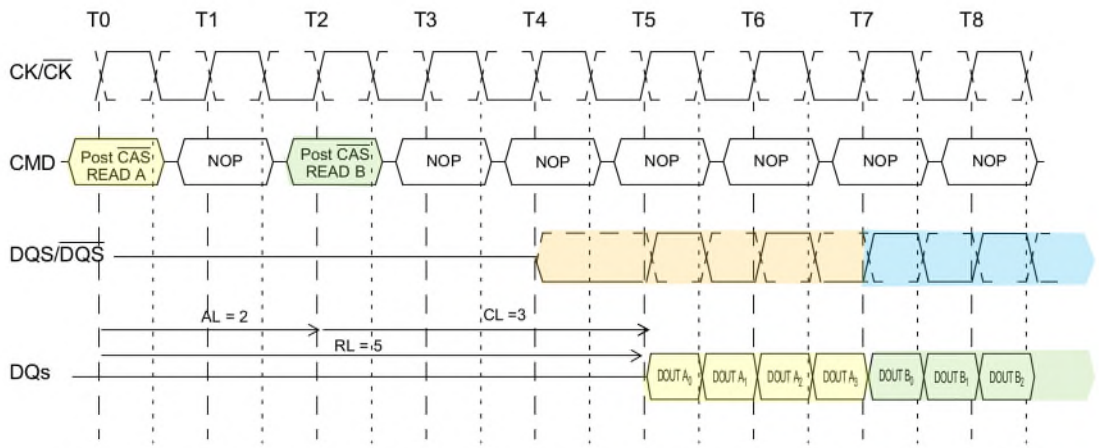

The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 27 — Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

Further, a POSITA would have alternatively been motivated to combine these teachings from Ellsberry to Perego, given that by doing so the Skilled Artisan would have implemented predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results or challenges in implementation.

472. Accordingly, Perego, either by itself or in combination with Ellsberry, discloses that that "*the buffer is configured to prevent the first burst of data strobe signals and the second burst of data strobe signals from colliding with each other*."

13. Claim 13 is Unpatentable

473. In my opinion, Claim 13 is unpatentable because it is obvious in view of Grounds 1-4.

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a) [13.a] Pre-Amble Interval and Post-Amble Interval

474. Claim 13 requires "*[t]he memory module of claim 12, wherein each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval, and....*"

475. For the reasons discussed above with reference to Claim 12 (*see supra* ¶¶452-472), Perego discloses, and in view of Ellsberry renders obvious, to a Skilled Artisan that each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval (t_{RPRE}) and a post-amble interval (t_{RPST}) in accordance with the JEDEC standards when Perego's module is implemented with DDR SDRAM memory devices. *See, e.g.*, EX1071 (Perego) at 10:56-59 ("Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices."); EX1064 (JESD79-2) at p. 26 (Fig. 24 reproduced below).

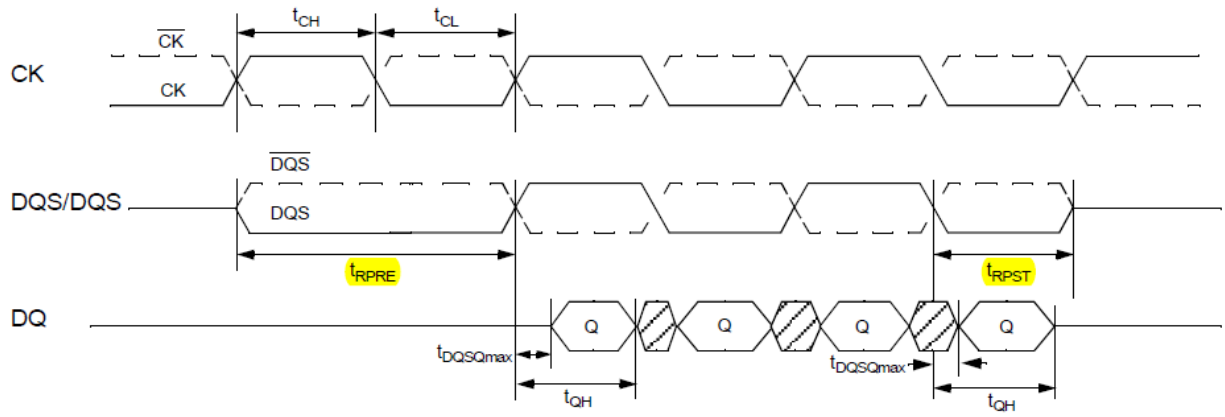

Figure 23 — Data Output (Read) Timing

See also id. at p. 65 (reproduced below in part).

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Read preamble	tRPRE
Read postamble	tRPST

476. Although the above understandings would have been within a Skilled Artisan's knowledge, a POSITA would have alternatively been motivated to combine the above teachings from JESD79-2 and/or Ellsberry to Perego, given that by doing so the Skilled Artisan would have implemented predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results or challenges in implementation. *Supra* at ¶¶182-192.

477. Therefore, Perego, either by itself or in combination with JESD79-2 and/or Ellsberry, discloses that "*each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval*."

b) [13.b] Combined Burst of Data Strobe Signals

478. Claim 13 requires "*wherein the buffer is configured to combine the first burst of data strobe signals and the second burst of data strobe signals into a combined burst of data strobe signals that does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals*."

479. For the reasons discussed above with reference to claim 12 (*see supra* ¶¶452-472), Perego discloses, and in view of Ellsberry renders obvious, to a

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Skilled Artisan that the buffer is configured to combine the first burst of data strobe signals (orange) and the second burst of data strobe signals (blue) into a combined burst of data strobe signals that does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals when they are joined at T7, in accordance with the JEDEC standards when Perego's module is implemented with rank multiplication in a JEDEC-style memory system and the two Read commands correspond to a seamless burst read operation directed to separate physical ranks emulating the same virtual rank. *Supra* ¶¶171-174, 277, 319, 432; *see also* EX1064 (JESD79-2) at p. 28 (Fig. 27, annotated version reproduced below, showing a seamless burst read operation with a combined burst of data strobe signals). For example, the JEDEC standard allows the seamless burst read operation "regardless of same or different banks as long as the banks are activated." *Id*. Thus, a Skilled Artisan would have understood that such a seamless burst read operation is allowed in a rank multiplication implementation of Perego's module where a bank address is used to select the target rank, and the first and second ranks emulate a single virtual rank. *Id*.

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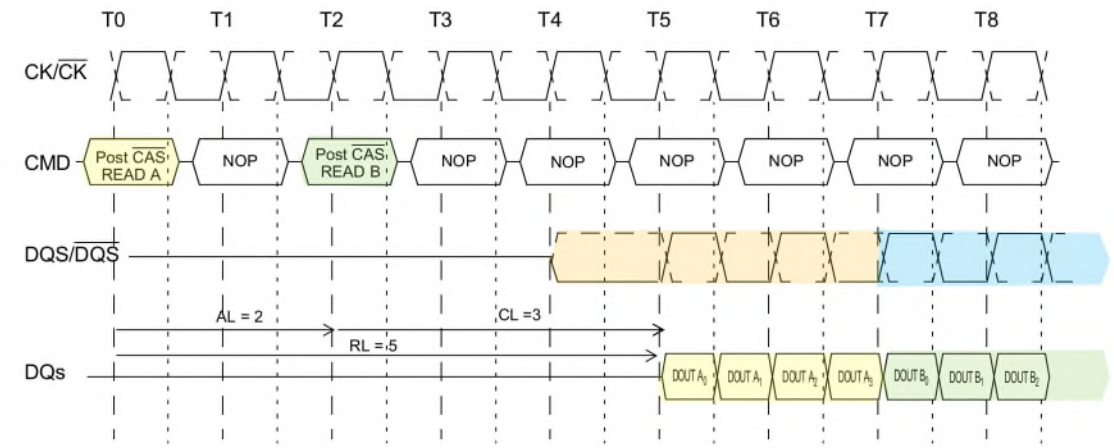

The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 27 — Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

480. For example, Perego discloses that its buffer "may employ a configurable datapath router within interface 591 to route requests between the primary channel and the target subset of secondary channel signal lines for each transaction." EX1071 at 15:34-37. A Skilled Artisan would have understood that such a data path router would combine the first and second data strobe signals to the first and second ranks such that the combined data strobe signal follows the JEDEC standard because the system memory controller expects a standard-compliant combined data strobe signal. Therefore, a Skilled Artisan would have been motivated to follow the JEDEC standard and combine the strobe signals accordingly.

481. Although the above understandings would have been within a Skilled Artisan's knowledge, a POSITA would have alternatively been motivated to combine the above teachings from JESD79-2 and/or Ellsberry to Perego, given that

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by doing so the Skilled Artisan would have implemented predictable variation by improving similar memory devices in the same way, and would not have yielded unexpected results or challenges in implementation. *Supra* at ¶¶182-192.

482. Therefore, Perego, either by itself or in combination with JESD79-2 and/or Ellsberry, discloses that "*the buffer is configured to combine the first burst of data strobe signals and the second burst of data strobe signals into a combined burst of data strobe signals that does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals*."

14. Claim 14 is Unpatentable

483. In my opinion, Claim 14 is unpatentable because it is obvious in view of Grounds 1-4.

484. Claim 14 requires "*[t]he memory module of claim 1, wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is selected to communicate data with the memory controller*."

485. Perego discloses to a Skilled Artisan that the buffer includes circuit components configurable to provide a first data path to a channel coupled to the first rank or a second data path to another channel coupled to the second rank, depending on whether the first rank or the second rank is selected to communicate

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data with the memory controller for the reasons discussed above with reference to claim elements [1.d.2]-[1.d.3], [1.e], and [1.f.1]-[1.f.2], *supra* ¶¶283-324. *See, e.g.*, EX1071 (Perego) at 15:34-37 ("… configurable width buffer device 391 may employ a configurable datapath router within interface 591 to route requests between the primary channel and the target subset of secondary channel signal lines for each transaction.") & FIGS. 5A & 5B (annotated versions reproduced below). Ellsberry also discloses these limitations. *Supra* at ¶¶319, 323; EX1073, e.g., at claim 1 ("a control unit to receive memory address and command information, …; and a memory bank switch … to receive data information and direct the data information to one of a plurality of physical memory banks in real-time according to control signals from the control unit").

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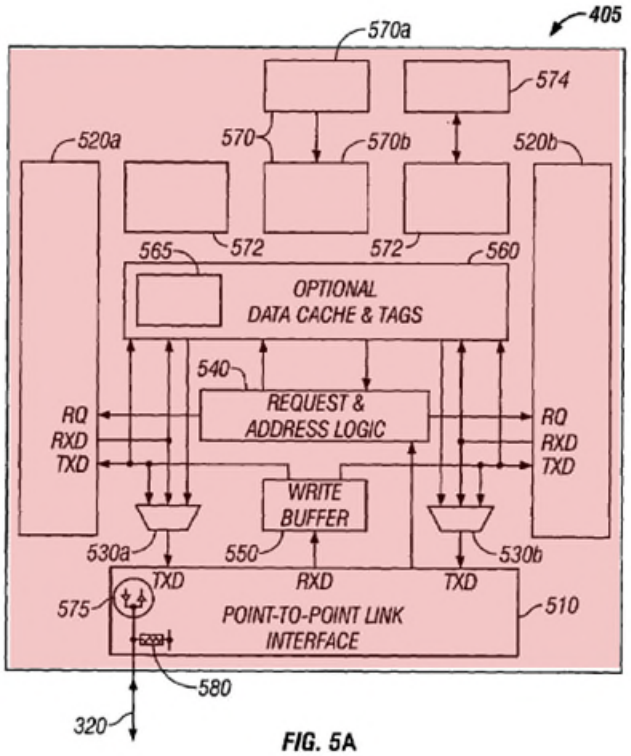
405
570a
574
520a
570
570b
520b
565
572
572
560
OPTIONAL
DATA CACHE & TAGS
540
REQUEST &
ADDRESS LOGIC
RQ
RXD
TXD
RQ
RXD
TXD
WRITE
BUFFER
530a
550
530b
TXD
RXD
TXD
575
POINT-TO-POINT LINK
INTERFACE
510
580
320

FIG. 5A

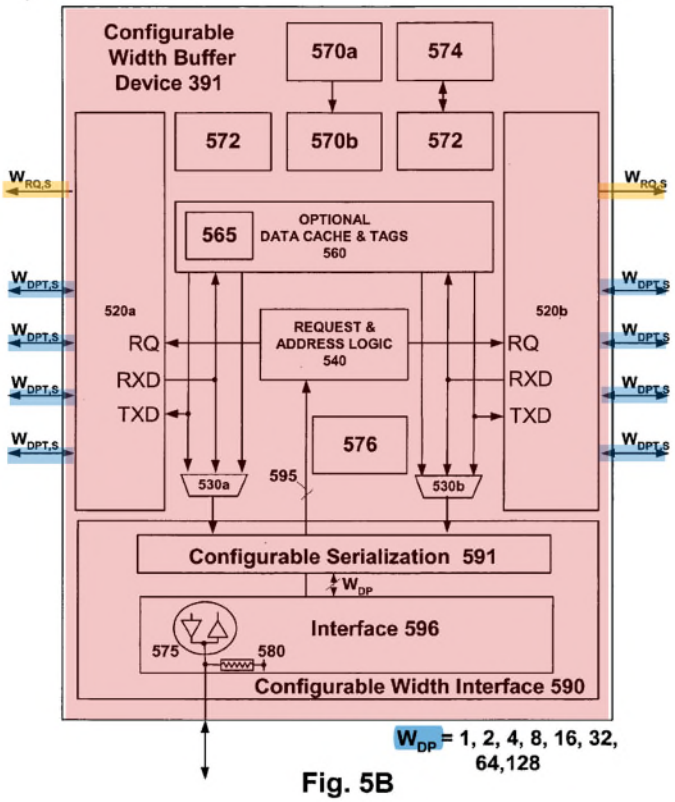
Configurable
Width Buffer
Device 391
570a
574
572
570b
572
565
OPTIONAL
DATA CACHE & TAGS
560
520a
520b
REQUEST &
ADDRESS LOGIC
540
RQ
RXD
TXD
RQ
RXD
TXD
576
530a
595
530b
Configurable Serialization 591
Interface 596
575
580
Configurable Width Interface 590
W_{DP} = 1, 2, 4, 8, 16, 32,
64,128

Fig. 5B

486. For example, Perego discloses that commands and corresponding data bursts are selectively routed to and from a subset of the memory devices and the memory controller through the buffer device, for example:

> "According to an embodiment of the present invention, multiplexers 530a and 530b perform bandwidth-concentrating operations, between interface 510 and interfaces 520a and 520b, as well as route data from an appropriate source (i.e. target a subset of channels, internal data, cache or write buffer)."

Id. at 11:56-61.

> "In a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370. One or more of memory devices 360 may respond by transmitting data to Buffer device 350 which receives the data via one or more of channels 370 and in response, transmits corresponding signals to controller 310 via point-to-point link 320a."

Id. at 6:15-25; *see also id*. at 21:16-20 ("Any number of channels 415a–415d, for example[,] two channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations.") & 15:40-45 ("By accessing a subset of secondary channel signal lines per transaction, a number of benefits may be derived. One of these benefits is reduced power consumption.").

487. A Skilled Artisan would have understood from this disclosure that Perego's buffer device includes circuit components, such as circuit components in multiplexers 530a and 530b and interfaces 520a, 520b and 510 or 590 (and the

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respective transceivers in those interfaces) that provide a first data path to the first rank or a second data path to the second rank, depending on whether the first rank or second rank is selected to communicate with the memory controller.

488. Therefore, Perego discloses and renders obvious to a Skilled Artisan alone or in combination with Ellsberry to a Skilled Artisan that "*the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is selected to communicate data with the memory controller*."

15. Claim 15 is Unpatentable

489. In my opinion, Claim 15 is unpatentable because it is obvious in view of Grounds 1-4.

490. Claim 15 requires "*[t]he memory module of claim 14, the at least one of the circuit components is configured to provide the first data path in response to the first control signals, and is configured to provide the second data path in response to the second control signals*."

491. As an initial matter, I note that the term "*the at least one of the circuit components*" lacks proper antecedent basis. For purposes of my analysis below I will assume this refers to one or more of the "*circuit components*" from Claim 14.

492. In any event, Perego discloses to a Skilled Artisan that at least one of the circuit components that provide the first data path to the first rank or the second

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data path to the second rank is configured to provide the first data path in response to the first control signals, and is configured to provide the second data path in response to the second control signals, for the reasons discussed above with reference to claim elements [1.f.1]-[1.f.2] and Claim 14. *See supra* ¶¶312-324 & 483-488. Ellsberry also discloses these limitations. *Supra* at ¶¶319, 323; EX1073, e.g., at claim 1 ("a control unit to receive memory address and command information, …; and a memory bank switch … to receive data information and direct the data information to one of a plurality of physical memory banks in real-time according to control signals from the control unit").

493. For example, Perego teaches that interfaces 520a, 520b, 510 and 590 include transceivers, such as transceivers 575, that are controlled in accordance with the received memory command. EX1071 at FIGS. 5A & 5B & 14:62-15:6 ("Channels 370 (FIG. 3C) may be subdivided into several addressable subsets. The address of the transaction will determine which target subset of channels 370 will be utilized for the data transfer portion of the transaction. … Typically, configuration of the transceivers may be effectuated by enabling or disabling how many transceivers are active in a given transfer between one or more memory devices and configurable width buffer device 391."). Perego also discloses that its buffer "may employ a configurable datapath router within interface 591 to route requests between the primary channel and the target subset of secondary channel

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signal lines for each transaction." *Id.* at 15:34-37. Perego further discloses that multiplexers 530a and 530b are also configured to route the data in accordance with the target of the transaction. *Id.* at 11:56-61 ("According to an embodiment of the present invention, multiplexers 530a and 530b perform bandwidth-concentrating operations, between interface 510 and interfaces 520a and 520b, as well as route data from an appropriate source (i.e. target a subset of channels, internal data, cache or write buffer)."). A Skilled Artisan would have understood that such transceivers, data path router, and multiplexers in Perego's buffer device are configured to provide the data path to the target rank in response to corresponding control signals.

494. Therefore, Perego discloses and renders obvious alone or in combination with Ellsberry that "*the at least one of the circuit components is configured to provide the first data path in response to the first control signals, and is configured to provide the second data path in response to the second control signals*."

16. Claim 16 is Unpatentable

495. In my opinion, Claim 16 is unpatentable because it is obvious in view of Grounds 1-4.

496. Claim 16 requires "*[t]he memory module of claim 1, wherein the logic is configured to enable the communication of the first data burst between the at*

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least one first memory integrated circuit and the memory controller in accordance with a latency value."

497. As shown in the table below, claim element [1.f.1] and Claim 6 are similar to Claim 16:

Claims 1, 6	**Claim 16**
[1.f.1] logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, [6] The memory module of claim 1, further comprising determining a latency value, wherein the communication of the first data burst between the at least one first memory integrated circuit and the memory controller is enabled in accordance with the latency value.	[16] The memory module of claim 1, wherein the logic is configured to enable the communication of the first data burst between the at least one first memory integrated circuit and the memory controller in accordance with a latency value.

498. As discussed above with reference to claim elements [1.f.1] and claim 6, the prior art references in Grounds 1-4 satisfy "*wherein the logic is configured to enable the communication of the first data burst between the at least one first memory integrated circuit and the memory controller in accordance with a latency value.*" *See supra* ¶¶312-324 & 369-381.

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17. Claim 17 is Unpatentable

499. In my opinion, Claim 17 is unpatentable because it is obvious in view of Grounds 1-4.

500. Claim 17 requires "*[t]he memory module of claim 16, wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the first data burst through the buffer*."

501. As shown in the table below, Claim 17 is nearly identical to Claim 8:

Claim 8	**Claim 17**
[8] The memory module of claim 1, wherein the buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the first data burst or the second data burst through the buffer.	[17] The memory module of claim 16, wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the first data burst through the buffer.

502. As discussed above with reference to Claim 8, the prior art references in Grounds 1-4 satisfy "*wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the first data burst through the buffer.*" *Supra* ¶¶411-419.

18. Claim 18 is Unpatentable

503. In my opinion, Claim 18 is unpatentable because it is obvious in view of Grounds 1-4.

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504. Claim 18 requires "*[t]he memory module of claim 16, wherein the logic is further configured to determine the latency value.*"

505. As shown in the table below, Claim 18 is similar to Claims [1.f.1] and 6:

Claims 1, 6	**Claim 18**
[1.f.1] logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, [6] The memory module of claim 1, further comprising determining a latency value, wherein the communication of the first data burst between the at least one first memory integrated circuit and the memory controller is enabled in accordance with the latency value.	[18] The memory module of claim 16, wherein the logic is further configured to determine the latency value.

506. As discussed above with reference to Claims [1.f.1] and 6, the prior art references in Grounds 1-4 satisfy "*wherein the logic is further configured to determine the latency value*." *Supra* ¶¶312-324 & 369-381.

507. For example, as discussed above with reference to Claim 6, a Skilled artisan would have understood from the disclosure of Perego that the memory

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controller is setting the latency values during initialization, in accordance with the JEDEC standards for DDR SDRAM memories. *See, e.g.*, EX1071 (Perego) at 12:20-34 ("A serial interface 574 may be employed to couple signals utilized in initialization of module or memory device identification values, test function, set/reset, access latency values, vendor specific functions or calibration."). A Skilled Artisan would have also understood that the logic in the buffer device of Perego determines an overall latency based on those settings and controls the data transfers accordingly, as discussed above with reference to Claims 3, 4, and 6. *See supra* ¶¶332-363, 369-381.

508. Accordingly, the prior art references in Grounds 1-4 satisfy "*wherein the logic is further configured to determine the latency value*."

19. Claim 19 is Unpatentable

509. In my opinion, Claim 19 is unpatentable because it is obvious in view of Grounds 1-4.

510. Claim 19 requires "*[t]he memory module of claim 16, wherein the logic is further configured to enable the communication of the second data burst between the at least one second memory integrated circuit and the memory controller in accordance with the latency value*."

511. As shown in the table below, Claim 19 is similar to Claim 6:

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Claim 6	**Claim 19**
[6] The memory module of claim 1, further comprising determining a latency value, wherein the communication of the first data burst between the at least one first memory integrated circuit and the memory controller is enabled in accordance with the latency value.	[19] The memory module of claim 16, wherein the logic is further configured to enable the communication of the second data burst between the at least one second memory integrated circuit and the memory controller in accordance with the latency value.

512. As discussed above with reference to Claim 6, the prior art references in Grounds 1-4 satisfy "*wherein the logic is further configured to enable the communication of the second data burst between the at least one second memory integrated circuit and the memory controller in accordance with the latency value*." *See supra* ¶¶369-381.

513. For example, a Skilled Artisan would have understood that both of the first and second data burst are communicated in accordance with the latency values, as discussed above with reference to Claims 3, 4, and 6. *See supra* ¶¶332-363, 369-381.

514. Accordingly, the prior art references in Grounds 1-4 satisfy "*wherein the logic is further configured to enable the communication of the second data burst between the at least one second memory integrated circuit and the memory controller in accordance with the latency value*."

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20. Claim 20 is Unpatentable

515. In my opinion, Claim 20 is unpatentable because it is obvious in view of Grounds 1-4.

516. Claim 20 requires "*[t]he memory module of claim 19, wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the second data burst through the buffer*."

517. As shown in the table below, Claim 20 is very similar to Claim 8:

Claim 8	**Claim 20**
[8] The memory module of claim 1, wherein the buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the first data burst or the second data burst through the buffer.	[20] The memory module of claim 19, wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the second data burst through the buffer.

518. As discussed above with reference to Claim 8, the prior art references in Grounds 1-4 satisfy the "*wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the second data burst through the buffer*" limitation. *See supra* ¶¶411-419.

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21. Claim 21 is Unpatentable

519. In my opinion, Claim 21 is unpatentable because it is obvious in view of Grounds 1-4.

a) [21.a.1] Method of Operating a Memory Module

520. Claim 21 requires "*[a] method of operating a memory module*."

521. As shown in the table below, claim limitation [21.a.1] is very similar to claim limitations [1.a.1] and [1.a.2]:

Claim 1	**Claim 21**
[1.a.1] A memory module [1.a.2] operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller	[21.a.1] A method of operating a memory module

522. For the reasons discussed above with reference to claim limitations [1.a.1] and [1.a.2], the prior art references in Grounds 1-4 satisfy "*[a] method of operating a memory module.*" *Supra* ¶¶212-228.

b) [21.a.2] Coupled to a memory controller

523. Claim 21 requires "*coupled to a memory controller via a memory bus*."

524. As shown in the table below, claim limitation [21.a] is very similar to claim limitation [1.a.2]:

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Claim 1	Claim 21
[1.a.2] operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller	[21.a.2] coupled to a memory controller via a memory bus,

525. For the reasons discussed above with reference to claim limitation [1.a.2], the prior art references in Grounds 1-4 satisfy "*coupled to a memory controller via a memory bus*." *Supra* ¶¶217-228.

c) [21.a.3] Ranks

526. Claim 21 requires "*the memory module comprising memory integrated circuits arranged in ranks and mounted on a printed circuit board*."

527. As shown in the table below, claim limitation [21.a.3] is very similar to claim limitations [1.d.1]:

Claim 1	Claim 21
[1.d.1] a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank; the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank	[21.a.3] the memory module comprising memory integrated circuits arranged in ranks and mounted on a printed circuit board

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528. For the reasons discussed above with reference to claim limitation [1.d.1], the prior art references in Grounds 1-4 satisfy *the memory module comprising memory integrated circuits arranged in ranks and mounted on a printed circuit board.*" *Supra* ¶¶261-282.

d) [21.a.4] Edge Connections

529. Claim 21 requires "*having a plurality of edge connections coupled to the memory bus*."

530. As shown in the table below, claim limitation [21.a.4] is very similar to claim limitation [1.b]:

Claim 1	**Claim 21**
[1.b] a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;	[21.a.4] having a plurality of edge connections coupled to the memory bus,

531. For the reasons discussed above with reference to claim limitation [1.b], the prior art references in Grounds 1-4 satisfy "*having a plurality of edge connections coupled to the memory bus.*" *Supra* ¶¶243-248.

e) [21.a.5] First Rank

532. Claim 21 requires "*the memory integrated circuits including at least one first memory integrated circuit in a first rank and at least one second memory integrated circuit in a second rank.*"

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533. As shown in the table below, claim limitation [21.a.5] is very similar to claim limitations [1.d.1]:

Claim 1	**Claim 21**
[1.d.1] a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank; the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank	[21.a.5] the memory integrated circuits including at least one first memory integrated circuit in a first rank and at least one second memory integrated circuit in a second rank,

534. For the reasons discussed above with reference to claim limitation [1.d.1], the prior art references in Grounds 1-4 satisfy "*the memory integrated circuits including at least one first memory integrated circuit in a first rank and at least one second memory integrated circuit in a second rank.*" *See supra* ¶¶261-282.

535. Accordingly, the prior art references in Grounds 1-4 satisfy the "*memory integrated circuits including at least one first memory integrated circuit in a first rank and at least one second memory integrated circuit in a second rank*" limitation.

f) [21.a.6] Comprising

536. Claim 21 requires "*the method comprising*."

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537. As discussed, above, the prior art references in Grounds 1-4 teach limitations [21.a.1]-[21.a.5]. *See supra* ¶¶520-535. Further, as discussed below, the prior art references in Grounds 1-4 similarly teach the limitations that the method must comprise. *See infra* ¶¶539-556.

538. Accordingly, the prior art references in Grounds 1-4 satisfy "*the method comprising*."

g) [21.b] Receiving a Second Set of Input Command and Address Signals

539. Claim 21 requires "*receiving at one or more circuits coupled to the printed circuit board a first set of input command and address signals representing a first memory command from the memory controller via the memory bus, the first memory command to cause the memory module to receive or output a first data burst*."

540. As shown in the table below, claim limitation [21.b] is very similar to claim limitations [1.c], [1.a.2], and [1.a.3]:

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Claim 1	**Claim 21**
[1.c] a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command; [1.a.2] operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, [1.a.3] the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst,	[21.b] receiving at one or more circuits coupled to the printed circuit board a first set of input command and address signals representing a first memory command from the memory controller via the memory bus, the first memory command to cause the memory module to receive or output a first data burst

541. For the reasons discussed above with reference to claim limitations [1.c], [1.a.2], and [1.a.3], the prior art references in Grounds 1-4 satisfy "*receiving at one or more circuits coupled to the printed circuit board a first set of input command and address signals representing a first memory command from the memory controller via the memory bus, the first memory command to cause the*

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memory module to receive or output a first data burst." *See supra* ¶¶249-260, 217-239.

h) [21.c] First Set of Output Command and Address Signals

542. Claim 21 requires "*generating a first set of output command and address signals in response to the first set of input command and address signals, the first set of output command and address signals selecting the first rank to receive or output the first data burst*."

543. As shown in the table below, claim limitation [21.c] is similar to claim limitations [1.c] and [1.d.2] and Claim 10:

Claims 1, 10	**Claim 21**
[1.c] a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command; [1.d.2] wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate [10] The memory module of claim 9, wherein the memory module produces at least third and fourth chip select signals in	[21.c] generating a first set of output command and address signals in response to the first set of input command and address signals, the first set of output command and address signals selecting the first rank to receive or output the first data burst

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response to the first memory command, the third chip select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the fourth chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.	

544. As discussed above with reference to claim limitations [1.c] and [1.d.2] and claim 10, the prior art references in Grounds 1-4 satisfy "*generating a first set of output command and address signals in response to the first set of input command and address signals, the first set of output command and address signals selecting the first rank to receive or output the first data burst.*" *Supra* ¶¶249-260, 283-303, 427-442.

i) [21.d] Second Set of Input Command and Address Signals

545. Claim 21 requires "*receiving at the one or more circuits a second set of input command and address signals representing a second memory command*

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from the memory controller via the memory bus, the second memory command to cause the memory module to receive or output a second data burst."

546. As shown in the table below, claim limitation [21.d] is very similar to claim limitation [1.c], [1.a.2], and [1.a.3]:

Claim 1	**Claim 21**
[1.c] a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command; [1.a.2] operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, [1.a.3] the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst,	[21.d] receiving at the one or more circuits a second set of input command and address signals representing a second memory command from the memory controller via the memory bus, the second memory command to cause the memory module to receive or output a second data burst

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547. As discussed above with reference to claim limitations [1.c], [1.a.2], and [1.a.3], the prior art references in Grounds 1-4 satisfy "*receiving at the one or more circuits a second set of input command and address signals representing a second memory command from the memory controller via the memory bus, the second memory command to cause the memory module to receive or output a second data burst.*" *See supra* ¶¶249-260, 217-239.

j) [21.e] Second set of Output Command and Address Signals

548. Claim 21 requires "*generating a second set of output command and address signals in response to the second set of input command and address signals, the second set of output command and address signals selecting the second rank to receive or output the second data burst*."

549. As shown in the table below, claim limitation [21.e] is very similar to claim limitation [1.c] and [1.d.2] and Claim 11:

Claims 1, 11	**Claim 21**
[1.c] a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command; [1.d.2] wherein the first rank is selected to receive or output the	[21.e] generating a second set of output command and address signals in response to the second set of input command and address signals, the second set of output command and address signals selecting the second rank to receive or output the second data burst

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first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command; [11] The memory module of claim 10, wherein the memory module produces at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first [sic: second] memory command, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an active value to cause the at least one second memory integrated circuit to receive or output data signals in response to the second memory command.	

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550. As discussed above with reference to claim limitations [1.c] and [1.d.2] and Claim 11, the prior art references in Grounds 1-4 satisfy "*generating a second set of output command and address signals in response to the second set of input command and address signals, the second set of output command and address signals selecting the second rank to receive or output the second data burst.*" *See supra* ¶¶249-260, 283-303, 443-450.

k) [21.f] First Control Signals

551. Claim 21 requires "*in response to the first memory command, providing first control signals to a buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer*."

552. As shown in the table below, claim limitation [21.f] is very similar to claim limitation [1.f.1]:

Claim 1	**Claim 21**
[1.f.1] logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer	[21.f] in response to the first memory command, providing first control signals to a buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer

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553. As discussed above with reference to claim limitation [1.f.1], the prior art references in Grounds 1-4 satisfy "*in response to the first memory command, providing first control signals to a buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer.*" *See supra* ¶¶312-324.

l) [21.g] Second Control Signals

554. Claim 21 requires "*in response to the second memory command, providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals*."

555. As shown in the table below, claim limitation [21.g] is similar to claim limitation [1.f.2]:

Claim 1	**Claim 21**
[1.f.2] wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals	[21.g] in response to the second memory command, providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals

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556. As discussed above with reference to claim limitation [1.f.2], the prior art references in Grounds 1-4 satisfy "*in response to the second memory command, providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.*" *See supra* ¶¶312-324.

22. Claim 22 is Unpatentable

557. In my opinion, Claim 22 is unpatentable because it is obvious in view of Grounds 1-4.

558. Claim 22 requires "*[t]he method of claim 21, further comprising isolating the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory system*."

559. As shown in the table below, Claim 22 is very similar to Claim 2:

Claim 2	**Claim 22**
[2] The memory module of claim 1, wherein the buffer is configured to isolate both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory controller.	[22] The method of claim 21, further comprising isolating the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory system.

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560. For the same reasons discussed above with reference to Claim 2, the prior art references in Grounds 1-4 satisfy "*further comprising isolating the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory system*." *Supra* ¶¶325-331.

561. Accordingly, the prior art references in Grounds 1-4 satisfy "*further comprising isolating the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory system*."

23. Claim 23 is Unpatentable

562. In my opinion, Claim 23 is unpatentable because it is obvious in view of Grounds 1-4.

a) [23.a] Input Chip-Select Signal

563. Claim 23 requires "*[t]he method of claim 21, wherein the first set of input command and address signals include at least one input chip-select signal*."

564. As shown in the table below, Claim 23 is very similar to Claim 9:

Claim 9	**Claim 23**
[9] The memory module of claim 1, wherein the first memory command includes at least one first chip select signal and the second memory command includes at least one second chip select signal.	[23.a] The method of claim 21, wherein the first set of input command and address signals include at least one input chip-select signal,

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565. For the same reasons discussed above with reference to Claim 9, the prior art references in Grounds 1-4 satisfy "*wherein the first set of input command and address signals include at least one input chip-select signal*." *See supra* ¶¶420-426.

b) [23.b] Generating Chip Select Signals

566. Claim 23 requires "*the method further comprising generating a first chip select signal and a second chip select signal in response to the first set of input command and address signals, the first chip-select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the second chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command*."

567. As shown in the table below, Claim 23 is very similar to Claim 10:

Claim 10	**Claim 23**
[10] The memory module of claim 9, wherein the memory module produces at least third and fourth chip select signals in response to the first memory command, the third chip select signal being provided to the at least one first memory integrated circuit and having an active value	[23.b] the method further comprising generating a first chip select signal and a second chip select signal in response to the first set of input command and address signals, the first chip-select signal being provided to the at least one first memory integrated circuit and having an

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to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the fourth chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.	active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the second chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.

568. For the same reasons discussed above with reference to Claim 10, the prior art references in Grounds 1-4 satisfy "*the method further comprising generating a first chip select signal and a second chip select signal in response to the first set of input command and address signals, the first chip-select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the second chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command*." *See supra* ¶¶427-442.

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24. Claim 24 is Unpatentable

569. In my opinion, Claim 24 is unpatentable because it is obvious in view of Grounds 1-4.

570. Claim 24 requires "*[t]he method of claim 21, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of the memory integrated circuits*."

571. As shown in the table below, Claim 24 is very similar to claim 3:

Claim 3	**Claim 24**
[3] The memory module of claim 1, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.	[24] The method of claim 21, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of the memory integrated circuits.

572. For the same reasons discussed above with reference to Claim 3, the prior art references in Grounds 1-4 satisfy "*wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of the memory integrated circuits*." *See supra* ¶¶332-353.

25. Claim 25 is Unpatentable

573. In my opinion, Claim 25 is unpatentable because it is obvious in view of Grounds 1-4.

574. Claim 25 requires "*[t]he method of claim 21, further comprising reporting an overall CAS latency of the memory module to the memory controller,*

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the overall CAS latency having one more clock cycle than an actual operational CAS latency of the memory integrated circuits."

575. As shown in the table below, Claim 25 is very similar to claim 4:

Claim 4	**Claim 25**
[4] The memory module of claim 1, further comprising an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of memory integrated circuits.	[25] The method of claim 21, further comprising reporting an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of the memory integrated circuits.

576. For the same reasons discussed above with reference to Claim 4, the prior art references in Grounds 1-4 satisfy "*further comprising reporting an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of the memory integrated circuits*." *See supra* ¶¶354-363.

26. Claim 26 is Unpatentable

577. In my opinion, Claim 26 is unpatentable because it is obvious in view of Grounds 1-4.

578. Claim 26 requires "*[t]he method of claim 21, wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second drank is caused to communicate data with the memory controller*."

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579. As shown in the table below, claim 26 is very similar to Claim 14:

Claim 14	**Claim 26**
[14] The memory module of claim 1, wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is selected to communicate data with the memory controller.	[26] The method of claim 21, wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second drank is caused to communicate data with the memory controller.

580. For the same reasons discussed above with reference to claim 14, the prior art references in Grounds 1-4 satisfy "*wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second drank is caused to communicate data with the memory controller*." *See supra* ¶¶483-488.

27. Claim 27 is Unpatentable

581. In my opinion, Claim 27 is unpatentable because it is obvious in view of Grounds 1-4.

582. Claim 27 requires "*[t]he method of claim 21, wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits*."

583. As shown in the table below, Claim 27 is very similar to Claim 5:

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Claim 5	**Claim 27**
[5] The memory module of claim 1, wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits.	[27] The method of claim 21, wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits.

584. For the same reasons discussed above with reference to Claim 5, the prior art references in Grounds 1-4 satisfy "*wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits*." *See supra* ¶¶364-368.

28. Claim 28 is Unpatentable

585. In my opinion, Claim 28 is unpatentable because it is obvious in view of Grounds 1-4.

a) [28.a] First and Second Read Command

586. Claim 28 requires "*[t]he method of claim 21, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and*."

587. As shown in the table below, claim 28 is very similar to claim element [12.a]:

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Claim 12	**Claim 28**
[12.a] The memory module of claim 1, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and	[28.a] The method of claim 21, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and

588. For the same reasons discussed above with reference to claim element [12.a], the prior art references in Grounds 1-4 satisfy "*wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands*." *See supra* ¶¶452-457.

b) [28.b] Outputs First and Second Data Burst

589. Claim 28 requires "*wherein the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein the memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory bus*."

590. As shown in the table below, claim 28 is very similar to claim element [12.b]:

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Claim 12	**Claim 28**
[12.b] wherein the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory bus, and	[28.b] wherein the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein the memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory bus,

591. For the same reasons discussed above with reference to claim element [12.b], the prior art references in Grounds 1-4 satisfy "*wherein the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein the memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory bus*." *See supra* ¶¶458-463.

c) [28.c] Third Burst of Data Strobe Signals

592. Claim 28 requires "*the method further comprising combining the first burst of data strobe signals and the second burst of data strobes to form a third burst of data strobe signals on the memory bus*."

593. As shown in the table below, Claim 28 is very similar to claim element [13.b]:

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Claim 13	Claim 28
[13.b] wherein the buffer is configured to combine the first burst of data strobe signals and the second burst of data strobe signals into a combined burst of data strobe signals that does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals.	[28.c] the method further comprising combining the first burst of data strobe signals and the second burst of data strobes to form a third burst of data strobe signals on the memory bus.

594. For the same reasons discussed above with reference to claim element [13.b], the prior art references in Grounds 1-4 satisfy "*the method further comprising combining the first burst of data strobe signals and the second burst of data strobes to form a third burst of data strobe signals on the memory bus*." *See supra* ¶¶478-482.

29. Claim 29 is Unpatentable

595. In my opinion, Claim 29 is unpatentable because it is obvious in view of Grounds 1-4.

a) [29.a] Pre-Amble Interval and Post-Amble Interval

596. Claim 29 requires "*[t]he method of claim 28, wherein each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval, and*."

597. As shown in the table below, claim element [29.a] is very similar to claim element [13.a]:

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Claim 13	**Claim 29**
[13.a] The memory module of claim 12, wherein each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval, and	[29.a] The method of claim 28, wherein each of the fist burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval, and

598. For the same reasons discussed above with reference to claim element [13.a], the prior art references in Grounds 1-4 satisfy "*wherein each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval*." *See supra* ¶¶474-477.

b) [29.b] The Third Burst of Data Strobes

599. Claim 29 requires "*wherein the third burst of data strobes does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals*."

600. As shown in the table below, claim element [29.b] is very similar to claim element [13.b]:

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Claim 13	**Claim 29**
[13.b] wherein the buffer is configured to combine the first burst of data strobe signals and the second burst of data strobe signals into a combined burst of data strobe signals that does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals.	[29.b] wherein the third burst of data strobes does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals.

601. For the same reasons discussed above with reference to claim element [13.b], the prior art references in Grounds 1-4 satisfy "*wherein the third burst of data strobes does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals*." *Supra* ¶¶478-482.

C. <u>Secondary Considerations</u>

602. At this stage of these proceedings, it is my understanding that Petitioner has no burden to identify and rebut secondary considerations. Rather, it is my understanding that Patent Owner must first present a prima facie case for such consideration, which Petitioners should then have the chance to rebut. That said, I have considered evidence of secondary considerations that I am aware of at this time, and I am currently unaware of any evidence of secondary considerations that would support a finding of non-obviousness. To the contrary, I understand

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that "simultaneous invention" can be a secondary consideration of obviousness, and here I believe there is ample evidence of such "simultaneous invention."

603. The 215 Patent discloses and claims "rank multiplication" as the solution to expensive, high-density memory devices where "the price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices." *See, e.g.*, EX1001 at 13:51-17:12. But in my opinion, Skilled Artisans already recognized that there was a "problem" with high density memory devices in that they cost ***much*** more than low density memory devices, *see, e.g. supra* ¶¶ 171-174, and they also recognized that the "solution" (and significant business opportunity) was "rank multiplication" where you replace one rank of (expensive) high-density memory devices with two or more ranks of (cheaper) low-density memory devices in a way that is transparent to the system memory controller (such that no changes are needed outside the memory module), *see id.* To give a concrete hypothetical example, if one rank of 1Gb of high-density memory cost $1,000, while two ranks of 512Mb of low-density memory cost $200, the "solution" of "rank multiplication" would present a significant business opportunity to create a module with 1Gb of memory that cost, for example, $500 — much less than the competing 1Gb module costing $1,000, but still a significant profit margin given that the memory only cost $200. In my opinion, Amidi, Perego, and Ellsberry all recognized this "problem" (and business opportunity) and

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all provided very similar solutions — with Ellsberry's solution nearly identical to the solution in the 215 Patent — all in the 18-month period before the earliest effective filing date of the claims of the 215 Patent. In my opinion, this is objective evidence that the claims of the 215 Patent were obvious. Indeed, as discussed above, hundreds of claims from this family of patents — all directed to "rank multiplication" — have been found invalid, providing ample evidence of widespread "simultaneous invention" of the subject matter and claims of the 215 Patent. *See, e.g.*, *supra* ¶¶ 89-95, 99.

* * *

I, Andrew Wolfe, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: January 10, 2023

Andrew Wolfe

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EXHIBIT LIST

Exhibit #	Description
1001	U.S. Patent No. 9,858,215 (issued January 2, 2018)
1002	File History of U.S. Patent No. 9,858,215 (filed May 18, 2015)
1003	Declaration of Dr. Andrew Wolfe
1004	Curriculum Vitae of Dr. Andrew Wolfe
1005	U.S. Provisional Application No. 60/645,087 (filed Jan. 19, 2005)
1006	U.S. Provisional Application No. 60/588,244 (filed July 15, 2004)
1007	U.S. Provisional Application No. 60/550,668 (filed March 5, 2004)
1008	U.S. Provisional Application No. 60/575,595 (filed May 28, 2004)
1009	U.S. Provisional Application No. 60/590,038 (filed July 21, 2004)
1010	File History of U.S. Patent No. 7,286,436 (filed March 7, 2005)
1011	U.S. Patent No. 7,286,436 (issued Oct. 23, 2007)
1012	U.S. Patent No. 7,289,386 (issued Oct. 30, 2007)
1013	Affirmance of the Examiner's Decision on Reexamination of '386 Patent (Feb. 25, 2015)
1014	Reexamination Certificate for '386 Patent (Aug. 19, 2016)
1015	U.S. Patent No. 7,619,912 (issued Nov. 17, 2009)
1016	Decision on Reexamination of '912 Patent (June 6, 2016); Decision Under 37 C.F.R. § 41.77(f) (July 27, 2018); and Decision on Rehearing (Jan. 31, 2019)
1017	Reexamination Certificate for '912 Patent (Feb. 8, 2021)
1018	Petition for *Inter Partes* Review of U.S. Patent No. 7,619,912 (Feb. 17, 2022)

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Exhibit #	Description
1019	Patent Owner Preliminary Response to Petition for *Inter Partes* Review of U.S. Patent No. 7,619,912 (July 21, 2022)
1020	Declaration of Michael C. Brogioli, Ph.D. in Support of Patent Owner Preliminary Response to Petition for *Inter Partes* Review of U.S. Patent No. 7,619,912 (July 21, 2022)
1021	Reply to Patent Owner Preliminary Response to Petition for *Inter Partes* Review of U.S. Patent No. 7,619,912 (Aug. 26, 2022)
1022	Sur-Reply to Patent Owner Preliminary Response to Petition for *Inter Partes* Review of U.S. Patent No. 7,619,912 (Sept. 9, 2022)
1023	Decision Granting Institution of *Inter Partes* Review of U.S. Patent No. 7,619,912 (Oct. 19, 2022)
1024	Patent Owner's Request for Rehearing of Decision Granting Institution of *Inter Partes* Review of U.S. Patent No. 7,619,912 (Nov. 2, 2022)
1025	Order of *Sua Sponte* Director Review of Decision Granting Institution of *Inter Partes* Review of U.S. Patent No. 7,619,912 (Jan. 5, 2023)
1026	U.S. Patent No. 7,864,627 (issued Jan. 4, 2011)
1027	Decision on Appeal of Reexamination of '627 Patent (May 30, 2016); Decision Under 37 C.F.R. § 41.77(f) (May 31, 2018)
1028	Reexamination Certificate for '627 Patent (Nov. 5, 2018)
1029	U.S. Patent No. 8,756,364 (issued June 17, 2014)
1030	IPR2017-00549 Final Written Decision ('364 Patent) (May 3, 2018)
1031	IPR Certificate for '364 Patent (May 26, 2020)
1032	U.S. Patent No. 7,532,537 (issued May 12, 2009)
1033	IPR2017-00667 Final Written Decision ('537 Patent) (July 18, 2018)

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Exhibit #	Description
1034	IPR2017-00668 Final Written Decision ('537 Patent) (July 18, 2018)
1035	IPR Certificate for '537 Patent (Apr. 27, 2020)
1036	U.S. Patent No. 7,636,274 (issued Dec. 22, 2009)
1037	Decision on Appeal of Reexamination of '274 Patent (May 9, 2017)
1038	Reexamination Certificate for '274 Patent (Nov. 5, 2018)
1039	U.S. Patent No. 7,881,150 (issued Feb. 1, 2011)
1040	IPR2014-00882 Final Written Decision on Remand ('150 Patent) (March 29, 2018)
1041	IPR2014-01011 Final Written Decision on Remand ('150 Patent) (March 29, 2018)
1042	IPR2015-01020 Final Written Decision ('150 Patent) (Sept. 28, 2016)
1043	IPR Certificate for '150 Patent (Mar. 6, 2019)
1044	File History of U.S. Patent No. 7,916,574 (filed Nov. 29, 2010)
1045	U.S. Patent No. 7,916,574 (issued Mar. 29, 2011)
1046	U.S. Patent No. 8,081,536 (issued Dec. 20, 2011)
1047	IPR2014-00883 Final Written Decision on Remand ('536 Patent) (March 29, 2018)
1048	IPR2015-01021 Final Written Decision ('536 Patent) (Sept. 28, 2016)
1049	IPR Certificate for '536 Patent (Mar. 11, 2019)
1050	File History of U.S. Patent No. 8,516,188 (filed Nov. 1, 2011)
1051	U.S. Patent No. 8,516,188 (issued Aug. 20, 2013)

Exhibit #	Description
1052	File History of U.S. Patent No. 9,037,774 (filed Aug. 20, 2013)
1053	U.S. Patent No. 9,037,774 (issued May 19, 2015)
1054	File History of U.S. Patent No. 10,489,314 (filed Dec. 28, 2017)
1055	U.S. Patent No. 10,489,314 (issued Nov. 26, 2019)
1056	Decisions Granting Institution of *Inter Partes* Reviews of U.S. Patent No. 10,489,314 (Nov. 1, 2022)
1057	File History of U.S. Patent No. 11,093,417 (filed Nov. 25, 2019)
1058	U.S. Patent No. 11,093,417 (issued Aug. 17, 2021)
1059	File History of U.S. Patent Application No. 17/403,832 (filed Aug. 16, 2021)
1060	JEDEC JESD79 standard for DDR SDRAM (June 2000)
1061	[intentionally omitted]
1062	JEDEC JESD21-C design specification for DDR SDRAM Registered DIMM (January 2002)
1063	[intentionally omitted]
1064	JEDEC JESD79-2 standard for DDR2 SDRAM (Sept. 2003)
1065	Declaration of Julie Carlson (JESD79-2)
1066	JEDEC JESD21-C design specification for DDR2 SDRAM Registered DIMM, Rev. 3.2 (Oct. 4, 2005)
1067	[intentionally omitted]
1068	Harold S. Stone, Microcomputer Interfacing (1982)
1069	Bruce Jacob, *Synchronous DRAM Architectures, Organizations, and Alternative Technologies* (Dec. 10, 2002)

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Exhibit #	Description
1070	Bruce Jacob et al., Memory Systems: Cache, DRAM, Disk (2008)
1071	U.S. Patent No. 7,363,422 to Perego et al. (filed Jan. 28, 2004)
1072	U.S. Patent No. 7,155,627 to Matsui (filed Aug. 22, 2003)
1073	U.S. Patent Application Publication No. 2006/0277355 to Ellsberry et al. (filed June 1, 2005)
1074	IPR2018-00362 Final Written Decision (June 27, 2019) ('907 Patent)
1075	U.S. Patent No. 9,606,907 (all claims cancelled)
1076	Decision Granting Institution of *Inter Partes* Review of U.S. Patent No. 10,949,339 (Oct. 19, 2022) (child of U.S. Patent No. 9,606,907, Exhibit 1075)
1077	U.S. Patent Application Publication No. 2002/0112119 to Halbert et al. (published Aug. 15, 2002)
1078	U.S. Patent No. 7,024,518 to Halbert et al. (filed Mar. 13, 2002)
1079	U.S. Patent Application Publication No. 2006/0117152 to Amidi et al. (filed Jan. 5, 2004)
1080	U.S. Patent No, 8,250,295 to Amidi et al. (filed Jan. 5, 2004)
1081	U.S. Patent. No. 5,513,135 to Dell et al. (issued Apr. 30, 1996)
1082	U.S. Patent Application Publication No. 2003/0039151 to Matsui (published Feb. 27, 2003)
1083	[intentionally omitted]
1084	[intentionally omitted]
1085	Amended Complaint in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. filed Aug. 15, 2022)
1086	Waiver of Service in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. filed Aug. 31, 2022)

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Exhibit #	Description
1087	[intentionally omitted]
1088	Amended Complaint in *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:22-cv-00294 (E.D. Tex. filed Aug. 15, 2022)
1089	Micron's Answer in *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:22-cv-00294 (E.D. Tex. filed Sept. 7, 2022)
1090	[intentionally omitted]
1091	*Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation* (June 21, 2022)
1092	Federal Court Management Statistics (Mar. 31, 2022), *available at* <https://www.uscourts.gov/statistics/table/na/federal-court-management-statistics/2022/03/31-1>

CLAIM LISTING

Ref. #	Listing of Challenged Claims
1.a.1	A memory module
1.a.2	operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller,
1.a.3	the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst,
1.a.4	the memory module comprising:
1.b	a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;
1.c	a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command;
1.d.1	a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank,
1.d.2	wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and
1.d.3	wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command;
1.e	a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus; and

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Ref. #	Listing of Challenged Claims
1.f.1	logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer,
1.f.2	wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.
2	The memory module of claim 1, wherein the buffer is configured to isolate both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory controller.
3	The memory module of claim 1, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.
4	The memory module of claim 1, further comprising an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits.
5	The memory module of claim 1, wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits.
6	The memory module of claim 1, further comprising determining a latency value, wherein the communication of the first data burst between the at least one first memory integrated circuit and the memory controller is enabled in accordance with the latency value.

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Ref. #	Listing of Challenged Claims
7	The memory module of claim 1, wherein the memory module is further coupled to the memory controller using an on-die-termination (ODT) bus, wherein each of the plurality of memory devices includes an ODT circuit, the memory module further comprising a termination circuit external to any of the plurality of memory devices, wherein the termination circuit is coupled to the ODT bus and to the ODT circuit of at least one of the plurality of memory devices, wherein the termination circuit is configured to provide external termination of the at least one of the plurality of memory devices in response to an ODT signal on the ODT bus, and wherein the ODT circuit in the at least one of the plurality of memory devices is disabled.
8	The memory module of claim 1, wherein the buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the first data burst or the second data burst through the buffer.
9	The memory module of claim 1, wherein the first memory command includes at least one first chip select signal and the second memory command includes at least one second chip select signal.
10	The memory module of claim 9, wherein the memory module produces at least third and fourth chip select signals in response to the first memory command, the third chip select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the fourth chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.

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Ref. #	Listing of Challenged Claims
11	The memory module of claim 10, wherein the memory module produces at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first [sic: second] memory command, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an active value to cause the at least one second memory integrated circuit to receive or output data signals in response to the second memory command.
12	The memory module of claim 1, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory bus, and wherein the buffer is configured to prevent the first burst of data strobe signals and the second burst of data strobe signals from colliding with each other.
13	The memory module of claim 12, wherein each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval, and wherein the buffer is configured to combine the first burst of data strobe signals and the second burst of data strobe signals into a combined burst of data strobe signals that does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals.
14	The memory module of claim 1, wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is selected to communicate data with the memory controller.

Ref. #	Listing of Challenged Claims
15	The memory module of claim 14, the at least one of the circuit components is configured to provide the first data path in response to the first control signals, and is configured to provide the second data path in response to the second control signals.
16	The memory module of claim 1, wherein the logic is configured to enable the communication of the first data burst between the at least one first memory integrated circuit and the memory controller in accordance with a latency value.
17	The memory module of claim 16, wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the first data burst through the buffer.
18	The memory module of claim 16, wherein the logic is further configured to determine the latency value.
19	The memory module of claim 16, wherein the logic is further configured to enable the communication of the second data burst between the at least one second memory integrated circuit and the memory controller in accordance with the latency value.
20	The memory module of claim 19, wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the second data burst through the buffer.
21.a	A method of operating a memory module coupled to a memory controller via a memory bus, the memory module comprising memory integrated circuits arranged in ranks and mounted on a printed circuit board having a plurality of edge connections coupled to the memory bus, the memory integrated circuits including at least one first memory integrated circuit in a first rank and at least one second memory integrated circuit in a second rank, the method comprising:
21.b	receiving at one or more circuits coupled to the printed circuit board a first set of input command and address signals representing a first memory command from the memory controller via the memory bus, the first memory command to cause the memory module to receive or output a first data burst;

Ref. #	Listing of Challenged Claims
21.c	generating a first set of output command and address signals in response to the first set of input command and address signals, the first set of output command and address signals selecting the first rank to receive or output the first data burst;
21.d	receiving at the one or more circuits a second set of input command and address signals representing a second memory command from the memory controller via the memory bus, the second memory command to cause the memory module to receive or output a second data burst;
21.e	generating a second set of output command and address signals in response to the second set of input command and address signals, the second set of output command and address signals selecting the second rank to receive or output the second data burst;
21.f	in response to the first memory command, providing first control signals to a buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer; and
21.g	in response to the second memory command, providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.
22	The method of claim 21, further comprising isolating the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory system.

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Ref. #	Listing of Challenged Claims
23	The method of claim 21, wherein the first set of input command and address signals include at least one input chip-select signal, the method further comprising generating a first chip select signal and a second chip select signal in response to the first set of input command and address signals, the first chip-select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the second chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.
24	The method of claim 21, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of the memory integrated circuits.
25	The method of claim 21, further comprising reporting an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of the memory integrated circuits.
26	The method of claim 21, wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is caused to communicate data with the memory controller.
27	The method of claim 21, wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits.

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Ref. #	Listing of Challenged Claims
28	The method of claim 21, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein the memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory bus, the method further comprising combining the first burst of data strobe signals and the second burst of data strobes to form a third burst of data strobe signals on the memory bus.
29	The method of claim 28, wherein each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval, and wherein the third burst of data strobes does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals.

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