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The following enclosures are transmitted herewith to be filed in the patent application of:

Inventor(s): Not yet named

APPLICATION ELEMENTS:

(X) Specification in thirty-two (32) pages;

(X) Drawings in eleven (11) sheets; and

(X) A return prepaid postcard.

Reference to prior domestic applications is made in the:

(X) Reference to prior domestic applications is made in the specification.

CONTINUITY INFORMATION:

Application	Relationship	Parent App. No.	Filing Date	Status
This Application	Claims Benefit of	60/550,668	03/05/04	N/A
This Application	Claims Benefit of	60/575,595	05/28/04	N/A
This Application	Claims Benefit of	60/590,038	07/21/04	N/A

(X) Incorporation by Reference. The entire disclosure of the prior applications is considered a part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

FILING FEES:

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I hereby certify that the accompanying

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Bruce S. Itchkawitz

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HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS

Claim of Priority

[0001] This application claims the benefit of U.S. Provisional Application No. 60/550,668, filed March 5, 2004, U.S. Provisional Application No. 60/575,595, filed May 28, 2004, and U.S. Provisional Application No. 60/590,038, filed July 21, 2004, each of which is incorporated in its entirety by reference herein.

Background of the Invention

Field of the Invention

[0002] The present invention relates generally to memory modules comprising a plurality of memory components or integrated circuits, and more particularly, to configurations of the memory components of the memory module.

Description of the Related Art

[0003] Memory modules typically comprise a plurality of memory components, such as dynamic random-access memory (DRAM) integrated circuits or devices, mounted on a printed circuit board (PCB). Memory modules typically have a memory configuration with a unique combination of rows, columns, and banks which result in a total memory capacity for the memory module.

[0004] For example, a 512-Megabyte memory module (termed a "512-MB" memory module, which actually has 2^{29} or 536,870,912 bytes of capacity) will typically utilize eight 512-Megabit DRAM devices (each identified as a "512-Mb" DRAM device, each actually having 2^{29} or 536,870,912 bits of capacity). The memory cells (or memory locations) of each 512-Mb DRAM device can be arranged in four banks, with each bank having an array of 2^{24} (or 16,777,216) memory locations arranged as 2^{13} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 64M 8-bit-wide memory locations (actually with four banks of 2^{27} or 134,217,728 one-bit memory cells arranged to provide a total of 2^{26} or 67,108,864 memory locations with 8 bits each) are identified as having a "64Mb x 8" or "64M x 8-bit" configuration, or as having a depth of 64M and a bit width of 8. Furthermore, certain commercially-available 512-MB

memory modules are termed to have a "64M x 8-byte" configuration or a "64M x 64-bit" configuration with a depth of 64M and a width of 8 bytes or 64 bits.

[0005] Similarly, a 1-Gigabyte memory module (termed a "1-GB" memory module, which actually has 2^{30} or 1,073,741,824 bytes of capacity) can utilize eight 1-Gigabit DRAM devices (each identified as a "1-Gb" DRAM device, each actually having 2^{30} or 1,073,741,824 bits of capacity). The memory locations of each 1-Gb DRAM device can be arranged in four banks, with each bank having an array of memory locations with 2^{14} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 128M 8-bit-wide memory locations (actually with a total of 2^{27} or 134,217,728 memory locations with 8 bits each) are identified as having a "128Mb x 8" or "128M x 8-bit" configuration, or as having a depth of 128M and a bit width of 8. Furthermore, certain commercially-available 1-GB memory modules are identified as having a "128M x 8-byte" configuration or a "128M x 64-bit" configuration with a depth of 128M and a width of 8 bytes or 64 bits.

[0006] The commercially-available 512-MB (64M x 8-byte) memory modules and the 1-GB (128M x 8-byte) memory modules described above are typically used in computer systems (e.g., personal computers) which perform graphics applications since such "x 8" configurations are compatible with data mask capabilities often used in such graphics applications. Conversely, memory modules with "x 4" configurations are typically used in computer systems such as servers which are not as graphics-intensive. Examples of such commercially available "x 4" memory modules include, but are not limited to, 512-MB (128M x 4-byte) memory modules comprising eight 512-Mb (128Mb x 4) memory components.

Summary of the Invention

[0007] In certain embodiments, a memory module comprises a plurality of memory components. Each memory component has a first bit width. The plurality of memory components are configured as one or more pairs of memory components. Each pair of memory components simulates a single virtual memory component having a second bit width which is twice the first bit width.

[0008] In certain embodiments, a memory module comprises a first memory component having a first data strobe pin. The memory module further comprises a second memory component having a second data strobe pin. The memory module further comprises a first resistor electrically coupled to the first data strobe pin. The memory module further comprises a second resistor electrically coupled to the second data strobe pin and to the first resistor. The first data strobe pin is electrically coupled to the second data strobe pin through the first resistor and through the second resistor.

[0009] In certain embodiments, a memory module comprises a termination bus. The memory module further comprises a first memory component having a first data strobe pin, a first termination signal pin electrically coupled to the termination bus, a first termination circuit, and at least one data pin. The first termination circuit selectively electrically terminates the first data strobe pin and the first data pin in response to a first signal received by the first termination signal pin from the termination bus. The memory module further comprises a second memory component having a second data strobe pin electrically coupled to the first data strobe pin, a second termination signal pin, a second termination circuit, and at least one data pin. The second termination signal pin is electrically coupled to a voltage. The second termination circuit is responsive to the voltage by not terminating the second data strobe pin or the second data pin. The memory module further comprises at least one termination assembly having a third termination signal pin, a third termination circuit, and at least one termination pin electrically coupled to the data pin of the second memory component. The third termination signal pin is electrically coupled to the termination bus. The third termination circuit selectively electrically terminates the data pin of the second memory component through the termination pin in response to a second signal received by the third termination signal pin from the termination bus.

[0010] In certain embodiments, a memory module comprises a pair of substantially identical memory components. Each memory component has a first bit width, a first number of banks of memory locations, a first number of row address bits, and a first number of column address bits. The memory module further comprises a serial-presence-detect (SPD) device comprising data that characterizes the pair of memory components as a virtual memory component having a second bit width equal to twice the first bit width, a

second number of banks of memory locations equal to the first number of banks, a second number of row address bits equal to the first number of row address bits, and a second number of column address bits equal to the first number of column address bits.

[0011] In certain embodiments, a memory module has a first memory capacity. The memory module comprises a plurality of substantially identical memory components configured as a first rank and a second rank. The memory components of the first rank are configured in pairs with their respective data strobe pins tied together. The memory components of the second rank are configured in pairs with their respective data strobe pins tied together. The memory module further comprises a logic element which receives a first set of address and control signals compatible with a second memory capacity. The second memory density is substantially equal to one-half of the first memory capacity. The logic element translates the first set of address and control signals into a second set of address and control signals compatible with the first memory capacity of the memory module. The logic element transmits the second set of address and control signals to the first rank and the second rank.

[0012] In certain embodiments, a memory module has a first plurality of memory locations with a first memory density. The memory module comprises a plurality of substantially identical memory components configured as a first rank, a second rank, a third rank, and a fourth rank. The memory module further comprises a logic element which receives a first set of address and control signals compatible with a second plurality of memory locations having a second memory density. The second memory density is substantially equal to one-half of the first memory density. The logic element translates the first set of address and control signals into a second set of address and control signals compatible with the first plurality of memory locations of the memory module. The logic element transmits the second set of address and control signals to the first rank, the second rank, the third rank, and the fourth rank.

Brief Description of the Drawings

[0013] Figure 1 schematically illustrates an exemplary memory module in which a data strobe (DQS) pin of a first memory component is electrically connected to a DQS pin of a second memory component while both DQS pins are active.

[0014] Figure 2 is an exemplary timing diagram of the voltages applied to the two DQS pins due to non-simultaneous switching.

[0015] Figure 3 schematically illustrates another exemplary memory module in which a DQS pin of a first memory component is connected to a DQS pin of a second memory component.

[0016] Figure 4 schematically illustrates an exemplary memory module in accordance with certain embodiments described herein.

[0017] Figures 5A and 5B schematically illustrate a first side and a second side, respectively, of a memory module with eighteen 64M x 4 bit, DDR-1 SDRAM FBGA memory components on each side of a 184-pin glass-epoxy printed circuit board.

[0018] Figures 6A and 6B schematically illustrate an exemplary embodiment of a memory module in which a first resistor and a second resistor are used to reduce the current flow between the first DQS pin and the second DQS pin.

[0019] Figure 7 schematically illustrates another exemplary memory module compatible with certain embodiments described herein.

[0020] Figure 8 schematically illustrates a particular embodiment of the memory module schematically illustrated by Figure 7.

[0021] Figure 9 schematically illustrates another exemplary memory module in accordance with certain embodiments described herein.

[0022] Figure 10A schematically illustrates an exemplary memory module which doubles the rank density in accordance with certain embodiments described herein.

[0023] Figure 10B schematically illustrates an exemplary logic element compatible with certain embodiments described herein.

[0024] Figure 11A schematically illustrates an exemplary memory module which doubles the number of ranks in accordance with embodiments described herein.

[0025] Figure 11B schematically illustrates another exemplary logic element compatible with certain embodiments described herein.

Detailed Description of Exemplary Embodiments

[0026] Most high-density memory modules are currently built with 512-Megabit ("512-Mb") memory components wherein each memory component has a 64M x 8-bit

configuration. For example, a 1-Gigabyte ("1-GB") memory module with error checking capabilities can be fabricated using eighteen such 512-Mb memory components. Alternatively, it can be economically advantageous to fabricate a 1-GB memory module using lower-density memory components and doubling the number of memory components used to produce the desired word width. For example, by fabricating a 1-GB memory module using thirty-six 256-Mb memory components with 64M x 4-bit configuration, the cost of the resulting 1-GB memory module can be reduced since the unit cost of each 256-Mb memory component is typically lower than one-half the unit cost of each 512-Mb memory component. The cost savings can be significant, even though twice as many 256-Mb memory components are used in place of the 512-Mb memory components.

[0027] Market pricing factors for DRAM devices are such that higher-density DRAM devices (e.g., 1-Gb DRAM devices) are much more than twice the price of lower-density DRAM devices (e.g., 512-Mb DRAM devices). In other words, the price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices. This pricing difference often lasts for months or even years after the introduction of the higher-density DRAM devices, until volume production factors reduce the costs of the newer higher-density DRAM devices. Thus, when the cost of a higher-density DRAM device is more than the cost of two lower-density DRAM devices, there is an economic incentive for utilizing pairs of the lower-density DRAM devices to replace individual higher-density DRAM devices.

[0028] For proper operation, the computer system advantageously recognizes the 1-GB memory module comprising the 256-Mb memory components with 64M x 4-bit configuration as a 1-GB memory module having 512-Mb memory components with 64M x 8-bit configuration (e.g., as a 1-GB memory module with 128M x 8-byte configuration). This advantageous result would desirably be achieved by electrically connecting together two output signal pins (e.g., DQS or data strobe pins) of the two 256-Mb memory components such that both output signal pins are concurrently active when the two memory components are concurrently enabled. The DQS or data strobe is a bi-directional signal that is used during both read cycles and write cycles to validate or latch data. As used herein, the terms "tying together" or "tied together" refer to a configuration in which

corresponding pins (e.g., DQS pins) of two memory components are electrically connected together and are concurrently active when the two memory components are concurrently enabled (e.g., by a common chip-select or CS signal). Such a configuration is different from standard memory module configurations in which the output signal pins (e.g., DQS pins) of two memory components are electrically coupled to the same source, but these pins are not concurrently active since the memory components are not concurrently enabled. However, a general guideline of memory module design warns against tying together two output signal pins in this way.

[0029] Figures 1 and 2 schematically illustrate a problem which may arise from tying together two output signal pins. Figure 1 schematically illustrates an exemplary memory module 5 in which a first DQS pin 12 of a first memory component 10 is electrically connected to a second DQS pin 22 of a second memory component 20. The two DQS pins 12, 22 are both electrically connected to a memory controller 30.

[0030] Figure 2 is an exemplary timing diagram of the voltages applied to the two DQS pins 12, 22 due to non-simultaneous switching. As illustrated by Figure 2, at time t_1, both the first DQS pin 12 and the second DQS pin 22 are high, so no current flows between them. Similarly, at time t_4, both the first DQS pin 12 and the second DQS pin 22 are low, so no current flows between them. However, for times between approximately t_2 and approximately t_3, the first DQS pin 12 is low while the second DQS pin 22 is high. Under such conditions, a current will flow between the two DQS pins 12, 22. This condition in which one DQS pin is low while the other DQS pin is high can occur for fractions of a second (e.g., 0.8 nanoseconds) during the dynamic random-access memory (DRAM) read cycle. During such conditions, the current flowing between the two DQS pins 12, 22 can be substantial, resulting in heating of the memory components 10, 20, and contributing to the degradation of reliability and eventual failure of these memory components.

[0031] A second problem may also arise from tying together two output signal pins. Figure 3 schematically illustrates another exemplary memory module 5 in which a first DQS pin 12 of a first memory component 10 is electrically connected to a second DQS pin 14 of a second memory component 20. The two DQS pins 12, 14 of Figure 3 are both electrically connected to a memory controller (not shown). The DQ (data input/output) pin

22 of the first memory component 10 and the corresponding DQ pin 24 of the second memory component 20 are each electrically connected to the memory controller by the DQ bus (not shown). Typically, each memory component 10, 20 will have a plurality of DQ pins (e.g., eight DQ pins per memory component), but for simplicity, Figure 3 only shows one DQ pin for each memory component 10, 20.

[0032] Each of the memory components 10, 20 of Figure 3 utilizes a respective on-die termination or "ODT" circuit 32, 34 which has termination resistors (e.g., 75 ohms) internal to the memory components 10, 20 to provide signal termination. Each memory component 10, 20 has a corresponding ODT signal pin 62, 64 which is electrically connected to the memory controller via an ODT bus 40. The ODT signal pin 62 of the first memory component 10 receives a signal from the ODT bus 40 and provides the signal to the ODT circuit 32 of the first memory component 10. The ODT circuit 32 responds to the signal by selectively enabling or disabling the internal termination resistors 52, 56 of the first memory component 10. This behavior is shown schematically in Figure 3 by the switches 42, 44 which are either closed (dash-dot line) or opened (solid line). The ODT signal pin 64 of the second memory component 20 receives a signal from the ODT bus 40 and provides the signal to the ODT circuit 34 of the second memory component 20. The ODT circuit 34 responds to the signal by selectively enabling or disabling the internal termination resistors 54, 58 of the second memory component 20. This behavior is shown schematically in Figure 3 by the switches 46, 48 which are either closed (dash-dot line) or opened (solid line). The switches 42, 44, 46, 48 of Figure 3 are schematic representations of the operation of the ODT circuits 32, 34, and do not signify that the ODT circuits 32, 34 necessarily include mechanical switches.

[0033] Examples of memory components 10, 20 which include such ODT circuits 32, 34 include, but are not limited to, DDR-2 memory components. Such memory components are configured to selectively enable or disable the termination of the memory component in this way in response to signals applied to the ODT signal pin of the memory component. For example, when the ODT signal pin 62 of the first memory component 10 is pulled high, the termination resistors 52, 56 of the first memory component 10 are enabled. When the ODT signal pin 62 of the first memory component 10 is pulled low (e.g.,

grounded), the termination resistors 52, 56 of the first memory component 10 are disabled. By selectively disabling the termination resistors of an active memory component, while leaving the termination resistors of inactive memory components enabled, such configurations advantageously preserve signal strength on the active memory component while continuing to eliminate signal reflections at the bus-die interface of the inactive memory components.

[0034] In certain configurations, as schematically illustrated by Figure 3, the DQS pins 12, 14 of each memory component 10, 20 are selectively connected to a voltage VTT through a corresponding termination resistor 52, 54 internal to the corresponding memory component 10, 20. Similarly, in certain configurations, as schematically illustrated by Figure 3, the DQ pins 22, 24 are selectively connected to a voltage VTT through a corresponding termination resistor 56, 58 internal to the corresponding memory component 10, 20. In certain configurations, rather than being connected to a voltage VTT, the DQ pins 12, 14 and/or the DQS pins 22, 24 are selectively connected to ground through the corresponding termination resistors 52, 54, 56, 58. The resistances of the internal termination resistors 52, 54, 56, 58 are selected to clamp the voltages so as to reduce the signal reflections from the corresponding pins. In the configuration schematically illustrated by Figure 3, each internal termination resistor 52, 54, 56, 58 has a resistance of approximately 75 ohms.

[0035] When connecting the first memory component 10 and the second memory component 20 together to form a double word width, both the first memory component 10 and the second memory component 20 are enabled at the same time (e.g., by a common CS signal). Connecting the first memory component 10 and the second memory component 20 by tying the DQS pins 12, 14 together, as shown in Figure 3, results in a reduced effective termination resistance for the DQS pins 12, 14. For example, for the exemplary configuration of Figure 3, the effective termination resistance for the DQS pins 12, 14 is approximately 37.5 ohms, which is one-half the desired ODT resistance (for 75-ohm internal termination resistors) to reduce signal reflections since the internal termination resistors 52, 54 of the two memory components 10, 20 are connected in parallel. This reduction in the termination resistance can result in signal reflections causing the memory component to malfunction.

[0036] Figure 4 schematically illustrates an exemplary memory module 100 in accordance with certain embodiments described herein. The memory module 100 comprises a first memory component 110 having a first data strobe (DQS) pin 112 and a second memory component 120 having a second data strobe (DQS) pin 122. The memory module 100 further comprises a first resistor 130 electrically coupled to the first DQS pin 112. The memory module 100 further comprises a second resistor 140 electrically coupled to the second DQS pin 122 and to the first resistor 130. The first DQS pin 112 is electrically coupled to the second DQS pin 122 through the first resistor 130 and through the second resistor 140.

[0037] Various types of memory modules 100 are compatible with embodiments described herein having the first resistor 130 and the second resistor 140. For example, memory modules 100 having memory capacities of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, as well as other capacities, are compatible with embodiments described herein. In addition, memory modules 100 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. Furthermore, memory modules 100 compatible with embodiments described herein include, but are not limited to, single in-line memory modules (SIMMs), dual in-line memory modules (DIMMs), small-outline DIMMs (SO-DIMMs), unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), mini-DIMMs, and micro-DIMMs.

[0038] Memory components 110, 120 compatible with embodiments described herein, including but not limited to, random-access memory (RAM), dynamic random-access memory (DRAM), synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., DDR-1, DDR-2, DDR-3). In addition, memory components having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein. Memory components 110, 120 compatible with embodiments described herein have packaging which include but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP). Memory components compatible with embodiments described herein are available from a number of sources, including but not limited to, Samsung Semiconductor,

Inc. of San Jose, California, Infineon Technologies AG of San Jose, California, and Micron Technology, Inc. of Boise, Idaho.

[0039] In certain embodiments, the memory module 100 is a 1-GB unbuffered Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) high-density dual in-line memory module (DIMM). Figures 5A and 5B schematically illustrate a first side 162 and a second side 164, respectively, of such a memory module 100 with eighteen 64M x 4-bit, DDR-1 SDRAM FBGA memory components on each side of a 184-pin glass-epoxy printed circuit board (PCB) 160. In certain embodiments, the memory module 100 further comprises a phase-lock-loop (PLL) clock driver 170, an EEPROM for serial-presence detect (SPD) data 180, and decoupling capacitors (not shown) mounted on the PCB in parallel to suppress switching noise on VDD and VDDQ power supply for DDR-1 SDRAM. By using synchronous design, such memory modules 100 allow precise control of data transfer between the memory module 100 and the system controller. Data transfer can take place on both edges of the DQS signal at various operating frequencies and programming latencies. Therefore, certain such memory modules 100 are suitable for a variety of high-performance system applications.

[0040] In certain embodiments, the memory module 100 comprises a plurality of memory components configured in pairs, each pair having a first memory component 110 and a second memory component 120. For example, in certain embodiments, a 128M x 72-bit DDR SDRAM high-density memory module 100 comprises thirty-six 64M x 4-bit DDR-1 SDRAM integrated circuits in FBGA packages configured in eighteen pairs. The first memory component 110 of each pair has the first DQS pin 112 electrically coupled to the second DQS pin 122 of the second memory component 120 of the pair. In addition, the first DQS pin 112 and the second DQS pin 122 are concurrently active when the first memory component 110 and the second memory component 120 are concurrently enabled.

[0041] In certain embodiments, the first resistor 130 and the second resistor 140 each has a resistance advantageously selected to reduce the current flow between the first DQS pin 112 and the second DQS pin 122 while allowing signals to propagate between the memory controller and the DQS pins 112, 122. In certain embodiments, each of the first resistor 130 and the second resistor 140 has a resistance in a range between approximately 5

ohms and approximately 50 ohms. For example, in certain embodiments, each of the first resistor 130 and the second resistor 140 has a resistance of approximately 22 ohms. Other resistance values for the first resistor 130 and the second resistor 140 are also compatible with embodiments described herein. In certain embodiments, the first resistor 130 comprises a single resistor, while in other embodiments, the first resistor 130 comprises a plurality of resistors electrically coupled together in series and/or in parallel. Similarly, in certain embodiments, the second resistor 140 comprises a single resistor, while in other embodiments, the second resistor 140 comprises a plurality of resistors electrically coupled together in series and/or in parallel.

[0042] Figures 6A and 6B schematically illustrate an exemplary embodiment of a memory module 100 in which the first resistor 130 and the second resistor 140 are used to reduce the current flow between the first DQS pin 112 and the second DQS pin 122. As schematically illustrated by Figure 6A, the memory module 100 is part of a computer system 200 having a memory controller 210. The first resistor 130 has a resistance of approximately 22 ohms and the second resistor 140 has a resistance of approximately 22 ohms. The first resistor 130 and the second resistor 140 are electrically coupled in parallel to the memory controller 210 through a signal line 220 having a resistance of approximately 25 ohms. The first resistor 130 and the second resistor 140 are also electrically coupled in parallel to a source of a fixed termination voltage (identified by VTT in Figures 6A and 6B) by a signal line 240 having a resistance of approximately 47 ohms. Such an embodiment can advantageously be used to allow two memory components having lower bit widths (e.g., 4-bit) to behave as a single virtual memory component having a higher bit width (e.g., 8-bit).

[0043] Figure 6B schematically illustrates exemplary current-limiting resistors 130, 140 in conjunction with the impedances of the memory components 110, 120. During an exemplary portion of a data read operation, the memory controller 210 is in a high-impedance condition, the first memory component 110 drives the first DQS pin 112 high (e.g., 2.7 volts), and the second memory component 120 drives the second DQS pin 122 low (e.g., 0 volts). The amount of time for which this condition occurs is approximated by the time between t_2 and t_3 of Figure 2, which in certain embodiments is approximately twice the tDQSQ (data strobe edge to output data edge skew time, e.g., approximately

0.8 nanoseconds). At least a portion of this time in certain embodiments is caused by simultaneous switching output (SSO) effects.

[0044] In certain embodiments, as schematically illustrated by Figure 6B, the DQS driver of the first memory component 110 has a driver impedance R_1 of approximately 17 ohms, and the DQS driver of the second memory component 120 has a driver impedance R_4 of approximately 17 ohms. Because the upper network of the first memory component 110 and the first resistor 130 (with a resistance R_2 of approximately 22 ohms) is approximately equal to the lower network of the second memory component 120 and the second resistor 140 (with a resistance R_3 of approximately 22 ohms), the voltage at the midpoint is approximately $0.5 * (2.7 - 0) = 1.35$ volts, which equals VTT, such that the current flow across the 47-ohm resistor of Figure 6B is approximately zero.

[0045] The voltage at the second DQS pin 122 in Figure 6B is given by $V_{DQS2} = 2.7 * R_4/(R_1+R_2+R_3+R_4) = 0.59$ volts and the current flowing through the second DQS pin 122 is given by $I_{DQS2} = 0.59 / R_4 = 34$ milliamps. The power dissipation in the DQS driver of the second memory component 120 is thus $P_{DQS2} = 34 \text{ mA} * 0.59 \text{ V} = 20$ milliwatts. In contrast, without the first resistor 130 and the second resistor 140, only the 17-ohm impedances of the two memory components 110, 120 would limit the current flow between the two DQS pins 112, 122, and the power dissipation in the DQS driver of the second memory component 120 would be approximately 107 milliwatts. Therefore, the first resistor 130 and the second resistor 140 of Figures 6A and 6B advantageously limit the current flowing between the two memory components during the time that the DQS pin of one memory component is driven high and the DQS pin of the other memory component is driven low.

[0046] In certain embodiments in which there is overshoot or undershoot of the voltages, the amount of current flow can be higher than those expected for nominal voltage values. Therefore, in certain embodiments, the resistances of the first resistor 130 and the second resistor 140 are advantageously selected to account for such overshoot/undershoot of voltages.

[0047] For certain such embodiments in which the voltage at the second DQS pin 122 is $V_{DQS2} = 0.59$ volts and the duration of the overdrive condition is approximately

0.8 nanoseconds at maximum, the total surge is approximately 0.59 V * 1.2 ns = 0.3 V-ns. For comparison, the JEDEC standard for overshoot/undershoot is 2.4 V-ns, so certain embodiments described herein advantageously keep the total surge within predetermined standards (e.g., JEDEC standards).

[0048] Figure 7 schematically illustrates another exemplary memory module 300 compatible with certain embodiments described herein. The memory module 300 comprises a termination bus 305. The memory module 300 further comprises a first memory component 310 having a first data strobe pin 312, a first termination signal pin 314 electrically coupled to the termination bus 305, a first termination circuit 316, and at least one data pin 318. The first termination circuit 316 selectively electrically terminating the first data strobe pin 312 and the first data pin 318 in response to a first signal received by the first termination signal pin 314 from the termination bus 305. The memory module 300 further comprises a second memory component 320 having a second data strobe pin 322 electrically coupled to the first data strobe pin 312, a second termination signal pin 324, a second termination circuit 326, and at least one data pin 328. The second termination signal pin 324 is electrically coupled to a voltage, wherein the second termination circuit 326 is responsive to the voltage by not terminating the second data strobe pin 322 or the second data pin 328. The memory module 300 further comprises at least one termination assembly 330 having a third termination signal pin 334, a third termination circuit 336, and at least one termination pin 338 electrically coupled to the data pin 328 of the second memory component 320. The third termination signal pin 334 is electrically coupled to the termination bus 305. The third termination circuit 336 selectively electrically terminates the data pin 328 of the second memory component 320 through the termination pin 338 in response to a second signal received by the third termination signal pin 334 from the termination bus 305.

[0049] Various types of memory modules 300 are compatible with embodiments described herein having the termination assembly 330 which provides termination to the data pin 328 of the second memory component 320. For example, memory modules 300 having memory capacities of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, as well as other capacities, are compatible with embodiments described herein. In addition, memory modules 300 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as

other widths (in bytes or in bits), are compatible with embodiments described herein. Furthermore, memory modules 300 compatible with embodiments described herein include, but are not limited to, single in-line memory modules (SIMMs), dual in-line memory modules (DIMMs), small-outline DIMMs (SO-DIMMs), unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), mini-DIMMs, and micro-DIMMs.

[0050] Memory components 310, 320 compatible with embodiments described herein, including but not limited to, random-access memory (RAM), dynamic random-access memory (DRAM), synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., DDR-1, DDR-2, DDR-3). In addition, memory components having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein. Memory components 310, 320 compatible with embodiments described herein have packaging which include but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP). Memory components compatible with embodiments described herein are available from a number of sources, including but not limited to, Samsung Semiconductor, Inc. of San Jose, California, Infineon Technologies AG of San Jose, California, and Micron Technology, Inc. of Boise, Idaho.

[0051] Figure 8 schematically illustrates a particular embodiment of the memory module 300 schematically illustrated by Figure 7. The memory module 300 comprises an on-die termination (ODT) bus 305. The memory module 300 comprises a first memory component 310 having a first data strobe (DQS) pin 312, a first ODT signal pin 314 electrically coupled to the ODT bus 305, a first ODT circuit 316, and at least one data (DQ) pin 318. The first ODT circuit 316 selectively electrically terminates the first DQS pin 312 and the DQ pin 318 of the first memory component 310 in response to an ODT signal received by the first ODT signal pin 314 from the ODT bus 305. This behavior of the first ODT circuit 316 is schematically illustrated in Figure 8 by the switches 372, 376 which are selectively closed (dash-dot line) or opened (solid line).

[0052] The memory module 300 further comprises a second memory component 320 having a second DQS pin 322 electrically coupled to the first DQS pin 312, a second ODT signal pin 324, a second ODT circuit 326, and at least one DQ pin 328. The first DQS

pin 312 and the second DQS pin 322 are concurrently active when the first memory component 310 and the second memory component 320 are concurrently enabled. The second ODT signal pin 324 is electrically coupled to a voltage (e.g., ground), wherein the second ODT circuit 326 is responsive to the voltage by not terminating the second DQS pin 322 or the second DQ pin 324. This behavior of the second ODT circuit 326 is schematically illustrated in Figure 8 by the switches 374, 378 which are opened.

[0053] The memory module 300 further comprises at least one termination assembly 330 having a third ODT signal pin 334 electrically coupled to the ODT bus 305, a third ODT circuit 336, and at least one termination pin 338 electrically coupled to the DQ pin 328 of the second memory component 320. The third ODT circuit 336 selectively electrically terminates the DQ pin 328 of the second memory component 320 through the termination pin 338 in response to an ODT signal received by the third ODT signal pin 334 from the ODT bus 305. This behavior of the third ODT circuit 336 is schematically illustrated in Figure 8 by the switch 380 which is either closed (dash-dot line) or opened (solid line).

[0054] In certain embodiments, the termination assembly 330 comprises discrete electrical components which are surface-mounted or embedded on the printed-circuit board of the memory module 300. In certain other embodiments, the termination assembly 330 comprises an integrated circuit mounted on the printed-circuit board of the memory module 300. Persons skilled in the art can provide a termination assembly 330 in accordance with embodiments described herein.

[0055] Certain embodiments of the memory module 300 schematically illustrated by Figure 8 advantageously avoid the problem schematically illustrated by Figure 3 of electrically connecting the internal termination resistances of the DQS pins of the two memory components in parallel. As described above in relation to Figure 3, Figures 7 and 8 only show one DQ pin for each memory component for simplicity. Other embodiments have a plurality of DQ pins for each memory component. In certain embodiments, each of the first ODT circuit 316, the second ODT circuit 326, and the third ODT circuit 336 are responsive to a high voltage or signal level by enabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by disabling the corresponding termination resistors. In other embodiments, each of the first ODT circuit 316, the second

ODT circuit 326, and the third ODT circuit 336 are responsive to a high voltage or signal level by disabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by enabling the corresponding termination resistors. Furthermore, the switches 372, 374, 376, 378, 380 of Figure 8 are schematic representations of the enabling and disabling operation of the ODT circuits 316, 326, 336 and do not signify that the ODT circuits 316, 326, 336 necessarily include mechanical switches.

[0056] The first ODT signal pin 314 of the first memory component 310 receives an ODT signal from the ODT bus 305. In response to this ODT signal, the first ODT circuit 316 selectively enables or disables the termination resistance for both the first DQS pin 312 and the DQ pin 318 of the first memory component 310. The second ODT signal pin 324 of the second memory component 320 is tied (e.g., directly hard-wired) to the voltage (e.g., ground), thereby disabling the internal termination resistors 354, 358 on the second DQS pin 322 and the second DQ pin 328, respectively, of the second memory component 320 (schematically shown by open switches 374, 378 in Figure 8). The second DQS pin 322 is electrically coupled to the first DQS pin 312, so the termination resistance for both the first DQS pin 312 and the second DQS pin 322 is provided by the termination resistor 352 internal to the first memory component 310.

[0057] The termination resistor 356 of the DQ pin 318 of the first memory component 310 is enabled or disabled by the ODT signal received by the first ODT signal pin 314 of the first memory component 310 from the ODT bus 305. The termination resistance of the DQ pin 328 of the second memory component 320 is enabled or disabled by the ODT signal received by the third ODT signal pin 334 of the termination assembly 330 which is external to the second memory component 320. Thus, in certain embodiments, the first ODT signal pin 314 and the third ODT signal pin 334 receive the same ODT signal from the ODT bus 305, and the termination resistances for both the first memory component 310 and the second memory component 320 are selectively enabled or disabled in response thereto when these memory components are concurrently enabled. In this way, certain embodiments of the memory module 300 schematically illustrated by Figure 8 provides external or off-chip termination of the second memory component 320.

[0058] Certain embodiments of the memory module 300 schematically illustrated by Figure 8 advantageously allow the use of two lower-cost readily-available 512-Mb DDR-2 SDRAM components to provide the capabilities of a more expensive 1-GB DDR-2 SDRAM component. Certain such embodiments advantageously reduce the total cost of the resultant memory module 300.

[0059] Figure 9 schematically illustrates another exemplary memory module 400 in accordance with certain embodiments described herein. The memory module 400 comprises a pair of substantially identical memory components 410, 420. Each memory component 410, 420 has a first bit width, a first number of banks of memory locations, a first number of rows of memory locations, and a first number of columns of memory locations. The memory module 400 further comprises a serial-presence-detect (SPD) device 430 comprising data that characterizes the pair of memory components 410, 420. The data characterize the pair of memory components 410, 420 as a virtual memory component having a second bit width equal to twice the first bit width, a second number of banks of memory locations equal to the first number of banks, a second number of rows of memory locations equal to the first number of rows, and a second number of columns of memory locations equal to the first number of columns.

[0060] Table 1 provides the numbers of rows and columns for various memory components as specified by JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published February 2004, and incorporated in its entirety by reference herein.

	128-Mb	256-Mb	512-Mb	1-Gb
Number of banks	4	4	4	4
Number of row address bits	12	13	13	14
Number of column address bits for "x 4" configuration	11	11	12	12
Number of column address bits for "x 8" configuration	10	10	11	11
Number of column address bits for "x 16" configuration	9	9	10	10

As described by Table 1, 512-Mb (128M x 4-bit) DRAM devices have 2^{13} rows and 2^{12} columns of memory locations, while 1-Gb (128M x 8-bit) DRAM devices have 2^{14} rows and 2^{11} columns of memory locations. Because of the differences in the number of rows and

the number of columns for the two types of memory components, complex address translation procedures and structures would typically be needed to fabricate a 1-GB (128M x 8-byte) memory module using sixteen 512-Mb (128M x 4-bit) DRAM devices.

[0061] Certain embodiments described herein provide an apparatus and method for utilizing two lower-density (e.g., 512-Mb) memory components to simulate one higher-density (e.g., 1-Gb) memory component without utilizing address translation procedures or structures. In certain embodiments, the apparatus and method described herein are useful for memory modules comprising a plurality of memory components mounted (e.g., soldered) on a printed circuit board (PCB).

[0062] Such memory modules generally include serial-presence-detect (SPD) data stored in an SPD device, such as a serial electrically-erasable, programmable, read-only memory (EEPROM) device, mounted on the PCB. This SPD data contains relevant information on the memory module, such as the number of row addresses, the number of column addresses, and the data width of each memory component. From the SPD data, the total memory capacity of the memory module can be calculated. Upon booting a computer comprising the memory module, the SPD device provides the SPD data to the basic input/output system (BIOS). The BIOS then uses the SPD data to configure the computer memory properly for maximum reliability and performance.

[0063] For a commercially-available 512-MB (64M x 8-byte) memory module utilizing eight 512-Mb memory components each with a 64M x 8-bit configuration, as described above, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3:	Defines the number of row address bits in the DRAM device in the memory module [13 for the 512-Mb memory component].
Byte 4:	Defines the number of column address bits in the DRAM device in the memory module [11 for the 512-Mb memory component].
Byte 13:	Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 512-Mb (64M x 8-bit) memory component].
Byte 14:	Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 512-Mb (64M x 8-bit) memory component].
Byte 17:	Defines the number of banks internal to the DRAM device used in the memory module [4 for the 512-Mb memory component].

[0064] Similarly, for a commercially-available 1-GB (128M x 8-byte) memory module utilizing eight 1-Gb memory components each with a 128M x 8-bit configuration, as described above, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: Defines the number of row address bits in the DRAM device in the memory module [14 for the 1-Gb memory component].
Byte 4: Defines the number of column address bits in the DRAM device in the memory module [11 for the 1-Gb memory component].
Byte 13: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 1-Gb (128M x 8-bit) memory component].
Byte 14: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 1-Gb (128M x 8-bit) memory component].
Byte 17: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 1-Gb memory component].

[0065] In certain embodiments disclosed herein, two lower-density memory components are used to simulate one higher-density memory component. In such embodiments, the SPD device of the memory module is programmed to describe the combined pair of lower-density memory components as one virtual or pseudo-higher-density memory component.

[0066] In an exemplary embodiment, two 512-Mb memory components, each with a 128M x 4-bit configuration, are used to simulate one 1-Gb memory component having a 128M x 8-bit configuration. The SPD device of the memory module is programmed to describe the pair of 512-Mb memory components as one virtual or pseudo-1-Gb memory component.

[0067] For example, to fabricate a 1-GB (128M x 8-byte) memory module, sixteen 512-Mb (128M x 4-bit) memory components can be used. The sixteen 512-Mb (128M x 4-bit) memory components are combined in eight pairs, with each pair serving as a virtual or pseudo-1-Gb (128M x 8-bit) memory component. In such embodiments, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: 13 row address bits.
Byte 4: 12 column address bits.
Byte 13: 8 bits wide for the primary virtual 1-Gb (128M x 8-bit) memory component.

Byte 14: 8 bits wide for the error checking virtual 1-Gb (128M x 8-bit) memory component.

Byte 17: 4 banks.

[0068] In this exemplary embodiment, bytes 3, 4, and 17 are programmed to have the same values as they would have for a 512-MB (128M x 4-byte) memory module utilizing 512-Mb (128M x 4-bit) memory components. However, bytes 13 and 14 of the SPD data are programmed to be equal to 8, corresponding to the bit width of the virtual or pseudo-higher-density 1-Gb (128M x 8-bit) memory component, for a total capacity of 1-GB. Thus, the SPD data does not describe the actual-lower-density memory components, but instead describes the virtual or pseudo-higher-density memory components. The BIOS accesses the SPD data and recognizes the memory module as having 4 banks of memory locations arranged in 2^{13} rows and 2^{12} columns, with each memory location having a width of 8 bits rather than 4 bits.

[0069] Certain embodiments which utilize the SPD data as described herein also advantageously do not require hardware changes, since the configuration of the memory module is stored in software. In addition, certain embodiments described herein advantageously avoid the need for row and column steering logic circuits.

[0070] In certain embodiments, the memory density of a memory module is advantageously doubled by providing twice as many memory components as would otherwise be provided. For example, pairs of lower-density memory components can be substituted for individual higher-density memory components to reduce costs or to increase performance. As another example, twice the number of memory components can be used to produce a higher-density memory configuration of the memory module. Each of these examples can be limited by the number of chip select signals which are available from the memory controller or by the size of the memory components. Certain embodiments described herein advantageously provide a logic mechanism to overcome such limitations.

[0071] Figure 10A schematically illustrates an exemplary memory module 500 which doubles the rank density in accordance with certain embodiments described herein. The memory module 500 has a a first memory capacity. The memory module 500 comprises a plurality of substantially identical memory components 510 configured as a first rank 520 and a second rank 530. The memory components 510 of the first rank 520 are configured in

pairs with their respective DQS pins tied together, as described above. Similarly, the memory components 510 of the second rank 530 are also configured in pairs with their respective DQS pins tied together, as described above. The memory module 500 further comprises a logic element 540 which receives a first set of address and control signals from a memory controller (not shown). The first set of address and control signals is compatible with a second memory capacity substantially equal to one-half of the first memory capacity. The logic element 540 translates the first set of address and control signals into a second set of address and control signals which is compatible with the first memory capacity of the memory module 500 and which is transmitted to the first rank 520 and the second rank 530.

[0072] The first rank 520 of Figure 10A has 18 memory components 510 and the second rank 530 of Figure 10A has 18 memory components 510. Other numbers of memory components 510 in each of the ranks 520, 530 are also compatible with embodiments described herein.

[0073] In the embodiment schematically illustrated by Figure 10A, the memory module 500 has a width of 8 bytes (or 64 bits) and each of the memory components 510 of Figure 10A has a bit width of 4 bits. Other memory module widths (e.g., 4 bytes, 16 bytes, 32 bytes, or 32 bits, 128 bits, 256 bits) and other memory component bit widths (e.g., 2, 8, 16, 32) are also compatible with embodiments described herein. The 4-bit-wide ("x 4") memory components 510 have one-half the width, but twice the depth of 8-bit-wide ("x 8") memory components. Thus, each pair of "x 4" memory components 510 has the same density as a single "x 8" memory component, and pairs of "x 4" memory components 510 can be used instead of individual "x 8" memory components to provide the memory density of the memory module 500. For example, a pair of 512-Mb 128M x 4-bit memory components has the same memory density as a 1-Gb 128M x 8-bit memory component.

[0074] For two "x 4" memory components 510 to work in tandem to mimic a "x 8" memory component, the relative DQS pins of the two memory components 510 are advantageously tied together, as described above. In addition, to access the memory density of a high-density memory module 500 comprising pairs of "x 4" memory components 510, an additional address line is used. While a high-density memory module comprising individual "x 8" memory components with the next-higher density would also utilize an additional

address line, the additional address lines are different in the two memory module configurations.

[0075] For example, a 1-Gb 128M x 8-bit DDR-1 DRAM memory component uses row addresses A13-A0 and column addresses A11 and A9-A0. A pair of 512-Mb 128M x 4-bit DDR-1 DRAM memory components uses row addresses A12-A0 and column addresses A12, A11, and A9-A0. In certain embodiments, a memory controller of a computer system utilizing a 1-GB 128M x 8 memory module 500 comprising pairs of the 512-Mb 128M x 4 memory components 510 supplies the address and control signals including the extra row address (A13) to the memory module 500. The logic element 540 receives the address and control signals from the memory controller and converts the extra row address (A13) into an extra column address (A12).

[0076] Figure 10B schematically illustrates an exemplary logic element 540 compatible with embodiments described herein. The logic element 540 is used for a memory module 500 comprising pairs of "x 4" memory components 510 with their respective DQS pins tied together to mimic individual "x 8" memory components, as described above. In certain embodiments, the logic element 540 comprises a programmable-logic device (PLD) 542, a first multiplexer 544 electrically coupled to the first rank 520 of memory components 510, and a second multiplexer 546 electrically coupled to the second rank 530 of memory components 510.

[0077] In certain embodiments, the PLD 542 comprises an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, or a complex programmable-logic device (CPLD). Sources of PLDs 542 compatible with embodiments described herein include, but are not limited to, Lattice Semiconductor Corporation of Hillsboro, Oregon, Altera Corporation of San Jose, California, and Xilinx Incorporated of San Jose, California. In certain embodiments, the PLD 542 and the first and second multiplexers 544, 546 are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD 542, first multiplexer 544, and second multiplexer 546 in accordance with embodiments described herein.

[0078] In the exemplary logic element 540 of Figure 10B, during a row access procedure (CAS is high), the first multiplexer 544 passes the A12 address through to the first rank 520, the second multiplexer 546 passes the A12 address through to the second rank 530, and the PLD 542 saves or latches the A13 address from the memory controller. In certain embodiments, a copy of the A13 address is saved by the PLD 542 for each of the internal banks (e.g., 4 internal banks) per memory component 510. During a subsequent column access procedure (CAS is low), the first multiplexer 544 passes the previously-saved A13 address through to the first rank 520 as the A12 address and the second multiplexer 546 passes the previously-saved A13 address through to the second rank 530 as the A12 address. The first rank 520 and the second rank 530 thus interpret the previously-saved A13 row address as the current A12 column address. In this way, the logic element 540 translates the extra row address into an extra column address in accordance with certain embodiments described herein.

[0079] Thus, by allowing two lower-density memory components to be used rather than one higher-density memory component, certain embodiments described herein provide the advantage of using lower-cost, lower-density memory components to build "next-generation" higher-density memory modules. Certain embodiments advantageously allow the use of lower-cost readily-available 512-Mb DDR-2 SDRAM components to replace more expensive 1-Gb DDR-2 SDRAM components. Certain embodiments advantageously reduce the total cost of the resultant memory module.

[0080] Figure 11A schematically illustrates an exemplary memory module 600 which doubles number of ranks in accordance with certain embodiments described herein. The memory module 600 has a first plurality of memory locations with a first memory density. The memory module 600 comprises a plurality of substantially identical memory components 610 configured as a first rank 620, a second rank 625, a third rank 630, and a fourth rank 635. The memory module 600 further comprises a logic element 640 which receives a first set of address and control signals from a memory controller (not shown). The first set of address and control signals is compatible with a second plurality of memory locations having a second memory density. The second memory density is substantially equal to one-half of the first memory density. The logic element 640 translates the first set of

address and control signals into a second set of address and control signals which is compatible with the first plurality of memory locations of the memory module 600 and which is transmitted to the first rank 620, the second rank 625, the third rank 630, and the fourth rank 635.

[0081] Each rank 620, 625, 630, 635 of Figure 11A has 9 memory components 610. Other numbers of memory components 610 in each of the ranks 620, 625, 630, 635 are also compatible with embodiments described herein.

[0082] In the embodiment schematically illustrated by Figure 11A, the memory module 600 has a width of 8 bytes (or 64 bits) and each of the memory components 610 of Figure 11A has a bit width of 8 bits. Other memory module widths (e.g., 4 bytes, 16 bytes, 32 bytes, or 32 bits, 128 bits, 256 bits) and other memory component bit widths (e.g., 4, 16, 32) are also compatible with embodiments described herein. Because the memory module 600 has twice the number of 8-bit-wide ("x 8") memory components 610 as does a standard 8-byte-wide memory module, the memory module 600 has twice the density as does a standard 8-byte-wide memory module. For example, a 1-GB 128M x 8-byte memory module with 36 512-Mb 128M x 8-bit memory components (arranged in four ranks) has twice the memory density as a 512-Mb 128M x 8-byte memory module with 18 512-Mb 128M x 8-bit memory components (arranged in two ranks).

[0083] To access the additional memory density of the high-density memory module 600, the two chip-select signals (CS0, CS1) are used with other address and control signals to gate a set of four gated CAS signals. For example, to access the additional ranks of four-rank 1-GB 128M x 8-byte DDR-1 DRAM memory module, the CS0 and CS1 signals along with the other address and control signals are used to gate the CAS signal appropriately, as schematically illustrated by Figure 11A. Figure 11B schematically illustrates an exemplary logic element 640 compatible with embodiments described herein. In certain embodiments, the logic element 640 comprises a programmable-logic device (PLD) 642 and four "OR" logic elements 652, 654, 656, 658 electrically coupled to corresponding ranks 620, 625, 630, 635 of memory components 610.

[0084] In certain embodiments, the PLD 642 comprises an ASIC, an FPGA, a custom-designed semiconductor device, or a CPLD. Sources of PLDs 642 compatible with

embodiments described herein include, but are not limited to, Lattice Semiconductor Corporation of Hillsboro, Oregon, Altera Corporation of San Jose, California, and Xilinx Incorporated of San Jose, California. In certain embodiments, the PLD 642 and the four "OR" logic elements 652, 654, 656, 658 are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD 642 and appropriate "OR" logic elements 652, 654, 656, 658 in accordance with embodiments described herein.

[0085] In the embodiment schematically illustrated by Figure 11B, the PLD 642 transmits each of the four "enabled CAS" (ENCAS0a, ENCAS0b, ENCAS1a, ENCAS1b) signals to a corresponding one of the "OR" logic elements 652, 654, 656, 658. The CAS signal is also transmitted to each of the four "OR" logic elements 652, 654, 656, 658. The CAS signal and the "enabled CAS" signals are "low" true signals. By selectively activating each of the four "enabled CAS" signals which are inputted into the four "OR" logic elements 652, 654, 656, 658, the PLD 642 is able to select which of the four ranks 620, 625, 630, 635 is active.

[0086] In certain embodiments, the PLD 642 uses sequential and combinatorial logic procedures to produce the gated CAS signals which are each transmitted to a corresponding one of the four ranks 620, 625, 630, 635. In certain other embodiments, the PLD 642 instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS0a, CS0b, CS1a, and CS1b) which are each transmitted to a corresponding one of the four ranks 620, 625, 630, 635.

[0087] Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined in the appended claims.

WHAT IS CLAIMED IS:

1. A memory module comprising:

a plurality of memory components, each memory component having a first bit width, wherein the plurality of memory components are configured as one or more pairs of memory components, each pair of memory components simulating a single virtual memory component having a second bit width which is twice the first bit width.

2. A memory module comprising:

a first memory component having a first data strobe pin;

a second memory component having a second data strobe pin;

a first resistor electrically coupled to the first data strobe pin; and

a second resistor electrically coupled to the second data strobe pin and to the first resistor, wherein the first data strobe pin is electrically coupled to the second data strobe pin through the first resistor and through the second resistor.

3. The memory module of Claim 2, wherein each of the first memory component and the second memory component comprises a double-data-rate-1 (DDR-1), double-data-rate-2 (DDR-2), or double-data-rate-3 (DDR-3) dynamic random-access memory (DRAM) integrated circuit.

4. The memory module of Claim 2, wherein each of the first memory component and the second memory component comprises ball-grid-array (BGA) packaging.

5. The memory module of Claim 4, wherein each of the first memory component and the second memory component comprises fine-pitch BGA (FBGA) packaging.

6. The memory module of Claim 2, wherein each of the first memory component and the second memory component comprises a synchronous dynamic random-access memory (SDRAM) integrated circuit.

7. The memory module of Claim 2, wherein each of the first memory component and the second memory component has a first bit width, wherein the first memory component and the second memory component simulate a single virtual memory component having a second bit width which is twice the first bit width.

8. The memory module of Claim 7, wherein the first bit width is 4 bits, 8 bits, or 16 bits.

9. A memory module comprising:

a termination bus;

a first memory component having a first data strobe pin, a first termination signal pin electrically coupled to the termination bus, a first termination circuit, and at least one data pin, the first termination circuit selectively electrically terminating the first data strobe pin and the first data pin in response to a first signal received by the first termination signal pin from the termination bus;

a second memory component having a second data strobe pin electrically coupled to the first data strobe pin, a second termination signal pin, a second termination circuit, and at least one data pin, the second termination signal pin electrically coupled to a voltage, wherein the second termination circuit is responsive to the voltage by not terminating the second data strobe pin or the second data pin; and

at least one termination assembly having a third termination signal pin, a third termination circuit, and at least one termination pin electrically coupled to the data pin of the second memory component, the third termination signal pin electrically coupled to the termination bus, the third termination circuit selectively electrically terminating the data pin of the second memory component through the termination pin in response to a second signal received by the third termination signal pin from the termination bus.

10. The memory module of Claim 9, wherein the first signal and the second signal are the same signal.

11. The memory module of Claim 9, wherein the termination bus comprises an on-die termination (ODT) bus, each of the first termination circuit, second termination circuit, and third termination circuit comprises an ODT circuit.

12. The memory module of Claim 9, wherein the voltage is ground.

13. The memory module of Claim 9, wherein each of the first memory component and the second memory component comprises a double-data-rate-1 (DDR-1), double-data-

rate-2 (DDR-2), or double-data-rate-3 (DDR-3) dynamic random-access memory (DRAM) integrated circuit.

14. The memory module of Claim 9, wherein each of the first memory component and the second memory component comprises ball-grid-array (BGA) packaging.

15. The memory module of Claim 14, wherein each of the first memory component and the second memory component comprises fine-pitch BGA (FBGA) packaging.

16. The memory module of Claim 9, wherein each of the first memory component and the second memory component comprises a synchronous dynamic random-access memory (SDRAM) integrated circuit.

17. The memory module of Claim 9, wherein each of the first memory component and the second memory component has a first bit width, wherein the first memory component and the second memory component simulate a single virtual memory component having a second bit width which is twice the first bit width.

18. The memory module of Claim 17, wherein the first bit width is 4 bits, 8 bits, or 16 bits.

19. A memory module comprising:

a pair of substantially identical memory components, each memory component having a first bit width, a first number of banks of memory locations, a first number of row address bits, and a first number of column address bits; and

a serial-presence-detect (SPD) device comprising data that characterizes the pair of memory components as a virtual memory component having a second bit width equal to twice the first bit width, a second number of banks of memory locations equal to the first number of banks, a second number of row address bits equal to the first number of row address bits, and a second number of column address bits equal to the first number of column address bits.

20. The memory module of Claim 19, wherein byte 3 of the SPD data comprises the first number of row address bits, byte 4 of the SPD data comprises the first number of column address bits, byte 13 of the SPD data comprises the second bit width, byte 14 of the

SPD data comprises the second bit width, and byte 17 of the SPD data comprises the first number of banks.

21. The memory module of Claim 19, wherein the first bit width is 4 bits.

22. The memory module of Claim 19, wherein the first bit width is 8 bits.

23. The memory module of Claim 19, wherein the memory module comprises a plurality of pairs of substantially identical memory components, each memory component having the first bit width, and the SPD device comprises data that characterizes each pair of memory components as a corresponding virtual memory component having the second bit width.

24. The memory module of Claim 19, wherein the memory module has a 1-GB (128M x 8-byte) configuration, and comprises eight pairs of memory components, each memory component having a 512-Mb (128M x 4-bit) configuration, the SPD device comprising data that characterizes each pair of memory components as a corresponding virtual memory component having the second bit width of 8 bits, 13 row address bits, and 12 column address bits.

25. The memory module of Claim 19, wherein the SPD device comprises an electrically-erasable programmable read-only memory (EEPROM) device.

26. A memory module having a first memory capacity, the memory module comprising:

a plurality of substantially identical memory components configured as a first rank and a second rank, the memory components of the first rank configured in pairs with their respective data strobe pins tied together, the memory components of the second rank configured in pairs with their respective data strobe pins tied together; and

a logic element which receives a first set of address and control signals compatible with a second memory capacity, the second memory density substantially equal to one-half of the first memory capacity, wherein the logic element translates the first set of address and control signals into a second set of address and control signals compatible with the first memory capacity of the memory module, the logic

element transmitting the second set of address and control signals to the first rank and the second rank.

27. A memory module having a first plurality of memory locations with a first memory density, the memory module comprising:

a plurality of substantially identical memory components configured as a first rank, a second rank, a third rank, and a fourth rank; and

a logic element which receives a first set of address and control signals compatible with a second plurality of memory locations having a second memory density, the second memory density substantially equal to one-half of the first memory density, wherein the logic element translates the first set of address and control signals into a second set of address and control signals compatible with the first plurality of memory locations of the memory module, the logic element transmitting the second set of address and control signals to the first rank, the second rank, the third rank, and the fourth rank.

HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS

Abstract of the Disclosure

A memory module comprises a plurality of memory components. Each memory component has a first bit width. The plurality of memory components are configured as one or more pairs of memory components. Each pair of memory components simulates a single virtual memory component having a second bit width which is twice the first bit width.

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030705

FIGURE 1:

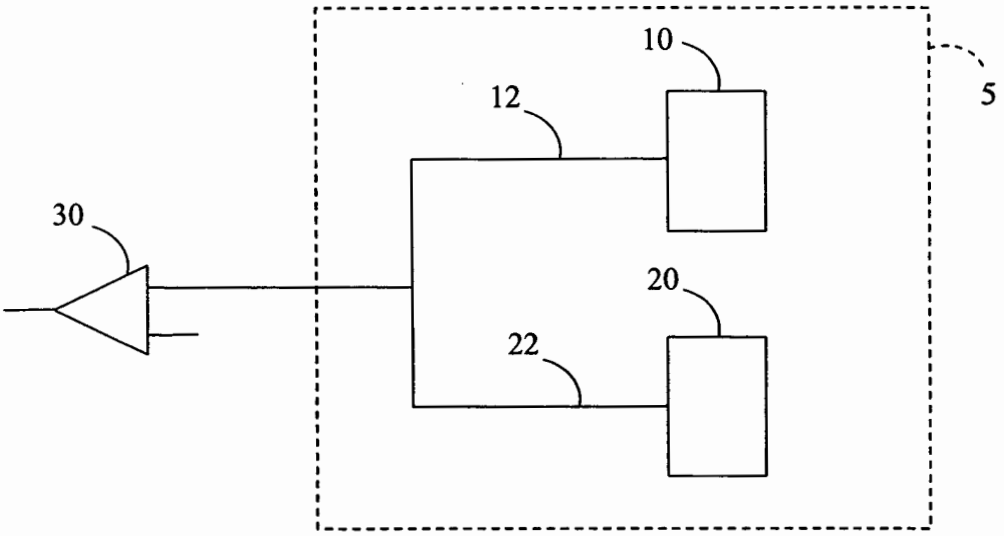


FIGURE 2:

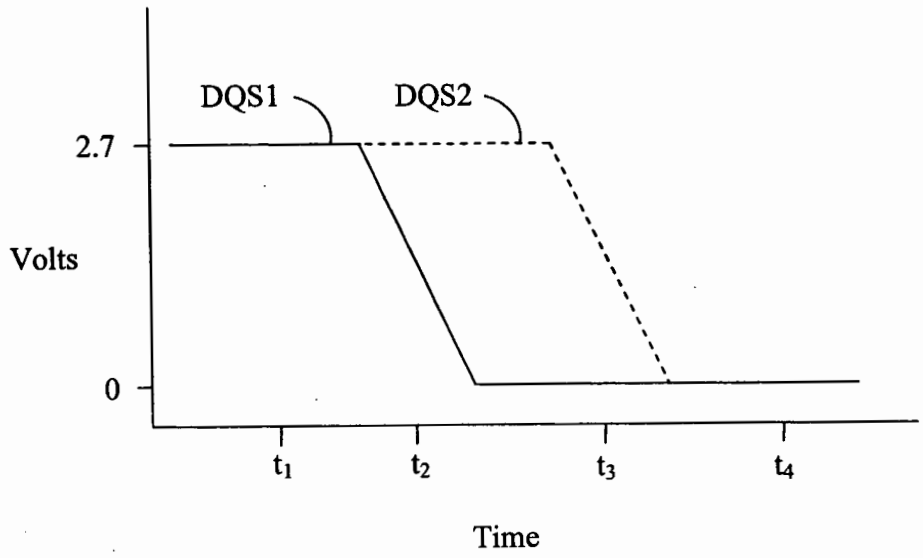
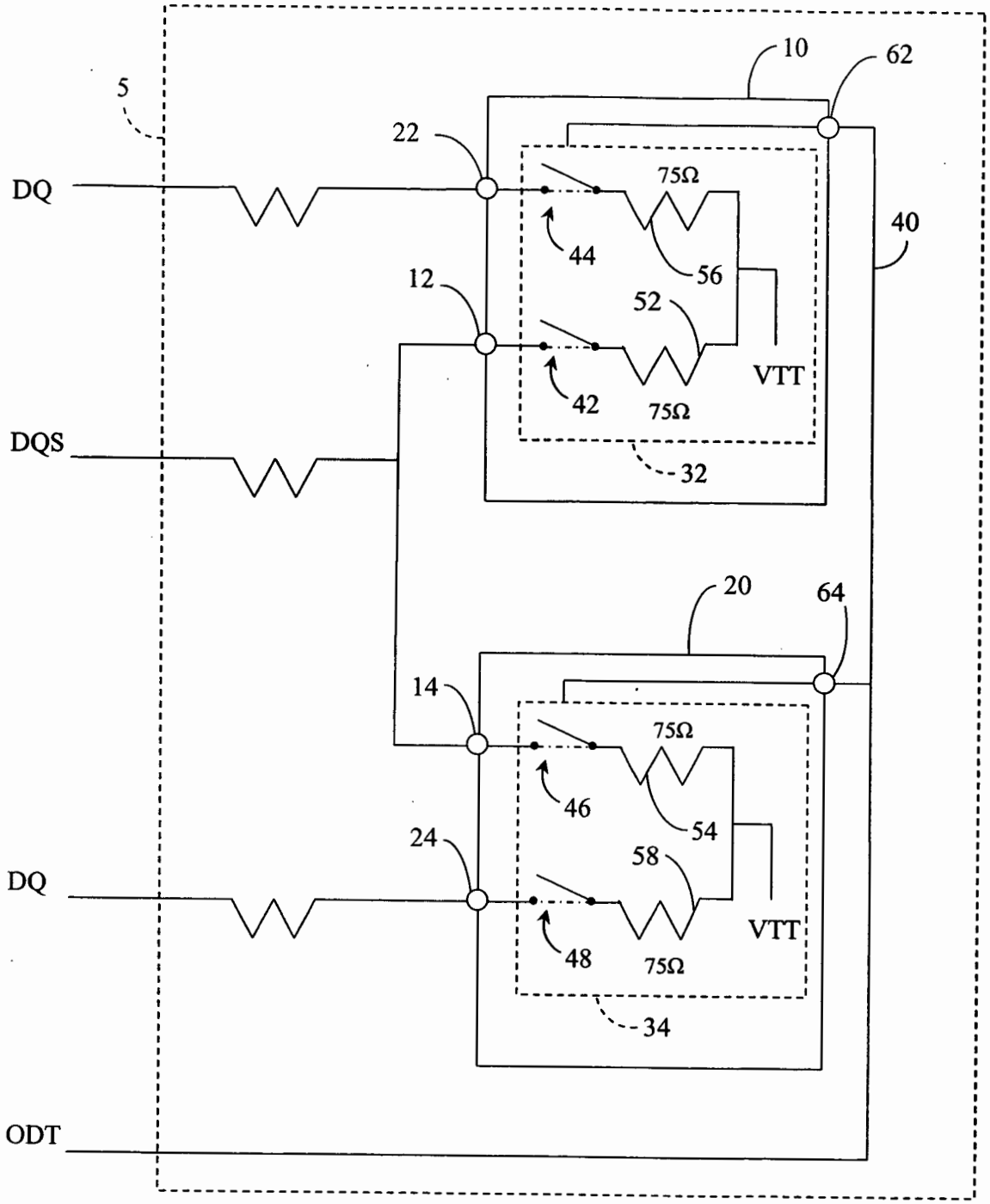


FIGURE 3:


5
10
62
22
DQ
75Ω
44
56
40
12
52
VTT
42
75Ω
DQS
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64
14
75Ω
46
54
24
58
DQ
VTT
48
75Ω
34
ODT

FIGURE 4:

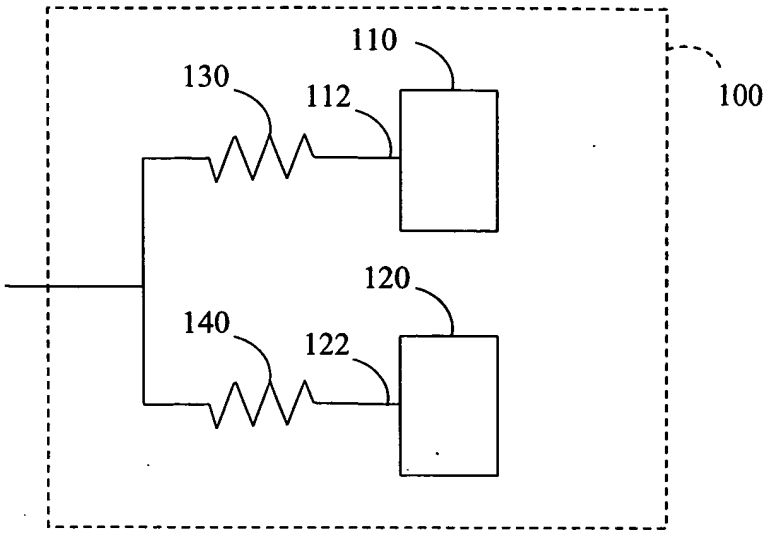


FIGURE 5A:

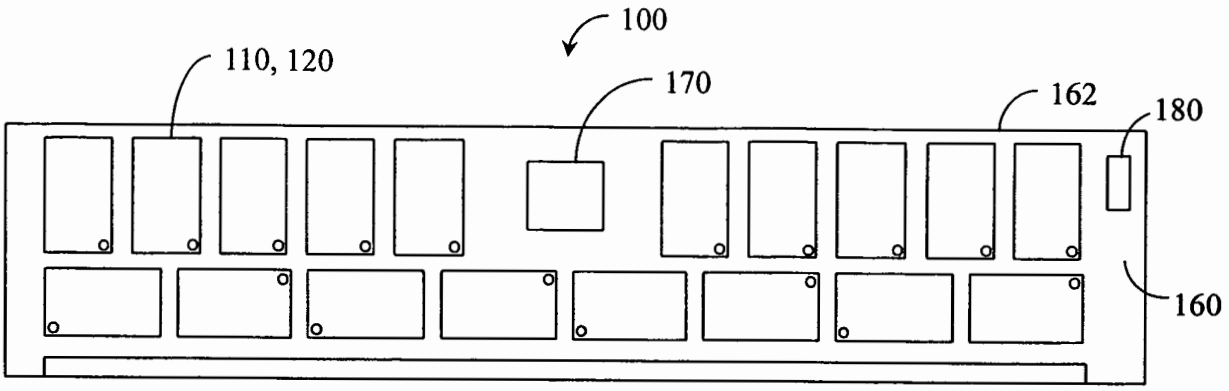


FIGURE 5B:

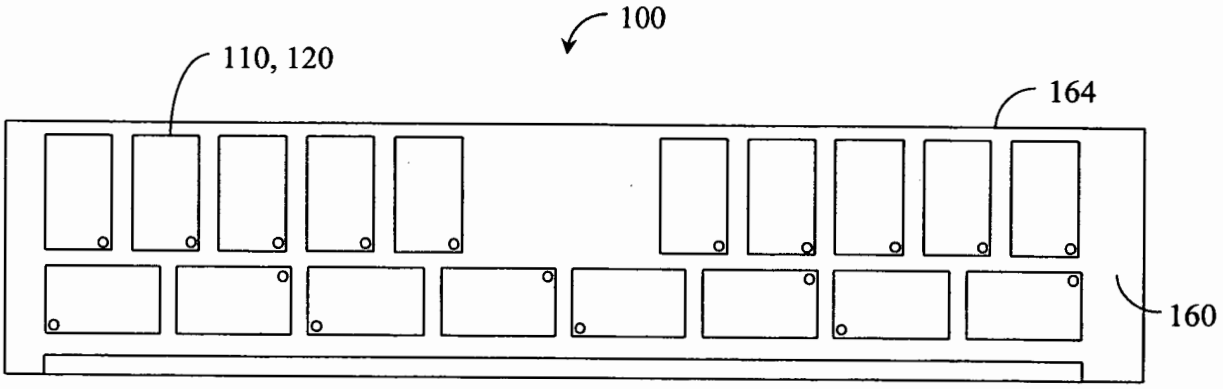


FIGURE 6A:

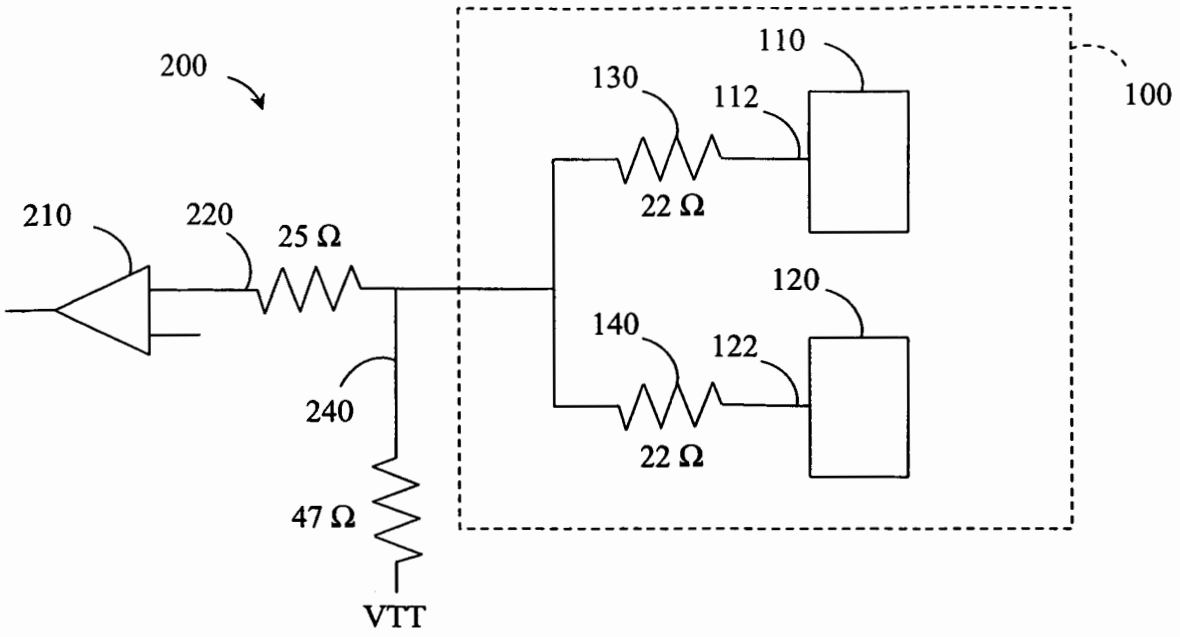


FIGURE 6B:

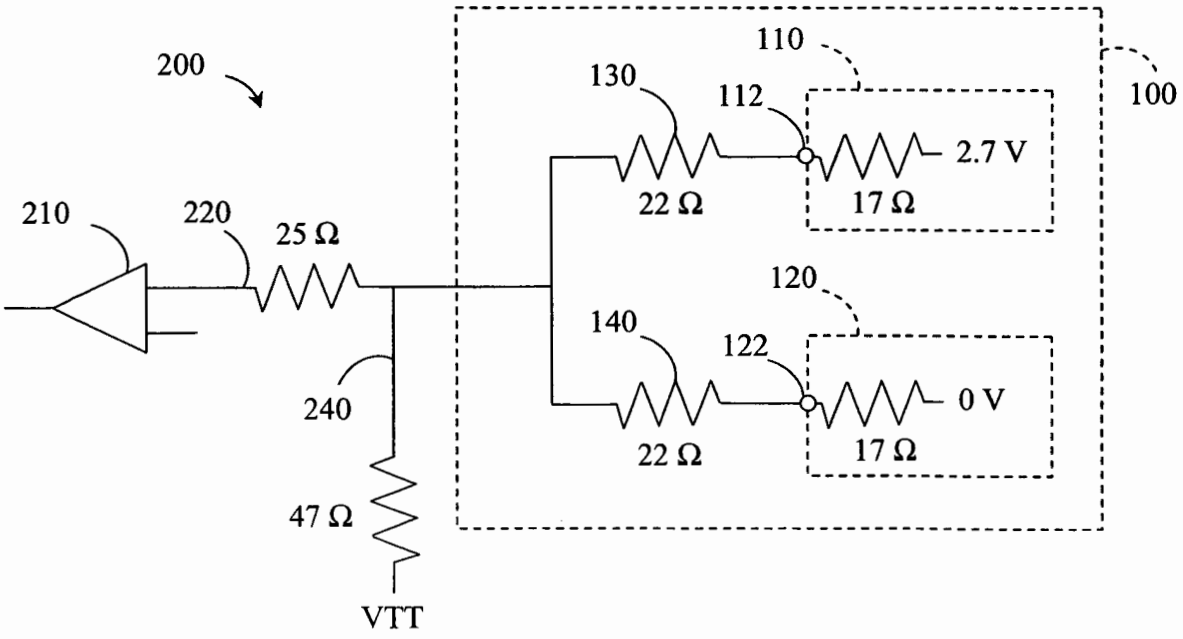
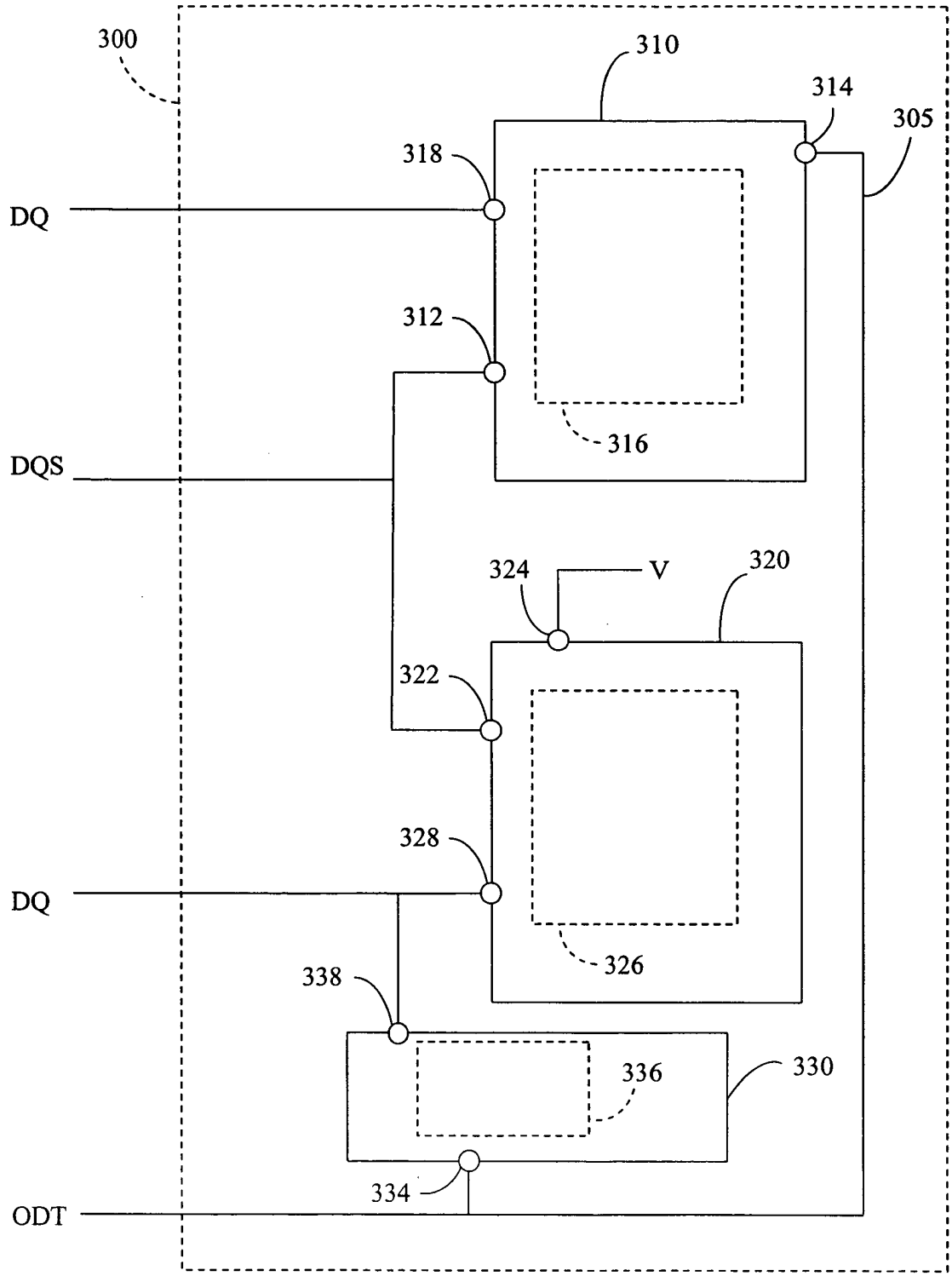


FIGURE 7:


300
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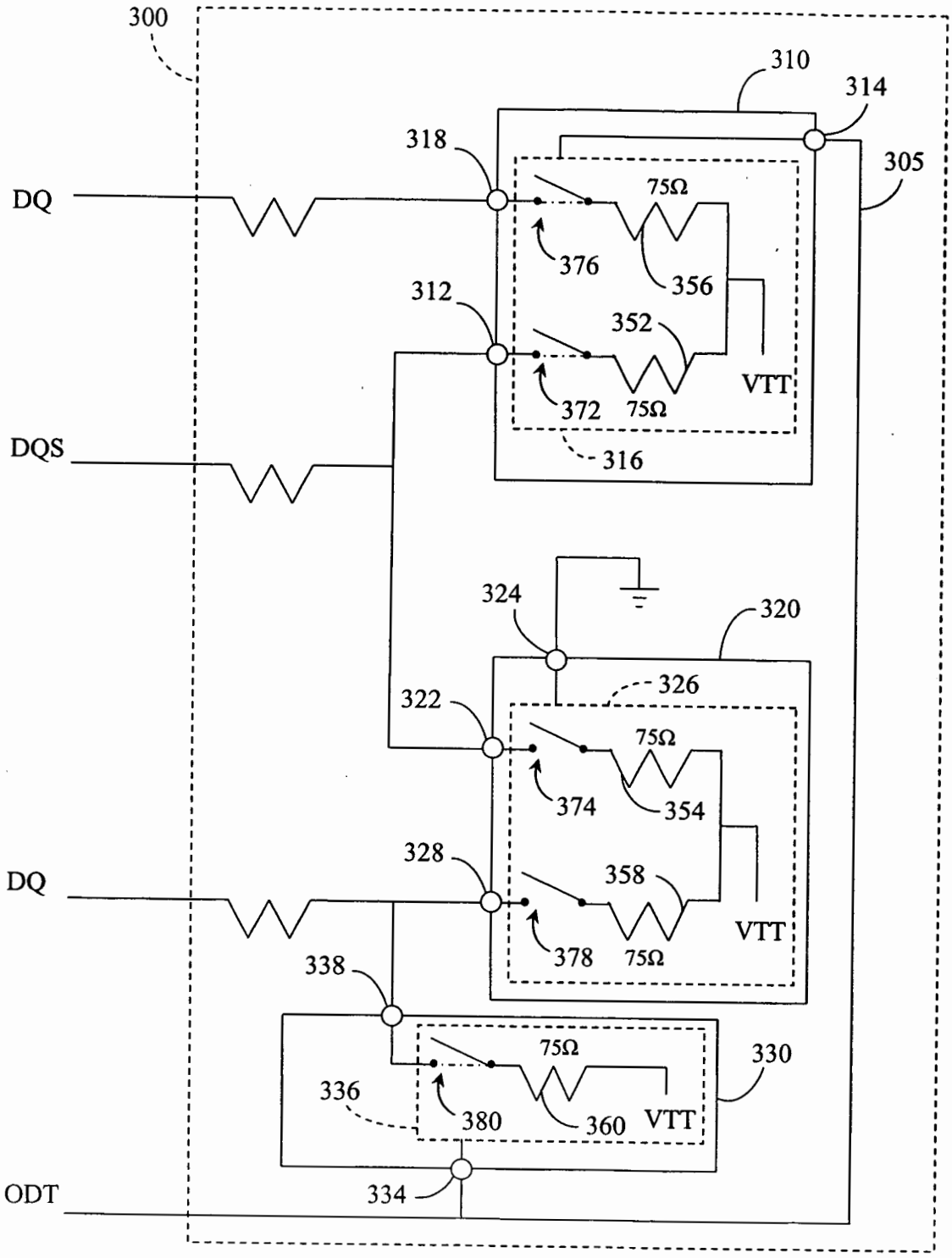
ODT

FIGURE 8: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VTT
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338
75Ω
330
336
380
360
VTT
334
ODT

FIGURE 9:

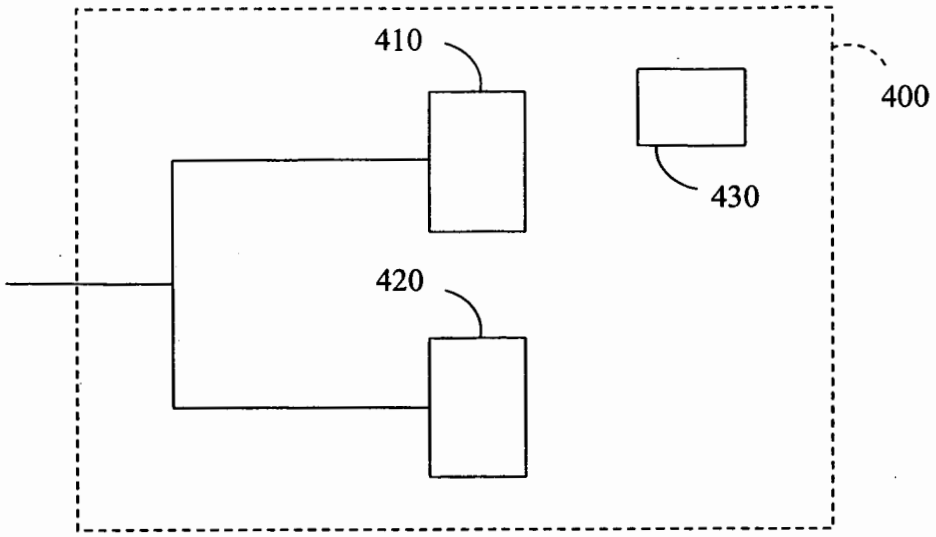


FIGURE 10A:

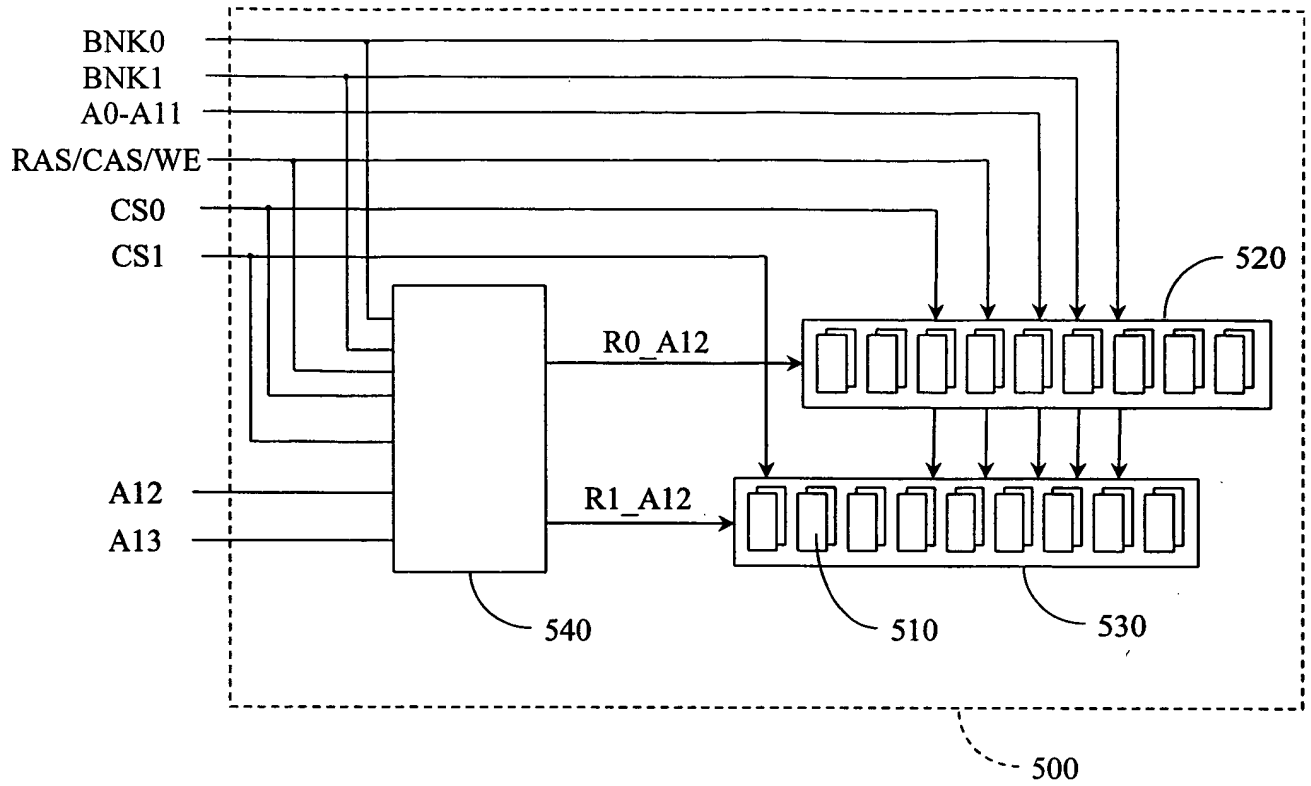


FIGURE 10B:

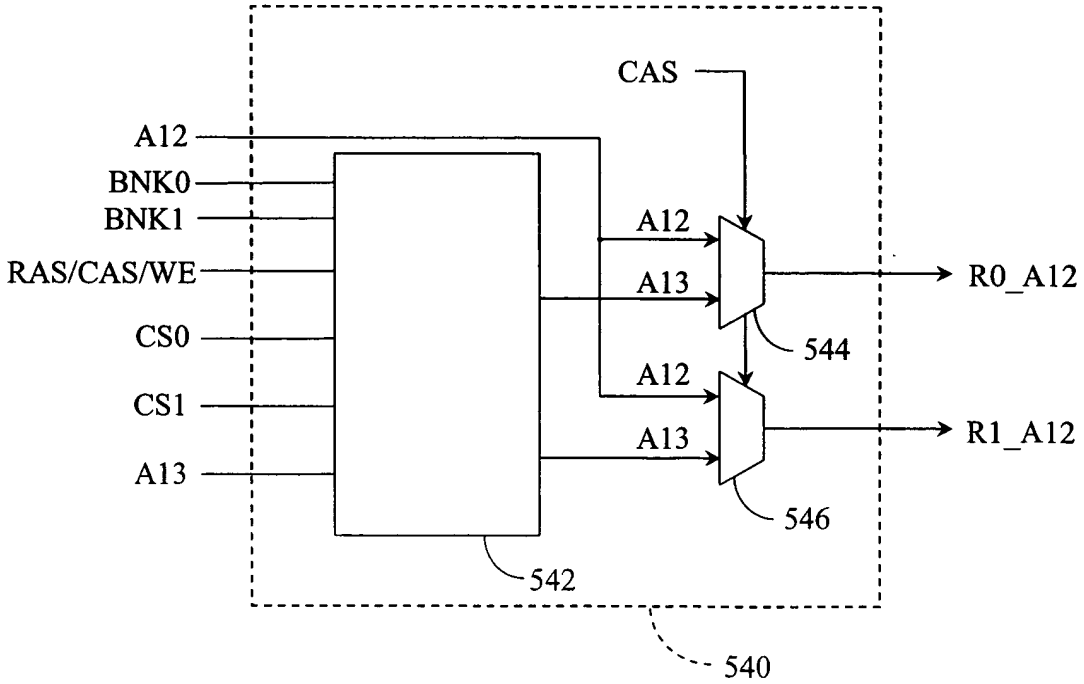


FIGURE 11A:

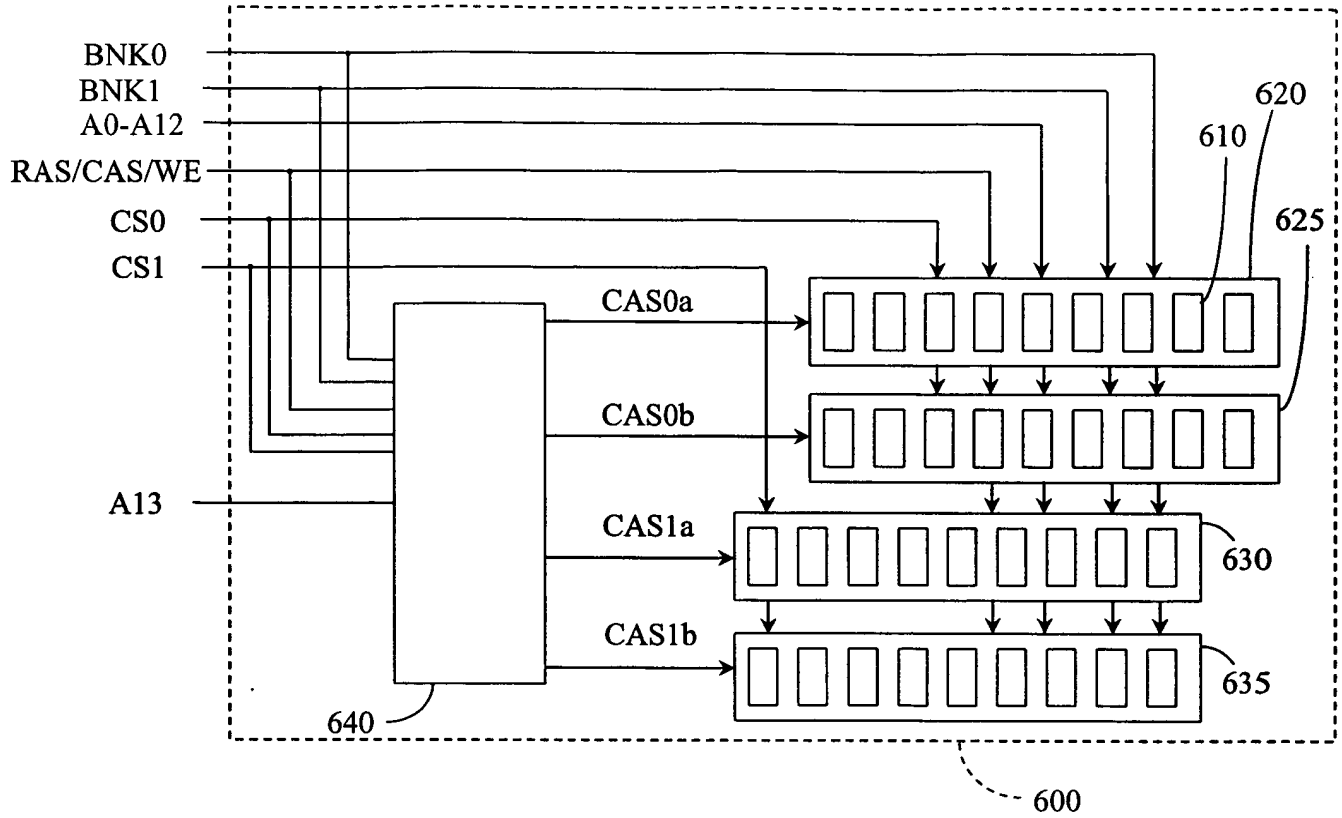
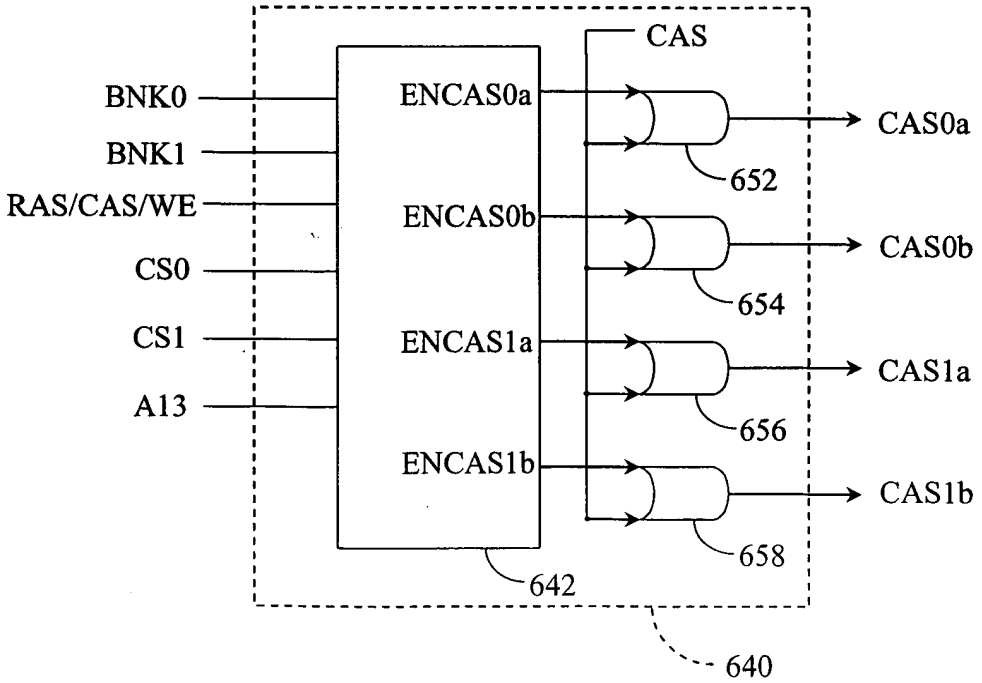


FIGURE 11B:



PATENT APPLICATION FEE DETERMINATION RECORD
Effective December 8, 2004

11075395

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	27	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	27 minus 20=	* 7
INDEPENDENT CLAIMS	6 minus 3 =	* 3
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE		OR	BASIC FEE	300
X$ 25=		OR	X$50=	350
X100=		OR	X200=	600
+180=		OR	+360=	
TOTAL		OR	TOTAL	1250

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/075,395	03/07/2005		NETL.018A

CONFIRMATION NO. 8121

FORMALITIES LETTER

OC000000015683232

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

Date Mailed: 04/07/2005

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  Applicant must submit $ **300** *to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).*
- The oath or declaration is missing. *A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.*
  Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(f) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Additional claim fees of **$950** as a non-small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$2080** for a Large Entity

- **$300** Statutory basic filing fee.
- **$130** Late oath or declaration Surcharge.

- The application search fee has not been paid. Applicant must submit **$500** to complete the search fee.
- The application examination fee has not been paid. Applicant must submit **$200** to complete the examination fee for a large entity

- Total additional claim fee(s) for this application is **$950**

  - **$600** for **3** independent claims over 3.
  - **$350** for **7** total claims over 20.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

A copy of this notice MUST be returned with the reply.

Office of Initial Patent Examination (703) 308-1202

PART 3 - OFFICE COPY

Docket No.: NETL.018A **Customer No. 20,995** IFW

OIPE JC99
AUG 0 8 2005
PATENT & TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT

Applicants	:	Jayesh R. Bhakta et al.
App. No	:	11/075,395
Filed	:	March 7, 2005
For	:	HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS
Examiner	:	Unknown
Art Unit	:	2186

CERTIFICATE OF MAILING

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

8/5/05
(Date)

Bruce S. Itchkawitz, Reg. No. 47,677

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is an Information Disclosure Statement by Applicant (PTO/SB/08 equivalent) listing twenty-five (25) references to be considered by the Examiner. Also enclosed are nine (9) non-patent literature as listed on the Information Disclosure Statement.

This Information Disclosure Statement is being filed before the receipt of a first Office Action on the merits, and presumably no fee is required. If a first Office Action on the merits was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 8/5/05

By:

Bruce S. Itchkawitz
Registration No. 47,677
Attorney of Record
Customer No. 20,995
(949) 760-0404

1721077
080505

OIPE JC99
AUG 0 8 2005
PATENT & TRADEMARK OFFICE

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	11/075,395
	Filing Date	March 7, 2005
	First Named Inventor	Jayesh R. Bhakta
	Art Unit	2186
(Multiple sheets used when necessary)	Examiner	Unknown
SHEET 1 OF 2	Attorney Docket No.	NETL.018A

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Publication Date	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1	5,247,643	09/21/1993	Shottan	
	2	5,703,826	12/30/1997	Hush et al.	
	3	6,154,418	11/28/2000	Li	
	4	6,453,381 B1	09/17/2002	Yuan et al.	
	5	6,518,794 B2	02/11/2003	Coteus et al.	
	6	6,681,301 B1	01/20/2004	Mehta et al.	
	7	6,785,189 B2	08/31/2004	Jacobs et al.	
	8	6,807,125 B2	10/19/2004	Coteus et al.	
	9	6,813,196 B2	11/02/2004	Park et al.	
	10	2001/0052057 A1	12/13/2001	Lai et al.	
	11	2002/0088633 A1	07/11/2002	Kong et al.	
	12	2003/0063514 A1	04/03/2003	Faue	
	13	2003/0191995 A1	10/09/2003	Abrosimov et al.	
	14	2003/0210575 A1	11/13/2003	Seo et al.	
	15	2004/0037158 A1	02/26/2004	Coteus et al.	
	16	2005/0036378 A1	02/17/2005	Kawaguchi et al.	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author, title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
	17	CUPPU, Vinodh, et al., "A Performance Comparison of Contemporary DRAM Architectures," IEEE Proceedings of the 26th International Symposium on Computer Architecture, May 2-4, 1999, Atlanta, Georgia, pp. 1-12.	
	18	JEDEC Standard No. 21-C, 4.20-2 – 168 Pin, PC133 SDRAM Registered Design Specification, Revision 1.4, Release 11a, February 2002.	
	19	JEDEC Standard No. 21-C, 4.20-3 – 144 Pin, PC133 SDRAM Unbuffered SO-DIMM, Reference Design Specification, Revision 1.02, Release 11.	
	20	JEDEC Standard No. 21-C, DDR SDRAM PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, Revision 1.3, Release 11b, January 2002.	
	21	JEDEC Standard No. 21-C, 4.20.5 – 184 Pin, PC1600/2100 DDR SDRAM Unbuffered DIMM Design Specification, Revision 1.1, Release 11b.	
	22	JEDEC Standard No. 21-C, 4.20.6 – 200 Pin, PC2700/PC2100/PC1600 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification, Revision 1.1, Release 11b, April 26, 2002.	

Examiner Signature	Date Considered

***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

T[1] - Place a check mark in this area when an English language Translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	11/075,395
	Filing Date	March 7, 2005
	First Named Inventor	Jayesh R. Bhakta
	Art Unit	2186
(Multiple sheets used when necessary)	Examiner	Unknown
SHEET 2 OF 2	Attorney Docket No.	NETL.018A

OIPE JC99 AUG 0 8 2005 PATENT & TRADEMARK OFFICE

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author, title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
	23	JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published February 2004.	
	24	INTEL CORPORATION, PC SDRAM Registered DIMM Design Support Document, Revision 1.2, October 1998.	
	25	INTEL CORPORATION, 66/100 MHz PC SDRAM 64-Bit Non-ECC/Parity 144 Pin Unbuffered SO-DIMM Specification, Revision 1.0, February 1999.	

1707974
080505

Examiner Signature	Date Considered
***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

T[1] - Place a check mark in this area when an English language Translation is attached.

66/100 MHz PC SDRAM 64-Bit Non-ECC/Parity 144 Pin UNBUFFERED SO-DIMM SPECIFICATION

Revision 1.0
February 1999

Intel Corporation

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Petitioners
Ex. 1010, p. 54

Changes:

Revision 1.0 October, 1998
Added 256Mbit support, and changed decoupling.

Revision 0.7 August 14, 1998
Added clock trace length data, and PB marking information.

Revision 0.51 July 15, 1998
Added figures 14 and 15

Revision 0.5 July 14, 1998
Add support for 66MHz

Revision 0.3 June 12, 1998
Removed support of X8 components

Revision 0.22 April 15, 1998
First external copy.

Petitioners
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1.0 Introduction

This specification defines the electrical, mechanical, and trace routing requirements for 144-pin, 3.3 volt, 66/100 MHz, 64-bit wide (non-ECC/Parity), 2 clock, unbuffered Synchronous DRAM Small Outline Dual In-Line Memory Modules (SDRAM SO-DIMMs). These SDRAM SO-DIMMs are intended for use as main memory installed in personal notebook computer motherboards.

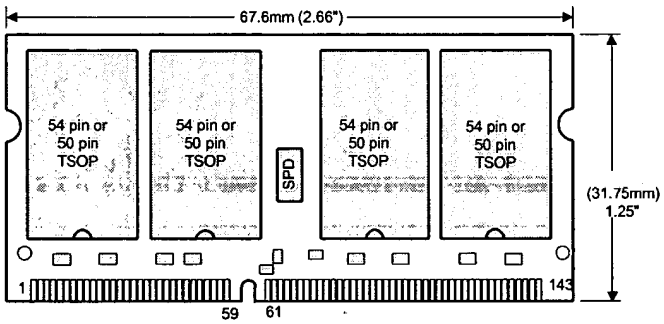

Figure 1: SO-DIMM with four 54-pin or 50-pin SDRAM per side

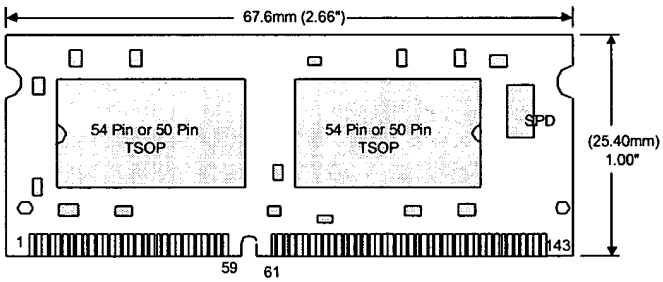

Figure 2: SO-DIMM with two 54-pin or 50-pin SDRAM per side

Related Documents

The related documents contain information that is critical to this specification. The revisions listed are the latest releases at the time of this writing. However, it is important to use the most current revisions of each of these documents when generating or modifying SO-DIMM designs.

Table 1: Related Documents

TITLE	REV	DATE
Intel PC/100 SDRAM Specification	1.62	Sept. 1998
Intel SDRAM SPD Data Structure Specification	1.2A	April 1997

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SO-DIMM Configurations
SDRAM SO-DIMM configurations are defined in the following tables:

Table 2: SDRAM Non Mixed-Mode Module Configurations

Config #	SO-DIMM Capacity	SO-DIMM Organization	SDRAM density	SDRAM Organization	# of SDRAMs	# Rows of SDRAM	# Banks in SDRAM	# Address bits row/bank/col
1	8 MB	1M X 64	16 Mbit	1MX16	4	1	2	11/1/8
2	16 MB	2M X 64	16 Mbit	1MX16	8	2	2	11/1/8
3	32 MB	4M X 64	64 Mbit	4MX16	4	1	4	12/2/8
4	64 MB	8M X 64	64 Mbit	4MX16	8	2	4	12/2/8
5	64 MB	8M X 64	128 Mbit	8MX16	4	1	4	12/2/9
6	128 MB	16M X 64	128 Mbit	8MX16	8	2	4	12/2/9
7	128 MB	16M X 64	256 Mbit	16MX16	4	1	4	13/2/9
8	256 MB	32M X 64	256 Mbit	16MX16	8	2	4	13/2/9

Table 3: SDRAM Mixed-Mode Module Configurations

Config #	SO-DIMM Capacity	SO-DIMM Organization	SDRAM density	SDRAM Organization	# of SDRAMs	# of Rows of SDRAM	Banks in SDRAM	# Address bits row/bank/col
M1	40 MB	1M x 64 + 4M x 64	16 Mb 64 Mb	1Mb x16 4Mb x 16	4 4	2	2 4	11/1/8 12/2/8
M2	72 MB	1M x 64 + 8M x 64	16 Mb 128 Mb	1Mb x 16 8Mb x 16	4 4	2	2 4	11/1/8 12/2/9
M3	136 MB	1M x 64 + 16M x 64	16 Mb 256 Mb	1Mb x 16 16Mb x 16	4 4	2	2 4	11/1/8 13/2/9
M4	96 MB	4M x 64 + 8M x 64	64 Mb 128 Mb	4Mb x 16 8Mb x 16	4 4	2	4 4	12/2/8 12/2/9
M5	160 MB	4M x 64 + 16M x 64	64 Mb 256 Mb	4Mb x 16 16Mb x 16	4 4	2	4 4	12/2/8 13/2/9
M6	192 MB	8M x 64 + 16M x 64	128 Mb 256 Mb	8Mb x 16 16Mb x 16	4 4	2	4 4	12/2/9 13/2/9

The following SO-DIMMS will be designed at Intel and offered as reference designs.

Table 4: SO-DIMM Reference Designs

Config #	SO-DIMM Capacity	SDRAM density	SDRAM Organization	# Rows of SDRAM	# Banks in SDRAM	Size of SO-DIMM	Corresponding Figure
3 / 5 / 7	32 MB / 64 MB / 128 MB	64, 128, 256 Mbit	4MX16 / 8MX16 / 16MX16	1	4	1.00	Figure 2
4 / 6 / 8	64 MB / 128 MB / 256 MB	64, 128, 256 Mbit	4MX16 / 8MX16 / 16MX16	2	4	1.25	Figure 1

Distinction between "banks" and "rows"

This document only uses "banks" when referring to banks of memory internal to the SDRAM component (two or four). "Rows" is used to define the number of sets of SDRAMs on the SO-DIMM that collectively make up 64 bits of data.

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2.0 Environmental Requirements

The SDRAM SO-DIMM shall be designed to operate within a notebook personal computer in a variety of environments. The temperature and humidity limits are as follows.

Table 5: SO-DIMM Environmental Requirements

Operating Temperature	0 °C to +65 °C ambient
Operating Humidity	10% to 90% relative humidity, noncondensing
Operating Pressure	10.106 PSI (up to 10,000 ft.)
Storage Temperature	-40 °C to + 70 °C
Storage Humidity	5% to 95% without condensation
Storage Pressure	1.682 PSI (up to 50,000 ft.) at 50 °C

Safety - UL Rating

Printed circuit board to have a flammability rating of 94V-O Markings to include UL tractability requirements per *UL Recognized Component Directory.*

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3.0 Mechanical Design

The following table and drawings give the specific dimensions and tolerances for a 144-pin SO-DIMM.

Table 6: SO-DIMM Dimensions and Tolerances

SYMBOL	DEFINITION	MIN	NOM	MAX	NOTES
A	Overall module height measured from Datum -B-.	25.25 mm 31.60 mm	25.40 mm 31.75 mm	25.55 mm 31.90 mm	Two sizes available: "1 inch" and "1.25 inch".
A1	The distance from Datum -B- to the centerline of the PWB alignment holes		6.00 mm BASIC		These holes are not used by the next level of assembly. The dimensions are supplied for information only. If the holes are used in manufacturing they should be tightly toleranced. The recommended positional tolerance is 0.10 mm.
A2	The distance from Datum -B- to the lower edge of the Component Area on the front side of the PWB.	3.2 mm			
A3	The distance from Datum -B- to the lower edge of the Component Area on the back side of the PWB.	4.0 mm			Dimensions applicable when components mounted on both sides. Application note: border of component area.
A4	The distance from Datum -B- to the centerline of the latch holes		20.00 mm BASIC		
D	The overall length of the PWB	67.45 mm	67.60 mm	67.75 mm	
D1	The distance between the centerline of the contact at the immediate left of the key zone and the inner edge of the left latch hole.		24.50 mm BASIC		
D2	The distance between the inner edge of the latch holes		63.60 mm BASIC		
D3	The distance between Datum -A- and the center of the contact at the immediate left of the key zone on the front side of the PWB.		2.50 mm BASIC		The position of the notch indicates that the operating voltage is 3.3 Volts. The centerlines of contacts on the front side of the PWB are not coincident with the centerlines of contacts on the backside of the PWB
D4	The distance between Datum -A- and the center of the contact at the immediate left of the key zone on the backside of the PWB.		2.10 mm BASIC		
D5	The distance between the centerline of D Datum -A-.		4.80 mm BASIC		
E	The overall thickness of the PWB with the components mounted. The overall thickness is measured from the highest component on the front side to the highest component on the backside			3.80 mm	Dimensions applicable when components mounted on both sides.
e1	The distance between the centerline of the contact to the immediate left of the key zone and the center of the left most contact.		23.20 mm BASIC		
e2	The distance between the centerline of the contact to the immediate right of the key zone and the center of the right most contact.		32.80 mm BASIC		

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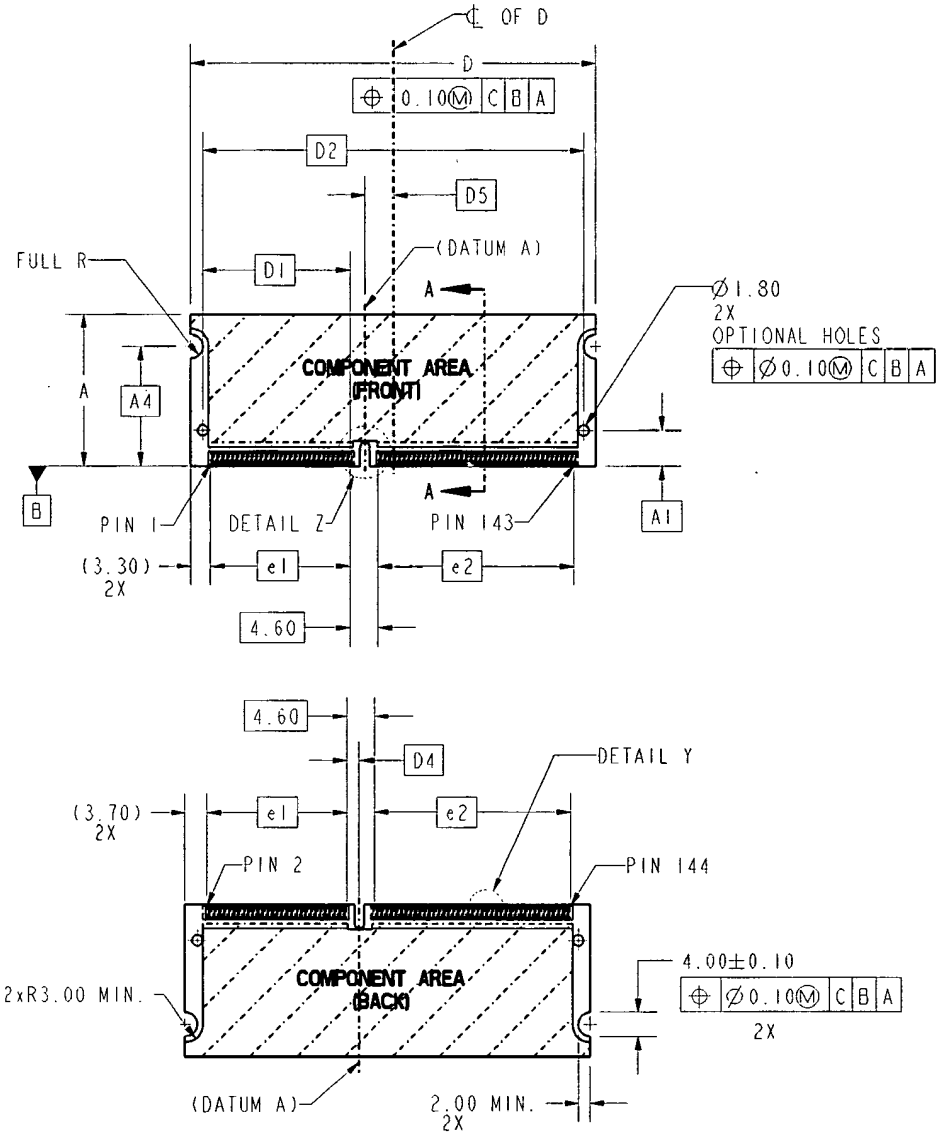

Figure 3: SO-DIMM Mechanical Drawing (1 of 5)

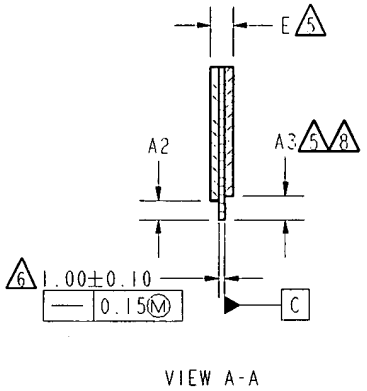

Figure 4: SO-DIMM Mechanical Drawing (2 of 5)

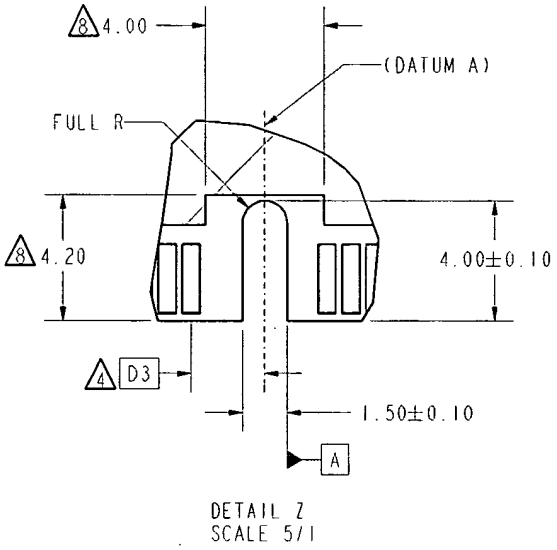

Figure 5: SO-DIMM Mechanical Drawing (3 of 5)

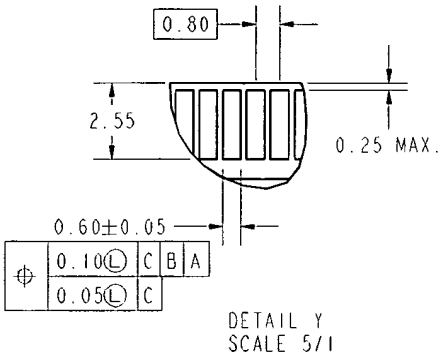

Figure 6: SO-DIMM Mechanical Drawing (4 of 5)

NOTES

1 DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.

2 TOLERANCES ON ALL DIMENSIONS +/- 0.15 UNLESS OTHERWISE SPECIFIED.

3 ALL DIMENSIONS ARE IN MILIMETERS.

4 APPLICATION NOTE:
VARYING THE POSITION OF THE NOTCH IDENTIFIES THE OPERATIONAL VOLTAGE. THE SO-DIMMS GENERATED FROM THIS SPECIFICATION OPERATE USING A VDDQ VOLTAGE OF 3.3 VOLTS.

5 DIMENSION APPLICABLE WHEN COMPONENTS MOUNTED ON BOTH SIDES

6 CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.

7 APPLICATION NOTE:
RECOMMENDED PLATING FOR CONTACT PADS SHALL BE ELECTROLYTIC GOLD PLATING 0.78 MICROMETER MIN. OVER NICKEL PLATING 2 MICROMETER MIN.

8 APPLICATION NOTE:
BORDER OF COMPONENT AREA.

Figure 7: SO-DIMM Mechanical Drawing (5 of 5)

Explanation of SO-DIMM Keying

All SO-DIMMs generated from this spec should have a notch cut into the edge connection that conveys information on the voltage of the SO-DIMM. The notch should be positioned between SO-DIMM pins 59 and 61 and should be centered between the two pins. This signifies that the SO-DIMM operates using a Vddq voltage of 3.3 Volts. Please see the mechanical drawings above for exact dimensions and placement of the notch.

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4.0 Module Pinout

The following table provides the 144-pin, 64-bit unbuffered SO-DIMM module connector pinout. Note that all odd-numbered pads reside on the primary (front) side of the SO-DIMM card, and all even-numbered pins reside on the secondary (back) side of the card.

Table 7: SDRAM SO-DIMM pinout

Signal Name	Pin	Pin	Signal Name
Vss	1	2	Vss
DQ0	3	4	DQ32
DQ1	5	6	DQ33
DQ2	7	8	DQ34
DQ3	9	10	DQ35
Vdd	11	12	Vdd
DQ4	13	14	DQ36
DQ5	15	16	DQ37
DQ6	17	18	DQ38
DQ7	19	20	DQ39
Vss	21	22	Vss
DQMB0	23	24	DQMB4
DQMB1	25	26	DQMB5
Vdd	27	28	Vdd
A0	29	30	A3
A1	31	32	A4
A2	33	34	A5
Vss	35	36	Vss
DQ8	37	38	DQ40
DQ9	39	40	DQ41
DQ10	41	42	DQ42
DQ11	43	44	DQ43
Vdd	45	46	Vdd
DQ12	47	48	DQ44
DQ13	49	50	DQ45
DQ14	51	52	DQ46
DQ15	53	54	DQ47
Vss	55	56	Vss
Reserved	57	58	Reserved
Reserved	59	60	Reserved
CLK0	61	62	CKE0
Vdd	63	64	Vdd
RAS#	65	66	CAS#
WE#	67	68	CKE1
S0#	69	70	A12

Signal Name	Pin	Pin	Signal Name
S1#	71	72	A13
Reserved	73	74	CLK1
Vss	75	76	Vss
Reserved	77	78	Reserved
Reserved	79	80	Reserved
Vdd	81	82	Vdd
DQ16	83	84	DQ48
DQ17	85	86	DQ49
DQ18	87	88	DQ50
DQ19	89	90	DQ51
Vss	91	92	Vss
DQ20	93	94	DQ52
DQ21	95	96	DQ53
DQ22	97	98	DQ54
DQ23	99	100	DQ55
Vdd	101	102	Vdd
A6	103	104	A7
A8	105	106	BA0
Vss	107	108	Vss
A9	109	110	BA1
A10	111	112	A11
Vdd	113	114	Vdd
DQMB2	115	116	DQMB6
DQMB3	117	118	DQMB7
Vss	119	120	Vss
DQ24	121	122	DQ56
DQ25	123	124	DQ57
DQ26	125	126	DQ58
DQ27	127	128	DQ59
Vdd	129	130	Vdd
DQ28	131	132	DQ60
DQ29	133	134	DQ61
DQ30	135	136	DQ62
DQ31	137	138	DQ63
Vss	139	140	Vss
SDA	141	142	SCL
Vdd	143	144	Vdd

Note: Reserved = Do not connect

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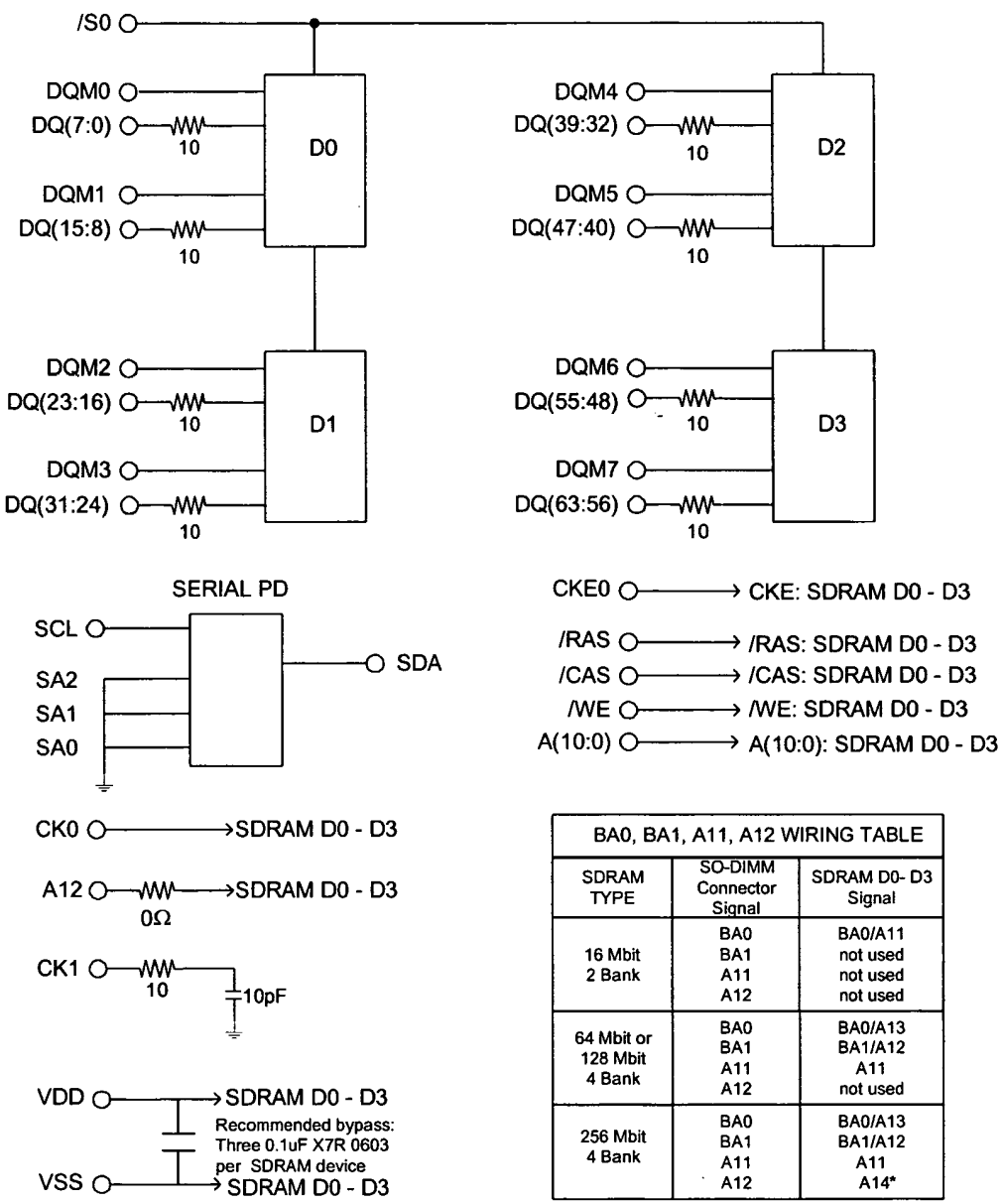
5.0 SDRAM SO-DIMM Block Diagrams



BA0, BA1, A11, A12 WIRING TABLE		
SDRAM TYPE	SO-DIMM Connector Signal	SDRAM D0- D3 Signal
16 Mbit 2 Bank	BA0 BA1 A11 A12	BA0/A11 not used not used not used
64 Mbit or 128 Mbit 4 Bank	BA0 BA1 A11 A12	BA0/A13 BA1/A12 A11 not used
256 Mbit 4 Bank	BA0 BA1 A11 A12	BA0/A13 BA1/A12 A11 A14*

Note: Use a zero ohm jumper to isolate A12 from the SDRAM pins in non-256Mbit designs. Limit the trace on the SO-DIMM Connector side of the jumper to 0.5 inches.

Note: To obtain most advantageous board layout, byte lanes may be swapped. Bits within a byte may also be swapped, however, bits between bytes may not be swapped.

Figure 8: 64-bit non-ECC SO-DIMM Block Diagram (1 Row, x16 SDRAMs)

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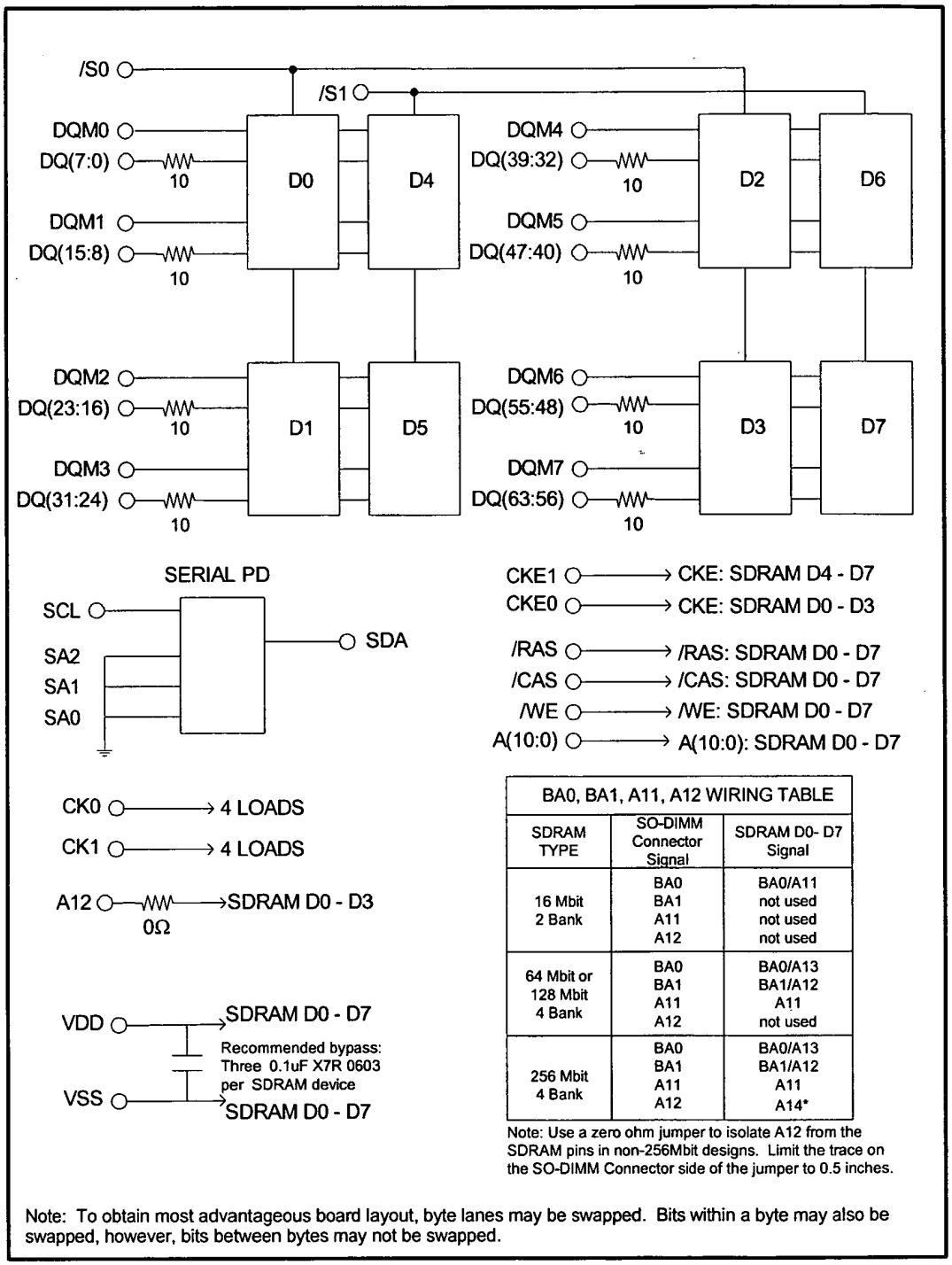

BA0, BA1, A11, A12 WIRING TABLE		
SDRAM TYPE	SO-DIMM Connector Signal	SDRAM D0- D7 Signal
16 Mbit 2 Bank	BA0 BA1 A11 A12	BA0/A11 not used not used not used
64 Mbit or 128 Mbit 4 Bank	BA0 BA1 A11 A12	BA0/A13 BA1/A12 A11 not used
256 Mbit 4 Bank	BA0 BA1 A11 A12	BA0/A13 BA1/A12 A11 A14*

Note: Use a zero ohm jumper to isolate A12 from the SDRAM pins in non-256Mbit designs. Limit the trace on the SO-DIMM Connector side of the jumper to 0.5 inches.

Note: To obtain most advantageous board layout, byte lanes may be swapped. Bits within a byte may also be swapped, however, bits between bytes may not be swapped.

Figure 9: 64-bit non-ECC SO-DIMM Block Diagram (2 Rows, x16 SDRAMs)

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6.0 SO-DIMM PCB Layout and Signal Routing

Printed Circuit Board

The SO-DIMM printed circuit board shall be at least a six layer stack-up using glass epoxy material. The PCB must have both a full ground plane layer and a full power plane layer. The required signal trace impedance is 55Ω ±15%. Components shall be of surface mount type, and may be mounted on one or both sides of the PCB.

Table 8: PCB Calculated Parameters

Parameter	Min	Max
Propagation delay: S_0 [ps/in] (outer layers)	141	153
Propagation delay: S_0 [ps/in] (inner layers)	167	180
Trace impedance: Z_0 [Ω] (all layers)	47	63

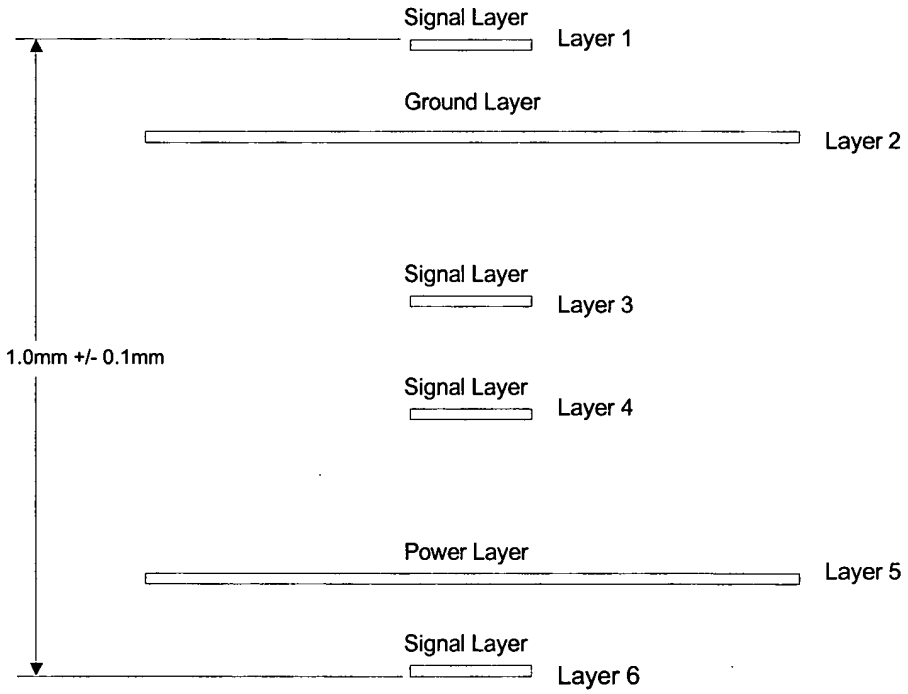

Figure 10: Example 6-layer PCB Stackup

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Edge Connection

The PCB edge connector contacts shall be gold plated per Figure 7, Note 7. Note: The PCB connector edge will not be chamfered.

EMI Reduction

To minimize radiation from clock traces on the SO-DIMMs, the following are requirements:

- Clocks must be routed with as much of the trace on an inner signal layer as possible.
- Clocks on the inner layer will have a 5 mill ground trace surrounding them, with vias stitched to ground at 0.5" intervals, or as often as routing allows.
- Both internal signal layers and the power plane should have a ground ring routed around the perimeter of the board and stitched to ground at intervals <0.5". The ground rings should be on the order of 20 mils wide, but can be reduced to 10 mils in areas where 20 mils cannot be accommodated.

Component Types and Placement

Components shall be of surface mount type, and may be mounted on one or both sides of the PCB. Components shall be positioned on the PCB to meet the min and max trace lengths required for SDRAM data signals. Bypass capacitors for SDRAM devices must be located as near as practical to the device power pins. It is also important to place each SDRAM in the optimum position to ensure meeting of trace length and topology requirements. Pin swapping of data pins within individual bytes should also be used for the same reason.

Exact spacing numbers are not provided, but are left up to the SO-DIMM manufacturer to determine based on manufacturing constraints and signal routing constraints imposed by this specification.

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Signal Groups

In this specification, the SDRAM timing-critical signals have been divided into groups whose members have identical loading and routing topologies. The following table summarizes the signal groups by listing the signals contained in each. The following sections will describe routing restrictions associated with each signal group.

Table 9: Signal Topology Categories

SIGNAL GROUP	SIGNALS IN GROUP
Clock	CLK [1:0]
Data	DQ [63:0]
Data Mask	DQMB [7:0]
Chip Select	S#[1:0]
Clock Enable	CKE[1:0]
Double cycle signals	A[12:0]
	BA[1:0]
	RAS#
	CAS#
	WE#

Signal Topology and Length Restrictions

In order to meet signal quality and setup/hold time requirements for the memory interface, certain routing topologies and trace length requirements must be met. The signal topology requirements are shown pictorially in the following pages. Each topology diagram is accompanied by a trace length table that lists the minimum and maximum lengths allowed for each trace segment and, where applicable, the min and max lengths for the entire net. Each diagram also shows where vias are allowed or includes a note that specifies where vias are allowed if they are not shown in the diagram.

Routing Rules

General Info: All signal traces except clocks are routed using 5/5 rules.
(5 mil traces and 5 mil minimum spacing between adjacent traces).

Clocks are routed using 5 mil traces and 5 mil space to the 5 mil ground trace.

No test points are required.

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Topology Diagram Explanation

The routing topology diagrams in this section are intended to be used to determine individual signal topologies on a SO-DIMM for any supported configuration.

These diagrams are read as follows:

Only the cylinders labeled with length designators represent actual physical trace segments. All other lines should be considered zero in length.

All loads and traces outside of the dashed boxes constitute the base topology which covers the minimum loading case for each signal.

Allowed vias are either shown as circles on the topology diagrams or are otherwise documented under each diagram in a separate note.

The topology for a given configuration can be determined by adding the traces and loads within the dashed boxes to the base topology. Add only the traces and loads within boxes that apply for the desired configuration.

The permitted segment length ranges for that topology are read from the table below each topology diagram.

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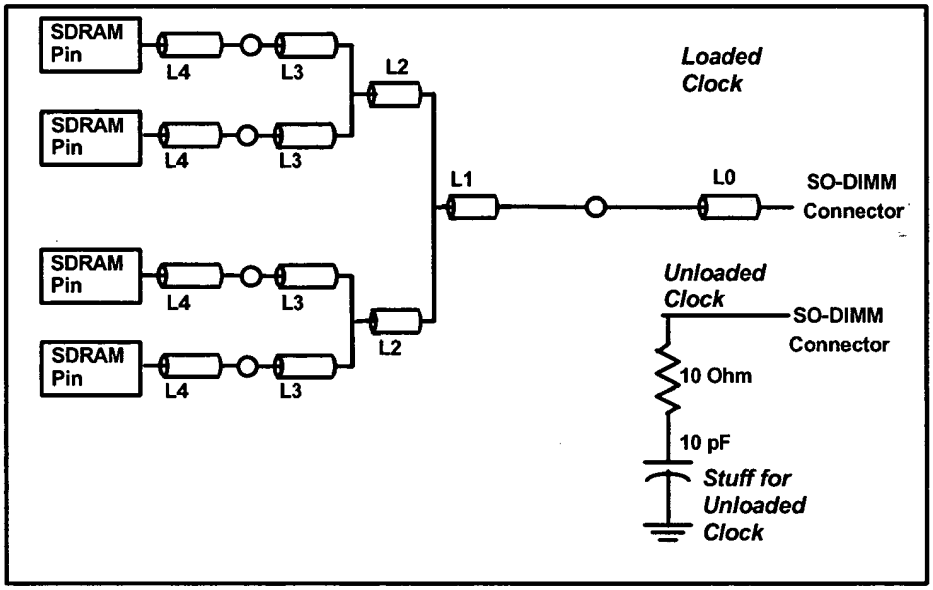
Topology for Clock: CLK[1:0]

Special attention must be given to the routing of the SDRAM clock signal(s) to ensure adequate signal quality, rise/fall time, minimum skew between clock edges at each SDRAM component, and predictable skew to motherboard chipset clocks. For that reason, all utilized clocks are made to look electrically similar by loading them with exactly four SDRAM loads. Clock signals must have either four SDRAM loads, or they must be terminated into 10 ohms and 10 pF. Trace lengths to the RC termination of unloaded clocks must be kept to an absolute minimum. Clock traces must be 5 mils wide with 15 mil spacing to any other signal including the clocks themselves.



Note: Either the L2 or the L3 trace segment may contain one additional via which is not shown in the diagram.

Figure 11: Signal routing topologies for Clocks

Table 10: Trace Length Table for Clock Topologies

Segment	L0	L1	L2	L3	L4	Total Min	Total Max
Length	0.10	1.00	0.80	0.50	0.10	2.45	2.55
Tolerance	± 0.05	± 0.02	± 0.02	± 0.02	± 0.05		
Layer	Outer	Inner	Inner	Inner	Outer		

1 All distances are given in inches and should be kept within tolerance, and routed on the indicated layer.
2 Total Min and Total Max refer to the min and max respectively of L0 + L1 + L2 + L3 + L4. Also, the total min and max limits are tighter than the sum of the individual min and max lengths. This implies that not all individual segment lengths may be adjusted to the min or max value at the same time.

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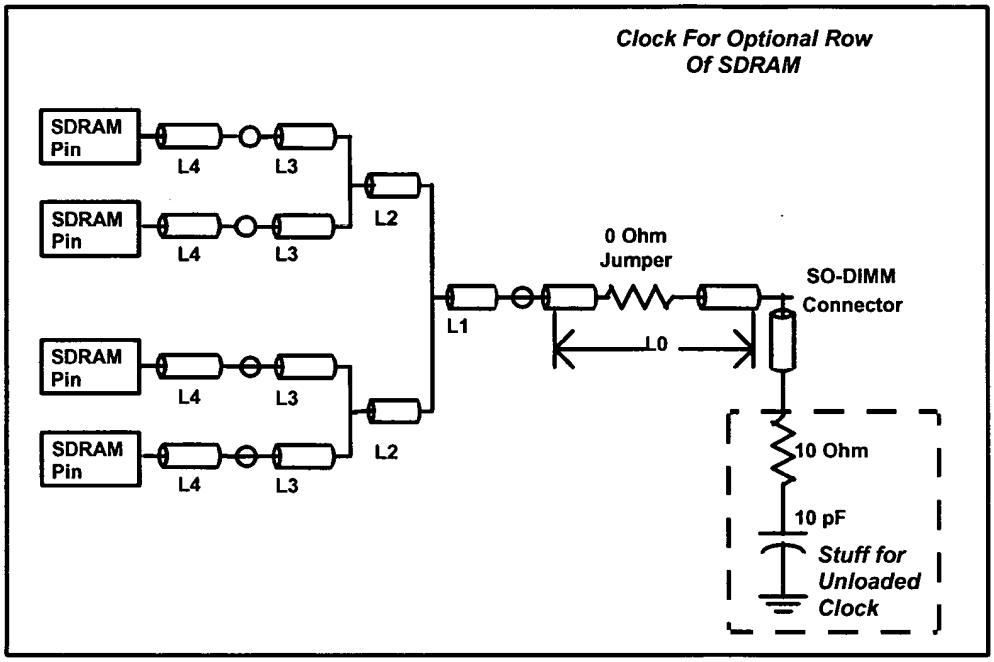
Topology for Clock with an option to not stuff a row of SDRAM: CLK[1]

If the PB is designed with the option to not stuff a row of SDRAM, a jumper must be included to disconnect the clock tree from the RC termination. The overall length of the net from the SO-DIMM pin to the SDRAM pin, through the jumper, must be the same as for clocks without this option. The diagram and table below explain this. In the picture, L0 is the sum of the trace lengths on both sides of the 0Ω jumper, and the distance through the 0Ω jumper. Trace lengths to the RC termination must be kept to an absolute minimum.



Note: Either the L2 or the L3 trace segment may contain one additional via which is not shown in the diagram.

Figure 12: Signal routing topologies for Clocks to Rows with Optional Stuffing

Table 11: Trace Length Table for Clocks to Rows with Optional Stuffing

Segment	L0	L1	L2	L3	L4	Total Min	Total Max
Length	0.25	0.85	0.80	0.50	0.10	2.45	2.55
Tolerance	± 0.05	± 0.02	± 0.02	± 0.02	± 0.05		
Layer	Outer	Inner	Inner	Inner	Outer		

1 All distances are given in inches and should be kept within tolerance, and routed on the indicated layer.
2 Total Min and Total Max refer to the min and max respectively of L0 + L1 + L2 + L3 + L4. Also, the total min and max limits are tighter than the sum of the individual min and max lengths. This implies that not all individual segment lengths may be adjusted to the min or max value at the same time.

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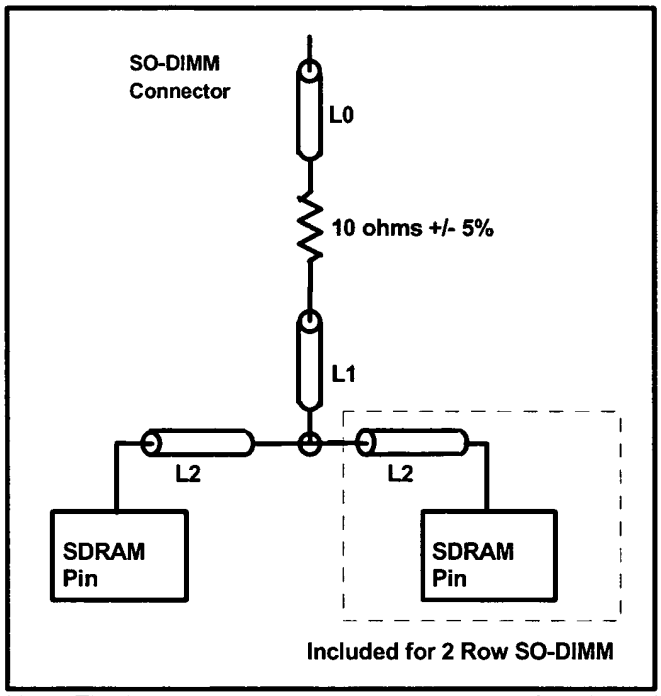
Topology for Data: DQ[63:0]

These signals are routed using a balanced "T" topology on any layer. The table defines the line length ranges allowed for these signals.

Figure 13: Signal routing topologies for Data



Note: The L1 trace segment may contain up to 2 additional vias which are not shown in the diagram.

Table 12: Trace Length Table for Data Topologies

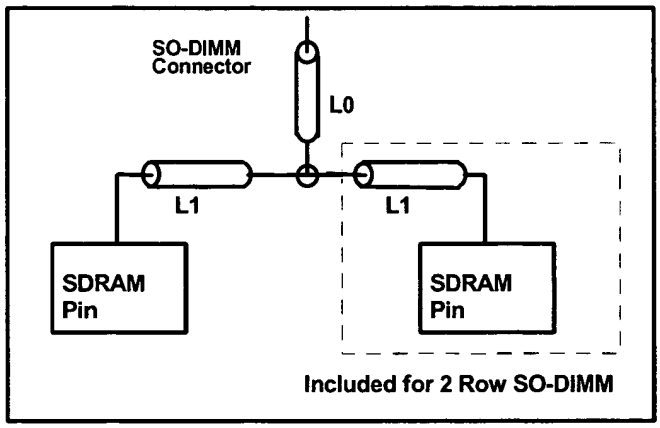
Comp Width	# of loads	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max	Total Min	Total Max
X16	1/2	0.10	0.50	0	0.90	0	0.25	0.60	1.00

1 All distances are given in inches
2 Total Min and Total Max refer to the min and max respectively of L0 + L1 + L2. Also, the total min and max limits are tighter than the sum of the individual min and max lengths. This implies that not all individual segment lengths may be adjusted to the min or max value at the same time.

Petitioners
Ex. 1010, p. 75

Topology for Data Mask: DQMB[7:0]

These signals are routed using a balanced "T" topology on any layer. The tables define the line length ranges allowed for these signals.



Note: The L0 trace segment may contain 1 additional via which is not shown in the diagram.

Figure 14: Signal routing topologies for Data Mask (1/2 Loads)

Table 13: Trace Length Table for Data Mask Topologies (1/2 Loads)

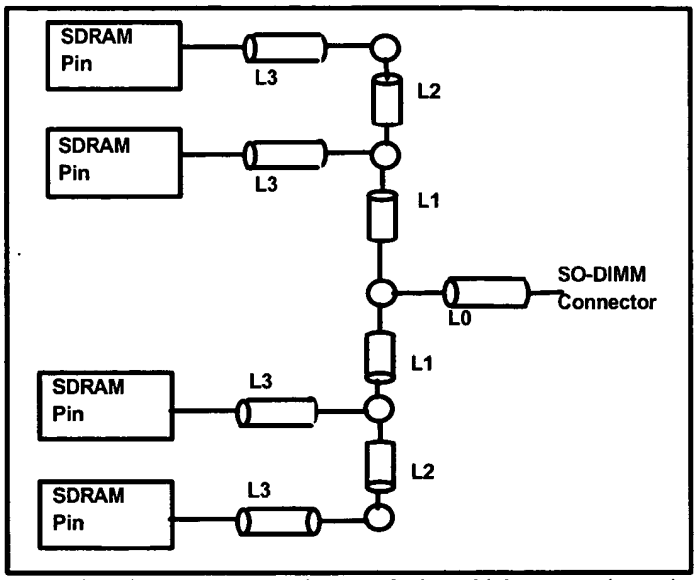
Comp Width	# loads	L0 Min	L0 Max	L1 Min	L1 Max	Total Min	Total Max
X16	1/2	0.75	1.10	0.00	0.30	1.00	1.40

1 All distances are given in inches

Petitioners
Ex. 1010, p. 76

Topology for Chip Select: S#[1:0]

This signal is routed using a balanced "comb" topology on any layer. The table below defines the line length ranges allowed for these signals.



Note: The L0 trace may contain up to 2 vias which are not shown in the diagram.

Figure 15: Signal routing topologies for Chip Select

Table 14: Trace Length Table for Chip Select Topologies

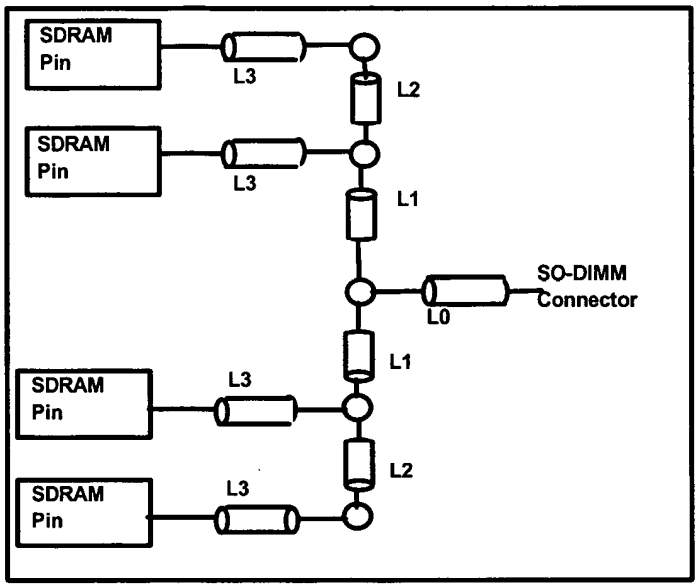
Comp Width	# of loads	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max	L3 Min	L3 Max	Total Min	Total Max
x16	4	0.50	1.10	0.10	0.50	0.0	0.60	0.05	0.35	1.00	2.30

1 All distances are given in inches.
2 Total distance is L0+L1+L3 or L0+L1+L2+L3. SO-DIMM connector to SDRAM Pin.

Petitioners
Ex. 1010, p. 77

Topology for Clock Enable: CKE#[1:0]

This signal is routed using a balanced "comb" topology on any layer. The table below defines the line length ranges allowed for each trace segment.



Note: The L0 trace may contain up to 2 vias which are not shown in the diagram.

Figure 16: Signal routing topologies for Clock Enable

Table 15: Trace Length Tables for Clock Enable Topologies

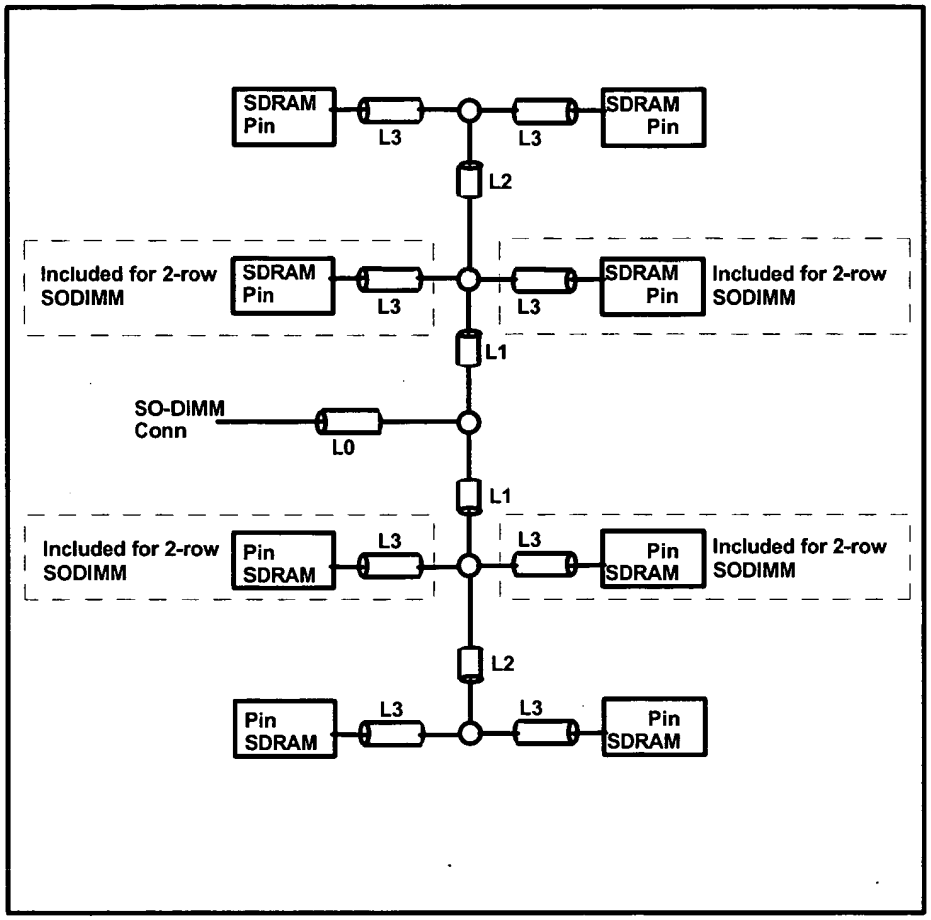
Comp Width	# of loads	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max	L3 Min	L3 Max	Total Min	Total Max
x16	4	0.50	1.10	0.0	0.50	0.0	1.00	0.05	0.35	1.0	2.3

1 All distances are given in inches.
2 Total distance is L0+L1+L3 or L0+L1+L2+L3. SO-DIMM connector to SDRAM Pin.

Petitioners
Ex. 1010, p. 78

Double Cycle Signals: MAx, BAx, SRAS#, SCAS#, WE#

These signals are routed using a balanced, double-sided "comb" topology on any layer. The table below defines the line length ranges allowed for these signals.



Note: The L0 trace may contain up to 2 vias which are not shown in the diagram.

Figure 17: Signal routing topologies for Double Cycle Signals

Table 16: Trace Length Table for Double Cycle Signal Topologies

Comp Width	# of loads	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max	L3 Min	L3 Max	Total Min	Total Max
x16	4/8	0.50	2.50	0.0	1.10	0.0	1.00	0.10	0.40	0.75	4.0

1 All distances are given in inches
2 Total distance is L0+L1+L3 or L0+L1+L2+L3. SO-DIMM connector to SDRAM Pin.

Petitioners
Ex. 1010, p. 79

7.0 SO-DIMM PCB and Final Assembly Labeling Requirements

Printed Circuit Board Labeling

The printed circuit board is required to have the following labeling contained in etch or silk-screen:

Vendor name and part number
Flammability indicator (see Section 2 of this document, under Safety)
The text: SO-DIMM-REV#.#
(#.# corresponds to the revision of this SO-DIMM spec to which the PCB is designed)

Assembled SO-DIMM Naming Convention

In order to be able to visually identify the critical parameters of a given SO-DIMM, the following naming convention will be used.

On component or sticker on DIMM (supplier option):
- use minimum 8point font

PCX-abc-def
Where X=MHz
a = CL value
b = trcd value
c = trp value
d = tac value
e = spd rev #
f = reserved

Example: PC100-322-620
is 100MHz, CL3, trcd=2, trp=2, tac=6, 2= spd rev 1.2 with the last digit reserved.

Note: A two digit designator for both the tac and spd fields is optional if appropriate.

Example: PC100-322-06120
is also 100MHz, CL3, trcd=2, trp=2, tac=6, 12= spd rev 1.2 with the last digit reserved.

8.0 SDRAM Component Specifications

The SDRAM components used with this 66/100 MHz SO-DIMM design spec MUST adhere to the most recent revision of the Intel "PC SDRAM Specification." Please refer to that document for all technical specifications and requirements of the SDRAM devices. Any violation of the requirements of the Intel PC SDRAM Component Specification constitutes a violation of the 66/100 MHz PC SDRAM Unbuffered SO-DIMM Specification.

9.0 EEPROM Component Specifications

The Serial Presence Detect function MUST be implemented on the PC SDRAM SO-DIMM. The component used and the data contents must adhere to the most recent version of the Intel "SDRAM Serial Presence Detect Specification". At the time of this writing, the current revision is 1.2A. Please refer to that document for all technical specifications and requirements of the serial presence detect devices. Any violation of the requirements of the Intel SDRAM Serial Presence Detect specification constitutes a violation of the PC SDRAM Unbuffered SO-DIMM Specification.

Petitioners
Ex. 1010, p. 80

OIPE IAP75
SEP 06 2005
PATENT & TRADEMARK OFFICE

PATENT

Case Docket No. NETL.018A
Date: September 1, 2005

TRANSMITTAL LETTER
RESPONSE TO MISSING PARTS

Applicant	:	J. Bhakta, et al.
App. No	:	11/075,395
Filed	:	March 7, 2005
For	:	HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS
Art Unit	:	2186

CERTIFICATE OF MAILING

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

September 1, 2005
(Date)

Bruce S. Itchkawitz, Reg. No. 47,677

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Notice to File Missing Parts of Nonprovisional Application Filed Under 37 CFR 1.53(b), which was mailed by the Office on April 7, 2005, enclosed are:

(X) An executed Declaration by Inventor(s).

(X) A Power of Attorney and copy of Assignment.

(X) A copy of the Notice to File Missing Parts.

(X) Return prepaid postcard.

(X) Fees as calculated below:

09/07/2005 CNGUYEN2 00000001 11075395
07 FC:1253 1020.00 OP

Case Docket No. NETL.018A
Date: September 1, 2005

FEE CALCULATION				
FEE TYPE		**FEE CODE**	**CALCULATION**	**TOTAL**
Basic Utility	37 CFR § 1.16(a)	1011 ($300)		$300
Search Fee		1111 ($500)		$500
Examination Fee		1311 ($200)		$200
Excess Claims > 20	27 - 20 = 7	1202 ($50)	7 x 50 =	$350
Independent > 3	6 - 3 = 3	1201 ($200)	3 x 200 =	$600
Multiple Claim		1203 ($360)		$0
Application Size Fee	43 - 100 = 0	1081 ($250)	0 x 250 =	$0
Surcharge	37 CFR § 1.16(e)	1051 ($130)		$130
1 Month Extension		1251 ($120)		$
2 Month Extension		1252 ($450)		$
3 Month Extension		1253 ($1,020)		$1,020
4 Month Extension		1254 ($1,590)		$
			SUB TOTAL	$
The present application qualifies for Small Entity status under 37 CFR § 1.27. **Fee reduced by 1/2.**				($0)
Non-English Spec.		1053 ($130)		$0
			TOTAL FEE DUE	**$3,100**

(X) A check in the amount of $3,100 to cover the above fees is enclosed.

The Commissioner is hereby authorized to charge any additional fees which may be required, now or in the future, or credit any overpayment, to Account No. 11-1410.

Bruce S. Itchkawitz
Registration No. 47,677
Attorney of Record
Customer No. 20,995
(949) 760-0404

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090105

1FW/$

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

OIPE
SEP 06 2005
PATENT & TRADEMARK OFFICE

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/075,395	03/07/2005		NETL.018A

CONFIRMATION NO. 8121

FORMALITIES LETTER

OC000000015683232

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

Date Mailed: 04/07/2005

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  Applicant must submit $ **300** *to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).*
- The oath or declaration is missing. *A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.*
  Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(f) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Additional claim fees of **$950** as a non-small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$2080** for a Large Entity

09/07/2005 CNGUYEN2 00000001 11075395

01 FC:1011	300.00 OP
02 FC:1111	500.00 OP
03 FC:1311	200.00 OP
04 FC:1201	600.00 OP
05 FC:1202	350.00 OP
06 FC:1051	130.00 OP

- **$300** Statutory basic filing fee.
- **$130** Late oath or declaration Surcharge.

- The application search fee has not been paid. Applicant must submit **$500** to complete the search fee.
- The application examination fee has not been paid. Applicant must submit **$200** to complete the examination fee for a large entity

- Total additional claim fee(s) for this application is **$950**

  - **$600** for **3** independent claims over 3.
  - **$350** for **7** total claims over 20.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

A copy of this notice MUST be returned with the reply.

Office of Initial Patent Examination (703) 308-1202

PART 2 - COPY TO BE RETURNED WITH RESPONSE

OIPE IAP75 SEP 06 2005 PATENT & TRADEMARK OFFICE

DECLARATION - USA PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are as stated below next to my name;

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS; the specification of which was filed on **March 7, 2005** as Application Serial No. **11/075,395**.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims;

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56;

I hereby claim the benefit under Title 35, United States Codes § 119(e) of any United States provisional applications listed below.

Application No.: 60/550,668	Filing Date: March 5, 2004
Application No.: 60/575,595	Filing Date: May 28, 2004
Application No.: 60/590,038	Filing Date: July 21, 2004

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole inventor: **Jayesh R. Bhakta**

Inventor's signature Jayesh R. Bhakta

Date June 21, 2005

Residence: **12220 Rose Street, Cerritos, California 90703**

Citizenship: **United States**

Mailing Address: **Same**

BEST AVAILABLE COPY

Full name of second inventor: **Jeffrey Solomon**

Inventor's signature _____

Date 6-21-05

Residence: **16 Silver Fir, Irvine, California 92604**

Citizenship: **United States**

Mailing Address: **Same**

Full name of third inventor: **William M. Gervasi**

Inventor's signature _____

Date 11 APRIL 05

Residence: **19 Half Moon Trail, Ladera Ranch, California 92694**

Citizenship: **United States**

Mailing Address: **Same**

Send Correspondence To:
KNOBBE, MARTENS, OLSON & BEAR, LLP
Customer No. 20,995

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032505

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OIPE IAP15
SEP 06 2005
PATENT & TRADEMARK OFFICE

ETL.018A PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jayesh R. Bhakta et al.
App. No.	:	11/075,395
Filed	:	March 7, 2005
For	:	HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS
Examiner	:	Unknown

ESTABLISHMENT OF RIGHT OF ASSIGNEE TO TAKE ACTION
AND
REVOCATION AND POWER OF ATTORNEY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The undersigned is empowered to act on behalf of the assignee below (the "Assignee"). A true copy of the original Assignment of the above-captioned application from the inventors to the Assignee is attached hereto. This Assignment represents the entire chain of title of this invention from the Inventors to the Assignee.

I declare that all statements made herein are true, and that all statements made upon information and belief are believed to be true, and further, that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that willful, false statements may jeopardize the validity of the application, or any patent issuing thereon.

App. No. : 11/075,395
Filed : March 7, 2005

The undersigned hereby revokes any previous powers of attorney in the subject application, and hereby appoints the registrants of Knobbe, Martens, Olson & Bear, LLP, **Customer No. 20,995**, as its attorneys with full power of substitution and revocation to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected herewith. This appointment is to be to the exclusion of the inventors and their attorney(s) in accordance with the provisions of 37 C.F.R. § 3.71.

Please use **Customer No. 20,995** for all communications.

NETLIST, INC.

Dated: 08/23/05

By: _____
Christopher Lopes

Title: Vice President

Address: 475 Goddard, Suite 100
Irvine, California 92618

1443236_1
032505

COPY

ASSIGNMENT

WHEREAS, We, Jayesh R. Bhakta, a United States citizen, residing at 12220 Rose Street, Cerritos, California 90703, Jeffrey Solomon, a United States citizen, residing at 16 Silver Fir, Irvine, California 92604, and William M. Gervasi, a United States citizen, residing at 19 Half Moon Trail, Ladera Ranch, California 92694, have invented certain new and useful improvements in a HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS for which we have filed an application for Letters Patent in the United States, Application No. 11/075,395, filed on March 7, 2005;

AND WHEREAS, Netlist, Inc. (hereinafter "ASSIGNEE"), a Delaware corporation, with its principal place of business at 475 Goddard, Suite 100, Irvine, California 92618, desires to acquire the entire right, title, and interest in and to the said improvements and the said Application:

NOW, THEREFORE, in return for good and valuable consideration, the receipt of which is hereby acknowledged, we, the said inventors, do hereby acknowledge that we have sold, assigned, transferred and set over, and by these presents do hereby sell, assign, transfer and set over, unto the said ASSIGNEE, its successors, legal representatives and assigns, the entire right, title, and interest throughout the world in, to and under the said improvements, and the said application and all provisional applications relating thereto, and all divisions, renewals and continuations thereof for said improvements, and all Letters Patent of the United States which may be granted thereon and all reissues and extensions thereof, and all rights of priority under International Conventions and applications for Letters Patent which may hereafter be filed for said improvements in any country or countries foreign to the United States, and all Letters Patent which may be granted for said improvements in any country or countries foreign to the United States and all extensions, renewals and reissues thereof; and we hereby authorize and request the Commissioner of Patents of the United States, and any Official of any country or countries foreign to the United States, whose duty it is to issue patents on applications as aforesaid, to issue all Letters Patent for said improvements to the said ASSIGNEE, its successors, legal representatives and assigns, in accordance with the terms of this instrument.

AND WE HEREBY covenant and agree that we will communicate to the said ASSIGNEE, its successors, legal representatives and assigns, any facts known to us respecting said improvements, and testify in any legal proceeding, sign all lawful papers, execute all divisional, continuing and reissue applications, make all rightful oaths and generally do everything possible to aid the said ASSIGNEE, its successors, legal representatives and assigns, to obtain and enforce proper patent protection for said improvements in all countries.

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 22 day of Aug., 2005.

Jayesh R. Bhakta

Jayesh R. Bhakta

STATE OF CALIFORNIA }
} ss.
COUNTY OF ORANGE }

On 22 AUG, 2005, before me, JOHN HARO, personally appeared Jayesh R. Bhakta ~~personally known to me~~ (or proved to me on the basis of satisfactory evidence) to be the person(s) whose name(s) is/are subscribed to the within instrument, and acknowledged to me that he executed the same in his authorized capacity(ies), and that by his signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

WITNESS my hand and official seal.

[SEAL]

Notary Signature

JOHN HARO
COMM...1473694
NOTARY PUBLIC-CALIFORNIA
ORANGE COUNTY
My Comm. Exp. March 2, 2008

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 22nd day of August, 2005.

Jeffrey Solomon

STATE OF CALIFORNIA }
COUNTY OF ORANGE } ss.

On 22ND AUG, 2005, before me, JOHN HARO, personally appeared Jeffrey Solomon ~~personally known to me~~ (or proved to me on the basis of satisfactory evidence) to be the person(s) whose name(s) is/are subscribed to the within instrument, and acknowledged to me that he executed the same in his authorized capacity(ies), and that by his signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

WITNESS my hand and official seal.

[SEAL]

JOHN HARO
COMM...1473694
NOTARY PUBLIC-CALIFORNIA
ORANGE COUNTY
My Comm. Exp. March 2, 2008

Notary Signature

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 29 day of APRIL, 2005.

William M. Gervasi

STATE OF California }
COUNTY OF Orange } ss.

On 4-29, 2005, before me, Nikki B. Ramos, personally appeared William M. Gervasi personally known to me (or proved to me on the basis of satisfactory evidence) to be the person(s) whose name(s) is/are subscribed to the within instrument, and acknowledged to me that he executed the same in his authorized capacity(ies), and that by his signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

WITNESS my hand and official seal.

[SEAL]

Notary Signature

NIKKI B. RAMOS
Commission # 1401793
Notary Public - California
Orange County
My Comm. Expires Feb 22, 2007

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042705

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
11/075,395		2824	2818

Correspondence Address / Fee Address Change

The following fields have been set to Customer Number 20995 on 12/08/2005

- Correspondence Address
- Maintenance Fee Address

The address of record for Customer Number 20995 is:
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE,CA 92614

IFW

Docket No.: NETL.018A

April 7, 2006
Page 1 of 1

OIPE IAP85
APR 11 2006
PATENT & TRADEMARK OFFICE

Please Direct All Correspondence to Customer Number **20995**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jayesh R. Bhakta et al.
App. No	:	11/075,395
Filed	:	March 7, 2005
For	:	HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS
Examiner	:	Richard T. Elms
Art Unit	:	2824

CERTIFICATE OF MAILING

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

April 7, 2006
(Date)

Bruce S. Itchkawitz, Reg. No. 47,677

STATUS LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon review of our records and any available PAIR record, it appears there has been no action in the above-referenced application since March 7, 2005.

Please inform us as to the status of this application.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 4/7/06

By:

Bruce S. Itchkawitz
Registration No. 47,677
Attorney of Record
Customer No. 20,995
(949) 760-0404

2509516
040706

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

DATE: 04/23/2006

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

To: Applicant of Serial Number 11075395
Filed on 07-MAR-2005
(Art Unit 2824)

It is estimated that this application will receive an Office action in approximately 5 months. This is an estimate that is based on the current inventory level of applications filed in this art area and the current staffing levels in this Art Unit. The USPTO is dedicated to minimizing first action and total pendency, and we are targeting resources to help address backlogs in art areas with high new application filings. Thank you for your inquiry.

Customer Service Office in Technology Center: 2800

Phone Number: 571-272-2800
Central Fax Number: 571-273-8300

Applicant/Attorney Contact Information:

Phone Number:
Fax Number:

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/075,395	03/07/2005	Jayesh R. Bhakta	NETL.018A	8121

20995 7590 09/14/2006

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER
NGUYEN, VAN THU T

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 09/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	11/075,395	BHAKTA ET AL.	
	Examiner	Art Unit	
	VanThu Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) 1-27 are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

Petitioners
Ex. 1010, p. 95

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claim 1, drawn to format or disposition of elements, classified in class 365, subclass 51.

II. Claims 2-8, drawn to hardware for storage elements, classified in class 365, subclass 52.

III. Claims 9-18, drawn to bus or line termination, classified in class 326, subclass 30.

IV. Claims 19-25, drawn to addressing, classified in class 365, subclass 230.01.

V. Claim 26, drawn to particular decoder or driver circuit, classified in class 365, subclass 230.06.

VI. Claim 27, drawn to particular decoder or driver circuit, classified in class 365, subclass 230.06.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I are II/III/IV/V/VI related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination I has separate utility such as each pair of memory components simulating a single virtual memory component. See MPEP § 806.05(d).

3. Inventions II are III/IV/V/VI related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the

instant case, subcombination II has separate utility such as first and second resistors connected between first and second data strobe pins. See MPEP § 806.05(d).

4. Inventions III are IV/V/VI related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination III has separate utility such as first and second termination circuits connected to a termination bus. See MPEP § 806.05(d).

5. Inventions IV are V/VI related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination IV has separate utility such as a serial-presence-detect (SPD) device. See MPEP § 806.05(d).

6. Inventions V are VI related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination VI has separate utility such as the first, second, third, fourth ranks are not tied in pair. See MPEP § 806.05(d).

7. The examiner has required restriction between subcombinations usable together. Where applicant elects a subcombination and claims thereto are subsequently found allowable, any claim(s) depending from or otherwise requiring all the limitations of the allowable subcombination will be examined for patentability in accordance with 37 CFR 1.104. See MPEP § 821.04(a). Applicant is advised that if any claim presented in a continuation or divisional

application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

8. Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required because the inventions have acquired a separate status in the art in view of their different classification and fields of search, restriction for examination purposes as indicated is proper.

9. Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species or invention to be examined even though the requirement be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

The election of an invention or species may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse.

Should applicant traverse on the ground that the inventions or species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions or species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C.103(a) of the other invention.

10. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the

application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Thursday, 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

September 11, 2006

VanThu Nguyen
Primary Examiner
Art Unit 2824

OIPE
OCT 10 2006
PATENT & TRADEMARK OFFICE

Please Direct All Correspondence to Customer Number **20995**

AMENDMENT / RESPONSE TRANSMITTAL

Applicants	:	Jayesh R. Bhakta et al.
App. No.	:	11/075,395
Filed	:	March 7, 2005
For	:	HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS
Examiner	:	Van Thu T. Nguyen
Art Unit	:	2824

CERTIFICATE OF MAILING

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

October 5, 2006
(Date)

Bruce S. Itchkawitz, Reg. No. 47,677

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith for filing in the above-identified application are the following enclosures:

(X) Response to the September 14, 2006 Election/Restriction Requirement in seven (7) pages; and

(X) A return prepaid postcard.

The fee has been calculated as shown below:

FEE CALCULATION				
FEE TYPE		**FEE CODE**	**CALCULATION**	**TOTAL**
Excess Claims	20 - 27 = 0	1202 ($50)		N/A
Excess Independent	2 - 6 = 0	1201 ($200)		N/A
Multiple Claim	*1.16(j)*	1203 ($360)		N/A
1 Month Extension	*1.17(a)(1)*	1251 ($120)		N/A
2 Month Extension	*1.17(a)(2)*	1252 ($450)		N/A
3 Month Extension	*1.17(a)(3)*	1253 ($1,020)		N/A
IDS Fee	*1.17(p)*	1806 ($180)		N/A
			TOTAL FEE DUE	0

Please Direct All Correspondence to Customer Number **20995**

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Bruce S. Itchkawitz
Registration No. 47,677
Attorney of Record
Customer No. 20,995
(949) 760-0404

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OIPE IAP14
OCT 10 2006
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jayesh R. Bhakta et al.	Group Art Unit 2824
App. No.	:	11/075,395	
Filed	:	March 7, 2005	
For	:	HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS	
Examiner	:	Van Thu T. Nguyen	

RESPONSE TO THE SEPTEMBER 14, 2006 ELECTION/RESTRICTION REQUIREMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the September 14, 2006 Election/Restriction Requirement, Applicants request the Examiner to consider the above-identified patent application in view of the following amendments and remarks.

Amendments to the Claims: Begin on page 2 of this Response.

Remarks: Begin on page 3 of this Response.

Petitioners
Ex. 1010, p. 102

AMENDMENTS TO THE CLAIMS

Please cancel Claims 1-25 and 27 without prejudice, as indicated below.

Please amend Claim 26.

Please add new Claims 28-46.

A complete listing of all claims is presented below with insertions underlined (e.g., insertion), and deletions struckthrough or in double brackets (e.g., ~~deletion~~ or [[deletion]]):

1.-25. (Cancelled)

26. (Currently Amended) A memory module having a first memory capacity, the memory module comprising:

a plurality of substantially identical memory components configured as a first rank and a second rank, the memory components of the first rank configured in pairs, the memory components of each pair having ~~with~~ their respective data strobe pins in electrical communication with one another~~tied together~~, the memory components of the second rank configured in pairs, the memory components of each pair having ~~with~~ their respective data strobe pins in electrical communication with one another~~tied together~~; and

a logic element which receives a first set of address and control signals compatible with a second memory capacity, the second memory density substantially equal to one-half of the first memory capacity, wherein the logic element translates the first set of address and control signals into a second set of address and control signals compatible with the first memory capacity of the memory module, the logic element transmitting the second set of address and control signals to the first rank and the second rank.

27. (Cancelled)

28. (New) The memory module of Claim 26, wherein the memory components of each pair of memory components has a first bit width and each pair of memory components simulates a single virtual memory component having a second bit width which is twice the first bit width.

29. (New) The memory module of Claim 28, wherein the first bit width is 4 bits, 8 bits, or 16 bits.

30. (New) The memory module of Claim 26, wherein each of the memory components comprises a double-data-rate-1 (DDR-1), double-data-rate-2 (DDR-2), or double-data-rate-3 (DDR-3) dynamic random-access memory (DRAM) integrated circuit.

31. (New) The memory module of Claim 26, wherein each of the memory components comprises ball-grid-array (BGA) packaging.

32. (New) The memory module of Claim 31, wherein each of the memory components comprises fine-pitch BGA (FBGA) packaging.

33. (New) The memory module of Claim 26, wherein each of the memory components comprises a synchronous dynamic random-access memory (SDRAM) integrated circuit.

34. (New) The memory module of Claim 26, further comprising a termination bus, each pair of memory components comprising a first memory component having a first data strobe pin, a first termination signal pin in electrical communication with the termination bus, a first termination circuit, and at least one data pin, wherein the first termination circuit selectively electrically terminates the first data strobe pin and the at least one data pin of the first memory component in response to a first signal received by the first termination signal pin from the termination bus.

35. (New) The memory module of Claim 34, wherein each pair of memory components comprises a second memory component having a second data strobe pin in electrical communication with the first data strobe pin, a second termination signal pin, a second termination circuit, and at least one data pin, wherein the second termination circuit is responsive to a voltage applied to the second termination signal pin by not terminating the second data strobe pin or the at least one data pin of the second memory component.

36. (New) The memory module of Claim 35, further comprising at least one termination assembly having a third termination signal pin, a third termination circuit, and at least one termination pin electrically coupled to the at least one data pin of the second memory component, the third termination signal pin in electrical communication with the termination bus, wherein the third termination circuit selectively electrically terminates the at least one data pin of the second memory component through the termination pin in response to a second signal received by the third termination signal pin from the termination bus.

37. (New) The memory module of Claim 36, wherein the first signal and the second signal are the same signal.

38. (New) The memory module of Claim 36, wherein the termination bus comprises an on-die termination (ODT) bus, and each of the first termination circuit, second termination circuit, and third termination circuit comprises an ODT circuit.

39. (New) The memory module of Claim 36, wherein the voltage is ground.

40. (New) The memory module of Claim 26, wherein each memory component has a first bit width, a first number of banks of memory locations, a first number of row address bits, and a first number of column address bits, the memory module further comprising a serial-presence-detect (SPD) device comprising data that characterizes each pair of memory components as a virtual memory component having a second bit width equal to twice the first bit width, a second number of banks of memory locations equal to the first number of banks, a second number of row address bits equal to the first number of row address bits, and a second number of column address bits equal to the first number of column address bits.

41. (New) The memory module of Claim 40, wherein byte 3 of the SPD data comprises the first number of row address bits, byte 4 of the SPD data comprises the first number of column address bits, byte 13 of the SPD data comprises the second bit width, byte 14 of the SPD data comprises the second bit width, and byte 17 of the SPD data comprises the first number of banks.

42. (New) The memory module of Claim 41, wherein the first bit width is 4 bits.

43. (New) The memory module of Claim 41, wherein the first bit width is 8 bits.

44. (New) The memory module of Claim 40, wherein the memory module has a 1-GB (128M x 8-byte) configuration, and comprises eight pairs of memory components, each memory component having a 512-Mb (128M x 4-bit) configuration, wherein the second bit width is 8 bits, the first number of row address bits is 13, and the second number of column address bits is 12.

45. (New) The memory module of Claim 41, wherein the SPD device comprises an electrically-erasable programmable read-only memory (EEPROM) device.

46. (New) A method of providing memory to a computer system, the method comprising:

providing a memory module having a first memory capacity, the memory module comprising a plurality of substantially identical memory components configured as a first rank and a second rank, the memory components of the first rank configured in pairs, the

memory components of each pair having their respective data strobe pins in electrical communication with one another, the memory components of the second rank configured in pairs, the memory components of each pair having their respective data strobe pins in electrical communication with one another; and

receiving at the memory module a first set of address and control signals compatible with a second memory capacity, the second memory density substantially equal to one-half of the first memory capacity;

translating the first set of address and control signals into a second set of address and control signals compatible with the first memory capacity of the memory module; and

transmitting the second set of address and control signals to the first rank and the second rank.

REMARKS

The foregoing amendments and the following remarks are responsive to the September 14, 2006 Election/Restriction Requirement. Claims 1-25 and 27 are cancelled without prejudice, Claim 26 remains as originally filed, and Claims 28-46 are added. Thus, Claims 26 and 28-46 are presented for further consideration. Please enter the amendments and consider the claims in view of the following remarks.

Response to Election/Restriction Requirement

In the September 14, 2006 Election/Restriction Requirement, the Examiner has required restriction to one of six inventions:

> Group I (Claim 1), drawn to format or disposition of elements, classified in Class 365, Subclass 51;
> Group II (Claims 2-8), drawn to hardware for storage elements, classified in Class 365, Subclass 52;
> Group III (Claims 9-18), drawn to bus or line termination, classified in Class 326, Subclass 30;
> Group IV (Claims 19-25), drawn to addressing, classified in Class 365, Subclass 230.01;
> Group V (Claim 26), drawn to particular decoder or driver circuit, classified in Class 365, Subclass 230.06; and
> Group VI (Claim 27), drawn to particular decoder or driver circuit, classified in Class 365, Subclass 230.06..

Applicants hereby elect, without traverse, to prosecute the claims directed to Group V (Claim 26), classified in Class 365, Subclass 230.06, in the present application. Please cancel nonelected Claims 1-25 and 27 without prejudice. Applicants reserve the right to pursue the nonelected claims in one or more continuing applications.

Applicants have also added new Claims 28-45, each of which depends from Claim 26 directly or indirectly, and new Claim 46 which is a method claim. Applicants submit that new Claims 28-46 are also in the elected Group V and do not add new matter to the present application. Applicants respectfully request that the Examiner consider the allowability of new Claims 28-46.

Summary

Applicants respectfully submit that the foregoing is fully responsive to the election/restriction requirement. Accordingly, prompt examination on the merits of Claims 26 and 28-46 is respectfully requested. If, however, any issues remain, the Examiner is respectfully requested to call Applicants' counsel at the number provided below to resolve such issues promptly.

Please charge any additional fees, including any fees for additional extensions of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 10/5/06

By: _____

Bruce S. Itchkawitz
Registration No. 47,677
Attorney of Record
2040 Main Street
Fourteenth Floor
Irvine, CA 92614
(949) 760-0404

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PTO/SB/06 (12-04)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 11/075,395

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))							
SEARCH FEE (37 CFR 1.16(k), (i), or (m))							
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	x 25 =		OR	x 50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	x 100 =			x 200 =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			180			360	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

10-10-06

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 27	=	x 25 =		OR	x 50 =	
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 6	=	x 100 =		OR	x 200	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					180		OR	360	
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

CLAIMS ONLY

Application Number: 11/075395

Filing Date:

Applicant(s):

* May be used for additional claims or amendments

CLAIMS	AS FILED		AFTER FIRST AMENDMENT		AFTER SECOND AMENDMENT		*		*		*	
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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L9	12	(termination adj2 pin$1) and (memory adj module$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/19 15:10
L12	3	(termination adj2 pin$1) and (memory adj chip)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/19 15:12
L13	19	(ODT$2 adj2 pin$1) and (memory adj2 (chip$1 or module$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/19 15:13
L15	19	(BHAKTA-JAYESH$3.in. or SOLOMON-JEFFREY.in. or GERVASI-WILLIAM$3.in.) and (memory adj module$1).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/19 15:44
L16	1	(translate$1 with first with set with address with second with compatible). clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/19 15:45
S69	23	virtual with width with twice	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/18 20:19
S71	122	virtual same (bit or band) same width same (twice or double or half)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/18 20:21
S72	106	S71 and @ad<"20040325"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/19 13:28
S74	19	(("5,247,643") or ("5,703,826") or ("6,154,418") or ("6,453,381") or ("6,518,794") or ("6,681,301") or ("6,785,189") or ("6,807,125") or ("6,813,196")).PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/18 20:37

EAST Search History

S76	15	"20010052057" or "20020088633" or "20030063514" or "20030191995" or "20030210575" or "20040037158" or "20050036378"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/18 20:36
S77	10	(mirror with (chip or IC)) and (virtual adj2 address$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/18 20:39
S78	10	S77 and @ad<"20040325"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/18 20:39
S79	9	("4724531" | "4994896" | "5502621" | "5579277").PN. OR ("5805520").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/12/18 20:45
S80	19	("5095407" | "5164916" | "5502621" | "5579277" | "5699315" | "5805520" | "5808897" | "5841686" | "5941447" | "5950220" | "5982655" | "5996880" | "6003130" | "6021459" | "6128244" | "6161177" | "6182213" | "6229727" | "RE36229").PN. OR ("7124223"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/12/18 20:50
S86	120	termination with data with strobe	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/19 13:43
S87	95	S86 and @ad<"20040325"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/19 14:46

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/075,395	03/07/2005	Jayesh R. Bhakta	NETL.018A	8121

20995 7590 01/02/2007
KNOBBE MARTENS OLSON & BEAR LLP
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FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER
NGUYEN, VAN THU T

ART UNIT	PAPER NUMBER
2824	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	01/02/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 01/02/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jcartee@kmob.com
eOAPilot@kmob.com

Office Action Summary	Application No.	Applicant(s)	
	11/075,395	BHAKTA ET AL.	
	Examiner	Art Unit	
	VanThu Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26 and 28-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26 and 28-33* is/are rejected.

7)☒ Claim(s) *34-45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/08/2005*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

Petitioners
Ex. 1010, p. 114

DETAILED ACTION

Election/Restrictions

1. Applicants' election without traverse of Group V, claim 26 and newly added claims 28-45, in the reply filed on 10/10/2006 is acknowledged. Claims 1-25 and 27 have been cancelled.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 26, 28-30, 33 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,944,694 to Pax (Pax).

Regarding claim 26, Pax discloses a memory module having a first memory capacity, the memory module comprising:

- a plurality of substantially identical memory components (see FIGs. 1-3) configured as a first rank and a second rank (each pair of the memory chips 104B-104B forms a rank), the memory components of the first rank configured in pairs with their respective data strobe pins tied together, the memory components of the second rank configured in pairs with their respective data strobe pins tied together (see FIG. 3); and

- a logic element (reroute multiplexer 500, see FIG. 9) which receives a first set of address (e.g. address signals A0-A3, see FIG. 5) and control signals (e.g. signals S0 and Clock, see FIG. 9) compatible with a second memory capacity (memory capacity of a single memory chip), the second memory density substantially equal to one-half of the first memory capacity (memory capacity of one memory chip and its mirror chip), wherein the logic element translates the first set of address and control signals into a second set of address and control signals compatible with the first memory capacity of the memory module (see FIG. 9), the logic element transmitting the second set of address and control signals to the first rank and the second rank (see column 8, lines 14-32).

Regarding claim 28, Pax discloses wherein the memory components of each pair of memory components has a first bit width (e.g. bit width of A0-A3) and each pair of memory components simulates a single virtual memory component having a second bit width (e.g. bit of S0, A0-A3) which is twice the first bit width.

Regarding claims 29-30, 33, Pax discloses the first bit width is 4 bits (A0-A3); the memory chips are SDRAM (see column 9, lines 34-43);

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pax.

Regarding claims 31-32, Pax does not mention that each of memory components comprising fine-pitch BGA (FPBGA) packaging.

However, it would have been obvious to one with ordinary skill in the art to use the FPBGA packaging for memory chips disclosed in Pax because it is well-known chip package in memory technology.

Allowable Subject Matter

6. Claims 34-45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Pax, Doblar et al. (US 6,996,686), and Anglada et al. (US 5,805,520) taken individually or in combination, do not teach the claimed invention having the following limitations, in combination with the remaining claimed limitations:

- **As in claim 34-39**: wherein the first termination circuit selectively electrically terminates the first data strobe pin and the at least one data pin of the first memory component in response to a first signal received by the first termination signal pin from the termination bus; or
- **As in claims 40-45**: further comprising a serial-presence-detect (SPD) device comprising data that characterizes each pair of memory components as a virtual

memory component having a second bit width equal to twice the first bit width, a second number of banks of memory locations equal to the first number of banks, a second number of row address bits equal to the first number of row address bits, and a second number of column address bits equal to the first number of column address bits.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Thursday, 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

December 19, 2006

VanThu Nguyen
Primary Examiner
Art Unit 2824

OIPE JC99
AUG 0 8 2005
PATENT & TRADEMARK OFFICE

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	11/075,395
	Filing Date	March 7, 2005
	First Named Inventor	Jayesh R. Bhakta
	Art Unit	~~2186~~ 2824
(Multiple sheets used when necessary)	Examiner	~~Unknown~~ VanThu Nguyen
SHEET 1 OF 2	Attorney Docket No.	NETL.018A

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Publication Date	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
VTN	1	5,247,643	09/21/1993	Shottan	
	2	5,703,826	12/30/1997	Hush et al.	
	3	6,154,418	11/28/2000	Li	
	4	6,453,381 B1	09/17/2002	Yuan et al.	
	5	6,518,794 B2	02/11/2003	Coteus et al.	
	6	6,681,301 B1	01/20/2004	Mehta et al.	
	7	6,785,189 B2	08/31/2004	Jacobs et al.	
	8	6,807,125 B2	10/19/2004	Coteus et al.	
	9	6,813,196 B2	11/02/2004	Park et al.	
	10	2001/0052057 A1	12/13/2001	Lai et al.	
	11	2002/0088633 A1	07/11/2002	Kong et al.	
	12	2003/0063514 A1	04/03/2003	Faue	
	13	2003/0191995 A1	10/09/2003	Abrosimov et al.	
	14	2003/0210575 A1	11/13/2003	Seo et al.	
	15	2004/0037158 A1	02/26/2004	Coteus et al.	
VTN	16	2005/0036378 A1	02/17/2005	Kawaguchi et al.	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author, title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
VTN	17	CUPPU, Vinodh, et al., "A Performance Comparison of Contemporary DRAM Architectures," IEEE Proceedings of the 26th International Symposium on Computer Architecture, May 2-4, 1999, Atlanta, Georgia, pp. 1-12.	
	18	JEDEC Standard No. 21-C, 4.20-2 – 168 Pin, PC133 SDRAM Registered Design Specification, Revision 1.4, Release 11a, February 2002.	
	19	JEDEC Standard No. 21-C, 4.20-3 – 144 Pin, PC133 SDRAM Unbuffered SO-DIMM, Reference Design Specification, Revision 1.02, Release 11.	
	20	JEDEC Standard No. 21-C, DDR SDRAM PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, Revision 1.3, Release 11b, January 2002.	
	21	JEDEC Standard No. 21-C, 4.20.5 – 184 Pin, PC1600/2100 DDR SDRAM Unbuffered DIMM Design Specification, Revision 1.1, Release 11b.	
VTN	22	JEDEC Standard No. 21-C, 4.20.6 – 200 Pin, PC2700/PC2100/PC1600 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification, Revision 1.1, Release 11b, April 26, 2002.	

Examiner Signature	/Van Thu Nguyen/	Date Considered	12/18/2006

***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

T[1] - Place a check mark in this area when an English language Translation is attached.

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	11/075,395
	Filing Date	March 7, 2005
	First Named Inventor	Jayesh R. Bhakta
	Art Unit	~~2186~~ 2824
(Multiple sheets used when necessary)	Examiner	~~Unknown~~ VanThu Nguyen
SHEET 2 OF 2	Attorney Docket No.	NETL.018A

OIPE JC99 AUG 0 8 2005 PATENT & TRADEMARK OFFICE

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author, title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
VTN	23	JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published February 2004.	
VTN	24	INTEL CORPORATION, PC SDRAM Registered DIMM Design Support Document, Revision 1.2, October 1998.	
VTN	25	INTEL CORPORATION, 66/100 MHz PC SDRAM 64-Bit Non-ECC/Parity 144 Pin Unbuffered SO-DIMM Specification, Revision 1.0, February 1999.	

1707974
080505

Examiner Signature	/Van Thu Nguyen/	Date Considered	12/18/2006

***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

T[1] - Place a check mark in this area when an English language Translation is attached.

Notice of References Cited	Application/Control No. 11/075,395	Applicant(s)/Patent Under Reexamination BHAKTA ET AL.	
	Examiner VanThu Nguyen	Art Unit 2824	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,996,686 B2	02-2006	Doblar et al.	711/157
*	B	US-6,944,694 B2	09-2005	Pax, George E.	710/107
*	C	US-5,805,520 A	09-1998	Anglada et al.	365/230.02
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination
	11/075,395	BHAKTA ET AL.
	Examiner	**Art Unit**
	VanThu Nguyen	2824

SEARCHED			
Class	Subclass	Date	Examiner
365	230.01 230.02 x 230.06 x	12/19/2006	VTN
711	5 6	12/19/2006	VTN
711	211 x	12/19/2006	VTN

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST search, including inventors and interference searches (see print out history)	12/19/2006	VTN

OIPE IAP17 FEB 21 2007 PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jayesh R. Bhakta et al.	Group Art Unit 2824
Appl. No.	:	11/075,395	
Filed	:	March 7, 2005	
For	:	HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS	
Examiner	:	Van Thu T. Nguyen	

AMENDMENT AND RESPONSE TO JANUARY 2, 2007 OFFICE ACTION

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the January 2, 2007 Office Action, Applicants request the Examiner to reconsider the above-identified patent application in view of the following amendments and remarks.

Amendments to the Claims: Begin on page 2 of this Response.

Remarks: Begin on page 7 of this Response.

Petitioners
Ex. 1010, p. 124

AMENDMENTS TO THE CLAIMS

Please amend Claims 26, 34, 40, and 46 as indicated below.

A complete listing of all claims is presented below with insertions underlined (e.g., insertion), and deletions struckthrough or in double brackets (e.g., ~~deletion~~ or [[deletion]]):

1.-25. (Cancelled)

26. (Currently Amended) A memory module having a first memory capacity, the memory module comprising:

a plurality of substantially identical memory components configured as a first rank and a second rank, the memory components of the first rank configured in pairs, the memory components of each pair having their respective data strobe pins in electrical communication with one another, the memory components of the second rank configured in pairs, the memory components of each pair having their respective data strobe pins in electrical communication with one another; and

a logic element which receives a first set of address and control signals compatible with a second memory capacity, the second memory capacity~~density~~ substantially equal to one-half of the first memory capacity, wherein the logic element translates the first set of address and control signals into a second set of address and control signals compatible with the first memory capacity of the memory module, the logic element transmitting the second set of address and control signals to the first rank and the second rank.

27. (Cancelled)

28. (Previously Presented) The memory module of Claim 26, wherein the memory components of each pair of memory components has a first bit width and each pair of memory components simulates a single virtual memory component having a second bit width which is twice the first bit width.

29. (Previously Presented) The memory module of Claim 28, wherein the first bit width is 4 bits, 8 bits, or 16 bits.

30. (Previously Presented) The memory module of Claim 26, wherein each of the memory components comprises a double-data-rate-1 (DDR-1), double-data-rate-2 (DDR-2), or double-data-rate-3 (DDR-3) dynamic random-access memory (DRAM) integrated circuit.

31. (Previously Presented) The memory module of Claim 26, wherein each of the memory components comprises ball-grid-array (BGA) packaging.

32. (Previously Presented) The memory module of Claim 31, wherein each of the memory components comprises fine-pitch BGA (FBGA) packaging.

33. (Previously Presented) The memory module of Claim 26, wherein each of the memory components comprises a synchronous dynamic random-access memory (SDRAM) integrated circuit.

34. (Currently Amended) ~~The memory module of Claim 26, further comprising~~ A memory module having a first memory capacity, the memory module comprising:

a plurality of substantially identical memory components configured as a first rank and a second rank, the memory components of the first rank configured in pairs, the memory components of each pair having their respective data strobe pins in electrical communication with one another, the memory components of the second rank configured in pairs, the memory components of each pair having their respective data strobe pins in electrical communication with one another;

a logic element which receives a first set of address and control signals compatible with a second memory capacity, the second memory capacity substantially equal to one-half of the first memory capacity, wherein the logic element translates the first set of address and control signals into a second set of address and control signals compatible with the first memory capacity of the memory module, the logic element transmitting the second set of address and control signals to the first rank and the second rank; and

a termination bus, each pair of memory components comprising a first memory component having a first data strobe pin, a first termination signal pin in electrical communication with the termination bus, a first termination circuit, and at least one data pin, wherein the first termination circuit selectively electrically terminates the first data strobe pin and the at least one data pin of the first memory component in response to a first signal received by the first termination signal pin from the termination bus.

35. (Previously Presented) The memory module of Claim 34, wherein each pair of memory components comprises a second memory component having a second data strobe pin in electrical communication with the first data strobe pin, a second termination signal pin, a second termination circuit, and at least one data pin, wherein the second termination circuit is responsive to a voltage applied to the second termination signal pin by not terminating the second data strobe pin or the at least one data pin of the second memory component.

36. (Previously Presented) The memory module of Claim 35, further comprising at least one termination assembly having a third termination signal pin, a third termination circuit, and at least one termination pin electrically coupled to the at least one data pin of the second memory component, the third termination signal pin in electrical communication with the termination bus, wherein the third termination circuit selectively electrically terminates the at least one data pin of the second memory component through the termination pin in response to a second signal received by the third termination signal pin from the termination bus.

37. (Previously Presented) The memory module of Claim 36, wherein the first signal and the second signal are the same signal.

38. (Previously Presented) The memory module of Claim 36, wherein the termination bus comprises an on-die termination (ODT) bus, and each of the first termination circuit, second termination circuit, and third termination circuit comprises an ODT circuit.

39. (Previously Presented) The memory module of Claim 36, wherein the voltage is ground.

40. (Currently Amended) A memory module having a first memory capacity, the memory module comprising:

a plurality of substantially identical memory components configured as a first rank and a second rank, the memory components of the first rank configured in pairs, the memory components of each pair having their respective data strobe pins in electrical communication with one another, the memory components of the second rank configured in pairs, the memory components of each pair having their respective data strobe pins in electrical communication with one another; and

a logic element which receives a first set of address and control signals compatible with a second memory capacity, the second memory capacity substantially equal to one-half of the first memory capacity, wherein the logic element translates the first set of address and control signals into a second set of address and control signals compatible with the first memory capacity of the memory module, the logic element transmitting the second set of address and control signals to the first rank and the second rank~~The memory module of Claim 26~~, wherein each memory component has a first bit width, a first number of banks of memory locations, a first number of row address bits, and a first

number of column address bits, the memory module further comprising a serial-presence-detect (SPD) device comprising data that characterizes each pair of memory components as a virtual memory component having a second bit width equal to twice the first bit width, a second number of banks of memory locations equal to the first number of banks, a second number of row address bits equal to the first number of row address bits, and a second number of column address bits equal to the first number of column address bits.

41. (Previously Presented) The memory module of Claim 40, wherein byte 3 of the SPD data comprises the first number of row address bits, byte 4 of the SPD data comprises the first number of column address bits, byte 13 of the SPD data comprises the second bit width, byte 14 of the SPD data comprises the second bit width, and byte 17 of the SPD data comprises the first number of banks.

42. (Previously Presented) The memory module of Claim 41, wherein the first bit width is 4 bits.

43. (Previously Presented) The memory module of Claim 41, wherein the first bit width is 8 bits.

44. (Previously Presented) The memory module of Claim 40, wherein the memory module has a 1-GB (128M x 8-byte) configuration, and comprises eight pairs of memory components, each memory component having a 512-Mb (128M x 4-bit) configuration, wherein the second bit width is 8 bits, the first number of row address bits is 13, and the second number of column address bits is 12.

45. (Previously Presented) The memory module of Claim 41, wherein the SPD device comprises an electrically-erasable programmable read-only memory (EEPROM) device.

46. (Currently Amended) A method of providing memory to a computer system, the method comprising:

providing a memory module having a first memory capacity, the memory module comprising a plurality of substantially identical memory components configured as a first rank and a second rank, the memory components of the first rank configured in pairs, the memory components of each pair having their respective data strobe pins in electrical communication with one another, the memory components of the second rank configured in pairs, the memory components of each pair having their respective data strobe pins in electrical communication with one another; and

receiving at the memory module a first set of address and control signals compatible with a second memory capacity, the second memory capacity~~density~~ substantially equal to one-half of the first memory capacity;

translating the first set of address and control signals into a second set of address and control signals compatible with the first memory capacity of the memory module; and

transmitting the second set of address and control signals to the first rank and the second rank.

REMARKS

The foregoing amendments and the following remarks are responsive to the January 2, 2007 Office Action. Claims 1-25 and 27 are cancelled without prejudice, Claims 26, 34, 40, and 46 are amended, and Claims 28-33, 35-39, and 41-45 remain as previously presented. Thus, Claims 26 and 28-46 are presented for further consideration. Please enter the amendments and reconsider the claims in view of the following remarks.

Comments on Allowable Subject Matter

In the January 2, 2007 Office Action, the Examiner objects to Claims 34-45 as being dependent upon a rejected base claim, but states that these claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As described herein, Applicants have amended Claims 34 and 40 to be in independent form including the limitations of base Claim 26. Each of Claims 35-39 depends either directly or indirectly from Claim 34 and each of Claims 41-45 depends either directly or indirectly from Claim 40. Therefore, Applicants submit that Claims 39-45 are in condition for allowance and Applicants respectfully request such action.

Response to Rejection of Claims 26, 28-30, and 33 Under 35 U.S.C. § 102(e)

In the January 2, 2007 Office Action, the Examiner rejects Claims 26, 28-30, and 33 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,944,694 issued to Pax ("Pax").

As currently pending, Claim 26 has been amended to correct an inadvertent typographical error and recites (emphasis added):

> 26. A memory module having a first memory capacity, the memory module comprising:
>
> a plurality of substantially identical memory components configured as a first rank and a second rank, the memory components of the first rank configured in pairs, the memory components of each pair having their respective data strobe pins in electrical communication with one another, the memory components of the second rank configured in pairs, the memory components of each pair having their respective data strobe pins in electrical communication with one another; and
>
> **a logic element which receives a first set of address and control signals compatible with a second memory capacity, the second memory capacity substantially equal to one-half of the first memory capacity, wherein the logic element translates the first set of address and control signals into a second set of address and control signals compatible with the first memory capacity of the memory module**, the

> logic element transmitting the second set of address and control signals to the first rank and the second rank.

Applicants submit that Claim 26 includes limitations that are not disclosed or suggested by Pax. For example, Applicant submits that Pax does not disclose or suggest "a logic element which receives a first set of address and control signals compatible with a second memory capacity ... substantially equal to one-half of the first memory capacity, wherein the logic element translates the first set of address and control signals into a second set of address and control signals compatible with the first memory capacity," as recited by Claim 26.

As disclosed in the present application at paragraph [0075], in an example embodiment of the memory module recited by Claim 26 (emphasis added):

> a 1-Gb 128M x 8-bit DDR-1 DRAM memory component uses row addresses A13-A0 and column addresses A11 and A9-A0. A pair of 512-Mb 128M x 4-bit DDR-1 DRAM memory components uses row addresses A12-A0 and column addresses A12, A11, and A9-A0. In certain embodiments, a memory controller of a computer system utilizing a 1-GB 128M x 8 memory module 500 comprising pairs of the 512-Mb 128M x 4 memory components 510 supplies the address and control signals including the extra row address (A13) to the memory module 500. **The logic element 540 receives the address and control signals from the memory controller and converts the extra row address (A13) into an extra column address (A12).**

As further disclosed in the present application at paragraph [0078] (emphasis added):

> In the exemplary logic element 540 of Figure 10B, during a row access procedure (CAS is high), the first multiplexer 544 passes the A12 address through to the first rank 520, the second multiplexer 546 passes the A12 address through to the second rank 530, and the PLD 542 saves or latches the A13 address from the memory controller. In certain embodiments, a copy of the A13 address is saved by the PLD 542 for each of the internal banks (e.g., 4 internal banks) per memory component 510. During a subsequent column access procedure (CAS is low), the first multiplexer 544 passes the previously-saved A13 address through to the first rank 520 as the A12 address and the second multiplexer 546 passes the previously-saved A13 address through to the second rank 530 as the A12 address. The first rank 520 and the second rank 530 thus interpret the previously-saved A13 row address as the current A12 column address. **In this way, the logic element 540 translates the extra row address into an extra column address** in accordance with certain embodiments described herein.

Thus, the logic element 540 "translates the first set of address and control signals into a second set of address and control signals compatible with the first memory capacity," as recited by Claim 26.

In contrast, Pax discloses a memory module which includes a "reroute multiplexer" or "remap multiplexer" which comprises a plurality of multiplexers which are responsive to a control signal to selectively route address signals. As described by Pax at column 7, lines 13-20:

> When the control signal (S) 340 is in a first state, each multiplexer is configured to pass the first input to the output, thus A0 appears across output 309, A1 appears across output 318, A2 appears across output 328 and A3 appears across 338. However, when the control signal (S) 340 is in a second state, each multiplexer switches so that A1 appears across output 309, A0 appears across output 318, A3 appears across output 328 and A2 appears across output 338.

Thus, Pax discloses that the multiplexers merely reroute the address signals depending on the state of the control signal. Pax does not disclose or suggest that the address signals are modified (*e.g.*, by changing a row address into a column address) to be compatible with a different memory capacity. Therefore, Pax does not disclose or suggest "a logic element" as recited by Claim 26.

Applicants submit that Claim 26 is patentably distinguished over Pax. Each of Claims 28-30 and 33 depends either directly or indirectly from Claim 26, so each of Claims 28-30 and 33 includes all the limitations of Claim 26 as well as other limitations of particular utility. Therefore, for at least the reasons stated above with regard to Claim 26, Applicants submit that Claims 28-30 and 33 are patentably distinguished over Pax. Applicants respectfully request that the Examiner withdraw the rejection of Claims 26, 28-30, and 33 and pass these claims to allowance.

Response to Rejection of Claims 31 and 32 Under 35 U.S.C. § 103(a)

In the January 2, 2007 Office Action, the Examiner rejects Claims 31 and 32 under 35 U.S.C. § 103(a) as being unpatentable over Pax. As described above, Applicants submit that Pax does not disclose or suggest all the limitations of Claim 26, so that Claim 26 is patentably distinguished over Pax. Each of Claims 31 and 32 depends either directly or indirectly from Claim 26, so each of Claims 31 and 32 includes all the limitations of Claim 26 as well as other limitations of particular utility. Therefore, for at least the reasons stated above with regard to Claim 26, Applicants submit that Claims 31 and 32 are patentably distinguished over Pax. Applicants respectfully request that the Examiner withdraw the rejection of Claims 31 and 32 and pass these claims to allowance.

Comments on Claim 46

In the January 2, 2007 Office Action, the Examiner neglected to address the patentability of Claim 46. As currently pending, Claim 46 has been amended to correct an inadvertent typographical error. Applicants respectfully request that the Examiner consider the allowability of Claim 46.

Summary

For the foregoing reasons, Applicants submit that Claims 26 and 28-46 are in condition for allowance, and Applicants respectfully request such action.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

Dated: 2/12/07

By: _____

Bruce S. Itchkawitz
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3408137
020907

Petitioners
Ex. 1010, p. 133

OIPE IAP17 FEB 21 2007 PATENT & TRADEMARK OFFICE

Please Direct All Correspondence to Customer Number **20995**

AMENDMENT / RESPONSE TRANSMITTAL

Applicant	:	Jayesh R. Bhakta et al.
App. No	:	11/075,395
Filed	:	March 7, 2005
For	:	HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS
Examiner	:	Van Thu T. Nguyen
Art Unit	:	2824

CERTIFICATE OF MAILING

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

February 12, 2007
(Date)

Bruce S. Itchkawitz, Reg. No. 47,677

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith for filing in the above-identified application are the following enclosures:

(X) Amendment and Response to Office Action in 10 pages.

The fee has been calculated as shown below:

FEE CALCULATION				
FEE TYPE		**FEE CODE**	**CALCULATION**	**TOTAL**
Excess Claims	20 - 27 = 0	1202 ($50)	0 x 50 =	$0
Excess Independent	4 - 6 = 0	1201 ($200)	0 x 200 =	$0
			TOTAL FEE DUE	$0

(X) Return prepaid postcard.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Bruce S. Itchkawitz
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Attorney of Record
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3416816/ap
021207

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/075,395	03/07/2005	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 02/21/2007

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 20	Minus	** 27	= 0	X $ =		OR	X $50=	0
Independent (37 CFR 1.16(h))	* 5	Minus	***6	= 0	X $ =		OR	X $200=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
Patsy Zimmerman

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	23	virtual with width with twice	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/28 15:27
L2	124	virtual same (bit or band) same width same (twice or double or half)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/28 15:27
L3	124	virtual same (bit or band) same width same (twice or double or half)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/28 15:27
L4	107	L3 and @ad<"20040325"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/28 15:28
L5	107	L3 and @ad<"20040325"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/28 15:28
L6	11	(mirror with (chip or IC)) and (virtual adj2 address$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/28 15:28
L7	11	L6 and @ad<"20040325"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/28 15:28
L8	123	termination with data with strobe	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/28 15:30
L9	123	termination with data with strobe	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/28 15:28

EAST Search History

L10	95	L9 and @ad<"20040325"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/28 15:28
L12	1	BHAKTA-JAYESH$2.in. and SOLOMON-JEFFREY.in. and GERVASI-WILLIAM$3.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/28 15:33
L13	1	((first adj5 set adj5 address) with compatible with (second adj5 memory adj5 capacity) with translates with transmitting with (first adj rank) with (second adj rank)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/28 15:34

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/075,395	03/07/2005	Jayesh R. Bhakta	NETL.018A	8121

20995 7590 04/03/2007
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER
NGUYEN, VAN THU T

ART UNIT	PAPER NUMBER
2824	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	04/03/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 04/03/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jcartee@kmob.com
eOAPilot@kmob.com

Office Action Summary	Application No.	Applicant(s)	
	11/075,395	BHAKTA ET AL.	
	Examiner	Art Unit	
	VanThu Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26 and 28-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *34-45* is/are allowed.

6)☒ Claim(s) *26,28-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

Petitioners
Ex. 1010, p. 139

Response to Amendment

1. This Office Action is in response to Amendment filed on 02/21/2007.

2. Claims 26, 28-45 are currently pending and examined.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 26, 28-30, 33 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,944,694 to Pax ("Pax").

Regarding claim 26, Pax discloses a memory module having a first memory capacity, the memory module comprising:

- a plurality of substantially identical memory components (see FIGs. 1-3) configured as a first rank and a second rank (each pair of the memory chips 104B-104B forms a rank), the memory components of the first rank configured in pairs with their respective data strobe pins tied together, the memory components of the second rank configured in pairs with their respective data strobe pins tied together (see FIG. 3); and
- a logic element (reroute multiplexer 500, see FIG. 9) which receives a first set of address (e.g. address signals A0-A3, see FIG. 5) and control signals (e.g. signals

S0 and Clock, see FIG. 9) compatible with a second memory capacity (memory capacity of a single memory chip), the second memory capacity substantially equal to one-half of the first memory capacity (memory capacity of one memory chip and its mirror chip), wherein the logic element translates the first set of address and control signals into a second set of address and control signals compatible with the first memory capacity of the memory module (see FIG. 9), the logic element transmitting the second set of address and control signals to the first rank and the second rank (see column 8, lines 14-32).

Regarding claim 28, Pax discloses wherein the memory components of each pair of memory components has a first bit width (e.g. bit width of A0-A3) and each pair of memory components simulates a single virtual memory component having a second bit width (e.g. bit of S0, A0-A3) which is twice the first bit width.

Regarding claims 29-30, 33, Pax discloses the first bit width is 4 bits (A0-A3); the memory chips are SDRAM (see column 9, lines 34-43);

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pax.

Regarding claims 31-32, Pax does not mention that each of memory components comprising fine-pitch BGA (FPBGA) packaging.

However, it would have been obvious to one with ordinary skill in the art to use the FPBGA packaging for memory chips disclosed in Pax because it is well-known chip package in memory technology.

Allowable Subject Matter

7. Claims 34-45 are allowed.

Response to Arguments

8. Applicant's arguments filed 02/21/2007 have been fully considered but they are not persuasive.

Applicant argues that Pax does not disclose or suggest the address signal are modified (e.g. by changing a row address into a column address) to be compatible with a different memory capacity. Therefore, Pax does not discloses or suggest "a logic element" as recited by claim 16.

In response to Applicant's argument, it is noted that the features upon which applicant relies (i.e., address signal being modified by changing a row address into a column address) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

As described by Pax at column 7, lines 13-20, and recited on page 9 of Applicant's Remark, the address signals A0-A3 are indeed modified by rerouting/remapping.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Thursday, 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

March 28, 2007

VanThu Nguyen
Primary Examiner
Art Unit 2824

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination
	11/075,395	BHAKTA ET AL.
	Examiner	Art Unit
	VanThu Nguyen	2824

SEARCHED			
Class	Subclass	Date	Examiner
365	230.01 230.02 x 230.06 x	12/19/2006	VTN
711	5 6	12/19/2006	VTN
711	211 x	12/19/2006	VTN
Update	search	3/28/2007	VTN

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST search, including inventors and interference searches (see print out history)	12/19/2006	VTN
Update EAST search (see print out history)	3/28/2007	VTN

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jayesh R. Bhakta et al.	Group Art Unit 2824
Appl. No.	:	11/075,395	
Filed	:	March 7, 2005	
For	:	HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS	
Examiner	:	Van Thu T. Nguyen	

AMENDMENT AND RESPONSE TO APRIL 3, 2007 FINAL OFFICE ACTION

Mail Stop AF
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the April 3, 2007 Final Office Action, Applicants request the Examiner to reconsider the above-identified patent application in view of the following amendments and remarks.

Amendments to the Claims: Begin on page 2 of this Response.

Remarks: Begin on page 6 of this Response.

Petitioners
Ex. 1010, p. 146

AMENDMENTS TO THE CLAIMS

Please cancel Claims 26, 28-33, and 46 without prejudice, as indicated below.

Please add Claims 47-54, as indicated below.

A complete listing of all claims is presented below with insertions underlined (e.g., insertion), and deletions struckthrough or in double brackets (e.g., ~~deletion~~ or [[deletion]]):

1.-33. (Cancelled)

34. (Previously Presented) A memory module having a first memory capacity, the memory module comprising:

a plurality of substantially identical memory components configured as a first rank and a second rank, the memory components of the first rank configured in pairs, the memory components of each pair having their respective data strobe pins in electrical communication with one another, the memory components of the second rank configured in pairs, the memory components of each pair having their respective data strobe pins in electrical communication with one another;

a logic element which receives a first set of address and control signals compatible with a second memory capacity, the second memory capacity substantially equal to one-half of the first memory capacity, wherein the logic element translates the first set of address and control signals into a second set of address and control signals compatible with the first memory capacity of the memory module, the logic element transmitting the second set of address and control signals to the first rank and the second rank; and

a termination bus, each pair of memory components comprising a first memory component having a first data strobe pin, a first termination signal pin in electrical communication with the termination bus, a first termination circuit, and at least one data pin, wherein the first termination circuit selectively electrically terminates the first data strobe pin and the at least one data pin of the first memory component in response to a first signal received by the first termination signal pin from the termination bus.

35. (Previously Presented) The memory module of Claim 34, wherein each pair of memory components comprises a second memory component having a second data strobe pin in electrical communication with the first data strobe pin, a second termination signal pin, a second termination circuit, and at least one data pin, wherein the second termination circuit is

responsive to a voltage applied to the second termination signal pin by not terminating the second data strobe pin or the at least one data pin of the second memory component.

36. (Previously Presented) The memory module of Claim 35, further comprising at least one termination assembly having a third termination signal pin, a third termination circuit, and at least one termination pin electrically coupled to the at least one data pin of the second memory component, the third termination signal pin in electrical communication with the termination bus, wherein the third termination circuit selectively electrically terminates the at least one data pin of the second memory component through the termination pin in response to a second signal received by the third termination signal pin from the termination bus.

37. (Previously Presented) The memory module of Claim 36, wherein the first signal and the second signal are the same signal.

38. (Previously Presented) The memory module of Claim 36, wherein the termination bus comprises an on-die termination (ODT) bus, and each of the first termination circuit, second termination circuit, and third termination circuit comprises an ODT circuit.

39. (Previously Presented) The memory module of Claim 36, wherein the voltage is ground.

40. (Previously Presented) A memory module having a first memory capacity, the memory module comprising:

a plurality of substantially identical memory components configured as a first rank and a second rank, the memory components of the first rank configured in pairs, the memory components of each pair having their respective data strobe pins in electrical communication with one another, the memory components of the second rank configured in pairs, the memory components of each pair having their respective data strobe pins in electrical communication with one another; and

a logic element which receives a first set of address and control signals compatible with a second memory capacity, the second memory capacity substantially equal to one-half of the first memory capacity, wherein the logic element translates the first set of address and control signals into a second set of address and control signals compatible with the first memory capacity of the memory module, the logic element transmitting the second set of address and control signals to the first rank and the second rank, wherein

each memory component has a first bit width, a first number of banks of memory locations, a first number of row address bits, and a first number of column address bits, the memory module further comprising a serial-presence-detect (SPD) device comprising data that characterizes each pair of memory components as a virtual memory component having a second bit width equal to twice the first bit width, a second number of banks of memory locations equal to the first number of banks, a second number of row address bits equal to the first number of row address bits, and a second number of column address bits equal to the first number of column address bits.

41. (Previously Presented) The memory module of Claim 40, wherein byte 3 of the SPD data comprises the first number of row address bits, byte 4 of the SPD data comprises the first number of column address bits, byte 13 of the SPD data comprises the second bit width, byte 14 of the SPD data comprises the second bit width, and byte 17 of the SPD data comprises the first number of banks.

42. (Previously Presented) The memory module of Claim 41, wherein the first bit width is 4 bits.

43. (Previously Presented) The memory module of Claim 41, wherein the first bit width is 8 bits.

44. (Previously Presented) The memory module of Claim 40, wherein the memory module has a 1-GB (128M x 8-byte) configuration, and comprises eight pairs of memory components, each memory component having a 512-Mb (128M x 4-bit) configuration, wherein the second bit width is 8 bits, the first number of row address bits is 13, and the second number of column address bits is 12.

45. (Previously Presented) The memory module of Claim 41, wherein the SPD device comprises an electrically-erasable programmable read-only memory (EEPROM) device.

46. (Cancelled)

47. (New) The memory module of Claim 34, wherein the memory components of each pair of memory components has a first bit width and each pair of memory components simulates a single virtual memory component having a second bit width which is twice the first bit width.

48. (New) The memory module of Claim 47, wherein the first bit width is 4 bits, 8 bits, or 16 bits.

49. (New) The memory module of Claim 34, wherein each of the memory components comprises ball-grid-array (BGA) packaging.

50. (New) The memory module of Claim 49, wherein each of the memory components comprises fine-pitch BGA (FBGA) packaging.

51. (New) The memory module of Claim 34, wherein each of the memory components comprises a synchronous dynamic random-access memory (SDRAM) integrated circuit.

52. (New) The memory module of Claim 40, wherein each of the memory components comprises ball-grid-array (BGA) packaging.

53. (New) The memory module of Claim 52, wherein each of the memory components comprises fine-pitch BGA (FBGA) packaging.

54. (New) The memory module of Claim 40, wherein each of the memory components comprises a synchronous dynamic random-access memory (SDRAM) integrated circuit.

REMARKS

The foregoing amendments and the following remarks are responsive to the April 3, 2007 Final Office Action. Claims 1-33 and 46 are cancelled without prejudice, Claims 34-45 remain as previously pending, and new Claims 47-54 are added. Thus, Claims 34-45 and 47-54 are presented for further consideration.

Comments on Allowable Subject Matter and New Claims Depending Therefrom

Applicants thank the Examiner for acknowledging the allowability of Claims 34-45. Applicants have added new Claims 47-51, each of which depends directly or indirectly from Claim 34. Applicants have also added new Claims 52-54, each of which depends directly or indirectly from Claim 40. Applicants submit that new Claims 47-54 do not add new matter to the present application, and Applicants respectfully request that the Examiner pass these claims to allowance.

Response to Rejection of Claims 26, 28-30, and 33 Under 35 U.S.C. § 102(e)

In the April 3, 2007 Final Office Action, the Examiner rejects Claims 26, 28-30, and 33 as being anticipated by U.S. Patent No. 6,944,694 issued to Pax ("Pax"). Applicants respectfully traverse this rejection. However, in the interest of expediting allowance of the present application, Applicants have cancelled Claims 26, 28-30, and 36 without prejudice, reserving the right to pursue allowance of these claims through continuation practice. Applicants respectfully request that the Examiner consider the patentability of the remaining pending claims.

Response to Rejection of Claims 31 and 32 Under 35 U.S.C. § 103(a)

In the April 3, 2007 Final Office Action, the Examiner rejects Claims 31 and 32 as being unpatentable over Pax. Applicants respectfully traverse this rejection. However, in the interest of expediting allowance of the present application, Applicants have cancelled Claims 31 and 32 without prejudice, reserving the right to pursue allowance of these claims through continuation practice. Applicants respectfully request that the Examiner consider the patentability of the remaining pending claims.

Summary

For the foregoing reasons, Applicants submit that Claims 34-45 and 47-54 are in condition for allowance, and Applicants respectfully request such action.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

Dated: 6/1/07 By: _____

Bruce S. Itchkawitz
Registration No. 47,677
KNOBBE, MARTENS, OLSON & BEAR, LLP
Attorney of Record
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3829779
053107

Electronic Acknowledgement Receipt

EFS ID:	1831982
Application Number:	11075395
International Application Number:	
Confirmation Number:	8121
Title of Invention:	High-density memory module utilizing low-density memory components
First Named Inventor/Applicant Name:	Jayesh R. Bhakta
Customer Number:	20995
Filer:	Bruce S. Itchkaeitz/Alexandra Benitez
Filer Authorized By:	Bruce S. Itchkaeitz
Attorney Docket Number:	NETL.018A
Receipt Date:	01-JUN-2007
Filing Date:	07-MAR-2005
Time Stamp:	18:16:27
Application Type:	Utility

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1		amend.pdf	276501	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment After Final	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	7

Warnings:

Information:

Total Files Size (in bytes):	276501

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

CLAIMS ONLY	Application Number 11/05395	Filing Date
	Applicant(s)	

* May be used for additional claims or amendments

CLAIMS	AS FILED		AFTER FIRST AMENDMENT		AFTER SECOND AMENDMENT			*		*		*	
	Indep	Depend	Indep	Depend	Indep	Depend		Indep	Depend	Indep	Depend	Indep	Depend
1							51						
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49							99						
50							100						
Total Indep							Total Indep			2			
Total Depend							Total Depend			18			
Total Claims							Total Claims			20			

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/075,395	03/07/2005	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 02/21/2007

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 20	Minus	** 27	= 0	X $ =		OR	X $50=	0
Independent (37 CFR 1.16(h))	* 5	Minus	***6	= 0	X $ =		OR	X $200=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT 6/1/07

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 26	Minus	** 27	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	* 2	Minus	***6	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
Patsy Zimmerman

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	BHAKTA-JAYESH$2.in. and SOLOMON-JEFFREY.in. and GERVASI-WILLIAM$3.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/06/11 14:53
L2	1	((first adj5 set adj5 address) with compatible with (second adj5 memory adj5 capacity) with translates with transmitting with (first adj rank) with (second adj rank)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/06/11 14:54
L3	127	virtual same (bit or band) same width same (twice or double or half)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/06/11 14:55
L4	107	L3 and @ad<"20040325"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/06/11 14:55
L5	126	termination with data with strobe	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/06/11 14:55
L6	95	L5 and @ad<"20040325"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/06/11 14:55

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NOTICE OF ALLOWANCE AND FEE(S) DUE

20995 7590 06/19/2007

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
NGUYEN, VAN THU T	
ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 06/19/2007

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/075,395	03/07/2005	Jayesh R. Bhakta	NETL.018A	8121

TITLE OF INVENTION: HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	09/19/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

20995 7590 06/19/2007

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Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/075,395	03/07/2005	Jayesh R. Bhakta	NETL.018A	8121

TITLE OF INVENTION: HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS

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nonprovisional	NO	$1400	$300	$0	$1700	09/19/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, VAN THU T	2824	365-001000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

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Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/075,395	03/07/2005	Jayesh R. Bhakta	NETL.018A	8121

20995 7590 06/19/2007

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER
NGUYEN, VAN THU T

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 06/19/2007

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 69 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 69 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 07/06) Approved for use through 06/30/2007.

Notice of Allowability	Application No.	Applicant(s)	
	11/075,395	BHAKTA ET AL.	
	Examiner	Art Unit	
	VanThu Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment after final filed on 06/01/2007*.

2. ☒ The allowed claim(s) is/are *34-45,47-54*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

VThu Ngu

VanThu Nguyen
Primary Examiner
Art Unit: 2824

Petitioners
Ex. 1010, p. 161

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Bib Data Sheet

CONFIRMATION NO. 8121

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/075,395	03/07/2005 RULE	365	2824	NETL.018A

APPLICANTS

Jayesh R. Bhakta, Cerritos, CA;
Jeffrey Solomon, Irvine, CA;
William M. Gervasi, Ladera Ranch, CA;

**** CONTINUING DATA ****************************** Y/VTN

This appln claims benefit of 60/550,668 03/05/2004 and claims benefit of 60/575,595 05/28/2004 and claims benefit of 60/590,038 07/21/2004

**** FOREIGN APPLICATIONS ************************ N/VTN

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 04/07/2005

		STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed ☐ yes ☑ no 35 USC 119 (a-d) conditions met ☐ yes ☑ no ☐ Met after Allowance Verified and Acknowledged Examiner's Signature VTN Initials		CA	11	27	6

ADDRESS
20995

TITLE

High-density memory module utilizing low-density memory components

FILING FEE RECEIVED		
2080	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Issue Classification	Application/Control No. 11/075,395	Applicant(s)/Patent under Reexamination BHAKTA ET AL.
	Examiner VanThu Nguyen	Art Unit 2824

ISSUE CLASSIFICATION

ORIGINAL		INTERNATIONAL CLASSIFICATION								
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED			
365	230.02	G	11	C	8	/00				/
CROSS REFERENCES										
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					/				/
365	230.06					/				/
711	211					/				/
						/				/
						/				/
						/				/

(Assistant Examiner) (Date)	VanThu Nguyen 6/11/07	Total Claims Allowed: 20
(Legal Instruments Examiner) (Date) 6/11/07	(Primary Examiner) (Date)	O.G. Print Claim(s): 1 / O.G. Print Fig.: 10A

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		31		61		91		121		151		181
	2		32		62		92		122		152		182
	3		33		63		93		123		153		183
	4	1	34		64		94		124		154		184
	5	2	35		65		95		125		155		185
	6	3	36		66		96		126		156		186
	7	4	37		67		97		127		157		187
	8	5	38		68		98		128		158		188
	9	6	39		69		99		129		159		189
	10	12	40		70		100		130		160		190
	11	13	41		71		101		131		161		191
	12	14	42		72		102		132		162		192
	13	15	43		73		103		133		163		193
	14	17	44		74		104		134		164		194
	15	16	45		75		105		135		165		195
	16		46		76		106		136		166		196
	17	7	47		77		107		137		167		197
	18	8	48		78		108		138		168		198
	19	9	49		79		109		139		169		199
	20	10	50		80		110		140		170		200
	21	11	51		81		111		141		171		201
	22	18	52		82		112		142		172		202
	23	19	53		83		113		143		173		203
	24	20	54		84		114		144		174		204
	25		55		85		115		145		175		205
	26		56		86		116		146		176		206
	27		57		87		117		147		177		207
	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jayesh R. Bhakta et al.	Group Art Unit 2824
Appl. No.	:	11/075,395	
Filed	:	March 7, 2005	
For	:	HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS	
Examiner	:	Van Thu T. Nguyen	

Please enter, Thanks
VTN
6/11/07

AMENDMENT AND RESPONSE TO APRIL 3, 2007 FINAL OFFICE ACTION

Mail Stop AF
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the April 3, 2007 Final Office Action, Applicants request the Examiner to reconsider the above-identified patent application in view of the following amendments and remarks.

Amendments to the Claims: Begin on page 2 of this Response.

Remarks: Begin on page 6 of this Response.

Petitioners
Ex. 1010, p. 164

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination
	11/075,395	BHAKTA ET AL.
	Examiner	Art Unit
	VanThu Nguyen	2824

SEARCHED			
Class	Subclass	Date	Examiner
365	230.01 230.02 230.06	12/19/2006	VTN
711	5 6	12/19/2006	VTN
711	211	12/19/2006	VTN
Update	search	3/28/2007	VTN
Update	search	6/11/2007	VTN

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
Same as	**above**	6/11/2007	**VTN**

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST search, including inventors and interference searches (see print out history)	12/19/2006	VTN
Update EAST search (see print out history)	3/28/2007	VTN
Update EAST search (see print out history)	6/11/2007	VTN

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

20995 7590 06/19/2007

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/075,395	03/07/2005	Jayesh R. Bhakta	NETL.018A	8121

TITLE OF INVENTION: HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	09/19/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, VAN THU T	2824	365-001000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
   - ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
   - ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
   (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
   (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Knobbe Martens
2 Olson & Bear LLP
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Netlist, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Irvine, California

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☑ Issue Fee
- ☑ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 11-1410 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date 9/17/07

Typed or printed name Bruce S. Itchkawitz Registration No. 47,677

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jayesh R. Bhakta et al.	Group Art Unit 2824
App. No.	:	11/075,395	
Filed	:	March 7, 2005	
For	:	HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS	
Examiner	:	Van Thu T. Nguyen	

COMMENTS ON EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop- ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Arlington, VA 22313-1450

Dear Sir:

Applicants respectfully disagree with the Examiner's Statement of Reasons for Allowance to the extent that the limitations recited by the Examiner are not present in all of the claims.

To the extent that there is any implication that the patentability of the claims rests on the recitation of a single feature, Applicants respectfully disagree with the Examiner's Statement because it is the combination of features that makes the claims patentable. Accordingly, Applicants submit that the claims of the present application are allowable because each of the claims recites a combination of features that are not taught or suggested by the prior art.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 9/17/07

By: _____

Bruce S. Itchkawitz
Registration No. 47,677
Attorney of Record
Customer No. 20,995
(949) 760-0404

4275277
091707

Petitioners
Ex. 1010, p. 167

Electronic Patent Application Fee Transmittal

Application Number:	11075395
Filing Date:	07-Mar-2005
Title of Invention:	HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS
First Named Inventor/Applicant Name:	Jayesh R. Bhakta
Filer:	Bruce S. Itchkawitz/Amy perez
Attorney Docket Number:	NETL.018A

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1400	1400
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1700**

Electronic Acknowledgement Receipt

EFS ID:	2205845
Application Number:	11075395
International Application Number:	
Confirmation Number:	8121
Title of Invention:	HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS
First Named Inventor/Applicant Name:	Jayesh R. Bhakta
Customer Number:	20995
Filer:	Bruce S. Itchkawitz/Alexandra Benitez
Filer Authorized By:	Bruce S. Itchkawitz
Attorney Docket Number:	NETL.018A
Receipt Date:	17-SEP-2007
Filing Date:	07-MAR-2005
Time Stamp:	19:04:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	$1700
RAM confirmation Number	3235
Deposit Account	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)

1	Issue Fee Payment (PTO-85B)	ifee.pdf	98469 6eb696a07b23e8c9a0173f2913f9fe5722168893	no	1
Warnings:					
Information:					
2	Miscellaneous Incoming Letter	comments.pdf	35001 81a2e0d3ef34266ad55aad5fee5b26b61c34a34c	no	1
Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	fee-info.pdf	8319 a250faef30e6f58de7030057b2c86e62404061a5	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	141789		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/075,395	10/23/2007	7286436	NETL.018A	8121

20995 7590 10/03/2007
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 69 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Jayesh R. Bhakta, Cerritos, CA;
Jeffrey Solomon, Irvine, CA;
William M. Gervasi, Ladera Ranch, CA;

Knobbe Martens Olson & Bear LLP

Intellectual Property Law

2040 Main Street
Fourteenth Floor
Irvine, CA 92614
Tel 949-760-0404
Fax 949-760-9502
www.kmob.com

Bruce S. Itchkawitz, Ph.D.
2bsi@kmob.com

November 4, 2008

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Re: Title: HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS
Letters Patent No. 7,286,436
Issued: October 23, 2007
Our Reference: NETL.018A

Dear Sir:

Enclosed for filing is a Certificate of Correction in connection with the above-identified patent.

As the errors cited in the Certificate of Correction were incurred through the fault of both the Patent Office and the Applicant, we have enclosed our check in the amount of $100. Please charge any additional fees to our Deposit Account No. 11-1410.

Respectfully submitted,

Knobbe, Martens, Olson & Bear, LLP

Bruce S. Itchkawitz
Registration No. 47,677
Customer No. 20,995

Enclosures

5142883
041108

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,286,436 B2
APPLICATION NO. : 11/075,395
ISSUE DATE : October 23, 2007
INVENTOR(S) : Bhakta et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At page 2, column 1, line 8, please delete "Research" and insert -- Revision --, therefor.

At column 1, line 63-64, please delete "128M 8-byte" and insert -- 128M x 8-byte --, therefor.

At column 1, line 64, please delete "128M 64-bit" and insert -- 128M x 64-bit --, therefor.

At column 1, line 67, please delete "128M 8-byte" and insert -- 128M x 8-byte --, therefor.

At column 2, line 9, please delete "128M 4-byte" and insert -- 128M x 4-byte --, therefor.

At column 3, line 58, please delete "64M 4-bit" and insert -- 64M x 4-bit --, therefor.

At column 4, line 24, please delete "64M 8-bit" and insert -- 64M x 8-bit --, therefor.

At column 4, line 33, please delete "64M 4-bit" and insert -- 64M x 4-bit --, therefor.

At column 4, line 56, please delete "64M 4-bit" and inset -- 64M x 4-bit --, therefor.

At column 4, line 58, please delete "64M 8-bit" and insert -- 64M x 8-bit --, therefor.

At column 4, line 59, please delete "128M 8-byte" and insert -- 128M x 8-byte --, therefor.

At column 7, line 52, please delete "64M 4-bit" and insert -- 64M x 4-bit, --, therefor.

At column 8, line 5, please delete "128M 72-bit" and insert -- 128M x 72-bit --, therefor.

At column 8, line 6, please delete "64M 4-bit" and insert -- 64M x 4-bit --, therefor.

At column 12, line 51, please delete "ets" and insert -- its --, therefor.

At column 12, line 66, please delete "128M 4-bit" and insert -- 128M x 4-bit --, therefor.

At column 13, line 1, please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 13, line 6, please delete "128M 8-byte" and insert -- 128M x 8-byte --, therefor.

At column 13, line 7, please delete "128M 4-bit" and insert -- 128M x 4-bit --, therefor.

At column 13, line 31, please delete "64M 8-byte" and insert -- 64M x 8-byte --, therefor.

MAILING ADDRESS OF SENDER:

Bruce S. Itchkawitz
KNOBBE, MARTENS, OLSON & BEAR, LLP
2040 Main Street, 14th Floor
Irvine, California 92614

DOCKET NO. NETL.018A

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,286,436 B2
APPLICATION NO. : 11/075,395
ISSUE DATE : October 23, 2007
INVENTOR(S) : Bhakta et al.

At column 13, line 33, please delete "64M 8-bit" and insert -- 64M x 8-bit --, therefor.

At column 13, line 44, please delete "64M 8-bit" and insert -- 64M x 8-bit --, therefor.

At column 13, line 47, please delete "64M 8-bit" and insert -- 64M x 8-bit --, therefor.

At column 13, lines 51-52, please delete "128M 8-byte" and insert -- 128M x 8-byte --, therefor.

At column 13, line 53, please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 13, line 64, please delete "128M 8-bit" and insert - - 128M x 8-bit --, therefor.

At column 13, line 67, please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 14, line 12, please delete "128M 4-bit" and insert -- 128M x 4-bit --, therefor.

At column 14, line 13, please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 14, line 17, please delete "128M 8-byte" and insert -- 128M x 8-byte --, therefor.

At column 14, line 18, please delete "128M 4-bit" and insert -- 128M x 4-bit --, therefor.

At column 14, line 19, please delete "128M 4-bit" and insert -- 128M x 4-bit --, therefor.

At column 14, line 21, please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 14, lines 27-28, please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 14, line 30, please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 14, line 34, please delete "128M 4-byte" and insert -- 128M x 4-byte --, therefor.

At column 14, line 35, please delete "128M 4-bit" and insert -- 128M x 4-bit --, therefor.

At column 14, line 38, please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 15, line 2, after "a" please delete "a" (second occurrence).

At column 15, line 40 (Approx.), please delete "128M 4-bit" and insert -- 128M x 4-bit --, therefor.

At column 15, line 41 (Approx.), please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 15, line 55, please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

MAILING ADDRESS OF SENDER:

Bruce S. Itchkawitz
KNOBBE, MARTENS, OLSON & BEAR, LLP
2040 Main Street, 14th Floor
Irvine, California 92614

DOCKET NO. NETL.018A

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,286,436 B2
APPLICATION NO. : 11/075,395
ISSUE DATE : October 23, 2007
INVENTOR(S) : Bhakta et al.

At column 15, line 57, please delete " 128M 4-bit" and insert -- 128M x 4-bit --, therefor.

At column 15, line 61, please delete "128M 8" and insert -- 128M x 8 --, therefor.

At column 15, line 62, please delete "128M 4" and insert -- 128M x 4 --, therefor.

At column 17, line 25 (Approx.), please delete "128M 8-byte" and insert -- 128M x 8-byte --, therefor.

At column 17, line 26 (Approx.), please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 17, lines 27-28 (Approx.), please delete "128M 8-byte" and insert -- 128M x 8-byte --, therefor.

At column 17, line 28 (Approx.), please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 17, line 34 (Approx.), please delete "128M 8-byte" and insert 128M x 8-byte --, therefor.

5142922
041108

MAILING ADDRESS OF SENDER:

Bruce S. Itchkawitz
KNOBBE, MARTENS, OLSON & BEAR, LLP
2040 Main Street, 14th Floor
Irvine, California 92614

DOCKET NO. NETL.018A

Electronic Patent Application Fee Transmittal

Application Number:	11075395
Filing Date:	07-Mar-2005
Title of Invention:	HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS
First Named Inventor/Applicant Name:	Jayesh R. Bhakta
Filer:	Bruce S. Itchkawitz/Amy Perez
Attorney Docket Number:	NETL.018A

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Certificate of correction	1811	1	100	100
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**100**

Electronic Acknowledgement Receipt

EFS ID:	4232048
Application Number:	11075395
International Application Number:	
Confirmation Number:	8121
Title of Invention:	HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS
First Named Inventor/Applicant Name:	Jayesh R. Bhakta
Customer Number:	20995
Filer:	Bruce S. Itchkawitz
Filer Authorized By:	
Attorney Docket Number:	NETL.018A
Receipt Date:	04-NOV-2008
Filing Date:	07-MAR-2005
Time Stamp:	20:21:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$100
RAM confirmation Number	11607
Deposit Account	111410
Authorized User	KNOBBE MARTENS OLSON AND BEAR

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	netl.pdf	176198 797e0e30a679cf693e72c06c0017ccd6a7d3811b	no	4
Warnings:					
Information:					
2	Fee Worksheet (PTO-06)	fee-info.pdf	30463 d41678e0ecef3741fd7983951431869210baa08e	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	206661	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,286,436 B2
APPLICATION NO. : 11/075395
DATED : October 23, 2007
INVENTOR(S) : Bhakta et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At page 2, column 1, line 8, please delete "Research" and insert -- Revision --, therefor.

At column 1, lines 63-64, please delete "128M 8-byte" and insert -- 128M x 8-byte --, therefor.

At column 1, line 64, please delete "128M 64-bit" and insert -- 128M x 64-bit --, therefor.

At column 1, line 67, please delete "128M 8-byte" and insert -- 128M x 8-byte --, therefor.

At column 2, line 9, please delete "128M 4-byte" and insert -- 128M x 4-byte --, therefor.

At column 3, line 58, please delete "64M 4-bit" and insert -- 64M x 4-bit --, therefor.

At column 4, line 24, please delete "64M 8-bit" and insert -- 64M x 8-bit --, therefor.

At column 4, line 33, please delete "64M 4-bit" and insert -- 64M x 4-bit --, therefor.

At column 4, line 56, please delete "64M 4-bit" and insert -- 64M x 4-bit --, therefor.

At column 4, line 58, please delete "64M 8-bit" and insert -- 64M x 8-bit --, therefor.

At column 4, line 59, please delete "128M 8-byte" and insert -- 128M x 8-byte --, therefor.

At column 7, line 52, please delete "64M 4-bit" and insert -- 64M x 4-bit, --, therefor.

At column 8, line 5, please delete "128M 72-bit" and insert -- 128M x 72-bit --, therefor.

At column 8, line 6, please delete "64M 4-bit" and insert -- 64M x 4-bit --, therefor.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,286,436 B2
APPLICATION NO. : 11/075395
DATED : October 23, 2007
INVENTOR(S) : Bhakta et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At column 12, line 51, please delete "ets" and insert -- its --, therefor.

At column 12, line 66, please delete "128M 4-bit" and insert -- 128M x 4-bit --, therefor.

At column 13, line 1, please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 13, line 6, please delete "128M 8-byte" and insert -- 128M x 8-byte --, therefor.

At column 13, line 7, please delete "128M 4-bit" and insert -- 128M x 4-bit --, therefor.

At column 13, line 31, please delete "64M 8-byte" and insert -- 64M x 8-byte --, therefor.

At column 13, line 33, please delete "64M 8-bit" and insert -- 64M x 8-bit --, therefor.

At column 13, line 44, please delete "64M 8-bit" and insert -- 64M x 8-bit --, therefor.

At column 13, line 47, please delete "64M 8-bit" and insert -- 64M x 8-bit --, therefor.

At column 13, lines 51-52, please delete "128M 8-byte" and insert -- 128M x 8-byte --, therefor.

At column 13, line 53, please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 13, line 64, please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 13, line 67, please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,286,436 B2
APPLICATION NO. : 11/075395
DATED : October 23, 2007
INVENTOR(S) : Bhakta et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At column 14, line 12, please delete "128M 4-bit" and insert -- 128M x 4-bit --, therefor.

At column 14, line 13, please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 14, line 17, please delete "128M 8-byte" and insert -- 128M x 8-byte --, therefor.

At column 14, line 18, please delete "128M 4-bit" and insert -- 128M x 4-bit --, therefor.

At column 14, line 19, please delete "128M 4-bit" and insert -- 128M x 4-bit --, therefor.

At column 14, line 21, please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 14, lines 27-28, please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 14, line 30, please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 14, line 34, please delete "128M 4-byte" and insert -- 128M x 4-byte --, therefor.

At column 14, line 35, please delete "128M 4-bit" and insert -- 128M x 4-bit --, therefor.

At column 14, line 38, please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,286,436 B2
APPLICATION NO. : 11/075395
DATED : October 23, 2007
INVENTOR(S) : Bhakta et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At column 15, line 2, after "a" please delete "a" (second occurrence).

At column 15, line 40 (Approx.), please delete "128M 4-bit" and insert -- 128M x 4-bit --, therefor.

At column 15, line 41 (Approx.), please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 15, line 55, please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 15, line 57, please delete "128M 4-bit" and insert -- 128M x 4-bit --, therefor.

At column 15, line 61, please delete "128M 8" and insert -- 128M x 8 --, therefor.

At column 15, line 62, please delete "128M 4" and insert -- 128M x 4 --, therefor.

At column 17, line 25 (Approx.), please delete "128M 8-byte" and insert -- 128M x 8-byte --, therefor.

At column 17, line 26 (Approx.), please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 17, lines 27-28 (Approx.), please delete "128M 8-byte" and insert -- 128M x 8-byte --, therefor.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,286,436 B2
APPLICATION NO. : 11/075395
DATED : October 23, 2007
INVENTOR(S) : Bhakta et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At column 17, line 28 (Approx.), please delete "128M 8-bit" and insert -- 128M x 8-bit --, therefor.

At column 17, line 34 (Approx.), please delete "128M 8-byte" and insert -- 128M x 8-byte --, therefor.

Signed and Sealed this

Sixteenth Day of December, 2008

JON W. DUDAS
Director of the United States Patent and Trademark Office

Customer No. 79141

REVOCATION
AND
GENERAL POWER OF ATTORNEY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The undersigned is an empowered representative of the Assignee and hereby appoints the registrant, Jamie J. Zheng, Customer No. 79141, as attorney to represent the Assignee before the United States Patent and Trademark Office (USPTO) in connection with the patent assigned to the Assignee according to the USPTO assignment records or assignment documents supplied with the accompanying Statement Under 37 CFR § 3.73(b). This appointment is to be to the exclusion of the inventor(s) and his attorney(s) in accordance with the provisions of 37 CFR § 3.71.

Submission of this paper in connection with any matter of the below named assignee, together with a statement under 37 CFR 3.73(b), shall serve to revoke any previous powers of attorneys in that matter.

A Statement under 37 CFR § 3.73(b) is attached setting forth a full chain of title for the subject patent owned by the Assignee named below.

Please recognize or change the correspondence address for the patent identified in the attached Statement to Customer No. 79141.

By:

Date: October 1, 2012

Name: Gail Sasaki Title: Vice President and CFO
Assignee: Netlist Inc.

PTO/SB/96 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Netlist, Inc.

Application No./Patent No.: 7,286,436 Filed/Issue Date: 23-Oct-2007

Titled:

HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS

Netlist, Inc., a Corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. [X] the assignee of the entire right, title, and interest in;

2. [ ] an assignee of less than the entire right, title, and interest in
(The extent (by percentage) of its ownership interest is _____ %); or

3. [ ] the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. [X] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 016949, Frame 0295, or for which a copy therefore is attached.

OR

B. [ ] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet(s).

[X] As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature	October 1, 2012 Date
Gail Sasaki Printed or Typed Name	VP and CFO Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	13925141
Application Number:	11075395
International Application Number:	
Confirmation Number:	8121
Title of Invention:	HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS
First Named Inventor/Applicant Name:	Jayesh R. Bhakta
Customer Number:	20995
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018A
Receipt Date:	05-OCT-2012
Filing Date:	07-MAR-2005
Time Stamp:	18:15:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	poa7286436.pdf	233027 d709b5e17b97e364f83c0d291c72fc025f4ce80f	no	2

Warnings:

The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing

Information:

Total Files Size (in bytes):	233027

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/075,395	03/07/2005	Jayesh R. Bhakta	NETL.018A

CONFIRMATION NO. 8121

POA ACCEPTANCE LETTER

79141
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

OC000000057371421

Date Mailed: 11/01/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/31/2012.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/dolipscomb/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/075,395	03/07/2005	Jayesh R. Bhakta	NETL.018A

CONFIRMATION NO. 8121

POWER OF ATTORNEY NOTICE

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

OC000000057371397

Date Mailed: 11/01/2012

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/31/2012.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/dolipscomb/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Docket No.: NETL.018A Customer No. 79141

ASSERTION OF ENTITLEMENT TO SMALL ENTITY STATUS UNDER 37 CFR 1.27

Applicant	:	Bhakta, et al.
App. No.	:	11/075,395
Filed	:	March 7, 2005
Patent No.		7286436
Issued		10/23/2007
For	:	HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS
Examiner	:	NGUYEN, VAN THU
Art Unit	:	2824
Conf. No.	:	8121
Docket No.	:	NETL.018A

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The Assignee, Netlist, Inc., of all rights and title to the above-identified patent is a small entity concern as defined in 37 C.F.R. 1.27(a). Assertion of entitlement to small entity status under 37 C.F.R. 1.27(c) is hereby made for this patent.

Applicants acknowledge the duty to file notification of a loss of entitlement to small entity status in the patent prior to paying, or at the time of paying, any maintenance fee due after the date on which status as a small entity is no longer appropriate.

Respectfully submitted,

Date: April 22, 2015

/Jamie J. Zheng/ 51167
Jamie J. Zheng (Reg. No.)
Customer No. 79141

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY.DOCKET NO./TITLE	REQUEST ID
11/075,395	03/07/2005	Jayesh R. Bhakta	129980-5005US	67126

Acknowledgement of Loss of Entitlement to Entity Status Discount

The entity status change request below filed through Private PAIR on 07/06/2018 has been accepted.

CERTIFICATIONS:

Change of Entity Status:

X Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be notification of loss of entitlement to small or micro entity status, as applicable.

This portion must be completed by the signatory or signatories making the entity status change in accordance with 37 CFR 1.4(d)(4).

Signature:	/Jamie J. Zheng/
Name:	Jamie J. Zheng
Registration Number:	51167