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Bhakta et al.

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(54) **MEMORY MODULE DECODER**

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Related U.S. Application Data

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(51) **Int. Cl.**

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G11C 8/12	(2006.01)
G06F 12/02	(2006.01)
G11C 5/04	(2006.01)
G11C 5/06	(2006.01)
G11C 7/10	(2006.01)
H05K 1/18	(2006.01)

(52) **U.S. Cl.**
CPC ***G11C 8/12*** (2013.01); ***G06F 12/0207*** (2013.01); ***G06F 12/0215*** (2013.01); ***G11C 5/04*** (2013.01); ***G11C 5/066*** (2013.01); ***G11C 7/1048*** (2013.01); ***H05K 1/181*** (2013.01); *G11C 2207/105* (2013.01); *H05K 2201/10159* (2013.01); *H05K 2203/1572* (2013.01); *Y02P 70/611* (2015.11)

(58) **Field of Classification Search**
None
See application file for complete search history.

(56) **References Cited**

To view the complete listing of prior art documents cited during the proceedings for Reexamination Control Numbers 95/000,546 and 95/000,577, please refer to the USPTO's public Patent Application Information Retrieval (PAIR) system under the Display References tab.

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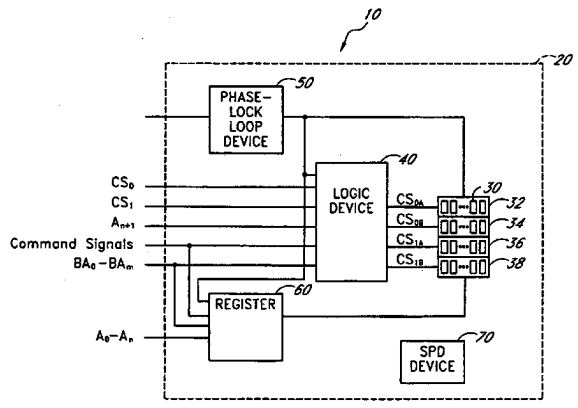
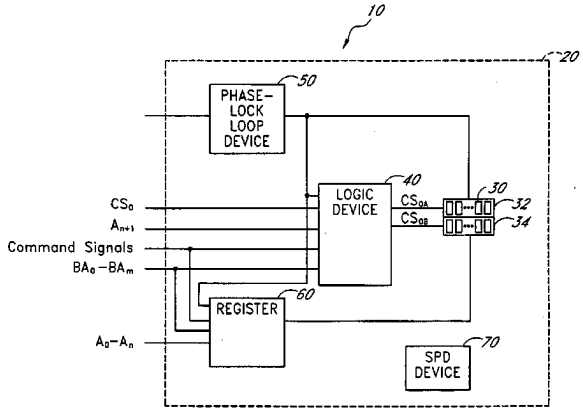
(57) **ABSTRACT**

A memory module connectable to a computer system includes a printed circuit board, a plurality of memory devices coupled to the printed circuit board, and a logic element coupled to the printed circuit board. The plurality of memory devices has a first number of memory devices. The logic element receives a set of input control signals from the computer system. The set of input control signals corresponds to a second number of memory devices smaller than the first number of memory devices. The logic element generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices.





INTER PARTES REEXAMINATION CERTIFICATE

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

Claims **1-13** are cancelled.

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