Paper No. 1

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner

Patent No. 7,619,912
Issued: November 17, 2009
Filed: September 27, 2007
Inventors: Jayesh R. Bhakta and Jeffrey C. Solomon
Title: MEMORY MODULE DECODER

Inter Partes Review No. IPR2022-00615

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,619,912

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EXHIBIT LIST

Exhibit #	Reference Name
1001	U.S. Patent No. 7,619,912 with *Inter Partes* Reexamination Certificate
1002	File History of U.S. Patent No. 7,619,912
1003	Declaration of Dr. Wolfe
1004	Curriculum Vitae of Dr. Wolfe
1005	U.S. Provisional Application No. 60/588,244
1006	U.S. Provisional Application No. 60/550,668
1007	U.S. Provisional Application No. 60/575,595
1008	U.S. Patent No. 7,289,386
1009	U.S. Patent No. 7,286,436
1010	Prosecution History for *Inter Partes* Reexamination No. 95/000,578 of the 912 Patent
1011	Decisions by the PTAB in *Inter Partes* Reexamination Nos. 95/000,578; 95/000,579; and 95/001,339 of the 912 Patent
1012	*Inter Partes* Reexamination Certificate for the 912 Patent (Feb. 8, 2021)
1013	Affirmance of the Examiner's Decision on Reexamination of '386 Patent (Feb. 25, 2015)
1014	Reexamination Certificate for '386 Patent (Aug. 19, 2016)
1015	U.S. Patent No. 7,636,274
1016	Appeal 2017-007075 Affirmance of the Examiner's Decision on Reexamination of '274 Patent (May 9, 2017)
1017	Reexamination Certificate for '274 Patent (Nov. 5, 2018)

Exhibit #	Reference Name
1018	U.S. Patent No. 7,881,150
1019	IPR2014-00882 Final Written Decision on Remand (’150 patent) (March 29, 2018)
1020	IPR2014-01011 Final Written Decision on Remand (’150 patent) (March 29, 2018)
1021	U.S. Patent No. 8,081,536
1022	IPR2014-00883 Final Written Decision on Remand (’536 patent) (March 29, 2018)
1023	IPR2015-01021 Final Written Decision (’536 patent) (Sept. 28, 2016)
1024	U.S. Patent No. 8,756,364
1025	IPR2017-00549 Final Written Decision (’364 patent) (May 3, 2018)
1026	U.S. Patent No. 7,532,537
1027	IPR2017-00667 Final Written Decision (’537 patent) (July 18, 2018)
1028	IPR2017-00668 Final Written Decision (’537 patent) (July 18, 2018)
1029	JEDEC JESD79-2 standard for DDR2 SDRAM (Sept. 2003)
1030	JEDEC JESD79 standard for DDR SDRAM (June 2000)
1031	Carlson Declaration for JESD79
1032	JEDEC JESD21-C design specification for DDR SDRAM Registered DIMM (January 2002)
1033	Bruce Jacob et al., Memory Systems: Cache, DRAM, Disk (2008)
1034	Bruce Jacob, *Synchronous DRAM Architectures, Organizations, and Alternative Technologies* (Dec. 10, 2002)
1035	U.S. Patent No. 7,363,422 to Perego et al.

Exhibit #	Reference Name
1036	U.S. Patent Pub. No. 2006/0117152 to Amidi et al.
1037	U.S. Patent Pub. No. 2006/0277355 to Ellsberry et al.
1038	IPR2018-00362 Final Written Decision (Patent 9,606,907) (June 27, 2019)
1039	Carlson Declaration for JESD79-2
1040	Carlson Declaration for JESD21-C
1041	U.S. Patent. No. 5,513,135 to Dell et al.
1042	J.P. 2002-184176 to Masashi
1043	Harold S. Stone, Microcomputer Interfacing (1982)
1044	U.S. Patent No. 6,209,074 to Dell et al.
1045	Google's Motion to Strike Netlist's New Assertion of Claim 16 of the 912 Patent, *Netlist, Inc. v. Google LLC*, No. 4:09-cv-05718 (N.D. Cal. filed July 30, 2021)
1046	Order Staying Discovery and Other Deadlines Pending Resolution of Motions, *Netlist, Inc. v. Google LLC*, No. 4:09-cv-05718 (N.D. Cal. filed Sept. 3, 2021)
1047	Order Continuing Hearing on Motions, *Netlist, Inc. v. Google LLC*, No. 4:09-cv-05718 (N.D. Cal. filed Nov. 9, 2021)
1048	Notice Setting Hearing on Motions, *Netlist, Inc. v. Google LLC*, No. 4:09-cv-05718 (N.D. Cal. filed Jan. 27, 2022)
1049	Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)
1050	Stipulation extending response to amended complaint to February 16, 2022, *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Dec. 30, 2021)

Exhibit #	Reference Name
1051	First Amended Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Jan. 18, 2022)
1052	Netlist's motion to dismiss the First Amended Complaint, *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Feb. 16, 2022)

CLAIM LISTING

Ref. #	Listing of Challenged Claims
[16.pre]	A memory module connectable to a computer system, the memory module comprising:
[16.a]	a printed circuit board;
[16.b]	a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board,
[16.b.i]	the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;
[16.c]	a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register,
[16.c.i]	the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal,
[16.c.ii]	the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks,
[16.c.iii]	the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks,
[16.c.iv]	wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and
[16.d]	a phase-lock loop device coupled to the printed circuit board,

Ref. #	Listing of Challenged Claims
[16.d.i]	the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,
[16.e]	wherein the command signal is transmitted to only one DDR memory device at a time.

I. PETITIONER'S MANDATORY NOTICES

A. Real Party-in-Interest (37 C.F.R. § 42.8(b)(1))

The real parties in interest are the Petitioner Samsung Electronics Co., Ltd.; and Samsung Semiconductor, Inc.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

The following judicial or administrative matters would affect, or be affected by, a decision in this proceeding concerning U.S. Patent No. 7,619,912.

The following proceedings are currently pending:

- *Netlist, Inc. v. Google LLC*, No. 4:09-cv-05718 (N.D. Cal. filed Dec. 4, 2009)
- *Samsung Electronics Co., Ltd. et al. v Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)
- U.S. Patent Application No. 17/403,832

The following proceedings are no longer pending:

- *Inter partes* Reexamination Nos. 95/000,578; 95/000,579; and 95/001,339 of U.S. Patent No. 7,619,912
- *Inter partes* Reexamination Nos. 95/000,546 and 95/000,577 of U.S. Patent No. 7,289,386

- *Inter partes* Reexamination Nos. 95/001,337 of U.S. Patent No. 7,636,274
- IPR2014-00882 of U.S. Patent No. 7,881,150
- IPR2014-00883 of U.S. Patent No. 8,081,536
- IPR2015-01021 of U.S. Patent No. 8,081,536
- IPR2017-00549 of U.S. Patent No. 8,756,364
- IPR2017-00667 of U.S. Patent No. 7,532,537
- IPR2017-00668 of U.S. Patent No. 7,532,537

C. Lead and Back-up Counsel (37 C.F.R. § 42.8(b)(3))

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D. Service Information (37 C.F.R. § 42.8(b)(4))

Service information is provided in the designation of counsel above. Petitioner consents to service of all documents via electronic mail to DLSamsungNetlistIPRs@BakerBotts.com.

II. INTRODUCTION

Petitioner respectfully requests trial on claim 16 of reexamined U.S. Patent 7,619,912 ("912 Patent")(EX1001) based on grounds not previously considered. The Board has already found many claims in this patent family invalid. EX1012-28.

III. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW

A. Certification the Patent May Be Contested by Petitioner (§42.104(a))

Petitioner certifies that the 912 Patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the 912 Patent claims on the grounds identified below.

B. Identification of Challenge (§42.104(b))

Petitioner challenges claim 16 of the reexamined 912 Patent (reprinted above on page x) on the following grounds:

Ground	Claims Challenged	35 U.S.C. §	References
1	16	103(a)	Perego
2	16	103(a)	Perego, Amidi
3	16	103(a)	Ellsberry

Petitioner's proposed claim constructions and the precise reasons why the claims are unpatentable are provided below. The evidence relied upon in this petition is listed above on page vi.

IV. RELEVANT INFORMATION CONCERNING THE CONTESTED PATENT

A. Effective Filing Date

The application for the 912 Patent, EX1002, is based on three provisional applications filed July 15, 2004 (EX1005, "the '244 provisional"), March 5, 2004 (EX1006, "the '668 provisional"), and May 28, 2004 (EX1007, "the '595 provisional"). EX1001,Front Page(60). The 912 Patent is also a continuation of an application filed July 1, 2005 (EX1008, "the '386 patent"), which is a continuation-in-part of an application filed March 7, 2005 (EX1009, "the '436 patent). EX1001,Front Page(63);EX1003,¶¶46-48.

The prior art for Grounds 1 and 2 predates March 5, 2004, and thus for those Grounds it does not matter if the claims of the 912 Patent can claim priority to the earliest provisional application. For Ground 3, which depends on a reference filed June 1, 2005, Petitioner contends that there is not adequate support for claim 16 of the 912 Patent in any of the applications before July 1, 2005, as explained below. *Infra*,§VI.B.1,pp.63-69;EX1003,¶¶49,189-196.

B. Person of Ordinary Skill in the Art

A POSITA in the field of memory module design in 2004 or 2005 would have had an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working the field. She would have been familiar with

various standards of the day including the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with the memory controller of a computer system. Specifically, she would have been knowledgeable about the JEDEC DDR (EX1030,EX1031) and DDR2 (EX1029,EX1039) SDRAM standards used to standardize the functioning of memory devices, and the JEDEC 21-C (EX1032,EX1040) standard used to specify different possibilities for the physical layout of memory devices on a module as well as different possibilities for density and organization of the memory devices to achieve a given memory capacity. Indeed, the 912 Patent refers to JEDEC and standardized memory devices and modules. EX1001 at 12:28,12:34,12:39-43. She would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs and CPLDs and more low-level circuits such as tri-state buffers, flip flops and registers. EX1003,¶¶50-52.

C. <u>The 912 Patent</u>

1. Technical Overview

The 912 Patent seeks to improve the capacity of a memory module, in part by appearing to the computer system as if it had higher density memory devices than it physically has. EX1001,32:26-38,6:64-7:19;EX1003,¶55-56.

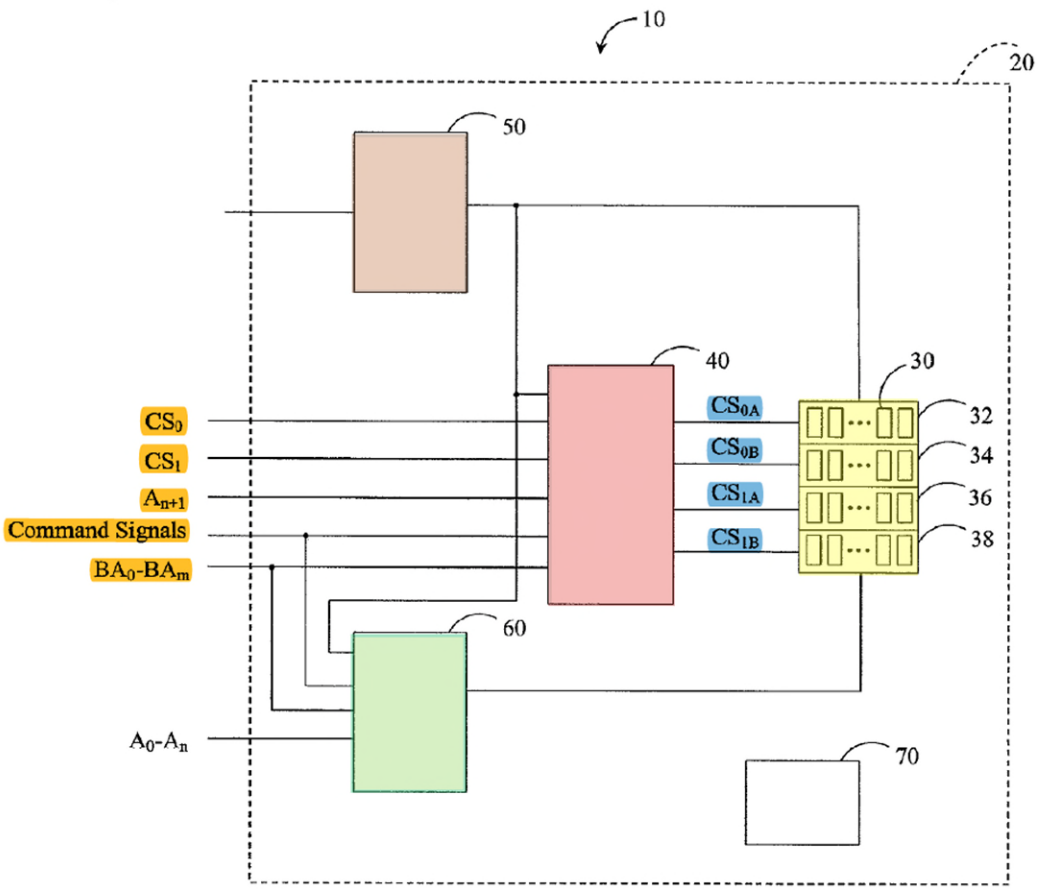
This is commonly called "rank multiplication."

"[T]he ranks of a memory module are selected or activated by address and command signals," which include "chip-select signals." EX1001,2:35-39. Dr. Wolfe explains that "[c]hip-select signals are standard signals in the JEDEC standards for DDR (sometimes called DDR-1) and DDR-2 memory devices." *See* EX1003,¶¶51,54,73-77. DDR memory devices are specifically listed as compatible with the claimed invention in the 912 Patent. EX1001,6:12-16,22:5-14;EX1003,¶54.

In particular, the 912 Patent (EX1001) discloses a memory module (10), including a "first number" of memory devices (30, yellow), a logic element (40, red), a phase-lock loop device (50, brown), and a register (60, green) on a printed circuit board (20). EX1001,5:6-45,FIG.1A. The logic element (40) receives a set of input control signals (orange), including two chip select signals (CS_0, CS_1), a row/column address signal (A_{n+1}), Command Signals, and bank address signals (BA_0-BA_m), all from a system memory controller (not shown). *Id.*;*see also*,*id.*,6:55-63. A "second number" of memory devices smaller than the "first number" of memory devices (yellow) on the module corresponds to the set of input control signals from the system memory controller. *Id.*,6:64-7:19. The "first number" of memory devices on the module correspond to a set of output signals (blue), including four chip select signals (CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B}) generated by the

logic element (40). *Id*.,7:35-8:64. In Figure 1A, the logic element 40 receives ***two*** chip select signals corresponding to ***two*** ranks, and the "first number" of memory devices (yellow) on the module are organized into ***four*** ranks 32, 34, 36, 38, which each receive a respective one of the ***four*** chip select signals (blue) generated by the logic element (40). *Id*.,6:31-34,7:20-29,7:35-39,7:55-8:64;EX1003,¶53.

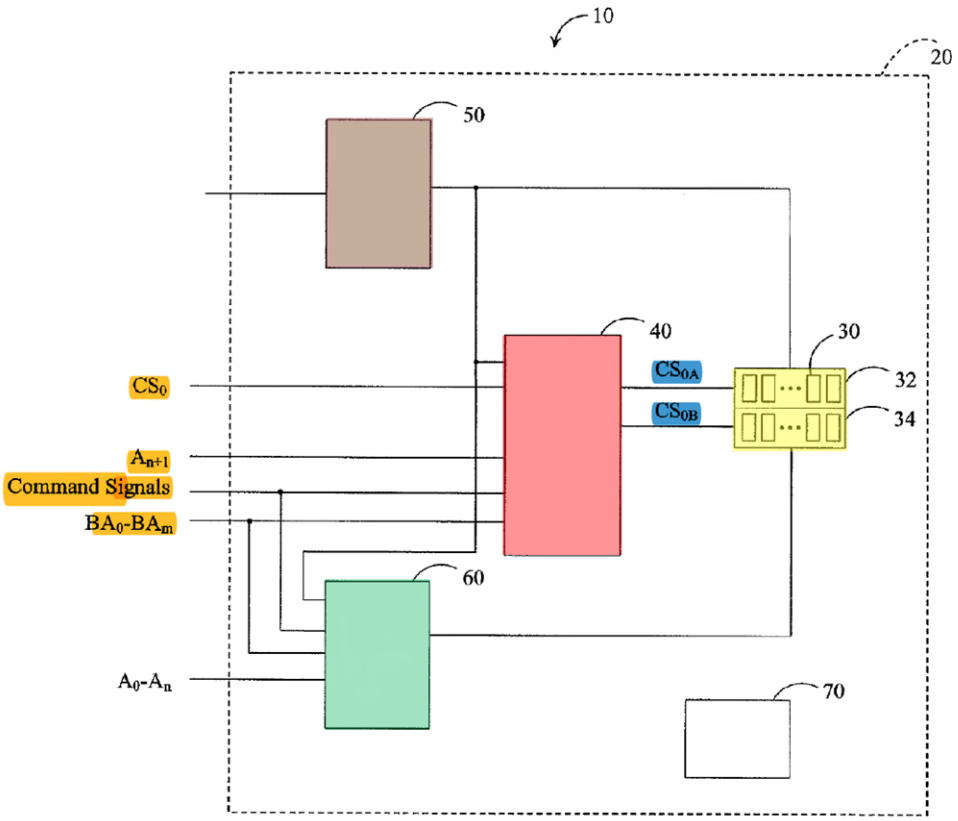
Figure 1A:



In another embodiment shown in Figure 1B below, the module receives a ***single*** chip select signal (CS_0, orange) corresponding to a ***single*** rank ("second number of ranks") and the logic element (40, red) generates ***two*** chip select signals

(CS_{0A} and CS_{0B}, blue, below) corresponding to ***two*** ranks of memory devices on the module ("first number of ranks"). EX1001,7:3-9&FIG.1B;EX1003,¶53.

Figure 1B:



However, using two memory devices to imitate a single memory device of higher capacity may cause "collisions" "between back-to-back adjacent read commands which cross memory device boundaries" because the system is not aware of the physical device boundaries. EX1001,23:60-24:12,FIG.5;*see also infra*,§VI.B.1,pp.63-69;EX1003,¶¶57,192-194. The 912 Patent prevents these collisions by selectively connecting the data bus to only one of the physical ranks at a time. *Id.*,24:23-25;EX1003,¶57.

2. Summary of the Prosecution History

The 912 Patent originally issued without any official rejections. EX1002,47-21,503-15,517-20. During *inter partes* reexamination, however, all claims were either cancelled or amended, EX1010-12, including claim 16, EX1010,3106-07;EX1001,43-44. EX1003,¶¶58-61.

Amidi (EX1036) was the primary reference during reexamination. *See,e.g.*,EX1010,1393-1406,3844-45,4704-05,7014-16,7708-09. Patent Owner acknowledged that Amidi "is probably the closest reference," EX1010,1502, but argued that Amidi fails to disclose or render obvious a "logic element" that uses "bank address signals" to generate "output control signals in response to input control signals, which include bank address signals," as required by all of the claims of the 912 Patent (including claim 16). *Id.*,1502-06,1646-50;EX1010,4003. The Board found that Amidi discloses both a "register" and a "logic element" that receive bank address signals, but not "the limitation of generating a CAS or chip-select signal in response to a bank address signal," EX1010,7036-37,7074-78. However, the Board found various claims obvious in light of Amidi in combination with other references. EX1010,7084-85,7096,7099-7104. In response, Patent Owner amended some claims (but ***not*** claim 16) to overcome these rejections. EX1010, 7317,7319-21,7712-13,7719-20,7720-21,7723-24,7726-27,7733-34,7737,7865-75,7933. EX1003,¶¶62-63.

Patent Owner also argued that Amidi failed to render obvious a PLL "operatively coupled" to the "logic element" as required by all of the claims of the 912 Patent (including claim 16) and that the construction of "operatively coupled" should be narrowed to require that "the operations of the logic element 40 are clocked either directly or indirectly (e.g., through a clock buffer) by the output of the PLL 50" and "the output of the PLL 50 controls the operation of the logic element 40." EX1010,1506-10,1656-60;EX1003,¶64.

With respect to claim 16, the Board agreed that Amidi did not disclose the last limitation of claim 16, "the command signal is transmitted to only one DDR memory device at a time." EX1010,7078-80,7742;EX1003,¶65.

D. Construction of Terms Used in the Claims

Except as set forth below, Petitioner contends for purposes of this proceeding that no further construction of the claim terms is needed, given that the prior art satisfies the ordinary meaning of the claim terms as well as the examples provided in the 912 Patent.

1. "rank" and "chip select signal"

The terms "rank" and "chip select signal" were common at the time of the 912 Patent. *E.g.*,EX1029,6("Chip Select: … $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command

code.”);EX1033,413;EX1032,4.20.4-10 to -16 (showing one chip-select signal for the memory devices that create the full bit-width of the module);EX1003,¶75.

A POSITA would have understood that “rank” refers to “an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip select signals, to read or write the full bit-width of the memory module.” EX1003,¶74. This is supported in the 912 Patent’s disclosure that “DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width.” EX1001,2:16-18. “During operation, the ranks of a memory module are selected or activated by address and command signals that are received from the processor. Examples of such address and command signals include, but are not limited to, rank-select signals, also called chip-select signals.” *Id.*,2:35-39; EX1003,¶73.

As already recognized by the Board, the term “bank” (or “physical bank”) was also sometimes used to refer to what is now typically called a “rank.” EX1003,¶76;EX1033,413;EX1023,13-14,20,28(invalidating claims to “ranks” based on “banks” in prior art); *compare* EX1030,7(“chip select” selects the “bank”), *with* EX1029,6(“chip select” selects the “rank”); *see also* EX1032,4.20.4-6(describing “S0-S3 SDRAM chip select lines” to select “Physical banks 0, 1, 2, and 3”); *id.*,4.20.4.10-16. Thus a POSITA would understand that “bank” and

"physical bank" could be used to mean the same thing as "rank" (given the "chip-select signal"):

10.2.2 Rank

Figure 10.5 shows a memory system populated with 2 ranks of DRAM devices. Essentially, a *rank* of memory is a *"bank"* of one or more DRAM devices that operate in lockstep in response to a given command. However, the word *bank* has already been used to describe the number of independent DRAM arrays within a DRAM device. To lessen the confusion associated with overloading the nomenclature, the word *rank* is now used to denote a set of DRAM devices that operate in lockstep to respond to a given command in a memory system.

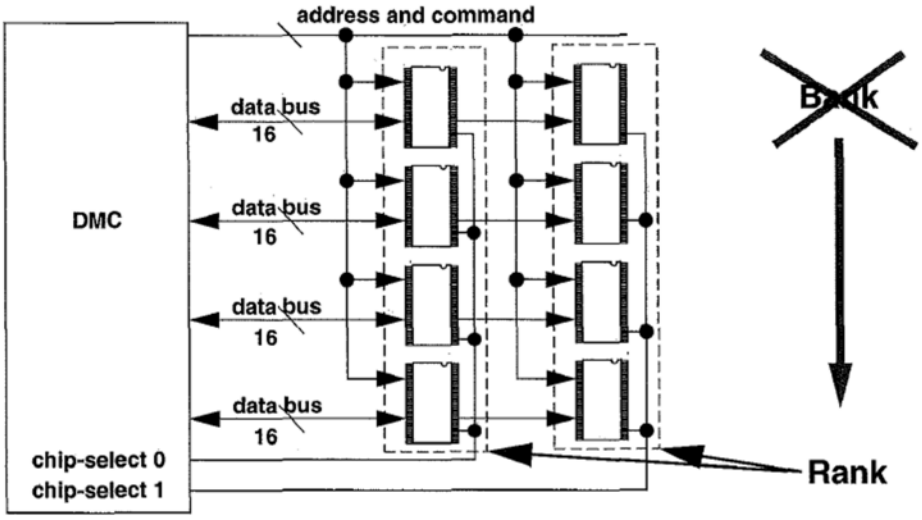


FIGURE 10.5: Memory system with 2 ranks of DRAM devices.

EX1033,413;*see also*,EX1034,4n.3,9;EX1003,¶76.

A "rank" comprises "one or more DRAM devices." EX1033,413. For example, the 912 Patent describes an embodiment with one memory device in each "rank": "[i]n certain embodiments, the command signal is passed through to the

selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to ***only one memory device*** or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices . . . ." EX1001 at 8:50-58.[1] In this embodiment, where there is only one memory device in the "rank," the bit width of the "rank" would be the same as the bit width of the memory device, for example 16 bits. The 912 Patent explains that "memory devices . . . having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein." *Id.*,6:16-:19. EX1003,¶77.

V. OVERVIEW OF THE PRIOR ART

A. Perego (EX1035)

U.S. Patent No. 7,363,422 to Perego ("Perego"), filed January 28, 2004 and published September 23, 2004, is prior art under §102(a)&(e). EX1035.

Perego discloses a flexible memory module compatible with "rank multiplication": Perego's memory module allows "[n]ew generations of memory devices [to] be phased in" with an existing system memory controller simply by

[1] Unless stated otherwise, all emphases in quotes have been added.

modifying the "buffer device" on the module, all while maintaining backward compatibility. EX1035,2:26-29,6:34-43;EX1003,¶81.

As shown below, Perego teaches a memory system 305, including a memory controller 310 connected to multiple buffered memory modules 330a-330n, such as memory module 340 (representing memory module 330a) which itself includes a buffer device (350, red) and multiple groups of memory devices (360, green and blue). EX1035,Abstract,4:63-5:15,FIG.3B (annotated below);EX1003,¶79.

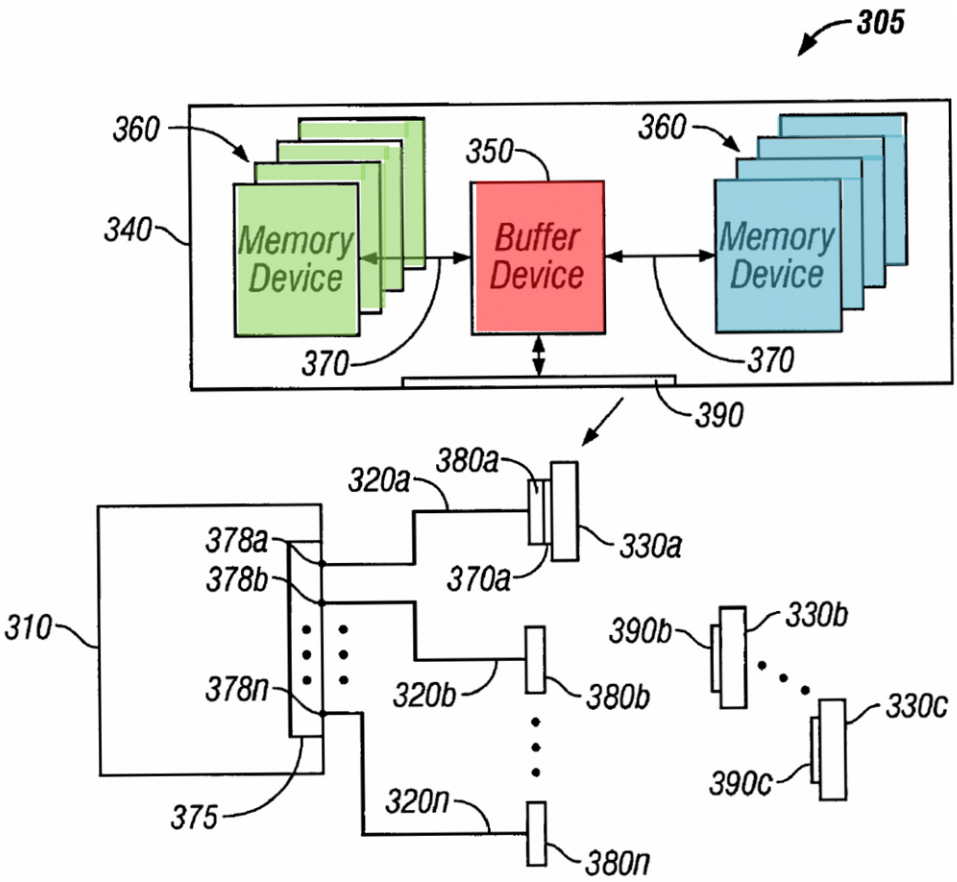


FIG. 3B

Perego's FIG. 3C (below) shows a buffered module 395, including a configurable width buffer device 391(red) and memory devices 360 organized in groups (green, blue), that can be used in conjunction with the memory system described above. EX1035,7:30-34,FIG.3C(annotated below);EX1003,¶80.

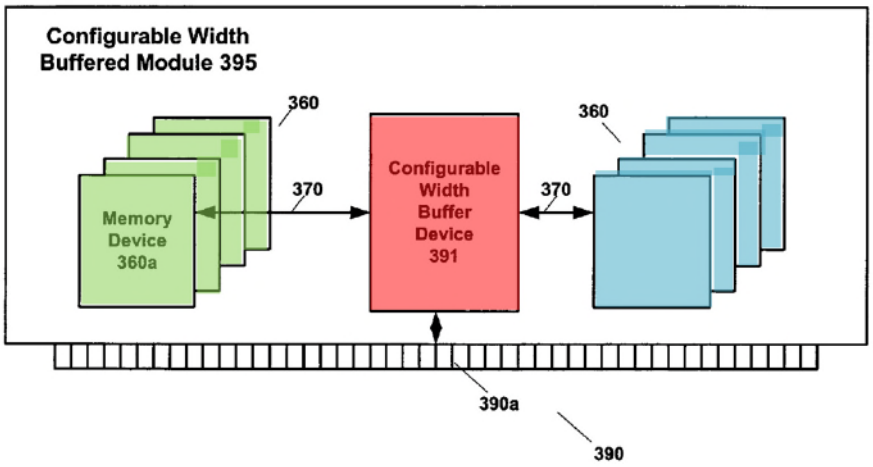


Fig. 3C

Perego's FIG. 5B (below) illustrates one implementation of "a configurable width buffer device 391 as seen in FIG. 3C," shown above. EX1035,13:6-10,FIG.5B. Buffer device 391 includes programmable interfaces 520a and 520b, which accommodate different numbers and types of memory devices, while configurable width interface 590 communicates with the memory controller. *Id*.,13:60-14:15;EX1003,¶82. In addition, serial interface 574 and operations circuit 572 provide information to the system memory controller for proper configuration and operation of the system. EX1035,12:20-34,FIGS.5A-5B;EX1003,¶84

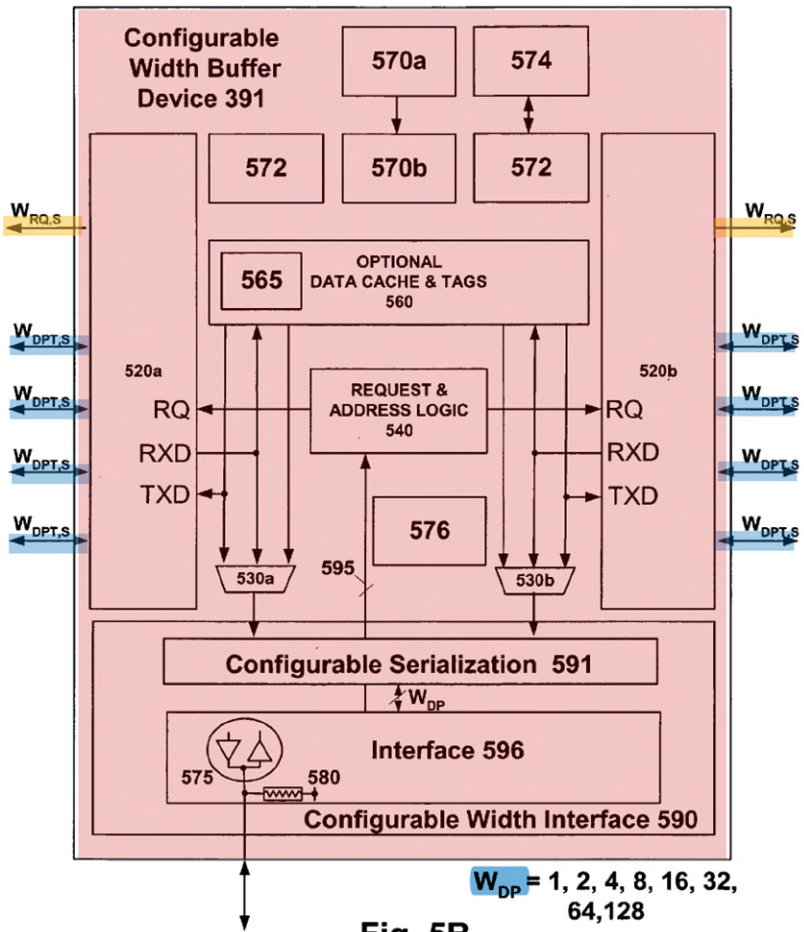


Fig. 5B

An embodiment of the configurable width interface 590 (below) includes input and output latches 597f–m (blue), or two latches for each data connection of the configurable width buffer device. EX1035,FIG.5C(annotated below),17:22-26,17:61-67;EX1003,¶83.

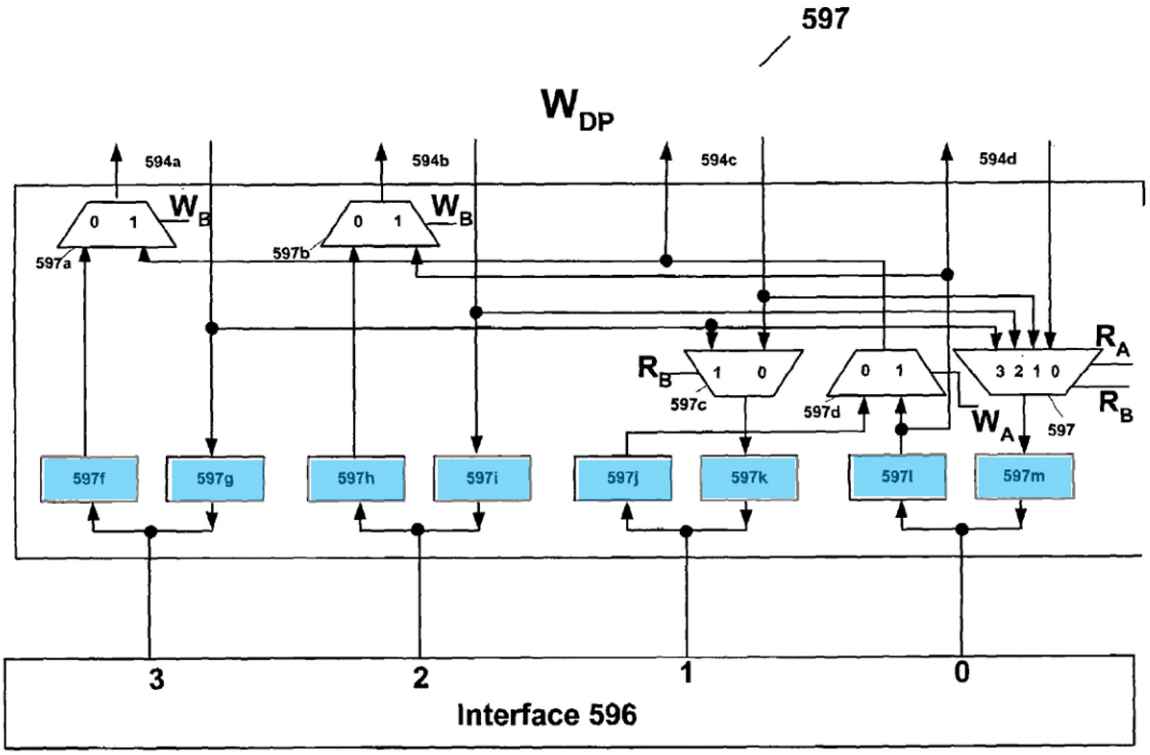


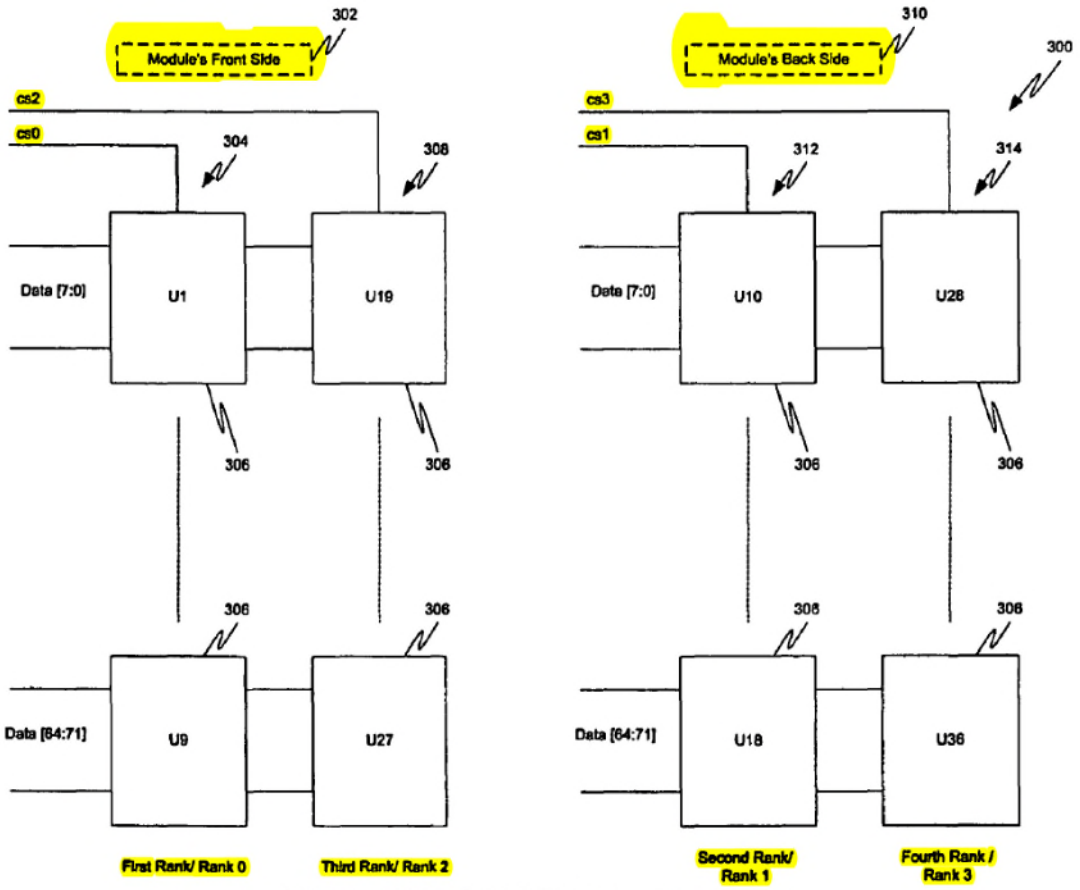
Fig. 5C

B. <u>Amidi (EX1036)</u>

US2006/017152 to Amidi ("<u>Amidi</u>"), published January 5, 2004, is prior art under §102(a)&(e). EX1036.

<u>Amidi</u> focuses on "rank multiplication": <u>Amidi</u> solves the need "for a transparent four rank memory module fitting into a memory socket having two chip select signals routed." EX1036,[0011]. This need exists "[b]ecause memory devices with lower densities are cheaper and more readily available." *Id.*,[0008];EX1003,¶86-88.

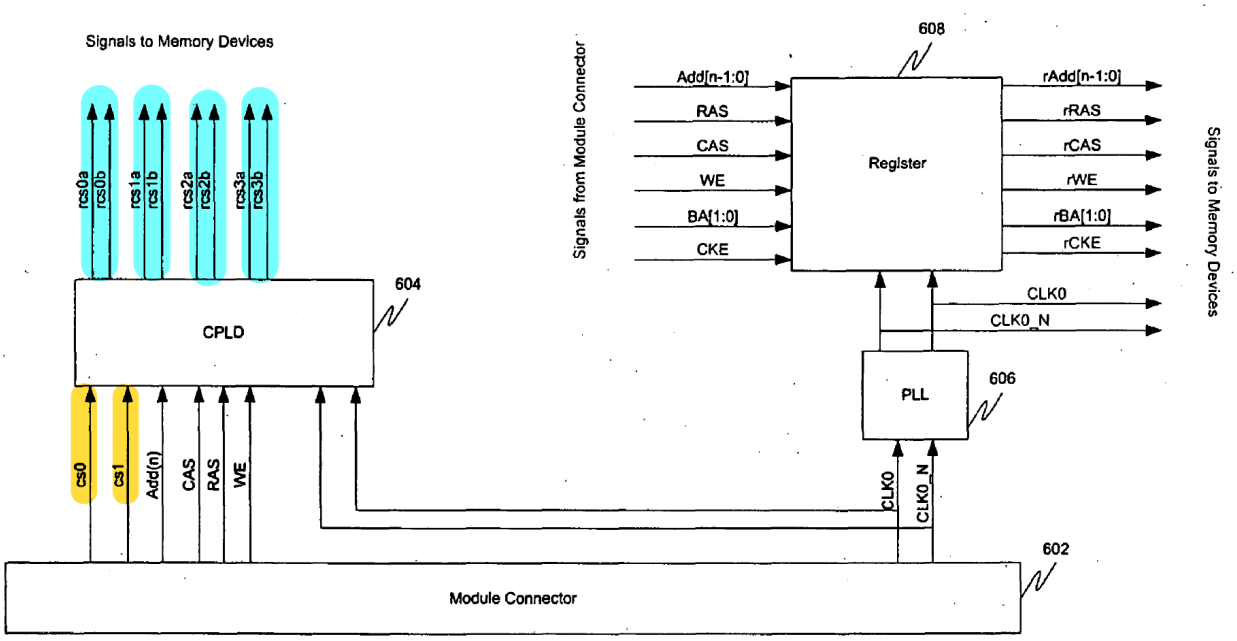
Each rank of Amidi's memory module has a corresponding chip select signal as shown in Amidi's Figure 3 (annotated below, showing four ranks, each receiving a respective chip select signal, cs0-cs3);EX1003,¶86-88.



Transparent Four Rank DDR Module Block Diagram
FIG. 3

Amidi's memory module includes a "[Complex Programmable Logic Device] CPLD 410 [which] emulates a two rank memory module on the four rank memory module 400. . . ." EX1036,[0041],FIG.4A;EX1003,¶89. Amidi's CPLD also "ensures that all commands for a two rank memory module conveyed by the module connector 602 are also performed on the four rank memory modules." EX1036,[0052]. To activate these ranks properly for all commands, Amidi's

CPLD uses command signals in addition to the chip select signals and the row address, and generates four chip select signals (one for each rank) as shown in the detailed block diagrams of Amidi's Figures 8 and 6A (annotated below, showing two received chip selects in orange and four generated chip selects in light blue). EX1036,[0043],[0050],[0052],[0064],FIGs.5,6A,8; EX1003,¶¶90-91.



Row Address Decoding
FIG.6A

Amidi also explains that other families or densities of memory devices "may be used to build the four rank memory module." EX1036,[0071];EX1003,¶92.

C. Ellsberry (EX1037)

US2006/0277355 to Ellsberry ("Ellsberry")(EX1037), filed June 1, 2005, is prior art under §102(a)&(e), assuming a priority date for the 912 Patent of July 1,

2005, *see infra*,§VI.B.1,pp.63-69;EX1003,¶¶189-196. In a Final Written Decision against Patent Owner involving another patent, the Board made numerous findings about what Ellsberry discloses. EX1038;EX1003,¶93. Those findings are now binding against Patent Owner. *MaxLinear, Inc. v. CF CRESPE LLC*, 880 F.3d 1373, 1377-78 (Fed. Cir. 2018).

Ellsberry also focuses on "rank multiplication": Ellsberry discloses a memory module that "expands the addressable memory banks on a module by making two smaller-capacity memory devices emulate a single higher-capacity memory device." EX1037,Abstract. Figure 12 illustrates a configuration of a such a memory module. EX1037,[0052],[0055],FIG.12(annotated below). EX1003,¶94.

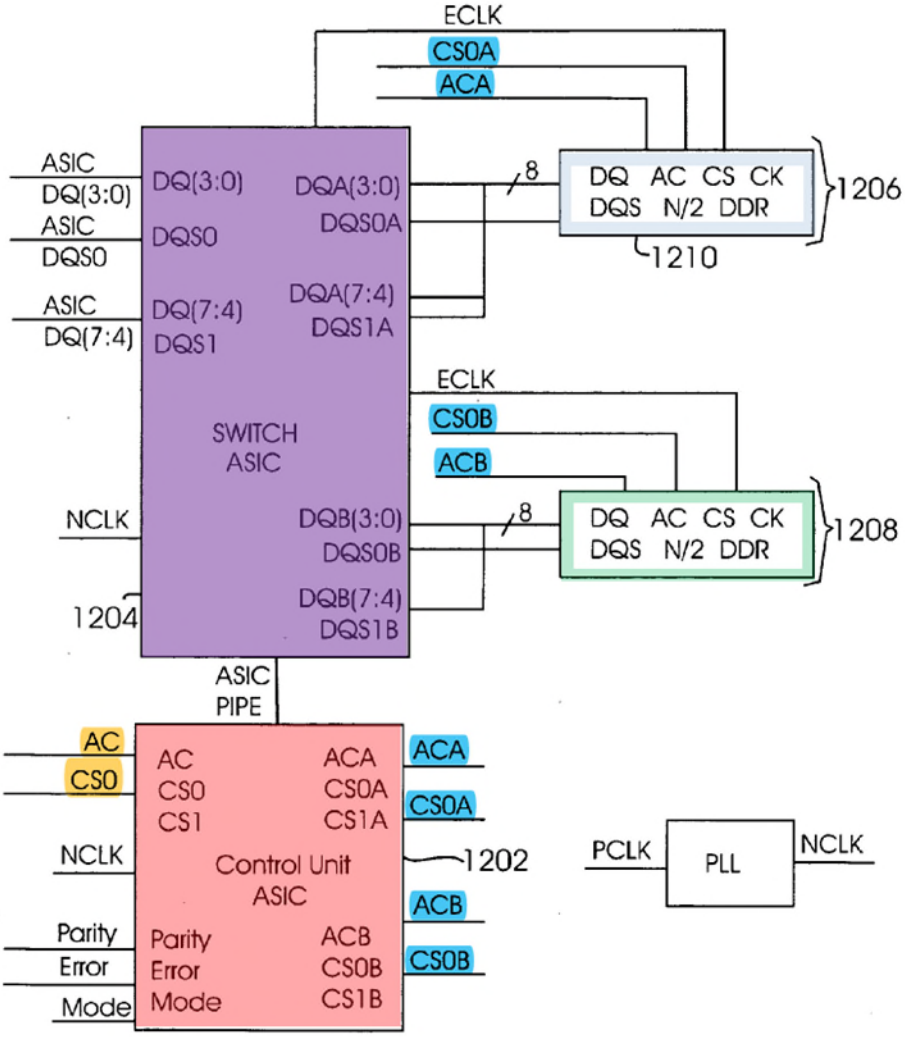


Fig. 12

VI. PRECISE REASONS FOR RELIEF REQUESTED

A. <u>Grounds 1 and 2: Claim 16 Is Obvious Over Perego Alone or In View of Amidi</u>

Claim 16 is obvious in light of <u>Perego</u> alone (Ground 1) or in view of <u>Amidi</u> (Ground 2).

1. Motivation to Combine Perego and Amidi

A POSITA would have been motivated to combine Perego and Amidi for Ground 2. EX1003,¶¶96-106. Both Perego and Amidi are analogous art to the 912 Patent as they are directed to the same field of memory modules and they seek to improve the performance and upgrade flexibility of memory modules. EX1035,3:13-28;EX1036,[0002],[0018];EX1001,1:21-24,5:1-5;EX1003,¶97. They both also teach that the module can hide the type of memory devices actually used from the system memory controller and pretend to have a different type of memory devices, providing further motivation to combine the two teachings. EX1035,10:56-67;EX.1036,[0011];EX1003,¶100.

A POSITA would have been motivated to implement the rank multiplication functionality taught by Amidi in the memory module of Perego to lower the cost and increase upgrade flexibility of the memory modules. EX1036,[0018]. This is bolstered by Perego's disclosure that its buffer device is designed for flexibility and backward compatibility, teaching a POSITA that Perego's memory module can include memory devices of prior generations while interfacing with new generations of memory controllers (or vice versa). EX1035,6:34-43,2:26-30;EX1003,¶¶99,101. These teachings, combined with Amidi's teachings on cost-effectiveness and practicality of using memory devices with lower densities, would have motivated a POSITA to use lower-capacity memory devices in memory

systems configured for higher-capacity memory devices. EX1036,[0018];EX1003,¶¶101,106. A POSITA would also have been motivated to configure Perego's buffer to respond to control signals for a different type of memory device than the one implemented on its module, such as a higher-capacity memory device, as taught by Amidi, to upgrade a system configured to handle those higher-capacity memory devices. EX1035,3:23-28;EX1036,[0071];EX1003,¶¶102-103.

This combination would have been well within the level of skill of a POSITA. For example, both Perego and Amidi disclose to a POSITA how to make a module with one type of memory devices and add an interface that can communicate with a memory controller configured to control a different type of memory device according to the relevant standards at the time. EX1036,[0004],[0047-49],[0055-57];EX1029,7-8;EX1003,¶104. Moreover, a POSITA would have understood that this combination would avoid problems like back-to-back read operations across memory device boundaries, *see supra* p.9, given Perego's teaching of a dedicated channel for each memory device. *See,e.g.,*EX1035,10:17-20,14:4-10,17:34-35,FIG.5D,18:65-66;EX1003,¶105. Therefore, the combination of Perego and Amidi would have provided nothing more than what was expected at the time, a memory module that is built with one type of memory devices, e.g., lower-capacity memory devices, and operates in a system where the memory

controller issues commands for another type of memory devices, such as higher-capacity memory devices. EX1003,¶106.

2. Claim 16

a) ***[16[pre]]:*** *Memory Module*

Perego discloses a "*memory module* [e.g., 340] *connectable to a computer system* [e.g., memory system 305]." EX1003,¶¶107-110.

As shown below in Figure 3B, a memory module, such as 340, is connectable to a computer system, such as memory system 305, including a controller 310 coupled to memory modules, such 330a, 330b and 330c through respective connectors 380a, 380b and 380c. EX1035,FIG.3B(annotated below). Memory module 340 includes a buffer device 350(red) and memory devices 360(green). EX1003,¶108.

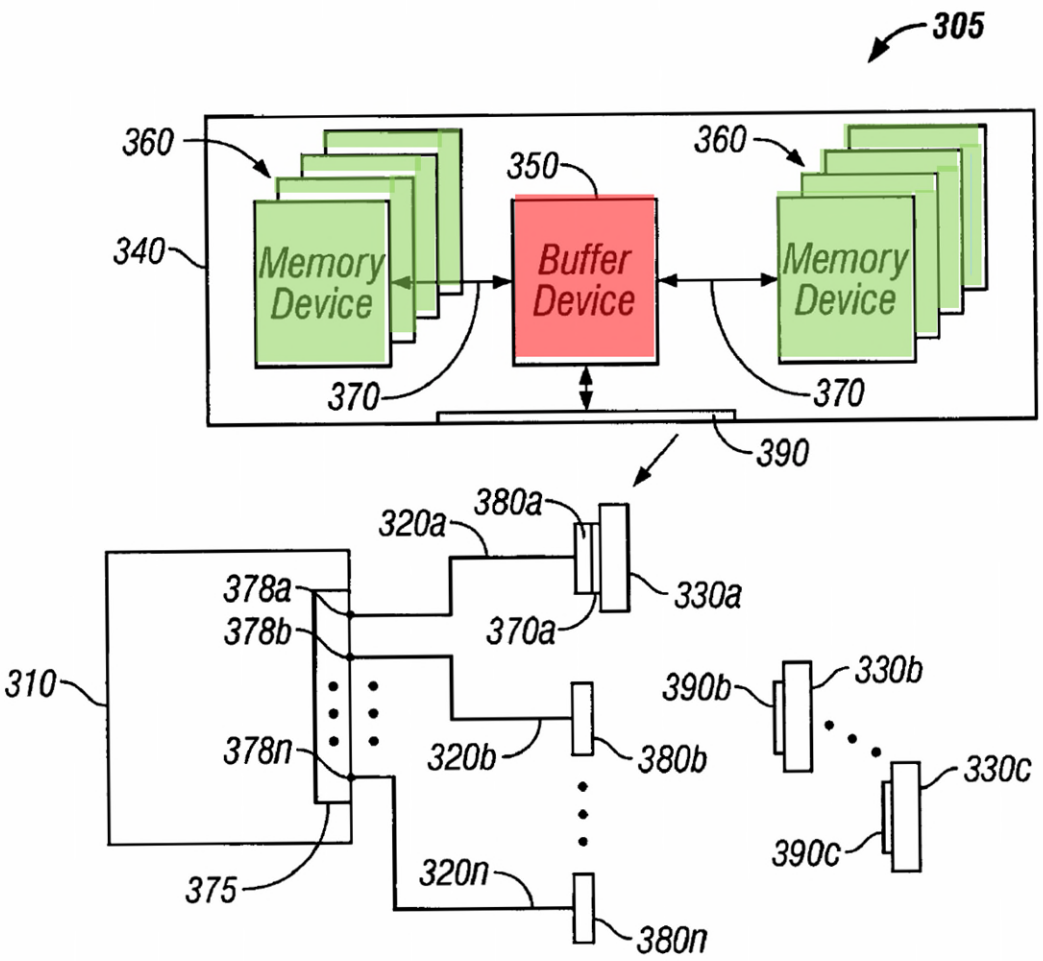


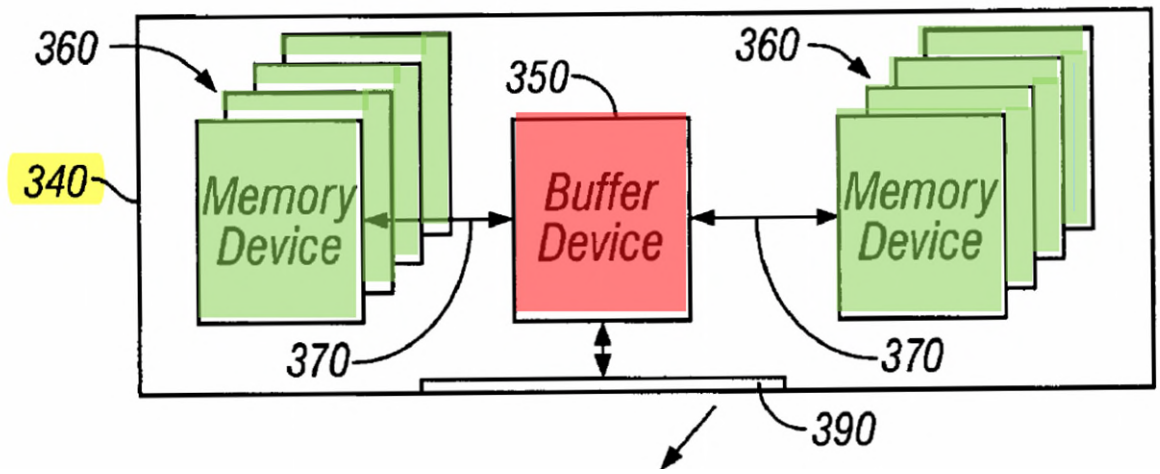
FIG. 3B

Perego teaches that the memory modules (also called "memory subsystems") "are incorporated onto individual substrates… that include connectors 390a-390c...," which include contacts, conducting elements, or pins. EX1035,5:56-6:11,7:39-41,4:19-22;EX1003,¶109.

b) [16.a]: *Printed Circuit Board;*

Perego discloses its memory module includes "*a printed circuit board*." EX1003,¶¶111-113. The memory modules (340, yellow below) "are incorporated onto individual substrates (e.g., PCBs)." EX1035,5:60-62,FIG.3B(annotated and

reproduced below in part). PCB stands for "printed circuit board." *Id.*,5:59-60;EX1003,¶112.

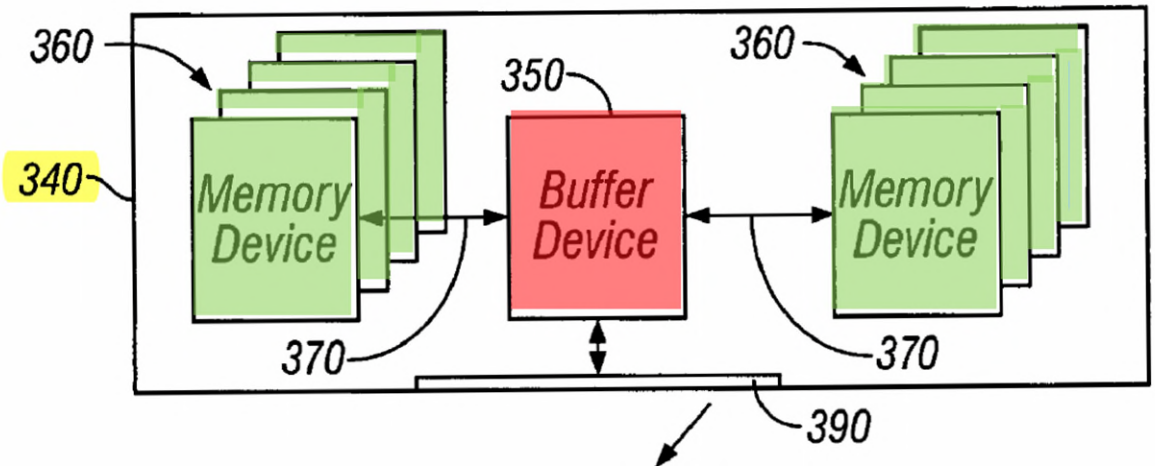


c) [16.b]: *DDR Memory Devices*

Perego discloses "*a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board*." EX1003,¶¶114-117.

Perego teaches that "memory devices 360[(green)] are discretely packaged Synchronous type DRAM integrated circuits (ICs), for example, DDR memory devices, …" EX1035,8:1-9,FIG.3B(annotated above); *see also id.*,3:62-4:3,10:56-59;EX1003,¶115.

These memory devices are coupled to the printed circuit board, as shown above for claim element [16.a]. EX1035,5:60-62,5:59-60,5:3-4;EX1003,¶¶111-113,116. Perego further explains that a "[b]uffer device 350[(red)] is coupled to the plurality of memory devices 360[(green)] via channels 370." *Id.*,5:4-6,FIG.3B(reproduced below in part, annotated),6:12-15;EX1003,¶116.



d) [16.b.i]: *First Number of Ranks*

Perego alone or in view of Amidi teaches [16.b.i]. EX1003,¶¶118-126.

Perego discloses, "*the plurality of DDR memory devices having a first number of DDR memory devices* [e.g., four x16 memory devices] *arranged in a first number of ranks* [e.g., four ranks]." For example, Perego describes "grouping memory devices into multiple independent target subsets (i.e. more independent banks)," EX1035,15:37-45, which a POSITA would have understood corresponds to a "*first number of ranks*" as construed, *supra* §IV.D.1,pp.11-14;EX1003,¶¶73-77,118.

A POSITA would have understood from Perego's disclosure that, in the context of DDR SDRAM devices, the "[o]ne or more memory devices" which respond to control and address information by transmitting data during a memory operation (e.g., read command) correspond to one "rank." *See supra* §IV.D.1,pp.11-14;EX1035,6:15-24,14:63-65;EX1003,¶¶119-120. A POSITA

would have understood that such command signals include chip select signals to select the rank for the memory operation. EX1029,p.6;EX1003,¶120.

Perego teaches that the width of the data transaction for a read or write command can be equal to the full width of the memory module, as required for a "*rank*" of memory devices. EX1035,14:16-31;EX1003,¶121. Thus, a POSITA would have understood that the number of subsets of memory devices, each subset having "[o]ne or more memory devices" participating in a data transaction, corresponds to the claimed "*first number of ranks*." EX1003,¶121.

To the extent one might argue that Perego does not adequately disclose the claimed ranks, they would have been obvious in light of Amidi, which teaches that DDR memory devices can be organized in multiple ranks on a memory module, with each rank having the same data width as the module and being capable of being selected to participate in a data transaction by a respective chip-select signal. EX1036,*e.g.*,[0003-04],[0034-35]&Fig.3. A POSITA would have understood organizing DDR memory devices into multiple ranks to be a well-known reliable technique for selecting memory devices that participate in a data read or write transaction, and that the chip-select signal was designed to select ranks, motivating a POSITA to organize the DDR memory devices in Perego's module into multiple ranks as taught by Amidi. EX1029,6;EX1032,4.20.4-10 to -16;EX1003,¶122. Furthermore, Perego and Amidi are analogous art, *supra*,§VI.A.1,pp.23-

25;EX1003,¶¶96-106,123, and such a combination would have been well within her level of skill at the time, since she would have been familiar with JEDEC standards specifically designed to organize DDR memory devices into ranks on a memory module, *supra*,§IV.B,p.5;EX1003,¶¶50-52,123.

With respect to the "*number*" of memory devices and ranks, Perego teaches an embodiment in which its module includes four memory devices arranged in four ranks, each rank having a single memory device with a "dedicated channel," as shown in Figure 4B below (modified to show the known JEDEC signals for DDR2 memory devices). EX1035,10:17-20,6:15-24("***one*** or more")&FIG.4B;*see also*,EX1029,6;EX1035,9:58-60,14:4-10,10:56-67,10:5-13;EX1003,¶124. Here, in each of channels 415a-d, the Buffer 405 interfaces with the respective memory device using the control (RQ), data (DQ), data strobe (DQS), and clock (CK) signals according to the JEDEC standards. EX1003,¶124.

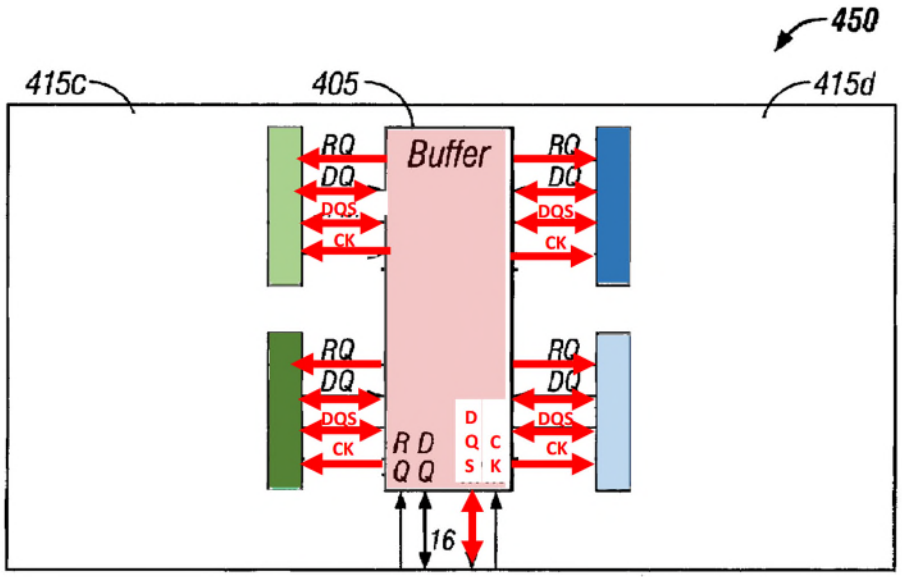


FIG. 4B

In this embodiment of Perego, also shown below in modified Figure 7 (showing four such modules), the "*first number of DDR memory devices*" is four, with each memory device having a width of 16 bits (W_A=16), like the width of the memory module (W_{DP}=16), resulting in four ranks ("*first number of ranks*"), each with a 16-bit width. *See*,EX1035,*e.g.*,14:12-15,14:16-40,FIGS.5B,7(modified below);EX1035,20:65-21:3;EX1003,¶125.

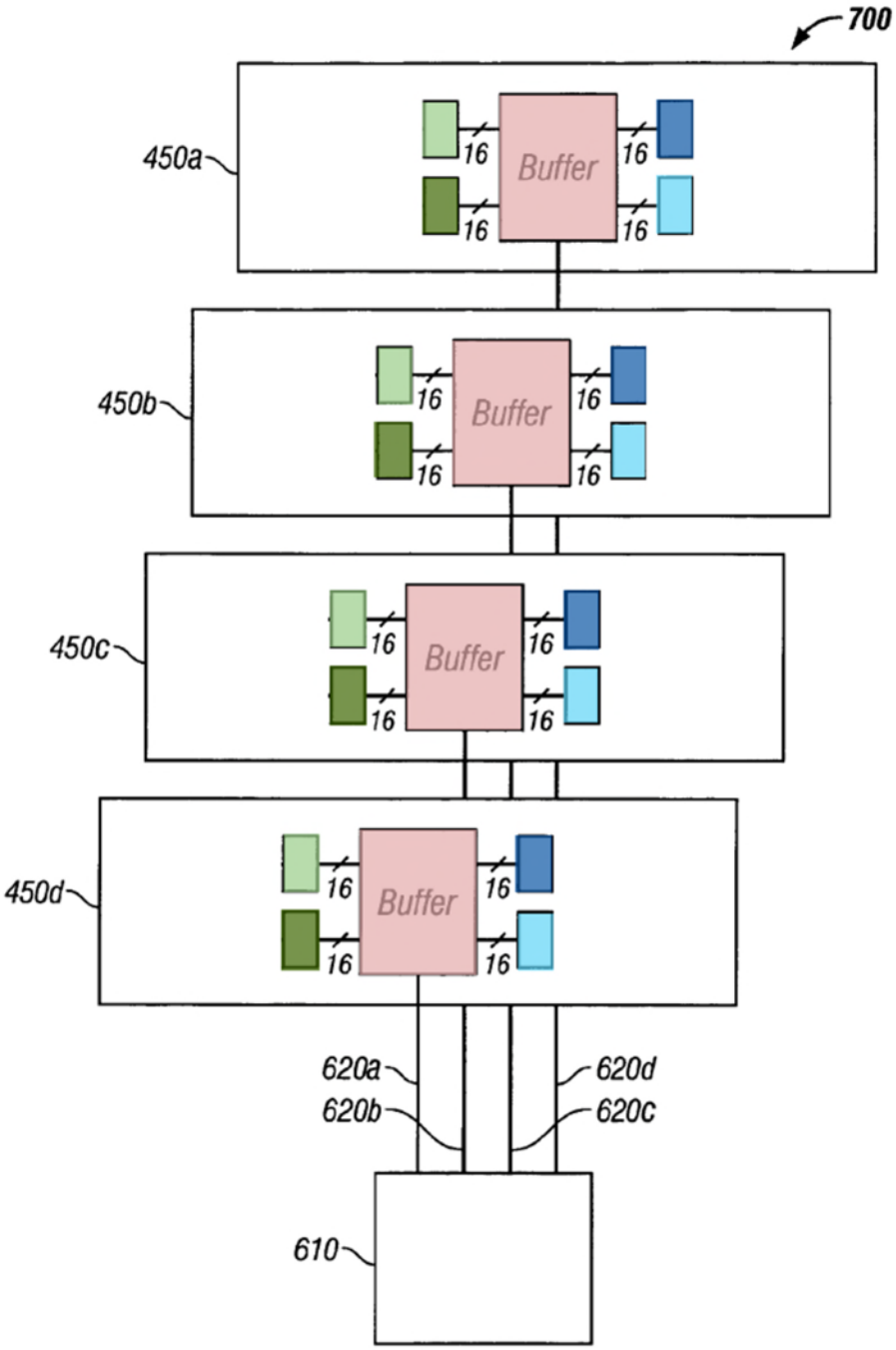


FIG. 7

e) [16.c]: *Circuit Comprising Logic Element and Register*

Perego discloses "*a circuit* [e.g., buffer device 405] *coupled to the printed circuit board, the circuit comprising a logic element* [e.g., 540 in Fig.5B] *and a register* [e.g., 597f-m in Fig.5C]." EX1003,¶¶127-131.

Perego's buffer device (e.g., 405) is a "*circuit*" and, as explained above, is coupled to the PCB. *Supra*,§§VI.A.2.b)-c),pp.26-27;EX1003,¶¶111-112,116;EX1035,5:56-67. The buffer device comprises a "*logic element*," including request & address logic 540, that translates a protocol employed by the system memory controller to one that is used by the memory device. EX1035,10:59-68;*see also*,FIG.4B(*supra* p.31, illustrating signals to memory device),9:58-60,FIG.5B(annotated below, illustrating that logic 540 provides the control and address lines (RQ) to the memory interfaces 520a and 520b based on signals received from configurable interface 590),13:54-59;EX1003,¶128.

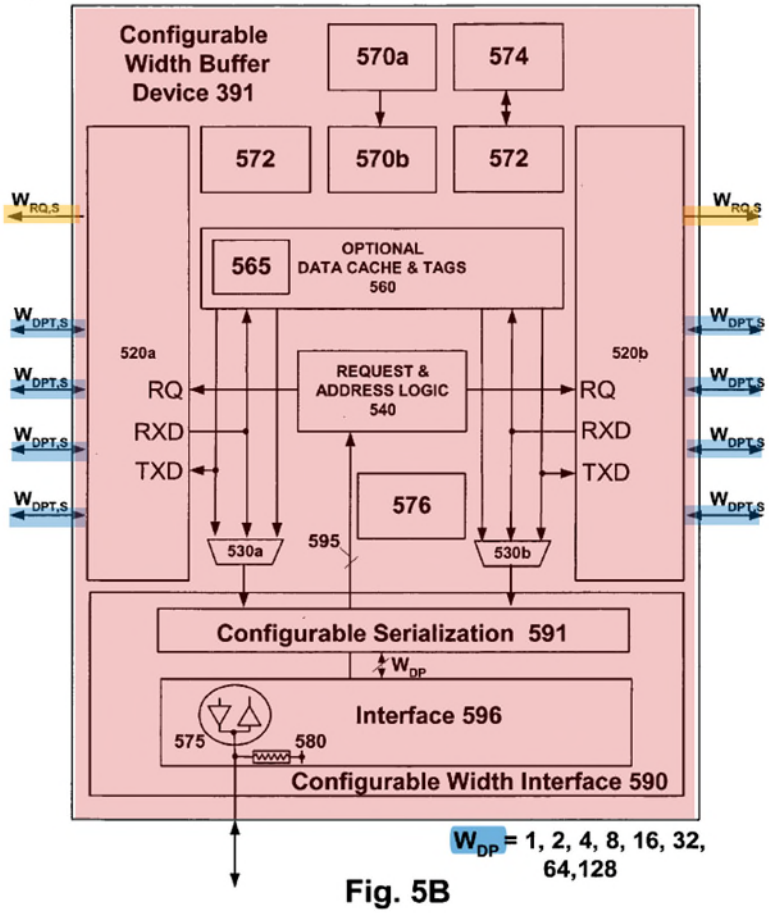


Fig. 5B

Perego teaches that its buffer device includes a "*register*" which "tranceives and provides isolation" of address, command, and data signals between the memory controller and the memory devices on the module, and that interface 596 within the buffer device decodes control and address information. EX1035,6:12-27,13:54-59. This disclosure would have informed a POSITA that Perego's interface 596 includes registers (e.g., 597f-m in Fig.5C) that latch the received address, command, and data signals to provide "isolation" and for decoding of the

control and address information, *see,e.g.,id.*,FIG.5C,17:61-63, similar to the standard registered modules of the time, EX1032,4.20.4-10 to -16;EX1003,¶129.

To the extent one might argue Perego does not adequately disclose the claimed "*register*," it would have been obvious in light of Amidi (e.g., register 408 in Fig.4A). EX1003,¶130. Like Perego's module that includes a buffer that isolates the memory devices from the control and address signals received from the system memory bus, Amidi describes using a register that performs this functionality. EX1036,[0038];EX1035,*e.g.*,6:12-27. A POSITA would have been motivated to use the functionality of Amidi's register in Perego to synchronize the incoming address and control signals with the local clock signal, and provide load isolation, thus improving performance. *Supra*,§VI.A.1,pp.23-25;EX1003,¶¶96-106,130. Since this technology was already standardized, EX1032,4.20.4-10 to -16 (showing register in bottom-left), the result of the combination would be as expected, a registered memory module.

f) [16.c.i]: *Set of Input Signals*

Perego discloses "*the logic element* [e.g., 540] *receiving a set of input signals* [e.g., signals associated with a read or write command per the JEDEC standard, EX1029,6,49] *from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at*

least one chip-select signal [per the JEDEC standard, EX1029,6,49&n.2 (A0-A15[2],BA0-BA2,CS)]." EX1003,¶¶132-135.

Perego explains that "control information and address information may be decoded" by logic 540. EX1035,13:54-59,FIGS.5B,4B(*supra* p.31);EX1003,¶133.

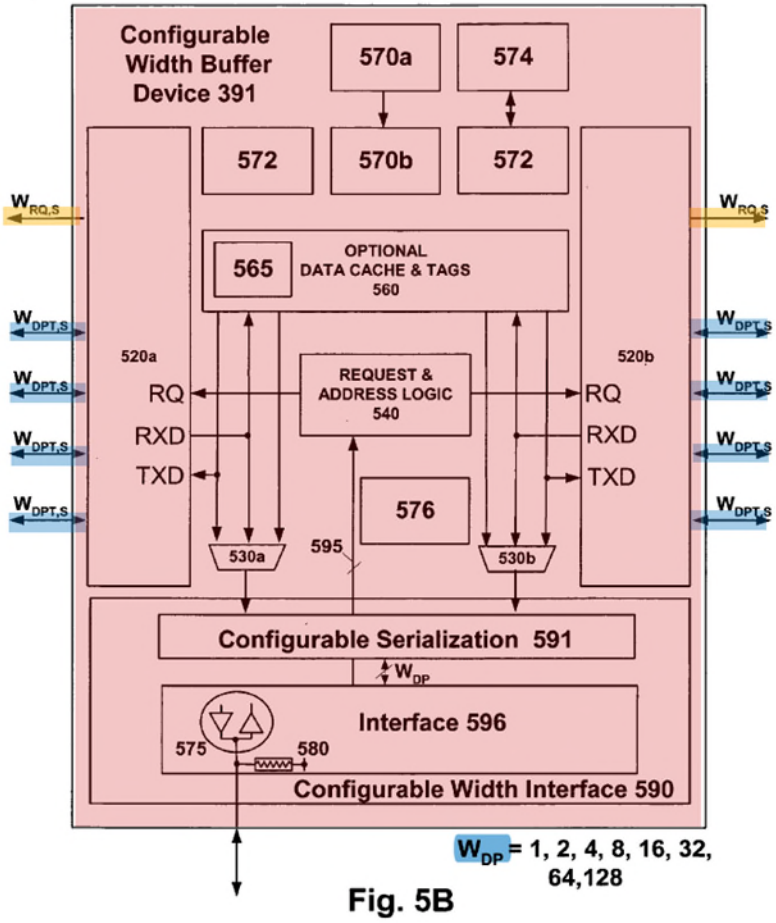


Fig. 5B

[2] A10 is used for a command signal, rather than an address signal, for certain commands, such as Precharge, Write, and Read. EX1029,6,7-8,33-34,37,49.

A POSITA would have understood that, for DDR memory devices, the "address lines" (and "address information") labeled RQ in Perego, EX1035,9:58-60,6:15-19, convey both row/column, and bank, addresses, per the JEDEC standard, EX1029,6,49;EX1035,10:56-59,3:67-4:3,8:1-9;EX1036,[0030-31], FIG.2;EX1003,¶134. The JEDEC standard is annotated below. EX1029,6; *see also id.* at 49 (showing use of the signals below for Bank Activate, Read, and Write commands);EX1032,4.20.4-6.

1.2 Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, and DM signal for x4x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (UDM), (LDM)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/$\overline{RDQS}$ is enabled by EMRS command.
BA0 - BA2	Input	**Bank Address Inputs:** BA0 and BA1 for 256 and 512Mb, BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A15	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands.
DQ	Input/Output	**Data Input/ Output:** Bi-directional data bus.
DQS, ($\overline{DQS}$) (UDQS), ($\overline{UDQS}$) (LDQS), ($\overline{LDQS}$) (RDQS), ($\overline{RDQS}$)	Input/Output	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15. For the x8, an RDQS option using DM pin can be enabled via the EMRS(1) to simplify read timing. The data strobes DQS, LDQS, UDQS, and RDQS may be used in single ended mode or paired with optional complementary signals $\overline{DQS}$, $\overline{LDQS}$, $\overline{UDQS}$, and $\overline{RDQS}$ to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables all complementary data strobe signals.

Moreover, as more fully explained below with reference to claim elements [16.c.ii] and [16.c.iii], a POSITA would have understood the logic element to need "*at least one row/column address signal, bank address signals, and at least one chip-select signal*" in order "to translate protocols" so the module can use DDR memory devices different than those the memory controller expected. EX1035,10:63-68;EX1003,¶¶135,137-168.

g) [16.c.ii]: *Second Number of Ranks*

Perego discloses "*the set of input signals configured to control a second number of DDR memory devices* [e.g., two x8 memory devices] *arranged in a second number of ranks* [e.g., one rank], *the second number of DDR memory devices* [e.g., two x8 memory devices] *smaller than the first number of DDR memory devices* [e.g., four x16 memory devices] *and the second number of ranks* [e.g., one rank] *less than the first number of ranks* [e.g., four ranks]." EX1003,¶¶137-164.

JEDEC had standardized memory devices of different bit-widths, e.g., "x4" (4-bit-wide), "x8" (8-bit-wide), and "x16" (16-bit-wide). EX1030,4-6;EX1034,1-2,20;EX1029,7.

Perego teaches that different types of memory devices — e.g., x4, x8, x16 — may be included on different modules by using the buffer device 405 (with a

configurable width) to translate the input signals. EX1035,10:63-67,14:12-15,3:25-28;EX1003,¶138.

A POSITA would have understood that Perego's module could use x16 memory devices to upgrade a memory system configured for memory modules having x8 memory devices (as was common, *see,e.g.*,EX1032,4.20.4-13,-25 to -26), and that some memory systems only had control for one or two ranks per module, *see,e.g.*,EX1036,[0004]. Thus, a POSITA would have understood Perego's translation protocol to allow use of a memory module with x16 memory devices in a system configured to control memory modules with one rank of memory devices (e.g., two x8 memory devices). EX1035,10:14-17. Perego also discloses that this module can be 16 bits wide (W_{DP} =16). EX1035,FIGS.4B("/16"),7("/16"),5B(W_{DP} =16);EX1003,¶139.

A POSITA would also have also understood the then-current trend to increase the data width of the memory devices, as evidenced by writings of the day, motivating a POSITA to increase the capacity of a memory module, e.g., by using four ranks of low density (inexpensive) x16 memory devices in place of one rank of high-capacity (expensive) x8 memory devices. *See,e.g.*,EX1034,20; EX1036,[0008];EX1035,3:23-25;EX1003,¶140. Given the finite number of different memory device bit-widths at the time and the expense of high-density

devices, this specific combination would have been obvious to try. *See,e.g.*,EX1036,[0004-05],[0008];EX1035,3:23-25;EX1003,¶141.

In particular, a POSITA would have understood from the JEDEC tables below that a 16-bit-wide one-rank memory module with a total capacity of 1Gb can be formed with ***two*** 64Mbx8 (8-bit-wide) DDR2 memory devices (blue below) in that rank. EX1029,p.7(Tables 2 and 3, annotated below);EX1003,¶142; *see also* EX1032,4.20.4-11,-29 (showing how x8 memory devices can be combined in a rank to create the bit-width for the module).

Table 2 — 512Mb Addressing

Configuration	128Mb x4	64Mb x 8	32Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 3 — 1Gb Addressing

Configuration	256Mb x4	128Mb x 8	64Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

In such a one-rank 1Gb module, 14 row address bits (A_0-A_{13}), 10 column address bits (A_0-A_9), and two bank address bits (BA0, BA1) are required to access a specific memory location. *Id*. (blue). To double the capacity of this one-rank module to 2Gb, the two 64Mbx8 DDR2 memory devices (blue) could be replaced

by two 128Mbx8 DDR2 memory devices (red), requiring three bank address bits (BA0-BA2) instead of two, while using the same number of row and column address bits. *Id.* At the time, however, a POSITA would have also understood that using two x8 memory devices each with 1Gb capacity may not be feasible, because those memory devices may be expensive or unavailable. EX1036,[0008];EX1003,¶142.

Thus, a POSITA would have understood that, following the trend at the time of Perego's disclosure, another option to double the capacity of the one-rank module to 2Gb would be to use wider lower-density memory devices, such as four 16-bit wide 32Mbx16 memory devices (green, above), e.g., consistent with Amidi's teaching to use "lower densit[y] devices" that are "cheaper." EX1036,[0008],[0004-0005];EX1029,7(Tables 2 and 3 annotated above);EX1003,¶143.

A POSITA would have also understood that, to behave like one 16-bit wide rank, Perego's module can advantageously use four x16 memory devices (32Mb x16, green) instead of four x8 memory devices (64MB x8, blue), because x16 devices would improve power consumption and performance. EX1035,15:40-45; EX1036,[0046-48];EX1029,p.7(above in part);EX1003,¶¶144-146. Using memory devices with smaller capacities would also save money. EX1036,[0008];EX1001,4:59-5:5;EX1003,¶145.

That is just one example. A second example, motivated by Amidi's teaching to use "lower densit[y] devices" that are "cheaper," EX1036,[0008],[0046-48] — and similar to "Example 2" in the 912 Patent, EX1001,cols.18-19, to the extent it embodies claim 16 — would be to use four lower-density x16 memory devices ("*first number of memory devices*") arranged in four ranks ("*first number of ranks*") communicating with the system controller like a module with two higher-density x16 memory devices ("*second number of memory devices*") arranged in two ranks ("*second number of ranks*"). EX1036,[0018],[0046-48]; *see also supra* §VI.A.1,pp.23-25. As shown below, in this example where each rank has one x16 memory device, the combination of Perego and Amidi can use the two x16 memory devices on the left (light and dark green) to selectively respond to input signals directed to one (virtual) higher-capacity memory device, and the two x16 memory devices on the right (light and dark blue) to selectively respond to input signals directed to another (virtual) higher-capacity device. EX1003,¶147.

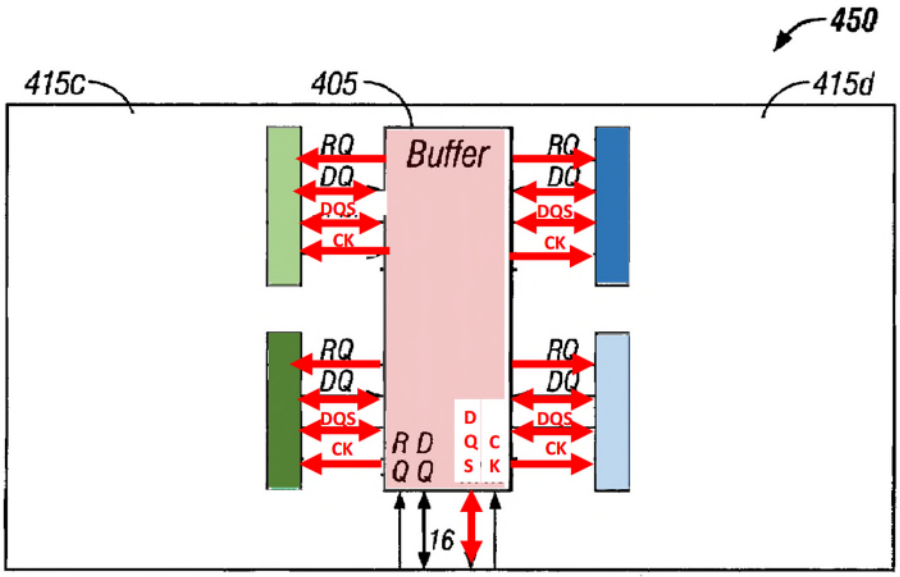


FIG. 4B

In this second example, a POSITA would have been motivated to build Perego's 16-bit wide module with four x16 memory devices for a system where the memory controller can control only two ranks per module, as in Amidi, and would have understood, as shown below, that the module could use the extra row address bit A13(orange) received for a (virtual) 128Mbx16 memory device (red) to select between two 64Mbx16 memory devices (blue) as the target of a read or write command. EX1036,[0049];EX1029,p.7(annotated below);EX1003,¶148.

Table 3 — 1Gb Addressing

Configuration	256Mb x4	128Mb x 8	64Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 4 — 2Gb Addressing

Configuration	512Mb x4	256Mb x 8	128Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A14	A0 ~ A14	A0 ~ A13
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

The following discussion returns back to the first example above (green 512Mb vs. red 1Gb), but the same principles apply equally to other examples, including the second example above (blue 1Gb vs. red 2Gb). EX1003,¶149.

Implementing a four-rank 2Gb module with one x16 memory device in each rank (green, below) that looks to the system memory controller like a one-rank 2Gb module with two x8 memory devices (red, below) was well within a POSITA's level of skill at the time. EX1003,¶150. Under the JEDEC standard below, the only difference between the row/column and bank address bits is the green box requires one less row address bit (A_{13}) and one less bank address bit (BA2) than the red box. EX1029,7 (annotated below);EX1003,¶150.

Table 2 — 512Mb Addressing

Configuration	128Mb x4	64Mb x 8	32Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 3 — 1Gb Addressing

Configuration	256Mb x4	128Mb x 8	64Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

A POSITA would have understood that the extra address bits — here, row address bit A_{13} and bank address bit BA2 — can be used to "determine which target subset of channels 370 will be utilized for the data transfer portion of the transaction." EX1035,14:62-65;EX1003,¶150. For example, to perform a read or write operation, the JEDEC standard (shown below) first requires a Bank Activate command with the row and bank address signals, followed by a read or write command with the corresponding bank address signals (but not the row address). EX1029,49&n.2 (reproduced below in part);EX1003,¶150.

Table 10 — Command truth table.

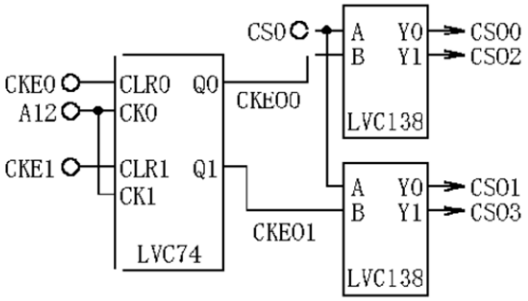
Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									

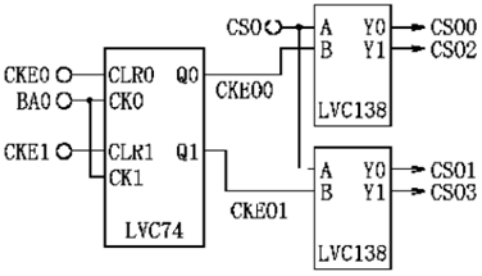
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.
NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

Thus, a POSITA would have understood that the target memory device and its target memory bank is selected in accordance with the bank address signals of the read or write command and the previously received row address and bank address signals of the activate command. *Id*.

Furthermore, a POSITA would have understood how to identify and use the differences in the address spaces of the physical and emulated devices to generate additional chip select signals for the additional ranks of the module through use of Perego's request & address logic 540. *See,e.g.*,EX1036,[0047-49,55-57]; EX1042,[0010]&FIG.1(reproduced in part below, left, showing the generation of additional chip select signals based on A12),[0020]&FIG.4(reproduced below, right, illustrating the same based on BA0);EX1003,¶¶151,157.





To the extent one might argue that Perego alone does not sufficiently disclose or render obvious this limitation, it would have been obvious in light of Amidi. Combining Perego with Amidi would have been obvious to a POSITA for reasons explained generally above, §VI.A.1,pp.23-25, and specifically for this limitation as explained below. EX1003,¶152.

Amidi teaches an emulator which controls ***four*** ranks based on signals from a memory controller for ***two*** ranks (e.g., only two chip-select signals). EX1036,[0011-12],FIG.6A. It would have been obvious to a POSITA to include the functionality of this emulator as taught by Amidi in an implementation of the protocol translation in Perego's module since both disclosures have transparent memory modules and this combination would reduce the cost of a high-capacity module compared to the same high-capacity module implemented with higher-capacity memory devices. EX1035,10:59-67;EX1036,Abstract; EX1003,¶¶153-154. Moreover, both Perego and Amidi teach using the address signals to select the target rank. EX1035,15:31-45;EX1036,[0043-44]&FIG.5. EX1003,¶155. Additionally, a POSITA would have been motivated to double the width of the memory devices on the module from x8 to x16 since it "requires very little engineering know-how," EX1034,20, and as discussed above would save power and increase performance, EX1003,¶¶144,155.

To the extent one might argue Amidi does not disclose that the "*logic element*" receives the claimed "*bank address signals*" as part of the "*set of input signals*," Perego, alone or in combination with Amidi, teaches this when Perego explains that request & address logic 540 (part of the "*logic element*") receives control and address information, which a POSITA would have understood includes bank address signals under the JEDEC standard for DDR memory devices. *See,e.g.*,EX1035,13:54-59;EX1029,6,49&n.2;EX1003,¶156.

In addition, a POSITA would have understood that both row address and bank address signals can be used to generate additional chip-select signals. *See, e.g.*, EX1042,[0010]&FIG.1(showing the generation of additional chip select signals based on A12),[0020]&FIG.4(illustrating the same based on BA0);EX1003,¶¶151,157. For example, Amidi teaches a POSITA that the row address is received before the read/write command (which includes a bank address and column address), consistent with the JEDEC standard. EX1036,[0061],FIG.6A;EX1030,1,5,13("Accesses begin with the registration of an ACTIVE command [with bank and row addresses], which is then followed by a READ or WRITE command [with bank and column addresses].");EX1029,49&n.2;EX1003,¶158. This was well known, as shown below. EX1034,4&FIG.5(below);EX1003,¶158.

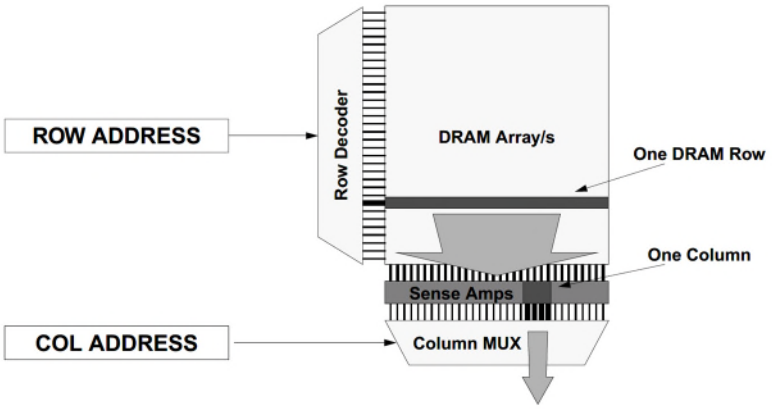


Figure 5: The Multi-Phase DRAM-Access Protocol
The row access drives a DRAM row into the sense amps. The column address drives a subset of the DRAM row onto the bus (e.g., 4 bits).

Given the two-step process above (first row address, second read/write command with column address), a POSITA would have understood Amidi would use the bank address signals to store and retrieve the row address bits for the later read or write command because, ***first***, under the JEDEC standard below, row addresses are received with an earlier Bank Activate command (and the later Read or Write command does not include the row address) so the row address must be stored and retrieved using the bank address signals, EX1030,1,5,13;EX1029,49&n.2;EX1044 (Dell),8:36-40, and ***second***, Amidi shows that its CPLD uses that stored row address bit (along with the chip-select signals) as an input to select the target rank of a read or write operation, EX1036,[0043],[0047-49],[0052],FIGS.3,5,8(add(n) input to blocks 812 and 814);EX1003,¶¶159,161.

Table 10 — Command truth table.

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.
NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

EX1029,49&n.2.

Indeed, during reexamination, the Board found that, based on Amidi's disclosure, it would have been obvious to a POSITA to store a row address for a subsequent read or write operation that operates on the columns of that row. EX1011,56-58,62(citing EX1044,8:36-40). EX1003,¶160.

Additionally, a POSITA would have known that, under the JEDEC standard, the bank address signals (BA) determine which internal bank of the target memory device(s) would perform the read or write operation. EX1036,FIG.6A("BA[1:0]"); EX1029,49&n.2(reproduced above in part). Thus, she would have understood — and been motivated — to use the bank address (BA) signals in Amidi to store and retrieve the row address bit (add(n)) for a specific bank, to keep track of which row address bit corresponds to which bank when the read or write command arrives. EX1003,¶162. Furthermore, she would have understood and found it obvious that in Amidi, the bank address signals are received by the logic performing row-

address-based rank multiplication to store and retrieve the right row address bit for the right bank. EX1003,¶163.

As explained by Dr. Wolfe, a POSITA would further have understood that other combinations of memory devices were also possible based, e.g., on the number of channels of Perego's buffer device. EX1003,¶164;EX1035,10:26-30,11:52-55. For example, in a memory module where the interfaces 520a and 520b have a total of eight channels, with each channel coupled to one x16 DDR memory device, and using the same rank multiplication based on row and bank address signals as discussed in the first example above, the "*first number of DDR memory devices*" would be eight x16 memory devices, and the "*first number of ranks*" would be eight ranks, emulating a module with two ranks ("*second number of ranks*"), each having two x8 memory devices, providing a total of four x8 emulated memory devices ("*second number of memory devices*"). *Id.*

h) [16.c.iii]: *Output Signals*

Perego teaches "*the circuit* [e.g., buffer device 405] *generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks*." EX1003,¶¶166-168.

Perego explains that "[i]n a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-

point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360..." EX1035,6:15-19. Perego further teaches that different types of memory devices may be used by utilizing the buffer to "translate protocols." *Id.*,10:63-67. A POSITA would have understood from Perego's disclosure that, when Perego's buffer circuit "translate[s] protocols" for the exemplary implementation of four ranks with one x16 memory device in each rank, it generates output signals according to the protocol of those x16 memory devices, in response to receiving a read command for x8 memory devices, as explained above for claim elements [16.b.i], *supra* §VI.A.2.d),pp.28-32, and [16.c.ii], *supra* §VI.A.2.g),pp.38-51. *See also* EX1035,FIG.4B(modified below, showing the implementation discussed above);EX1003,¶167.

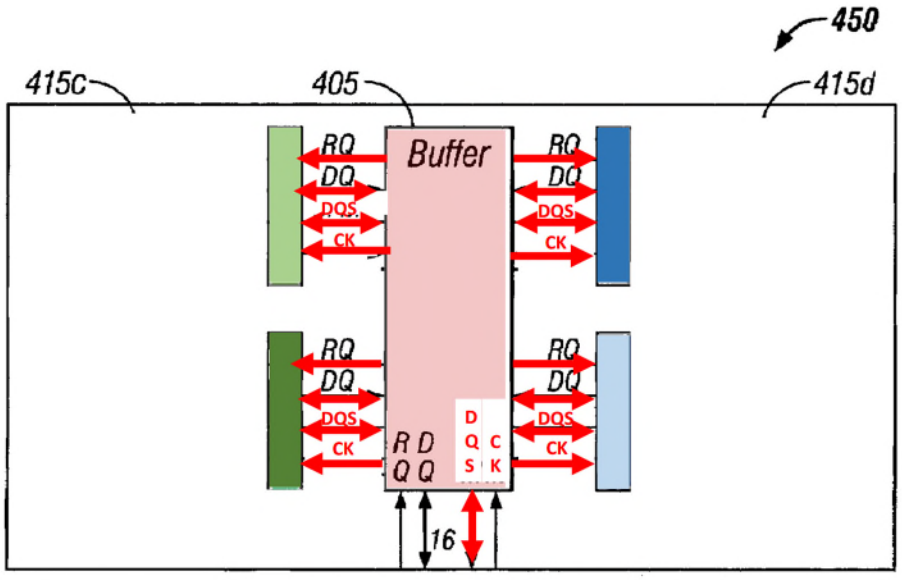


FIG. 4B

i) ***[16.c.iv]:*** *Selecting one or two ranks…and transmitting the command signal*

Perego teaches "*wherein the circuit* [e.g., buffer device 405] *further responds to a command signal* [e.g., for a read or write command per the JEDEC standard, EX1029,6,49] *and the set of input signals from the computer system by selecting one or two ranks* [e.g., one rank] *of the first number of ranks* [e.g., four ranks] *and transmitting the command signal to at least one DDR memory device of the selected one or two ranks* [e.g., one rank] *of the first number of ranks* [e.g., four ranks]." EX1003,¶¶169-172.

Perego discloses selecting "one" memory device and transmitting the corresponding signals to the selected memory device, as explained above for [16.c.iii], *supra* §VI.A.2.h),p.52;EX1003,¶¶166-168;EX1035,6:15-19. Moreover, a POSITA would have understood that such a x16 memory device can form one rank, as it can provide the same data width as the width of the memory module, as explained above for [16.b.i], *supra* §VI.A.2.d),pp.28-32; *see also* EX1035,FIG.4B(modified below, showing the implementation discussed above);EX1003,¶170.

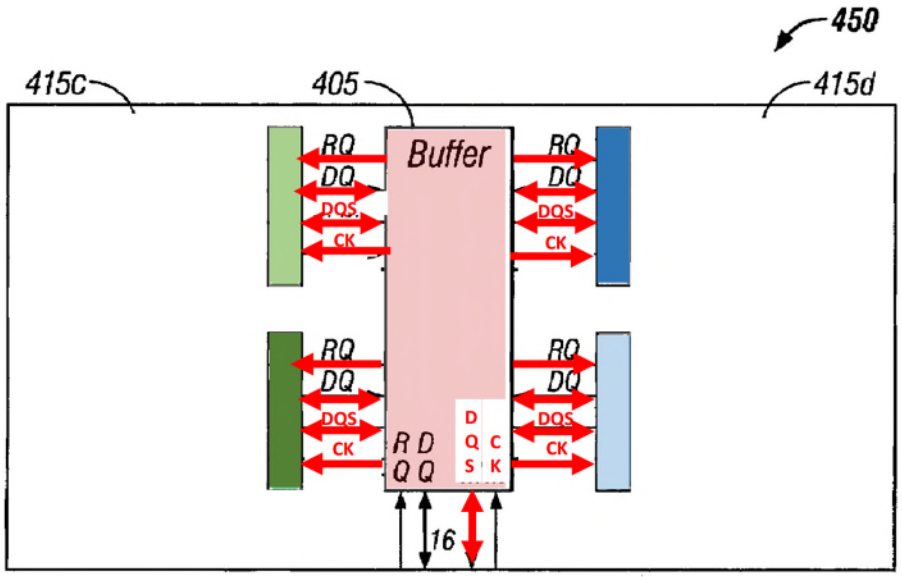


FIG. 4B

A POSITA would have understood Perego's disclosure that "the target subset of secondary channel signal lines may be selected via address bits provided as part of the primary channel request" teaches that the address information received from the memory controller can be used to select the target rank for the memory transaction, providing several benefits, including more independent ranks and thus potential capacity. EX1035,15:31-45;EX1003,¶171.

Moreover, as previously explained, a POSITA would have been motivated to use the rank multiplication functionality of Amidi in the memory module of Perego. *Supra*,§VI.A.1,pp.23-25;EX1003,¶¶96-106;EX1036,[0043-44],FIG.5. As previously discussed for [16.c.ii],§VI.A.2.g),pp.38-51,EX1003,¶¶137-165(especially ¶142), the specific combination of using x16 memory devices on the module despite the system sending address and control information for x8

memory devices requires selection of one of the ranks according to row and bank address bits of the commands received from the memory system controller (which include chip-select signals). Thus, Perego alone and in view of Amidi teaches a POSITA that the selection of the target rank is done in response to a command signal and in response to "*the set of input signals*" that includes "*at least one row/column address signal, bank address signals, and at least one chip-select signal*." EX1003,¶172.

Dr. Wolfe explains that "the '912 Patent itself does not expressly describe selecting the target rank based on both a row/column address and a bank address, meaning that Perego alone and in view of Amidi actually provides a better disclosure of the claimed invention than the '912 Patent itself." EX1003,¶173. The 912 Patent illustrates, in its EXAMPLE 1 code, "memory density multiplication" based on a bank address BA_2, without any row/column address, while the EXAMPLE 2 code provides "[a]nother exemplary section of Verilog code compatible with memory density multiplication" based on a row address bit A_{13} (where the bank address signals are only used to selectively store A_{13}). EX1001,14:17-23,17:28-31,cols.18-19;EX1003,¶173. As previously discussed, a POSITA would have understood, e.g., from Amidi's disclosure and her knowledge of the relevant JEDEC standards, that a row address density bit is stored selectively

for each internal bank of a DDR memory device. *Supra*,§VI.A.2.g),pp.48-51;EX1003,¶¶158-163;*see also*,EX1029,49&n.2;EX1003,¶173.

Thus, to the extent using the bank address signals only for storing the respective row address bit satisfies the claimed "*selecting*" (similar to EXAMPLE 2 of the 912 Patent), the "second example" of the Perego-Amidi combination renders the claim obvious even using only row-address-based selection, because such selection also uses the bank address signals for storing that row address. *Supra*,§VI.A.2.g),pp.38-51;EX1003,¶¶146-148,158-163;*see also*,EX1029,7(annotated Tables 3 and 4 below);EX1003,¶174.

Table 3 — 1Gb Addressing

Configuration	256Mb x4	128Mb x 8	64Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 4 — 2Gb Addressing

Configuration	512Mb x4	256Mb x 8	128Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A14	A0 ~ A14	A0 ~ A13
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Amidi explains that, using a row address bit (A_{13}) can allow two smaller capacity 64Mbx16 devices to emulate one 128Mbx16 device. EX1036,[0047-49]. Thus, for

the reasons previously discussed, a POSITA would have been motivated to implement the Perego-Amidi combination so that four ranks, each having one 64Mbx16 device, emulate two ranks with one 128Mbx16 device in each rank as seen by the system memory controller. *Supra*,§VI.A.2.g),pp.42-44 ("second example"). In this "second example" of the combination, shown below, the system memory controller would see only two ranks. EX1003,¶174.

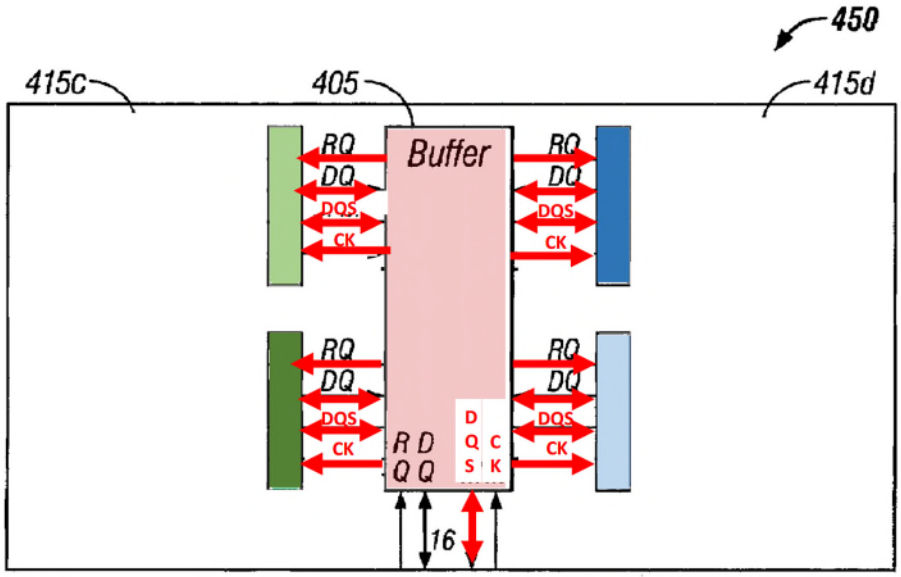


FIG. 4B

j) [16.d]: *Phase-Lock Loop Device*

Perego discloses "*a phase-lock loop device* [e.g., clock circuit 570a-b] *coupled to the printed circuit board*." EX1003,¶¶176-179.

For example, Perego describes buffer device 405 including a "clock circuit 570a–b [which] includes one or more clock alignment circuits for phase or delay adjusting internal clock signals with respect to an external clock (not shown).

Clock alignment circuit may utilize [an external or internal clock] to generate internal synchronizing clock signals having a predetermined temporal relationship." EX1035,12:65-13:5. Perego also explains that the function of "a phase lock loop (PLL) generator device [is] to generate phase aligned clock signals for each memory device disposed on the module." *Id*.,12:61-64. Thus, a POSITA at the time of Perego's disclosure would have understood that Perego's clock circuit 570a-b is a "*phase-lock loop device*." EX1003,¶177.

Amidi likewise discloses a phase-lock loop device, such as PLL 606, which is coupled to its printed circuit board, consistent with the JEDEC standard. EX1036,FIG.6A,[0050];*see also*,EX1032,4.20.4-29 to -35. While Amidi discloses the PLL as a separate integrated circuit, and Perego discloses a PLL internal to its buffer circuit, this distinction does not appear relevant to claim 16 in light of the 912 Patent's disclosure. EX1001,5:51-55,6:48-54;EX1003,¶178. To the extent it matters, either arrangement would have been obvious to a POSITA as evidenced by Perego's and Amidi's disclosures. EX1003,¶178.

k) ***[16.d.i]:*** *PLL Coupled to DDR Memory Devices, Logic Element, and Register*

Perego teaches that "*the phase-lock loop device* [e.g., in the buffer device 405] *[is] operatively coupled to the plurality of DDR memory devices, the logic element, and the register*." EX1003,¶¶180-183.

For example, as explained for [16.c], *supra*,§VI.A.2.e),pp.33-35, Perego teaches that the buffer device includes the "*logic element*" and the "*register*." Perego further teaches that the buffer device includes memory device interfaces 520 which "receive and transmit to *memory devices* disposed on the module..." EX1035,11:48-51,FIG.5B(annotated below);EX1003,¶181.

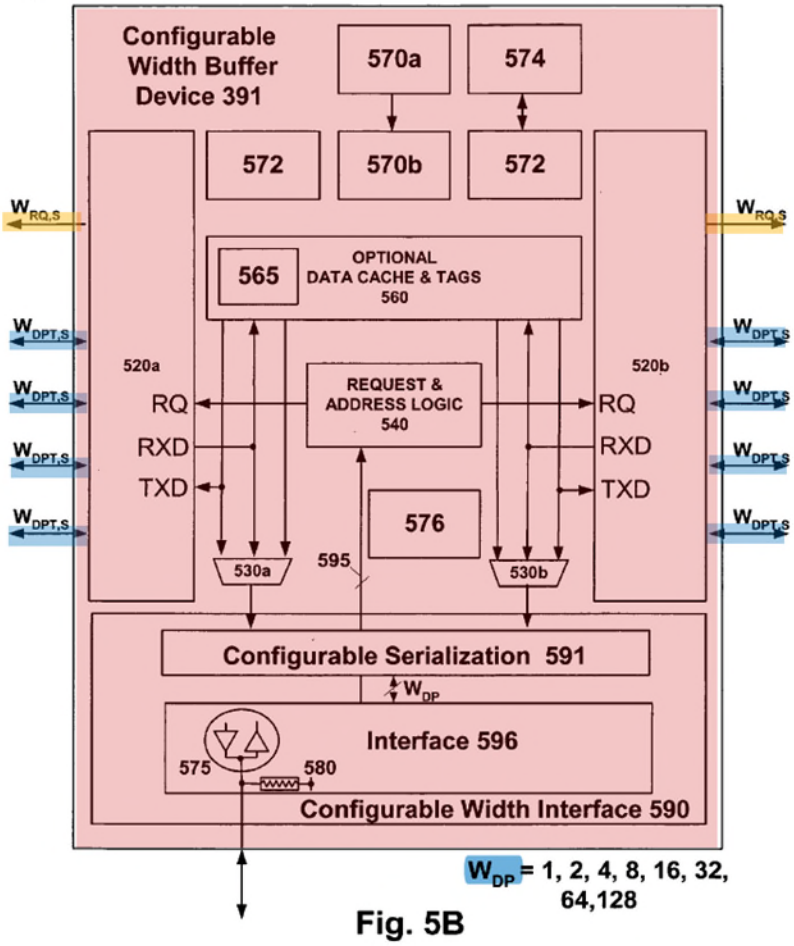


Fig. 5B

As discussed above in [16.d], *supra*,§VI.A.2.j),p.57, a POSITA would have recognized that Perego's clock circuit 570a-b includes a "*phase-lock loop device*" that provides internal clock and synchronizing signals to the circuits within the

buffer device. EX1035,12:65-13:5;EX1003,¶181. Therefore, clock circuit 570a-b ("*phase-lock loop device*") is operatively coupled to the configurable width interface 590 (including the claimed "*register*"), request & address logic 540 (in the claimed "*logic element*"), and the interfaces 520 which are themselves operatively coupled to "*the DDR memory devices*" in the implementation discussed above and shown below. *See* EX1035,FIG.4B(reproduced below with Perego's modifications for DDR memory devices);EX1003,¶182.

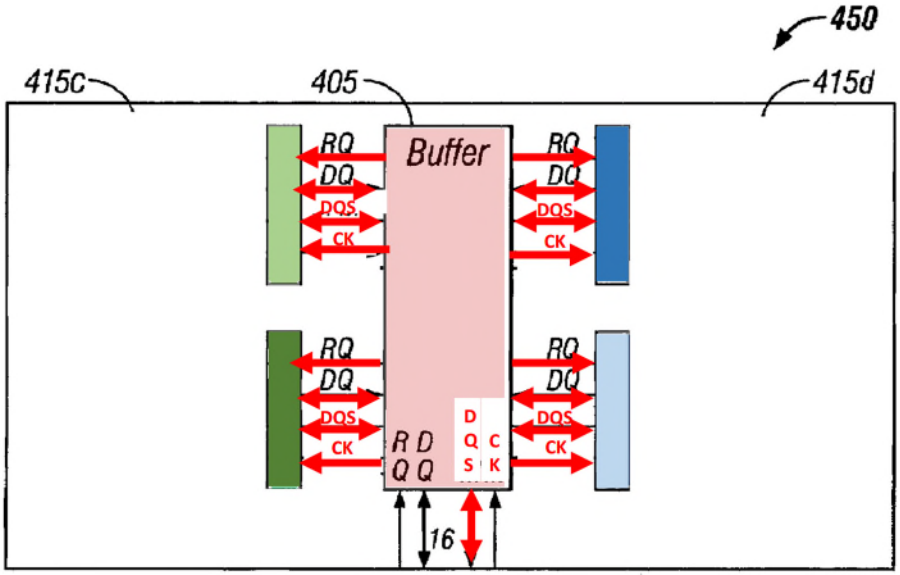


FIG. 4B

The buffer 405 provides the clock signals to the DDR x16 memory devices. A POSITA would have understood that, in a DDR module, the clock signals provided to the memory devices are generated by a "*phase-lock loop device*" (i.e., PLL) as confirmed by Amidi and the JEDEC standard. EX1036,FIG.6A;EX1032,4.20.4-17;EX1003,¶182.

In the past, Patent Owner has argued that Amidi does not disclose its PLL being coupled to the claimed "*logic element*." *See supra*,§IV.C.2,p.11;EX1003,¶64. Yet, a POSITA would have understood that a logic element that generates chip-select signals for the memory devices must be in sync with the other signals, including the clock signal, received by the memory devices from the PLL. EX1029,p.6 ("All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK."). Consequently, in Perego alone or in combination with Amidi, a POSITA would have understood, and been motivated to, operatively couple a "*logic element*," like Perego's request & address logic 540, to the clock generation circuitry 570a-b ("*PLL*") that provides clock signals for the memory devices. EX1003,¶183.

l) [16.e]: *Signal to Only One DDR at a Time.*

Perego discloses "*wherein the command signal* [e.g., for a read or write command per the JEDEC standard, EX1029,6,49] *is transmitted to only one DDR memory device at a time*," for the reasons described for claim elements [16.b.i],§VI.A.2.d),pp.28-32, and [16.c.iv],§VI.A.2.i),pp.53-57, in an implementation like the one illustrated below, where each memory device has a "dedicated channel." EX1035,10:17-21,FIG.4B(modified below);EX1003,¶¶185-187.

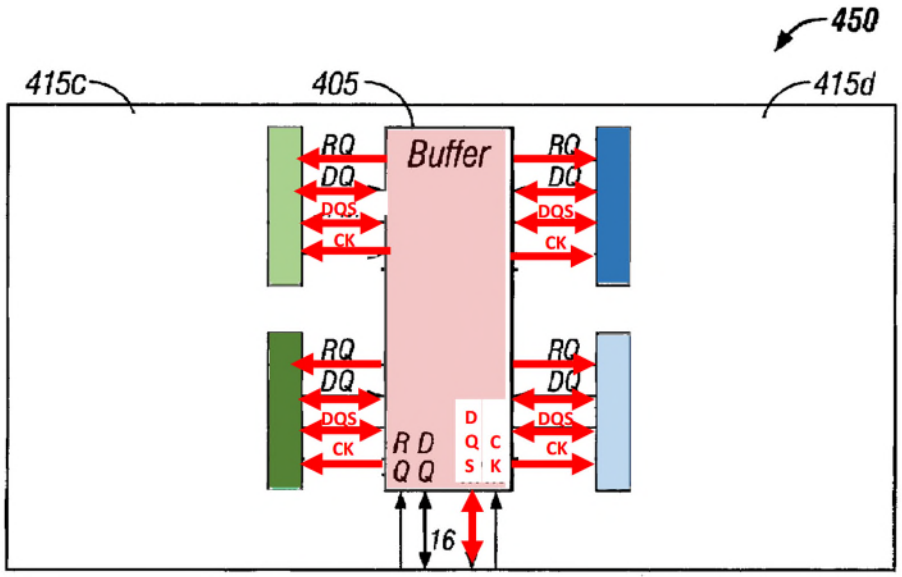


FIG. 4B

For example, Perego explains that, "[i]n a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370." EX1035,6:15-19. Thus, Perego directly teaches selecting "one" memory device and transmitting the corresponding signals to the selected memory device. Perego also discloses benefits from "multiple independent target subsets (i.e. more independent banks)" including reduced power and higher performance. EX1035,15:31-45. A POSITA would have understood from this that the command signal is not transmitted to memory devices that do not participate in the data transaction (e.g., they do not receive the read or write command), consistent with the JEDEC standard, *supra* §IV.D.1,pp.11-14;EX1029,6,49. EX1003,¶186. Consequently, when the width of

one memory device is equivalent to that of the module, the command received at a specific time is transmitted to only one DDR memory device at a time. *Id.* In the case of a read command, for example, the read command is sent to only one memory device at a time so only that one memory device provides data in response to that read command. *Id.*

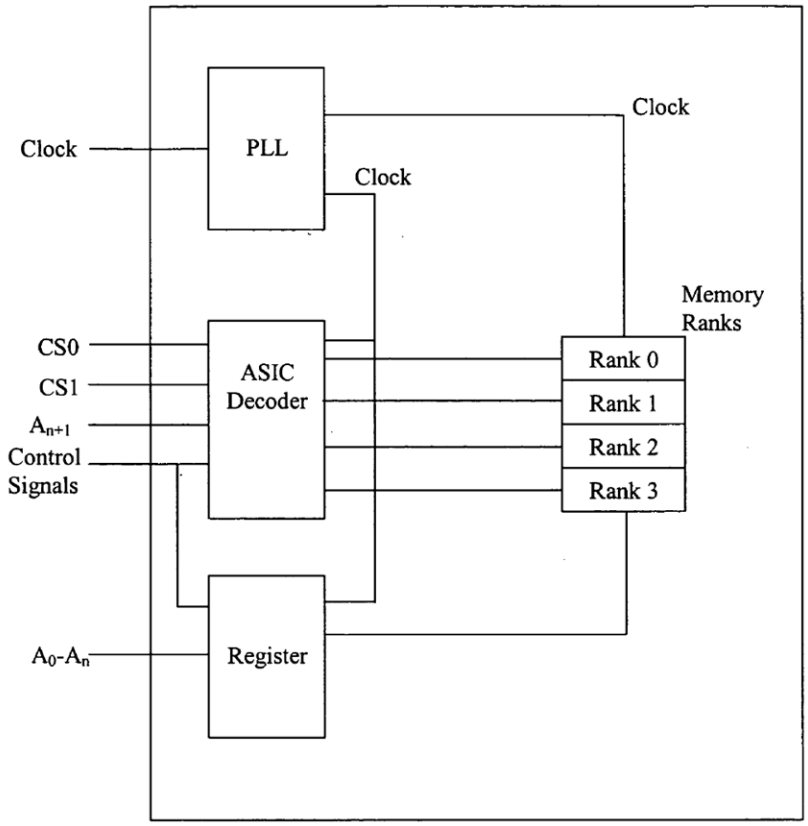
B. Ground 3: Claim 16 Is Obvious Over Ellsberry

Claim 16 is also obvious in light of Ellsberry (Ground 3).

1. Ellsberry is Prior Art to Claim 16

Ellsberry is prior art to claim 16 of the 912 Patent. A POSITA would have understood that neither the '668 provisional (filed 3/5/04) (EX1006), the '595 provisional (filed 7/15/04) (EX1007), nor the '244 provisional (filed 7/15/04) (EX1005) provide support for the full scope of claim 16 of the 912 Patent. For example, the '668 and '595 provisionals do not disclose the claimed "*logic element*" or that such a "*logic element*" receives "*at least one row/column address signal, bank address signals, and at least one chip-select signal,*" as required by claim 16. EX1003,¶189. The '244 provisional is the first priority application disclosing an ASIC Decoder, which could be a "*logic element,*" but there is no disclosure it receives any "*bank address*" signals as required by claim 16, confirming that the applicants, at that time, did not have possession of every requirement of claim 16. EX1005,10,FIG.1(below); EX1003,¶189.

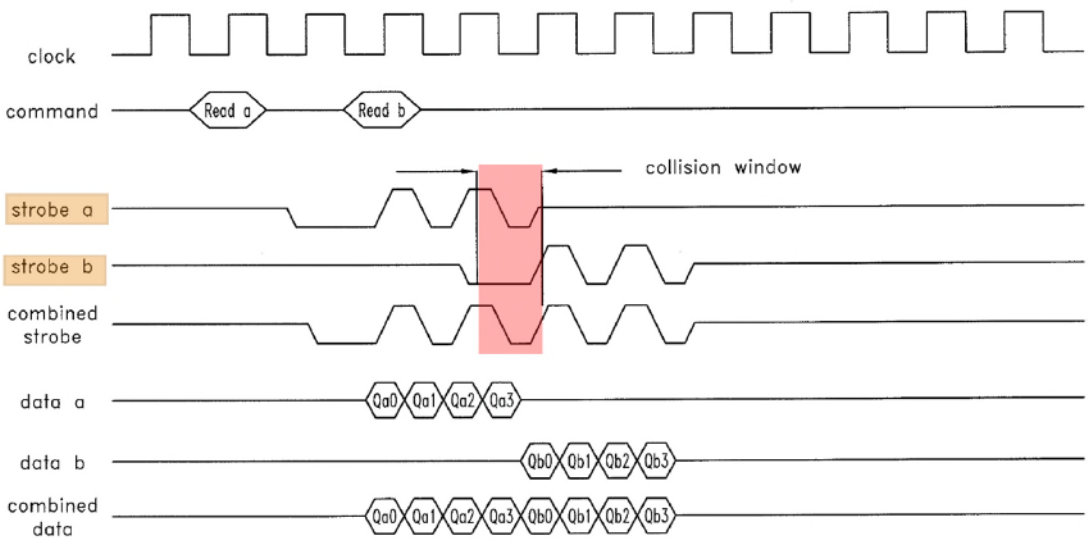
Figure 1:



A POSITA would have understood that the next priority application for the 912 Patent, the ’436 Patent (filed 3/7/05) (EX1009) — which does not reference the ’244 provisional — also fails to provide the necessary support for claim 16 of the 912 Patent, e.g., by lacking any embodiment including “*a circuit*” comprising “*a logic element*” and “*a register*” as required by claim 16 and shown in Figure 1A of the 912 Patent (40 and 60, respectively), and by lacking any Verilog code showing the use of “*row*” and/or “*bank address signals*” (like EXAMPLEs 1 and 2 in the 912 Patent). EX1003,¶190. The Verilog code was only added 7/1/05 as part of the continuation-in-part. *Id.*

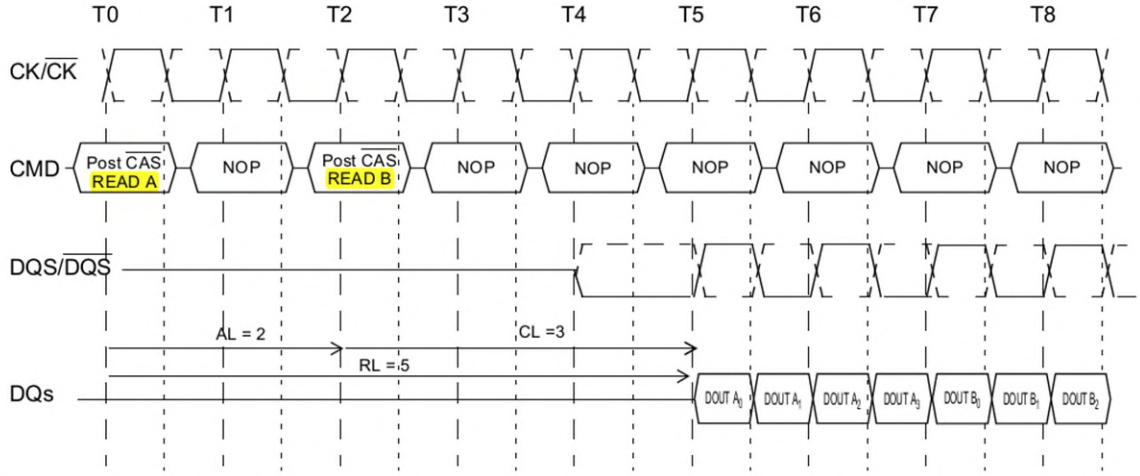
Furthermore, the subject matter added by the ’386 Patent (filed 7/1/05 as a continuation-in-part of the ’436 Patent) includes recognition of the problem of “back-to-back adjacent read commands which cross memory device boundaries” causing a “collision” window when “the last data strobe of memory device ‘a’ collides with the pre-amble time interval of the data strobe of memory device ‘b’…” EX1001,23:65-24:12&FIG.5;EX1008,24:16-30&FIG.5 (annotated below to highlight the collision, red, between strobes a and b, orange);EX1003,¶192.

FIG. 5



As shown above, a POSITA would have understood that such a “collision” would cause signal errors and potentially destroy the drivers in the memory devices. EX1043,89-90. A POSITA would have understood from the ’386 Patent that the disclosures in the earlier applications would ***not*** have worked in normal operation

because their disclosures failed to address these collisions during read operations, making the memory module unusable as a practical matter. EX1003,¶192. Indeed, a POSITA would have known that back-to-back read commands were part of the JEDEC standards, and thus part of the normal operation of memory modules at the time. *See,e.g.*,EX1029,28-29&Fig.27(annotated below);EX1030,19(Fig. 8 illustrating consecutive reads for DDR1 memories);EX1003,¶193.



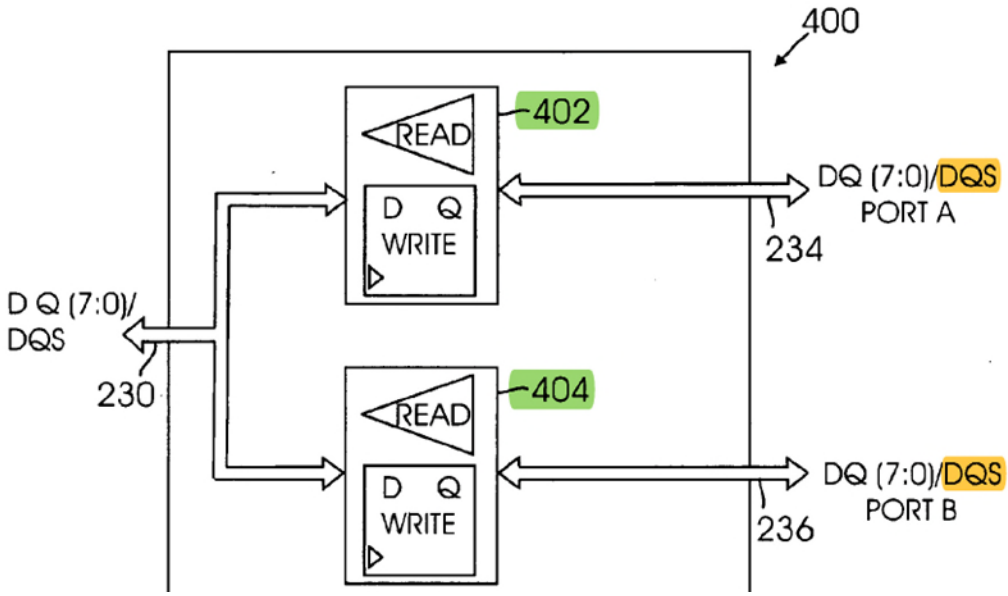
The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 27 — Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

The earlier ’436 Patent does not describe how to avoid collisions in this situation. EX1009,18:3-6. Thus, a memory module made following the disclosure of the ’436 Patent and/or the prior provisional applications would fail — and even possibly “burn” the drivers of the memory devices — during standard back-to-back read operations. EX1003,¶193.

The portions of the 912 Patent added July 1, 2005, disclose for the first time in this priority chain a solution to the previously-described problems: during back-to-back read operations, "collisions are avoided by a mechanism which *electrically isolates the DQS data strobe signal lines 104 of the memory devices from one another…*" EX1001,24:23-28,25:58-60;EX1008,24:41-56,26:9-12. Claim 16 does not exclude back-to-back adjacent read commands, so the description added in the July 1, 2005 application was necessary to support and/or enable the full scope of the claim. EX1003,¶194.

By then, Ellsberry (filed 6/1/05) had already disclosed this solution to back-to-back read operations, since its memory bank switch has a separate port (Port A and Port B) for each of the two memory devices emulating a higher-capacity memory device. EX1037,*e.g.*,FIG.4(reproduced below in part, annotated);EX1003,¶195.



Ellsberry teaches that, during back-to-back read operations, data and strobe signals are driven to the system bus only by ***one*** bidirectional driver (through one port) to avoid bus conflicts. EX1003,¶195;EX1037,[0031],[0040],[0045]&FIG.4; *see also* EX1043,89-90. Ellsberry's solution is similar to 912 Patent's later-disclosed solution to the same problem, *see*,EX1001,25:6-25,FIG.6D, except that the 912 Patent uses FET switches for the selective coupling instead of Ellsberry's bidirectional drivers, EX1001,24:45-49, and Ellsberry describes FET switches as too slow and imprecise to comply with current JEDEC standards. EX1037,[0009],[0057];EX1003,¶195.

Therefore, a POSITA would have understood that, before July 1, 2005, the inventors of the 912 Patent were not in possession of, and did not provide an

enabling disclosure for, the full scope of claim 16 of the 912 Patent — making Ellsberry prior art. EX1003,¶¶188,196.

2. Claim 16

a) [16[pre]]: *Memory Module*

Ellsberry discloses a "*memory module* [e.g., 106] *connectable to a computer system* [e.g., 100]." EX1003,¶¶197-203. Indeed, the Board has already determined, in a Final Written Decision against Patent Owner, that Ellsberry discloses "*[a] memory module . . . configured to communicate with a memory controller*" wherein the memory module includes a "*printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket*," which encompasses the requirements of [16.pre]. EX1038,17,23-25;EX1003,¶202.

Ellsberry describes a memory module, such as 106 with a capacity expanding device 108, connectable to a computer system, such as 100 including a processing unit 102 and I/O controller 104. EX1037,[0023],[0027],FIG.1(below); EX1003,¶¶198-199.

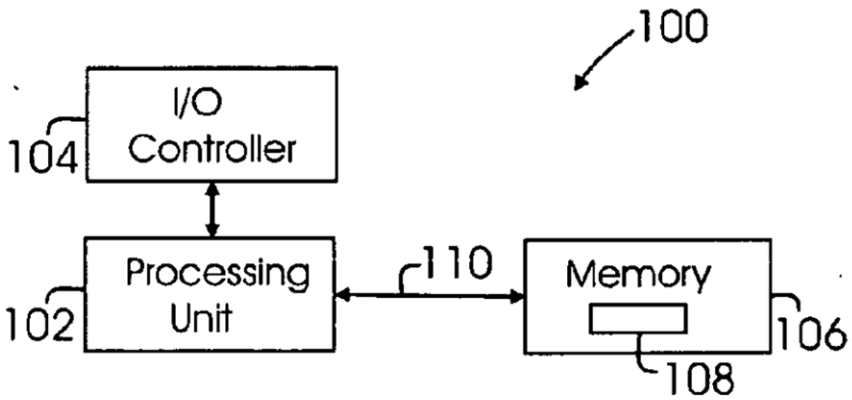


Fig. 1

Describing an embodiment of its memory module, Ellsberry discloses that "FIG. 12 illustrates a single chip-select memory configuration in which one control unit 1202[(red)] and one bank switch 1204[(blue)] are used to control two memory banks 1206[(light blue)] &1208[(light green)], each memory bank having one memory device 1210." EX1037,[0055],[0052]&FIG.12(annotated below);EX1003,¶200.

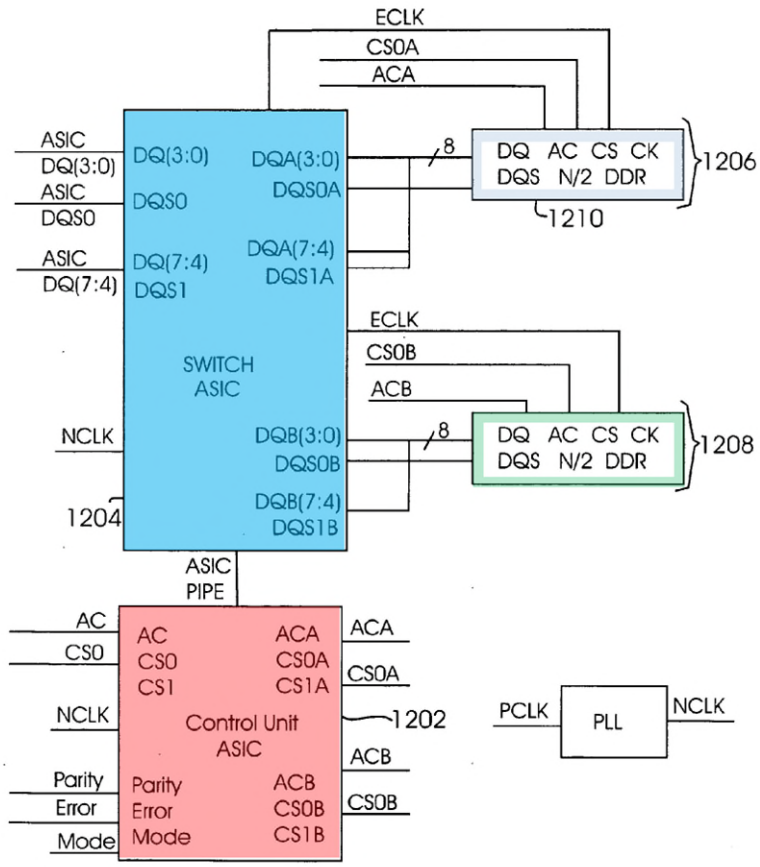


Fig. 12

While Figure 12 above has only two memory devices (and two ranks, identified by chip-select signals CS0A and CS0B), Ellsberry also discloses other implementations with more memory devices (and ranks), such as Figure 13 below (four memory devices (and four ranks, CS0A, CS1A, CS0B, and CS1B)). EX1037,FIG.13(annotated below). The following analysis of Ellsberry applies equally to that implementation. EX1003,¶201.

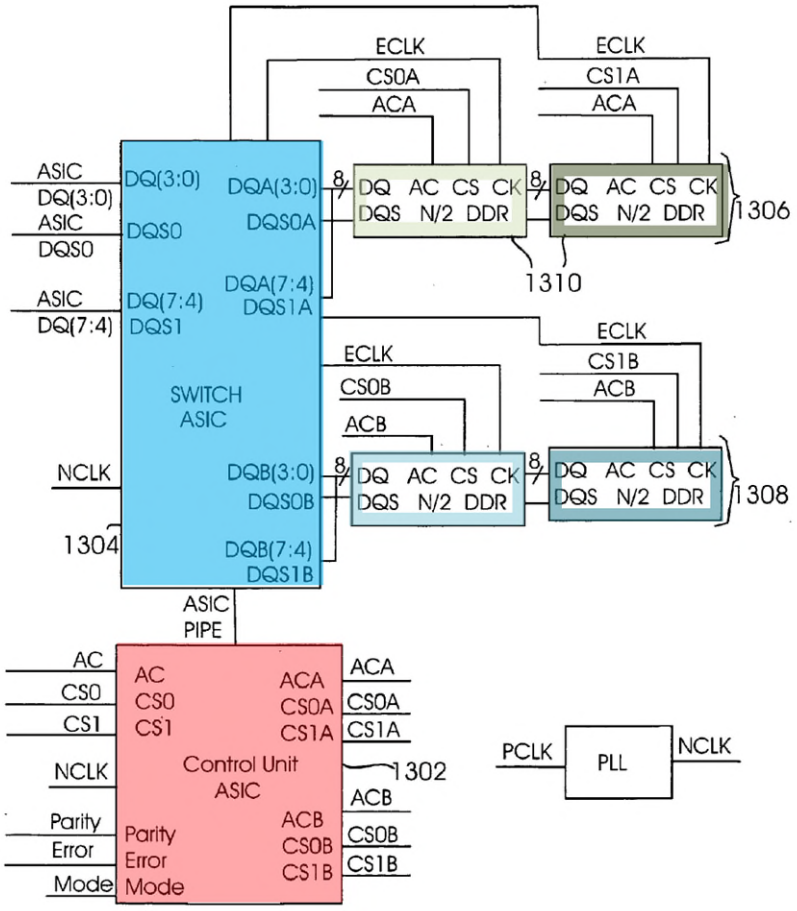


Fig. 13

b) [16.a]: ***<u>Printed Circuit Board</u>***

<u>Ellsberry</u> discloses "*a printed circuit board*." EX1003,¶¶204-208. Indeed, the Board has already determined, in a Final Written Decision against Patent Owner, that <u>Ellsberry</u> discloses a memory module with a "*printed circuit board (PCB),*" encompassing the requirements of [16.a]. EX1038,23-24;EX1003,¶207.

For example, <u>Ellsberry</u> explains that, "[t]ypically, memory modules include a small ***circuit board*** with contact pads along one edge to couple to a slot on another circuit board, such as a computer motherboard." EX1037,[0002];

EX1003,¶205. A POSITA would have understood and found obvious at the time that Ellsberry's "circuit board" is a printed circuit board (PCB). For example, Ellsberry discloses that the DDR2 memory devices have a "FBGA" package which a POSITA would have understood is designed for mounting the memory devices on the PCB. EX1037,FIG.5;*see also*,EX1032 4.20.4-22,-66("BGA" for "printed circuit board");EX1029,1-5. Furthermore, using printed circuit boards was common for memory modules at the time. *See,e.g.*,EX1035,5:60-62; EX1032,4.20.4-29,-66;EX1003,¶206.

c) [16.b]: *DDR Memory Devices*

Ellsberry discloses "*a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board*." EX1003,¶¶209-213. Indeed, the Board has already determined, in a Final Written Decision against Patent Owner, that Ellsberry discloses a memory module with "*memory devices*" on a "*printed circuit board (PCB),*" where the memory devices are shown as "DDR2" memory devices, encompassing the requirements of [16.b]. EX1038,4,23-26;EX1003,¶212.

Ellsberry discloses "DDR" and "DDR2" memory devices. EX1037, [0026],[0046];EX1003,¶211. Ellsberry further explains that "'memory module' refers to any package in which one or more memory devices are mounted..." EX1037,[0023]. As previously explained for claim element [16.a], Ellsberry teaches that such a package includes a circuit board (e.g., PCB). EX1003,¶¶204-

208. For example, "[m]emory devices are typically mounted on…the small circuit board of the memory module." EX1037,[0003];EX1003,¶¶210.

d) [16.b.i]: *First Number of Ranks*

Ellsberry discloses "*the plurality of DDR memory devices having a first number of DDR memory devices* [e.g., two x8 memory devices] *arranged in a first number of ranks* [e.g., two ranks]." EX1003,¶¶214-223. Indeed, the Board has already determined, in a Final Written Decision against Patent Owner, that Ellsberry discloses *"a plurality of memory devices,"* EX1038,19 (citing EX1037,[0003],[0026],[0030],[0032]), where those memory devices are organized in "ranks" as properly construed here, *see supra*,§IV.D.1,pp.11-14. Specifically, the Board pointed to "four memory banks (i.e., Bank 0, Bank 1, Bank 2, and Bank 3)" corresponding to data groups, EX1038,19, and found that each of Ellsberry's multiple (M) data groups simultaneously output or receive one byte (n=8 bits), thus acting on the full bit width ($N=M\times n$) of the module. *Id*.,17,19-21(citing EX1037,[0031],[0040],FIG.2). Thus, the Board found that each of Ellsberry's four "banks" discloses a respective "*rank"* as understood by a POSITA,*supra*,§IV.D.1,pp.11-14. These findings by the Board encompass the requirements of [16.b.i]. EX1003,¶222.

Figure 12 is an implementation of Ellsberry with two x8 DDR memory devices arranged in two "*ranks*" as properly construed (called memory banks 1206

&1208 corresponding to ports A and B, respectively), indicated by chip-select signals CS0A and CS0B. EX1037,FIG.12(annotated below);*supra*,§IV.D.1,pp.11-14(construing "*rank*");EX1003,¶215.

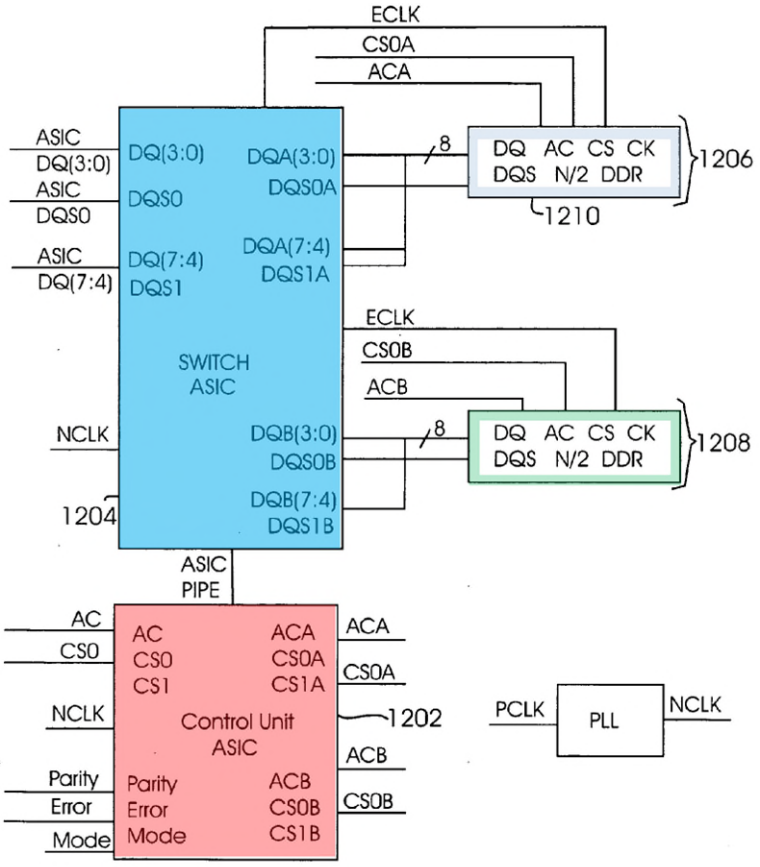


Fig. 12

As shown above, Ellsberry teaches that each memory device has its own separate chip select signal (CS0A, CS0B) and the same data width of 8 bits ("/8") as the module with a single data buffer (blue, coupled to eight system data lines DQ[7:4] and DQ[3:0]). EX1037,FIG.12 (annotated above). Thus, Ellsberry discloses a memory module which is eight bits wide and has two 8-bit wide ranks (light blue,

and light green, above), each controlled by a separate chip select signal. The module shown in Figure 13 is similar except with four 8-bit wide ranks, each controlled by a separate chip select signal (CS0A, CS1A, CS0B, CS1B). EX1003,¶216.

Ellsberry teaches a POSITA that a memory module can include only a single data group having a data buffer and corresponding memory devices. EX1037,[0021],[0030]. Ellsberry teaches a POSITA that the configuration can, but is not required to, be expanded to several data groups. *Id.*,[0035]; *see also,e.g.*,EX1035,FIG.5B(W_{DP}=8 bits);EX1003,¶217.

To the extent one might argue that Ellsberry does not disclose a module with a single data group, it would have been obvious to a POSITA to make a memory module with only a single data group, as expressly illustrated in Ellsberry's Figures 10-13. A POSITA would have understood that this single data group would have been simpler to make and required fewer parts, leaving fewer error sources, than a module with multiple data groups. EX1003,¶218. Moreover, the 912 Patent itself discloses that a "rank" could be a single memory device, as discussed above, *supra*,§IV.D.1,pp.11-14;EX1003,¶¶219-220.

Ellsberry's disclosure is consistent with the understanding of a POSITA that a memory module can have a single rank, which rank can contain a single memory device. EX1033,413("Essentially, a *rank* of memory is a '*bank*' of ***one or more***

DRAM devices that operate in lockstep…");EX1037,[0023](“‘memory module’ refers to any package in which ***one or more*** memory devices are mounted...”);EX1003,¶221.

e) [16.c]: *Circuit Comprising Logic Elements and Register*

Ellsberry discloses “*a circuit* [(e.g., Control Unit ASIC, red)] *coupled to the printed circuit board, the circuit comprising a logic element* [(e.g., control block)] *and a register* [(e.g., register 302)],” as shown in Figure 3 (annotated below). EX1003,¶¶224-225.

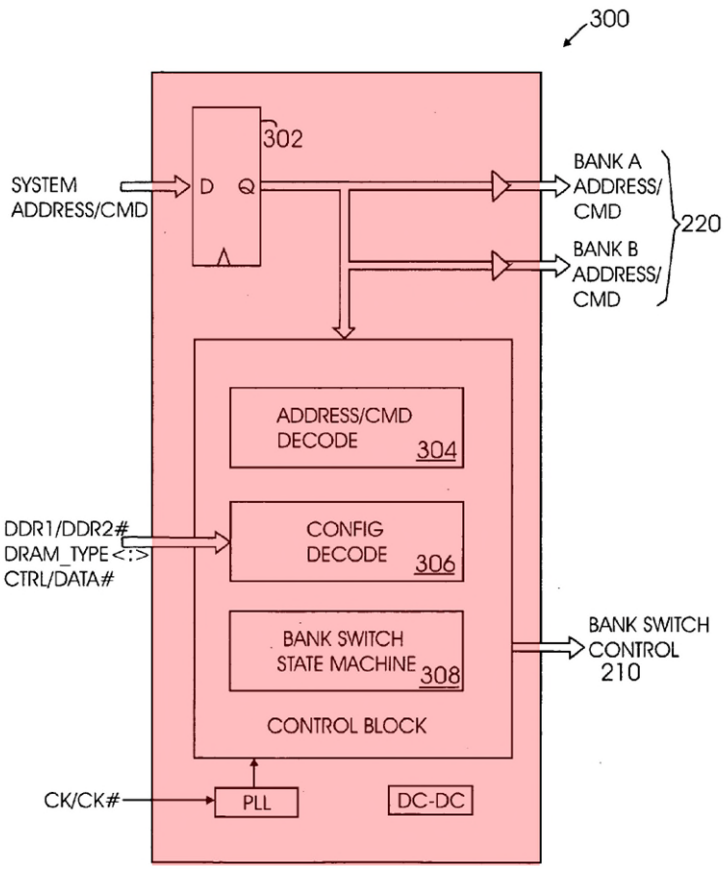


Fig. 3

Indeed, the Board has already determined, in a Final Written Decision against Patent Owner, that Ellsberry discloses *"a module control circuit . . . to produce first module control signals,"* EX1038,18-19, where those signals are identified as "registered" signals, *see* EX1037,FIG.2. These findings by the Board encompass the requirements in [16.c] of a "*circuit*" comprising a "*logic element*" (e.g., to generate first module control signals) and "*register*" (e.g., to output "registered" signals). EX1003,¶226.

Ellsberry discloses that "[m]emory addresses and command information are received from the DIMM interface 202, buffered in a register 302 … The memory address and command information is also decoded 304 … A bank switch state machine 308 then determines which memory bank should be activated or accessed." EX1037,[0039]. A POSITA would have understood from this that the "Control Block" shown in Figure 3 includes a "*logic element*" and "*register*." EX1003,¶224.

Ellsberry further teaches that the control unit (red, above) is coupled to the circuit board. EX1037,[0047],[0049] ("memory controller 510 is mounted on the substrate 502 …. According to one embodiment of the invention, a memory controller 510 is a control unit 204"),[0039] (explaining control unit 204 can include address and command processing system 300 in Fig.3). Thus, a POSITA would have understood that the "*circuit*" of Ellsberry's Figure 3 can be implemented as part of the Control Unit (red, below) in Figure 12 (and Figure 13 in the case of four ranks). EX1037,[0052];EX1003,¶225.

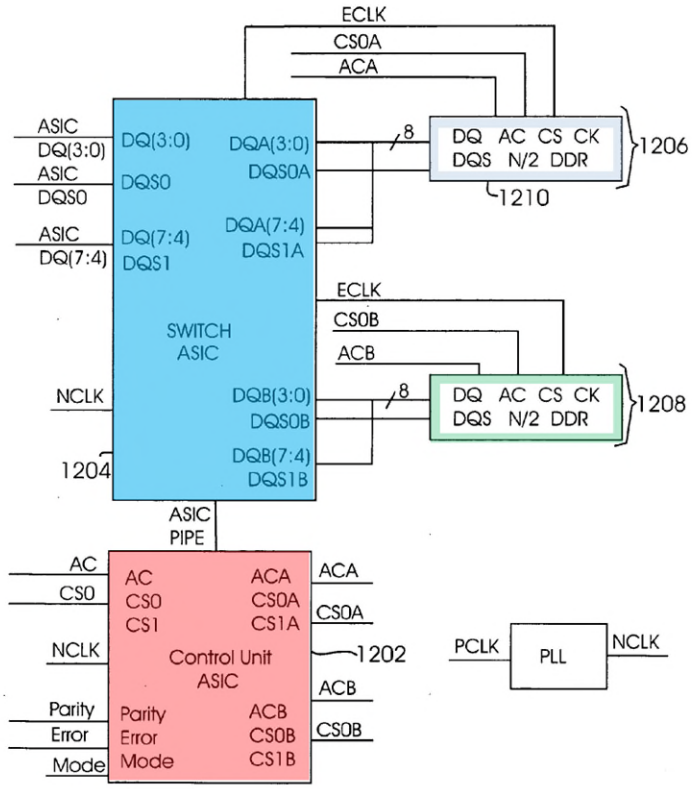


Fig. 12

f) [16.c.i]: Set of Input Signals

Ellsberry discloses "*the logic element* [e.g., the Control Block in Control ASIC (red)] *receiving a set of input signals from the computer system* [e.g., signals associated with a read or write command per the JEDEC standard, EX1029,6,49], *the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal* [per the JEDEC standard, EX1029,6,49&n.2 (A0-A15[3],BA0-BA2,CS)]." *See,e.g.*,EX1037,FIG.3(annotated

[3] See p.36,n.2.

below left, illustrating the registered system address/CMD signals received by the Control Block in the Control ASIC, red),FIG.12(annotated below right, illustrating the Control ASIC, red, receiving input address and command signals AC with input chip select signal CS0 separately shown);EX1003,¶¶228-230.

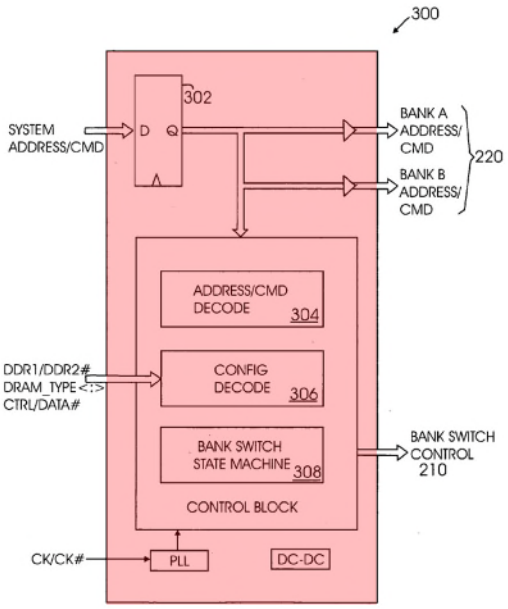


Fig. 3

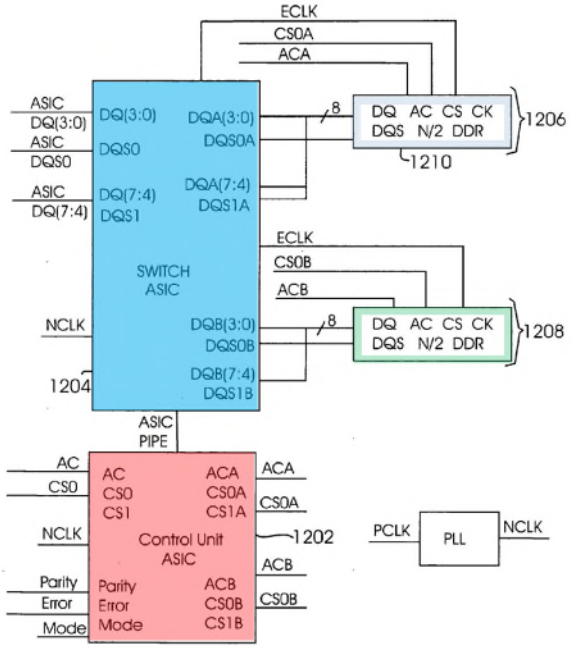


Fig. 12

A POSITA would have understood that the received address and command signals include "*row/column address*" signals (in Address/Command, "AC," signals), "*bank address*" signals (in "AC" signals, to determine target bank within each memory device for the read or write command), and a "*chip-select*" signal (CS, needed to select the rank of memory device(s) for the read or write command), consistent with the JEDEC standard for DDR memory devices, below. *Id*.,FIG.8B,n.3;EX1029,6(annotated below);EX1003,¶228.

1.2 Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, and DM signal for x4x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (UDM), (LDM)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/$\overline{RDQS}$ is enabled by EMRS command.
BA0 - BA2	Input	**Bank Address Inputs:** BA0 and BA1 for 256 and 512Mb, BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A15	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands.
DQ	Input/Output	**Data Input/ Output:** Bi-directional data bus.
DQS, ($\overline{DQS}$) (UDQS), ($\overline{UDQS}$) (LDQS), ($\overline{LDQS}$) (RDQS), ($\overline{RDQS}$)	Input/Output	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15. For the x8, an RDQS option using DM pin can be enabled via the EMRS(1) to simplify read timing. The data strobes DQS, LDQS, UDQS, and RDQS may be used in single ended mode or paired with optional complementary signals $\overline{DQS}$, $\overline{LDQS}$, $\overline{UDQS}$, and $\overline{RDQS}$ to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables all complementary data strobe signals.

The signals highlighted above are also shown below, where Bank Activate includes a row address for a specific bank, and Read and Write commands include a column address for a specific bank, where the bank is identified by bank address (BA) signals. *Id.*,49&n.2;EX1003,¶228.

Table 10 — Command truth table.

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.
NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

Ellsberry teaches that the bank switch state machine 308 in the control unit ASIC uses the received bank address signals, including Bank A(2) (purple, below), to map the primary (input) address space of a simulated DDR2 memory device (e.g., red, below) to the address space of two actual DDR2 memory devices on the module (e.g., blue and green, below). EX1037,[0039],FIG.7D(annotated below);EX1003,¶229.

Configuration	Primary Address Space	RC Mode INVERT	Mode	PHY Bank Select	Secondary Address Space
DDR II, 2 X 256M (x8)	BA 0h - 3h Row 0000h -3FFFh Column 000h - 3FFh	X	ROW	ROW A(13)	BA 0h - 3h Row 0000h-1FFFh Column 000h-3FFh BA 0h - 3h Row 2000h-3FFFh Column 000h-3FFh
DDR II,2 X 512M (x4)	BA 0h - 7h Row 0000h - 3FFFh Column 000h - 7FFh	X	BANK	BANK A(2)	BA 0h - 3h Row 0000h-3FFFh Column 000h-7FFh BA 4h -7h Row 0000h-3FFFh Column 000h-7FFh
DDR II ,2 X 512M (x8)	BA 0h - 7h Row 0000h - 3FFFh Column 000h - 3FFh	X	BANK	BANK A(2)	BA 0h - 3h Row 0000h-3FFFh Column 000h-3FFh BA 4h -7h Row 0000h-3FFFh Column 000h-3FFh

Fig. 7D

As shown above, the state machine selects the physical bank that is the target of a read or write operation based on bank address signals, including Bank A(2) when two 512Mb(x8) memory devices, one in each rank, emulates one 1Gb(x8) memory device—consistent with the JEDEC standard (EX1029,7) showing bank address BA2 is the difference between 512Mb and 1Gb addressing for x8 memory devices. EX1037,[0037]; *supra*,§VI.A.2.f),p.40(blue 512Mb vs. red 1Gb);EX1003,¶¶142,229.

Below is another example, where two 256Mb(x8) memory devices emulate one 512Mb(x8) memory device, using row address bit A(13) for the selection—consistent with the JEDEC standard (EX1029,7) showing that the difference

between 256Mb and 512Gb addressing is row address A_{13} for x8 memory devices. EX1037,[0037],FIG.7(annotated below in part);EX1003,¶230.

Configuration	Primary Address Space	RC Mode INVERT	Mode	PHY Bank Select	Secondary Address Space
DDR II, 2 X 256M (x8)	BA 0h - 3h Row 0000h -3FFFh Column 000h - 3FFh	X	ROW	ROW A(13)	BA 0h - 3h Row 0000h-1FFFh Column 000h-3FFh BA 0h - 3h Row 2000h-3FFFh Column 000h-3FFh
DDR II,2 X 512M (x4)	BA 0h - 7h Row 0000h - 3FFFh Column 000h - 7FFh	X	BANK	BANK A(2)	BA 0h - 3h Row 0000h-3FFFh Column 000h-7FFh BA 4h -7h Row 0000h-3FFFh Column 000h-7FFh
DDR II ,2 X 512M (x8)	BA 0h - 7h Row 0000h - 3FFFh Column 000h - 3FFh	X	BANK	BANK A(2)	BA 0h - 3h Row 0000h-3FFFh Column 000h-3FFh BA 4h -7h Row 0000h-3FFFh Column 000h-3FFh

Fig. 7D

As shown in Ellsberry's Figure 7 (above), the mapping from the Primary to the Secondary Address Space also receives the bank address signals (BA) of the "Primary Address Space" used by the system memory controller. For the same reasons discussed above for Amidi, *supra*,§VI.A.2.g),pp.48-51, a POSITA would have understood that the row address bit A(13) is bank specific and arrives before the read or write command, so Ellsberry's logic would use the bank address signals

(BA) to properly store and retrieve the respective row address bit A(13) for each activated bank. EX1003,¶¶158-163,230.

g) [16.c.ii]: *Second Number of Ranks*

Ellsberry teaches that "*the set of input signals* [(including AC and CS0, orange below)] *configured to control a second number of DDR memory devices* [e.g., one x8 memory device] *arranged in a second number of ranks* [e.g., one rank], *the second number of DDR memory devices* [e.g., one] *smaller than the first number of DDR memory devices* [e.g., two x8 memory devices] *and the second number of ranks* [e.g., one] *less than the first number of ranks* [e.g., two]." EX1037,*e.g.*,FIG. 12 (annotated below);EX1003,¶¶232-243.

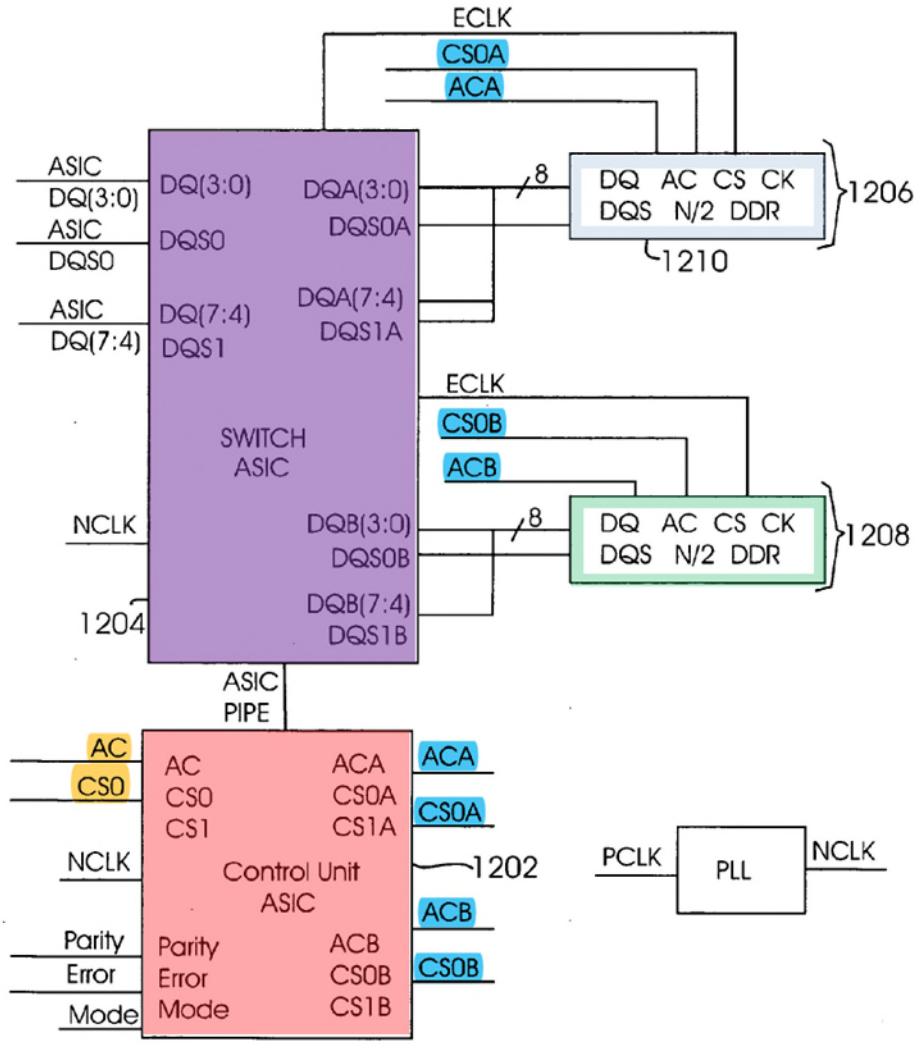


Fig. 12

See also,EX1037,FIG.13;EX1003,¶232.

Ellsberry explains that, in one implementation, the primary address space (included in the "*set of input signals*") corresponds to a single x8 DDR2 memory device with 1Gb (2 times 512Mb) capacity (red, below), and the memory module uses two x8 DDR2 memory devices each having 512Mb capacity (yellow and

blue/green below) to simulate the larger (1Gb) memory device. EX1037,FIG.7D(annotated below);EX1003,¶233.

Configuration	Primary Address Space	RC Mode INVERT	Mode	PHY Bank Select	Secondary Address Space
DDR II, 2 X 256M (x8)	BA 0h - 3h Row 0000h -3FFFh Column 000h - 3FFh	X	ROW	ROW A(13)	BA 0h - 3h Row 0000h-1FFFh Column 000h-3FFh BA 0h - 3h Row 2000h-3FFFh Column 000h-3FFh
DDR II,2 X 512M (x4)	BA 0h - 7h Row 0000h - 3FFFh Column 000h - 7FFh	X	BANK	BANK A(2)	BA 0h - 3h Row 0000h-3FFFh Column 000h-7FFh BA 4h -7h Row 0000h-3FFFh Column 000h-7FFh
DDR II ,2 X 512M (x8)	BA 0h - 7h Row 0000h - 3FFFh Column 000h - 3FFh	X	BANK	BANK A(2)	BA 0h - 3h Row 0000h-3FFFh Column 000h-3FFh BA 4h -7h Row 0000h-3FFFh Column 000h-3FFh

Fig. 7D

A POSITA at the time would have understood from this that the primary address space (red, above) corresponds to a JEDEC 8-bit wide (x8) memory device with a total capacity of 1Gb (red below), and the secondary address space (light green and blue, above) corresponds to two JEDEC 8-bit wide (x8) memory devices, each with a capacity of 512Mb (blue/green below). EX1029,7 (annotated below). Ellsberry illustrates that the primary address space uses three bank address bits (BA 0h-7h above; BA0-BA2 below), 14 row address bits (Row 0000h-3FFFh above; A_0-A_{13} below) and 10 column address bits (Column 000h-3FFh above; A_0-

A_9 below) consistent with the JEDEC standard below for a 128Mbx8 (i.e.,1Gb) memory device (red below). *Id.*;EX1003,¶234

Table 2 — 512Mb Addressing

Configuration	128Mb x4	64Mb x 8	32Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 3 — 1Gb Addressing

Configuration	256Mb x4	128Mb x 8	64Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Similarly, the secondary address space in Ellsberry corresponds to the JEDEC standard (light blue and green, above, in this example). EX1037,FIG.7(above);EX1003,¶235. As taught by Ellsberry, the difference in the address spaces (green/blue vs. red) is a bank address bit, Bank A(2) (BA2 above), which is used to select one of the two physical ranks on the module for a given address in the primary address space, showing that Ellsberry uses the three bank address signals (BA) in the JEDEC standard to determine which rank of memory devices to select. EX1003,¶235.

This particular implementation of Ellsberry is nearly identical to the "EXAMPLE 1" Verilog code in the 912 Patent, which also uses bank address bit

BA2. EX1001,14:17-23. This Verilog code simply follows the JEDEC standard for identifying different commands, including those related to pre-charge operations as conveyed by the pre-charge signal on line A10 (blue, below). *Id.*,col.14. In particular, the value a10_in (blue) is used to differentiate precharging all banks or a single bank. *Id.*;EX1003,¶236.

```
// Gated Chip Selects
assign      pcs0a_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                    // ref,md reg set
            | (~rs0_in_N & ras_in_N & cas_in_N)                              // ref exit, pwr dn
            | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)         // pchg all
            | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ~ba2_in)// pchg single bnk
            | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N      & ~ba2_in)    // activate
            | (~rs0_in_N & ras_in_N & ~cas_in_N            & ~ba2_in)        // xfr
            ;
assign      pcs0b_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                    // ref,md reg set
            | (~rs0_in_N & ras_in_N & cas_in_N)                              // ref exit, pwr dn
            | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)         // pchg all
            | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ba2_in)// pchg single bnk
            | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N      & ba2_in)     // activate
            | (~rs0_in_N & ras_in_N & ~cas_in_N            & ba2_in) // xfr
            ;
//-----------------------------------
```

Ellsberry is similar, and identifies A10 as part of the command code (below). EX1037,FIG.8B,n.3;EX1003,¶237.

> 3. A command consists of RAS_n, CAS_n, CS, WE_n, and A(10).

Depending on A10, Ellsberry discloses that an all-bank-precharge command is sent to both memory devices DDR A **and** DDR B, while a single-bank-precharge command is sent only to the target memory device DDR A **or** DDR B, as shown below. EX1037,FIG.8A(annotated below);EX1003,¶238.

Command	Mode	Addr	P Bank	DDR A		DDR B	
				Command	Addr	Command	Addr
MRS	X	X	X	MRS	1	MRS	1
EMRS	X	X	X	EMRS	2	EMRS	2
REFRESH	X	X	X	REFRESH	X	REFRESH	X
SELF REFRESH ENTRY	X	X	X	SLF REFRESH ENTRY	X	SLF REFRESH ENTRY	X
SELF REFRESH EXIT	X	X	X	SLF REFRESH EXIT	X	SLF REFRESH EXIT	X
SINGLE BANK PRECHARGE	Col	X	X	SB PRECHG	X	SB PRECHG	X
	Row/ Bank	X	A	SB PRECHG	X	NOP	X
			B	NOP	X	SB PRECHG	X
ALL BANK PRECHARGE	X	X	X	AB PRECHG	X	AB PRECHG	X
ACTIVATE	Col	X	X	ACTIVATE	X	ACTIVATE	X
	Row/ Bank	X	A	ACTIVATE	X	NOP	X
			B	NOP	X	ACTIVATE	X
WRITE	X	X	A	WRITE	X	NOP	X
			B	NOP	X	WRITE	X
WRITE WITH AUTO PRECHARGE	Row/ Bank	X	A	WRITEAP	X	NOP	X
			B	NOP	X	WRITEAP	X
	Col	X	X	WRITEAP	X	WRITEAP	X
READ	X	X	A	READ	X	NOP	X
			B	NOP	X	READ	X
READ WITH AUTO PRECHARGE	Row/ Bank	X	A	READAP	X	NOP	X
			B	NOP	X	READAP	X
	Col	X	X	READAP	X	READAP	X

ⓐ ⓑ ⓒ ⓓ ⓔ ⓕ ⓖ ⓗ ⓘ

Fig. 8A

A POSITA would have understood that using line A10 for pre-charging comes from the JEDEC standard, below. EX1029,7,49 (annotated below);EX1003,¶¶234,239.

Table 10 — Command truth table.

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3

Therefore, Ellsberry discloses to a POSITA using the transition bit Bank A(2) along with line A10 to perform rank multiplication—just like EXAMPLE 1 of the 912 Patent. EX1003,¶¶236,239.

Another example from Ellsberry is shown below, where two 256Mb(x8) memory devices (yellow and blue/green) simulate one 512Mb(x8) memory device (red). EX1037,FIG.7D(annotated below);EX1003,¶240.

Configuration	Primary Address Space	RC Mode INVERT	Mode	PHY Bank Select	Secondary Address Space
DDR II, 2 X 256M (x8)	BA 0h - 3h Row 0000h -3FFFh Column 000h - 3FFh	X	ROW	ROW A(13)	BA 0h - 3h Row 0000h-1FFFh Column 000h-3FFh BA 0h - 3h Row 2000h-3FFFh Column 000h-3FFh
DDR II,2 X 512M (x4)	BA 0h - 7h Row 0000h - 3FFFh Column 000h - 7FFh	X	BANK	BANK A(2)	BA 0h - 3h Row 0000h-3FFFh Column 000h-7FFh BA 4h -7h Row 0000h-3FFFh Column 000h-7FFh
DDR II ,2 X 512M (x8)	BA 0h - 7h Row 0000h - 3FFFh Column 000h - 3FFh	X	BANK	BANK A(2)	BA 0h - 3h Row 0000h-3FFFh Column 000h-3FFh BA 4h -7h Row 0000h-3FFFh Column 000h-3FFh

Fig. 7D

Like the previous Ellsberry example, this implementation also follows the JEDEC standard, shown below, where here row address A13 is the difference between 256Mb (green) and 512Mb (red) addressing. EX1029,p7(annotated below). As explained before, a POSITA would have understood that the row address bit A13 is bank specific and arrives before the read or write command; therefore, Ellsberry's logic uses the bank address signals to properly store and retrieve the respective row address bit A13 for each activated bank. *See supra*,§VI.A.2.g),pp.48-51;EX1003,¶¶158-163,241;*see also*,*e.g.*,EX1044,8:36-40.

Table 1 — 256Mb Addressing

Configuration	64Mb x4	32Mb x 8	16Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A12	A0 ~ A12	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A8
Page size *1	1 KB	1 KB	1 KB

Table 2 — 512Mb Addressing

Configuration	128Mb x4	64Mb x 8	32Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

The example above from Ellsberry is nearly identical to the "EXAMPLE 2" Verilog code in the 912 Patent. EX1001,17:28-31. Similar to the teaching of Ellsberry, EXAMPLE 2 uses the bank address signals (brown below) to select one of four registers (red) to store the row address bit "a13" (orange below) received with an earlier activate command (blue below). *Id*.,cols.,17-18;EX1003,¶242.

```
// latched a13 flags cs0, banks 0-3
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & ~bnk1_R & ~bnk0_R ) // activate
  begin
        1_a13_00 <= a13_r ;
  end
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & ~bnk1_R & bnk0_R)   // activate
  begin
        1_a13_01 <= a13_r ;
  end
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & bnk1_R & ~bnk0_R)   // activate
  begin
        1_a13_10 <= a13_r ;
  end
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & bnk1_R & bnk0_R)    // activate
  begin
        1_a13_11 <= a13_r ;
  end
```

In EXAMPLE 2, the selection of the target rank is based on the stored row address bit a13 (orange), not the bank address signals. *Id*.,13:21(below),17:29-31;EX1003,¶242.

TABLE 4

Density Transition	Density Transition Bit
256 Mb to 512 Mb	A_{13}
512 Mb to 1 Gb	BA_2
1 Gb to 2 Gb	A_{14}
2 Gb to 4 Gb	to be determined

20

h) [16.c.iii]: *Output Signals*

Ellsberry teaches "*the circuit* [e.g., Control Unit ASIC (red below)] *generating a set of output signals*[e.g., ACA, CS0A, ACB, CS0B (blue below),] *in*

response to the set of input signals [e.g., AC, CS0 (orange below)], *the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks* [e.g., two ranks 1206, 1208 (light blue, light green, below, corresponding to the chip-select signals CS0A and CS0B, respectively)]." *See,e.g.*,EX1037,FIG.12(annotated below, showing two "*ranks*" corresponding to CS0A,CS1A with input control signals for only one "*rank*" corresponding to CS0),FIG.13(showing four "*ranks*," with input control signals for only two "*ranks*");EX1003,¶¶244-246.

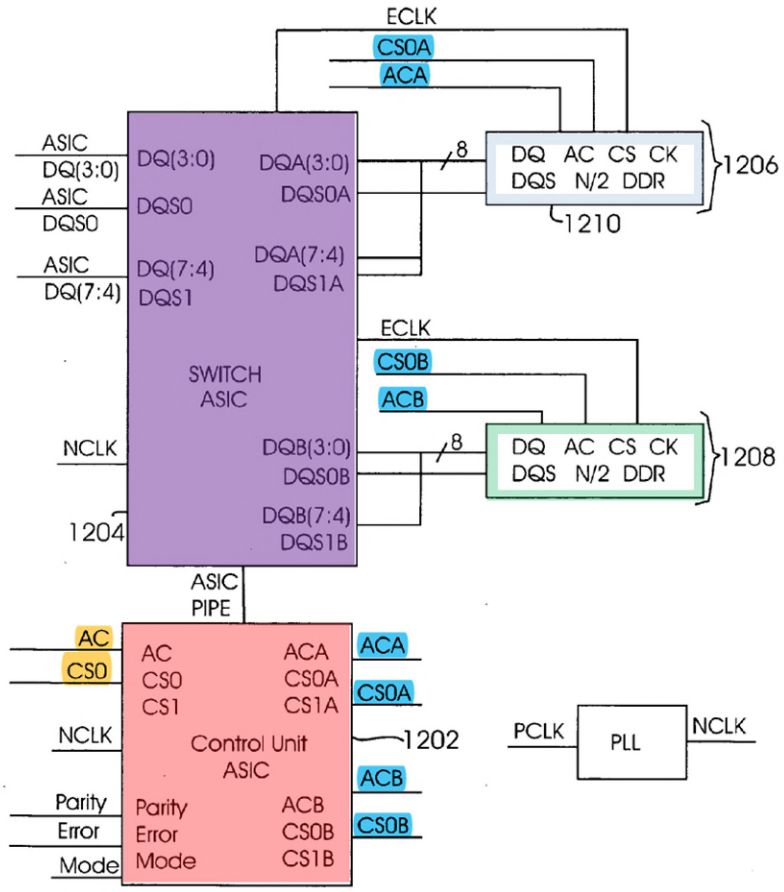


Fig. 12

In addition to Figures 12-13, Figure 8 of Ellsberry describes the relationship between the input signals received by the Control Unit ("*circuit*")(red, above), and the "*output signals*" it sends to the memory devices, consistent with the JEDEC standards. EX1037,*e.g.*,[0050]&FIG.8A (annotated below);EX1029,6,49&n.2. As illustrated below, the column on the left shows the command received by the Control Unit from the system memory controller, and the "DDR A" and "DDR B" columns on the right show the commands sent to the memory device connected to Port A and Port B, respectively. *Id*.,[0042];EX1003,¶245.

Command	Mode	Addr	P Bank	DDR A		DDR B	
				Command	Addr	Command	Addr
MRS	X	X	X	MRS	1	MRS	1
EMRS	X	X	X	EMRS	2	EMRS	2
REFRESH	X	X	X	REFRESH	X	REFRESH	X
SELF REFRESH ENTRY	X	X	X	SLF REFRESH ENTRY	X	SLF REFRESH ENTRY	X
SELF REFRESH EXIT	X	X	X	SLF REFRESH EXIT	X	SLF REFRESH EXIT	X
SINGLE BANK PRECHARGE	Col	X	X	SB PRECHG	X	SB PRECHG	X
	Row/ Bank	X	A	SB PRECHG	X	NOP	X
			B	NOP	X	SB PRECHG	X
ALL BANK PRECHARGE	X	X	X	AB PRECHG	X	AB PRECHG	X
ACTIVATE	Col	X	X	ACTIVATE	X	ACTIVATE	X
	Row/ Bank	X	A	ACTIVATE	X	NOP	X
			B	NOP	X	ACTIVATE	X
WRITE	X	X	A	WRITE	X	NOP	X
			B	NOP	X	WRITE	X
WRITE WITH AUTO PRECHARGE	Row/ Bank	X	A	WRITEAP	X	NOP	X
			B	NOP	X	WRITEAP	X
	Col	X	X	WRITEAP	X	WRITEAP	X
READ	X	X	A	READ	X	NOP	X
			B	NOP	X	READ	X
READ WITH AUTO PRECHARGE	Row/ Bank	X	A	READAP	X	NOP	X
			B	NOP	X	READAP	X
	Col	X	X	READAP	X	READAP	X

a b c d e f g h i

Fig. 8A

Ellsberry further explains how the Control Unit maps the row, column, and bank address signals received from the system controller (primary address space, red below) to the addresses of the physical memory devices on the module (secondary address space, blue/green below). EX.1037,[0037],FIG.7(FIG.7D below, annotated to highlight the first and second examples discussed above with reference to claim element [16.c.ii]);EX1003,¶¶246,232-243.

Configuration	Primary Address Space	RC Mode INVERT	Mode	PHY Bank Select	Secondary Address Space
DDR II, 2 X 256M (x8)	BA 0h - 3h Row 0000h -3FFFh Column 000h - 3FFh	X	ROW	ROW A(13)	BA 0h - 3h Row 0000h-1FFFh Column 000h-3FFh BA 0h - 3h Row 2000h-3FFFh Column 000h-3FFh
DDR II,2 X 512M (x4)	BA 0h - 7h Row 0000h - 3FFFh Column 000h - 7FFh	X	BANK	BANK A(2)	BA 0h - 3h Row 0000h-3FFFh Column 000h-7FFh BA 4h -7h Row 0000h-3FFFh Column 000h-7FFh
DDR II ,2 X 512M (x8)	BA 0h - 7h Row 0000h - 3FFFh Column 000h - 3FFh	X	BANK	BANK A(2)	BA 0h - 3h Row 0000h-3FFFh Column 000h-3FFh BA 4h -7h Row 0000h-3FFFh Column 000h-3FFh

Example 2

Example 1

Fig. 7D

i) [16.c.iv]: Selecting one or two ranks…and transmitting the command signal

Ellsberry discloses "*wherein the circuit* [e.g., Control Unit ASIC (red below)] *further responds to a command signal* [e.g., for a read or write command per the JEDEC standard, EX1029,6,49] *and the set of input signals from the computer system by selecting one or two ranks* [e.g., one rank] *of the first number of ranks* [e.g., two ranks] *and transmitting the command signal to at least one DDR memory device of the selected one or two ranks* [e.g., one rank] *of the first number of ranks* [e.g., two ranks]." EX1003,¶¶248-254.

Ellsberry explains that the "control unit maps a received logical address to a physical address corresponding to the particular memory bank configuration employed. It also directs commands to the memory banks to indicate which memory bank should be operational and which one should be passive (do nothing)." EX1037,[0011]. Ellsberry further explains, and shows in Figure 8 below, that the control unit may "send either the same command [e.g., REFRESH or ALL BANK PRECHARGE below] to both memory banks (DDR A and DDR B) or different commands to each memory bank [e.g., READ or WRITE (with chip-select asserted) to one, and NOP (with chip-select not asserted) to others, EX1029,48,49]…data is written to a memory bank [] while the other memory bank [] receive a NOP [i.e., "no operation" command, EX1029,48,49]." *Id*.,[0042],FIG.8A(annotated below);EX1003,¶249.

Command	Mode	Addr	P Bank	DDR A		DDR B	
				Command	Addr	Command	Addr
MRS	X	X	X	MRS	1	MRS	1
EMRS	X	X	X	EMRS	2	EMRS	2
REFRESH	X	X	X	REFRESH	X	REFRESH	X
SELF REFRESH ENTRY	X	X	X	SLF REFRESH ENTRY	X	SLF REFRESH ENTRY	X
SELF REFRESH EXIT	X	X	X	SLF REFRESH EXIT	X	SLF REFRESH EXIT	X
SINGLE BANK PRECHARGE	Col	X	X	SB PRECHG	X	SB PRECHG	X
	Row/ Bank	X	A	SB PRECHG	X	NOP	X
			B	NOP	X	SB PRECHG	X
ALL BANK PRECHARGE	X	X	X	AB PRECHG	X	AB PRECHG	X
ACTIVATE	Col	X	X	ACTIVATE	X	ACTIVATE	X
	Row/ Bank	X	A	ACTIVATE	X	NOP	X
			B	NOP	X	ACTIVATE	X
WRITE	X	X	A	WRITE	X	NOP	X
			B	NOP	X	WRITE	X
WRITE WITH AUTO PRECHARGE	Row/ Bank	X	A	WRITEAP	X	NOP	X
			B	NOP	X	WRITEAP	X
	Col	X	X	WRITEAP	X	WRITEAP	X
READ	X	X	A	READ	X	NOP	X
			B	NOP	X	READ	X
READ WITH AUTO PRECHARGE	Row/ Bank	X	A	READAP	X	NOP	X
			B	NOP	X	READAP	X
	Col	X	X	READAP	X	READAP	X

a b c d e f g h i

Fig. 8A

The first example discussed above (512Mb to 1Gb), *supra*,pp.83-84,87-92, corresponds to "Bank" addressing mode in Figure 8A above, because an Activate command from the system controller is sent to either DDR A (memory device in rank A) or DDR B (memory device in rank B) depending on the bank address bit BA(2), while the other memory device receives a NOP command. EX1037,[0042],FIG.8A;EX1029,48,49;EX1003,¶¶229,233-235,250. In this example, the selection of the target rank is based on the bank address signals while

a precharge command on signal line A10 is also considered, like in the 912 Patent's EXAMPLE 1. *See supra*,pp.87-92,EX1003,¶¶236-239. Thus to the extent EXAMPLE 1 in the 912 Patent embodies claim 16, Ellsberry discloses the same to a POSITA. EX1003,¶251.

The second example in Ellsberry discussed above (256Mb to 512Mb), *supra*,pp.84-86,92-95, corresponds to the "Row" addressing mode in Figure 8A above since the selection of the rank on the module depends on row address bit A(13). EX1037,FIG.8A;EX1003,¶¶240-241. Here, the selection of the target rank is based on the row address bit which is bank specific and is stored and retrieved according to the bank address signals, like in EXAMPLE 2 of the Verilog code in the 912 Patent. *See supra*, *supra*, 92-95;EX1003,¶242. Thus to the extent EXAMPLE 2 in the 912 Patent embodies claim 16, Ellsberry discloses the same to a POSITA. EX1003,¶252.

To the extent claim 16 requires selection of the target rank to depend on each element in the "*set of input signals*," such an implementation would have been obvious in light of Ellsberry's disclosure, because she would have understood that Ellsberry's rank multiplication is not limited to the expressly disclosed examples. EX1037,FIG.7,[0058]. For example, in light of the JEDEC standard (EX1029,7, annotated below), a POSITA would have understood that Ellsberry's technique can be applied so that four ranks of 512Mb x16 memory devices (green

box) act like one rank of two 1Gb x8 memory devices (red box), where both a row address A_{13} and bank address signals, including BA2, are used to select the target rank, as discussed above. *Supra*,pp.40-41,44-46;EX1003,¶¶142-151,253.

Table 2 — 512Mb Addressing

Configuration	128Mb x4	64Mb x 8	32Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 3 — 1Gb Addressing

Configuration	256Mb x4	128Mb x 8	64Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

j) [16.d]: Phase-Lock Loop Device

Ellsberry discloses "*a phase-lock loop device coupled to the printed circuit board*." EX1003,¶¶255-257;EX1037,[0002],FIG.12 (reproduced below, annotated, showing PLL, yellow, on the bottom right),FIG.13.

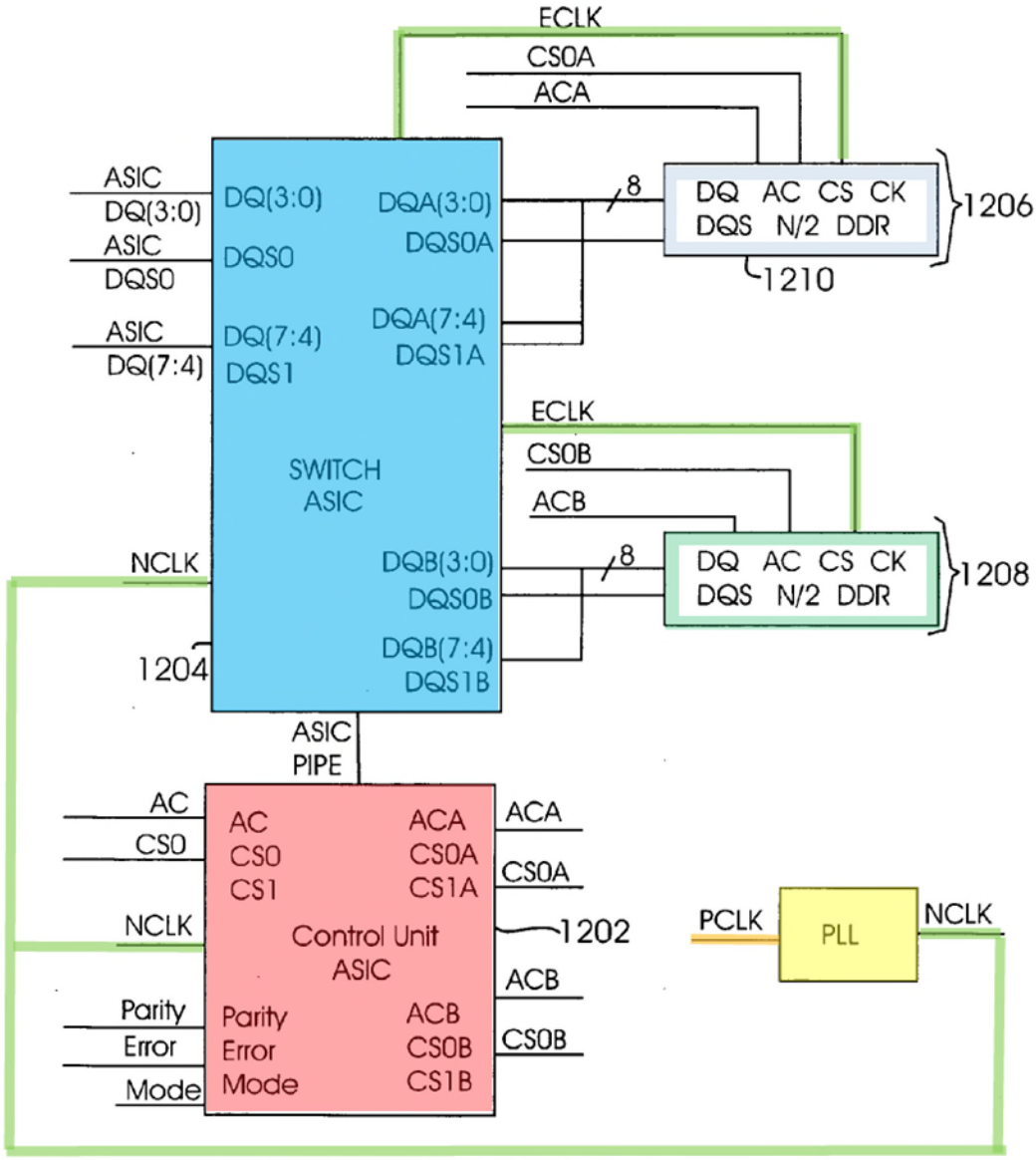


Fig. 12

Ellsberry teaches that a "phase lock loop (PLL) 238 [(yellow)] regenerates a clock signal that can be used by the components on the memory system 200." EX1037,[0030],FIG.2(reproduced below in part, annotated);EX1003,¶256.

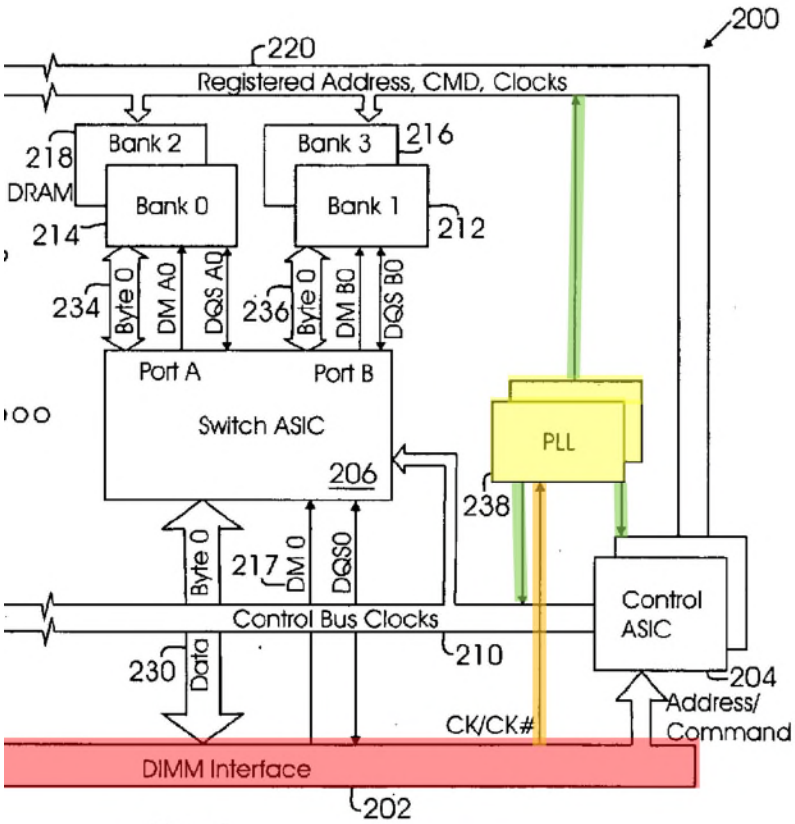


Fig. 2

Ellsberry teaches that the PLL is coupled to the circuit board. *See,e.g.*,EX1037,FIG.5(reproduced below, annotated, showing PLL 514, yellow, coupled to circuit board 502 having an edge interface 506, red),[0048]("An external phase lock loop (PLL) 514[(yellow)] receives a clock signal [(orange line in Figs. 2 and 12 above)] from the edge interface 506[(red)] and provides a clock signal [(green lines in Figs. 2 and 12 above)] to the memory module components"); *see also id.*,[0039],[0045],[0049],FIGS.3,4 (also showing a PLL on the circuit board). EX1003,¶257.

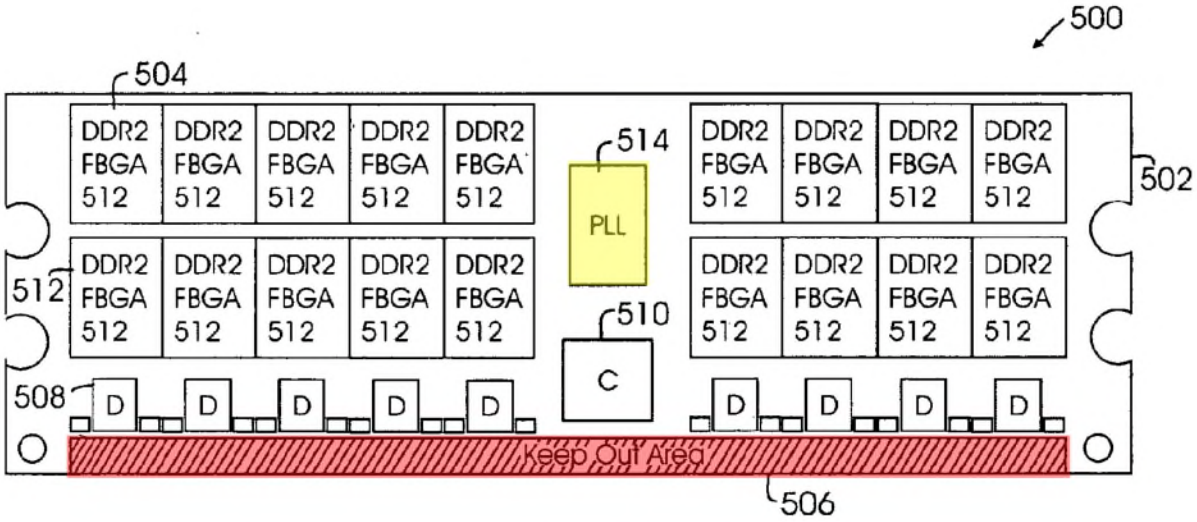


Fig. 5

k) ***[16.d.i]:*** *PLL Coupled to DDR Memory Devices, Logic Element, and Register*

Ellsberry shows "*the phase-lock loop device* [e.g., as shown in FIGS. 2-5,12-13] *operatively coupled to the plurality of DDR memory devices, the logic element* [e.g., the Control Block in the Control Unit ASIC in Fig.3], *and the register* [e.g., register 302 in the Control Unit ASIC in Fig. 3]." EX1003,¶¶259-263.

For example, as explained directly above for [16.d], Ellsberry teaches a PPL. EX1037,[0030],FIGS.2-5,12-13; EX1003,¶¶255-257. As further shown in Ellsberry's Figure 12 (annotated below), and Figure 13, the PLL receives a clock signal (PCLK, orange) and generates a clock signal NCLK (green), which is provided to the Control Unit ASIC (red) and to the Switch ASIC (blue). The Switch ASIC then uses the clock signal NCLK to derive the clock ECLK (green) provided to the memory devices (light blue, light green). Thus, Ellsberry's PLL

circuit is also operatively coupled to the plurality of DDR memory devices. EX1003,¶260.

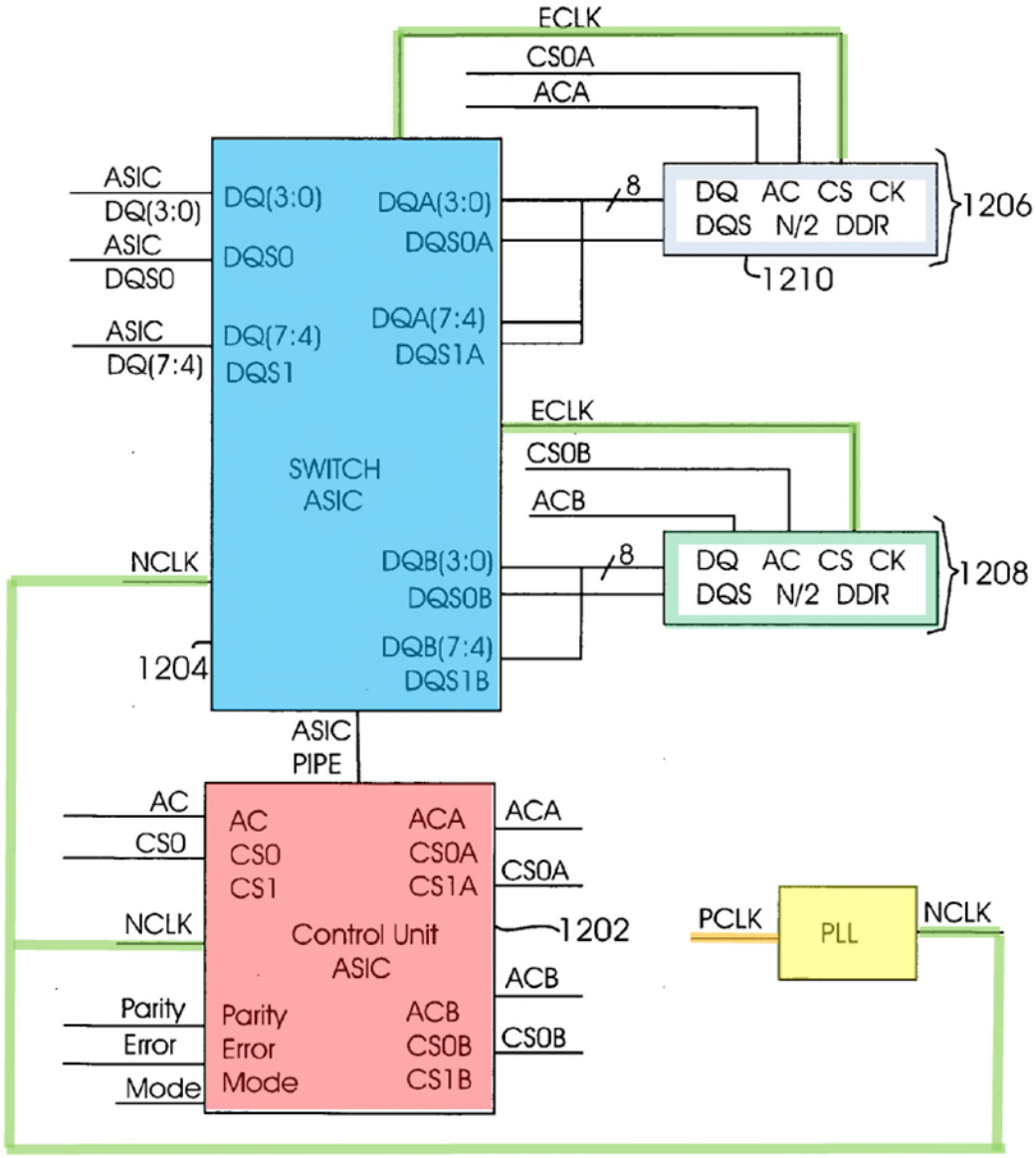


Fig. 12

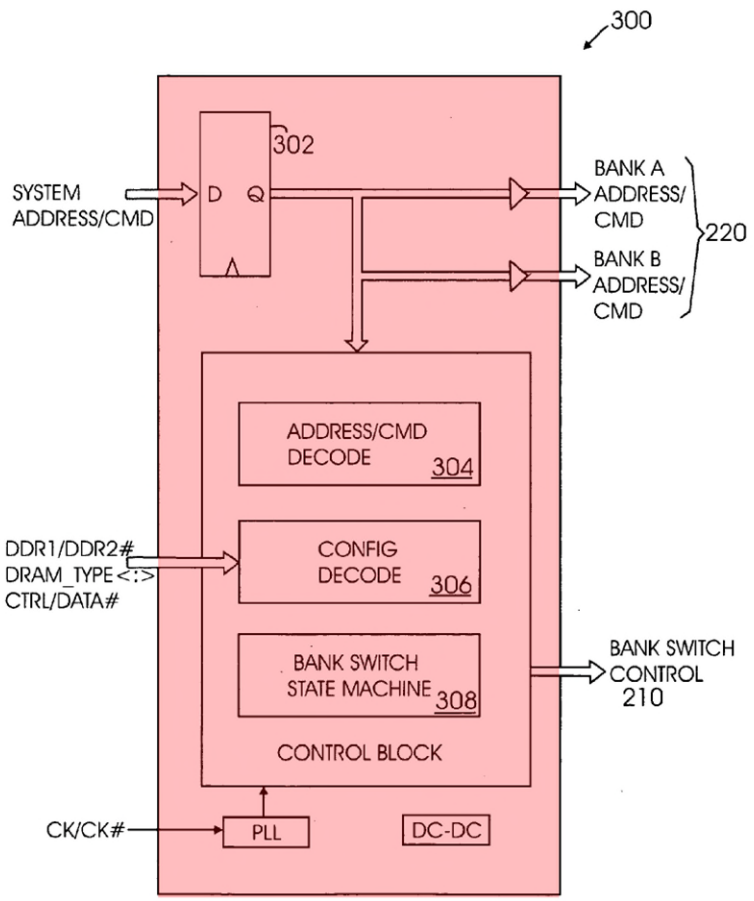


Fig. 3

The Control Unit ASIC (red) further uses the clock signal NCLK from the PLL to derive its own local clocks that are provided to both the Control Block and the register 302 in the Control ASIC. EX1037,FIGS.3(annotated above),12-13;EX1003,¶261.

To the extent one might argue that Ellsberry does not sufficiently disclose that a local clock of the Control Unit ASIC is provided to the register 302 (Fig.3, above), it would have been obvious to a POSITA at the time of Ellsberry's

disclosure. EX1003,¶262. A POSITA would have understood that register 302 is clocked by a local clock signal as indicated by the small triangle at the bottom of register 302. *Id.* As previously discussed, Ellsberry teaches that the Control Unit ASIC, which includes the register 302, receives the clock NCLK from the PLL circuit, and Ellsberry states that the PLL "regenerates a clock signal that can be used by the components on the memory system 200." EX1037,[0030]. Thus, Ellsberry's PLL provides a clock to the Control Unit ASIC which can be used to operate its components, including the register 302. Consequently, a POSITA would have understood and been motivated to use the local clock in the Control Unit ASIC to operate the register 302. EX1003,¶262.

l) [16.e]: *Signal to Only One DDR at a Time*

Ellsberry discloses "*wherein the command signal* [e.g., for a read or write command per the JEDEC standard, EX1029,6,49] *is transmitted to only one DDR memory device at a time*" for the reasons discussed above for [16.b.i], *supra*,§VI.B.2.d),pp.74-77, and [16.c.iv], *supra*,§VI.B.2.i),pp.99-103. EX1003,¶¶264-265. For example, in an implementation of FIG. 12 (reproduced and annotated below) an Activate, Write, or Read command signal is transmitted to only the selected memory device, say DDR A (light blue), and the other memory device, here DDR B (light green), receives a no-operation (NOP) command, as

shown in Figure 8A below. EX1037,FIG.8,12; EX1029,6,48,49; EX1038,32-37; EX1003,¶¶264-265.

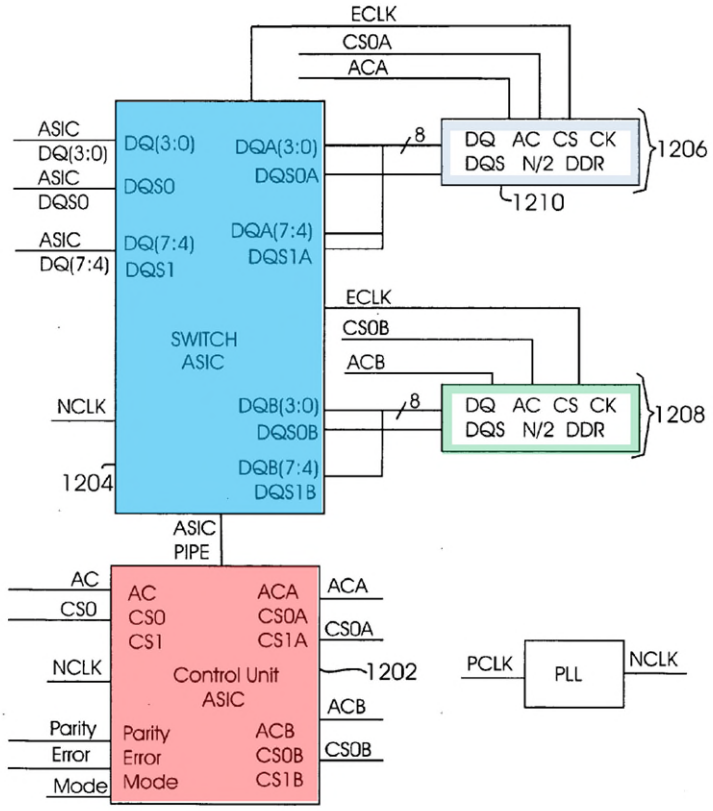


Fig. 12

Command	Mode	Addr	P Bank	DDR A		DDR B	
				Command	Addr	Command	Addr
MRS	X	X	X	MRS	1	MRS	1
EMRS	X	X	X	EMRS	2	EMRS	2
REFRESH	X	X	X	REFRESH	X	REFRESH	X
SELF REFRESH ENTRY	X	X	X	SLF REFRESH ENTRY	X	SLF REFRESH ENTRY	X
SELF REFRESH EXIT	X	X	X	SLF REFRESH EXIT	X	SLF REFRESH EXIT	X
SINGLE BANK PRECHARGE	Col	X	X	SB PRECHG	X	SB PRECHG	X
	Row/ Bank	X	A	SB PRECHG	X	NOP	X
			B	NOP	X	SB PRECHG	X
ALL BANK PRECHARGE	X	X	X	AB PRECHG	X	AB PRECHG	X
ACTIVATE	Col	X	X	ACTIVATE	X	ACTIVATE	X
	Row/ Bank	X	A	ACTIVATE	X	NOP	X
			B	NOP	X	ACTIVATE	X
WRITE	X	X	A	WRITE	X	NOP	X
			B	NOP	X	WRITE	X
WRITE WITH AUTO PRECHARGE	Row/ Bank	X	A	WRITEAP	X	NOP	X
			B	NOP	X	WRITEAP	X
	Col	X	X	WRITEAP	X	WRITEAP	X
READ	X	X	A	READ	X	NOP	X
			B	NOP	X	READ	X
READ WITH AUTO PRECHARGE	Row/ Bank	X	A	READAP	X	NOP	X
			B	NOP	X	READAP	X
	Col	X	X	READAP	X	READAP	X

ⓐ ⓑ ⓒ ⓓ ⓔ ⓕ ⓖ ⓗ ⓘ

Fig. 8A

See also,EX1037,[0042],[0010],[0033];EX1003,¶264.

VII. SECONDARY CONSIDERATIONS

As shown above, the 912 Patent is remarkably similar to Ellsberry, and both were filed within one month of each other. Amidi and Perego also recognized and solved the same problem in the 18 months before the 912 Patent. Such "simultaneous invention" is a secondary consideration of obviousness. EX1003,¶266.

VIII. OTHER CONSIDERATIONS

Discretionary denial of institution is not warranted:

A. §325(d)

Advanced Bionics and §325(d) do not support discretionary denial because this Petition raises new grounds (Perego, Perego in view of Amidi, and Ellsberry) not previously considered and not substantially similar to grounds previously considered. Indeed, Perego was not cited or discussed during prosecution or reexamination, and Ellsberry was not substantively considered because the Examiner simply assumed Ellsberry was not prior art, EX1002,510, which is incorrect as explained above, *supra* §VI.B.1,pp.63-69. And as also explained above, Perego alone and Ellsberry alone each render claim 16 obvious, confirming that they are not cumulative of the references that were considered when claim 16 was allowed. Thus factors (a)-(f) weigh against discretionary denial. *See Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8, 17-18 (PTAB Dec. 15, 2017) (precedential in relevant part).

While Amidi was considered during reexamination, Amidi is used here only as a secondary reference with respect to a few specific limitations to the extent one were to conclude that Perego alone does not disclose or render those limitations obvious, as explained in detail above. "The fact that one piece of art from the combination was previously presented and/or argued to the Office alone is

insufficient to satisfy the first prong of *Advanced Bionics* two-part test…." *Thorne Research, Inc. v. Trustees of Dartmouth College*, IPR2021-00491, Paper 18, 8 (PTAB Aug. 12, 2021); *see also Sony Interactive Entertainment LLC v. Bot M8, LLC*, IPR2020-00726, Paper 13, 12 (PTAB Oct. 6, 2020) (similar); *Comcast Cable Commc'ns, LLC v. Rovi Guides, Inc.*, IPR2019-01434, Paper 14, 14-15 (PTAB Feb. 12, 2020) (similar).

B. §314(a)

There is also no basis for discretionary denial under §314(a).

1. *Fintiv*

Fintiv does not apply with respect to the co-pending litigation between the parties involving the 912 Patent because it was only recently filed and it requests a declaratory judgment of non-infringement, not invalidity. EX1049,1050,1051,1052. Furthermore, there currently is no trial date (factor 2), no discovery has taken place (factor 3), nor is invalidity currently at issue (factor 4). At present it is unclear if or when invalidity will become an issue in that case (factor 6). In any event, given that Patent Owner has not even answered the complaint yet, the Final Written Decision here likely would occur before any trial on invalidity in the district court (factor 2), regardless of any potential stay of the district court action (factor 1).

There is also no basis for discretionary denial under *Fintiv* in light of the co-pending litigation between Google and Patent Owner involving the 912 Patent: ***Factor 1***: Discovery is currently stayed pending resolution of motions that may end that case. EX1046;EX1047. Furthermore, there is a pending motion to strike claim 16 from the case, EX1045, which if granted would eliminate any overlap between that case and this proceeding. ***Factor 2***: Petitioner is unaware of any existing trial date in the Google case, which "weighs significantly against exercising [the Board's] discretion to deny institution of the proceeding." *Google LLC v. Uniloc 2017 LLC*, IPR2020-00441, Paper 13, 35 (PTAB Jul. 17, 2020). ***Factor 3***: Petitioner is unaware of any investment by the court or the parties in the Google litigation with respect to claim 16. To the contrary, it appears that Patent Owner only recently tried to inject claim 16 into that case, and in response Google has filed a motion to keep claim 16 out of the case. EX1045; *Google LLC v. Parus Holdings, Inc.*, IPR2020-00846, Paper 9, 17-18 (PTAB Oct. 21, 2020) (focusing on work already completed, rather than work that might be done in the future). ***Factor 4***: Even if claim 16 remains in the case, Petitioner is unaware of any potential for overlap with the issues in this IPR. ***Factor 5***: Petitioner is a separate company from Google and not a party to the Google case. ***Factor 6***: The grounds presented in this Petition are "particularly strong" and were not previously

considered, which favors institution. *Google*, Paper 9,21 (citing *Fintiv*, Paper 11,14-15).

2. *General Plastic*

Under *General Plastic*, the reexamination filed by Google against the 912 Patent is not a basis for discretionary denial. As an initial matter, *General Plastic* concerned an IPR against the same patent (see factor 3), not a reexamination filed over a decade ago before IPRs were available. To the extent *General Plastic* is even relevant, Petitioner was not involved in the prior reexamination (factor 1) and had no reason to be involved (factors 2, 4, 5). That reexamination was filed by Google and others in response to litigation against them that did not involve Petitioner. That litigation was stayed for 10 years pending the reexamination, EX1045,3:3-20, and only recently (after the reexamination concluded) did Patent Owner suggest for the first time that Petitioner may be infringing claim 16 of the 912 Patent as amended during reexamination, *see* EX1051,¶¶14,40;EX1045,4:4-11,9:14-10:26. In addition, Petitioner was licensed to the 912 Patent starting in 2015, and it was only recently that Patent Owner purported to terminate that license, with a district court in October 2021 ruling that the license termination was effective. EX1051,¶¶21,34. Accordingly, Petitioner now has a reason to challenge claim 16 of the 912 Patent (factors 2, 4), whereas during the pendency of the prior reexamination Petitioner did not (factors 1, 5).

Thus, the timing of this petition is "directly related to Patent Owner's litigation activity" and "any potential prejudice to Patent Owner in having to respond to multiple [proceedings] is outweighed by actual prejudice to Petitioner if institution is denied" because the prior reexamination concluded before Petitioner had any reason to challenge the validity of claim 16 of the 912 Patent. *Google LLC v. Uniloc 2017 LLC*, IPR2020-00396, Paper 11, 16 (PTAB Aug. 3, 2020). In addition, Petitioner did not "wait[] to file the Petition to gain an unfair advantage." *Unified Patents, LLC v. Oceana Innovations LLC*, IPR2020-01463, Paper 11, 13 (PTAB Feb. 23, 2021). There was simply no reason for Petitioner to file an IPR against claim 16 back when the reexamination was pending.

Furthermore, the first *General Plastic* factor "weigh[s] ***overwhelmingly*** against a discretionary denial in this proceeding" given that Petitioner and Google were not co-defendants and are not related companies. *Unified Patents Inc. v. Bradium Technologies LLC*, IPR2018-00952, Paper 31, 20 (PTAB Dec. 20, 2018); *see also Sony Mobile Communications AB v. Ancora Technologies, Inc.*, IPR2021-00663, Paper 17, 10 (PTAB June 10, 2021) (finding no "significant relationship" because "Patent Owner sued Petitioner . . . separately from its competitors"); *Google LLC*, IPR2020-00396, Paper 11, 11 (same); *Prollenium US Inc. v. Allergan Industrie, SAS*, IPR2019-01505, Paper 18, 43-44 (PTAB Mar. 19, 2020) (finding no "significant relationship," even though petitioner relied on overlapping

references with earlier petition, because "this is Prollenium's first Petition, and Prollenium has no connection to the prior petitioner").

IX. CONCLUSION

Petitioner therefore respectfully requests that Trial be instituted and that claim 16 be canceled as unpatentable.

Dated: February 17, 2022

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. § 42.24, because it contains 13,931 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. § 42.24.

Dated: February 17, 2022

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CERTIFICATE OF SERVICE

I hereby certify that on this 17th day of February, 2022, a copy of this Petition, including all attachments, appendices and exhibits, has been served in its entirety by FedEx Express on the following counsel of record for patent owner:

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