UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2022-00615
U.S. Patent No. 7,619,912

DECLARATION OF MICHAEL C. BROGIOLI, PH.D. IN SUPPORT OF PATENT OWNER'S PRELIMINARY RESPONSE

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I, Michael C. Brogioli, declare as follows:

I. INTRODUCTION

1. Netlist, Inc. has retained me to provide testimony regarding the technology involved in U.S. Patent No. 7,619,912 ("the '912 patent") and how it compares with the asserted art.

2. I am being compensated for my work in this matter at my standard hourly rate for consulting services. My compensation is not dependent on the outcome of the case and does not affect the substance of my statements in this Declaration. I have no financial interest in the matter or the patents at issue.

3. I have reviewed the specification and the claims of the '912 patent. I am familiar with the technology involved therein, having worked in the field for the past 23 years.

4. To prepare this Declaration, I have considered the petition, Dr. Wolfe's declaration, the exhibits already submitted, my own experience and knowledge, and the documents cited herein. I provide my testimony from the perspective of a person of ordinary skill in the art at the time of the invention. I was at least a person of ordinary skill in the art at the time of the invention. I am

familiar with the knowledge and skill level of these people at the time of the invention because I was intimately involved in the industry at the time and had frequent interactions with such people at the relevant time. I have also been asked to apply the plain and ordinary meaning of the terms from the perspective of a person of ordinary skill in the art in light of the specification and other intrinsic evidence.

II. EXPERT QUALIFICATIONS AND COMPENSATION

5. Below is a summary of my education and experience. My *curriculum vitae*, included as **Appendix A** hereto, records my education, experience, and publications in greater detail.

6. I am currently an Adjunct Professor of Electrical and Computer engineering at Rice University in Houston, Texas, and Managing Director of Polymathic Consulting in Austin, Texas. I received my Bachelor of Electrical Engineering from Rensselaer Polytechnic Institute in 1999, my Master of Science in Electrical and Computer Engineering from Rice University in 2003, and my Doctorate of Electrical and Computer Engineering from Rice University in 2007.

7. While at Rice University, I developed various computer architecture designs for embedded and high-performance systems, including memory systems. For example, from 1999 to 2003, I worked in the area of low-power computing, specifically focusing on dynamic power management and performance of configurable memory systems, including SRAM based caches. From 2002 to 2004, I developed Spinach, a computer architecture design and modeling toolset, which models system components common to all programmable computing environments, including memory systems, microprocessors, interconnects, etc. From 2004 to 2009, I developed Spinach DSP-FPGA, a modular and composable simulator design infrastructure for programmable and reconfigurable embedded SOC architectures specifically targeting mobile, low-power, and embedded and portable computing devices. From 2005 to 2009, I developed and published a retargetable compiler infrastructure and hardware design exploration toolkit for systems related to embedded computing technologies, which is also used in the design space exploration of memory systems and related technologies. Many of these tools

have been used at United States universities in the area of electrical and computer engineering research.

8. In the late 1990s, I was a hardware and software developer at Vicarious Visions in New York, developing third-party titles for Nintendo's handheld consoles, in addition to various hardware interfaces and software optimizations related to the limited memory I/O and size. During my career, I have served as Chief Technology Officer, advisory board, and board of directors member, often in co-founding roles.

9. From June 2006 to August 2007, I worked as the Technical Co-Founder of Method Seven LLC in Boston, MA, working with high-performance software and hardware systems architecture. I am currently a co-founder, co-inventor, and Chief Technology Officer of Network Native, an Internet of Things technology company as well as others that are detailed on my CV (Appendix A).

10. I have held the position of Adjunct Professor at Rice University since 2009 and the position of Managing Director at Polymathic Consulting since 2011. At Rice University, I instruct graduate-level curriculum in the areas of computer architecture, hardware and software systems. I also advise on

university research and various design initiatives. At Polymathic Consulting, I work with a range of technologists from early-stage start-ups to Fortune 500 companies on similar technologies.

11. From 2008 to 2009, I was Senior Engineer working in high-performance compiler designs and next-generation microprocessors and architectures at Freescale Semiconductor in Austin, TX. From November 2009 to October 2011, I was Chief Architect, Senior Member Technical Staff, at Freescale Semiconductor in Austin, TX (formerly Motorola), responsible for management of technology, engineering roadmaps, design lead on software infrastructure, and next-generation microprocessor architectures for embedded computing. During my tenure at Freescale Semiconductor, I was in charge of system developer tools for processor design, both in the hardware and software spaces. These included tools used for the programming of processors, simulation and design of processors, and related technologies.

12. I have previously worked for Texas Instruments' Advanced Architecture and Chip Technology division in Houston, Texas, in the areas of high-performance mobile and embedded systems design at the hardware and

systems software level, specifically around heterogeneous computing, high-speed bus, and interconnect technologies. I also have worked at Intel Corporation's Microprocessor Research Labs in the areas of computer architecture and compiler technologies.

13. I am recognized as an expert in the field of computer architecture, computer hardware and computer software systems as they relate to the subject matter at hand. I am a member of the Institute of Electrical and Electronics Engineers (IEEE) and have been a Program Committee member for the IEEE and ACM Design Automation Conference since 2011, and have held the role of Program Chair of Design Automation Conference in the area of Embedded Computing.

14. Over the past 15 plus years, I have authored numerous peer-reviewed publications, as well as engineering books in the area of computer hardware and software design. Many of these incorporate technologies specific to the subject matter at hand, including memory system design, optimization for memory systems, and interconnect technology. These publications are disclosed in my *curriculum vitae*, attached as Appendix A. I have previously served as an

engineering consultant and testifying witness on matters related to, and including, microprocessors, chip technology, memory systems, memory modules and related aspects of JEDEC standards, as well as various memory and interconnect technologies. My *curriculum vitae* contains more information on my background and experience, as well as the cases in which I have served as an expert witness over at least the past four years.

15. I am also a named inventor on the following United States patent applications: U.S. Pat. Appl. 17/578,408; U.S. Pat. Appl. 17/306,839; U.S. Pat. Appl. 17/060,625; U.S. Pat. Appl. 16/721,913; and U.S. Pat. Appl. 15/110,643.

16. More information regarding the patent applications for which I am a named inventor can be found in my *curriculum vitae*, attached as Appendix A.

17. I have extensive firsthand experience with the technology underlying the ’912 Patent. I have worked with various SRAM and DRAM technologies, including software and systems optimization related to size and performance of such memories, since the late 1990s. My development of various embedded systems work in the late 1990s include SRAM technologies and high speed access of said systems. Further work in the late 1990s included

optimization of memory intensive applications for efficient high performance usage of SRAM and DRAM memory systems, and optimizations for memory system I/O. My work in the early 2000s was around the use of configurable memory systems and caches comprised of SRAM technologies, and the optimization of memory accesses to maximize CPU compute throughput. I have designed memory system architectures, and system simulation and design technologies both in my doctoral research and publications, as well as within my various roles in industry going back to the early and mid-2000s.

III. A PERSON OF ORDINARY SKILL IN THE ART

18. I have been asked to apply Samsung's definition of a person of ordinary skill in the art for this declaration, in particular the supposed knowledge that such persons would have had at the time of the invention. I understand that Samsung asserts that such people would be familiar with the "various standards of the day including the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with the memory controller of a computer system." Pet., 5-6. I understand that Samsung also asserts that a

person of ordinary skill in the art would have been "familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuitries such as ASICs and CPLDs, and more low-level circuits such as tri-state buffers, flip flops and registers." Pet., 6. I apply Samsung's proposed level of knowledge in my analysis.

IV. THE '912 PATENT

A. General Overview

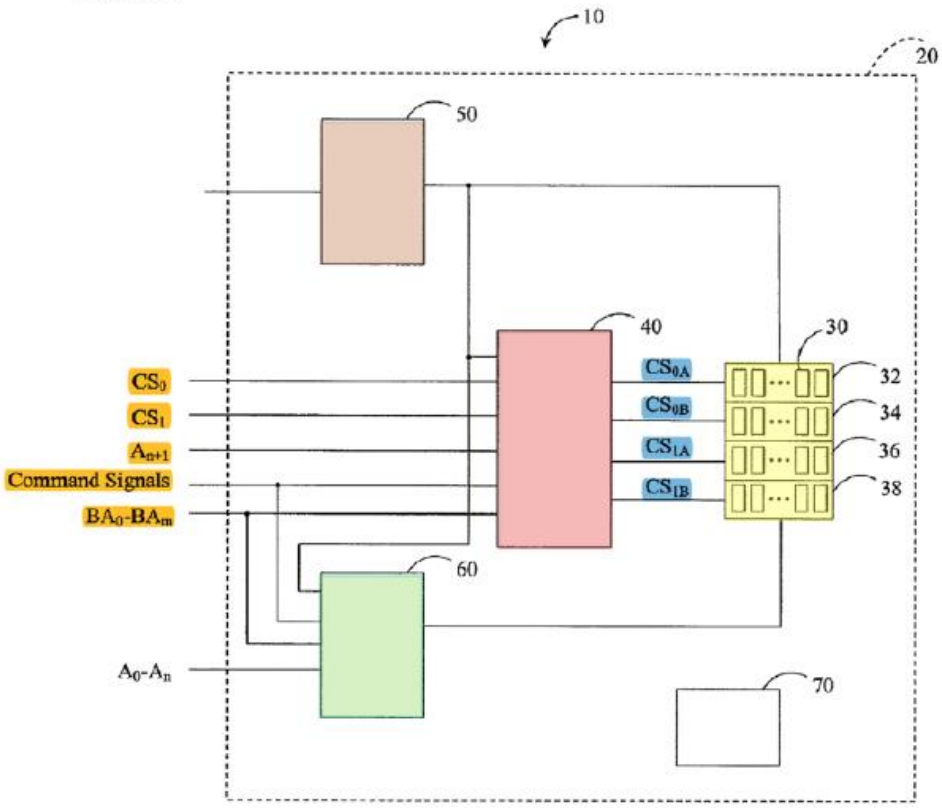
19. The '912 patent relates to memory module technology, and more specifically, to a concept called rank multiplication. A memory module is a device that contains individual memory devices (e.g. DRAM chips) arranged in "ranks" on a printed circuit board. *Id.* at 1:26-31; *see infra*, V. A memory module communicates with a computer system (e.g. a computer server) via the computer system's memory controller. *Id.* at 11:43-48. At the time of the invention, most computer systems supported accessing only one or two ranks, limiting the number of ranks that can be added per memory module. *Id.*, 1:20-2:42.

20. The ’912 patent teaches that one way to upgrade the memory capacity of a memory module is to use on-module logic to present a memory module with, *e.g.*, 2n physical ranks of memory devices, as a module with n (virtual) ranks to the computer system. *Id.*, 6:64-7:19. In this way, “even though the memory module 10 actually has the first number of [physical] ranks of memory devices 30, the memory module 10 simulates a virtual memory module by operating as having the second number of [logical or virtual] ranks of memory devices 30.” *Id.*, 7:9-13. This technique is commonly referred to as “rank multiplication.”

21. Rank multiplication allows a designer to expand the number of ranks and hence the total memory capacity on a memory module. It also enables them to construct a memory module of a given capacity using lower density memory devices that often cost less. *Id.*, 4:42-58, 22:5-14. For example, for the same 1 GB memory capacity, it could be more cost-effective to use thirty-six 256-Mb DRAMs arranged in 4 ranks than eighteen 512-Mb DRAMs arranged in two ranks. *Id.*, 4:42-58, 4:59-5:5.

22. Figure 1A from the ’912 patent, with Petitioner’s annotations below, illustrates an example of a memory module with rank multiplication capability. The memory module has a register 60 (green), a logic element 40 (red), and a phase-lock loop (“PLL”) device 50 (brown).

Figure 1A:



23. The logic element receives a set of input control signals from the computer system that include chip-select signals CS_0-CS_1, address signal A_{n+1},

and bank address signals BA_0-BA_m. *Id.*, 7:35-53; Fig. 1A. From the computer system's perspective, it is connected to only two ranks of memory devices, to be selected by CS_0 or CS_1, even though the memory devices are arranged in four physical ranks. *Id.*, 6:55-7:19. In response to the received input control signals, the logic element then generates a set of output control signals, corresponding to the four physical ranks of the memory devices. *Id.*, 6:61-63. The logic element 40 also receives command signals (such as read/write) from the computer system. *Id.*, 6:55-61, 7:46-53. In response to the command signal and the input signals, the logic element transmits the command signal to the memory devices on the selected rank of the memory module. *Id.*, 7:50-53. In some embodiments, command signals are transmitted to only a single memory device on a multi-device rank at a time. *Id.*, p. 44, 3:9-43.[1]

[1] For shorthand, I refer to individual elements of claim 16 in the same manner as Petitioner. *See* Pet. x-xi.

B. Relevant Prosecution History

24. The application that issued as the ’912 patent was filed on September 27, 2007. EX1002. There were no official rejections during the prosecution of the ’912 patent. *Id.* The ’912 patent issued on November 17, 2009. EX1001.

25. On April 20, 2010, a first request for *inter partes* reexamination of claims 1-51 of the ’912 patent was filed by third party requester Inphi Corp. (“Inphi”), which was assigned control No. 95/001,339. EX1010, 1366. In its request for reexamination, Inphi asserted that claim 16 of the ’912 patent was invalid because “[o]ne of ordinary skill in the art would have understood from [Amidi] that the command signal may be transmitted to the DDR memory devices serially in a sequential fashion.” EX2016, 141.

26. On October 20, 2010, a second request for *inter partes* reexamination of claims 1, 3-4, 6- 11, 15, 18-22, 24-25, 27-29, 31-34, 36-39, 41-45, and 50 of the ’912 patent was filed by third party requester SMART Modular Technologies (WWH), Inc. (“SM”), which was assigned control No. 95/000,578. EX1010, 1366. On October 21, 2010, a third request for *inter*

partes reexamination of claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-34, 36-39, 41-45, and 50 of the ’912 patent was filed by third party requester Google, Inc. (“Google”) which was assigned control No. 95/000,579. *Id.* On February 25, 2011, the PTO merged the ’578, ’579, and ’339 proceedings into a single proceeding. *Id.*, 1367. The PTO authorized all Requesters to file comments. EX1010, 1367 n.1 (Decision Merging Proceedings: “Each time that the patent owner files a response to an action on the merits from the Patent and Trademark Office, the third-party requester shall have one opportunity to file written comments addressing issues raised by the action of the Office or the patent owner's response thereto.”).

27. On April 4, 2011, the Examiner issued a non-final Office Action in the merged proceedings, wherein the Examiner rejected certain claims of the ’912 patent, but affirmed the validity of claim 16. EX1010, 1402-03, 1405. Specifically, the Examiner concluded that, “[w]ith respect to claims 16, 17, Requester 1 asserts that ‘[o]ne of ordinary skill in the art would have understood from [Amidi] that the command signal may be transmitted to the DDR memory devices serially in a sequential fashion’ without any reasoned explanation to

support the assertion. Conclusion of obviousness requires more than a mere conclusory statement." *Id.*, 1402-03; *see also id.*, 1405 (same for Ground 5: Amidi in view of a reference called "Dell2").

28. On October 14, 2011, the Examiner issued another Office Action which again confirmed claim 16 as patentable. *Id.*, 2899-900. On January 14, 2012, Patent Owner filed a response to the October 14, 2011 Office Action, in which Patent Owner rewrote claim 16 in independent form. *Id.*, 3106-07. No other changes were made to claim 16 throughout reexamination. *See* EX1001, p. 44, 3:9-43.

29. On February 13, 2012, Inphi filed its comments in the merged proceedings. EX2029, 26-28. In these comments, Inphi argued that the examiner should reconsider the confirmation of claim 16:

> The Examiner should reconsider the confirmation and allowance of claim 16 over Amidi because the limitation, "wherein the command signal is transmitted to only one DDR memory device at a time" is disclosed by Amidi. As in all DDR memory devices, Amidi provides RAS and CAS signals to isolate a particular memory device in an array of memory cells at the intersection of

> the particular row and column given by those signals…. The intersection of row and column accesses given by RAS and CAS signals, and associated address signals, is for the purpose of accessing a single memory cell. Id. For instance, as shown in Murdocca at p. 248, each intersection of row and column is a unique memory device. Thus, this limitation is inherent in Amidi.

Id., 26-27.

30. On November 13, 2012, the Examiner issued another non-final Office Action in the merged proceedings, wherein the Examiner again confirmed the patentability of claim 16:

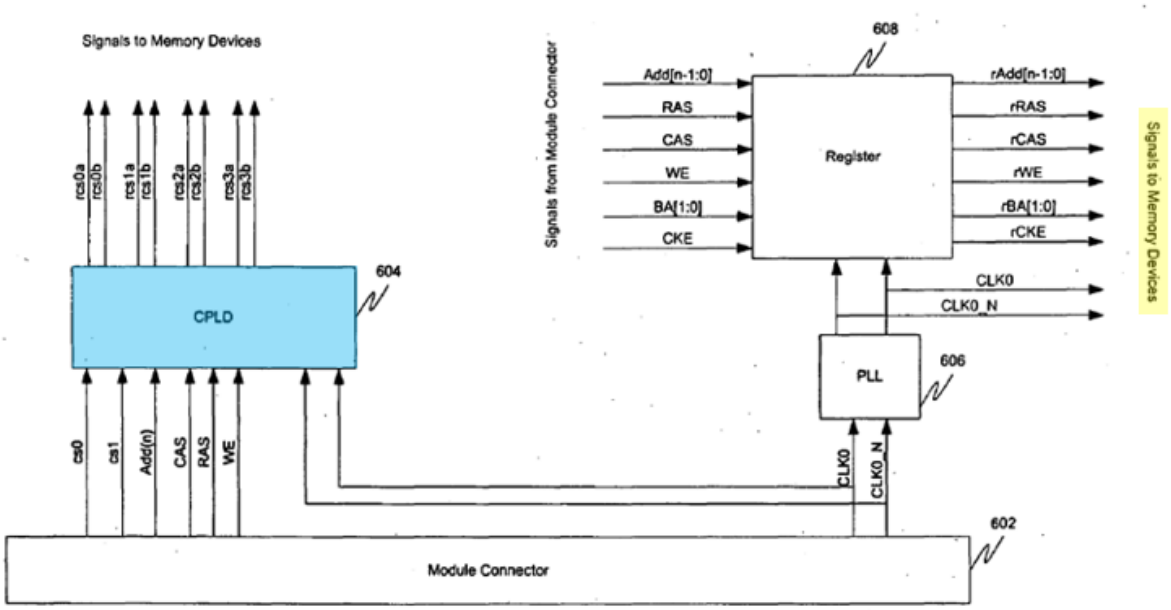
> With respect to claims 16 and 17, Requester 1 asserts that "[o]ne of ordinary skill in the art would have understood from the '152 publication that the command signal may be transmitted to the DDR memory devices serially in a sequential fashion" without any reasoned explanation to support the assertion. Conclusion of obviousness requires more than a mere conclusory statement. The claims require transmission of a command signal to only one DDR memory device at a time. Requester has not provided a reasonable explanation as to why one skilled in the art would transmit a

> command signal to only one DDR memory device at a time ***when there is a plurality of memory devices in a rank***.

Id., 3865-67. Additionally, the Examiner responded to Inphi's February 13, 2012 comments, rejecting the argument that Amidi disclosed Element [16.e]:

> With respect to claims 16 and 17, Requester 1 argues that the limitation "wherein the command signal is transmitted to only one DDR memory device at a time" is disclosed by Amidi allegedly because Amidi provides RAS and CAS signals to isolate a particular memory device in an array of memory cells at the intersection of the particular row and column given by those signals for the purpose of accessing a single memory cell (Comments, pp. 19-20). This is not a persuasive argument because Amidi does not disclose that RAS or CAS signals are transmitted to only one DDR memory device that is being accessed at a time. ***In fact, Figure 6 shows that RAS and CAS signals are transmitted to all devices***. See also JEDEC standard 21-C, p. 4.20-3- 12. RAS, CAS, and WE signals are transmitted to all 18 devices D0-D17 in the DIMM module.

Id., 3904.



Row Address Decoding
FIG.6A

31. On August 14, 2013, SM filed comments in response to the November 13, 2012 Office action, in which, SM argued that Amidi disclosed [16.e] to the extent this limitation was construed to cover single-device ranks:

> **Scope and Content of Amidi**[.] In addition to the limitations of Claim 15, Claim 16 requires "the command signal is transmitted to only one DDR memory device at a time." To the extent the Examiner construes the limitation "the command signal is transmitted to only one DDR memory device at a time" as requiring only that the command signals are sent to a single rank

> because ***"one memory device" encompasses a rank of memory, Amidi discloses this limitation***.

Id., 4442.

32. On March 21, 2014, the Examiner issued an Action Closing Prosecution, in which the Examiner entered SM's comments into the record, but nonetheless maintained its construction of claim 16. *Id.*, 4828, 4830, 4702-4, 4723-25. Thereafter, the parties filed their respective notices of appeal to the Patent Trial and Appeal Board ("Board").

33. On May 31, 2016, the Board issued a Decision on appeal, affirming the Examiner's decision to confirm as valid claim 16. EX1011, 78-80. The Board explained:

> We agree that Amidi teaches using a command signal to read or write to a cell within a DDR memory device. *See* Amidi ¶ 61. Presumably, because Amidi discusses a particular cell within a bank, Requester 1 contends that the command signals are being transmitted to one DDR memory device at a time as recited. R1 App. Br. 18; R1 Reb. Br. 9. Yet, as the Examiner indicates:

> Requester 1 asserts that "[o]ne of ordinary skill in the art would have understood from the '152 publication [of Amidi] that the command signal may be transmitted to the DDR memory devices serially in a sequential fashion" without any reasoned explanation to support the assertion…. The claims require transmission of a command signal *to only one DDR memory device at a time*. Requester has not provided a reasonable explanation as to why one skilled in the art would transmit a command *signal to only one DDR memory device at a time when there is a plurality of memory devices in a rank*.

RAN 29 (emphasis added).

That is, Figures 6A and 6B of Amidi show various command signals (e.g., CS0, CS1, CKE, CAS, RAS, and WE) being transmitted to more than one memory device. Amidi ¶ 62, Fig. 6A-6B (stating "Signals to Memory Devices" at the far right) Moreover, Amidi's Figures 6A and 6B undermines Requester l's assertion that delivering command signals to two or more memory cells at a time would create data bus contention. See R1 Reb. Br. 9. That is, Amidi's Figures 6A and 6B further teach or suggest that the command signal is transmitted to a cell within multiple

> memory devices at a time. Thus, although Dr. Wang's testimony states that the RAS and CAS signals are used to isolate a particular memory cell in an array of a memory device (2d Wang Decl. ¶ 13), there is countering evidence in Amidi to demonstrate that isolating a cell relates to isolating a cell within multiple memory devices at the same time.

EX1011, 79-80.

34. The Board's May 31, 2016 Order also included new grounds of rejection for claims other than 16. *Id.*, 105. Following remand to the Examiner, Patent Owner amended certain claims, but did not amend claim 16. EX1010, 7279-80. The parties thereafter filed their respective appeals to the Board, and the Board again affirmed claim 16. EX1011, 152.

35. The parties filed their respective appeals to the U.S. Court of Appeals for the Federal Circuit, which affirmed the Board. *Google LLC v. Netlist, Inc.*, 810 F. App'x 902 (Fed. Cir. 2020).

C. Priority Date of the '912 Patent

36. The '912 patent claims priority to three provisional applications: Nos. 60/588,244 (EX1005, "the '244 provisional") filed on July 15, 2004,

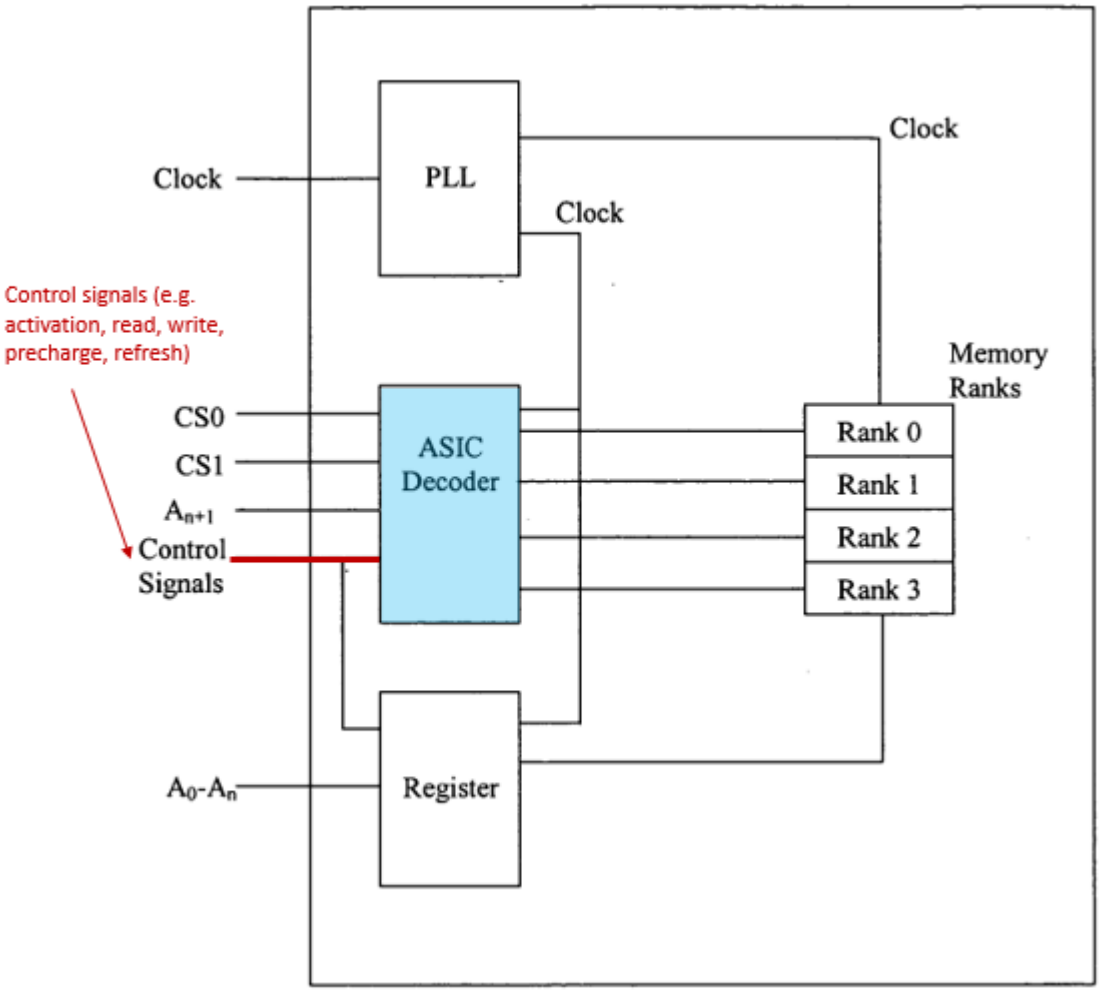
60/550,668 (EX1006, "the '668 provisional") filed on March 5, 2004, and 60/575,595 (EX1007, "the '595 provisional") filed on May 28, 2004. EX1001. The '912 patent also claims priority to application No. 11/173,175, filed July 1, 2005, now U.S. Patent No. 7,289,386 (the '386 patent) (EX1008), which is a continuation-in-part of application No. 11/075,395, filed March 7, 2005, now U.S. Patent No. 7,286,436 (the '436 patent) (EX1009). EX1001. I understand that in connection with Ground 3, Petitioner argues that Ellsberry (filed on June 1, 2005) is prior art to the '912 patent because none of the three provisional applications and the '436 patent provide sufficient disclosure to support certain claim elements. For the reasons that follow, I disagree.[2]

1. The '244 Provisional (EX1005)

37. The '244 provisional discloses a memory module comprising DRAM devices arranged in a rank and a memory module decoder that is configured to simulate a memory module with a smaller number of ranks (e.g.,

[2] For purposes of this declaration, I have been asked to only render an opinion on Petitioner's arguments regarding the '244 provisional and '436 patent.

two logical ranks) than the module actually has (e.g., four physical ranks). EX1005, [0001]-[0002], [0005]-[0008], [0024]-[0025]. The decoder comprises an ASIC (blue) that "decodes two chip-select signals and one control signal (such as an address signal) and converts them into four chip-select signals." *Id.*, [0005]. The decoder also receives certain control signals, e.g. command signals that "include, but are not limited to, activation read, write, precharge, and refresh." *Id.*, [0019].



38. With respect to certain four-rank memory module embodiments, "the ASIC uses one additional address signal (A_{n+1}) and at least one control signal. Exemplary control signals compatible with embodiments described herein control functions including, but are not limited to, refresh, precharge, and

other operations used for the proper functioning of the memory module." *Id.* [0010]; *see also id.*, [0025] ("The decoder is configured to receive input signals comprising a first number of chip-select signals and at least one control signal and to convert the input signals into output signals, the output signals comprising a second number of chip-select signals and to pass the output signals to the first number of ranks, the second number of chip-select signals being greater than or equal to the first number of chip-select signals."); Figure 1 (reproduced above).

39. I agree with Petitioner that the "ASIC Decoder" of the '244 provisional corresponds to a "logic element." Pet., 63; EX1003, ¶189. However, I disagree with the Petitioner's characterization of the '244 provisional as containing "no disclosure [the ASIC Decoder] receives any 'bank address' signals." Pet., 63.

40. Specifically, a person of ordinary skill would understand, per the JEDEC DRAM standards of the day, that the "control signals" for the certain memory operations—such as READ/WRITE—received by the decoder ASIC (blue) would include bank address signals. Under Petitioner's proposed level of skill in the art, a person of ordinary skill in the art at the time of the '912 patent

"would have been knowledgeable about the JEDEC DDR (EX1030, EX1031) and DDR2 (EX1029, EX1039) SDRAM standards." Pet., 6.

41. According to the JEDEC standards, performing certain commands such as Bank Activation, Write, and Read necessarily requires bank address signals as part of the command code. For example, JESD79-2 provides that bank address inputs "BA0-BA2 define to which bank an Active, Read, Write or Precharge command is being applied." EX1029, 6 (reproduced below). The Command Truth Table of JESD79-2 also indicates that "Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated on." *Id.*, 49 n.2 (reproduced below, both as-truncated in the Petition and in full). Likewise, JESD79 provides that "Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied." EX1030, 7.

1.2 Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, and DM signal for x4x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (UDM), (LDM)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/$\overline{RDQS}$ is enabled by EMRS command.
BA0 - BA2	Input	**Bank Address Inputs:** BA0 and BA1 for 256 and 512Mb, BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A15	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands.

(EX1029, 6)

Table 10 — Command truth table.

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.
NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

Pet. 45-46 (truncated truth table of JESD 79-2, EX1029, 49)

Table 10 — Command truth table.

Function	CKE Previous Cycle	CKE Current Cycle	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1,2
Refresh (REF)	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1,7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.

NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

NOTE 3 Burst reads or writes at BL=4 cannot be terminated or interrupted. See sections "Reads interrupted by a Read" and "Writes interrupted by a Write" in section 2.2.4 for details.

NOTE 4 The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined in section 2.2.7.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See section 2.2.2.4.

NOTE 6 "X" means "H or L (but a defined logic level)".

NOTE 7 Self refresh exit is asynchronous.

EX1029, 49 (complete truth table)

42. I note that this evidence is cited by the Petition itself. Pet., 45-49. In fact, citing to the command truth table of JESD79-2, Petitioner states that "to perform a read or write operation, the JEDEC standard … first requires ***a Bank Activate command with*** the row and ***bank address signals***, followed by ***a read or write command with the corresponding bank address signals***." Pet., 45 (citing EX1029, 49 n.2). The Petition also relies on the JEDEC standard to argue that Perego-422 discloses receiving "bank address signals" by a logic element. Pet., 36-37 ("A POSITA would have understood that, for DDR memory devices, the 'address lines' (and address information") labeled RQ in Perego … convey both row/column, and bank, addresses, per the JEDEC standard.") (citing EX1029 and EX1032).

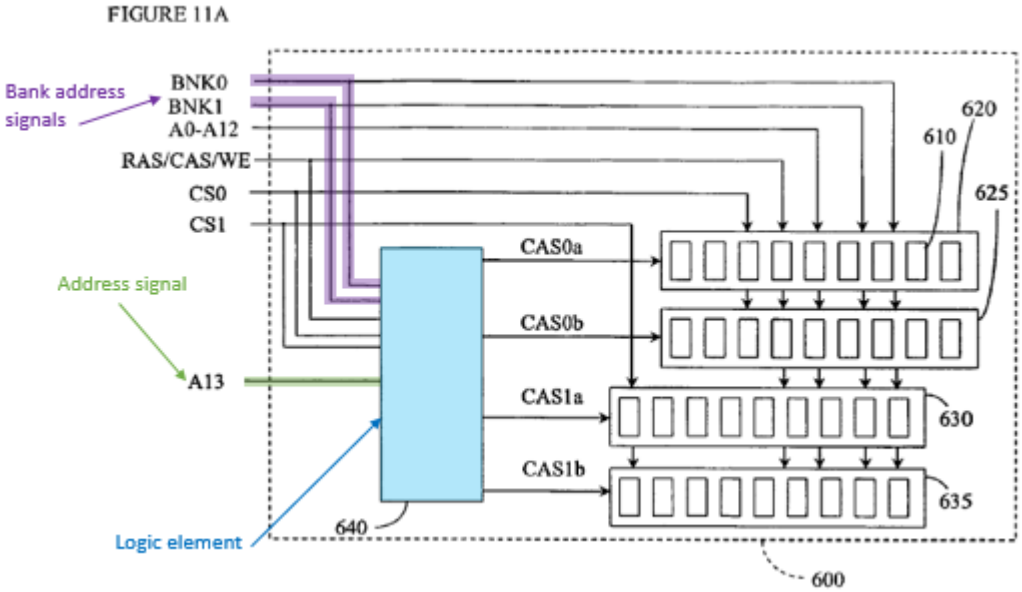
43. Accordingly, a person of ordinary skill in the art would have understood that the '244 provisional disclosed a "logic element" receiving "bank address signals" as such signals were part of the control signals received for read, write, and precharge. Thus, based on the '244 provisional's disclosure and the purported knowledge of a person of ordinary skill in the art (specifically, the above JEDEC standards), a person of ordinary skill in the art would have

understood that the inventors were in possession of the concept that bank address signals were received by the logic element. *See supra*, ¶¶37-42.

2. The ’436 Patent (EX1009)

44. The ’436 patent discloses increasing the memory capacity or memory density of a memory module by implementing a logic element that performs operations on certain input signals. EX1009, 3:5-38; 17:30-18:11. Figure 11A illustrates an embodiment featuring a four-rank memory module with a logic element 640 (blue) which receives a first set of address and control signals, including at least bank address signals BNK0 and BNK1, address signal A13, and command signals such as RAS/CAS/WE, CS0 and CS1 (chip select 0 and 1). The ’436 patent explains that “[t]o access the additional memory density of the high-density memory module 600, the two chip-select signals (CS0, CS1) are used with other address and control signals to gate a set of four gated CAS signals.” *Id.*, 17:31-34; *see also id.*, 17:34-39 (“For example, to access the additional ranks of four-rank 1-GB 128M 8-byte DDR1 DRAM memory module, the CS0 and CS1 signals along with the other address and control

signals are used to gate the CAS signal appropriately, as schematically illustrated by FIG. 11A.”).



45. As depicted in Figure 11A above, the logic element (blue) “receives a first set of address and control signals,” including bank address signals (BNK0-1, purple), address signal A13, and chip-select signals CS0-CS1, and “translates the first set of address and control signals into a second set of address and control signals which is compatible with the first plurality of memory locations of the memory module 600 and which is transmitted to the first rank 620, the second rank 625, the third rank 630, and the fourth rank 635.” *Id.*, 16:57-17:10. The

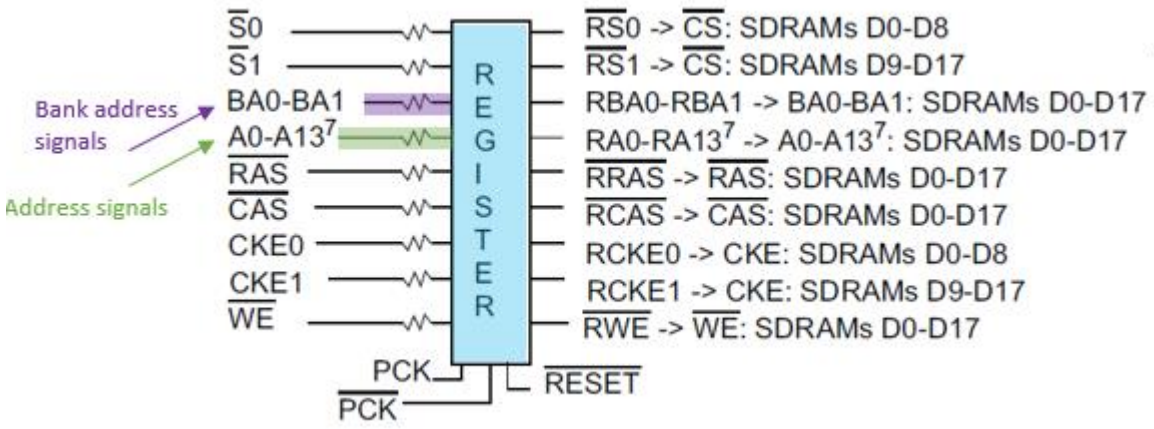
’436 patent further explains that, in certain embodiments, the logic element comprises a programmable logic device “PLD,” where “the PLD uses sequential and combinatorial logic procedures to produce the gated CAS signals,” each transmitted to one of the corresponding four ranks, or in other embodiments, “the PLD 642 instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS0a, CS0b, CS1a, and CS1b),” each transmitted to one of the corresponding four ranks. *Id.*, 17:41-43, 18:3-11. The ’436 patent expressly provides that the PLD can “comprise[] an ASIC, an FPGA, a custom-designed semiconductor device, or a CPLD.” *Id.*, 17:46-48; *see also id.*, 16:6-15 (similar disclosure for embodiment depicted in Figures 10A-10B). Specific examples of PLDs include those made by Altera or Xilinx. *Id.*, 17:48-52. In addition to the embodiment in Figures 11A-11B, the ’436 patent also illustrates a similar embodiment in Figures 10A-10B. *Id.*, 14:66-16:56.

46. I understand Petitioner makes three arguments regarding the adequacy of the ’436 patent’s disclosure. I address each in turn.

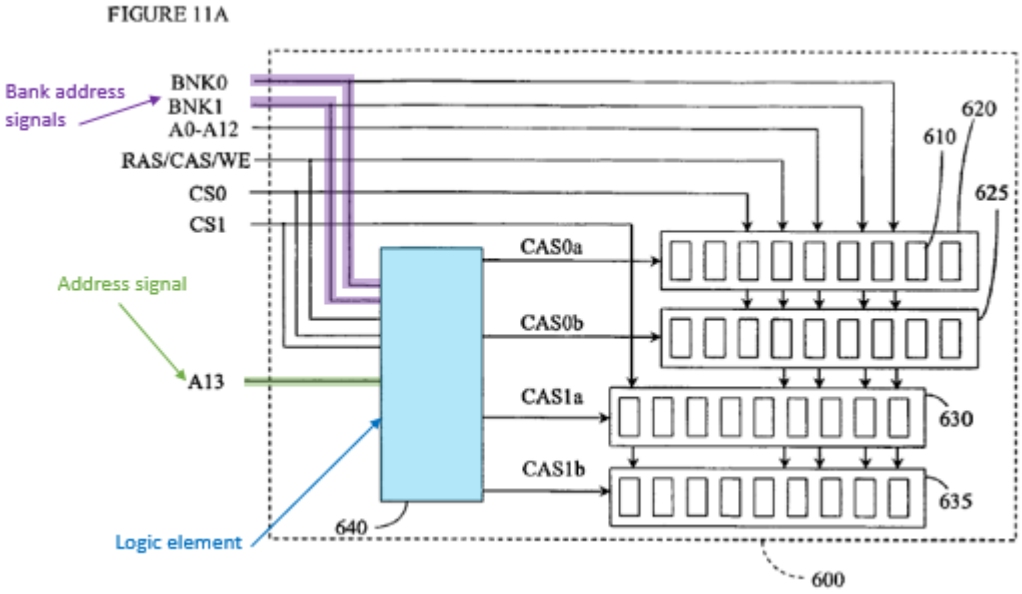
a) Alleged Absence of the "Circuit"

47. Petitioner's first argument is that the '436 patent "lack[s] any embodiment including 'a circuit' comprising 'a logic element' and 'a register' as ... shown in Figure 1A of the 912 Patent." Pet., 64. I disagree for the reasons that follow.

48. The '436 patent expressly discloses embodiments featuring registered DIMMs, which are commonly understood to be memory modules with a register between a computer system's memory controller and the DRAM devices on the module. EX1009, 7:22-28 ("[M]emory modules 100 compatible with embodiments described herein include, but are not limited to, ... registered DIMMs (RDIMMs)."). The JEDEC design specification for DDR RDIMMs, JEDEC No. 21C, which Samsung alleges to be part of the knowledge possessed by a person of ordinary skill in the art, schematically depicts a register, for example, for a x72 RDIMM. *See, e.g.*, EX1032, 4.20.4-10 to 4.20.4-16 (example below).



(EX1032, 4.20.4-12)



(EX1009, Fig. 11A)

49. I note that several of the signals entering the "REGISTER" function block above are also depicted as entering logic element 640 in Figure 11A of the '436 patent, including two bank address signals (BA0, BA1 in the figure from JEDEC No. 21C, BNK0, BNK1 in Figure 11A from the '436 patent), address signal A13, and two chip-select signals (S0/S1 in the figure from JEDEC No. 21C, CS0 and CS1 in Figure 11A from the '436 patent), indicating that the "register" and "logic element" are part of the same component illustrated in the "REGISTER" function block in JEDEC No. 21C.

50. Moreover, a person of ordinary skill in the art would understand the "REGISTER" function block in an RDIMM would include both logic elements for data processing and a register for storing data bits because (1) translating the input bits to output registered bits would involve the use of logic elements to process the input bits; and (2) the description of the functional block as a "register" would indicate to a person of ordinary skill in the art that the block included register functionality. I also understand that during reexamination, the Board also found that "registers [for an RDIMM] perform some type of logic function or comprise a logic circuit." EX1011, 19.

51. The exemplary logic elements disclosed by the ’436 patent include various PLDs such as ASICs, FPGAs, and CPLDs. EX1009, 16:12-20, 17:46-52. A person of ordinary skill in the art would have understood that integrated devices such as ASICs, FPGAs, and CPLDs include both logic elements (*e.g.*, for performing logical operations) and registers (*e.g.*, for storing, buffering, and/or transmitting signals). This is consistent with the Board’s findings in the ’912 reexamination, in which, in referring to identical disclosure in the ’912 patent during reexamination, the Board observed that “the expansive examples in the ’912 patent of a logic element cover custom devices or a device of various discrete electrical components, which includes at least some types of registers.” EX1011, 19; *see also id.*, 17 (“The ’912 patent states that logic element 40 in certain embodiments can be a PLD, an ... (ASIC), ... (FPGA), or a ... (CPLD).”). Moreover, the ’436 patent specifically mentions Xilinx PLDs as an example of the claimed logic element. EX1009, 16:16-20, 17:48-50. One example of a Xilinx PLD suitable for memory applications is the Xilinx FPGA depicted below, which features a logic elements and a register:

XILINX SOLUTIONS

FIGURE 2-4: SPARTAN-3 FEATURES

The Spartan-3 FPGA memory architecture provides the optimal granularity and efficient area utilization.

Shift register SRL16 blocks

- Each CLB LUT works as a 16-bit fast, compact shift register
- Cascade LUTs to build longer shift registers
- Implement pipeline registers and buffers for video or wireless

EX2031, 27.

52. Likewise, with respect to certain embodiments shown in Figures 10A-10B, the '436 patent expressly discloses a "logic element 540" that includes a programmable-logic device PLD 542. The PLD 542 would "save[] or latch[] the A13 address" during a row access for use as "an extra column address" in the subsequent column access. EX1009, 16:27-45. A person of ordinary skill in the art would have understood that the PLD includes registers to latch the

received address signal A13, and thus that the logic element 540 includes both the logic element and the "register" element for storing extra address bits.

53. Thus, a person of ordinary skill in the art would have understood that the '436 discloses a circuit comprising a logic element and a register.

b) Alleged Absence of Using "Row" and/or "Bank Address" Signals

54. Petitioner's second argument is that the '436 "lack[s] any Verilog code showing the use of 'row' and/or 'bank address signals'" such as Examples 1 and 2 of the '912 patent. Pet., 64; EX1003, ¶190 (Dr. Wolfe asserting that the '436 patent lacks "any Verilog code showing the use of the row address and/or bank address signals for rank multiplication"). I disagree for the reasons that follow.

55. I note that claim 16 only requires "the circuit generating a set of output signals ***in response*** to the set of input signals" that include row and bank address signals. This is disclosed, for example, in Figure 11B from the '436 patent, which shows four gated CAS signals generated in response to the set of input signals that include both row address signal A13 and bank address signals

BNK0/1. *See also* EX1009, Fig. 10B (logic element 540 outputting rank selection signals in response to input signals that include bank address signals and row address signal A13).

56. Moreover, the '436 patent explains that "[t]o access the additional memory density of the high-density memory module 600, the two chip-select signals (CS0, CS1) ***are used with other address and control signals*** to gate a set of four CAS signals." EX1009, 17:30-34. "For example, to access the additional ranks of four-rank 1-GB 128M 8-byte DDR1 DRAM memory module, the CS0 and CS1 signals along with the other address and control signals are used to gate the CAS signal appropriately, as schematically illustrated by FIG. 11A." *Id.*, 17:34-39.

57. As seen in the annotated figure above, the logic element (blue) receives both address signal (A13) and bank address signals (BNK0-1), and in response to A13, BNK0-1, as well as command signals CS0, CS1, RAS/CAS/WE, the logic element outputs four gated CAS signals. *Id.*, 17:31-34, 18:6-9, Fig. 11A; EX1029, 49 ("All DDR2 SDRAM commands are defined by states of CS, RAS, CAS, WE and CKE at the rising edge of the clock.").

Thus, a person of ordinary skill in the art would therefore necessarily understand from Figure 11A that the "other address … signals" used by the '436 patent to "gate a set of four CAS signals" or generate four chip-select signals include the row address A13 and the bank addresses BNK0 and BNK1. EX1009, 17:31-34, 18:6-9.

58. Additionally, as previously discussed, a person of ordinary skill in the art would know that a bank address signal (e.g. BNK0 or BNK1) would be used, for example, to select the targeted memory bank for a command, per the DDR standards. EX1009, 12:48-52 ("'JEDEC standard JESD79D, [DDR] SDRAM Specification," … [is] incorporated in its entirety by reference herein"); EX1029, 6 ("BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied."), 49 (Command truth table, and Note 2: "Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon"); *supra*, ¶¶37-42.

59. I also note that Petitioner asserts in the Petition that Perego-422 inherently discloses a logic element that receives a row address and bank address signals per the JEDEC standard. Pet., 36-37; Pet. 44-45 ("[T]o perform a read

or write operation, the JEDEC standard (shown below) first requires a Bank Activate command with the row and bank address signals, followed by a read or write command with the corresponding bank address signals…. Thus, a person of ordinary skill in the art would have understood that the target memory device and its target memory bank ***is selected in accordance with the bank address signals*** of the read or write command and ***the previously received row address and bank address signals*** of the activate command.”).

60. Under the same logic that Petitioner has applied, a person of ordinary skill in the art would have understood that the ’436 discloses a circuit using a row and bank address signal.

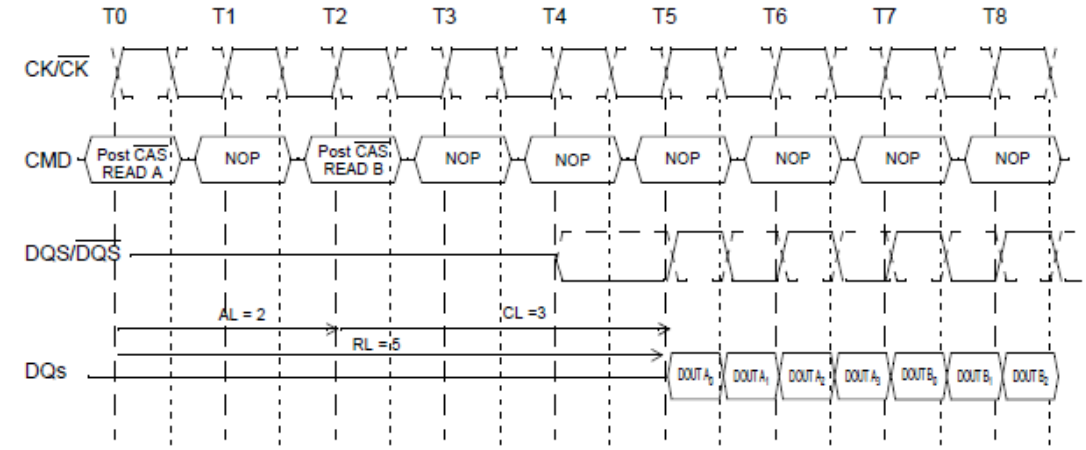
c) Alleged Non-Enablement of the ’436 Invention

61. Petitioner’s third argument is that the ’436 patent fails to disclose any solution to the problem of executing a “standard” back-to-back read command which cross memory device boundaries (“BBARX”), and thus the disclosure of the ’436 patent does not adequately support claim 16. Pet. 65-68. Petitioner contends that material added in the July 1, 2005 application that issued as the ’386 patent is necessary to support claim 16. *Id.*, 66. As the ’386 patent

explains, a BBARX (*i.e.*, across memory device "a" in Rank0 and memory device "b" in Rank1) may result in collisions when "the last data strobe of memory device 'a' collides with the pre-amble time interval of the data strobe of memory device 'b.'" EX1008, 24:16-30. One solution to this problem is to "insert wait time intervals or clock cycles to avoid collisions or interference between [BBARX]," but in the context of rank multiplication, the memory controller is unaware of the physical boundaries of the memory devices on a rank. *Id.*, 24:15-30.

62. As an initial matter, Petitioner cites to various commands that were a part of the JEDEC standards of the day to argue that BBARX were "part of the normal operation of memory modules at the time." Pet., 66. Petitioner cites to the "seamless burst read operation" for DDR2 memories (EX1029, Fig. 27), as one such example. *Id.* JESD 79-2 explains that a "[b]urst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle)." EX1029, 25. As illustrated below, in a seamless burst operation, the memory controller issues two read commands (Read A, Read B) at T0 and T2, separated by a NOP, which is followed by four-

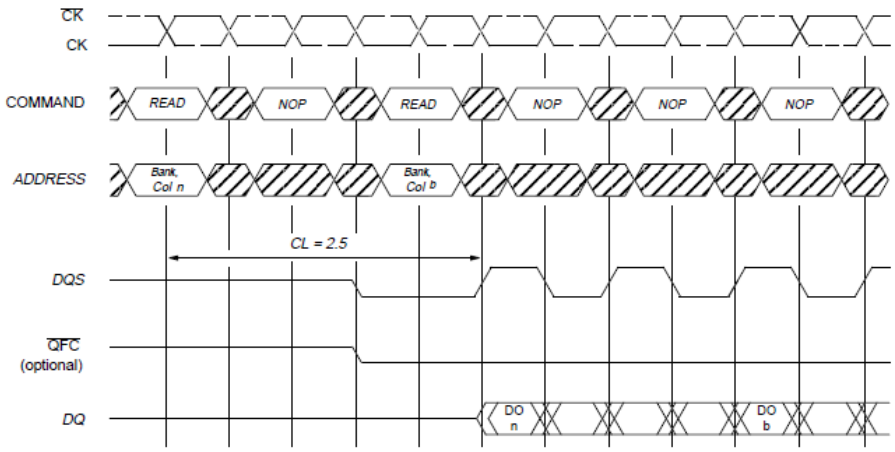
bit bursts of data starting at T5. *Id.*, 28. However, the timing issues that arise in the context of successive read bursts are different from a BBARX because there is only a single DQS preamble for the same read operation by the same memory device and there is no DQS collision window. This is because the seamless burst command is bursting data to/from a single memory device via separate burst commands, via a single set of DQ and DQS lines whose signaling does not overlap simultaneously in time. In other words, the resultant DQ and DQS signaling for each of the READ A and READ B commands, as illustrated in the figure below, do not occur at the same point in time which could result in a collision.



The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 27 — Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

63. Nor do the DDR standards Petitioner cite feature BBARX. Petitioner's Figure 8 shows successive read commands to different columns *within* the same memory device, as confirmed by the description "Read commands shown must be to ***the same device***." EX1030, 19 (Figure 8, reproduced below).



DO n (or b) = Data Out from column n (or column b)
Burst Length = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
3 subsequent elements of Data Out appear in the programmed order following DO n
3 (or 7) subsequent elements of Data Out appear in the programmed order following DO b
Shown with nominal tDQSCK, and tDQSQ
Read commands shown must be to the same device

Figure 8
CONSECUTIVE READ BURSTS – REQUIRED CAS LATENCIES

64. Even if it was necessary for a memory system designer to find a solution to the BBARX issue, based on the ’436 patent disclosure and knowledge of the art, such a designer could overcome the supposed challenge of executing BBARX on a rank-multiplied module without undue experimentation. For example, a person of ordinary skill in the art could readily configure the memory controller in a memory system featuring the ’436 module to use appropriate timing sequences to avoid such collisions by inserting a delay between

successive read commands, without the need to know the physical boundaries of the memory devices. The memory designer could also use a serial presence detect (SPD) device to inform the memory controller of the physical boundaries of each memory device. A SPD device "store[s] the configuration information of the memory module on a read-only memory device whose content can be retrieved by the memory controller as part of the system initialization process," which allows the memory controller to "obtain the configuration and timing parameters required to optimally access data from DRAM devices on the memory module." EX1033, 421. By configuring a SPD device to inform the memory controller of the physical boundaries of the memory module, a person of ordinary skill in the art could insert delays where appropriate to avoid BBARX collisions.

V. CLAIM CONSTRUCTION

A. "Rank"

65. Petitioner and Dr. Wolfe contend that the term "rank" would be understood by a person of ordinary skill in the art to refer to "an independent set of one or more memory devices on a memory module that act together in

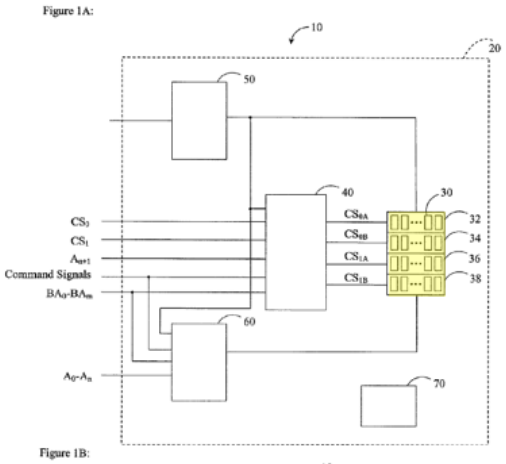
response to command signals, including chip select signals, to read or write the full bit- width of the memory module." Pet., 12; EX1003, ¶73. Petitioner also contends that "the term 'bank' was … used to refer to what is now typically called a 'rank.'" I agree with Petitioner that, in some contexts, the word "bank" was used to refer to what is now understood as a "rank" of memory devices. However, for the reasons that follow, I disagree with Petitioner's construction to the extent it allows for a single memory device to form a "rank."

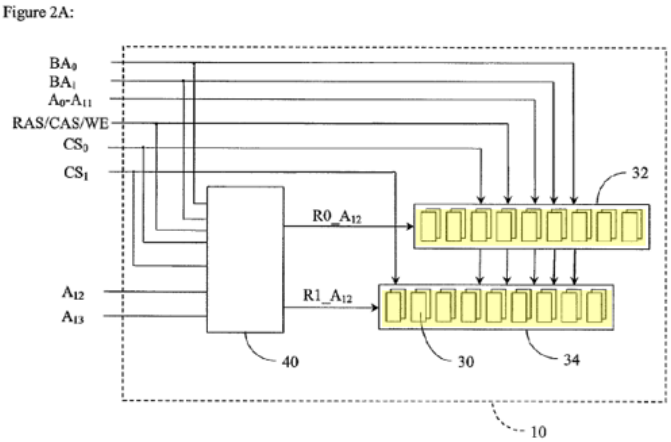
66. I understand that during reexamination, the Examiner allowed claim 16 by concluding that Amidi did not teach a person of ordinary skill in the art how to "transmit command signal to only one DDR memory device at a time ***when there is a plurality of memory devices in a rank***." EX1010, 3865-67; *supra*, ¶30. I understand that SM submitted comments challenging this claim construction, specifically arguing that Amidi rendered claim 16 obvious to the extent that claim 16 "requir[ed] only that the command signals are sent to a single rank ***because "one memory device" encompasses a rank of [one] memory***." EX1010, 4442; *see supra*, ¶31. In the subsequent Office action, the Examiner maintained the construction of claim 16. EX1010, 4828, 4830, 4702-

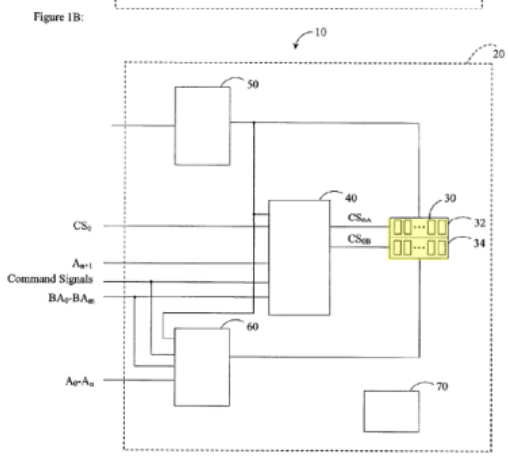
4, 4723-25; *see supra*, ¶32. The Board affirmed the Examiner's decision upholding the patentability of claim 16 because the claims require a plurality of memory devices in a rank and Amidi does not disclose addressing a single device within the plurality of devices that constitutes a rank. EX1011, 79-80; *see supra*, ¶33. I agree with the Examiner's and Board's construction because, as explained below, that construction comports with the intrinsic evidence, which consistently shows that a "rank" of memory devices includes more than one memory device.

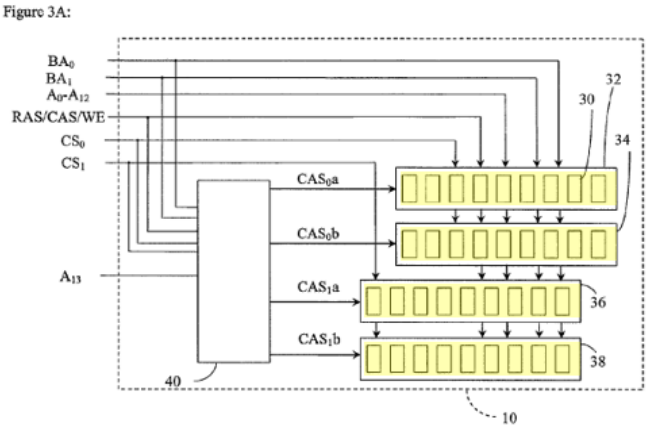
67. Additionally, I understand that in *Netlist Inc. v. Google LLC*, Case No. 3:09-cv-4718 (N.D. Cal.), Patent Owner and defendant Google LLC have agreed that the term "rank" as used in the '912 patent should be construed to mean "a group of memory devices enabled to receive and transmit data by a common chip-select signal." EX2026, 7. This is consistent with the Board's construction. I agree with the parties' construction in the Google Action because, as explained below, that construction comports with the intrinsic evidence, which consistently shows that a "rank" of memory devices includes more than one memory device.

68. The figures in the ’912 patent consistently show memory modules featuring multiple memory devices in each rank. *See id.*, Fig. 1A-B, 2A, 3A (reproduced below, with multi-device ranks highlighted).









69. The written description makes repeated and consistent references to ranks composed of multiple memory devices:

- "[I]n certain embodiments, two ranks of memory devices having a memory density are used to simulate ***a single rank of memory devices*** having twice the memory density…." *Id.*, 12:13-25.
- "Thus, in certain embodiments, even though the memory module 10 actually has the first number of ***ranks of memory devices*** 30, the memory module 10 simulates a virtual memory module by operating as having the second number of ***ranks of memory devices*** 30." *Id.*, 7:9-13.
- "[I]n certain embodiments, the ***memory devices*** 30 are arranged in four ranks, as schematically illustrated by FIG. 1A. In other embodiments, the ***memory devices*** 30 are arranged in two ranks, as schematically illustrated by FIG. 1B. Other numbers of ***ranks of the memory devices*** 30 are also compatible with embodiments described herein." *Id.*, 6:31-38.

See also id., 7:55-8:43, 8:64-9:18 (Tables 1 and 2 providing logic tables "for the selection among ***ranks of memory devices*** 30"); *id.*, 10:31-35 ("In certain embodiments, the SPD device 70 comprises data which characterize the memory module 10 as having fewer ***ranks of memory devices*** than the memory module 10 actually has, ….").

70. The specification also distinguishes embodiments directed to the simulation of a single high-density "memory device" as depicted in Figure 1C from embodiments directed to the simulation of "ranks" of memory devices. *Compare* EX1001, 12:12-15 (discussing emulating a single, high density memory device where "[i]n certain embodiments, ***two memory devices*** having a memory density are used to simulate a ***single memory device*** having twice the memory density") *with id.*, 12:15-21 ("[I]n certain embodiments, two ***ranks of memory devices*** having a memory density are used to simulate ***a single rank of memory devices*** having twice the memory density").

71. I understand that Petitioner relies upon the following passage from the '912 patent to support its interpretation that a "rank" of memory devices encompasses a single memory device:

> In certain embodiments, the command signal is passed through to the selected rank only (**e.g., state 4 of Table 1**). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e**.g., state 6 of Table 1**). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time.

EX1001, 8:50-58 (quoted at Pet. 13-14).

72. Table 1 is a logic diagram "for the selection among ***ranks of memory devices*** using chip-select signals," indicating that the description that follows refers to ranks of multiple memory devices. *Id.*, 7:56-8:10.

Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using chip-select signals.

TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:

1. CS_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

73. In state 4 above, the rank corresponding to CS_{1A} is chosen. *Id.*, 8:29-32 ("In Logic State 4: CS_1 is active low, A_{n+1}, is non-active, and Command is active. CS_{1A} is pulled low, thereby selecting Rank 2."). Based on the description of Table 1 above, state 4 is referring to transmitting a command signal to a rank with ***multiple memory devices***, in this example, a rank of two memory devices, such that "the command signal (e.g., read) is sent to only one memory device or the other memory device" in the same rank "so that data is

supplied from one memory device at a time." *Id.*, 8:50-54. Read in context, the embodiments described with reference to Table 1 refer to transmitting a command signal to one of multiple memory devices in the selected rank, *e.g.*, one of ***two memory devices*** in a ***two-device rank***.

74. A construction of "rank" that requires more than one memory device is also consistent with Petitioner's evidence. For example, Petitioner cites EX1033 (Memory Systems Textbook), which states that: "[T]he word *rank* is now used to denote ***a set of DRAM devices that operate in lockstep*** to respond to a given command in a memory system." EX1033, at 413; *see also id.*, 421 ("Table 10.1 shows that a DRAM memory module can be organized as multiple ranks of DRAM devices on the same memory module, ***with each rank consisting of multiple DRAM devices***, and the memory module can have differing numbers of rows and columns."). But for a "set of DRAM devices" to "operate in lockstep" together (e.g., in response to a read command), there must necessarily be more than one memory device. In other words, the reference to "operat[ing] in lockstep" makes no sense in the context of a single-device rank,

because in such a rank, there would be no other DRAM devices that operate "in lockstep" in response to a command.

VI. OVERVIEW OF THE REFERENCES

75. I provide the following brief overview of each reference cited in the Petition.

A. Perego-422

76. U.S. Patent No. 7,363,422 to Perego ("Perego-422") was filed January 28, 2004, and issued as a patent on April 22, 2008. EX1035. While Perego-422 was not considered during the prosecution of the '912 patent, I note that a related patent, U.S. Patent No. 7,356,639 to Perego ("Perego-639") was disclosed by Patent Owner in an Information Disclosure Statement dated June 19, 2009, and considered by the Examiner. *See* EX1002, 125, 523.

77. Perego-422 discloses a memory system architecture with point-to-point topology which includes buffered modules having a configurable width buffer device. EX1035, Abstract; 5:35-55, 8:10-17, 8:20-26. In Perego-422's memory system 305, depicted below, buffered modules 330a-330n include a configurable-width data buffer (red) that receives signals from the memory

controller via point-to-point links 320a-n. *Id.*, 5:64-6:3, 6:12-18. The buffer device communicates to the plurality of memory devices on the buffered module via channels 370. *Id.*, 5:4-6, 6:18-24. Perego-422 provides that these channels "may be subdivided into several addressable subsets," and discloses an embodiment wherein "the target subset of secondary channel signal lines may be selected via address bits provided as part of the primary channel request" from the memory controller. *Id.*, 14:62-65, 15:31-40. Perego-422 explains that one purported benefit of accessing a subset of secondary channel signal lines per transaction is that this allows "grouping memory devices into multiple independent target subsets (i.e. more independent banks)." *Id.*, 15:40-45.

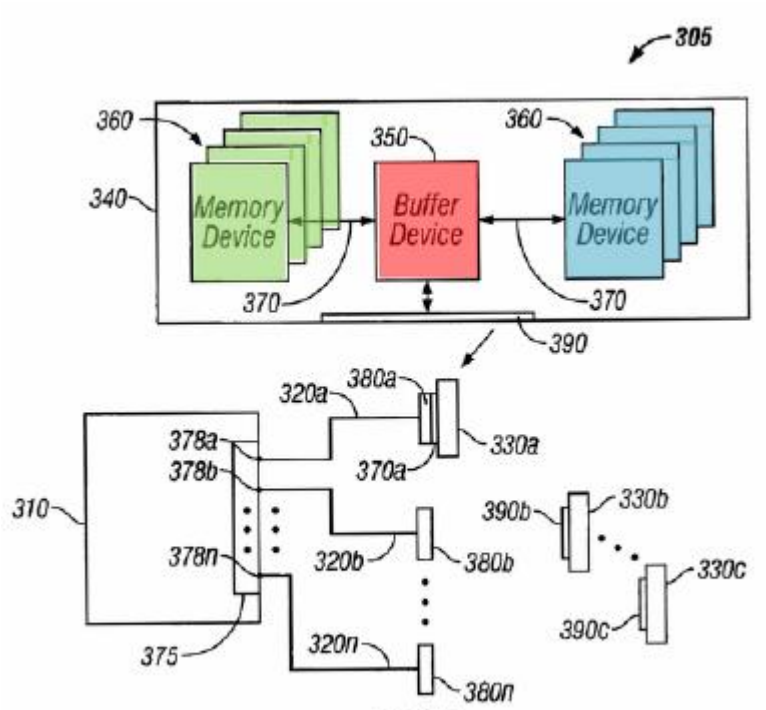


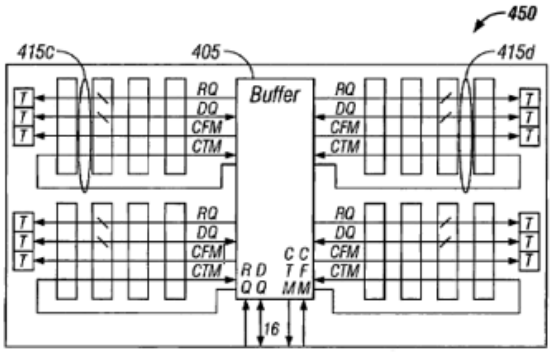
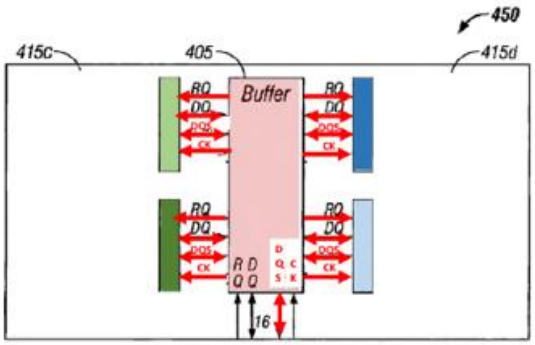
FIG. 3B

78. Figures 4A-4C depict buffered memory modules according to embodiments of Perego-422's invention. *Id.*, 9:26-33. I understand that Petitioner relies on a modified version of Perego-422's Figure 4B, *see, e.g.*, Pet. 62. In Petitioner's modified version of Figure 4B, the buffered module of Perego-422 features four single-device ranks with one x16 memory device in each rank. Pet. 41-42. I understand that Petitioner contends that each of the memory devices has its own "dedicated" channel, and thus the four channels

correspond to the claimed "first number of ranks." Pet. 30; EX1003, ¶124 (Dr. Wolfe modifying Fig. 4B such that "each of channels 415a-d is coupled to a single respective DDR memory device").

79. For context, the original Figure 4B of Perego-422 shows a memory module with multiple memory devices (*e.g.*, 32) that communicate with the data buffer via four channels (415a-415d). *Id.*, 9:26-33, 10:22-36, Fig. 4B (reproduced below side-by-side with Petitioner's modified version of Figure 4B). Perego-422 explains that these channels may operate in pairs or simultaneously. *Id.*, 10:22-36. In the paired arrangement, "channels 415c and 415d are ***routed in parallel*** with channels 415a and 415b." *Id.*, 10:24-25. In the simultaneous arrangement, "channels 415a and 415b may operate ***simultaneously*** with channels 415c and 415d." *Id.*, 10:32-33. For the paired arrangement, a person of ordinary skill in the art would regard the memory devices in channels 415a and 415b as belonging to a single rank because they operate together in response to a command, and similarly the memory devices in channels 415c and 415d as belonging to a single rank because they operate together in response to a command. Similarly, when all four channels operate

simultaneously, a person of ordinary skill in the art would regard all memory devices in the four channels as belonging to a single rank because of their "togetherness." In other words, neither arrangement is compatible with Petitioner's single-device rank construct based on Figure 4B. *See infra*, VII.B.

 FIG. 4B EX1035, Fig. 4B	 FIG. 4B Pet., 62 (modified Figure 4B)

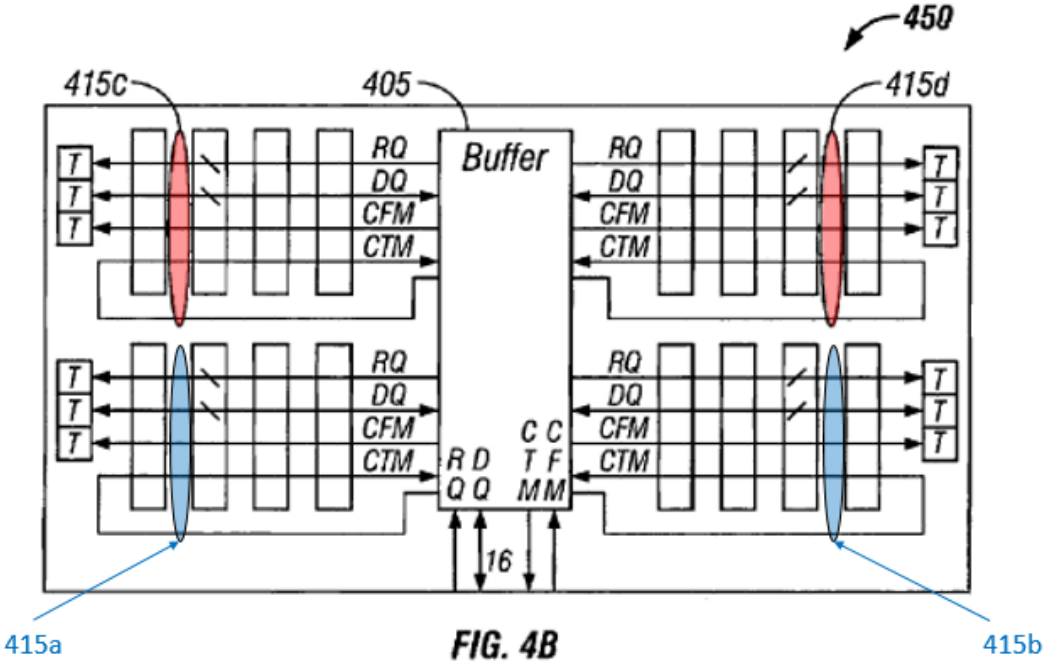


FIG. 4B

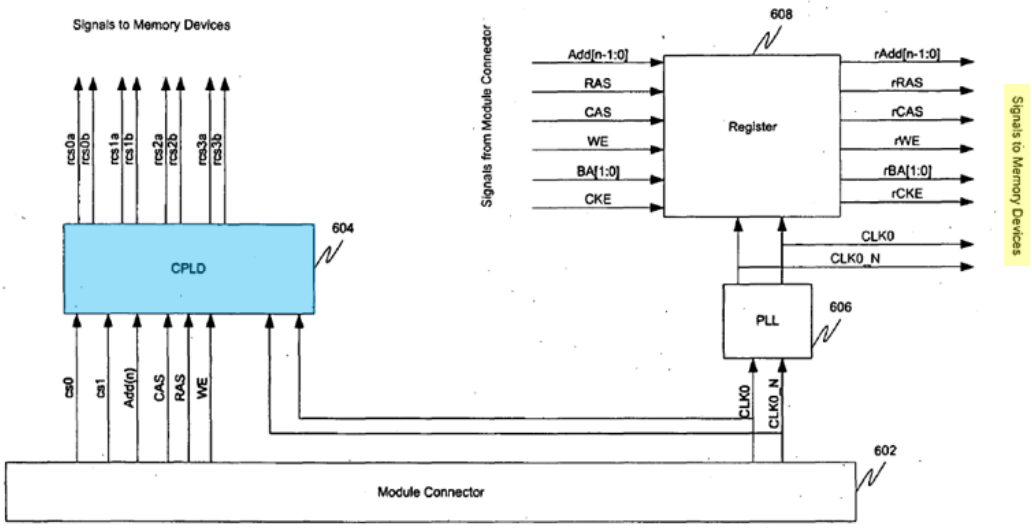
EX1035, Fig. 4B (annotated to show four channels 415a-d).

B. Amidi

80. U.S. Patent Application Publication No. 2006/0117152 to Amidi et al. ("Amidi") was filed on January 5, 2004 and published on June 1, 2006. EX1036.

81. Amidi discloses a four-rank "transparent" memory module which emulates a memory module with two ranks in order to "fit[] into a memory socket having two chip select signals routed." EX1036, Abstract [0011]. Figure

6A illustrates Amidi's four-rank memory module, which features a CPLD that receives as input two chip-select signals (cs0/cs1), Add(n), and commands (*e.g.*, RAS/CAS/WE) and "generates rcs2 and rcs3, besides rcs0 and rcs1 off of CS0, CS1 and Add(n) from the memory controller side." *Id.*, [0050]-[0051].



Row Address Decoding
FIG.6A

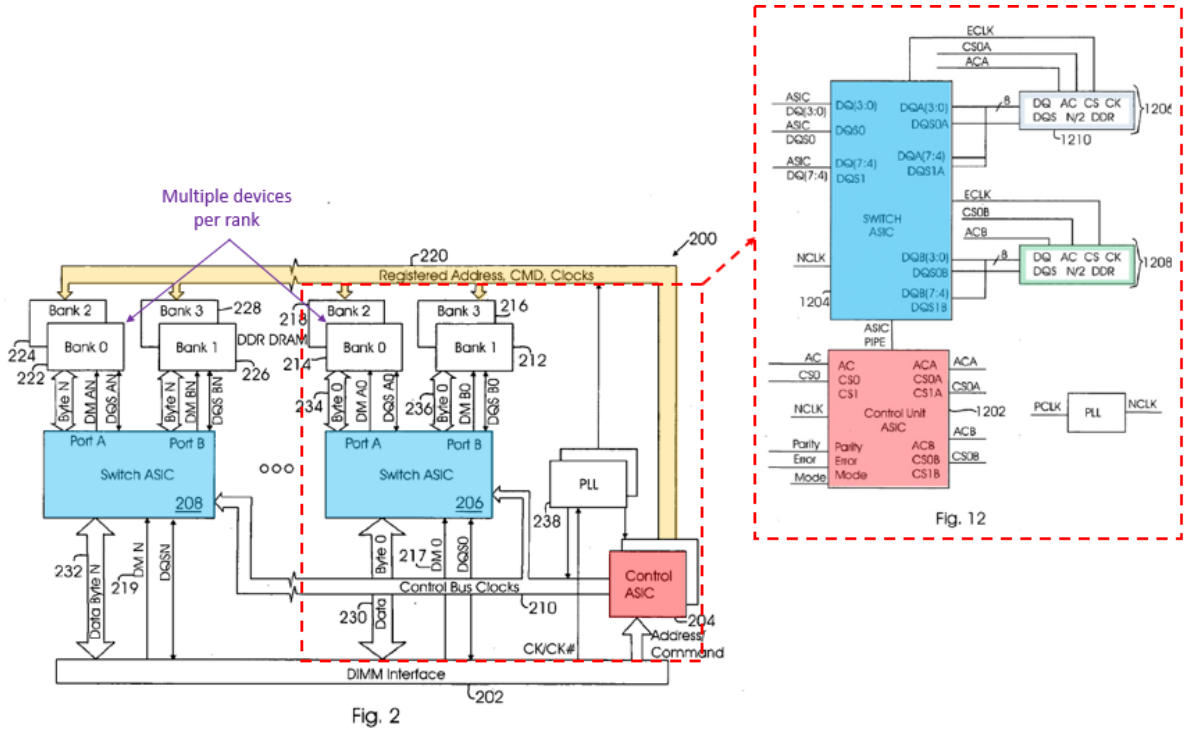
82. As summarized above, Amidi was considered extensively throughout the '912 reexamination. *See supra*, IV.B. The Examiner concluded that Amidi's RAS and CAS signals ("command signals") were not transmitted to only one DDR memory device on the selected rank, as required by the claims.

EX1010, 3865-67, 3904. The Board later affirmed this finding, emphasizing the Examiner's conclusion that "Requester has not provided a reasonable explanation as to why one skilled in the art would transmit a command signal to ***only one DDR memory device at a time when there is a plurality of memory devices in a rank***." EX1011, 79. The Board explained that Figures 6A and 6B of Amidi "show[ed] various command signals [] being transmitted to more than one memory device," as evidenced by the label "Signals to Memory ***Devices***" on those figures. *Id.*

C. Ellsberry

83. U.S. Patent Application Publication No. 2006/0277355 (EX1037) ("Ellsberry") was filed on June 1, 2005. Ellsberry was cited by the Examiner during prosecution of the '912 patent, but was not considered as prior art because "the Examiner … assumed Ellsberry was not prior art." Pet., 112; EX1002, 510. As discussed above, I agree with the Examiner that Ellsberry is not prior art to the '912 patent, which claims priority to, *inter alia*, the '244 provisional and the '436 patent. *See supra,* IV.C.

84. Ellsberry discloses a memory module architecture, depicted in Figure 2, that "permits transparent bank switching of memory devices." EX1037, [0001]. Control ASIC 204 (red) "receives memory addresses and commands over the DIMM interface 202" from the system memory controller, and switch ASICs 206 and 208 (blue) "receive data information from the DIMM interface 202 via data buses 230 & 232, respectively." *Id.*, [0028]-[0029]. Each switch ASIC is connected to a number of memory banks (e.g., Bank 0-3 below), each with one or more memory devices. *Id.* Switch ASICs 206 and 208 receive respectively data byte group N and data byte group 0, provided "simultaneously" by the DIMM interface 202. *Id.*, [0030], Fig. 2 (depicting at least two data groups); Fig. 5 (depicting nine data groups). As explained in greater detail below in Section VII.C, Figures 10-13 illustrate parts of Ellsberry's overall memory module architecture depicted in Figure 2. *See id.*, Figs. 2 and 12 (reproduced below, annotated); EX1038, 50 (Board noting that "Figure 13 shows ***part of a memory module***"), 51, 57, 77, 81; EX2032, 40 n.11.



85. Control ASIC 204 sends command signals to memory devices in different memory banks via bus 220. *Id.*, [0030]. Each switch ASIC includes two data ports, Port A and Port B, coupled respectively to data busses 234 and 236. One method Ellsberry discloses for sending commands to selected banks is the use of a row/bank addressing scheme to send commands to an intended bank, while sending NOP commands to the other bank. *Id.*, [0042] ("Row/Bank addressing is used, then a READAP command is sent to the intended bank while

a NOP command is sent to the other bank."). I note that Petitioner's analysis only relies on Ellsberry's row/bank addressing mode. *See* Pet., 100-101, 109-110.

VII. ANALYSIS OF THE PETITION'S GROUNDS

86. I understand Petitioner asserts three grounds to challenge claim 16 of the '912 patent:

Ground	Claim challenged	35 U.S.C. §	References
1	16	103(a)	Perego
2	16	103(a)	Perego, Amidi
3	16	103(a)	Ellsberry

A. Grounds 1 and 2: Petitioner's Combination of Perego and Amidi Does Not Disclose [16.b.i]/[16.c.ii]

87. Claim 16 requires a "plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ***ranks***," and "a second number of DDR memory devices arranged in a second number of ***ranks***." EX1001, p. 44, 3:9-43. As discussed above, in the context of the '912 patent, a "rank" comprises more than one memory device. *See supra*, V. By contrast, both Grounds 1 and 2 of the Petition rest on hypothetical constructs

featuring single-device ranks, with one memory device corresponding to each of the four channels in Perego-422's Figure 4B. Pet., 28-43; *supra*, ¶¶78-79.

88. As a preliminary matter, I note that Petitioner has not shown that each channel constitutes a rank even under Petitioner's own definition of "rank," because it has not shown that any of Perego-422's memory devices "***act together*** in response to command signals." *E.g.*, Pet., 28-29. *See infra*, ¶¶94-97.

89. Even if Perego-422 discloses the concept of organizing memory devices in "ranks," the Petition is admittedly limited to single-device ranks only. Petitioner's first example (Ground 1) features four x16 memory devices arranged in what it defines as four ranks ("first number of ranks"). Pet., 30 ("With respect to the 'number' of memory devices and ranks, Perego teaches an embodiment in which its module includes four memory devices arranged in four ranks, each rank having a single memory device with a 'dedicated channel,' as shown in Figure 4B below …."); *id.*, 39-41 (contending that "[a] POSITA would have understood that Perego's module could use x16 memory devices to upgrade a memory system configured for memory modules having [two] x8 memory devices" arranged in one rank (second number of ranks)). That is, Petitioner's

first example is concededly limited to a first number of single-device "ranks," not the claimed ranks, which comprise multiple devices. *See supra*, V.

90. Petitioner's second example (Ground 2) features four x16 memory devices arranged in what it defines as four ranks ("first number of ranks") that Petitioner contends can simulate a module with two x16 memory devices arranged in what it defines as two ranks ("second number of ranks") based on the combination of Perego-422 and Amidi. Pet., 42-43 ("In this second example, a POSITA would have been motivated to build Perego's 16-bit wide module with four x16 memory devices for a system where the memory controller can control only two ranks per module, as in Amidi."). As with Example 1, Petitioner's relied-upon construct is a module "where each rank has one x16 memory device." Pet., 42; *id*., 43 (modified Fig. 4B). As above, Petitioner's second example is concededly limited to a first number of single-device "ranks," not the claimed ranks, which comprise multiple devices. *See supra*, V.

91. Accordingly, the Petition's Ground 1 (Perego) and Ground 2 (Perego in view of Amidi) fail to disclose Elements [16.b.i]/[16.c.ii].

B. Grounds 1 and 2: Petitioner's Combination of Perego and Amidi Does Not Disclose [16.e.]

92. Claim 16 requires that "the command signal [be] transmitted to only one DDR memory device at a time." EX1001, p. 44, 3:42-43. Petitioner only asserts that the limitation is met if each rank has a single device. *See, e.g.*, Pet., 61-62 ("Perego discloses 'wherein the command signal [e.g., for a read or write command per the JEDEC standard, EX1029,6,49] is transmitted to only one DDR memory device at a time,' … in an implementation like the one illustrated below, where each memory device has a 'dedicated channel.'") and Fig. 4B (reproduced below as modified by Petitioner); *id.*, 62-63 ("Consequently, when the width of one memory device is equivalent to that of the module, the command received at a specific time is transmitted to only one DDR memory device at a time."). But as explained in Section V above, each "rank" is understood to have two or more memory devices; and claim 16 requires sending a command to a single device at a time even though there are multiple devices in each rank. For this reason alone, the Petition's Ground 1 (Perego) and Ground 2 (Perego in view of Amidi) fail to disclose Elements [16.e].

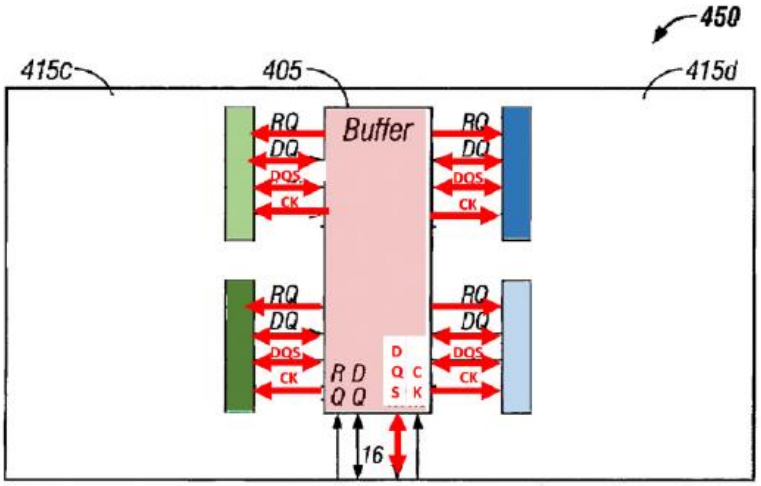


FIG. 4B

93. Even accepting for the sake of argument Petitioner's construction that a "rank" could theoretically be composed of a single memory device, I note that Perego-422 does not disclose a memory module with only a single device in each "rank." As noted above, Petitioner assumes that each channel in modified Figure 4B corresponds to a rank. *See* Pet., 61-62; EX1003, ¶124; *supra*, ¶78. That is not supported by Perego-422's specification. The buffer circuit in Figure 4B communicates with the memory devices via four channels 415a-415d, either in a paired arrangement (one pair, 415c/415d, another pair 415a/415b), or in a simultaneous arrangement (all four channels simultaneously). EX1035, 9:26-

33, 10:22-36. In the paired arrangement, "channels 415c and 415d are ***routed in parallel*** with channels 415a and 415b." *Id.*, 10:23-36. In the simultaneous arrangement, "channels 415a and 415b may operate ***simultaneously*** with channels 415c and 415d." *Id.*, 10:32-33.

94. Even under Petitioner's construction, neither of these arrangements allows for the possibility of single-device ranks. Petitioner contends that a person of ordinary skill in the art would understand the term "rank" to mean "an independent set of one or more memory devices on a memory module ***that act together in response to command signals***, including chip-select signals, to read or write the full bit-width of the memory module." Pet., 12. Perego-422 would inform a person of ordinary skill in the art that, in the paired arrangement, the devices connected to channels 415c/d correspond to one "rank" because they are "routed in parallel," that is, the memory devices would be understood to "act together in response to command signals." For similar reasons, a person of ordinary skill in the art would understand that the devices connected to channels 415a/b correspond to another "rank." Thus, in the paired arrangement, Perego-422's Figure 4B illustrates two ranks: one corresponding to memory devices

connected to channels 415c/d, the other corresponding to memory devices connected to channels 415a/b. Likewise, a person of ordinary skill in the art would understand that the simultaneous arrangement corresponds to a one-rank module, because all the memory devices connected to channels 415a-d "act together in response to command signals."

95. Applying these principles from Perego-422's express teachings to Petitioner's single-device construct, a person of ordinary skill in the art would understand Petitioner's modified Figure 4B to correspond to either a two-rank module, with ***two devices in each rank*** (paired-channel arrangement) or a one-rank module, with ***four devices in the rank*** (simultaneous-channel arrangement).

96. Petitioner does not assert that Perego-422 teaches a person of ordinary skill in the art how to transmit a command signal to one memory device at a time when each "rank" includes more than one channel of devices, and accordingly, the Petition's Ground 1 (Perego) and Ground 2 (Perego in view of Amidi) fail to disclose Elements [16.e].

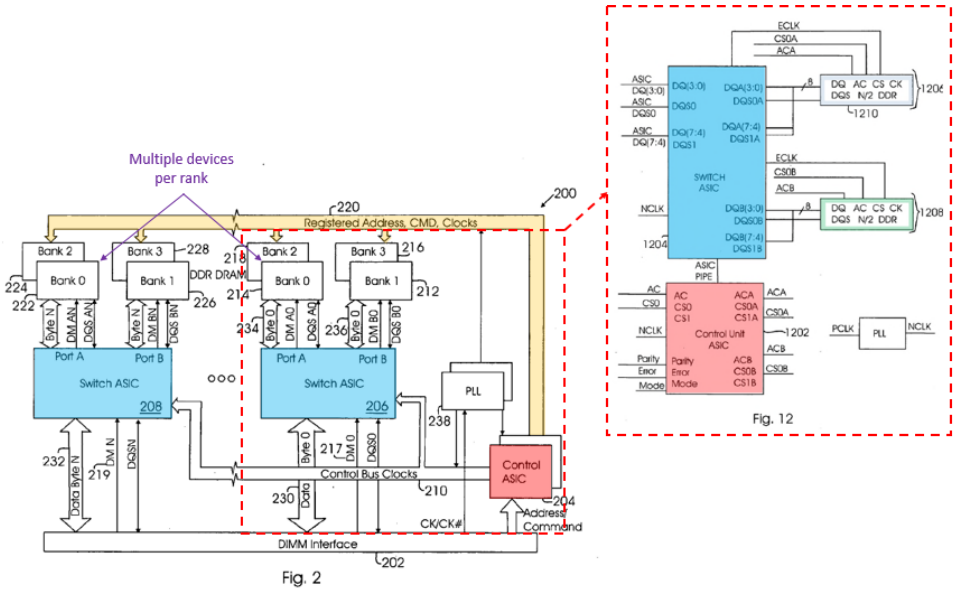
C. Ground 3: Ellsberry Does Not Disclose [16.e.]

97. Claim 16 recites "wherein the command signal is transmitted to only one DDR memory device at a time." EX1001, p. 44, 3:42-43; Element [16.e]. I understand that Petitioner contends that Ellsberry discloses transmitting a command signal to one DDR memory device at a time based on Ellsberry's alleged disclosure of a construct featuring single-device ranks where "an Activate, Write, or Read command signal is transmitted to only the selected memory device" and the other memory device "receives a no-operation (NOP) command." Pet., 109-10. Petitioner relies specifically on Figure 12 of Ellsberry, which Petitioner interprets as disclosing an 8-bit memory module with a single device per rank. *Id.*, 75-76. For the reasons stated below, I disagree with this interpretation.

98. First, as discussed above in Section V, in the context of the '912 patent, the term "rank," properly construed, excludes single-devices. *See also* EX1011, 79 (Board agreeing with the Examiner that Inphi had failed to demonstrate from Amidi "why one skilled in the art would transmit a command signal to only one DDR memory device at a time ***when there is a plurality of***

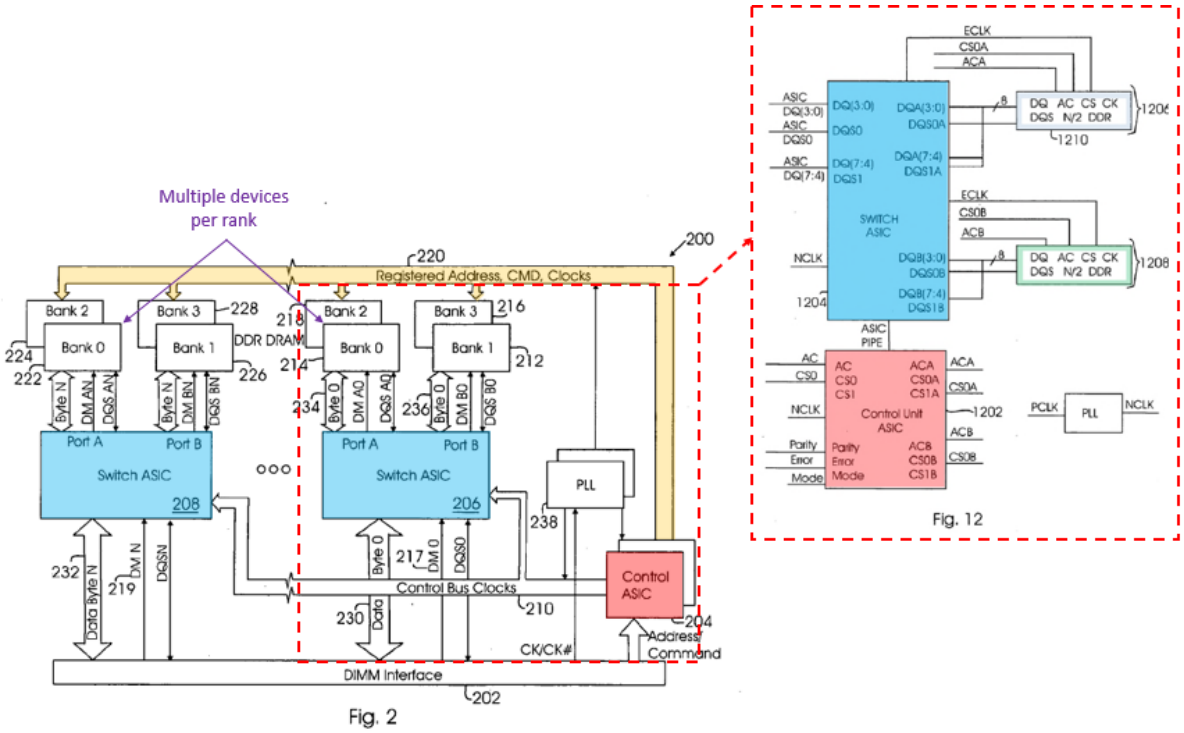
memory devices in a rank"). Petitioner's hypothetical single-device construct fails to render claim 16 obvious because it does not account for the requirement of multi-device ranks.

99. Second, even accepting for the sake of argument Petitioner's construction that a "rank" could theoretically be composed of a single memory device, I note that Ellsberry does not disclose a memory module with only a single device in each "rank." Petitioner contends Figures 12 and 13 illustrate this arrangement, but Figures 12 and 13 show only components connected to a single switch ASIC, which is only one of multiple switch ASICs that are part of Ellsberry's overall architecture. *See supra*, ¶84.



100. This is consistent with the Board's previous findings that certain of Figures 10-13 depict only a part of Ellsberry's overall architecture depicted in Figure 2. *See, e.g.,* EX1038, 50 (noting "Figure 13 shows ***part of a memory module***"), 51 ("Duplicating Figure 13's architecture, as shown in Figure 2 …"), 57 ("Petitioner contends a person of ordinary skill in the art would have combined Ellsberry's Figures 2, 5, and 13 for the eight-bit memory device, or would have combined Ellsberry's Figures 2, 6, and 11 for the four-bit memory device, because of their inclusion in the same patent application, and because Ellsberry specifically relates them to each other. ***We agree with Petitioner's contention***.") (internal citations omitted), 77 (noting that "in reference to Figures 10, 11, 12, and 13, Ellsberry states '[t]hese configurations employ the control unit and bank switch previously described,' ***thus relating these figures to the earlier-described control units and switches*** (including Figures 2, 5, and 6)."), 81 ("Figures 11 and 13 are more detailed embodiments of parts of Ellsberry's Figure 2"); EX2032, 40 n.11 (Institution Decision in IPR2022-00063) (agreeing with Samsung that "FIGS. 2, 5, and 13 of Ellsberry correspond to a 'First Embodiment' utilizing four ranks, each composed of nine 8-bit memory devices

for a total bit width of 72”). Thus, a person of ordinary skill in the art would understand that Figures 12 and 13 show the structure for a single switch ASIC, where Ellsberry’s memory module has multiple switch ASICs. Figure 2, for example, shows multiple switch ASICs, each connecting to four banks:



(EX1037, Fig. 2 as compared to Fig. 12)

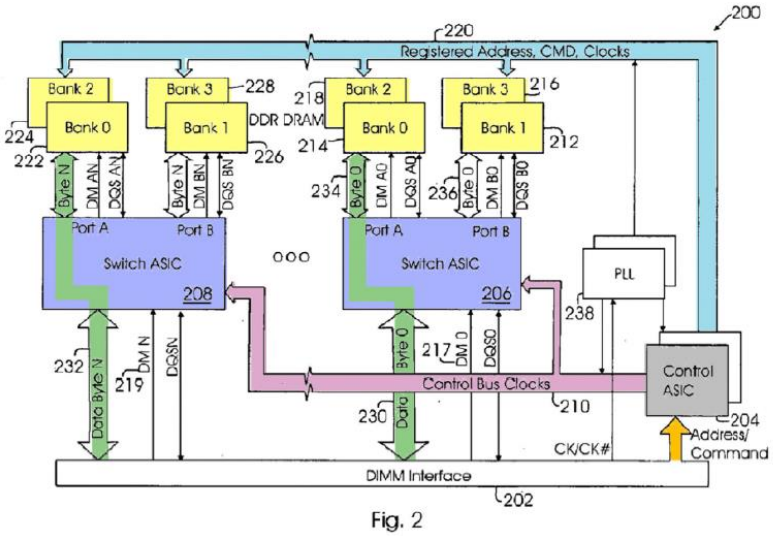


Fig. 2

(EX1037, Fig. 2 as annotated by Petitioner in IPR2022-00639)

101. Moreover, as depicted above, each switch ASIC receives a byte-wide range of data bits from the DIMM interface, *e.g.*, "Data Byte 0" through "Data Byte N" (green). EX1037, Fig. 2, [0030]. A person of ordinary skill in the art would thus understand that Ellsberry's overall architecture would include N switch ASICs, corresponding to, for example, a 64-bit (N = 8) or 72-bit (N = 9) memory module.

102. I understand that Petitioner maps Ellsberry's "banks" to the claimed "ranks." *See* Pet., 74 ("[E]ach of Ellsberry's four 'banks' discloses a respective 'rank'"); *id.*, 12 ("[T]he term 'bank' was … used to refer to what is now typically

called a 'rank'"). Thus, for example, in Figure 2, when Bank 1 is selected, there are at least two Bank 1 devices, device 226 connected to switch ASIC 208 and device 212 connected to Switch ASIC 206. Petitioner does not address how Ellsberry selects the target memory device for a command signal in Ellsberry's multi-device "bank" arrangement. As depicted above in Figure 2, commands are transmitted from control ASIC 204 via bus 220 to the memory banks directly, i.e., the at least two Bank 1 devices 226 and 212; not to switch ASICs 206 and 208. Thus, a person of ordinary skill in the art would understand that, if commands are sent to devices in Bank 1, commands will be transmitted to at least two devices at a time via bus 220.

103. Figure 5 also shows multiple bank switches 508 (which is the same as bank switch 206 described in Figure 2), each connected to two memory devices 504 and 512, as is consistent with Figure 12. EX1037, [0050] ("In one implementation of the invention, illustrated in FIG. 5, the memory devices 504 & 512 on the memory module 500 may be arranged as nine memory bank switches or sets 508 having two memory banks 504 & 512 each."). Again, I note

that Petitioner has not addressed how commands may be sent to a single device when there are multiple devices in a rank.

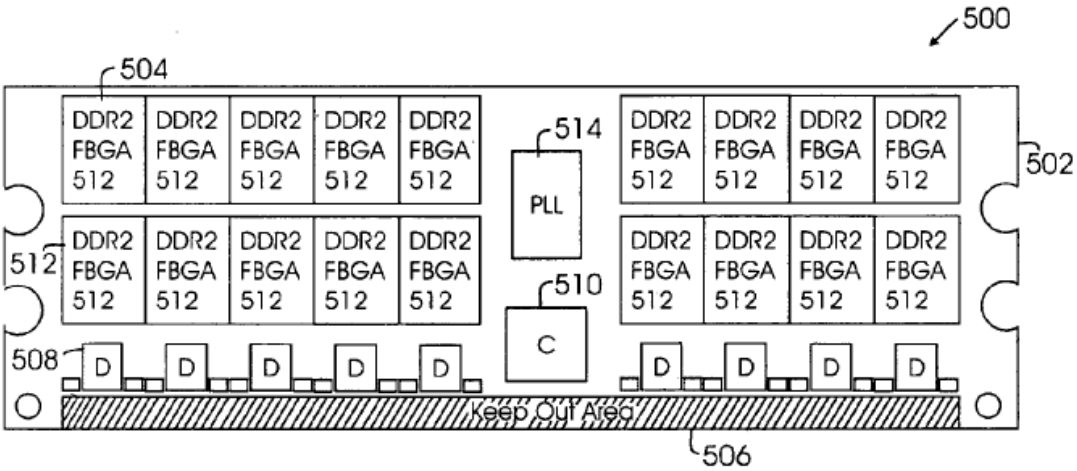


Fig. 5

104. Petitioner's citations to Ellsberry do not demonstrate that Ellsberry discloses a memory module having only a single bank switch ASIC (or what Petitioner calls "a single data buffer"). Pet., 75, 76 (citing EX1037, [0021], [0030], [0035]). For example, [0021] states that "FIGS. 10, 11, 12 and 13 illustrate different configurations of memory modules (e.g., DIMMs) that can be built using combinations of the control unit and bank switch according to various embodiments of the invention." But as discussed above, Figures 10-13 only represent a part of Ellsberry's overall multi-switch architecture. *Supra*, ¶99-103.

And as the Board previously noted, "in reference to Figures 10, 11, 12, and 13, Ellsberry states '[t]hese configurations employ the control unit and bank switch previously described,' ***thus relating these figures to the earlier-described control units and switches*** (including Figures 2, 5, and 6).'" EX1038, 77 (citing EX1037, [0052]).

105. As another example, [0030] which Petitioner relies on teaches that each switch ASIC in Figure 2 receives from the DIMM interface a range of data bits corresponding to a respective data group. EX1037, [0030] ("According to one embodiment of the invention, the DIMM interface 202 provides a range of data bits simultaneously (e.g., Data Group 0 through Data Group N)."). However, [0030] discusses multiple data groups, not a single data group. *Id.* ("***A first data group*** (i.e., Data Group 0) is received by a first memory bank switch 206 while ***a second data group*** (i.e., Data Group N) is received by a second memory bank switch 208.").

106. As further example, Petitioner appears be arguing that [0035] suggests starting from a single data group. *See* EX1003, ¶217 ("Ellsberry explains that the operation of ***one data group***, as shown in Figs. 12 and 13, 'is

expanded when implementing a wider memory bus formed by several data groups composed of a plurality of memory bank switches and the associated memories.'") (quoting EX1037, [0035]). However, I note that the sentence immediately before that makes reference to ***two*** switch ASICs, which Ellsberry states correspond to ***two*** data groups:

> The control unit 204 then handles mapping the logical memory addresses it receives via the DIMM interface 202 to a corresponding bank for a particular memory bank coupled to the ***switches 206 and 208***. This same principal is expanded when implementing a wider memory bus formed by several data groups composed of a plurality of memory bank switches and the associated memories.

EX1037, [0035]. As discussed above, Ellsberry notes that each bank switch 206 and 208 corresponds to a respective data group. [0030] (noting that "***a first data group*** … is received by ***bank switch 206*** while a ***second data group*** … is received by ***bank switch 208***"). Thus, a person of ordinary skill in the art would understand Ellsberry as disclosing starting with at least two bank switches, consistent with Figure 2's illustration of Ellsberry's overall architecture.

107. Petitioner also argues that it would have been obvious to a person of ordinary skill in the art to make a module with only a single data group, "as

expressly illustrated in Ellsberry's Figures 10-13," Pet., 76. But as discussed above, these figures only show a part of the total multi-data group module. *See supra*, ¶99.

108. Ellsberry discloses multiple switch ASICs, but no means of transmitting a command signal to individual memory devices in the same rank, which Petitioner equates to Ellsberry's "bank." Pet., 74 ("[E]ach of Ellsberry's four 'banks' discloses a respective 'rank'"); *id.*, 12. Ellsberry explains that "command information [is] received from the DIMM interface 202, buffered in a register 302 and ***sent to all memory banks*** (e.g., Bank 0, Bank 1, Bank 2 and Bank 3) over address bus 202." EX1037, [0039]; *see also id.*, [0030] ("The four memory banks (i.e., Bank 0, Bank 1, Bank 2, and Bank 3) 212, 214, 216, and 218 are also communicatively coupled to an address bus 220 through which they receive address and command information from the control unit 204."). As shown in Figure 2, each of the data buses includes byte-wide data groups (Data Byte 0-N) corresponding to each switch ASIC 206 and 208. *Id.*, Fig. 2, [0030]. Under Petitioner's theory, where a "bank" is interchangeable with "rank," and a "rank" is "an independent set of one or more memory devices on a memory

module that act together in response to command signals," Pet., 12, a person of ordinary skill in the art would understand that ***all the devices*** in one of the banks on Ellsberry's multi-switch module (e.g., Bank1 composed of memory devices 212 and 226) act together in response to command signals. This is consistent with Ellsberry's disclosure that interface 202 sends a range of byte-wise data signals corresponding to each switch ASIC 206 and 208 "***simultaneously***," such that "[d]ata may be read from or written to [the] memory devices." EX1037, [0030]. That is, read and write commands are sent simultaneously to multiple devices of the same rank. Accordingly, the Petition's Ground 3 fails to disclose Element [16.e].

* * *

I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that all these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed this 21st Day of July, 2022, in Austin, Texas.

Michael C. Brogioli, Ph.D.

APPENDIX A

Michael C. Brogioli, Ph.D.

Contact Information

Michael C. Brogioli, Ph.D.
Polymathic Consulting
100 Congress Avenue, Suite 2000
Austin, TX 78701 USA

Office: (512) 370-4936
Cell (preferred): (713) 732-0217
Fax: (512) 469-6306
E-mail: michael@polymathicconsulting.com

Expertise

Software Analysis, Software Architecture, Embedded Computing, Microprocessor Designs, Software Based Simulation, Computer Hardware Design, Computer Networks, Computer and Network Based Gaming Platforms, High Performance Computing, Digital Signal Processing.

Education

Rice University, Houston, Texas USA

Ph.D., Electrical and Computer Engineering, 2007

- Dissertation Topic: "Reconfigurable Heterogeneous DSP/FPGA Based Embedded Architectures for Numerically Intensive Embedded Computing Workloads."
- Advising Committee: Dr. Joseph R. Cavallaro, Dr. Keith D. Cooper, Dr. Scott Rixner

Rice University, Houston, Texas USA

M.S., Electrical and Computer Engineering, 2003

- Dissertation Topic: "Dynamically Reconfigurable Data Caches in Low Power Computing."
- Advising Committee: Dr. Keith D. Cooper, Dr. Scott Rixner, Dr. Robert Jump

Rensselaer Polytechnic Institute, Troy, New York USA

B.S., Electrical Engineering, Cum Laude, 1999

- Advisor: Dr. William Pearlman

Certificates

Harvard Business School, Boston, Massachusetts, USA

Certificate in Investment Portfolios with Alternate Investments, 2022

- Venture Capital, Growth Equity, Distress Investing, Private Debt, Hedge Funds, Portfolio Construction.

Professional Experience

Polymathic Consulting, TX USA
Managing Director **2011 - Present**
Founder and managing director of Polymathic Consulting, servicing clients ranging from early stage technology start-up endeavors to Fortune 100 and beyond. Clients turn to Polymathic for expansive, proven engineering, research and development, intellectual property and technical leadership to effectively advance their real world business needs.

IEEE and ACM Design Automation Conference, USA
Steering Committee
Conference Chair, Embedded Systems and Software Track **2016 - Present**
Design Automation Conference is the premiere technical conference and trade show specializing in Hardware, Software, Internet of Things, Embedded Systems and related Design Methodologies. Conference chair, responsible for the review, critique, and acceptance of academia and industry based publications in the areas of embedded systems, embedded software, and embedded system design.

Rice University, TX USA
Adjunct Professor, Electrical and Computer Engineering **2009 - Present**

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Professor of Ph.D. candidate level courses in wireless telecommunications, embedded computing software, embedded computing hardware, and software/hardware optimization in modern computing systems utilizing modern high level programming languages. Advisor of senior and graduate student based projects revolving around multi-core heterogeneous systems as they pertain to wireless telecommunications, medical and video.

RISC-V Foundation, Berkeley, CA USA
Technical Committee **2018 - Present**
RISC-V is an open CPU instruction set architecture (ISA) based on established reduced instruction set computing (RISC) principles. The RISC-V Foundation is a non-profit consortium chartered to standardize, protect, and promote the free and open RISC-V instruction set architecture together with its hardware and software ecosystem for use in all computing devices.

Freescale Semiconductor, TX USA
Chief Architect, Senior Member Technical Staff **2009 - 2011**
Technical architect of Freescale's DSP compilers and related technology. Responsible for management of technology, engineering roadmaps, design lead on compiler infrastructure and optimizations (high level and low level), next generation ABI definitions and next generation architecture solutions. Technical lead on multi-year engagement with processor architects in design of next generation DSP cores. Developed software infrastructure for migrating OEM competitor software stacks to Freescale solutions, tools generation, software packages, migration strategies and white papers. Technical lead on Tier-1 OEM customer relationships, evaluations of 3rd party technologies for potential partnerships and acquisitions, led various university research collaborations on behalf of Freescale. Development and deployment of internal software engineering policies and practices.

Freescale Semiconductor, TX USA
Senior Compiler Engineer V
High Performance Compiler Design, Processor Architecture **2008 - 2009**
Team leader on compiler engineering effort to provide intuitive, interactive end user experience for DSP compiler tool suite. Designed a framework to guide users in achieving highly optimized compiled VLIW code. Assembly listing reports for optimization failure advice, porting advice when migrating from competitor architectures, advice on code modifications for optimization enablement. Lead designer, engineering effort director, project planning and scoping, release schedule, and drafting of specification. Development of various compiler optimizations for VLIW processing as well as software emulation layers for running competitor software solutions on Freescale silicon.

Advising of next-gen DSP core architecture team in creating a highly orthogonal, compiler targetable multi-clustered VLIW based digital signal processor architecture. Work with future basestation architecture teams on designing next-gen basestation architecture for 4G LTE incorporating control and data plane processing with appropriate programming models.

Method Seven, MA USA
Technical Co-Founder
High Performance Software and Hardware Systems Architecture **2006 - 2007**
Founded Method Seven, a financial engineering company applying biologically inspired machine learning to financial market analysis. Principal software systems architect and hardware systems architect for both research and deployment platforms. Led research and development of platform for scans and overlays covering the NASDAQ, NYSE, and AMEX markets using proprietary technologies.

Texas Instruments, TX USA
Advanced Architecture and Chip Technologies
Microprocessor and Systems Architecture **2005**
System modelling and architectural exploration of Davinci^{TM}system-on-chip (SOC) architecture

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designed for embedded video processing. SystemC based simulation models of on–chip crossbars, bus arbitration and bridge technology, as well as on–chip and off–chip memory controllers within application specific heterogeneous SOC architectures.

Fulbright and Jaworski LLP, TX USA
Scientific Advisor, Intellectual Property
Electrical, Computer Engineering and Computer Science **2005 - 2007**
Intellectual property consultant and technology advisor on litigation and prosecution work including, but not limited to: CDMA2000 3G wireless standards, wireless communications systems, embedded computing, and large scale modular software systems. Reverse engineering of source code varying from VHDL to high level object oriented applications, as well at patent prosecution and litigation work.

Intel Corporation, CA USA
Microprocessor Research Labs
Compiler Engineering **2000**
Implemented speculative multi–threading support in Intel's IA–64 compiler. Developed new program analysis and back end code generation phases to support speculatively launching threads at runtime. Analyzed the performance potentials of SPEC95 benchmarks with respect to speculatively multi–threaded execution.

Rice University, TX USA
Computer Architecture and Circuit Design (Instructor) **2000 - 2003**
Graduate instructor of graduate and undergraduate curriculim in the areas of Electrical and Computer Engineering, specifically relating to Computer Architecture and Circuit Design. Advised student projects, instructed classes and led laboratory work.

Vicarious Visions, NY USA
Lead Software Engineer **1999**
Principal engineer on Activision's "AMF Extreme Bowling" for Nintendo's Color Gameboy gaming console. Developed PC based audio and graphics development tools suite for use with Color Gameboy game production. Coded innovative, highly optimized assembly routines for real time speech and full motion video on the console's limited Zilog Z80 processor resources.

Stratus Computer, MA USA
Hardware Engineering **1997 - 1998**
Debugged locked step CPU operation and memory management issues in Stratus' fault tolerant UNIX release 3.4. Qualified Hewlett Packard PA–8000 series CPU modules under Stratus' proprietary OS release, VOS 14.0, during alpha and beta test phases. Wrote C code and UNIX shell scripts for recreating documented system failures, and to automate remote kernel updates and OS installs as well as data logging.

Rensselaer Polytechnic Institute, NY USA
Digital Microelectronics Design (Instructor) **1997 - 1998**
Undergraduate instructor of undergraduate courses in digital microelectronics and circuit design. Instructed weekly lessons, computer design labs, graded exams and problem sets.

Rensselaer Electric Motor Sports, NY USA
Hardware and Software Engineering **1995 - 1997**
This project was funded by, and led by, General Motors Corporation and Honda of America. Hardware and software co-design of embedded operating system and hardware platform for electrical vehicle prototypes, running on 16-bit Motorola 68K dual processor platform. Designed power engineering test platform for dynamometers, including hardware and user interface software.

Appointed Conference Committees and Organizations

IEEE International Conference on Communications, USA
Technical Review Committee, Machine Learning for Communications Track **2021 - Present**
Technical committee member responsible for the review, critique, and acceptance of academia and industry based publications and research in the areas of machine learning for communications systems.

IEEE International Symposium on Circuits and Systems, USA
Technical Review Committee **2021 - Present**
Technical committee member responsible for the review, critique, and acceptance of academia and industry based publications and research in the areas of computing, including energy aware systems, multicore processing, and adaptive computing.

IEEE and ACM Design Automation Conference, USA
Technical Steering Committee, Embedded Computing Track **2019 - Present**
Technical Steering Committee member responsible for the review, critique, and acceptance of academia and industry based publications and research in the area of embedded computing and related systems, including embedded hardware, embedded software, firmware and tools.

IEEE and ACM Design Automation Conference, USA
Co-chair, Program Committee, Embedded Systems and Software Track **2014 - 2019**
Co-chair and Program Committee member responsible for the review, critique, and acceptance of academia and industry based publications in the areas of embedded systems, embedded software, and embedded system design. Design Automation Conference is an annual technical conference and trade show specializing in electronic systems.

IEEE and ACM Design Automation Conference, USA
Program Committee, Designer and User Track **2011 - Present**
Program Committee member responsible for the review, critique, and acceptance of academia and industry based publications in the areas of automated system design, both of hardware, software, and system analysis. Design Automation Conference is an annual technical conference and trade show specializing in electronic systems.

ACM Great Lakes Symposium on VLSI, Stresa-Lago Maggiore, Italy
Program Committee **2007**
Reviewer and committee member in the area of system-on-chip architectures, VLSI design, and compiler driven architecture design space exploration.

IEEE International Symposium on Personal Indoor and Mobile Radio Communications, Helsinki, Finland
Program Committee **2006**
Reviewer and committee member in the area of personal and mobile area radio communications and related systems.

ACM International Conference on Parallel Architectures and Compilation Techniques, Charlottesville, VA, USA
Program Committee **2002**
Reviewer and committee member in the area of parallel computer architectures, programming languages and related compiler technologies.

Books and Contributed Chapters

Brogioli, Michael C., and Kraeling, Mark B., *Internet of Things - A Synopsis of the Internet of Things, its History, Application, Technology, Architecture, and Challenges Moving Forward*, Software Engineering for Embedded Systems - Methods, Practical Techniques and Applications, 2nd Edition, Elsevier Publishing, 2019.

Brogioli, Michael C., *Software and Compiler Optimization for Microcontrollers, Embedded Processors and DSPs*, Software Engineering for Embedded Systems - Methods, Practical Techniques and Applications, 2nd Edition, Elsevier Publishing, 2019.

Brogioli, Michael C., *Embedded and Multicore System Architecture - Design and Optimization*, Software Engineering for Embedded Systems - Methods, Practical Techniques and Applications, 2nd Edition, Elsevier Publishing, 2019.

Leotescu, Florin, and Cristian, Marius and Brogioli, Michael C., *Performance Analysis using NXP's i.MX RT1050 Crossover Processor and the Zephyr Real-Time Operating System*, Software Engineering for Embedded Systems - Methods, Practical Techniques and Applications, 2nd Edition, Elsevier Publishing, 2019.

Wu, Michael and Sun, Yang and Wang, Guohui and Brogioli, Michael C. and Cavallaro, J. R., *Implementation of a High Throughput 3GPP Turbo Decoder on GPU Architectures*, Software Development for Networking Applications – Expert Guides Series, Elsevier Publishing, Atlanta, GA, 2018.

Brogioli, M. C., *On The C++ Programming Language for Embedded Software, Systems, and Platforms*, Software Engineering for Embedded Systems – Expert Guides Series, Elsevier Publishing, Atlanta, GA, 2013.

Brogioli, M. C., *Software Optimizations for Memory Performance in Embedded Systems*, Software Engineering for Embedded Systems – Expert Guides Series, Elsevier Publishing, Atlanta, GA, 2013.

Invited Co-Author, *Signal Processing Systems Handbook, Second Edition*, Springer Publishing Company, 11 West 42nd Street, New York, NY, 2012.

Brogioli, M. C., *Software Programmable DSP Architectures*, Expert Guide DSP for Embedded and Real-Time Systems, pp. 63-75, Elsevier Publishing, Atlanta, GA, 2012.

Brogioli, M. C., *The DSP Hardware / Software Continuum*, Expert Guide DSP for Embedded and Real-Time Systems,, pp. 103-113, Elsevier Publishing, Atlanta, GA, 2012.

Brogioli, M. C., *DSP Optimization - Memory Optimization*, Expert Guide DSP for Embedded and Real-Time Systems, pp. 217-241, Elsevier Publishing, Atlanta, GA, 2012.

Brogioli, M. C. and Dew, Stephen, *Optimizing DSP Software - High level Languages and Programming Models*, Expert Guide DSP for Embedded and Real-Time Systems,, pp. 167-179, Elsevier Publishing, Atlanta, GA, 2012.

Sun, Yang, Amiri, Kiarash, Brogioli, Michael, Wang, Guohui, and Cavallaro, Joseph R., *DSP Hardware Accelerator Architectures for Communication Applications*, Springer Publishing, New York, NY, Spring 2012.

Sun, Yang, and Amiri, Kiarash, and Brogioli, Michael C., and Cavallaro, Joseph, *Application-Specific Accelerators for Communications*, Springer Publishing Company, 11 West 42nd Street, New York, NY, 2010.

Invited Co-Author, *Signal Processing Systems Handbook, First Edition*, Springer Publishing Company, 11 West 42nd Street, New York, NY, 2010.

Publications and Invited Papers

Brogioli, Michael, C., and Games, William, and Moats, Richard, *Current and Future Challenges in Internet of Things (IoT) Development Silos (Part I)*, Embedded Computing Design Magazine,

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USA, 2020.

Brogioli, Michael, C., and Games, William, and Moats, Richard, *On Solving the IoT Development Silo Problem* IEEE Real-Time and Embedded Technology and Applications Symposium, Tools and Demos Session, Montreal, Canada, 2019.

Moats, Richard, and Games, Bill, and Brogioli, M. C., *Arch - A New Language For The Next Wave of Network-Connected Embedded Development*, Design Automation Conference, Austin, Texas, 2017.

Moats, Richard, and Games, Bill, and Brogioli, M. C., *Network Native - The Next Wave of Connected Embedded Development*, Network Native Inc., Austin, Texas, 2017.

Invited Paper, Arokia I, Brogioli, Michael, Jain, Nitjin and Garg, Umang, *LTE Layer 1 Software Design on Heterogeneous Multicore DSP Platforms*, IEEE 45th Asilomar Conference on Signals, Systems and Computers, Pacific Grove, CA, 2011.

Kyriakopoulous, Konstantinos, Brogioli, Michael C., and Zhang, Ruihao, *Improving Software Systems Quality through Well Defined Development Methodologies*, 2011 Test Methodology and Efficiency Symposium, Freescale Semiconductor, Austin, TX, USA, 2011.

Brogioli, Michael C., and Cavallaro, J.R., *Compiler Driven Architecture Design Space Exploration for Embedded DSP Workloads: A Study in Software Programmability Versus Hardware Acceleration*, IEEE 43rd Asilomar Conference on Signals, Systems and Computers, Pacific Grove, CA, 2009.

Brogioli, Michael C., and Zhang, Ruihao, *Compiler Feedback: Guiding Performance of Compiled C Code*, Freescale Semiconductor White Paper, Austin, TX, 2009.

Brogioli, M.C., and Cavallaro, J., *RISD: A Retargetable Compiler Infrastructure for Scalable Multi-Clustered VLIW DSP Architectures*, IEEE 5th Dallas Circuits and Systems Workshop, Dallas, TX, 2007.

Brogioli, Michael C., Radosavljevic, P., and Cavallaro, J., *A General Hardware/Software Codesign Methodology for Embedded Signal Processing and Multimedia Workloads*, IEEE 40th Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, CA, 2006.

Brogioli, Michael C., Radosavljevic, P., and Cavallaro, J., *Hardware/Software Co-design Methodology for DSP/FPGA Partitioning: A Case Study for Meeting Real-Time Processing Deadlines in 3.5G Mobile Receivers*, 49th IEEE International Midwest Symposium on Circuits and Systems, San Juan, Puerto Rico, 2006.

Brogioli, Michael C., Willmann, P.D., and Rixner, S., *Parallelization Strategies for Network Interface Firmware*, IEEE/ACM 4th Annual Workshop on Optimizations for DSP and Embedded Systems (In Conjunction with IEEE/ACM International Symposium on Code Generation and Optimization), Manhattan, NY, 2006.

Brogioli, Michael C., Gadhiok, M., and Cavallaro, J., *Design and Analysis of Heterogeneous DSP/FPGA Based Architectures for 3GPP Wireless Systems*, IEEE Real-Time and Embedded Technology and Applications Symposium Work-in-Progress Sessions, San Jose, CA, 2006.

Brogioli, Michael C., and Cavallaro, J., *Modelling Heterogeneous DSP-FPGA Based System Partitioning with Extensions to the Spinach Simulation Environment*, IEEE 39th Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, CA, 2005.

Joseph R. Cavallaro, Michael C. Brogioli, Alexandre de Baynast, and Predrag, Radosavljevic, *Re-*

configurable Architectures for Wireless Systems: Design Exploration and Integration Challenges, Wireless World Research Forum, Toronto, CA, 2004.

Brogioli, Michael C., Pai, V.S., Willmann, P.D., *Spinach: A Liberty–Based Simulator For Programmable Network Interface Architectures*, ACM SIGPLAN/SIGBED Conference on Languages Compilers and Tools for Embedded Systems, San Diego, CA, 2004.

Brogioli, Michael C., *Dynamically Reconfigurable Data Caches in Low Power Computing*, Masters Thesis, Rice University, Houston Texas, 2002.

Brogioli, Michael C., and Jones, Bryan, *Dynamically Configurable Caches in Low Power Computing*, Internal White Paper, Rice University, Houston Texas, 2001.

Patents

Donald W. Games, Michael C. Brogioli Ph.D., Richard Moats, *System And Method for Holistic Application Development and Deployment in a Distributed Heterogeneous Computing Environment*, U.S. Patent Application 17/745,792, filed May 2022. Patent Pending.

Gregory D. Chiocco and Michael C. Brogioli, *Systems and Methods for Traversing A Three Dimensional Space*, U.S. Patent Application 17/578,408, filed January 2022. Patent Pending.

Gregory D. Chiocco and Michael C. Brogioli, *Systems and Methods for Aggregating Harvest Yield Data*, U.S. Patent Application 17/306,839, filed April 2020. Patent Pending.

Gregory D. Chiocco and Michael C. Brogiolil, *Systems And Methods For eCommunication in GNSS Based Autonomous Vehicle Deployment*, U.S. Patent Application 17/060,625, filed March 2021. Patent Pending.

Michael C. Brogioli and Gregory D. Chiocco, *Systems and Methods for Connected Computation in Network Constrained Systems*, U.S. Patent Application 62907727, filed October 2019. Patent Pending.

Donald W. Games, Michael C. Brogioli Ph.D., Richard Moats, *System And Method for Holistic Application Development and Deployment in a Distributed Heterogeneous Computing Environment*, U.S. Patent Application 62782009, filed December 2018. Patent Pending.

Michael C. Brogioli, Ph.D., Cesar Taylor M.D., and Howard Roberts, *Location Agnostic Platform for Medical Condition Monitoring and Prediction and Method of Use Thereof*, Patent No: 147145.010100/US, 2014.

Cesar Taylor M.D., and Michael C. Brogioli Ph.D., and Howard Roberts, *System for Holistic Pain Monitoring and Prediction and Method of User Thereof*, Patent No: 147145.010200/US, 2014.

Cesar Taylor M.D., and Michael C. Brogioli Ph.D., and Howard Roberts, *System for Prevention of Narcotic Diversion and Method of Use Thereof*, Patent No: 147145.010300/US, 2014.

Howard Roberts, Cesar Taylor M.D., and Michael C. Brogioli Ph.D., *Magnetometer Breathing Sensor and Method of User Thereof*, Patent No: 147145.010400/US, 2014.

Leadership and Board Membership

Tandem Motion Company FL, USA
Advisory Board **2021 - Present**
Advisory board member on intellectual property strategy, fundraising, finance and select technologies. Tandem is building hybrid solutions for heavy duty internal combustion engine vehicles.

MIT MassChallenge USA
Mentor, Speaker **2017 - Present**
MassChallenge is a global startup accelerator with a focus on high-impact, early-stage entrepreneurs. Through its global network of accelerators in Boston, London, Mexico City, Geneva, Jerusalem and Texas, coupled with unrivaled access to our corporate partners, MassChallenge has driven growth and created value the world over. To date, MassChallenge has raised over $2B in funding, generated over $900M in revenue, and created over 65,000 jobs.

ScribeSense, TX USA
Board of Directors **2017**
ScribeSense is a *patented* cloud-based grading platform for schools and the only solution for grading free-form paper tests. ScribeSense automatically grades handwritten tests with 99% accuracy. Teachers scan and upload their own tests using a standard school scanner. ScribeSense's visual analytics enables data-driven decision making so schools can improve student learning and retain top teacher talent.

Southwest Angel Network for Social Impact, TX USA
Board of Directors **2015 - 2019**
The Southwest Angel Network for Social Impact (SWAN Impact) is a community of like-minded investors who enjoy working together to *Make the world a better place, one company at a time.* We believe that we can have the most significant impact by funding for-profit start-up companies who are building sustainable businesses.

Network Native, TX USA
Board of Directors, Co-Founder, Interim CTO **2015 - Present**
Board member and co-inventor, advising in the areas of Internet of Things technologies, specifically related to product developer solutions, programming languages and platforms, security and infrastrucure. Business development, marketing, and fund raising. Have held various roles, including but not limited to interim CTO.

NewCrew, TX USA
Advisory Board **2015 - 2016**
Board member advising in the areas of mobile computing, social computing, and geofencing technologies. Business development, marketing, and fund raising.

AngelSpan, TX USA
Advisory Board **2015 - 2016**
Board member advising in the areas of professional investor relations to start-ups, resource allocation, and a platform for increased efficiency and valuation of early stage companies and venture capital portfolios.

Student Loan Genius (now Vault), TX USA
Advisory Board, Interim CTO **2013 - 2014**
Advisory board member and interim CTO advising in the areas of financial transactions systems and enterprise software, as they pertain to solving the student loan debt crisis for early stage science, technology, engineering and medicine (STEM) employees. Technology, recruiting, fund raising.

HealthBits, TX USA
Board Member, Co-Inventor **2013 - 2014**
Board member advising in the areas of large scale enterprise software systems, real-time computing and medical sensing devices across complex event processing systems.

Osmek, TX USA
Interim CTO, Advisory Board **2012 - 2014**

Interim CTO and board member advising in the areas of large scale cloud based content management software systems. Providing innovative media content management for heterogeneous web enabled devices with geolocational services, primarily using PHP and Python programming languages.

Academia

Rice University, Houston, Texas USA
DSP Compiler Design **2005 - 2009**
Developed *RISD*, a retargetable compiler infrastructure for clustered VLIW DSP architectures. By taking pre-existing code schedules and binaries for existing DSP applications, RISD takes a flexible machine definition for which the code should be recompiled. Users can specify the number of VLIW clusters, functional units per VLIW cluster, functional unit mix per VLIW cluster, register file sizes, cluster interconnect topology (point-to-point versus 2d mesh network), multi-cluster scheduling algorithms, and inter-cluster cross-register file bandwidth and latencies.

Compiler framework was used to perform compiler driven design space exploration of massively multi-clustered VLIW based architectures versus FPGA and ASIP implementations of software kernels. RISD was used in studies comparing tradeoffs in computational throughput versus gates required to implement programmable DSP cores containing many register files and VLIW compute clusters, versus FPGA efficiency when including routing overhead for large scale problems.

Rice University, Houston, Texas USA
DSP/FPGA Based System-On-Chip Architectural Simulator Design **2004 - 2009**
Developed *Spinach DSP-FPGA*, a modular and composable simulator design infrastructure for programmable and reconfigurable embedded SOC architectures. Designed and developed modular and composable software modules to bit-true, cycle accurately simulate Texas Instruments C62x and C64x DSPs and MIPS style processors. Additionally designed and developed support for SRAM and DRAM style memories, heterogeneous memory systems, heterogeneous clock domains, as well as runtime reconfigurable Xilinx Virtex II based FPGA computing elements, cache and memory controllers, bus arbiters, and on-chip interconnect fabric.

System was validated against compiled code DSP firmware from Texas Instruments' Code Composer Studio running on the simulator versus actual hardware benchmarks. Simulation platform was used to investigate highly heterogeneous multi-processor DSP based SOC architectures containing one or more Xilinx style FPGA based hardware coprocessors. Studies in 3.5G wireless telecommunications as well as H.26x video processing were performed to gain insight into overall system bottlenecks, hardware and software partitioning strategies, and tradeoffs of overall system design.

Rice University, Houston, Texas USA
Programmable Network Interface Architecture Simulator Design **2002 - 2004**
National Science Foundation Grant Nos. CCF-0532448 and CNS-0532452
Developed *Spinach*, a simulator design toolset for modelling programmable network interface architectures. Spinach models system components common to all programmable environments (ALUs, control and data paths, register files, instruction processing), as well as components specific to embedded computing (software controlled SRAM scratchpad memory, hardware assists for DMA and medium access control). Spinach is a simulator design infrastructure, rather than a simulator per se. As such, the same underlying C code framework is used to model a uniprocessor Gigabit network interface, a multi-processor Gigabit network interface, or a 10 Gigabit multi-processor network interface with highly heterogeneous memory systems. Only a small number of lines of high level scripting language code is required to describe each of the various systems.

Spinach was validated by modeling the Tigon-2 programmable Ethernet controller by Alteon Websystems, running actual compiled code Ethernet processing firmware and by comparing the reported results to actual hardware benchmarks. Spinach was also used to obtain new insights into the performance of Gigabit and 10 Gigabit network interfaces both in terms of hardware architecture and firmware parallelization strategies. *Public Website: https://sourceforge.net/projects/spinach/*

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Rice University, Houston, Texas USA
Software Engineering and Consulting **2000**
Implemented instruction selection and register allocation optimizations in UHFFT, an adaptive and portable software library for the Fast Fourier Transform. Performed in depth analysis of register pressure, compiler generated spill code, memory hierarchy utilization, and instruction selection for non–trivially sized FFT matrices running on commercially available hardware platforms. Utilized reverse Cuthill–McKee technique to achieve near optimal computation orderings and minimize live data set sizes, as well as optimize register allocation and instruction selection phases of compilation.

Selected Expert Witness, Consulant Engagements

Sonrai Memory Limited* v. Oracle Corporation
Russ, August, and Kabat LLP, Los Angeles, CA, USA
Expert Witness in Memory and Compression Technology **2021 - 2022**
Case Subject Matter - Memory controllers, memory technology and data compression technology.
Work Performed - Expert consulting, claim construction, declarations, deposition.

Certain Laptops, Desktops, Servers, Mobile Phones, Tablets, and Components Thereof, Inv. No. 337-TA-1280
Sonrai Memory Limited*
Russ, August, and Kabat LLP, Los Angeles, CA, USA
Expert Witness in Low Power Systems **2021 - Present**
Case Subject Matter - System on chips, operating systems and system components related power consumption in computing devices.
Work Performed - Expert consulting, claim construction declarations, expert reports, depositions (to date).

Future Link Systems LLC* v. Advanced Microdevices, Inc.
Future Link Systems LLC* v. Apple, Inc
Future Link Systems LLC* v. Broadcom, Inc; Broadcom Corp.
Future Link Systems LLC* v. Qualcomm, Inc.; Qualcomm Technologies
Future Link Systems LLC* v. Realtek Semiconductor Corp.
Russ, August, and Kabat LLP, Los Angeles, CA, USA
Expert Witness in Circuit Design and Interconnects **2020 - 2022**
Case Subject Matter - Semiconductor circuit design and reuse, PCI Express and related interconnect technologies.
Work Performed - Expert consulting, claim construction, declarations, depositions.

Certain UMTS and LTE Cellular Communications Modules and Products and Products Containing the Same, Inv. No. 337-TA-1240
Philips RS North America LLC and Koninklijke Philips N.V.*
Foley & Lardner LLP, MA, USA
Expert Witness in Wireless Computing Technology **2020 - 2021**
Case Subject Matter - Embedded computing technology related to wireless mobile devices, including 3GPP standards based functionality.
Work Performed - Expert consulting, expert reports, deposition, trial testimony.

Acqis* v. Samsung Electronics Co., LTD
Robins Kaplan LLP, USA
Expert Witness in Mobile Devices and Interconnects **2021**
Case Subject Matter - Chip and chipset interconnect technology relating to mobile and non-mobile devices.
Work Performed - Expert consulting, expert reports, depositions.

Neodron Limited* v. Texas Instruments, Inc
Neodron Limited* v. Cypress Semiconductor Corp

Neodron Limited* v. Renesas Electronics Corp
Neodron Limited* v. ST Microelectronics N.V.
Russ, August, and Kabat LLP, Los Angeles, CA, USA
Expert Witness in Touch Screen Technology and Related Systems **2020 - 2021**
Case Subject Matter - Expert witness in hardware/software systems for touch screen techology, including analog and digital signaling and processing.
Work Performed - Expert consulting, declarations.

Qualcomm Inc. v. Monterey Research LLC*
Desmarais LLP, NY, USA
Expert Witness in Memory Systems Technology **2021**
Case Subject Matter - SRAM and DRAM technology, burst functionality and related matters.
Work Performed - Expert consulting, IPR declarations, depositions.

Advanced Micro Devices Inc. v. Monterey Research LLC*
Desmarais LLP, NY, USA
Expert Witness in Memory Systems, Interconnects **2021**
Case Subject Matter - SRAM and DRAM technology, multi-ported memory systems, boot technology and related technologies.
Work Performed - Expert consulting, IPR declarations, depositions.

Analog Devices Inc. v. Xilinx Inc.*
Morrison & Foerster LLP, CA, USA
Expert Witness in FPGAs and Configurable Computing **2020 - 2021**
Case Subject Matter - FPGAs and solutions related to crossbar interconnects, high speed transceivers, and configurable computing.
Work Performed - Expert consulting, IPR declarations, depositions.

TriOptima AB v. Quantile Technologies Limited*
Caldwalader Wickersham & Taft, New York, USA
Expert Witness in Source Code for FinTech Systems **2020**
Case Subject Matter - Technology implementations of financial services related to compression and derivatives markets.
Work Performed - Expert consulting, source code review.

Unified Patents LLC v. JustService.net LLC*
Sheridan Ross P.C., Colorado, USA
Expert Witness in Virtual Data Storage Systems **2020 - 2021**
Case Subject Matter - Web enabled virtual data storage systems for backup, storing and transferring of data.
Work Performed - Expert consulting, declarations, depositions.

Karya Property Management, LLC* v. ResMan, LLC
Baker Botts LLP, Houston, Texas, USA
Expert Witness in Distributed Software Systems **2020 - 2021**
Case Subject Matter - Expert witness in the areas of distributed software systems, including data base technologies, as they relate to propety management software and related systems.
Work Performed - Expert consulting, claim construction, IPR declarations, CBM declarations, depositions, expert reports.

Certain Touch-Controlled Mobile Devices, Computers, and Components Thereof, Inv. No. 337-TA-1193
Neodron Limited*
Russ, August, and Kabat LLP, Los Angeles, CA, USA

Expert Witness in Touch Screen Technology and Related Systems **2020**
Case Subject Matter - Expert witness in hardware/software systems for touch screen techology in mobile devices.
Work Performed - Expert consulting.

VLSI Technology LLC* v. Intel Corporation
Irell & Manella LLP, Los Angeles, CA USA
Expert Witness in Computer Architecture **2020 - 2021**
Case Subject Matter - Expert witness in the area of computer architecture, microprocessors and power management.
Work Performed - Expert consulting and source code review, expert reports, depositions, trial testimony.

Optimum Imaging Technologies LLC* v. Canon Inc.
Ruyak Cherian LLP, Washington D.C., USA
Expert Witness in FPGA Based Image Processing Systems **2019 - 2021**
Case Subject Matter - Expert witness and consultant in the area of heterogeneous FPGA/DSP/CPU based systems as applied to image and video processing technology.
Work Performed - Expert consulting, claim construction declarations, expert reports, depositions, IPR declarations.

Dish Network, LLC v. Contemporary Display LLC*
Toler Law Group, P.C., Texas., USA
Expert Witness in Real Time Video Processing **2020**
Case Subject Matter - Expert Witness in real-time video processing technology over the Internet, including related user interfaces and quality of service.
Work Performed - Consulting, IPR declarations, deposition.

Dish Network, LLC v. Contemporary Display LLC*
Toler Law Group, P.C., Texas., USA
Expert Witness in Real Time Video Processing **2020**
Case Subject Matter - Expert Witness in real-time video processing technology over Internet, including related user interfaces and quality of service.
Work Performed - Consulting, IPR declarations, deposition.

Multimedia Content Management LLC* v. Dish Network LLC
Sheridan Ross P.C., Colorado, USA
Expert Witness in Real Time Video Processing **2019 - 2020**
Case Subject Matter - Expert Witness in Internet based real-time video processing set top boxes, and related content processing and distribution.
Work Performed - Expert consulting.

Exegy Inc. et al v. ACTIV Financial Systems, Inc.*
Wolf Greenfield & Sachs P.C., USA
Expert Witness High Speed Computing for Financial Services **2019 - 2021**
Case Subject Matter - Expert Witness in microprocessor and FPGA based system design for high speed financial services, high speed RDMA systems, etc.
Work Performed - Expert consulting, IPR declarations, depositions.

Certain Touch-Controlled Mobile Devices, Computers, and Components Thereof, Inv. No. 337-TA-1162
Neodron Limited*
Russ, August, and Kabat LLP, Los Angeles, CA, USA
Expert Witness in Touch Screen Technology and Related Systems **2019 - 2020**

Case Subject Matter - Expert witness in hardware/software systems for touch screen techology in mobile devices.
Work Performed - Expert consulting, claim construction declaration, expert reports, depositions.

Maxell, Ltd., et al.,* v. Apple Inc.
Mayer Brown LLP, Washington D.C., USA
Expert Witness in Embedded Computer Architecture **2019 - 2021**
Case Subject Matter - Expert witness and consulting engineer in low power computing and power management.
Work Performed - Expert consulting, claim construction declaration, claim construction deposition, expert reports, infringement and validity depositions.

Nuvoton Technology Corporation* v. Microchip Technology Inc.
Finnegan, Henderson, Farabow, Garrett & Dunner, Washington D.C., USA
Expert Witness in Embedded Computer Architecture **2019 - 2020**
Case Subject Matter - Expert witness in embedded memory system hardware, direct memory access engines, memory controllers, and analog/digital and digital/analog ASICs.
Work Performed - Expert consulting, declarations, claim construction deposition, IPR declarations, deposition testimony.

Shuttlewagon Inc.*, v. Innovative Quality Solutions, LLC
Stroz Friedberg, Massachusetts, USA
Expert Witness in Embedded Computing **2019**
Case Subject Matter - Expert witness in Programmable Logic Controllers (PLCs), IEC 61131 IE / CodeSys and real-time computing as it pertains to industrial equipment, as well as misappropriation of proprietary technology.
Work Performed - Expert consulting.

RDM, Inc. v. Citoc Inc.*
Citoc Incorporated, Texas, USA
Expert Witness in Cloud / Web Based Computing **2019**
Case Subject Matter - Expert witness cloud deployed, web based, infrastructure management software and best practices in deploying solutions to consumers. Work Performed - Expert consulting.

ResMan, LLC v. Karya Property Management, LLC et al.*
Beck Redden LLP, Texas, USA
Expert Witness in Software Design **2019 - 2021**
Case Subject Matter - Expert witness in trade secret matters related to design and architecture of consumer facing software products.
Work Performed - Expert consulting, expert reports, depositions, trial testimony.

Qualcomm* v. Apple Inc.
Case No. 3:17-cv-02398-DMS-MDD
Quinn Emanuel Urquhart & Sullivan, CA, USA
Expert Witness in Mobile Devices and Computer Architecture **2019**
Case Subject Matter - Expert witness in mobile devices, computer architecture, and software system design for wireless communications.
Work Performed - Expert consulting.

Vasu Networks Corporation*
Skiermont Derby, Texas, USA
Consulting Expert in Cellular Network Technologies **2019**
Case Subject Matter - Consulting expert in matters related to Single Radio Voice Call Continuity, Dual Radio Voice Call Continuity, and various heterogeneous wireless technologies and standards

committees related to seamless connectivity.
Work Performed - Consulting expert.

Qualcomm* v. Apple Inc.
Case No. 37-2017-00041389-CU-BC-NC
Quinn Emanuel Urquhart & Sullivan, CA, USA
Expert Witness in Mobile Devices and Computer Architecture **2018 - 2019**
Case Subject Matter - Expert witness in mobile devices, computer architecture, and software system design for wireless communications.
Work Performed - Expert consulting.

Qualcomm* v. Apple Inc.
Inv No. 337-TA-1093
Quinn Emanuel Urquhart & Sullivan, CA, USA
Expert Witness in Mobile Devices and Computer Architecture **2017 - 2018**
Case Subject Matter - Expert witness in mobile devices, computer architecture, and software system design for wireless communications.
Work Performed - Expert consulting, expert reports, depositions, trial testimony.

Qualcomm* v. Apple Inc.
Quinn Emanuel Urquhart & Sullivan, CA, USA
Case No. 3:17-CV-1375-DMS-MDD
Expert Witness in Mobile Devices and Computer Architecture **2018 - 2019**
Case Subject Matter - Expert witness in wireless mobile devices, computer architecture, and software system design.
Work Performed - Expert consulting, expert reports, depositions, trial testimony.

Redzone Wireless LLC v. Netgear Inc.*
Bird Marella, CA, USA
Expert Witness in Wireless Hardware/Software Systems **2018 - 2019**
Case Subject Matter - Manufacturing of software and hardware used in wireless routers and base stations, including chipsets and software solutions.
Work Performed - Expert consulting, expert reports, depositions.

Nvidia* v. ZiiLabs Corporation
Quinn Emanuel Urquhart & Sullivan, NY, USA
Expert Witness in GPU Architecture, Computer Architecture **2018**
Case Subject Matter - Expert witness in the areas of Graphics Processor (GPU) architectures, memory systems architectures, and microprocessor design.
Work Performed - Expert consulting.

Acqis* v. EMC Corporation
Cooley LLP, CA, USA
Expert Witness in Computer Architecture **2017 - 2018**
Case Subject Matter - Expert witness in the areas of PCI, PCI-Express, system-on-chip technology, and computer memory technologies.
Work Performed - Expert consulting.

Qualcomm* v. Apple Inc.
Certain Mobile Electronic Devices and Radio Frequency and Processing Components Thereof, Inv No. 337-TA-1065
Quinn Emanuel Urquhart & Sullivan, CA, USA
Expert Witness in Mobile Devices and Computer Architecture **2017 - 2018**

Case Subject Matter - Expert witness in mobile devices, computer architecture, and software system design.
Work Performed - Expert consulting, expert reports, depositions.

Network Management Solutions* v. AT&T Mobility et. al
IP Law Leaders, Washington DC, USA
Expert Witness in Cellular Network Management **2017**
Case Subject Matter - Expert witness in mobile devices, wireless technology, 3GPP standards, and alarm management.
Work Performed - Expert consulting.

Certain Memory Modules and Components Thereof, and Products Containing Same, Investigation No. 337-TA-1023
Netlist* v. S.K. Hynix
Mintz Levin Cohn Ferris Glovsky and Popeo PC, Boston, MA, USA
Expert Witness in Computer Architecture and Memory Systems **2016 - 2017**
Case Subject Matter - Expert witness in the area of JEDEC standards essential DRAM memory module technology, relating to DIMM, R-DIMM and LR-DIMM as it applies to server based computing.
Work Performed - Expert consulting, source code review, declarations, expert reports, depositions, ITC trial testimony.

Certain Audio Processing Hardware, Software, and Products Containing Same, Inv. No. 337-TA-1026
Andrea Electronics Corporation*
Pepper Hamilton, LLP, Washington, DC, USA
Expert Witness in Audio Processing Hardware and Software **2017**
Case Subject Matter - Expert witness in hardware/software based digital signal processing systems audio processing and noise cancellation technology.
Work Performed - Expert consulting.

Specialized Monitoring Solutions, LLC v. Lutron Electronics Co., Inc.*
Vinson & Elkins LLP, Texas USA
Expert Witness in Embedded and Distributed Software Systems **2017**
Case Subject Matter - Expert witness in embedded software and hardware systems, as well as distributed data storage and sensing.
Work Performed - Expert consulting, claim construction analysis.

Huawei Technologies Co., Ltd.*, v. Samsung Electronics America, Inc. et al
Sidley Austin LLP, California USA
Expert Witness in 4G and Legacy Cellular Technologies **2016 - 2017**
Case Subject Matter - Expert witness in 4G and legacy cellular technologies.
Work Performed - Expert consulting, affidavits, claim construction.

Godo Kaisha IP Bridge 1* v. Broadcom Limited et. al
Ropes & Gray LLP, New York USA
Expert Witness in Computer Architecture **2016 - 2017**
Case Subject Matter - Consultant in the area of ARM based embedded computing architecture and system on-chip technology. Reverse engineering of VHDL, Verilog and RTL based technologies, as it pertains to multicore system architectures.
Work Performed - Expert consulting, source code review, claim construction.

Huawei Technologies Co. Ltd.* v. T-Mobile US, Inc. and T-Mobile USA, Inc.
Fish & Richardson P.C., Texas USA

Expert Witness in 4G and Legacy Cellular Technologies **2016 - 2017**
Case Subject Matter - Expert witness in 4G and legacy cellular technologies.
Work Performed - Expert consulting, claim construction, affidavits.

ACI Worldwide Corp. v. Mastercard International Incorporated*
Armstrong Teasdale LLP, Missouri, USA
Expert witness regarding financial transaction systems **2016 - 2017**
Case Subject Matter - Expert witness in trade secret misappropriation as it pertains to middleware message passing systems and financial transaction networks.
Work Performed - Expert consulting, source code review, declarations, expert reports, depositions.

Sony Computer Entertainment America v. Rothschild Digital Media Innovations*
Carey Rodriguez Milian Gonya, LLP, Florida, USA
Expert witness regarding distributed multimedia systems **2016**
Case Subject Matter - Expert witness in the area of distributed computing systems and multimedia technologies.
Work Performed - Expert consulting, declarations, expert reports, deposition testimony.

DTS, Inc., et al. v. Nero AG, et al.*
Glaser Weil Fink Jacobs Howard Avchen & Shapiro, Los Angeles CA, USA
Expert witness regarding distributed multimedia systems **2016**
Case Subject Matter - Expert witness in the area of software solutions for audio and video codecs.
Work Performed - Expert consulting, source code review, experimental analysis, expert reports, depositions.

Advanced Silicon Technologies*
Mintz Levin Cohn Ferris Glovsky and Popeo PC, Boston, MA, USA
Expert Consultant in Microprocessor Architecture, Intellectual Property **2015 - 2016**
Case Subject Matter - Consultant in the area of computer architecture and microprocessor technologies, specifically related to memory systems.
Work Performed - Expert consulting.

Certain Audio Processing Hardware and Software and Products Containing the Same, ITC Inv. No. 337-TA-949
Lenovo (United States), Inc.*
Toshiba Corp
Akin Gump Strauss Hauer & Feld LLP, Philadelphia, PA, USA
Expert Witness in Digital Signal Processing, Intellectual Property **2015 - 2016**
Case Subject Matter - Expert witness in hardware/software based digital signal processing systems tailored for noise cancellation technology.
Work Performed - Expert consulting, source code review, claim construction, expert reports, deposition.

Intel Corporation v. Future Link Systems*
Irell & Manella LLP, Los Angeles, CA USA
Expert Witness in Computer Architecture **2015 - 2018**
Case Subject Matter - Expert witness in the areas of PCI, PCI-Express, system-on-chip technology, and computer memory technologies.
Work Performed - Expert consulting, source code review, declarations, expert reports, deposition testimony.

Advanced Touchscreen and Gesture Technologies, LLC* v. Samsung Electronics, America, Inc., et al.
Robins Kaplan LLP, Intellectual Property, Minnesota, USA

Expert Witness in Mobile Devices and User Interfaces **2015 - 2017**
Case Subject Matter - Expert witness in the analysis and reverse engineering of software systems pertaining to mobile devices, and human computer interfaces.
Work Performed - Expert consulting, declarations, expert reports.

Intellectual Ventures* v. Ericsson et al.
Dechert LLP, Los Angeles, CA, USA
Expert Witness in 3GPP standards and LTE Technologies, Intellectual Property 2014 - 2016
Case Subject Matter - Expert witness in 3GPP standards as they pertain to LTE cellular communications networks, in addition to system hardware and software design.
Work Performed - Expert consulting, source code review, declarations, claim construction, tutorials.

Papst Licensing GMBH & Co. KG.*
DiNovo & Price Ellwanger Hardy, Austin, TX USA
Expert Witness in FPGA Technologies, Intellectual Property **2014 - 2016**
Case Subject Matter - Consultant in FPGA computing platforms and design flow processes, prior art, and infringement analysis.
Work Performed - Expert consulting, claim construction.

Locata LBS* v. Paypal Inc., et al.
Glaser Weil Fink Jacobs Howard Avchen & Shapiro, Los Angeles, CA, USA
Expert Witness in Geofencing Systems, Intellectual Property **2014 - 2015**
Case Subject Matter - Expert witness in geofencing technology, geolocational technology, and systems architecture as it pertains to mobile cellular telecommunications and enterprise software systems.
Work Performed - Expert consulting, claim construction, expert reports, deposition testimony.

Cell and Network Selection LLC v. ZTE*
Pillsbury, Winthrop Shaw & Pittman, San Diego, CA, USA
Expert Witness in 3G/4G Cellular Technology, Intellectual Property **2014 - 2015**
Case Subject Matter - Expert witness in technology pertaining to 3G, 3.5G, 3.75G and 4G wireless handset technology.
Work Performed - Expert consulting, claim construction, expert reports, deposition testimony.

CA Inc. D/B/A CA Technologies* v. AppDynamics, Inc.
Bracewell & Giuliani, Houston, TX, USA
Holland & Knight, Boston MA USA
Expert Witness in Enterprise Software Monitoring, Intellectual Property 2014 - 2015
Case Subject Matter - Expert witness in technology pertaining to dynamic runtime profiling of distributed software applications, specifically around Java and .NET technologies.
Work Performed - Expert consulting, source code review, declarations, expert reports, deposition testimony.

M Seven System Limited v. Leap Wireless International, Inc.* et al.
Glaser Weil Fink Jacobs Howard Avchen & Shapiro, Los Angeles, CA, USA
Expert Witness in 3G/4G Feature Phone Software Systems, Intellectual Property 2014
Case Subject Matter - Expert witness in the area of mobile telecommunications technology, particularly cellular handset hardware and software design.
Work Performed - Expert consulting, source code review.

Lunareye v. Passtime*.
Conley Rose, P.C., Austin, TX, USA
Expert Witness in GPS Tracking Solutions **2014**

Case Subject Matter - Expert witness in the area of mobile GPS tracking solutions software and hardware systems.
Work Performed - Expert consulting.

Certain Wireless Devices With 3G and/or 4G Capabilities and Components Thereof, ITC Inv. No. 337-TA-868
Interdigital, Inc.*
Wilson, Sonsini, Goodrich & Rosati LLP, Austin, TX, USA
Expert Witness in 3G/4G Cellular Techology, Intellecutal Property 2013 - 2015
Case Subject Matter - Expert witness in software systems and hardware systems, as they pertain to 3G/4G cellular communications and standards.
Work Performed - Expert consulting, source code review, claim construction, declarations, expert report, depositions, ITC trial testimony.

Investment Technology Group* v. United States Internal Revenue Services
Expert Witness in Financial Services Technology 2013
Case Subject Matter - Expert witness in the area of high performance software systems targeting financial market services.
Work Performed - Expert consulting, source code review, declarations, depositions.

Carrier Corporation v. Goodman Manufacturing*, et al.
Baker Botts LLP, Houston, TX USA
Expert Witness in Software and Hardware Systems, Intellectual Property 2013 - 2014
Case Subject Matter - Expert witness in the area of microprocessor based, serial distributed communications systems.
Work Performed - Expert consulting, source code review.

Gametek LLC* v. Facebook Inc. et al.
Collins, Edmonds, Porgorzelski, Schlather & Tower PLLC, Houston, TX USA
***Expert Witness in Mobile Gaming Technologies, Intellectual Property* 2013**
Case Subject Matter - Expert witness in internet based client-server software systems for mobile and web browser based gaming technology.
Work Performed - Expert consulting, source code review.

Ultimate Pointer LLC* v. Nintendo Co. LTD et al.
Conley Rose P.C., Houston, TX USA
Expert Witness in Console Based Video Game Technology, Intellectual Property 2013 - 2015
Case Subject Matter - Expert witness in hardware and software systems for console based video game technology.
Work Performed - Expert consulting, source code review, declarations, expert reports, deposition testimony.

Alliantgroup, L.P. v. Tax Point Advisors*
Jeffrey Feingold and Tax Point Advisors, Houston, TX USA
Expert Witness in Internet Technology 2013
Case Subject Matter - Expert witness in IP based internet technology, packet spoofing and information systems.
Work Performed - Expert consulting, declarations.

Kerry T. Thibodeaux, M.D. v. American Lifecare Inc.*
Cox, Cox Filo, Camel & Wilson, Lake Charles, LA USA
Expert Witness in Medical Software Systems 2013
Case Subject Matter - Expert witness in medical billing and expense recording enterprise software

systems.
Work Performed - Expert consulting.

Opelousas General Hospital Authority et al v. Fairpay Solutions Inc*
Cox, Cox Filo, Camel & Wilson, Lake Charles, LA USA
Expert Witness in Medical Software Systems **2013**
Case Subject Matter - Expert witness in medical billing and expense recording enterprise software systems.
Work Performed - Expert consulting.

Wi-LAN USA, Inc. and Wi-LAN, Inc.* v. Alcatel-Lucent USA Inc.
Vinson Elkins LLP, Dallas, TX USA
Expert Witness in 3GPP LTE Technology, Intellectual Property **2012 - 2013**
Case Subject Matter - Reverse engineering, analysis and education of counsel in the 3GPP LTE specification, and related software and hardware systems.
Work Performed - Expert consulting, source code review, claim construction, expert declarations.

Wi-LAN USA, Inc. and Wi-LAN, Inc.* v. Ericsson Inc., and Telefonaktiebolaget LM Ericsson
Vinson Elkins LLP, Dallas, TX USA
Expert Witness in 3GPP LTE Technology, Intellectual Property **2012 - 2013**
Case Subject Matter - Reverse engineering, analysis and education of counsel in the 3GPP LTE specification, and related software and hardware systems.
Work Performed - Expert consulting, source code review, claim construction, expert declarations.

E-Contact Technologies, LLC v. Dell Inc.*, et al.
Baker Botts LLP, Houston, TX USA
Expert Witness in Mobile Operating Systems, Intellectual Property **2012**
Case Subject Matter - Reverse engineering and analysis of the Android operating system as it pertained to mobile and tablet computing devices. Source code reverse engineering, system architecture and related analysis.
Work Performed - Expert consulting, source code review.

CheckFree Corporation* and CashEdge, Inc.* v. Metavante Corporation and Fidelity National Information Services, Inc.
Paul, Weiss, Rifkind, Wharton & Garrison LLP, New York, NY USA
Expert Witness in Banking and Billing Software Systems, Intellectual Property **2012**
Case Subject Matter - Software systems analysis and reverse engineering of large scale software based financial billing systems. Source code reverse engineering, claim chart generation, expert report generation and testimony.
Work Performed - Expert consulting, source code review.

Realtime Data, LLC v. NASDAQ*, Chase Bank*, Goldman Sachs* et al.
Proskauer Rose LLP, New York, NY USA
Expert Witness High Performance Software Systems, Intellectual Property **2012**
Case Subject Matter - Expert witness for joint defense counsel in the matter of large scale high frequency financial data aggregation platforms.
Work Performed - Expert consulting, claim construction, technical tutorials, declaration, expert reports, deposition testimony.

Realtime Data, LLC v. Thomson Reuters* et al.
Vinson & Elkins LLP, Austin, TX USA
Consultant in High Performance Software Systems, Intellectual Property **2011 - 2012**
Case Subject Matter - Expert witness for joint defense counsel in the matter of large scale high

frequency financial data aggregation platforms.
Work Performed - Expert consulting, claim construction, technical tutorials, declaration, expert reports, deposition testimony.

General Electric Co.* v. Mitsubishi Heavy Industries Ltd.
Weil, Gotshal & Manges LLP, Dallas, TX USA
Expert Witness in Hardware/Software Analysis, Intellectual Property 2010 - 2011
Case Subject Matter - Reverse engineering of real-time embedded system software source code and hardware system architecture pertaining to variable speed wind turbines and FPGA based subsystems.
Work Performed - Expert consulting, declarations, source code review.

Atlantic Specialty Insurance et al v. AE Outfitters Retail Company*, et al
Smith Mazure Director Wilkins Young & Yagerman, P.C., NY USA
Expert Witness in Embedded Hardware/Software Systems 2011
Case Subject Matter - Hardware and software system analysis of real-time networked embedded computing systems as it pertains to fire alarm infrastructure and fault handling.
Work Performed - Expert consulting, technical tutorial, expert declarations.

Gamestop*, Inc v. Bexar Appraisal
Brusniak and Blackwell PC, Dallas, TX USA
Expert Witness in Software Analysis, Intellectual Property Litigation 2011
Case Subject Matter - Expert witness on the tangibility of software as it pertains to embedded computing, networking, and gaming platforms.
Work Performed - Expert consulting, expert declarations.

Quality Analytic Systems, Inc. v. Zebec Data Systems*
Rymer, Moore, Jackson & Echols, P.C., Houston, TX USA
Expert Witness in Software Systems 2011
Case Subject Matter - Reverse engineering and software analysis of enterprise level internet based medical billing software systems.
Work Performed - Expert consulting, source code review, declarations, arbitration.

Passlogix, Inc. v. 2FA Inc.*
Expert Witness in Smart Card Middleware Solutions, Trade Secret Exposure 2010
Case Subject Matter - Trade secret analysis of software and systems architecture as it pertains to optimal selection of smart card middleware solutions on a given computer system.
Work Performed - Expert consulting, expert declarations.

Terra Nova Sciences*. v. JOA Oil and Gas, B. V. et al.
Abraham & Watkins et al. LLP, Houston, TX USA
Expert Witness in Software Systems, Intellectual Property Litigation 2010
Case Subject Matter - Expert software analyst of algorithms and geomechanics modeling systems as they pertain to oil well reservoirs.
Work Performed - Expert consulting, source code review.

Paltalk Holdings, Inc.* v. Sony Computer Entertainment America Inc. et al.
Heim Payne & Chorush LLP, Houston, TX USA
Software Analysis Expert, Intellectual Property Litigation **2010**
Case Subject Matter - Reverse engineering of internet based client-server video game console and server software architecture.
Work Performed - Expert consulting, source code review, infringement analysis.

Technomedia International, Inc.* v. International Training Services, Inc., et al.

Bracewell & Giuliani, LLP, Houston, TX USA
Expert Witness in Software Analysis, Contract Dispute **2010**
Case Subject Matter - Web enabled teaching materials as it pertains to oil well drilling. Analysis of internet based audio and video content delivery mechanisms and related website architecture.
Work Performed - Expert consulting, expert reports.

Gamestop, Inc* v. Bexar Appraisal
Brusniak and Blackwell PC, Dallas, TX USA
Expert Witness in Software Analysis, Tax Dispute **2009 - 2010**
Case Subject Matter - On the tangibility of software as it pertains to embedded computing, networking, and gaming platforms.
Work Performed - Expert consulting, expert reports.

Whetstone Electronics, LLC* v. Epson America, et al.
DiNovo & Price Ellwanger Hardy, Austin, TX USA
Expert Witness in System Analysis, Intellectual Property Litigation **2009 - 2011**
Case Subject Matter - Embedded computing systems pertaining to printer technology and computer hardware acceleration (microprocessors, DSP, FPGA and CPLD).
Work Performed - Expert consulting.

Whetstone Electronics, LLC* v. Xerox Corporation, et al
DiNovo & Price Ellwanger Hardy, Austin, TX USA
Expert Witness in System Analysis, Intellectual Property Litigation **2009 - 2011**
Case Subject Matter - Embedded computing systems pertaining to printer technology and computer hardware acceleration (microprocessors, DSP, FPGA and CPLD).
Work Performed - Expert consulting.

General Electric, Inc.* v. Mitsubishi Heavy Industries, Inc.
Vinson & Elkins LLP, Austin, TX USA
Expert Witness in Hardware and Software Analysis, Intellectual Property 2008 - 2009
Case Subject Matter - Real time embedded computing and hardware/software designs for variable speed wind turbines, including digital signal processing DSP and FPGA based subsystems.
Work Performed - Expert consulting, source code review, technical tutorials, declarations, expert reports, depositions, ITC trial preparation.

ecording enterprise software systems.
Work Performed - Expert consulting.

Wi-LAN USA, Inc. and Wi-LAN, Inc.* v. Alcatel-Lucent USA Inc.
Vinson Elkins LLP, Dallas, TX USA
Expert Witness in 3GPP LTE Technology, Intellectual Property **2012 - 2013**
Case Subject Matter - Reverse engineering, analysis and education of counsel in the 3GPP LTE specification, and related software and hardware systems.
Work Performed - Expert consulting, source code review, claim construction, expert declarations.

Wi-LAN USA, Inc. and Wi-LAN, Inc.* v. Ericsson Inc., and Telefonaktiebolaget LM Ericsson
Vinson Elkins LLP, Dallas, TX USA
Expert Witness in 3GPP LTE Technology, Intellectual Property **2012 - 2013**
Case Subject Matter - Reverse engineering, analysis and education of counsel in the 3GPP LTE specification, and related software and hardware systems.
Work Performed - Expert consulting, source code review, claim construction, expert declarations.

E-Contact Technologies, LLC v. Dell Inc.*, et al.

Baker Botts LLP, Houston, TX USA
Expert Witness in Mobile Operating Systems, Intellectual Property **2012**
Case Subject Matter - Reverse engineering and analysis of the Android operating system as it pertained to mobile and tablet computing devices. Source code reverse engineering, system architecture and related analysis.
Work Performed - Expert consulting, source code review.

CheckFree Corporation* and CashEdge, Inc.* v. Metavante Corporation and Fidelity National Information Services, Inc.
Paul, Weiss, Rifkind, Wharton & Garrison LLP, New York, NY USA
Expert Witness in Banking and Billing Software Systems, Intellectual Property **2012**
Case Subject Matter - Software systems analysis and reverse engineering of large scale software based financial billing systems. Source code reverse engineering, claim chart generation, expert report generation and testimony.
Work Performed - Expert consulting, source code review.

Realtime Data, LLC v. NASDAQ*, Chase Bank*, Goldman Sachs* et al.
Proskauer Rose LLP, New York, NY USA
Expert Witness High Performance Software Systems, Intellectual Property **2012**
Case Subject Matter - Expert witness for joint defense counsel in the matter of large scale high frequency financial data aggregation platforms.
Work Performed - Expert consulting, claim construction, technical tutorials, declaration, expert reports, deposition testimony.

Realtime Data, LLC v. Thomson Reuters* et al.
Vinson & Elkins LLP, Austin, TX USA
Consultant in High Performance Software Systems, Intellectual Property **2011 - 2012**
Case Subject Matter - Expert witness for joint defense counsel in the matter of large scale high frequency financial data aggregation platforms.
Work Performed - Expert consulting, claim construction, technical tutorials, declaration, expert reports, deposition testimony.

General Electric Co.* v. Mitsubishi Heavy Industries Ltd.
Weil, Gotshal & Manges LLP, Dallas, TX USA
Expert Witness in Hardware/Software Analysis, Intellectual Property **2010 - 2011**
Case Subject Matter - Reverse engineering of real-time embedded system software source code and hardware system architecture pertaining to variable speed wind turbines and FPGA based subsystems.
Work Performed - Expert consulting, declarations, source code review.

Atlantic Specialty Insurance et al v. AE Outfitters Retail Company*, et al
Smith Mazure Director Wilkins Young & Yagerman, P.C., NY USA
Expert Witness in Embedded Hardware/Software Systems **2011**
Case Subject Matter - Hardware and software system analysis of real-time networked embedded computing systems as it pertains to fire alarm infrastructure and fault handling.
Work Performed - Expert consulting, technical tutorial, expert declarations.

Gamestop*, Inc v. Bexar Appraisal
Brusniak and Blackwell PC, Dallas, TX USA
Expert Witness in Software Analysis, Intellectual Property Litigation **2011**
Case Subject Matter - Expert witness on the tangibility of software as it pertains to embedded computing, networking, and gaming platforms.
Work Performed - Expert consulting, expert declarations.

Quality Analytic Systems, Inc. v. Zebec Data Systems*
Rymer, Moore, Jackson & Echols, P.C., Houston, TX USA
Expert Witness in Software Systems **2011**
Case Subject Matter - Reverse engineering and software analysis of enterprise level internet based medical billing software systems.
Work Performed - Expert consulting, source code review, declarations, arbitration.

Passlogix, Inc. v. 2FA Inc.*
Expert Witness in Smart Card Middleware Solutions, Trade Secret Exposure **2010**
Case Subject Matter - Trade secret analysis of software and systems architecture as it pertains to optimal selection of smart card middleware solutions on a given computer system.
Work Performed - Expert consulting, expert declarations.

Terra Nova Sciences*. v. JOA Oil and Gas, B. V. et al.
Abraham & Watkins et al. LLP, Houston, TX USA
Expert Witness in Software Systems, Intellectual Property Litigation **2010**
Case Subject Matter - Expert software analyst of algorithms and geomechanics modeling systems as they pertain to oil well reservoirs.
Work Performed - Expert consulting, source code review.

Paltalk Holdings, Inc.* v. Sony Computer Entertainment America Inc. et al.
Heim Payne & Chorush LLP, Houston, TX USA
Software Analysis Expert, Intellectual Property Litigation **2010**
Case Subject Matter - Reverse engineering of internet based client-server video game console and server software architecture.
Work Performed - Expert consulting, source code review, infringement analysis.

Technomedia International, Inc.* v. International Training Services, Inc., et al.
Bracewell & Giuliani, LLP, Houston, TX USA
Expert Witness in Software Analysis, Contract Dispute **2010**
Case Subject Matter - Web enabled teaching materials as it pertains to oil well drilling. Analysis of internet based audio and video content delivery mechanisms and related website architecture.
Work Performed - Expert consulting, expert reports.

Gamestop, Inc* v. Bexar Appraisal
Brusniak and Blackwell PC, Dallas, TX USA
Expert Witness in Software Analysis, Tax Dispute **2009 - 2010**
Case Subject Matter - On the tangibility of software as it pertains to embedded computing, networking, and gaming platforms.
Work Performed - Expert consulting, expert reports.

Whetstone Electronics, LLC* v. Epson America, et al.
DiNovo & Price Ellwanger Hardy, Austin, TX USA
Expert Witness in System Analysis, Intellectual Property Litigation **2009 - 2011**
Case Subject Matter - Embedded computing systems pertaining to printer technology and computer hardware acceleration (microprocessors, DSP, FPGA and CPLD).
Work Performed - Expert consulting.

Whetstone Electronics, LLC* v. Xerox Corporation, et al
DiNovo & Price Ellwanger Hardy, Austin, TX USA
Expert Witness in System Analysis, Intellectual Property Litigation **2009 - 2011**
Case Subject Matter - Embedded computing systems pertaining to printer technology and computer hardware acceleration (microprocessors, DSP, FPGA and CPLD).
Work Performed - Expert consulting.

General Electric, Inc.* v. Mitsubishi Heavy Industries, Inc.
Vinson & Elkins LLP, Austin, TX USA
Expert Witness in Hardware and Software Analysis, Intellectual Property 2008 - 2009
Case Subject Matter - Real time embedded computing and hardware/software designs for variable speed wind turbines, including digital signal processing DSP and FPGA based subsystems.
Work Performed - Expert consulting, source code review, technical tutorials, declarations, expert reports, depositions, ITC trial preparation.

Paltalk Holdings, Inc.* v. Microsoft Corporation
Heim Payne & Chorush LLP, Houston, TX USA
Technical Expert, Intellectual Property Litigation 2007 - 2008
Case Subject Matter - Internet based client servere console gaming architecture for real time experience.
Work Performed - Expert consulting, source code review, technical tutorials.

Paltalk Holdings, Inc.* v. Microsoft Corporation
Heim Payne & Chorush LLP, Houston, TX USA
Technical Expert, Intellectual Property Litigation 2007 - 2008
Case Subject Matter - Internet based client servere console gaming architecture for real time experience.
Work Performed - Expert consulting, source code review, technical tutorials.

SuperSpeed Software, LLC* v. IBM Corporation
Heim Payne & Chorush LLP, Houston, TX USA
Technical Expert in Software Analysis, Intellectual Property Litigation 2007 - 2008
Case Subject Matter - Computer database technology, parallel file systems and clustered computing.
Work Performed - Expert consulting, technical tutorial, source code review.

QPSX Developments 5 Pty Ltd.* v. Juniper Networks, Inc.
Fulbright and Jaworski LLP, Houston, TX USA
Technical Consultant, Intellectual Property Litigation **2006 - 2007**
Case Subject Matter - Data transmission algorithms for computer networks.
Work Performed - Consulting, claim construction, claim chart preparation, technical tutorials.

Commonwealth Scientific and Indus. Research Org.* v. Buffalo Tech. Inc.
Fulbright and Jaworski LLP, Houston, TX USA
Technical Consultant, Intellectual Property Litigation 2006 - 2007
Case Subject Matter - High speed data rate network for wireless local area networks.
Work Performed - Consulting, claim construction, claim chart preparation, technical tutorials.

Microsoft Corporation v. Commonweatlh Scientific and Indus. Research Org.*
Fulbright and Jaworski LLP, Houston, TX USA
Technical Consultant, Intellectual Property Litigation 2006 - 2007
Case Subject Matter - High speed data rate communications for wireless local area networks.
Work Performed - Consulting, claim construction, claim chart preparation, technical tutorials.

Tantivy Communications, Inc.* v. Lucent Technologies, Inc.
Fulbright and Jaworski LLP, Houston, TX USA
Technical Consultant, Intellectual Property Litigation 2004 - 2005
Case Subject Matter - CDMA2000 based cellular networks, including data retransmission algorithms at multiple layers.
Work Performed - Consulting, claim construction, claim chart preparation, technical tutorials.

Volunteer Organizations

Rice Alliance for Technology and Entrepreneurship Austin, Texas, USA

Executive Committee **2009 - Present**
The Rice Alliance for Technology and Entrepreneurship strives to improve the entrepreneurial ecosystem of Central Texas by: helping entrepreneurs successfully found, fund, grow and exit new companies, helping investors successfully identify and engage with promising new ventures, and showcasing emerging technologies and business models to further educate and engage the community.

Capital Factory, TX USA
Mentor **2014 - Present**
Mentor, advisor and investor in one of the most successful start-up accelerators in the United States.

OwlSpark - Rice University, Houston, Texas, USA
Mentor **2014**
Mentor and advisor to university based early stage technology companies within Rice University's accelerator program.

Incubation Station, TX USA
Mentor **2013**
Incubation Station is an accelerator that brings together a consortium of Austins notable entrepreneurs, investors and advisors for the purpose of mentoring high-potential, market-validated consumer product companies to more effectively manufacture, distribute, market and grow their products and services.

Honors and Awards

Texas Instruments Fellowship Recipient
Nokia Grant Recipient
National Science Foundation Grant Recipient
Rice University Fellowship Recipient
Rensselaer Alumni Scholarship Recipient
Linear Tech / Mueller Scholarship Recipient
Rensselaer Polytechnic Institute: Graduated Cum Laude, Deans List All Semesters
Eta Kappa Nu - National Electrical and Computer Engineering Honors Society
IEEE Member - Institute of Electrical and Electronics Engineers (brogioli@ieee.org)

Petitioners
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