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PAPER

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SMART MODULAR TECHNOLOGIES (WWH), INC.,
Requester

v.

NETLIST, INC.,
Patent Owner

Appeal 2015-007761
Reexamination Control No. 95/001,758
United States Patent No. 7,864,627 B2
Technology Center 3900

Before JEFFREY B. ROBERTSON, DENISE M. POTHIER, and
JEREMY J. CURCURI, *Administrative Patent Judges*.

POTHIER, *Administrative Patent Judge*.

DECISION ON APPEAL

I. STATEMENT OF CASE

This proceeding arose out of a third party request by SMART Modular Technologies (WWH), Inc., for *inter partes* reexamination of U.S. Patent No. 7,864,627 B2 (“the ’627 patent”) to Jayesh R. Bhakta and Jeffrey Solomon, entitled *Memory Module Decoder* issued January 4, 2011 and assigned to Netlist, Inc.

We have jurisdiction under 35 U.S.C. §§ 134(b) and 315 (pre AIA).

Patent Owner appeals the decision in the Examiner’s Right of Appeal Notice (RAN) rejecting claims 2–12, 14–18, and 23–35 of the ’627 patent. App. Br. 2. Requester responded, disputing the Patent Owner’s contentions and supporting the Examiner’s decision. *See generally* Resp. Br. 5–18. Patent Owner filed a rebuttal brief. *See generally* Reb. Br.

The Examiner’s Answer incorporates the RAN by reference, which rejects claims 2–12, 14–18, and 23–35. RAN 1.

An oral hearing was conducted on December 11, 2015. The transcript of the oral hearing has been made of record.

We have been informed that the ’627 patent relates to (1) U.S. Patent Nos. 7,619,912, 7,532,537, 7,636,274, and 7,289,386 (the ’912, ’537, ’274, and ’386 patents, respectively), (2) merged reexamination Control Nos. 95/000,546 and 95/000,577 for the ’386 patent, which was appealed to the Board as Appeal No. 2014-007777, and where the rejection of pending claims was affirmed on February 25, 2015,¹ (3) reexamination Control No. 95/001,381 for the ’537 patent, which

¹ Subsequent to the decision, Patent Owner and Google Inc. filed their notices of appeal to the Federal Circuit on October 26, 2015 and October 30, 2015, respectively. On February 15, 2016, the appeal was dismissed. *Netlist, Inc. v. Google Inc.*, Nos. 16-1270 and 16-1271, slip op. at 1 (Fed. Cir. January 28, 2016).

was appealed to the Board as Appeal No. 2013-009066, and where the Examiner's decision to confirm the patentability of the claims was affirmed on January 16, 2014;² (4) reexamination Control No. 95/001,337 for the '274 patent, which has been reopened based on the Board decision dated January 16, 2014 (Appeal No. 2013-009044),³ (5) merged reexamination Control Nos. 95/000,578, 95/000,579, and 95/001,339 for the '912 patent which has been appealed to the Board as Appeal No. 2015-006849 and was heard on November 24, 2015, (6) various AIA proceedings, including IPR2014-00882, IPR2014-00883, and IPR 2014-01011,⁴ and (7) several court proceedings.⁵ App. Br. 1–2.

We AFFIRM rejections of claims 2–12, 14–18, and 23–35, designating some of rejections of claims 2–12, 14–18, 23–27, and 29–35 (Grounds 8–10) as new grounds.

Claims 1 (canceled), 6, and 12 read as follows with emphasis added:

1. A circuit configured to be mounted on a memory module so as to be electrically coupled to a first number of double data-rate (DDR) memory

² Subsequently, Requester appealed the Board decision to the Federal Circuit, which affirmed the Board's decision on November 13, 2015. *Inphi Corp. v. Netlist, Inc.*, 805 F.3d 1350 (Fed. Cir. 2015).

³ On January 16, 2014, the Board affirmed in part the proceeding for Control No. 95/001,377 and presented new grounds of rejection for various claims. The proceeding has been remanded to the Central Reexamination Unit.

⁴ *Diablo Techs., Inc. v. Netlist, Inc.*, Case IPR2014-00882, Paper No. 33 (PTAB December 14, 2015) (final written decision for U.S. Patent No. 7,881,150 B2), *Diablo Techs., Inc. v. Netlist, Inc.*, Case IPR2014-00883, Paper No. 33 (PTAB December 14, 2015) (final written decision for U.S. Patent No. 8,081,536 B1), and *Diablo Techs., Inc. v. Netlist, Inc.*, Case IPR2014-01011, Paper No. 34 (PTAB December 14, 2015) (final written decision for U.S. Patent No. 7,881,150 B2).

⁵ *Netlist, Inc. v. Inphi Corp.*, Case No. 2:09-cv-6900 (C.D. Cal.), *Netlist, Inc. v. Google, Inc.*, Case No. 4:09-cv-05718 (N.D. Cal.), and *Google, Inc. v. Netlist, Inc.*, Case No. 4:08-cv-04144 (N.D. Cal.), all stayed due to the reexamination proceedings.

devices arranged in a first number of ranks on the memory module, the memory module configured to be electrically coupled to a memory controller of a computer system so as to receive a set of input signals from the computer system, the set of input signals comprising row/column address signals, bank address signals, and chip select signals, the set of input signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit comprising:

a logic element configurable to receive the set of input signals;

a register; and

a phase-lock loop circuit configurable to be operatively coupled to the first number of DDR memory devices, the logic element, and the register,

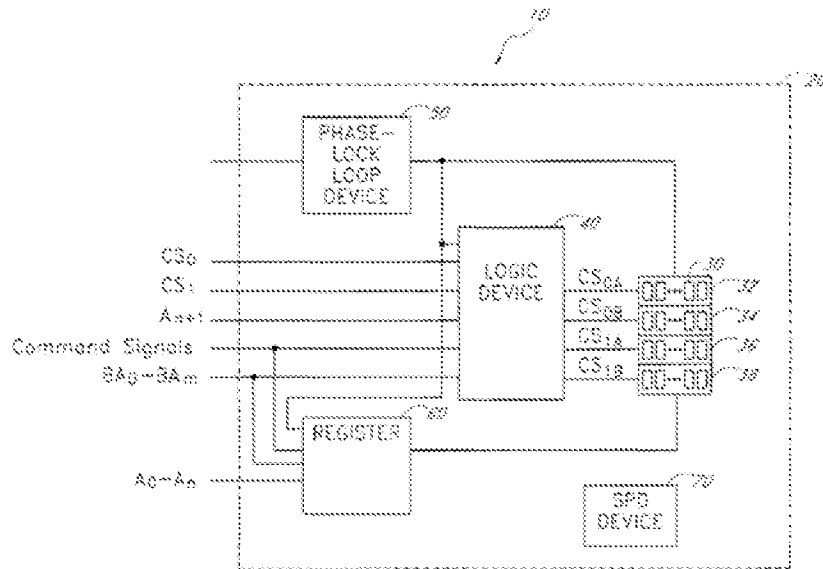
wherein the circuit is configurable to generate a set of output signals in response to the set of input signals, the set of output signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit is configurable to further respond to the set of input signals from the computer system by generating and transmitting the set of output signals to the first number of DDR memory devices.

6. The circuit of claim 1, wherein *the bank address signals of the set of input signals are received by both the logic element and the register.*

12. The circuit of claim 1, wherein *the circuit is configurable to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure.*

App. Br. 53, Claims App'x and '627 patent 32:42–33:2.

The '627 patent illustrates an exemplary memory module 10 in Figure 1A below:



Memory Module illustrated in Figure 1A

The '627 patent 3:33–35, 5:9–11; Fig. 1. Memory module 10 contains printed circuit board 20. Memory devices 30, phase lock loop (PLL) 50, logic element 40, and register 60 are coupled to printed circuit board 20. The '627 patent 5:11–17, 24–27; Fig. 1A.

Memory devices 30 are a first number of memory devices (e.g., 4 DDR devices). The '627 patent 5:14–15, 6:11–15; Fig. 1A. The logic element 40 receives input control signals that correspond to a second number of memory devices smaller than the first number of memory devices (e.g., 2). The '627 patent 5:16–20; Fig. 1A. Input control signals includes address signals, such as bank address signals (e.g., BA₀–BA_m), row address signals, column address signals, gated column address strobe signal, and rank or chip-select signals (e.g., CS₀ and CS₁), and command signals (e.g., refresh and precharge). The '627 patent 2:38–40, 6:52–58; Fig. 1A. Logic element 40 generates output control signals (e.g., CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B}) in response to the input control signals, the output control

signals corresponding to the first number of memory devices (e.g., 4). The '627 patent 5:20–23; Fig. 1A.

Additionally, in certain embodiments, the output control signals correspond to a first number of ranks (e.g., 4) in which the memory devices 30 are arranged. The '627 patent 6:61–63, 7:2. On the other hand, the input control signals correspond to a second number of ranks (e.g., 2) per memory module, for which the computer system is configured. The '627 patent 6:66–7:3, 7:17–22; Fig. 1A. The second number of ranks is smaller than the first number of ranks. *See id.* In such a scenario, memory module 10 simulates a virtual memory module, and this may occur when the number of memory devices 30 of memory module 10 is larger than the number of memory devices 30 per memory module the computer system is configured to use. The '627 patent 7:9–17. This arrangement can improve memory module performance, capacity, or both. The '627 patent 1:23–26.

As shown above in Figure 1A, the bank address signals, $BA_0 - BA_m$, are received by both register 60 and logic element 40.

In addition, Figure 2B shows logic element 40 that can save or latch an input control signal (e.g., A_{13}) during a row access procedure (e.g., column access strobe (CAS) high) at program logic device (PLD) 42 and can transmit this signal as an output control signal during a subsequent column access procedure (e.g., CAS low). The '627 patent 21:52–64; Fig. 2A. Figure 2B illustrates this below:

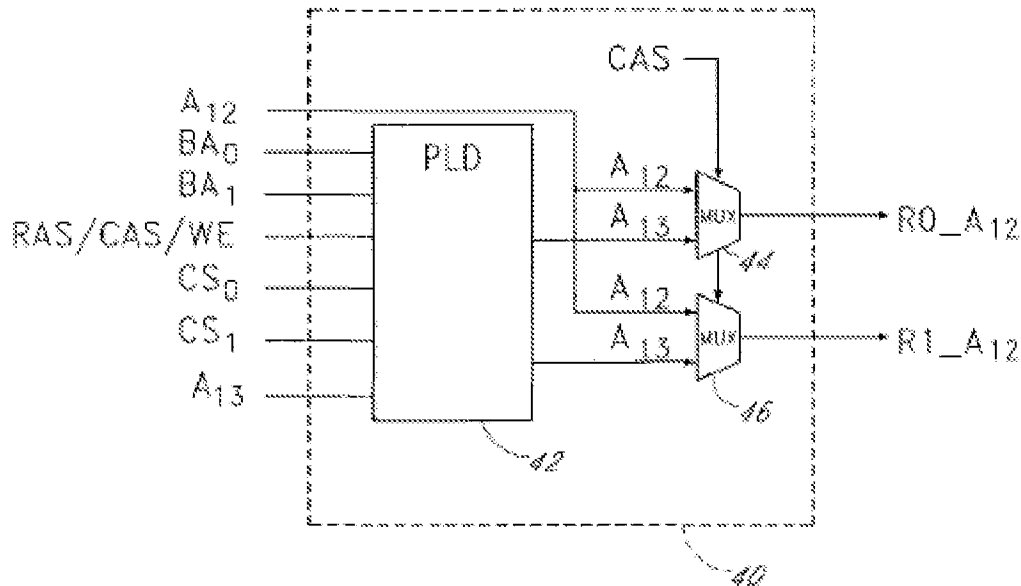


Figure 2B Showing Logic Element 40 with PLD 42 Storing Signals

The '627 patent 3:46–47; Fig. 2B. In this exemplary logic element, ranks 32 and 34 (shown in Figure 2A) interpret the previously-saved row address (e.g., A_{13}) as a current column address (e.g., A_{12}), and logic element 40 translates the extra row address into an extra column address. The '627 patent, 21:64–22:2; Fig. 2A–B.

Cited Prior Art

The Examiner relies on the following as evidence of unpatentability:

Dell (Dell)	US 5,926,827	July 20, 1999
Wong	US 6,414,868 B1	July 2, 2002
Dell (Dell 184)	US 6,446,184 B2	Sept. 3, 2002
Amidi	US 2006/0117152 A1	June 1, 2006 (filed Jan. 5, 2004)

JEDEC Standard No. 21-C, *PC2100 and PC1600 DDR SDRAM Registered DIMM, Design Specification*, Rev. 1.3 pages 4.20.4-1–4.20.4-82 (Jan. 2002) (JEDEC 21-C)

JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification JESD79C (Rev. of JESD79B) 1-75 (Mar. 2003) (JEDEC 79C)

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Control 95/001,758
Patent 7,864,627

JEDEC STANDARD, Definition of the SSTV16859 2.5 V 13-Bit to 26-Bit SSTL_2 Registered Buffer for Stacked DDR DIMM Applications, JESD82-4B (Rev. of JESD82-4A) 1-12 (May 2003) (JEDEC 82-4B)⁶

Pete Vogt, *Fully Buffered DIMM Server Memory Architecture: Capacity, Performance, Reliability, and Longevity* (2004) (Vogt).

The following Declarations are presented in this proceeding:

Declaration of Dr. Carl Sechen dated February 15, 2012 (Sechen Decl.),

Declaration of Dr. Carl Sechen dated March 19, 2013 (2nd Sechen Decl.),

Declaration of Dr. Carl Sechen dated November 26, 2013 (3rd Sechen Decl.),

Declaration of Dr. Nader Bagherzadeh dated September 6, 2011 (Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh dated March 15 2012 (2nd Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh dated April 18, 2013 (3rd Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh dated December 26, 2013 (4th Bagherzadeh Decl.).

Adopted Rejections

Patent Owner appeals the following rejections adopted by the Examiner:

⁶ Notably, JEDEC 21-C, JEDEC 79C, and JEDEC 82-4B are often referred to collectively as JEDEC or JEDEC standards in the presented rejections, the briefs, and declarations. *See, e.g.*, Sechen Decl. ¶¶ 8-9.

Reference(s)	Basis	Claims	RAN
Dell and JEDEC (Ground 2 ⁷)	§ 103	2, 3, 5, 7, 8, 10–12, 14–18, 23–32	6, 8–14
Dell, JEDEC, and Vogt (Ground 3)	§ 103(a)	9	6, 15–16
Wong and JEDEC (Ground 5)	§ 103(a)	2, 3, 5, 7, 8, 10–12, 14–18, 23–32	6, 17–22
Wong, JEDEC, and Vogt (Ground 6)	§ 103(a)	9	6, 23
Amidi and JEDEC (Ground 8)	§ 103(a)	2–8, 10–12, 14–18, 23–27, 29–35	7, 24–25
Amidi, JEDEC, and Vogt (Ground 9)	§ 103(a)	9	7, 26
Amidi and Dell 184 (Ground 10)	§ 103(a)	2, 3, 5–8, 10–12, 14–18, 23–27, 29–35	7, 26

App. Br. 9–10.

ISSUES ON APPEAL

We review the appealed rejections for error based upon the issues identified by Patent Owner in its appeal brief, and in light of the arguments and evidence produced thereon. *Cf. Ex parte Frye*, 94 USPQ2d 1072, 1075 (BPAI 2010) (precedential) (citing *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992)). “Any arguments or authorities not included in the briefs permitted under this section or

⁷ Throughout the documents in this proceeding, the Examiner, Patent Owner and Requester refer to the various rejections by ground number. *See, e.g.*, RAN 6. We include the ground number here and in the Opinion.

[37 C.F.R.] §§ 41.68 and 41.71 will be refused consideration by the Board, unless good cause is shown.” 37 C.F.R. § 41.66(c)(1)(vii).

Based on the arguments and evidence presented by Patent Owner, the main issues on appeal are whether the Examiner erred in determining that:

I. A. Dell and JEDEC teach or suggest “the storing limitations” recited in claims 2, 3, 5, 7, 8, 10–12, 14–18, and 23–32 and B. Dell, JEDEC, and Vogt teach or suggest the limitations in claim 9;

II. A. Amidi and JEDEC teach or suggest (1) “the bank address limitation” in claim 6 and (2) “the storing limitations” recited in claims 2–8, 10–12, 14–18, 23–27, and 29–35 and B. Dell, JEDEC, and Vogt teach or suggest the limitations in claim 9;

III. A. Amidi and Dell 184 teach or suggest the bank address limitation” in claim 6 and B. Amidi and Dell 184 teach or suggest “the storing limitations” recited in claims 2, 3, 5–8, 10–12, 14–18, 23–27, and 29–35?

ANALYSIS

I. Rejections based on Dell

A. Dell and JEDEC (Ground 2)

Claims 2, 3, 5, 7, 8, 10–12, 14–18, and 23–32 are rejected based on Dell and JEDEC. RAN 6, 8–14. Patent Owner argues claims 2, 3, 5, 7, 8, 10–12, and 14–18 as a group. App. Br. 22–37. We select as representative claim 12 (37 C.F.R. § 41.67(c)(1)(vii)), which recites “the circuit is configurable to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure.” At the outset, we note that this claim requires the circuit — separate from the recited DDR memory devices — to

be configurable to store an input signal without specifying the type of input signal stored or the location within the circuit where the signal is configured to be stored. Resp. Br. 17–18.

The Examiner finds that Dell teaches all the limitations in canceled claim 1, except for (1) the memory devices are double-data-rate (DDR) devices, (2) the circuit comprises a register, (3) the address signals comprise at least one row/column address signal, bank address signals, and chip-select signals, and (4) the memory module comprises a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of memory devices, the logic element, and the register. RAN 10. The Examiner turns to JEDEC to teach these missing features. RAN 10–11 (citing JEDEC 21-C, title page and 4.20.4-17, 18, and 29). For claim 12, the Examiner further cites to JEDEC 79C to teach that the bank addresses stored in Register 2 are used in row and column address procedures for the duration of the read/write cycle and cites to Dell to teach that the RAS signal is also used for the duration of a read/write cycle as well as A11 is latched. RAN 11 (citing JEDEC 79C 12 and Dell, Fig. 4 with latch 56 that stores A11).

Patent Owner does not contend that JEDEC when combined with Dell teaches DDR memory devices, a circuit having a register, and a memory module configured to receive the recited input address signals and having a PLL device mounted as recited and operatively coupled as recited. App. Br. 22–37; Reb. Br. 10–15. Rather, the arguments focus on whether JEDEC teaches or suggests a circuit configurable to store an input signal during a row access procedure for subsequent use during a column access procedure. *Id.* We thus confine our discussion to the points disputed by Patent Owner.

Specifically, Patent Owner contends that the Examiner repeatedly relies on the bank address signals in a memory module register in JEDEC 21-C to address the storing limitations. App. Br. 32; Reb. Br. 13–14 (citing RAN 10). As noted above, the Examiner relies on Dell’s Figure 4 and latch 56 and page 12 of JEDEC 79C in formulating the obviousness rejection for claim 12. RAN 11; Resp. Br. 11. Moreover, these teachings discuss storing signals other than bank address or RAS signals addressed by Patent Owner and its expert, Dr. Sechen. As such, even assuming that Patent Owner is correct that certain values that enter a memory device register are replaced every clock cycle such that they are not stored (*see* App. Br. 22–32, Sechen Decl. ¶¶ 15, 18–20; 2nd Sechen Decl. ¶¶ 53, 59), these arguments focused on how the bank address and RAS signals are treated within a register according to JEDEC 21-C do not consider the teachings of Dell and JEDEC 79C fully. App. Br. 22–32; Reb. Br. 13–15.

Requester refers to JEDEC 79C, contending that a row remains active until a PRECHARGE command is issued. Resp. Br. 16–17 (citing JEDEC 79C 12, *cited in* RAN 11). In particular, Requester asserts that the truth table (i.e., Truth Table 1a) illustrates that the active command activates a row and that this row remains active and is used (e.g., during a READ command) until a PRECHARGE command deactivates the row. Resp. Br. 16 (citing 2nd Bagherzadeh Decl. ¶ 30 (reproducing Truth Table 1a)). Furthermore, Requester contends that one skilled in the art would have understood from JEDEC 79C that the address bits (e.g., those associated with row address bits) are stored in a latch to keep the row active and are available to a register for use with the storing column address for the read access. Resp. Br. 16–17 (citing 4th Bagherzadeh Decl. ¶¶ 6, 8–9; JEDEC 79C 21–22).

We agree that JEDEC 79C at least suggests to one skilled in the art to store various inputs during a row access procedure for use later, including during a column access procedure. To illustrate this point, we refer to Truth Table 1a in JEDEC 79C. JEDEC 79C 12, *cited in* RAN 11 and *reproduced in* Sechen Decl. ¶ 13 and 2nd Sechen Decl. ¶ 30. JEDEC 79C shows an ACTIVE command (e.g., a row access procedure that activates a row), a READ command (e.g., a column access procedure), a WRITE command (e.g., a column access procedure), and a PRECHARGE command (e.g., a procedure that deactivates a row). *Id.*; *see also* 4th Bagherzadeh Decl. ¶ 6. Also, JEDEC 79C further explains that READ or WRITE commands occur after an ACTIVE command and “may be issued to *that* row” (JEDEC 79C 21 (emphasis added)); 4th Bagherzadeh Decl. ¶¶ 8–9, *cited in* Resp. Br. 17. JEDEC 79C even further discusses that a subsequent ACTIVE command to a different row in the same bank “can only be issued after the previous active row has been ‘closed’ (pre-charged).” *Id.* Thus, these teachings suggest to one skilled in the art to store row information (e.g., input signals related to active row) from the ACTIVE command for subsequent use during a READ or WRITE command so as to issue the READ or WRITE command to the correct or “that” row. JEDEC 79C 21; *see* Resp. Br. 16–17.

Additionally, some of the signals in Truth Table 1a or certain command/control signals are the same. *Id.* For example, each of an ACTIVE command (e.g., a row access procedure) and a READ command (e.g., a subsequent column access procedure) have the same bank address (e.g., Bank under ADDR) and chip select signals (e.g., L under CS). *Id.* Patent Owner also identifies Bank Y values that are the same for the ACT (e.g., active) and RD/WR (e.g., read/write) commands. App. Br. 24 (discussing Figure 9 of JEDEC 79C); *see also* JEDEC

79C 21. This truth table indicates to one skilled in the art that some signal values for both a row access procedure and a column access procedure are the same. Given that some of the values do not change between procedures (e.g., row and column address procedures), the teachings further suggest to an ordinary skilled artisan, when employing background knowledge and creative steps, that Dell's memory module can benefit (e.g., less processing) from storing unchanged values for later use. *See, e.g.,* Resp. Br. 16–17.

Patent Owner argues that the storage of a DDR command signal in the module register differs from the storage of the same signal in the DDR memory device. App. Br. 26–27. In essence, Patent Owner contends that JEDEC 79C stores a signal within the memory device and not within the recited circuit, which is separate from the memory device and at a different location. *See* App. Br. 26–27, 35–36. Patent Owner asserts that any stored information will be located in the mode registers within the control logic of JEDEC 79C's Figure 3, which is a functional block diagram of a DDR synchronous dynamic random access memory (SDRAM) (e.g., a memory device) and not a circuit separate from the memory devices as recited. JEDEC 79C 5, *reproduced in* App. Br. 26.

Although this figure shows a diagram of a memory device (e.g., a DDR SDRAM) and the mode register and the latch are located within this functional diagram, these components are separate from the actual memory banks. JEDEC 79C 5. Additionally, the rejection does not specifically propose to store input signals used later within the mode register (or latch) shown in Figure 3. *See* RAN 11; Resp. Br. 11. As Requester indicates, the rejection relies on JEDEC Standards as a whole. *See* Resp. Br. 15 (citing RAN 6), 19.

Importantly, the Examiner also relies on Dell and its teachings. RAN 11; Resp. Br. 11. Specifically, Dell show a logic element (e.g., 46) includes latch 56 that stores an address signal (e.g., A11) during read and write operations. Dell 5:29–30, 6:9–11, Fig. 4. The accompanying disclosure for Figure 4 discusses a logic element being located on chip (e.g., ASIC chip 46) separate from the memory storage (e.g., the memory devices). Dell 4:56–57, Figs. 3–4. Also, Dell teaches an address value (e.g., A11) is latched in address latch 56 (e.g., stored), and once latched, the address bit A11 is freed and not required to stay in its state during the entire operation. Dell 5:29–33, Fig. 4. That is, Dell teaches storing an input signal (e.g., A11) during the entire operation, including during ACTIVE and READ/WRITE operations, and that, as discussed above when addressing JEDEC, suggests storing signals until a row is deactivated. When considering such teachings collectively, we determine that one skilled in the art would have recognized including a circuit, separate from any memory device, to store an input signal during a row access procedure for subsequent use during a column access procedure.

Next, Patent Owner argues that Dell and JEDEC cannot be combined and are incompatible. App. Br. 37–41; Reb. Br. 16–17. Specifically, Patent Owner argues Dell performs asynchronous DRAM operations that are directed to EDO (Extended Data Out)⁸ technology and JEDEC performs synchronous DDR operations. *Id.* Given this distinction, Patent Owner asserts one skilled in the art would not have modified Dell’s memory device with JEDEC’s memory device.

⁸ Patent Owner relies on an article by Professor Bruce L. Jacob, entitled *Synchronous DRAM Architectures, Organizations, and Alternative Technologies* 5 (Dec. 10, 2002), in asserting this distinction. See App. Br. 39–40. Notably, this article was made of record in another proceeding. See App. Br. 28 n.1.

App. Br. 37–38 (citing Sechen Decl. ¶ 10; 3rd Sechen Decl. ¶¶ 39–44). Patent Owner further asserts that the Examiner relies on the “highly generic point” that both Dell and JEDEC discuss DIMMS (dual in-line memory modules) in determining that the teachings in Dell and JEDEC are combinable. App. Br. 39–41. In Patent Owner’s view, however, the references use disparate systems that are not combinable and one skilled in the art would have been deterred from combining as proposed because the technologies are not “backward-compatible.” *Id.* Patent Owner also contends that the timing and signaling differences between synchronous and asynchronous operations further demonstrate the incompatibility. App. Br. 41–43 (citing 3rd Sechen Decl. ¶¶ 51, 53, 62–63, 67–68).

We are not persuaded. First, as discussed above, the proposed combination of Dell and JEDEC, in the rejection, does not suggest replacing or modifying Dell’s DRAM operations. Rather, as discussed above, Dell teaches a location to store input signals that is separate from any memory device. Dell 4:56–57, 5:29–33, 6:9–11, Figs. 3–4. As such, JEDEC’s teachings in this regard (e.g., related to where to store input signals) are cumulative. Even so, JEDEC 79C further suggests to one skilled in the art storing certain input signals (e.g., chip select (CS) or bank address signals) within a circuit for later use until they are deactivated. JEDEC 79C 12. And even when combined, the rejection does not require any DRAM operation in Dell (e.g., read or write commands) to be modified. *See* Resp. Br. 18 (stating “combining . . . does not restrict [Dell] to the technology in the JEDEC Standard.”) Nor does the rejection necessitate storing the input signals within Dell’s DRAM. That is, the rejection does not propose modifying Dell’s memory devices themselves but rather storing an input signal within a circuit outside of the memory devices (e.g., Dell’s memory storage devices).

Second, although there may be differences between Dell and JEDEC's memory devices, we disagree that the combination as proposed would somehow be incompatible, such that one skilled in the art would have been discouraged from combining JEDEC's teachings with Dell. *See* App. Br. 39–41. Specifically, Patent Owner contends that mixing SDRAM and DDR DIMMS is not possible. App. Br. 40–41 (citing to an article by Hewlett-Packard, entitled *Memory technology evolution: an overview of system memory technologies* (2007)).⁹ Yet, as discussed previously, the rejection does not propose to mix such technologies. Thus, Dr. Sechen testimony related to the “huge technological hurdles” with substituting JEDEC 21-C's memory devices for Dell's is not directed to the rejection as proposed. 3rd Sechen Decl. ¶¶ 39–42. Moreover, the Examiner's statement that “it would have been obvious to design Dell's DIMM in compliance with the JEDEC standards” for compatibility purposes (RAN 11) does not indicate that the rejection proposed replacing the memory devices in Dell's DIMM with DDR memory devices as Patent Owner asserts. App. Br. 39–41; *see* 3rd Sechen Decl. ¶ 43. Rather, the rejection just proposes compliance of some sort.

Given the record, there is insufficient evidence presented by Patent Owner that the combined teachings as proposed would create a “barrier that prevents the Examiner's combination” or that one skilled in the art would have determined that JEDEC's DDR SDRAM technology would be “even less compatible” with Dell's purported DRAM technology. App. Br. 41.

Patent Owner also argues that the timing and signaling differences between synchronous and asynchronous operations make the proposed combination incompatible. App. Br. 41–43. As stated previously, the rejection does not

⁹ This article was made of record in another proceeding. *See* App. Br. 40 n.2.

propose to replace one asynchronous type of operations within Dell's memory devices for JEDEC's synchronous operations. Instead, as previously discussed, JEDEC is used to illustrate a suggestion, given certain known commands that exist in either technology (e.g., active, read, and write operations), to store certain values between row and column procedures. There is insufficient evidence in the record that applying JEDEC's teachings related to such commands and the information needed to process such commands within Dell's system would so alter or destroy Dell's memory module system. *See id.* Thus, Dr. Sechen's testimony in this regard (*see* Sechen 2nd Supp. Decl. ¶¶ 51, 53, 62, 63) is not probative.

Along with the above contentions, Patent Owner also specifically argues other features found in independent claim 23 — namely “the second set of output signals being generated using the saved density transition value.” App. Br. 46–51; Reb. Br. 19–21. Claims 24–32 depend directly or indirectly from claim 23. We select claim 23 as representative. For the arguments that repeat those already presented, we refer to our above discussion for details.

Concerning claim 23, the Examiner refers to the rejection of claims 1 and 12 (RAN 12) and additionally states Dell teaches a density transition value (RAN 13 (referring to A11 and citing Dell, Fig. 4)). Patent Owner also indicates that the rejection for Ground 2 based on Dell and JEDEC also relies on Requester's March 2012 Comments. App. Br. 47 (citing Requester's March 2012 Comments 24).

Patent Owner argues that the rejection of this claim is flawed because Dell does not discuss a column access procedure subsequent to row access procedure but rather teaches the opposite. App. Br. 48 (citing Dell 6:9–21). We are not persuaded. This disputed discussion in Dell addresses a CBR refresh cycle and not the previously discussed activate, read, or write cycles. *See* Dell 6:9–11.

Moreover, Patent Owner contends that “the A11-related signals of Dell [] would be held constant during a column access procedure subsequent to the row access procedure” App. Br. 48; Reb. Br. 19. Yet, as noted above, Dell states that once the address bit A11 value is latched (Dell 5:29–30), “the address bit A11 is freed and not required to stay in its state during the entire operation.” Dell 5:31–33. Accordingly, and contrary to Patent Owner’s position (App. Br. 48), this freed address bit and its ability to change its state suggests to one having ordinary skill in the art that the address bit can transition into other generated values (e.g., the claimed “density transition value”). *See* Dell 5:29–33.

Patent Owner further refers to the RAN and its discussion of November 2013 Comments. App. Br. 50–51 (citing RAN 30 and “Requester’s November 2013 Comments”). Concerning these comments, Patent Owner argues that the rejection relies on storing input signals in the DDR memory device of JEDEC 79C and refers back to its previous discussion surrounding this position. *See* App. Br. 51 (referring to Section VII. B.3).

However, the Examiner discusses the November 27, 2013 Comments only when addressing Patent Owner’s assertions and further refers to the *December 26, 2013* Comments to respond to these assertions. RAN 30 (citing December 26, 2013 Comments 3–13). In these Comments, the Requester discusses JEDEC’s teaching of latching row address bits so that they are active for a subsequent read or write command. *See* December 26, 2013 Comments 4–6 (citing JEDEC 79C, 1, 19; 4th Bagherzadeh Decl. ¶¶ 8–9). Granted, Figure 3 of JEDEC 79C shows the latch located within the memory device’s functional diagram (*see* December 26, 2013 Comments 5), but as noted previously, the latch is not part of the memory arrays. Also, as noted, the rejection does not require that the latch must be located

within the memory device. The December 26, 2013 Comments also discuss Dell's teaching to latch an input signal (e.g., A11) for an entire memory operation and indicates that these teachings must be considered in their entirety. *See* December 26, 2013 Comments 7–9, 14–15 (citing Dell 4:16–23, 28–35, 58–63, 5:29–33; JEDEC 79C, 19–22). We agree with Requester and refer to our above discussion.

Patent Owner further points to Requester's comments related to JEDEC standard being used to provide timing and duration of elements. Reb. Br. 21 (discussing Resp. Br. 25). As discussed above, Requester's comments are referring to JEDEC's teaching that one skilled in the art would have known or recognized a row access procedure (e.g., ACTIVE) occurring prior to a column access procedure and that suggests storing certain information during the entire operation. Moreover, as discussed above, the combined teachings of JEDEC and Dell suggest storing such information within a circuit outside of the memory devices. Thus, even if Patent Owner is correct that signals are stored within *memory device* registers for only one cycle (Reb. Br. 21), this contention does not rebut what the collective teachings suggest and predictably yield—a circuit configured to save certain values, including density transition values, during a row access procedure and generate a second set of output signals using the save transition value during a column access procedure subsequent to the row access procedure as recited in claim 23.

For the above-discussed reasons, we sustain the adopted rejection of claims 2, 3, 5, 7, 8, 10–12, 14–18, and 23–32 based on Dell and JEDEC (Ground 2) under § 103.

B. Dell, JEDEC, and Vogt (Ground 3)

Claim 9 is rejected based on Dell, JEDEC, and Vogt. RAN 6, 15–16. Claim 9 is not separately argued. *See* App. Br. 22–44. For the above reasons, we sustain the rejection of claim 9 and refer to the above discussion of Ground 2.

II. Rejections based on Amidi

A. Amidi and JEDEC (Ground 8)

The Examiner adopts the proposed rejection based on Amidi and JEDEC for claims 4, 6, 7, 12, 15, and 17 and further rejects claims 2, 3, 5, 8, 10, 11, 14, 16, 18, 23–27, and 29–35. RAN 7. The Examiner additionally refers to Ground 7, which is a rejection based on Amidi under § 102, when discussing the rejection for Ground 8. RAN 24. Even more, the Examiner provides an alternative basis for rejecting the claims that relies on the teachings of JEDEC 21-C and Amidi collectively. RAN 24–25.

Initially, Patent Owner contends that Amidi is the only reference relied upon in the adopted rejection for Ground 8. App. Br. 14. We are not persuaded because the rejection adopts that proposed by Requester (RAN 7), which relies on Amidi and JEDEC, as well as explicitly proposes an alternative rejection based on both Amidi and JEDEC (RAN 24–25). In particular, Requester’s Comments proposing to reject at least claims 4, 6, 7, 12, 15, and 17 based on Amidi and JEDEC were adopted by the Examiner (ACP 7 and RAN 7) who further explains how Ground 8 relies on the teachings of Amidi and JEDEC to teach both the storing and bank address limitations. *See* RAN 30–31 (incorporating Requester’s December 26, 2013 Comments 3–18 by reference when addressing Ground 8).

Moreover, even though the Examiner withdrew the rejection based on Amidi under § 102 (Ground 7)¹⁰ (App. Br. 14), the withdrawn rejection based on anticipation does not automatically withdraw the rejection based on § 103, which is under a different statutory basis. Granted, the Examiner states that the claims are obvious over Amidi “because these claims are anticipated by Amidi” (RAN 24), but as stated above, this is not the only basis for the obviousness rejection of the claims adopted or discussed by the Examiner. Also, although the Examiner states “Amidi does not expressly disclose the duration, for which the address bits are stored in the Register 608” (RAN 23–24), the Examiner has not also determined that Amidi does not teach or suggest the limitations of claim 6, for example, under obviousness.

Patent Owner argues the Examiner erred in adopting the proposed rejections based on Amidi, separately arguing the claims in two groups — (1) claim 6 which recites “the bank address signals of the set of input signals are received by both the logic element and the register” (the bank address limitation) and (2) claims 2–5, 7, 8, 10–12, 14–18, 23–27, and 29–35¹¹ which recite “the circuit is configurable to store an input signal of the set of input signals during a row access procedure for

¹⁰ The Non-Final Action mailed September 26, 2013 (Non-Final Act.) rejected claims 2, 3, 5–8, 10–12, 14–18, 23–27, and 29–35. Non-Final Act. 23–26. In the Action Closing Prosecution (ACP) mailed March 27, 2014, the Examiner withdrew the § 102 rejection of claims 6, 12, 15, 23–27, and 29–35 and stated the § 102 rejection of claims 2, 3, 5, 7, 8, 10, 11, 14, and 16–18 is not adopted. ACP 7, 23–24.

¹¹ Although Patent Owner includes claims 9 and 28 in the listing of rejected claims (*see e.g.*, App. Br. 22), these claims have not been included in Ground 8 by the Examiner. RAN 7, 24–25.

subsequent use during a column access procedure” or a similar limitation¹² (the storing limitation). *See, e.g.*, App. Br. 9–10. We in turn will address each group separately.

1. *Bank Address Limitation* (Claim 6)

Patent Owner argues that the Examiner erred in rejecting claim 6. App. Br. 10. Claim 6 depends from canceled claim 1 and further recites “the bank address signals of the set of input signals are received by both the logic element and the register” of the recited circuit. App. Br. 53, Claims App’x. As noted above, the Examiner adopted the Requester’s reasoning that relies on both Amidi and JEDEC to reject claim 6. *See* RAN 7, 24–25 and Requester’s December 26, 2013 Comments 15–18, *incorporated at* RAN 31 (when addressing claim 6).

When discussing Ground 8, Patent Owner contends that claim 6 is not taught by Amidi, because bank address signals are only received by the register as is conventionally known and Amidi’s complex programmable logic device (CPLD) (e.g., 410 in Fig. 4A) does not receive the bank address signals. App. Br. 14–15. Patent Owner admits Amidi’s CPLD receives an address signal (e.g., Add(n) or Add(n-1)) but contends that this signal is a row or column address signal, and “bank address signals are not treated in the same way as row and column address signals.” App. Br. 15. Yet, this argument overlooks that the Examiner has mapped the recited “logic element” to both Amidi’s CPLD 410 *and* Register 408 and the recited “register” to Register 418. RAN 24 (referring to Ground 7, which was last discussed in the September 26, 2013 Non-Final Act. 24¹³); Resp. Br. 4. Thus, even

¹² Requester indicates and we agree that claims 4, 12, 15, and 23 include similar limitations. Resp. Br. 9–10.

¹³ Although this portion of the Non-Final Action discusses canceled claim 1, claim 6 includes the limitation of claim 1.

if Patent Owner is correct that Amidi does not disclose a CPLD receiving bank address signals, Amidi shows a register (e.g., 608) receiving bank address signals. Amidi, Figs. 6A–B.

With respect to the Examiner’s mapping (*see* App. Br. 16), Patent Owner further argues that Amidi fails to teach a logic element and register receiving the bank address signals as recited. App. Br. 15–21. The Examiner relies on Figures 4A, 4B, and 6A to show the bank address signals being received by both the recited “logic element” (i.e., 410 and 408) and “register” (i.e., 418). RAN 24; September 26, 2013 Non-Final Act. 24, 26. The Examiner further states JEDEC 21-C discloses a DDR DIMM design specification that uses two registers, where in combination with Amidi, the recited “logic element” is CPLD 604 and JEDEC Register 2 and the recited “register” is JEDEC Register 1. RAN 24–25 (citing JEDEC 21C 4.20.4-18); Resp. Br. 7 (quoting this passage in the RAN). When combined, the Examiner finds that Amidi’s DIMM would be designed “according to JEDEC standard to have a marketable memory module that conforms to the industry standard.” RAN 25; Resp. Br. 5 (quoting this passage in the RAN).

Patent Owner argues that, following the JEDEC design standard set forth in JEDEC 21-C, only Register 2 — not Register 1 — would receive bank address signals. Reb. Br. 5. We agree. JEDEC 21-C shows a specific JEDEC design specification where certain signals are received by Register 1 and others are received by Register 2. JEDEC 21-C 4.20.4-18, *reproduced in part at* App. Br. 13, Reb. Br. 6, 2nd Sechen Decl. ¶ 19. This diagram shows that Register 2 receives both BA0 and BA1 and that the Register 1 receives no bank address signals. JEDEC 21-C 4.20.4-18. That is, combining this *specific* teaching with Amidi would result in only one of the two mapped registers receiving bank address

signals. Additionally, as Patent Owner indicates during prosecution, one examiner recognized that Register 1 in JEDEC 21-C does not receive bank address signals. Reb. Br. 6 (citing November 16, 2011 Office Act. 9).

Accordingly, the Examiner's proposed mapping (RAN 24-25) would result in only the recited "logic element," which includes Register 2, and not the recited "register," which is mapped to Register 1, receiving "the bank address signals of the set of input signals" as recited in claim 6.

But, the rejection also adopts the Requester's proposed rejection (RAN 7), which refers to Amidi's Figures 4A, 4B, and 6A to show the bank address signals being received by both the recited "logic element" (e.g., 410 and 408) and "register" (e.g., 418). RAN 24 (referring to Ground 7); September 26, 2013 Non-Final Act. 24, 26 (last discussing the basis for the rejection of Ground 7). The Examiner further incorporates Requester's December 26, 2013 Comments 15–18 in response to Patent Owner's contentions concerning claim 6. RAN 31. These comments discuss other parts of JEDEC 21-C, showing a register receiving bank address signals, such as the register shown in the lower left corner of the block diagram on page 4.20.4-13. Requester's December 26, 2013 Comments 16 (citing JEDEC 21C 4.20.4-13). Using this reasoning, there is no specific mapping of Register 1 or 2 to the recited logic element and the other of Register 1 or 2 to the recited register of claim 6. Rather, the rejection indicates both registers in Amidi (e.g., 408 and 418) behave like the register shown on page 4.2.4-13. *Id.*

Furthermore, under an obviousness analysis, we consider what ordinary skilled artisans would have recognized from Amidi's disclosure, when employing their inferences and creative steps. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S.

398, 418 (2007). To this end, Patent Owner asserts that one skilled in the art¹⁴ would not understand each of Amidi's Registers 408 and 410 in Figures 4A and 4B to be Register 608 in Figure 6A. App. Br. 16. More specifically, Patent Owner contends that one skilled in the art would have understood Registers 408 and 418 together constitute Register 608, like JEDEC 21-C shows as a single register box, and that only one of the two registers (e.g., 408 or 418 in Amidi's Figures 4A-B) receives the bank address signals when considered in the context of JEDEC design specifications. App. Br. 17–19. Patent Owner refers to Amidi, JEDEC 21-C, and Dr. Sechen's testimony to support this position. App. Br. 16–19 (citing Amidi ¶ 7; JEDEC 21-C, 4.20.4-16, 4.20.4-18, 4.20.4-33; 2nd Sechen Decl. ¶ 19; 3rd Sechen Decl. ¶¶ 17–19, 23, 26–28). Even more so, Patent Owner contends that there is no reason in Amidi to have each Register 408 and 418 be Register 608. App. Br. 20–21 (citing 3rd Sechen Decl. ¶ 29).

Amidi shows bank address signals are received by register 608 (e.g., BA[1:0]). Amidi, Fig. 6A. Unlike the address signals (A0-A11) that Amidi explicitly states are received by both registers 408 and 418 (Amidi ¶ 49), the accompanying disclosure in Amidi does not discuss whether the bank address signals are also received by both registers 408 and 418 shown in Figures 4A and B.

¹⁴ Notably, Dr. Bagherzadeh states “the level of skill in my opinion is a person with a degree in either electrical or computer engineering or in a closely related discipline, and would have taken courses in digital design or computer architecture. One of ordinary skill would further have at least 2 years of experience in designing computer memory systems and would have an understanding of industry standards adopted by Joint Electronic Devices Engineering Council (JEDEC).” Bagherzadeh Decl. ¶ 15. Dr. Sechen states he “adopt[s] the level of skill proposed by a requester for that reexamination” and discusses a similar credential list for an ordinarily skilled artisan. Sechen Decl. ¶ 10 (referring to the reexamination of related U.S. Patent No. 7,619,912).

See Amidi ¶¶ 37–42, 49. Rather, we must determine whether one skilled in the art would have recognized, based on Amidi and JEDEC’s teachings, both registers 408 and 418 receive bank address signals.

Dr. Sechen testifies that one skilled in the art would have recognized Figures 4A, 4B, and 6A in the context of JEDEC 21-C design specifications. 3rd Sechen Decl. ¶ 17. In this context, Dr. Sechen contends that register 608 shown in Amidi’s Figure 6A behaves the same as the register box in JEDEC 21-C, where only one register receives bank address signals, due to the same nomenclature. 2nd Sechen Decl. ¶¶ 18–19; 3rd Sechen Decl. ¶¶ 18–19, 26–28. On the other hand, Dr. Bagherzadeh testifies that one skilled in the art would have understood register 608 in Figure 6A represents both of registers 408 and 418. *See* 2nd Bagherzadeh Decl. ¶ 16.

We agree that the nomenclature of register in JEDEC 21-C (e.g., JEDEC 21-C, p. 4.20.4-12 and 16) is similar to register 608 in Amidi’s Figure 6A. *See* 3rd Sechen Decl. ¶ 18. Also, as Dr. Sechen indicates, JEDEC 21-C is a design specification for DDR SDRAM registered DIMMs, including 72-bit registered DIMMs. 2nd Sechen Decl. ¶ 18 (citing JEDEC 21-C, pp. 4.20.4-15–16). Amidi, in Figures 4A and B, also describes a 72-bit registered DDR module. Amidi ¶¶ 37, 42, Figs. 4A–B (describing “Transparent 72-bit Registered DDR Module”). Yet, there are differences between JEDEC 21-C and Amidi. For example, the register in JEDEC also includes two additional input signals, S0 and S1, which are described as chip select lines. JEDEC 21-C, 4.20.4-6. Amidi, in contrast, shows the chip select lines, cs0 and cs1, entering CPLD 604.

Additionally, Amidi addresses other differences between its memory module and those designs shown in JEDEC 21-C. One noted by Dr. Bagherzadeh (2nd

Bagherzadeh Decl. ¶¶ 13–14; 4th Bagherzadeh Decl. ¶ 20) includes that Amidi creates a transparent four rank memory module fitting into a memory able to take inputs for a two-rank memory module. *See* Amidi ¶¶ 1, 4, 8, 11–12, 49. JEDEC 21-C design examples do not discuss such a transparent four rank memory module. *See generally* JEDEC 21-C. Another example previously discussed includes Amidi stating “address lines A0-A11 go to module *register 408 and 418* and address lines A12 goes into CPLD.” Amidi ¶ 49 (emphasis added). Amidi also shows address signals Add[n-1:0] (e.g., A0-A11) entering register 608 in Figure 6A and Add(n) (e.g., A12) entering CPLD 604. *Id.* at Fig. 6A. Importantly, this design deviates from JEDEC 21-C design specifications, which shows the different address signals inputted into registers 1 and 2. JEDEC 21-C, 4.20.4-18.

Thus, the record establishes distinctions between Amidi and the JEDEC 21-C design specifications that one skilled in the art would have recognized. As such, we agree with Requester’s assertion that Amidi is not a technology restricted to JEDEC design standards. Resp. Br. 8. For these reasons, we disagree with Dr. Bagherzadeh’s statement that “Amidi discloses JEDEC dual in-line memory module (DIMM)” in all its aspects. *See* 2nd Bagherzadeh Decl. ¶ 14, *cited at* App. Br. 17. Additionally, other than Amidi referring to the JEDEC standard when discussing fitting TSSOP (thin-shrink small outline package) placements per side or per module based on “defined height limits” (Amidi ¶ 7), Amidi has examples of its memory module design that do not comport with JEDEC design specifications and do not discuss any other such restriction to adhere to JEDEC standards (*see generally* Amidi). Thus, although an ordinary skilled artisan would have *consulted* with the JEDEC design specifications, including JEDEC 21-C,

when designing a circuit for a memory module or DIMM, Amidi discloses that its design deviates from JEDEC design specifications in various ways.

When considering these teachings of Amidi, Amidi suggests that register 608 represents both registers 408 and 418 in Figures 4A and B. For example, Amidi discloses address lines A0 through A11 enter registers 408 and 418. Amidi ¶ 49, Fig. 6A. Amidi's Figure 6A shows various other signal lines entering register 608, including bank address signal lines (e.g., BA[1:0]). Amidi, Fig. 6A. Following from above, Amidi Figure 6A thus suggests to one skilled in the art that both registers 408 and 418 may receive additional signals as shown entering register 608, including bank address signals. *See id.*

Also, one having ordinary skill is not an automaton and would have employed their background knowledge and creative steps when designing memory modules. That is, one skilled in the art would have recognized that memory modules that explicitly differ from JEDEC design specifications, such as Amidi's (e.g., emulating a two rank memory module on a four-rank memory module), may affect the memory module in other ways and require further unspoken differences, including other signals being received by registers or CPLD in Amidi. For instance, one skilled in the art would have recognized directing other signals, including bank address signals, to Amidi's two registers or its CPLD can further assist in emulating a two rank memory module in a four rank memory module in a cost effective and flexible manner. *See Amidi* ¶¶ 11, 23, 41, 49, 57, 59, 62, Fig. 7.

And even if one skilled in the art would have consulted with JEDEC 21-C designs, JEDEC 21-C itself teaches the ordinarily skilled artisan that modifications to the reference design may be required. Also, JEDEC 21-C does not state its design specifications are sufficient for all types of memory modules. Specifically,

JEDEC 21-C discusses reference design examples as “an initial basis for Registered DIMM designs” but further clarifies that modifications to the reference designs may be required to meet “all system timing, signal integrity, and thermal requirements.” JEDEC 21-C, 4.20.4-5.

Accordingly, when comparing JEDEC 21-C with Amidi, an ordinary skilled artisan would have recognized Amidi’s memory module design differs from JEDEC reference designs and that modification from the JEDEC reference designs would need to occur. JEDEC 21-C, 4.20.4-5. These modifications suggest signals other than address signals (e.g., bank address signals) being received by Amidi’s registers and CPLD to meet system timing, signal integrity, and thermal requirements. And combining the teachings in Amidi at least suggest to an ordinary skilled artisan that signals other than the explicitly-disclosed address signals A0-A11, such as bank address signals BA0 and BA1, are received by each of registers 408 and 418 or CPLD 604 in a similar fashion. We therefore disagree with Patent Owner that “there would be no suggestion or motivation in Amidi to have each of Registers 408 and 418 be Register 608” or that “duplication [of the register] would not make any sense.” App. Br. 20 (citing 3rd Sechen Decl. ¶ 29); *see* Resp. Br. 7–8.

When considering (1) Amidi deviates from JEDEC design specifications in multiple ways, including (a) emulating a two rank memory module using a transparent four rank memory module, (b) receiving address signals A0–A11 at registers 408 and 418, and (c) diverting its chip-select signals to a logic element; (2) the suggestion in Amidi that one skilled in the art would have recognized based on deviations from JEDEC design specifications that signals other than address signals also enter Amidi’s register shown in Figure 6A; and (3) the background

knowledge and creative steps an ordinarily skilled artisan would have employed given Amidi's teachings and suggestions alone or in combination with JEDEC, we determine that one skilled in the art would have recognized using bank address signals received by both registers (e.g., one mapped to the recited "register" and the other mapped to the recited "logic element") or a CPLD to account for the design requirements of Amidi and preferences of the artisan. To the extent that changes are needed to Amidi to connect signals other than row/column address signals, including bank address signals, to the registers, such a change permits the logic circuit designer the flexibility to design a logic circuit for "other families of memory devices or densities of memory devices" used to build the four rank memory module (Amidi ¶ 71; *see also* 2nd Bagherzadeh Decl. ¶ 14) and so that the registers to meet system timing, signal integrity, and thermal requirements (JEDEC 21-C, 4.20.4-5).

Patent Owner contends that bank address signals entering both registers (e.g., 408 and 418) implies duplication of the register function and that this duplication makes no sense to one skilled in the art when considering power and dimensional requirements as well as the increase costs. App. Br. 20–21 (citing 3rd Sechen Decl. ¶¶ 29–34). For support, Dr. Sechen testifies that an ordinarily skilled artisan would have been aware of dimensional requirements for JEDEC modules, including height requirements discussed by Amidi, and that given these concerns, one would not have understood Amidi suggests each register 408 and 418 to be the entire register function. 3rd Sechen Decl. ¶¶ 30–31.

Although we appreciate Dr. Sechen's perspective, we are not persuaded. First, the above discussions concerning Amidi, and what one of ordinary skill in the art would have understood from Amidi, teach input address signals are received

by both registers 408 and 418. *See* Amidi ¶ 49, Fig. 6A. Also, these teachings in Amidi do not require that the *entire* register function be duplicated in each of registers 408 and 418.

Second, even if duplicated in its entirety, Amidi's statement related to considering the "standard defined height limits by JEDEC" for TSSOP placement per side and per module (Amidi ¶ 7) does not require compliance in other design aspects as previously discussed. Third, there is inadequate evidence in the record between the height or dimensional requirements discussed in Amidi that are according to JEDEC specifications (*id.*) and how Dr. Sechen concludes that this sole dimensional requirement would lead an ordinarily skilled logic circuit designer not to understand Amidi suggests each of registers 408 and 418 to receive at least some of the signals shown in Figure 6A entering register 608. *See* 3rd Sechen Decl. ¶¶ 30–31.

Dr. Sechen further discusses the power requirements that would result from each register 408 and 418 if duplicated. 3rd Sechen Decl. ¶¶ 32–34. In particular, Dr. Sechen states that one skilled in the art would have concluded that two registers behave as a single register according to JEDEC design specifications so as to "minimize power." 3rd Sechen Decl. ¶ 34. To be sure, power consumption would be a factor to an ordinarily skilled artisan when designing a memory module. However, as explained above, Amidi does not possess a traditional JEDEC logic circuit design and requires modifications from JEDEC design specifications. Thus, although we appreciate Dr. Sechen's insights that "JEDEC 21-C at page 4.20.4-62 explains that a single Register (comprising Registers 1 and 2) is sufficient to handle a module having 36 DDR DRAM devices in a stacked arrangement" (3rd Sechen Decl. ¶ 33), we are not persuaded sufficiently that any

increased power consumption in Amidi resulting from directing bank address signals to both registers 408 and 418 would be unworkable.

Even if more power is consumed in Amidi's memory module when the registers are duplicated, balancing the relative advantages (e.g., flexibility of using less expensive chips) and disadvantages (e.g., increased power consumption) are engineering tradeoffs well within the level of ordinarily skilled artisans. That is, Amidi teaches creating a transparent four rank memory module that fits into a memory socket having two chip select signals (e.g., emulating the function of a two rank memory module) because such lower density memory devices are cheaper and more readily available. *See* Amidi ¶¶ 1, 4, 8, 11–12. The record thus supports that a logic circuit designer employing his or her background knowledge would have considered various design factors (e.g., cost, loading, power consumption) when designing a memory module.

Notably, Requester asserts that the registers perform some type of logic. *See* Resp. Br. 5 (stating “registers including logic circuitry.”) Patent Owner does not dispute this determination. *See generally* App. Br. and Reb. Br. As such, the record includes a finding that a register is itself “a logic element” as recited. To the extent this issue is in dispute, we refer to the discussion in the opinion of Appeal No. 2015-006849 concerning how “a logic element” is broadly, but reasonably, construed.

For the above-discussed reasons, we sustain the rejection of claim 6 based on Amidi and JEDEC (Ground 8) under § 103. However, to the extent that our analysis differs from the outstanding rejection, we designate this rejection a new ground pursuant to 37 C.F.R. § 41.77(b).

2. *The Storing Limitations* (Claims 2–5, 7, 8, 10–12, 14–18, 23–27, and 29–35)

Patent Owner argues the claims having storing limitations as a group. App. Br. 22–37. We select claim 12 as representative and, as noted previously, this claim requires the circuit is configurable to store an input signal without specifying the type of input signal stored or the location within the circuit where the signal is configured to be stored. To reiterate, claim 12 recites “the circuit is configurable to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure.”

Some arguments proffered by Patent Owner repeat those discussed above concerning JEDEC and conventional command operations within DDR memory devices as recited. *See, e.g.*, App. Br. 23–31. We are not persuaded and refer to our previous discussion addressing Ground 2 based on Dell and JEDEC. We further determine that one skilled in the art would have recognized that Amidi’s input signals into circuit components of its memory module (e.g., CPLD 604 or register 608) deviate from at least some of JEDEC’s design conventions as previously discussed. Even more, we note that the rejection is based on the teachings of both Amidi *and* JEDEC. Thus, individual attacks on JEDEC or Amidi are not persuasive.

To teach the storing limitations, the Examiner states the claims are rejected based on Amidi and JEDEC standards (RAN 7) and refers to Ground 7 (RAN 24). When last addressing Ground 7, the Examiner states:

bank addresses BA[1:0] stored in the registers are used in row and column address procedures, see Figure 6, 608 [of Amidi]; input signal RAS is also stored in registers and transmitted as an output control

signal rRAS). RAS signal is used for the duration of a read/write cycle (see IBM Application Note: Understanding DRAM Operation, 1996).

September 26, 2013 Non-Final Act. 25.

Subsequently, the Examiner determined that “‘Amidi does not expressly disclose the duration, for which the address bits are stored in the Register 608’. [sic] Consequently, the claims are not anticipated by Amidi.” RAN 23–24. Presumably, this statement indicates that, although Amidi may store the address bits at some point, Amidi does not demonstrate that it *necessarily* stores the input signal for duration that includes “during a row access procedure for subsequent use during a column access procedure.”¹⁵ However, the Examiner also does not state that Amidi fails to suggest such a feature under an obviousness analysis.

As indicated above, Requester’s Comments proposing to reject at least claim 12 based on Amidi and JEDEC were adopted by the Examiner (ACP 7 and RAN 7) and further explains how Ground 8 relies on the teachings of Amidi and JEDEC collectively to teach the storing limitation. *See* RAN 30 (incorporating by reference Requester’s December 26, 2013 Comments 3–13 with the exception of withdrawing the anticipation rejection (Ground 7)), 25 (indicating April 18, 2013 Requester’s Comments 12–13 are persuasive for claim 4). As discussed above when addressing Ground 2 based on Dell and JEDEC, JEDEC 79C teaches and suggests storing (e.g., latching) input signals from a row access procedure for subsequent column access procedure. Requester’s December 26, 2013 Comments

¹⁵ When discussing Grounds 3–6, 13, and 19, the Examiner states “none of the rejections . . . were based on the IBM Note” and “references to the IBM note” are excluded from the “explanation of the rejections.” ACP 29. The Examiner does not make a similar statement for Grounds 8–10.

3–5 (citing JEDEC 79C 1, Fig. 3; Bagherzadeh Decl. ¶ 9). So as not to be repetitive, we refer to our previous discussion for more details concerning these portions of JEDEC 79C.

For this rejection (Ground 8), we also consider Amidi and its teachings. Requester’s December 26, 2013 Comments 12–13.¹⁶ In particular, Requester emphasizes that Amidi teaches (1) a four-rank memory module that takes input signals meant for a two-rank memory module, (2) has a CPLD (e.g., 410, 604) that receives input signals (e.g., address signals) and generates output signals accessible to four ranks, (3) row address signals are provided and on a separate cycle column address signals are provided, and (4) address signals (e.g., Add[n-1:0]) are stored in registers during row addressing. *Id.* at 12–13 (citing Amidi, ¶¶ 3, 12, 52, 61, Fig. 6A); Resp. Br. 12–13. When combining this teaching with JEDEC’s discussion of latching row address bits for later use as discussed above, the rejection proposes that the combined memory module yields a circuit configurable to store an input signal during a row access procedure for subsequent use during a column access procedure. Requester’s December 26, 2013 Comments 13.

Concerning the cited and discussed portions of Amidi, Amidi discusses emulating a two rank memory module with a four rank memory module. Amidi ¶ 12. To achieve this emulation, Amidi discusses generating signals (e.g., rcs0–rcs3) that exit CPLD 604 from the input signals (i.e., CS0, CS1, and Add(n)) to “ensure[] that all command for a two rank memory module . . . are also performed on the four rank memory modules.” Amidi ¶ 52. Amidi discusses generating rcs2

¹⁶ The heading on page 12 of the comments states “Amidi In View of Wong Teaches The Storing Limitation,” but the substance of this section discusses Amidi and JEDEC. *See* Requester’s December 26, 2013 Comments 12–13. We presume the reference to Wong is a harmless, typographical error.

and rcs3 signals, besides rcs0 and rcs1, when various CS0 and CS1 commands are issued (e.g., Auto Precharge all Banks, Auto Refresh, Load Mode Register). *Id.* Yet, this portion of Amidi does not explicitly state the input signals (e.g., CS0, CS1, or Add(n)) are stored in part of the circuit (e.g., CPLD) during a row access procedure for later use during a column access procedure.

Amidi specifically discusses internal circuitry within a CPLD for Row Address Decoding (e.g., a row access procedure) and Column Address Decoding (e.g., a column access procedure). Amidi ¶ 61,¹⁷ cited in Resp. Br. 12-13, Request 689, and April 18, 2013 Requester's Comments 12–13. Here, Amidi states the column address decoding scheme is unique, requiring two sets of addresses rather than the standard DDR memory module where only one set of address lines is required in order to access a cell. Amidi ¶ 61. Amidi even further states the first set includes the Row address provided with proper control and command signals and the second set, on a separate cycle, includes the Column address provided with its proper control and command signals in order to read or write “to that particular cell.” *Id.*

Although both the row and the column address require “control and command signals” (*id.*; see R2 Resp. Br. 12–13), Amidi does not discuss explicitly storing the proper control and command signals (e.g. input signals) during a row access procedure that are used later during a column access procedure. Amidi ¶ 61. Nonetheless, one skilled in the art armed with this teaching in Amidi would recognized that in order to read or write to *a particular cell* from one step (e.g., a row address) to another step (e.g., a column address) that at least some data would either need to be repeated or stored for later use. *See id.* That is, there are a finite

¹⁷ Requester cited wrong paragraph 60 of Amidi.

number of identified, predictable solutions (e.g., repeat or store value) for using the same signal values from one procedure to another (e.g., row to column) and one skilled in the art would have reasons to pursue these known options (e.g., design and processing considerations) in order to read or write to the correct cell at the column address step.

This is further illustrated in Amidi's Figures 6A and 6B that show some of the same signals (e.g., cs0, cs1, CAS, RAS, WE) being used in both the row and column decoding processes. Amidi, Figs. 6A–B. Thus, one skilled in the art would have recognized that some of the same signals are used in both cycles and an artisan would have a good reason to store these signals in order to read or write to the correct cell. *See* Amidi ¶ 61, Figs. 6A–B. Also, as discussed above, JEDEC 79C further demonstrates in Truth Table 1a that the same signals have the same values between row and column access procedures. JEDEC 79C 12. Patent Owner also identifies Bank Y values that are the same for the ACT (e.g., active) and RD/WR (e.g., read/write) commands. App. Br. 24 (discussing Figure 9 of JEDEC 79C). When combining these teachings, the combination suggests to one skilled in the art storing certain signals during a row access procedure for subsequent use during a column address procedure, as recited in claim 12, so that the correct cell is acted upon in each procedure.

Additionally, we determine that Amidi's teaching suggests that the *proper* control and command signals to read or write to the particular cell (e.g., address and bank address signals) would involve at least some of the same signals received during the row address decoding step, when applying the background and creative steps one skilled in the art would have employed. As such, one skilled in the art would have recognized that some efficiencies are to be gained from designing a

circuit that stores input signal values during a row access decoding procedure that repeat *later* during a column access decoding procedure.

Regarding JEDEC 79C, Patent Owner argues that this reference teaches latching or storing a signal internal to a memory device and not a circuit separate from the memory device. App. Br. 26–27, 34–36. We are not persuaded and refer to our previous discussion of this argument related to JEDEC 79C when addressing the rejection based on Dell and JEDEC. Moreover, Amidi teaches circuitry (e.g., CPLD 604 and register 608) separate from the memory device (e.g., Amidi, Figs. 6A–B shows signals from CPLD and register go to the memory devices), where, as discussed above, Amidi and JEDEC collectively suggests storing input signals for later use during a column access procedure. Thus, when combined, the rejection does not propose to store the input signals within the memory device discussed in JEDEC 79C or any other memory device. Nor does the rejection propose to modify Amidi’s memory devices, but rather to store input signals within a circuit outside of the memory devices (e.g., Amidi’s CPLD or elsewhere prior to signals being sent to the memory devices as shown in Figures 6A and B).

Finally, arguments concerning incompatibility of EDO-based versus DDR technology are not applicable to this ground (Amidi and JEDEC). App. Br. 39–43. That is, both are DDR SDRAM systems. Amidi ¶¶ 4, 42, 47–48, 55–57; JEDEC 21-C, title.

Patent Owner also specifically argues other features found in independent claim 23 — namely “the second set of output signals being generated using the saved density transition value.” App. Br. 49–51; Reb. Br. 19–21. Claims 24–32 depend directly or indirectly from claim 23. We select claim 23 as representative.

For those arguments that repeat those already presented, we refer to our above discussion for details.

Regarding claim 23, the Examiner refers to Ground 7 (RAN 24), which when last rejected relied on Amidi (September 26, 2013 Non-Final Act. 27). Here, the Examiner relies on the CS signal saved in a load mode register 804 in Figure 8. September 26, 2013 Non-Final Act. 27 (citing Amidi, Fig. 8). Patent Owner argues Amidi fails to teach using the CS signal to meet the recited “using a saved density transition value.” App. Br. 50. Additionally, Patent Owner contends that the rejection does not explain how this CS value saved relates to the recited “first column access procedure subsequent to the row access procedure.” *Id.* (emphasis omitted).

Notably, Patent Owner does not dispute the Examiner’s finding that Amidi teaches saving a CS value in the load mode register. *Id.* We thus presume that Amidi teaches storing input signals, including a chip select signal (e.g., CS), in a load register (e.g., 804), which is separate from any register in the recited memory device. As for Patent Owner’s assertion that Amidi fails to use such a saved value as recited in claim 23 (*id.*), we are not persuaded for reasons already discussed. That is, we determined that Amidi and JEDEC collectively teach or suggest saving storing various signals, including a chip select signal, during a row access procedure for later use during a column access procedure to read or write to the correct cell as well as to generate the correct chip select signals. We refer to our above discussion for details.

Patent Owner further refers to the RAN and addresses Requester’s November 27, 2013 Comments. App. Br. 50–51 (citing RAN 30 and Requester’s

November 27, 2013 Comments 14–15). We refer to our previous discussion about this argument and are not persuaded.

Patent Owner further points to Requester’s comments related to JEDEC standard being used to provide timing and duration of elements. Reb. Br. 21 (discussing Resp. Br. 25). Even if Patent Owner is correct that signals are stored within memory device *registers* for only one cycle (Reb. Br. 21), this contention does not rebut what the collective teachings suggest and predictably yield — a circuit configured to save certain values, including density transition values, during a row access procedure and generate a second set of output signals using the save transition value during a column access procedure subsequent to the row access procedure, as recited in claim 23.

Based on the record, the Examiner has not erred in rejecting claims 2–5, 7, 8, 10–12, 14–18, 23–27, and 29–35 based on Amidi in combination with JEDEC. To extent this rejection deviates from the position presented by the Examiner, we designate this rejection a new ground.

B. Obviousness Rejection Based on Amidi, JEDEC, and Vogt – Ground 9

Claim 9 is rejected based on Dell, JEDEC, and Vogt. RAN 6, 15–16. Claim 9 is not separately argued. *See* App. Br. 22–44. For the above reasons, we sustain the rejection of claim 9 and refer to the above discussion of Ground 8.

III. Obviousness Rejection Based on Amidi and Dell 184 – Ground 10

A. The Bank Address Limitation (Claim 6)

Patent Owner presents the same arguments for this rejection as discussed above when addressing Ground 8. App. Br. 21–22 (discussing Ground 10); App. Br. 10–22. As discussed above, Amidi in combination with what one skilled in the art would have recognized from Amidi’s teachings when employing creative steps

and inferences teach and suggest the bank address limitation. We refer above for details.

Yet, the Examiner does not adopt the Requester's proposed rejection for claim 6. *See* RAN 26; *see also* App. Br. 14. Thus, to the extent this rejection deviates from the position presented by the Examiner, we designate the rejection of this claim a new ground.

B. *The Storing Limitations* (Claims 2, 3, 5, 7, 8, 10–12 14–18, 23–27, 29–35)

Patent Owner also argues this rejection as a group. App. Br. 44–51. We select claim 12 as representative. 37 C.F.R. § 41.67(c)(1)(vii).

Some arguments are the same as those discussed above concerning Amidi. We are not persuaded and refer to our previous discussion when addressing Amidi under Ground 8. Even more, we note that this rejection is based on the teachings of both Amidi *and* Dell 184, and thus, individual attacks on Amidi or Dell 184 are not persuasive.

To teach the storing limitation, the Examiner states the claims are rejected based on Amidi and Dell 184 and that the proposed rejection of claims 23–27 and 29–35 is adopted. RAN 7, 26. The proposed rejection of claim 23 adopted discusses Amidi and Dell 184. April 20, 2012 Requester's Comments 112–113 (referring to claims 1 and 12), 80–106 (discussing claims 1 and 12). Specifically, the rejection discusses how both Amidi and Dell 184 disclose a memory module that uses memory devices with different attributes than the computer system expects and how both use an extra, input address bit to address the actual memory devices properly. April 20, 2012 Requester's Comments 82–83, 94–95, 102–106 (citing Amidi ¶¶ 5–11, 45–50, Fig. 6A; Dell 184, 2:48–59). That is, Amidi and

Dell 184, collectively, teach that ranks and banks both may be expanded; therefore, a skilled artisan would recognize various combinations of inputs to achieve expansion including bank address inputs as broadly recited. Moreover, this combination teaches using the logic circuit or element (e.g., Amidi's CPLD) to receive input signals for the above-discussed purpose.

Further, the rejection discusses how Dell 184 teaches storing such an extra bit. *Id.* at 83–84 (citing Dell 184, 8:39–48, 2:48–59). The rejection even further provides a reason to combine the references to achieve a DIMM that uses memory devices with various different attributes or configured differently than what the system expects. *Id.* at 85–86 (citing Amidi ¶¶ 41–60, 71; Dell 184, Abstract, 2:48–59, 4:6–9).

Thus, although the Examiner determines the claims are obvious because they are anticipated (RAN 26) and then withdraws the anticipation rejection of these claims under Amidi (RAN 23), the Examiner also adopts the proposed rejection based on Amidi and Dell for at least claim 23, which has similar storing limitations to claim 12. Also, the Examiner's finding that the combination does not teach storing a *bank address* signals (RAN 27 (when addressing claim 28)) does not conflict with the adopted rejection of claim 12, which only recite storing input signals. Paragraph 64 that follows from the paragraph discussing claim 28 in the RAN addresses claim 28 and not the claims in general. *See* RAN 27.

Additionally, even though the Examiner determined that “Amidi does not expressly disclose the duration, for which the address bits are stored in the Register 608” (RAN 23–24), this statement does not indicate further that Amidi fails to suggest such a feature under an obviousness analysis. We therefore disagree that

the rejection of Ground 10 has been withdrawn or fails to establish a *prima facie* case. *See* App. Br. 44–45.

Regarding the rejection, Patent Owner argues that the bank address (e.g., BA1) has been mischaracterized in Dell 184 as a density transition bit. App. Br. 45 (citing March 16, 2012 Requester’s Comments 102).¹⁸ Notably, the language of “a density transition value” is found in claim 23 but not claim 12. As such, this argument does not apply to claim 12. The discussion in the Comments states that “the density transition bit is an extra row address (which will be decoded/remapped into a bank address signal).” April 20, 2012 Requester’s Comments 105. As such, we disagree that Requester describes or mischaracterizes the transition bit as the bank address signal to satisfy the limitations of the claims. *Id.*

Moreover, we fail to see a distinction between using a value to remap signals and using the value to transition to another value, as Patent Owner asserts. *See* App. Br. 45. We refer to our discussion of Dell in Ground 2 for details. *See also* Dell 184, 9:37–41, 63–66 (discussing how the highest order address signal transitions to another value). As previously noted, the claims (e.g., claims 12 and 23) only require storing an input signal or a density transition value without specifying the value needs to be a bank address signal value.

As to whether this value is a *density* transition value, we further note that the rejection is based on both Amidi and Dell 184. Amidi discusses transitioning from an expected system having memory devices with one density to a system that has memory devices with a second density. Amidi ¶¶ 43–49. Amidi further suggests other families of devices, including those with other densities, can be used with

¹⁸ The March 16, 2012 Requester’s Comments were found defective and replaced by amended comments on April 20, 2012.

Amidi. Amidi ¶ 71. Dell 184 teaches one such known memory device which has different bank numbers than the system expects. Dell 184, Abstract, 2:48–59. Dell 184 achieves the transition between the expected and actual bank number using the remapping function. Thus, when combining these teachings, these references teach a density transition value as recited and provide a reason with some rational underpinning to be combined. *See* April 20, 2012 Requester’s Comments 85–86. As such, whether Dr. Bagherzadeh provides sufficient reason to combine (see App. Br. 46), the adopted rejection does.

As for Ground 10, Patent Owner also asserts its disagreement with the Examiner’s reliance on the CS signal and its value saved in a register of Amidi to teach the limitations of claim 23. App. Br. 49–50 (referring to September 26, 2013 Requester’s Comments 27). We are not persuaded as discussed above when addressing Ground 8 and Amidi.

Accordingly, for previously stated reasons, we sustain the adopted rejection of claims 2, 3, 5, 7, 8, 10–12, 14–18, 23–27, and 29–35 based on Amidi and Dell 184 under § 103.

Remaining Rejections

The above discussions address all the claims on appeal and are dispositive, rendering it unnecessary to reach the propriety of any remaining, adopted rejections. *See Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984); *In re Gleave*, 560 F.3d 1331, 1338 (Fed. Cir. 2009); and 37 C.F.R. § 41.77 (a) (“The Patent Trial and Appeal Board ... may affirm or reverse each decision of the examiner on all issues raised on each appealed claim.”)

IV. CONCLUSIONS

We affirm the Examiner's decision to reject claims 2–12, 14–18, and 23–35.

We affirm the rejections of: (1) claims 2, 3, 5, 7, 8, 10–12, 14–18, and 23–32 based on Dell and JEDEC (Ground 2), (2) claim 9 based on Dell, JEDEC, and Vogt (Ground 3), and (3) claims 2, 3, 5, 7, 8, 10–12, 14–18, 23–27, and 29–35 based on Amidi and Dell 184 (Ground 10).

We designate the rejections for: (1) claims 2–8, 10–12, 14–18, 23–27, and 29–35 based on Amidi and JEDEC (Ground 8), (2) claim 9 based on Amidi, JEDEC, and Vogt (Ground 9), and (3) claim 6 based on Amidi and Dell '184 as new grounds.

We do not reach the propriety of the remaining rejections.

V. TIME PERIOD FOR RESPONSE

Pursuant to 37 C.F.R. § 41.77(a), the above-noted reversal constitutes a new ground of rejection. Section 41.77(b) provides that “[a] new ground of rejection . . . shall not be considered final for judicial review.” That section also provides that Patent Owner, WITHIN ONE MONTH FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new grounds of rejection to avoid termination of the appeal proceeding as to the rejected claims:

(1) *Reopen prosecution.* The owner may file a response requesting reopening of prosecution before the examiner. Such a response must be either an amendment of the claims so rejected or new evidence relating to the claims so rejected, or both.

(2) *Request rehearing.* The owner may request that the proceeding be reheard under § 41.79 by the Board upon the same record. The request for rehearing must address any new ground of rejection and state with particularity the

points believed to have been misapprehended or overlooked in entering the new ground of rejection and also state all other grounds upon which rehearing is sought.

In accordance with 37 C.F.R. § 41.79(a)(1), the “[p]arties to the appeal may file a request for rehearing of the decision within one month of the date of: . . . [t]he original decision of the Board under § 41.77(a).” A request for rehearing must be in compliance with 37 C.F.R. § 41.79(b). Comments in opposition to the request and additional requests for rehearing must be in accordance with 37 C.F.R. § 41.79(c)-(d), respectively. Under 37 C.F.R. § 41.79(e), the times for requesting rehearing under paragraph (a) of this section, for requesting further rehearing under paragraph (c) of this section, and for submitting comments under paragraph (b) of this section may not be extended.

An appeal to the United States Court of Appeals for the Federal Circuit under 35 U.S.C. §§ 141-144 and 315 and 37 C.F.R. § 1.983 for an *inter partes* reexamination proceeding “commenced” on or after November 2, 2002 may not be taken “until all parties’ rights to request rehearing have been exhausted, at which time the decision of the Board is final and appealable by any party to the appeal to the Board.” 37 C.F.R. § 41.81. *See also* MPEP § 2682 (8th ed., Rev. 8, July 2010).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

Requests for extensions of time in this *inter partes* reexamination proceeding are governed by 37 C.F.R. § 1.956. *See* 37 C.F.R. § 41.79.

In the event neither party files a request for rehearing within the time provided in 37 C.F.R. § 41.79, and this decision becomes final and appealable under 37 C.F.R. § 41.81, a party seeking judicial review must timely serve notice

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Patent 7,864,627

on the Director of the United States Patent and Trademark Office. *See* 37 C.F.R.
§§ 90.1 and 1.983.

AFFIRMED
37 C.F.R. § 41.77(b)

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EXAMINER

PEIKARI, BEHZAD

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SMART MODULAR TECHNOLOGIES, INC.,
Requester

v.

NETLIST, INC.,
Patent Owner

Appeal 2018-003280
Reexamination Control No. 95/001,758
United States Patent No. 7,864,627 B2
Technology Center 3900

Before JEFFREY B. ROBERTSON, DENISE M. POTHIER, and
JEREMY J. CURCURI, *Administrative Patent Judges*.

POTHIER, *Administrative Patent Judge*.

DECISION UNDER 37 C.F.R. § 41.77(f)

I. STATEMENT OF THE CASE

In an earlier Decision (“Dec.”) mailed May 31, 2016, we affirmed the rejections of (1) claims 2, 3, 5, 7, 8, 10–12, 14–18, and 23–32 based on Dell¹ and JEDEC² (Ground 2³), (2) claim 9 based on Dell, JEDEC, and Vogt⁴ (Ground 3), and (3) claims 2, 3, 5, 7, 8, 10–12, 14–18, 23–27, and 29–35 based on Amidi⁵ and Dell ’184⁶ (Ground 10). Dec. 46. We designated the rejections for: (1) claims 2–8, 10–12, 14–18, 23–27, and 29–35 based on Amidi and JEDEC (Ground 8), (2) claim 9 based on Amidi, JEDEC, and Vogt (Ground 9), and (3) claim 6 based on Amidi and Dell ’184 as new grounds. *Id.* On August 1, 2016, Patent Owner elected to reopen prosecution before the Examiner pursuant to 37 C.F.R. § 41.77(b)(1) (“PO Response”), submitting claim amendments and a Third

¹ U.S. Patent No. 5,926,827 (issued July 20, 1999) (Dell).

² JEDEC Standard No. 21-C, *PC2100 and PC1600 DDR SDRAM Registered DIMM, Design Specification, Rev. 1.3* pages 4.20.4-1–4.20.4-82 (Jan. 2002) (JEDEC 21-C); *JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification JESD79C* (Rev. of JESD79B) 1-75 (Mar. 2003) (JEDEC 79C); *JEDEC STANDARD, Definition of the SSTV16859 2.5 V 13-Bit to 26-Bit SSTL_2 Registered Buffer for Stacked DDR DIMM Applications, JESD82-4B* (Rev. of JESD82-4A) 1-12 (May 2003) (JEDEC 82-4B). As indicated in the previous Decision, JEDEC 21-C, JEDEC 79C, and JEDEC 82-4B are often referred to collectively as JEDEC or JEDEC standards in the presented rejections, the briefs, and declarations. *See, e.g.*, Sechen Decl. ¶ 8.

³ Throughout the documents in this proceeding, the Examiner, Patent Owner and Requester refer to the various rejections by ground number. *See, e.g.*, Right of Appeal Notice (RAN) 6. We include the ground number here and in the Opinion.

⁴ Pete Vogt, *Fully Buffered DIMM Server Memory Architecture: Capacity, Performance, Reliability, and Longevity* (2004) (Vogt).

⁵ U.S. Publ. 2006/0117152 A1 (published June 1, 2006 and filed Jan. 5, 2004) (Amidi).

⁶ U.S. Patent 6,446,184 B2 (issued Sept. 3, 2002) (Dell 184).

Supplemental Declaration of Carl Sechen, Ph.D., dated July 31, 2016 (“3d Supp. Sechen Decl.”). Requester filed comments under 37 C.F.R. § 41.77(c) dated August 31, 2016 (“3PR Comments”) along with a Declaration of Nader Bagherzadeh, Ph.D., dated August 31, 2016 (“5th Bagherzadeh Decl.”). On February 9, 2017, Patent Owner’s request to reopen prosecution was granted, and the proceeding was remanded to the Examiner for consideration of the new grounds of rejection of certain claims. Order 5.

Prior to granting the remand, claims 1, 13, and 19–22 were canceled (PO Response 9), and claims 2–12, 14–18, and 23–35 of the ’627 patent were pending. In Patent Owner’s Response, claims 6, 12, and 15 were amended, and claims 4 and 23–35 were canceled. *See* PO Response 2–8; Ex. Deter. 4. As such, claims 2, 3, 5–12, and 14–18 are pending in this proceeding. *See* PO Response 9; *see also* Ex. Deter. 6.

On remand, the Examiner maintained the rejections of claims 2, 3, 5–12, and 14–18 pertaining to the new grounds in the “Determination Under 37 C.F.R. §41.77(d)” (Ex. Deter.) mailed October 2, 2017. Ex. Deter. 7. Patent Owner did not submit comments as set forth in 37 C.F.R. § 41.77(e), and Requester did not submit a reply.

This proceeding has been returned to the Board under 37 C.F.R. § 41.77(f). Our new Decision is deemed to incorporate our earlier Decision, except for any portion specifically withdrawn. 37 C.F.R. § 41.77(f).

Claims 6, 12, and 15 are now independent claims; the remaining claims depend directly or indirectly from either claim 12 or claim 15. Illustrative, independent claim 6 reads as follows:

6. (Amended) A circuit configured to be mounted on a memory module so as to be electrically coupled to a first number of double-

data-rate (DDR) memory devices arranged in a first number of ranks on the memory module, the memory module configured to be electrically coupled to a memory controller of a computer system so as to receive a set of input signals from the computer system, the set of input signals comprising row/column address signals, bank address signals, and chip-select signals, the set of input signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit comprising:

a logic element configurable to receive the bank address signals, at least one chip select signal of the chip-select signals, and at least one row address signal of the row/column address signals from among the set of input signals;

a register; and

a phase-lock loop circuit configurable to be operatively coupled to the first number of DDR memory devices, the logic element, and the register, wherein, in response to signals received from the computer system, the phase-lock loop (PLL) circuit transmits a PLL clock signal to the first number of DDR memory devices, the logic element, and the register,

wherein the circuit is configurable to generate a set of output signals in response to the set of input signals, the set of output signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit is configurable to further respond to the set of input signals from the computer system by generating and transmitting the set of output signals to the first number of DDR memory devices,

wherein the register (i) receives, from among the set of input signals, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the first number of DDR memory devices, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element, wherein the bank address signals of the set of input signals are received by both the logic element and the register,

wherein the logic element generates rank-selecting signals of the output signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and [sic] (iii) the at least one chip-select signal received by the logic element and (iv) the PLL clock signal,

wherein the circuit further responds to an input command signal from the computer system by generating an output command signal comprising a read command signal or a write command signal, wherein the at least one row address signal is a density transition bit, and the logic element stores the density transition bit during an activate command for a selected bank, wherein the density transition bit is stored for subsequent use for the output command signal.

PO Response 2–4 (underlining amendments relative to the originally issued claims and italicizing newly added subject matter relative to the claims as originally appealed).

The following summarizes the declarations in this proceeding:

Declaration of Dr. Carl Sechen, dated February 15, 2012 (Sechen Decl.),

Declaration of Dr. Carl Sechen, dated March 19, 2013 (2d Sechen Decl.),

Declaration of Dr. Carl Sechen, dated November 26, 2013 (3d Sechen Decl.),

Third Supplemental Declaration of Dr. Carl Sechen, dated July 31, 2016 (3d Supp. Sechen Decl.),⁷

Declaration of Dr. Nader Bagherzadeh, dated September 6, 2011 (Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh, dated March 15 2012 (2d Bagherzadeh Decl.),

⁷ This is the fourth declaration of Dr. Sechen. Although the nomenclature of this declaration (“3d Supp. Sechen Decl.”) departs from the previous Sechen declarations, we abbreviate this declaration as indicated for consistency with Patent Owner’s Response.

Declaration of Dr. Nader Bagherzadeh, dated April 18, 2013 (3d Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh, dated December 26, 2013 (4th Bagherzadeh Decl.), and

Declaration of Dr. Nader Bagherzadeh, dated August 31, 2016 (5th Bagherzadeh Decl.).

Maintained Rejections

In the Examiner's Determination, the Examiner maintains the following new grounds of rejection:

References	Basis	Claims	Presented/Maintained
Amidi and JEDEC (Ground 8)	§ 103(a)	2, 3, 5–8, 10–12, and 14–18	Dec. 21–41; Ex. Deter. 7
Amidi, JEDEC, and Vogt (Ground 9)	§ 103(a)	9	Dec. 41; Ex. Deter. 7
Amidi and Dell '184 (Ground 10)	§ 103(a)	6	Dec. 41–42; Ex. Deter. 7

II. ISSUES

The main issues are whether Patent Owner has presented sufficient arguments and evidence to overcome the new grounds of rejection for claims 2, 3, 5–12, and 14–18 presented in the May 31, 2016 Decision.

III. ANALYSIS

A. Amidi and JEDEC (Ground 8)

In our May 31, 2016 Decision, claims 2, 3, 5–8, 10–12, and 14–18 were newly rejected under 35 U.S.C. § 103 based on Amidi and JEDEC. Dec. 21–41.

Patent Owner presents several arguments related to this new ground, asserting the amendments to independent claims 6, 12, and 15 overcome the new ground. PO Response 10, 14–20. Among the contentions, Patent Owner asserts the claimed “‘logic element’ now requires the use of at least four different signals: ‘(i) the at least one row address signal, (ii) the bank address signals, and [sic] (iii) the at least one chip-select signal received by the logic element and (iv) the PLL [phase lock loop] clock signal.’” *Id.* at 16. Patent Owner contends (1) an ordinarily skilled artisan “would readily understand that these more signals are beyond ‘the design requirements of Amidi’” (*id.* (citing 3d Supp. Sechen Decl. ¶ 30)) and (2) the claimed “‘logic element’ and ‘circuit’ now require significant design elements that go far beyond Amidi’s design: *e.g.*, the ‘logic element’ generating ‘rank-selecting signals in response at least in part to’” the above signals (i)-(iv) (*id.* at 17). *See also id.* at 18 (citing 3d Supp. Sechen Decl. ¶ 34).

Requester responds that one skilled in the art would have understood Amidi discloses the claimed “logic element” in independent claims 6, 12, and 15. 3PR Comments 4–5 (citing 5th Bagherzadeh Decl. ¶¶ 8–9). Requester points to Amidi’s CPLD (complex programmable logic device) in Figure 6A generating rank-select signals (*e.g.*, rcs0-3) based on a row address signal (*e.g.*, Add(n)) and a chip-select signal (cs0). *Id.* at 5 (citing Amidi ¶¶ 50, 52, Fig. 6A). Next, Requester states Amidi teaches its logic element generates rank-select signals in response to a PLL-clock signal. *Id.* Referring to the discussion of “the PLL Clock Amendment” (*id.* at 2–3), Requester explains an ordinarily skilled artisan would have found it obvious to provide the CPLD an output clock signal from its PLL (*e.g.*, 606) instead of an input clock signal from a memory controller. *Id.* at 5. Finally, Requester asserts one skilled in the art “would understand that the bank address

signal could be routed to the CPLD to meet design specifications or to meet system timing, signal integrity, and thermal requirements because the location and number of the logic elements impacts [sic] all of those features” and is a design choice. *Id.* at 5–6 (citing 5th Bagherzadeh Decl. ¶ 9); *see also id.* at 9–11 (citing 5th Bagherzadeh ¶¶ 14–16).

The Examiner maintains the rejection of claims 2, 3, 5–8, 10–12, and 14–18 based on Amidi and JEDEC. Ex. Deter. 7–15. The Examiner states Patent Owner has not adequately addressed the obviousness analysis concerning Amidi’s CPLD functionality (*id.* at 13) and the features in the claim amendments were already addressed in our earlier Decision (*id.* at 13–14 (discussing previously pending claims 23 and 26)). Specifically, The Examiner concludes “[f]or the reasons set forth above in reference to [R]equester’s arguments, and because every feature of these amendments was already considered and designated as obvious in view of Amidi and/or Amidi in view of other cited references by the Board in the Opinion of May 31, 2016, the rejections should be maintained.” *Id.* at 15.

Upon review of this record, the rejection of claims 2, 3, 5–8, 10–12, and 14–18 based on Amidi and JEDEC in our earlier decision is withdrawn. Among other amendments, independent claim 6 newly recites “the logic element generates rank-selecting signals of the output signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and [sic] (iii) the at least one chip-select signal received by the logic element and (iv) the PLL clock signal.”⁸ PO Response 3. Requester contends the broadest reasonable construction of the above limitation should be the logic element generating rank-selecting

⁸ Throughout this Decision, these signals will be referred to collectively as signals (i)-(iv) or individually as signal (i), (ii), (iii), or (iv).

signals in response to *at least one of* the four enumerated signals (i) through (iv) or “one or more of a combination of the four signals depending on the design specifications and the system purpose.” 3PR Comments 10 (citing 5th Bagherzadeh Decl. ¶ 15).

We disagree. Claim 6 recites the logic element generates the rank-selecting signals “in response at least part to” signal (i), signal (ii), signal (iii), *and* signal (iv). PO Response 3. The broadest, reasonable construction of claim 6 requires the logic element to generate rank-select or chip-select⁹ signals in response to *at least signals* (i), (ii), (iii), *and* (iv) because of the express language contained in the claim. That is, the recited phrase “at least” requires the logic element to generate the “rank-selecting signals” or chip-select signals in response to claim 6’s signals (i) *through* (iv), but other, additionally unrecited signals can also be involved in generating the rank-selecting signals. PO Response 3.

Turning to Amidi, Requester notes Amidi teaches signal (i) or a row-address signal (e.g., Add(n) or Add(n-1)) and signal (iii) or a chip-select signal (e.g., cs0, cs1) are received by the logic element (e.g., CPLD 604) and rank-selecting signals (e.g., rcs0a-rcs3b) are generated in response. 3PR Comments 5; *see also* Amidi ¶¶ 52, 60, Figs. 6A-6B. We agree. We further agree with Requester that an ordinarily skilled artisan would have found it obvious to provide the CPLD in Amidi’s Figures 6A and 6B with an output clock signal from its PLL (e.g., 606) instead of an input clock signal from a memory controller as shown. *Id.* at 5. In particular, although Amidi discloses its CPLD (e.g., 604) receives clock signals (e.g., CLK0, CLK0_N) from the memory controller (e.g., 602), the same clock

⁹ The ’627 patent explains “rank-select signals” are “also called chip-select signals.” The ’627 patent 2:39–40.

signals are also outputted from PLL 606. *See* Amidi, Figs. 6A–B; *see also* Ex. Deter. 9 (stating “those same signals [(i.e., clock signals CLK0 and CLK0_N)] are provided to the CPLD 604”); 5th Bagherzadeh Decl. ¶ 5 (stating “the PLL input clock is logically identical to the PLL output clock”). Patent Owner has not rebutted this finding, and this finding is rational and supported by evidence drawn from the record. Given the record demonstrates PLL’s input clock signals are the same as the output clock signals, we conclude that directing the clock signals from a PLL (e.g., a “PLL” clock signal from PLL 608 in Amidi’s Figure 6A) instead of from the module connector (e.g., 602 in Amidi’s Figure 6A) would have been within ordinarily skilled artisans’ knowledge when accounting for the inferences and creative steps that these artisans would have employed. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007).

We further agree with Examiner that one of ordinary skill in the art would have recognized rank-selecting signals would be generated in response to such a PLL clock signal directed to Amidi’s CPLD “depending on the needs and specific requirements of the [Amidi] circuit.” Ex. Deter. 9. For example, as Requester explains, one skilled in the art would have recognized that using the buffered, clock signal from Amidi’s PLL 606 (e.g., a “PLL clock signal”) rather than from module connector 602 can improve upon performance, such as signal synchronization. 3PR Comments 2 (citing 5th Bagherzadeh Decl. ¶ 5). Patent Owner provides no rebuttal to Requester’s explanation, which has a reason with some rational basis supported by evidence drawn from the record for using the PLL clock signal to generate rank-selecting signals. At best, Patent Owner contests Amidi as lacking a “PLL clock signal” (PO Response 16; *see also* 3d Supp. Sechen Decl. ¶ 28) without considering what Amidi suggests to one skilled

in the art related to “PLL” clock signals being directed to Amidi’s CPLD under an obviousness analysis. *See* Ex. Deter. 8 (stating “patent owner’s arguments are framed as if addressing an anticipation rejection, rather than a question of obviousness.”).

As for recited signal (ii) or “the bank address signals,” we determined in our earlier Decision “one skilled in the art would have recognized directing other signals, including bank address signals, to Amidi’s two registers or its CPLD.” Dec. 29. At the outset, we note in our earlier Decision both a register (e.g., 408) and a CPLD (e.g., 410) in Amidi were mapped to the claimed “logic element” of the previously recited claim 6. *See* Dec. 23 (stating “the Examiner has mapped the recited ‘logic element’ to both Amidi’s CPLD 410 and Register 408”). We further explained that (1) Amidi shows a register (e.g., 408 or 608) receiving bank address signals (e.g., BA[1:0]) (*id.* at 24 (citing Amidi, Figs. 4A–B, 6A)) as well as (2) Amidi and JEDEC at least suggest both registers receiving bank address signals (*id.* at 27–31). Thus, the earlier Decision determined Amidi and JEDEC teach or suggest bank address signals directed to both registers or to both the previously recited “register” and a component of the previously recited “logic element.” *Id.*

However, as currently claimed, claim 6 newly recites the logic element “generates rank-selecting signals” in response to signals (i)–(iv). In Amidi, its CPLD (e.g., 604 in Figures 6A–B) generates rank-selecting signals (e.g., rcs0a–3b). Amidi, Figs. 6A–B. Because Amidi’s registers (e.g., 408, 418, and 608) do not teach or suggest “generat[ing] rank-selecting signals” (e.g., rcs0a–rcs3b) and the signals Amidi’s registers received do not attribute to the generated rank-selecting signals, Amidi’s register (e.g., 408) cannot reasonably be mapped to the component of claim 6’s “logic element” that generates the recited “rank-selecting

signals” in response to signals (i)–(iv). As such, regardless of whether or not Amidi’s registers and their functions can be duplicated so that both receive bank address signals (*see* PO Response 17; *see also* 3PR Comments 11), this discussion does not address whether Amidi teaches or suggests the new, specific “logic element” recitation that generates rank-selecting signals in response to signals (i)–(iv) found in independent claims 6, 12, and 15.

Focusing on Amidi’s CPLD and whether one skilled in the art would have recognized Amidi’s CPLD (1) is “configurable to receive the bank address signals” and (2) “generates rank-selecting signals” in response to signal (ii) or the recited “bank address signals” as well signals (i), (iii), and (iv) as now recited in claims 6, 12, and 15, we stated previously that “one skilled in the art would have recognized directing other signals, including bank address signals, to Amidi’s two registers or its *CPLD* can further assist in emulating a two rank memory module in a four rank memory module in a cost effective and flexible manner. *See* Amidi ¶¶ 11, 23, 41, 49, 57, 59, 62, Fig. 7.” Dec. 29 (emphasis added). Notably, these statements were made in the context of addressing a previous limitation in claim 6, which only included “a logic element configurable to receive the set of input signals” (claim 1, from which claim 6 depended)¹⁰ and “the bank address signals of the set of input signals are received by . . . the logic element” (claim 6). App. Br. 53 (Claims App’x).¹¹

Previous claim 6 also had no recitation that the logic element generates rank-selecting signals. *See id.* Rather, previous claim 6 recited the entire “circuit”—not the specific “logic element”—is “configurable to further respond to

¹⁰ The ’627 patent 32:56–57.

¹¹ Patent Owner submitted its Appeal Brief on October 15, 2014.

the set of input signals from the computer system by generating . . . output signals” (claim 1, from which claim 6 depended).¹² Previous claim 6 had no specific recitation that the logic element generates rank-selecting signals as presently recited. Thus, our previous discussion concerning directing signals, including bank address signals, to Amidi’s CPLD for various reasons did not specifically address whether one skilled in the art would have recognized directing bank address signals to a logic element to generate rank-selecting signals in response to the input signals, including the bank address signals, now recited in claims 6, 12, and 15. *See* Dec. 29–31.

Amidi does not discuss or show using bank address signals to generate rcs0a through rcs3b. *See* Amidi ¶¶ 41, 49, 57, 62, Figs. 6A–B. Patent Owner also states, and we agree, “Amidi’s design plainly uses just one address signal Add(n) and not the combination of the address signal Add(n) with any of the bank address signals BA[1:0].”). PO Response 16 (discussing Amidi’s Figure 6A). However, we previously reasoned

one skilled in the art would have recognized that memory modules that explicitly differ from JEDEC design specifications, such as Amidi’s (e.g., emulating a two rank memory module on a four-rank memory module), may affect the memory module in other ways and require further unspoken differences, including other signals being received by . . . CPLD in Amidi. For instance, one skilled in the art would have recognized directing other signals, including bank address signals, to Amidi’s . . . CPLD[.]

Dec. 29.

One reason provided in the previous Decision for directing bank address signals to Amidi’s CPLD included “assist[ing] in emulating a two rank memory

¹² The ’627 patent 32:66–33:2.

module in a four rank memory module in a cost effective and flexible manner.” *Id.* Although this reason addresses why bank address signals may be received by a CPLD, this reasoning does not sufficiently address why one skilled in the art would have specifically recognized using Amidi’s CPLD (e.g., a logic element as recited in claim 6) “generates rank-selecting signals” in response to any received bank address signal in addition to a row address signal (e.g., Add(n) in Figure 6A) already used by Amidi. One skilled in the art may have recognized sending bank address signals to Amidi’s CPLD provides flexibility to a memory module designer in assisting with emulating a two-rank memory module in a four-rank memory module. *See* Dec. 29–30 (citing Amidi ¶¶ 11, 23, 41, 49, 57, 59, 62, Fig. 7 and JEDEC 21-C, 4.20.4-5). However, having a logic circuit specifically generate “rank-selecting signals . . . in response to” bank address signals in combination with signals (i), (iii), and (iv), as claim 6 presently recites, does not necessarily follow from this general suggestion in the art. *See* 3d Supp. Sechen Decl. ¶ 30 (“A POSITA¹³ would readily understand that these more signals are beyond ‘the design requirements of Amidi.’”).

We further discussed in our previous Decision that an artisan would have recognized directing bank address signals to Amidi’s CPLD “to account for the design requirements of Amidi and preferences of the artisan.” Dec. 31 (citing Amidi ¶ 71, JEDEC 21-C, 4.20.4-5, and 2d Bagherzadeh Decl. ¶ 14)); *see also* PO Response 16; *see also* 3PR Comments 10. For example, both Amidi and JEDEC discuss modifying memory modules, suggesting directing signals, including bank address signals, to different components in memory modules. *See* Amidi ¶ 71; *see also* JEDEC 21-C, 4.20.4-5. Yet, these general teachings or suggestions are not

¹³ POSITA stands for a person of ordinary skill in the art.

adequate to demonstrate one skilled in the art would have known of the specifically recited “logic element generates rank-selecting signals” in response to both a row address signal and bank address signals, as well as signals (iii) and (iv) presently recited in claim 6. *See* PO Response 16.

In our previous Decision, we discussed directing bank address signals to Amidi’s CPLD for reasons, including, to meet timing, signal integrity, and thermal requirements. Dec. 30 (referring to JEDEC 21-C, 4.20.4-5). Requester further adds receiving bank address signals at Amidi’s logic element or CPLD is a design choice “to meet design specification” for an ordinarily skilled artisan that “effect[s] various characteristics including signal integrity, drive capability, and latency.” 3PR Comment 5 (citing 5th Bagherzadeh Decl. ¶ 8). However, similar to above, these reasons (e.g., to effect signal integrity, drive capability, and latency) for directing bank address signals to Amidi’s CPLD do not demonstrate sufficiently why one skilled in the art would have recognized to direct bank address signals to the specifically recited “logic element” in order to generate “rank-selecting signals” in response to both a row address signal and bank address signals, as well as signals (iii) and (iv) now recited in claim 6. For instance, the bank address signals may be directed to Amidi’s CPLD for other reasons, such as to ensure proper timing within the entire circuit or to reduce register latency (*see* Dec. 30), without using these signals to generate rank-selecting signals. Additionally, Dr. Sechen testifies a PLL clock signal—not the bank address signals—is more relevant to system timing. *See* 3d Supp. Sechen Decl. ¶ 29.

Requester additionally provides Dr. Bagherzadeh’s testimony, which contends configuring a logic element to receive row address and bank address signals as recited is a “design choice” to an ordinary artisan. *See* 5th Bagherzadeh

Decl. ¶ 8, *cited in* Requester Comments 5. Requester and Dr. Bagherzadeh rely on an ordinarily skilled artisan's understanding after taking a "VLSI Design," an "Organization of Digital Computers," or an "Introduction to Digital Logic Laboratory" course to conclude that modifying Amidi's CPLD and arriving at the claimed "logic element" in claim 6 would have been obvious to an ordinary artisan in order to achieve a desired signal integrity, drive capability, and latency characteristics. *See* 5th Bagherzadeh Decl. ¶ 8. These classes, and what an ordinary artisan "would understand from her studies" (*id.*), may suggest generally to an ordinary circuit designer designing a circuit to opt for one component to receive signals over another component and that this selection effects circuit characteristics, including signal integrity, drive capability, and latency. *See, e.g., id.* Yet, this general understanding fails to provide a reason with a rational underpinning why one skilled in the art would design a circuit's logic element, like Amidi's CPLD, to generate the recited "rank-selecting signals" in response to signals (i) through (iv), including both a row address signal and bank address signals, as claim 6 now specifically claims. *See id., cited in* 3PR Comments 5.

Concerning latency and its impact on Amidi's CPLD design, Requester provides a little more explanation why one skilled in the art would have recognized directing bank address signals to Amidi's CPLD to generate "rank-selecting signals" as now recited in claim 6. 3PR Comments 5–6. Requester states "routing a bank address line through the CPLD would mean that a register might have less logic to perform and the latency would be reduced while the additional routing or fewer registers would also impact the system integrity and thermal characteristics." *Id.* at 6 (citing 5th Bagherzadeh Decl. ¶ 9); *see also id.* at 10 (citing 5th Bagherzadeh Decl. ¶ 16). We acknowledge Requester may be correct that one

skilled in the art who has taken a VLSI Design or Digital Logic course would have recognized latency increases or decreases based on where signals are routed within a circuit. Yet, having this general understanding does not provide ample support to demonstrate a reason with a rational underpinning why one skilled in the art would design the logic element, like Amidi's CPLD, to generate rank-selecting signals in response to signals (i) through (iv), including both a row address signal and bank address signals, as now specifically recited in claim 6.

Patent Owner indicates our previous Decision may have contemplated one skilled in the art would recognize directing bank address signals to the CPLD as an *alternative* to a row address signal for generating rank-selecting signals in order to provide flexibility to the designer. *See* PO Response 15–16 (referring to our previous Decision and the discussed reasons to direct bank address signals to Amidi's CPLD); *see also* 3d Supp. Sechen Decl. ¶ 28. For example, Dr. Bagherzadeh indicates DDR2 devices were known and that “one of ordinary skill would have understood that the BA2 address bit is not needed in 256Mb to 512MB JEDEC compliant DDR2 SDRAMs.” 3d Bagherzadeh Decl. ¶ 10; *see also id.* ¶ 5, 8–9. Although Dr. Bagherzadeh does not additionally suggest using the free-bank address bit (e.g., BA2 address bit) to select a rank or a chip select (*see id.* ¶¶ 5, 8–10), this testimony coupled with Amidi's teachings previously discussed (*see* Amidi ¶¶ 49, 51–52, 71) may suggest to one skilled in the art using a bank address signal *rather* than row address signal for rank-selecting signals depending on the density of the memory devices.

However, these teachings and testimony do not teach or suggest Amidi's CPLD generates rank-selecting signals in response to *both* a row address signal

and bank address signals¹⁴ in addition to signals (iii) and (iv) as now recited in claim 6. 3d Supp. Sechen Decl. ¶ 29 (stating “Amidi’s CPLD is designed to operate without any bank address signals”), ¶¶ 30, 34 (stating “Amidi was not aware of and did not implement any of these [recited] design elements, which would indicate a different principle of operation to a POSITA . . . [and] would involve much more than ‘engineering tradeoffs’ to a POSITA.”)

Nor does JEDEC, alone or in combination with Amidi, provide a requisite teaching to suggest this claimed feature missing from Amidi. Notably, Dr. Bagherzadeh states a “POSITA would understand that Amidi discloses using all four input signals because those inputs are necessary to determine what rank to select per the JEDEC Standard. JEDEC 79C.” 5th Bagherzadeh Decl. ¶ 14, *cited in* 3PR Comments 10. Yet, Dr. Bagherzadeh does not cite any portion of JEDEC 79C supporting this proposition that all four input signals (i) through (iv) in claim 6 are necessary to determine a selected rank. *See id.* JEDEC 79C indicates a bank—not a rank—is opened or selected using an ACTIVE command, and an ACTIVE, READ, or WRITE command that selects a bank (e.g., bank-selecting signal) may involve an address signal (e.g., ADDR column). JEDEC 79C, 12, 21. There is no discussion of using bank address signals in rank selection. *See id.* Moreover, JEDEC does not sufficiently discuss a CPLD, like Amidi’s, and

¹⁴ The ’627 patent discusses using a row address signal (e.g., A_{n+1} or A_{13}) or bank address signal (e.g., BA_2) for generating rank-select signals (e.g., CS_{0A} - CS_{1B}) depending on the density transition (e.g., 256 Mb to 512 Mb memory devices or 512 Mb to 1Gb) of its memory devices (e.g., 32, 34, 36, 38). *See* the ’627 patent 7:45–8:32, 12:18–21, 13:1–11, 14:11–17, Fig. 1A. The ’627 patent further shows both a row address signal (e.g., A_{n+1}) and bank address signals (e.g., BA_0 - BA_m) are sent to its logic device (e.g., 40) to generate rank-selecting signals (e.g., CS_{0A} - $1B$). *See id.*

whether or not such a logic element would receive bank address signals to generate rank-selecting signals. *See generally* JEDEC 79C. Thus, Amidi, alone or in combination with JEDEC, does not contemplate a logic element (e.g., Amidi’s CPLD) receiving both a row address signal and bank address signals in addition to signals (iii) and (iv) as now recited in claim 6. *See* 3d Supp. Sechen Decl. ¶ 35 (stating “even in combination, Amidi in view of JEDEC fails to disclose all recitations of claim 6.”).

Notably, the Examiner contends that the above newly recited limitations in claim 6 were addressed in our previous Decision when discussing prior pending claims 23 and 26. Deter. 13–14. Although many similarities exist, current claim 6 differs from the previously rejected claims 23 and 26. For example, prior pending claim 23 recited “a logic element configurable to receive the set of input signals,” which included one row/column address signal, bank address signals, and a chip select signal, and the circuit—not the logic element— “is configurable to generate a first set of output signals in response to the set of input signals.” App. Br. 55–56 (Claims App’x). Also, previous pending claim 23 did not specifically recite “generat[ing] rank-selecting signals of the output signals” in response to the set of input signals, rather just generating a set of output signals. *Compare* PO Response 3, *with* App. Br. 55–56.

To be sure, previously pending claim 26 was more specific to the circuit being “configurable to further respond to the set of input signals from the computer system by selecting at least one rank of the first number of ranks.” App. Br. 56 (Claims App’x). Yet, this previous recitation did not specifically recite the “logic element” is configured to “generate[] rank-selecting signals” as currently recited in claim 6. Instead, previous claim 26 recited the *entire circuit* is configurable to

respond to the set of input signals by selecting a rank. *Id.* Thus, the previous Decision did not squarely address the newly recited “logic element generates rank-selecting signals of the output signals in response to” signals (i)-(iv) in claim 6.

We reconsider amended claim 6, all the evidence, and the arguments presented. The record does not contain adequate evidence and explanation how Amidi and JEDEC teach or suggest to an ordinarily skilled artisan the “logic element that generates rank-selecting signals in response to” signals (i) through (iv) now recited in claim 6.

Both, newly amended independent claims 12 and 15 similarly recite “the logic element generates rank-selecting signals of the output signals in response at least in part to (1) the at least one row address signal, (ii) the bank address signals, and [sic] (iii) the at least one chip-select signal and (iv) the PLL clock signal.” PO Response 5, 7 (Claims App’x). For reasons similar to those discussed above, we determine the evidence and arguments in the record do not demonstrate a reason with sufficient, rational underpinning in Amidi, JEDEC, and/or based on an ordinarily skilled artisan’s background knowledge why one skilled in the art would design a logic element to generate rank-selecting signals in response to signals (i) through (iv) as now recited in claim 6.

Accordingly, we withdraw the rejection in our earlier decision of independent claims 6, 12, and 15 and dependent claims 2, 3, 5, 7, 8, 10, 11, 14, and 16–18 based on Amidi and JEDEC.

B. Amidi, JEDEC, and Vogt (Ground 9)

Claim 9 depends from claim 12 (PO Response 4) and is rejected under Amidi, JEDEC, and Vogt. Dec. 41. Vogt has not been relied upon to teach the above-noted feature missing from Amidi and JEDEC. *See id.* (citing RAN 7,

25–26¹⁵). For reasons similar to those discussed above related to independent claim 12, we withdraw the rejection in our earlier decision of dependent claim 9 based on Amidi, JEDEC, and Vogt.

C. Amidi and Dell '184 (Ground 10)

Independent claim 6 is also rejected based on Amidi and Dell '184. Dec. 41–42. We reconsider this rejection of claim 6 as now amended. In the previous Decision, we discussed Amidi and what one skilled in the art would have recognized when employing the creative steps and inferences in concluding claim 6 would be obvious. *Id.* As addressed above, the record does not demonstrate sufficiently the claimed “logic element generates rank-selecting signals” in response to the specifically recited signals in claim 6 based on Amidi and an ordinary skilled artisan’s background knowledge. In particular, when addressing Amidi, we previously discussed how this reference does not teach or suggest generating *rank-selecting* or chip-select signals *in response to* the specifically recited *signals (i) through (iv)* now recited in claim 6. We further stated, although Amidi and an ordinary artisan’s background knowledge may suggest directing a bank address signal to Amidi’s CPLD, the record does not suggest adequately one skilled in the art would have known to design a logic element, such as Amidi’s CPLD, to generate rank-selecting in response to signals (i) through (iv), including both a row address signal and bank addressing signals.

As for Dell '184, this reference suggest having a logic circuit receiving both address inputs and bank address signals from a memory controller. Dell '184, Abstract, 2:48–3:5, *cited in part* in Dec. 43. Specifically, Dell '184 teaches a logic

¹⁵ The previous Decision (Dec. 41) mistakenly referred to the rejection of *Dell*, JEDEC, and Vogt and pages 6, 15, and 16 of the RAN.

circuit (e.g., element 24 and function 50) that receives these address signals and specifically uses an address signal or a bank address signal to remap from N (e.g., 2) banks to M (e.g., 4) banks. *Id.*; *id.* at 4:23–58, 8:35–9:4, Fig. 1. However, the additionally generated and remapped signal is a *bank-selecting* signal that may assist in bank expansion (*see* Dec. 42–43), not a rank-selecting or chip-selecting signal as now recited in claim 6. Moreover, even assuming, without deciding, one skilled in the art would have recognized applying Dell ’184’s bank expansion teaching to Amidi’s rank expansion technique, Dell ’184 teaches a logic circuit uses either address signal or a bank address signal for remapping the additional signal rather than generating any rank-selecting signals *in response to signals (i) through (iv)*, which includes *both* a row address signal and bank address signals, as claim 6 now recites.

Our previous Decision also stated Dell ’184 “provides a reason to combine the references to achieve a DIMM that uses memory devices with various different attributes or configured differently than what the system expects.” *Id.* at 42–43 (citing the April 20, 2012 Requester’s Comments 85–86, Amidi ¶¶ 41–60, 71, and Dell ’184, Abstract, 2:48–59, 4:6–9). Yet, this reason based on Dell ’184 (and also Amidi) does not teach or suggest adequately to an ordinarily skilled artisan a known DIMM configured differently than what the system expects, such that its logic element generates the specifically recited rank-selecting signals in response to signals (i) through (iv) as now recited in claim 6.

We further cited to the Right of Appeal Notice (RAN) and Requester’s comments in our earlier Decision. *Id.* at 42 (citing RAN 7, 26 and April 20, 2012 Requester’s Comments 80–106, 112–113). The RAN does not discuss Amidi or Dell ’184 in any detail. RAN 7, 26. As for Requester’s comments, the discussion

of canceled claim 23 refers to claim 1 (now canceled) and claim 12 (now amended) to teach its recited features. April 20, 2012 Requester's Comments 112–113.

When addressing claims 1 and 12, Requester repeats the above discussion of Amidi and Dell '184 related to memory devices and remapping addressing signals to control the actual memory devices real configuration, which we previously stated does not suggest adequately generating rank-selecting signals in response to signals (i) through (iv) as now recited in claim 6. April 20, 2012 Requester's Comments 85–86 (citing Amidi ¶¶ 41–60, 71 and Dell '184 Abstract, 2:20–29, 48–59, 4:6–9), 90–95 (citing Amidi ¶¶ 37, 50, 52, 64, Fig. 6A and Dell '184, 2:48–59, Fig. 1), 99–101 (citing Amidi ¶ 52, Fig. 6A), 103–106 (citing Amidi ¶¶ 47–49, Fig. 5 and Dell '184, 2:48–59, 8:39–48).

Also, some of the discussion in the April 20, 2012 Requester's comments related to storing an input signal does not specifically concern the recited “logic circuit generates rank-selecting signals” in response to signals (i) through (iv) as now recited in claim 6. *See id.* Requester's comments address the recitations in canceled claim 1 of the input signals received by the memory module include row/column address signals and bank address signals (April 20, 2012 Requester's Comments 89–92 (citing Amidi ¶¶ 50, 52, Figs. 1, 6A)) and a logic element configurable to receive the set of input signals (*id.* at 93–95 (citing Amidi ¶¶ 37, 50, 64, 71, Fig. 4A and Dell '184, 2:48–59, Fig. 1)). However, as previously discussed, these teachings do not demonstrate to one skilled in the art that a logic circuit that generates rank-selecting signals in response to signals (i) through (iv) as now recited in claim 6 would have been known.

Requester additionally relies on Dr. Bagherzadeh's testimony, which essentially repeats the above discussion and Requester's position related to Amidi

and Dell '184's teachings. *See, e.g.*, April 20, 2012 Requester's Comments 85–86, 94 (citing 2d Bagherzadeh Decl. ¶¶ 14, 23–24). As previously noted, these teachings do not provide a sufficient teaching with a rational underpinning for one skilled in the art to suggest a logic circuit that *generates rank-selecting signals* in response to signals (i) through (iv) as now recited in claim 6.

Requester's comments also address canceled claim 26 and how Amidi's CPLD and register collectively teach or suggest the formerly recited *circuit*—not a logic element—configurable to select a rank in response to the set of inputs signals and Dell '184 in combination with Amidi teach or suggest storing an address bit. April 20, 2012 Requester's Comments 117–119 (citing Amidi ¶¶ 50, 52, Dell '184, and 2d Bagherzadeh Decl. ¶¶ 27–28). As amended claim 6 now exists, we are not persuaded by Requester's comments for the above-stated reasons. Moreover, Dr. Bagherzadeh's additional testimony does not provide adequate evidence to remedy what is missing from Amidi, Dell '184, and what one skilled in the art would have known to suggest the recited “logic circuit” that “generates rank-selecting signals” in response to signals (i) through (iv) as now recited in claim 6. *See* 2d Bagherzadeh Decl. ¶¶ 27–28.

Accordingly, we withdraw the rejection in our earlier decision of claim 6 based on Amidi and Dell '184.

IV. AFFIRMED REJECTIONS

In the earlier Decision, we affirmed the following rejections:

Reference(s)	Basis	Claims	
Dell and JEDEC (Ground 2)	§ 103	2, 3, 5, 7, 8, 10–12, and 14–18	RAN 6, 8–14; Dec. 10-20
Dell, JEDEC, and Vogt (Ground 3)	§ 103(a)	9	RAN 6, 15–16; Dec. 21
Amidi and Dell '184 (Ground 10)	§ 103(a)	2, 3, 5, 7, 8, 10–12, and 14–18	RAN 7, 26; Dec. 42-45

Based on the amendments to claim 12 and 15 (now independent claims), we revisit these sustained rejections.

A. Rejections based on Dell

1. Dell and JEDEC (Ground 2)

Upon review, we reverse the rejection of independent claims 12 and 15 based on Dell and JEDEC. The record does not sufficiently demonstrate Dell and JEDEC teach or suggest “the logic element generates rank-selecting signals of the output signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and [sic] (iii) the at least one chip-select signal received by the logic element and (iv) the PLL clock signal” as now recited in claims 12 and 15. Similar to the above discussion of Amidi, Dell does not teach or suggest generating rank-selecting signals in response to both a row address signal and bank address signals as well as signals (iii) and (iv).

Dell teaches using a row address signals (e.g., A11) inputted into a logic element (e.g., logic device 46) to change a signal actuating a single bank of DRAMS into one actuating two banks of DRAMS. Dell 4:56–62, 5:10–14, Abstract, Figs. 3–4; *see also* 2d Bagherzadeh Decl. ¶ 9. Thus, Dell suggests a logic element using a row address signal to generate bank-selecting signals. *See*

Dell 4:56–62, 5:10–14, Abstract, Figs. 3–4. However, just like Amidi, Dell does not teach or suggest a logic element using bank address signals as well as a row address signal, a chip-select signal, and a PLL clock signal to generate rank-selecting signals as recited in amended claims 12 and 15.

Likewise, as discussed above, JEDEC does not remedy this deficiency in Dell. *See generally* JEDEC 21-C and 79C. Nor does Dr. Bagherzadeh’s testimony related to what an ordinary artisan would recognized when employing their background knowledge support a suggestion that this missing feature in claims 12 and 15 is known. *See* 2d Bagherzadeh Decl. ¶¶ 9, 25. Namely, as indicated above, we are not persuaded the evidence and arguments in the record demonstrate a reason with sufficient, rational underpinning in Dell, JEDEC and/or based on an ordinarily skilled artisan’s background knowledge why one skilled in the art would design a logic element, like Dell’s logic device 46, to generate rank-selecting signals in response to signals (i) through (iv) as now recited.

Accordingly, based on the amendments to claims 12 and 15, all the evidence, and the arguments presented, we reverse the rejection of claims 12, 15, and dependent claims 2, 3, 5, 7, 8, 10, 11, 14, and 16–18 based on Dell and JEDEC.

2. Dell, JEDEC, and Vogt (Ground 3)

Claim 9 depends from claim 12 (PO Response 4) and is rejected under Dell, JEDEC, and Vogt (Dec. 21). Vogt has not been relied upon to teach the above-noted feature missing from Dell and JEDEC. *See id.* (citing RAN 6, 15–16). For reasons similar to those discussed above related to independent claim 12, we reverse the rejection of claim 9 and refer to the above discussion of Ground 2.

B. Rejection Based on Amidi and Dell '184 (Ground 10)

Claims 2, 3, 5, 7, 8, 10–12, 14–18, 23–27, and 29–35 are rejected under 35 U.S.C. § 103 based on Amidi and Dell '184. RAN 7, 26; Dec. 42–45. Claims 12 and 15 are independent claims that include similar “logic element” limitations to claim 6 or a logic element generates rank-selecting signals in response to signals (i) through (iv). *Compare* PO Response 5, 7, *with id.* at 3. The remaining claims depend directly or indirectly from claims 12 or 15 and thus include the previously discussed “logic circuit” limitation.

As discussed above, the record does not sufficiently demonstrate Amidi and Dell '184 alone or collectively suggest the above “logic circuit” recitation. We refer above when discussing claim 6 (Ground 10) for more details. Accordingly, we reverse the rejection of claims 2, 3, 5, 7, 8, 10–12, and 14–18 based on Amidi and Dell '184.

V. REJECTIONS PREVIOUSLY NOT REACHED

In the earlier Decision, we did not reach the following rejections:

Reference(s)	Basis	Claims	
Wong ¹⁶ and JEDEC (Ground 5)	§ 103(a)	2, 3, 5, 7, 8, 10–12, and 14–18	RAN 6, 17–22; Dec. 45–46
Wong, JEDEC, and Vogt (Ground 6)	§ 103(a)	9	RAN 6, 22–23; Dec. 45–46

¹⁶ U.S. Patent No. 6,414,868 B1 (issued July 2, 2002) (Wong).

A. Wong and JEDEC (Ground 5)

Based on the amendments to claims 12 and 15, we also reconsider the rejections based on Wong and JEDEC. Wong and JEDEC do not teach or suggest “the logic element generates rank-selecting signals of the output signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and [sic] (iii) the at least one chip-select signal received by the logic element and (iv) the PLL clock signal” as recited in claims 12 and 15. Similar to the above discussions of Amidi and Dell, Wong does not teach or suggest generating rank-selecting signals in response to both a row address signal and bank address signals as well as a chip-select signal and a PLL clock signal as amended claims 12 and 15 now recite.

Wong teaches a memory expansion module that uses row address signals (e.g., A0–A13), at least one of these signals (e.g., A13) used as a bank selection input to bank control circuit 2000 to drive signals to a selected memory bank (e.g., between an upper bank and a lower bank). Wong 3:24–25, 4:60–63, 5:26–35, Abstract, Figs. 3–6; *see also* 2d Bagherzadeh Decl. ¶ 11. Wong at best suggests a logic element (e.g., bank control circuit 2000) that uses a row address signal to generate bank-selecting signal. *See* Wong 3:24–25, 4:60–63, 5:26–35, Abstract, Figs. 3, 4A-B, 6. However, just like Amidi and Dell, Wong does not teach or suggest a logic element using bank address signals and thus signals (i) through (iv) to generate rank-selecting signals as recited in claims 12 and 15.

Also, as discussed above, JEDEC does not remedy this feature missing from Wong. Nor does Dr. Bagherzadeh’s testimony concerning what an ordinary artisan would recognized when employing their background knowledge suggest that this missing feature in claims 12 and 15 is known. *See* 2d Bagherzadeh Decl.

¶¶ 11, 26. Namely, as indicated above, we are not persuaded the evidence and arguments in the record demonstrate a reason with sufficient, rational underpinning in Wong and JEDEC or based on an ordinarily skilled artisan's background knowledge why one skilled in the art would design the logic element, like Wong's bank control circuit 2000, to generate rank-selecting signals in response to both bank address signals as well as signals (i), (iii), and (iv) as now recited in amended claims 12 and 15.

Upon reconsideration, based on the amendments to claims 12 and 15, all the evidence, and the arguments presented, we reverse the rejection of claims 12, 15, and dependent claims 2, 3, 5, 7, 8, 9, 10, 11, 14, and 16–18 based on Wong and JEDEC.

B. Wong, JEDEC, and Vogt (Ground 6)

As for claim 9, this claim depends from independent claim 12 (PO Response 4) and is rejected based on Wong, JEDEC, and Vogt (RAN 6, 22–23). Notably, Vogt is not relied upon to teach or cure the above-noted deficiencies. *See* September 26, 2013 Office Action 22–23. For reasons similar to those discussed above related to independent claim 12, we reverse the rejection of claim 9 and refer to the above discussion concerning Ground 5.

VI. CONCLUSIONS

For the above reasons, we withdraw the following new grounds of rejection presented in the earlier Decision: (1) claims 2, 3, 5–8, 10–12, and 14–18 based on Amidi and JEDEC (Ground 8), (2) claim 9 based on Amidi, JEDEC, and Vogt (Ground 9), and (3) claim 6 based on Amidi and Dell '184 (Ground 10), (4) claims 2, 3, 5, 7, 8, 10–12, and 14–18 based on Dell and JEDEC (Ground 2), (5) claim 9

based on Dell, JEDEC, and Vogt (Ground 3), and (6) claims 2, 3, 5, 7, 8, 10–12, and 14–18 based on Amidi and Dell '184 (Ground 10).

Additionally, upon reconsideration, we reverse the following affirmed rejections presented in the earlier Decision: (1) claims 2, 3, 5, 7, 8, 10–12, and 14–18 based on Dell and JEDEC (Ground 2), (5) claim 9 based on Dell, JEDEC, and Vogt (Ground 3), and (3) claims 2, 3, 5, 7, 8, 10–12, and 14–18 based on Amidi and Dell '184 (Ground 10). We also reverse the following rejections, previously not reached: (4) claims 2, 3, 5, 7, 8, 10–12, and 14–18 based on Wong and JEDEC (Ground 5), and (5) claim 9 based Wong, JEDEC, and Vogt (Ground 6).

Requests for extensions of time in this *inter partes* reexamination proceeding are governed by 37 C.F.R. §§ 1.304, 1.956, and 41.79(e). *See* 37 C.F.R. § 41.79.

In the event neither party files a request for rehearing within the time provided in 37 C.F.R. § 41.79, and this decision becomes final and appealable under 37 C.F.R. § 41.81, a party seeking judicial review must timely serve notice on the Director of the United States Patent and Trademark Office. *See* 37 C.F.R. §§ 90.1 and 1.983.

REVERSED; 37 C.F.R. § 41.77(f)

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