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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and SK HYNIX MEMORY SOLUTIONS INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2017-00549
Patent 8,756,364 B1

Before STEPHEN C. SIU, MATTHEW R. CLEMENTS, and SHEILA F. McSHANE, *Administrative Patent Judges*.

SIU, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

SK Hynix Inc. ("Petitioner") requested *inter partes* review of claims 1–4, 6, 7, 10, 13, 17, and 23 of U.S. Patent No. 8,756,364 B1 ("the '364 patent," Ex. 1001). Paper 1 ("Pet."). On May 15, we issued a Decision to Institute an *inter partes* review (Paper 7, "Inst. Dec.") of claims 1–4, 6, 7, 10, 13, 17, and 23 of the '364 patent under 35 U.S.C. § 103(a) as unpatentable over Halbert[1] and Amidi.[2] Inst. Dec. 4, 12.

After institution of trial, Netlist, Inc. ("Patent Owner") filed a Patent Owner's Response (Paper 12, "PO Resp."), to which Petitioner replied (Paper 16, "Pet. Reply"). Oral argument was conducted on February 14, 2018. A transcript of that argument has been made of record. Paper 28.

We have jurisdiction under 35 U.S.C. § 318(a). After considering the evidence and arguments of both parties, and for the reasons set forth below, we determine that Petitioner met its burden of showing, by a preponderance of the evidence, that claims 1–4, 6, 7, 10, 13, 17, and 23 of the '364 patent are unpatentable.

RELATED MATTERS

The '364 patent is the subject of the following: *Netlist, Inc. v. SK Hynix Inc.*, Case No. 8:16-cv-01605 (C.D. Cal.) and *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (International Trade Commission). *See* Pet. iii; Paper 4.

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[1] US Patent Publication 2002/0112119 A1, published August 15, 2002 ("Halbert," Ex. 1005).
[2] US 8,250,295 B2, issued August 21, 2012 ("Amidi," Ex. 1006).

THE ’364 PATENT (EX. 1001)

The ’364 Patent describes improvements to memory modules. Ex. 1001, 1:32–33.

ILLUSTRATIVE CLAIM

Independent claim 1 is representative of the claimed subject matter. Claim 1 is reproduced below:

> 1. A memory module to be coupled to a memory controller via a plurality of signal lines, including input control signal lines, DQ data signal lines and DQS data strobe signal lines, the memory module comprising:
>
> a first logic element to receive input control signals associated with a first memory command from the memory controller via the input control signal lines, and to generate output control signals in response to the input control signals;
>
> memory devices organized in a number of ranks including a first rank receiving a first set of one or more of the output control signals and at least one second rank receiving at least one second set of one or more of the output control signals, wherein a first memory device in the first rank and at least one second memory device in the at least one second rank communicate with the memory controller via a common set of the DQ and DQS signal lines among the plurality of signal lines; and
>
> a second logic element to selectively enable data communication between the first memory device and the memory controller via the common set of the DQ and DQS signal lines in response to the first memory command while isolating a load associated with the at least one second memory device from the common set of the DQ and DQS signal lines;
>
> wherein the first logic element is configured to determine a latency value based on a previous memory command received by the memory module from the memory controller, and wherein the first logic element controls the second logic element to selectively enable the data communication according to the latency value.

OVERVIEW OF PRIOR ART

Halbert (Exhibit 1005)

Halbert describes memory devices, systems, and module architectures. Ex. 1005 ¶ 2.

Amidi (Exhibit 1006)

Amidi describes a four rank memory module with two chip select signals routed. Ex. 1006, 2:47–49.

THE PARTIES' POST-INSTITUTION ARGUMENTS

In our Decision on Institution, we concluded that the arguments and evidence advanced by Petitioner demonstrated a reasonable likelihood that claims 1–4, 6, 7, 10, 13, 17, and 23 of the '364 patent are unpatentable under 35 U.S.C. § 103(a) over Halbert and Amidi. Inst. Dec. 12. We must now determine whether Petitioner has established by a preponderance of the evidence that the specified claims are unpatentable over the cited prior art. 35 U.S.C. § 316(e). We previously instructed Patent Owner that "any arguments for patentability not raised in the [Patent Owner Response] will be deemed waived." Paper 8, 3; *see also* 37 C.F.R. § 42.23(a) ("Any material fact not specifically denied may be considered admitted."); *In re Nuvasive, Inc.*, 842 F.3d 1376, 1379–1382 (Fed. Cir. 2016) (holding Patent Owner waived an argument addressed in Preliminary Response by not raising the same argument in the Patent Owner Response). Additionally, the Board's Trial Practice Guide states that the Patent Owner Response "should identify all the involved claims that are believed to be patentable and state

the basis for that belief." Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012).

With a complete record before us, we note that we have reviewed arguments and evidence advanced by Petitioner to support its unpatentability contentions where Patent Owner chose not to address certain limitations in its Patent Owner Response. In this regard, the record now contains persuasive, unrebutted arguments and evidence presented by Petitioner regarding the manner in which the asserted prior art teaches corresponding limitations of the claims against which that prior art is asserted. Based on the preponderance of the evidence before us, we conclude that the prior art identified by Petitioner teaches or suggests all uncontested limitations of the reviewed claims. The limitations that Patent Owner contests in the Patent Owner Response are addressed below.

ANALYSIS

Petitioner's Initial Positions

Petitioner asserts that a combination of Halbert and Amidi renders obvious claims 1–4, 6, 7, 10, 13, 17, and 23. Pet. 54–62. We have reviewed the Petition, Patent Owner's Response, and Petitioner's Reply, as well as the relevant evidence discussed in those papers and other record papers, and are persuaded that the record sufficiently establishes Petitioner's contentions for claims 1–4, 6, 7, 10, 13, 17, and 23, and we adopt Petitioner's contentions discussed below as our own.

For example, claim 1 recites a memory module comprising a first logic element and that the first logic element is configured to receive input control signals from a memory controller and to generate output control

signals in response to the input control signals. Petitioner argues that Halbert discloses this feature. Pet. 30–33. For example, as Petitioner explains, Halbert discloses a "module controller 110" that receives input control signals (e.g., "ADD/CMD") and, in response, generates output control signals (e.g., "RDQS," "DIR," etc.). Ex. 1005, Fig. 4.

Claim 1 recites memory devices organized in a first rank and a second rank, each of which receives a set of output control signals, and that a device in each of the first and second ranks communicates with the memory controller via a common set of DQ and DQS signal lines. Petitioner argues that Halbert discloses this feature. Pet. 33–36. As Petitioner explains, Halbert discloses memory devices organized in a first rank (e.g., "Rank 140") and a second rank (e.g., "Rank 142"), each of which receives RADD and RCMD signals, and each of which communicates with a memory controller via a common set of DQ and DQS signal lines (e.g., "DQ" and "DQS"). Ex. 1005, Fig. 4.

In addition, as Petitioner explains, Amidi confirms that it was known to those of ordinary skill in the art to provide different control signals to different devices in different "ranks." Pet. 54–55. For example, as Petitioner states, Amidi discloses memory devices organized in different "ranks" in which "each rank receiv[es] a different set of control[] signals." *Id*. (citing Ex. 1006, Figs. 3, 6A). Petitioner also provides a rationale as to why it would have been obvious to one of ordinary skill in the art to have combined the teachings of Halbert and Amidi. *Id*. at 54–59. Petitioner points to the analogous nature of the prior art, i.e. memory module design, as well as their relevant pertinence to the particular problem of the '364 patent, that is, efficient support of multi-rank memory modules. *Id*. at 54.

Claim 1 recites a second logic element to selectively enable data communication between the first memory device and the memory controller via the common set of the DQ and DQS signal lines while isolating a load associated with a second memory device from the common set of the DQ and DQS signal lines. Petitioner argues that Halbert discloses this feature. Pet. 36–42. As Petitioner explains, Halbert discloses a "data interface circuit 120" that enables communication between module controller 110 (i.e., a "first logic element") and the memory controller via a common set of DQ and DQS signal lines "selectively" (e.g., during separate clock cycles or during different modes). *Id.*; Ex. 1005, Figs. 4, 7, 8.

As Petitioner also explains, Halbert discloses that the communication between module controller 110 and the memory controller occurs while a load associated with data interface circuit 120 is isolated from the common set of the DQ and DQS signal lines because, for example, the memory module of Halbert includes "MUX/DEMUX 24 and related circuitry" interposed between the common DQ and DQS signal lines and memory devices and, according to Petitioner, one of skill in the art "would understand that a multiplexer [and/or 'tri-state logic devices']. . . electrically separates, and therefore isolates" the common DQ and DQS signal lines for an associated load of the data interface circuit 120. Pet. 41–42 (citing Ex. 1003 ¶ 148).

Claim 1 recites that the first logic element is configured to determine a latency value based on a previous memory command and controls the second logic element to selectively enable the data communication according to the latency value. Petitioner argues that Halbert discloses this feature. Pet. 43–45. As Petitioner explains, Halbert discloses that "latency"

of placing data on bus lines with respect to memory modules was known in the art and implemented on prior art devices, that the system of Halbert is "compatible with" pre-existing memory technology, that known operations (e.g., "read" or "write" operations) may be performed with the Halbert system in a similar fashion as in pre-existing devices and systems, and that the module controller 110 (i.e., the "first logic element") synchronizes operation of the memory module via timing and synchronization signals. *Id*. at 43–44.

In addition, Petitioner argues that latency values "were conventionally set by a . . . command issued by the memory controller of the system" and that such commands would "pass first through the module controller 110 [i.e., a 'first logic element'] [that] 'snoops' the . . . signals . . . to control the interface circuits." Pet. 49–50 (citing Ex. 1003 ¶¶ 166–168; Ex. 1005 ¶¶ 29, 34; Ex 1007, 8)). Petitioner also states that it would have been obvious to one of ordinary skill in the art to have provided for a first logic element, such as the "module controller 110" of Halbert, that determines a latency value to control a second logic element (e.g., the interface of Halbert), given that it was known that the "module controller 110" of Halbert (i.e., a "first logic element") receives and "snoops" data streams that contain commands to set a latency and that the "module controller 110" would control interface circuits based on such "snooped" signals. *Id.* at 50–52.

Petitioner has provided a similar detailed analysis of claims 2–4, 6, 7, 10, 13, 17, and 23. *See* Pet. 54–62. Notwithstanding Patent Owner's arguments, which we have considered and which we address below, we are persuaded by Petitioner's showing, which we adopt as our own findings and

conclusions, that claims 1–4, 6, 7, 10, 13, 17, and 23 are unpatentable under 35 U.S.C. § 103(a) as obvious over Halbert and Amidi.

Whether the proposed combination of Halbert and Amidi would have been "predictable and expected"

Patent Owner argues that the proposed combination of Halbert and Amidi would not have been a "predictable and expected result" because it "proposes novel, not 'known,' uses of CAS latency values"—i.e., "determining CAS latency values by Halbert's module controller 110, which is external to memory device array 140/142" and "using CAS latency values by Halbert's module controller 110 for setting the timing of a directional signal like Halbert's DIR signal shown in Figs. 4 and 5." PO Resp. 6–8

Petitioner counters

> (i) that the use of CAS latency was a known, reliable, standardized technique for communicating between a system memory controller and memory devices, (ii) that Halbert discloses a module controller that snoops commands from the memory controller for controlling the timing of module control signals (*e.g.*, "DIR"), and that CAS latency is set by one of those commands, and (iii) that Halbert discloses that its system is compatible with existing memory controllers and memory devices that operated in conjunction with a load mode register command set forth in the relevant JEDEC standard of the time

Pet. Reply 3 (citing Pet. at 27–28, 43–45, 49–52; Ex.1003, ¶¶94–97,158–73). Moreover, Petitioner argues that "Dr. Sechen conceded that both CAS latency and the Mode Register Set command were known to those [of] ordinary skill in the prior art . . . and that a Skilled Artisan would have known how to successfully implement circuitry to snoop such a command and practice the Latency Limitation." Pet. Reply 5 (citing Ex. 1024, 88:23–89:15, 137:2–21, 172:23–173:19).

We agree with Petitioner. Patent Owner's argument is predicated on a mischaracterization of the proposed combination as using CAS latency to adjust the timing only of the DIR signal. The DIR signal, however, is just an example of the values that Halbert's module controller snoops from CMD signals. Ex. 1005 ¶ 34. Petitioner proposes explicitly snooping CAS latency, not DIR, from the Mode Register Set command and using CAS latency to adjust the timing of the interface circuits, not DIR:

> In the system of Halbert[,] memory commands from the system memory controller pass first through the module controller 110. Ex. 1005 at [0029]. Moreover, Halbert discloses that his module controller 110 "snoops" the command signals as they pass through and will use the "snooped" signals to generate module control signals to control the interface circuits for the interface circuits 125 and 130. Ex. 1005 at [0034]; *see also id.* at 6:5-8. Ex. 1003, ¶168.
>
> It would have been obvious for the module controller 110 of Halbert to snoop the Mode Register Set commands from the memory controller and thereby determine the appropriate CAS latency values to be used . . . , and a person of ordinary skill would have been motivated to include such functionality in the system of Halbert, for several reasons. Ex. 1003, ¶169.

Pet. 50. Petitioner also explains why a person of ordinary skill in the art would have been motivated to do so:

> First, it would have been advantageous, and possibly necessary, to do so in order for the system of Halbert to output data signals on the DQ signal lines at the appropriate time. CAS latency was a well known and conventional characteristic of memory systems at the time. *See, e.g.*, Ex. 1017 at 8 (Samsung SDRAM datasheet showing SDRAM CAS latency programmable between 2 and 3 clock cycles). In order to provide a memory controller with data read from a DRAM the data must be available on the DQ bus at the appropriate time. That timing requires taking into consideration the appropriate CAS latency for the memory devices being used. *See, e.g.*, Ex. 1007 at 17 (disclosing that

> READ data during READ bursts are available following the CAS latency). Ex. 1003, ¶170.
>
> A skilled artisan would also have been motivated to include this functionality in Halbert based on Halbert's disclosure that his system seeks to be "compatible with an existing memory controller/bus and with existing memory devices." Ex. 1005 at [0023]. The simplest way to provide such compatibility would have been for Halbert's module controller 110 to snoop the Mode Register Set commands issued by the memory controller during initialization in order to obtain necessary configuration information, such as CAS latency. Those commands already were communicated through the module controller in the system of Halbert, that module controller already had the ability to snoop such commands, and the commands already included the CAS latency information Halbert's system needed to communicate data back to the memory controller. As Dr. Stone explains, "[e]xtending this existing functionality to snoop the Mode Register Set commands to obtain the necessary and well-known CAS latency information was therefore an easy and advantageous way to improve system performance, and also would have been an entirely predictable variation of what is disclosed in Halbert." Ex. 1003, ¶171

Pet. 51–52. Based on Petitioner's explanation, and taking into account the testimony of Dr. Sechen, we remain persuaded that the use of Halbert's module controller 110 to snoop CAS latency from the Mode Register Set command would have been predictable and led to the expected result.

Whether the proposed combination would have been uniquely challenging or difficult

Patent Owner argues that our preliminary determination in the Decision on Institution that the proposed combination would not have been uniquely challenging or difficult was incorrect because (1) the proposed combination relies upon novel, not "known," uses of CAS latency values;

and (2) "it merely states that elements are 'known,' which is not the requ[i]site 'reason' or 'reasoning' identified by MPEP." PO Resp. 9–11.

We are not persuaded by Patent Owner's arguments that the proposed combination relies upon novel, not known, uses of CAS latency values for the reasons discussed above. We also are not persuaded by Patent Owner's MPEP-based argument because it mischaracterizes our preliminary determination that the Petition articulates sufficiently a reason to combine Halbert and Amidi. Our determination was not based solely on whether it would have been uniquely challenging or difficult for a person of ordinary skill in the art to make the combination, but rather on Petitioner's extensive argument and evidence, including the testimony of Dr. Stone (Ex. 1003), as discussed above.

Whether combination would have been common sense

Patent Owner argues that it would have been contrary to the common sense of one of ordinary skill in the art to have determined a known parameter by a component that uses that known parameter because, according to Patent Owner, it would have been common sense to one of ordinary skill in the art to have performed the following alternative actions:

1) "do nothing,"
2) "simply use . . . 'the first READ command' [to "assert the DIR signal"],"
3) "use . . . 'transition on MDQS' to 'data strobe MDQS low,'" or
4) perform a prior art method that "involve[s] . . . less components, power consumption, and layout area, . . . and resources."

PO Resp. 13–20, 27. Based on these alternatives, Patent Owner concludes that

> a POSITA would see that implementations based on Halbert's own teachings (*e.g.*, READ command detection or MDQS transition low detection) would involve four to five times less components, power consumption, and layout area, along with correspondingly lesser amounts in time and resources in designing, implementing, and testing, than the implementation of Hynix's proposed modification based on [the proposed combination].

Id. at 27.

We are not persuaded by Patent Owner's argument at least because Patent Owner's proposed alternatives, even if assumed to be "common sense," do not show that the proposed combination is *not* common sense. Moreover, Patent Owner focuses on alternatives for determining the timing of Halbert's DIR signal (*id.* at 14 (citing Ex. 2002, Stone Depo., 34:2–18), but Dr. Stone did not identify only Halbert's DIR signal in the cited testimony. He also identified RDQS, REG_SEL, RDQS0 and RDQS1. Ex. 2002, 34:2–18. Even assuming Patent Owner is right about DIR, it does not follow that Patent Owner's "contrasting implementation[s]" (*id.*) would adjust the timing for all of the necessary signals while still achieving the purported advantages over Petitioner's proposed combination.

Whether the combination would have
been obvious even with work or expense
or even if not "advantageous and/or necessary"

Patent Owner reiterates arguments that one of ordinary skill in the art would have encountered additional "work" or "expense" upon combination of the cited prior art references and that there would have been no "apparent

reason" for one of ordinary skill in the art to have combined the cited references. PO Resp. Br. 28–32. Patent Owner also repeats arguments that the "proposed modification . . . [is] not 'advantageous and/or necessary." PO Resp. 33-42.

We are not persuaded by Patent Owner's arguments. The focus of 35 U.S.C. § 103 is on the obviousness of an invention to a person of ordinary skill in the art. *Environmental Design, Ltd. v. Union Oil Co.*, 713 F.2d 693, 697 (Fed. Cir. 1983). "That a given combination would not be made by businessmen for economic reasons does not mean that persons skilled in the art would not make the combination because of some technological incompatibility. Only the latter fact would be relevant." *In re Farrenkopf*, 713 F.2d 714, 718 (Fed. Cir. 1983) (citing *Orthopedic Equipment Co. v. United States*, 702 F.2d 1005, 1013 (Fed. Cir. 1983)). Even assuming that the proposed combination would have required additional work or expense over other alternatives, neither makes the combination nonobvious. Obviousness does not require that the proposed combination would have been *necessary* or more *advantageous* than other possible combinations.

PETITIONER'S MOTION TO EXCLUDE

Petitioner objects to Exhibits 2001–2002 and moves to exclude "Dr. Sechen's redirect testimony in response to improper leading questions." Paper 13, 18 (citing Ex. 1024, 182:20–184:15). Patent Owner opposes Petitioner's Motion to Exclude. Paper 23. Petitioner's objections to evidence and motion to exclude are moot because, even without dismissing

this evidence, we are persuaded that the claims are unpatentable. As a result, Petitioner's motion to exclude is dismissed.

SAS INSTITUTE INC. v. IANCU

The Supreme Court issued its decision on April 24, 2018, in *SAS Institute Inc. v. Iancu* concerning final written decisions issued by the Board addressing all claims a petitioner challenged in a petition. *SAS Institute Inc. v. Iancu*, No. 16-969, 2018 WL 1914661 (April 24, 2018). To the extent either Patent Owner or Petitioner believes that the Court's decision in *SAS Institute* requires additional consideration in this proceeding, the parties may file a rehearing request pursuant to 37 C.F.R. § 42.71(d).

CONCLUSION

Petitioner has shown by a preponderance of the evidence that claims 1–4, 6, 7, 10, 13, 17, and 23 are unpatentable under 35 U.S.C. § 103(a) over Halbert and Amidi.

ORDERS

After due consideration of the record before us, it is:

ORDERED that claims 1–4, 6, 7, 10, 13, 17, and 23 of the '364 patent are held unpatentable;

FURTHER ORDERED that Petitioner's Motion to Exclude is dismissed; and

FURTHER ORDERED that, because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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