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Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INPHI CORPORATION
Requester and Appellant

v.

NETLIST, INC.
Patent Owner and Respondent

Appeal 2017-007075
Inter partes Reexamination Control 95/001,337
United States Patent 7,636,274 B2
Technology Center 3900

Before JOHN A. JEFFERY, KEVIN F. TURNER, and
DENISE M. POTHIER, *Administrative Patent Judges*.

JEFFERY, *Administrative Patent Judge*.

DECISION ON APPEAL

In an earlier Decision, Appeal Number 2013-009044 mailed January 16, 2014 ("Bd. Dec."), another panel of this Board[1] affirmed-in-part the Examiner's decision rejecting claims 1–104 in connection with this *inter partes* reexamination of U.S. Patent 7,636,274 B2 ("'274 patent"). In that decision, the earlier panel affirmed the Examiner's decision declining to reject then-pending claims 1, 4–17, 23, 28–30, 32–34, 39–41, 44–47, 54–61, 63–66, 69, 74–76, 79, 84–86, 88, 89, and 94–96 under § 103 over QBMA and JEDEC.[2]

The earlier panel, however, reversed the Examiner's decision declining to reject the then-pending claims under § 103 as follows:

(1) claims 1–3, 18–22, 24–28, 31, 35–39, 42, 43, 48–53, 56, 62, 67, 68, 70–73, 84, and 87 over QBMA and Dell ("Issue 3")[3];

(2) claims 1–14, 16–21, 23–48, 50–53, 55–64, 66–94, 96, and 97 over Wong and Karabatsos ("Issue 6");

(3) claims 1–6, 8–14, 16, 18–46, 48–64, 67–97 over Dell and Karabatsos ("Issue 7");

(4) claims 98–104 over QBMA and Dell ("Issue 8");

(5) claims 98–104 over Karabatsos and Dell ("Issue 9");

(6) claims 98–104 over QBMA, Dell, and Kazuo ("Issue 10");

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[1] Judge Pothier replaces then-Judge Weinberg in the current panel.
[2] These and other previously-cited references are cited in full on pages 6 and 7 of the Board's earlier decision. Therefore, we omit their full citations here for brevity.
[3] For clarity and consistency, we refer to the issue numbers corresponding to those used by the parties, the Examiner, and the panel in the earlier Board decision.

(7) claims 98–104 over Karabatsos, Dell, and Kazuo ("Issue 11"); and

(8) claims 98–104 over Wong, Karabatsos, and Kazuo ("Issue 12").

Bd. Dec. 26.

On February 18, 2014, Requester filed a request to rehear the Board decision. About one month later, Patent Owner filed (1) comments on Requester's rehearing request, and (2) a request to reopen prosecution under § 41.77(b)(1). *See* Respondent's Comments to Request for Rehearing Under 37 C.F.R. § 41.79(c) filed Mar. 19, 2014; *see also* Patent Owner's Response Requesting to Reopen Prosecution Pursuant to 37 C.F.R. § 41.77(b)(1) filed Mar. 18, 2014 ("Mar. 2014 PO Amd't"). Patent Owner's latter request included an amendment (1) cancelling claims 6, 16, 19–21, 24, 35, 44, 47, 49, 50, 52, 67, 68, 70, 80, 89, 91, and 92, and (2) amending claims 1, 15, 22, 25–29, 36–39, 45, 51, 53, 56, 58, 60, 65, 71–75, 81, 82, 84, 90, 96, 98–100, 102, and 104. *Id.* at 21. Patent Owner also filed a supplemental declaration from Dr. Carl Sechen dated March 17, 2014, in connection with this latter response. Supplemental Declaration of Dr. Carl Sechen Under 37 C.F.R. § 1.132 filed Mar. 18, 2014 ("Supp. Sechen Decl.").

About one month later, Requester filed comments on Patent Owner's response (1) arguing that the proposed amended claims remained unpatentable over the references cited by the Board in its new ground of rejection, and (2) proposing a new rejection based on new prior art, namely Amidi,[4] Klein,[5] and Matsui.[6] *See* Third Party Requester's Comments on

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[4] US 2006/01171152 A1, published June 1, 2006.
[5] US 6,349,051 B1, issued Feb. 19, 2002.
[6] US 7,155,627 B2, issued Dec. 26, 2006.

Patent Owner's Response, and Corrected Response, Requesting to Reopen Prosecution Pursuant to 37 C.F.R. § 41.77(b)(1) filed Apr. 17, 2014 ("Apr. 2014 TPR Comments"). Requester also filed a supplemental declaration of Dr. David Wang dated April 15, 2014, in connection with this response.

On June 26, 2014, the Board granted Requester's rehearing request in part. Specifically, the Board modified its decision to add new grounds of rejection for claims 15 and 65, but otherwise did not change any other aspect of its original decision. *See* Dec. on Req. for Reh'g filed June 26, 2014, at 4–6. After the Board's decision on rehearing, Patent Owner filed an amendment proposing to cancel claims 15 and 65. *See* Amendment Under 37 C.F.R. § 41.63(a) filed July 29, 2014.

On September 5, 2014, Requester filed corrected comments on Patent Owner's response requesting to reopen prosecution. As in Requester's April 2014 comments, Requester in the September 2014 comments (1) argued that the proposed amended claims remain unpatentable over the references cited by the Board in its new ground of rejection, and (2) proposed a new rejection based on new prior art, namely Amidi, Klein, and Matsui ("Issue 13").[7] *See* Third Party Requester's Corrected Comments on Patent Owner's Response, and Corrected Response, Requesting to Reopen Prosecution Pursuant to 37 C.F.R. § 41.77(b)(1), filed Sept. 5, 2014 ("Sept. 2014 TPR Comments"). Accompanying these comments were, among other things, a supplemental declaration of Dr. David Wang dated April 15, 2014 ("Supp. Wang Decl.") and a declaration of Dr. Srinivasan Jagannathan ("Jagannathan Decl."), the

[7] For clarity, we refer to this proposed rejection as "Issue 13" consistent with the parties' nomenclature.

latter of which was filed in connection with an *inter partes* review proceeding (IPR2014-00883) involving a different patent.

After this submission, the Board (1) granted Patent Owner's request to reopen prosecution; (2) entered all of Patent Owner's proposed amendments and accompanying evidence; (3) entered all of Requester's comments and accompanying evidence; and (4) remanded the case to the Examiner for a determination under 37 C.F.R. § 41.77(d) in view of these submissions and the Board's decision mailed January 16, 2014. *See* Order Remanding *Inter Partes* Reexamination Under 37 C.F.R. § 41.77(d) to the Examiner mailed Sept. 26, 2014 ("Remand Order"), at 2–4, *vacated in part by* Revised Order Remanding *Inter Partes* Reexamination Under 37 C.F.R. § 41.77(d) to the Examiner mailed July 14, 2015 ("Revised Remand Order").[8]

After this revised remand order, the proceeding returned to the Examiner for consideration under 37 C.F.R. § 41.77(d). In that determination, the Examiner concluded that the following rejections under § 103 should be maintained:

(1) claims 1–3, 18, 22, 25–28, 31, 36–39, 42, 43, 48, 51, 53, 56, 62, 71–73, 84, and 87 over QBMA and Dell ("Issue 3");

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[8] The Board's revised order was responsive to a mandamus order to enter Requester's comments in their entirety. *See* Revised Remand Order, at 2 (citing *In re Inphi Corp.*, No. 2015-126, slip op. at 7 (Fed. Cir. June 30, 2015)). In view of the court's order, the Examiner's first determination under 37 C.F.R. § 41.77(d) mailed June 15, 2015 was vacated on July 8, 2015. Therefore, unless otherwise indicated, all references to the Examiner's § 41.77(d) determination in this opinion are to the Examiner's subsequent determination mailed September 11, 2015.

(2) claims 1–5, 7–14, 17, 18, 23, 25–34, 36–43, 45, 46, 48, 51, 53, 55–64, 66, 69, 71–79, 81–88, 90, 93, 94, 96, and 97 over Wong and Karabatsos ("Issue 6");

(3) claims 1–5, 8–14, 18, 22, 23, 25–34, 36–43, 45, 46, 48, 51, 53–64, 69, 71–79, 81–88, 90, and 93–97 over Dell and Karabatsos ("Issue 7");

(4) claims 98–104 over QBMA and Dell ("Issue 8");

(5) claims 98–104 over Karabatsos and Dell ("Issue 9");

(6) claims 98–104 over QBMA, Dell, and Kazuo ("Issue 10");

(7) claims 98–104 over Karabatsos, Dell, and Kazuo ("Issue 11");

(8) claims 98–104 over Wong, Karabatsos, and Kazuo ("Issue 12");

(9) claims 1–5, 7–14, 17, 18, 22, 23, 25–34, 36–43, 45, 46, 48, 51, 53–64, 66, 69, 71–79, 81–88, 90, and 93–104 over Amidi, Klein, and Matsui ("Issue 13"). *See* Determination Under 37 C.F.R. § 41.77(d) mailed Sept. 11, 2015 ("Ex'r Det."), at 13.

In response to the Examiner's determination, both Patent Owner and Requester submitted comments and accompanying declarations under 37 C.F.R. § 41.77(e) that were not entered. *See* Office Communication mailed Nov. 8, 2016, at 2–3 (declining to enter (1) Patent Owner's comments and accompanying declaration from Dr. Carl Sechen received Oct. 14, 2015, and (2) Requester's comments and accompanying declaration from Dr. David Wang received Nov. 13, 2015).

After the Examiner declined to enter the post-determination comments and evidence, Patent Owner petitioned to enter its comments under § 41.77(e) on November 22, 2016. That petition was granted-in-part to give (1) Patent Owner an opportunity file comments and evidence responsive to

the Examiner's determination that is narrowly tailored to Issue 13, and (2) Requester an opportunity to reply to those comments, if filed, with evidence similarly narrowly tailored to Issue 13. *See* Petition Decision mailed Jan. 23, 2017, at 5–6.

After this petition decision, Patent Owner filed revised comments with an accompanying declaration by Dr. Carl Sechen narrowly tailored to Issue 13. *See* Patent Owner's Revised Comments In Response to Examiner's Determination Pursuant to 37 C.F.R. § 41.77(e) filed Feb. 22, 2017 ("PO Revised Feb. 2017 Comments"); *see also* Revised Second Supplemental Declaration of Dr. Carl Sechen Under 37 C.F.R. § 1.132 filed Feb. 22, 2017 ("Rev. 2d Supp. Feb. 2017 Sechen Decl."). Requester filed a reply to these revised comments along with a redacted second supplemental declaration of Dr. David Wang likewise narrowly tailored to Issue 13. *See* Requester's Reply to Patent Owner's Revised Comments in Response to Examiner's Determination Pursuant to 37 C.F.R. § 41.77(e) filed Mar. 22, 2017 ("TPR Mar. 2017 Reply"); *see also* Redacted Second Supplemental Declaration of David Wang, Ph.D. filed Mar. 22, 2017 ("Redacted 2d Supp. Wang Decl.").

The proceeding then returned to us to reconsider the matter and issue a new decision under 37 C.F.R. § 41.77(f).

Independent claim 1 is reproduced below:

> 1. A memory module comprising:
>
> a plurality of double-data-rate (DDR) memory devices arranged in one or more ranks, each DDR memory device having a corresponding first load and a corresponding second load, each DDR memory device having a data strobe signal (DQS) line and a DQS line load for the DQS line as the corresponding second load;

a circuit comprising a logic element and a register,

the circuit electrically coupled to the plurality of DDR memory devices and configured to be electrically coupled to a memory controller of a computer system to receive a set of input signals from the computer system, the set of input signals comprising row/column address signals, bank address signals, and DDR chip-select signals, the set of input signals compatible with a system memory domain of the computer system, the circuit configured to be electrically coupled to the memory controller of the computer system to receive a DDR command from the computer system,

the circuit configurable to monitor the DDR command to control isolation of one or more of the DQS line loads of the DDR memory devices from the computer system or from each other,

the circuit configurable to be responsive to the set of input signals by selectively isolating one or more of the corresponding first loads of the DDR memory devices from the computer system,

the circuit configurable to translate the DDR command between the system memory domain of the computer system and a physical memory domain of the memory module for a selection of at least one rank among the one or more ranks, wherein the system memory domain has a first memory density per rank, and the physical memory domain has a second memory density per rank less than the first memory density per rank; and

a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register.

RELATED PROCEEDINGS

In addition to the related proceedings noted on pages 3 and 4 of the earlier panel's decision, we add the following regarding some of those proceedings and others. First, the Board's decision affirming the Examiner's decision declining to reject the claims in *inter partes*

reexamination proceeding Control No. 95/001,381 (Appeal No. 2013-9066) involving U.S. Patent 7,532,537—the parent of the '274 patent—was affirmed by the Court of Appeals for the Federal Circuit ("Federal Circuit"). *See Inphi Corp. v. Netlist, Inc.*, 805 F.3d 1350 (Fed. Cir. 2015).

Second, the Board affirmed the Examiner's rejection of the appealed claims in merged reexamination Control Nos. 95/000,546 and 95/000,577 for U.S. Patent 7,289,386. *See Google Inc. v. Netlist, Inc.*, No. 2014-007777 (PTAB Feb. 24, 2015), *reh'g denied* (PTAB Aug. 27, 2015). After the Federal Circuit dismissed an appeal of that decision, a reexamination certificate issued. *See Netlist, Inc. v. Google Inc., Smart Modular Technologies, Inc.*, Nos. 16-1270, -1271 (Fed. Cir. Jan. 28, 2016) (non-precedential); *see also* US 7,289,386 C1 issued Aug. 19, 2016.

Another panel of this Board also affirmed-in-part the Examiner's decision to reject or not reject various claims in three merged *inter partes* reexaminations, namely Control Nos. 95/000,578, 95/000,579, and 95/001,339. *See Inphi Corp. v. Netlist, Inc.*, No. 2015-006849 (PTAB May 31, 2016). That panel also affirmed the Examiner's decision to reject various claims in *inter partes* reexamination Control No. 95/001,758. *See Smart Modular Technologies (WWH), Inc. v. Netlist, Inc.*, No. 2015-007761 (PTAB May 31, 2016). In addition, that panel reversed the Examiner's decision favorable to patentability of various claims in *inter partes* reexamination Control No. 95/002,399. *See Netlist, Inc. v. Smart Modular Technologies, Inc.*, No. 2016-006595 (PTAB Nov. 10, 2016). Prosecution reopened in all of these proceedings, and the cases were remanded to the Examiner for respective determinations under 37 C.F.R. § 41.77(d).

Lastly, this appeal is related to several *inter partes* review proceedings where the Board issued final written decisions that were appealed to the Federal Circuit. *See Diablo Technologies, Inc. v. Netlist, Inc.*, No. IPR2014-00882 (PTAB Dec. 14, 2015); *Diablo Technologies, Inc. v. Netlist, Inc.*, No. IPR2014-00883 (PTAB Dec. 14, 2015); *Diablo Technologies, Inc. v. Netlist, Inc.*, No. IPR2014-01011 (PTAB Dec. 14, 2015).

THE REJECTION OVER AMIDI, KLEIN, AND MATSUI

The Examiner finds that Amidi, Klein, and Matsui teach or suggest the limitations of the appealed claims for the reasons explained in the claim charts on pages 17 to 43 of Requester's comments filed September 5, 2014 that the Examiner incorporates by reference. Ex'r Det. 12. In those incorporated charts, Amidi is said to disclose a memory module with plural DDR memory devices arranged in one or more ranks in Figures 4A and 4B, where each DDR memory device has (1) corresponding first and second loads, and (2) a data strobe signal (DQS) line and a DQS line load for the DQS line as the corresponding second load. Sept. 2014 TPR Comments 17. Amidi is also said to disclose a circuit coupled to the DDR memory devices configured to be electrically coupled to a memory controller to receive the recited set of input signals and DDR command from the computer system. *Id.* Amidi's circuit is also said to (1) be configurable to translate the DDR command between the system memory domain and the memory module's physical memory domain to select at least one rank, and (2) disclose the recited phase-lock loop device. *Id.* at 17–18.

The Examiner, however, also relies on Klein and Matsui for teaching or suggesting that the circuit is configurable to (1) monitor the DDR command to control isolation of one or more of the DQS line loads of the DDR memory device from the computer system or from each other, and (2) be responsive to the set of input signals by selectively isolating one or more of the corresponding first loads of the DDR memory devices from the system. *Id.* According to the Examiner, to selectively reduce capacitive loading on a memory controller data bus, Klein places transfer gates 64 between the dynamic random access memories (DRAMs) and the data bus as shown in Figure 6. *Id.* (citing Klein, col. 6, ll. 7–30).

The Examiner then concludes that in view of Matsui's disclosure that using DDR synchronous DRAMs (SDRAMs) (as in Amidi) requires matching logic controls and time delays for the DQS and data signal (DQ) lines, it would have been obvious to include additional field effect transistors (FETs) for the DQS lines in Klein's transfer gates so that both DQ and DQS can be isolated from the computer system. Sept. 2014 TPR Comments 17.

The Examiner also concludes that, based on Amidi, Klein, and Matsui, it would have been obvious to (1) incorporate into Amidi's memory module 400 four sets of Klein's transfer gates (including FETs for the DQS lines per Matsui), and (2) control each set of transfer gates with a respective one of Amidi's rank chip select signals to select at least one rank among the four ranks of memory devices 404. *Id.* at 18. According to the Examiner, Amidi's rank chip select signals are used to control Klein's transfer gates in Figure 6 via an inverter decoder in Figure 7 so that the DDR command that is monitored to control DQS isolation is the same command that is translated

for memory module rank selection. *Id.* *Accord* Ex'r Det. 12 (noting this equivalence).

Patent Owner argues that the cited prior art does not teach or suggest (1) controlling DQS isolation, and (2) a memory module monitoring a DDR command to control DQS isolation. PO Revised Feb. 2017 Comments 11–14. According to Patent Owner, Matsui says nothing about controlling DQS load isolation, and Matsui's signal line values and propagation delays are physically distinct effects and concepts from DQS load/line isolation as claimed. *Id.* at 11. According to Patent Owner, Matsui's DQ and DQS connections in Figure 16 appear to be fixed and hard-wired and, therefore, not subject to any isolation control, let alone DQS isolation control as claimed. *Id.* at 12. Patent Owner adds that Matsui teaches against using a DQS signal, characterizing it as inferior to the proposed DQS signal. *Id.*

Patent Owner also contends that modifying Klein to receive Amidi's rank chip select signals from an on-module complex programmable logic device (CPLD) is inconsistent with Klein's off-module memory controller. *Id.* at 13. In addition, Patent Owner contends that the proposed rank-level arrangement of Klein's transfer gates for multiple ranks on a memory module is inconsistent with Klein's module-level transfer gates. *Id.*

Patent Owner adds that controlling isolation across multiple ranks based on on-module monitoring of a DDR command as proposed is not only not disclosed in the cited references, but this proposal is inconsistent with conventional system-level DQS management. *Id.* at 13–14. Lastly, Patent Owner contends that the cited prior art does not teach or suggest a module-level solution for DQS signal management, much less a solution to

the known, non-trivial cross-rank signal management issue—an issue that is said to be "difficult" via system-level techniques. *Id.* at 14.

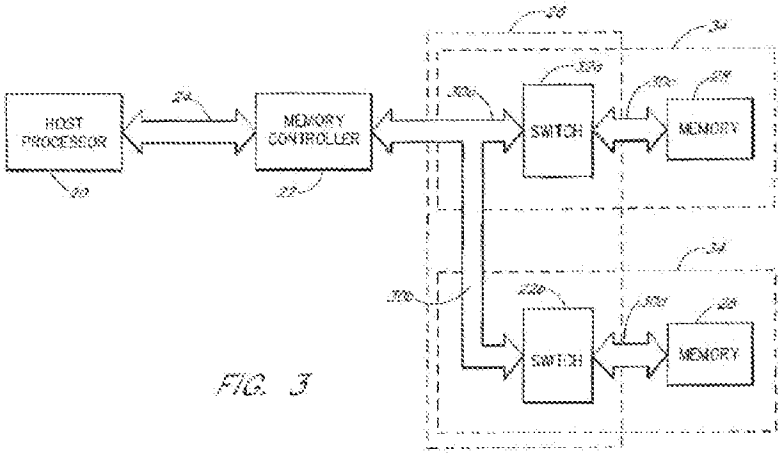
ISSUE

Under § 103, has the Examiner erred in rejecting claim 1 by finding that Amidi, Klein, and Matsui collectively would have taught or suggested a memory module circuit configurable to monitor a received DDR command to control isolation of one or more DQS line loads of plural DDR memory devices from the computer system or from each other?

ANALYSIS

We begin by noting, as does Requester, that Patent Owner does not dispute that Amidi, Klein, and Matsui collectively teach or suggest the amended claims' limitations reciting (1) a memory module or a circuit thereon configurable for monitoring and translating a DDR command for rank/device selection recited in the independent claims, and (2) relative system and physical memory domain memory densities stated in terms of (a) one-bit memory cells in independent claims 56 and 84, and (b) association with DDR chip select signals in independent claim 96. *Accord* TPR Mar. 2017 Reply 18 (noting this point). Rather, as Requester indicates (*id.* at 19), Patent Owner disputes essentially two aspects of various independent claims, namely (1) controlling DQS isolation, and (2) a memory module monitoring a DDR command to control DQS isolation. *See* PO Revised Feb. 2017 Comments 11–14.

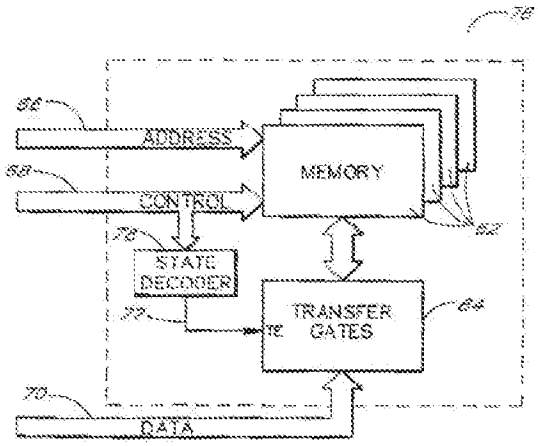
On this record, we see no error in the Examiner's rejection in this regard. In Klein, switches associated with memory elements selectively decouple memory elements from a bus when those elements are not accessed, thus reducing capacitive loading on the bus. Klein, col. 2, l. 49 – col. 3, l. 28. In the embodiment of Klein's Figure 3 for example, each branch of the data bus between memory controller 22 and memory elements 28 includes a switch 32a, 32b selectively isolating bus segments running from the memory controller to the memory circuitry. Klein, col. 4, ll. 5–27. Klein's Figure 3 is reproduced below:



Klein's switching circuit in Figure 3

Other embodiments in Klein, however, provide switches and switch control circuitry on a memory module itself, rather than on a motherboard. Klein, col. 5, ll. 40–42. As shown in Klein's Figure 6, for example, memory module 76 includes transfer gates 64 and state decoder 78. The transfer gates are a type of bus switch, such as that shown in Klein's Figure 2, that remains closed when the memory module is not accessed, but opens during memory access. *Id.*, col. 5, ll. 59–64. As shown in Klein's Figure 6, the state decoder receives control signals from the host system, and outputs gate

control signals 72 that are asserted to open the transfer gates via the "transfer enable" (TE) signal line during memory accesses. Klein, col. 2, ll. 49–51; col. 6, ll. 17–24. Klein's Figure 6 is reproduced below:



Klein's Figure 6 showing state decoder coupled to transfer gates

In the embodiment of Klein's Figure 7, the state decoder comprises an inverter 80 that (1) receives chip select signals, and (2) outputs signals to the transfer gates' TE signal line. Klein, col. 6, ll. 31–39.

In light of this functionality, we agree with the Examiner that it would have been obvious to enhance Amidi by including four sets of transfer gates, such as those shown in Klein, where each set is controlled by respective rank chip select signals in Amidi that are inverted by an inverter-based state decoder such as that shown in Klein's Figure 7. *Accord* Sept. 2014 TPR Comments 17–18. Such a switching arrangement would at least isolate the associated devices and lines in Amidi, thus reducing capacitive loading—a predictable result. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 417 (2007).

Moreover, because DQ signals require DQS signals to act as a clocking reference as Dr. Wang indicates (Redacted 2d Supp. Wang Decl. ¶ 11), providing Klein's switching arrangement for DQS signal lines in addition to their corresponding DQ signal lines in Amidi as proposed would have been at least an obvious variation. As Dr. Wang explains, DQS signals must be routed, buffered, *isolated*, or *coupled* in a manner similar to their corresponding DQ signals for a DDR SDRAM to function properly. *Id.* Therefore, isolating and coupling DQS signal lines via Klein's transfer gates in addition to their corresponding DQ signal lines would predictably reduce capacitive loading resulting from the DQS lines and their associated components. *Accord id.* ¶ 13. Patent Owner's arguments regarding Matsui's lacking DQS load/line isolation control (PO Revised Feb. 2017 Comments 11) do not show nonobviousness where, as here, the rejection is based on the cited references' collective teachings. *See In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986).

We reach this conclusion even assuming, without deciding, that the DQ and DQS connections associated with buffer 105 in Matsui's Figure 16 are fixed and hard-wired as Patent Owner contends. PO Revised Feb. 2017 Comments 12 (citing Rev. 2d Supp. Feb. 2017 Sechen Decl. ¶ 15). Although we appreciate Dr. Sechen's insights in this regard, Patent Owner's argument is not germane to the limited purpose for which Matsui was cited. That is, Matsui was cited merely to show that treating DQ and DQS signals similarly to ensure synchronization and proper operation is known in the art (*see* Matsui, col. 24, ll. 14–49), and, therefore, controlling isolation of lines

(and their associated loads) for both types of signals in the Amidi/Klein system would have been obvious. *See* Sept. 2014 TPR Comments 17–18.

Therefore, Patent Owner's arguments regarding Matsui's individual shortcomings in this regard do not show nonobviousness where, as here, the rejection is based on the cited references' collective teachings. *See Merck*, 800 F.2d at 1097. Nor does the proposed combination require physically substituting or bodily incorporating Matsui's features into the Amidi/Klein system. *See In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012) (citations omitted); *see also In re Keller*, 642 F.2d 413, 425 (CCPA 1981). Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. *Id.* On this record, we see no error in the proposed combination given the cited references' collective teachings.

Nor do we find that Matsui teaches away from using DQS signals as Patent Owner seems to suggest. *See* PO Revised Feb. 2017 Comments 12. To be sure, Matsui proposes to use a data phase signal (DPS) instead of a DQS signal for *higher-speed* transmissions. Matsui, col. 24, ll. 56–62. But we see no reason why DQS signals could not be used for *lower-speed* transmissions even assuming, without deciding, that DQS signals are inferior to, or less desirable than, DPS signals at higher speeds. That is, even if DQS is inferior at higher speeds, that alone is insufficient to teach away from the DQS alternative where, as here, the disclosure does not criticize, discredit, or otherwise discourage that alternative. *See In re Fulton*, 391 F.3d 1195, 1200–01 (Fed. Cir. 2004).

Nor are we persuaded by Patent Owner's contentions that the proposed combination is inconsistent with the cited references because,

among other things, (1) Amidi's chip select signals are from an on-module CPLD—not an off-module controller as in Klein, and (2) controlling DQS isolation across multiple ranks based on *on-module* monitoring of a DDR command is inconsistent with conventional *system-level* practices. PO Revised Feb. 2017 Comments 13–14 (citing Rev. 2d Supp. Feb. 2017 Sechen Decl. ¶¶ 20–22). But as Dr. Wang indicates, Dr. Sechen does not indicate any differences in the functionality of one chip select signal over another, let alone identify functionality differences between transfer gates. Redacted 2d Supp. Wang Decl. ¶ 16. *Accord* TPR Mar. 2017 Reply (noting this point). Moreover, Dr. Sechen's theory that because system-level management is "non-trivial," skilled artisans would expect on-module implementations to be even more difficult (Rev. 2d Supp. Feb. 2017 Sechen Decl. ¶ 22) is speculative and unsubstantiated by any persuasive evidence on this record. Although we appreciate Dr. Sechen's insights, the lack of persuasive corroborating evidence on this record pertaining to module-level versus system-level implementations reduces the probative value of Dr. Sechen's statements in this regard.

Although Dr. Sechen avers that the cited prior art does not teach or suggest a *module*-level solution for cross-rank DQS signal management—despite acknowledging a solution to that problem at the *system* level (*id.* ¶ 23)—we nonetheless see no error in the proposed combination. Indeed, Dr. Wang's own book cited by Dr. Sechen in paragraph 22 of his latest declaration teaches that a memory system should be treated holistically, and views the entire memory system broadly as encompassing a wide range of components. *See* Redacted 2d Supp. Wang Decl. ¶ 18. As Dr. Wang

explains, skilled artisans would have applied previously-known solutions that exist for one memory system subset to another, closely-related and adjacent memory system subset. *Id.* ¶ 19. Given these factors, the weight of the evidence on this record favors the Examiner's position at least to the extent that applying system-level techniques to module-level implementations would have been at least an obvious variation to those of ordinary skill in the art.

Therefore, we are not persuaded that the Examiner erred in rejecting claim 1 over Amidi, Klein, and Matsui, and claims 2–5, 7–14, 17, 18, 22, 23, 25–34, 36–43, 45, 46, 48, 51, 53–64, 66, 69, 71–79,[9] 81–88, 90, and 93–104 not argued separately with particularity.

THE OTHER REJECTIONS

Because our decision is dispositive regarding patentability of all appealed claims based on the foregoing prior art references with respect to Issue 13, we need not reach the merits of the Examiner's decision to also reject:

(1) claims 1–3, 18, 22, 25–28, 31, 36–39, 42, 43, 48, 51, 53, 56, 62, 71–73, 84, and 87 over QBMA and Dell ("Issue 3");

(2) claims 1–5, 7–14, 17, 18, 23, 25–34, 36–43, 45, 46, 48, 51, 53, 55–64, 66, 69, 71–79, 81–88, 90, 93, 94, 96, and 97 over Wong and Karabatsos ("Issue 6");

(3) claims 1–5, 8–14, 18, 22, 23, 25–34, 36–43, 45, 46, 48, 51, 53–64, 66, 69, 71–79, 81–88, 90, and 93–97 over Dell and Karabatsos ("Issue 7");

[9] We note in passing that claim 79 depends from cancelled claim 70.

(4) claims 98–104 over QBMA and Dell ("Issue 8");

(5) claims 98–104 over Karabatsos and Dell ("Issue 9");

(6) claims 98–104 over QBMA, Dell, and Kazuo ("Issue 10");

(7) claims 98–104 over Karabatsos, Dell, and Kazuo ("Issue 11"); and

(8) claims 98–104 over Wong, Karabatsos, and Kazuo ("Issue 12").

See Beloit Corp. v. Valmet Oy, 742 F.2d 1421, 1423 (Fed. Cir. 1984) (approving ITC's determination based on a single dispositive issue, and not reaching other issues not decided by the lower tribunal).

CONCLUSION

Under § 103, the Examiner did not err in rejecting 1–5, 7–14, 17, 18, 22, 23, 25–34, 36–43, 45, 46, 48, 51, 53–64, 66, 69, 71–79, 81–88, 90, and 93–104 over Amidi, Klein, and Matsui.

We do not reach the Examiner's other rejections of those claims.

DECISION

The Examiner's decision declining to reject claims 1–5, 7–14, 17, 18, 22, 23, 25–34, 36–43, 45, 46, 48, 51, 53–64, 66, 69, 71–79, 81–88, 90, and 93–104 is affirmed.

Requests for extensions of time in this *inter partes* reexamination proceeding are governed by 37 C.F.R. § 1.956. *See* 37 C.F.R. § 41.79.

In the event neither party files a request for rehearing within the time provided in 37 C.F.R. § 41.79, and this decision becomes final and appealable under 37 C.F.R. § 41.81, a party seeking judicial review must

timely serve notice on the Director of the United States Patent and Trademark Office. *See* 37 C.F.R. §§ 90.1 and 1.983.

AFFIRMED

PETITIONER:

Jamie J. Zheng
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

THIRD PARTY REQUESTER:

PILLSBURY WINTHROP SHAW PITTMAN LLP
PO Box 10500
McLean, VA 22102

ELD