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Paper 37
Entered: March 29, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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DIABLO TECHNOLOGIES INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

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Case IPR2014-01011
Patent 7,881,150 B2

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Before LINDA M. GAUDETTE, BRYAN F. MOORE, and GEORGIANNA W. BRADEN, *Administrative Patent Judges*.

GAUDETTE, *Administrative Patent Judge*.

DECISION ON REMAND
*35 U.S.C. § 144 and 37 C.F.R. § 42.5(a)*

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# I. INTRODUCTION

This Decision addresses the order of the United States Court of Appeals for the Federal Circuit in *Netlist, Inc. v. Diablo Technologies, Inc.*, 701 F. App'x 1001 (Fed. Cir. 2017) ("*Netlist*"), vacating our opinion with respect to U.S. Patent 7,881,150 B2 (Ex. 1001 ("the '150 patent")), and remanding for further proceedings. Having analyzed the entirety of the record anew in light of the court's directive in *Netlist*, we conclude that Petitioner has shown by a preponderance of the evidence that claims 15–17, 22, 24, 26, and 31–33 of the '150 patent are unpatentable.

## *A. Procedural History*

Diablo Technologies, Inc. ("Petitioner") filed a Petition (Paper 5, Corrected Petition ("Pet.")) requesting *inter partes* reviews of claims 15–17, 22, 24, 26, and 31–33 of the '150 patent. On the same day, Diablo also filed a second petition requesting *inter partes* review of the '150 patent in *Diablo Technologies, Inc. v. Netlist, Inc.*, Case IPR2014-00882 ("IPR882"), and a petition requesting *inter partes* review of U.S. Patent 8,081,536 B1 ("the '536 patent") in *Diablo Technologies, Inc. v. Netlist, Inc.*, Case IPR2014-00883 ("IPR883"). The '536 patent is a continuation of the application that issued as the '150 patent. *See* IPR883, Ex. 1001 (the '536 patent), (63).

In its Petition, Petitioner did not assert that any claim terms required express construction. *See* Pet. 8–11. Netlist, Inc. ("Patent Owner"), however, filed a Preliminary Response to the Petition wherein it proposed constructions for three claim terms, including the term "selectively electrically coupling," recited in challenged independent claims 15 and 31. Paper 9 ("Prelim. Resp."), 13–19.

In our Institution Decision, we agreed that express construction of the term "selectively electrically coupling" was necessary, but determined Patent Owner had not proposed the broadest reasonable construction of this term. *See* Paper 12 ("Inst. Dec."), 9–11. Accordingly, we applied our own construction of "selectively electrically coupling" in instituting an *inter partes* review of '150 patent claims 15–17, 22, 24, 26, and 31–33. *See generally id.* at 13–29.

Patent Owner subsequently filed a Patent Owner Response (Paper 26 ("PO Resp.")), and Petitioner filed a Reply (Paper 28). In its arguments in support of patentability, Patent Owner implicitly construed "selectively isolating" as "isolating in response to a selection." *See* PO Resp. 50 ("The Petition does not explain how its alleged 'selectively isolate' is in response to a selection."). The term "selectively isolating" is recited in challenged independent claim 24 and the term "selectively isolate" is recited in challenged dependent claim 26.[1]

An oral hearing, consolidated with IPR882 and IPR883, was held on July 28, 2015. Paper 32 (Record of Oral Hearing).

On December 14, 2015, this Board issued a Final Written Decision in the present *inter partes* review, wherein we modified our prior construction of "selectively electrically coupling" and also construed the term "selectively isolating"; we declined to adopt the constructions of these terms applied by Patent Owner. *See* Paper 34 ("Final Decision" or "Final Dec."),

[1] For convenience, our discussion below refers to the term "selectively isolating." However, our findings and conclusions also apply to the term "selectively isolate."

11–13. In our Final Decision, we held all challenged claims of the '150 patent unpatentable as follows:

| References | Basis | Claims Challenged | Claims Held Unpatentable |
|---|---|---|---|
| Ludwig[2] & Amidi[3] | § 103 | 15–17, 22, 24, 26, and 31–33 | 15–17, 22, 24, 26, and 31–33 |
| Amidi | § 102(e) | 22, 24, and 26 | 22 and 26 |

Final Dec. 45. We likewise applied these constructions of the terms "selectively electrically coupling" and "selectively isolating" in holding unpatentable all challenged claims of the '150 patent in IPR882, and applied our own construction of the '536 patent claim term "selectively isolating" in holding unpatentable all challenged '536 patent claims in IPR883. IPR882, Paper 33; IPR883, Paper 33.

Patent Owner filed a Notice of Appeal to the United States Court of Appeals for the Federal Circuit requesting review of our unpatentability determinations. Paper 35. The Federal Circuit consolidated the appeal from our decision in the present *inter partes* review with Patent Owner's concurrently-filed appeals from our decisions in related cases IPR882 and IPR883. *Netlist*, 701 F. App'x at 1002.

On July 25, 2017, the Federal Circuit issued a decision determining that we erred in our construction of the '150 patent claim term "selectively electrically coupling." *Id.* at 1005. The court further determined that because the construction of "selectively isolating" applied in our analysis of the challenges to the '150 patent claims was based on an erroneous

[2] U.S. Patent 5,581,498 (Ex. 1011).
[3] U.S. Patent Publication 2006/0117152 A1 (Ex. 1008).

construction of "selectively electrically coupling," we likewise erred in the construction of "selectively isolating" applied in this *inter partes* review as well as in IPR882. *Id.* (noting that "[t]he specification uses the terms 'coupling' and 'isolating' in a similar fashion"). The court observed that we had construed the term "selectively isolating" differently in IPR883, but found the record was unclear as to which construction of "selectively isolating" we actually had applied in our analysis of the challenges to the '536 patent. *Id.* at 1005–06. The court directed us on remand to construe "selectively isolating" in view of its construction of "selectively electrically coupling," and to reconsider whether the references disclose circuits that are capable of selectively isolating based on our new construction. *See id.* at 1005.

The court's mandate issued on August 31, 2017. Neither party sought to provide additional briefing or requested that we take new evidence upon remand. Here, we determine that no new argument or evidence is necessary because the claim constructions we apply on remand were proposed by Patent Owner (*compare* PO Resp. 12, 50, *with* Section II *infra*) and "the effect thereof has been fully briefed" (Patent Trial and Appeal Board Standard Operating Procedure ("SOP") 9[4] (Rev. 1), 8). *See Netlist*, 701 F. App'x at 1005 ("Indeed, the parties below raised factual disputes about

[4] SOP 9 addresses the procedure for handling all decisions on cases remanded from the Court of Appeals for the Federal Circuit to the Patent Trial and Appeal Board for further proceedings. SOP 9 currently is available at https://www.uspto.gov/sites/default/files/documents/sop_9_%20procedure_for_decisions_remanded_from_the_federal_circuit.pdf.

whether prior art circuits perform selective electrical coupling, even under Netlist's construction. But because the Board based its conclusions of obviousness and anticipation on an erroneous construction, the Board must assess these factual issues on remand."). We address the errors identified by the Federal Circuit in view of the record as of December 14, 2015, the date of issuance of the Board's Final Decision. For the reasons that follow, we conclude that Petitioner has shown by a preponderance of the evidence that claims 15–17, 22, 24, 26, and 31–33 of the '150 patent are unpatentable.

*B. The '150 Patent*

The '150 patent is described in the Final Written Decision. *See* Final Dec. 3–6. A summary description is provided below.

The '150 patent relates to a memory module of a computer system with improved performance and memory capacity. Ex. 1001, 1:30–33. The memory module includes a plurality of memory devices (arranged in ranks), and a circuit electrically coupled to the memory devices. *Id.* at 4:59–63, Fig. 1. The circuit includes a logic element, such as a complex programmable-logic device (CPLD). *Id.* at 6:4–9. In response to a set of input address and command signals from a memory controller, the circuit generates a set of output address and command signals (*id.* at 15:23–31), whereby the circuit selectively isolates the loads of some of the memory devices from the computer system (*id.* at 6:48–50).

Figure 3A, reproduced below, is a schematic diagram of a circuit in accordance with certain embodiments of the invention. *Id.* at 4:14–18.

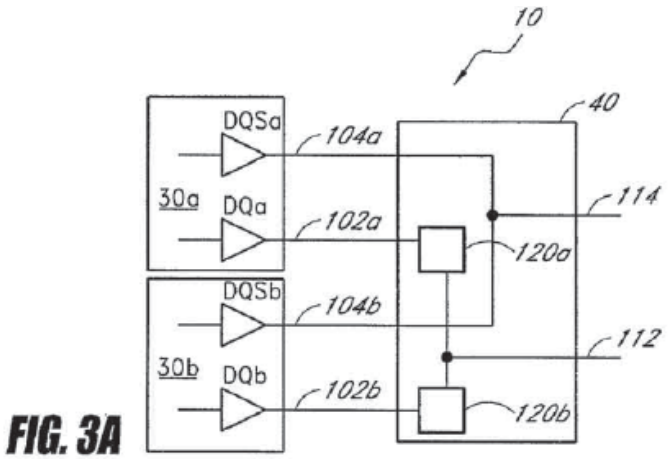



FIG. 3A

As shown in Figure 3A, the logic element of circuit 40 uses switches 120a, 120b to selectively isolate or selectively electrically couple one or both of DQ data signal lines 102a, 102b of memory devices 30a and 30b from common data signal line 112. *Id.* at 3:45–47, 7:2–5, 19–26. By selectively isolating the loads of memory devices that are not being accessed by the memory controller, the capacitive load on the memory controller can be substantially reduced. *Id.* at 7:27–31.

## II. CLAIM CONSTRUCTION

"A claim in an unexpired patent that will not expire before a final written decision is issued shall be given its broadest reasonable construction in light of the specification of the patent in which it appears." 37 C.F.R. § 42.100(b). Pursuant to that standard, the claim language should be read in light of the specification, as it would be interpreted by one of ordinary skill in the art. *In re Suitco Surface, Inc.*, 603 F.3d 1255, 1260 (Fed. Cir. 2010). An inventor may provide a meaning for a term that is different from its ordinary meaning by defining the term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480

(Fed. Cir. 1994). "[W]here multiple patents 'derive from the same parent application and share many common terms, we must interpret the claims consistently across all asserted patents.'" *SightSound Tech., LLC v. Apple Inc.*, 809 F.3d 1307, 1316 (Fed. Cir. 2015) (quoting *NTP, Inc. v. Research in Motion, Ltd.*, 418 F.3d 1282, 1293 (Fed. Cir. 2005)).

In our Final Decision, we construed the terms "selectively electrically coupling," "selectively isolating," and "circuit configured to be mounted on a memory module." *See* Final Dec. 8–15. The Federal Circuit agreed with our construction of "circuit configured to be mounted on a memory module," but determined we erred in our constructions of "selectively electrically coupling" and "selectively isolating." *See Netlist*, 701 F. App'x at 1004–05.

"Selectively electrically coupling" is recited in each of challenged independent claims 15 and 31 as follows:

> A circuit configured to be mounted on a memory module so as to be electrically coupled to a first double-data-rate (DDR) memory device having a first data signal line and a first data strobe line, to a second DDR memory device having a second data signal line and a second data strobe line, and to a common data signal line . . . wherein the circuit is configurable to be responsive to the set of input signals [comprising row address signals, column address signals, bank address signals and chip-select signals] by *selectively electrically coupling* the first data signal line to the common data signal line and *selectively electrically coupling* the second data signal line to the common data signal line.

Ex. 1001, 42:41–46, 48–50, 58–62, 44:29–34, 36–38, 46–50 (emphasis added). The Federal Circuit determined the broadest reasonable construction of this term is "coupling in response to a selection." *Netlist*,



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701 F. App'x at 1004. As instructed by the court, below we construe the term "selectively isolating" in view of the court's construction of "selectively electrically coupling." *See id.* at 1005–06.

"Selectively isolating" is recited in challenged '150 patent claims 22 and 26 as follows:

> 22. A circuit configured to be mounted on a memory module so as to be electrically coupled to a plurality of [DDR] memory devices arranged in one or more ranks on the memory module . . . wherein the circuit is configurable to be responsive to the set of input signals [comprising row address signals, column address signals, bank address signals and chip-select signals] by *selectively isolating* one or more loads of the DDR memory devices from the computer system.

Ex. 1001, 43:35–38, 40–42, 51–54 (emphasis added).

> 26. The circuit of claim 22, further configurable to *selectively isolate a data signal line* of a DDR memory device of the plurality of DDR memory devices from the computer system.

*Id.* at 44:8–11 (emphasis added).

As noted above, Petitioner did not propose an explicit construction of "selectively isolating." *See* Pet. 8–11. In its Patent Owner Response, Patent Owner implicitly construed the term "selectively isolating" as "isolating in response to a selection." *See* PO Resp. 50. As also indicated above, the '536 patent is a continuation of the application that issued as the '150 patent and, therefore, the two patents share the same written description. *See Netlist*, 701 F. App'x at 1003. In IPR883, involving the related '536 patent and claims reciting the term "selectively isolating," Patent Owner explicitly proposed construing this term as "isolating in response to a selection." IPR883, Paper 8, 14–15. In support of this construction, Patent Owner cited



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disclosure in the '536 patent that corresponds to column 6, line 63 through column 8, line 20 of the '150 patent. *See* IPR883, Paper 8, 14–15; *compare* Ex. 1001, 6:63–8:20, *with* IPR883, Ex. 1001, 7:32–8:56. The referenced disclosure describes, with reference to Figures 3A, 3B, that by selectively isolating DQ data signal line 102a of memory device 30a from common DQ data signal line 112, which is coupled to the computer system, circuit 40 "selectively allows" (1) a DQ data signal to be transmitted from the memory controller of the computer system to DQ data signal line 102b of memory device 30b, and (2) a DQ data signal from DQ data signal line 102b of memory device 30b to be transmitted to the memory controller via common DQ data signal line 112 (*see* Ex. 1001, 6:63–7:12). The '150 patent explains that by selectively isolating DQ data signal line 102a and DQS data strobe signal line 104a of memory device 30a (i.e., the memory device that is not being accessed by the computer system) from the common data signal and data strobe signal lines 112, 114 to the memory controller, the load from memory device 30a is isolated from the memory controller, thereby reducing the capacitive load on the memory controller. *Id.* at 6:40–47, 58–62. The '150 patent describes DQ data signal line 102b (i.e., the data signal line to the memory device that is being accessed by the computer system), as "selectively electrically couple[d]" to common DQ signal line 112. *See id.* at 7:19–33.

In construing the claim term "selectively electrically coupling," the Federal Circuit determined that this term "is directed to *how* the circuit performs th[e] function [of activating some memory devices and not others], which is by coupling or decoupling specific data signal lines." *Netlist*, 701 F. App'x at 1005. Noting that "the claims call out exactly which two data



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lines must be coupled," the court determined that our construction of "selectively electrically coupling" as "making a selection between at least two components so as to transfer power or signal information from one selected component to at least the other selected component," was unreasonable. *Id.* at 1004–05. The court explained that "the 'selection' is to couple or uncouple the first/second data signal line to the common signal line, not to select among multiple components." *Id.* at 1005.

The above cited disclosure in the '150 patent similarly is directed to how the circuit performs the function of reducing the load to the computer system, which is by isolating the load of specific memory devices from the memory controller, and to how the circuit performs the function of preventing data transmission between a specific memory device and the computer system, which is by isolating specific data signal lines from the common signal line.

Patent Owner, in its arguments in support of patentability in the Patent Owner Response, asserts that the term "selectively isolating" requires electrical separation. PO Resp. 23. Patent Owner's expert, Dr. Carl Sechen, testified that in a system in which the chip select signal lines and the data bus lines are permanently hard-wired via an electrical conduit to the memory devices, load isolation is not possible without switches on these lines to enable electrical decoupling. Ex. 2002 (Declaration of Dr. Carl Sechen) ¶ 78; *see also* Ex. 1027 (Transcript of Dr. Carl Sechen's deposition), 133:6–14.

We are not persuaded that the broadest reasonable construction of "selectively isolating" requires electrical separation. The '150 patent discloses that:



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> As used herein, the term "load" is a broad term which includes, without limitation, electrical load, such as capacitive load, inductive load, or impedance load. As used herein, *the term "isolation" is a broad term which includes, without limitation, electrical separation* of one or more components from another component or from one another.

Ex. 1001, 5:3–8 (emphasis added). Patent Owner has not identified, nor do we find, any disclosure in the '150 patent that supports a broadest reasonable construction of the claim term "selectively isolating" as requiring electrical separation. To the contrary, use of the term "electrically" throughout the '150 patent to specify how the data signal lines are selectively coupled, suggests that the inventors did not intend to limit how the data signal lines are selectively isolated or the type of loads that are selectively isolated. *See, e.g.*, Ex. 1001, 8:48–52 ("In certain embodiments, the load isolation provided by the circuit 40 advantageously allows the memory module 10 to present a reduced load (*e.g.*, *electrical load*, such as capacitive load, inductive load, or impedance load) to the computer system." (emphasis added)); *id.* at 9:9–12 ("In certain embodiments, load isolation advantageously provides system memory with reduced electrical loading."); *cf.* Ex. 2002 ¶¶ 65–66 ("[T]he claim term 'selectively electrically coupling' is more specific than just a generic 'coupling.'. . . [T]he added word 'electrically' specifies an electrical aspect to 'coupling' to [one of ordinary skill in the art].") Because we are not persuaded that the claim term "selectively isolating" requires electrical separation, we also decline to construe this term as requiring a switch or other specific component that would enable electrical decoupling. *See Netlist*, 701 F. App'x at 1005 ("To be clear, we do not limit 'selectively electrically coupling' to a switch or



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other specific component. Nor do we hold that 'selectively electrically coupling' necessarily precludes a hard-wired connection.").

Accordingly, consistent with the Federal Circuit's determination that the broadest reasonable construction of "selectively electrically coupling" is "coupling in response to a selection," *id.* at 1004, we determine the broadest reasonable construction of the claim term "selectively isolating" is "isolating in response to a selection."[5]

## III. ANALYSIS

To prevail in its patentability challenges, a petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). In its decision, the Federal Circuit found that we applied erroneous constructions of "selectively electrically coupling" and "selectively isolating" in determining Petitioner had met its burden to prove unpatentability. *See Netlist*, 701 F. App'x at 1004–05. Following the court's directive in its construction of the claim term "selectively electrically coupling" as "coupling in response to a selection," in this decision we construe "selectively isolating" as "isolating in response to a selection." *See* Section II *supra*. As instructed by the court, we apply these constructions in reconsidering whether Petitioner has met its burden to show that (1) Amidi discloses "selectively isolating," and (2) the combination of Ludwig and Amidi discloses "selectively isolating" and "selectively electrically coupling." *See Netlist*, 701 F. App'x at 1005–06. The court did not identify any other error in our findings and, therefore, we

[5] We apply the same construction of this term in our decisions on remand in IPR882 and IPR883.



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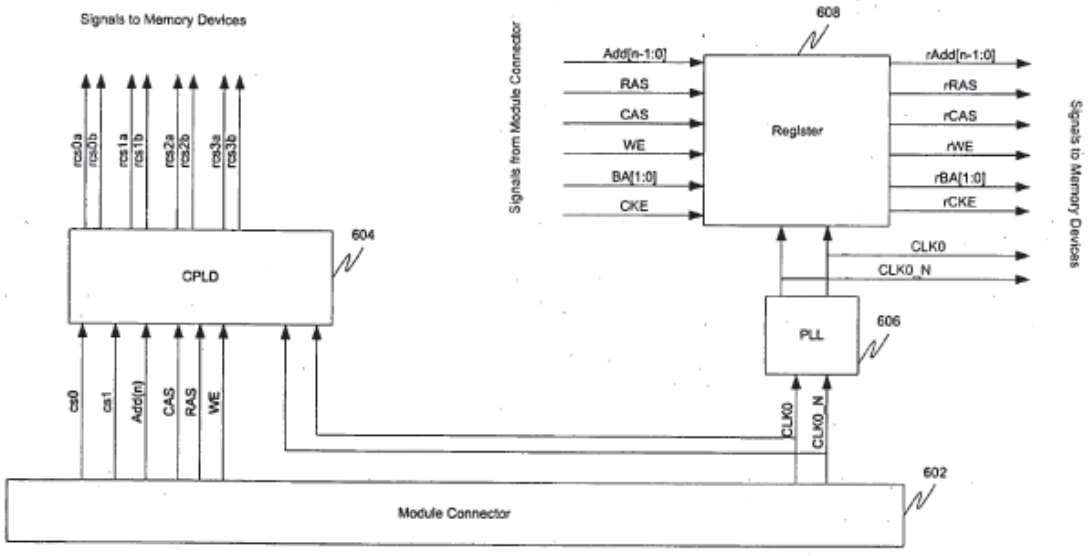
do not revisit our determinations that: Amidi discloses all other limitations of claims 22 and 26; the combination of Ludwig and Amidi discloses or suggests all other limitations of challenged claims 15–17, 22, 24, 26, and 31–33; and that one of ordinary skill in the art would have had a reason to combine Ludwig and Amidi, and a reasonable expectation of success in so doing. *See generally*, Final Dec. 19–45.

*A. The Prior Art*

The prior art is described in the Final Decision. *See* Final Dec. 20–25. Below we provide summary descriptions.

*1. Amidi (Ex. 1008)*

Amidi discloses a transparent four rank memory module for use in a standard two rank sub-system. Ex. 1008, Title. As illustrated in Figure 6A, reproduced below, Amidi's memory module includes complex programmable logic device ("CPLD") 604, phase-lock loop ("PLL") 606, and register 608. *Id.* ¶¶ 28, 50.




Row Address Decoding
FIG.6A



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Figure 6A is a block diagram schematically illustrating a row address decoding system for a transparent four rank memory module in accordance with an embodiment of Amidi's invention. *Id.* ¶ 21. Module connector 602 sends signals from a memory controller (not shown) to CPLD 604, PLL 606, and register 608. *Id.* ¶¶ 38, 50. The signals sent to CPLD 604 include chip select, row address, and column address signals. *Id.* ¶¶ 41, 50. CPLD 604 includes internal decoding circuitry for determining which rank from the four ranks of memory devices to activate based upon the address and command signals from the memory controller. *See id.* ¶¶ 41, 43, 57, 61. CPLD 604 generates and relays the command signals to activate a rank of memory devices. *Id.* ¶ 62.

*2. Ludwig (Ex. 1011)*

Ludwig is directed

> to increas[ing] density of electronic components available for electronic host systems, by providing a stack of chips which: (a) fits into the same space as that required by a single chip; and (b) mimics a single chip in such a way that the host system "sees" the stack as if it were a single chip.

Ex. 1011, 1:43–48. Ludwig incorporates an interface ("VIC") chip into a stack of IC chips to form a "VIC stack." *Id.* at 2:6–9. The VIC chip "contains all the IC circuitry required to interface the stack with the host system." *Id.* at 1:55–57. Operation of a VIC chip is described in connection with Ludwig Figure 11, reproduced below.



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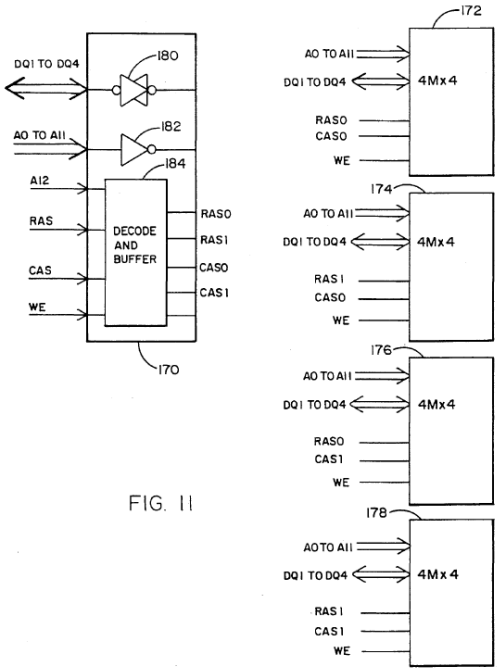



FIG. 11

Figure 11 is a diagram of a 64 MEG DRAM package having VIC chip 170 that includes decode and buffer circuitry 184, and four stacked 16 MEG DRAM IC chips 172, 174, 176, and 178. *Id.* at 9:35–36. "Data lines DQ1-DQ4, after passing through tri-state buffers 180, are connected to each of the four IC chips. Address lines A0-A11 also are connected to each of the four IC chips, after passing through buffers 182." *Id.* at 9:38–41. The decode circuitry uses address lines and a chip enable ("CE") signal to select which of the four IC chips is enabled. *Id.* at 7:17–19.

*B. Alleged Anticipation of Claims 22, 24, and 26 by Amidi*

Independent claim 22 recites: "wherein the circuit is configurable to be responsive to the set of input signals [comprising row address signals, column address signals, bank address signals and chip-select signals] by *selectively isolating one or more loads* of the DDR memory devices from the computer system." Ex. 1001, 43:40–42, 51–54 (emphasis added). Claim 26 recites: "The circuit of claim 22, further configurable to *selectively*

*isolate a data signal line* of a DDR memory device of the plurality of DDR memory devices from the computer system." *Id.* at 44:8–11 (emphasis added). Petitioner relies on the declaration testimony of Srinivasan Jagannathan, Ph.D. in support of its contention that Amidi discloses these claim limitations. *See* Pet. 20; Ex. 1007 (Declaration of Dr. Srinivasan Jagannathan); *see also* Ex. 1028 (Supplemental Declaration of Dr. Srinivasan Jagannathan).

*1. Claim 22 – "wherein the circuit is configurable to be responsive to the set of input signals by selectively isolating one or more loads of the DDR memory devices from the computer system"*

Petitioner contends Amidi discloses a circuit comprising a logic element (CPLD), a phase-lock loop device (PLL), and a register. Pet. 22 (citing Ex. 1008 ¶¶ 37, 50). Petitioner asserts that Amidi discloses a memory module having one or more ranks of DDR memory devices that are electrically coupled to the components of the circuit. *Id.* at 23–24 (citing Ex. 1008 ¶¶ 37, 42, Figs. 4A, 4B, 6A). Petitioner asserts that each stack of DDR memory devices has a data signal line and a data strobe line, and "at least two DDR memory devices are connected to the same (common) memory bus ('common data signal line')." *Id.* at 26 (citing Ex. 1008 ¶¶ 32, 34, 35, Fig. 3). Petitioner contends Amidi's circuit is responsive to input signals, including row address, column address, bank address, and chip-select signals. *See id.* at 27 (citing Ex. 1008 ¶ 50, Fig. 6A). In particular, Petitioner asserts that in response to chip select signals cs0, cs1 and address signal Add(n) from a memory controller, Amidi's CPLD generates signals to activate a selected one of four ranks of memory devices, while inactivating the other three ranks from the data bus, thereby enabling the activated rank



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to read from or write data to the system bus. *Id.* at 31–32 (citing Ex. 1008 ¶¶ 43, 44, 62).

Petitioner notes Amidi discloses that the register, which receives input address and bank address signals "may eliminate the loading of 36 devices in case of stacking or loading of 18 devices in case of monolithic memory devices from the main controller by separating the controller side signaling with memory side signal loading fan-out." *Id.* at 33 (quoting Ex. 1008 ¶ 38). Petitioner thus contends "Amidi discloses that the circuit, including the CPLD, PLL and register, is 'responsive to the set of input signals by selectively isolating one or more loads of the DDR memory devices from the computer system.'" *Id.* (quoting Ex. 1001, 43:51–54 (claim 22)).

Dr. Jagannathan testified that Amidi teaches the CPLD generates a chip select signal that enables a rank of memory devices. Ex. 1007 ¶ 72 (citing Ex. 1008 ¶¶ 43–44). Dr. Jagannathan testified that one of ordinary skill in the art would understand that the enabled rank, referred to in Amidi as the "active" rank, is then able to read from or write data to the system bus, while the data pins of the memory devices of the inactive ranks would be disconnected from the common bus (i.e., in a high-impedance state). *Id.* (citing Ex. 1008 ¶ 43); *see also id.* ¶ 42 ("A person of ordinary skill would understand that a high-impedance state on the DQ pins means that the chip is essentially not driving these pins."); Ex. 1028 ¶ 28 ("[W]hen the data is transmitted . . . , the data pins of the inactive ranks are in a high impedance state. This is a requirement of the JEDEC standards. (See JEDEC79C (Ex. 101[7]), pp. 7, 22, 31.)"[6]). Dr. Jagannathan's testimony is supported by the

[6] In our Final Decision, we found that "a person of ordinary skill in the art at

cited disclosure in JEDEC79C. *See* Ex. 1017, 7 ("[D]uring power-up . . . the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access)."), 22 ("Upon completion of a [READ] burst, assuming no other commands have been initiated, the DQs will go High-Z."), 31 ("Upon completion of a [WRITE] burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored."). Moreover, neither Patent Owner nor Dr. Sechen disputes that the data pins of the inactive ranks remain in a high-impedance state during a read or write transaction. *See, e.g.*, PO Resp. 46–50 (addressing Petitioner's challenge to claims 22, 24, and 26); Ex. 2002 ¶ 80 (wherein Dr. Sechen addresses the testimony in paragraph 72 of Dr. Jagannathan's declaration (Ex. 1007)). According to Dr. Jagannathan, "[o]ne of ordinary skill would understand that when the data pins are in high impedance state, a load . . . associated with the data pins of these memory devices are isolated from the computer system." Ex. 1007 ¶ 72.

Patent Owner argues that "choosing a rank of memory devices and inactivating other ranks is not selectively isolating a load of DDR memory

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the time of the '150 patent would have . . . familiarity with computer memory systems and related industry standards such as JEDEC standards for DRAM memories and memory modules." Final Dec. 17. Dr. Jagannathan testified that "DRAM memory modules used in personal computer applications typically conform[] to [JEDEC] standards." Ex. 1007 ¶ 27. Dr. Sechen does not disagree with this testimony. *See, e.g.*, Ex. 2002 ¶ 18 ("[M]emory modules must be designed to properly interface with a memory controller and remain compliant with relevant JEDEC standards for proper operational performance and interoperability."). JEDEC79C provides a standard for DDR SDRAM memory devices. Ex. 1017, i.



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circuits, because neither involves electrical separation from the computer system." PO Resp. 47 (citing Ex. 1001, 5:5–8). Patent Owner's argument is supported by Dr. Sechen's testimony that a person of ordinary skill in the art would understand that

> [a]t a memory device of Amidi, . . . there would be data pins hard-wired via an electrical conduit to the respective lines of Amidi's 72-line data bus. (Ex. 1021, JEDEC21C 4-20-4, p. 4.20.4-44.) Each data pin contributes its electrical load to its respective line of Amidi's 72-line data bus. Due to the permanent hard-wiring via an electrical conduit of the memory device's data pin to its line of Amidi's 72-line data bus, its electrical load is always electrically connected, not separated nor isolated, regardless of any rank selection or de-selection in Amidi. Accordingly, these signal lines of Amidi would always be electrically coupled to the memory devices and never subject to acts of selective electrically coupling. Similarly, already connected and never separated, these signal lines of Amidi are never subject to an act of selectively isolating.

Ex. 2002 ¶ 79.

Patent Owner also argues that Petitioner fails to identify description in Amidi of a circuit distinct from the DDR memory circuit that is configured to "selectively isolate," as required by claim 22, and that Petitioner does not explain how the "alleged 'selectively isolate' is in response to a selection" or "identify any address signal or chip-select signal for the alleged 'selectively isolate.'" PO Resp. 50.

Having considered the parties' respective arguments and evidence cited in support thereof, we are persuaded that Amidi discloses a "circuit . . . configurable to be responsive to the set of input signals by selectively isolating one or more loads of the DDR memory devices from the computer system" as recited in claim 22. As explained in our Final Decision (Final



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Dec. 43–44), we are satisfied that Petitioner has identified a circuit (comprising a CPLD, a PLL and a register), separate from the DDR memory circuit, that responds to address and chip select signals from a memory controller by generating a signal to activate the selected rank(s) of memory devices thereby enabling those ranks to read and write data to the system bus (Pet. 22 (citing Ex. 1008 ¶¶ 37, 50), 27 (citing Ex. 1008 ¶ 50, Fig. 6A), 31–32 (citing Ex. 1008 ¶¶ 43, 44, 62); *see also* Ex. 1007 ¶¶ 72–74 (wherein Dr. Jagannathan explains how the CPLD, PLL, and register are configurable to isolate the loads of the memory devices from the computer system)).

We decline to give weight to Dr. Sechen's testimony that because the signal lines of Amidi are hard-wired, they are never subject to an act of selectively isolating (*see* Ex. 2002 ¶ 79), as this testimony is based on an erroneous interpretation of "selectively isolating" as requiring electrical separation. As discussed in Section II, above, we do not construe "selectively isolating" as requiring *electrical* separation or as requiring a switch or other specific component that would enable electrical decoupling. Likewise, the '150 patent does not support interpreting the claim term "load" as limited to electrical loads. *See* Section II *supra*. We find Dr. Jagannathan applies the broadest reasonable constructions of "selectively isolating" (i.e., "isolating in response to a selection") and "load" (i.e., a broad term that is not limited to an electrical load) in his analysis of Amidi, and we credit his testimony that one of ordinary skill in the art would have understood that *in response to the selection* of a rank of memory devices to drive or receive data signals, the data bus pins on the memory devices of the inactive ranks would be in a high impedance state such that the associated *data loads* of the inactive ranks *are* thereby *isolated* from the computer system. *See* Ex. 1007



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¶ 72. We note that Dr. Sechen agrees with Dr. Jagannathan that the ranks of memory devices that are not activated "do not drive (or receive) data signals onto (or from) the data bus (*i.e.*, data lines)." Ex. 2002 ¶ 77; *see* Ex. 1007 ¶ 72.

In sum, we are satisfied that Amidi discloses "selectively isolating" under our construction of this term as "isolating in response to a selection."

*2. Claim 26 – further configurable to selectively isolate a data signal line of a DDR memory device of the plurality of DDR memory devices from the computer system.*

Petitioner contends a person of ordinary skill in the art would recognize that selectively isolating the loads of the memory devices necessarily would require isolating the data signal lines of the memory devices from the computer system. Pet. 39–40 (citing Ex. 1007 ¶ 72). Patent Owner does not advance any additional arguments or evidence in support of patentability of claim 26.

We find Dr. Jagannathan's uncontroverted testimony supports Petitioner's contention. *See* Ex. 1007 ¶ 72. We credit that testimony and determine Petitioner has met its burden to show that Amidi discloses a circuit that is "further configurable to selectively isolate a data signal line of a DDR memory device of the plurality of DDR memory devices from the computer system" as recited in claim 26.

*3. Claim 24*

In our Final Decision, we determined Petitioner did not carry its burden to demonstrate, by a preponderance of the evidence, that Amidi anticipates claim 24. Final Dec. 44. This determination was not based on our constructions of "selectively isolating" and/or "selectively electrically

coupling. Accordingly, we do not reconsider our finding that Petitioner has not shown claim 24 to be unpatentable as anticipated by Amidi.

### *C. Alleged Obviousness of Claims 15–17, 22, 24, 26, and 31–33 in view of Amidi and Ludwig*

Claims 22 and 26 recite "selectively isolating," as discussed in Section III.B, above. Independent claims 15 and 31 recite:

> wherein the circuit is configurable to be responsive to the set of input signals [comprising row address signals, column address signals, bank address signals and chip-select signals] by *selectively electrically coupling* the first data signal line to the common data signal line and *selectively electrically coupling* the second data signal line to the common data signal line.

Ex. 1001, 42:48–50, 58–62, 44:36–38, 46–50 (emphasis added).

Petitioner's contentions with respect to Amidi are discussed in Section III.B, above. Petitioner contends Ludwig discloses a memory module comprising "four stacked 16 MEG DRAM IC chips 172, 174, 176 and 178 ('first DDR memory device' and 'second DDR memory device')[,] . . . each having read and write lines DQ1-DQ4 ('first data signal line' and 'second data signal lines') . . . ." Pet. 24 (citing Ex. 1011, Fig. 11); *id.* at 23 (citing Ex. 1011, 2:1–6). Petitioner contends Ludwig discloses a circuit (VIC chip) on the memory module (*id.* at 21 (citing Ex. 1011, 2:1–9)) that is electrically coupled between the memory stack and memory controller (*id.* at 26 (citing Ex. 1011, 5:8–11)). Petitioner contends the VIC chip receives input signals, including row and column address signals, and chip enable signals (*id.* at 27 (citing Ex. 1011, 8:44–48, 6:17–20)), and determines which of the 4 IC chips in the stack will be enabled (*id.* at 31 (citing Ex. 1011, 9:43–60)). Petitioner contends one of ordinary skill in the art would have recognized that the input signals received by Amidi's CPLD, including row address

signals, column address signals, bank address signals, and chip-select signals, could be received by Ludwig's decoder 64 for larger memories that are not organized as monolithic arrays. *Id.* at 27–28 (citing Ex. 1007 ¶¶ 117, 119). Petitioner asserts that decode and buffer circuitry 184, which is part of the VIC chip, "selectively couples the first data signal line of the first DRAM IC chip 172 to data lines DQ1 to DQ4 ('common data signal line') . . . [, and] also couples second data signal lines of the second DRAM IC chip 174 to the DQ1 to DQ4 ('common data signal line')." *Id.* at 31 (citing Ex. 1011, Fig. 11, 9:43–60; Ex. 1007 ¶ 112). Petitioner further contends Ludwig "discloses that the tri-state buffers in the VIC chip isolate the loads of one [or] more memory devices that are not enabled." *Id.* at 32 (citing Ex. 1011, 7:16–19). In other words, Petitioner proposes controlling Amidi's memory module with Ludwig's VIC chip. *See* Prelim. Resp. 41; Ex. 2002 ¶ 85.

Patent Owner argues that "selectively electrically coupling" (claims 15 and 31) "implies a decoupled state of those 'signal lines' from which 'selectively electrically coupling' is performed." PO Resp. 31. Patent Owner contends Amidi's data lines are never in a decoupled state that would allow them to be subject to acts of "selectively electrically coupling," because the data lines of its four ranks are hard-wired in permanent coupling to the same 72-line data bus. *Id.* Dr. Sechen acknowledged, however, that adding switches on Amidi's chip select signal lines or data bus lines would enable decoupling of the data bus lines from the memory controller to the memory devices. *See* Ex. 2002 ¶ 80 (Amidi's "data bus remains electrically coupled to all of the memory devices, including to all of the inactive ranks, for there are indeed no switches to facilitate any type of decoupling or isolating.").



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We credit Dr. Jagannathan's undisputed testimony that Ludwig's tri-state buffers are structural elements "(switches)" that are capable of electrically coupling/decoupling memory device data signal lines to/from a common data signal line, and are capable of isolating the load of one or more non-enabled memory devices from the system bus. Ex. 1007 ¶¶ 112, 114; *see* PO Resp. 32–33; Ex. 1027, 214:2–17 (wherein Dr. Sechen testified that he "never offered opinions on . . . whether a tristate buffer met the requirements of selectively electrically coupling."). Because it is supported by the cited disclosure in Ludwig, we also credit Dr. Jagannathan's testimony that "Ludwig teaches that the VIC [chip] contains logic to selectively couple the data and control lines of a single memory device from the stack to the data and control bus connected to the computer system" (Ex. 1007 ¶ 103 (citing, e.g., Ex. 1011, 7:43–61, 9:31–40, Fig. 11)) in response to an input signal from the host system selecting a memory device to enable (*id.* ¶ 111 (citing, e.g., Ex. 1011, 9:31–60)).

> [W]e credit the testimony of Dr. Jagannathan that a person of ordinary skill in the art would have had reason to combine the teachings of Ludwig and Amidi, which both relate to memory modules, and are directed to solving the same problem of using additional memory devices in a memory module to increase the overall memory density of the module without hindering the ability of the module to interface with a pre-existing memory controller.

Final Dec. 36 (citing Ex. 1007 ¶ 116); *see also* Ex. 1007 ¶ 118 (wherein Dr. Jagannathan testified that one of ordinary skill in the art would have recognized the benefits of applying "the circuit including a CPLD, a PLL, and a register in Amidi to the interface chip in Ludwig. . . . For example, Ludwig teaches 'a valuable added function [of the VIC chip] might be



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synchronized memory signals to enhance the speed of the memory function'" (quoting Ex. 1011, 10:11–13)).

In sum, we are satisfied that the combination of Ludwig and Amidi discloses "selectively electrically coupling" under the Federal Circuit's construction of this term as "coupling in response to a selection." We are also satisfied that this combination discloses "selectively isolating" under our construction of this term as "isolating in response to a selection" for the reasons discussed in Section III.B. Moreover, even if we were to construe "selectively isolating" as requiring electrical separation, as proposed by Patent Owner (PO Resp. 47), we credit Dr. Jagannathan's testimony that the combination of Ludwig and Amidi discloses this feature, because Dr. Jagannathan's testimony is supported by the cited disclosure in Ludwig (Ex. 1007 ¶ 105 (citing, e.g., Ex. 1011, 7:43–61, 9:31–40, Fig. 11)). Dr. Jagannathan explains that Ludwig's chip-select signals, "when true, would electrically couple a data signal line of a selected memory device to the system data bus," and "when false, would electrically separate (i.e., 'isolate') from the common bus a load (e.g., 'capacitive load') associated with data pins of the memory devices controlled by that chip-select signal." *Id.*

## IV. CONCLUSION

Having reconsidered the parties' respective arguments and evidence cited in support thereof in light of our construction of "selectively isolating" as "isolating in response to a selection," and in light of the court's construction of "selectively electrically coupling" as "coupling in response to a selection," we are persuaded that Amidi, alone or in combination with Ludwig, discloses a circuit "configurable to be responsive to the set of input



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signals [comprising row address signals, column address signals, bank address signals and chip-select signals] by selectively isolating one or more loads of the DDR memory devices from the computer system," as recited in claim 22, and "further configurable to selectively isolate a data signal line of a DDR memory device of the plurality of DDR memory devices from the computer system," as recited in claim 26. We also are persuaded that combining Ludwig's VIC chip with Amidi's memory module would have resulted in a circuit "configurable to be responsive to the set of input signals [comprising row address signals, column address signals, bank address signals and chip-select signals] by selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line," as recited in claims 15 and 31. Accordingly, given the Federal Circuit's directive, because we find the asserted prior art discloses or suggests these claim limitations, we determine that '150 patent claims 15–17, 22, 24, 26, and 31–33 are unpatentable.

## V. ORDER

Accordingly, it is

ORDERED that claims 15–17, 22, 24, 26, and 31–33 of U.S. Patent 7,881,150 B2 are unpatentable; and

FURTHER ORDERED that this is a final written decision under 35 U.S.C. § 318(a). Parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.



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