Trials@uspto.gov
571.272.7822

Paper No. 36
Entered: September 28, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK CORP.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2015-01020
Patent 7,881,150 B2

Before BRYAN F. MOORE, GEORGIANNA W. BRADEN, and PETER P. CHEN, *Administrative Patent Judges*.

CHEN, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318 and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

SanDisk Corporation ("Petitioner") filed a Petition (Paper 2, "Pet.") to institute an *inter partes* review of claims 15–17, 22, 24, 26, and 31–33 (the "challenged claims") of U.S. Patent No. 7,881,150 B2 (issued Feb. 1, 2011, "the '150 patent"). Netlist, Inc. ("Patent Owner") did not file a Preliminary Response. On October 8, 2015, we instituted an *inter partes* review of all of the challenged claims on the following grounds alleged in the Petition.

References	Basis	Claims Challenged
Takeda[1] and JEDEC[2]	§ 103(a)	15, 16, 31, and 32
Takeda, JEDEC, and Connolly[3]	§ 103(a)	17, 22, 24, 26, and 33

See Paper 6 ("Dec. to Inst."), 17–18.

After institution of trial, Patent Owner filed a Patent Owner Response (Paper 13, "PO Resp."), to which Petitioner filed a Reply (Paper 16, "Pet. Reply"). An oral argument was held on June 28, 2016, consolidated with the oral hearing for IPR2015-01021. *See* Paper 30. A transcript ("Tr.") of the oral argument is included in the record. Paper 32. We requested post-hearing briefing regarding Patent Owner's contention that Petitioner's Reply and accompanying declaration were improper. *See* Paper 30 ("Pet. Post Hrg Br."), Paper 33 ("PO Post Hrg Br.").

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[1] Japanese Patent Publication H10-320270 (certified English translation), Dec. 4, 1998 (Ex. 1004) ("Takeda").

[2] JEDEC Standard 21-C, DDR SDRAM Registered DIMM Design Specification, Jan. 1, 2002 (Ex. 1011) ("JEDEC").

[3] U.S. Patent No. 6,070,217, May 30, 2000 (Ex. 1005) ("Connolly").

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B. Related Proceedings

Petitioner informs us that the ’150 patent is involved in the following federal district court case: *Netlist, Inc. v. Smart Modular Technologies*, Case No. 4:13-CV-05889-YGR (N.D. Cal.). Paper 10, 1. In addition, Petitioner filed two other petitions requesting *inter partes* review of the same challenged claims of the ’150 patent, resulting in the institution of IPR2014-00882 and IPR2014-01011. *Id.* at 2. We have issued final decisions in those proceedings finding the challenged claims to be unpatentable. *See* Case IPR2014-00882, slip op. at 50 (PTAB Dec. 14, 2015); Case IPR2014-01011, slip op. at 45 (PTAB Dec. 14, 2015).

C. The ’150 Patent

The ’150 patent is titled “Circuit Providing Load Isolation and Memory Domain Translation for Memory Module” and is directed to a memory module of a computer system with improved performance and memory capacity. Ex. 1001, 1:35–38. Memory module 10 includes a plurality of memory devices 30 (arranged in ranks 32) and circuit 40. *Id.* at 4:56–65; Fig. 1. Circuit 40 is electrically coupled to memory devices 30 and memory controller 20 of a computer system. *Id.* at 4:56–65; Fig. 1. Circuit 40 receives input signals from memory controller 20. *Id.* The memory modules improve performance and memory capacity by isolating electrical loads of the memory devices from the computer system. *Id.* at 4:65–66. Figure 1 is reproduced below.

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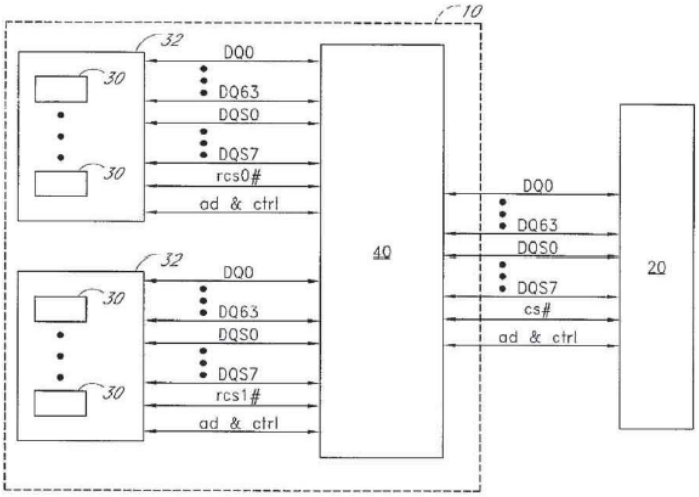

Figure 1 is a schematic of a memory module with circuit 40 and memory devices 30 and connectable to memory controller 20. Input signals (corresponding to a number of memory devices) from memory controller 20, such as chip select signals ("cs#"), are directed to memory module 10, which can act as a virtual memory module. *Id*. at 16:47–57; Figs. 1, 9A, 9B. As shown in Figure 1, based on the received input signals from memory controller 20, circuit 40 generates output signals corresponding to a larger number of memory devices on the memory module. *Id*. at Fig. 1. The output signals include a different number of chip select signals (e.g., "rcs0#" and "rcs1#") corresponding to the larger number of memory devices 30 shown in ranks 32. *Id*. at 16:66–17:3; Fig. 1.

Circuit 40 includes a logic element, such as a programmable logic device (PLD), an application-specific integrated circuit (ASIC), a field programmable gate array (FPGA), or a complex programmable logic device (CPLD). *Id*. at 6:40–45. Figure 9A is reproduced below.

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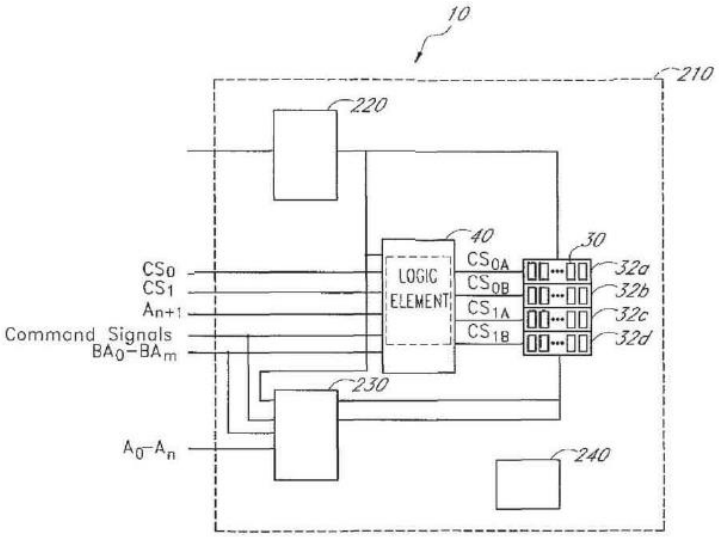

Figure 9A is a schematic of circuit 40 receiving a set of input command signals from memory controller 20 of the computer system. Circuit 40 also includes register 230 and phase-lock loop device (PLL) 220. *Id.* at 15:34–41; Fig. 9A. Figure 9A illustrates circuit 40 receiving a set of input command signals, address signals (A_{n+1}), including bank address signals (BA_0-BA_m), row address signals (A_0-A_n), column address signals, gated column address strobe signals, and chip-select signals (CS_0, CS_1), from memory controller 20 of the computer system. *Id.* at 16:24–30; 17:11–29. In response to the set of input address and command signals, circuit 40 generates a set of output address and command signals. *Id.* at 16:31–33.

With the output address and command signals, circuit 40 isolates the electrical loads of some of memory devices 30 from the computer system. *Id.* at 6:48–62. According to the ’150 patent, load isolation may result in specific benefits including reduced load related to data signal lines. *Id.* at 14:34–40. In order to isolate the loads, the logic element of circuit 40 translates between a system memory domain of the computer system and a

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physical memory domain of memory module 10. *Id.* at 6:48–62. Figure 3A is reproduced below.

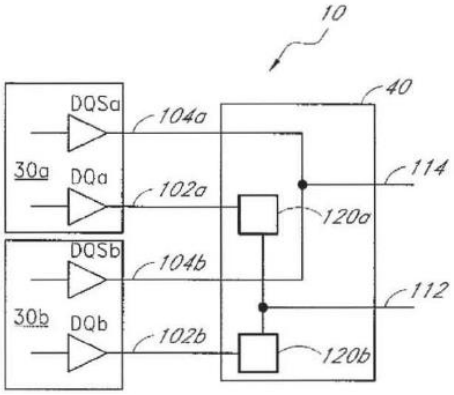

Figure 3A is a schematic of circuit 40 receiving a set of input command signals from memory controller 20 of the computer system. Circuit 40 comprises a logic element integral with and comprising switches 120 which are coupled to DQ data signal lines and DQS data strobe signal lines. Circuit 40 isolates the load of a memory device by isolating one or both of DQ data signal lines 102a and 102b of two memory devices 30a and 30b, from common DQ data signal line 112 that is coupled to the computer system. *Id.* at 6:63–7:2, Fig. 3A. Circuit 40 can electrically couple one or both of the DQ data signal lines 102a and 102b of the two memory devices 30a and 30b to the common data signal line 112, at the same time. *Id.* at 7:22–26. Circuit 40 also allows a DQ data signal to be transmitted from memory controller 20 of the computer system to one or both of DQ data signal lines 102a, 102b. *Id.* at 7:2–5. The logic element of circuit 40 uses switches 120a and 120b to selectively electrically couple one or more data signal lines to a common data signal line. *Id.* at 8:30–34.

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D. Illustrative Claim

Petitioner challenges claims 15–17, 22, 24, 26, and 31–33 of the ’150 patent, of which claims 15, 22, and 31 are independent claims. Claim 15 is illustrative of the challenged claims and is reproduced below:

15. A circuit configured to be mounted on a memory module so as to be electrically coupled to a first double-data-rate (DDR) memory device having a first data signal line and a first data strobe line, to a second DDR memory device having a second data signal line and a second data strobe line, and to a common data signal line,

    the memory module configured to be electrically coupled to a memory controller of a computer system so as to receive a set of input signals comprising row address signals, column address signals, bank address signals, and chip-select signals, the set of input signals compatible with a system memory domain of the computer system, the circuit comprising:

    a logic element;

    a register;

    a phase-lock loop device configured to be operationally coupled to the first DDR memory device, the second DDR memory device, the logic element, and the register,

    wherein the circuit is configurable to be responsive to the set of input signals by selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line, the circuit configurable to translate between the system memory domain of the computer system and a physical memory domain of the memory module,

    wherein the system memory domain has a first memory density per memory device, and the physical memory domain has a second memory density per memory device less than the first memory density per memory device.

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Ex. 1001, 42:41–43:2.

II. DISCUSSION

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are interpreted according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016) ("We conclude that the regulation represents a reasonable exercise of the rulemaking authority that Congress delegated to the Patent Office."). Under that standard, and absent any special definitions, we give claim terms their ordinary and customary meaning as would be understood by one of ordinary skill in the art at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

1. "Selectively Electrically Coupling"

In the Final Written Decisions in related IPR2014-00882 and IPR2014-01011 involving the same '150 patent, we construed the term "selectively electrically coupling" as "making a selection between at least two components so as to transfer power or signal information from one component to at least one other component." *See e.g.*, Case IPR2014-00882, slip op. at 11–13 (PTAB Dec. 14, 2015) (Paper 33).

Petitioner agrees with the construction set forth in the Final Written Decisions in the two related IPRs. Reply 1–3; Tr. 7:3–9. Patent Owner, however, contends that "selectively electrically coupling" should be construed as "the act of selecting or not selecting to create a structural pathway for electricity." Ex. 1029, 74:6–75:23; Tr. 70:4–9. According to Patent Owner, the Board's construction is unreasonably broad, whereas its

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proffered construction is more consistent with the disclosure of the ’150 patent. PO Resp. 13–16 (citing Ex. 1001, 5:29–30, 7:22; Ex. 2001 ¶¶ 41–42, 45–46). Patent Owner specifically argues that “electrically coupling” in the ’150 patent is provided by a structural pathway for electricity, which is also consistent with the meaning of “electrically coupling” as a term of art. *Id.* (citing Ex. 2001 ¶ 41, 46). Patent Owner further argues that a person of ordinary skill in the art would understand the act of electrically coupling to take place between two components, between which a structural pathway for electricity would be formed. *Id.*

We are unpersuaded by Patent Owner’s position. First, the claim language does not recite any physical or structural connection, rather, only “electrically coupling.” Pet. Reply 3, 8–9. In addition, the specification of the ’150 patent does not define explicitly the term “selectively electrically coupling.” Therefore, as in IPR2014-00882 and IPR2014-01011, we refer to its ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *Translogic Tech.*, 504 F.3d at 1257. A technical dictionary, the IEEE Dictionary,[4] defines “electrical coupling” as “[e]lectrical charges in conductors of a disturbed circuit formed by electrical induction.” Ex. 3001. The IEEE Dictionary explains that “[s]ince the ratio of a conductor’s electrostatic charge to the potential difference between conductors (required to maintain that charge) is the general definition of capacitance, electrical coupling is also called capacitive coupling.” *Id*. The IEEE Dictionary defines

[4] IEEE 100: The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition, Standards Information Network, IEEE Press (2000).

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"coupling capacitance (1) (ground systems)" ("capacitive coupling") as "[t]he association of two or more circuits with one another by means of capacitance mutual to the circuits." Ex. 3002. We understand this to mean that the two or more circuits are associated in such a way that power or signal information may be transferred from one circuit to another. The Oxford English Dictionary defines "selectively" as "[i]n a selective manner; by selection." Ex. 3003. The Oxford English Dictionary also defines "select" as "[t]o choose or pick out in preference to another or others." Ex. 3004.

Accordingly, as in IPR2014-00882 and IPR2014-01011, we construe "selectively electrically coupling," as "making a selection between at least two components so as to transfer power or signal information from one selected component to at least the other selected component," because such a construction is consistent with the ordinary and customary meaning of "selectively electrically coupling."

2. All Other Claim Terms

We determine that no explicit construction is necessary for any other terms in the challenged claims.

B. Principles of Law

To prevail in its challenges to the patentability of the claims, a petitioner must establish facts supporting its challenges by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

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KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")). This burden never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burden of proof in *inter partes* review). Furthermore, Petitioner cannot satisfy its burden of proving obviousness by employing "mere conclusory statements." *In re Magnum Oil Tools Int'l, Ltd.*, No. 2015-1300, 2016 WL 3974202, at *10 (Fed. Cir. July 25, 2016).

Thus, to prevail in an *inter partes* review, Petitioner must explain how the proposed combinations of prior art would have rendered the challenged claims unpatentable. At this final stage, we determine whether a preponderance of the evidence of the record shows that that the challenged claims would have been obvious over the proposed combinations of prior art.

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We analyze the instituted grounds of unpatentability in accordance with the above-stated principles.

C. Level of Ordinary Skill in the Art

In determining whether an invention would have been obvious at the time it was made, we determine the level of ordinary skill in the pertinent art at the time of the invention. *Graham*, 383 U.S. at 17. "The importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry." *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991).

Petitioner's Declarant, Srinivasan Jagannathan, Ph.D. ("Dr. Jagannathan"), testifies that a person of ordinary skill in the art at the time of the '150 patent:

> would understand basic memory and data communication concepts, with a bachelor's degree in any of electrical engineering, computer engineering, computer science, or related field. Course work for one of ordinary skill in the art would have included a course on computer organization, principles of digital design, or computer architecture. One of ordinary skill in the art would also have around one year of experience related to computer memory systems. For example, such experience may include experience in DRAM memory technology and related industry standards such as JEDEC standards for DRAM memories and memory modules.

Ex. 1002 ¶ 56. Patent Owner's Declarant, Carl Sechen, Ph.D. ("Dr. Sechen"), testifies that one of ordinary skill in the art at the time of the '150 patent would have had an undergraduate degree in electrical engineering or computer engineering, at least two years of professional experience in the design of memory systems, familiarity with the latest JEDEC standard specifications for memory devices and modules, and familiarity with the

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latest DRAM (dynamic random access memory) memory devices widely available in the market. Ex. 2001 ¶ 14. Dr. Sechen further testifies that a person of ordinary skill in the art would have design proficiency in memory modules comprising DDR memory technology, such as memory modules with JEDEC standard DDR SDRAM (synchronous DRAM) devices. *Id.* ¶ 15.

Based on our review of the ’150 patent and the types of problems and solutions described in the ’150 patent and cited prior art, we conclude a person of ordinary skill in the art at the time of the ’150 patent would have a Bachelor’s degree in electrical engineering, computer engineering, computer science, or related field, and at least one year of work experience, including familiarity with computer memory systems and related industry standards such as JEDEC standards for DRAM memories and memory modules. We further note that the applied prior art reflects the appropriate level of skill at the time of the claimed invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

D. Declarant Testimony

Patent Owner argues that Petitioner’s Declarant, Dr. Srinivasan Jagannathan, does not qualify as a person of ordinary skill in the art at the time of the invention because of his alleged lack of experience designing memory modules. PO Resp. 16–17. According to Patent Owner, Dr. Jagannathan’s experience and background is directed to software and is not relevant to the case. *Id.* at 18–23. Patent Owner argues that, unlike Dr. Jagannathan, its Declarant, Dr. Sechen, has significant practical experience designing memory modules. *Id.* at 18; Ex. 2001 ¶¶ 3, 4, Exhibit A.

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As to his hardware and memory design experience, Dr. Jagannathan was awarded a Doctorate degree in Computer Science, and has two decades of experience in the design, development, and analysis of a wide range of hardware, software, network and database systems. Ex. 1002 ¶ 2. He has designed and implemented hardware virtual memory caches, and researched theoretical performance measures of various cache coherency protocols. *Id.* Dr. Jagannathan also stated during his deposition in IPR2014-00882 that he has experience in the design of memory systems. Ex. 2003, 124:12–126:1. Patent Owner contends, however, that Dr. Jagannathan fails to qualify as a person of ordinary skill in the art because he lacks sufficient professional experience physically designing (i.e., "actually putting down a design and saying this is what it would be") a memory module. PO Resp. 21 (citing Ex. 2003, 125:14–17). We disagree.

To testify as an expert under Federal Rule of Evidence 702, a person need not be a person of ordinary skill in the art, but rather must be "qualified in the pertinent art." *Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1363–64 (Fed. Cir. 2008); *see SEB S.A. v. Montgomery Ward & Co.*, 594 F.3d 1360, 1372–73 (Fed. Cir. 2010) (upholding a district court's ruling to allow an expert to provide testimony at trial because the expert "had sufficient relevant technical expertise" and the expert's "knowledge, skill, experience, training [and] education . . . [wa]s likely to assist the trier of fact to understand the evidence"); *Mytee Prods., Inc. v. Harris Research, Inc.*, 439 F. App'x 882, 886–87 (Fed. Cir. 2011) (non-precedential) (upholding admission of the testimony of an expert who "had experience relevant to the field of the invention," despite admission that he was not a person of ordinary skill in the art). As noted above, Dr. Jagannathan has designed and

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implemented hardware virtual memory caches, and researched theoretical performance measures of various cache coherency protocols, and has experience in the design of memory systems. We find that, although Dr. Jagannathan may be less experienced than Dr. Sechen in the area of memory module design, he is nonetheless qualified sufficiently to testify about memory systems and memory modules.

E. Asserted Obviousness of Claims 15, 16, 31, and 32 in view of Takeda and JEDEC

Petitioner contends claims 15, 16, 31, and 32 of the ’150 patent are unpatentable under 35 U.S.C. § 103 in view of Takeda and JEDEC. Pet. 13–32. For reasons that follow, we determine Petitioner has not demonstrated by a preponderance of the evidence that claims 15, 16, 31, and 32 are unpatentable.

1. Overview of Takeda (Ex. 1004)

Takeda is titled “Memory Module” and discloses a memory module having more banks of SDRAMs than are expected by the computer system to which it is connected. Ex. 1004, Abstract, ¶ 4. The computer system indicates the number of banks that it expects to find on a memory module by providing a fixed number of fully decoded chip select signals to the memory module. *Id.* ¶ 12, Fig. 2. Thus, the memory module of Takeda simulates a memory module having the expected configuration. Because Takeda’s memory module has more banks than the computer expects, the circuitry on the memory module generates the required extra chip select signals to operate the additional banks. Ex. 1004 ¶¶ 12–13. Figure 1 of Takeda is reproduced below (with annotations by Petitioner).

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Ex. 1042, p. 15

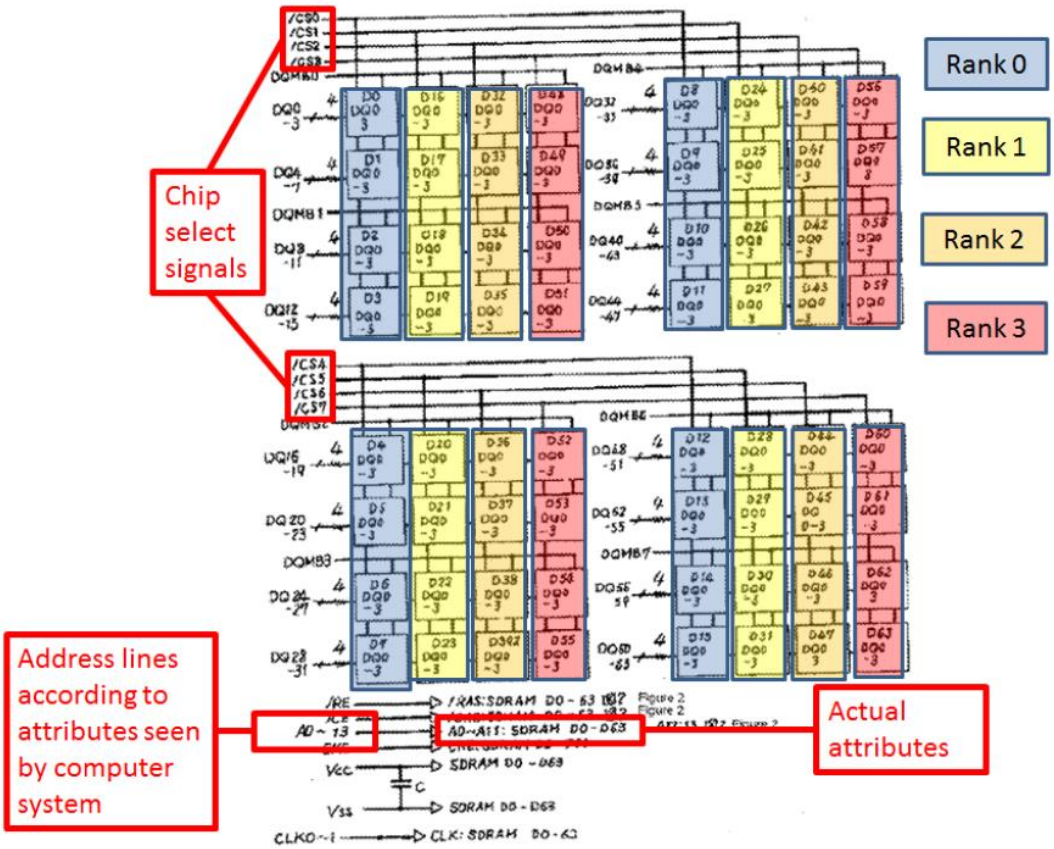

Figure 1 is a schematic of the configuration of a plurality of banks composed of a plurality of multibit DRAMs. In particular, Figure 1 of Takeda identifies the banks ("ranks") of SDRAM chips along with their associated chip select signals. An illustration of the bank control unit is shown in Figure 2 of Takeda reproduced below (with annotations by Petitioner).

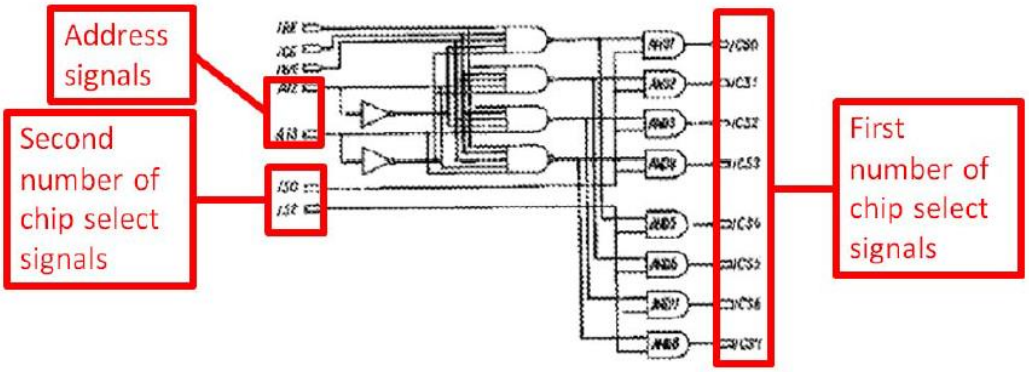

Figure 2 is a schematic of the bank control unit of Takeda. The signals on the left side of the bank control unit are received from "outside the module" while the signals on the right are generated to control the plurality of banks on the memory module. Ex. 1004 ¶ 5.

2. Overview of JEDEC (Ex. 1011)

JEDEC is a product datasheet describing electrical requirements for DDR SDRAM dual in-line memory modules (DIMMs) as existed in 2002, and illustrates the configuration of the DDR memory and data signals lines, data strobe lines, row/column address signals, bank address signals, and chip select signals. Ex. 1011, 6, 13.[5] JEDEC further discloses a memory module that includes a register and a phase-locked loop (PLL) device. *Id.* at 13, 17, 29. The PLL of JEDEC directly provides the clock signal to the SDRAM memory devices. *Id.* at 17.

3. Analysis

Petitioner relies on the Declaration of Dr. Jagannathan (Ex. 1002) and contends the combined disclosures of Takeda and JEDEC, as summarized

[5] Page numbers in the upper right of Ex. 1011 are styled "Page 4.20.4–__."

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Ex. 1042, p. 17

above, disclose each limitation of claims 15, 16, 31, and 32 of the ’150 patent. Petitioner first argues that the combination discloses the preamble of independent claims 15 and 31, including the memory module being configured to be electrically coupled to a memory controller so as to receive the recited types of input signals. Pet. 18–21 (citing Ex. 1002 ¶¶ 64, 67, 68, 92, 95, 103; Ex. 1004 ¶¶ 5, 12–14, Fig. 1; Ex. 1011, 6–7, 10–16). In particular, Petitioner contends that although Takeda discloses the use of SDRAM memory devices, DDR memory devices could also be used because they are compatible with SDRAM devices, as expressly stated in the JEDEC reference. Pet. 19; Ex. 1002 ¶¶ 67–68, Ex. 1011, 13 (“x64 DIMM, populated as two physical banks of x8 DDR SDRAMs”).

Petitioner asserts Takeda discloses the recited logic element and JEDEC discloses the recited register. Pet. 17, 22–24 (citing Ex. 1002 ¶¶ 63, 94, 102; Ex. 1004 ¶ 5; Ex. 1011, 13, 29).

Petitioner further contends JEDEC discloses the recited phase-locked loop that is operationally coupled to the first and second DDR memory devices, the logic element, and the register. *Id.* at 17, 24–26 (citing Ex. 1011, 17, 29). Petitioner next contends the combination discloses that the recited circuit is responsive to the set of input signals by selectively electrically coupling the first and second data signal lines to the common data signal line, stating “[b]oth JEDEC and Takeda disclose memory architectures having more than one bank with a common data line between memory devices of different banks.” *Id.* at 26–28 (citing Ex. 1002 ¶¶ 60–62, 66, 95, 100; Ex. 1004, Fig.1; Ex. 1011, 13).

Finally, Petitioner contends Takeda and JEDEC disclose the recited limitation of the circuit being “configurable to translate between the system

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Ex. 1042, p. 18

memory domain of the computer system and a physical memory domain of the memory module." *Id.* at 29–31 (citing Ex. 1004 ¶¶ 3, 15, 16, Fig. 2).

Petitioner provides a rationale for combining Takeda with JEDEC, including the accurate statement that, "Takeda explicitly discloses that the design standards for memory module design are provided in JEDEC documents." Pet. 17–18 (citing Ex. 1004 ¶ 2); *see id.* at 19, 24.

Patent Owner argues the combination does not teach or suggest the recited circuit performing the selectively electrically coupling. PO Resp. 3–10. According to Patent Owner, "the express language of claims 15 and 31 . . . require a 'circuit' to perform the 'selectively electrically coupling' . . . ." *Id*. at 4. We agree. The plain language of claims 15 and 31 requires the circuit to perform the selectively electrically coupling function. *Id*. at 9; Ex. 1001, 7:19–21, 8:21–34, 42:52–53, 43:6–7, 44:39–40, 44:61–62. In particular, claims 15 and 31 recite that the "circuit is configurable to be responsive to the set of input signals by selectively electrically coupling the first data signal line . . . ." Ex. 1001, 42:58–60, 44:46–48. Thus, the circuit is what performs the selectively electrically coupling, in response to input signals. More specifically, claims 15 and 31 recite that the circuit includes a logic element (which can comprise switches) that performs selectively electrically coupling. *Id*. at 7:19–21, 8:21–34.

Claims 15 and 31 further recite that the circuit is coupled to DDR memory devices. *Id*. at 42:41–45, 44:28-32. Patent Owner contends, "[i]n the claim language, this 'circuit' is plainly distinct from the claimed 'DDR memory device.'" PO Resp. 4. At his deposition, Petitioner's Declarant Dr. Jagannathan confirmed that "the circuit is something that's distinct from the – from the memory device." Ex. 2002, 134:22–135:17.

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Ex. 1042, p. 19

Patent Owner further argues that neither Takeda nor JEDEC teach or suggest a circuit selectively electrically coupling. PO Resp. 2–6. Dr. Jagannathan testified that in the combination of Takeda and JEDEC, the function of selectively electrically coupling occurs in a memory device. *Id*. at 3–4; Ex. 2002, 150:12–151:9, 153:7–11. As stated by Dr. Jagannathan, the memory device is separate and distinct from the circuit.

Accordingly, the combination of Takeda and JEDEC teaches or suggests selectively electrically coupling, occurring not in the recited circuit of independent claims 15 and 31 (and, dependent claims 16 and 32), but rather, in the separate memory device. We, therefore, are not persuaded that Petitioner has proven by a preponderance of the evidence that claims 15, 16, 31, and 32 would have been obvious in light of the combination of Takeda and JEDEC.

F. Asserted Obviousness of Claims 17, 22, 24, 26, and 33 in view of Takeda, JEDEC, and Connolly

Petitioner cites to the Jagannathan declaration and contends claims 17, 22, 24, 26, and 33 of the ’150 patent are unpatentable under 35 U.S.C. § 103 in view of Takeda, JEDEC, and Connolly. Pet. 32–41. For reasons that follow, we determine Petitioner has demonstrated by a preponderance of the evidence that claims 17, 22, 24, 26, and 33 are unpatentable.

1. Overview of Connolly (Ex. 1005)

Connolly is titled “High Density Memory Module with In-line Bus Switches Being Enabled in Response to Read/Write Selection State of Connected RAM Banks to Improve Data Bus Performance” and describes a memory device isolation technique that aims to reduce the capacitance load of memory chips on a bus: “What is needed in order to better utilize less

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expensive RAM chips in systems with otherwise limited memory expansion is a way to minimize data line capacitance loading so that oversize memory modules with banks of RAM chips can be added to the system." Ex. 1005, 1:48–53.

In order to reduce this capacitive loading, Connolly provides "a two-part solution to reducing data line capacitance to an acceptable system limit." *Id.* at 1:63–64. First, Connolly provides switches between the memory chips on a memory module. *Id*. at 1:64–67. "DRAMs 900-1 to 900-10, preferably SDRAMs, are coupled through bit switches 909-1 to 909-10 as controlled by ASIC 910." *Id*. at 5:7–13, Fig. 6A, 1:67–2:4. "The second part of the solution according to the invention is logic generating a signal that enables the bus switches. The logic may be in an application specific integrated circuit (ASIC)." *Id*. at 2:20–23. Figure 6A of Connolly is reproduced below.

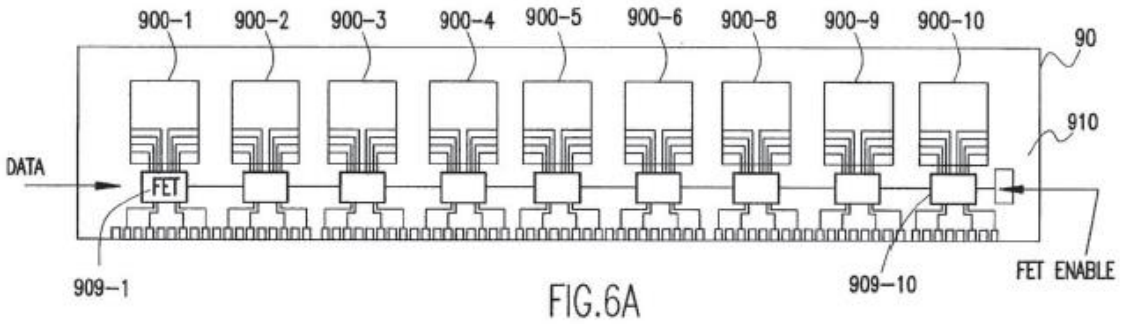

Figure 6A depicts memory module 90 with integrated circuit ("ASIC") 910 and memory chips SDRAMs 900-1 to 900-10, coupled through bit switches 909-1 to 909-10 as controlled by ASIC 910. *Id.* at 5:5–13. In describing Figure 6C which is similar to Figure 6A, the specification states that each SDRAM is "controlling its respective bit switch." *Id*. at 6:1–2. Figure 3 of Connolly is reproduced below.

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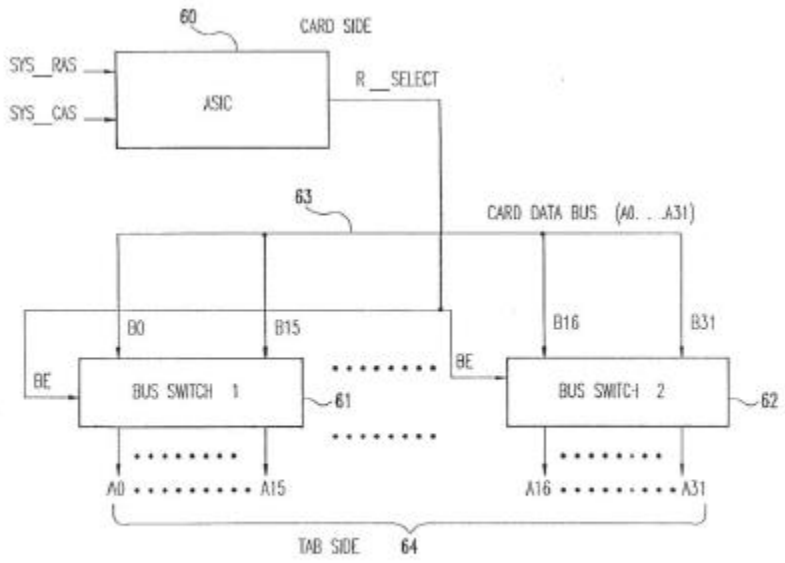

FIG.3

Figure 3 is a block diagram showing ASIC 60 receiving row address strobe (RAS) and column address strobe (CAS) signals. ASIC 60 determines the READ/WRITE state of the memory from the RAS and CAS signals and generates an RC_SELECT signal to the enable inputs of bus switches 61 and 62. *Id*. at 4:12–17.

2. *Patent Owner's Request to Exclude Petitioner's Reply and Jagannathan Supplemental Declaration.*

Preliminarily, Patent Owner seeks to exclude Petitioner's Reply and the Supplemental Declaration of Dr. Jagannathan (Ex. 1028). Paper 23; PO Post Hrg Br. Patent Owner contends Petitioner's Reply adds a new theory of how the combination of Takeda, JEDEC, and Connolly teaches or suggests the elements of these claims. *Id*. Specifically, Patent Owner argues that the Petition asserted the output chip select signal of Takeda was itself "the logic signal" to enable operation of bit-switches, but the Reply instead asserted for the first time that Takeda's chip-select signal merely generated a new logic signal, which in turn enabled operation of bit-switches:

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> In its Reply, Petitioner exceeded the scope of the Patent Owner Response. Rather than directly address the inoperability of the original combination theory, Petitioner introduced a new combination theory: using an output chip-select signal <u>to generate a new logic signal</u> to enable bit-switches, via new logic circuitry.

Paper 23, 1; *see* PO Post Hrg Br. 1–5. Patent Owner focuses on paragraph 106 of the first Jagannathan Declaration (Ex. 1002), which states:

> Moreover, since Connolly teaches a logic element to enable the bit switches, one of ordinary skill would find it obvious to use the chip-select signals output from the Takeda bank-control unit as the logic signal to enable the bit switches. Thus, when a chip-select output from the bank control unit is used to enable a particular DDR SDRAM device, it is also used to enable the bit switch inline with data signal lines from that DDR SDRAM device. The bit-switches from the data lines of the non-selected SDRAM devices would then isolate those data signal lines from the computer system.

Ex. 1002 ¶ 106. According to Patent Owner, the first sentence of paragraph 106 states that one of ordinary skill would "use the chip-select signals output from the Takeda bank-control unit *as the logic signal to enable* the bit switches" (emphasis added). Paper 23, 1; PO Post Hrg Br., 2–3. Patent Owner asserts that Petitioner's Reply improperly recasts the combination by arguing therein that the chip select signal is used only "'to determine the enable input' to the bit switches." Paper 23, 2 (citing Pet. Reply 23); PO Post Hrg Br. 5.

Petitioner, in rebuttal, points to the second sentence of paragraph 106, which states the chip select signal "is *also used to enable* the bit switch" (emphasis added). Paper 25, 2; Pet. Post Hrg Br. 4. Petitioner contends that its "combination and rationale has remained consistent throughout the

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proceeding," noting the Petition "explicitly set forth the argument that the chip-select signals are used to generate the switch enable signals." Pet. Post Hrg Br. 3 (citing Pet. 35–36). At oral hearing, Petitioner acknowledged that the first sentence of paragraph 106 was "inartfully" drafted. Tr. 29:21–24.

Petitioner further contends Patent Owner had notice of Petitioner's theory and opportunity to address the issue, because of Dr. Jagannathan's testimony at deposition, which occurred ten days before Patent Owner filed its Response. Pet. Post Hrg Br. 7. Dr. Jagannathan testified at deposition that the chip select signal is used to determine the enable input to the bit switches. *Id*. at 7–9 (citing Ex. 2002, 187:22–188:10, 218:6–17). At oral hearing, Patent Owner acknowledged it was aware of Dr. Jagannathan's chip select signal explanation no later than the deposition, which preceded Patent Owner's Response by ten days. Tr. 43:9–44:1.

We have reviewed the parties' contentions on this issue, and exercise our discretion to determine that Petitioner's Reply and the Jagannathan Supplemental Declaration will not be excluded. We find that, although they may be "inartfully" drafted, the first Jagannathan declaration and Petition sufficiently outlined Petitioner's position on the function of the chip select signal, namely, that the chip select signal was not itself the logic signal enabling operation of bit-switches. We further find that Petitioner's Reply and the Supplemental Jagannathan Declaration did not present an entirely new rationale of unpatentability based on Takeda, JEDEC, and Connolly. *Cf. Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369–70 (Fed. Cir. 2016) (affirming Board's exclusion of reply brief and declaration that changed unpatentability theory to "an entirely new rationale").

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Moreover, there is no dispute that Patent Owner was aware of Petitioner's position by no later than the Jagannathan deposition, which preceded Patent Owner's Response by ten days. Patent Owner could have addressed Petitioner's chip select signal contention, procedurally or substantively, in its Response, but chose to raise the issue only after Petitioner filed its Reply and Supplemental Jagannathan Declaration. Accordingly, Patent Owner had notice of Petitioner's position and an opportunity to refute that position in its Response.

3. Analysis – Claims 17 and 33

Petitioner relies on the First Declaration of Dr. Jagannathan (Ex. 1002) and the Supplemental Declaration of Dr. Jagannathan (Ex. 1028), and contends the combined disclosures of Takeda, JEDEC, and Connolly disclose each limitation of claims 17, 22, 24, 26, and 33. Pet. 32–41; Pet. Reply 14–25.

Dependent claims 17 and 33 depend from claims 15 and 31 and recite that the circuit further comprises one or more switches that perform the selective electrical coupling. Ex. 1001, 43:6–12, 44:61–67. Petitioner asserts that Connolly meets this limitation, because it uses one or more switches between memory devices on a memory module. Pet. 34 (citing Ex. 1005, 1:67–2:4). As illustrated in Connolly Figure 6A, "DRAMs 900-1 to 900-10, preferably SDRAMs, are coupled through bit switches 909-1 to 909-10 as controlled by ASIC 910." *Id.* (citing Ex. 1005, 5:5–13). Petitioner asserts that Connolly uses switches (in circuit 910) to selectively electrically couple the data signal line of a memory device to the common data signal line, thereby isolating the unselected memory devices to reduce the capacitive load of the memory chips. *Id.* at 34–35 (citing Ex. 1005, 1:48–

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63). Switches 909-1 to 909-10 are described as part of circuit 910. Ex. 1005, 5:5–17, Fig. 6A. We determine that Connolly thereby teaches that the selectively electrically coupling, as recited in independent claims 15 and 31, occurs in its circuit.

Petitioner also asserts that Connolly discloses its switches are operatively coupled to the logic element, as recited in the claims, to receive control signals from the logic element: "As shown in the block diagram of Figure 3, the ASIC 60 (corresponding to ASICs 310 and 410 of Figure 1) receives the system's RAS and CAS signals, determines the READ/WRITE state of the memory from the RAS and CAS signals and generates therefrom, an RC_SELECT signal to the enable inputs of bus switches 61 and 62." *Id.* at 35 (citing Ex. 1005, 4:12–17). Thus, according to Petitioner, Connolly's switches are controlled by signals from the ASIC. *Id.*

Lastly, as described above, Petitioner contends that Connolly's switch enable signals are activated "relative to which [of Takeda's] chip select signals are activated." *Id.* at 35–36. Petitioner explains:

> [T]he combination of Takeda, JEDEC, and Connolly suggests using a chip select signal to determine the enable input to the bit switches of Connolly. Specifically, Takeda uses the chip select signal (CS0–CS7) to select a particular rank of memory devices. It would have been obvious to a POSITA that the chip select signals would also be used to determine the enable state of bit switches on the data lines of those memory devices, particularly given Connolly's use of RAS and CAS signals in its logic element.

Pet. Reply 21.

Patent Owner argues one of ordinary skill in the art would not have perceived a reasonable expectation of success as to the combination, and, in particular, that the combination exceeds any suggestion of the references,

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would be inoperable, and beyond the level of skill of a person of ordinary skill in the art (POSITA). PO Resp. 20–40. Petitioner, however, asserts the first two of these arguments are based on Patent Owner's characterization of Takeda's chip select signal also constituting the logic signal enabling bit-switches. Pet. Reply 14–23. According to Petitioner, Takeda, JEDEC, and Connolly do teach or suggest Petitioner's actual contention that the chip select signal is used to determine the enable input to the bit switches. *Id.* at 15–22. Petitioner states:

> Thus, the Petition relies on the concept of selectively coupling data lines from different memory devices to the common data lines taught by the combination of Takeda and JEDEC. (*Id.* [Pet.] at pp. 27-28.) Connolly is relied upon primarily for its teaching of using bit switches to isolate data lines, and it would have been obvious for a POSITA to incorporate similar bit switches within the system of Takeda and JEDEC. (Petition, pp. 33-36; Appendix A of Jagannathan [decl.], pp. 29-31; Jagannathan Tr., 185:15-22.)

Id. at 18–19. We agree with Petitioner's contentions, described above, that the references teach the limitations of claims 17 and 33, and adopt them as our own. We also agree with Petitioner that it has demonstrated the operability of its actual combination for use of Takeda's chip select signal as described above, and adopt Petitioner's contentions in that regard as our own. *Id.* at 22–23.

As to Patent Owner's argument that such use of Takeda's chip select signal would be beyond the skill level of a POSITA, Petitioner asserts Connolly does describe using command signals from a memory device to enable switches. Pet. 35; Pet. Reply 24 (citing Ex. 1005, 4:12–17, Fig. 3; Ex. 2002, 220:22–221:21, 222:18–224:5; Ex. 1028 ¶ 13)*; see* Tr. 75:4–21.

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Petitioner adds that, in general, JEDEC specifications, which are expressly referenced in Takeda, provide descriptions of signals used for proper timing operation of memory devices, and more specifically, the JEDEC reference describes a standard for DDR memory devices. Pet. Reply 24 (citing Ex. 1002 ¶¶ 38–44; Ex. 1028 ¶¶ 13, 16–19; Ex. 2002, 219:1–11, 220:22–221:21, 222:18–224:5).

Petitioner also cites the deposition testimony of Patent Owner's declarant that a POSITA would understand timing issues for DDR memory devices as described in the JEDEC standards. Pet. 24 (citing Ex. 1029, 31:23–32:1, 33:10–34:3). We also note that, as cited by Petitioner, we rejected a similar argument by a different Petitioner, in related IPR2014-00882, slip op. at 30–31. In summary, we agree with Petitioner that a POSITA would have possessed the requisite skill level to understand usage of Takeda's chip select signal to enable Connolly's bit switch, and adopt Petitioner's contentions in that regard as our own.

Therefore, after considering the entirety of the record, we determine that Takeda, JEDEC, and Connolly teach the switches recited for the selective coupling and the related limitations in dependent claims 17 and 33.

4. Claims 22, 24, and 26

For independent claim 22, which recites that the circuit is selectively isolating one or more loads of the DDR memory devices from the computer system (Ex. 1001, 43:51–54), Petitioner contends Connolly teaches a circuit that can "selectively isolate" a load because Connolly provides switches between the memory chips on a module to reduce (i.e., isolate) the capacitive load on the bus. Pet. 38–39 (citing Ex. 1005, 1:48–53, 1:67–2:4, 5:7–13). In particular, Petitioner contends Figure 6A of Connolly shows

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"DRAMs 900-1 to 900-10, preferably SDRAMs, are coupled through bit switches 909-1 to 909-10 as controlled by ASIC 910 (corresponding to ASICs 310 and 410 of FIG. 1)." (citing Ex. 1005, 5:7–13.) Petitioner also contends Connolly's switches are, as recited in claim 22, responsive to the set of input signals because Connolly's FETs are controlled by signals from the ASIC, which in turn are generated based on a received set of input signals. Pet. 39 (citing Ex. 1005, 4:12–17).

In addition, Petitioner explains how the combination of Takeda, JEDEC, and Connolly renders dependent claims 24 and 26 obvious. *Id.* at 40–41 (citing Ex. 1002, ¶¶ 74, 106). Dependent claim 24 (Ex. 1001, 43:3–5) recites two or more of the logic element, register, and phase-locked loop are part of the same component. Ex. 1001, 44:1–3. Petitioner points to JEDEC's memory module circuit, which as illustrated includes the phase-lock loop device and the register, as meeting this limitation. Pet. 31–32 (citing Ex. 1011, 29 (Figure)). Petitioner further asserts that one of ordinary skill would recognize that any two or more of the register, phase-locked loop device, and logic element could be implemented on a single integrated circuit. Pet. 40, citing Ex. 1002 ¶ 74. We agree that JEDEC's Figure (Ex. 1011, 29) discloses the phase-locked loop and register as part of the memory module circuit, and thus agree with and adopt as our own, Petitioner's arguments that JEDEC teaches the limitation of claim 24.

Dependent claim 26 recites that a data signal line of a DDR device is selectively isolated (Ex. 1001, 44:8–11). Petitioner contends that a person of ordinary skill in the art would recognize that Connolly's isolation of the memory device could also apply to isolate the data signal line of the device. Pet. 41. We credit the testimony of Dr. Jagannathan (Ex. 1002 ¶ 106) and

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agree that Connolly's teaching of isolation could be applied with a reasonable expectation of success by a person of ordinary skill in the art to isolate another part of the memory module, i.e., a data signal line of a memory device, and adopt Petitioner's arguments in that regard as our own.

5. Reason to Combine

Petitioner contends, citing to the Jagannathan Declaration, that a person of ordinary skill in the art would have had reason to combine the teachings of Takeda, JEDEC, and Connolly. Pet. 32–34, 39–41. Petitioner asserts that all three references relate to the design of memory modules, and that one of ordinary skill would have used Connolly's load isolation technique with the Takeda or JEDEC memory architectures because of the recognized reduced power consumption in reading from or writing to memory devices:

> [A] [person of ordinary skill in the art] would have been motivated to apply the known technique of switching data outputs of different memory devices disclosed by Connolly to the known memory circuits of either Takeda or JEDEC to yield predictable results of reducing capacitive loading, thus reducing power consumption.

Pet. 33–34; Ex. 1002 ¶¶ 45, 104–107. In addition, Petitioner notes that Takeda also expressly refers to JEDEC standards, by stating that "[k]nown configurations for memory modules which are used in computers and the like have been disclosed in JEDEC documents in the past." Pet. 17; Ex. 1004 ¶ 2. Consequently, "[b]ecause JEDEC provides the standards for implementing an overall DDR SDRAM architecture, a PHOSITA would have consulted JEDEC when designing and implementing the concepts taught in Takeda." Pet. 17–18 (citing Ex. 1002 ¶ 100).

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We have also considered Patent Owner's arguments regarding alleged lack of reasonable expectation of success, and Petitioner's arguments in response, and as discussed above, are persuaded by Petitioner's position. PO Resp. 20-40, Pet. Reply 14–24. We agree with and adopt Petitioner's reasoning and find Petitioner has shown sufficiently a reason to combine Takeda, JEDEC, and Connolly, providing articulated reasoning supported by rational underpinning for combining the references. *See KSR Int'l*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). Petitioner's reasoning includes explanations of reasons to combine and the underlying factual bases for one of skill to have done so. We specifically credit the testimony of Dr. Jagannathan, who explains that the combination of Takeda, JEDEC, and Connolly would constitute the use of a known technique to improve a similar device thereby yielding predictable results. Pet. 33–34 (citing Ex. 1002 ¶¶ 74, 104–107); *see* Ex. 1028 ¶ 16–19. We give Dr. Jagannathan's testimony substantial weight because it is supported by Takeda, JEDEC, and Connolly's disclosures and what Takeda, JEDEC, and Connolly would have conveyed to a person of ordinary skill in the art at the time of the invention.

Therefore, for the foregoing reasons and weighing the evidence as a whole, we conclude that Petitioner has shown by a preponderance of the evidence that claims 17, 22, 24, 26, and 33 would have been obvious over Takeda, JEDEC, and Connolly.

III. CONCLUSION

Based on the evidence and arguments, Petitioner has demonstrated by a preponderance of the evidence that claims 17, 22, 24, 26, and 33 of the '150 patent would have been obvious over Takeda, JEDEC, and Connolly.

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IV. ORDER

For the reasons given, it is

ORDERED that claims 17, 22, 24, 26, and 33 of the ’150 patent are unpatentable;

FURTHER ORDERED that claims 15, 16, 31, and 32 have not been shown to be unpatentable; and

FURTHER ORDERED that because this is a final written decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

FOR PETITIONER:

Lori Gordon
lgordon-PTAB@skgf.com

Rob Sokohl
rsokohl-PTAB@skgf.com

FOR PATENT OWNER:

Mehran Arjomand
David Kim
Erol Basol
Jean Nguyen
Jonathan Statman
63516-150-IPR3@mofo.com

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