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Paper No. 38
Entered: September 28, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK CORP.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2015-01021
Patent 8,081,536 B1

Before BRYAN F. MOORE, GEORGIANNA W. BRADEN, and PETER P. CHEN, *Administrative Patent Judges*.

MOORE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318 and 37 C.F.R. § 42.73

I. INTRODUCTION

A. *Background*

SanDisk Corporation ("Petitioner") filed a Petition (Paper 2, "Pet.") to institute an *inter partes* review of claims 1, 16, 17, 24, 30, and 31 (the "challenged claims") of U.S. Patent No. 8,081,536 B1 (issued Dec. 20, 2011, "the '536 Patent"). Netlist, Inc. ("Patent Owner") did not file a Preliminary Response. On October 8, 2015, we instituted an *inter partes* review of all of the challenged claims on the following grounds alleged in the Petition.

References	Basis	Claims Challenged
Takeda[1], JEDEC[2], and Connolly[3]	§ 103(a)	1, 16, 17, 24, 30, and 31

See Paper 8 ("Dec. to Inst."), 18.

After institution of trial, Patent Owner filed a Patent Owner Response (Paper 15, "PO Resp."), to which Petitioner filed a Reply (Paper 18, "Reply"). An oral argument was held on June 28, 2016, consolidated with the oral hearing for IPR2015-01020. *See* Paper 24. A transcript ("Tr.") of the oral argument is included in the record. Paper 34. We requested post-hearing briefing regarding Patent Owner's contention that Petitioner's Reply and accompanying Declaration were improper. *See* Paper 32 ("Pet. Post Hrg Br."), Paper 35 ("PO Post Hrg Br.").

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[1] Japanese Patent Publication H10-320270 (certified English translation), Dec. 4, 1998 (Ex. 1003) ("Takeda").

[2] JEDEC Standard 21-C, DDR SDRAM Registered DIMM Design Specification, Jan. 1, 2002 (Ex. 1006) ("JEDEC").

[3] U.S. Patent No. 6,070,217, May 30, 2000 (Ex. 1007) ("Connolly").

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B. Related Proceedings

Petitioner informs us that the ’536 Patent is involved in the following federal district court case: *Netlist, Inc. v. Smart Modular Technologies*, Case No. 4:13-CV- 05889-YGR (N.D. Cal.). Pet. 1. In addition, Diablo Technologies, Inc. filed a petition requesting *inter partes* review of the same challenged claims of the ’536 Patent, resulting in the institution of IPR2014-00883. *Id.* We have issued a final decision in that proceeding finding the challenged claims to be unpatentable. *See* Case IPR2014-00883, slip op. at 37 (PTAB Dec. 14, 2015).

C. The ’536 Patent

The ’536 Patent is directed to a memory module of a computer system with improved performance and memory capacity. Ex. 1001, 1:35–38. Memory module 10 includes a plurality of memory devices 30 (arranged in ranks 32) and circuit 40. *Id.* at 4:56–65, Fig. 1. Circuit 40 is electrically coupled to memory devices 30 and memory controller 20 of a computer system. *Id.* at 4:56–65, Fig. 1. The memory modules improve performance and memory capacity by isolating electrical loads of the memory devices from the computer system. *Id.* at 4:65–66.

Circuit 40 receives input signals from memory controller 20. *Id.* Figure 1 is reproduced below.

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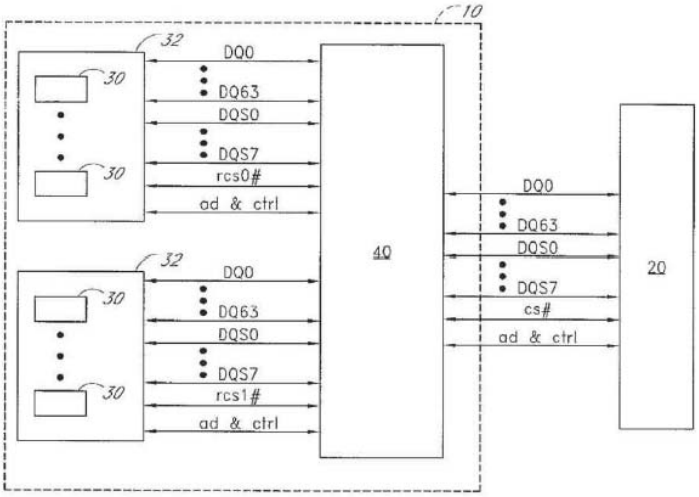

Figure 1 is a schematic of a memory module with circuit 40 and memory devices 30 and connectable to memory controller 20.

Figure 1, above, illustrates input signals (corresponding to a number of memory devices) from memory controller 20, such as chip select signals ("cs#") that are directed to memory module 10, which can act as a virtual memory module. *Id*. at 16:47–57, Figs. 1, 9A, 9B. As shown in Figure 1, based on the received input signals from memory controller 20, circuit 40 generates output signals corresponding to a larger number of memory devices on the memory module. *Id*. at Fig. 1. The output signals include a different number of chip select signals (e.g., "rcs0#" and "rcs1#") corresponding to the larger number of memory devices 30 shown in ranks 32. *Id*. at 16:66–17:3, Fig. 1.

Circuit 40 includes a logic element, such as a programmable logic device (PLD), an application-specific integrated circuit (ASIC), a field programmable gate array (FPGA), or a complex programmable logic device (CPLD). *Id*. at 6:40–45. Figure 9A is reproduced below.

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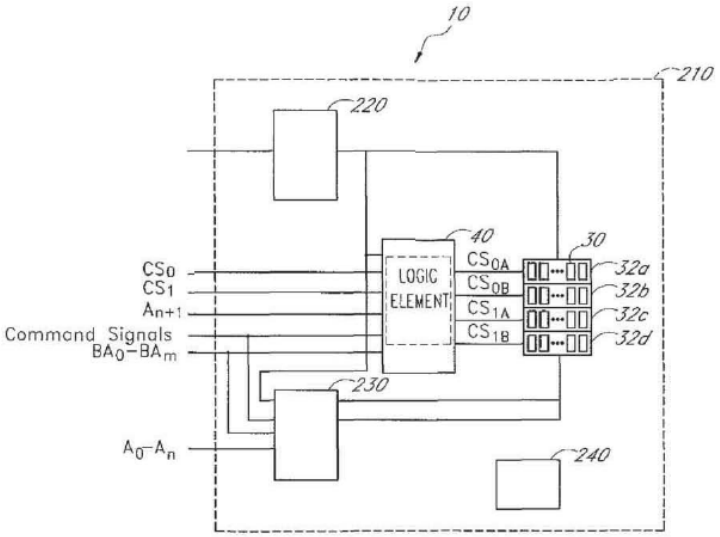

Figure 9A is a schematic of circuit 40 receiving a set of input command signals from memory controller 20 of the computer system.

As shown in Figure 9A, above, circuit 40 also includes register 230 and phase-lock loop device (PLL) 220. *Id.* at 15:34–41, Fig. 9A. Figure 9A illustrates circuit 40 receiving a set of input command signals, address signals (A_{n+1}), including bank address signals (BA_0-BA_m), row address signals (A_0-A_n), column address signals, gated column address strobe signals, and chip-select signals (CS_0, CS_1), from memory controller 20 of the computer system. *Id.* at 16:24–30, 17:11–29. In response to the set of input address and command signals, circuit 40 generates a set of output address and command signals. *Id.* at 16:31–33.

With the output address and command signals, circuit 40 isolates the electrical loads of some of memory devices 30 from the computer system. *Id.* at 6:48–62. According to the ’536 Patent, load isolation may result in specific benefits including reduced load related to data signal lines. *Id.* at 14:34–40. In order to isolate the loads, the logic element of circuit 40 translates between a system memory domain of the computer system and a

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physical memory domain of memory module 10. *Id.* at 6:48–62. Figure 3A is reproduced below.

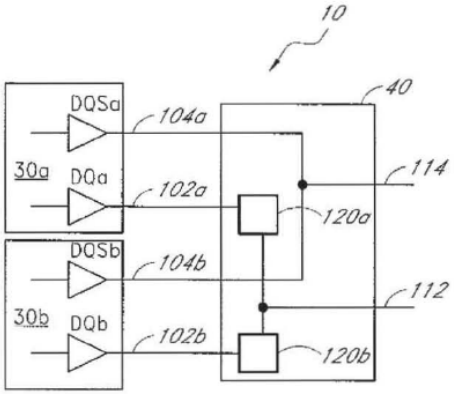

Figure 3A is a schematic of circuit 40 receiving a set of input command signals from memory controller 20 of the computer system.

As shown in Figure 3A, above, the circuit isolates the load of a memory device by isolating one or both of DQ data signal lines 102a and 102b of two memory devices 30a and 30b, from common DQ data signal line 112 that is coupled to the computer system. *Id.* at 6:63–7:2, Fig. 3A. Circuit 40 can electrically couple one or both of the DQ data signal lines 102a and 102b of the two memory devices 30a and 30b to the common data signal line 112, at the same time. *Id.* at 7:22–26. Circuit 40 also allows a DQ data signal to be transmitted from memory controller 20 of the computer system to one or both of DQ data signal lines 102a, 102b. *Id.* at 7:2–5. The logic element of circuit 40 uses switches 120a and, 120b to isolate or couple one or both of DQ data signal lines 102a and 102b of memory devices 30a and 30b from common data signal line 112. *Id* at 5–16.

D. Illustrative Claim

As noted above, Petitioner challenges claims 1, 16, 17, 24, 30, and 31 of the ’536 Patent, of which claims 1 and 24 are independent claims. Claim 1 is illustrative of the challenged claims and is reproduced below:

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1. A circuit configured to be mounted on a memory module configured to be operationally coupled to a computer system, the memory module having a first number of ranks, each rank of the first number of ranks comprising a plurality of double-data-rate (DDR) memory circuits that are configured to be activated concurrently with one another for receiving and transmitting data having a bit width of the rank in response at least in part to a first number of DDR chip-select signals, the circuit including at least one configuration in which the circuit is configured to:

receive a set of signals comprising address signals and a second number of DDR chip-select signals smaller than the first number of DDR chip-select signals;

generate phase-locked clock signals and transmit the phase-locked clock signals to the DDR memory circuits of the first number of ranks;

selectively isolate a load of the DDR memory circuits of at least one rank of the first number of ranks from the computer system in response at least in part to the set of signals; and

generate the first number of DDR chip-select signals in response at least in part to the phase-locked clock signals, the address signals, and the second number of DDR chip-select signals.

II. DISCUSSION

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are interpreted according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016) ("We conclude that the regulation represents a reasonable exercise of the rulemaking authority that Congress delegated to the Patent Office."). Under that standard, and absent any special definitions, we give claim terms their ordinary and customary meaning as would be understood by one of ordinary

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skill in the art at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

1. "Rank"

In the Decision to Institute, we construed the term "rank" as "a block or area that is created using some or all of the memory chips on a memory module." Dec. to Inst. 8–9.

In their papers, neither party challenged our constructions of these claim terms. Thus, for the term "rank," we see no reason to alter the construction of this claim term as set forth in the Decision to Institute as recited above, and we incorporate our previous analysis for purposes of this decision.

2. All Other Claim Terms

We determine that no explicit construction is necessary for any other terms in the challenged claims.

B. Principles of Law

To prevail in its challenges to the patentability of the claims, a petitioner must establish facts supporting its challenges by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in

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the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")). This burden never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burden of proof in *inter partes* review). Furthermore, Petitioner cannot satisfy its burden of proving obviousness by employing "mere conclusory statements." *In re Magnum Oil Tools Int'l, Ltd.*, No. 2015-1300, 2016 WL 3974202, at *10 (Fed. Cir. July 25, 2016).

Thus, to prevail in an *inter partes* review, Petitioner must explain how the proposed combinations of prior art would have rendered the challenged claims unpatentable. At this final stage, we determine whether a preponderance of the evidence of record shows that the challenged claims would have been obvious over the proposed combinations of prior art.

We analyze the instituted grounds of unpatentability in accordance with the above-stated principles.

C. Level of Ordinary Skill in the Art

In determining whether an invention would have been obvious at the time it was made, we determine the level of ordinary skill in the pertinent art at the time of the invention. *Graham*, 383 U.S. at 17. "The importance of

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resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry." *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991).

Petitioner's Declarant, Srinivasan Jagannathan, Ph.D. ("Dr. Jagannathan"), testifies that a person of ordinary skill in the art at the time of the '536 Patent:

> would understand basic memory and data communication concepts, with a bachelor's degree in any of electrical engineering, computer engineering, computer science, or related field. Course work for one of ordinary skill in the art would have included a course on computer organization, principles of digital design, or computer architecture. One of ordinary skill in the art would also have around one year of experience related to computer memory systems. For example, such experience may include experience in DRAM memory technology and related industry standards such as JEDEC standards for DRAM memories and memory modules.

Ex. 1002 ¶ 53. Patent Owner's Declarant, Carl Sechen, Ph.D. ("Dr. Sechen"), testifies that one of ordinary skill in the art at the time of the '536 Patent would have had an undergraduate degree in electrical engineering or computer engineering, at least two years of professional experience in the design of memory systems, familiarity with the latest JEDEC standard specifications for memory devices and modules, and familiarity with the latest DRAM (dynamic random access memory) memory devices widely available in the market. Ex. 2001 ¶ 14. Dr. Sechen further testifies that a person of ordinary skill in the art would have design proficiency in memory modules comprising DDR memory technology, such as memory modules with JEDEC standard DDR SDRAM (synchronous DRAM) devices. *Id.* ¶ 15.

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Based on our review of the ’536 Patent and the types of problems and solutions described in the ’536 Patent and cited prior art, we conclude a person of ordinary skill in the art at the time of the ’536 Patent would have a Bachelor’s degree in electrical engineering, computer engineering, computer science, or related field, and at least one year of work experience, including familiarity with computer memory systems and related industry standards such as JEDEC standards for DRAM memories and memory modules. We further note that the applied prior art reflects the appropriate level of skill at the time of the claimed invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

D. Declarant Testimony

Patent Owner argues that Petitioner’s Declarant, Dr. Srinivasan Jagannathan, does not qualify as a person of ordinary skill in the art at the time of the invention because of his alleged demonstrated technical errors and/or insufficient familiarity concerning the technological issues at hand. PO Resp. 23–24. Patent Owner argues that, unlike Dr. Jagannathan, its Declarant, Dr. Sechen, has significant practical experience designing memory modules *Id.* at 24; Ex. 2001, Exhibit A. .

As to his relevant hardware and memory design experience, Dr. Jagannathan was awarded a Doctorate degree in Computer Science, and has two decades of experience in the design, development, and analysis of a wide range of hardware, software, network and database systems. Ex. 1002 ¶ 2. He has designed and implemented hardware virtual memory caches, and researched theoretical performance measures of various cache coherency protocols. *Id.* Dr. Jagannathan also stated during his deposition

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in IPR2014-00883 that he has experience in the design of memory systems. Ex. 2003, 124:12–126:1.

To testify as an expert under Federal Rule of Evidence 702, a person need not be a person of ordinary skill in the art, but rather must be "qualified in the pertinent art." *Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1363–64 (Fed. Cir. 2008); *see SEB S.A. v. Montgomery Ward & Co.*, 594 F.3d 1360, 1372–73 (Fed. Cir. 2010) (upholding a district court's ruling to allow an expert to provide testimony at trial because the expert "had sufficient relevant technical expertise" and the expert's "knowledge, skill, experience, training [and] education . . . [wa]s likely to assist the trier of fact to understand the evidence"); *Mytee Prods., Inc. v. Harris Research, Inc.*, 439 F. App'x 882, 886–87 (Fed. Cir. 2011) (non-precedential) (upholding admission of the testimony of an expert who "had experience relevant to the field of the invention," despite admission that he was not a person of ordinary skill in the art). As noted above, Dr. Jagannathan has designed and implemented hardware virtual memory caches, and researched theoretical performance measures of various cache coherency protocols, and has experience in the design of memory systems. We find that Dr. Jagannathan is qualified sufficiently to testify about memory systems and memory modules.

E. Asserted Obviousness of Claims 1, 16, 17, 24, 30, and 31 in view of Takeda, JEDEC, and Connolly

Petitioner contends claims 1, 16, 17, 24, 30, and 31 of the '536 Patent are unpatentable under 35 U.S.C. § 103 in view of Takeda, JEDEC, and Connolly. Pet. 31–43. Patent Owner disputes Petitioner's contentions as to whether Takeda, JEDEC, and Connolly can be combined. PO Resp. 1. For

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reasons that follow, we determine Petitioner has demonstrated by a preponderance of the evidence that claims 1, 16, 17, 24, 30, and 31 are unpatentable.

1. Overview of Takeda

Takeda discloses a memory module having more banks than are expected by the computer system to which it is connected. Ex. 1004 ¶ 4. The computer system indicates the number of banks that it expects to find on a memory module by providing a fixed number of fully decoded chip select signals to the memory module. *Id.* ¶ 12, Fig. 2. Thus, the memory module of Takeda simulates to the computer system a memory module having the expected configuration. Because Takeda's memory module has more banks than the computer expects, the circuitry on the memory module generates the required extra chip selects to operate the additional banks. *Id.* ¶¶ 12–13; *see* Ex. 1002 ¶¶ 58–59. Petitioner's Declarant asserts "Takeda refers throughout to a "bank" of memory devices and therefore the 'banks' of Takeda are ranks." Pet. 14 (citing Ex. 1002 ¶¶ 55–56). Given this understanding, Figure 1 of Takeda is reproduced below with annotations by Petitioner.

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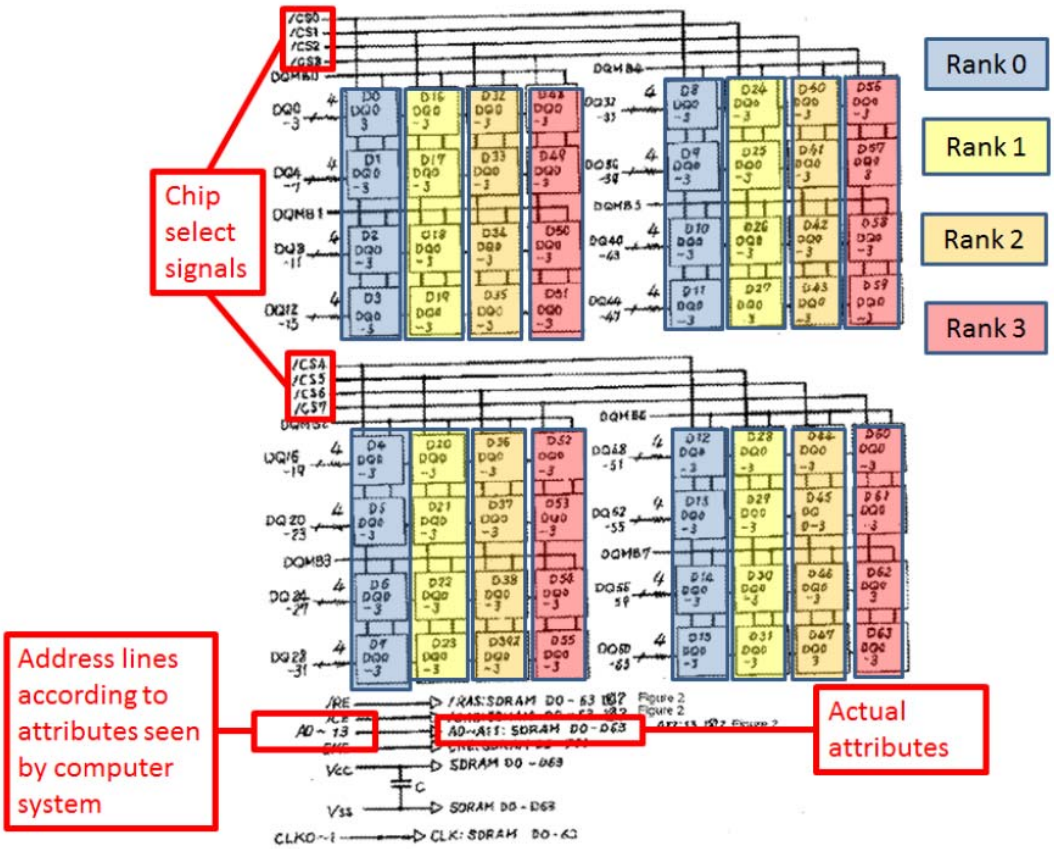

Figure 1 is a schematic of the configuration of a plurality of banks composed of a plurality of multibit DRAMs.

Figure 1 of Takeda identifies the ranks of SDRAM chips along with their associated chip select signals. An illustration of the bank control unit is shown in Figure 2 of Takeda, reproduced below with annotations by Petitioner.

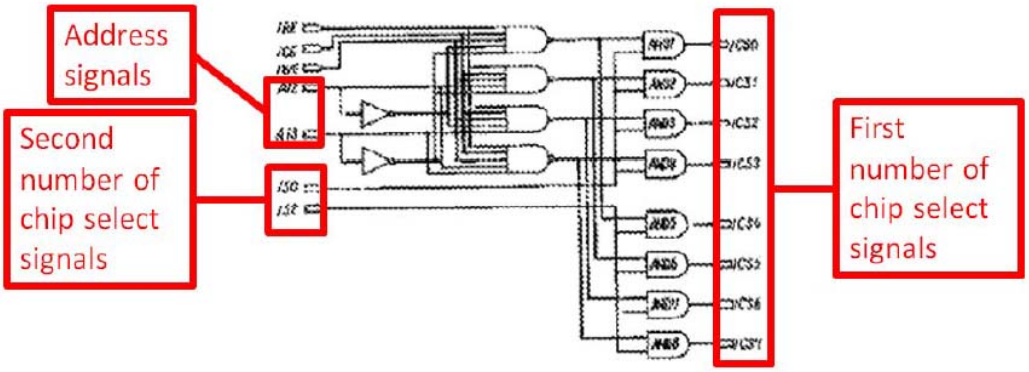

Figure 2 is a schematic of the bank control unit of Takeda.

As shown in Figure 2 above, the signals on the left side of the bank control unit are received from "outside the module" while the signals on the right are generated to control the plurality of banks on the memory module. Ex. 1004 ¶ 5.

2. Overview of JEDEC

JEDEC is a product datasheet describing electrical requirements for DDR SDRAM dual in-line memory modules (DIMMs) as existed in 2002, and illustrates the configuration of the DDR memory and data signals lines, data strobe lines, row/column address signals, bank address signals, and chip select signals. Ex. 1006, 6, 13.[4] JEDEC discloses a memory module that includes a phase-locked loop (PLL) device. Ex. 1006, 17, 29. The PLL of JEDEC directly provides the clock signal to the SDRAM memory devices. *Id.* at 17.

[4] Page numbers in the upper right of Ex. 1006 are styled "Page 4.20.4–__."

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3. Overview of Connolly

Connolly aims to reduce the capacitance load of the memory chips on the bus: "[w]hat is needed in order to better utilize less expensive RAM chips in systems with otherwise limited memory expansion is a way to minimize data line capacitance loading so that oversize memory modules with banks of RAM chips can be added to the system." Ex. 1007, 1:48–53. In order to reduce this capacitive loading, Connolly provides "a two-part solution to reducing data line capacitance to an acceptable system limit." *Id.* at 1:63–64. First, Connolly provides, 1:67–2:4. switches between the memory chips on a module: "DRAMs 900-1 to 900-10, preferably SDRAMs, are coupled through bit switches 909-1 to 909-10 as controlled by ASIC 910 (corresponding to ASICs 310 and 410 of Figure 1). *Id.* at 5:7–13; Fig. 6A; 1:67–2:4. "The second part of the solution according to the invention is logic generating a signal that enables the bus switches. The logic may be in an application specific integrated circuit (ASIC)." *Id*. at 2:20–23.The memory chips in Connolly are arranged within banks of memory. Ex. 1007, Fig. 1.

An illustration of banks of memory shown in Figure 1 is reproduced below (cropped and with annotations by Petitioner) .

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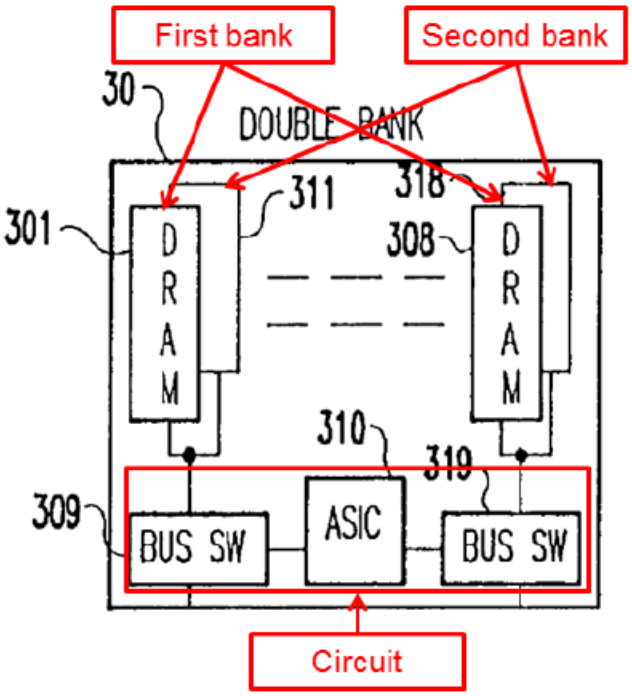

Annotated Figure 1 above is a schematic of the multibank DIMMs of Connolly showing two banks.

4. *Patent Owner's Request to Exclude Petitioner's Reply and Jagannathan Supplemental Declaration.*

Patent Owner seeks to exclude Petitioner's Reply and the Supplemental Declaration of Dr. Jagannathan (Ex. 1029). Paper 25; PO Post Hrg Br. Patent Owner contends Petitioner's Reply adds a new theory of how the combination of Takeda, JEDEC, and Connolly teaches or suggests the elements of these claims. *Id*. Specifically, Patent Owner argues that the Petition asserted the output chip-select signal of Takeda was itself "the logic signal" to enable operation of bit-switches, but the Reply instead asserted for the first time that Takeda's chip-select signal merely generated a new logic signal, which in turn enabled operation of bit-switches:

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> In its Reply, Petitioner exceeded the scope of the Patent Owner Response. Rather than directly address the inoperability of the original combination theory, Petitioner introduced a new combination theory: using an output chip-select signal <u>to generate a new logic signal</u> to enable bit-switches, via new logic circuitry.

Paper 25, 1; s*ee* PO Post Hrg Br. 1–5. Patent Owner focuses on paragraph 113 of the first Jagannathan Declaration (Ex. 1002), which states:

> Moreover, since Connolly teaches a logic element to enable the bit switches, one of ordinary skill would find it obvious to use the chip-select signals output from the Takeda bank-control unit as the logic signal to enable the bit switches. Thus, when a chip-select output from the bank control unit is used to enable a particular DDR SDRAM device, it is also used to enable the bit switch inline with data signal lines from that DDR SDRAM device. The bit-switches from the data lines of the non-selected SDRAM devices would then isolate those data signal lines from the computer system.

Ex. 1002 ¶ 113. According to Patent Owner, the first sentence of the above-quoted section of paragraph 113 states that one of ordinary skill would "use the chip-select signals output from the Takeda bank-control unit *as the logic signal to enable* the bit switches" (emphasis added). Paper 25, 1; PO Post Hrg Br., 2–3. Patent Owner asserts that Petitioner's Reply improperly recasts the combination by arguing therein that the chip select signal is used only "'to determine the enable input' to the bit switches." Paper 25, 2 (citing Pet. Reply 3); PO Post Hrg Br. 5.

Petitioner, in rebuttal, points to the following sentence of paragraph 113, which states the chip select signal "is *also used to enable* the bit switch" (emphasis added). Paper 27, 2; Pet. Post Hrg Br. 4. Petitioner contends that its "combination and rationale has remained consistent

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throughout the proceeding," noting the Petition "explicitly set forth the argument that the chip-select signals are used to generate the switch enable signals." Pet. Post Hrg Br. 3 (citing Pet. 35–36). At oral hearing, Petitioner acknowledged that the first sentence in the above-quoted section of paragraph 113 was "inartfully" drafted. Tr. 29:21–24.

Petitioner further contends Patent Owner had notice of Petitioner's theory and opportunity to address the issue, because of Dr. Jagannathan's testimony at deposition, which occurred ten days before Patent Owner filed its Response. Pet. Post Hrg Br. 7. Dr. Jagannathan testified that the chip select signal is used to determine the enable input to the bit switches. *Id*. at 7–9 (citing Ex. 2002, 187:22–188:10, 218:6–17). At oral hearing, Patent Owner acknowledged it was aware of Dr. Jagannathan's chip select signal explanation no later than the deposition, which preceded its Response by ten days. Tr. 43:9–44:1.

We have reviewed the parties' contentions on this issue, and exercise our discretion to determine that Petitioner's Reply and the Jagannathan Supplemental Declaration will not be excluded. We find that, although they may be "inartfully" drafted, the first Jagannathan Declaration and Petition sufficiently outlined Petitioner's position on the function of the chip select signal, namely, that the chip select signal was not itself the logic signal enabling operation of bit-switches. We further find that Petitioner's Reply and the Supplemental Jagannathan Declaration did not present an entirely new rationale of unpatentability based on Takeda, JEDEC, and Connolly. *Cf. Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369–70 (Fed. Cir. 2016) (affirming Board's exclusion of reply brief and

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Declaration that changed unpatentability theory to "an entirely new rationale").

Moreover, there is no dispute that Patent Owner was aware of Petitioner's position by no later than the Jagannathan deposition, which preceded Patent Owner's Response by ten days. Patent Owner could have addressed Petitioner's chip select signal contention, procedurally or substantively, in its Response, but chose to raise the issue only after Petitioner filed its Reply and Supplemental Jagannathan Declaration. Accordingly, Patent Owner had notice of Petitioner's position and an opportunity to refute that position in its Response.

5. Analysis

As to claims 1 and 24, Petitioner first argues that the combination teaches or suggests "a memory module configured to be operationally coupled to a computer system" and a "method of operating" such a memory module. In Takeda, the circuit "convert[s] drive signals from outside the module, which are sent in order to control the plurality of banks, to signals for controlling the plurality of banks." Pet. 34 (citing Ex. 1004 ¶ 5). Petitioner then explains that Takeda discloses a circuit that is mounted on a memory module. *Id*. at 35 (citing Ex. 1002 ¶ 61). Petitioner also contends that JEDEC discloses a phase-lock loop device. *Id*. at 38–39 (citing Ex. 1006, 29–35; Figure (on page 17); Ex. 1002 ¶¶ 45–47, 66, 111–112). According to Petitioner, Takeda discloses "a plurality of banks comprising a plurality of current-generation SDRAMs . . ." (*Id.* at 35 (citing Ex. 1004 ¶ 5)), where the "banks" disclosed in Takeda are, according to Petitioner, the same as the claimed "ranks." *Id.* (citing Ex. 1002 ¶ 56). Petitioner asserts that "[a]lthough Takeda describes the use of SDRAM circuits, a PHOSITA

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[person of ordinary skill in the art] would readily understand that the teachings of Takeda could be applied to any synchronous memory architecture, which includes a 'DDR memory circuit.'" *Id.* at 22.

Petitioner then argues that Takeda discloses the use of 4 banks (ranks): D0–D15; D16–D31; D32–D47; and D48–D63, with each bank (rank) selected using pairs of chip select signals selected from CS0–CS7 (a first number of chip select signals). Pet. 37 (citing Ex. 1004, 11–13; Ex. 1002 ¶¶ 55–59). Petitioner states that each SDRAM of a selected bank would operate concurrently to output data on the data buses DQ0 – DQ63 (defining the bit width of the selected bank). *Id*. (citing Ex. 1002 ¶¶ 58–60). Thus, according to Petitioner, it would be obvious to a PHOSITA that the DDR memory circuits "are configured to be activated concurrently with one another . . . . in response at least in part to a first number of DDR chip select signals." Petitioner further asserts the circuit of Takeda "receiv[es] a set of signals comprising address signals" and a "second number of [] chip select signals." *Id*. at 37–38.

Petitioner then argues that Connolly teaches a circuit that can "selectively isolate" a load because Connolly provides switches between the memory chips on a module to reduce (i.e., isolate) the capacitive load on the bus. Pet. 41. As illustrated in Figure 6A, the "DRAMs 900-1 to 900-10, preferably SDRAMs, are coupled through bit switches 909-1 to 909-10 as controlled by ASIC 910 (corresponding to ASICs 310 and 410 of Fig. 1)." *Id.* (citing Ex. 1007, 1:67–2:4; 5:7–13). Connolly uses switches to selectively electrically couple a memory device (memory circuits of at least one rank) and its associated load to the computer system and decouple other memory devices (memory circuits of at least one rank) and their associated

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loads from the computer system, thereby isolating the unselected memory devices to reduce the capacitive load of the memory chips on the data bus: "[w]hat is needed in order to better utilize less expensive RAM chips in systems with otherwise limited memory expansion is a way to minimize data line capacitance loading so that oversize memory modules with banks of RAM chips can be added to the system." Pet. 52 (citing Ex. 1007, 1:48–53).

Petitioner asserts that Connolly discloses that the operation of its switches (field effect transistors, or FETs) is responsive at least in part to the set of signals: "As shown in the block diagram of Figure 3A, the ASIC 60 (corresponding to ASICs 310 and 410 of Figure 1) receives the system's RAS and CAS signals, determines the READ/WRITE state of the memory from the RAS and CAS signals and generates therefrom, an RC_SELECT signal to the enable inputs of bus switches 61 and 62." *Id.* at 41 (citing Ex. 1007, 4:12–17). Thus, Connolly's FETs are controlled by signals from the ASIC, which in turn are generated based on a received set of input signals. *Id.*

According to Petitioner, in Takeda, the shared data bus line (DQ0-3) connects to memory chips D0, D16, D32, and D48, with each memory chip in a different bank. Pet. 41. Since each chip shares the same data bus, each chip may be isolated from one another, using the FET switches taught by Connolly. *Id.* When this is performed for each row of chips in Takeda, an entire bank of chips is isolated. Ex. 1002 ¶¶ 97, 113. Because Connolly already determines the switch on/off state based on signals related to the operation of the memory chips, it would have been obvious to a PHOSITA that the switches of Connolly would operate based at least on the generated chip select signals to isolate certain memory devices (memory circuits). Pet.

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15 (citing Ex. 1002 ¶ 113). The FET enabled signals of Connolly are activated relative to which chip select signals are activated (e.g., the CS0-CS7 generated from the logic element of Takeda). *Id.* (citing Ex. 1002 ¶ 113).

Finally, according to Petitioner, the memory module circuit of Takeda "generat[es] the first number of [DDR] chip-select signals in response to at least in part . . . . the address signals, and the second number of DDR chip-select signals." *Id.* at 42. As shown in Figure 2 from Takeda, the logic circuitry generates the first number of chip-select signals at least in part based on the address signals (A12 and A13) and the second number of chip-select signals (S0 and S2). *Id.* (citing Ex. 1002 ¶¶ 59–60). Petitioner admits that Takeda does not explicitly disclose that the generation of the first number of chip-select signals is in response in part to "the phase-locked clock signals." According to Petitioner, however, the timing diagram of Takeda shown in Figure 3 illustrates how each of the signal transitions is influenced by the clock signal (CLK). *Id.* (citing Ex. 1002 ¶ 62). Petitioner asserts it would be obvious to a PHOSITA that the clock signal could be improved to be a phase-locked clock signal as shown in JEDEC and discussed above. Petitioner, therefore, concludes that the combination of Takeda and JEDEC discloses that the generation of the first number of chip-select signals can additionally be in response to the phase-locked clock signals of JEDEC. *Id.* (citing Ex. 1002 ¶ 112.)

According to Petitioner and the testimony of its Declarant Dr. Jagannathan, a person of ordinary skill in the art would have been motivated to combine the teachings of Takeda and JEDEC, because Takeda discloses that JEDEC documents are used to describe memory module configurations,

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and a PHOSITA would have been motivated to apply the known technique of phase locking clock signals as taught in JEDEC to the known memory circuit of Takeda to yield the predictable result of providing timing signals to the elements of the memory module. Pet. 26 (citing Ex. 1004 ¶ 2; Ex. 1006, 17, 29; Ex. 1002 ¶¶ 45–46, 99, 111–112). Additionally, we credit the testimony of Dr. Jagannathan that a person of ordinary skill in the art would have had reason to combine the teachings of Takeda, JEDEC, and Connolly, which all relate to memory devices, such as DIMMS and describe isolating memory device loads. *See* Ex. 1002 ¶¶ 42, 45–46, 96–98, 111–114.

As described above, Petitioner contends that Connolly's switch enable signals are activated "relative to which [of Takeda's] chip select signals are activated." Pet. at 35–36. Petitioner explains:

> [T]he combination of Takeda, JEDEC, and Connolly suggests using a chip select signal to determine the enable input to the bit switches of Connolly. Specifically, Takeda uses the chip select signal (CS0–CS7) to select a particular rank of memory devices. It would have been obvious to a POSITA that the chip select signals would also be used to determine the enable state of bit switches on the data lines of those memory devices, particularly given Connolly's use of RAS and CAS signals in its logic element.

Pet. Reply 8–9 (citations omitted).

Based on the record before us, we are persuaded by Petitioner's contention that the limitations of challenged claims 1 and, 24 are taught by Takeda, JEDEC, and Connolly, and adopt that contention as our own. First, we are persuaded by Petitioner's reasoning and the evidentiary record as a whole that Connolly discloses that a switch and switch control circuitry are provided on a memory module. We are further persuaded that JEDEC teaches a PLL. We also are persuaded that Takeda discloses a circuit with a

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logic element that is mounted on a memory module and that is electrically coupled to memory ranks made of a plurality of memory devices that one of ordinary skill in the art would recognize could be DDR memory devices. We also are persuaded that the teachings of Connolly could have been implemented using the circuitry disclosed in Takeda so as to selectively isolate a load of the DDR memory devices from a computer system in response at least in part to a set of signal as required in the challenged claims.

Patent Owner argues one of ordinary skill in the art would not have perceived a reasonable expectation of success as to the combination, and, in particular, that the combination exceeds any suggestion of the references, would be inoperable, and beyond the level of skill of a person of ordinary skill in the art (POSITA). PO Resp. 2–18. Petitioner, however, asserts the first two of these arguments are based on Patent Owner's characterization of Takeda's chip select signal also constituting the logic signal enabling bit-switches. Pet. Reply 2–3. According to Petitioner, Takeda, JEDEC, and Connolly do teach or suggest Petitioner's actual contention that the chip select signal is used to determine the enable input to the bit switches. *Id.* Petitioner states:

> Thus, the Petition relies on the concept of selectively activating certain chip select signals, as taught by Takeda and JEDEC, to isolate memory devices using the switches of Connolly. (Petition, pp. 33–34.) Connolly is relied upon primarily for its teaching of using bit switches to isolate data lines, and it would have been obvious for a POSITA to incorporate similar bit switches within the system of Takeda and JEDEC. (Petition, pp. 32–34; Exhibit 1002, Appendix B of Jagannathan I, pp. 11–15; Exhibit 2002, Jagannathan Tr., 185:15–22.) Thus, whether or

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> not Connolly switches at the rank level is moot given the combination proposed by Petitioner.

Id. at 5. We agree with Petitioner contentions, described above, that the references teach the limitations of the challenged claims, and adopt them as our own. We also agree with Petitioner that it has demonstrated the operability of its actual combination for use of Takeda's chip select signal as described above, and adopt Petitioner's contentions in that regard as our own. Pet. *Id.* at 10–13.

As to Patent Owner's argument that such use of Takeda's chip select signal would be beyond the skill level of a person of ordinary skill in the art, Petitioner asserts Connolly does describe using command signals from a memory device to determine the on/off state of the switches. Pet. 41; Pet. Reply 11 (citing Ex. 1005, 4:12–17, Fig. 3; Ex. 2002, 219:1–11; 220:22–221:21; 222:18–224:5; Ex. 1029 ¶ 7)*; see* Tr. 75:4–21. Petitioner adds that, in general, JEDEC specifications, which are expressly referenced in Takeda, provide descriptions of signals used for proper timing operation of memory devices, and more specifically, the JEDEC reference describes a standard for DDR memory devices. Pet. Reply 12 (citing Ex. 1002 ¶¶ 38–40; Ex. 1029 ¶¶ 7, 11–13; Ex. 2002, 219:1–11; 220:22–221:21; 222:18– 224:5).

Petitioner also cites the deposition testimony of Patent Owner's declarant that a person of ordinary skill in the art would understand timing issues for DDR memory devices as described in the JEDEC standards. Pet. Reply 12 (citing Ex. 1029, 31:23–32:1, 33:10–34:3). We also note that, as cited by Petitioner, we rejected a similar argument by a different Petitioner, in related IPR2014-00882, slip op. at 30–31. In summary, we agree with Petitioner that a person of ordinary skill in the art would have possessed the

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requisite skill level to understand usage of Takeda's chip select signal to enable Connolly's bit switch, and adopt Petitioner's contentions in that regard as our own.

Thus, we have also considered Patent Owner's arguments regarding alleged lack of reasonable expectation of success, and Petitioner's arguments in response, and as discussed above, are persuaded by Petitioner's position. PO Resp. 1–23, Pet. Reply 1–13. We agree with and adopt Petitioner's reasoning and find Petitioner has shown sufficiently a reason to combine Takeda, JEDEC, and Connolly, providing articulated reasoning supported by rational underpinning for combining the references. *See KSR Int'l*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). Petitioner's reasoning includes explanations of reasons to combine and the underlying factual bases for one of skill to have done so. We specifically credit the testimony of Dr. Jagannathan, which explains that the combination of Takeda, JEDEC, and Connolly would constitute the use of a known technique to improve a similar device thereby yielding predictable results. Pet. 31–34 (citing Ex. 1002 111–114); *see* Ex. 1029 ¶ 8–12. We give Dr. Jagannathan's testimony substantial weight because it is supported by Takeda, JEDEC, and Connolly's disclosures and what Takeda, JEDEC, and Connolly would have conveyed to a person of ordinary skill in the art at the time of the invention.

Dependent claims 16 and 30 recite "the memory module has attributes and the circuit in the at least one configuration is further configured to store data accessible to the computer system, wherein the data characterizes the memory module as having attributes that are different from the attributes of the memory module." Petitioner asserts JEDEC teaches a serial presence

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detect (SPD) element on the memory module configured to store data accessible to the computer system. Pet. 29 (citing Ex. 1006, 13). Petitioner further asserts JEDEC's SPD element is the same as the SPD device that the '536 Patent describes as a typical component of a memory module. *Id.* (citing Ex. 1001, 18:56–60; Ex. 1002 ¶¶ 48–49). Petitioner also contends that the data stored in the SPD of the memory module of Takeda and JEDEC combined characterizes the memory module as having attributes that are different from the attributes of the memory module. *Id.* This is because, according to Petitioner, Takeda discloses a bank control unit that emulates a two rank memory module to the computer system whereas the actual memory module has four ranks. *Id.*

Thus, Petitioner contends it would have been obvious to a person of ordinary skill in the art that information at least related to the emulated number of ranks must be stored in the SPD so that the memory controller interfaces with the emulated memory organization of the memory module. *Id.* Therefore, according to Petitioner, the information stored in the SPD would characterize the memory module with having different attributes (e.g., two ranks) than the actual attributes of the memory module (e.g., four ranks). *Id*. We agree with Petitioner's contentions and adopt them as our own and, as noted above, find Petitioner has shown sufficiently a reason to combine Takeda, JEDEC, and Connolly, providing articulated reasoning supported by rational underpinning for combining the references. *See* Pet. 28–30, 43.

Dependent claims 17 and 31 further recite "the attributes are selected from a group consisting of: a number of row addresses, a number of column addresses, a number of DDR memory circuits, a data width of the DDR

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memory circuits, a memory density per DDR memory circuit, a number of ranks, and a memory density per rank." Petitioner contends "an SPD as specified in JEDEC stores attributes including data related to row addresses, column addresses, and number of physical banks on the module as identified in the table on page 68 of JEDEC." Pet. 30–31. We agree with Petitioner's contentions as adopt them as our own and, as noted above, find Petitioner has shown sufficiently a reason to combine Takeda, JEDEC, and Connolly, providing articulated reasoning supported by rational underpinning for combining the references. *See* Pet. 30–31, 43.

Therefore, for the foregoing reasons and weighing the evidence as a whole, we conclude that Petitioner has shown by a preponderance of the evidence that claims 1, 16, 17, 24, 30, and 31 would have been obvious over Takeda, JEDEC, and Connolly.

III. CONCLUSION

Based on the evidence and arguments, Petitioner has demonstrated by a preponderance of the evidence that claims 1, 16, 17, 24, 30, and 31 of the '536 Patent would have been obvious over Takeda, JEDEC, and Connolly.

IV. ORDER

For the reasons given, it is

ORDERED that claims 1, 16, 17, 24, 30, and 31 of the '536 Patent are unpatentable; and

FURTHER ORDERED that because this is a final written decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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