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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NETL.018P2C6
	Application Number	
Title of Invention	CIRCUIT FOR MEMORY MODULE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1

Applicant Authority ◉ Inventor ◯ Legal Representative under 35 U.S.C. 117 ◯ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jeffrey	C.	Solomon	

Residence Information (Select One) ◉ US Residency ◯ Non US Residency ◯ Active US Military Service

City	Irvine	State/Province	CA	Country of Residence	US

Citizenship under 37 CFR 1.41(b) US

Mailing Address of Applicant:

Address 1	16 Silver Fir		
Address 2			
City	Irvine	State/Province	CA
Postal Code	92604	Country	US

Applicant 2

Applicant Authority ◉ Inventor ◯ Legal Representative under 35 U.S.C. 117 ◯ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jayesh	R.	Bhakta	

Residence Information (Select One) ◉ US Residency ◯ Non US Residency ◯ Active US Military Service

City	Cerritos	State/Province	CA	Country of Residence	US

Citizenship under 37 CFR 1.41(b) US

Mailing Address of Applicant:

Address 1	12220 Rose Street		
Address 2			
City	Cerritos	State/Province	CA
Postal Code	90703	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NETL.018P2C6
	Application Number	
Title of Invention	CIRCUIT FOR MEMORY MODULE	

Customer Number	20995		
Email Address	efiling@kmob.com	Add Email	Remove Email

Application Information:

Title of the Invention	CIRCUIT FOR MEMORY MODULE		
Attorney Docket Number	NETL.018P2C6	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	23	**Suggested Figure for Publication (if any)**	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☒ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	◯ US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	20995		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	13032470	2011-02-22
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
13032470	Continuation of	12955711	2010-11-29

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NETL.018P2C6
	Application Number	
Title of Invention	CIRCUIT FOR MEMORY MODULE	

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12955711	Continuation of	12629827	2009-12-02	7881150	2011-02-01
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12629827	Continuation of	12408652	2009-03-20	7636274	2009-12-22
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/408652	Continuation of	11/335875	2006-01-19	7532537	2009-05-12
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11/335875	non provisional of	60/645087	2005-01-19		
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11/335875	Continuation in part of	11/173175	2005-07-01	7289386	2007-10-30
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11/173175	non provisional of	60/588244	2004-07-15		
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11/173175	Continuation in part of	11/075395	2005-03-07	7286436	2007-10-23
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11/075395	non provisional of	60/550668	2004-03-05		
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11/075395	non provisional of	60/575595	2004-05-28		
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11/075395	non provisional of	60/590038	2004-07-21		

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

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This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country[i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			○ Yes ◉ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1

If the Assignee is an Organization check here. ☒

Organization Name	NETLIST, INC.		
Mailing Address Information:			
Address 1	51 Discovery, Ste. 150		
Address 2			
City	Irvine	**State/Province**	CA
Country[i]	US	Postal Code	92618
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the **Add** button.

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature				Date (YYYY-MM-DD)	2011-11-01
First Name	Bruce	Last Name	Itchkawitz	Registration Number	47677

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

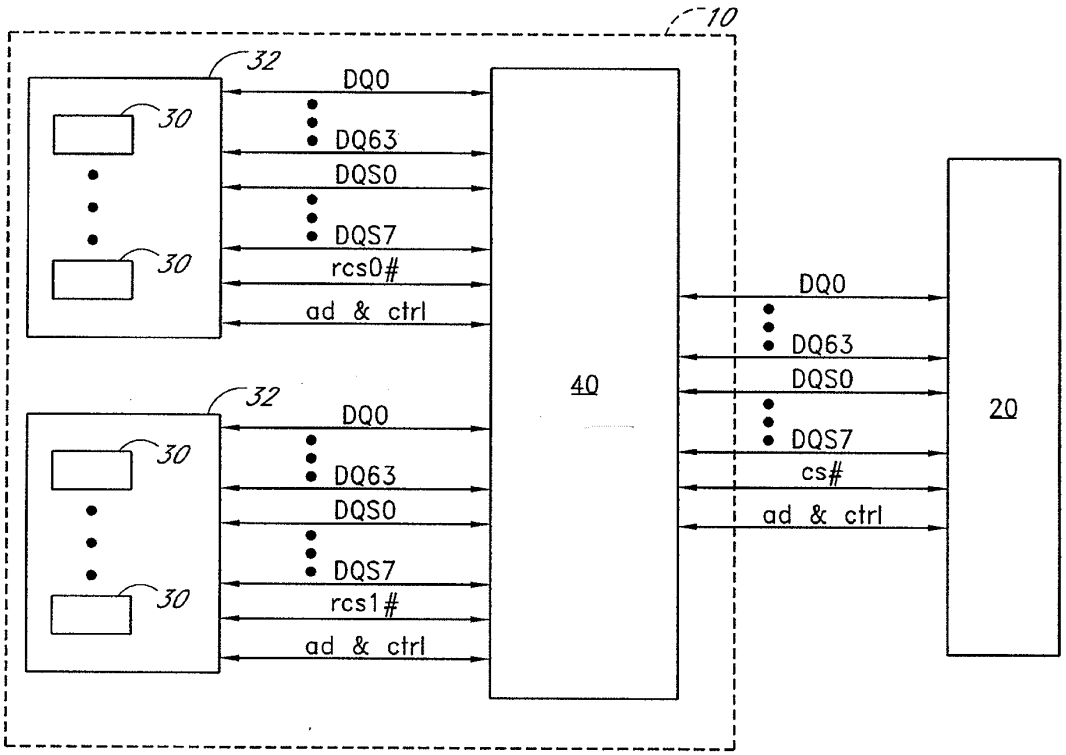

10
32
30
30
DQ0
DQ63
DQS0
DQS7
rcs0#
ad & ctrl
32
30
30
DQ0
DQ63
DQS0
DQS7
rcs1#
ad & ctrl
40
DQ0
DQ63
DQS0
DQS7
cs#
ad & ctrl
20

FIG. 1

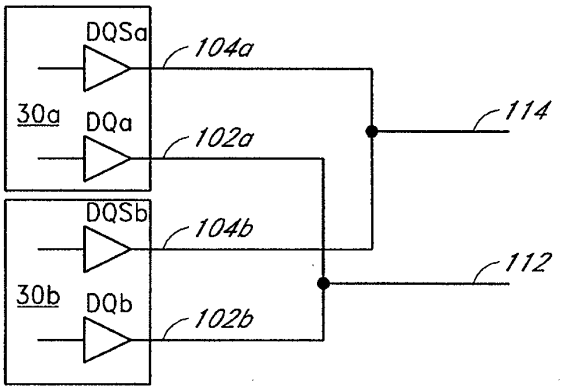


FIG. 2

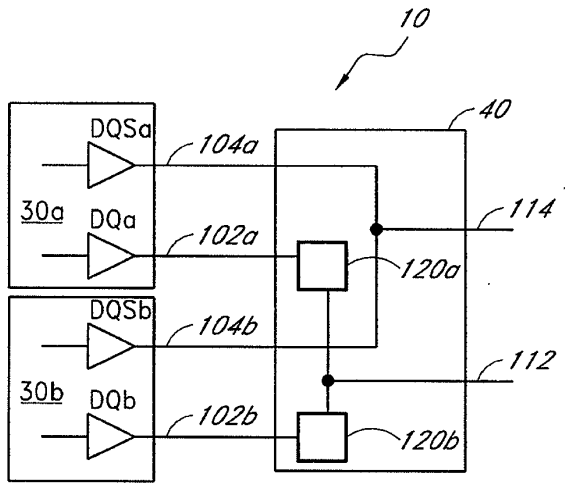

10
40
DQSa
104a
30a
DQa
102a
114
120a
DQSb
104b
112
30b
DQb
102b
120b

FIG. 3A

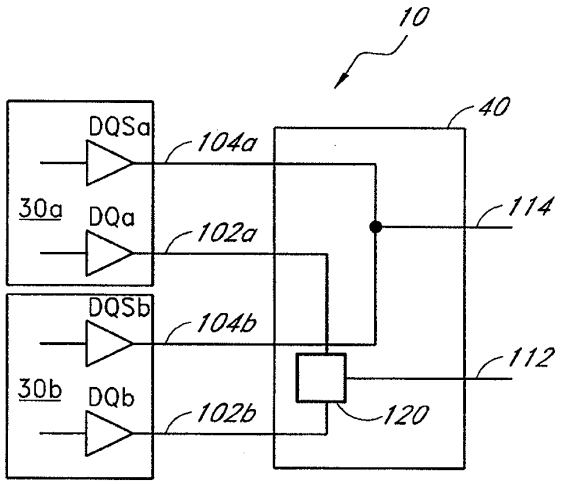

10
40
DQSa
104a
30a
DQa
102a
114
DQSb
104b
112
30b
DQb
102b
120

FIG. 3B

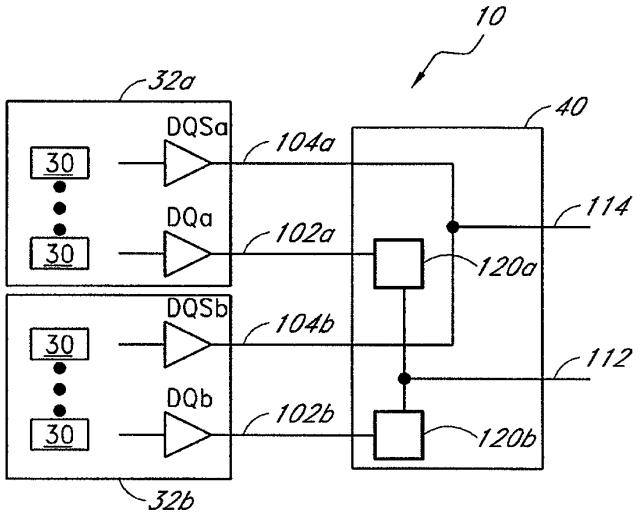

10
32a
40
DQSa
104a
30
DQa
102a
114
120a
30
DQSb
104b
30
112
DQb
102b
30
120b
32b

FIG. 4A

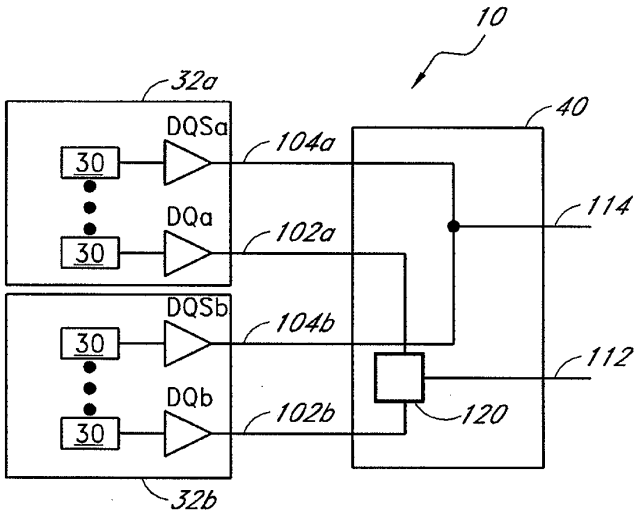

10
32a
40
DQSa
104a
30
DQa
102a
114
30
DQSb
104b
30
112
DQb
102b
120
30
32b

FIG. 4B

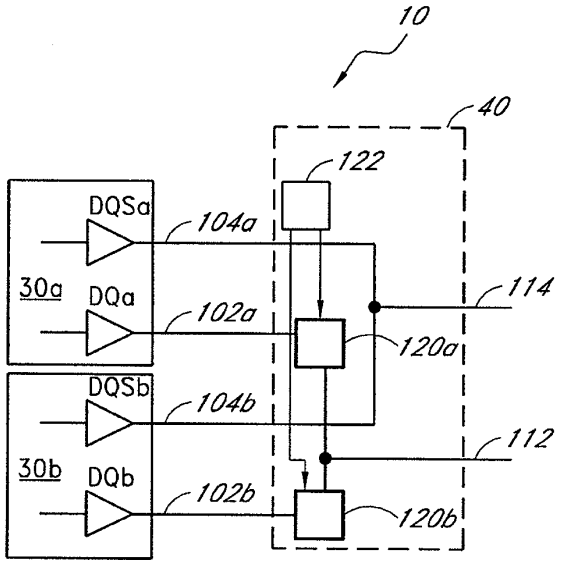

10
40
122
DQSa
104a
30a
DQa
102a
114
120a
DQSb
104b
112
30b
DQb
102b
120b

FIG. 5A

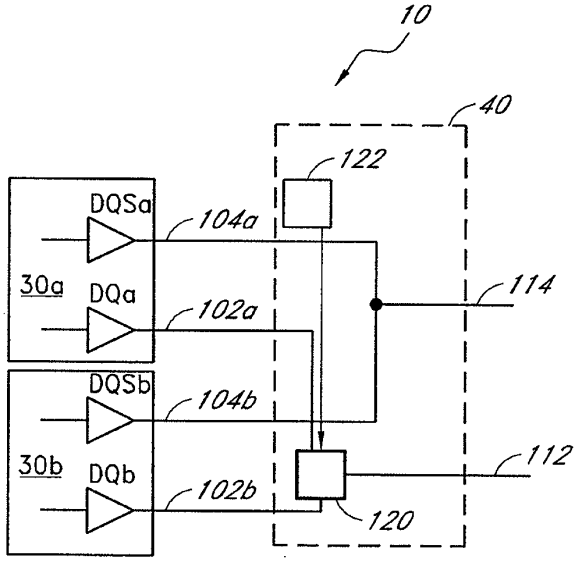

10
40
122
DQSa
104a
30a
DQa
102a
114
DQSb
104b
30b
DQb
102b
112
120

FIG. 5B

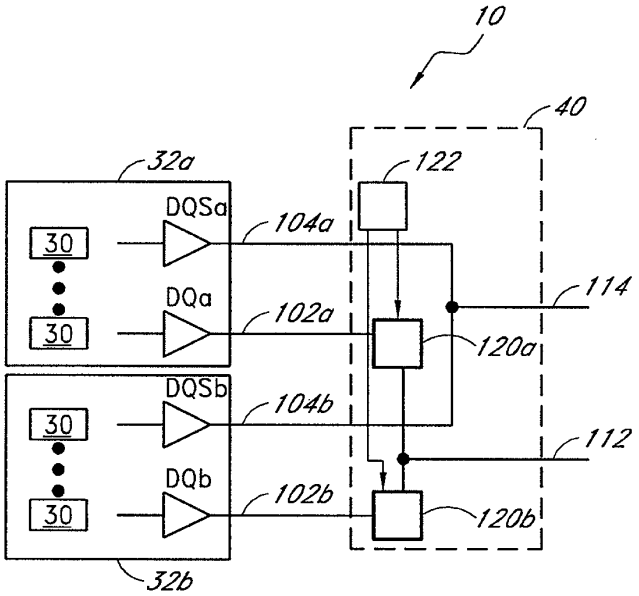

10
40
32a
122
DQSa
104a
30
DQa
102a
114
30
120a
DQSb
104b
30
112
DQb
102b
30
120b
32b

FIG. 5C

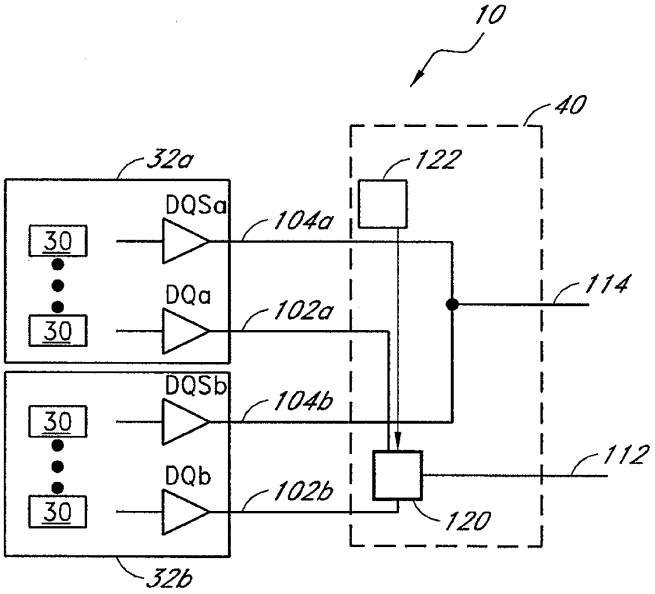

10
40
32a
122
DQSa
104a
30
114
DQa
102a
30
DQSb
104b
30
112
DQb
102b
30
120
32b

FIG. 5D

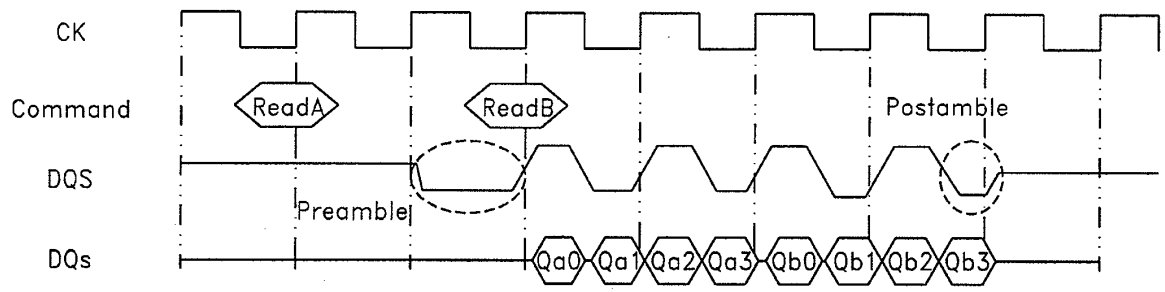

CK
Command
ReadA
ReadB
Postamble
DQS
Preamble
DQs
Qa0
Qa1
Qa2
Qa3
Qb0
Qb1
Qb2
Qb3

FIG. 6A

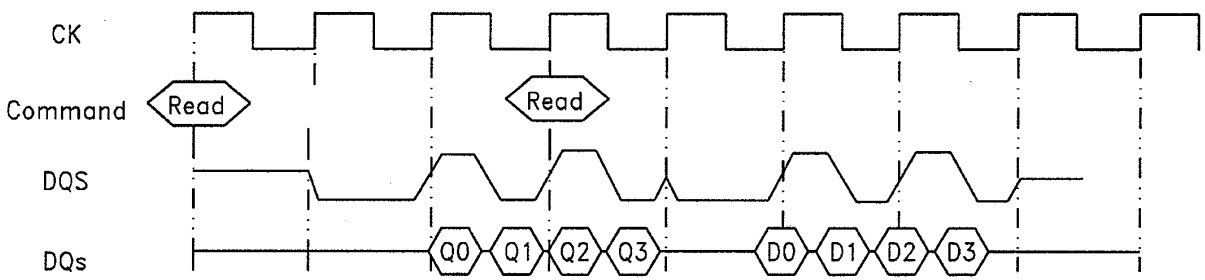

CK
Command
Read
Read
DQS
DQs
Q0
Q1
Q2
Q3
D0
D1
D2
D3

FIG. 6B

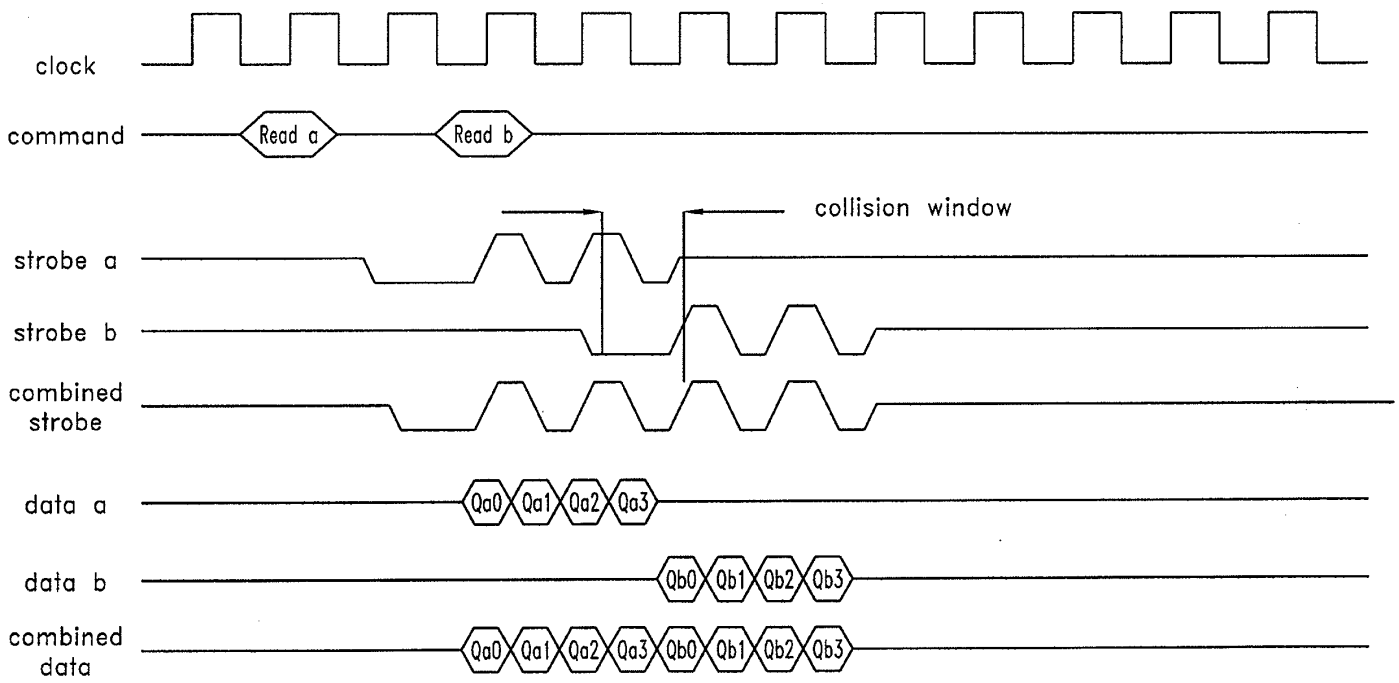

clock
command
Read a
Read b
collision window
strobe a
strobe b
combined strobe
data a
Qa0
Qa1
Qa2
Qa3
data b
Qb0
Qb1
Qb2
Qb3
combined data
Qa0
Qa1
Qa2
Qa3
Qb0
Qb1
Qb2
Qb3

FIG. 7

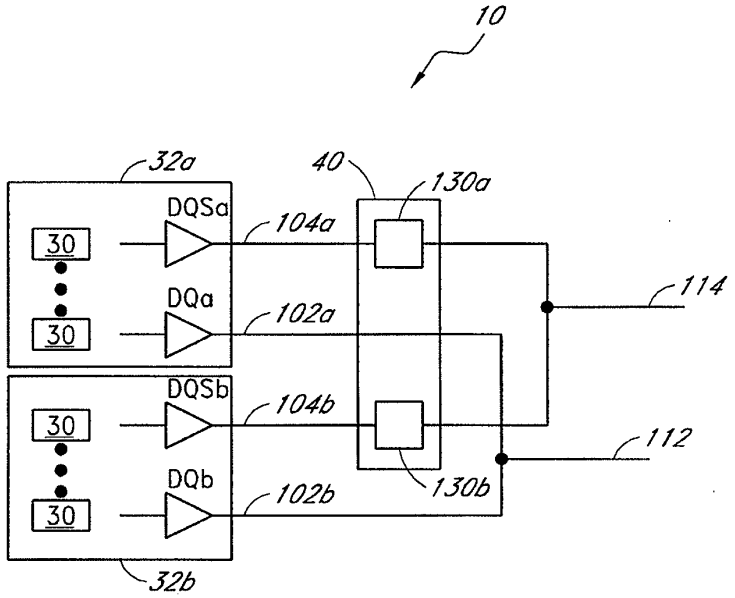

10
32a
40
130a
DQSa
104a
30
30
DQa
102a
114
DQSb
104b
30
30
112
DQb
102b
130b
32b

FIG. 8A

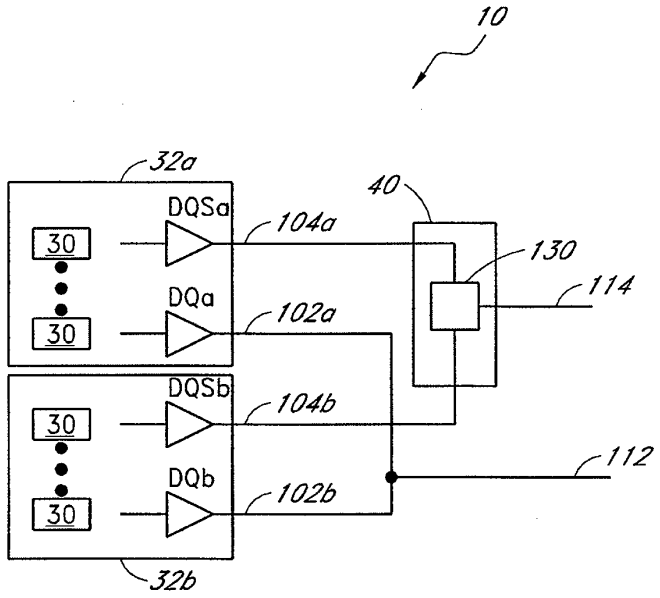

10
32a
40
DQSa
104a
30
30
130
114
DQa
102a
DQSb
104b
30
30
112
DQb
102b
32b

FIG. 8B

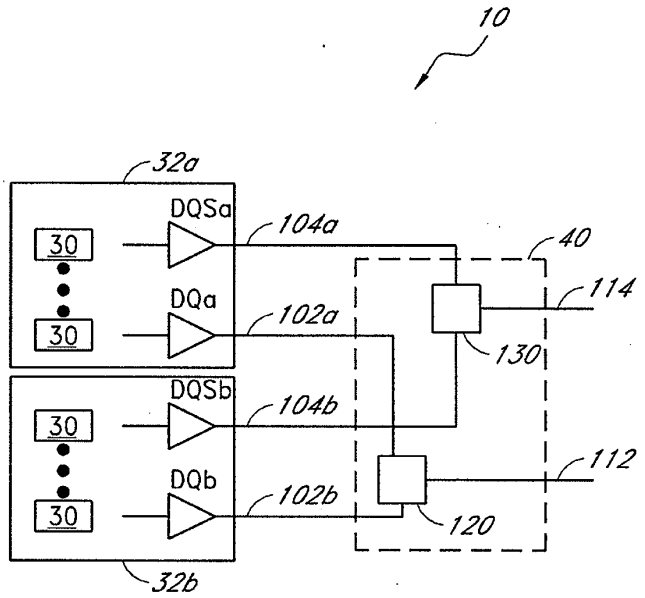

10
32a
DQSa
104a
40
30
114
DQa
102a
30
130
DQSb
104b
30
112
DQb
102b
30
120
32b

FIG. 8C

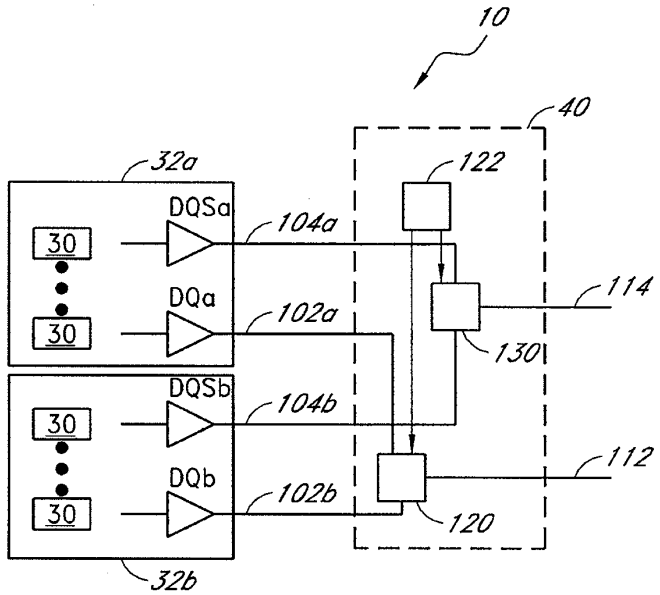

10
40
32a
122
DQSa
104a
30
114
DQa
102a
30
130
DQSb
104b
30
112
DQb
102b
30
120
32b

FIG. 8D

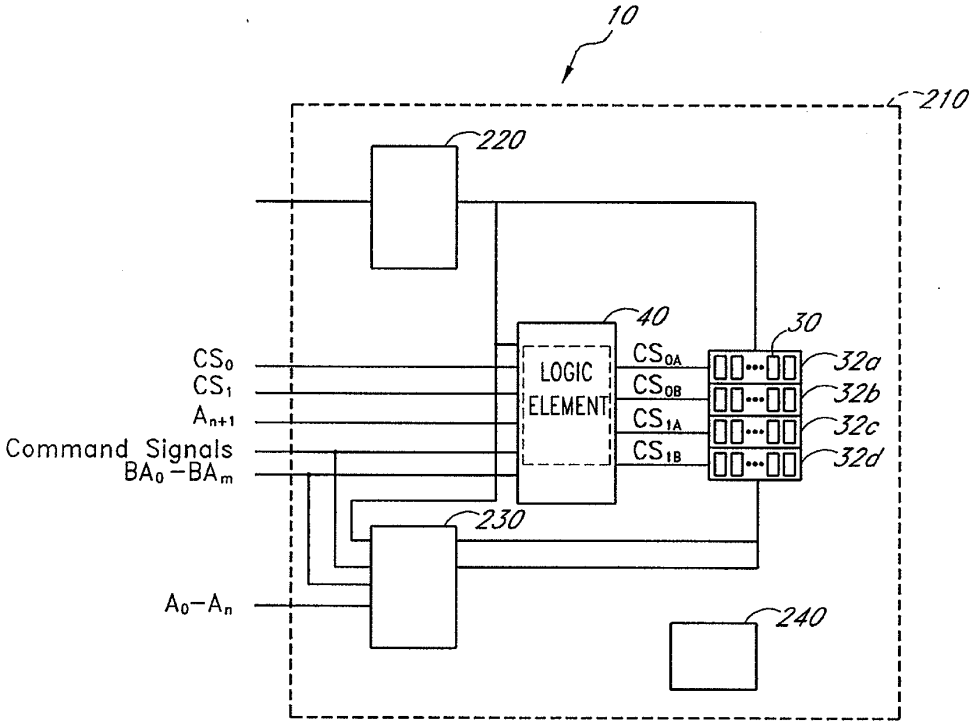

10
210
220
40
30
LOGIC ELEMENT
CS0
CS1
An+1
Command Signals
BA0 – BAm
CS0A
CS0B
CS1A
CS1B
32a
32b
32c
32d
230
A0–An
240

FIG. 9A

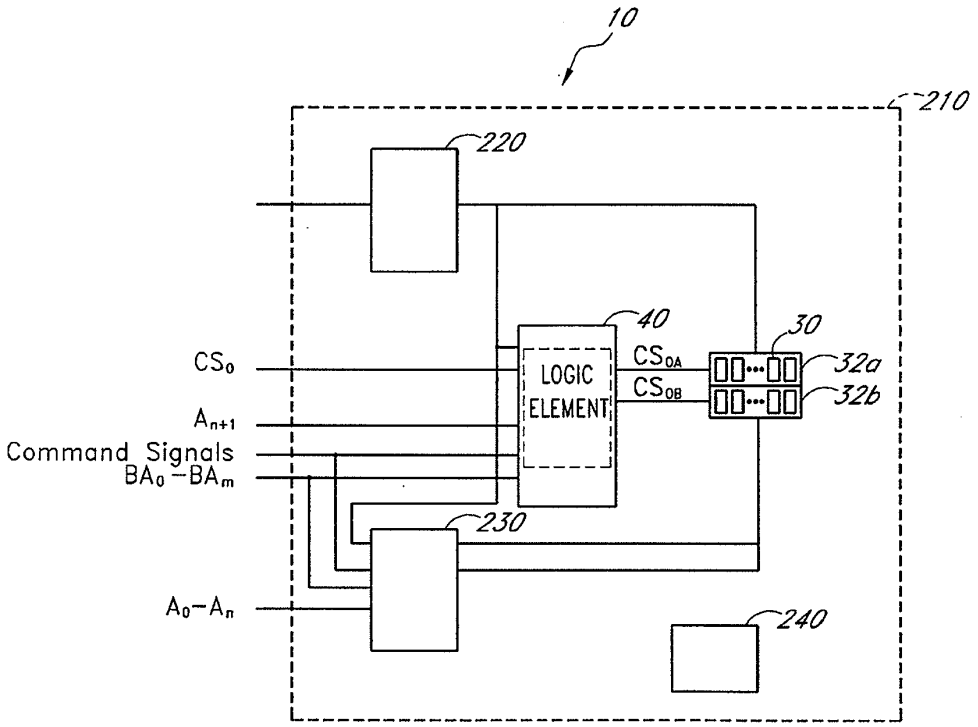

10
210
220
40
30
LOGIC ELEMENT
CS_{0A}
CS_{0B}
32a
32b
CS_0
A_{n+1}
Command Signals
$BA_0 - BA_m$
230
$A_0 - A_n$
240

FIG. 9B

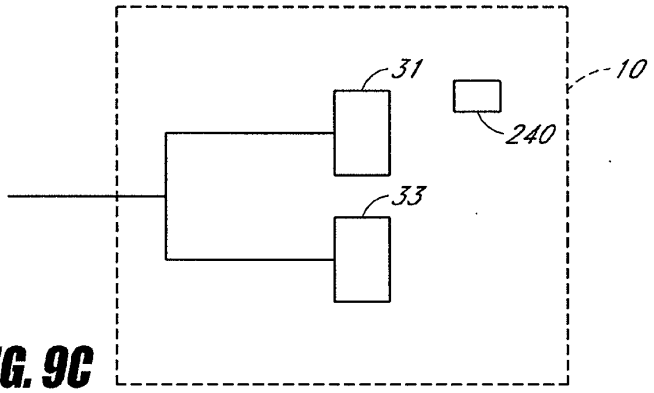


FIG. 9C

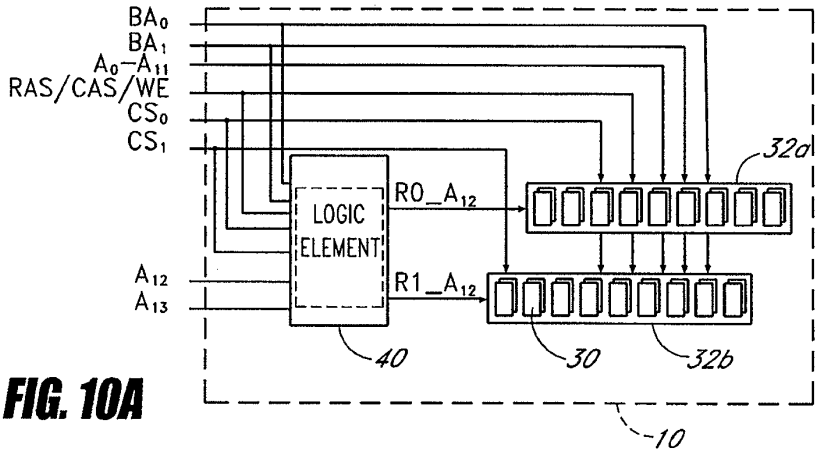


FIG. 10A

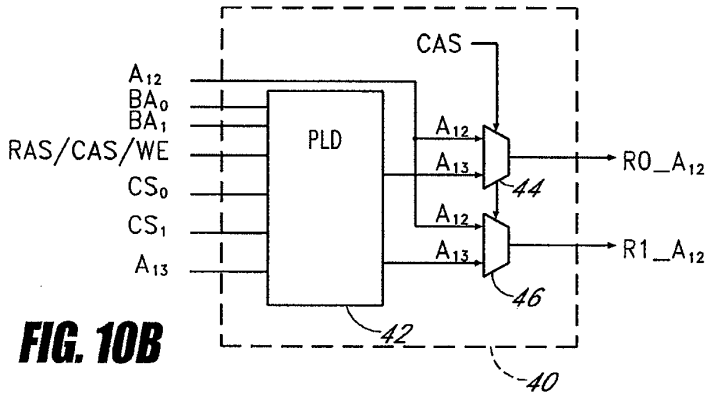


FIG. 10B

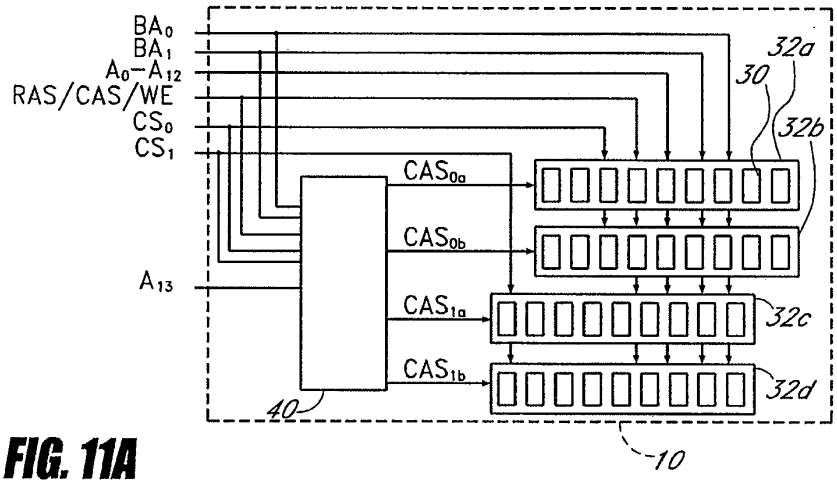


FIG. 11A

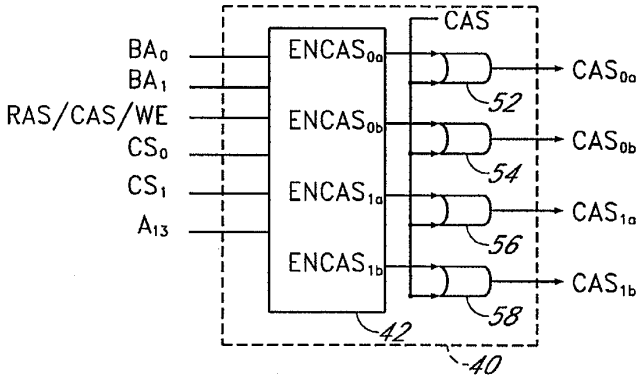


FIG. 11B

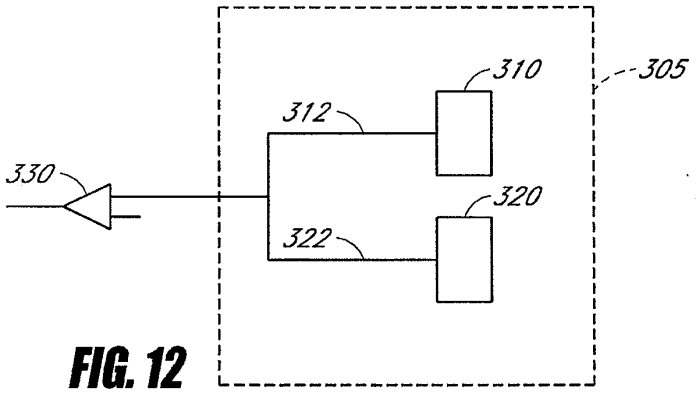


FIG. 12

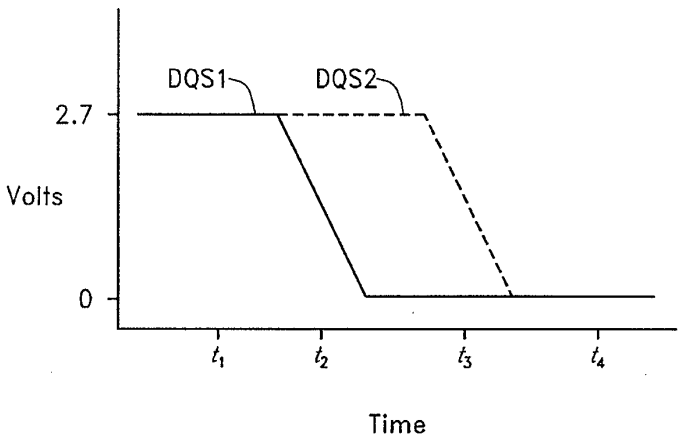


FIG. 13

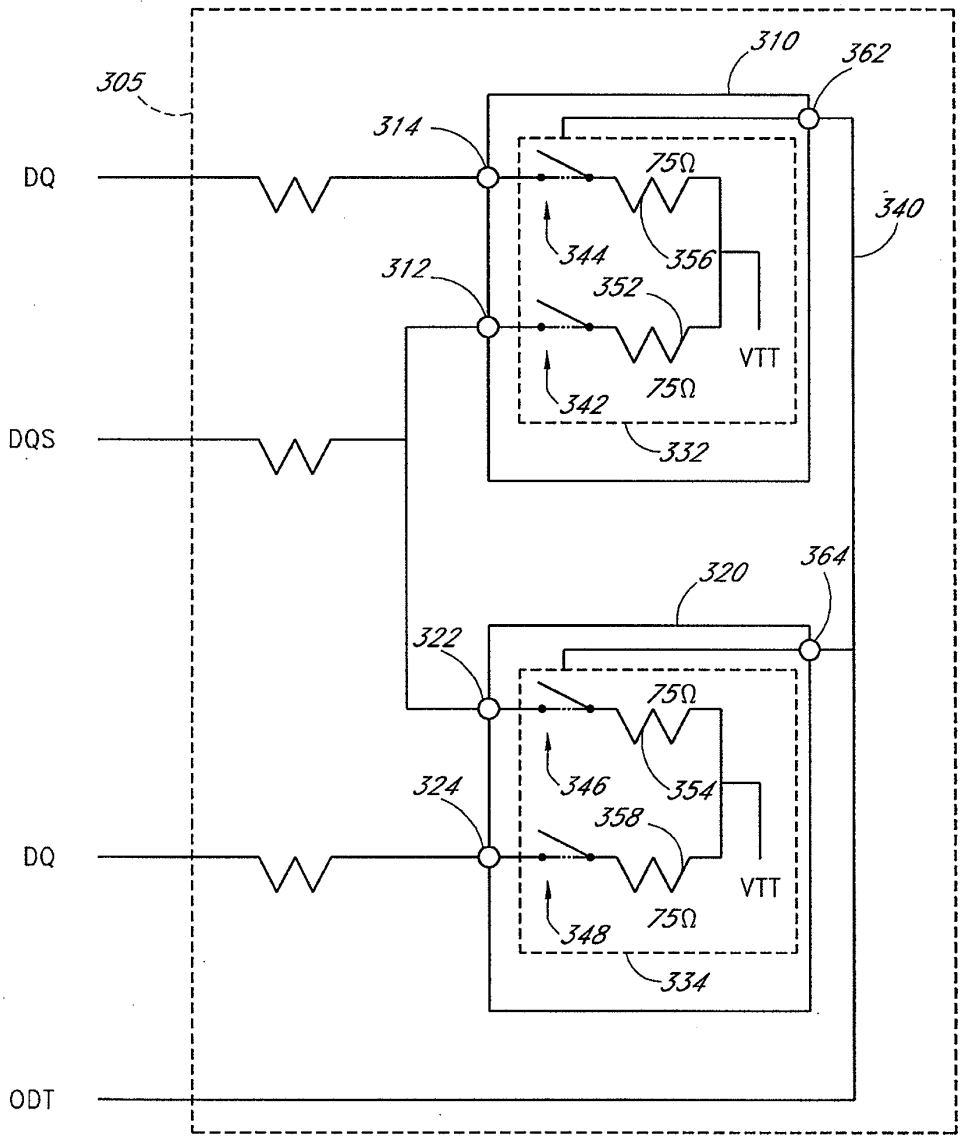

305
310
362
314
DQ
75Ω
340
344
356
312
352
VTT
342
75Ω
DQS
332
364
320
322
75Ω
346
354
324
358
DQ
VTT
348
75Ω
334
ODT

FIG. 14

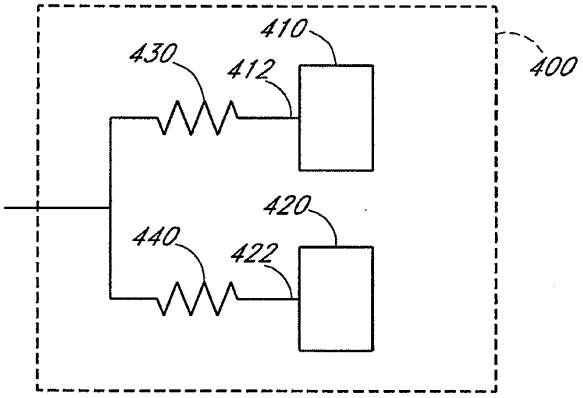


FIG. 15

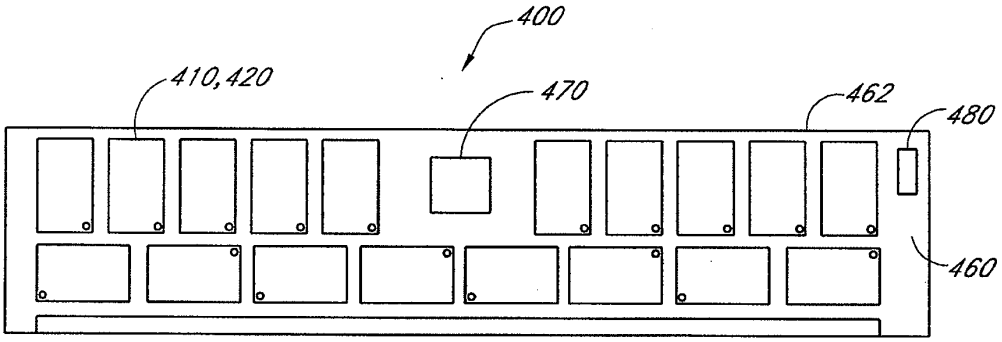


FIG. 16A

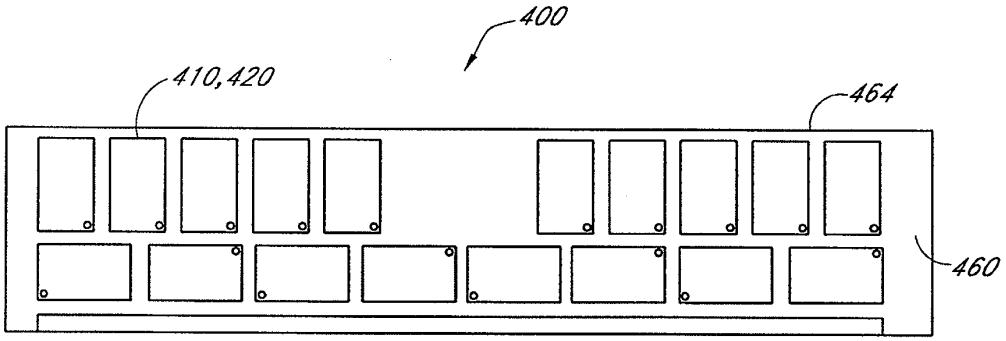


FIG. 16B

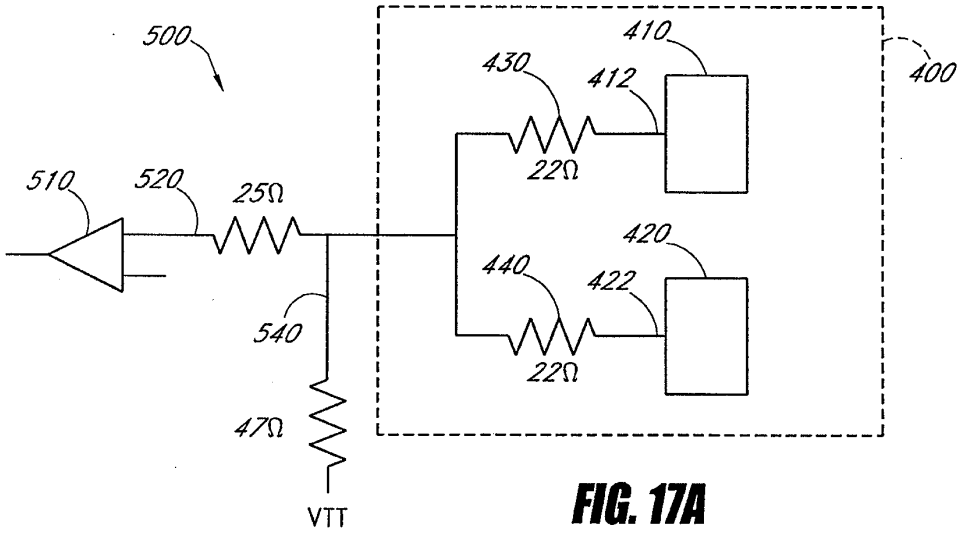


FIG. 17A

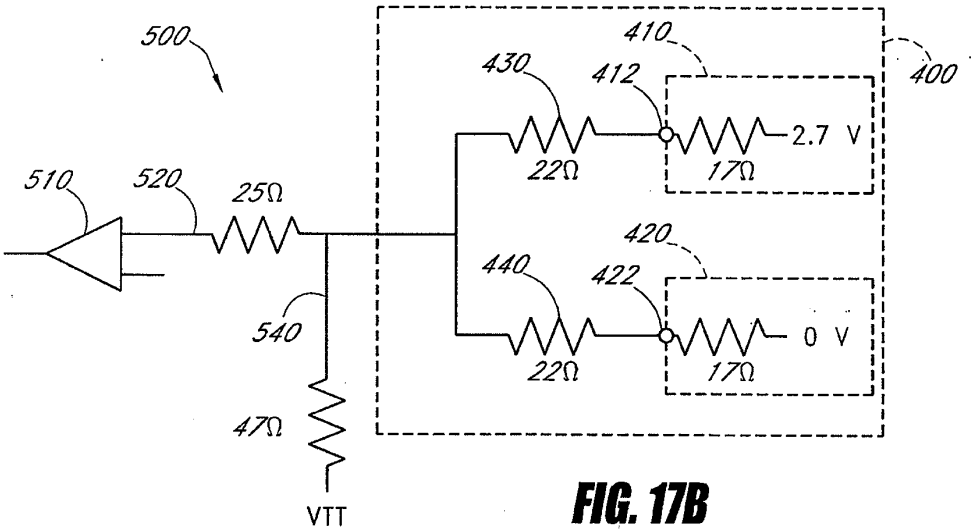
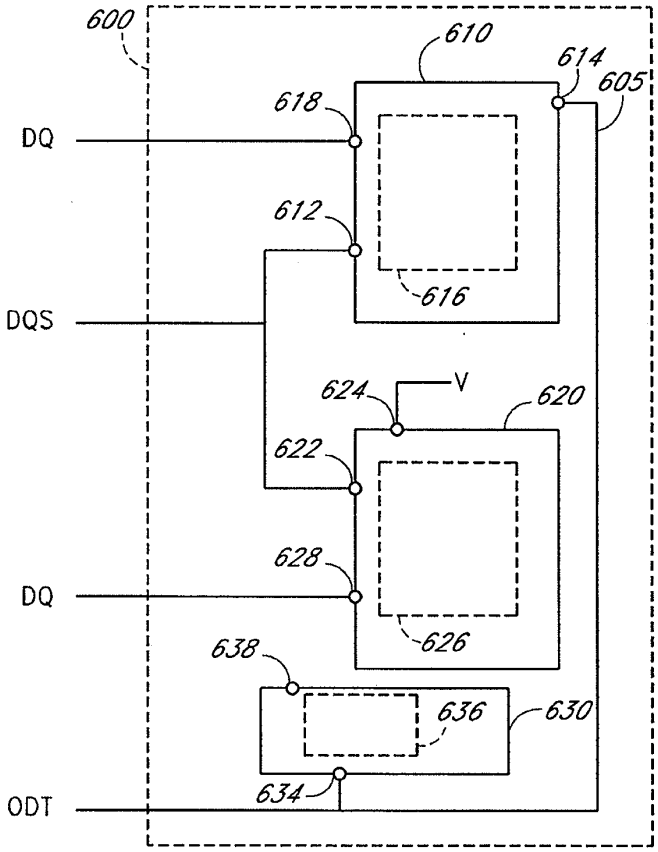


FIG. 17B


600
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DQS
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V
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628
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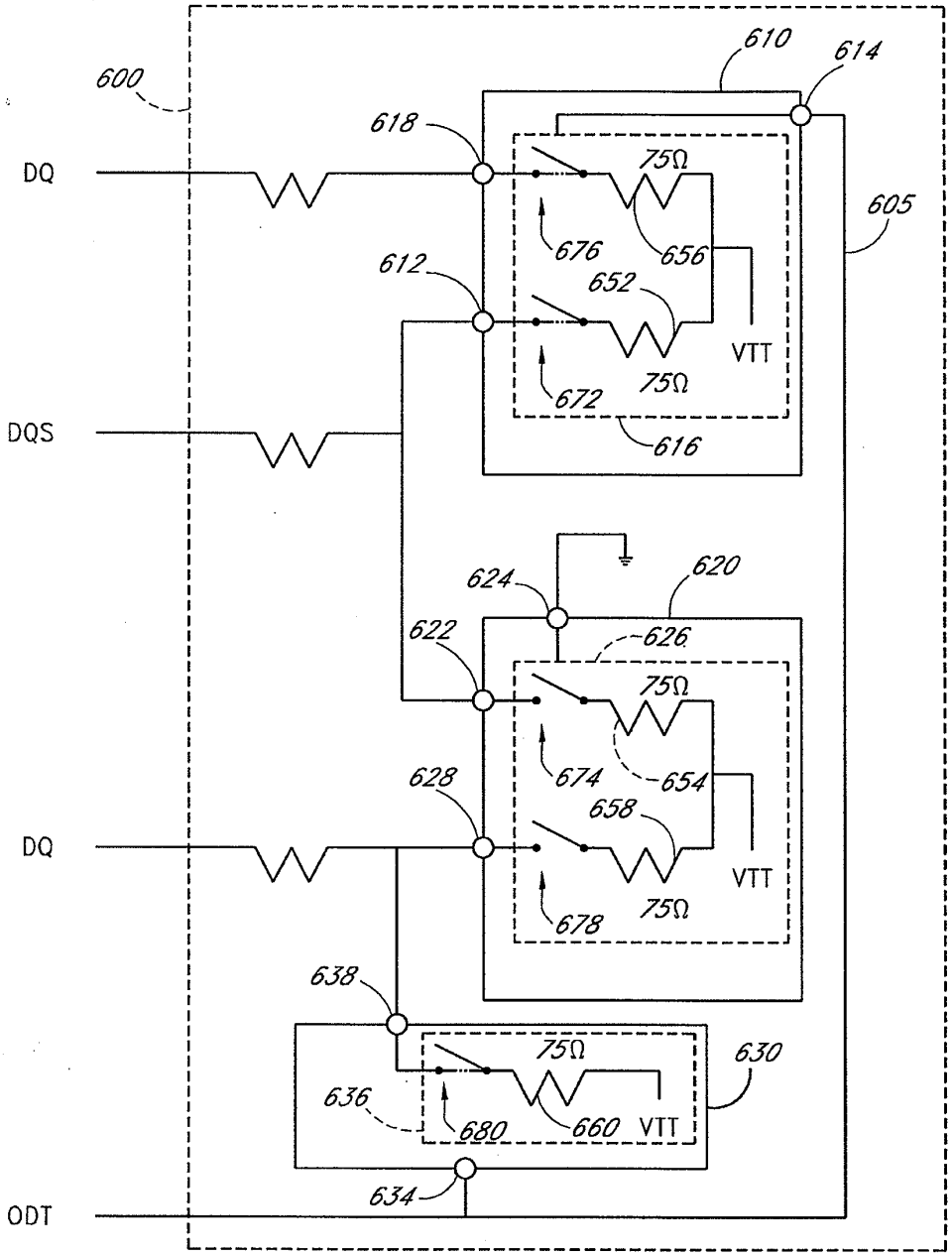
ODT

FIG. 18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620
622
626
75Ω
674
654
628
658
DQ
VTT
678
75Ω
638
75Ω
630
636
680
660
VTT
634
ODT

FIG. 19

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DECLARATION - USA PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are as stated below next to my name;

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled MEMORY MODULE WITH A CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION; the specification of which was filed on January 19, 2006 as Application Serial No. 11/335,875.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims;

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56;

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States applications listed below, and insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56, which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S.A. Applications

Application No.: 11/173,175	Filing Date: 07/01/05	Status: Pending
Application No.: 60/588,244	Filing Date: 07/15/04	Status: N/A
Application No. 11/075,395	Filing Date: 03/07/05	Status: Pending
Application No. 60/550,668	Filing Date: 03/05/04	Status: N/A
Application No. 60/575,595	Filing Date: 05/28/04	Status: N/A
Application No. 60/590,038	Filing Date: 07/21/04	Status: N/A
Application No. 60/645,087	Filing Date: 01/19/05	Status: N/A

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issued thereon.

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Date June 29, 2006

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Citizenship: United States

Mailing Address: Same

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Inventor's signature Jayesh R. Bhakta

Date June 28, 2006

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Mailing Address: Same

Send Correspondence To:
KNOBBE, MARTENS, OLSON & BEAR, LLP
Customer No. 20,995

2486602
033006

CIRCUIT FOR MEMORY MODULE

Cross-Reference to Related Applications

[0001] The present application is a continuation of U.S. Pat. Appl. No. 13/032,470, filed February 22, 2011, which is a continuation of U.S. Pat. Appl. No. 12/955,711, filed November 29, 2010, which is a continuation of U.S. Pat. Appl. No. 12/629,827, filed December 2, 2009 and issued as U.S. Pat. No. 7,881,150, which is a continuation of U.S. Pat. Appl. No. 12/408,652, filed March 20, 2009 and issued as U.S. Pat. No. 7,636,274, which is a continuation of U.S. Pat. Appl. No. 11/335,875, filed January 19, 2006 and issued as U.S. Pat. No. 7,532,537, which claims the benefit of U.S. Provisional Appl. No. 60/645,087, filed January 19, 2005 and which is a continuation-in-part of U.S. Pat. Appl. No. 11/173,175, filed July 1, 2005 and issued as U.S. Pat. No. 7,289,386, which claims the benefit of U.S. Provisional Appl. No. 60/588,244, filed July 15, 2004 and which is a continuation-in-part of U.S. Pat. Appl. No. 11/075,395, filed March 7, 2005 and issued as U.S. Pat. No. 7,286,436, which claims the benefit of U.S. Provisional Appl. No. 60/550,668, filed March 5, 2004, U.S. Provisional Appl. No. 60/575,595, filed May 28, 2004, and U.S. Provisional Appl. No. 60/590,038, filed July 21, 2004. U.S. Pat. Appl. Nos. 13/032,470, 12/955,711, 12/629,827, 12/408,652, 11/335,875, 11/173,175, and 11/075,395 and U.S. Provisional Appl. Nos. 60/550,668, 60/575,595, 60/590,038, 60/588,244, and 60/645,087 are each incorporated in their entirety by reference herein.

Background of the Invention

Field of the Invention

[0002] The present invention relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules.

Description of the Related Art

[0003] Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the processor of the

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computer system. Memory modules typically have a memory configuration with a unique combination of rows, columns, and banks which result in a total memory capacity for the memory module.

[0004] For example, a 512-Megabyte memory module (termed a "512-MB" memory module, which actually has 2^{29} or 536,870,912 bytes of capacity) will typically utilize eight 512-Megabit DRAM devices (each identified as a "512-Mb" DRAM device, each actually having 2^{29} or 536,870,912 bits of capacity). The memory cells (or memory locations) of each 512-Mb DRAM device can be arranged in four banks, with each bank having an array of 2^{24} (or 16,777,216) memory locations arranged as 2^{13} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 64M 8-bit-wide memory locations (actually with four banks of 2^{27} or 134,217,728 one-bit memory cells arranged to provide a total of 2^{26} or 67,108,864 memory locations with 8 bits each) are identified as having a "64Mb x 8" or "64M x 8-bit" configuration, or as having a depth of 64M and a bit width of 8. Furthermore, certain commercially-available 512-MB memory modules are termed to have a "64M x 8-byte" configuration or a "64M x 64-bit" configuration with a depth of 64M and a width of 8 bytes or 64 bits.

[0005] Similarly, a 1-Gigabyte memory module (termed a "1-GB" memory module, which actually has 2^{30} or 1,073,741,824 bytes of capacity) can utilize eight 1-Gigabit DRAM devices (each identified as a "1-Gb" DRAM device, each actually having 2^{30} or 1,073,741,824 bits of capacity). The memory locations of each 1-Gb DRAM device can be arranged in four banks, with each bank having an array of memory locations with 2^{14} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 128M 8-bit-wide memory locations (actually with a total of 2^{27} or 134,217,728 memory locations with 8 bits each) are identified as having a "128Mb x 8" or "128M x 8-bit" configuration, or as having a depth of 128M and a bit width of 8. Furthermore, certain commercially-available 1-GB memory modules are identified as having a "128M x 8-byte" configuration or a "128M x 64-bit" configuration with a depth of 128M and a width of 8 bytes or 64 bits.

[0006] The commercially-available 512-MB (64M x 8-byte) memory modules and the 1-GB (128M x 8-byte) memory modules described above are typically used in

computer systems (e.g., personal computers) which perform graphics applications since such "x 8" configurations are compatible with data mask capabilities often used in such graphics applications. Conversely, memory modules with "x 4" configurations are typically used in computer systems such as servers which are not as graphics-intensive. Examples of such commercially available "x 4" memory modules include, but are not limited to, 512-MB (128M x 4-byte) memory modules comprising eight 512-Mb (128Mb x 4) memory devices.

[0007] The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "x 64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "x 72" organization.

[0008] The memory capacity of a memory module increases with the number of memory devices. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks. For example, a memory module with four ranks has double the memory capacity of a memory module with two ranks and four times the memory capacity of a memory module with one rank. Rather than referring to the memory capacity of the memory module, in certain circumstances, the memory density of the memory module is referred to instead.

[0009] During operation, the ranks of a memory module are selected or activated by address and command signals that are received from the processor. Examples of such address and command signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support one-rank and two-rank memory modules. By only supporting one-rank and two-rank memory modules, the memory density that can be incorporated in each memory slot is limited.

[0010] Various aspects of the design of a memory module impose limitations on the size of the memory arrays of the memory module. Certain such aspects are particularly important for memory modules designed to operate at higher frequencies. Examples of such aspects include, but are not limited to, memory device (e.g., chip) densities, load fan-out, signal integrity, available rank selects, power dissipation, and thermal profiles.

Summary of the Invention

[0011] In certain embodiments, a circuit is configured to be mounted on a memory module configured to be operationally coupled to a computer system. The memory modules has a first number of ranks, each rank of the first number of ranks comprising a plurality of double-date-rate (DDR) memory circuits that are configured to be activated concurrently with one another for receiving and transmitting data having a bit width of the rank in response at least in part to a first number of chip-select signals. The circuit is configurable to receive a set of signals comprising address signals and a second number of chip-select signals smaller than the first number of chip-select signals. The circuit is further configurable to generate phase-locked clock signals, wherein the circuit is configurable to transmit the phase-locked clock signals to the first number of ranks. The circuit is further configurable to selectively isolate a load of at least one rank of the first number of ranks from the computer system in response at least in part to the set of signals. The circuit is further configurable to generate the first number of chip-select signals in response at least in part to the phase-locked clock signals, the address signals, and the second number of chip-select signals.

[0012] In certain embodiments, a method operates a memory module configured to be operationally coupled to a computer system. The memory module has a first number of ranks, each rank of the first number of ranks comprising a plurality of double-data-rate (DDR) memory circuits that are configured to be activated concurrently with one another for receiving and transmitting data having a bit width of the rank in response at least in part to a first number of chip-select signals. The method comprises receiving a set of signals comprising address signals and a second number of chip-select signals smaller than the first number of chip-select signals. The method further comprises using the memory module to generate phase-locked clock signals and transmitting the phase-locked clock signals to the first number of ranks. The method further comprises selectively isolating a load of at least one rank of the first number of ranks from the computer system in response at least in part to the set of signals. The method further comprises generating the first number of chip-select signals in response at least in part to the phase-locked clock signals, the address signals, and the second number of chip-select signals.

[0013] In certain embodiments, a circuit is configured to be mounted on a memory module configured to be operationally coupled to a computer system. The memory module has a first number of ranks, each rank of the first number of ranks comprising a plurality of double-data-rate (DDR) memory circuits that are configured to be activated concurrently with one another for receiving and transmitting data having a bit width of the rank in response at least in part to a first number of chip-select signals. The circuit is configurable to receive a set of signals comprising a command signal, address signals, and a second number of chip-select signals smaller than the first number of chip-select signals. The circuit is further configurable to generate phase-locked clock signals, wherein the circuit is configurable to transmit the phase-locked clock signals to the first number of ranks. The circuit is further configurable to store an address signal of the set of signals during a row access procedure and to pass the stored address signal as an address signal to the first number of ranks during a subsequent column address procedure. The circuit is further configurable to respond at least in part to the phase-locked clock signals, address signals, and the second number of chip-select signals by selecting at least one rank of the first number of ranks to receive the command signal and transmitting the command signal to the selected at least one rank. The circuit is further configurable to selectively isolate a data signal line load of at least one rank of the first number of ranks from the computer system in response at least in part to the set of signals by presenting a load of the circuit to the computer system. The circuit is further configurable to generate the first number of chip-select signals in response at least in part to the phase-locked clock signals, the address signals, and the second number of chip-select signals.

Brief Description of the Drawings

[0014] Figure 1 schematically illustrates an example memory module in accordance with certain embodiments described herein.

[0015] Figure 2 schematically illustrates a circuit diagram of two memory devices of a conventional memory module.

[0016] Figures 3A and 3B schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two

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memory devices from the computer system in accordance with certain embodiments described herein.

[0017] Figures 4A and 4B schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two ranks of memory devices from the computer system in accordance with certain embodiments described herein.

[0018] Figures 5A-5D schematically illustrate example memory modules having a circuit comprising a logic element and one or more switches operatively coupled to the logic element in accordance with certain embodiments described herein.

[0019] Figure 6A shows an exemplary timing diagram of a gapless read burst for a back-to-back adjacent read condition from one memory device.

[0020] Figure 6B shows an exemplary timing diagram with an extra clock cycle between successive read commands issued to different memory devices for successive read accesses from different memory devices.

[0021] Figure 7 shows an exemplary timing diagram in which the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b."

[0022] Figures 8A-8D schematically illustrate circuit diagrams of example memory modules comprising a circuit which multiplexes the DQS data strobe signal lines from one another in accordance with certain embodiments described herein.

[0023] Figure 9A schematically illustrates an example memory module with four ranks of memory devices compatible with certain embodiments described herein.

[0024] Figure 9B schematically illustrates an example memory module with two ranks of memory devices compatible with certain embodiments described herein.

[0025] Figure 9C schematically illustrates another example memory module in accordance with certain embodiments described herein.

[0026] Figure 10A schematically illustrates an exemplary memory module which doubles the rank density in accordance with certain embodiments described herein.

[0027] Figure 10B schematically illustrates an exemplary circuit compatible with embodiments described herein.

[0028] Figure 11A schematically illustrates an exemplary memory module which doubles number of ranks in accordance with certain embodiments described herein.

[0029] Figure 11B schematically illustrates an exemplary circuit compatible with embodiments described herein.

[0030] Figure 12 schematically illustrates an exemplary memory module in which a data strobe (DQS) pin of a first memory device is electrically connected to a DQS pin of a second memory device while both DQS pins are active.

[0031] Figure 13 is an exemplary timing diagram of the voltages applied to the two DQS pins due to non-simultaneous switching.

[0032] Figure 14 schematically illustrates another exemplary memory module in which a DQS pin of a first memory device is connected to a DQS pin of a second memory device.

[0033] Figure 15 schematically illustrates an exemplary memory module in accordance with certain embodiments described herein.

[0034] Figures 16A and 16B schematically illustrate a first side and a second side, respectively, of a memory module with eighteen 64M x 4 bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board.

[0035] Figures 17A and 17B schematically illustrate an exemplary embodiment of a memory module in which a first resistor and a second resistor are used to reduce the current flow between the first DQS pin and the second DQS pin.

[0036] Figure 18 schematically illustrates another exemplary memory module compatible with certain embodiments described herein.

[0037] Figure 19 schematically illustrates a particular embodiment of the memory module schematically illustrated by Figure 18.

Detailed Description of Example Embodiments

Load Isolation

[0038] Figure 1 schematically illustrates an example memory module 10 compatible with certain embodiments described herein. The memory module 10 is connectable to a memory controller 20 of a computer system (not shown). The memory module 10 comprises a plurality of memory devices 30, each memory device 30 having a

corresponding load. The memory module 10 further comprises a circuit 40 electrically coupled to the plurality of memory devices 30 and configured to be electrically coupled to the memory controller 20 of the computer system. The circuit 40 selectively isolates one or more of the loads of the memory devices from the computer system. The circuit 40 comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module 10.

[0039] As used herein, the term "load" is a broad term which includes, without limitation, electrical load, such as capacitive load, inductive load, or impedance load. As used herein, the term "isolation" is a broad term which includes, without limitation, electrical separation of one or more components from another component or from one another. As used herein, the term "circuit" is a broad term which includes, without limitation, an electrical component or device, or a configuration of electrical components or devices which are electrically or electromagnetically coupled together (e.g., integrated circuits), to perform specific functions.

[0040] Various types of memory modules 10 are compatible with embodiments described herein. For example, memory modules 10 having memory capacities of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, as well as other capacities, are compatible with embodiments described herein. Certain embodiments described herein are applicable to various frequencies including, but not limited to 100 MHz, 200 MHz, 400 MHz, 800 MHz, and above. In addition, memory modules 10 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. In certain embodiments, the memory module 10 comprises a printed circuit board on which the memory devices 30 are mounted, a plurality of edge connectors configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, and a plurality of electrical conduits which electrically couple the memory devices 30 to the circuit 40 and which electrically couple the circuit 40 to the edge connectors. Furthermore, memory modules 10 compatible with embodiments described herein include, but are not limited to, single in-line memory modules (SIMMs), dual in-line memory modules (DIMMs), small-outline DIMMs (SO-

DIMMs), unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), fully-buffered DIMM (FBDIMM), rank-buffered DIMMs (RBDIMMs), mini-DIMMs, and micro-DIMMs.

[0041] Memory devices 30 compatible with embodiments described herein include, but are not limited to, random-access memory (RAM), dynamic random-access memory (DRAM), synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., SDR, DDR-1, DDR-2, DDR-3). In addition, memory devices 30 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein. Memory devices 30 compatible with embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP). Memory devices 30 compatible with embodiments described herein are available from a number of sources, including but not limited to, Samsung Semiconductor, Inc. of San Jose, California, Infineon Technologies AG of San Jose, California, and Micron Technology, Inc. of Boise, Idaho. Persons skilled in the art can select appropriate memory devices 30 in accordance with certain embodiments described herein.

[0042] In certain embodiments, the plurality of memory devices 30 comprises a first number of memory devices 30. In certain such embodiments, the circuit 40 selectively isolates a second number of the memory devices 30 from the computer system, with the second number less than the first number.

[0043] In certain embodiments, the plurality of memory devices 30 are arranged in a first number of ranks. For example, in certain embodiments, the memory devices 30 are arranged in two ranks, as schematically illustrated by Figure 1. In other embodiments, the memory devices 30 are arranged in four ranks. Other numbers of ranks of the memory devices 30 are also compatible with embodiments described herein.

[0044] In certain embodiments, the circuit comprises a logic element selected from a group consisting of: a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, and a complex programmable-logic device (CPLD). In certain embodiments, the logic element of the circuit 40 is a custom device. Sources of logic elements compatible with embodiments described herein include, but are not limited to,

Lattice Semiconductor Corporation of Hillsboro, Oregon, Altera Corporation of San Jose, California, and Xilinx Incorporated of San Jose, California. In certain embodiments, the logic element comprises various discrete electrical elements, while in certain other embodiments, the logic element comprises one or more integrated circuits.

[0045] In certain embodiments, the circuit 40 further comprises one or more switches which are operatively coupled to the logic element to receive control signals from the logic element. Examples of switches compatible with certain embodiments described herein include, but are not limited to, field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Texas.

[0046] Figure 2 schematically illustrates a circuit diagram of two memory devices 30a, 30b of a conventional memory module showing the interconnections between the DQ data signal lines 102a, 102b of the memory devices 30a, 30b and the DQS data strobe signal lines 104a, 104b of the memory devices 30a, 30b. Each of the memory devices 30a, 30b has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, however, for simplicity, Figure 2 only illustrates a single DQ data signal line and a single DQS data strobe signal line for each memory device 30a, 30b. The DQ data signal lines 102a, 102b and the DQS data strobe signal lines 104a, 104b are typically conductive traces etched on the printed circuit board of the memory module. As shown in Figure 2, each of the memory devices 30a, 30b has their DQ data signal lines 102a, 102b electrically coupled to a common DQ line 112 and their DQS data strobe signal lines 104a, 104b electrically coupled to a common DQS line 114. The common DQ line 112 and the common DQS line 114 are electrically coupled to the memory controller 20 of the computer system. Thus, the computer system is exposed to the loads of both memory devices 30a, 30b concurrently.

[0047] In certain embodiments, the circuit 40 selectively isolates the loads of at least some of the memory devices 30 from the computer system. The circuit 40 of certain embodiments is configured to present a significantly reduced load to the computer system. In certain embodiments in which the memory devices 30 are arranged in a plurality of ranks, the circuit 40 selectively isolates the loads of some (e.g., one or more) of the ranks of the memory module 10 from the computer system. In certain other embodiments, the circuit 40

selectively isolates the loads of all of the ranks of the memory module 10 from the computer system. For example, when a memory module 10 is not being accessed by the computer system, the capacitive load on the memory controller 20 of the computer system by the memory module 10 can be substantially reduced to the capacitive load of the circuit 40 of the memory module 10.

[0048] As schematically illustrated by Figures 3A and 3B, an example memory module 10 compatible with certain embodiments described herein comprises a circuit 40 which selectively isolates one or both of the DQ data signal lines 102a, 102b of the two memory devices 30a, 30b from the common DQ data signal line 112 coupled to the computer system. Thus, the circuit 40 selectively allows a DQ data signal to be transmitted from the memory controller 20 of the computer system to one or both of the DQ data signal lines 102a, 102b. In addition, the circuit 40 selectively allows one of a first DQ data signal from the DQ data signal line 102a of the first memory device 30a or a second DQ data signal from the DQ data signal line 102b of the second memory device 30b to be transmitted to the memory controller 20 via the common DQ data signal line 112 (see, e.g., triangles on the DQ and DQS lines of Figures 3A and 3B which point towards the memory controller). While various figures of the present application denote read operations by use of DQ and DQS lines which have triangles pointing towards the memory controller, certain embodiments described herein are also compatible with write operations (e.g., as would be denoted by triangles on the DQ or DQS lines pointing away from the memory controller).

[0049] For example, in certain embodiments, the circuit 40 comprises a pair of switches 120a, 120b on the DQ data signal lines 102a, 102b as schematically illustrated by Figure 3A. Each switch 120a, 120b is selectively actuated to selectively electrically couple the DQ data signal line 102a to the common DQ signal line 112, the DQ data signal line 102b to the common DQ signal line 112, or both DQ data signal lines 102a, 102b to the common DQ signal line 112. In certain other embodiments, the circuit 40 comprises a switch 120 electrically coupled to both of the DQ data signal lines 102a, 102b, as schematically illustrated by Figure 3B. The switch 120 is selectively actuated to selectively electrically couple the DQ data signal line 102a to the common DQ signal line 112, the DQ data signal line 102b to the common DQ signal line 112, or both DQ signal lines 102a, 102b to the

common DQ signal line 112. Circuits 40 having other configurations of switches are also compatible with embodiments described herein. While each of the memory devices 30a, 30b has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, Figures 3A and 3B only illustrate a single DQ data signal line and a single DQS data strobe signal line for each memory device 30a, 30b for simplicity. The configurations schematically illustrated by Figures 3A and 3B can be applied to all of the DQ data signal lines and DQS data strobe signal lines of the memory module 10.

[0050] In certain embodiments, the circuit 40 selectively isolates the loads of ranks of memory devices 30 from the computer system. As schematically illustrated in Figures 4A and 4B, example memory modules 10 compatible with certain embodiments described herein comprise a first number of memory devices 30 arranged in a first number of ranks 32. The memory modules 10 of Figures 4A and 4B comprises two ranks 32a, 32b, with each rank 32a, 32b having a corresponding set of DQ data signal lines and a corresponding set of DQS data strobe lines. Other numbers of ranks (e.g., four ranks) of memory devices 30 of the memory module 10 are also compatible with certain embodiments described herein. For simplicity, Figures 4A and 4B illustrate only a single DQ data signal line and a single DQS data strobe signal line from each rank 32.

[0051] The circuit 40 of Figure 4A selectively isolates one or more of the DQ data signal lines 102a, 102b of the two ranks 32a, 32b from the computer system. Thus, the circuit 40 selectively allows a DQ data signal to be transmitted from the memory controller 20 of the computer system to the memory devices 30 of one or both of the ranks 32a, 32b via the DQ data signal lines 102a, 102b. In addition, the circuit 40 selectively allows one of a first DQ data signal from the DQ data signal line 102a of the first rank 32a and a second DQ data signal from the DQ data signal line 102b of the second rank 32b to be transmitted to the memory controller 20 via the common DQ data signal line 112. For example, in certain embodiments, the circuit 40 comprises a pair of switches 120a, 120b on the DQ data signal lines 102a, 102b as schematically illustrated by Figure 4A. Each switch 120a, 120b is selectively actuated to selectively electrically couple the DQ data signal line 102a to the common DQ data signal line 112, the DQ data signal line 102b to the common DQ data signal line 112, or both DQ data signal lines 102a, 102b to the common DQ data signal line

112. In certain other embodiments, the circuit 40 comprises a switch 120 electrically coupled to both of the DQ data signal lines 102a, 102b, as schematically illustrated by Figure 4B. The switch 120 is selectively actuated to selectively electrically couple the DQ data signal line 102a to the common DQ data signal line 112, the DQ data signal line 102b to the common DQ data signal line 112, or both DQ data signal lines 102a, 102b to the common DQ data signal line 112. Circuits 40 having other configurations of switches are also compatible with embodiments described herein.

[0052] In the example embodiments schematically illustrated by Figures 3A, 3B, 4A, and 4B, the circuit 40 comprises a logic element which is integral with and comprises the switches 120 which are coupled to the DQ data signal lines and the DQS data strobe signal lines. In certain such embodiments, each switch 120 comprises a data path multiplexer/demultiplexer. In certain other embodiments, the circuit 40 comprises a logic element 122 which is a separate component operatively coupled to the switches 120, as schematically illustrated by Figures 5A-5D. The one or more switches 120 are operatively coupled to the logic element 122 to receive control signals from the logic element 122 and to selectively electrically couple one or more data signal lines to a common data signal line. Example switches compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Texas. Example logic elements 122 compatible with certain embodiments described herein include, but are not limited to, programmable-logic devices (PLD), application-specific integrated circuits (ASIC), field-programmable gate arrays (FPGA), custom-designed semiconductor devices, and complex programmable-logic devices (CPLD). Example logic elements 122 are available from Lattice Semiconductor Corporation of Hillsboro, Oregon, Altera Corporation of San Jose, California, and Xilinx Incorporated of San Jose, California.

[0053] In certain embodiments, the load isolation provided by the circuit 40 advantageously allows the memory module 10 to present a reduced load (e.g., electrical load, such as capacitive load, inductive load, or impedance load) to the computer system by selectively switching between the two ranks of memory devices 30 to which it is coupled. This feature is used in certain embodiments in which the load of the memory module 10 may

otherwise limit the number of ranks or the number of memory devices per memory module. In certain embodiments, the memory module 10 operates as having a data path rank buffer which advantageously isolates the ranks of memory devices 30 of the memory module 10 from one another, from the ranks on other memory modules, and from the computer system. This data path rank buffer of certain embodiments advantageously provides DQ-DQS paths for each rank or sets of ranks of memory devices which are separate from one another, or which are separate from the memory controller of the computer system. In certain embodiments, the load isolation advantageously diminishes the effects of capacitive loading, jitter and other sources of noise. In certain embodiments, the load isolation advantageously simplifies various other aspects of operation of the memory module 10, including but not limited to, setup-and-hold time, clock skew, package skew, and process, temperature, voltage, and transmission line variations.

[0054] For certain memory module applications that utilize multiple ranks of memory, increased load on the memory bus can degrade speed performance. In certain embodiments described herein, selectively isolating the loads of the ranks of memory devices 30 advantageously decreases the load on the computer system, thereby allowing the computer system (e.g., server) to run faster with improved signal integrity. In certain embodiments, load isolation advantageously provides system memory with reduced electrical loading, thereby improving the electrical topology to the memory controller 20. In certain such embodiments, the speed and the memory density of the computer system are advantageously increased without sacrificing one for the other.

[0055] In certain embodiments, load isolation advantageously increases the size of the memory array supported by the memory controller 20 of the computer system. The larger memory array has an increased number of memory devices 30 and ranks of memory devices 30 of the memory module 10, with a corresponding increased number of chip selects. Certain embodiments described herein advantageously provide more system memory using fewer chip selects, thereby avoiding the chip select limitation of the memory controller.

[0056] An exemplary section of Verilog code corresponding to logic compatible with a circuit 40 which provides load isolation is listed below in Example 1. The exemplary

code of Example 1 corresponds to a circuit 40 comprising six FET switches for providing load isolation to DQ and DQS lines.

[0057] Example 1:

```
//============================= declarations
  reg          rasN_R, casN_R, weN_R;
  wire         actv_cmd_R, pch_cmd_R, pch_all_cmd_R, ap_xfr_cmd_R_R;
  wire         xfr_cmd_R,mrs_cmd,rd_cmd_R;
//-------------------------- DDR 2 FET
  reg          brs0N_R;                    // registered chip sel
  reg          brs1N_R;                    // registered chip sel
  reg          brs2N_R;                    // registered chip sel
  reg          brs3N_R;                    // registered chip sel
  wire         sel;
  wire         sel_01;
  wire         sel_23;
  wire         rd_R1;
  wire         wr_cmd_R,wr_R1;
  reg          rd_R2,rd_R3,rd_R4,rd_R5;
  reg          wr_R2,wr_R3,wr_R4,wr_R5;
  reg          enfet1,enfet2,enfet3,enfet4,enfet5,enfet6;
  wire         wr_01_R1,wr_23_R1;
  reg          wr_01_R2,wr_01_R3,wr_01_R4;
  reg          wr_23_R2,wr_23_R3,wr_23_R4;
  wire         rodt0_a,rodt0_b;
//============================= logic
 always @(posedge clk_in)
        begin
                brs0N_R <= brs0_in_N;     // cs0
                brs1N_R <= brs1_in_N;     // cs1
                brs2N_R <= brs2_in_N;     // cs2
                brs3N_R <= brs3_in_N;     // cs3
                rasN_R  <= brras_in_N ;
                casN_R  <= brcas_in_N ;
                weN_R   <= bwe_in_N ;
        end
assign sel = ~brs0N_R | ~brs1N_R | ~brs2N_R | ~brs3N_R ;
assign sel_01 = ~brs0N_R | ~brs1N_R ;
assign sel_23 = ~brs2N_R | ~brs3N_R ;
assign actv_cmd_R = !rasN_R & casN_R & weN_R; // activate cmd
assign pch_cmd_R = !rasN_R & casN_R & !weN_R ;// pchg cmd
assign xfr_cmd_R = rasN_R & !casN_R;          // xfr cmd
assign mrs_cmd = !rasN_R & !casN_R & !weN_R ;  // md reg set cmd
assign rd_cmd_R = rasN_R & !casN_R & weN_R ;   // read cmd
assign wr_cmd_R = rasN_R & !casN_R & !weN_R ;  // write cmd
//-------------------------------------
assign   rd_R1 = sel & rd_cmd_R;  // rd cmd cyc 1
assign   wr_R1 = sel & wr_cmd_R;  // wr cmd cyc 1
//-----------------------------------------
  always @(posedge clk_in)
        begin
                rd_R2 <= rd_R1 ;
                rd_R3 <= rd_R2;
```


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```
                rd_R4 <= rd_R3;
                rd_R5 <= rd_R4;
//              rd0_o_R6 <= rd0_o_R5;
                wr_R2 <= wr_R1 ;
                wr_R3 <= wr_R2;
                wr_R4 <= wr_R3;
                wr_R5 <= wr_R4;
        end
//----------------------------------------
assign  wr_01_R1 = sel_01 & wr_cmd_R;  // wr cmd cyc 1 for cs 2 & cs3
assign  wr_23_R1 = sel_23 & wr_cmd_R;  // wr cmd cyc 1 for cs 2 & cs3
  always @(posedge clk_in)
        begin
                wr_01_R2 <= wr_01_R1 ;
                wr_01_R3 <= wr_01_R2;
                wr_01_R4 <= wr_01_R3;
                wr_23_R2 <= wr_23_R1 ;
                wr_23_R3 <= wr_23_R2;
                wr_23_R4 <= wr_23_R3;
        end
assign  rodt0_ab = (rodt0)          // odt cmd from sys
                | (wr_23_R1)        // wr 1st cyc to other rnks (assume single dimm per channel)
                | (wr_23_R2)        // wr 2nd cyc to other rnks (assume single dimm per channel)
                | (wr_23_R3)        // wr 3rd cyc to other rnks (assume single dimm per channel)
                ;
assign  rodt1_ab = (rodt1)          // odt cmd from sys
                | (wr_01_R1)        // wr 1st cyc to other rnks (assume single dimm per channel)
                | (wr_01_R2)        // wr 2nd cyc to other rnks (assume single dimm per channel)
                | (wr_01_R3)        // wr 3rd cyc to other rnks (assume single dimm per channel)
                ;
//----------------------------------------
 always @(posedge clk_in)
        begin
  if (
    | (rd_R2)                       // pre-am rd
    | (rd_R3)                       // 1st cyc of rd brst (cl3)
    | (rd_R4)                       // 2nd cyc of rd brst (cl3)
    | (wr_R1)                       // pre-am wr
    | (wr_R2)                       // wr brst 1st cyc
    | (wr_R3)                       // wr brst 2nd cyc
     ) begin
                enfet1 <= 1'b1;     // enable fet
                enfet2 <= 1'b1;     // enable fet
                enfet3 <= 1'b1;     // enable fet
                enfet4 <= 1'b1;     // enable fet
                enfet5 <= 1'b1;     // enable fet
                enfet6 <= 1'b1;     // enable fet
       end
  else
       begin
                enfet1 <= 1'b0;     // disable fet
                enfet2 <= 1'b0;     // disable fet
                enfet3 <= 1'b0;     // disable fet
                enfet4 <= 1'b0;     // disable fet
                enfet5 <= 1'b0;     // disable fet
```

```
                enfet6 <= 1'b0;          // disable fet
        end
    end
```

Back-to-Back Adjacent Read Commands

[0058] Due to their source synchronous nature, DDR SDRAM (e.g., DDR1, DDR2, DDR3) memory devices operate with a data transfer protocol which surrounds each burst of data strobes with a pre-amble time interval and a post-amble time interval. The pre-amble time interval provides a timing window for the receiving memory device to enable its data capture circuitry when a known valid level is present on the strobe signal to avoid false triggers of the memory device's capture circuit. The post-amble time interval provides extra time after the last strobe for this data capture to facilitate good signal integrity. In certain embodiments, when the computer system accesses two consecutive bursts of data from the same memory device, termed herein as a "back-to-back adjacent read," the post-amble time interval of the first read command and the pre-amble time interval of the second read command are skipped by design protocol to increase read efficiency. Figure 6A shows an exemplary timing diagram of this "gapless" read burst for a back-to-back adjacent read condition from one memory device.

[0059] In certain embodiments, when the second read command accesses data from a different memory device than does the first read command, there is at least one time interval (e.g., clock cycle) inserted between the data strobes of the two memory devices. This inserted time interval allows both read data bursts to occur without the post-amble time interval of the first read data burst colliding or otherwise interfering with the pre-amble time interval of the second read data burst. In certain embodiments, the memory controller of the computer system inserts an extra clock cycle between successive read commands issued to different memory devices, as shown in the exemplary timing diagram of Figure 6B for successive read accesses from different memory devices.

[0060] In typical computer systems, the memory controller is informed of the memory boundaries between the ranks of memory of the memory module prior to issuing read commands to the memory module. Such memory controllers can insert wait time intervals or clock cycles to avoid collisions or interference between back-to-back adjacent

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read commands which cross memory device boundaries, which are referred to herein as "BBARX."

[0061] In certain embodiments described herein in which the number of ranks 32 of the memory module 10 is doubled or quadrupled, the circuit 40 generates a set of output address and command signals so that the selection decoding is transparent to the computer system. However, in certain such embodiments, there are memory device boundaries of which the computer system is unaware, so there are occasions in which BBARX occurs without the cognizance of the memory controller 20 of the computer system. As shown in Figure 7, the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b," resulting in a "collision window."

[0062] Figures 8A-8D schematically illustrate circuit diagrams of example memory modules 10 comprising a circuit 40 which multiplexes the DQS data strobe signal lines 104a, 104b of two ranks 32a, 32b from one another in accordance with certain embodiments described herein. While the DQS data strobe signal lines 104a, 104b of Figures 8A-8D correspond to two ranks 32a, 32b of memory devices 30, in certain other embodiments, the circuit 40 multiplexes the DQS data strobe signal lines 104a, 104b corresponding to two individual memory devices 30a, 30b.

[0063] Figure 8A schematically illustrates a circuit diagram of an exemplary memory module 10 comprising a circuit 40 in accordance with certain embodiments described herein. In certain embodiments, BBARX collisions are avoided by a mechanism which electrically isolates the DQS data strobe signal lines 104a, 104b from one another during the transition from the first read data burst of one rank 32a of memory devices 30 to the second read data burst of another rank 32b of memory devices 30.

[0064] In certain embodiments, as schematically illustrated by Figure 8A, the circuit 40 comprises a first switch 130a electrically coupled to a first DQS data strobe signal line 104a of a first rank 32a of memory devices 30 and a second switch 130b electrically coupled to a second DQS data strobe signal line 104b of a second rank 32b of memory devices 30. In certain embodiments, the time for switching the first switch 130a and the second switch 130b is between the two read data bursts (e.g., after the last DQS data strobe of the read data burst of the first rank 32a and before the first DQS data strobe of the read data

burst of the second rank 32b). During the read data burst for the first rank 32a, the first switch 130a is enabled. After the last DQS data strobe of the first rank 32a and before the first DQS data strobe of the second rank 32b, the first switch 130a is disabled and the second switch 130b is enabled.

[0065] As shown in Figure 8A, each of the ranks 32a, 32b otherwise involved in a BBARX collision have their DQS data strobe signal lines 104a, 104b selectively electrically coupled to the common DQS line 114 through the circuit 40. The circuit 40 of certain embodiments multiplexes the DQS data strobe signal lines 104a, 104b of the two ranks 32a, 32b of memory devices 30 from one another to avoid a BBARX collision.

[0066] In certain embodiments, as schematically illustrated by Figure 8B, the circuit 40 comprises a switch 130 which multiplexes the DQS data strobe signal lines 104a, 104b from one another. For example, the circuit 40 receives a DQS data strobe signal from the common DQS data strobe signal line 114 and selectively transmits the DQS data strobe signal to the first DQS data strobe signal line 104a, to the second DQS data strobe signal line 104b, or to both DQS data strobe signal lines 104a, 104b. As another example, the circuit 40 receives a first DQS data strobe signal from the first rank 32a of memory devices 30 and a second DQS data strobe signal from a second rank 32b of memory devices 30 and selectively switches one of the first and second DQS data strobe signals to the common DQS data strobe signal line 114.

[0067] In certain embodiments, the circuit 40 also provides the load isolation described above in reference to Figures 1-5. For example, as schematically illustrated by Figure 8C, the circuit 40 comprises both the switch 120 for the DQ data signal lines 102a, 102b and the switch 130 for the DQS data strobe signal lines 104a, 104b. While in certain embodiments, the switches 130 are integral with a logic element of the circuit 40, in certain other embodiments, the switches 130 are separate components which are operatively coupled to a logic element 122 of the circuit 40, as schematically illustrated by Figure 8D. In certain such embodiments, the control and timing of the switch 130 is performed by the circuit 40 which is resident on the memory module 10. Example switches 130 compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas

Instruments, Inc. of Dallas, Texas, and multiplexers, such as the SN74AUC2G53 2:1 analog multiplexer/demultiplexer available from Texas Instruments, Inc. of Dallas, Texas.

[0068] The circuit 40 of certain embodiments controls the isolation of the DQS data strobe signal lines 104a, 104b by monitoring commands received by the memory module 10 from the computer system and producing "windows" of operation whereby the appropriate switches 130 are activated or deactivated to enable and disable the DQS data strobe signal lines 104a, 104b to mitigate BBARX collisions. In certain other embodiments, the circuit 40 monitors the commands received by the memory module 10 from the computer system and selectively activates or deactivates the switches 120 to enable and disable the DQ data signal lines 102a, 102b to reduce the load of the memory module 10 on the computer system. In still other embodiments, the circuit 40 performs both of these functions together.

Command Signal Translation

[0069] Most high-density memory modules are currently built with 512-Megabit ("512-Mb") memory devices wherein each memory device has a 64M x 8-bit configuration. For example, a 1-Gigabyte ("1-GB") memory module with error checking capabilities can be fabricated using eighteen such 512-Mb memory devices. Alternatively, it can be economically advantageous to fabricate a 1-GB memory module using lower-density memory devices and doubling the number of memory devices used to produce the desired word width. For example, by fabricating a 1-GB memory module using thirty-six 256-Mb memory devices with 64M x 4-bit configuration, the cost of the resulting 1-GB memory module can be reduced since the unit cost of each 256-Mb memory device is typically lower than one-half the unit cost of each 512-Mb memory device. The cost savings can be significant, even though twice as many 256-Mb memory devices are used in place of the 512-Mb memory devices. For example, by using pairs of 512-Mb memory devices rather than single 1-Gb memory devices, certain embodiments described herein reduce the cost of the memory module by a factor of up to approximately five.

[0070] Market pricing factors for DRAM devices are such that higher-density DRAM devices (e.g., 1-Gb DRAM devices) are much more than twice the price of lower-density DRAM devices (e.g., 512-Mb DRAM devices). In other words, the price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices.

This pricing difference often lasts for months or even years after the introduction of the higher-density DRAM devices, until volume production factors reduce the costs of the newer higher-density DRAM devices. Thus, when the cost of a higher-density DRAM device is more than the cost of two lower-density DRAM devices, there is an economic incentive for utilizing pairs of the lower-density DRAM devices to replace individual higher-density DRAM devices.

[0071] Figure 9A schematically illustrates an exemplary memory module 10 compatible with certain embodiments described herein. The memory module 10 is connectable to a memory controller 20 of a computer system (not shown). The memory module 10 comprises a printed circuit board 210 and a plurality of memory devices 30 coupled to the printed circuit board 210. The plurality of memory devices 30 has a first number of memory devices 30. The memory module 10 further comprises a circuit 40 coupled to the printed circuit board 210. The circuit 40 receives a set of input address and command signals from the computer system. The set of input address and command signals correspond to a second number of memory devices 30 smaller than the first number of memory devices 30. The circuit 40 generates a set of output address and command signals in response to the set of input address and command signals. The set of output address and command signals corresponds to the first number of memory devices 30.

[0072] In certain embodiments, as schematically illustrated in Figure 9A, the memory module 10 further comprises a phase-lock loop device 220 coupled to the printed circuit board 210 and a register 230 coupled to the printed circuit board 210. In certain embodiments, the phase-lock loop device 220 and the register 230 are each mounted on the printed circuit board 210. In response to signals received from the computer system, the phase-lock loop device 220 transmits clock signals to the plurality of memory devices 30, the circuit 40, and the register 230. The register 230 receives and buffers a plurality of command signals and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals), and transmits corresponding signals to the appropriate memory devices 30. In certain embodiments, the register 230 comprises a plurality of register devices. While the phase-lock loop device 220, the register 230, and the circuit 40 are described herein in certain embodiments as being

separate components, in certain other embodiments, two or more of the phase-lock loop device 220, the register 230, and the circuit 40 are portions of a single component. Persons skilled in the art are able to select a phase-lock loop device 220 and a register 230 compatible with embodiments described herein.

[0073] In certain embodiments, the memory module 10 further comprises electrical components which are electrically coupled to one another and are surface-mounted or embedded on the printed circuit board 210. These electrical components can include, but are not limited to, electrical conduits, resistors, capacitors, inductors, and transistors. In certain embodiments, at least some of these electrical components are discrete, while in other certain embodiments, at least some of these electrical components are constituents of one or more integrated circuits.

[0074] In certain embodiments, the printed circuit board 210 is mountable in a module slot of the computer system. The printed circuit board 210 of certain such embodiments has a plurality of edge connections electrically coupled to corresponding contacts of the module slot and to the various components of the memory module 10, thereby providing electrical connections between the computer system and the components of the memory module 10.

[0075] In certain embodiments, the plurality of memory devices 30 are arranged in a first number of ranks 32. For example, in certain embodiments, the memory devices 30 are arranged in four ranks 32a, 32b, 32c, 32d, as schematically illustrated by Figure 9A. In certain other embodiments, the memory devices 30 are arranged in two ranks 32a, 32b, as schematically illustrated by Figure 9B. Other numbers of ranks 32 of the memory devices 30 are also compatible with embodiments described herein.

[0076] As schematically illustrated by Figures 9A and 9B, in certain embodiments, the circuit 40 receives a set of input command signals (e.g., refresh, precharge) and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) from the memory controller 20 of the computer system. In response to the set of input address and command signals, the circuit 40 generates a set of output address and command signals.

[0077] In certain embodiments, the set of output address and command signals corresponds to a first number of ranks in which the plurality of memory devices 30 of the memory module 10 are arranged, and the set of input address and command signals corresponds to a second number of ranks per memory module for which the computer system is configured. The second number of ranks in certain embodiments is smaller than the first number of ranks. For example, in the exemplary embodiment as schematically illustrated by Figure 9A, the first number of ranks is four while the second number of ranks is two. In the exemplary embodiment of Figure 9B, the first number of ranks is two while the second number of ranks is one. Thus, in certain embodiments, even though the memory module 10 actually has the first number of ranks of memory devices 30, the memory module 10 simulates a virtual memory module by operating as having the second number of ranks of memory devices 30. In certain embodiments, the memory module 10 simulates a virtual memory module when the number of memory devices 30 of the memory module 10 is larger than the number of memory devices 30 per memory module for which the computer system is configured to utilize. In certain embodiments, the circuit 40 comprises logic (e.g., address decoding logic, command decoding logic) which translates between a system memory domain of the computer system and a physical memory domain of the memory module 10.

[0078] In certain embodiments, the computer system is configured for a number of ranks per memory module which is smaller than the number of ranks in which the memory devices 30 of the memory module 10 are arranged. In certain such embodiments, the computer system is configured for two ranks of memory per memory module (providing two chip-select signals CS_0, CS_1) and the plurality of memory modules 30 of the memory module 10 are arranged in four ranks, as schematically illustrated by Figure 9A. In certain other such embodiments, the computer system is configured for one rank of memory per memory module (providing one chip-select signal CS_0) and the plurality of memory modules 30 of the memory module 10 are arranged in two ranks, as schematically illustrated by Figure 9B.

[0079] In the exemplary embodiment schematically illustrated by Figure 9A, the memory module 10 has four ranks of memory devices 30 and the computer system is configured for two ranks of memory devices per memory module. The memory module 10 receives row/column address signals or signal bits (A_0-A_{n+1}), bank address signals (BA_0-

BA_m), chip-select signals (CS_0 and CS_1), and command signals (e.g., refresh, precharge, etc.) from the computer system. The A_0-A_n row/column address signals are received by the register 230, which buffers these address signals and sends these address signals to the appropriate ranks of memory devices 30. The circuit 40 receives the two chip-select signals (CS_0, CS_1) and one row/column address signal (A_{n+1}) from the computer system. Both the circuit 40 and the register 230 receive the bank address signals (BA_0-BA_m) and at least one command signal (e.g., refresh, precharge, etc.) from the computer system.

Logic Tables

[0080] Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices 30 using chip-select signals.

Table 1:

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:

1. CS_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

[0081] In Logic State 1: CS_0 is active low, A_{n+1} is non-active, and Command is active. CS_{0A} is pulled low, thereby selecting Rank 0.

[0082] In Logic State 2: CS_0 is active low, A_{n+1} is active, and Command is active. CS_{0B} is pulled low, thereby selecting Rank 1.

[0083] In Logic State 3: CS_0 is active low, A_{n+1} is Don't Care, and Command is active high. CS_{0A} and CS_{0B} are pulled low, thereby selecting Ranks 0 and 1.

[0084] In Logic State 4: CS_1 is active low, A_{n+1} is non-active, and Command is active. CS_{1A} is pulled low, thereby selecting Rank 2.

[0085] In Logic State 5: CS_1 is active low, A_{n+1} is active, and Command is active. CS_{1B} is pulled low, thereby selecting Rank 3.

[0086] In Logic State 6: CS_1 is active low, A_{n+1} is Don't Care, and Command is active. CS_{1A} and CS_{1B} are pulled low, thereby selecting Ranks 2 and 3.

[0087] In Logic State 7: CS_0 and CS_1 are pulled non-active high, which deselects all ranks, i.e., CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are pulled high.

[0088] The "Command" column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently.

[0089] Table 2 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices 30 using gated CAS signals.

Table 2:

CS*	RAS*	CAS*	WE*	Density Bit	A_{10}	Command	CAS0*	CAS1*
1	x	x	x	x	x	NOP	x	x
0	1	1	1	x	x	NOP	1	1
0	0	1	1	0	x	ACTIVATE	1	1
0	0	1	1	1	x	ACTIVATE	1	1
0	1	0	1	0	x	READ	0	1
0	1	0	1	1	x	READ	1	0
0	1	0	0	0	x	WRITE	0	1

0	1	0	0	1	x	WRITE	1	0
0	0	1	0	0	0	PRECHARGE	1	1
0	0	1	0	1	0	PRECHARGE	1	1
0	0	1	0	x	1	PRECHARGE	1	1
0	0	0	0	x	x	MODE REG SET	0	0
0	0	0	1	x	x	REFRESH	0	0

[0090] In certain embodiments in which the density bit is a row address bit, for read/write commands, the density bit is the value latched during the activate command for the selected bank.

Serial-Presence-Detect Device

[0091] Memory modules typically include a serial-presence detect (SPD) device 240 (e.g., an electrically-erasable-programmable read-only memory or EEPROM device) comprising data which characterize various attributes of the memory module, including but not limited to, the number of row addresses the number of column addresses, the data width of the memory devices, the number of ranks, the memory density per rank, the number of memory devices, and the memory density per memory device. The SPD device 240 communicates this data to the basic input/output system (BIOS) of the computer system so that the computer system is informed of the memory capacity and the memory configuration available for use and can configure the memory controller properly for maximum reliability and performance.

[0092] For example, for a commercially-available 512-MB (64M x 8-byte) memory module utilizing eight 512-Mb memory devices each with a 64M x 8-bit configuration, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: Defines the number of row address bits in the DRAM device in the memory module [13 for the 512-Mb memory device].

Byte 4: Defines the number of column address bits in the DRAM device in the memory module [11 for the 512-Mb memory device].

Byte 13: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 512-Mb (64M x 8-bit) memory device].

Byte 14: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 512-Mb (64M x 8-bit) memory device].

Byte 17: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 512-Mb memory device].

[0093] In a further example, for a commercially-available 1-GB (128M x 8-byte) memory module utilizing eight 1-Gb memory devices each with a 128M x 8-bit configuration, as described above, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: Defines the number of row address bits in the DRAM device in the memory module [14 for the 1-Gb memory device].

Byte 4: Defines the number of column address bits in the DRAM device in the memory module [11 for the 1-Gb memory device].

Byte 13: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 1-Gb (128M x 8-bit) memory device].

Byte 14: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 1-Gb (128M x 8-bit) memory device].

Byte 17: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 1-Gb memory device].

[0094] In certain embodiments, the SPD device 240 comprises data which characterize the memory module 10 as having fewer ranks of memory devices than the memory module 10 actually has, with each of these ranks having more memory density. For example, for a memory module 10 compatible with certain embodiments described herein having two ranks of memory devices 30, the SPD device 240 comprises data which characterizes the memory module 10 as having one rank of memory devices with twice the memory density per rank. Similarly, for a memory module 10 compatible with certain embodiments described herein having four ranks of memory devices 30, the SPD device 240 comprises data which characterizes the memory module 10 as having two ranks of memory devices with twice the memory density per rank. In addition, in certain embodiments, the SPD device 240 comprises data which characterize the memory module 10 as having fewer memory devices than the memory module 10 actually has, with each of these memory devices having more memory density per memory device. For example, for a memory module 10 compatible with certain embodiments described herein, the SPD device 240 comprises data which characterizes the memory module 10 as having one-half the number of memory devices that the memory module 10 actually has, with each of these memory devices

having twice the memory density per memory device. Thus, in certain embodiments, the SPD device 240 informs the computer system of the larger memory array by reporting a memory device density that is a multiple of the memory devices 30 resident on the memory module 10. Certain embodiments described herein advantageously do not require system level changes to hardware (e.g., the motherboard of the computer system) or to software (e.g., the BIOS of the computer system).

[0095] Figure 9C schematically illustrates an exemplary memory module 10 in accordance with certain embodiments described herein. The memory module 10 comprises a pair of substantially identical memory devices 31, 33. Each memory device 31, 33 has a first bit width, a first number of banks of memory locations, a first number of rows of memory locations, and a first number of columns of memory locations. The memory module 10 further comprises an SPD device 240 comprising data that characterizes the pair of memory devices 31, 33. The data characterize the pair of memory devices 31, 33 as a virtual memory device having a second bit width equal to twice the first bit width, a second number of banks of memory locations equal to the first number of banks, a second number of rows of memory locations equal to the first number of rows, and a second number of columns of memory locations equal to the first number of columns.

[0096] In certain such embodiments, the SPD device 240 of the memory module 10 is programmed to describe the combined pair of lower-density memory devices 31, 33 as one virtual or pseudo-higher-density memory device. In an exemplary embodiment, two 512-Mb memory devices, each with a 128M x 4-bit configuration, are used to simulate one 1-Gb memory device having a 128M x 8-bit configuration. The SPD device 240 of the memory module 10 is programmed to describe the pair of 512-Mb memory devices as one virtual or pseudo-1-Gb memory device.

[0097] For example, to fabricate a 1-GB (128M x 8-byte) memory module, sixteen 512-Mb (128M x 4-bit) memory devices can be used. The sixteen 512-Mb (128M x 4-bit) memory devices are combined in eight pairs, with each pair serving as a virtual or pseudo-1-Gb (128M x 8-bit) memory device. In certain such embodiments, the SPD device 240 contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: 13 row address bits.
Byte 4: 12 column address bits.

Byte 13: 8 bits wide for the primary virtual 1-Gb (128M x 8-bit) memory device.
Byte 14: 8 bits wide for the error checking virtual 1-Gb (128M x 8-bit) memory device.
Byte 17: 4 banks.

[0098] In this exemplary embodiment, bytes 3, 4, and 17 are programmed to have the same values as they would have for a 512-MB (128M x 4-byte) memory module utilizing 512-Mb (128M x 4-bit) memory devices. However, bytes 13 and 14 of the SPD data are programmed to be equal to 8, corresponding to the bit width of the virtual or pseudo-higher-density 1-Gb (128M x 8-bit) memory device, for a total capacity of 1-GB. Thus, the SPD data does not describe the actual-lower-density memory devices, but instead describes the virtual or pseudo-higher-density memory devices. The BIOS accesses the SPD data and recognizes the memory module as having 4 banks of memory locations arranged in 2^{13} rows and 2^{12} columns, with each memory location having a width of 8 bits rather than 4 bits.

[0099] In certain embodiments, when such a memory module 10 is inserted in a computer system, the computer system's memory controller then provides to the memory module 10 a set of input address and command signals which correspond to the number of ranks or the number of memory devices reported by the SPD device 240. For example, placing a two-rank memory module 10 compatible with certain embodiments described herein in a computer system compatible with one-rank memory modules, the SPD device 240 reports to the computer system that the memory module 10 only has one rank. The circuit 40 then receives a set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices 30 of the memory module 10.

[0100] Similarly, when a two-rank memory module 10 compatible with certain embodiments described herein is placed in a computer system compatible with either one- or two-rank memory modules, the SPD device 240 reports to the computer system that the memory module 10 only has one rank. The circuit 40 then receives a set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices 30 of the memory module 10.

[0101] Furthermore, a four-rank memory module 10 compatible with certain embodiments described herein simulates a two-rank memory module whether the memory module 10 is inserted in a computer system compatible with two-rank memory modules or with two- or four-rank memory modules. Thus, by placing a four-rank memory module 10 compatible with certain embodiments described herein in a module slot that is four-rank-ready, the computer system provides four chip-select signals, but the memory module 10 only uses two of the chip-select signals.

[0102] In certain embodiments, the circuit 40 comprises the SPD device 240 which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device 240 of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array. In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit 40. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices 30 from the memory controller 20. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three. In still other embodiments, the SPD device 240 does not utilize this extra cycle of time.

Memory Density Multiplication

[0103] In certain embodiments, two memory devices having a memory density are used to simulate a single memory device having twice the memory density, and an additional address signal bit is used to access the additional memory. Similarly, in certain embodiments, two ranks of memory devices having a memory density are used to simulate a single rank of memory devices having twice the memory density, and an additional address

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signal bit is used to access the additional memory. As used herein, such simulations of memory devices or ranks of memory devices are termed as "memory density multiplication," and the term "density transition bit" is used to refer to the additional address signal bit which is used to access the additional memory by selecting which rank of memory devices is enabled for a read or write transfer operation.

[0104] For example, for computer systems which are normally limited to using memory modules which have a single rank of 128M x 4-bit memory devices, certain embodiments described herein enable the computer system to utilize memory modules which have double the memory (e.g., two ranks of 128M x 4-bit memory devices). The circuit 40 of certain such embodiments provides the logic (e.g., command and address decoding logic) to double the number of chip selects, and the SPD device 240 reports a memory device density of 256M x 4-bit to the computer system.

[0105] In certain embodiments utilizing memory density multiplication embodiments, the memory module 10 can have various types of memory devices 30 (e.g., DDR1, DDR2, DDR3, and beyond). The circuit 40 of certain such embodiments utilizes implied translation logic equations having variations depending on whether the density transition bit is a row, column, or internal bank address bit. In addition, the translation logic equations of certain embodiments vary depending on the type of memory module 10 (e.g., UDIMM, RDIMM, FBDIMM, etc.). Furthermore, in certain embodiments, the translation logic equations vary depending on whether the implementation multiplies memory devices per rank or multiplies the number of ranks per memory module.

[0106] Table 3A provides the numbers of rows and columns for DDR-1 memory devices, as specified by JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published February 2004, and incorporated in its entirety by reference herein.

Table 3A:

	128-Mb	256-Mb	512-Mb	1-Gb
Number of banks	4	4	4	4
Number of row address bits	12	13	13	14
Number of column address bits for "x 4" configuration	11	11	12	12
Number of column address bits for "x 8" configuration	10	10	11	11

Number of column address bits for "x 16" configuration	9	9	10	10

[0107] As described by Table 3A, 512-Mb (128M x 4-bit) DRAM devices have 2^{13} rows and 2^{12} columns of memory locations, while 1-Gb (128M x 8-bit) DRAM devices have 2^{14} rows and 2^{11} columns of memory locations. Because of the differences in the number of rows and the number of columns for the two types of memory devices, complex address translation procedures and structures would typically be needed to fabricate a 1-GB (128M x 8-byte) memory module using sixteen 512-Mb (128M x 4-bit) DRAM devices.

[0108] Table 3B shows the device configurations as a function of memory density for DDR2 memory devices.

Table 3B:

	Number of Rows	Number of Columns	Number of Internal Banks	Page Size (x4s or x8s)
256 Mb	13	11	4	1 KB
512 Mb	14	11	4	1 KB
1 Gb	14	11	8	1 KB
2 Gb	15	11	8	1 KB
4 Gb	16	11	8	1 KB

Table 4 lists the corresponding density transition bit for the density transitions between the DDR2 memory densities of Table 3B.

Table 4:

Density Transition	Density Transition Bit
256 Mb to 512 Mb	A_{13}
512 Mb to 1 Gb	BA_2
1 Gb to 2 Gb	A_{14}
2 Gb to 4 Gb	A_{15}

Other certain embodiments described herein utilize a transition bit to provide a transition from pairs of physical 4-Gb memory devices to simulated 8-Gb memory devices.

[0109] In an example embodiment, the memory module comprises one or more pairs of 256-Mb memory devices, with each pair simulating a single 512-Mb memory device. The simulated 512-Mb memory device has four internal banks while each of the two 256-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 256-Mb memory devices. In certain embodiments, the additional row address bit is translated by

the circuit 40 to the rank selection between each of the two 256-Mb memory devices of the pair. Although there are eight total internal banks in the rank-converted memory array, the computer system is only aware of four internal banks. When the memory controller activates a row for a selected bank, the circuit 40 activates the same row for the same bank, but it does so for the selected rank according to the logic state of the additional row address bit A_{13}.

[0110] In another example embodiment, the memory module comprises one or more pairs of 512-Mb memory devices, with each pair simulating a single 1-Gb memory device. The simulated 1-Gb memory device has eight internal banks while each of the two 512-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 512-Mb memory devices. In certain embodiments, the mapped BA_2 (bank 2) bit is used to select between the two ranks of 512-Mb memory devices to preserve the internal bank geometry expected by the memory controller of the computer system. The state of the BA_2 bit selects the upper or lower set of four banks, as well as the upper and lower 512-Mb rank.

[0111] In another example embodiment, the memory module comprises one or more pairs of 1-Gb memory devices, with each pair simulating a single 2-Gb memory device. Each of the two 1-Gb memory devices has eight internal banks for a total of sixteen internal banks, while the simulated 2-Gb memory device has eight internal banks. In certain embodiments, the additional row address bit translates to the rank selection between the two 1-Gb memory devices. Although there are sixteen total internal banks per pair of 1-Gb memory devices in the rank-converted memory array, the memory controller of the computer system is only aware of eight internal banks. When the memory controller activates a row of a selected bank, the circuit 40 activates the same row for the same bank, but is does so for the selected rank according to the logic state of the additional row address bit A_{14}.

[0112] The circuit 40 of certain embodiments provides substantially all of the translation logic used for the decoding (e.g., command and address decoding). In certain such embodiments, there is a fully transparent operational conversion from the "system memory" density domain of the computer system to the "physical memory" density domain of the memory module 10. In certain embodiments, the logic translation equations are programmed in the circuit 40 by hardware, while in certain other embodiments, the logic

translation equations are programmed in the circuit 40 by software. Examples 1 and 2 provide exemplary sections of Verilog code compatible with certain embodiments described herein. As described more fully below, the code of Examples 1 and 2 includes logic to reduce potential problems due to "back-to-back adjacent read commands which cross memory device boundaries or "BBARX." Persons skilled in the art are able to provide additional logic translation equations compatible with embodiments described herein.

[0113] An exemplary section of Verilog code compatible with memory density multiplication from 512 Mb to 1 Gb using DDR2 memory devices with the BA_2 density transition bit is listed below in Example 2. The exemplary code of Example 2 corresponds to a circuit 40 which receives one chip-select signal from the computer system and which generates two chip-select signals.

[0114] Example 2:

```
always @(posedge clk_in)
  begin
        rs0N_R <= rs0_in_N;     // cs0
        rasN_R <= ras_in_N;
        casN_R <= cas_in_N;
        weN_R <= we_in_N;
  end

// Gated Chip Selects
assign          pcs0a_1  = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                      // ref,md reg set
                 |(~rs0_in_N & ras_in_N & cas_in_N)                                 // ref exit, pwr dn
                 |(~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)            // pchg all
                 |(~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ~ba2_in)// pchg single bnk
                 |(~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N      & ~ba2_in)       // activate
                 |(~rs0_in_N & ras_in_N & ~cas_in_N              & ~ba2_in)         // xfr
                 ;
assign          pcs0b_1  = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                      // ref,md reg set
                 |(~rs0_in_N & ras_in_N & cas_in_N)                                 // ref exit, pwr dn
                 |(~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)            // pchg all
                 |(~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ba2_in)// pchg single bnk
                 |(~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N      & ba2_in)        // activate
                 |(~rs0_in_N & ras_in_N & ~cas_in_N              & ba2_in) // xfr
                 ;
//-------------------------------------
  always @(posedge clk_in)
   begin
        a4_r <= a4_in ;
        a5_r <= a5_in ;
        a6_r <= a6_in ;
        a10_r <= a10_in ;
        ba0_r <= ba0_in ;
        ba1_r <= ba1_in ;
        ba2_r <= ba2_in ;
        q_mrs_cmd_cycl <= q_mrs_cmd ;
  end
//////////////////////////////////////////////////////////////////////////
// determine the cas latency
//////////////////////////////////////////////////////////////////////////
assign q_mrs_cmd_r = (!rasN_R & !casN_R & !weN_R)
            & !rs0N_R
          & (!ba0_r & !ba1_r)
```

```
                ;           // md reg set cmd

  always @(posedge clk_in)
   if (~reset_N)            // lmr
                cl3 <= 1'b1 ;
   else if (q_mrs_cmd_cyc1)         // load mode reg cmd
   begin
                cl3 <= (~a6_r & a5_r & a4_r ) ;
   end

  always @(posedge clk_in)
   if (~reset_N)                // reset
                cl2 <= 1'b0 ;
   else if (q_mrs_cmd_cyc1)         // load mode reg cmd
   begin
                cl2 <= (~a6_r & a5_r & ~a4_r ) ;
   end

  always @(posedge clk_in)
   if (~reset_N)                // reset
                cl4 <= 1'b0 ;
   else if (q_mrs_cmd_cyc1)         // load mode reg cmd
   begin
                cl4 <= (a6_r & ~a5_r & ~a4_r ) ;
   end

 always @(posedge clk_in)
   if (~reset_N)                cl5 <= 1'b0 ;
   else if (q_mrs_cmd_cyc1)         // load mode reg cmd
   begin
                cl5 <= (a6_r & ~a5_r & a4_r ) ;
   end

assign          pre_cyc2_enfet = (wr_cmd_cyc1 & acs_cyc1 & cl3)   // wr brst cl3 preamble
                                ;
assign          pre_cyc3_enfet = (rd_cmd_cyc2 & cl3)              // rd brst cl3 preamble
                                | (wr_cmd_cyc2 & cl3)             // wr brst cl3 1st pair
                                | (wr_cmd_cyc2 & cl4)             // wr brst cl4 preamble

                                ;

assign          pre_cyc4_enfet = (wr_cmd_cyc3 & cl3)              // wr brst cl3 2nd pair
                                | (wr_cmd_cyc3 & cl4)             // wr brst cl4 1st pair

                                | (rd_cmd_cyc3 & cl3)             // rd brst cl3 1st pair
                                | (rd_cmd_cyc3 & cl4)             // rd brst cl4 preamble
                                ;

assign          pre_cyc5_enfet = (rd_cmd_cyc4  & cl3)             // rd brst cl3 2nd pair
                                | (wr_cmd_cyc4  & cl4)            // wr brst cl4 2nd pair

                                | (rd_cmd_cyc4  & cl4)            // rd brst cl4 1st pair
                                ;

// dq
assign          pre_dq_cyc = pre_cyc2_enfet
                  | pre_cyc3_enfet
                  | pre_cyc4_enfet
                  | pre_cyc5_enfet
                  ;

assign          pre_dq_ncyc = enfet_cyc2
                  | enfet_cyc3
                  | enfet_cyc4
                  | enfet_cyc5
                  ;

// dqs
```

```
assign          pre_dqsa_cyc = (pre_cyc2_enfet & ~ba2_r)
                  | (pre_cyc3_enfet & ~ba2_cyc2)
                  | (pre_cyc4_enfet & ~ba2_cyc3)
                  | (pre_cyc5_enfet & ~ba2_cyc4)
                  ;
assign          pre_dqsb_cyc = (pre_cyc2_enfet & ba2_r)
                  | (pre_cyc3_enfet & ba2_cyc2)
                  | (pre_cyc4_enfet & ba2_cyc3)
                  | (pre_cyc5_enfet & ba2_cyc4)
                  ;

assign          pre_dqsa_ncyc = (enfet_cyc2 & ~ba2_cyc2)
                  | (enfet_cyc3 & ~ba2_cyc3)
                  | (enfet_cyc4 & ~ba2_cyc4)
                  | (enfet_cyc5 & ~ba2_cyc5)
                  ;
assign          pre_dqsb_ncyc = (enfet_cyc2 & ba2_cyc2)
                  | (enfet_cyc3 & ba2_cyc3)
                  | (enfet_cyc4 & ba2_cyc4)
                  | (enfet_cyc5 & ba2_cyc5)
                  ;

always @(posedge clk_in)
  begin
        acs_cyc2 <= acs_cyc1 ;          // cs active
        ba2_cyc2 <= ba2_r ;
        ba2_cyc3 <= ba2_cyc2 ;
        ba2_cyc4 <= ba2_cyc3 ;
        ba2_cyc5 <= ba2_cyc4 ;

        rd_cmd_cyc2 <= rd_cmd_cyc1 & acs_cyc1;
        rd_cmd_cyc3 <= rd_cmd_cyc2 ;
        rd_cmd_cyc4 <= rd_cmd_cyc3 ;
        rd_cmd_cyc5 <= rd_cmd_cyc4 ;
        rd_cmd_cyc6 <= rd_cmd_cyc5 ;
        rd_cmd_cyc7 <= rd_cmd_cyc6 ;

        wr_cmd_cyc2 <= wr_cmd_cyc1 & acs_cyc1;
        wr_cmd_cyc3 <= wr_cmd_cyc2 ;
        wr_cmd_cyc4 <= wr_cmd_cyc3 ;
        wr_cmd_cyc5 <= wr_cmd_cyc4 ;
  end

 always @(negedge clk_in)
  begin
        dq_ncyc <= dq_cyc;
        dqs_ncyc_a <= dqs_cyc_a;
        dqs_ncyc_b <= dqs_cyc_b;
  end

// DQ FET enables
assign          enq_fet1  = dq_cyc  | dq_ncyc        ;
assign          enq_fet2  = dq_cyc  | dq_ncyc  ;
assign          enq_fet3  = dq_cyc  | dq_ncyc        ;
assign          enq_fet4  = dq_cyc  | dq_ncyc  ;
assign          enq_fet5  = dq_cyc  | dq_ncyc  ;
// DQS FET enables
assign          ens_fet1a = dqs_cyc_a  | dqs_ncyc_a   ;
assign          ens_fet2a = dqs_cyc_a  | dqs_ncyc_a   ;
assign          ens_fet3a = dqs_cyc_a  | dqs_ncyc_a   ;
assign          ens_fet1b = dqs_cyc_b  | dqs_ncyc_b   ;
assign          ens_fet2b = dqs_cyc_b  | dqs_ncyc_b   ;
assign          ens_fet3b = dqs_cyc_b  | dqs_ncyc_b   ;
```

[0115] Another exemplary section of Verilog code compatible with memory density multiplication from 256 Mb to 512 Mb using DDR2 memory devices and gated CAS

signals with the row A_{13} density transition bit is listed below in Example 3. The exemplary code of Example 3 corresponds to a circuit 40 which receives one gated CAS signal from the computer system and which generates two gated CAS signals.

[0116] Example 3:

```
// latched a13 flags cs0, banks 0-3
  always @(posedge clk_in)
   if (actv_cmd_R & ~rs0N_R & ~bnk1_R & ~bnk0_R )  // activate
   begin
            l_a13_00 <= a13_r ;
   end
  always @(posedge clk_in)
   if (actv_cmd_R & ~rs0N_R & ~bnk1_R &  bnk0_R)     // activate
   begin
            l_a13_01 <= a13_r ;
   end
  always @(posedge clk_in)
   if (actv_cmd_R & ~rs0N_R & bnk1_R & ~bnk0_R)      // activate
   begin
            l_a13_10 <= a13_r ;
   end
  always @(posedge clk_in)
   if (actv_cmd_R & ~rs0N_R & bnk1_R & bnk0_R)       // activate
   begin
            l_a13_11 <= a13_r ;
   end
// gated cas
assign cas_i = ~(casN_R);
assign   cas0_o = ( ~rasN_R & cas_i)
            | ( rasN_R &  ~l_a13_00 & ~bnk1_R & ~bnk0_R & cas_i)
            | ( rasN_R &  ~l_a13_01 & ~bnk1_R &  bnk0_R & cas_i)
            | ( rasN_R &  ~l_a13_10 &  bnk1_R & ~bnk0_R & cas_i)
            | ( rasN_R &  ~l_a13_11 &  bnk1_R &  bnk0_R & cas_i)
            ;
assign   cas1_o = ( ~rasN_R  & cas_i)
            | ( rasN_R & l_a13_00          & ~bnk1_R & ~bnk0_R & cas_i)
            | ( rasN_R & l_a13_01          & ~bnk1_R &  bnk0_R & cas_i)
            | ( rasN_R & l_a13_10          &  bnk1_R & ~bnk0_R & cas_i)
            | ( rasN_R & l_a13_11          &  bnk1_R &  bnk0_R & cas_i)
            ;
assign      pcas_0_N = ~cas0_o;
assign      pcas_1_N = ~cas1_o;

assign      rd0_o_R1 = rasN_R & cas0_o & weN_R & ~rs0N_R;  // rnk0 rd cmd  cyc

assign      rd1_o_R1 = rasN_R & cas1_o & weN_R & ~rs0N_R;  // rnk1 rd cmd  cyc

assign      wr0_o_R1 = rasN_R & cas0_o & ~weN_R & ~rs0N_R;  // rnk0 wr cmd  cyc

assign      wr1_o_R1 = rasN_R & cas1_o & ~weN_R & ~rs0N_R ; // rnk1 wr cmd  cyc

  always @(posedge clk_in)
   begin
            rd0_o_R2 <= rd0_o_R1 ;
            rd0_o_R3 <= rd0_o_R2;
            rd0_o_R4 <= rd0_o_R3;
            rd0_o_R5 <= rd0_o_R4;

            rd1_o_R2 <= rd1_o_R1 ;
            rd1_o_R3 <= rd1_o_R2;
            rd1_o_R4 <= rd1_o_R3;
            rd1_o_R5 <= rd1_o_R4;

            wr0_o_R2 <= wr0_o_R1 ;
```

```
            wr0_o_R3 <= wr0_o_R2;
            wr0_o_R4 <= wr0_o_R3;

            wr1_o_R2 <= wr1_o_R1 ;
            wr1_o_R3 <= wr1_o_R2;
            wr1_o_R4 <= wr1_o_R3;
end

always @(posedge clk_in)
begin
if (
   (rd0_o_R2 & ~rd1_o_R4)                                  // pre-am rd if no ped on rnk 1
  | rd0_o_R3                                               // 1st cyc of rd brst
  | rd0_o_R4                                               // 2nd cyc of rd brst
  | (rd0_o_R5 & ~rd1_o_R2 & ~rd1_o_R3)                     // post-rd cyc if no ped on rnk 1
  | (wr0_o_R1)                                             // pre-am wr
  | wr0_o_R2 | wr0_o_R3                                    // wr brst 1st & 2nd cyc
  | (wr0_o_R4)                                             // post-wr cyc  (chgef9)
  | wr1_o_R1 | wr1_o_R2 | wr1_o_R3 | wr1_o_R4 // rank 1  (chgef9)
   )
                    en_fet_a <= 1'b1;                      // enable fet
else
                    en_fet_a <= 1'b0;                      // disable fet
end

always @(posedge clk_in)
          begin
          if (
                (rd1_o_R2 & ~rd0_o_R4)
              | rd1_o_R3
              | rd1_o_R4
              | (rd1_o_R5 & ~rd0_o_R2 & ~rd0_o_R3)
            | (wr1_o_R1)                                   // (chgef8)
            | wr1_o_R2  | wr1_o_R3
      | (wr1_o_R4)                                         // post-wr cyc          (chgef9)
      | wr0_o_R1 | wr0_o_R2 | wr0_o_R3 | wr0_o_R4           // rank 0  (chgef9)
              )
                    en_fet_b <= 1'b1;                      //
          else
                    en_fet_b <= 1'b0;
          end
```

[0117] In certain embodiments, the chipset memory controller of the computer system uses the inherent behavioral characteristics of the memory devices (e.g., DDR2 memory devices) to optimize throughput of the memory system. For example, for each internal bank in the memory array, a row (e.g., 1KB page) is advantageously held activated for an extended period of time. The memory controller, by anticipating a high number of memory accesses or hits to a particular region of memory, can exercise this feature to advantageously eliminate time-consuming pre-charge cycles. In certain such embodiments in which two half-density memory devices are transparently substituted for a single full-density memory device (as reported by the SPD device 240 to the memory controller), the memory devices advantageously support the "open row" feature.

[0118] Figure 10A schematically illustrates an exemplary memory module 10 which doubles the rank density in accordance with certain embodiments described herein.

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The memory module 10 has a first memory capacity. The memory module 10 comprises a plurality of substantially identical memory devices 30 configured as a first rank 32a and a second rank 32b. In certain embodiments, the memory devices 30 of the first rank 32a are configured in pairs, and the memory devices 30 of the second rank 32b are also configured in pairs. In certain embodiments, the memory devices 30 of the first rank 32a are configured with their respective DQS pins tied together and the memory devices 30 of the second rank 32b are configured with their respective DQS pins tied together, as described more fully below. The memory module 10 further comprises a circuit 40 which receives a first set of address and command signals from a memory controller (not shown) of the computer system. The first set of address and command signals is compatible with a second memory capacity substantially equal to one-half of the first memory capacity. The circuit 40 translates the first set of address and command signals into a second set of address and command signals which is compatible with the first memory capacity of the memory module 10 and which is transmitted to the first rank 32a and the second rank 32b.

[0119] The first rank 32a of Figure 10A has 18 memory devices 30 and the second rank 32b of Figure 10A has 18 memory devices 30. Other numbers of memory devices 30 in each of the ranks 32a, 32b are also compatible with embodiments described herein.

[0120] In the embodiment schematically illustrated by Figure 10A, the memory module 10 has a width of 8 bytes (or 64 bits) and each of the memory devices 30 of Figure 10A has a bit width of 4 bits. The 4-bit-wide ("x 4") memory devices 30 of Figure 10A have one-half the width, but twice the depth of 8-bit-wide ("x 8") memory devices. Thus, each pair of "x 4" memory devices 30 has the same density as a single "x 8" memory device, and pairs of "x 4" memory devices 30 can be used instead of individual "x 8" memory devices to provide the memory density of the memory module 10. For example, a pair of 512-Mb 128M x 4-bit memory devices has the same memory density as a 1-Gb 128M x 8-bit memory device.

[0121] For two "x 4" memory devices 30 to work in tandem to mimic a "x 8" memory device, the relative DQS pins of the two memory devices 30 in certain embodiments are advantageously tied together, as described more fully below. In addition, to access the

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memory density of a high-density memory module 10 comprising pairs of "x 4" memory devices 30, an additional address line is used. While a high-density memory module comprising individual "x 8" memory devices with the next-higher density would also utilize an additional address line, the additional address lines are different in the two memory module configurations.

[0122] For example, a 1-Gb 128M x 8-bit DDR-1 DRAM memory device uses row addresses A_{13}-A_0 and column addresses A_{11} and A_9-A_0. A pair of 512-Mb 128M x 4-bit DDR-1 DRAM memory devices uses row addresses A_{12}-A_0 and column addresses A_{12}, A_{11}, and A_9-A_0. In certain embodiments, a memory controller of a computer system utilizing a 1-GB 128M x 8 memory module 10 comprising pairs of the 512-Mb 128M x 4 memory devices 30 supplies the address and command signals including the extra row address (A_{13}) to the memory module 10. The circuit 40 receives the address and command signals from the memory controller and converts the extra row address (A_{13}) into an extra column address (A_{12}).

[0123] Figure 10B schematically illustrates an exemplary circuit 40 compatible with embodiments described herein. The circuit 40 is used for a memory module 10 comprising pairs of "x 4" memory devices 30 which mimic individual "x 8" memory devices. In certain embodiments, each pair has the respective DQS pins of the memory devices 30 tied together. In certain embodiments, as schematically illustrated by Figure 10B, the circuit 40 comprises a programmable-logic device (PLD) 42, a first multiplexer 44 electrically coupled to the first rank 32a of memory devices 30, and a second multiplexer 46 electrically coupled to the second rank 32b of memory devices 30. In certain embodiments, the PLD 42 and the first and second multiplexers 44, 46 are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD 42, first multiplexer 44, and second multiplexer 46 in accordance with embodiments described herein.

[0124] In the exemplary circuit 40 of Figure 10B, during a row access procedure (CAS is high), the first multiplexer 44 passes the A_{12} address through to the first rank 32, the second multiplexer 46 passes the A_{12} address through to the second rank 34, and the PLD 42 saves or latches the A_{13} address from the memory controller. In certain embodiments, a copy

of the A_{13} address is saved by the PLD 42 for each of the internal banks (e.g., 4 internal banks) per memory device 30. During a subsequent column access procedure (CAS is low), the first multiplexer 44 passes the previously-saved A_{13} address through to the first rank 32a as the A_{12} address and the second multiplexer 46 passes the previously-saved A_{13} address through to the second rank 32b as the A_{12} address. The first rank 32a and the second rank 32b thus interpret the previously-saved A_{13} row address as the current A_{12} column address. In this way, in certain embodiments, the circuit 40 translates the extra row address into an extra column address in accordance with certain embodiments described herein.

[0125] Thus, by allowing two lower-density memory devices to be used rather than one higher-density memory device, certain embodiments described herein provide the advantage of using lower-cost, lower-density memory devices to build "next-generation" higher-density memory modules. Certain embodiments advantageously allow the use of lower-cost readily-available 512-Mb DDR-2 SDRAM devices to replace more expensive 1-Gb DDR-2 SDRAM devices. Certain embodiments advantageously reduce the total cost of the resultant memory module.

[0126] Figure 11A schematically illustrates an exemplary memory module 10 which doubles number of ranks in accordance with certain embodiments described herein. The memory module 10 has a first plurality of memory locations with a first memory density. The memory module 10 comprises a plurality of substantially identical memory devices 30 configured as a first rank 32a, a second rank 32b, a third rank 32c, and a fourth rank 32d. The memory module 10 further comprises a circuit 40 which receives a first set of address and command signals from a memory controller (not shown). The first set of address and command signals is compatible with a second plurality of memory locations having a second memory density. The second memory density is substantially equal to one-half of the first memory density. The circuit 40 translates the first set of address and command signals into a second set of address and command signals which is compatible with the first plurality of memory locations of the memory module 10 and which is transmitted to the first rank 32a, the second rank 32b, the third rank 32c, and the fourth rank 32d.

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[0127] Each rank 32a, 32b, 32c, 32d of Figure 11A has 9 memory devices 30. Other numbers of memory devices 30 in each of the ranks 32a, 32b, 32c, 32d are also compatible with embodiments described herein.

[0128] In the embodiment schematically illustrated by Figure 11A, the memory module 10 has a width of 8 bytes (or 64 bits) and each of the memory devices 30 of Figure 11A has a bit width of 8 bits. Because the memory module 10 has twice the number of 8-bit-wide ("x 8") memory devices 30 as does a standard 8-byte-wide memory module, the memory module 10 has twice the density as does a standard 8-byte-wide memory module. For example, a 1-GB 128M x 8-byte memory module with 36 512-Mb 128M x 8-bit memory devices (arranged in four ranks) has twice the memory density as a 512-Mb 128M x 8-byte memory module with 18 512-Mb 128M x 8-bit memory devices (arranged in two ranks).

[0129] To access the additional memory density of the high-density memory module 10, the two chip-select signals (CS_0, CS_1) are used with other address and command signals to gate a set of four gated CAS signals. For example, to access the additional ranks of four-rank 1-GB 128M x 8-byte DDR-1 DRAM memory module, the CS_0 and CS_1 signals along with the other address and command signals are used to gate the CAS signal appropriately, as schematically illustrated by Figure 11A. Figure 11B schematically illustrates an exemplary circuit 40 compatible with embodiments described herein. In certain embodiments, the circuit 40 comprises a programmable-logic device (PLD) 42 and four "OR" logic elements 52, 54, 56, 58 electrically coupled to corresponding ranks 32a, 32b, 32c, 32d of memory devices 30.

[0130] In certain embodiments, the PLD 42 comprises an ASIC, an FPGA, a custom-designed semiconductor device, or a CPLD. In certain embodiments, the PLD 42 and the four "OR" logic elements 52, 54, 56, 58 are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD 42 and appropriate "OR" logic elements 52, 54, 56, 58 in accordance with embodiments described herein.

[0131] In the embodiment schematically illustrated by Figure 11B, the PLD 42 transmits each of the four "enabled CAS" ($ENCAS_0a$, $ENCAS_0b$, $ENCAS_1a$, $ENCAS_1b$) signals to a corresponding one of the "OR" logic elements 52, 54, 56, 58. The CAS signal is

also transmitted to each of the four "OR" logic elements 52, 54, 56, 58. The CAS signal and the "enabled CAS" signals are "low" true signals. By selectively activating each of the four "enabled CAS" signals which are inputted into the four "OR" logic elements 52, 54, 56, 58, the PLD 42 is able to select which of the four ranks 32a, 32b, 32c, 32d is active.

[0132] In certain embodiments, the PLD 42 uses sequential and combinatorial logic procedures to produce the gated CAS signals which are each transmitted to a corresponding one of the four ranks 32a, 32b, 32c, 32d. In certain other embodiments, the PLD 42 instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS_0a, CS_0b, CS_1a, and CS_1b) which are each transmitted to a corresponding one of the four ranks 32a, 32b, 32c, 32d.

Tied Data Strobe Signal Pins

[0133] For proper operation, the computer system advantageously recognizes a 1-GB memory module comprising 256-Mb memory devices with 64M x 4-bit configuration as a 1-GB memory module having 512-Mb memory devices with 64M x 8-bit configuration (e.g., as a 1-GB memory module with 128M x 8-byte configuration). This advantageous result is desirably achieved in certain embodiments by electrically connecting together two output signal pins (e.g., DQS or data strobe pins) of the two 256-Mb memory devices such that both output signal pins are concurrently active when the two memory devices are concurrently enabled. The DQS or data strobe is a bi-directional signal that is used during both read cycles and write cycles to validate or latch data. As used herein, the terms "tying together" or "tied together" refer to a configuration in which corresponding pins (e.g., DQS pins) of two memory devices are electrically connected together and are concurrently active when the two memory devices are concurrently enabled (e.g., by a common chip-select or CS signal). Such a configuration is different from standard memory module configurations in which the output signal pins (e.g., DQS pins) of two memory devices are electrically coupled to the same source, but these pins are not concurrently active since the memory devices are not concurrently enabled. However, a general guideline of memory module design warns against tying together two output signal pins in this way.

[0134] Figures 12 and 13 schematically illustrate a problem which may arise from tying together two output signal pins. Figure 12 schematically illustrates an exemplary

memory module 305 in which a first DQS pin 312 of a first memory device 310 is electrically connected to a second DQS pin 322 of a second memory device 320. The two DQS pins 312, 322 are both electrically connected to a memory controller 330.

[0135] Figure 13 is an exemplary timing diagram of the voltages applied to the two DQS pins 312, 322 due to non-simultaneous switching. As illustrated by Figure 13, at time t_1, both the first DQS pin 312 and the second DQS pin 322 are high, so no current flows between them. Similarly, at time t_4, both the first DQS pin 312 and the second DQS pin 322 are low, so no current flows between them. However, for times between approximately t_2 and approximately t_3, the first DQS pin 312 is low while the second DQS pin 322 is high. Under such conditions, a current will flow between the two DQS pins 312, 322. This condition in which one DQS pin is low while the other DQS pin is high can occur for fractions of a second (e.g., 0.8 nanoseconds) during the dynamic random-access memory (DRAM) read cycle. During such conditions, the current flowing between the two DQS pins 312, 322 can be substantial, resulting in heating of the memory devices 310, 320, and contributing to the degradation of reliability and eventual failure of these memory devices.

[0136] A second problem may also arise from tying together two output signal pins. Figure 14 schematically illustrates another exemplary memory module 305 in which a first DQS pin 312 of a first memory device 310 is electrically connected to a second DQS pin 322 of a second memory device 320. The two DQS pins 312, 322 of Figure 14 are both electrically connected to a memory controller (not shown). The DQ (data input/output) pin 314 of the first memory device 310 and the corresponding DQ pin 324 of the second memory device 320 are each electrically connected to the memory controller by the DQ bus (not shown). Typically, each memory device 310, 320 will have a plurality of DQ pins (e.g., eight DQ pins per memory device), but for simplicity, Figure 14 only shows one DQ pin for each memory device 310, 320.

[0137] Each of the memory devices 310, 320 of Figure 14 utilizes a respective on-die termination or "ODT" circuit 332, 334 which has termination resistors (e.g., 75 ohms) internal to the memory devices 310, 320 to provide signal termination. Each memory device 310, 320 has a corresponding ODT signal pin 362, 364 which is electrically connected to the memory controller via an ODT bus 340. The ODT signal pin 362 of the first memory device

310 receives a signal from the ODT bus 340 and provides the signal to the ODT circuit 332 of the first memory device 310. The ODT circuit 332 responds to the signal by selectively enabling or disabling the internal termination resistors 352, 356 of the first memory device 310. This behavior is shown schematically in Figure 14 by the switches 342, 344 which are either closed (dash-dot line) or opened (solid line). The ODT signal pin 364 of the second memory device 320 receives a signal from the ODT bus 340 and provides the signal to the ODT circuit 334 of the second memory device 320. The ODT circuit 334 responds to the signal by selectively enabling or disabling the internal termination resistors 354, 358 of the second memory device 320. This behavior is shown schematically in Figure 14 by the switches 346, 348 which are either closed (dash-dot line) or opened (solid line). The switches 342, 344, 346, 348 of Figure 14 are schematic representations of the operation of the ODT circuits 332, 334, and do not signify that the ODT circuits 332, 334 necessarily include mechanical switches.

[0138] Examples of memory devices 310, 320 which include such ODT circuits 332, 334 include, but are not limited to, DDR2 memory devices. Such memory devices are configured to selectively enable or disable the termination of the memory device in this way in response to signals applied to the ODT signal pin of the memory device. For example, when the ODT signal pin 362 of the first memory device 310 is pulled high, the termination resistors 352, 356 of the first memory device 310 are enabled. When the ODT signal pin 362 of the first memory device 310 is pulled low (e.g., grounded), the termination resistors 352, 356 of the first memory device 310 are disabled. By selectively disabling the termination resistors of an active memory device, while leaving the termination resistors of inactive memory devices enabled, such configurations advantageously preserve signal strength on the active memory device while continuing to eliminate signal reflections at the bus-die interface of the inactive memory devices.

[0139] In certain configurations, as schematically illustrated by Figure 14, the DQS pins 312, 322 of each memory device 310, 320 are selectively connected to a voltage VTT through a corresponding termination resistor 352, 354 internal to the corresponding memory device 310, 320. Similarly, in certain configurations, as schematically illustrated by Figure 14, the DQ pins 314, 324 are selectively connected to a voltage VTT through a

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corresponding termination resistor 356, 358 internal to the corresponding memory device 310, 320. In certain configurations, rather than being connected to a voltage VTT, the DQ pins 314, 324 and/or the DQS pins 312, 322 are selectively connected to ground through the corresponding termination resistors 352, 354, 356, 358. The resistances of the internal termination resistors 352, 354, 356, 358 are selected to clamp the voltages so as to reduce the signal reflections from the corresponding pins. In the configuration schematically illustrated by Figure 14, each internal termination resistor 352, 354, 356, 358 has a resistance of approximately 75 ohms.

[0140] When connecting the first memory device 310 and the second memory device 320 together to form a double word width, both the first memory device 310 and the second memory device 320 are enabled at the same time (e.g., by a common CS signal). Connecting the first memory device 310 and the second memory device 320 by tying the DQS pins 312, 322 together, as shown in Figure 14, results in a reduced effective termination resistance for the DQS pins 312, 322. For example, for the exemplary configuration of Figure 14, the effective termination resistance for the DQS pins 312, 322 is approximately 37.5 ohms, which is one-half the desired ODT resistance (for 75-ohm internal termination resistors) to reduce signal reflections since the internal termination resistors 352, 354 of the two memory devices 310, 320 are connected in parallel. This reduction in the termination resistance can result in signal reflections causing the memory device to malfunction.

[0141] Figure 15 schematically illustrates an exemplary memory module 400 in accordance with certain embodiments described herein. The memory module 400 comprises a first memory device 410 having a first data strobe (DQS) pin 412 and a second memory device 420 having a second data strobe (DQS) pin 422. The memory module 400 further comprises a first resistor 430 electrically coupled to the first DQS pin 412. The memory module 400 further comprises a second resistor 440 electrically coupled to the second DQS pin 422 and to the first resistor 430. The first DQS pin 412 is electrically coupled to the second DQS pin 422 through the first resistor 430 and through the second resistor 440.

[0142] In certain embodiments, the memory module 400 is a 1-GB unbuffered Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) high-density dual in-line memory module (DIMM). Figures 16A and 16B schematically illustrate a first side 462 and

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a second side 464, respectively, of such a memory module 400 with eighteen 64M x 4-bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board (PCB) 460. In certain embodiments, the memory module 400 further comprises a phase-lock-loop (PLL) clock driver 470, an EEPROM for serial-presence detect (SPD) data 480, and decoupling capacitors (not shown) mounted on the PCB in parallel to suppress switching noise on VDD and VDDQ power supply for DDR-1 SDRAM. By using synchronous design, such memory modules 400 allow precise control of data transfer between the memory module 400 and the system controller. Data transfer can take place on both edges of the DQS signal at various operating frequencies and programming latencies. Therefore, certain such memory modules 400 are suitable for a variety of high-performance system applications.

[0143] In certain embodiments, the memory module 400 comprises a plurality of memory devices configured in pairs, each pair having a first memory device 410 and a second memory device 420. For example, in certain embodiments, a 128M x 72-bit DDR SDRAM high-density memory module 400 comprises thirty-six 64M x 4-bit DDR-1 SDRAM integrated circuits in FBGA packages configured in eighteen pairs. The first memory device 410 of each pair has the first DQS pin 412 electrically coupled to the second DQS pin 422 of the second memory device 420 of the pair. In addition, the first DQS pin 412 and the second DQS pin 422 are concurrently active when the first memory device 410 and the second memory device 420 are concurrently enabled.

[0144] In certain embodiments, the first resistor 430 and the second resistor 440 each has a resistance advantageously selected to reduce the current flow between the first DQS pin 412 and the second DQS pin 422 while allowing signals to propagate between the memory controller and the DQS pins 412, 422. In certain embodiments, each of the first resistor 430 and the second resistor 440 has a resistance in a range between approximately 5 ohms and approximately 50 ohms. For example, in certain embodiments, each of the first resistor 430 and the second resistor 440 has a resistance of approximately 22 ohms. Other resistance values for the first resistor 430 and the second resistor 440 are also compatible with embodiments described herein. In certain embodiments, the first resistor 430 comprises a single resistor, while in other embodiments, the first resistor 430 comprises a plurality of

resistors electrically coupled together in series and/or in parallel. Similarly, in certain embodiments, the second resistor 440 comprises a single resistor, while in other embodiments, the second resistor 440 comprises a plurality of resistors electrically coupled together in series and/or in parallel.

[0145] Figures 17A and 17B schematically illustrate an exemplary embodiment of a memory module 400 in which the first resistor 430 and the second resistor 440 are used to reduce the current flow between the first DQS pin 412 and the second DQS pin 422. As schematically illustrated by Figure 17A, the memory module 400 is part of a computer system 500 having a memory controller 510. The first resistor 430 has a resistance of approximately 22 ohms and the second resistor 440 has a resistance of approximately 22 ohms. The first resistor 430 and the second resistor 440 are electrically coupled in parallel to the memory controller 510 through a signal line 520 having a resistance of approximately 25 ohms. The first resistor 430 and the second resistor 440 are also electrically coupled in parallel to a source of a fixed termination voltage (identified by VTT in Figures 17A and 17B) by a signal line 540 having a resistance of approximately 47 ohms. Such an embodiment can advantageously be used to allow two memory devices having lower bit widths (e.g., 4-bit) to behave as a single virtual memory device having a higher bit width (e.g., 8-bit).

[0146] Figure 17B schematically illustrates exemplary current-limiting resistors 430, 440 in conjunction with the impedances of the memory devices 410, 420. During an exemplary portion of a data read operation, the memory controller 510 is in a high-impedance condition, the first memory device 410 drives the first DQS pin 412 high (e.g., 2.7 volts), and the second memory device 420 drives the second DQS pin 422 low (e.g., 0 volts). The amount of time for which this condition occurs is approximated by the time between t_2 and t_3 of Figure 13, which in certain embodiments is approximately twice the tDQSQ (data strobe edge to output data edge skew time, e.g., approximately 0.8 nanoseconds). At least a portion of this time in certain embodiments is caused by simultaneous switching output (SSO) effects.

[0147] In certain embodiments, as schematically illustrated by Figure 17B, the DQS driver of the first memory device 410 has a driver impedance R_1 of approximately

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17 ohms, and the DQS driver of the second memory device 420 has a driver impedance R_4 of approximately 17 ohms. Because the upper network of the first memory device 410 and the first resistor 430 (with a resistance R_2 of approximately 22 ohms) is approximately equal to the lower network of the second memory device 420 and the second resistor 440 (with a resistance R_3 of approximately 22 ohms), the voltage at the midpoint is approximately 0.5 * (2.7 - 0) = 1.35 volts, which equals VTT, such that the current flow across the 47-ohm resistor of Figure 17B is approximately zero.

[0148] The voltage at the second DQS pin 422 in Figure 17B is given by $V_{DQS2} = 2.7 * R_4/(R_1+R_2+R_3+R_4) = 0.59$ volts and the current flowing through the second DQS pin 422 is given by $I_{DQS2} = 0.59 / R_4 = 34$ milliamps. The power dissipation in the DQS driver of the second memory device 420 is thus $P_{DQS2} = 34$ mA * 0.59 V = 20 milliwatts. In contrast, without the first resistor 430 and the second resistor 440, only the 17-ohm impedances of the two memory devices 410, 420 would limit the current flow between the two DQS pins 412, 422, and the power dissipation in the DQS driver of the second memory device 420 would be approximately 107 milliwatts. Therefore, the first resistor 430 and the second resistor 440 of Figures 17A and 17B advantageously limit the current flowing between the two memory devices during the time that the DQS pin of one memory device is driven high and the DQS pin of the other memory device is driven low.

[0149] In certain embodiments in which there is overshoot or undershoot of the voltages, the amount of current flow can be higher than those expected for nominal voltage values. Therefore, in certain embodiments, the resistances of the first resistor 430 and the second resistor 440 are advantageously selected to account for such overshoot/undershoot of voltages.

[0150] For certain such embodiments in which the voltage at the second DQS pin 422 is $V_{DQS2} = 0.59$ volts and the duration of the overdrive condition is approximately 0.8 nanoseconds at maximum, the total surge is approximately 0.59 V * 1.2 ns = 0.3 V-ns. For comparison, the JEDEC standard for overshoot/undershoot is 2.4 V-ns, so certain embodiments described herein advantageously keep the total surge within predetermined standards (e.g., JEDEC standards).

[0151] Figure 18 schematically illustrates another exemplary memory module 600 compatible with certain embodiments described herein. The memory module 600 comprises a termination bus 605. The memory module 600 further comprises a first memory device 610 having a first data strobe pin 612, a first termination signal pin 614 electrically coupled to the termination bus 605, a first termination circuit 616, and at least one data pin 618. The first termination circuit 616 selectively electrically terminating the first data strobe pin 612 and the first data pin 618 in response to a first signal received by the first termination signal pin 614 from the termination bus 605. The memory module 600 further comprises a second memory device 620 having a second data strobe pin 622 electrically coupled to the first data strobe pin 612, a second termination signal pin 624, a second termination circuit 626, and at least one data pin 628. The second termination signal pin 624 is electrically coupled to a voltage, wherein the second termination circuit 626 is responsive to the voltage by not terminating the second data strobe pin 622 or the second data pin 628. The memory module 600 further comprises at least one termination assembly 630 having a third termination signal pin 634, a third termination circuit 636, and at least one termination pin 638 electrically coupled to the data pin 628 of the second memory device 620. The third termination signal pin 634 is electrically coupled to the termination bus 605. The third termination circuit 636 selectively electrically terminates the data pin 628 of the second memory device 620 through the termination pin 638 in response to a second signal received by the third termination signal pin 634 from the termination bus 605.

[0152] Figure 19 schematically illustrates a particular embodiment of the memory module 600 schematically illustrated by Figure 18. The memory module 600 comprises an on-die termination (ODT) bus 605. The memory module 600 comprises a first memory device 610 having a first data strobe (DQS) pin 612, a first ODT signal pin 614 electrically coupled to the ODT bus 605, a first ODT circuit 616, and at least one data (DQ) pin 618. The first ODT circuit 616 selectively electrically terminates the first DQS pin 612 and the DQ pin 618 of the first memory device 610 in response to an ODT signal received by the first ODT signal pin 614 from the ODT bus 605. This behavior of the first ODT circuit 616 is schematically illustrated in Figure 14 by the switches 672, 676 which are selectively closed (dash-dot line) or opened (solid line).

[0153] The memory module 600 further comprises a second memory device 620 having a second DQS pin 622 electrically coupled to the first DQS pin 612, a second ODT signal pin 624, a second ODT circuit 626, and at least one DQ pin 628. The first DQS pin 612 and the second DQS pin 622 are concurrently active when the first memory device 610 and the second memory device 620 are concurrently enabled. The second ODT signal pin 624 is electrically coupled to a voltage (e.g., ground), wherein the second ODT circuit 626 is responsive to the voltage by not terminating the second DQS pin 622 or the second DQ pin 624. This behavior of the second ODT circuit 626 is schematically illustrated in Figure 14 by the switches 674, 678 which are opened.

[0154] The memory module 600 further comprises at least one termination assembly 630 having a third ODT signal pin 634 electrically coupled to the ODT bus 605, a third ODT circuit 636, and at least one termination pin 638 electrically coupled to the DQ pin 628 of the second memory device 620. The third ODT circuit 636 selectively electrically terminates the DQ pin 628 of the second memory device 620 through the termination pin 638 in response to an ODT signal received by the third ODT signal pin 634 from the ODT bus 605. This behavior of the third ODT circuit 636 is schematically illustrated in Figure 19 by the switch 680 which is either closed (dash-dot line) or opened (solid line).

[0155] In certain embodiments, the termination assembly 630 comprises discrete electrical components which are surface-mounted or embedded on the printed-circuit board of the memory module 600. In certain other embodiments, the termination assembly 630 comprises an integrated circuit mounted on the printed-circuit board of the memory module 600. Persons skilled in the art can provide a termination assembly 630 in accordance with embodiments described herein.

[0156] Certain embodiments of the memory module 600 schematically illustrated by Figure 19 advantageously avoid the problem schematically illustrated by Figure 12 of electrically connecting the internal termination resistances of the DQS pins of the two memory devices in parallel. As described above in relation to Figure 14, Figures 18 and 19 only show one DQ pin for each memory device for simplicity. Other embodiments have a plurality of DQ pins for each memory device. In certain embodiments, each of the first ODT circuit 616, the second ODT circuit 626, and the third ODT circuit 636 are responsive to a

high voltage or signal level by enabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by disabling the corresponding termination resistors. In other embodiments, each of the first ODT circuit 616, the second ODT circuit 626, and the third ODT circuit 636 are responsive to a high voltage or signal level by disabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by enabling the corresponding termination resistors. Furthermore, the switches 672, 674, 676, 678, 680 of Figure 18 are schematic representations of the enabling and disabling operation of the ODT circuits 616, 626, 636 and do not signify that the ODT circuits 616, 626, 636 necessarily include mechanical switches.

[0157] The first ODT signal pin 614 of the first memory device 610 receives an ODT signal from the ODT bus 605. In response to this ODT signal, the first ODT circuit 616 selectively enables or disables the termination resistance for both the first DQS pin 612 and the DQ pin 618 of the first memory device 610. The second ODT signal pin 624 of the second memory device 620 is tied (e.g., directly hard-wired) to the voltage (e.g., ground), thereby disabling the internal termination resistors 654, 658 on the second DQS pin 622 and the second DQ pin 628, respectively, of the second memory device 620 (schematically shown by open switches 674, 678 in Figure 19). The second DQS pin 622 is electrically coupled to the first DQS pin 612, so the termination resistance for both the first DQS pin 612 and the second DQS pin 622 is provided by the termination resistor 652 internal to the first memory device 510.

[0158] The termination resistor 656 of the DQ pin 618 of the first memory device 610 is enabled or disabled by the ODT signal received by the first ODT signal pin 614 of the first memory device 610 from the ODT bus 605. The termination resistance of the DQ pin 628 of the second memory device 620 is enabled or disabled by the ODT signal received by the third ODT signal pin 634 of the termination assembly 630 which is external to the second memory device 620. Thus, in certain embodiments, the first ODT signal pin 614 and the third ODT signal pin 634 receive the same ODT signal from the ODT bus 605, and the termination resistances for both the first memory device 610 and the second memory device 620 are selectively enabled or disabled in response thereto when these memory devices are concurrently enabled. In this way, certain embodiments of the memory module 600

schematically illustrated by Figure 19 provides external or off-chip termination of the second memory device 620.

[0159] Certain embodiments of the memory module 600 schematically illustrated by Figure 19 advantageously allow the use of two lower-cost readily-available 512-Mb DDR-2 SDRAM devices to provide the capabilities of a more expensive 1-GB DDR-2 SDRAM device. Certain such embodiments advantageously reduce the total cost of the resultant memory module 600.

[0160] Certain embodiments described herein advantageously increase the memory capacity or memory density per memory slot or socket on the system board of the computer system. Certain embodiments advantageously allow for higher memory capacity in systems with limited memory slots. Certain embodiments advantageously allow for flexibility in system board design by allowing the memory module 10 to be used with computer systems designed for different numbers of ranks (e.g., either with computer systems designed for two-rank memory modules or with computer systems designed for four-rank memory modules). Certain embodiments advantageously provide lower costs of board designs.

[0161] In certain embodiments, the memory density of a memory module is advantageously doubled by providing twice as many memory devices as would otherwise be provided. For example, pairs of lower-density memory devices can be substituted for individual higher-density memory devices to reduce costs or to increase performance. As another example, twice the number of memory devices can be used to produce a higher-density memory configuration of the memory module. Each of these examples can be limited by the number of chip select signals which are available from the memory controller or by the size of the memory devices. Certain embodiments described herein advantageously provide a logic mechanism to overcome such limitations.

[0162] Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

WHAT IS CLAIMED IS:

1. A circuit configured to be mounted on a memory module configured to be operationally coupled to a computer system, the memory module having a first number of ranks, each rank of the first number of ranks comprising a plurality of double-data-rate (DDR) memory circuits that are configured to be activated concurrently with one another for receiving and transmitting data having a bit width of the rank in response at least in part to a first number of chip-select signals, the circuit configurable to:

receive a set of signals comprising address signals and a second number of chip-select signals smaller than the first number of chip-select signals;

generate phase-locked clock signals, wherein the circuit is configurable to transmit the phase-locked clock signals to the first number of ranks;

selectively isolate a load of at least one rank of the first number of ranks from the computer system in response at least in part to the set of signals; and

generate the first number of chip-select signals in response at least in part to the phase-locked clock signals, the address signals, and the second number of chip-select signals.

CIRCUIT FOR MEMORY MODULE

Abstract

A circuit is configured to be mounted on a memory module configured to be operationally coupled to a computer system. The memory module has a first number of ranks of double-data-rate (DDR) memory circuits activated by a first number of chip-select signals. The circuit is configurable to receive a set of signals comprising address signals and a second number of chip-select signals smaller than the first number of chip-select signals. The circuit is further configurable to generate phase-locked clock signals, to selectively isolate a load of at least one rank of the first number of ranks from the computer system in response at least in part to the set of signals, and to generate the first number of chip-select signals in response at least in part to the phase-locked clock signals, the address signals, and the second number of chip-select signals.

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110111

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Filer:	Bruce S. Itchkawitz
Attorney Docket Number:	NETL.018P2C6

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	380	380
Utility Search Fee	1111	1	620	620
Utility Examination Fee	1311	1	250	250
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1250**

Electronic Acknowledgement Receipt

EFS ID:	11314928
Application Number:	13287081
International Application Number:	
Confirmation Number:	6130
Title of Invention:	CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	20995
Filer:	Bruce S. Itchkawitz/Erica Van Sciver
Filer Authorized By:	Bruce S. Itchkawitz
Attorney Docket Number:	NETL.018P2C6
Receipt Date:	01-NOV-2011
Filing Date:	
Time Stamp:	21:26:08
Application Type:	Utility under 35 USC 111(a)

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Payment Type	Credit Card
Payment was successfully received in RAM	$1250
RAM confirmation Number	6010
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Application Data Sheet	ADS.pdf	329197 e9a23b80f39cfc10455282ae2be73d1e81fa347b	no	5
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
2	Drawings-only black and white line drawings	drawings.pdf	540946 0f50a723e8f1af86ab5c28d7268d01949a76690e	no	23
Warnings:					
Information:					
3	Oath or Declaration filed	declaration.pdf	104428 933065aff0a4d2c62db32c6d59b04acc91d402ec	no	2
Warnings:					
Information:					
4		SPEC.pdf	3155216 3af4c4d17004d7f585c8da806f07ffe0724e50b7	yes	55
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	53	
	Claims		54	54	
	Abstract		55	55	
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	32937 7006bca04744b6977334c6fbfa33f2e0b1c96808	no	2
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		Total Files Size (in bytes):	4162724		

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Docket No.: NETL.018P2C6
App. No.: 13/287,081

Please Direct All Correspondence to Customer Number 20995

RESCISSION OF ANY PRIOR DISCLAIMERS AND REQUEST TO REVISIT ART

Applicant	:	Jeffrey C. Solomon
App. No	:	13/287,081
Filed	:	November 1, 2011
For	:	CIRCUIT FOR MEMORY MODULE
Examiner	:	Unknown
Art Unit	:	2827
Conf #	:	6130

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The claims of the present application are different and possibly broader in scope than the claims pursued in the parent application(s). To the extent any prior amendments or characterizations of the scope of any claim or referenced art could be construed as a disclaimer of any subject matter supported by the present disclosure, Applicant hereby rescinds and retracts such disclaimer. Accordingly, the references previously considered in the parent application(s) may need to be re-visited.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

Dated: November 15, 2011

Bruce S. Itchkawitz
Registration No. 47,677
Agent of Record
Customer No. 20995
(949) 760-0404

12278242/111511

Electronic Acknowledgement Receipt

EFS ID:	11412876
Application Number:	13287081
International Application Number:	
Confirmation Number:	6130
Title of Invention:	CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	20995
Filer:	Bruce S. Itchkawitz/Lori Larson
Filer Authorized By:	Bruce S. Itchkawitz
Attorney Docket Number:	NETL.018P2C6
Receipt Date:	15-NOV-2011
Filing Date:	01-NOV-2011
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Application Type:	Utility under 35 USC 111(a)

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	rescission.pdf	38231 17b3d922210945e65436e3516c55cc22379c5d36	no	1

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/287,081

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	620
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 60 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 250 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1250

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT A	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT A	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT A	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT B	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT B	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT B	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/287,081	11/01/2011	2827	1250	NETL.018P2C6	1	1

CONFIRMATION NO. 6130

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

FILING RECEIPT

OC000000050937724

Date Mailed: 11/17/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Jeffrey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Assignment For Published Patent Application

NETLIST, INC., Irvine, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 13/032,470 02/22/2011
which is a CON of 12/955,711 11/29/2010 PAT 7,916,574
which is a CON of 12/629,827 12/02/2009 PAT 7,881,150
which is a CON of 12/408,652 03/20/2009 PAT 7,636,274
which is a CON of 11/335,875 01/19/2006 PAT 7,532,537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7,289,386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7,286,436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004
and claims benefit of 60/590,038 07/21/2004

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)

If Required, Foreign Filing License Granted: 11/14/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/287,081**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No
Title

CIRCUIT FOR MEMORY MODULE

Preliminary Class

365

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PTO/SB/81 (01-09)
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POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS

Application Number	13/287,081
Filing Date	01-NOV-2011
First Named Inventor	Solomon, Jeffrey
Title	CIRCUIT FOR MEMORY MODULE
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C6

I hereby revoke all previous powers of attorney given in the above-identified application.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith: 79141

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified application to:

☒ The address associated with the above-mentioned Customer Number.

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the:

☐ Applicant/Inventor.

OR

☒ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) (Form PTO/SB/96) submitted herewith or filed on _____.

SIGNATURE of Applicant or Assignee of Record

Signature		Date	September 20, 2012
Name	Gail Sasaki	Telephone	949-435-0025
Title and Company	VP and CFO		

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Netlist, Inc.

Application No./Patent No.: 13/287081 Filed/Issue Date: 1-Nov-2011

Titled: CIRCUIT FOR MEMORY MODULE

Netlist, Inc. (Name of Assignee), a Corporation (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. [X] the assignee of the entire right, title, and interest in;

2. [ ] an assignee of less than the entire right, title, and interest in (The extent (by percentage) of its ownership interest is _____ %); or

3. [ ] the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. [X] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 018104, Frame 0964, or for which a copy therefore is attached.

OR

B. [ ] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____
   The document was recorded in the United States Patent and Trademark Office at
   Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____
   The document was recorded in the United States Patent and Trademark Office at
   Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____
   The document was recorded in the United States Patent and Trademark Office at
   Reel _____, Frame _____, or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet(s).

[X] As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature	SEPTEMBER 20, 2012 Date
Gail Sasaki Printed or Typed Name	VP and CFO Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Acknowledgement Receipt

EFS ID:	13836660
Application Number:	13287081
International Application Number:	
Confirmation Number:	6130
Title of Invention:	CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	20995
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C6
Receipt Date:	25-SEP-2012
Filing Date:	01-NOV-2011
Time Stamp:	18:52:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	POA018P2C6.pdf	321901 ccd68430a5aeeaa7b55db35913e056b396f79d1c	no	2

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Information:	
Total Files Size (in bytes):	321901

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
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New International Application Filed with the USPTO as a Receiving Office
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www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/287,081	11/01/2011	Jeffrey C. Solomon	NETL.018P2C6

CONFIRMATION NO. 6130

POA ACCEPTANCE LETTER

79141
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

OC000000056853011

Date Mailed: 10/10/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/25/2012.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/mnguyen/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Electronically filed **

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Solomon, et al.	Confirmation No.:	6130
Serial No.:	13/287,081	Art Unit:	2827
Filed:	November 1, 2011	Examiner:	
For:	***CIRCUIT FOR MEMORY MODULE***	Attorney Docket No.:	NETL.018P2C6
		Date:	October 11, 2012

PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENTS to the CLAIMS are reflected in the listing of claims, which begins on Page 2 of this paper.

REMARKS begin on Page 5 of this paper.

IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Cancelled)

2. (New) A logic element to receive input control signals from a memory controller, the logic element comprising:

a first data line and a first data strobe line, the logic element to receive, in response to a first command from the memory controller, a first data signal via the first data line and a first data strobe signal via the first data strobe line, wherein the first command corresponding to a first set of input control signals;

a second data line and a second data strobe line, the logic element to receive, in response to a second command from the memory controller, a second data signal via the second data line and a second data strobe signal via the second data strobe line, wherein the second command corresponding to a second set of input control signals, the second data strobe signal partially overlapping in time with the first data strobe signal; and

a third data line coupled to the memory controller, the logic element to monitor commands from the memory controller and to generate a combined data signal on the third data line in response to the first command and the second command, the combined data signal combining at least part of the first data signal and at least part of the second data signal.

3. (New) The logic element of claim 2, wherein the logic element further comprises a third data strobe line, the logic element to generate a combined data strobe signal on the third data strobe line in response to the first command and the second command, the combined data strobe signal corresponding to the combined data signal and combining at least part of the first data strobe signal and part of the second data strobe signal.

4. (New) The logic element of Claim 3, wherein the combined data strobe signal has a timing relationship with respect to the combined data signal, and the combined data strobe signal is used to either validate or latch data in the combined data signal.

5. (New) The logic element of Claim 2, wherein the logic element further comprises a third data strobe line, and wherein the logic element selectively couples at least part of the first data strobe signal and at least part of the second data strobe signal to the third data strobe

line in response to the first command and the second command to form a combined data strobe signal.

6. (New) The logic element of Claim 2, further comprising a buffer to electrically and selectively isolate the first and second data lines from the third data line, wherein the logic element is configured to:

receive a third command from the memory controller, the third command corresponding to a third set of input control signals, the third set of input control signals including a plurality of address and control signals, wherein the third command is a load mode register command;

determine a column address strobe latency (CL) value using a subset of address signals of the plurality of address and control signals; and

determine a time delay using the CL value, the time delay corresponding to a first number of clock cycles.

7. (New) The logic element of Claim 6, wherein the subset of address signals include three address signals

8. (New) The logic element of Claim 6, wherein the buffer adds the first number of clock cycles time delay to the combined data signal and to the combined data strobe signal.

9. (New) The logic element of claim 2, wherein each set of input control signals of the first set of input control signals and the second set of input control signals include at least one chip select signal, at least one address signal, and at least one of a row access signal and a column access signal.

10. (New) The logic element of Claim 2, wherein the logic element comprises an integrated circuit.

11. (New) The logic element of Claim 2, wherein each of the first command and the second command comprises one or more of a read command and a read burst command.

12. (New) The logic element of Claim 2, wherein the first and second commands are successive commands.

13. (New) The logic element of Claim 2, wherein the first data signal includes one or more data values.

14. (New) The logic element of Claim 2, wherein part of the first data strobe signal overlaps with a preamble time interval of the second data strobe signal.

15. (New) The logic element of Claim 2, wherein the first data strobe signal has a first timing relationship with respect to the first data signal, and the first data strobe signal is used to either validate or latch data in the first data signal, and wherein the second data strobe signal has a second timing relationship with respect to the second data signal, and the second data strobe signal is used to either validate or latch data in the second data signal.

16. (New) The logic element of Claim 2, wherein the first data line and the first strobe line are coupled to at least one first memory device, and wherein the second data line and the second strobe line are coupled to at least one second memory device.

17. (New) The logic element of Claim 16, wherein the first command and the second command are back-to-back adjacent read commands crossing memory device boundaries.

18. (New) The logic element of Claim 1, further comprising:

a buffer to electrically and selectively isolate the first and second data lines from the third data line, the buffer including combinatorial logic, registers, and logic pipelines.

19. (New) The logic element of Claim 1, further comprising:

a buffer to electrically and selectively isolate the first and second data lines from the third data line, the buffer adding a one-clock cycle time delay to the first data signal when the first data signal is being transferred through the buffer from the first data line to the third data line in response to the first command, the buffer adding a one-clock cycle time delay to the second data signal when the second data signal is being transferred through the buffer from the second data line to the third data line in response to the second command

20. (New) The logic element of Claim 19, wherein the logic element provides functions of a data path multiplexer /demultiplexer using the one-clock cycle time delay.

21. (New) The logic element of Claim 1, wherein, during a time interval in which the first data strobe signal overlaps with the second data strobe signal, the first data strobe signal has a first voltage level corresponding to a first logic value, the second data strobe signal has a second voltage level corresponding to a second logic value, the first logic value being different from the second logic value.

REMARKS

Claim 1 is cancelled, and new claims 2-21 are added. Support for the newly added claims can be found throughout the specification and drawings. No new matter is added.

The Examiner is invited to contact the undersigned attorney at (650) 273-6008, if a telephone call could help answer any questions regarding this amendment or the application.

Respectfully submitted,

Date: October 11, 2012

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer Number 79141

Electronic Acknowledgement Receipt

EFS ID:	13968012
Application Number:	13287081
International Application Number:	
Confirmation Number:	6130
Title of Invention:	CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C6
Receipt Date:	11-OCT-2012
Filing Date:	01-NOV-2011
Time Stamp:	23:49:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Preliminary Amendment	PreliminaryAmendment10_11_12.pdf	92453 15168eac8e1c9094c857e5e7fd4bbd20a5edf7da	no	5

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Total Files Size (in bytes):	92453

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	
13/287,081	11/01/2011	☐ To be Mailed

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 10/11/2012

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $ =		OR	X $62=	0
Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $ =		OR	X $250=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/EAON SMALLWOOD/

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	14

Complete if Known	
Application Number	13/287,081
Filing Date	1-Nov-2011
First Named Inventor	Jeffrey C. Solomom
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C6

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	4218740	08-19-1980	MOTOROLA INC	
	2	4368515	01-11-983	Nielsen	
	3	4392212	07-05-1983	Miyasaka et al.	
	4	4633429	12-30-1986	Lewandowski et al.	
	5	4670748	06-02-1987	Williams	
	6	4706214	11-10-1987	Mitsubishi Denki Kabushiki Kaisha	
	7	4866603	09-02-1989	Chiba	
	8	4958322	09-18-1990	Kosugi et al.	
	9	4961172	10-02-1990	Shubat et al.	
	10	4961204	10-02-1990	Hitachi Ltd	
	11	4980850	12/25/1990	Morgan	
	12	5247643	09-21-1993	Shottan	
	13	5272664	12-21-1993	Silicon Graphics Inc	
	14	5345412	09-06-1994	Shiratsuchi	
	15	5357478	10-18-1994	Mitsubishi Electric Corp	
	16	5388072	02-07-1995	IBM	
	17	5392252	02-21-1995	Visi Technology Inc	
	18	5426753	06-20-1995	Moon	
	19	5483497	01-09-1996	Mochizuki et al.	
	20	5485589	01-16-1996	Dell Usa Lp	
	21	5495435	02-27-1996	Sugahara	
	22	5513135	04-30-1996	Dell et al.	
	23	5532954	07-02-1996	Bechtolsheim et al.	
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	25	5572691	11-05-1996	Koudmani	
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Complete if Known	
Application Number	13/287,081
Filing Date	1-Nov-2011
First Named Inventor	Jeffrey C. Solomom
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C6

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Filing Date	1-Nov-2011
First Named Inventor	Jeffrey C. Solomom
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C6

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Application Number:	13287081
International Application Number:	
Confirmation Number:	6130
Title of Invention:	CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
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Receipt Date:	07-DEC-2012
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Time Stamp:	18:42:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	COVER_NETL018P2C6.pdf	58909 73ad4a67641f3dbe60297e697ceced7de726af62	no	2

Warnings:

Information:

2	Information Disclosure Statement (IDS) Form (SB08)	IDS018P2C6.pdf	348185 6cf35f0ba1c35c2dae2a014c5d8b812e85330b49	no	14

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT

Applicant	:	Solomon et al.
App. No.	:	13/287,081
Filed	:	11/01/2011
For	:	CIRCUIT FOR MEMORY MODULE
Examiner	:	Unknown
Art Unit	:	2827
Conf No.	:	6130

CERTIFICATE OF EFS WEB TRANSMISSION

I hereby certify that this correspondence and any other attachment noted on the Automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web Server on:

December 7, 2012

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 330 references.

This application is related to commonly-owed co-pending U.S. Patent Application Serial No. 13/287,042, entitled "Circuit for Providing Chip-Select Signals to a Plurality of Ranks of a DDR Memory Module," filed on November 1, 2011 (referred hereafter as the "Related Application"). Copies of the foreign documents and/or their translation and non-patent literature listed in the Form PTO/SB/08a/b Equivalent submitted herewith can be found in the file wrapper of the Related Application. Applicant understands that the Examiner has access to sophisticated online Patent Office electronic systems that provide ready access to complete file histories including cited art. Thus, and are thus not submitted herewith. Thus, Applicant has not enclosed copies of these foreign documents and/or their translation and non-patent literature. If the Examiner cannot readily access these documents, Application would be pleased to provide copies of any of the foreign

documents and/or their translation and non-patent literature listed in the Form PTO/SB/08a/b Equivalent submitted herewith.

Applicant would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

This Information Disclosure Statement is being filed before the receipt of a first Office Action on the merits, and presumably no fee is required. If a first Office Action on the merits was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 50-5963.

Respectfully submitted,

Dated: December 7, 2012

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 273-6008

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	6

Complete if Known	
Application Number	13/287,081
Filing Date	01-Nov-2011
First Named Inventor	Jeffrey C. Solomom
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C6

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number / Number-Kind Code [2] (if known) / Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	4,249,253	02-03-1981	Gentili et al.	
	2	4,571,676	02-18-1986	Mantellina et al.	
	3	4,592,011	05-27-1986	Mantellina et al.	
	4	5,060,188	10-22-1991	Zulian et al.	
	5	5,463,590-A	10-31-1995	Watanabe	
	6	5,953,280-A	09-14-1999	Watsui	
	7	6,188,641-B1	02-13-2001	Uchida	
	8	6,205,516-B1	03-20-2001	Usami	
	9	6,438,062-B1	08-20-2002	Curtis	
	10	6,480,439-B2	11-12-2002	Tokutome et al.	
	11	US RE 36229	06-15-1999	Cady	
	12	8,250,295-B2	08-21-2012	Amidi et al.	
	13	Reexam Appl. No. 95/000,546 for U.S. Pat. No. 7,289,386 filed 05/11/2010; Owned by Netlist, Inc.			
	14	Reexam Appl. No. 95/000,577 for U.S. Pat. No. 7,289,386 filed 10/20/2010; Owned by Netlist, Inc.			
	15	Reexam Appl. No. 95/000,578 for U.S. Pat. No. 7,619,912 filed 10/20/2010; Owned by Netlist, Inc.			
	16	Reexam Appl. No. 95/000,579 for U.S. Pat. No. 7,619,912 filed 10/21/2010; Owned by Netlist, Inc.			
	17	Reexam App. No. 95/001,337 for U.S. Pat. No. 7,636,274 filed 06/0 4/2010; Owned by Netlist, Inc.			
	18	Reexam Appl. No. 95/001,381 for U.S. Pat. No. 7,532,537; filed 06/09/2010; Owned by Netlist, Inc.			
	19	Reexam Appl. No. 95/001,338; for U.S. Pat. No. 7,532,537 filed 04/19/2010; Owned by Netlist, Inc.			
	20	Reexam Appl. No. 95/001,758 for U.S. Pat. No. 7,864,627 filed 09/15/2011; Owned by Netlist, Inc.			
	21	Reexam Appl. No. 95/001,339 for U.S. Pat. No. 7,619,912; filed 06/08/2010; Owned by Netlist, Inc.			

EXAMINER **DATE CONSIDERED**

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	2	of	6

Complete if Known	
Application Number	13/287,081
Filing Date	01-Nov-2011
First Named Inventor	Jeffrey C. Solomom
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C6

US PATENT APPLICATIONS

Examiner Initials *	Cite No. [1]	Document Number	Filing Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	22	US20080046631A1	02-21-2008	Takaku et al.	
	23	Application Number 11/075,395, filed 03/07/2005; and its entire prosecution history.			
	24	Application Number 11/142,989, filed 12/07/2006; and its entire prosecution history.			
	25	Application Number 11/173,175, filed 07/01/2005; and its entire prosecution history.			
	26	Application Number 11/335,875, filed 01/19/2006; and its entire prosecution history.			
	27	Application Number 11/862,931, filed Sep. 27, 2007; and its entire prosecution history.			
	28	Application Number 12/577,682, filed 10/ 12/2009; and its entire prosecution history.			
	29	Application Number 12/629,827, filed 12/02/2009; and its entire prosecution history.			
	30	Application Number 12/902,073, filed 10/11/2010; (Prosecution history of Application Number 11/0125966)			
	31	Application Number 12/981,380, filed 12/29/2010; and its entire Prosecution History.			
	32	Application Number 12/981,380, filed 11/29/2010; and its entire Prosecution History.			
	33	Application Number 13/032,470, filed 02/22/2011; and its entire Prosecution History.			

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Filing Date	01-Nov-2011
First Named Inventor	Jeffrey C. Solomom
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C6

Sheet	3	of	6

US PATENT APPLICATIONS

Examiner Initials *	Cite No. [1]	Document Number	Filing Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	34	Application Number 13/154,172, filed 06/06/2011; and its entire prosecution history.			

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Foreign Patent Document	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	35	JP-2009-237492	09-09-1997	Toshiba Corp.	Machine Translation	√
	36	JP-2000-285674	10-13-2000	Fujitsu Ltd.	Translation of Abstract Only	
	37	JP-2002-184176	06-28-2002	NEC Tohoku Ltd.		√
	38	JP-2003-007963	01-10-2003	Hitachi Ltd.et al.	Machine Translation	√
	39	JP-2008-046989	02-28-2008	Fujitsu Ltd	Translation of Abstract Only	
	40	JP-2010-320270-A	12-04-1998	Matsushita Electric Inc. Co.	Translation	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	41	ANONYMOUS. (May 2002). "Hynix HYMD512G726(L)8-K/H/L Registered DDR SDRAM DIMM, 128Mx72 bits Product Description," Rev. 0.1/May, 02, pp. 1-16.	
	42	"Elipida Memory to Speak at Intel's Memory Implementers Forum Roundtable Event", Intel Developer Forum, [Online]. Retrieved from the Internet: <URSL: http://www.elpida.com/en/news/2004/02-18.html>, (Jun. 14, 2011), 1 pg. cited by examiner .	
	43	Google, Inc. v. Netlist, Inc., No. 4:08-cv-04144-SBA, Netlist Inc.'s Answer to Complaint and Counterclaim (N.D. Ca. Filed Nov. 18, 2008).	
	44	Google, Inc. v. Netlist, Inc., No. C 08-04144 SBA Google Inc.'s Invalidity Contentions Pursuant to PAT. L.F. 3-3, dated Apr. 13, 2009.	
	45	Google, Inc. v. Netlist, Inc., No. C08 04144, Complaint for Declaratory Relief, (N.D. Ca Dated Aug. 29, 2008).	
	46	Google, Inc. v. Netlist, Inc., No.4:08-cv-04144-SBA, Google Inc.'s Invalidity Contentions Pursuant to Pat. L.F. 3-3, dated 13 April 2009.	
	47	International Preliminary Report on Patentability for International Application No. PCT/US2010/040826, date of mailing November 28, 2011 (NETL.048VPC) in 34 pages.	

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Application Number	13/287,081
Filing Date	01-Nov-2011
First Named Inventor	Jeffrey C. Solomom
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C6

Sheet	4	of	6

NON PATENT LITERATURE DOCUMENTS

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	48	International Search Report and Written Opinion for Related Application No. PCT/US2010/040826, mailed on September 27, 2010, in 15 pages.	
	49	JEDEC Standard No. 21-C, 4.20.6-200 Pin. PC2700/PC2100/PC1600 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification, Revision 1.1, Release 11b, Apr. 26, 2002.	
	50	JEDEC Standard No. 21-C, 4.20-2-168 Pin, PC133 SDRAM Registered SO-DIMM, Reference Design Specification, Revision 1.02, Release 11. Published Oct. 2003.	
	51	Jedec Standard No. 21-C, DDR SDRAM PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, Revision 1.3, Release 11b, Jan. 2002.	
	52	Karabatsos, C., "Quad Band Memory (QBM) Technology", Kentron Technologies, Inc., Apr. 2001, pp. 1-5.	
	53	Letter from G. Hopkins Guy III, Orrick, Herrington & Sutcliffe LLP, to R. Scott Oliver, Morrison & Foerster, (Apr. 14, 2009).	
	54	MetaRAM, Inc. v. Netlist, Inc. No. 3:09-cv-01309-VRW, MetaRam's Reply to Netlist's Counterclaims, (N.D. Ca. Filed Jun. 3, 2009).	
	55	MetaRam, Inc. v. Netlist, Inc., No. 3:09-cv-01309-VRW, Netlist's Answer to Complaint and Counterclaims, (N.D. Ca, filed May 11, 2009).	
	56	MetaRAM, Inc. v. Netlist, Inc., No. C09 01309, Complaint for Patent Infringement, (N.D. Ca. Filed Mar. 25, 2009).	
	57	Micron "DDR2 SDRAM Registered DIMM (RDIMM)," 2003 Micron Technology, Inc. 18 pages.	
	58	Miles J. Murdocca et al., "Principles of Computer Architecture", Prentice Hall, Inc., Upper Saddle River, NJ, 2000, pp. 243-252.	
	59	Netlist, Inc. v. MetaRam, Inc., No. 09-165-GMS, MetaRAM, Inc.'s Answer and Affirmative Defenses to Plaintiff's Complaint, dated Apr. 20, 2009.	
	60	Netlist, Inc. v. MetaRAM, Inc., No. 1:09-ccv-00165-GMS, Complaint for Patent Infringement, (D. Del. Filed Mar. 12, 2009).	
	61	Non-Final Action Closing Prosecution mailed September 1, 2010, for Control No. 95/001,339, filed April 10, 2010, 17 pages.	
	62	Non-Final Action Closing Prosecution mailed June 21, 2011, for Control No. 95/001,381, filed June 9, 2010, 34 pages.	
	63	Non-Final Action Closing Prosecution mailed March 12, 2012, for Control No. 95/001,337, filed April 19, 2010, 33 pages.	
	64	Non-Final Action mailed August 27, 2010, for Control No. 95/000,546, filed May 11, 2010, 16 pages.	
	65	Non-Final Action mailed September 8, 2010, for Control No. 95/001,381, filed June 9, 2010, 17 pages.	
	66	Non-Final Action mailed April 4, 2011, for Control No. 95/001,339, filed April 20, 2010, 61 pages. (merged with 95/000,578 and 95/000,579)	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known	
Application Number	13/287,081
Filing Date	01-Nov-2011
First Named Inventor	Jeffrey C. Solomom
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C6

Sheet	5	of	6

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	67	Non-Final Action mailed June 15, 2011, for Control No. 95/001,381, filed June 9, 2010, 33 pages.	
	68	Non-Final Action mailed September 27, 2011, for Control No. 95/001,337, filed April 19, 2010, 19 pages.	
	69	Non-Final Action mailed October 4, 2011, for Control No. 95/001,339, filed April 20, 2010, 77 pages. (merged with 95/000,578 and 95/000,579)	
	70	Non-Final Action mailed October 14, 2011, for Control No. 95/001,339, filed April 30, 2010, 99 pages. (merged with 95/000,578 and 95/000,579)	
	71	Non-Final Office Action mailed November 16, 2011, for Application No. 95/001,758 filed September 14, 2011, 25 pages.	
	72	Order Granting Request for Inter Partes Reexamination mailed November 16, 2011, for Application No. 95/001,758, filed September 14, 2011, 13 pages.	
	73	Order Granting Request for Inter Partes Reexamination mailed August 9, 2010, for Control No. 95/000,546, filed May 11, 2010, 22 pages.	
	74	Order Granting Request for Inter Partes Reexamination mailed August 27, 2010, for Control No. 95/001,337, filed April 19, 2010, 21 pages.	
	75	Order Granting Request for Inter Partes Reexamination mailed September 1, 2010, for Control No. 95/001,339, filed April 20, 2010, 14 pages.	
	76	Order Granting Request for Inter Partes Reexamination mailed September 8, 2010, for Control No. 95/000,381, filed June 9, 2010, 21 pages.	
	77	Order Granting Request for Inter Partes Reexamination mailed January 14, 2011, for Control No. 95/000,579, filed October 21, 2010, 12 pages.	
	78	Order Granting Request for Inter Partes Reexamination mailed January 18, 2011, for Control No. 95/000,577, filed October 20, 2010, 17 pages.	
	79	Order Granting Request for Inter Partes Reexamination mailed January 18, 2011, for Control No. 95/000,578, filed October 20, 2010, 14 pages.	
	80	Request for Inter Partes Reexamination for U.S. Patent No. 8,250,295, filed September 15, 2012, 601 pages. (submitted in three parts.)	
	81	Right of appeal Notice mailed February 7, 2012, for Control No. 95/001,381, 33 pages.	
	82	Right of Appeal Notice mailed June 22, 2012, for Control No. 95/001,337, filed June 4 2010, 34 pages.	
	83	Russell, Gill, "Intel Micron Hybrid Memory Cube: The Future of Exascale Computing," Bright Side of News. Sept. 19, 2011, <http:www.brightsideofnews.com/news/2011/9/19/intel-mocron-hybrid-momory-cube-the-future-of-exascale-compting.aspx> Printed October 13, 2011 in 8 pages.	
	84	Sunaga et al. "An Enable Signal Circuit for Multiple Small Banks," IP.com, IPCOM000015887D, 2002.	

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	85	U.S. District Court Northern District of California, Case No. CV08 04144, GOOGLE INC. vs. NETLIST, INC., Attachment 1 to Exhibit B To Joint Claim Construction And Prehearing Statement, filed Jun. 12, 2009 in 7 pages.	
	86	US District Court Civil Docket; Google Inc. v. Netlist Inc.; 4:08cv04144; Date filed Aug. 29, 2008.	
	87	US District Court Civil Docket; Netlist Inc. v. Inphi Corporation; 2:09cv6900; Date filed Sep. 22, 2009. cited by other .	
	88	Written Opinion for International Application No. PCT/US2010/040826, date of mailing October 24, 2011 (NETL.048VPC) in 7 pages.	

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Electronic Acknowledgement Receipt

EFS ID:	14417478
Application Number:	13287081
International Application Number:	
Confirmation Number:	6130
Title of Invention:	CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/Jennifer Lu
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	NETL.018P2C6
Receipt Date:	07-DEC-2012
Filing Date:	01-NOV-2011
Time Stamp:	18:48:07
Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	COVER_NETL018P2C6b.pdf	60305 7ab7ae4f42ac83d520b9c8ac8540f64107cf92b0	no	2

Warnings:

Information:

2	Information Disclosure Statement (IDS) Form (SB08)	IDS018P2C6b.pdf	181105 ab0c5281195d2aaf9a0ee47c76be1c5b0f4771fd	no	6

Warnings:

Information:

This is not an USPTO supplied IDS fillable form

Total Files Size (in bytes):	241410

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT

Applicant	:	Solomon et al.
App. No.	:	13/287,081
Filed	:	11/01/2011
For	:	CIRCUIT FOR MEMORY MODULE
Examiner	:	Unknown
Art Unit	:	2827
Conf No.	:	6130

CERTIFICATE OF EFS WEB TRANSMISSION

I hereby certify that this correspondence and any other attachment noted on the Automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web Server on:

December 7, 2012

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 88 references.

On the Form PTO/SB/08a/b Equivalent, Applicant has listed 9 reexamination proceedings (citation nos. 13 through 21) and 12 prosecution file histories (citation nos. 23 through 34) for issued and/or pending applications. Applicant requests the Examiner to consider the entire prosecution histories in these other pending applications and patents when determining the patentability of the claims of the present application. Applicants understand that the Examiner has access to sophisticated online Patent Office electronic systems that provide ready access to complete file histories, including, for example, specification, drawings, claims, cited art, office actions, responses and notice of allowance. Thus, Applicant has not enclosed copies of these office actions and associated responses. If the Examiner cannot readily access these documents, Applicant would be pleased to provide any of the office actions and associated responses at any time upon request.

This application is related to commonly-owed co-pending U.S. Patent Application Serial No. 13/287,042, entitled "Circuit for Providing Chip-Select Signals to a Plurality of Ranks of a DDR Memory Module," filed on November 1, 2011 (referred hereafter as the "Related Application"). Copies of the foreign documents and/or their translation and non-patent literature listed in the Form PTO/SB/08a/b Equivalent submitted herewith can be found in the file wrapper of the Related Application. Applicant understands that the Examiner has access to the online Patent Office electronic systems that provide ready access to complete file histories including cited art. Thus, Applicant has not enclosed copies of these foreign documents and/or their translation and non-patent literature. If the Examiner cannot readily access these documents, Application would be pleased to provide copies of any of the foreign documents and/or their translation and non-patent literature listed in the Form PTO/SB/08a/b Equivalent submitted herewith.

Applicant would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

This Information Disclosure Statement is being filed before the receipt of a first Office Action on the merits, and presumably no fee is required. If a first Office Action on the merits was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 50-5963.

Respectfully submitted,

Dated: December 7, 2012

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 273-6008

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 04/08/2013
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

EXAMINER
SOFOCLEOUS, ALEXANDER

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 04/08/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/287,081	11/01/2011	Jeffrey C. Solomon	NETL.018P2C6	6130

TITLE OF INVENTION: CIRCUIT FOR MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$0	$0	$1780	07/08/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 04/08/2013
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/287,081	11/01/2011	Jeffrey C. Solomon	NETL.018P2C6	6130

TITLE OF INVENTION: CIRCUIT FOR MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$0	$0	$1780	07/08/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
SOFOCLEOUS, ALEXANDER	2824	711-105000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

PTOL-85 (Rev. 02/11)

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29	NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27	NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status.	NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/287,081	11/01/2011	Jeffrey C. Solomon	NETL.018P2C6	6130

79141 7590 04/08/2013
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

EXAMINER
SOFOCLEOUS, ALEXANDER

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 04/08/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 97 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 97 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	13/287,081	SOLOMON ET AL.	
	Examiner	Art Unit	
	ALEXANDER SOFOCLEOUS	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Application filed November 1, 2011*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *2-21*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/ALEXANDER SOFOCLEOUS/
Primary Examiner, Art Unit 2824

DETAILED ACTION

1. This action is responsive to the following communication: Application filed on November 01, 2011, the two Information Disclosure Statements filed on December 7, 2012.

2. Claims 2-21 are pending. Claim 1 is cancelled. Claims 7, 18, 19, and 21 are amended by Examiner's Amendment to correct claim dependency and add a period. Claim 2 is independent.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Jamie Zheng on March 20, 2013 and March 21, 2013.

In the Claims, **Claim 7**, add a period (--.--) at the end of the clause.

In the Claims, **Claim 18**, line 1, change "Claim 1" to --Claim 2--.

In the Claims, **Claim 19**, line 1, change "Claim 1" to --Claim 2--.

Also in **Claim 19**, add a period (--.--) at the end of the clause.

In the Claims, **Claim 21**, line 1, change "Claim 1" to --Claim 2--.

Prosecution Histories for Parent applications and Reexam proceedings

4. It is noted that the parent applications' claims, very generally (and in no way limiting what those claims cover), relate a memory module having circuitry that receives rank select signals from a memory controller (that expects the memory module to support a certain number of ranks) and doubles the amount the rank select signals to select one of the ranks on the memory (wherein the actual ranks on the memory module are double what the memory controller is expecting) in reliance upon several signals including a phase-locked clock signal from the phase-lock loop.

As merely an example of the differences in the instant application (and in no way limiting the subject matter claimed), the following quick summary is provided. This application's claims appear to relate to the features shown in, e.g., Figures 7-8B; *namely*, the back-to-back read operations in which a DQS collision is handled such that data from the two successive read operations are output back-to-back, undisturbed (see Spec. 17-20; ¶¶ [0058], [0068]).

In this regard, the parent application prosecution histories are presently considered not material to patentability of these claims. Nevertheless, they have been considered because it is understood that when deciding what to cite and what not to cite, a "better safe than sorry" approach is favored for a future patentee.

5. The parent patents' corresponding reexamination ("reexam") proceedings' histories were considered during prosecution of the parent applications because the issues raised therein were material to those parent claims. But, here because the distinct subject matter claimed as discussed *supra*, their proceedings histories are considered not material.

In short, the cited reexams (95/000,546; 95/000,577; 95/000,578; 95/000,579; 95/001,337; 95/001,338; 95/001,339; 95/001,381; 95/001,1758) have been considered.

Information Disclosure Statement

6. Acknowledgment is made of Applicants' two Information Disclosure Statement (IDS) Form PTO-1449 filed on December 7, 2012. These IDS have been considered.

Applicant is thanked for identifying related application 13/287,042 (presently not examined) for which the cited Foreign publications and non-patent literature are available. The Examiner has reviewed and considered these publications.

In passing, it is noted that citation 36 (for JP-2000-285674) has been struck-through because a copy does not appear to be on record; Nevertheless, this JP publication corresponds to US 6,188,641 (citation 7) and has been considered.

Citations 35 and 40 were cosmetically corrected to from "JP-2009-237492" and "JP-2010-320270-A" to --JP 09-237492-- and --JP 10-320270--, respectively.

Allowable Subject Matter

7. **Claims 2-21 are allowed.**

The following is an examiner's statement of reasons for allowance:

With respect to independent claim 2, there is no teaching, suggestion, or motivation for combination in the prior art to a first data line and a first data strobe line, the logic element to receive, in response to a first command from the memory controller,

a first data signal via the first data line and a first data strobe signal via the first data strobe line, wherein the first command corresponding to a first set of input control signals;

a second data line and a second data strobe line, the logic element to receive, in response to a second command from the memory controller, a second data signal via the second data line and a second data strobe signal via the second data strobe line, wherein the second command corresponding to a second set of input control signals, the second data strobe signal partially overlapping in time with the first data strobe signal; and

a third data line coupled to the memory controller, the logic element to monitor commands from the memory controller and to generate a combined data signal on the third data line in response to the first command and the second command, the combined data signal combining at least part of the first data signal and at least part of the second data signal.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CONCLUSION

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

None of the prior art, alone or in combination, meet all of the following limitations:

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/ALEXANDER SOFOCLEOUS/
Primary Examiner, Art Unit 2824

1. (Cancelled)

2. A circuit to receive input control signals from a memory controller, the circuit comprising:

a first data line and a first data strobe line, the circuit to receive, in response to a first command from the memory controller, a first data signal via the first data line and a first data strobe signal via the first data strobe line, wherein the first command corresponding to a first set of input control signals;

a second data line and a second data strobe line, the circuit to receive, in response to a second command from the memory controller, a second data signal via the second data line and a second data strobe signal via the second data strobe line, wherein the second command corresponding to a second set of input control signals, the second data strobe signal partially overlapping in time with the first data strobe signal;

a third data line coupled to the memory controller; and

a logic element to monitor commands from the memory controller and to generate a combined data signal on the third data line in response to the first command and the second command, the combined data signal combining at least part of the first data signal and at least part of the second data signal.

3. The circuit of claim 2, wherein the circuit further comprises a third data strobe line, the logic element to generate a combined data strobe signal on the third data strobe line in response to the first command and the second command, the combined data strobe signal corresponding to the combined data signal and combining at least part of the first data strobe signal and part of the second data strobe signal.

4. The circuit of Claim 3, wherein the combined data strobe signal has a timing relationship with respect to the combined data signal, and the combined data strobe signal is used to either validate or latch data in the combined data signal.

5. The circuit of Claim 2, wherein the circuit further comprises a third data strobe line, and wherein the logic element selectively couples at least part of the first data strobe signal and at least part of the second data strobe signal to the third data strobe line in response to the first command and the second command to form a combined data strobe signal.

6. The circuit of Claim 2, wherein the logic element is configured to:

respond to a third command from the memory controller, the third command corresponding to a third set of input control signals, the third set of input control signals including a plurality of address and control signals, wherein the third command is a load mode register command;

determine a column address strobe latency (CL) value using a subset of address signals of the plurality of address and control signals; and

determine a time delay using the CL value, the time delay corresponding to a first number of clock cycles.

7. The circuit of Claim 6, wherein the subset of address signals include three address signals.

8. The circuit of Claim 6, wherein the logic element includes a buffer to electrically and selectively isolate the first and second data lines from the third data line, the buffer adds the time delay corresponding to the first number of clock cycles to the combined data signal and to the combined data strobe signal.

9. The circuit of claim 2, wherein each set of input control signals of the first set of input control signals and the second set of input control signals include at least one chip select signal, at least one address signal, and at least one of a row access signal and a column access signal.

10. The circuit of Claim 2, wherein the circuit comprises one or more integrated circuit.

11. The circuit of Claim 2, wherein each of the first command and the second command comprises one or more of a read command and a read burst command.

12. The circuit of Claim 2, wherein the first and second commands are successive commands.

13. The circuit of Claim 2, wherein the first data signal includes one or more data values.

14. The circuit of Claim 2, wherein part of the first data strobe signal overlaps with a preamble time interval of the second data strobe signal.

15. The circuit of Claim 2, wherein the first data strobe signal has a first timing relationship with respect to the first data signal, and the first data strobe signal is used to either validate or latch data in the first data signal, and wherein the second data strobe signal has a second timing relationship with respect to the second data signal, and the second data strobe signal is used to either validate or latch data in the second data signal.

16. The circuit of Claim 2, wherein the first data line and the first strobe line are coupled to at least one first memory device, and wherein the second data line and the second strobe line are coupled to at least one second memory device.

17. The circuit of Claim 16, wherein the first command and the second command are back-to-back adjacent read commands crossing memory device boundaries.

18. The circuit of Claim 2, further comprising:

a buffer to electrically and selectively isolate the first and second data lines from the third data line, the buffer including combinatorial logic, registers, and pipelines.

19. The circuit of Claim 2, further comprising:

a buffer to electrically and selectively isolate the first and second data lines from the third data line, the buffer adding a one-clock cycle time delay to the first data signal when the first data signal is being transferred through the buffer from the first data line to the third data line in response to the first command, the buffer adding a one-clock cycle time delay to the second data signal when the second data signal is being transferred through the buffer from the second data line to the third data line in response to the second command.

20. The circuit of Claim 19, wherein the logic element provides functions of a data path multiplexer /demultiplexer using the one-clock cycle time delay.

21. The circuit of Claim 2, wherein, during a time interval in which the first data strobe signal overlaps with the second data strobe signal, the first data strobe signal has a first voltage level corresponding to a first logic value, the second data strobe signal has a second voltage level corresponding to a second logic value, the first logic value being different from the second logic value.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Art Unit	2827
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Attorney Docket Number	NETL.018P2C6

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Complete if Known	
Application Number	13/287,081
Filing Date	1-Nov-2011
First Named Inventor	Jeffrey C. Solomom
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C6

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Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Complete if Known	
Application Number	13/287,081
Filing Date	1-Nov-2011
First Named Inventor	Jeffrey C. Solomom
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C6

Sheet	12	of	14

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Corporation, Defendant Inphi Corporation's Answer to Plaintiff's First Amended Complaint for Patent Infringement, filed Feb. 11, 2010 in 9 pages. cited by other .	
	302	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Defendant Inphi Corporation's Notice of Motion and Motion for Stay Pending Reexaminations and Interference Proceeding Regarding the Patents-In-Suit; Memorandum of Points and Authorities in Support Thereof, filed Apr. 21, 2010 in 28 pages. cited by other .	
	303	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Plaintiff Netlist Inc's Opposition to Defendant Inphi Corporation's Motion for Stay Pending Reexaminations and Interference Proceedings Regarding the Patents-In-Suit, filed May 3, 2010 in 23 pages. cited by other .	
	304	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. Inphi Corporation, Plaintiff Netlist, Inc's First Amended Complaint For Patent Infringement, filed Dec. 23, 2009 in 8 pages. cited by other .	
	305	U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Defendant Netlist, Inc.'s Claim Construction Reply Brief, filed Sep. 22, 2009 in 19 pages. cited by other .	
	306	U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Defendant Netlist, Inc.'s Opening Claim Construction Brief, filed Jul. 28, 2009 in 21 pages. cited by other .	
	307	U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Defendant Netlist, Inc.'s Opposition to Google Inc's Motion for Summary Judgment of Invalidity, filed Jul. 6, 2010 in 13 pages. cited by other .	
	308	U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Exhibit A To Joint Claim Construction And Prehearing Statement, filed Jun. 12, 2009 in 2 pages. cited by other .	
	309	U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Exhibit B to Joint Claim Construction and Prehearing Statement, filed Jun. 12, 2009 in 36 pages. cited by other .	
	310	U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Joint Claim Construction and Prehearing Statement, filed Jun. 12, 2009 in 5 pages. cited by other .	
	311	U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Netlist, Inc.'s Answer to Complaint and Counterclaims, filed Nov. 18, 2008 in 9 pages. cited by other .	
	312	U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Order Re Claim Construction, filed Nov. 16, 2009 in 1 page. cited by other .	
	313	U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Plaintiff Google's Reply to Counterclaims, filed Dec. 8, 2008 in 4 pages. cited by	

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		other .	
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	317	U.S. District Court Northern District of California, Case No. CV08 04144, GOOGLE INC. vs. NETLIST, INC., Appendix 1 To Google's Responsive Claim Construction Brief, filed Aug. 25, 2009 in 4 pages. cited by other .	
	318	U.S. District Court Northern District of California, Case No. CV08 04144, GOOGLE INC. vs. NETLIST, INC., Attachment 2 To Exhibit B To Joint Claim Construction And Prehearing Statement, filed Jun. 12, 2009 in 12 pages. cited by other .	
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	321	U.S. District Court Northern District of California, Case No. CV09 05718, NETLIST, INC. vs. GOOGLE, INC., Defendant Google Inc's Responsive Claim Construction Brief, filed Aug. 4, 2010 in 27 pages. cited by other .	
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	325	U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Joint Claim Construction And Prehearing Statement Under Patent Local Rule 4-3, filed Jun. 25, 2010 in 5 pages. cited by other .	

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First Named Inventor	Jeffrey C. Solomom
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Attorney Docket Number	NETL.018P2C6

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	326	U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Plaintiff Netlist, Inc.'s Reply to Defendant Google Inc.'s Counterclaim, filed Mar. 8, 2010 in 11 pages. cited by other .	
	327	U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Plaintiff Netlist, Inc's Opening Claim Construction Brief, filed Jul. 16, 2010 in 29 pages. cited by other .	
	328	US District Court Civil Docket; Netlist Inc. v. Google Inc.; 4:09cv5718; Date filed Dec. 4, 2009. In 10 pages. cited by other .	
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First Named Inventor	Jeffrey C. Solomom
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C6

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US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known) Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	4,249,253	02-03-1981	Gentili et al.	
	2	4,571,676	02-18-1986	Mantellina et al.	
	3	4,592,011	05-27-1986	Mantellina et al.	
	4	5,060,188	10-22-1991	Zulian et al.	
	5	5,463,590-A	10-31-1995	Watanabe	
	6	5,953,280-A	09-14-1999	Watsui	
	7	6,188,641-B1	02-13-2001	Uchida	
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	9	6,438,062-B1	08-20-2002	Curtis	
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	11	US RE 36229	06-15-1999	Cady	
	12	8,250,295-B2	08-21-2012	Amidi et al.	
	13	Reexam Appl. No. 95/000,546 for U.S. Pat. No. 7,289,386 filed 05/11/2010; Owned by Netlist, Inc.			
	14	Reexam Appl. No. 95/000,577 for U.S. Pat. No. 7,289,386 filed 10/20/2010; Owned by Netlist, Inc.			
	15	Reexam Appl. No. 95/000,578 for U.S. Pat. No. 7,619,912 filed 10/20/2010; Owned by Netlist, Inc.			
	16	Reexam Appl. No. 95/000,579 for U.S. Pat. No. 7,619,912 filed 10/21/2010; Owned by Netlist, Inc.			
	17	Reexam App. No. 95/001,337 for U.S. Pat. No. 7,636,274 filed 06/0 4/2010; Owned by Netlist, Inc.			
	18	Reexam Appl. No. 95/001,381 for U.S. Pat. No. 7,532,537; filed 06/09/2010; Owned by Netlist, Inc.			
	19	Reexam Appl. No. 95/001,338; for U.S. Pat. No. 7,532,537 filed 04/19/2010; Owned by Netlist, Inc.			
	20	Reexam Appl. No. 95/001,758 for U.S. Pat. No. 7,864,627 filed 09/15/2011; Owned by Netlist, Inc.			
	21	Reexam Appl. No. 95/001,339 for U.S. Pat. No. 7,619,912; filed 06/08/2010; Owned by Netlist, Inc.			

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Sheet	2	of	6

US PATENT APPLICATIONS

Examiner Initials *	Cite No. [1]	Document Number	Filing Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	22	US20080046631A1	02-21-2008	Takaku et al.	
	23	Application Number 11/075,395, filed 03/07/2005; and its entire prosecution history.			
	24	Application Number 11/142,989, filed 12/07/2006; and its entire prosecution history.			
	25	Application Number 11/173,175, filed 07/01/2005; and its entire prosecution history.			
	26	Application Number 11/335,875, filed 01/19/2006; and its entire prosecution history.			
	27	Application Number 11/862,931, filed Sep. 27, 2007; and its entire prosecution history.			
	28	Application Number 12/577,682, filed 10/ 12/2009; and its entire prosecution history.			
	29	Application Number 12/629,827, filed 12/02/2009; and its entire prosecution history.			
	30	Application Number 12/902,073, filed 10/11/2010; (Prosecution history of Application Number 11/0125966)			
	31	Application Number 12/981,380, filed 12/29/2010; and its entire Prosecution History.			
	32	Application Number 12/981,380, filed 11/29/2010; and its entire Prosecution History.			
	33	Application Number 13/032,470, filed 02/22/2011; and its entire Prosecution History.			

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	34	Application Number 13/154,172, filed 06/06/2011; and its entire prosecution history.			

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Examiner Initials *	Cite No. [1]	Foreign Patent Document	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
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	40	JP 10-320270 ~~JP-2010-320270-A~~	12-04-1998	Matsushita Electric Inc. Co.	Translation	

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	42	"Elipida Memory to Speak at Intel's Memory Implementers Forum Roundtable Event", Intel Developer Forum, [Online]. Retrieved from the Internet: <URSL: http://www.elpida.com/en/news/2004/02-18.html>, (Jun. 14, 2011), 1 pg. cited by examiner .	
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	49	JEDEC Standard No. 21-C, 4.20.6-200 Pin. PC2700/PC2100/PC1600 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification, Revision 1.1, Release 11b, Apr. 26, 2002.	
	50	JEDEC Standard No. 21-C, 4.20-2-168 Pin, PC133 SDRAM Registered SO-DIMM, Reference Design Specification, Revision 1.02, Release 11. Published Oct. 2003.	
	51	Jedec Standard No. 21-C, DDR SDRAM PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, Revision 1.3, Release 11b, Jan. 2002.	
	52	Karabatsos, C., "Quad Band Memory (QBM) Technology", Kentron Technologies, Inc., Apr. 2001, pp. 1-5.	
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	57	Micron "DDR2 SDRAM Registered DIMM (RDIMM)," 2003 Micron Technology, Inc. 18 pages.	
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	64	Non-Final Action mailed August 27, 2010, for Control No. 95/000,546, filed May 11, 2010, 16 pages.	
	65	Non-Final Action mailed September 8, 2010, for Control No. 95/001,381, filed June 9, 2010, 17 pages.	
	66	Non-Final Action mailed April 4, 2011, for Control No. 95/001,339, filed April 20, 2010, 61 pages. (merged with 95/000,578 and 95/000,579)	

EXAMINER /Alexander Sofocleous/ **DATE CONSIDERED** 03/20/2013

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.[1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /AGS/

PTO/SB/08a/b(07-09)
Approved for use through 7/31/2012. OMB 0651-0031
US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Use as many sheets as necessary)

Complete if Known	
Application Number	13/287,081
Filing Date	01-Nov-2011
First Named Inventor	Jeffrey C. Solomom
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C6

Sheet	5	of	6

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	67	Non-Final Action mailed June 15, 2011, for Control No. 95/001,381, filed June 9, 2010, 33 pages.	
	68	Non-Final Action mailed September 27, 2011, for Control No. 95/001,337, filed April 19, 2010, 19 pages.	
	69	Non-Final Action mailed October 4, 2011, for Control No. 95/001,339, filed April 20, 2010, 77 pages. (merged with 95/000,578 and 95/000,579)	
	70	Non-Final Action mailed October 14, 2011, for Control No. 95/001,339, filed April 30, 2010, 99 pages. (merged with 95/000,578 and 95/000,579)	
	71	Non-Final Office Action mailed November 16, 2011, for Application No. 95/001,758 filed September 14, 2011, 25 pages.	
	72	Order Granting Request for Inter Partes Reexamination mailed November 16, 2011, for Application No. 95/001,758, filed September 14, 2011, 13 pages.	
	73	Order Granting Request for Inter Partes Reexamination mailed August 9, 2010, for Control No. 95/000,546, filed May 11, 2010, 22 pages.	
	74	Order Granting Request for Inter Partes Reexamination mailed August 27, 2010, for Control No. 95/001,337, filed April 19, 2010, 21 pages.	
	75	Order Granting Request for Inter Partes Reexamination mailed September 1, 2010, for Control No. 95/001,339, filed April 20, 2010, 14 pages.	
	76	Order Granting Request for Inter Partes Reexamination mailed September 8, 2010, for Control No. 95/000,381, filed June 9, 2010, 21 pages.	
	77	Order Granting Request for Inter Partes Reexamination mailed January 14, 2011, for Control No. 95/000,579, filed October 21, 2010, 12 pages.	
	78	Order Granting Request for Inter Partes Reexamination mailed January 18, 2011, for Control No. 95/000,577, filed October 20, 2010, 17 pages.	
	79	Order Granting Request for Inter Partes Reexamination mailed January 18, 2011, for Control No. 95/000,578, filed October 20, 2010, 14 pages.	
	80	Request for Inter Partes Reexamination for U.S. Patent No. 8,250,295, filed September 15, 2012, 601 pages. (submitted in three parts.)	
	81	Right of appeal Notice mailed February 7, 2012, for Control No. 95/001,381, 33 pages.	
	82	Right of Appeal Notice mailed June 22, 2012, for Control No. 95/001,337, filed June 4 2010, 34 pages.	
	83	Russell, Gill, "Intel Micron Hybrid Memory Cube: The Future of Exascale Computing," Bright Side of News. Sept. 19, 2011, <http:www.brightsideofnews.com/news/2011/9/19/intel-mocron-hybrid-momory-cube-the-future-of-exascale-compting.aspx> Printed October 13, 2011 in 8 pages.	
	84	Sunaga et al. "An Enable Signal Circuit for Multiple Small Banks," IP.com, IPCOM000015887D, 2002.	

EXAMINER /Alexander Sofocleous/ **DATE CONSIDERED** 03/20/2013

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PTO/SB/08a/b(07-09)
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Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C6

Sheet	6	of	6

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	85	U.S. District Court Northern District of California, Case No. CV08 04144, GOOGLE INC. vs. NETLIST, INC., Attachment 1 to Exhibit B To Joint Claim Construction And Prehearing Statement, filed Jun. 12, 2009 in 7 pages.	
	86	US District Court Civil Docket; Google Inc. v. Netlist Inc.; 4:08cv04144; Date filed Aug. 29, 2008.	
	87	US District Court Civil Docket; Netlist Inc. v. Inphi Corporation; 2:09cv6900; Date filed Sep. 22, 2009. cited by other .	
	88	Written Opinion for International Application No. PCT/US2010/040826, date of mailing October 24, 2011 (NETL.048VPC) in 7 pages.	

EXAMINER /Alexander Sofocleous/ **DATE CONSIDERED** 03/20/2013

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /AGS/

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13287081	SOLOMON ET AL.
	Examiner	**Art Unit**
	ALEXANDER SOFOCLEOUS	2824

CPC- SEARCHED

Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner

US CLASSIFICATION SEARCHED

Class	Subclass	Date	Examiner

SEARCH NOTES

Search Notes	Date	Examiner
711/104, 105, 115, 167 (keyword search only - see EAST search history)	03/19/2013	AGS
365/193 (keyword search only - see EAST search history)	03/19/2013	AGS
reviewed parent application histories	03/20/2013	AGS
see EAST search history	03/23/2013	AGS

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
711	105, 167	03/19/2013	AGS
365	193	03/19/2013	AGS

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S42	1	("6188641").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/03/20 13:44
S41	1	("7472220").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/03/20 12:12
S35	8	S29 (S33).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2013/03/19 20:22
S34	61	S29 S33	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2013/03/19 20:22
S33	621	strobe with (conflict$3 or overlap$4 or compet$3 or contention or contend$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2013/03/19 20:22
S32	15	S29 (S30).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2013/03/19 20:21
S31	88	S29 S30	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2013/03/19 20:21
S30	2015	strobe with (conflict$3 or overlap$4 or compet$3 or conten$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2013/03/19 20:21
S29	8703	((365/193) or (711/104,105,115,167)).CCLS.	US-PGPUB; USPAT;	OR	OFF	2013/03/19 20:20

			USOCR			
S28	11	(S24 or S25) S27 (pre$1amble)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2013/03/19 20:13
S27	5627	successive near2 (command or read)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2013/03/19 20:13
S26	18	(S24 or S25) S23 (pre$1amble)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2013/03/19 20:13
S25	2242	(711/105).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/03/19 20:13
S24	1628	(365/193).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/03/19 20:13
S23	294	((strobe or dqs) with colli$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2013/03/19 20:13
S22	75	(S17 or S18) S21	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2013/03/19 13:02
S21	5627	successive near2 (command or read)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2013/03/19 13:02
S20	28	(S17 or S18) S9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2013/03/19 13:01
S19	62	S17 S18	US-PGPUB; USPAT; USOCR; FPRS; EPO;	AND	ON	2013/03/19 13:01

			JPO; DERWENT; IBM_TDB			
S18	2242	(711/105).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/03/19 13:01
S17	1628	(365/193).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/03/19 13:01
S16	29	("20020091958" | "20020122348" | "5457659" | "6061292" | "6240042" | "6317369" | "6381194" | "6392946" | "6600681" | "6603706" | "6615345" | "6681301").PN. OR ("6819599").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2013/03/19 12:58
S15	1	(10/210483).APP.	USPAT; USOCR	AND	ON	2013/03/19 12:58
S14	12	("20040022088" | "5896347" | "6215710" | "6321343" | "6557071" | "6570815" | "7230466").PN. OR ("7362648").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2013/03/19 12:56
S13	1	(11/251787).APP.	USPAT; USOCR	AND	ON	2013/03/19 12:55
S12	1	(10/277066).APP.	USPAT; USOCR	AND	ON	2013/03/19 12:53
S11	1	("6021264").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/03/19 12:50
S10	142	((strobe or dqs) with colli$4) same memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2013/03/19 12:48
S9	294	((strobe or dqs) with colli$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2013/03/19 12:45
S8	1	(second adj2 (strobe or dqs)) with (first adj2 (strobe or dqs)) with colli$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2013/03/19 12:42
S7	13	("20020079943" | "20030147299" | "20050018494" | "20090161454" | "4133050" | "4600845" | "4970687" | "6046616" | "6215726" | "6563759" | "7016237" | "7463534" | "7791965").PN. OR ("7990783").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2013/03/19 12:31
S6	1109	(second adj2 (strobe or dqs)) with (first adj2 (strobe or dqs))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	AND	OFF	2013/03/18 16:35

			DERWENT; IBM_TDB			
S4	2	(11/335875).APP.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/02/27 16:50
S3	9	(second adj2 (strobe or dqs)) with overlap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2013/02/27 16:46
S2	68	((data adj strobe) or dqs) with overlap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2013/02/27 16:34
S1	0	(13/287081).APP.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/02/27 16:32

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S40	8	S37 S38	US-PGPUB; USPAT; UPAD	AND	ON	2013/03/19 20:24
S39	58	S36 S38	US-PGPUB; USPAT; UPAD	AND	ON	2013/03/19 20:24
S38	8614	((365/193) or (711/104,105,115,167)).CCLS.	US-PGPUB; USPAT; UPAD	OR	OFF	2013/03/19 20:24
S37	60	(strobe with (conflict$3 or overlap$4 or compet$3 or contention or contend$3)).clm.	US-PGPUB; USPAT; UPAD	AND	ON	2013/03/19 20:24
S36	515	strobe with (conflict$3 or overlap$4 or compet$3 or contention or contend$3)	US-PGPUB; USPAT; UPAD	AND	ON	2013/03/19 20:24
S5	0	"Term Removed"	US-PGPUB; USPAT; UPAD	OR	OFF	2013/02/27 16:32

3/23/2013 9:10:19 PM
C:\Users\asofocleous\Documents\EAST\Workspaces\13287081.wsp

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13287081	SOLOMON ET AL.
	Examiner	**Art Unit**
	ALEXANDER SOFOCLEOUS	2824

CPC

Symbol	Type	Version

CPC Combination Sets

Symbol	Type	Set	Ranking	Version

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
711	105	G 0 6 F 13 / 00 (2006.01.01)	

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
365	193				
711	115	167			

NONE (Assistant Examiner)	(Date)	Total Claims Allowed: 20	
/ALEXANDER SOFOCLEOUS/ Primary Examiner.Art Unit 2824 (Primary Examiner)	03/23/2013 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 7

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13287081	SOLOMON ET AL.
	Examiner	**Art Unit**
	ALEXANDER SOFOCLEOUS	2824

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/ALEXANDER SOFOCLEOUS/ Primary Examiner.Art Unit 2824 (Primary Examiner)	03/23/2013 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 7

U.S. Patent and Trademark Office

Part of Paper No. 20130315

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13287081	SOLOMON ET AL.
	Examiner	**Art Unit**
	ALEXANDER SOFOCLEOUS	2824

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1	16	17												
1	2	17	18												
2	3	18	19												
3	4	19	20												
4	5	20	21												
5	6														
6	7														
7	8														
8	9														
9	10														
10	11														
11	12														
12	13														
13	14														
14	15														
15	16														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/ALEXANDER SOFOCLEOUS/ Primary Examiner.Art Unit 2824 (Primary Examiner)	03/23/2013 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 7

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BIB DATA SHEET

CONFIRMATION NO. 6130

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/287,081	11/01/2011 RULE	711	2824	NETL.018P2C6

APPLICANTS

INV001Jeffrey C. Solomon, Irvine, CA;
INV002Jayesh R. Bhakta, Cerritos, CA;

**** CONTINUING DATA ***************************

This application is a CON of 13/032,470 02/22/2011 PAT 8081536
which is a CON of 12/955,711 11/29/2010 PAT 7916574
which is a CON of 12/629,827 12/02/2009 PAT 7881150
which is a CON of 12/408,652 03/20/2009 PAT 7636274
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7289386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7286436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004
and claims benefit of 60/590,038 07/21/2004

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

11/14/2011

Foreign Priority claimed	☐ Yes ☑ No		STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119(a-d) conditions met	☐ Yes ☑ No	☐ Met after Allowance	CA	23	1	1
Verified and Acknowledged	/ALEXANDER SOFOCLEOUS/ Examiner's Signature	Initials				

ADDRESS

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306
UNITED STATES

TITLE

CIRCUIT FOR MEMORY MODULE

FILING FEE RECEIVED		
1250	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/287,081	11/01/2011	Jeffrey C. Solomon	NETL.018P2C6	6130

79141 7590 04/25/2013
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

EXAMINER
SOFOCLEOUS, ALEXANDER

ART UNIT	PAPER NUMBER
2824	

NOTIFICATION DATE	DELIVERY MODE
04/25/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jz@jzpatent.com

Applicant-Initiated Interview Summary	Application No.	Applicant(s)	
	13/287,081	SOLOMON ET AL.	
	Examiner	Art Unit	
	ALEXANDER SOFOCLEOUS	2824	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Alex Sofocleous (PTO personnel)*. (3)_____.

(2) *Jamie Zheng (app's rep*. (4)_____.

Date of Interview: *16 April 2013*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☐103 ☒Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *2-21*.

Identification of prior art discussed: *none*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

On April 16, 2013, Applicant brought to the attention of the Examiner that the prior Notice of Allowance appeared to be missing portions in the Detailed Action. It was agreed to correct the paperwork to reflect the correct Examiner's Amendment, the corresponsing allowable subject matter, and the closest art of record .

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/ALEXANDER SOFOCLEOUS/ Primary Examiner, Art Unit 2824	

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

SUPPLEMENTAL Notice of Allowability	Application No.	Applicant(s)	
	13/287,081	SOLOMON ET AL.	
	Examiner	Art Unit	
	ALEXANDER SOFOCLEOUS	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Application filed 11/1/11 and supplemental to the NOA mailed 4/8/13*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *2-21*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/ALEXANDER SOFOCLEOUS/
Primary Examiner, Art Unit 2824

DETAILED ACTION

1. THIS ACTION IS SUPPLEMENTAL TO THE NOTICE OF ALLOWANCE MAILED APRIL 8, 2013 and REPLACES THE PRIOR "DETAILED ACTION."[1]

2. This action is responsive to the following communication: Application filed on November 01, 2011, the two Information Disclosure Statements filed on December 7, 2012.

3. Claims 2-21 are pending. Claim 1 is cancelled. Claims 7, 18, 19, and 21 are amended by Examiner's Amendment to correct claim dependency and add a period. Claim 2 is independent.

EXAMINER'S AMENDMENT

4. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Jamie Zheng on March 20, 2013 and March 21, 2013.

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[1] There appears to have been computer problems, which resulted an incomplete Notice of Allowance being mailed. The incomplete NOA omitted the full Examiner's Amendment to the claims, the corresponding allowable subject matter, and the discussion of the most relevant prior art. Attempts were made to recover the correct NOA's Detailed Action to no avail; the other forms have been reviewed and were correct.

This Notice of Allowance replaces the prior Detailed Action only, because the other forms are correct. The prior Detailed Action from the Notice of Allowance mailed 4/8/13 should be disregarded.

In the Claims, **replace Claim 2** with the following:

--2. (Currently Amended) A circuit to receive input control signals from a memory controller, the circuit comprising:

a first data line and a first data strobe line, the circuit to receive, in response to a first command from the memory controller, a first data signal via the first data line and a first data strobe signal via the first data strobe line, wherein the first command corresponding to a first set of input control signals;

a second data line and a second data strobe line, the circuit to receive, in response to a second command from the memory controller, a second data signal via the second data line and a second data strobe signal via the second data strobe line, wherein the second command corresponding to a second set of input control signals, the second data strobe signal partially overlapping in time with the first data strobe signal;

a third data line coupled to the memory controller; and

a logic element to monitor commands from the memory controller and to generate a combined data signal on the third data line in response to the first command and the second command, the combined data signal combining at least part of the first data signal and at least part of the second data signal.--

In the Claims, Claim 3, line 1, change “logic element of claim 2, wherein the logic element” to --circuit of claim 2, wherein the circuit--.

In the Claims, Claim 4, line 1, change "The logic element" to --The circuit--.

In the Claims, Claim 5, line 1, change “logic element of claim 2, wherein the

logic element" to --circuit of claim 2, wherein the circuit--.

In the Claims, replace Claim 6 with the following:

--6. (Currently Amended) The circuit of Claim 2, wherein the logic element is configured to:

respond to a third command from the memory controller, the third command corresponding to a third set of input control signals, the third set of input control signals including a plurality of address and control signals, wherein the third command is a load mode register command;

determine a column address strobe latency (CL) value using a subset of address signals of the plurality of address and control signals; and

determine a time delay using the CL value, the time delay corresponding to a first number of clock cycles.--

In the Claims, **Claim 7**, line 1, change "The logic element" to --The circuit-- and add a period (--.--) at the end of the clause.

In the Claims, replace Claim 8 with the following:

--8. (Currently Amended) The circuit of Claim 6, wherein the logic element includes a buffer to electrically and selectively isolate the first and second data lines from the third data line, the buffer adds the time delay corresponding to the first number of clock cycles to the combined data signal and to the combined data strobe signal.--

In the Claims, replace Claim 10 with the following:

--10. (Currently Amended) The circuit of Claim 2, wherein the circuit comprises one or more integrated circuit.--

In the Claims, **Claim 11**, line 1, change "The logic element" to --The circuit--.

In the Claims, **Claim 12**, line 1, change "The logic element" to --The circuit--.

In the Claims, **Claim 13**, line 1, change "The logic element" to -- The circuit--.

In the Claims, **Claim 14**, line 1, change "The logic element" to --The circuit--.

In the Claims, **Claim 15**, line 1, change "The logic element" to --The circuit--.

In the Claims, **Claim 16**, line 1, change "The logic element" to --The circuit--.

In the Claims, **Claim 17**, line 1, change "The logic element" to --The circuit--.

In the Claims, **Claim 18**, line 1, change “The logic element of Claim 1” to --The circuit of Claim 2--.

In the Claims, **Claim 19**, line 1, change “The logic element of Claim 1” to --The circuit of Claim 2-- and add a period (--.--) at the end of the clause.

In the Claims, **Claim 20**, line 1, change "The logic element" to --The circuit--.

In the Claims, **Claim 21**, line 1, change “The logic element of Claim 1” to --The circuit of Claim 2--.

Prosecution Histories for Parent applications and Reexam proceedings

5. It is noted that the parent applications’ claims, very generally (and in no way limiting what those claims cover), relate a memory module having circuitry that receives rank select signals from a memory controller (that expects the memory module to support a certain number of ranks) and doubles the amount the rank select signals to select one of the ranks on the memory (wherein the actual ranks on the memory module are double what the memory controller is expecting) in reliance upon several signals

including a phase-locked clock signal from the phase-lock loop.

As merely an example of the differences in the instant application (and in no way limiting the subject matter claimed), the following quick summary is provided. This application's claims appear to relate to the features shown in, e.g., Figures 7-8B; *namely*, the back-to-back read operations in which a DQS collision is handled such that data from the two successive read operations are output back-to-back, undisturbed (see Spec. 17-20; ¶¶ [0058], [0068]).

In this regard, the parent application prosecution histories are presently considered not material to patentability of these claims. Nevertheless, they have been considered because it is understood that when deciding what to cite and what not to cite, a "better safe than sorry" approach is favored for a future patentee.

6. The parent patents' corresponding reexamination ("reexam") proceedings' histories were considered during prosecution of the parent applications because the issues raised therein were material to those parent claims. But, here because the distinct subject matter claimed as discussed *supra*, their proceedings histories are considered not material.

In short, the cited reexams (95/000,546; 95/000,577; 95/000,578; 95/000,579; 95/001,337; 95/001,338; 95/001,339; 95/001,381; 95/001,1758) have been considered.

Information Disclosure Statement

7. Acknowledgment is made of Applicants' two Information Disclosure Statement (IDS) Form PTO-1449 filed on December 7, 2012. These IDS have been considered.

Applicant is thanked for identifying related application 13/287,042 (presently not examined) for which the cited Foreign publications and non-patent literature are available. The Examiner has reviewed and considered these publications.

In passing, it is noted that citation 36 (for JP-2000-285674) has been struck-through because a copy does not appear to be on record; Nevertheless, this JP publication corresponds to US 6,188,641 (citation 7) and has been considered.

Citations 35 and 40 were cosmetically corrected to from "JP-2009-237492" and "JP-2010-320270-A" to --JP 09-237492-- and --JP 10-320270--, respectively.

Allowable Subject Matter

8. **Claims 2-21 are allowed.**

The following is an examiner's statement of reasons for allowance:

With respect to independent claim 2, there is no teaching, suggestion, or motivation for combination in the prior art to the circuit to receive, in response to a first command from the memory controller, a first data signal via a first data line and a first data strobe signal via a first data strobe line; the circuit to receive, in response to a second command from the memory controller, a second data signal via a second data line and a second data strobe signal via a second data strobe line, the second data strobe signal partially overlapping in time with the first data strobe signal; a third data line coupled to the memory controller; and a logic element to monitor commands from the memory controller and to generate a combined data signal on the third data line in

response to the first command and the second command, the combined data signal combining at least part of the first data signal and at least part of the second data signal, in combination with the other limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CONCLUSION

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Schaefer (US 6,819,599), Engelahardt (US 6,915,400), and Park et al. (US 7,362,648).

Schaefer teaches problems with more than one memory device simultaneously competing for controlling data transfer by explaining, at least, a timing diagram with a DQS postamble for a first command undesirably overlapping with the DQS preamble of a subsequent command. To solve this problem, Schaefer teaches reduce the preamble window by delaying the beginning of the data strobe preamble signal so that the preamble of a second command does not interfere with the postamble of a first command.

Engelahardt teaches an SRAM in the context of a third scenario called "Writing while read access in progress." In this scenario, a write transmission occurs after a

read strobe signal has become activated, for which the write strobe would ordinarily interfere with the read strobe; however, to correct for potential glitches and access collisions, Engelahardt teach utilizing a read block signal.

Park et al., filed after instant application's earliest effective filing date, teach problems associated with collisions with the data strobes generated from first and second memory devices. Similar to the Schaefer and Engelahardt, Park et al. seek to prevent collisions from happening.

None of the prior art, alone or in combination, meet all of the following limitations: the circuit to receive, in response to a first command from the memory controller, a first data signal via a first data line and a first data strobe signal via a first data strobe line; the circuit to receive, in response to a second command from the memory controller, a second data signal via a second data line and a second data strobe signal via a second data strobe line, the second data strobe signal partially overlapping in time with the first data strobe signal; a third data line coupled to the memory controller; and a logic element to monitor commands from the memory controller and to generate a combined data signal on the third data line in response to the first command and the second command, the combined data signal combining at least part of the first data signal and at least part of the second data signal, as recited in claim 2.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/ALEXANDER SOFOCLEOUS/
Primary Examiner, Art Unit 2824

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Customer No. 79141

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/287,081	11/1/2011	Jeffrey C. Solomon	NETL.018P2C6	6130

TITLE OF INVENTION:

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$890	$0	$0	$890	7/8/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 JAMIE J. ZHENG, Ph.D, Esq.
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Netlist, Inc.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Irvine, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☑ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☑ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-5963 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Jamie J. Zheng/ Date July 2, 2013

Typed or printed name Jamie J. Zheng Registration No. 51,167

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	13287081
Filing Date:	01-Nov-2011
Title of Invention:	CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NETL.018P2C6

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	2501	1	890	890
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
		Total in USD ($)		**890**

Electronic Acknowledgement Receipt

EFS ID:	16213547
Application Number:	13287081
International Application Number:	
Confirmation Number:	6130
Title of Invention:	CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C6
Receipt Date:	02-JUL-2013
Filing Date:	01-NOV-2011
Time Stamp:	10:45:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$890
RAM confirmation Number	9890
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Issue Fee Payment (PTO-85B)	2013-07-02_Issue_Fee_Transmittal_NETL018P1C6.pdf	74205 a6f403514aa92a12749a4c98626856a5dd9f9156	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30280 802c930ec62ee8d385a84772869c6cb39cf5602e	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	104485	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	3	of	14

Complete if Known	
Application Number	13/287,081
Filing Date	1-Nov-2011
First Named Inventor	Jeffrey C. Solomom
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C6

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Sheet	4	of	14

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Application Number	13/287,081
Filing Date	1-Nov-2011
First Named Inventor	Jeffrey C. Solomom
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C6

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Sheet	1	of	14

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Application Number	13/287,081
Filing Date	1-Nov-2011
First Named Inventor	Jeffrey C. Solomom
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C6

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Sheet	2	of	14

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First Named Inventor	Jeffrey C. Solomom
Art Unit	2827
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C6

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Change(s) applied to document, /S.P./ 5/29/2013

Change(s) applied to document, /S.P./ 5/21/2013

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/287,081	08/20/2013	8516188	NETL.018P2C6	6130

79141 7590 07/31/2013
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 97 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Jeffrey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY.DOCKET NO./TITLE	REQUEST ID
13/287,081	11/01/2011	Jeffrey C. Solomon	N3044.10002US19	37466

Acknowledgement of Loss of Entitlement to Entity Status Discount

The entity status change request below filed through Private PAIR on 04/06/2017 has been accepted.

CERTIFICATIONS:

Change of Entity Status:

X Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be notification of loss of entitlement to small or micro entity status, as applicable.

This portion must be completed by the signatory or signatories making the entity status change in accordance with 37 CFR 1.4(d)(4).

Signature:	/Jamie J. Zheng/
Name:	Jamie J. Zheng
Registration Number:	51167