PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	N3044.10002US22
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jeffrey	C.	Solomon	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	Irvine	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	16 Silver Fir
Address 2	
City	Irvine
State/Province	CA
Postal Code	92604
Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jayesh	R.	Bhakta	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	Cerritos	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	12220 Rose Street
Address 2	
City	Cerritos
State/Province	CA
Postal Code	90703
Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

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	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	79141		
Email Address	Docket@mabr.com	Add Email	Remove Email
Email Address	JZheng@mabr.com	Add Email	Remove Email

Application Information:

Title of the Invention	MEMORY MODULE WITH DATA BUFFERING		
Attorney Docket Number	N3044.10002US22	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	23	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	79141		

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	Application Number	
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Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending				Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
	Continuation of	14/715486	2015-05-18		

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14/715486	Continuation of	13/971232	2013-08-20	9037774	2015-05-19

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/971232	Continuation of	13/287081	2011-11-01	8516188	2013-08-20

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/287081	Continuation of	13032470	2011-02-22	8081536	2011-12-20

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13032470	Continuation of	12955711	2010-11-29	7916574	2011-03-29

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12955711	Continuation of	12/629827	2009-12-02	7881150	2011-02-01

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/629827	Continuation of	12/408652	2009-03-20	7636274	2009-12-22

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/408652	Continuation of	11/335875	2006-01-19	7532537	2009-05-12

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	N3044.10002US22
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/335875	Claims benefit of provisional	60/645087	2005-01-19
Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11/335875	Continuation in part of	11/173175	2005-07-01	7289386	2007-10-30

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/173175	Claims benefit of provisional	60/588244	2004-07-15
Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11/173175	Continuation in part of	11/075395	2005-03-07	7286436	2007-10-23

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/075395	Claims benefit of provisional	60/550668	2004-03-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/075395	Claims benefit of provisional	60/575595	2004-05-28
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/075395	reissue of	60/590038	2004-07-21

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

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	Application Number	
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This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	N3044.10002US22
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Netlist, Inc.		
Mailing Address Information For Applicant:			
Address 1	175 Technology, #150		
Address 2			
City	Irvine	**State/Province**	CA
Country	US	Postal Code	92618
Phone Number	949-435-0025	Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	N3044.10002US22
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Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Jaime J. Zheng/			Date (YYYY-MM-DD)	2017-12-28
First Name	Jaime J.	Last Name	Zheng	Registration Number	51167

Additional Signature may be generated within this form by selecting the Add button. Add

PTO/AIA/14 (11-15)
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This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Customer No. 79141
Attorney Docket No.: NETL.018P2C7

Modified PTO/AIA/01 (06-12)

DECLARATION FOR UTILITY OR DESIGN APPLICATION

Title of Invention	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE

As a below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 13/971,231 filed on August 20, 2013.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Note to Inventor: 37 C.F.R. § 1.63(c) states: "A person may not execute an oath or declaration for an application unless that person has reviewed and understands the contents of the application, including the claims, and is aware of the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56."

First Inventor (Legal Name): Jefferey C. Solomon

Signature: Jeffrey C. Solomon Date (Optional): 10-14-2013

Second Inventor (Legal Name): Jayesh R. Bhakta

Signature: Jayesh Bhakta Date (Optional): 10-14-2013

MEMORY MODULE WITH DATA BUFFERING

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a continuation of U.S. Pat. Appl. No. 14/715,486, filed May 18, 2015, to be issued as U.S. Pat. No. 9,858,215 on January 2, 2018, which is a continuation of U.S. Pat. Appl. No. 13/971,231, filed August 20, 2013, now Pat. No. 9,037,774, which is a continuation of U.S. Pat. Appl. No. 13/287,081, filed November 1, 2011, now U.S. Pat. No. 8,516,188, which is a continuation of U.S. Pat. Appl. No. 13/032,470, filed February 22, 2011, now U.S. Pat. No. 8,081,536, which is a continuation of U.S. Pat. Appl. No. 12/955,711, filed November 29, 2010, now U.S. Pat. No. 7,916,574, which is a continuation of U.S. Pat. Appl. No. 12/629,827, filed December 2, 2009, now U.S. Pat. No. 7,881,150, which is a continuation of U.S. Pat. Appl. No. 12/408,652, filed March 20, 2009, now U.S. Pat. No. 7,636,274, which is a continuation of U.S. Pat. Appl. No. 11/335,875, filed January 19, 2006, now U.S. Pat. No. 7,532,537, which claims the benefit of U.S. Provisional Appl. No. 60/645,087, filed January 19, 2005 and which is a continuation-in-part of U.S. Pat. Appl. No. 11/173,175, filed July 1, 2005, now U.S. Pat. No. 7,289,386, which claims the benefit of U.S. Provisional Appl. No. 60/588,244, filed July 15, 2004 and which is a continuation-in-part of U.S. Pat. Appl. No. 11/075,395, filed March 7, 2005, now U.S. Pat. No. 7,286,436, which claims the benefit of U.S. Provisional Appl. No. 60/550,668, filed March 5, 2004, U.S. Provisional Appl. No. 60/575,595, filed May 28, 2004, and U.S. Provisional Appl. No. 60/590,038, filed July 21, 2004, U.S. Pat. Appl. Nos. 13/287,081, 13/032,470, 12/955,711, 12/629,827, 12/408,652, 11/335,875, 11/173,175, and 11/075,395, and U.S. Provisional Appl. Nos. 60/550,668, 60/575,595, 60/590,038, 60/588,244, and 60/645,087 are each incorporated in its entirety by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules.

2. Description of the Related Art

Petitioners
Ex. 1054, p. 12

[0003] Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the processor of the computer system. Memory modules typically have a memory configuration with a unique combination of rows, columns, and banks which result in a total memory capacity for the memory module.

[0004] For example, a 512-Megabyte memory module (termed a "512-MB" memory module, which actually has 2^{29} or 536,870,912 bytes of capacity) will typically utilize eight 512-Megabit DRAM devices (each identified as a "512-Mb" DRAM device, each actually having 2^{29} or 536,870,912 bits of capacity). The memory cells (or memory locations) of each 512-Mb DRAM device can be arranged in four banks, with each bank having an array of 2^{24} (or 16,777,216) memory locations arranged as 2^{13} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 64 M 8-bit-wide memory locations (actually with four banks of 2^{27} or 134,217,728 one-bit memory cells arranged to provide a total of 2^{26} or 67,108,864 memory locations with 8 bits each) are identified as having a "64 Mb×8" or "64 M×8-bit" configuration, or as having a depth of 64 M and a bit width of 8. Furthermore, certain commercially-available 512-MB memory modules are termed to have a "64 M×8-byte" configuration or a "64 M×64-bit" configuration with a depth of 64 M and a width of 8 bytes or 64 bits.

[0005] Similarly, a 1-Gigabyte memory module (termed a "1-GB" memory module, which actually has 2^{30} or 1,073,741,824 bytes of capacity) can utilize eight 1-Gigabit DRAM devices (each identified as a "1-Gb" DRAM device, each actually having 2^{30} or 1,073,741,824 bits of capacity). The memory locations of each 1-Gb DRAM device can be arranged in four banks, with each bank having an array of memory locations with 2^{14} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 128 M 8-bit-wide memory locations (actually with a total of 2^{27} or 134,217,728 memory locations with 8 bits each) are identified as having a "128 Mb×8" or "128 M×8-bit" configuration, or as having a depth of 128 M and a bit width of 8. Furthermore, certain commercially-available 1-GB memory modules are identified as having a "128 M×8-byte" configuration or a "128 M×64-bit" configuration with a depth of 128 M and a width of 8 bytes or 64 bits.

[0006] The commercially-available 512-MB (64 M×8-byte) memory modules and

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the 1-GB (128 M×8-byte) memory modules described above are typically used in computer systems (e.g., personal computers) which perform graphics applications since such "×8" configurations are compatible with data mask capabilities often used in such graphics applications. Conversely, memory modules with "×4" configurations are typically used in computer systems such as servers which are not as graphics-intensive. Examples of such commercially available "×4" memory modules include, but are not limited to, 512-MB (128 M×4-byte) memory modules comprising eight 512-Mb (128 Mb×4) memory devices.

[0007] The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "×64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "×72" organization.

[0008] The memory capacity of a memory module increases with the number of memory devices. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks. For example, a memory module with four ranks has double the memory capacity of a memory module with two ranks and four times the memory capacity of a memory module with one rank. Rather than referring to the memory capacity of the memory module, in certain circumstances, the memory density of the memory module is referred to instead.

[0009] During operation, the ranks of a memory module are selected or activated by address and command signals that are received from the processor. Examples of such address and command signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support one-rank and two-rank memory modules. By only supporting one-rank and two-rank memory modules, the memory density that can be incorporated in each memory slot is limited.

[0010] Various aspects of the design of a memory module impose limitations on the size of the memory arrays of the memory module. Certain such aspects are particularly important for memory modules designed to operate at higher frequencies. Examples of such aspects include, but are not limited to, memory device (e.g., chip) densities, load fan-out, signal integrity, available rank selects, power dissipation, and thermal profiles.

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SUMMARY OF THE INVENTION

[0011] In certain embodiments, a memory module is operable to communicate data with a memory controller via a data bus in response to memory commands received from the memory controller. The memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst. The memory module comprises a plurality of memory integrated circuits including at least one first memory integrated circuit and at least one second memory integrated circuit, and further comprises a buffer coupled between the at least one first memory integrated circuit and the data bus, and between the at least one second memory integrated circuit and the data bus. The buffer couples the at least one first memory integrated circuit to the data bus and isolates the at least one second memory integrated circuit from the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command. The buffer then couples the at least one second memory integrated circuit to the data bus and isolates the at least one first memory integrated circuit from the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command.

[0012] Certain embodiments provide a method of operating a memory module coupled to a memory controller via a memory bus that includes a control/address (C/A) bus and a data bus. The memory module comprises memory integrated circuits, including at least one first memory integrated circuit and at least one second memory integrated circuit. The method comprises receiving from the memory controller a first set of input C/A signals associated with a first memory command via the C/A bus, the first memory command to cause the memory module to receive or output a first data burst; generating a first set of output C/A signals in response to the first set of input C/A signals, the first set of output C/A signals causing the at least one first memory integrated circuit to receive or output the first data burst; receiving from the memory controller a second set of input control/address signals associated with a second memory command via the C/A bus, the second memory command to cause the memory module to receive or output a second data burst; generating a second set of output C/A signals in response to the second set of input C/A signals, the second set of output C/A signals causing the at least one second memory integrated circuit to receive or output the second data

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burst; coupling the at least one first memory integrated circuit to the data bus and isolating the at least one second memory integrated circuit from the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command; and coupling the at least one second memory integrated circuit to the data bus and isolating the at least one first memory integrated circuit from the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command.

[0013] In certain embodiments, a circuit is configured to be mounted on a memory module that is operable to communicate data with a memory controller via a data bus in response to memory commands received from the memory controller. The memory module including at least one first memory integrated circuit and at least one second memory integrated circuit. The memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the at least one first memory integrated circuit to receive or output a first data burst and the second memory command to cause the at least one second memory integrated circuit to receive or output a second data burst. The circuit comprises logic that couples the at least one first memory integrated circuit to the data bus and that isolates the at least one second memory integrated circuit from the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command. The logic then couples the at least one second memory integrated circuit to the data bus and isolates the at least one first memory integrated circuit from the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. 1 schematically illustrates an example memory module in accordance with certain embodiments described herein.

[0015] FIG. 2 schematically illustrates a circuit diagram of two memory devices of a conventional memory module.

[0016] FIGS. 3A and 3B schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two memory devices from the computer system in accordance with certain embodiments described herein.

[0017] FIGS. 4A and 4B schematically illustrate example memory modules having

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a circuit which selectively isolates one or both of the DQ data signal lines of the two ranks of memory devices from the computer system in accordance with certain embodiments described herein.

[0018] FIGS. 5A-5D schematically illustrate example memory modules having a circuit comprising a logic element and one or more switches operatively coupled to the logic element in accordance with certain embodiments described herein.

[0019] FIG. 6A shows an exemplary timing diagram of a gapless read burst for a back-to-back adjacent read condition from one memory device.

[0020] FIG. 6B shows an exemplary timing diagram with an extra clock cycle between successive read commands issued to different memory devices for successive read accesses from different memory devices.

[0021] FIG. 7 shows an exemplary timing diagram in which the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b."

[0022] FIGS. 8A-8D schematically illustrate circuit diagrams of example memory modules comprising a circuit which multiplexes the DQS data strobe signal lines from one another in accordance with certain embodiments described herein.

[0023] FIG. 9A schematically illustrates an example memory module with four ranks of memory devices compatible with certain embodiments described herein.

[0024] FIG. 9B schematically illustrates an example memory module with two ranks of memory devices compatible with certain embodiments described herein.

[0025] FIG. 9C schematically illustrates another example memory module in accordance with certain embodiments described herein.

[0026] FIG. 10A schematically illustrates an exemplary memory module which doubles the rank density in accordance with certain embodiments described herein.

[0027] FIG. 10B schematically illustrates an exemplary circuit compatible with embodiments described herein.

[0028] FIG. 11A schematically illustrates an exemplary memory module which doubles number of ranks in accordance with certain embodiments described herein.

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[0029] FIG. 11B schematically illustrates an exemplary circuit compatible with embodiments described herein.

[0030] FIG. 12 schematically illustrates an exemplary memory module in which a data strobe (DQS) pin of a first memory device is electrically connected to a DQS pin of a second memory device while both DQS pins are active.

[0031] FIG. 13 is an exemplary timing diagram of the voltages applied to the two DQS pins due to non-simultaneous switching.

[0032] FIG. 14 schematically illustrates another exemplary memory module in which a DQS pin of a first memory device is connected to a DQS pin of a second memory device.

[0033] FIG. 15 schematically illustrates an exemplary memory module in accordance with certain embodiments described herein.

[0034] FIGS. 16A and 16B schematically illustrate a first side and a second side, respectively, of a memory module with eighteen 64 M×4 bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board.

[0035] FIGS. 17A and 17B schematically illustrate an exemplary embodiment of a memory module in which a first resistor and a second resistor are used to reduce the current flow between the first DQS pin and the second DQS pin.

[0036] FIG. 18 schematically illustrates another exemplary memory module compatible with certain embodiments described herein.

[0037] FIG. 19 schematically illustrates a particular embodiment of the memory module schematically illustrated by FIG. 18.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Load Isolation

[0038] FIG. 1 schematically illustrates an example memory module **10** compatible with certain embodiments described herein. The memory module **10** is connectable to a memory controller **20** of a computer system (not shown). The memory module **10** comprises a plurality of memory devices **30**, each memory device **30** having a corresponding load. The memory module **10** further comprises a circuit **40** electrically coupled to the plurality of

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memory devices **30** and configured to be electrically coupled to the memory controller **20** of the computer system. The circuit **40** selectively isolates one or more of the loads of the memory devices from the computer system. The circuit **40** comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module **10**.

[0039] As used herein, the term "load" is a broad term which includes, without limitation, electrical load, such as capacitive load, inductive load, or impedance load. As used herein, the term "isolation" is a broad term which includes, without limitation, electrical separation of one or more components from another component or from one another. As used herein, the term "circuit" is a broad term which includes, without limitation, an electrical component or device, or a configuration of electrical components or devices which are electrically or electromagnetically coupled together (e.g., integrated circuits), to perform specific functions.

[0040] Various types of memory modules **10** are compatible with embodiments described herein. For example, memory modules **10** having memory capacities of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, as well as other capacities, are compatible with embodiments described herein. Certain embodiments described herein are applicable to various frequencies including, but not limited to 100 MHz, 200 MHz, 400 MHz, 800 MHz, and above. In addition, memory modules **10** having widths of 4 bytes, 8 bytes, 16 bytes, 32bytes, or 32bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. In certain embodiments, the memory module **10** comprises a printed circuit board on which the memory devices **30** are mounted, a plurality of edge connectors configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, and a plurality of electrical conduits which electrically couple the memory devices **30** to the circuit **40** and which electrically couple the circuit **40** to the edge connectors. Furthermore, memory modules **10** compatible with embodiments described herein include, but are not limited to, single in-line memory modules (SIMMs), dual in-line memory modules (DIMMs), small-outline DIMMs (SO-DIMMs), unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), fully-buffered DIMM (FBDIMM), rank-buffered DIMMs (RBDIMMs), mini-DIMMs, and micro-DIMMs.

[0041] Memory devices **30** compatible with embodiments described herein include,

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but are not limited to, random-access memory (RAM), dynamic random-access memory (DRAM), synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., SDR, DDR-1, DDR-2, DDR-3). In addition, memory devices **30** having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein. Memory devices **30** compatible with embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP). Memory devices **30** compatible with embodiments described herein are available from a number of sources, including but not limited to, Samsung Semiconductor, Inc. of San Jose, Calif., Infineon Technologies AG of San Jose, Calif., and Micron Technology, Inc. of Boise, Id. Persons skilled in the art can select appropriate memory devices **30** in accordance with certain embodiments described herein.

[0042] In certain embodiments, the plurality of memory devices **30** comprises a first number of memory devices **30**. In certain such embodiments, the circuit **40** selectively isolates a second number of the memory devices **30** from the computer system, with the second number less than the first number.

[0043] In certain embodiments, the plurality of memory devices **30** are arranged in a first number of ranks. For example, in certain embodiments, the memory devices **30** are arranged in two ranks, as schematically illustrated by FIG. 1. In other embodiments, the memory devices **30** are arranged in four ranks. Other numbers of ranks of the memory devices **30** are also compatible with embodiments described herein.

[0044] In certain embodiments, the circuit comprises a logic element selected from a group consisting of: a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, and a complex programmable-logic device (CPLD). In certain embodiments, the logic element of the circuit **40** is a custom device. Sources of logic elements compatible with embodiments described herein include, but are not limited to, Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif. In certain embodiments, the logic element comprises various discrete electrical elements, while in certain other embodiments, the logic element comprises one or more integrated circuits.

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[0045] In certain embodiments, the circuit **40** further comprises one or more switches which are operatively coupled to the logic element to receive control signals from the logic element. Examples of switches compatible with certain embodiments described herein include, but are not limited to, field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex.

[0046] FIG. 2 schematically illustrates a circuit diagram of two memory devices **30a, 30b** of a conventional memory module showing the interconnections between the DQ data signal lines **102a**, **102b** of the memory devices **30a, 30b** and the DQS data strobe signal lines **104a**, **104b** of the memory devices **30a, 30b**. Each of the memory devices **30a, 30b** has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, however, for simplicity, FIG. 2 only illustrates a single DQ data signal line and a single DQS data strobe signal line for each memory device **30a, 30b**. The DQ data signal lines **102a**, **102b** and the DQS data strobe signal lines **104a**, **104b** are typically conductive traces etched on the printed circuit board of the memory module. As shown in FIG. 2, each of the memory devices **30a, 30b** has their DQ data signal lines **102a**, **102b** electrically coupled to a common DQ line **112** and their DQS data strobe signal lines **104a**, **104b** electrically coupled to a common DQS line **114**. The common DQ line **112** and the common DQS line **114** are electrically coupled to the memory controller **20** of the computer system. Thus, the computer system is exposed to the loads of both memory devices **30a, 30b** concurrently.

[0047] In certain embodiments, the circuit **40** selectively isolates the loads of at least some of the memory devices **30** from the computer system. The circuit **40** of certain embodiments is configured to present a significantly reduced load to the computer system. In certain embodiments in which the memory devices **30** are arranged in a plurality of ranks, the circuit **40** selectively isolates the loads of some (e.g., one or more) of the ranks of the memory module **10** from the computer system. In certain other embodiments, the circuit **40** selectively isolates the loads of all of the ranks of the memory module **10** from the computer system. For example, when a memory module **10** is not being accessed by the computer system, the capacitive load on the memory controller **20** of the computer system by the memory module **10** can be substantially reduced to the capacitive load of the circuit **40** of the memory module **10**.

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[0048] As schematically illustrated by FIGS. 3A and 3B, an example memory module **10** compatible with certain embodiments described herein comprises a circuit **40** which selectively isolates one or both of the DQ data signal lines **102a**, **102b** of the two memory devices **30a, 30b** from the common DQ data signal line **112** coupled to the computer system. Thus, the circuit **40** selectively allows a DQ data signal to be transmitted from the memory controller **20** of the computer system to one or both of the DQ data signal lines **102a**, **102b**. In addition, the circuit **40** selectively allows one of a first DQ data signal from the DQ data signal line **102a** of the first memory device **30a** or a second DQ data signal from the DQ data signal line **102b** of the second memory device **30b** to be transmitted to the memory controller **20** via the common DQ data signal line **112** (see, e.g., triangles on the DQ and DQS lines of FIGS. 3A and 3B which point towards the memory controller). While various figures of the present application denote read operations by use of DQ and DQS lines which have triangles pointing towards the memory controller, certain embodiments described herein are also compatible with write operations (e.g., as would be denoted by triangles on the DQ or DQS lines pointing away from the memory controller).

[0049] For example, in certain embodiments, the circuit **40** comprises a pair of switches **120** *a*, **120** *b* on the DQ data signal lines **102a**, **102b** as schematically illustrated by FIG. 3A. Each switch **120** *a*, **120** *b* is selectively actuated to selectively electrically couple the DQ data signal line **102a** to the common DQ signal line **112**, the DQ data signal line **102b** to the common DQ signal line **112**, or both DQ data signal lines **102a**, **102b** to the common DQ signal line **112**. In certain other embodiments, the circuit **40** comprises a switch **120** electrically coupled to both of the DQ data signal lines **102a**, **102b**, as schematically illustrated by FIG. 3B. The switch **120** is selectively actuated to selectively electrically couple the DQ data signal line **102a** to the common DQ signal line **112**, the DQ data signal line **102b** to the common DQ signal line **112**, or both DQ signal lines **102a**, **102b** to the common DQ signal line **112**. Circuits **40** having other configurations of switches are also compatible with embodiments described herein. While each of the memory devices **30a, 30b** has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, FIGS. 3A and 3B only illustrate a single DQ data signal line and a single DQS data strobe signal line for each memory device **30a, 30b** for simplicity. The configurations schematically illustrated by FIGS. 3A and 3B can be applied to all of the DQ data signal lines and DQS data strobe signal lines of the memory module **10**.

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[0050] In certain embodiments, the circuit **40** selectively isolates the loads of ranks of memory devices **30** from the computer system. As schematically illustrated in FIGS. 4A and 4B, example memory modules **10** compatible with certain embodiments described herein comprise a first number of memory devices **30** arranged in a first number of ranks **32**. The memory modules **10** of FIGS. 4A and 4B comprises two ranks **32a**, **32b**, with each rank **32a**, **32b** having a corresponding set of DQ data signal lines and a corresponding set of DQS data strobe lines. Other numbers of ranks (e.g., four ranks) of memory devices **30** of the memory module **10** are also compatible with certain embodiments described herein. For simplicity, FIGS. 4A and 4B illustrate only a single DQ data signal line and a single DQS data strobe signal line from each rank **32**.

[0051] The circuit **40** of FIG. 4A selectively isolates one or more of the DQ data signal lines **102a**, **102b** of the two ranks **32a**, **32b** from the computer system. Thus, the circuit **40** selectively allows a DQ data signal to be transmitted from the memory controller **20** of the computer system to the memory devices **30** of one or both of the ranks **32a**, **32b** via the DQ data signal lines **102a**, **102b**. In addition, the circuit **40** selectively allows one of a first DQ data signal from the DQ data signal line **102a** of the first rank **32a** and a second DQ data signal from the DQ data signal line **102b** of the second rank **32b** to be transmitted to the memory controller **20** via the common DQ data signal line **112**. For example, in certain embodiments, the circuit **40** comprises a pair of switches **120** *a*, **120** *b* on the DQ data signal lines **102a**, **102b** as schematically illustrated by FIG. 4A. Each switch **120** *a*, **120** *b* is selectively actuated to selectively electrically couple the DQ data signal line **102a** to the common DQ data signal line **112**, the DQ data signal line **102b** to the common DQ data signal line **112**, or both DQ data signal lines **102a**, **102b** to the common DQ data signal line **112**. In certain other embodiments, the circuit **40** comprises a switch **120** electrically coupled to both of the DQ data signal lines **102a**, **102b**, as schematically illustrated by FIG. 4B. The switch **120** is selectively actuated to selectively electrically couple the DQ data signal line **102a** to the common DQ data signal line **112**, the DQ data signal line **102b** to the common DQ data signal line **112**, or both DQ data signal lines **102a**, **102b** to the common DQ data signal line **112**. Circuits **40** having other configurations of switches are also compatible with embodiments described herein.

[0052] In the example embodiments schematically illustrated by FIGS. 3A, **3**B, **4**A, and **4**B, the circuit **40** comprises a logic element which is integral with and comprises the

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switches **120** which are coupled to the DQ data signal lines and the DQS data strobe signal lines. In certain such embodiments, each switch **120** comprises a data path multiplexer/demultiplexer. In certain other embodiments, the circuit **40** comprises a logic element **122** which is a separate component operatively coupled to the switches **120**, as schematically illustrated by FIGS. 5A-5D. The one or more switches **120** are operatively coupled to the logic element **122** to receive control signals from the logic element **122** and to selectively electrically couple one or more data signal lines to a common data signal line. Example switches compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex. Example logic elements **122** compatible with certain embodiments described herein include, but are not limited to, programmable-logic devices (PLD), application-specific integrated circuits (ASIC), field-programmable gate arrays (FPGA), custom-designed semiconductor devices, and complex programmable-logic devices (CPLD). Example logic elements **122** are available from Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif.

[0053] In certain embodiments, the load isolation provided by the circuit **40** advantageously allows the memory module **10** to present a reduced load (e.g., electrical load, such as capacitive load, inductive load, or impedance load) to the computer system by selectively switching between the two ranks of memory devices **30** to which it is coupled. This feature is used in certain embodiments in which the load of the memory module **10** may otherwise limit the number of ranks or the number of memory devices per memory module. In certain embodiments, the memory module **10** operates as having a data path rank buffer which advantageously isolates the ranks of memory devices **30** of the memory module **10** from one another, from the ranks on other memory modules, and from the computer system. This data path rank buffer of certain embodiments advantageously provides DQ-DQS paths for each rank or sets of ranks of memory devices which are separate from one another, or which are separate from the memory controller of the computer system. In certain embodiments, the load isolation advantageously diminishes the effects of capacitive loading, jitter and other sources of noise. In certain embodiments, the load isolation advantageously simplifies various other aspects of operation of the memory module **10**, including but not limited to, setup-and-hold time, clock skew, package skew, and process, temperature, voltage, and transmission line variations.

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[0054] For certain memory module applications that utilize multiple ranks of memory, increased load on the memory bus can degrade speed performance. In certain embodiments described herein, selectively isolating the loads of the ranks of memory devices **30** advantageously decreases the load on the computer system, thereby allowing the computer system (e.g., server) to run faster with improved signal integrity. In certain embodiments, load isolation advantageously provides system memory with reduced electrical loading, thereby improving the electrical topology to the memory controller **20**. In certain such embodiments, the speed and the memory density of the computer system are advantageously increased without sacrificing one for the other.

[0055] In certain embodiments, load isolation advantageously increases the size of the memory array supported by the memory controller **20** of the computer system. The larger memory array has an increased number of memory devices **30** and ranks of memory devices **30** of the memory module **10**, with a corresponding increased number of chip selects. Certain embodiments described herein advantageously provide more system memory using fewer chip selects, thereby avoiding the chip select limitation of the memory controller.

[0056] An exemplary section of Verilog code corresponding to logic compatible with a circuit **40** which provides load isolation is listed below in Example 1. The exemplary code of Example 1 corresponds to a circuit **40** comprising six FET switches for providing load isolation to DQ and DQS lines.

[0057] Example 1

```
//============================== declarations
reg             rasN_R, casN_R, weN_R;
wire            actv_cmd_R, pch_cmd_R, pch_all_cmd_R, ap_xfr_cmd_R_R;
wire            xfr_cmd_R,mrs_cmd,rd_cmd_R;
```


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```
//- - - - - - - - - - - - - - - - - - - - - - - - - - DDR 2 FET
  reg                   brs0N_R;                        // registered chip sel
  reg                   brs1N_R;                        // registered chip sel
  reg                   brs2N_R;                        // registered chip sel
  reg                   brs3N_R;                        // registered chip sel
  wire                  sel;
  wire                  sel_01;
  wire                  sel_23;
  wire                  rd_R1;
  wire                  wr_cmd_R,wr_R1;
  reg                   rd_R2,rd_R3,rd_R4,rd_R5;
  reg                   wr_R2,wr_R3,wr_R4,wr_R5;
  reg                   enfet1,enfet2,enfet3,enfet4,enfet5,enfet6;
  wire                  wr_01_R1,wr_23_R1;
  reg                   wr_01_R2,wr_01_R3,wr_01_R4;
  reg                   wr_23_R2,wr_23_R3,wr_23_R4;
  wire                  rodt0_a,rodt0_b;

//================================================ logic
  always @(posedge clk_in)
          begin
                  brs0N_R <= brs0_in_N;     // cs0
                  brs1N_R <= brs1_in_N;     // cs1
                  brs2N_R <= brs2_in_N;     // cs2
                  brs3N_R <= brs3_in_N;     // cs3
                  rasN_R  <= brras_in_N ;
                  casN_R  <= brcas_in_N ;
                  weN_R   <= bwe_in_N ;
          end
assign sel = ~brs0N_R | ~brs1N_R | ~brs2N_R | ~brs3N_R ;
assign sel_01 = ~brs0N_R | ~brs1N_R ;
assign sel_23 = ~brs2N_R | ~brs3N_R ;
assign actv_cmd_R = !rasN_R & casN_R & weN_R; // activate cmd
assign pch_cmd_R = !rasN_R & casN_R & !weN_R ;// pchg cmd
assign xfr_cmd_R = rasN_R & !casN_R;                  // xfr cmd
assign mrs_cmd = !rasN_R & !casN_R & !weN_R ;   // md reg set cmd
assign rd_cmd_R = rasN_R & !casN_R & weN_R ;    // read cmd
assign wr_cmd_R = rasN_R & !casN_R & !weN_R ; // write cmd
//-----------------------------------------
assign    rd_R1 = sel & rd_cmd_R;  // rd cmd cyc 1
assign    wr_R1 = sel & wr_cmd_R; // wr cmd cyc 1

//-----------------------------------------
  always @(posedge clk_in)
          begin
                  rd_R2 <= rd_R1 ;
                  rd_R3 <= rd_R2;
```


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```
                rd_R4 <= rd_R3;
                rd_R5 <= rd_R4;
//              rd0_o_R6 <= rd0_o_R5;
                wr_R2 <= wr_R1 ;
                wr_R3 <= wr_R2;
                wr_R4 <= wr_R3;
                wr_R5 <= wr_R4;
        end
//-------------------------------
assign  wr_01_R1 = sel_01 & wr_cmd_R; // wr cmd cyc 1 for cs 2 & cs3
assign  wr_23_R1 = sel_23 & wr_cmd_R; // wr cmd cyc 1 for cs 2 & cs3
  always @(posedge clk_in)
        begin
                wr_01_R2 <= wr_01_R1 ;
                wr_01_R3 <= wr_01_R2;
                wr_01_R4 <= wr_01_R3;
                wr_23_R2 <= wr_23_R1 ;
                wr_23_R3 <= wr_23_R2;
                wr_23_R4 <= wr_23_R3;
        end
assign  rodt0_ab = (rodt0)          // odt cmd from sys
                | (wr_23_R1)        // wr 1st cyc to other rnks (assume single dimm per channel)
                | (wr_23_R2)        // wr 2nd cyc to other rnks (assume single dimm per channel)
                | (wr_23_R3)        // wr 3rd cyc to other rnks (assume single dimm per channel)
                ;
assign  rodt1_ab = (rodt1)          // odt cmd from sys
                | (wr_01_R1)        // wr 1st cyc to other rnks (assume single dimm per channel)
                | (wr_01_R2)        // wr 2nd cyc to other rnks (assume single dimm per channel)
                | (wr_01_R3)        // wr 3rd cyc to other rnks (assume single dimm per channel)
                ;

//-------------------------------
always @(posedge clk_in)
        begin
  if (
     | (rd_R2)                      // pre-am rd
     | (rd_R3)                      // 1st cyc of rd brst (cl3)
     | (rd_R4)                      // 2nd cyc of rd brst (cl3)
     | (wr_R1)                      // pre-am wr
     | (wr_R2)                      // wr brst 1st cyc
     | (wr_R3)                      // wr brst 2nd cyc
      ) begin
                enfet1 <= 1'b1;     // enable fet
                enfet2 <= 1'b1;     // enable fet
                enfet3 <= 1'b1;     // enable fet
                enfet4 <= 1'b1;     // enable fet
                enfet5 <= 1'b1;     // enable fet
                enfet6 <= 1'b1;     // enable fet
        end
```


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```
else
    begin
                enfet1 <= 1'b0;          // disable fet
                enfet2 <= 1'b0;          // disable fet
                enfet3 <= 1'b0;          // disable fet
                enfet4 <= 1'b0;          // disable fet
                enfet5 <= 1'b0;          // disable fet

                enfet6 <= 1'b0;          // disable fet
    end
end
```

Back-to-Back Adjacent Read Commands

[0058] Due to their source synchronous nature, DDR SDRAM (e.g., DDR1, DDR2, DDR3) memory devices operate with a data transfer protocol which surrounds each burst of data strobes with a pre-amble time interval and a post-amble time interval. The pre-amble time interval provides a timing window for the receiving memory device to enable its data capture circuitry when a known valid level is present on the strobe signal to avoid false triggers of the memory device's capture circuit. The post-amble time interval provides extra time after the last strobe for this data capture to facilitate good signal integrity. In certain embodiments, when the computer system accesses two consecutive bursts of data from the same memory device, termed herein as a "back-to-back adjacent read," the post-amble time interval of the first read command and the pre-amble time interval of the second read command are skipped by design protocol to increase read efficiency. FIG. 6A shows an exemplary timing diagram of this "gapless" read burst for a back-to-back adjacent read condition from one memory device.

[0059] In certain embodiments, when the second read command accesses data from a different memory device than does the first read command, there is at least one time interval (e.g., clock cycle) inserted between the data strobes of the two memory devices. This inserted time interval allows both read data bursts to occur without the post-amble time interval of the first read data burst colliding or otherwise interfering with the pre-amble time interval of the second read data burst. In certain embodiments, the memory controller of the computer system inserts an extra clock cycle between successive read commands issued to different memory devices, as shown in the exemplary timing diagram of FIG. 6B for successive read accesses from different memory devices.

[0060] In typical computer systems, the memory controller is informed of the memory boundaries between the ranks of memory of the memory module prior to issuing read

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commands to the memory module. Such memory controllers can insert wait time intervals or clock cycles to avoid collisions or interference between back-to-back adjacent read commands which cross memory device boundaries, which are referred to herein as "BBARX."

[0061] In certain embodiments described herein in which the number of ranks **32** of the memory module **10** is doubled or quadrupled, the circuit **40** generates a set of output address and command signals so that the selection decoding is transparent to the computer system. However, in certain such embodiments, there are memory device boundaries of which the computer system is unaware, so there are occasions in which BBARX occurs without the cognizance of the memory controller **20** of the computer system. As shown in FIG. 7, the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b," resulting in a "collision window."

[0062] FIGS. 8A-8D schematically illustrate circuit diagrams of example memory modules **10** comprising a circuit **40** which multiplexes the DQS data strobe signal lines **104a**, **104b** of two ranks **32a**, **32b** from one another in accordance with certain embodiments described herein. While the DQS data strobe signal lines **104a**, **104b** of FIGS. 8A-8D correspond to two ranks **32a**, **32b** of memory devices **30**, in certain other embodiments, the circuit **40** multiplexes the DQS data strobe signal lines **104a**, **104b** corresponding to two individual memory devices **30a, 30b**.

[0063] FIG. 8A schematically illustrates a circuit diagram of an exemplary memory module **10** comprising a circuit **40** in accordance with certain embodiments described herein. In certain embodiments, BBARX collisions are avoided by a mechanism which electrically isolates the DQS data strobe signal lines **104a**, **104b** from one another during the transition from the first read data burst of one rank **32a** of memory devices **30** to the second read data burst of another rank **32b** of memory devices **30**.

[0064] In certain embodiments, as schematically illustrated by FIG. 8A, the circuit **40** comprises a first switch **130a** electrically coupled to a first DQS data strobe signal line **104a** of a first rank **32a** of memory devices **30** and a second switch **130b** electrically coupled to a second DQS data strobe signal line **104b** of a second rank **32b** of memory devices **30**. In certain embodiments, the time for switching the first switch **130a** and the second switch **130b** is between the two read data bursts (e.g., after the last DQS data strobe of the read data burst of the first rank **32a** and before the first DQS data strobe of the read data burst of the second rank

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32b). During the read data burst for the first rank **32a**, the first switch **130a** is enabled. After the last DQS data strobe of the first rank **32a** and before the first DQS data strobe of the second rank **32b**, the first switch **130a** is disabled and the second switch **130b** is enabled.

[0065] As shown in FIG. 8A, each of the ranks **32a**, **32b** otherwise involved in a BBARX collision have their DQS data strobe signal lines **104a**, **104b** selectively electrically coupled to the common DQS line **114** through the circuit **40**. The circuit **40** of certain embodiments multiplexes the DQS data strobe signal lines **104a**, **104b** of the two ranks **32a**, **32b** of memory devices **30** from one another to avoid a BBARX collision.

[0066] In certain embodiments, as schematically illustrated by FIG. 8B, the circuit **40** comprises a switch **130** which multiplexes the DQS data strobe signal lines **104a**, **104b** from one another. For example, the circuit **40** receives a DQS data strobe signal from the common DQS data strobe signal line **114** and selectively transmits the DQS data strobe signal to the first DQS data strobe signal line **104a**, to the second DQS data strobe signal line **104b**, or to both DQS data strobe signal lines **104a**, **104b**. As another example, the circuit **40** receives a first DQS data strobe signal from the first rank **32a** of memory devices **30** and a second DQS data strobe signal from a second rank **32b** of memory devices **30** and selectively switches one of the first and second DQS data strobe signals to the common DQS data strobe signal line **114**.

[0067] In certain embodiments, the circuit **40** also provides the load isolation described above in reference to FIGS. 1-5. For example, as schematically illustrated by FIG. 8C, the circuit **40** comprises both the switch **120** for the DQ data signal lines **102a**, **102b** and the switch **130** for the DQS data strobe signal lines **104a**, **104b**. While in certain embodiments, the switches **130** are integral with a logic element of the circuit **40**, in certain other embodiments, the switches **130** are separate components which are operatively coupled to a logic element **122** of the circuit **40**, as schematically illustrated by FIG. 8D. In certain such embodiments, the control and timing of the switch **130** is performed by the circuit **40** which is resident on the memory module **10**. Example switches **130** compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex., and multiplexers, such as the SN74AUC2G53 2:1 analog multiplexer/demultiplexer available from Texas Instruments, Inc. of Dallas, Tex.

[0068] The circuit **40** of certain embodiments controls the isolation of the DQS data

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strobe signal lines **104a**, **104b** by monitoring commands received by the memory module **10** from the computer system and producing "windows" of operation whereby the appropriate switches **130** are activated or deactivated to enable and disable the DQS data strobe signal lines **104a**, **104b** to mitigate BBARX collisions. In certain other embodiments, the circuit **40** monitors the commands received by the memory module **10** from the computer system and selectively activates or deactivates the switches **120** to enable and disable the DQ data signal lines **102a**, **102b** to reduce the load of the memory module **10** on the computer system. In still other embodiments, the circuit **40** performs both of these functions together.

Command Signal Translation

[0069] Most high-density memory modules are currently built with 512-Megabit ("512-Mb") memory devices wherein each memory device has a 64 M×8-bit configuration. For example, a 1-Gigabyte ("1-GB") memory module with error checking capabilities can be fabricated using eighteen such 512-Mb memory devices. Alternatively, it can be economically advantageous to fabricate a 1-GB memory module using lower-density memory devices and doubling the number of memory devices used to produce the desired word width. For example, by fabricating a 1-GB memory module using thirty-six 256-Mb memory devices with 64 M×4-bit configuration, the cost of the resulting 1-GB memory module can be reduced since the unit cost of each 256-Mb memory device is typically lower than one-half the unit cost of each 512-Mb memory device. The cost savings can be significant, even though twice as many 256-Mb memory devices are used in place of the 512-Mb memory devices. For example, by using pairs of 512-Mb memory devices rather than single 1-Gb memory devices, certain embodiments described herein reduce the cost of the memory module by a factor of up to approximately five.

[0070] Market pricing factors for DRAM devices are such that higher-density DRAM devices (e.g., 1-Gb DRAM devices) are much more than twice the price of lower-density DRAM devices (e.g., 512-Mb DRAM devices). In other words, the price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices. This pricing difference often lasts for months or even years after the introduction of the higher-density DRAM devices, until volume production factors reduce the costs of the newer higher-density DRAM devices. Thus, when the cost of a higher-density DRAM device is more than the cost of two lower-density DRAM devices, there is an economic incentive for utilizing pairs of the lower-density DRAM devices to replace individual higher-density DRAM devices.

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[0071] FIG. 9A schematically illustrates an exemplary memory module **10** compatible with certain embodiments described herein. The memory module **10** is connectable to a memory controller **20** of a computer system (not shown). The memory module **10** comprises a printed circuit board **210** and a plurality of memory devices **30** coupled to the printed circuit board **210**. The plurality of memory devices **30** has a first number of memory devices **30**. The memory module **10** further comprises a circuit **40** coupled to the printed circuit board **210**. The circuit **40** receives a set of input address and command signals from the computer system. The set of input address and command signals correspond to a second number of memory devices **30** smaller than the first number of memory devices **30**. The circuit **40** generates a set of output address and command signals in response to the set of input address and command signals. The set of output address and command signals corresponds to the first number of memory devices **30**.

[0072] In certain embodiments, as schematically illustrated in FIG. 9A, the memory module **10** further comprises a phase-lock loop device **220** coupled to the printed circuit board **210** and a register **230** coupled to the printed circuit board **210**. In certain embodiments, the phase-lock loop device **220** and the register **230** are each mounted on the printed circuit board **210**. In response to signals received from the computer system, the phase-lock loop device **220** transmits clock signals to the plurality of memory devices **30**, the circuit **40**, and the register **230**. The register **230** receives and buffers a plurality of command signals and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals), and transmits corresponding signals to the appropriate memory devices **30**. In certain embodiments, the register **230** comprises a plurality of register devices. While the phase-lock loop device **220**, the register **230**, and the circuit **40** are described herein in certain embodiments as being separate components, in certain other embodiments, two or more of the phase-lock loop device **220**, the register **230**, and the circuit **40** are portions of a single component. Persons skilled in the art are able to select a phase-lock loop device **220** and a register **230** compatible with embodiments described herein.

[0073] In certain embodiments, the memory module **10** further comprises electrical components which are electrically coupled to one another and are surface-mounted or embedded on the printed circuit board **210**. These electrical components can include, but are not limited to, electrical conduits, resistors, capacitors, inductors, and transistors. In certain

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embodiments, at least some of these electrical components are discrete, while in other certain embodiments, at least some of these electrical components are constituents of one or more integrated circuits.

[0074] In certain embodiments, the printed circuit board **210** is mountable in a module slot of the computer system. The printed circuit board **210** of certain such embodiments has a plurality of edge connections electrically coupled to corresponding contacts of the module slot and to the various components of the memory module **10**, thereby providing electrical connections between the computer system and the components of the memory module **10**.

[0075] In certain embodiments, the plurality of memory devices **30** are arranged in a first number of ranks **32**. For example, in certain embodiments, the memory devices **30** are arranged in four ranks **32a**, **32b**, **32** *c*, **32** *d*, as schematically illustrated by FIG. 9A. In certain other embodiments, the memory devices **30** are arranged in two ranks **32a**, **32b**, as schematically illustrated by FIG. 9B. Other numbers of ranks **32** of the memory devices **30** are also compatible with embodiments described herein.

[0076] As schematically illustrated by FIGS. 9A and 9B, in certain embodiments, the circuit **40** receives a set of input command signals (e.g., refresh, precharge) and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) from the memory controller **20** of the computer system. In response to the set of input address and command signals, the circuit **40** generates a set of output address and command signals.

[0077] In certain embodiments, the set of output address and command signals corresponds to a first number of ranks in which the plurality of memory devices **30** of the memory module **10** are arranged, and the set of input address and command signals corresponds to a second number of ranks per memory module for which the computer system is configured. The second number of ranks in certain embodiments is smaller than the first number of ranks. For example, in the exemplary embodiment as schematically illustrated by FIG. 9A, the first number of ranks is four while the second number of ranks is two. In the exemplary embodiment of FIG. 9B, the first number of ranks is two while the second number of ranks is one. Thus, in certain embodiments, even though the memory module **10** actually has the first number of ranks of memory devices **30**, the memory module **10** simulates a virtual

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memory module by operating as having the second number of ranks of memory devices **30**. In certain embodiments, the memory module **10** simulates a virtual memory module when the number of memory devices **30** of the memory module **10** is larger than the number of memory devices **30** per memory module for which the computer system is configured to utilize. In certain embodiments, the circuit **40** comprises logic (e.g., address decoding logic, command decoding logic) which translates between a system memory domain of the computer system and a physical memory domain of the memory module **10**.

[0078] In certain embodiments, the computer system is configured for a number of ranks per memory module which is smaller than the number of ranks in which the memory devices **30** of the memory module **10** are arranged. In certain such embodiments, the computer system is configured for two ranks of memory per memory module (providing two chip-select signals CS_0, CS_1) and the plurality of memory modules **30** of the memory module **10** are arranged in four ranks, as schematically illustrated by FIG. 9A. In certain other such embodiments, the computer system is configured for one rank of memory per memory module (providing one chip-select signal CS_0) and the plurality of memory modules **30** of the memory module **10** are arranged in two ranks, as schematically illustrated by FIG. 9B.

[0079] In the exemplary embodiment schematically illustrated by FIG. 9A, the memory module **10** has four ranks of memory devices **30** and the computer system is configured for two ranks of memory devices per memory module. The memory module **10** receives row/column address signals or signal bits (A_0-A_{n+1}), bank address signals (BA_0-BA_m), chip-select signals (CS_0 and CS_1), and command signals (e.g., refresh, precharge, etc.) from the computer system. The A_0-A_n row/column address signals are received by the register **230**, which buffers these address signals and sends these address signals to the appropriate ranks of memory devices **30**. The circuit **40** receives the two chip-select signals (CS_0, CS_1) and one row/column address signal (A_{n+1}) from the computer system. Both the circuit **40** and the register **230** receive the bank address signals (BA_0-BA_m) and at least one command signal (e.g., refresh, precharge, etc.) from the computer system.

Logic Tables

[0080] Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using chip-select signals.

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TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:

1. CS_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

[0081] In Logic State 1: CS_0 is active low, A_{n+1} is non-active, and Command is active. CS_{0A} is pulled low, thereby selecting Rank **0**.

[0082] In Logic State 2: CS_0 is active low, A_{n+1} is active, and Command is active. CS_{0B} is pulled low, thereby selecting Rank **1**.

[0083] In Logic State 3: CS_0 is active low, A_{n+1} is Don't Care, and Command is active high. CS_{0A} and CS_{0B} are pulled low, thereby selecting Ranks **0** and **1**.

[0084] In Logic State 4: CS_1 is active low, A_{n+1} is non-active, and Command is active. CS_{1A} is pulled low, thereby selecting Rank **2**.

[0085] In Logic State 5: CS_1 is active low, A_{n+1} is active, and Command is active. CS_1B is pulled low, thereby selecting Rank **3**.

[0086] In Logic State 6: CS_1 is active low, A_{n+1} is Don't Care, and Command is active. CS_{1A} and CS_1B are pulled low, thereby selecting Ranks **2** and **3**.

[0087] In Logic State 7: CS_0 and CS_1 are pulled non-active high, which deselects all ranks, i.e., CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are pulled high.

[0088] The "Command" column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such

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embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently.

[0089] Table 2 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using gated CAS signals.

TABLE 2

CS*	RAS*	CAS*	WE*	Density Bit	A_{10}	Command	CAS0*	CAS1*
1	x	x	x	x	x	NOP	x	x
0	1	1	1	x	x	NOP	1	1
0	0	1	1	0	x	ACTIVATE	1	1
0	0	1	1	1	x	ACTIVATE	1	1
0	1	0	1	0	x	READ	0	1
0	1	0	1	1	x	READ	1	0
0	1	0	0	0	x	WRITE	0	1
0	1	0	0	1	x	WRITE	1	0
0	0	1	0	0	0	PRE-CHARGE	1	1
0	0	1	0	1	0	PRE-CHARGE	1	1
0	0	1	0	x	1	PRE-CHARGE	1	1
0	0	0	0	x	x	MODE REG SET	0	0
0	0	0	1	x	x	REFRESH	0	0

[0090] In certain embodiments in which the density bit is a row address bit, for read/write commands, the density bit is the value latched during the activate command for the selected bank.

Serial-Presence-Detect Device

[0091] Memory modules typically include a serial-presence detect (SPD) device **240** (e.g., an electrically-erasable-programmable read-only memory or EEPROM device) comprising data which characterize various attributes of the memory module, including but not limited to, the number of row addresses the number of column addresses, the data width of the memory devices, the number of ranks, the memory density per rank, the number of memory

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devices, and the memory density per memory device. The SPD device **240** communicates this data to the basic input/output system (BIOS) of the computer system so that the computer system is informed of the memory capacity and the memory configuration available for use and can configure the memory controller properly for maximum reliability and performance.

[0092] For example, for a commercially-available 512-MB (64 M×8-byte) memory module utilizing eight 512-Mb memory devices each with a 64 M×8-bit configuration, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte **3**: Defines the number of row address bits in the DRAM device in the memory module [13 for the 512-Mb memory device].

Byte **4**: Defines the number of column address bits in the DRAM device in the memory module [11 for the 512-Mb memory device].

Byte **13**: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 512-Mb (64 M×8-bit) memory device].

Byte **14**: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 512-Mb (64 M×8-bit) memory device].

Byte **17**: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 512-Mb memory device].

[0093] In a further example, for a commercially-available 1-GB (128 M×8-byte) memory module utilizing eight 1-Gb memory devices each with a 128 M×8-bit configuration, as described above, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte **3**: Defines the number of row address bits in the DRAM device in the memory module [14 for the 1-Gb memory device].

Byte **4**: Defines the number of column address bits in the DRAM device in the memory module [11 for the 1-Gb memory device].

Byte **13**: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 1-Gb (128 M×8-bit) memory device].

Byte **14**: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 1-Gb (128 M×8-bit) memory device].

Byte **17**: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 1-Gb memory device].

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[0094] In certain embodiments, the SPD device **240** comprises data which characterize the memory module **10** as having fewer ranks of memory devices than the memory module **10** actually has, with each of these ranks having more memory density. For example, for a memory module **10** compatible with certain embodiments described herein having two ranks of memory devices **30**, the SPD device **240** comprises data which characterizes the memory module **10** as having one rank of memory devices with twice the memory density per rank. Similarly, for a memory module **10** compatible with certain embodiments described herein having four ranks of memory devices **30**, the SPD device **240** comprises data which characterizes the memory module **10** as having two ranks of memory devices with twice the memory density per rank. In addition, in certain embodiments, the SPD device **240** comprises data which characterize the memory module **10** as having fewer memory devices than the memory module **10** actually has, with each of these memory devices having more memory density per memory device. For example, for a memory module **10** compatible with certain embodiments described herein, the SPD device **240** comprises data which characterizes the memory module **10** as having one-half the number of memory devices that the memory module **10** actually has, with each of these memory devices having twice the memory density per memory device. Thus, in certain embodiments, the SPD device **240** informs the computer system of the larger memory array by reporting a memory device density that is a multiple of the memory devices **30** resident on the memory module **10**. Certain embodiments described herein advantageously do not require system level changes to hardware (e.g., the motherboard of the computer system) or to software (e.g., the BIOS of the computer system).

[0095] FIG. 9C schematically illustrates an exemplary memory module **10** in accordance with certain embodiments described herein. The memory module **10** comprises a pair of substantially identical memory devices **31**, **33**. Each memory device **31**, **33** has a first bit width, a first number of banks of memory locations, a first number of rows of memory locations, and a first number of columns of memory locations. The memory module **10** further comprises an SPD device **240** comprising data that characterizes the pair of memory devices **31**, **33**. The data characterize the pair of memory devices **31**, **33** as a virtual memory device having a second bit width equal to twice the first bit width, a second number of banks of memory locations equal to the first number of banks, a second number of rows of memory locations equal to the first number of rows, and a second number of columns of memory locations equal to the first number of columns.

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[0096] In certain such embodiments, the SPD device **240** of the memory module **10** is programmed to describe the combined pair of lower-density memory devices **31**, **33** as one virtual or pseudo-higher-density memory device. In an exemplary embodiment, two 512-Mb memory devices, each with a 128 M×4-bit configuration, are used to simulate one 1-Gb memory device having a 128 M×8-bit configuration. The SPD device **240** of the memory module **10** is programmed to describe the pair of 512-Mb memory devices as one virtual or pseudo-1-Gb memory device.

[0097] For example, to fabricate a 1-GB (128 M×8-byte) memory module, sixteen 512-Mb (128 M×4-bit) memory devices can be used. The sixteen 512-Mb (128 M×4-bit) memory devices are combined in eight pairs, with each pair serving as a virtual or pseudo-1-Gb (128 M×8-bit) memory device. In certain such embodiments, the SPD device **240** contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: 13 row address bits.

Byte 4: 12 column address bits.

Byte 13: 8 bits wide for the primary virtual 1-Gb (128 M×8-bit) memory device.

Byte 14: 8 bits wide for the error checking virtual 1-Gb (128 M×8-bit) memory device.

Byte 17: 4 banks.

[0098] In this exemplary embodiment, bytes **3**, **4**, and **17** are programmed to have the same values as they would have for a 512-MB (128 M×4-byte) memory module utilizing 512-Mb (128 M×4-bit) memory devices. However, bytes **13** and **14** of the SPD data are programmed to be equal to 8, corresponding to the bit width of the virtual or pseudo-higher-density 1-Gb (128 M×8-bit) memory device, for a total capacity of 1-GB. Thus, the SPD data does not describe the actual-lower-density memory devices, but instead describes the virtual or pseudo-higher-density memory devices. The BIOS accesses the SPD data and recognizes the memory module as having 4 banks of memory locations arranged in 2^{13} rows and 2^{12} columns, with each memory location having a width of 8 bits rather than 4 bits.

[0099] In certain embodiments, when such a memory module **10** is inserted in a computer system, the computer system's memory controller then provides to the memory module **10** a set of input address and command signals which correspond to the number of ranks or the number of memory devices reported by the SPD device **240**. For example, placing a two-rank memory module **10** compatible with certain embodiments described herein in a

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computer system compatible with one-rank memory modules, the SPD device **240** reports to the computer system that the memory module **10** only has one rank. The circuit **40** then receives a set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices **30** of the memory module **10**.

[00100] Similarly, when a two-rank memory module **10** compatible with certain embodiments described herein is placed in a computer system compatible with either one- or two-rank memory modules, the SPD device **240** reports to the computer system that the memory module **10** only has one rank. The circuit **40** then receives a set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices **30** of the memory module **10**.

[00101] Furthermore, a four-rank memory module **10** compatible with certain embodiments described herein simulates a two-rank memory module whether the memory module **10** is inserted in a computer system compatible with two-rank memory modules or with two- or four-rank memory modules. Thus, by placing a four-rank memory module **10** compatible with certain embodiments described herein in a module slot that is four-rank-ready, the computer system provides four chip-select signals, but the memory module **10** only uses two of the chip-select signals.

[00102] In certain embodiments, the circuit **40** comprises the SPD device **240** which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device **240** of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array. In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit **40**. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices **30** from the memory controller **20**. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered

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DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three. In still other embodiments, the SPD device **240** does not utilize this extra cycle of time.

Memory Density Multiplication

[00103] In certain embodiments, two memory devices having a memory density are used to simulate a single memory device having twice the memory density, and an additional address signal bit is used to access the additional memory. Similarly, in certain embodiments, two ranks of memory devices having a memory density are used to simulate a single rank of memory devices having twice the memory density, and an additional address signal bit is used to access the additional memory. As used herein, such simulations of memory devices or ranks of memory devices are termed as "memory density multiplication," and the term "density transition bit" is used to refer to the additional address signal bit which is used to access the additional memory by selecting which rank of memory devices is enabled for a read or write transfer operation.

[00104] For example, for computer systems which are normally limited to using memory modules which have a single rank of 128 M×4-bit memory devices, certain embodiments described herein enable the computer system to utilize memory modules which have double the memory (e.g., two ranks of 128 M×4-bit memory devices). The circuit **40** of certain such embodiments provides the logic (e.g., command and address decoding logic) to double the number of chip selects, and the SPD device **240** reports a memory device density of 256 M×4-bit to the computer system.

[00105] In certain embodiments utilizing memory density multiplication embodiments, the memory module **10** can have various types of memory devices **30** (e.g., DDR1, DDR2, DDR3, and beyond). The circuit **40** of certain such embodiments utilizes implied translation logic equations having variations depending on whether the density transition bit is a row, column, or internal bank address bit. In addition, the translation logic equations of certain embodiments vary depending on the type of memory module **10** (e.g., UDIMM, RDIMM, FBDIMM, etc.). Furthermore, in certain embodiments, the translation

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logic equations vary depending on whether the implementation multiplies memory devices per rank or multiplies the number of ranks per memory module.

TABLE 3A

	128-Mb	256-Mb	512-Mb	1-Gb
Number of banks	4	4	4	4
Number of row address bits	12	13	13	14
Number of column address bits for "x 4" configuration	11	11	12	12
Number of column address bits for "x 8" configuration	10	10	11	11
Number of column address bits for "x 16" configuration	9	9	10	10

[00106] Table 3A provides the numbers of rows and columns for DDR-1 memory devices, as specified by JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published February 2004, and incorporated in its entirety by reference herein.

[00107] As described by Table 3A, 512-Mb (128 M×4-bit) DRAM devices have 2^{13} rows and 2^{12} columns of memory locations, while 1-Gb (128 M×8-bit) DRAM devices have 2^{14} rows and 2^{11} columns of memory locations. Because of the differences in the number of rows and the number of columns for the two types of memory devices, complex address translation procedures and structures would typically be needed to fabricate a 1-GB (128 M×8-byte) memory module using sixteen 512-Mb (128 M×4-bit) DRAM devices.

[00108] Table 3B shows the device configurations as a function of memory density for DDR2 memory devices.

TABLE 3B

	Number of Rows	Number of Columns	Number of Internal Banks	Page Size (x4s or x8s)
256 Mb	13	11	4	1 KB
512 Mb	14	11	4	1 KB
1 Gb	14	11	8	1 KB
2 Gb	15	11	8	1 KB
4 Gb	16	11	8	1 KB

Table 4 lists the corresponding density transition bit for the density transitions between the DDR2 memory densities of Table 3B.

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TABLE 4

Density Transition	Density Transition Bit
256 Mb to 512 Mb	A_{13}
512 Mb to 1 Gb	BA_2
1 Gb to 2 Gb	A_{14}
2 Gb to 4 Gb	A_{15}

Other certain embodiments described herein utilize a transition bit to provide a transition from pairs of physical 4-Gb memory devices to simulated 8-Gb memory devices.

[00109] In an example embodiment, the memory module comprises one or more pairs of 256-Mb memory devices, with each pair simulating a single 512-Mb memory device. The simulated 512-Mb memory device has four internal banks while each of the two 256-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 256-Mb memory devices. In certain embodiments, the additional row address bit is translated by the circuit **40** to the rank selection between each of the two 256-Mb memory devices of the pair. Although there are eight total internal banks in the rank-converted memory array, the computer system is only aware of four internal banks. When the memory controller activates a row for a selected bank, the circuit **40** activates the same row for the same bank, but it does so for the selected rank according to the logic state of the additional row address bit A_{13}.

[00110] In another example embodiment, the memory module comprises one or more pairs of 512-Mb memory devices, with each pair simulating a single 1-Gb memory device. The simulated 1-Gb memory device has eight internal banks while each of the two 512-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 512-Mb memory devices. In certain embodiments, the mapped BA_2 (bank **2**) bit is used to select between the two ranks of 512-Mb memory devices to preserve the internal bank geometry expected by the memory controller of the computer system. The state of the BA_2 bit selects the upper or lower set of four banks, as well as the upper and lower 512-Mb rank.

[00111] In another example embodiment, the memory module comprises one or more pairs of 1-Gb memory devices, with each pair simulating a single 2-Gb memory device. Each of the two 1-Gb memory devices has eight internal banks for a total of sixteen internal banks, while the simulated 2-Gb memory device has eight internal banks. In certain embodiments, the additional row address bit translates to the rank selection between the two

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1-Gb memory devices. Although there are sixteen total internal banks per pair of 1-Gb memory devices in the rank-converted memory array, the memory controller of the computer system is only aware of eight internal banks. When the memory controller activates a row of a selected bank, the circuit **40** activates the same row for the same bank, but is does so for the selected rank according to the logic state of the additional row address bit A_{14}.

[00112] The circuit **40** of certain embodiments provides substantially all of the translation logic used for the decoding (e.g., command and address decoding). In certain such embodiments, there is a fully transparent operational conversion from the "system memory" density domain of the computer system to the "physical memory" density domain of the memory module **10**. In certain embodiments, the logic translation equations are programmed in the circuit **40** by hardware, while in certain other embodiments, the logic translation equations are programmed in the circuit **40** by software. Examples 1 and 2 provide exemplary sections of Verilog code compatible with certain embodiments described herein. As described more fully below, the code of Examples 1 and 2 includes logic to reduce potential problems due to "back-to-back adjacent read commands which cross memory device boundaries or "BBARX." Persons skilled in the art are able to provide additional logic translation equations compatible with embodiments described herein.

[00113] An exemplary section of Verilog code compatible with memory density multiplication from 512 Mb to 1 Gb using DDR2 memory devices with the BA_2 density transition bit is listed below in Example 2. The exemplary code of Example 2 corresponds to a circuit **40** which receives one chip-select signal from the computer system and which generates two chip-select signals.

[00114] Example 2

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```
always @(posedge clk_in)
    begin
                    cs0N_R <= cs0_in_N;    // cs0
                    rasN_R <= ras_in_N;
                    casN_R <= cas_in_N;
                    weN_R <= we_in_N;
    end
// Gated Chip Selects
assign              pcs0a_1 = (~cs0_in_N & ~ras_in_N & ~cas_in_N)                                   // ref,md reg set
                    | (~cs0_in_N & ras_in_N & cas_in_N)                                             // ref exit, pwr dn
                    | (~cs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)                        // pchg all
                    | (~cs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ~ba2_in)             // pchg single bnk
                    | (~cs0_in_N & ~ras_in_N & cas_in_N & we_in_N       & ~ba2_in)                  // activate
                    | (~cs0_in_N & ras_in_N & ~cas_in_N                & ~ba2_in)                  // xfr
                    ;
assign              pcs0b_1 = (~cs0_in_N & ~ras_in_N & ~cas_in_N)                                   // ref,md reg set
                    | (~cs0_in_N & ras_in_N & cas_in_N)                                             // ref exit, pwr dn
                    | (~cs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)                        // pchg all
                    | (~cs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ba2_in)              // pchg single bnk
                    | (~cs0_in_N & ~ras_in_N & cas_in_N & we_in_N       & ba2_in)                   // activate
                    | (~cs0_in_N & ras_in_N & ~cas_in_N                & ba2_in) // xfr
                    ;
//---------------------------------------------------
 always @(posedge clk_in)
    begin
                    a4_r <= a4_in ;
                    a5_r <= a5_in ;
                    a6_r <= a6_in ;
                    a10_r <= a10_in ;
                    ba0_r <= ba0_in ;
                    ba1_r <= ba1_in ;
                    ba2_r <= ba2_in ;
                    q_mrs_cmd_cyc1 <= q_mrs_cmd ;
    end
////////////////////////////////////////////////////////////////
// determine the cas latency
////////////////////////////////////////////////////////////////
assign q_mrs_cmd_r = (!rasN_R & !casN_R & !weN_R)
                       & !cs0N_R
                    & (!ba0_r & !ba1_r)
                    ;      // md reg set cmd
    always @(posedge clk_in)
        if (~reset_N)      // hmr
                    cl3 <= 1'b1 ;
        else if (q_mrs_cmd_cyc1)   // load mode reg cmd
      begin
                    cl3 <= (~a6_r & a5_r & a4_r ) ;
      end
    always @(posedge clk_in)
        if (~reset_N)              // reset
```

```
                cl2 <= 1'b0 ;
            else if (q_mrs_cmd_cyc1)   // load mode reg cmd
        begin
                cl2 <= (~a6_r & a5_r & ~a4_r ) ;
        end
      always @(posedge clk_in)
            if (~reset_N)              // reset
                cl4 <= 1'b0 ;
            else if (q_mrs_cmd_cyc1)   // load mode reg cmd
        begin
                cl4 <= (a6_r & ~a5_r & ~a4_r ) ;
        end
  always @(posedge clk_in)
            if (~reset_N)              cl5 <= 1'b0 ;
            else if (q_mrs_cmd_cyc1)   // load mode reg cmd
        begin
                cl5 <= (a6_r & ~a5_r & a4_r ) ;
        end
assign          pre_cyc2_enfet = (wr_cmd_cyc1 & acs_cyc1 & cl3)      // wr brst cl3 preamble
                               ;
assign          pre_cyc3_enfet = (rd_cmd_cyc2 & cl3)                 // rd brst cl3 preamble
                               | (wr_cmd_cyc2 & cl3)                 // wr brst cl3 1st pair
                               | (wr_cmd_cyc2 & cl4)                 // wr brst cl4 preamble
                               ;
assign          pre_cyc4_enfet = (wr_cmd_cyc3 & cl3)                 // wr brst cl3 2nd pair
                               | (wr_cmd_cyc3 & cl4)                 // wr brst cl4 1st pair
                               | (rd_cmd_cyc3 & cl3)                 // rd brst cl3 1st pair
                               | (rd_cmd_cyc3 & cl4)                 // rd brst cl4 preamble
                               ;
assign          pre_cyc5_enfet = (rd_cmd_cyc4 & cl3)                 // rd brst cl3 2nd pair
                               | (wr_cmd_cyc4 & cl4)                 // wr brst cl4 2nd pair
                               | (rd_cmd_cyc4 & cl4)                 // rd brst cl4 1st pair
                               ;
// dq
assign          pre_dq_cyc = pre_cyc2_enfet
                   | pre_cyc3_enfet
                   | pre_cyc4_enfet
                   | pre_cyc5_enfet
                   ;
assign          pre_dq_ncyc = enfet_cyc2
                   | enfet_cyc3
                   | enfet_cyc4
                   | enfet_cyc5
                   ;
// dqs
assign          pre_dqsa_cyc = (pre_cyc2_enfet & ~ba2_r)
                   | (pre_cyc3_enfet & ~ba2_cyc2)
                   | (pre_cyc4_enfet & ~ba2_cyc3)
                   | (pre_cyc5_enfet & ~ba2_cyc4)
                   ;
assign          pre_dqsb_cyc = (pre_cyc2_enfet & ba2_r)
                   | (pre_cyc3_enfet & ba2_cyc2)
                   | (pre_cyc4_enfet & ba2_cyc3)
                   | (pre_cyc5_enfet & ba2_cyc4)
                   ;
assign          pre_dqsa_ncyc = (enfet_cyc2 & ~ba2_cyc2)
                   | (enfet_cyc3 & ~ba2_cyc3)
                   | (enfet_cyc4 & ~ba2_cyc4)
                   | (enfet_cyc5 & ~ba2_cyc5)
                   ;
assign          pre_dqsb_ncyc = (enfet_cyc2 & ba2_cyc2)
                   | (enfet_cyc3 & ba2_cyc3)
                   | (enfet_cyc4 & ba2_cyc4)
                   | (enfet_cyc5 & ba2_cyc5)
                   ;
```

```
always @(posedge clk_in)
        begin
                        acs_cyc2 <= acs_cyc1 ;        // cs active
                        ba2_cyc3 <= ba2_r ;
                        ba2_cyc3 <= ba2_cyc2 ;
                        ba2_cyc4 <= ba2_cyc3 ;
                        ba2_cyc5 <= ba2_cyc4 ;
                        rd_cmd_cyc2 <= rd_cmd_cyc1 & acs_cyc1;
                        rd_cmd_cyc3 <= rd_cmd_cyc2 ;
                        rd_cmd_cyc4 <= rd_cmd_cyc3 ;
                        rd_cmd_cyc5 <= rd_cmd_cyc4 ;
                        rd_cmd_cyc6 <= rd_cmd_cyc5 ;
                        rd_cmd_cyc7 <= rd_cmd_cyc6 ;
                        wr_cmd_cyc2 <= wr_cmd_cyc1 & acs_cyc1;
                        wr_cmd_cyc3 <= wr_cmd_cyc2 ;
                        wr_cmd_cyc4 <= wr_cmd_cyc3 ;
                        wr_cmd_cyc5 <= wr_cmd_cyc4 ;
        end
 always @(negedge clk_in)
        begin
                        dq_ncyc <= dq_cyc;
                        dqs_ncyc_a <= dqs_cyc_a;
                        dqs_ncyc_b <= dqs_cyc_b;
        end
// DQ FET enables
assign                  enq_fet1 = dq_cyc | dq_ncyc             ;
assign                  enq_fet2 = dq_cyc | dq_ncyc ;
assign                  enq_fet3 = dq_cyc | dq_ncyc             ;
assign                  enq_fet4 = dq_cyc | dq_ncyc ;
assign                  enq_fet5 = dq_cyc | dq_ncyc ;
// DQS FET enables
assign                  ens_fet1a = dqs_cyc_a | dqs_ncyc_a   ;
assign                  ens_fet2a = dqs_cyc_a | dqs_ncyc_a   ;
assign                  ens_fet3a = dqs_cyc_a | dqs_ncyc_a   ;
assign                  ens_fet1b = dqs_cyc_b | dqs_ncyc_b   ;
assign                  ens_fet2b = dqs_cyc_b | dqs_ncyc_b   ;
assign                  ens_fet3b = dqs_cyc_b | dqs_ncyc_b   ;
```

[00115] Another exemplary section of Verilog code compatible with memory density multiplication from 256 Mb to 512 Mb using DDR2 memory devices and gated CAS signals with the row A_{13} density transition bit is listed below in Example 3. The exemplary code of Example 3 corresponds to a circuit **40** which receives one gated CAS signal from the computer system and which generates two gated CAS signals.

[00116] Example 3

```
// latched a13 flags cs0, banks 0-3
   always @(posedge clk_in)
      if (actv_cmd_R & ~rs0N_R & ~bnk1_R & ~bnk0_R )   // activate
      begin
                        1_a13_00 <= a13_r ;
      end
   always @(posedge clk_in)
      if (actv_cmd_R & ~rs0N_R & ~bnk1_R & bnk0_R)      // activate
      begin
                        1_a13_01 <= a13_r ;
      end
   always @(posedge clk_in)
      if (actv_cmd_R & ~rs0N_R & bnk1_R & ~bnk0_R)      // activate
```


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```
    begin
            1_a13_10 <= a13_r ;
    end
  always @(posedge clk_in)
    if (actv_cmd_R & ~rs0N_R & bnk1_R & bnk0_R)      // activate
    begin
            1_a13_11 <= a13_r ;
    end
// gated cas
assign cas_i = ~(casN_R);
assign   cas0_o = ( ~rasN_R & cas_i)
                | ( rasN_R & ~1_a13_00 & ~bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & ~1_a13_01 & ~bnk1_R & bnk0_R & cas_i)
                | ( rasN_R & ~1_a13_10 & bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & ~1_a13_11 & bnk1_R & bnk0_R & cas_i)
                ;
assign   cas1_o = ( ~rasN_R & cas_i)
                | ( rasN_R & 1_a13_00          & ~bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & 1_a13_01          & ~bnk1_R & bnk0_R & cas_i)
                | ( rasN_R & 1_a13_10          & bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & 1_a13_11          & bnk1_R & bnk0_R & cas_i)
                ;
assign          pcas_0_N = ~cas0_o;
assign          pcas_1_N = ~cas1_o;
assign          rd0_o_R1 = rasN_R & cas0_o & weN_R & ~rs0N_R;   // rnk0 rd cmd cyc
assign          rd1_o_R1 = rasN_R & cas1_o & weN_R & ~rs0N_R;   // rnk1 rd cmd cyc
assign          wr0_o_R1 = rasN_R & cas0_o & ~weN_R & ~rs0N_R;  // rnk0 wr cmd cyc
assign          wr1_o_R1 = rasN_R & cas1_o & ~weN_R & ~rs0N_R ;  // rnk1 wr cmd cyc
    always @(posedge clk_in)
        begin
            rd0_o_R2 <= rd0_o_R1 ;
            rd0_o_R3 <= rd0_o_R2;
            rd0_o_R4 <= rd0_o_R3;
            rd0_o_R5 <= rd0_o_R4;
            rd1_o_R2 <= rd1_o_R1 ;
            rd1_o_R3 <= rd1_o_R2;
            rd1_o_R4 <= rd1_o_R3;
            rd1_o_R5 <= rd1_o_R4;
            wr0_o_R2 <= wr0_o_R1 ;
            wr0_o_R3 <= wr0_o_R2;
            wr0_o_R4 <= wr0_o_R3;
            wr1_o_R2 <= wr1_o_R1 ;
            wr1_o_R3 <= wr1_o_R2;
            wr1_o_R4 <= wr1_o_R3;
        end
    always @(posedge clk_in)
        begin
        if (
                (rd0_o_R2 & ~rd1_o_R4)                                  // pre-am rd if no ped on rnk 1
              | rd0_o_R3                                                // 1st cyc of rd brst
              | rd0_o_R4                                                // 2nd cyc of rd brst
              | (rd0_o_R5 & ~rd1_o_R2 & ~rd1_o_R3)                      // post-rd cyc if no ped on rnk 1
              | (wr0_o_R1)                                              // pre-am wr
              | wr0_o_R2 | wr0_o_R3                                     // wr brst 1st & 2nd cyc
              | (wr0_o_R4)                                              // post-wr cyc (chgef9)
              | wr1_o_R1 | wr1_o_R2 | wr1_o_R3 | wr1_o_R4               // rnnk 1 (chgef9)
              )
                                en_fet_a <= 1'b1;                       // enable fet
        else
                                en_fet_a <= 1'b0;                       // disable fet
        end
```

```
always @(posedge clk_in)
        begin
        if (
                (rd1_o_R2 & ~rd0_o_R4)
              | rd1_o_R3
              | rd1_o_R4
              | (rd1_o_R5 & ~rd0_o_R2 & ~rd0_o_R3)
            | (wr1_o_R1)                                        // (chgef8)
            | wr1_o_R2 | wr1_o_R3
  | (wr1_o_R4)                                                  // post-wr cyc      (chgef0)
  | wr0_o_R1 | wr0_o_R2 | wr0_o_R3 | wr0_o_R4                   // rank 0 (chgef9)
                )
                    en_fet_b <= 1'b1;                           //
        else
                    en_fet_b <= 1'b0;
        end
```

[00117] In certain embodiments, the chipset memory controller of the computer system uses the inherent behavioral characteristics of the memory devices (e.g., DDR2 memory devices) to optimize throughput of the memory system. For example, for each internal bank in the memory array, a row (e.g., 1 KB page) is advantageously held activated for an extended period of time. The memory controller, by anticipating a high number of memory accesses or hits to a particular region of memory, can exercise this feature to advantageously eliminate time-consuming pre-charge cycles. In certain such embodiments in which two half-density memory devices are transparently substituted for a single full-density memory device (as reported by the SPD device **240** to the memory controller), the memory devices advantageously support the "open row" feature.

[00118] FIG. 10A schematically illustrates an exemplary memory module **10** which doubles the rank density in accordance with certain embodiments described herein. The memory module **10** has a first memory capacity. The memory module **10** comprises a plurality of substantially identical memory devices **30** configured as a first rank **32a** and a second rank **32b**. In certain embodiments, the memory devices **30** of the first rank **32a** are configured in pairs, and the memory devices **30** of the second rank **32b** are also configured in pairs. In certain embodiments, the memory devices **30** of the first rank **32a** are configured with their respective DQS pins tied together and the memory devices **30** of the second rank **32b** are configured with their respective DQS pins tied together, as described more fully below. The memory module **10** further comprises a circuit **40** which receives a first set of address and command signals from a memory controller (not shown) of the computer system. The first set of address and command signals is compatible with a second memory capacity substantially equal to one-half of the first memory capacity. The circuit **40** translates the first set of address and command

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signals into a second set of address and command signals which is compatible with the first memory capacity of the memory module **10** and which is transmitted to the first rank **32a** and the second rank **32b**.

[00119] The first rank **32a** of FIG. 10A has 18 memory devices **30** and the second rank **32b** of FIG. 10A has 18 memory devices **30**. Other numbers of memory devices **30** in each of the ranks **32a**, **32b** are also compatible with embodiments described herein.

[00120] In the embodiment schematically illustrated by FIG. 10A, the memory module **10** has a width of 8 bytes (or 64 bits) and each of the memory devices **30** of FIG. 10A has a bit width of 4 bits. The 4-bit-wide ("×4") memory devices **30** of FIG. 10A have one-half the width, but twice the depth of 8-bit-wide ("×8") memory devices. Thus, each pair of "×4" memory devices **30** has the same density as a single "×8" memory device, and pairs of "×4" memory devices **30** can be used instead of individual "×8" memory devices to provide the memory density of the memory module **10**. For example, a pair of 512-Mb 128 M×4-bit memory devices has the same memory density as a 1-Gb 128 M×8-bit memory device.

[00121] For two "×4" memory devices **30** to work in tandem to mimic a "×8" memory device, the relative DQS pins of the two memory devices **30** in certain embodiments are advantageously tied together, as described more fully below. In addition, to access the memory density of a high-density memory module **10** comprising pairs of "×4" memory devices **30**, an additional address line is used. While a high-density memory module comprising individual "×8" memory devices with the next-higher density would also utilize an additional address line, the additional address lines are different in the two memory module configurations.

[00122] For example, a 1-Gb 128 M×8-bit DDR-1 DRAM memory device uses row addresses A_{13}-A_0 and column addresses A_{11} and A_9-A_0. A pair of 512-Mb 128 M×4-bit DDR-1 DRAM memory devices uses row addresses A_{12}-A_0 and column addresses A_{12}, A_{11}, and A_9-A_0. In certain embodiments, a memory controller of a computer system utilizing a 1-GB 128 M×8 memory module **10** comprising pairs of the 512-Mb 128 M×4 memory devices **30** supplies the address and command signals including the extra row address (A_{13}) to the memory module **10**. The circuit **40** receives the address and command signals from the memory controller and converts the extra row address (A_{13}) into an extra column address (A_{12}).

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[00123] FIG. 10B schematically illustrates an exemplary circuit **40** compatible with embodiments described herein. The circuit **40** is used for a memory module **10** comprising pairs of "×4" memory devices **30** which mimic individual "×8" memory devices. In certain embodiments, each pair has the respective DQS pins of the memory devices **30** tied together. In certain embodiments, as schematically illustrated by FIG. 10B, the circuit **40** comprises a programmable-logic device (PLD) **42**, a first multiplexer **44** electrically coupled to the first rank **32a** of memory devices **30**, and a second multiplexer **46** electrically coupled to the second rank **32b** of memory devices **30**. In certain embodiments, the PLD **42** and the first and second multiplexers **44**, **46** are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42**, first multiplexer **44**, and second multiplexer **46** in accordance with embodiments described herein.

[00124] In the exemplary circuit **40** of FIG. 10B, during a row access procedure (CAS is high), the first multiplexer **44** passes the A_{12} address through to the first rank **32**, the second multiplexer **46** passes the A_{12} address through to the second rank **34**, and the PLD **42** saves or latches the A_{13} address from the memory controller. In certain embodiments, a copy of the A_{13} address is saved by the PLD **42** for each of the internal banks (e.g., 4 internal banks) per memory device **30**. During a subsequent column access procedure (CAS is low), the first multiplexer **44** passes the previously-saved A_{13} address through to the first rank **32a** as the A_{12} address and the second multiplexer **46** passes the previously-saved A_{13} address through to the second rank **32b** as the A_{12} address. The first rank **32a** and the second rank **32b** thus interpret the previously-saved A_{13} row address as the current A_{12} column address. In this way, in certain embodiments, the circuit **40** translates the extra row address into an extra column address in accordance with certain embodiments described herein.

[00125] Thus, by allowing two lower-density memory devices to be used rather than one higher-density memory device, certain embodiments described herein provide the advantage of using lower-cost, lower-density memory devices to build "next-generation" higher-density memory modules. Certain embodiments advantageously allow the use of lower-cost readily-available 512-Mb DDR-2 SDRAM devices to replace more expensive 1-Gb DDR-2 SDRAM devices. Certain embodiments advantageously reduce the total cost of the resultant memory module.

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[00126] FIG. 11A schematically illustrates an exemplary memory module **10** which doubles number of ranks in accordance with certain embodiments described herein. The memory module **10** has a first plurality of memory locations with a first memory density. The memory module **10** comprises a plurality of substantially identical memory devices **30** configured as a first rank **32a**, a second rank **32b**, a third rank **32** *c*, and a fourth rank **32** *d*. The memory module **10** further comprises a circuit **40** which receives a first set of address and command signals from a memory controller (not shown). The first set of address and command signals is compatible with a second plurality of memory locations having a second memory density. The second memory density is substantially equal to one-half of the first memory density. The circuit **40** translates the first set of address and command signals into a second set of address and command signals which is compatible with the first plurality of memory locations of the memory module **10** and which is transmitted to the first rank **32a**, the second rank **32b**, the third rank **32** *c*, and the fourth rank **32** *d*.

[00127] Each rank **32a**, **32b**, **32** *c*, **32** *d* of FIG. 11A has 9 memory devices **30**. Other numbers of memory devices **30** in each of the ranks **32a**, **32b**, **32** *c*, **32** *d* are also compatible with embodiments described herein.

[00128] In the embodiment schematically illustrated by FIG. 11A, the memory module **10** has a width of 8 bytes (or 64 bits) and each of the memory devices **30** of FIG. 11A has a bit width of 8 bits. Because the memory module **10** has twice the number of 8-bit-wide ("×8") memory devices **30** as does a standard 8-byte-wide memory module, the memory module **10** has twice the density as does a standard 8-byte-wide memory module. For example, a 1-GB 128 M×8-byte memory module with 36 512-Mb 128 M×8-bit memory devices (arranged in four ranks) has twice the memory density as a 512-Mb 128 M×8-byte memory module with 18 512-Mb 128 M×8-bit memory devices (arranged in two ranks).

[00129] To access the additional memory density of the high-density memory module **10**, the two chip-select signals (CS_0, CS_1) are used with other address and command signals to gate a set of four gated CAS signals. For example, to access the additional ranks of four-rank 1-GB 128 M×8-byte DDR-1 DRAM memory module, the CS_0 and CS_1 signals along with the other address and command signals are used to gate the CAS signal appropriately, as schematically illustrated by FIG. 11A. FIG. 11B schematically illustrates an exemplary circuit **40** compatible with embodiments described herein. In certain embodiments, the circuit **40**

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comprises a programmable-logic device (PLD) **42** and four "OR" logic elements **52**, **54**, **56**, **58** electrically coupled to corresponding ranks **32a**, **32b**, **32** *c*, **32** *d* of memory devices **30**.

[00130] In certain embodiments, the PLD **42** comprises an ASIC, an FPGA, a custom-designed semiconductor device, or a CPLD. In certain embodiments, the PLD **42** and the four "OR" logic elements **52**, **54**, **56**, **58** are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42** and appropriate "OR" logic elements **52**, **54**, **56**, **58** in accordance with embodiments described herein.

[00131] In the embodiment schematically illustrated by FIG. 11B, the PLD **42** transmits each of the four "enabled CAS" ($ENCAS_0a$, $ENCAS_0b$, $ENCAS_1a$, $ENCAS_1b$) signals to a corresponding one of the "OR" logic elements **52**, **54**, **56**, **58**. The CAS signal is also transmitted to each of the four "OR" logic elements **52**, **54**, **56**, **58**. The CAS signal and the "enabled CAS" signals are "low" true signals. By selectively activating each of the four "enabled CAS" signals which are inputted into the four "OR" logic elements **52**, **54**, **56**, **58**, the PLD **42** is able to select which of the four ranks **32a**, **32b**, **32** *c*, **32** *d* is active.

[00132] In certain embodiments, the PLD **42** uses sequential and combinatorial logic procedures to produce the gated CAS signals which are each transmitted to a corresponding one of the four ranks **32a**, **32b**, **32** *c*, **32** *d*. In certain other embodiments, the PLD **42** instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS_0a, CS_0b, CS_1a, and CS_1b) which are each transmitted to a corresponding one of the four ranks **32a**, **32b**, **32** *c*, **32** *d*.

Tied Data Strobe Signal Pins

[00133] For proper operation, the computer system advantageously recognizes a 1-GB memory module comprising 256-Mb memory devices with 64 M×4-bit configuration as a 1-GB memory module having 512-Mb memory devices with 64 M×8-bit configuration (e.g., as a 1-GB memory module with 128 M×8-byte configuration). This advantageous result is desirably achieved in certain embodiments by electrically connecting together two output signal pins (e.g., DQS or data strobe pins) of the two 256-Mb memory devices such that both output signal pins are concurrently active when the two memory devices are concurrently enabled. The DQS or data strobe is a bi-directional signal that is used during both read cycles

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and write cycles to validate or latch data. As used herein, the terms "tying together" or "tied together" refer to a configuration in which corresponding pins (e.g., DQS pins) of two memory devices are electrically connected together and are concurrently active when the two memory devices are concurrently enabled (e.g., by a common chip-select or CS signal). Such a configuration is different from standard memory module configurations in which the output signal pins (e.g., DQS pins) of two memory devices are electrically coupled to the same source, but these pins are not concurrently active since the memory devices are not concurrently enabled. However, a general guideline of memory module design warns against tying together two output signal pins in this way.

[00134] FIGS. 12 and 13 schematically illustrate a problem which may arise from tying together two output signal pins. FIG. 12 schematically illustrates an exemplary memory module **305** in which a first DQS pin **312** of a first memory device **310** is electrically connected to a second DQS pin **322** of a second memory device **320**. The two DQS pins **312**, **322** are both electrically connected to a memory controller **330**.

[00135] FIG. 13 is an exemplary timing diagram of the voltages applied to the two DQS pins **312**, **322** due to non-simultaneous switching. As illustrated by FIG. 13, at time t_1, both the first DQS pin **312** and the second DQS pin **322** are high, so no current flows between them. Similarly, at time t_4, both the first DQS pin **312** and the second DQS pin **322** are low, so no current flows between them. However, for times between approximately t_2 and approximately t_3, the first DQS pin **312** is low while the second DQS pin **322** is high. Under such conditions, a current will flow between the two DQS pins **312**, **322**. This condition in which one DQS pin is low while the other DQS pin is high can occur for fractions of a second (e.g., 0.8 nanoseconds) during the dynamic random-access memory (DRAM) read cycle. During such conditions, the current flowing between the two DQS pins **312**, **322** can be substantial, resulting in heating of the memory devices **310**, **320**, and contributing to the degradation of reliability and eventual failure of these memory devices.

[00136] A second problem may also arise from tying together two output signal pins. FIG. 14 schematically illustrates another exemplary memory module **305** in which a first DQS pin **312** of a first memory device **310** is electrically connected to a second DQS pin **322** of a second memory device **320**. The two DQS pins **312**, **322** of FIG. 14 are both electrically connected to a memory controller (not shown). The DQ (data input/output) pin **314** of the first

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memory device **310** and the corresponding DQ pin **324** of the second memory device **320** are each electrically connected to the memory controller by the DQ bus (not shown). Typically, each memory device **310**, **320** will have a plurality of DQ pins (e.g., eight DQ pins per memory device), but for simplicity, FIG. 14 only shows one DQ pin for each memory device **310**, **320**.

[00137] Each of the memory devices **310**, **320** of FIG. 14 utilizes a respective on-die termination or "ODT" circuit **332**, **334** which has termination resistors (e.g., 75 ohms) internal to the memory devices **310**, **320** to provide signal termination. Each memory device **310**, **320** has a corresponding ODT signal pin **362**, **364** which is electrically connected to the memory controller via an ODT bus **340**. The ODT signal pin **362** of the first memory device **310** receives a signal from the ODT bus **340** and provides the signal to the ODT circuit **332** of the first memory device **310**. The ODT circuit **332** responds to the signal by selectively enabling or disabling the internal termination resistors **352**, **356** of the first memory device **310**. This behavior is shown schematically in FIG. 14 by the switches **342**, **344** which are either closed (dash-dot line) or opened (solid line). The ODT signal pin **364** of the second memory device **320** receives a signal from the ODT bus **340** and provides the signal to the ODT circuit **334** of the second memory device **320**. The ODT circuit **334** responds to the signal by selectively enabling or disabling the internal termination resistors **354**, **358** of the second memory device **320**. This behavior is shown schematically in FIG. 14 by the switches **346**, **348** which are either closed (dash-dot line) or opened (solid line). The switches **342**, **344**, **346**, **348** of FIG. 14 are schematic representations of the operation of the ODT circuits **332**, **334**, and do not signify that the ODT circuits **332**, **334** necessarily include mechanical switches.

[00138] Examples of memory devices **310**, **320** which include such ODT circuits **332**, **334** include, but are not limited to, DDR2 memory devices. Such memory devices are configured to selectively enable or disable the termination of the memory device in this way in response to signals applied to the ODT signal pin of the memory device. For example, when the ODT signal pin **362** of the first memory device **310** is pulled high, the termination resistors **352**, **356** of the first memory device **310** are enabled. When the ODT signal pin **362** of the first memory device **310** is pulled low (e.g., grounded), the termination resistors **352**, **356** of the first memory device **310** are disabled. By selectively disabling the termination resistors of an active memory device, while leaving the termination resistors of inactive memory devices enabled, such configurations advantageously preserve signal strength on the active memory

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device while continuing to eliminate signal reflections at the bus-die interface of the inactive memory devices.

[00139] In certain configurations, as schematically illustrated by FIG. 14, the DQS pins **312**, **322** of each memory device **310**, **320** are selectively connected to a voltage VTT through a corresponding termination resistor **352**, **354** internal to the corresponding memory device **310**, **320**. Similarly, in certain configurations, as schematically illustrated by FIG. 14, the DQ pins **314**, **324** are selectively connected to a voltage VTT through a corresponding termination resistor **356**, **358** internal to the corresponding memory device **310**, **320**. In certain configurations, rather than being connected to a voltage VTT, the DQ pins **314**, **324** and/or the DQS pins **312**, **322** are selectively connected to ground through the corresponding termination resistors **352**, **354**, **356**, **358**. The resistances of the internal termination resistors **352**, **354**, **356**, **358** are selected to clamp the voltages so as to reduce the signal reflections from the corresponding pins. In the configuration schematically illustrated by FIG. 14, each internal termination resistor **352**, **354**, **356**, **358** has a resistance of approximately 75 ohms.

[00140] When connecting the first memory device **310** and, the second memory device **320** together to form a double word width, both the first memory device **310** and the second memory device **320** are enabled at the same time (e.g., by a common CS signal). Connecting the first memory device **310** and the second memory device **320** by tying the DQS pins **312**, **322** together, as shown in FIG. 14, results in a reduced effective termination resistance for the DQS pins **312**, **322**. For example, for the exemplary configuration of FIG. 14, the effective termination resistance for the DQS pins **312**, **322** is approximately 37.5 ohms, which is one-half the desired ODT resistance (for 75-ohm internal termination resistors) to reduce signal reflections since the internal termination resistors **352**, **354** of the two memory devices **310**, **320** are connected in parallel. This reduction in the termination resistance can result in signal reflections causing the memory device to malfunction.

[00141] FIG. 15 schematically illustrates an exemplary memory module **400** in accordance with certain embodiments described herein. The memory module **400** comprises a first memory device **410** having a first data strobe (DQS) pin **412** and a second memory device **420** having a second data strobe (DQS) pin **422**. The memory module **400** further comprises a first resistor **430** electrically coupled to the first DQS pin **412**. The memory module **400** further comprises a second resistor **440** electrically coupled to the second DQS pin **422** and to the first

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resistor **430**. The first DQS pin **412** is electrically coupled to the second DQS pin **422** through the first resistor **430** and through the second resistor **440**.

[00142] In certain embodiments, the memory module **400** is a 1-GB unbuffered Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) high-density dual in-line memory module (DIMM). FIGS. 16A and 16B schematically illustrate a first side **462** and a second side **464**, respectively, of such a memory module **400** with eighteen 64 M×4-bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board (PCB) **460**. In certain embodiments, the memory module **400** further comprises a phase-lock-loop (PLL) clock driver **470**, an EEPROM for serial-presence detect (SPD) data **480**, and decoupling capacitors (not shown) mounted on the PCB in parallel to suppress switching noise on VDD and VDDQ power supply for DDR-1 SDRAM. By using synchronous design, such memory modules **400** allow precise control of data transfer between the memory module **400** and the system controller. Data transfer can take place on both edges of the DQS signal at various operating frequencies and programming latencies. Therefore, certain such memory modules **400** are suitable for a variety of high-performance system applications.

[00143] In certain embodiments, the memory module **400** comprises a plurality of memory devices configured in pairs, each pair having a first memory device **410** and a second memory device **420**. For example, in certain embodiments, a 128 M×72-bit DDR SDRAM high-density memory module **400** comprises thirty-six 64 M×4-bit DDR-1 SDRAM integrated circuits in FBGA packages configured in eighteen pairs. The first memory device **410** of each pair has the first DQS pin **412** electrically coupled to the second DQS pin **422** of the second memory device **420** of the pair. In addition, the first DQS pin **412** and the second DQS pin **422** are concurrently active when the first memory device **410** and the second memory device **420** are concurrently enabled.

[00144] In certain embodiments, the first resistor **430** and the second resistor **440** each has a resistance advantageously selected to reduce the current flow between the first DQS pin **412** and the second DQS pin **422** while allowing signals to propagate between the memory controller and the DQS pins **412**, **422**. In certain embodiments, each of the first resistor **430** and the second resistor **440** has a resistance in a range between approximately 5 ohms and approximately 50 ohms. For example, in certain embodiments, each of the first resistor **430** and the second resistor **440** has a resistance of approximately 22 ohms. Other resistance values

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for the first resistor **430** and the second resistor **440** are also compatible with embodiments described herein. In certain embodiments, the first resistor **430** comprises a single resistor, while in other embodiments, the first resistor **430** comprises a plurality of resistors electrically coupled together in series and/or in parallel. Similarly, in certain embodiments, the second resistor **440** comprises a single resistor, while in other embodiments, the second resistor **440** comprises a plurality of resistors electrically coupled together in series and/or in parallel.

[00145] FIGS. 17A and 17B schematically illustrate an exemplary embodiment of a memory module **400** in which the first resistor **430** and the second resistor **440** are used to reduce the current flow between the first DQS pin **412** and the second DQS pin **422**. As schematically illustrated by FIG. 17A, the memory module **400** is part of a computer system **500** having a memory controller **510**. The first resistor **430** has a resistance of approximately 22 ohms and the second resistor **440** has a resistance of approximately 22 ohms. The first resistor **430** and the second resistor **440** are electrically coupled in parallel to the memory controller **510** through a signal line **520** having a resistance of approximately 25 ohms. The first resistor **430** and the second resistor **440** are also electrically coupled in parallel to a source of a fixed termination voltage (identified by VTT in FIGS. 17A and 17B) by a signal line **540** having a resistance of approximately 47 ohms. Such an embodiment can advantageously be used to allow two memory devices having lower bit widths (e.g., 4-bit) to behave as a single virtual memory device having a higher bit width (e.g., 8-bit).

[00146] FIG. 17B schematically illustrates exemplary current-limiting resistors **430**, **440** in conjunction with the impedances of the memory devices **410**, **420**. During an exemplary portion of a data read operation, the memory controller **510** is in a high-impedance condition, the first memory device **410** drives the first DQS pin **412** high (e.g., 2.7 volts), and the second memory device **420** drives the second DQS pin **422** low (e.g., 0 volts). The amount of time for which this condition occurs is approximated by the time between t_2 and t_3 of FIG. 13, which in certain embodiments is approximately twice the tDQSQ (data strobe edge to output data edge skew time, e.g., approximately 0.8 nanoseconds). At least a portion of this time in certain embodiments is caused by simultaneous switching output (SSO) effects.

[00147] In certain embodiments, as schematically illustrated by FIG. 17B, the DQS driver of the first memory device **410** has a driver impedance R_1 of approximately 17 ohms, and the DQS driver of the second memory device **420** has a driver impedance R_4 of

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approximately 17 ohms. Because the upper network of the first memory device **410** and the first resistor **430** (with a resistance R_2 of approximately 22 ohms) is approximately equal to the lower network of the second memory device **420** and the second resistor **440** (with a resistance R_3 of approximately 22 ohms), the voltage at the midpoint is approximately 0.5*(2.7–0)=1.35 volts, which equals VTT, such that the current flow across the 47-ohm resistor of FIG. 17B is approximately zero.

[00148] The voltage at the second DQS pin **422** in FIG. 17B is given by $V_{DQS2}=2.7*R_4/(R_1+R_2+R_3+R_4)=0.59$ volts and the current flowing through the second DQS pin **422** is given by $I_{DQS2}=0.59/R_4=34$ milliamps. The power dissipation in the DQS driver of the second memory device **420** is thus $P_{DQS2}=34$ mA*0.59 V=20 milliwatts. In contrast, without the first resistor **430** and the second resistor **440**, only the 17-ohm impedances of the two memory devices **410**, **420** would limit the current flow between the two DQS pins **412**, **422**, and the power dissipation in the DQS driver of the second memory device **420** would be approximately 107 milliwatts. Therefore, the first resistor **430** and the second resistor **440** of FIGS. 17A and 17B advantageously limit the current flowing between the two memory devices during the time that the DQS pin of one memory device is driven high and the DQS pin of the other memory device is driven low.

[00149] In certain embodiments in which there is overshoot or undershoot of the voltages, the amount of current flow can be higher than those expected for nominal voltage values. Therefore, in certain embodiments, the resistances of the first resistor **430** and the second resistor **440** are advantageously selected to account for such overshoot/undershoot of voltages.

[00150] For certain such embodiments in which the voltage at the second DQS pin **422** is $V_{DQS2}=0.59$ volts and the duration of the overdrive condition is approximately 0.8 nanoseconds at maximum, the total surge is approximately 0.59 V*1.2 ns=0.3 V-ns. For comparison, the JEDEC standard for overshoot/undershoot is 2.4 V-ns, so certain embodiments described herein advantageously keep the total surge within predetermined standards (e.g., JEDEC standards).

[00151] FIG. 18 schematically illustrates another exemplary memory module **600** compatible with certain embodiments described herein. The memory module **600** comprises a termination bus **605**. The memory module **600** further comprises a first memory device **610**

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having a first data strobe pin **612**, a first termination signal pin **614** electrically coupled to the termination bus **605**, a first termination circuit **616**, and at least one data pin **618**. The first termination circuit **616** selectively electrically terminating the first data strobe pin **612** and the first data pin **618** in response to a first signal received by the first termination signal pin **614** from the termination bus **605**. The memory module **600** further comprises a second memory device **620** having a second data strobe pin **622** electrically coupled to the first data strobe pin **612**, a second termination signal pin **624**, a second termination circuit **626**, and at least one data pin **628**. The second termination signal pin **624** is electrically coupled to a voltage, wherein the second termination circuit **626** is responsive to the voltage by not terminating the second data strobe pin **622** or the second data pin **628**. The memory module **600** further comprises at least one termination assembly **630** having a third termination signal pin **634**, a third termination circuit **636**, and at least one termination pin **638** electrically coupled to the data pin **628** of the second memory device **620**. The third termination signal pin **634** is electrically coupled to the termination bus **605**. The third termination circuit **636** selectively electrically terminates the data pin **628** of the second memory device **620** through the termination pin **638** in response to a second signal received by the third termination signal pin **634** from the termination bus **605**.

[00152] FIG. 19 schematically illustrates a particular embodiment of the memory module **600** schematically illustrated by FIG. 18. The memory module **600** comprises an on-die termination (ODT) bus **605**. The memory module **600** comprises a first memory device **610** having a first data strobe (DQS) pin **612**, a first ODT signal pin **614** electrically coupled to the ODT bus **605**, a first ODT circuit **616**, and at least one data (DQ) pin **618**. The first ODT circuit **616** selectively electrically terminates the first DQS pin **612** and the DQ pin **618** of the first memory device **610** in response to an ODT signal received by the first ODT signal pin **614** from the ODT bus **605**. This behavior of the first ODT circuit **616** is schematically illustrated in FIG. 14 by the switches **672**, **676** which are selectively closed (dash-dot line) or opened (solid line).

[00153] The memory module **600** further comprises a second memory device **620** having a second DQS pin **622** electrically coupled to the first DQS pin **612**, a second ODT signal pin **624**, a second ODT circuit **626**, and at least one DQ pin **628**. The first DQS pin **612** and the second DQS pin **622** are concurrently active when the first memory device **610** and the

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second memory device **620** are concurrently enabled. The second ODT signal pin **624** is electrically coupled to a voltage (e.g., ground), wherein the second ODT circuit **626** is responsive to the voltage by not terminating the second DQS pin **622** or the second DQ pin **624**. This behavior of the second ODT circuit **626** is schematically illustrated in FIG. 14 by the switches **674**, **678** which are opened.

[00154] The memory module **600** further comprises at least one termination assembly **630** having a third ODT signal pin **634** electrically coupled to the ODT bus **605**, a third ODT circuit **636**, and at least one termination pin **638** electrically coupled to the DQ pin **628** of the second memory device **620**. The third ODT circuit **636** selectively electrically terminates the DQ pin **628** of the second memory device **620** through the termination pin **638** in response to an ODT signal received by the third ODT signal pin **634** from the ODT bus **605**. This behavior of the third ODT circuit **636** is schematically illustrated in FIG. 19 by the switch **680** which is either closed (dash-dot line) or opened (solid line).

[00155] In certain embodiments, the termination assembly **630** comprises discrete electrical components which are surface-mounted or embedded on the printed-circuit board of the memory module **600**. In certain other embodiments, the termination assembly **630** comprises an integrated circuit mounted on the printed-circuit board of the memory module **600**. Persons skilled in the art can provide a termination assembly **630** in accordance with embodiments described herein.

[00156] Certain embodiments of the memory module **600** schematically illustrated by FIG. 19 advantageously avoid the problem schematically illustrated by FIG. 12 of electrically connecting the internal termination resistances of the DQS pins of the two memory devices in parallel. As described above in relation to FIG. 14, FIGS. 18 and 19 only show one DQ pin for each memory device for simplicity. Other embodiments have a plurality of DQ pins for each memory device. In certain embodiments, each of the first ODT circuit **616**, the second ODT circuit **626**, and the third ODT circuit **636** are responsive to a high voltage or signal level by enabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by disabling the corresponding termination resistors. In other embodiments, each of the first ODT circuit **616**, the second ODT circuit **626**, and the third ODT circuit **636** are responsive to a high voltage or signal level by disabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by

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enabling the corresponding termination resistors. Furthermore, the switches **672**, **674**, **676**, **678**, **680** of FIG. 18 are schematic representations of the enabling and disabling operation of the ODT circuits **616**, **626**, **636** and do not signify that the ODT circuits **616**, **626**, **636** necessarily include mechanical switches.

[00157] The first ODT signal pin **614** of the first memory device **610** receives an ODT signal from the ODT bus **605**. In response to this ODT signal, the first ODT circuit **616** selectively enables or disables the termination resistance for both the first DQS pin **612** and the DQ pin **618** of the first memory device **610**. The second ODT signal pin **624** of the second memory device **620** is tied (e.g., directly hard-wired) to the voltage (e.g., ground), thereby disabling the internal termination resistors **654**, **658** on the second DQS pin **622** and the second DQ pin **628**, respectively, of the second memory device **620** (schematically shown by open switches **674**, **678** in FIG. 19). The second DQS pin **622** is electrically coupled to the first DQS pin **612**, so the termination resistance for both the first DQS pin **612** and the second DQS pin **622** is provided by the termination resistor **652** internal to the first memory device **510**.

[00158] The termination resistor **656** of the DQ pin **618** of the first memory device **610** is enabled or disabled by the ODT signal received by the first ODT signal pin **614** of the first memory device **610** from the ODT bus **605**. The termination resistance of the DQ pin **628** of the second memory device **620** is enabled or disabled by the ODT signal received by the third ODT signal pin **634** of the termination assembly **630** which is external to the second memory device **620**. Thus, in certain embodiments, the first ODT signal pin **614** and the third ODT signal pin **634** receive the same ODT signal from the ODT bus **605**, and the termination resistances for both the first memory device **610** and the second memory device **620** are selectively enabled or disabled in response thereto when these memory devices are concurrently enabled. In this way, certain embodiments of the memory module **600** schematically illustrated by FIG. 19 provides external or off-chip termination of the second memory device **620**.

[00159] Certain embodiments of the memory module **600** schematically illustrated by FIG. 19 advantageously allow the use of two lower-cost readily-available 512-Mb DDR-2 SDRAM devices to provide the capabilities of a more expensive 1-GB DDR-2 SDRAM device. Certain such embodiments advantageously reduce the total cost of the resultant memory module **600**.

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[00160] Certain embodiments described herein advantageously increase the memory capacity or memory density per memory slot or socket on the system board of the computer system. Certain embodiments advantageously allow for higher memory capacity in systems with limited memory slots. Certain embodiments advantageously allow for flexibility in system board design by allowing the memory module **10** to be used with computer systems designed for different numbers of ranks (e.g., either with computer systems designed for two-rank memory modules or with computer systems designed for four-rank memory modules). Certain embodiments advantageously provide lower costs of board designs.

[00161] In certain embodiments, the memory density of a memory module is advantageously doubled by providing twice as many memory devices as would otherwise be provided. For example, pairs of lower-density memory devices can be substituted for individual higher-density memory devices to reduce costs or to increase performance. As another example, twice the number of memory devices can be used to produce a higher-density memory configuration of the memory module. Each of these examples can be limited by the number of chip select signals which are available from the memory controller or by the size of the memory devices. Certain embodiments described herein advantageously provide a logic mechanism to overcome such limitations.

[00162] Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

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WE CLAIM:

1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a data bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output at least one first data signal and the second memory command to cause the memory module to receive or output at least one second data signal, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, each rank of the plurality of ranks having a same bit width as the memory module, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank, wherein the first rank is selected to receive or output the at least one first data signal in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected to receive or output the at least one second data signal in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command;

a data buffer coupled between the at least one first memory integrated circuit and the data bus, and between the at least one second memory integrated circuit and the data bus; and

logic coupled to the data buffer and configured to respond to the first memory command by providing first control signals to the data buffer to enable communication of the at least one first data signal between the at least one first memory integrated circuit and the memory controller through the data buffer, wherein the logic is further configured to respond to the second memory command by providing second control signals to the data buffer to enable communication of the at least one second data signal between the at least one second memory integrated circuit and the memory controller through the data buffer;

wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.

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2. The memory module of claim 1, wherein the data buffer is configured to isolate both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the data bus when the memory module is not being accessed by the memory controller.

3. The memory module of claim 1, wherein the first memory command includes a first set of chip select signals and the second memory command includes a second set of chip select signals that are different from the first set of chip select signals.

4. The memory module of claim 1, wherein the first memory command includes at least first chip select signal and the second memory command includes at least one second chip select signal, wherein the memory module produces at least third and fourth chip select signals in response to the first memory command, the third chip select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the fourth chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.

5. The memory module of claim 4, wherein the memory module produces at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first memory command, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an active value to cause the at least one second memory integrated circuit to receive or output data signals in response to the second memory command.

6. The memory module of claim 1, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the memory module outputs the at least one first data signal together with at least one

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first data strobe signal in response to the first read command, wherein memory module outputs the at least one second data signal together with at least one second data strobe signal in response to the second read command, wherein the at least one second data signal follows the at least one first data signal on the data bus, and wherein the data buffer is configured to prevent the at least one first data strobe signal and the at least one second data strobe signal from colliding with each other.

7. The memory module of claim 6, wherein each of the at least one first data strobe signal and the at least one second data strobe signal includes a pre-amble interval and a post-amble interval, and wherein the data buffer is configured to combine the at least one first data strobe signal and the at least one second data strobe signal into a combined burst of data strobe signals that does not include the post-amble interval of the at least one first data strobe signal and the pre-amble interval of the at least one second data strobe signal.

8. The memory module of claim 1, further comprising an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits.

9. The memory module of claim 1, wherein the memory module is further coupled to the memory controller using an on-die-termination (ODT) bus, wherein each of the plurality of memory devices includes an ODT circuit, the memory module further comprising a termination circuit external to any of the plurality of memory devices, wherein the termination circuit is coupled to the ODT bus and to the ODT circuit of at least one of the plurality of memory devices, wherein the termination circuit is configured to provide external termination of the at least one of the plurality of memory devices in response to an ODT signal on the ODT bus, and wherein the ODT circuit of the at least one of the plurality of memory devices is disabled.

10. The memory module of claim 1, wherein the data buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the at least one first data signal or the at least one second data signal through the data buffer.

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11. The memory module of claim 1, wherein the logic is further configured to determine the overall CAS latency.

12. The memory module of claim 11, wherein the logic is further configured to enable the communication of the at least one second data signal between the at least one second memory integrated circuit and the memory controller in accordance with the overall CAS latency.

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MEMORY MODULE WITH DATA BUFFERING

ABSTRACT OF THE DISCLOSURE

A memory module operable to communicate data with a memory controller via a data bus comprises a plurality of memory integrated circuits including first memory integrated circuits and second memory integrated circuits, a data buffer coupled between the first memory integrated circuits and the data bus, and between the second memory integrated circuits and the data bus, and logic coupled to the data buffer. The logic is configured to respond to a first memory command by providing first control signals to the data buffer to enable communication of at least one first data signal between the first memory integrated circuits and the memory controller through the data buffer, and is further configured to respond to a second memory command by providing second control signals to the data buffer to enable communication of at least one second data signal between the second memory integrated circuit and the memory controller through the data buffer.

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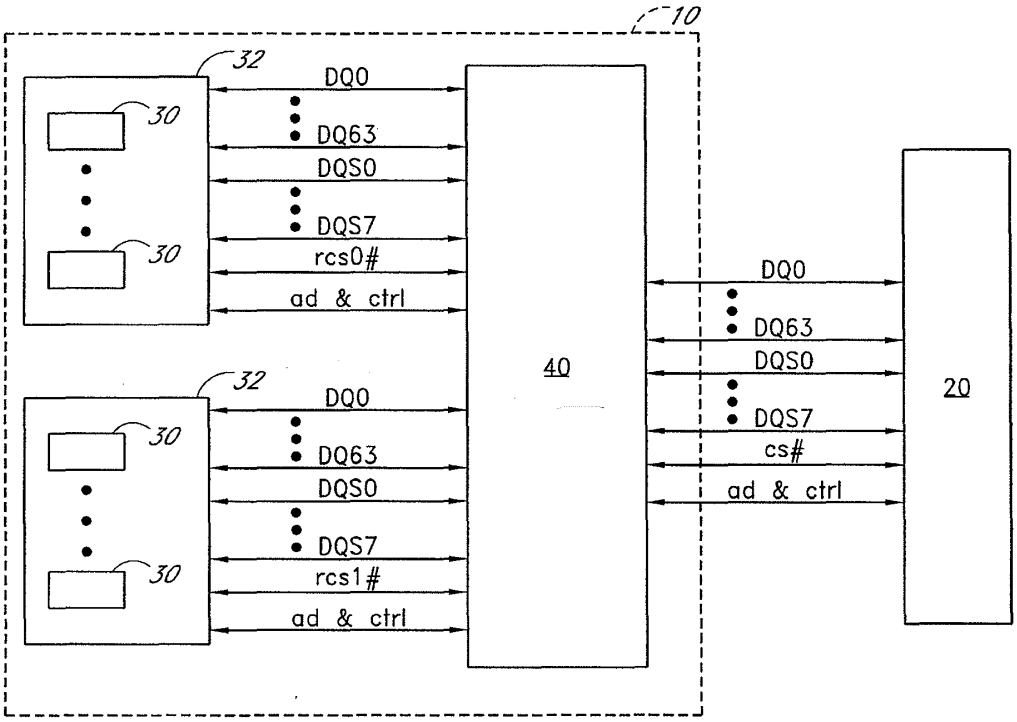

10
32
30
30
DQ0
DQ63
DQS0
DQS7
rcs0#
ad & ctrl
32
30
30
DQ0
DQ63
DQS0
DQS7
rcs1#
ad & ctrl
40
DQ0
DQ63
DQS0
DQS7
cs#
ad & ctrl
20

FIG. 1

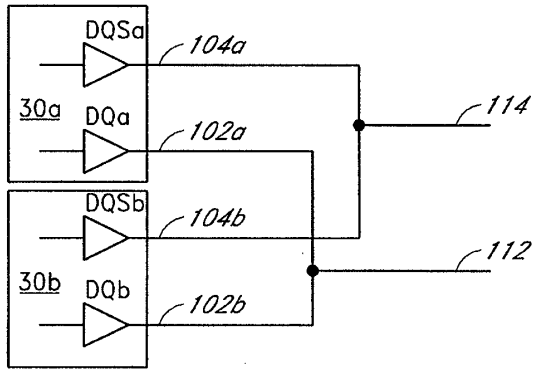


FIG. 2

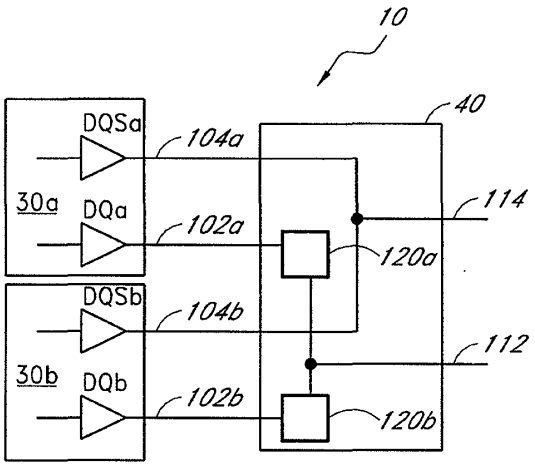

10
40
DQSa
104a
30a
DQa
102a
114
120a
DQSb
104b
112
30b
DQb
102b
120b

FIG. 3A

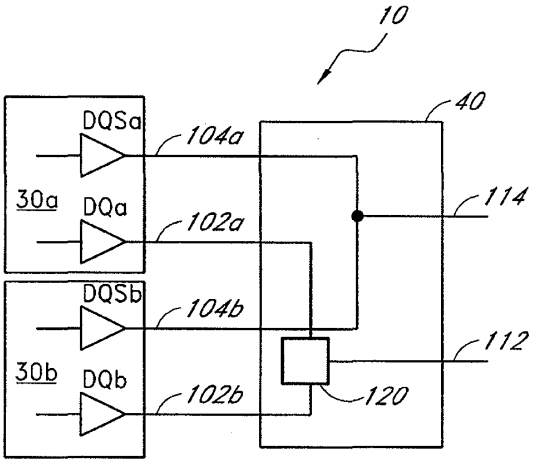

10
40
DQSa
104a
30a
DQa
102a
114
DQSb
104b
112
30b
DQb
102b
120

FIG. 3B

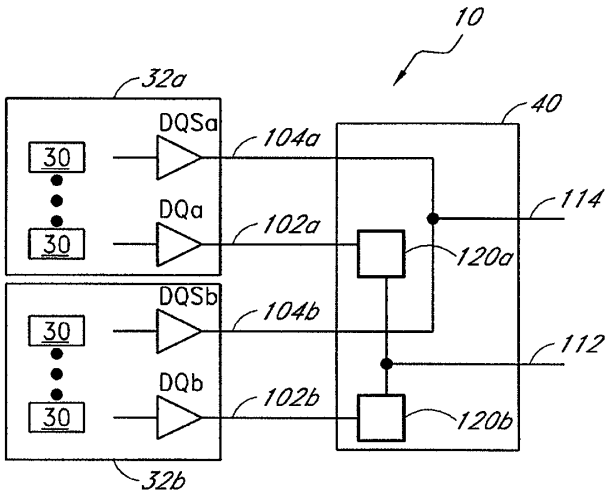

10
32a
40
DQSa
104a
30
DQa
102a
114
30
120a
DQSb
104b
30
112
DQb
102b
30
120b
32b

FIG. 4A

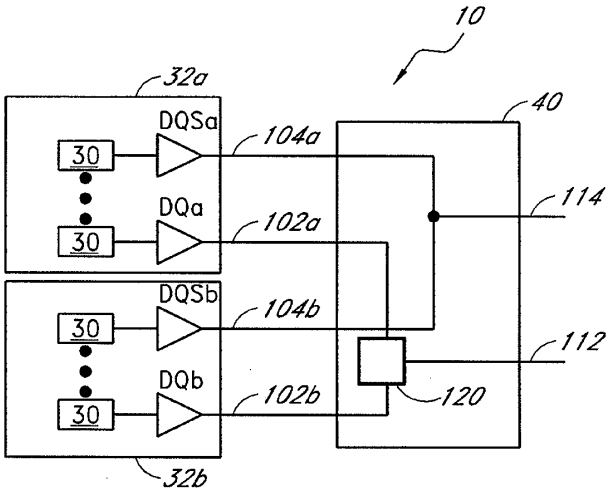

10
32a
40
DQSa
104a
30
114
DQa
102a
30
DQSb
104b
30
112
DQb
102b
30
120
32b

FIG. 4B

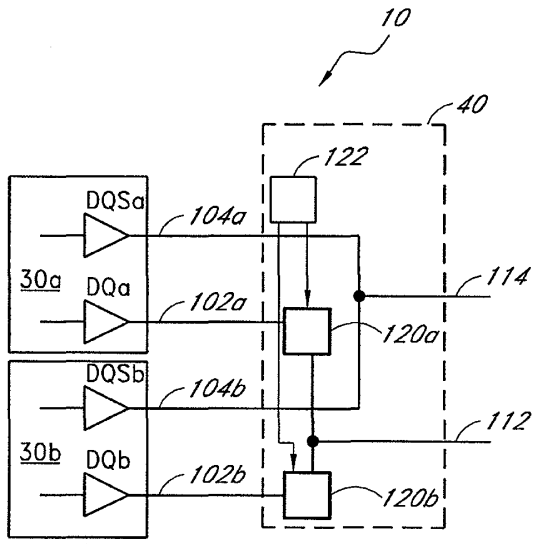

10
40
122
DQSa
104a
30a
DQa
102a
114
120a
DQSb
104b
112
30b
DQb
102b
120b

FIG. 5A

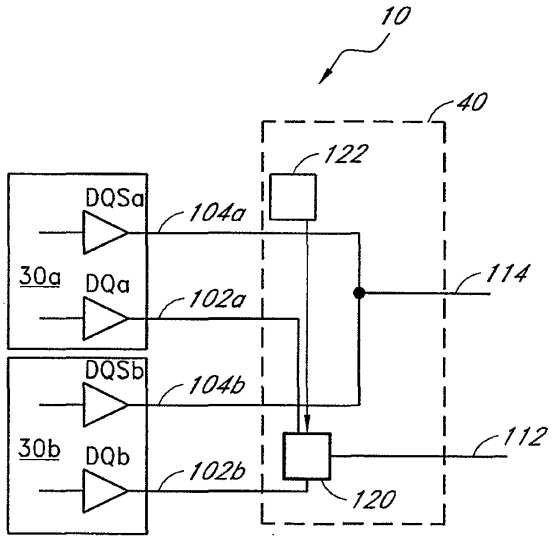

10
40
122
DQSa
104a
30a
DQa
102a
114
DQSb
104b
112
30b
DQb
102b
120

FIG. 5B

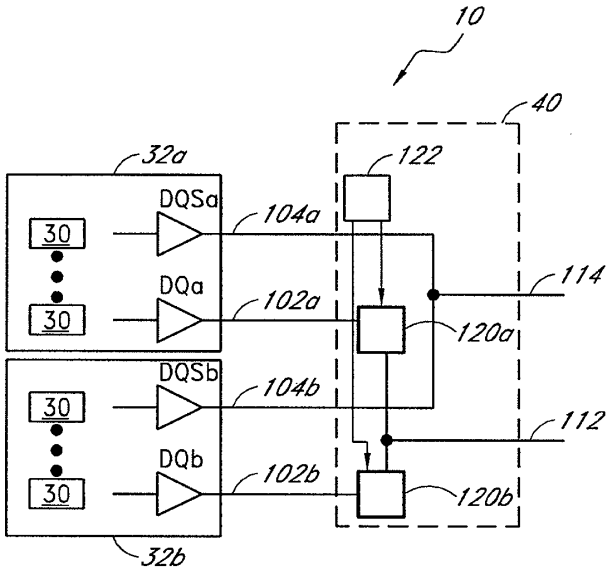

10
40
32a
122
DQSa
104a
30
DQa
102a
114
120a
DQSb
104b
112
DQb
102b
120b
32b

FIG. 5C

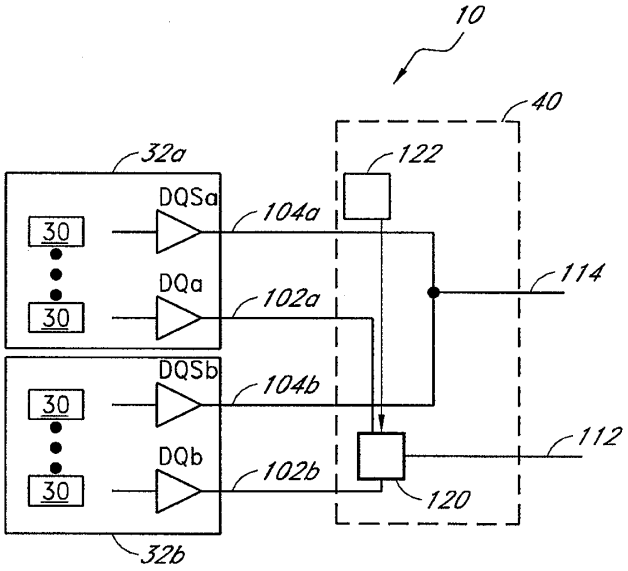

10
40
32a
122
DQSa
104a
30
DQa
102a
114
DQSb
104b
112
DQb
102b
120
32b

FIG. 5D

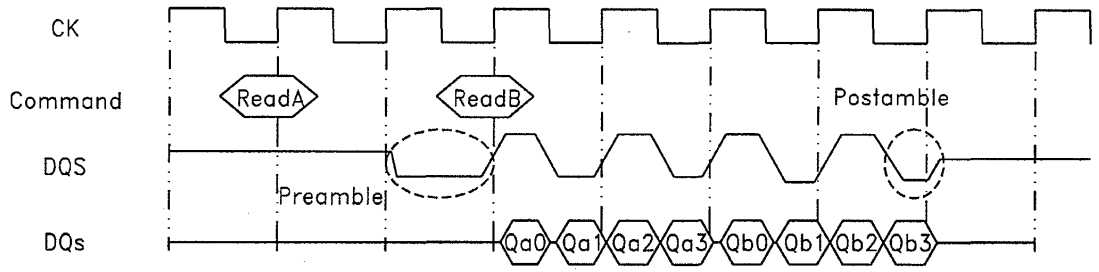

CK
Command
ReadA
ReadB
Postamble
DQS
Preamble
DQs
Qa0
Qa1
Qa2
Qa3
Qb0
Qb1
Qb2
Qb3

FIG. 6A

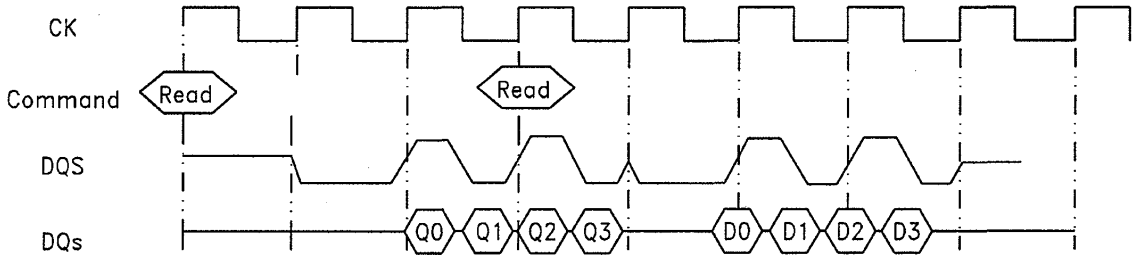

CK
Command
Read
Read
DQS
DQs
Q0
Q1
Q2
Q3
D0
D1
D2
D3

FIG. 6B

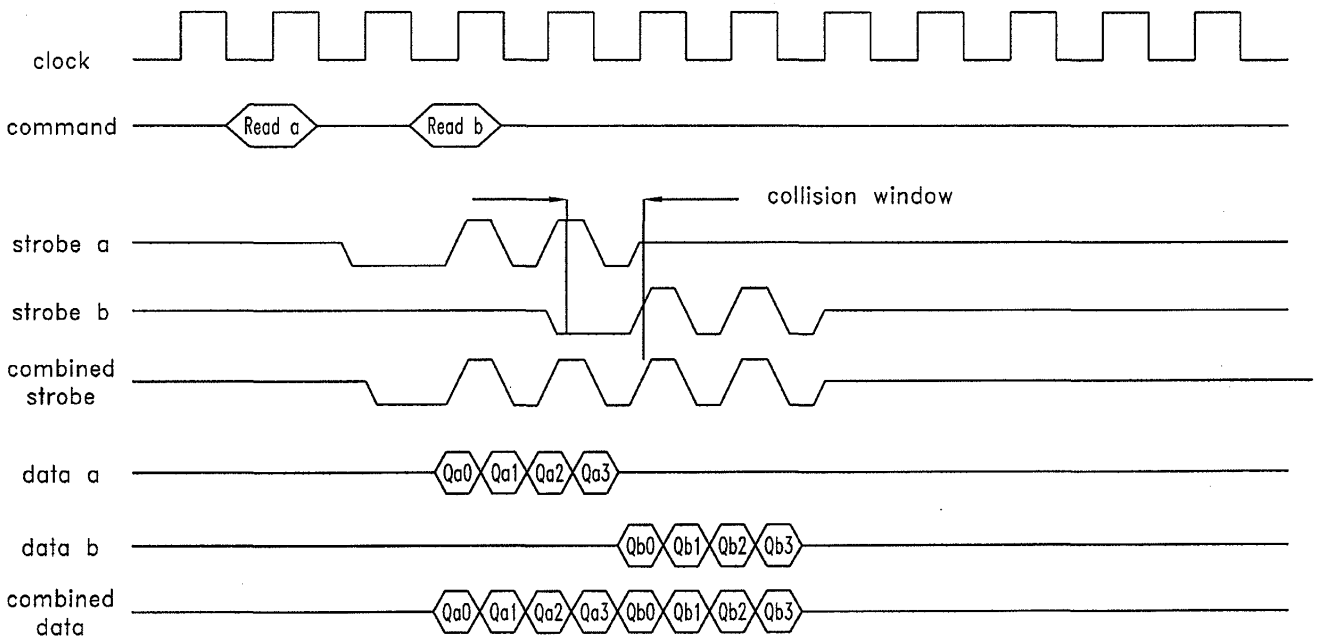

clock
command
Read a
Read b
collision window
strobe a
strobe b
combined strobe
data a
Qa0
Qa1
Qa2
Qa3
data b
Qb0
Qb1
Qb2
Qb3
combined data
Qa0
Qa1
Qa2
Qa3
Qb0
Qb1
Qb2
Qb3

FIG. 7

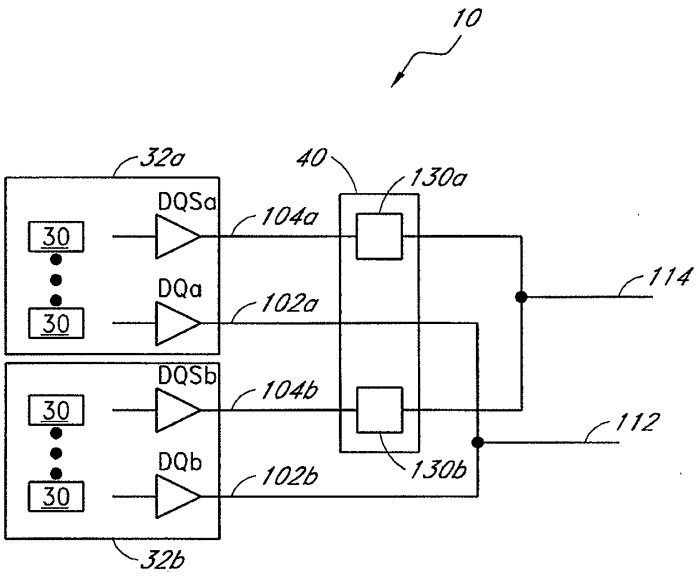

10
32a
40
130a
DQSa
104a
30
30
DQa
102a
114
DQSb
104b
30
30
112
DQb
102b
130b
32b

FIG. 8A

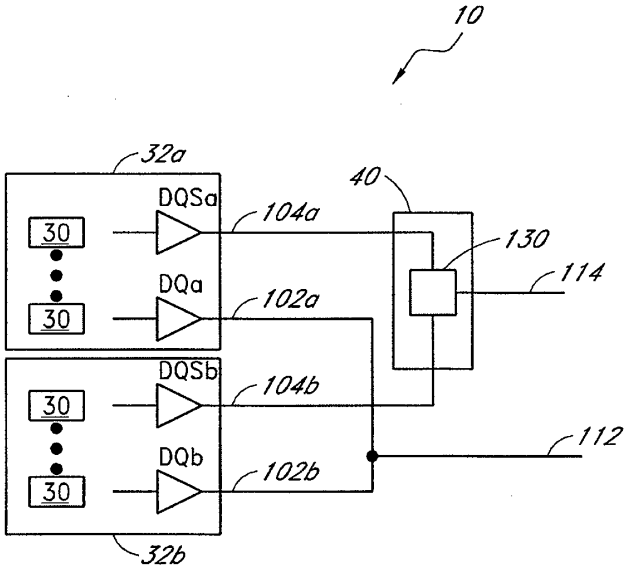

10
32a
40
DQSa
104a
130
30
30
114
DQa
102a
DQSb
104b
30
30
112
DQb
102b
32b

FIG. 8B

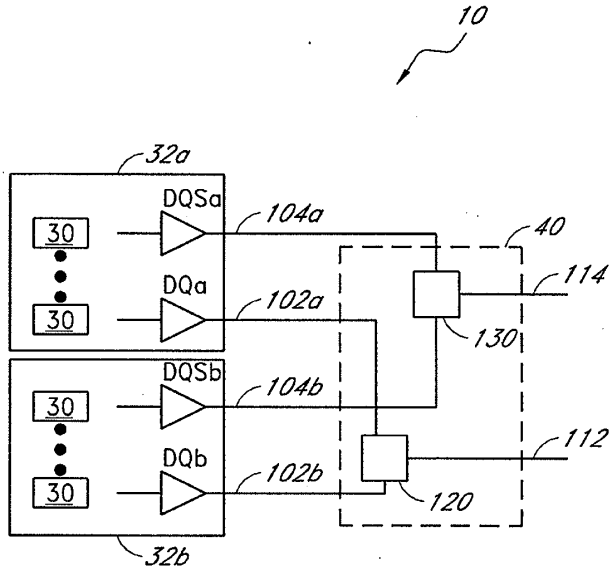

10
32a
DQSa
104a
40
30
114
DQa
102a
30
130
DQSb
104b
30
112
DQb
102b
30
120
32b

FIG. 8C

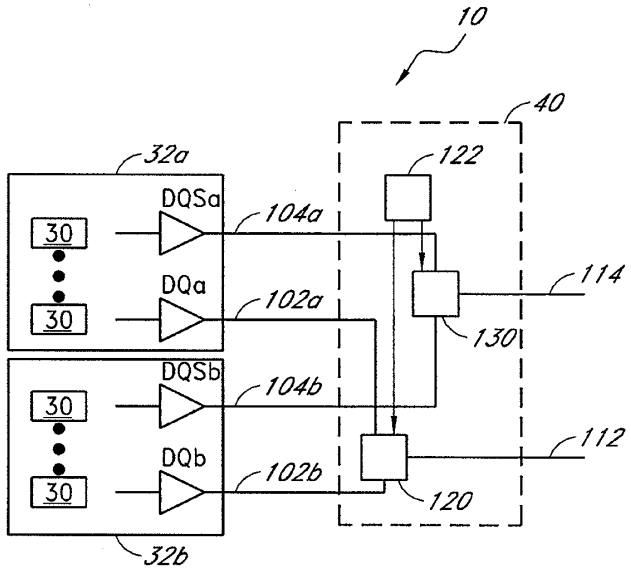

10
40
32a
122
DQSa
104a
30
114
DQa
102a
30
130
DQSb
104b
30
112
DQb
102b
30
120
32b

FIG. 8D

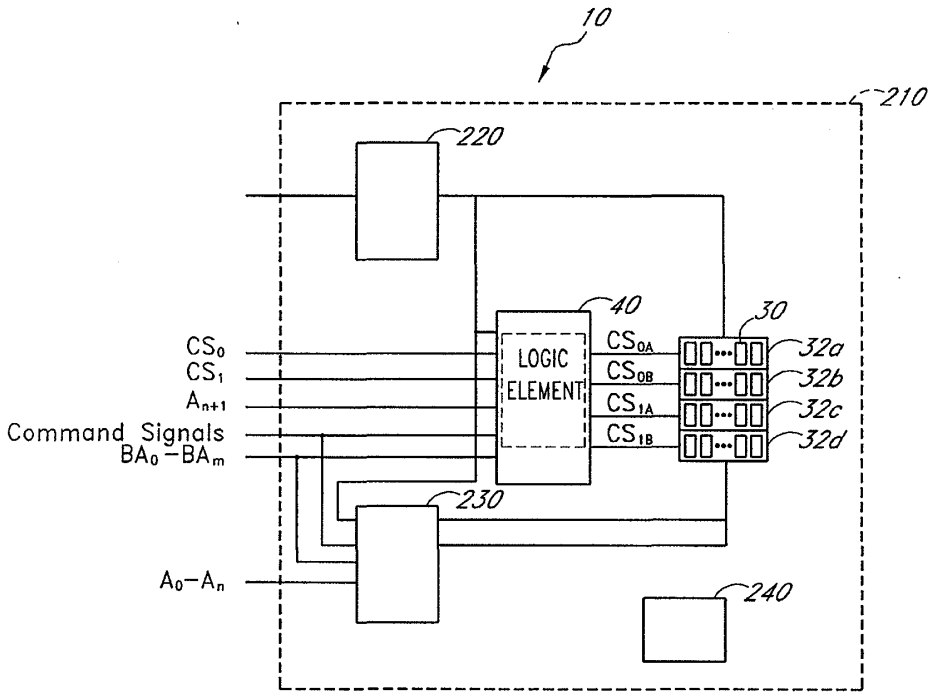

10
210
220
40
30
LOGIC ELEMENT
CS0
CS1
An+1
Command Signals
BA0 – BAm
CS0A
CS0B
CS1A
CS1B
32a
32b
32c
32d
230
A0 – An
240

FIG. 9A

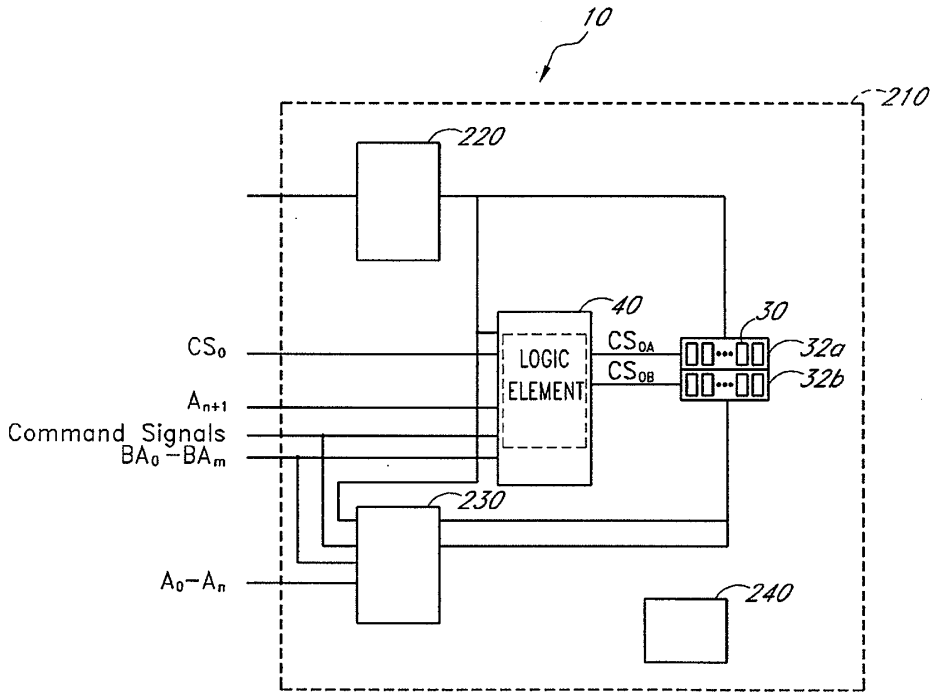

10
210
220
40
30
LOGIC ELEMENT
CS_0
A_{n+1}
Command Signals
BA_0-BA_m
CS_{0A}
CS_{0B}
32a
32b
230
A_0-A_n
240

FIG. 9B

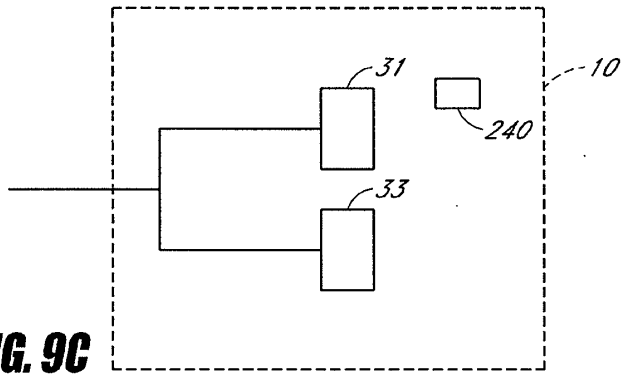


FIG. 9C

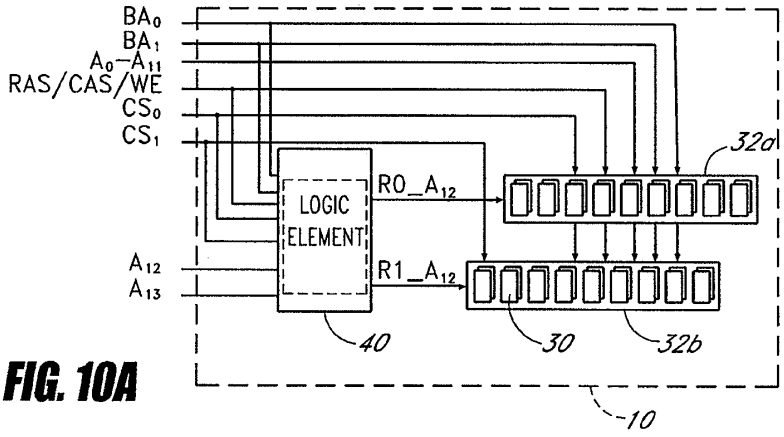


FIG. 10A

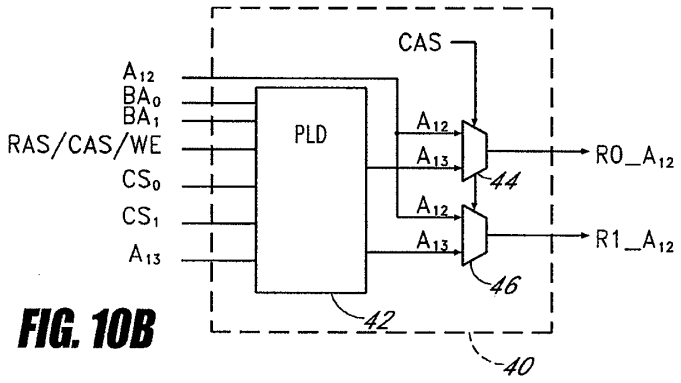


FIG. 10B

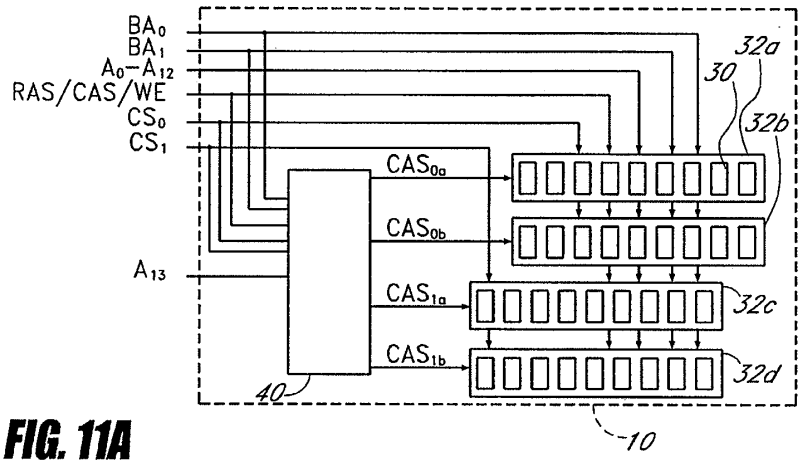


FIG. 11A

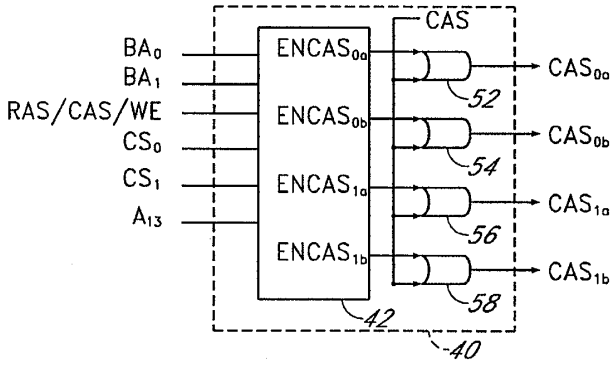


FIG. 11B

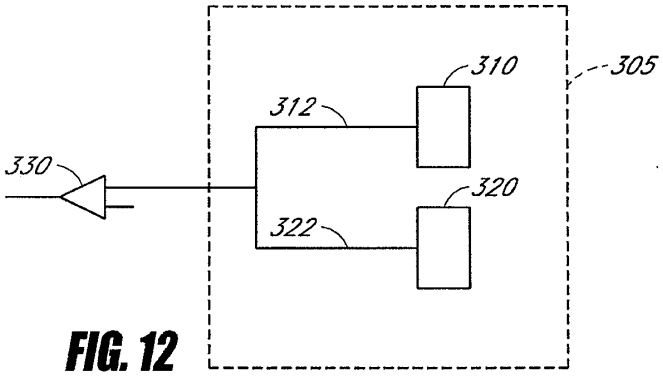


FIG. 12

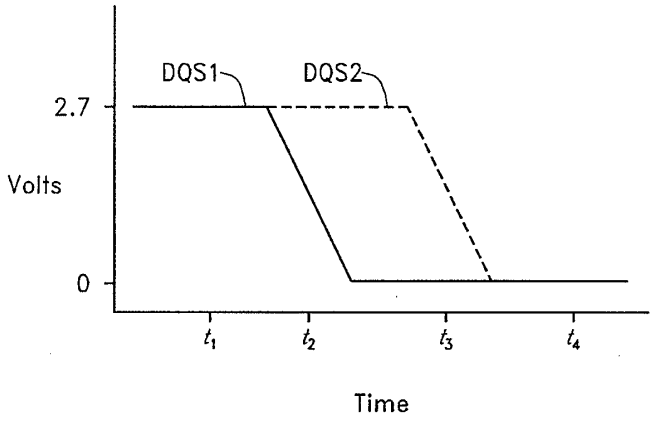


FIG. 13

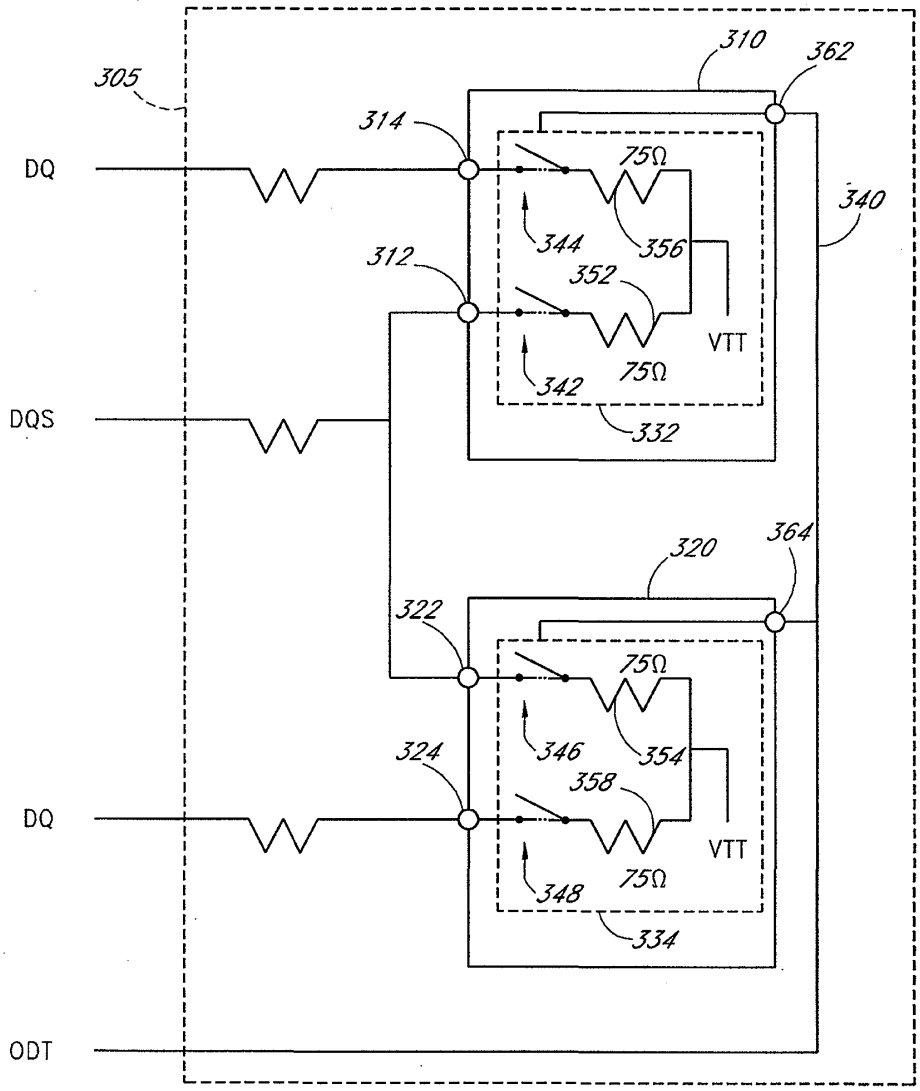

305
310
362
314
75Ω
340
DQ
344
356
312
352
VTT
75Ω
342
DQS
332
320
364
322
75Ω
346
354
324
358
DQ
VTT
75Ω
348
334
ODT

FIG. 14

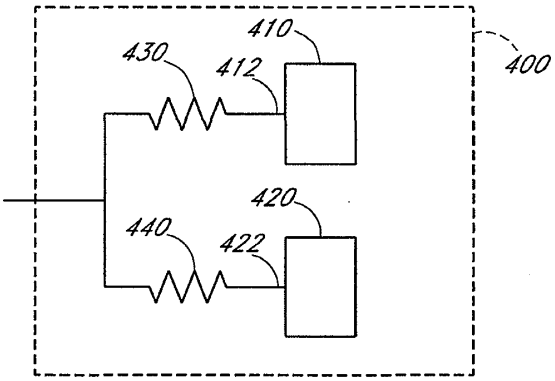


FIG. 15

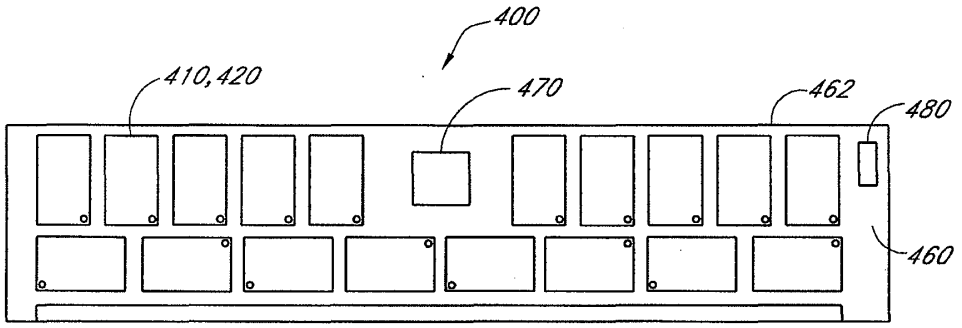


FIG. 16A

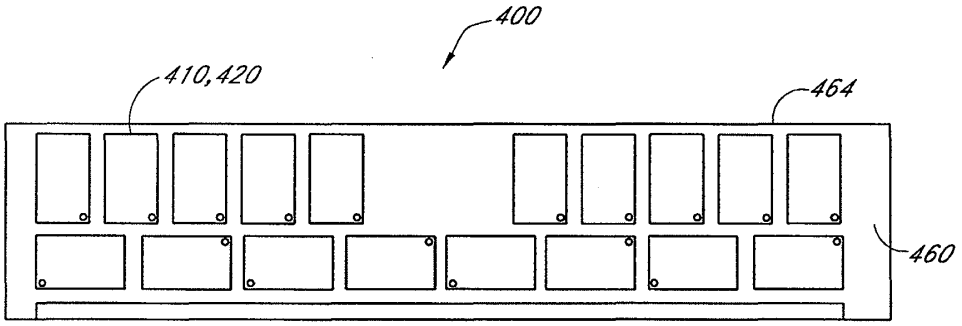


FIG. 16B

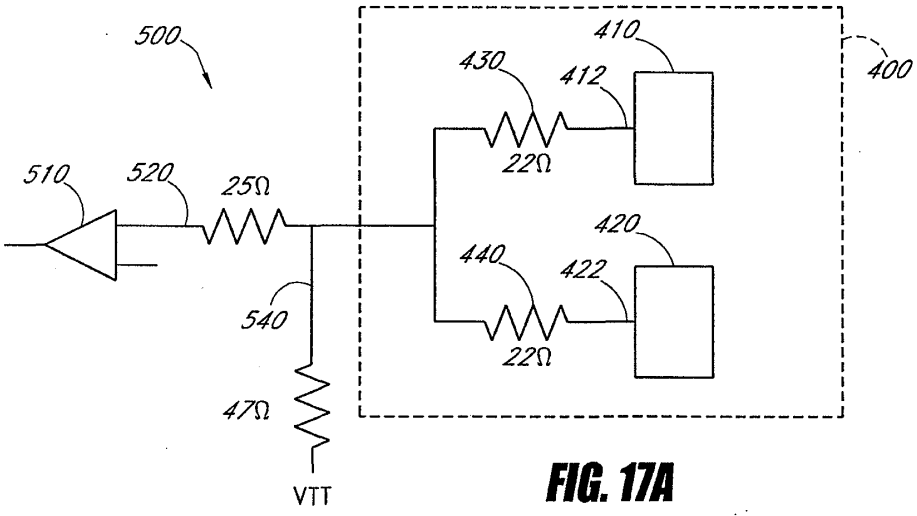


FIG. 17A

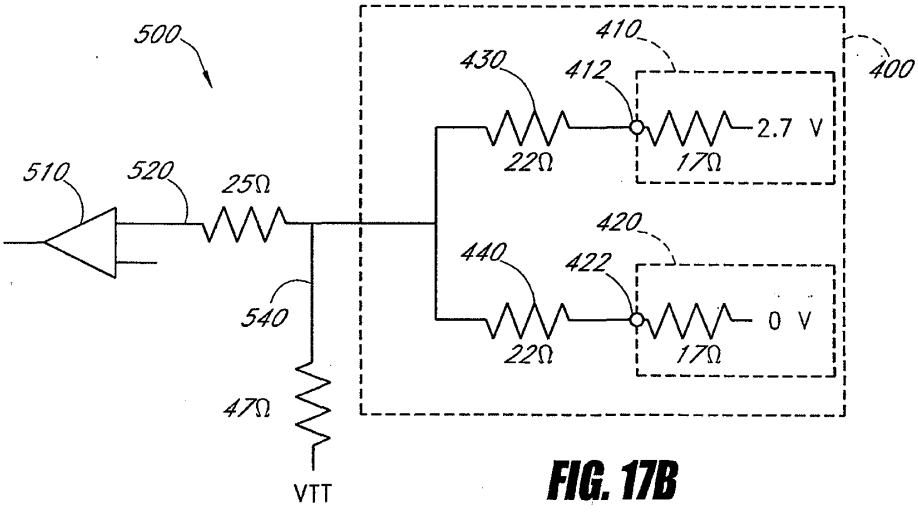


FIG. 17B

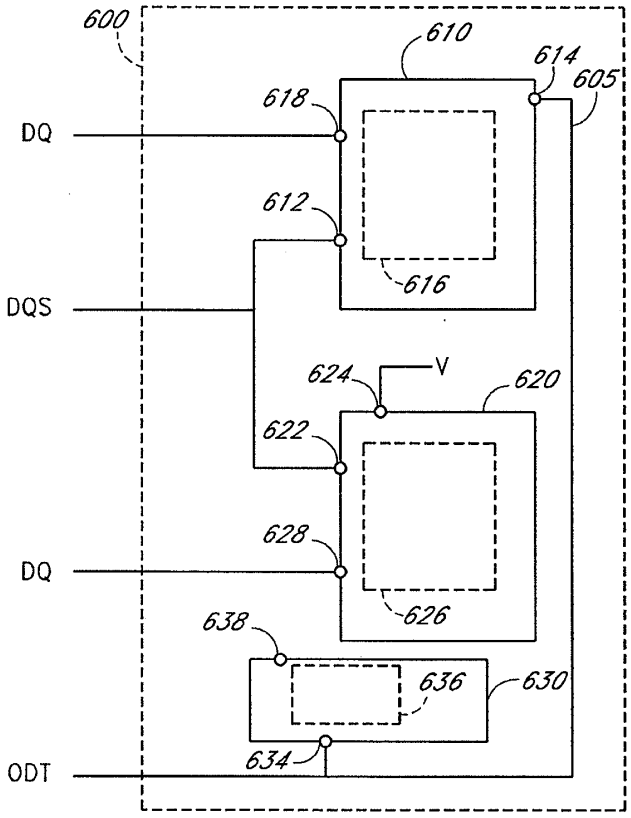

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FIG. 18

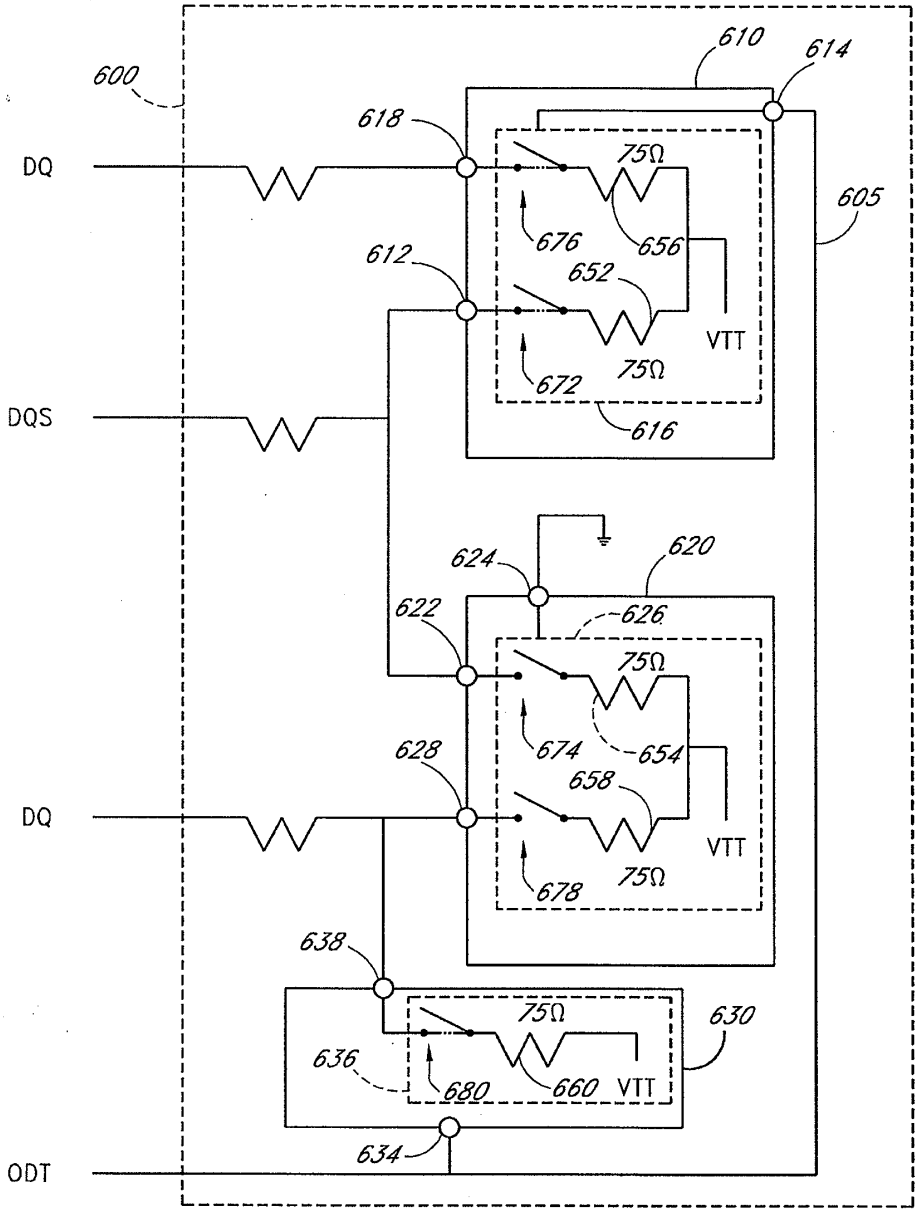

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FIG. 19

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Filer:	Jamie Jie Zheng/Maria Nadal
Attorney Docket Number:	N3044.10002US22

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	280	280
UTILITY SEARCH FEE	1111	1	600	600
UTILITY EXAMINATION FEE	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1600**

Electronic Acknowledgement Receipt	
EFS ID:	31361017
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/Maria Nadal
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	N3044.10002US22
Receipt Date:	28-DEC-2017
Filing Date:	
Time Stamp:	20:26:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	N3044-10002US22_ADS.pdf	1824020 44d9aaacbf209567658c2e0cd169ba60e0865e52	no	10
Warnings:					

Information:					
2	Oath or Declaration filed	N3044_10002US22_OATH.pdf	67889 ab704ad8916a80dc8102fd47b36b942e00c108f0	no	1
Warnings:					
Information:					
3		N3044-1002US22_CON_APPLICATION.pdf	3782042 7a9575fa5c3b18664cde3198775ba6824f7ffce3	yes	57
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	52	
	Claims		53	56	
	Abstract		57	57	
Warnings:					
Information:					
4	Drawings-only black and white line drawings	N3044-10002US22_DRAWINGS.pdf	1047623 656a7d8456716ccfc670dcbb544a0b99143661b1	no	23
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	35018 c13139fcb4c9238c391b0de52d8ea8b477ecd658	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	6756592		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/17 (03-13)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL

Complete if known	
Application Number	15/857,519
Filing Date	2017-12-28
First Named Inventor	Jeffrey C. Solomon
Examiner Name	
Art Unit	
Practitioner Docket No.	N3044.10002US22

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

TOTAL AMOUNT OF PAYMENT ($) 1600

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 505394 Deposit Account Name: Maschoff Brennan

For the above-identified deposit account, the Director is hereby authorized to (check all that apply):

☑ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☐ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayment of fee(s)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES (U = undiscounted fee; S = small entity fee; M = micro entity fee)

	FILING FEES			SEARCH FEES			EXAMINATION FEES			
Application Type	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**Fees Paid ($)**
Utility	280	140*	70	600	300	150	720	360	180	1600.00
Design	180	90	45	120	60	30	460	230	115	
Plant	180	90	45	380	190	95	580	290	145	
Reissue	280	140	70	600	300	150	2,160	1,080	540	
Provisional	260	130	65	0	0	0	0	0	0	

* The $140 small entity status filing fee for a utility application is further reduced to $70 for a small entity status applicant who files the application via EFS-Web.

2. EXCESS CLAIM FEES

Fee Description	**Undiscounted Fee ($)**	**Small Entity Fee ($)**	**Micro Entity Fee ($)**
Each claim over 20 (including Reissues)	80	40	20
Each independent claim over 3 (including Reissues)	420	210	105
Multiple dependent claims	780	390	195

Total Claims		**Extra Claims**	**Fee ($)**		**Fee Paid ($)**
12	-20 or HP =	0	x 0	=	0

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		**Extra Claims**	**Fee ($)**		**Fee Paid ($)**
0	-3 or HP =	0	x 0	=	0

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	**Fee ($)**	**Fee Paid ($)**

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $400 ($200 for small entity) ($100 for micro entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		**Extra Sheets**		**Number of each additional 50 or fraction thereof**	**Fee ($)**		**Fee Paid ($)**
800	- 100 =	200	/ 50 =	0 (round **up** to a whole number)	x 0	=	0

4. OTHER FEE(S)

	Fees Paid ($)
Non-English specification, $130 fee (no small or micro entity discount)	0
Non-electronic filing fee under 37 CFR 1.16(t) for a utility application, $400 fee ($200 small or micro entity)	0
Other (e.g., late filing surcharge): _____	0

SUBMITTED BY

Signature	/Jaime J. Zheng/	Registration No. (Attorney/Agent) 51167	Telephone
Name (Print/Type)	Jaime J. Zheng		Date 2017-12-28

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	15857519
Filing Date:	
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Filer:	Jamie Jie Zheng/Maria Nadal
Attorney Docket Number:	N3044.10002US22

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	280	280
UTILITY SEARCH FEE	1111	1	600	600
UTILITY EXAMINATION FEE	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1600**

Electronic Acknowledgement Receipt	
EFS ID:	31361212
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/Maria Nadal
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	N3044.10002US22
Receipt Date:	28-DEC-2017
Filing Date:	
Time Stamp:	21:03:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Fee Worksheet (SB06)	N3044_10002US22_FEE_TRANSMITTAL.pdf	264337 4161063c728222a5094777114603 9fce7d8278b5	no	2
Warnings:					

Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	35338 eb1eb665715dbc8d9ba55b8586bde5194b276105	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	299675	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Patent Application Fee Transmittal

Application Number:	15857519
Filing Date:	
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Filer:	Jamie Jie Zheng/Maria Nadal
Attorney Docket Number:	N3044.10002US22

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	280	280
UTILITY SEARCH FEE	1111	1	600	600
UTILITY EXAMINATION FEE	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1600**

Electronic Acknowledgement Receipt	
EFS ID:	31361077
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Correspondence Address:	Jamie J. Zheng, Ph.D Esq. MASCHOFF BRENNAN 1389 Center Drive Suite 300 Park City UT 84098 US (435) 252-1360 bisraelsen@mabr.com
Filer:	Jamie Jie Zheng/Maria Nadal
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	N3044.10002US22
Receipt Date:	28-DEC-2017
Filing Date:	
Time Stamp:	20:35:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Fee Worksheet (SB06)	fee-info.pdf	35339 c7352f95be99ab9cee39eee426a7c6a9af7cf3e3	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	35339		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

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New International Application Filed with the USPTO as a Receiving Office

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Confirmation No.	:	**9826**
Appln. No.	:	**15/857,519**
Applicant	:	**Netlist, Inc.**
First Inventor	:	**Jeffrey C. Solomon**
Filed	:	**December 28, 2017**
TC/A.U.	:	**2139**
Examiner	:	**Not yet assigned**
Docket No.	:	**N3044.10002US22**
Customer No.	:	**97149**
Title	:	**Memory Module with Data Buffering**

CORRECTED APPLICATION DATA SHEET

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner,

The Applicant hereby submits the following Corrected Application Data Sheet in the above referenced patent application. Attached please find a marked Application Data Sheet showing the desired changes; specifically in the Domestic Benefit 13/971232 should be **13/971231**.

The Commissioner is authorized to charge any fee which may be required in connection with this communication or credit any overpayment to deposit account No. 50-5394.

Respectfully submitted,

Dated: 2 January 2018

/Jaime Zheng /
Jaime Zheng, Ph.D.
Registration No. 51167
Customer No. 97149

MASCHOFF BRENNAN
1389 Center Drive, Suite 300
Park City, Utah 84098
Irvine, California 92618
Telephone: 949-202-1901
Email: Docket@mabr.com

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	N3044.10002US22
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jeffrey	C.	Solomon	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Irvine	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	16 Silver Fir		
Address 2			
City	Irvine	State/Province	CA
Postal Code	92604	Country i	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jayesh	R.	Bhakta	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Cerritos	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	12220 Rose Street		
Address 2			
City	Cerritos	State/Province	CA
Postal Code	90703	Country i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	N3044.10002US22
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	79141		
Email Address	Docket@mabr.com	Add Email	Remove Email
Email Address	JZheng@mabr.com	Add Email	Remove Email

Application Information:

Title of the Invention	MEMORY MODULE WITH DATA BUFFERING		
Attorney Docket Number	N3044.10002US22	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	23	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	79141		

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	N3044.10002US22
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	14/715486	2015-05-18

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14/715486	Continuation of	~~13/971233~~13971231	2013-08-20	9037774	2015-05-19

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/971232	Continuation of	13/287081	2011-11-01	8516188	2013-08-20

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/287081	Continuation of	13032470	2011-02-22	8081536	2011-12-20

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13032470	Continuation of	12955711	2010-11-29	7916574	2011-03-29

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12955711	Continuation of	12/629827	2009-12-02	7881150	2011-02-01

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/629827	Continuation of	12/408652	2009-03-20	7636274	2009-12-22

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/408652	Continuation of	11/335875	2006-01-19	7532537	2009-05-12

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	N3044.10002US22
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/335875	Claims benefit of provisional	60/645087	2005-01-19

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11/335875	Continuation in part of	11/173175	2005-07-01	7289386	2007-10-30

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/173175	Claims benefit of provisional	60/588244	2004-07-15

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11/173175	Continuation in part of	11/075395	2005-03-07	7286436	2007-10-23

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/075395	Claims benefit of provisional	60/550668	2004-03-05

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/075395	Claims benefit of provisional	60/575595	2004-05-28

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/075395	reissue of	60/590038	2004-07-21

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	N3044.10002US22
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[1] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[j] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	N3044.10002US22
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	N3044.10002US22
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

(●) Assignee	( ) Legal Representative under 35 U.S.C. 117	( ) Joint Inventor
( ) Person to whom the inventor is obligated to assign.	( ) Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Netlist, Inc.		
Mailing Address Information For Applicant:			
Address 1	175 Technology, #150		
Address 2			
City	Irvine	**State/Province**	CA
Country	US	Postal Code	92618
Phone Number	949-435-0025	Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	N3044.10002US22
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Jaime J. Zheng/			Date (YYYY-MM-DD)	2017-12-28
First Name	Jaime J.	Last Name	Zheng	Registration Number	51167

Additional Signature may be generated within this form by selecting the Add button.

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	N3044.10002US22
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	31384813
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/Maria Nadal
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	N3044.10002US22
Receipt Date:	02-JAN-2018
Filing Date:	
Time Stamp:	17:41:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		N3044-10002US22_CORRECTED_ADS_1-2-2018.pdf	789455 f74020ac0e3abb3e65de7cca2edc60e38023041e	yes	11

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	1
	Application Data Sheet	2	11
Warnings:			
Information:			
	Total Files Size (in bytes):	789455	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Document Code: IMIS

Notice of Fee Due

Application Number: 15857519 Date:01/23/18

Fees are due for the application or document dated 12/28/17 . The payment was not collectable for the reason indicated below.

Note: If the fee due is for any of the filing fees, the surcharge for late payment of the filing fees is now due as well.

- ☐ Insufficient payment by check or money order.
- ☐ No authorization to charge a deposit account.
- ☐ Invalid deposit account number.
- ☒ User name not listed in deposit account 50-5394 at 11:45AM (time).
- ☐ Insufficient funds in deposit account at AM (time).
- ☐ Insufficient payment by credit card.
- ☐ Declined credit card _____:_____ (time).

Fee code(s) to be applied:	1011	$280
	1111	$600
	1311	$720
		$
		$
		$
Amount in holding fee code:		$
	1622/2622	$
	1999	$

Total remaining due from applicant: $1600

RAM Operator_____AS_____

Rev. 04/10/2013

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/857,519	12/28/2017	2139	0.00	N3044.10002US22	12	1

CONFIRMATION NO. 9826

79141
Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

FILING RECEIPT



Date Mailed: 02/05/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jeffrey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 14/715,486 05/18/2015 PAT 9858215
which is a CON of 13/971,231 08/20/2013 PAT 9037774
which is a CON of 13/287,081 11/01/2011 PAT 8516188
which is a CON of 13/032,470 02/22/2011 PAT 8081536
which is a CON of 12/955,711 11/29/2010 PAT 7916574
which is a CON of 12/629,827 12/02/2009 PAT 7881150
which is a CON of 12/408,652 03/20/2009 PAT 7636274
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7289386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7286436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004
and claims benefit of 60/590,038 07/21/2004

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 02/02/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/857,519**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

MEMORY MODULE WITH DATA BUFFERING

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign

patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/857,519

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	12 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/857,519	12/28/2017	Jeffrey C. Solomon	N3044.10002US22

CONFIRMATION NO. 9826

79141
Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

FORMALITIES LETTER

OC000000097150452

Date Mailed: 02/05/2018

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1880** TOTAL FEE BALANCE DUE.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ttran/

Electronically filed July 5, 2018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jeffrey C. Solomon	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	To be assigned
For:	MEMORY MODULE WITH DATA BUFFERING	Attorney Docket No:	129980-5023US

RESPONSE TO THE NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION WITH PETITION FOR EXTENSION OF TIME

Mail Stop: MISSING PARTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Notice to File Missing Parts mailed February 5, 2018, enclosed is the Notice to File Missing Parts of Nonprovisional Application for the above-identified application. The fee for the late oath or declaration surcharge is estimated to be $160.

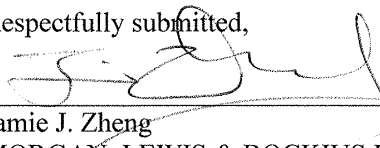
Also enclosed please find a Fee Transmittal Form setting forth the calculation for the statutory basic filing, search and examination fees, together with the excess claim fees due in this matter. The fees calculated for the statutory basic filing, search and examination fees together with the excess claim fees and application size fee (if applicable) are estimated to be $1720.

Petition for Extension of Time under 37 CFR 1.136. It is respectfully requested that the time for response to the Notice to File Missing Parts dated February 5, 2018 be extended for a period of three months from April 5, 2018 to July 5, 2018.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US).

Respectfully submitted,

Date: July 5, 2018



51167

Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/857,519	12/28/2017	Jeffrey C. Solomon	N3044.10002US22

CONFIRMATION NO. 9826

79141
Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

FORMALITIES LETTER

OC000000097150452

Date Mailed: 02/05/2018

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

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- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
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- $ **760** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1880** TOTAL FEE BALANCE DUE.

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/ttran/

Electronic Patent Application Fee Transmittal

Application Number:	15857519
Filing Date:	28-Dec-2017
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Filer:	Jamie Jie Zheng/Lata olivier
Attorney Docket Number:	129980-5023US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	160	160
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 3 months with $0 paid	1253	1	1400	1400
Miscellaneous:				
		Total in USD ($)		**3280**

Electronic Acknowledgement Receipt	
EFS ID:	33101399
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/Lata olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023US
Receipt Date:	05-JUL-2018
Filing Date:	28-DEC-2017
Time Stamp:	21:00:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$3280
RAM confirmation Number	070618INTEFSW00005645500310
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	129980_5023US_RESPONSE.pdf	150945 c4bcc5d6af94136e8f6212e4729252613fb6a2fb	no	4
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	39380 886e5059f7c1e41f5999604f3c0f22bbb243479e	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	190325		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/857,519	12/28/2017	2139	1880	129980-5023US	12	1

CONFIRMATION NO. 9826

UPDATED FILING RECEIPT

79141
Morgan Lewis Bockius LLP / Jamie Zheng Ph.D.
1400 Page Mill Road
Palo Alto, CA 94304

OC000000100818980

Date Mailed: 07/10/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jeffrey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 14/715,486 05/18/2015 PAT 9858215
which is a CON of 13/971,231 08/20/2013 PAT 9037774
which is a CON of 13/287,081 11/01/2011 PAT 8516188
which is a CON of 13/032,470 02/22/2011 PAT 8081536
which is a CON of 12/955,711 11/29/2010 PAT 7916574
which is a CON of 12/629,827 12/02/2009 PAT 7881150
which is a CON of 12/408,652 03/20/2009 PAT 7636274
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7289386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7286436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004
and claims benefit of 60/590,038 07/21/2004

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 02/02/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/857,519**

Projected Publication Date: 10/18/2018

Non-Publication Request: No

Early Publication Request: No

Title

MEMORY MODULE WITH DATA BUFFERING

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/857,519

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	12 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

Electronically filed September 14, 2018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Netlist, Inc.	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	BANSAL, Gurteg
For:	*MEMORY MODULE WITH DATA BUFFERING*	Attorney Docket No.:	129980-5023-US
		Date:	September 14, 2018

PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

Applicant files herewith a Preliminary Amendment in the above-referenced patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US).

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a data bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output first data and first data strobes ~~at least one first data signal~~ and the second memory command to cause the memory module to receive or output second data and second data strobes ~~at least one second data signal~~, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks ~~including a first rank and a second rank~~, each rank of the plurality of ranks having a same bit width as the memory module, ~~the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank,~~ wherein the plurality of ranks include a first rank ~~is~~ selected to receive or output the first data and first data strobes ~~at least one first data signal~~ in response to the first memory command ~~and is not selected to communicate data with the memory controller in response to the second memory command~~, and ~~wherein the~~a second rank ~~is~~ selected to receive or output the second data and second data strobes ~~at least one second data signal~~ in response to the second memory command ~~and is not selected to communicate data with the memory controller in response to the first memory command~~;

a data buffer coupled between ~~the~~ at least one first memory integrated circuit in the first rank and the data bus, and between ~~the~~ at least one second memory integrated circuit in the second rank and the data bus; and

logic coupled to the data buffer and configured to respond to the first memory command by providing first control signals to the data buffer to enable communication of respective bits of the ~~at least one~~ first data ~~signal~~ and respective data strobes of the first data strobes between the at

least one first memory integrated circuit and the memory controller through the data buffer, wherein the logic is further configured to respond to the second memory command by providing second control signals to the data buffer to enable communication of respective bits of the ~~at least one~~ second data and respective strobes of the second data strobes ~~signal~~ between the at least one second memory integrated circuit and the memory controller through the data buffer, the first data including a first data burst and the second data including a second data burst following the first data burst on the data bus;

wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.

2. (Currently Amended) The memory module of claim 1, wherein each of the plurality memory integrated circuits has a corresponding load, and wherein the data buffer is configured to isolate the loads of both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory controller~~data bus when the memory module is not being accessed by the memory controller~~.

3. The memory module of claim 1, wherein the logic is coupled to the printed circuit board and is further configured to respond to the first read/write memory command by outputting a first set of command signals and to respond to the second read/write command by outputting a second set of command signals, the first set of command signals including ~~wherein the first memory command includes~~ a first set of chip select signals corresponding to respective ones of the plurality of ranks and the second ~~memory~~ set of command ~~includes~~ signals including a second set of chip select signals corresponding to respective ones of the plurality of ranks ~~that are different from the first set of chip select signals~~, the first set of chip select signals including a first chip select signal having an active signal value while the rest of the first set of chip select signals each has a non-active signal value, the second set of chip select signals including a second chip select signal having an active signal value while the rest of the second set of chip select signals each has a non-active signal value, wherein the first rank is configured to receive the first chip select signal and the second rank is configured to receive the second chip select signal.

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Original) The memory module of claim 1, further comprising an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits.

9. (Original) The memory module of claim 1, wherein the memory module is further coupled to the memory controller using an on-die-termination (ODT) bus, wherein each of the plurality of memory devices includes an ODT circuit, the memory module further comprising a termination circuit external to any of the plurality of memory devices, wherein the termination circuit is coupled to the ODT bus and to the ODT circuit of at least one of the plurality of memory devices, wherein the termination circuit is configured to provide external termination of ~~the~~ at least one of the plurality of memory devices in response to an ODT signal on the ODT bus, and wherein the ODT circuit of the at least one of the plurality of memory devices is disabled.

10. (Currently Amended) The memory module of claim 1, wherein the data buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the ~~at least one~~ respective bits of the first data ~~signal~~ and respective data strobes of the first data strobes or the ~~at least one~~ respective bits of the second data ~~signal~~ and respective data strobes of the second data strobes through the data buffer.

11. (Original) The memory module of claim 1, wherein the logic is further configured to determine the overall CAS latency.

12. (Currently Amended) The memory module of claim 1 ~~11~~, wherein the logic is further configured to enable ~~the~~ communication of the first data and the first data strobes or the second data and the second data strobes ~~at least one second data signal between the at least one second memory integrated circuit~~ between the memory module and the memory controller in accordance with the overall CAS latency.

13. (New) The memory module of claim 1, wherein each of the plurality of ranks is 72-bit wide, wherein the plurality of memory integrated circuits include 36 4-bit wide memory integrated circuits configured in 18 pairs, wherein the at least one first memory integrated circuit includes a first pair of memory integrated circuits configured to communicate a respective byte of the first data, and wherein the at least one second memory integrated circuit includes a second pair of memory integrated circuits configured to communicate a respective byte of the second data.

14. (New) The memory module of claim 13, wherein the first pair of memory integrated circuits are configured to simulate an 8-bit wide memory device, and the second pair of memory integrated circuits are configured to simulate another 8-bit wide memory device.

15. (New) The memory module of claim 13, further comprising an SPD device programmed with data to characterize each pair of memory integrated circuits as a virtual 8-bit wide memory device.

16. (New) The memory module of claim 1, wherein the data buffer includes switches each coupled between a respective data or strobe pin of the at least one first memory device and a corresponding signal line in the data bus, and between a respective data or strobe pin of the at least one second memory device and the corresponding signal line in the data bus, and wherein the first control signals include control signals for enabling the switches and the second control signals include control signals for enabling the switches.

17. (New) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to read/write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to respond to a first read/write memory command by outputting a first set of command signals, the first set of command signals including a first plurality of chip select signals, the first plurality of chip select signals including a first chip select signal having an active signal value while the rest of the first plurality of chip select signals each has a non-active signal value;

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Ex. 1054, p. 145

memory devices mounted on the printed circuit board and arranged in a plurality of ranks, each rank of the plurality of ranks having a same data width as the memory module, wherein the plurality of ranks correspond to, and are configured to receive, respective ones of the first plurality of chip select signals, wherein a first rank in the plurality of ranks receiving the first chip select signal is selected to receive or output a first burst of data and a first burst of data strobes in response to the first read/write command, wherein each of the memory devices is 4-bits wide, and wherein each of the plurality of ranks is 72-bits wide and include 18 memory devices configured in pairs;

at least one buffer coupled between data and strobe signal lines in the memory bus and corresponding data and strobe pins of the memory devices in each of the plurality of ranks; and

wherein the logic is further configured to output control signals to the at least one buffer to enable communication of the first burst of data and the first burst of data strobes between the first rank and the memory controller through the at least one buffer; and

wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the memory devices.

18. (New) The memory module of claim 17, wherein each of the 4-bit-wide memory devices has a corresponding load, and the at least one buffer is configured to isolate the loads of the memory devices from the memory bus.

19. (New) The memory module of claim 17, wherein the first burst of data include a set of consecutively transmitted data bits for each data signal line in the memory bus.

20. (New) The memory module of claim 17, wherein the logic is further configured to respond to a second read/write memory command by outputting a second set of command signals, the second set of command signals including a second plurality of chip select signals corresponding to respective ranks of the plurality of ranks, the second plurality of chip select signals including a second chip select signal having the active signal value while the rest of the second plurality of chip select signals each has a non-active signal value, wherein a second rank different from the first rank is configured to receive the second chip select signal and is selected to output or receive a second burst of data and a second burst of data strobes in response to the second read/write command, wherein the logic is further configured to output control signals to the at least one buffer to enable communication of the second burst of data and the second burst

of strobes between the second rank and the memory controller through the at least one buffer, the second burst of data following the first burst of data on the memory bus.

21. (New) The memory module of claim 17, wherein each pair of 4-bit-wide memory devices are configured to simulate an 8-bit-wide memory device.

22. (New) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to read/write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to respond to a read/write memory command by outputting a set of command signals, the set of command signals including a plurality of chip select signals, the plurality of chip select signals including one chip select signal having an active signal value while the rest of the plurality of chip select signals each has a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of ranks each having a same data width as the memory module, wherein the plurality of ranks correspond to, and are configured to receive, respective ones of the plurality of chip select signals, wherein a first rank receiving the chip select signal having the active signal value is selected to receive or output a first burst of data and a first burst of data strobes in response to the read/write command, wherein each of the memory devices is 4-bits wide, and have a set of data pins and one or more data strobe pins, and wherein each of the plurality of ranks is 72-bits wide and include 18 memory devices configured in pairs;

a plurality of switches each coupled between a data or strobe signal line in the memory bus and a corresponding data or strobe pin in each of the plurality of ranks; and

wherein the logic is further configured to output control signals for enabling the switches to allow communication of the first burst of data and the first burst of data strobes between the first rank and the memory controller; and

wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the memory devices.

23. (New) The memory module of claim 22, wherein the first burst of data include a set of consecutively transmitted data bits for each data signal line in the memory bus.

24. (New) The memory module of claim 22, wherein the logic is further configured to respond to a subsequent read/write memory command by outputting subsequent set of command signals, the subsequent set of command signals including a subsequent plurality of chip select signals corresponding to respective ranks of the plurality of ranks, the subsequent plurality of chip select signals including one subsequent chip select signal having the active signal value while the rest of the subsequent plurality of chip select signals each has a non-active signal value, wherein a second rank different from the first rank is configured to receive the subsequent chip select signal having the active signal value and is selected to output or receive a second burst of data and a second burst of data strobes in response to the subsequent read/write command, wherein the logic is further configured to output control signals for enabling the switches to allow communication of the second burst of data and the second burst of data strobes between the second rank and the memory controller.

REMARKS

In this Preliminary Amendment, claims 4-7 are cancelled, claims 1-3, 10, and 12 are amended for accuracy and clarity, and new claims 13-24 are presented. Support for the amendments and new claims can be found throughout the Specification and Drawings (for example, in paragraphs [0047], [0053], [0058], [0068], [0072], [0081]-[0089], [0097], [0122], and [0144], and FIGS. 6A-6B and FIG. 8D). Therefore, no new matter is added.

CONCLUDING REMARKS

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner consider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 843-4000, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: September 14, 2018

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
Phone: (650) 843-4000

Electronic Acknowledgement Receipt	
EFS ID:	33732310
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5023US
Receipt Date:	14-SEP-2018
Filing Date:	28-DEC-2017
Time Stamp:	20:22:50
Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980_5023US_PRE_AMEND.pdf	162755 406fbae426815e934513d9c72a83eb90a4af800b	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Claims	2	8
	Applicant Arguments/Remarks Made in an Amendment	9	9
Warnings:			
Information:			
	Total Files Size (in bytes):	162755	

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed September 14, 2018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Netlist, Inc.	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	BANSAL, Gurteg
For:	*MEMORY MODULE WITH DATA BUFFERING*	Attorney Docket No.:	129980-5023-US
		Date:	September 14, 2018

PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

Applicant files herewith a Preliminary Amendment in the above-referenced patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US).

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a data bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output first data and first data strobes ~~at least one first data signal~~ and the second memory command to cause the memory module to receive or output second data and second data strobes ~~at least one second data signal~~, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks ~~including a first rank and a second rank~~, each rank of the plurality of ranks having a same bit width as the memory module, ~~the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank,~~ wherein the plurality of ranks include a first rank ~~is~~ selected to receive or output the first data and first data strobes ~~at least one first data signal~~ in response to the first memory command ~~and is not selected to communicate data with the memory controller in response to the second memory command~~, and ~~wherein the~~a second rank ~~is~~ selected to receive or output the second data and second data strobes ~~at least one second data signal~~ in response to the second memory command ~~and is not selected to communicate data with the memory controller in response to the first memory command~~;

a data buffer coupled between ~~the~~ at least one first memory integrated circuit in the first rank and the data bus, and between ~~the~~ at least one second memory integrated circuit in the second rank and the data bus; and

logic coupled to the data buffer and configured to respond to the first memory command by providing first control signals to the data buffer to enable communication of respective bits of the ~~at least one~~ first data ~~signal~~ and respective data strobes of the first data strobes between the at

least one first memory integrated circuit and the memory controller through the data buffer, wherein the logic is further configured to respond to the second memory command by providing second control signals to the data buffer to enable communication of respective bits of the ~~at least one~~ second data and respective strobes of the second data strobes ~~signal~~ between the at least one second memory integrated circuit and the memory controller through the data buffer, the first data including a first data burst and the second data including a second data burst following the first data burst on the data bus;

wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.

2. (Currently Amended) The memory module of claim 1, wherein each of the plurality memory integrated circuits has a corresponding load, and wherein the data buffer is configured to isolate the loads of both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory controller~~data bus when the memory module is not being accessed by the memory controller~~.

3. (Currently Amended) The memory module of claim 1, wherein the logic is coupled to the printed circuit board and is further configured to respond to the first read/write memory command by outputting a first set of command signals and to respond to the second read/write command by outputting a second set of command signals, the first set of command signals including ~~wherein the first memory command includes~~ a first set of chip select signals corresponding to respective ones of the plurality of ranks and the second ~~memory~~ set of command ~~includes~~ signals including a second set of chip select signals corresponding to respective ones of the plurality of ranks ~~that are different from the first set of chip select signals~~, the first set of chip select signals including a first chip select signal having an active signal value while the rest of the first set of chip select signals each has a non-active signal value, the second set of chip select signals including a second chip select signal having an active signal value while the rest of the second set of chip select signals each has a non-active signal value, wherein the first rank is configured to receive the first chip select signal and the second rank is configured to receive the second chip select signal.

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Original) The memory module of claim 1, further comprising an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits.

9. (Original) The memory module of claim 1, wherein the memory module is further coupled to the memory controller using an on-die-termination (ODT) bus, wherein each of the plurality of memory devices includes an ODT circuit, the memory module further comprising a termination circuit external to any of the plurality of memory devices, wherein the termination circuit is coupled to the ODT bus and to the ODT circuit of at least one of the plurality of memory devices, wherein the termination circuit is configured to provide external termination of ~~the~~ at least one of the plurality of memory devices in response to an ODT signal on the ODT bus, and wherein the ODT circuit of the at least one of the plurality of memory devices is disabled.

10. (Currently Amended) The memory module of claim 1, wherein the data buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the ~~at least one~~ respective bits of the first data ~~signal~~ and respective data strobes of the first data strobes or the ~~at least one~~ respective bits of the second data ~~signal~~ and respective data strobes of the second data strobes through the data buffer.

11. (Original) The memory module of claim 1, wherein the logic is further configured to determine the overall CAS latency.

12. (Currently Amended) The memory module of claim 1 ~~11~~, wherein the logic is further configured to enable ~~the~~ communication of the first data and the first data strobes or the second data and the second data strobes ~~at least one second data signal between the at least one second memory integrated circuit~~ between the memory module and the memory controller in accordance with the overall CAS latency.

13. (New) The memory module of claim 1, wherein each of the plurality of ranks is 72-bit wide, wherein the plurality of memory integrated circuits include 36 4-bit wide memory integrated circuits configured in 18 pairs, wherein the at least one first memory integrated circuit includes a first pair of memory integrated circuits configured to communicate a respective byte of the first data, and wherein the at least one second memory integrated circuit includes a second pair of memory integrated circuits configured to communicate a respective byte of the second data.

14. (New) The memory module of claim 13, wherein the first pair of memory integrated circuits are configured to simulate an 8-bit wide memory device, and the second pair of memory integrated circuits are configured to simulate another 8-bit wide memory device.

15. (New) The memory module of claim 13, further comprising an SPD device programmed with data to characterize each pair of memory integrated circuits as a virtual 8-bit wide memory device.

16. (New) The memory module of claim 1, wherein the data buffer includes switches each coupled between a respective data or strobe pin of the at least one first memory device and a corresponding signal line in the data bus, and between a respective data or strobe pin of the at least one second memory device and the corresponding signal line in the data bus, and wherein the first control signals include control signals for enabling the switches and the second control signals include control signals for enabling the switches.

17. (New) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to read/write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to respond to a first read/write memory command by outputting a first set of command signals, the first set of command signals including a first plurality of chip select signals, the first plurality of chip select signals including a first chip select signal having an active signal value while the rest of the first plurality of chip select signals each has a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of ranks, each rank of the plurality of ranks having a same data width as the memory module, wherein the plurality of ranks correspond to, and are configured to receive, respective ones of the first plurality of chip select signals, wherein a first rank in the plurality of ranks receiving the first chip select signal is selected to receive or output a first burst of data and a first burst of data strobes in response to the first read/write command, wherein each of the memory devices is 4-bits wide, and wherein each of the plurality of ranks is 72-bits wide and include 18 memory devices configured in pairs;

at least one buffer coupled between data and strobe signal lines in the memory bus and corresponding data and strobe pins of the memory devices in each of the plurality of ranks; and

wherein the logic is further configured to output control signals to the at least one buffer to enable communication of the first burst of data and the first burst of data strobes between the first rank and the memory controller through the at least one buffer; and

wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the memory devices.

18. (New) The memory module of claim 17, wherein each of the 4-bit-wide memory devices has a corresponding load, and the at least one buffer is configured to isolate the loads of the memory devices from the memory bus.

19. (New) The memory module of claim 17, wherein the first burst of data include a set of consecutively transmitted data bits for each data signal line in the memory bus.

20. (New) The memory module of claim 17, wherein the logic is further configured to respond to a second read/write memory command by outputting a second set of command signals, the second set of command signals including a second plurality of chip select signals corresponding to respective ranks of the plurality of ranks, the second plurality of chip select signals including a second chip select signal having the active signal value while the rest of the second plurality of chip select signals each has a non-active signal value, wherein a second rank different from the first rank is configured to receive the second chip select signal and is selected to output or receive a second burst of data and a second burst of data strobes in response to the second read/write command, wherein the logic is further configured to output control signals to the at least one buffer to enable communication of the second burst of data and the second burst

of strobes between the second rank and the memory controller through the at least one buffer, the second burst of data following the first burst of data on the memory bus.

21. (New) The memory module of claim 17, wherein each pair of 4-bit-wide memory devices are configured to simulate an 8-bit-wide memory device.

22. (New) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to read/write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to respond to a read/write memory command by outputting a set of command signals, the set of command signals including a plurality of chip select signals, the plurality of chip select signals including one chip select signal having an active signal value while the rest of the plurality of chip select signals each has a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of ranks each having a same data width as the memory module, wherein the plurality of ranks correspond to, and are configured to receive, respective ones of the plurality of chip select signals, wherein a first rank receiving the chip select signal having the active signal value is selected to receive or output a first burst of data and a first burst of data strobes in response to the read/write command, wherein each of the memory devices is 4-bits wide, and have a set of data pins and one or more data strobe pins, and wherein each of the plurality of ranks is 72-bits wide and include 18 memory devices configured in pairs;

a plurality of switches each coupled between a data or strobe signal line in the memory bus and a corresponding data or strobe pin in each of the plurality of ranks; and

wherein the logic is further configured to output control signals for enabling the switches to allow communication of the first burst of data and the first burst of data strobes between the first rank and the memory controller; and

wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the memory devices.

23. (New) The memory module of claim 22, wherein the first burst of data include a set of consecutively transmitted data bits for each data signal line in the memory bus.

24. (New) The memory module of claim 22, wherein the logic is further configured to respond to a subsequent read/write memory command by outputting subsequent set of command signals, the subsequent set of command signals including a subsequent plurality of chip select signals corresponding to respective ranks of the plurality of ranks, the subsequent plurality of chip select signals including one subsequent chip select signal having the active signal value while the rest of the subsequent plurality of chip select signals each has a non-active signal value, wherein a second rank different from the first rank is configured to receive the subsequent chip select signal having the active signal value and is selected to output or receive a second burst of data and a second burst of data strobes in response to the subsequent read/write command, wherein the logic is further configured to output control signals for enabling the switches to allow communication of the second burst of data and the second burst of data strobes between the second rank and the memory controller.

REMARKS

This Preliminary Amendment replaces the Preliminary Amendment filed earlier on even date herewith, where claim 3 is missing the status identifier.

Claims 4-7 are cancelled, claims 1-3, 10, and 12 are amended for accuracy and clarity, and new claims 13-24 are presented. Support for the amendments and new claims can be found throughout the Specification and Drawings (for example, in paragraphs [0047], [0053], [0058], [0068], [0072], [0081]-[0089], [0097], [0122], and [0144], and FIGS. 6A-6B and FIG. 8D). Therefore, no new matter is added.

CONCLUDING REMARKS

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner consider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 843-4000, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: September 14, 2018

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

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1400 Page Mill Road
Palo Alto, CA 94304
Phone: (650) 843-4000

Electronic Acknowledgement Receipt

EFS ID:	33732372
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5023US
Receipt Date:	14-SEP-2018
Filing Date:	28-DEC-2017
Time Stamp:	20:29:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980_5023US_PRE_AMEND.pdf	162921 06480aeb7c3df57dde7f195e2ec4d6229ef35661	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Claims	2	8
	Applicant Arguments/Remarks Made in an Amendment	9	9
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New International Application Filed with the USPTO as a Receiving Office
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/857,519	Filing Date 12/28/2017	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	09/14/2018	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**0**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
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The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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Sheet 1 of 40

Complete if Known	
Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number / Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1.	Patent Trial and Appeal Board Decision on Request for Rehearing for Reexamination Control No. 95/001,381, mailed August 13, 2014, 7 pages.	
	2.	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control Nos. 95/000,546 and 95/000,577, mailed February 25,2015, 25 pages.	
	3.	Patent Trial and Appeal Board Decision on Request for Rehearing for Reexamination Control Nos. 95/000,546 and 95/000,577, mailed August 27, 2015, 5 pages.	
	4.	Examiner's Determination after Board Decision on Appeal for Reexamination Control No. 95/001,337, mailed September 11, 2015, 16 pages.	
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	6.	Inter Partes Review Case No. IPR2014-01020, Exhibit 1002 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on April 7, 2015.	
	7.	Inter Partes Review Case No. IPR2014-01020, Exhibit 1023 to Petition for Inter Partes Review, curriculum vitae of Dr. Srinivasan Jagannathan, filed on April 7, 2015.	
	8.	Inter Partes Review Case No. IPR2014-01020, Exhibit 1025 to Petition for Inter Partes Review, "operational," *The Pocket Oxford American Dictionary of Current English,* Oxford University Press, 2002, filed on April 7, 2015.	
	9.	Inter Partes Review Case No. IPR2014-01020, Decision to Institute Inter Partes Review of D U.S. Patent No. 7,881,150, dated October 8, 2015.	
	10.	Inter Partes Review Case No. IPR2015-01 021, Petition for Inter Partes Review of U.S. Patent No. 8,081,536, filed on April 7, 2015	
	11.	Inter Partes Review Case No. IPR2014-01 021, Corrected Exhibit 1002 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on April 22, 2015.	
	12.	Inter Partes Review Case No. IPR2014-01 021, Exhibit 1026 to Petition for Inter Partes Review, curriculum vitae of Dr. Srinivasan Jagannathan, filed on April 7, 2015.	
	13.	Inter Partes Review Case No. IPR2014-01 021, Decision to Institute Inter Partes Review of U.S. Patent No. 8,081,536, dated October 8, 2015	
	14.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.,* Corrected Joint Claim Construction and Prehearing Statement Pursuant to Patent L.R. 4-3, including Exhibit A, filed August 27,2014, 28 pages.	
	15.	U.S. Court of Appeals for the Federal Circuit, Decision on Appeal for Reexamination Control No. 95/001,381, filed November 13, 2015, 14 pages	

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Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Sheet 3 of 40

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Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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	35.	5655153	08-05-1997	EMC CORP	
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Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

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Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

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First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

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Sheet 9 of 40

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Filing Date	***December 28, 2017***
First Named Inventor	***Jeffrey C. Solomon***
Art Unit	***2139***
Examiner Name	***Bansal, Gurtej***
Attorney Docket Number	***129980-5023-US***

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				First Named Inventor	*Jeffrey C. Solomon*
				Art Unit	*2139*
				Examiner Name	*Bansal, Gurtej*
Sheet	10	of	40	Attorney Docket Number	*129980-5023-US*

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	*15/857,519*
				Filing Date	*December 28, 2017*
				First Named Inventor	*Jeffrey C. Solomon*
				Art Unit	*2139*
				Examiner Name	*Bansal, Gurtej*
Sheet	11	of	40	Attorney Docket Number	*129980-5023-US*

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
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Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

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First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

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First Named Inventor	*Jeffrey C. Solomon*
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	347.	Karabatsos, C., "Quad Band Memory (QBM) Technology", Kentron Technologies, Inc., Apr. 2001, pp. 1-5.	
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	349.	MetaRAM, Inc. v. Netlist, Inc. No. 3:09-cv-01309-VRW, MetaRam's Reply to Netlist's Counterclaims, (N.D. Ca. Filed Jun. 3, 2009).	
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	356.	Non-Final Action Closing Prosecution mailed September 1, 2010, for Control No. 95/001,339, filed April 10, 2010, 17 pages.	
	357.	Non-Final Action Closing Prosecution mailed June 21, 2011, for Control No. 95/001,381, filed June 9, 2010, 34 pages.	
	358.	Non-Final Action Closing Prosecution mailed March 12, 2012, for Control No. 95/001,337, filed April 19, 2010, 33 pages.	
	359.	Non-Final Action mailed August 27, 2010, for Control No. 95/000,546, filed May 11, 2010, 16 pages.	
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	362.	Non-Final Action mailed June 15, 2011, for Control No. 95/001,381, filed June 9, 2010, 33 pages.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jeffrey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	17	of	40	Attorney Docket Number	***129980-5023-US***

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	363.	Non-Final Action mailed September 27, 2011, for Control No. 95/001,337, filed April 19, 2010, 19 pages.	
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				Art Unit	*2139*
				Examiner Name	*Bansal, Gurtej*
Sheet	18	of	40	Attorney Docket Number	*129980-5023-US*

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	381.	US District Court Civil Docket; Google Inc. v. Netlist Inc.; 4:08cv04144; Date filed Aug. 29, 2008.	
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	383.	Written Opinion for International Application No. PCT/US2010/040826, date of mailing October 24, 2011 (NETL.048VPC) in 7 pages.	

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US PATENT DOCUMENTS

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	30.	Non-Final Office Action, U.S. Pat. App. 12/761,179, September 13, 2012, 20 pages	
	31.	Non-final office action, U.S. Patent Application No. 13/288,850, October 14, 2013, 24 pages	
	32.	Non-final office action, U.S. Patent Application No. 13/411,344, December 31, 2013, 28 pages	
	33.	Non-final office action, U.S. Patent Application No. 13/473,413, November 17, 2011, 46 pages	
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	39.	Patent Owner's Response to Office Action mailed November 13, 2012 for Reexamination Control Nos.95/000,578; 95/000,579, and 95/001,339, filed January 14, 2013, 96 pages.	
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	44.	Patent Owner's Appeal Brief for Reexamination Control Nos. 95/000,546 and 95/000,577, filed October 2, 2013, 46 pages	
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	47.	Action Closing Prosecution mailed March 27, 2014 for Reexamination Control No. 95/001,758, filed September 14, 2011, 40 pages	
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				First Named Inventor	***Jeffrey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
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	51.	Order Granting Request for Inter Partes Reexamination and Non-Final Office Action mailed December 7,2012, for Control No. 95/002,399, filed September 15, 2012, 89 pages.	
	52.	Non-Final Office Action mailed December 19, 2012, for Control No. 95/001,758, filed September 14, 2011, 36 Pages.	
	53.	Request for Inter Partes Reexamination; Reexam U.S. Patent Application No. 95/001,758, for U.S. Patent No. 7,864,627, filed September 15, 2011, 814 pages (submitted in four parts.)	
	54.	Request for Inter Partes Reexamination; Reexam U.S. Patent Application No. 95/001,381, for U.S. Patent No. 7,532,537, filed June 9, 2010, 247 pages	
	55.	Notice of Allowance, U.S. Pat. App. 12/761,179, July 11, 2013, 37 pages	
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	1.	5388240	02-01-1995	IBM Corporation	
	2.	5463590	10-31-1995	Watanabe	
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	4.	6188641	02-13-2001	Uchida	
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US PATENT APPLICATIONS

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	22.	13/411,344	3/2/2012	Lee	Entire Prosecution History
	23.	13/970,606	8/20/2013	Netlist, Inc.	Entire Prosecution History
	24.	13/971,231	8/20/2013	Netlist, Inc.	Entire Prosecution History
	25.	14/229,844	3/29/2014	Netlist, Inc.	Entire Prosecution History
	26.	14/324,990	7/7/2014	Netlist, Inc.	Entire Prosecution History
	27.	14/337,168	7/21/2014	Netlist, Inc.	Entire Prosecution History

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	28.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
	29.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
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	32.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
	33.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
	34.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3001 to Decision – Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued December 16, 2014	
	35.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3002 to Decision – Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued December 16, 2014	
	36.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3003 to Decision – Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued December 16, 2014	
	37.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3004 to Decision – Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued December 16, 2014	
	38.	McCluskey, Edward J., *Logic Design Principles with Emphasis on Testable Semicustom Circuits*, Prentice Hall, 1986, pp. 104-107 and 119-120.	
	39.	Inter Partes Review Case No. IPR2014-01029, Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on June 24, 2014.	
	40.	Inter Partes Review Case No. IPR2014-01029, Exhibit 1008 to Petition for Inter Partes Review, "Declaration of Charles J. Neuhauser, Ph.D. under 37 C.F.R. § 1.68," filed on June 24, 2014.	
	41.	Inter Partes Review Case No. IPR2014-01029, Supplemental Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on July 23, 2014.	
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	43.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014.	
	44.	Inter Partes Review Case No. IPR2014-01029, Petitioner's Request for Rehearing pursuant to 37 C.F.R. § 42.71, filed on January 15, 2015.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jeffrey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	24	of	40	Attorney Docket Number	***129980-5023-US***

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	45.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Request for Rehearing, Issued on March 3, 2015.	
	46.	Inter Partes Review Case No. IPR2014-01369, Corrected Petition for Inter Partes Review of Claims 1-19 of U.S. Patent No. 8,516,185, filed on September 22, 2014.	
	47.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1008 to Corrected Petition for Inter Partes Review, "Declaration of Dr. Nader Bagherzadeh under 37 C.F.R. § 1.68," filed on September 22, 2014.	
	48.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1013 to Corrected Petition for Inter Partes Review, "Webster's II New College Dictionary," filed on September 22, 2014.	
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	50.	Inter Partes Review Case No. IPR2014-01369, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued March 9, 2014.	
	51.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Smart Storage Systems, Inc.'s Invalidity Contentions, dated June 6, 2014	
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	53.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Diablo Technologies, Inc.'s Invalidity Contentions, dated June 6, 2014.	
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	55.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
	56.	Inter Partes Review of U.S. Patent No. 8,081,536, IPR Case No. IPR2014-00883, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
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				First Named Inventor	***Jeffrey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	25	of	40	Attorney Docket Number	***129980-5023-US***

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Examiner Name	*Bansal, Gurtej*
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US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	6011710	01-04-2000	Wiggers	
	2.	6381140	04-30-2002	Liao, Sheng-Chi	
	3.	6747887	06-08-2004	Halbert et al.	
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	14.	EP 1 816 570 A2	08-08-2007	Rambus, Inc.		
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	18.	Office Action mailed April 2, 2014, for Japanese Patent Application No. 2012-520662 and English translation thereof, 7 pages	
		International Search Report and Written Opinion, PCT/US2011/059209, January 31, 2013	
		Inter Partes Review Case No. 2014-00882, Patent Owner Response, filed May 8, 2015	
	19.	Inter Partes Review Case No. 2014-00882, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015	

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	20.	Inter Partes Review Case No. 2014-00882, Petitioner's Request for Oral Argument, filed July 1, 2015	
	21.	Inter Partes Review Case No. 2014-00882, Patent Owner's Request for Oral Argument, filed July 3, 2015	
	22.	Inter Partes Review Case No. 2014-00882, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015	
	23.	Inter Partes Review Case No. 2014-00882, Record of Oral Hearing, filed November 16, 2015	
	24.	Inter Partes Review Case No. 2014-00882, Final Written Decision 35 USC 318 and 37 CFR 42.73, filed December 14, 2015	
	25.	Inter Partes Review Case No. 2014-00882, Netlist Inc.'s Notice of Appeal, filed February 10, 2016	
	26.	Inter Partes Review Case No. 2014-00882, Exhibit 1022, 'Professor Carl Sechen Deposition Transcript,' filed June,19,2015	
	27.	Inter Partes Review Case No. 2014-00882, Exhibit 1023, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015	
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	45.	Inter Partes Review Case No. 2014-00883, Exhibit 1025, 'Professor Carl Sechen Deposition Transcript,' filed June 19,2015	
	46.	Inter Partes Review Case No. 2014-00883, Exhibit 1026, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015	
	47.	Inter Partes Review Case No. 2014-01011, Patent Owner Response, filed May 8, 2015	
	48.	Inter Partes Review Case No. 2014-01011, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015	
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	76.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Exhibits G.1-G.6 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	*15/857,519*
				Filing Date	*December 28, 2017*
				First Named Inventor	*Jeffrey C. Solomon*
				Art Unit	*2139*
				Examiner Name	*Bansal, Gurtej*
Sheet	30	of	40	Attorney Docket Number	*129980-5023-US*

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	77.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.,* Exhibit H to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	78.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.,* Diablo Technologies, Inc.'s Invalidity Contentions, dated June 6, 2014.	
	79.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.,* Exhibits F-1 to F-5 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	80.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.,* Exhibits G-1 to G-6 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.	
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US PATENT DOCUMENTS

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	1.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Related Matters, filed April 28, 2015	
	2.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner Response to Petition, filed February 22, 2016	
	3.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Objections to Evidence, filed February 29, 2016	
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	6.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER MOTION FOR OBSERVATIONS, filed June 2, 2016	
	7.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016	
	8.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, ORDER Trial Hearing, filed June 8, 2016	
	9.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016	
	10.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Response to Motion for Observations, filed June 10, 2016	
	11.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Response to Netlist's Submission, filed June 13, 2016	
	12.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's Objections to Petitioner's Demonstrative Exhibits, filed June 23, 2016	

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	14.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Updated Exhibit List, filed June 24, 2016	
	15.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016	
	16.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, May 10, 2016 Deposition of Carl Sechen, filed May 19, 2016	
	17.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Demonstrative Exhibits, filed June 24, 2016	
	18.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016	
	19.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2002, "Videotaped Deposition of Srinivasan Jagannathan, Ph.D on February 12, 2016," filed February 22, 2016	
	20.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2003, "Videotaped Deposition of Srinivasan Jagannathan, Ph.D on April 20, 2015," filed February 22, 2016	
	21.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2007, "Deposition of Dr. Srinivasan Jagannathan on May 25, 2016," filed June 2, 2016	
	22.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner Response to Petition, filed February 22, 2016	
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	28.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner's SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016	
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	35.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016	

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US PATENT DOCUMENTS

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	2.	5,313,624	1994-05-17	Harriman	
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	21.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Record of Oral Hearing, dated July 26, 2016	
	22.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Final Written Decision, issued September 28, 2016	
	23.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3001 to Final Decision, issued September 28, 2016	

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	24.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3001-2 to Final Decision, issued September 28, 2016	
	25.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3002 to Final Decision, issued September 28, 2016	
	26.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3003 to Final Decision, issued September 28, 2016	
	27.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3004 to Final Decision, issued September 28, 2016	
	28.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Final Decision, issued September 28, 2016	
	29.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Petition for Inter Partes Review, filed December 30, 2016	
	30.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Exhibit 1003, "Declaration of Harold S. Stone," filed December 30, 2016	
	31.	Inter Partes Review of U.S. Patent No. 8516185, Case No. IPR2017-00577, Petition for Inter Partes Review, filed January 5, 2017	
	32.	Inter Partes Review of U.S. Patent No. 8516185, Case No. IPR2017-00577, Exhibit 1003, "Declaration of Harold S. Stone," filed January 5, 2017	
	33.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Exhibit 1008, Declaration of John J. Kelly Regarding Records of Joint Electron Device Engineering Council (JEDEC), filed December 30, 2016	
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	39.	BUSINESS WIRE, Samsung Announces Mass Production of DDR2; Industry's First 1 GigaByte DDR2 DIMM Offers High Speed and Low Power Necessary for Next-Generation PCs and Servers, March 24, 2003.	
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	42.	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control No. 95/001,758, mailed May 31, 2016, 49 pages.	
	43.	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control Nos. 95/000,546 and 95/000,577, mailed February 25, 2015, 25 pages.	
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	49.	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control No. 95/001,381, mailed January 16, 2014, 24 pages.	
	50.	Requester Request for Rehearing after Board Decision dated 02/18/2014 for Reexamination Control No. 95/001337	
	51.	Patent Owner Response after Board Decision dated 03/18/2014 for Reexamination Control No. 95/001337	

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Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	52.	Affidavit-traversing rejectns or objectns rule 132 dated 03/18/2014 for Reexamination Control No. 95/001337	
	53.	Patent Owner Response after Board Decision dated 03/19/2014 for Reexamination Control No. 95/001337	
	54.	Affidavit-traversing rejectns or objectns rule 132 dated 03/19/2014 for Reexamination Control No. 95/001337	
	55.	Patent Owner Comments on Req for Rehearing timely dated 03/19/2014 for Reexamination Control No. 95/001337	
	56.	Reexam - Affidavit/Decl/Exhibit Filed by 3rd Party dated 04/17/2014 for Reexamination Control No. 95/001337	
	57.	Requester Comments on Patent Owner Response after Board Decision dated 04/17/2014 for Reexamination Control No. 95/001337	
	58.	New Board of Appeals Decision after Board Decision with New Ground of Rejection: New Ground of Rejection dated 06/26/2014 for Reexamination Control No. 95/001337	
	59.	Patent Owner Response after Board Decision dated 07/29/2014 for Reexamination Control No. 95/001337	
	60.	Reexam Petition Decision - Denied dated 08/05/2014 for Reexamination Control No. 95/001337	
	61.	Requester Comments on Patent Owner Response after Board Decision dated 09/05/2014 for Reexamination Control No. 95/001337	
	62.	Reexam - Affidavit/Decl/Exhibit Filed by 3rd Party dated 09/05/2014 for Reexamination Control No. 95/001337	
	63.	Examiner's Determination on Patent Owner Response/Requester Comments after Board Decision dated 06/15/2015 for Reexamination Control No. 95/001337	
	64.	Examiner's Determination on Patent Owner Response/Requester Comments after Board Decision dated 09/11/2015 for Reexamination Control No. 95/001337	
	65.	ffidavit-traversing rejectns or objectns rule 132 dated 10/14/2015 for Reexamination Control No. 95/001337	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

PTO/SB/08a/b(07-09)
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	38	of	40

Complete if Known	
Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	66.	Affidavit-traversing rejectns or objectns rule 132 (26 pages) dated 10/14/2015 for Reexamination Control No. 95/001337	
	67.	Patent Owner Comments on Examiner's Determination after Board Decision dated 10/14/2015 for Reexamination Control No. 95/001337	
	68.	Reexam - Affidavit/Decl/Exhibit Filed by 3rd Party dated 11/13/2015 for Reexamination Control No. 95/001337	
	69.	Reqr Comments on Examiners Determ after Board Decision dated 11/13/2015 for Reexamination Control No. 95/001337	
	70.	Other Reference-Patent/App/Search documents dated 11/22/2016 for Reexamination Control No. 95/001337	
	71.	Petition under Rule 41.3 to Chief Admin Patent Judge dated 11/22/2016 for Reexamination Control No. 95/001337	
	72.	Administrative Remand to Examiner dated 01/19/2017 for Reexamination Control No. 95/001337	
	73.	Reexam Petition Decision - Granted - in-part dated 01/23/2017 for Reexamination Control No. 95/001337	
	74.	Affidavit-traversing rejectns or objectns rule 132 dated 02/22/2017 for Reexamination Control No. 95/001337	
	75.	Patent Owner Comments on Examiner's Determination after Board Decision dated 02/22/2017 for Reexamination Control No. 95/001337	
	76.	Reexam - Affidavit/Decl/Exhibit Filed by 3rd Party dated 03/22/2017 for Reexamination Control No. 95/001337	
	77.	Requester Comments on Patent Owner Response after Board Decision dated 03/22/2017 for Reexamination Control No. 95/001337	
	78.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, DECISION Institution of Inter Partes Review, entered May 15, 2017.	
	79.	Inter Partes Review of U.S. Patent No. 7,532,537, Case No. IPR2017-00667, DECISION Institution of Inter Partes Review, entered July 21, 2017.	
	80.	Inter Partes Review of U.S. Patent No. 7,532,537, Case No. IPR2017-00668, DECISION Institution of Inter Partes Review, entered July 21, 2017.	

EXAMINER **DATE CONSIDERED**

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PTO/SB/08a/b(07-09)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	39	of	40

Complete if Known	
Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	81.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, DECISION Institution of Inter Partes Review, entered July 7, 2017.	
	82.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, SCHEDULING ORDER, entered July 7, 2017.	
	83.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-0549, Patent Owner's Response, filed September 15, 2017.	
	84.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-0549, Exhibit 2001 (DECLARATION OF PROFESSOR CARL SECHEN), filed September 15, 2017.	
	85.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-0549, Exhibit 2001 (DECLARATION OF PROFESSOR CARL SECHEN), filed September 15, 2017.	
	86.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-0549, PETITIONERS' OBJECTIONS TO EVIDENCE, filed September 15, 2017.	
	87.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2003 (DECLARATION OF R. JACOB BAKER, PH.D., P.E.), filed October 25, 2017.	
	88.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2004 (Deposition of HAROLD S. STONE, PH.D.), filed October 25, 2017.	
	89.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2005 (Memory Systems: Cache,DRAM, Disk), filed October 25, 2017.	
	90.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2006 (PC2100 and PC1600 DDR SDRAM Registered DIMM, Design Specification, Revision 1.3, January 2002), filed October 25, 2017.	
	91.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2007 (DRAM CIRCUIT DESIGN: Fundamental and High-Speed Topics), filed October 25, 2017.	
	92.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, PATENT OWNER'S RESPONSE, filed October 25, 2017.	

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PTO/SB/08a/b(07-09)
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US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** *(Use as many sheets as necessary)*				**Complete if Known**	
				Application Number	*15/857,519*
				Filing Date	*December 28, 2017*
				First Named Inventor	*Jeffrey C. Solomon*
				Art Unit	*2139*
				Examiner Name	*Bansal, Gurtej*
Sheet	40	of	40	Attorney Docket Number	*129980-5023-US*

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	93.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, PETITIONERS' OBJECTIONS TO EVIDENCE, filed October 31, 2017.	

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Electronic Acknowledgement Receipt	
EFS ID:	33746963
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	79141
Filer:	Gary Scott Williams/Edith Fuentes
Filer Authorized By:	Gary Scott Williams
Attorney Docket Number:	129980-5023US
Receipt Date:	17-SEP-2018
Filing Date:	28-DEC-2017
Time Stamp:	20:16:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5023US_IDS.pdf	4065403 a415ce9078a4037fb1785336910a3f510114e53c	yes	44

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	4
	Information Disclosure Statement (IDS) Form (SB08)	5	44
Warnings:			
Information:			
	Total Files Size (in bytes):	4065403	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed September 17, 2018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Solomon et al.	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	Bansal, Gurtej
For:	MEMORY MODULE WITH DATA BUFFERING	Attorney Docket No.:	129980-5023-US

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☐ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☐ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

Petitioners
Ex. 1054, p. 206

2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☒ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

Petitioners
Ex. 1054, p. 207

4d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☒ Copies of publications listed on Form PTO-1449 from prior application Serial No. **14/715,486**, filed on **May 18, 2015**; **13/971,231** , filed on **August 20, 2013**; **13/287,081** , filed on **November 1, 2011**; **13/032,470** , filed on **February 22, 2011**; **12/955,711** , filed on **November 29, 2010**; **12/629,827** , filed on **December 2, 2009**; **12/408,652** , filed on **March 20, 2009**; **11/335,875** , filed on **January 19, 2006**; **11/173,175** , filed on **July 1, 2005**; **11/075,395** , filed on **March 7, 2005**, of which this application claims priority under 35 U.S.C. §120, are not being submitted

pursuant to 37 C.F.R. §1.98(d).

7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

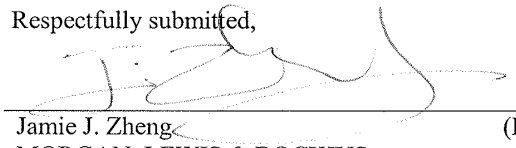
9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: September 17, 2018



51,167

Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

Petitioners
Ex. 1054, p. 209

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 10/11/2018

Morgan Lewis Bockius LLP (PA)-J. Zheng
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER
BANSAL, GURTEJ

ART UNIT	PAPER NUMBER
2139	

DATE MAILED: 10/11/2018

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/857,519	12/28/2017	Jeffrey C. Solomon	129980-5023US	9826

TITLE OF INVENTION: MEMORY MODULE WITH DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	01/11/2019

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Petitioners
Ex. 1054, p. 210

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 10/11/2018
Morgan Lewis Bockius LLP (PA)-J. Zheng
1400 Page Mill Road
Palo Alto, CA 94304

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/857,519	12/28/2017	Jeffrey C. Solomon	129980-5023US	9826

TITLE OF INVENTION: MEMORY MODULE WITH DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	01/11/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
BANSAL, GURTEJ	2139	711-105000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Petitioners
Ex. 1054, p. 211

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/857,519	12/28/2017	Jeffrey C. Solomon	129980-5023US	9826

79141 7590 10/11/2018

Morgan Lewis Bockius LLP (PA)-J. Zheng
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER	
BANSAL, GURTEJ	

ART UNIT	PAPER NUMBER
2139	

DATE MAILED: 10/11/2018

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Petitioners
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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/857,519	Applicant(s) Solomon et al.	
	Examiner GURTEJ BANSAL	Art Unit 2139	AIA Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to Examiner initated interview dated August 17, 2018.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-3 and 8-24 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information , please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 09/17/2018.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☑ Interview Summary (PTO-413), Paper No./Mail Date. August 17, 2018.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

Examiner-Initiated Interview Summary	Application No. 15/857,519	Applicant(s) Solomon et al.	
	Examiner GURTEJ BANSAL	Art Unit 2139	AIA Status No

All participants (applicant, applicant's representative, PTO personnel):

(1) GURTEJ BANSAL. (3) _____.

(2) JAMIE ZHENG (Reg. No. 51,167. (4) _____.

Date of Interview: 17 August 2018.

Type: ☑ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☐ No.
If Yes, brief description: _____.

Issues Discussed ☐ 101 ☑ 112 ☑ 102 ☑ 103 ☑ Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: 1.

Identification of prior art discussed: N/A.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Examiner discussed amendments to the claims to place the application in condition for allowance. Applicant agreed to make such amendments and indicated that a preliminary amendment would be filed in order to amend the claims..

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/857,519	Solomon et al.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

CPC								
Symbol							**Type**	**Version**
G06F	/	13	/	1673			F	2013-01-01
G11C	/	5	/	04			I	2013-01-01
G11C	/	15	/	00			I	2013-01-01
G11C	/	7	/	1072			I	2013-01-01
G06F	/	13	/	4282			I	2013-01-01
G06F	/	13	/	4243			I	2013-01-01
G06F	/	12	/	00			I	2013-01-01
G06F	/	13	/	00			I	2013-01-01

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	27 September 2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	20	9A

U.S. Patent and Trademark Office — Part of Paper No.: 20180927

Petitioners
Ex. 1054, p. 216

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/857,519	Solomon et al.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

INTERNATIONAL CLASSIFICATION					
CLAIMED					
G06F	/	12	/	00	

NON-CLAIMED					
	/		/		

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	27 September 2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	20	9A

Petitioners
Ex. 1054, p. 217

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/857,519	Solomon et al.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	6	10	15	19										
2	2	7	11	16	20										
3	3	8	12	17	21										
	4	10	13	18	22										
	5	11	14	19	23										
	6	12	15	20	24										
	7	9	16												
4	8	13	17												
5	9	14	18												

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	27 September 2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	20	9A

U.S. Patent and Trademark Office — Part of Paper No.: 20180927

Petitioners
Ex. 1054, p. 218

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/857,519	Solomon et al.
	Examiner	Art Unit
	GURTEJ BANSAL	2139

CPC - Searched*		
Symbol	Date	Examiner
G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc.	09/27/2018	GB

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Inventor Search in PE2E	09/27/2018	GB
Text Search in EAST (See Attached)	09/27/2018	GB
NPL Search in Google Scholar (See Attached)	09/27/2018	GB

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc.	09/27/2018	GB

/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	

Petitioners
Ex. 1054, p. 219

Google Scholar | DIMM rank CS strobes

Articles | About 881 results (0.07 sec) | My profile | My library

Any time
Since 2018
Since 2017
Since 2014
Custom range...

Sort by relevance
Sort by date

include patents
include citations

Create alert

Load reduction system and method for **DIMM**-based memory systems [PDF] googleapis.com

C Haywood, G Raghavan, C Xu - US Patent 8,275,936, 2012 - Google Patents

... When the **ranks** are striped across multiple **DIMMs** as described herein, then the **rank** decoding function is performed by the iMB on each **DIMM**, with the iMB performing the same function in parallel but selecting different DRAMs according to its **DIMM** position ...

Cited by 11 Related articles All 3 versions

Memory buffer for buffer-on-board applications

SA Berke - US Patent 8,553,469, 2013 - Google Patents

... Description, **Ranks**, **Rank #**, DCS[ ]_n, Assertion, QACS[ ]_n, QBCS[ ]_n, or 10, 01, assertion ... is that it may encounter difficulties in trying to support two single **rank DIMMs** simultaneously ... mapping information contained in Table 2 to implement two general purpose **DIMM** slots behind ...

Cited by 43 Related articles All 4 versions

Emulation of abstracted **DIMMs** using abstracted DRAMs

MJS Smith, SN Rajan, DT Wang - US Patent 8,438,328, 2013 - Google Patents

One embodiment of the present invention sets forth an abstracted memory subsystem comprising abstracted memories, which each may be configured to present memory-related characteristics onto a memory system interface. The characteristics can be presented on the memory ...

Cited by 71 Related articles All 5 versions

Algorithm for adjustment of DDR write interface timing

P Fleming, P Ostropolski - 2008 - IET

... with two channels of DDR2-667MT/s memory supporting 3 Dual **Rank DIMMs** per channel ... the JEDEC raw card type supported or the number of **DIMMs** on the ... 1. "DDR2 SDRAM Specification", JEDEC Standard – JES 2. "DDR2 SDRAM Registered **DIMM** Design Specification ...

Cited by 5 Related articles All 4 versions

On-die termination snooping for 2T applications in a memory system implementing non-self-terminating ODT schemes

PA Laberge - US Patent 7,516,281, 2009 - Google Patents

... includes a memory controller 2 and two (2) dual-inline-memory-modules 3 (ie, **DIMM**-0, **DIMM**-1). Each ... the WE# and **CS#** signals which are sent by the system controller 2 to the **DIMMs** 3 and ... These signals may be **rank** specific (eg, WE0# and **CS#**0 for **rank**-0, WE#1 and **CS#**1 ...

Cited by 44 Related articles All 4 versions

Increasing the number of **ranks** per channel [PDF] googleapis.com

L Warnes, D Carr, MB Calhoun, AR Mandle - US Patent 8,539,145, 2013 - Google Patents

... or connector, only if the quad **rank DIMM** has the same number of pins as the lower **ranked DIMM** ... All eight **CS** signals are bussed to the two 16 **rank DIMMs** to get the encoding/decoding ... For example, **DIMM** 120 receives a set of four encoded **CS** signals and **DIMM** 130 receives ...

Cited by 6 Related articles All 2 versions

[PDF] ECE/**CS** 757: Advanced Computer Architecture II [PDF] wisc.edu

M Hill, D Wood, G Sohi, J Smith, NE Jerger, M Dubois... - 2017 - ece757.ece.wisc.edu

... Eg 4 16-bit wide DRAMs for a 64-bit parallel access – **DIMM** – Dual Inline Memory Module • Combine **DIMMs** to form multiple **ranks** • Attach a number to **DIMMs** to a memory channel ... Interleave patterns: – **Rank**, Row, Bank, Column, [byte] – Row, **Rank**, Bank, Column, [byte] ...

Related articles All 4 versions

Concurrent status register read

BJ Wolford, JE Sullivan Jr - US Patent 7,593,279, 2009 - Google Patents

... status information from the DRAM devices 100 a and 100 b. The controller 102 issues a MRS command in cycle 1 to both **ranks** (**CS**[0] and **CS**[1] both ... A READ command is issued to **rank** 0 (only **CS**[0] asserted) t MRS cycles later, in cycle 3, and SDRAM device 100 a returns ...

Cited by 7 Related articles All 4 versions

Emulation of abstracted **DIMMS** using abstracted DRAMS

MJS Smith, SN Rajan, DT Wang - US Patent 8,631,193, 2014 - Google Patents

One embodiment of the present invention sets forth an abstracted memory subsystem comprising abstracted memories, which each may be configured to present memory related characteristics onto a memory system interface. The characteristics can be presented on the memory ...

Cited by 28 Related articles All 4 versions

High performance dynamic ram interface

CS Steele, WC Athas Jr, CL Seitz - US Patent 4,937,791, 1990 - Google Patents

... With the present invention, however, the assertion of the RAS and CAS **strobes** is maintained--only the contents of that assertion, ie the column address, changes ... Multi-**rank** partial width memory modules ... Programming of **DIMM** termination resistance values ...

Cited by 104 Related articles All 2 versions

Google
1 2 3 4 5 6 7 8 9 10 >
1 Next

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United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 9826

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/857,519	12/28/2017	711	2139	129980-5023US

APPLICANTS
Netlist, Inc., Irvine, CA;

INVENTORS
Jeffrey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

**** CONTINUING DATA ***************************
This application is a CON of 14/715,486 05/18/2015 PAT 9858215
which is a CON of 13/971,231 08/20/2013 PAT 9037774
which is a CON of 13/287,081 11/01/2011 PAT 8516188
which is a CON of 13/032,470 02/22/2011 PAT 8081536
which is a CON of 12/955,711 11/29/2010 PAT 7916574
which is a CON of 12/629,827 12/02/2009 PAT 7881150
which is a CON of 12/408,652 03/20/2009 PAT 7636274
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7289386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7286436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004
and claims benefit of 60/590,038 07/21/2004

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
02/02/2018

Foreign Priority claimed ❑ Yes ☑ No 35 USC 119(a-d) conditions met ❑ Yes ☑ No Verified and Acknowledged /GURTEJ BANSAL/ Examiner's Signature	❑ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	23	12	1

ADDRESS
Morgan Lewis Bockius LLP (PA)-J. Zheng
1400 Page Mill Road
Palo Alto, CA 94304
UNITED STATES

TITLE
MEMORY MODULE WITH DATA BUFFERING

FILING FEE RECEIVED	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time)

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1880	No._____ for following:	❑ 1.18 Fees (Issue) ❑ Other _____ ❑ Credit

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 40

Complete if Known	
Application Number	15/857,519
Filing Date	December 28, 2017
First Named Inventor	Jeffrey C. Solomon
Art Unit	2139
Examiner Name	Bansal, Gurtej
Attorney Docket Number	129980-5023-US

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number / Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1.	Patent Trial and Appeal Board Decision on Request for Rehearing for Reexamination Control No. 95/001,381, mailed August 13, 2014, 7 pages.	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 2 of 40

Complete if Known	
Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Application Number	15/857,519
Filing Date	December 28, 2017
First Named Inventor	Jeffrey C. Solomon
Art Unit	2139
Examiner Name	Bansal, Gurtej
Attorney Docket Number	129980-5023-US

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Sheet 4 of 40

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Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

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Sheet 5 of 40

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Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

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Sheet 6 of 40

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Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
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Sheet 7 of 40

Complete if Known	
Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

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Examiner Initials *	Cite No. [1]	Document Number / Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Complete if Known	
Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

US PATENT DOCUMENTS

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Sheet 9 of 40

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Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

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Sheet 10 of 40

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Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

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Sheet 11 of 40

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Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

NON PATENT LITERATURE DOCUMENTS

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 13 of 40

Complete if Known	
Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
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	305.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Defendant Inphi Corporation's Answer to Plaintiff's Complaint for Patent Infringement, filed Nov. 12, 2009 in 6 pages. cited by other.	
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	311.	U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Defendant Netlist, Inc.'s Opening Claim Construction Brief, filed Jul. 28, 2009 in 21 pages. cited by other.	
	312.	U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Defendant Netlist, Inc.'s Opposition to Google Inc's Motion for Summary Judgment of Invalidity, filed Jul. 6, 2010 in 13 pages. cited by other.	
	313.	U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Exhibit A To Joint Claim Construction And Prehearing Statement, filed Jun. 12, 2009 in 2 pages. cited by other.	

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Sheet 14 of 40

Complete if Known	
Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

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	314.	U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Exhibit B to Joint Claim Construction and Prehearing Statement, filed Jun. 12, 2009 in 36 pages. cited by other.	
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	316.	U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Netlist, Inc.'s Answer to Complaint and Counterclaims, filed Nov. 18, 2008 in 9 pages. cited by other.	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 15 of 40

Complete if Known	
Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 16 of 40

Complete if Known	
Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

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	357.	Non-Final Action Closing Prosecution mailed June 21, 2011, for Control No. 95/001,381, filed June 9, 2010, 34 pages.	
	358.	Non-Final Action Closing Prosecution mailed March 12, 2012, for Control No. 95/001,337, filed April 19, 2010, 33 pages.	
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				Filing Date	*December 28, 2017*
				First Named Inventor	*Jeffrey C. Solomon*
				Art Unit	*2139*
				Examiner Name	*Bansal, Gurtej*
Sheet	17	of	40	Attorney Docket Number	*129980-5023-US*

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	365.	Non-Final Action mailed October 14, 2011, for Control No. 95/001,339, filed April 30, 2010, 99 pages. (merged with 95/000,578 and 95/000,579)	
	366.	Non-Final Office Action mailed November 16, 2011, for Application No. 95/001,758 filed September 14, 2011, 25 pages.	
	367.	Order Granting Request for Inter Partes Reexamination mailed November 16, 2011, for Application No. 95/001,758, filed September 14, 2011, 13 pages.	
	368.	Order Granting Request for Inter Partes Reexamination mailed August 9, 2010, for Control No. 95/000,546, filed May 11, 2010, 22 pages.	
	369.	Order Granting Request for Inter Partes Reexamination mailed August 27, 2010, for Control No. 95/001,337, filed April 19, 2010, 21 pages.	
	370.	Order Granting Request for Inter Partes Reexamination mailed September 1, 2010, for Control No. 95/001,339, filed April 20, 2010, 14 pages.	
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	372.	Order Granting Request for Inter Partes Reexamination mailed January 14, 2011, for Control No. 95/000,579, filed October 21, 2010, 12 pages.	
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				First Named Inventor	*Jeffrey C. Solomon*
				Art Unit	*2139*
				Examiner Name	*Bansal, Gurtej*
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	383.	Written Opinion for International Application No. PCT/US2010/040826, date of mailing October 24, 2011 (NETL.048VPC) in 7 pages.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	19	of	40

Complete if Known	
Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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	2.	5537584	07-16-1996	Miyai et al.	
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	30.	Non-Final Office Action, U.S. Pat. App. 12/761,179, September 13, 2012, 20 pages	
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First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

Sheet 21 of 40

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Art Unit	*2139*
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US PATENT DOCUMENTS

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	22.	13/411,344	3/2/2012	Lee	Entire Prosecution History
	23.	13/970,606	8/20/2013	Netlist, Inc.	Entire Prosecution History
	24.	13/971,231	8/20/2013	Netlist, Inc.	Entire Prosecution History
	25.	14/229,844	3/29/2014	Netlist, Inc.	Entire Prosecution History
	26.	14/324,990	7/7/2014	Netlist, Inc.	Entire Prosecution History
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	28.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
	29.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
	30.	Inter Partes Review of U.S. Patent No. 8,081,536, IPR Case No. IPR2014-00883, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
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	34.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3001 to Decision – Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued December 16, 2014	
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	46.	Inter Partes Review Case No. IPR2014-01369, Corrected Petition for Inter Partes Review of Claims 1-19 of U.S. Patent No. 8,516,185, filed on September 22, 2014.	
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Sheet	25	of	40

Complete if Known	
Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

NON PATENT LITERATURE DOCUMENTS

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	60.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3003 to Decision – Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued December 16, 2014	
	61.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3004 to Decision – Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued December 16, 2014	
	62.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014.	

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US PATENT DOCUMENTS

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	2.	6381140	04-30-2002	Liao, Sheng-Chi	
	3.	6747887	06-08-2004	Halbert et al.	
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	14.	EP 1 816 570 A2	08-08-2007	Rambus, Inc.		
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	18.	Office Action mailed April 2, 2014, for Japanese Patent Application No. 2012-520662 and English translation thereof, 7 pages	
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		Inter Partes Review Case No. 2014-00882, Patent Owner Response, filed May 8, 2015	
	19.	Inter Partes Review Case No. 2014-00882, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015	

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	20.	Inter Partes Review Case No. 2014-00882, Petitioner's Request for Oral Argument, filed July 1, 2015	
	21.	Inter Partes Review Case No. 2014-00882, Patent Owner's Request for Oral Argument, filed July 3, 2015	
	22.	Inter Partes Review Case No. 2014-00882, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015	
	23.	Inter Partes Review Case No. 2014-00882, Record of Oral Hearing, filed November 16, 2015	
	24.	Inter Partes Review Case No. 2014-00882, Final Written Decision 35 USC 318 and 37 CFR 42.73, filed December 14, 2015	
	25.	Inter Partes Review Case No. 2014-00882, Netlist Inc.'s Notice of Appeal, filed February 10, 2016	
	26.	Inter Partes Review Case No. 2014-00882, Exhibit 1022, 'Professor Carl Sechen Deposition Transcript,' filed June,19,2015	
	27.	Inter Partes Review Case No. 2014-00882, Exhibit 1023, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015	
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Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

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	45.	Inter Partes Review Case No. 2014-00883, Exhibit 1025, 'Professor Carl Sechen Deposition Transcript,' filed June 19,2015	
	46.	Inter Partes Review Case No. 2014-00883, Exhibit 1026, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015	
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	7.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016	
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	11.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Response to Netlist's Submission, filed June 13, 2016	
	12.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's Objections to Petitioner's Demonstrative Exhibits, filed June 23, 2016	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
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Sheet 32 of 40

Complete if Known	
Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	13.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's Demonstrative Exhibits, filed June 24, 2016	
	14.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Updated Exhibit List, filed June 24, 2016	
	15.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016	
	16.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, May 10, 2016 Deposition of Carl Sechen, filed May 19, 2016	
	17.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Demonstrative Exhibits, filed June 24, 2016	
	18.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016	
	19.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2002, "Videotaped Deposition of Srinivasan Jagannathan, Ph.D on February 12, 2016," filed February 22, 2016	
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	21.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2007, "Deposition of Dr. Srinivasan Jagannathan on May 25, 2016," filed June 2, 2016	
	22.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner Response to Petition, filed February 22, 2016	
	23.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Objections to Evidence, filed February 29, 2016	
	24.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Reply, filed May 19, 2016	
	25.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner Request for Oral Argument, filed June 2, 2016	
	26.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, PATENT OWNER MOTION FOR OBSERVATIONS, filed June 2, 2016	

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	27.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016	
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	30.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Response to Patent Owner's Submission, filed June 13, 2016	
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Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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	22.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Final Written Decision, issued September 28, 2016	
	23.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3001 to Final Decision, issued September 28, 2016	

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	24.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3001-2 to Final Decision, issued September 28, 2016	
	25.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3002 to Final Decision, issued September 28, 2016	
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	54.	Affidavit-traversing rejectns or objectns rule 132 dated 03/19/2014 for Reexamination Control No. 95/001337	
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	56.	Reexam - Affidavit/Decl/Exhibit Filed by 3rd Party dated 04/17/2014 for Reexamination Control No. 95/001337	
	57.	Requester Comments on Patent Owner Response after Board Decision dated 04/17/2014 for Reexamination Control No. 95/001337	
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	63.	Examiner's Determination on Patent Owner Response/Requester Comments after Board Decision dated 06/15/2015 for Reexamination Control No. 95/001337	
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	67.	Patent Owner Comments on Examiner's Determination after Board Decision dated 10/14/2015 for Reexamination Control No. 95/001337	
	68.	Reexam - Affidavit/Decl/Exhibit Filed by 3rd Party dated 11/13/2015 for Reexamination Control No. 95/001337	
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	72.	Administrative Remand to Examiner dated 01/19/2017 for Reexamination Control No. 95/001337	
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	74.	Affidavit-traversing rejectns or objectns rule 132 dated 02/22/2017 for Reexamination Control No. 95/001337	
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	80.	Inter Partes Review of U.S. Patent No. 7,532,537, Case No. IPR2017-00668, DECISION Institution of Inter Partes Review, entered July 21, 2017.	

EXAMINER /GURTEJ BANSAL/ DATE CONSIDERED 09/27/2018

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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PTO/SB/08a/b(07-09)
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Use as many sheets as necessary)

Sheet 39 of 40

Complete if Known	
Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	81.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, DECISION Institution of Inter Partes Review, entered July 7, 2017.	
	82.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, SCHEDULING ORDER, entered July 7, 2017.	
	83.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-0549, Patent Owner's Response, filed September 15, 2017.	
	84.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-0549, Exhibit 2001 (DECLARATION OF PROFESSOR CARL SECHEN), filed September 15, 2017.	
	85.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-0549, Exhibit 2001 (DECLARATION OF PROFESSOR CARL SECHEN), filed September 15, 2017.	
	86.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-0549, PETITIONERS' OBJECTIONS TO EVIDENCE, filed September 15, 2017.	
	87.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2003 (DECLARATION OF R. JACOB BAKER, PH.D., P.E.), filed October 25, 2017.	
	88.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2004 (Deposition of HAROLD S. STONE, PH.D.), filed October 25, 2017.	
	89.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2005 (Memory Systems: Cache,DRAM, Disk), filed October 25, 2017.	
	90.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2006 (PC2100 and PC1600 DDR SDRAM Registered DIMM, Design Specification, Revision 1.3, January 2002), filed October 25, 2017.	
	91.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, Exhibit 2007 (DRAM CIRCUIT DESIGN: Fundamental and High-Speed Topics), filed October 25, 2017.	
	92.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, PATENT OWNER'S RESPONSE, filed October 25, 2017.	

EXAMINER /GURTEJ BANSAL/ DATE CONSIDERED 09/27/2018

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Substitute for form 1449/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** *(Use as many sheets as necessary)*				**Complete if Known**	
				Application Number	*15/857,519*
				Filing Date	*December 28, 2017*
				First Named Inventor	*Jeffrey C. Solomon*
				Art Unit	*2139*
				Examiner Name	*Bansal, Gurtej*
Sheet	40	of	40	Attorney Docket Number	*129980-5023-US*

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	93.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-0577, PETITIONERS' OBJECTIONS TO EVIDENCE, filed October 31, 2017.	

EXAMINER /GURTEJ BANSAL/ DATE CONSIDERED 09/27/2018

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	3717	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2011/07/03 21:54
S2	75	365/189.2.ccls.	USPAT	OR	OFF	2011/07/03 21:54
S3	104	365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:27
S4	6392	abstract$3 with (DRAM DIMM memory)	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:40
S5	48	abstracted adj2 (DRAM DIMM memory)	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:40
S6	109	abstracted adj2 (DRAM DIMM memory) or aDRAM	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:42
S7	1	"7515453".pn.	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:00
S8	771	interface same (DDR2 and (DDR or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:17
S9	504	interface with (DDR2 and (DDR or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:18
S10	5	365/189.2.ccls. and (DDR2 and (DDR or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:19
S11	10	365/189.2.ccls. and (DDR and (DDR2 or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:24
S12	1	"20070088995".pn.	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:29
S13	241	CKE with precharge	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:48
S14	0	365/189.2.ccls and CKE with precharge	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:48
S15	111	CKE with precharge same power	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:48
S16	36	silent with alarm with clock	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:54
S17	0	silent with alarm with clock and lark.in.	US-	OR	OFF	2011/07/05

			PGPUB; USPAT			21:54
S18	0	silent with alarm with clock and hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:54
S19	4	alarm with clock and hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:55
S20	0	julia-hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:58
S21	2	julia.in. and hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:59
S22	16	lark.as.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:00
S23	629	precharge same power and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:01
S24	3	precharge same power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:03
S25	1	self with refresh and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:08
S26	3	pre$1charge with power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:09
S27	11	pre$1chargesame power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:09
S28	3	pre$1charge same power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:09
S29	55	pre$1charge same power and CKE and DRAM same DDR same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:22
S30	59	pre$1charge same power and CKE and DRAM same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:25
S31	73	pre$1charge same power and CKE and DDR same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:26
S32	89	refresh same power and CKE and DDR same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:17
S33	10	365/189.2.ccls. and (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:27
S34	54	SPD and (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:29
S35	16	SPD same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:29
S36	0	module with transmit same (pre$1charge	US-	OR	OFF	2011/07/06

		refresh) and CKE	PGPUB; USPAT			00:45
S37	19	memory with transmit same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:45
S38	23	configure same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:48
S39	14	configure with (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:48
S40	1	DDR with DRAM and tCKE with timing with memory	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:52
S41	273	intelligent adj3 (buffer or register)	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:01
S42	9	intelligent adj3 (buffer or register) and pre$charge	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:01
S43	298	SPD same2 (pre$1charge refresh)	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:03
S44	197	SPD same (pre$1charge refresh)	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:03
S45	59	SPD same2 (pre$1charge refresh) and DDR same DRAM	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:03
S46	38	SPD same (pre$1charge refresh) and DDR same DRAM	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:04
S47	3	SPD same (pre$1charge refresh) and DDR same DRAM and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:05
S48	59	SPD same2 (pre$1charge refresh) and DDR same DRAM	US-PGPUB; USPAT	OR	OFF	2011/07/06 10:59
S49	1	SPD same pre$1charge with power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:01
S50	25	SPD same self adj refresh	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:01
S51	0	SPD same self adj refresh and DDR	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:04
S52	2	SPD same self adj refresh and DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:04
S53	22	SPD same self adj refresh same power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:07
S54	2	SPD same self adj refresh and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:24
S55	0	SPD same self adj refresh and tCKE	US-	OR	OFF	2011/07/06

			PGPUB; USPAT			11:26
S56	0	SPD same pre$1charge and tCKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:27
S57	2617837	SPD swith power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:29
S58	578	SPD with power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:29
S59	16	SPD with power same (self adj refresh self$1refresh pre adj charge pre$charge)	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:30
S60	21	SPD same self adj refresh and (pre$1charge or pre adj charge)	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:37
S61	1	"20050246558".pn.	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:41
S62	2	SPD same power with management with mode	US-PGPUB; USPAT	OR	OFF	2011/07/06 12:40
S63	13	365/189.2.ccls. and CS	USPAT	OR	OFF	2011/07/06 12:55
S64	21	365/189.2.ccls. and CS	US-PGPUB; USPAT	OR	OFF	2011/07/06 12:55
S65	171	DIMM same CS	US-PGPUB; USPAT	OR	OFF	2011/07/06 13:00
S66	53	365/189.2.ccls. and (tRP tRCD TWL tRFC timing tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:34
S67	7	365/189.2.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:34
S68	1631	"365".clas. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S69	0	365/189.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S70	446	365/189.$.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S71	36	365/189.$.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR) and DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S72	1	365/189.$.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR) same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:37
S73	3	burst with plurality with DIMM	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:43
S74	0	burst with each with DIMM	US-PGPUB;	OR	OFF	2011/07/06 14:44

			USPAT			
S75	6	burst with multiple with DIMM	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:44
S76	6	burst with multiple with DIMM and read	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:46
S77	5	burst with multiple with DIMM same read	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:47
S78	11	burst with DIMMs same read	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:47
S79	0	365/189.2.ccls. and CKE with (high and low)	USPAT	OR	OFF	2011/07/06 16:19
S80	529	CKE with (high and low)	USPAT	OR	OFF	2011/07/06 16:20
S81	17	CKE with (high and low) and DDR2	USPAT	OR	OFF	2011/07/06 16:20
S82	0	365/189.2.ccls. and CKE with (high and low)	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:20
S83	44	CKE with (high and low) and DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:21
S84	87	CKE with (high and low) same pre$1charge	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:24
S85	0	CKE with (high and low) same pre$1charge same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:24
S86	0	CKE with (high and low) same self adj refresh same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:25
S87	0	CKE with ((high and low) or assert) same self adj refresh same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:25
S88	0	CKE with ((high and low) or assert) same pre$1fetch same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:25
S89	0	CKE with (high or low or assert) same pre$1fetch same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:26
S90	0	CKE with (high or low or assert) same pre$1fetch same2 SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:26
S91	2	CKE with (high or low or assert) same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:26
S92	10	SPD same2 CKE with (high or low or assert)	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:27
S93	1	"20090216936".pn.	US-PGPUB; USPAT	OR	OFF	2012/01/20 18:08
S94	1	"20090216939".pn.	US-	OR	OFF	2012/01/20

			PGPUB; USPAT			18:17
S95	152	buffer with DRAM with protocol	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:25
S96	152	buffer$3 with DRAM with protocol	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:37
S97	572	buffer with $1RAM with protocol	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:38
S98	1	"20030131160".pn.	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:47
S99	1729	buffer with $1RAM with (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:48
S100	626	buffer with DRAM with (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:48
S101	124	buffer with chip with DRAM with (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:51
S102	185	buffer near5 DRAM near5 (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:14
S103	499	buffer with DRAM with type	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:18
S104	51	buffer with DRAM with type with (multiple different tim$3 various)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:19
S105	224	buffer with DRAM with DDR	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:21
S106	3	buffer with DRAM with (timing signal) with adjust	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:32
S107	146	buffer with DRAM with (timing signal) with delay	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:32
S108	31	buffer with DRAM with (timing signal) with DDR$1	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:32
S109	70	buffer with DRAM with (timing signal protocol) and buffer with DDR$1 with (timing signal protocol)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:37
S110	118	buffer with DRAM with (timing signal protocol) and buffer with SDRAM with (timing signal protocol)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:48
S111	36	buffer with DRAM with SDRAM with interface	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:52
S112	48	buffer with DRAM with (SDRAM DDR2 DDR3) with interface	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:52
S113	73	interface with buffer with DRAM with	US-	OR	OFF	2012/01/21

		(DDR$1 SDRAM)	PGPUB; USPAT			02:03
S114	141	interface same buffer with DRAM with (DDR$1 SDRAM)	US-PGPUB; USPAT	OR	OFF	2012/01/21 02:10
S115	2	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/15 14:11
S116	64	DIMM with DRAM and CS with (DIMM DRAM) and buffer with (DIMM DRAM)	US-PGPUB; USPAT	OR	OFF	2013/01/15 14:12
S117	1	"5918229".pn.	US-PGPUB; USPAT	OR	OFF	2013/01/18 14:08
S118	1	"20060184942".pn.	US-PGPUB; USPAT	OR	OFF	2013/01/18 14:35
S119	130	(different multiple distinct) with file adj locking	US-PGPUB; USPAT	OR	OFF	2013/01/18 17:46
S120	0	abstracted with DIMM and DRAM	USPAT	OR	OFF	2013/01/21 13:21
S121	0	abstracted with DIMM	USPAT	OR	OFF	2013/01/21 13:21
S122	2	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 13:21
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S132	83	DIMM with CS and DIMM with DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 21:55
S133	3	("20050038924" | "20080052462" | "6681301").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/01/21 22:03
S134	104	US-20050289292-$.DID. OR US-20050289317-$.DID. OR US-20060002201-$.DID. OR US-6986118-$.DID. OR US-20060010339-$.DID. OR US-6992501-$.DID. OR US-6992950-$.DID. OR US-20060248387-$.DID. OR US-20060041730-$.DID. OR US-7000062-$.DID. OR US-7003618-$.DID. OR US-7003639-$.DID. OR US-20060038597-$.DID. OR US-20060039204-$.DID. OR US-20060039205-$.DID. OR US-20060041711-$.DID. OR US-7007095-$.DID. OR US-7007175-$.DID. OR US-20060044913-$.DID. OR US-20060044909-$.DID. OR US-7010642-$.DID. OR US-7010736-$.DID. OR US-20060049502-$.DID. OR US-20060050574-$.DID. OR US-20060056244-$.DID. OR US-20060062047-$.DID. OR US-20060067141-$.DID. OR US-7024518-$.DID. OR US-7028215-$.DID. OR US-7026708-$.DID. OR US-7028234-$.DID. OR US-20060085616-$.DID. OR US-7033861-$.DID. OR US-7035150-$.DID. OR US-20060087900-$.DID. OR US-20060090054-$.DID. OR US-20060090031-$.DID. OR US-7043599-$.DID. OR US-7045396-$.DID. OR US-7045901-$.DID. OR US-7046538-$.DID. OR US-20060106951-$.DID. OR US-20060112219-$.DID. OR US-20060112214-$.DID. OR US-7053470-$.DID. OR US-7053478-$.DID. OR US-20060117160-$.DID. OR US-20060117152-$.DID. OR US-7058776-$.DID. OR US-662006D-$.DID. OR US-7058863-$.DID. OR US-20060118933-	US-PGPUB; USPAT; USOCR	OR	OFF	2013/01/21 22:15

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S135	140	US-20060198178-$.DID. OR US-20060203590-$.DID. OR US-20060206738-$.DID. OR US-7119428-$.DID. OR US-20060236165-$.DID. OR US-20060236201-$.DID. OR US-20060233012-$.DID. OR US-7127567-$.DID. OR US-7126399-$.DID. OR US-20060248261-$.DID. OR US-7133960-$.DID. OR US-7136978-$.DID. OR US-20060262586-$.DID. OR US-7149145-$.DID. OR US-7149824-$.DID. OR US-20060294295-$.DID. OR US-20070005998-$.DID. OR US-7173863-$.DID. OR US-20070050530-$.DID. OR US-20070058471-$.DID. OR US-20070070669-$.DID. OR US-20070088995-$.DID. OR US-7200021-$.DID. OR US-7205789-$.DID. OR US-7210059-$.DID. OR US-20070091696-$.DID. OR US-7215561-$.DID. OR US-20070106860-$.DID. OR US-7218566-$.DID. OR US-7224595-$.DID. OR US-7228264-$.DID. OR US-7231562-$.DID. OR US-20070136537-$.DID. OR US-	US-PGPUB; USPAT; USOCR	OR	OFF	2013/01/21 22:17

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S136	2185	DRAM with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:35
S137	31	DRAM with DIMM and DIMM with virtual$5	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:35
S138	43	DRAM with DIMM and CS with module	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:39
S139	43	virtual with DIMM and DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:49
S140	57	buffer with CS and DIMM with DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:16
S141	2	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:22
S142	37	virtual$5 near3 DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:22
S143	29	virtual$5 near3 DIMM and DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:22
S144	541	(plurality multiple) with DIMM with single	US-PGPUB; USPAT	OR	ON	2013/01/21 23:25
S145	200	(plurality multiple) near3 DIMM with single	US-PGPUB; USPAT	OR	ON	2013/01/21 23:25
S146	170	(plurality multiple) near3 DIMM with single and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/21 23:25
S147	132	logical with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/21 23:35
S148	112	logical with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/21 23:35
S149	334	(group) with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/22 00:47
S150	55	emulat$3 with DIMM and DRAM	US-	OR	ON	2013/01/22

			PGPUB; USPAT			00:52
S151	71	virtual with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/22 09:39
S152	10	(plurality multiple) with virtual with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/22 09:40
S153	47	(plurality multiple) with (virtual logical emulat$3) with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/22 09:40
S154	1	"7133960".pn.	US-PGPUB; USPAT	OR	ON	2013/01/22 09:42
S155	17	rank with (appear$3) with DIMM	USPAT	OR	OFF	2013/01/30 13:21
S159	180	(virtual logical abstract$3) with DIMM	US-PGPUB; USPAT	OR	ON	2013/02/18 23:49
S160	22	(virtual logical abstract$3) adj DIMM	US-PGPUB; USPAT	OR	ON	2013/02/18 23:49
S161	344	(virtual logical abstract$3) adj RAM	US-PGPUB; USPAT	OR	ON	2013/02/19 00:01
S162	98	(virtual logical abstract$3) adj DRAM	US-PGPUB; USPAT	OR	ON	2013/02/19 00:01
S168	2	"201100052062".pn. "5910010".pn. "5222014".pn.	US-PGPUB; USPAT	OR	OFF	2013/04/16 23:55
S169	18	US-20030110339-$.DID. OR US-20030174569-$.DID. OR US-20040049624-$.DID. OR US-20050044302-$.DID. OR US-20060277355-$.DID. OR US-20080130364-$.DID. OR US-20080282084-$.DID. OR US-20080282341-$.DID. OR US-20090049266-$.DID. OR US-20090070520-$.DID. OR US-20090063865-$.DID. OR US-20090063896-$.DID. OR US-20090089480-$.DID. OR US-6047361-$.DID. OR WO-199725674-$.DID. OR KR-2005120344-$.DID. OR US-3201318-$.DID. OR KR-1020087019582-$.DID. OR US-1201321-$.DID. OR US-6201324-$.DID. OR US-4201331-$.DID. OR US-9201340-$.DID. OR US-182013D-$.DID.	US-PGPUB; USPAT	OR	OFF	2013/07/24 15:48
S170	105	(virtual logical abstract$3) adj DRAM	US-PGPUB; USPAT	OR	ON	2013/07/24 15:59
S171	60	emulat$3 with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/07/24 15:59
S172	4337	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/07/24 16:02

S173	3	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/07/24 16:04
S178	1054	buffer with data with CS	US-PGPUB; USPAT	OR	OFF	2017/04/26 15:45
S179	1637	buffer with DIMM	US-PGPUB; USPAT	OR	OFF	2017/04/26 15:49
S180	100	buffer and fan$4 with (rank dimm)	US-PGPUB; USPAT	OR	OFF	2017/04/26 16:14
S181	249	buffer same parallel with (rank dimm)	US-PGPUB; USPAT	OR	OFF	2017/04/26 16:26
S182	112	buffer same parallel with (ranks dimms)	US-PGPUB; USPAT	OR	OFF	2017/04/26 16:26
S183	60	daisy with chain with DIMM same buffer	US-PGPUB; USPAT	OR	OFF	2017/04/27 00:11
S184	9041	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	US-PGPUB; USPAT	OR	OFF	2017/04/30 15:23
S189	1	bust with rank$1 with select$3	US-PGPUB; USPAT	OR	OFF	2017/08/17 00:07
S190	38	burst with rank$1 with select$3	US-PGPUB; USPAT	OR	OFF	2017/08/17 00:07
S191	38	burst with rank with select$3	US-PGPUB; USPAT	OR	ON	2017/08/17 08:16
S192	141	burst same rank$1 same select$3	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:16
S193	113	buffer same parallel with (ranks dimms)	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:34
S194	5288	G06F13/1673.cpc. G011C7/1072.cpc. G011C15/00.cpc. G06F13/4282.cpc. G06F13/4243.cpc.	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:36
S195	299	DIMM same CS	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:46
S196	322	DIMM same (CS chip$1select)	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:46
S197	83	DIMM with DRAM and CS with (DIMM) and buffer with (DIMM DRAM)	US-PGPUB; USPAT	OR	OFF	2017/08/17 09:29
S198	195	DIMM with rank with select$3	US-PGPUB; USPAT	OR	OFF	2017/08/17 10:08
S200	35	DIMM same rank same burst	US-PGPUB; USPAT	OR	OFF	2017/08/17 15:23

S204	69	ranks same dimm same strobe	US-PGPUB; USPAT	OR	OFF	2018/09/27 12:55
S205	154	ranks same dimm same strobe	US-PGPUB; USPAT	OR	ON	2018/09/27 12:55
S206	150	(virtual logical abstract$3) adj DRAM	US-PGPUB; USPAT	OR	ON	2018/09/27 13:51
S207	355	DIMM same (CS chip$1select)	US-PGPUB; USPAT	OR	OFF	2018/09/27 14:01
S208	153	greater with CAS with latency	US-PGPUB; USPAT	OR	OFF	2018/09/27 20:45
S209	1	greater with CAS with latency with actual	US-PGPUB; USPAT	OR	OFF	2018/09/27 20:46
S210	375	(great$3 increas$3) with CAS with latency	US-PGPUB; USPAT	OR	OFF	2018/09/27 21:32
S211	7	(great$3 increas$3) with CAS with latency same DIMM	US-PGPUB; USPAT	OR	OFF	2018/09/27 21:32
S212	11706	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc.	US-PGPUB; USPAT	OR	OFF	2018/09/27 21:56

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4948	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc.	USPAT	OR	OFF	2018/09/27 23:32
L2	0	strobes.clm. and ranks.clm. and bits.clm.	USPAT	OR	OFF	2018/09/27 23:33
L3	0	L1 and L2	USPAT	OR	OFF	2018/09/27 23:33
S156	4194	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/01/30 13:35
S157	1321	emulated.clm.	USPAT	OR	OFF	2013/01/30 13:45
S158	3	S156 and S157	USPAT	OR	OFF	2013/01/30 13:45
S163	4205	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/02/19 00:04
S164	1330	emulated.clm.	USPAT	OR	OFF	2013/02/19 00:04
S165	4205	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/02/19 00:04
S166	1330	emulated.clm.	USPAT	OR	OFF	2013/02/19 00:04
S167	3	S165 and S166	USPAT	OR	OFF	2013/02/19 00:04
S174	4343	711/5.ccls. 711/105.ccls. 711/167.ccls.	USPAT	OR	OFF	2013/07/24

		365/189.2.ccls.				16:04
S175	4343	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/07/24 16:06
S176	1399	emulated.clm.	USPAT	OR	OFF	2013/07/24 16:06
S177	4	S175 and S176	USPAT	OR	OFF	2013/07/24 16:06
S185	4964	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	USPAT	OR	OFF	2017/04/30 15:24
S186	6228	data.clm. adj path.clm.	USPAT	OR	OFF	2017/04/30 15:28
S187	120	S185 and S186	USPAT	OR	OFF	2017/04/30 15:28
S188	8	S185 and S186 and rank.clm.	USPAT	OR	OFF	2017/04/30 15:28
S199	5127	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	USPAT	OR	OFF	2017/08/17 10:17
S201	5127	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	USPAT	OR	OFF	2017/08/17 15:22
S202	0	S201 and buffer.clm. and rank.clm. and burst.clm.	USPAT	OR	OFF	2017/08/17 15:22
S203	8	DIMM with rank with selection	USPAT	OR	OFF	2017/08/17 15:23

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15/857,519	12/28/2017	Jeffrey C. Solomon	129980-5023US

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Morgan Lewis Bockius LLP (PA)-J. Zheng
1400 Page Mill Road
Palo Alto, CA 94304

PUBLICATION NOTICE

OC000000103156196

Title:MEMORY MODULE WITH DATA BUFFERING

Publication No.US-2018-0300267-A1
Publication Date:10/18/2018

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Document Description: Application Data Sheet to update/correct info
Doc Code: ADS.CORR

CORRECTED ADS FORM

Application Number	15857519
Title of Invention	MEMORY MODULE WITH DATA BUFFERING

Inventor Information

****If no data is shown, no data has been corrected****

	Data of Record	Updated Data
Order Number	1	
Name	~~Jeffrey C. Solomon~~	Jefferey C. Solomon
Residence Information		
Residency	us-residency	
City	Irvine	
State	CA	
Country of Residence	US	
Mailing Address of Inventor		
Address 1	16 Silver Fir	
Address 2		
City,State/Province, Postal Code	Irvine CA 92604	
Country	US	

Corrected ADS 1.0

Document Description: Application Data Sheet to update/correct info
Doc Code: ADS.CORR

	Data of Record	Updated Data
Order Number	2	
Name	Jayesh R. Bhakta	
Residence Information		
Residency	us-residency	
City	Cerritos	
State	CA	
Country of Residence	US	
Mailing Address of Inventor		
Address 1	12220 Rose Street	
Address 2		
City,State/Province, Postal Code	Cerritos CA 90703	
Country	US	

Application Information

	Data of Record	Updated Data
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	
Attorney Docket Number	129980-5023US	
Entity Type	Regular Undiscounted	

Domestic Benefit/National Stage Information

****If no data is shown, no data has been corrected****

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121,365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S. C. 119(e) or 120, and 37 CFR 1.78(a).

Corrected ADS 1.0

Document Description: Application Data Sheet to update/correct info
Doc Code: ADS.CORR

		Data of Record	Updated Data
	Prior Application Status		
	Application Number		
	Continuity Type		
	Prior Application Number		
	Filing Date (YYYY-MM-DD)		
	Patent Number		
	Issue Date (YYYY-MM-DD)		

Foreign Priority Information

****If no data is shown, no data has been corrected****

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

		Data of Record	Updated Data
	Application Number		
	Country		
	Filing Date		
	Access Code		

Applicant Information

****If no data is shown, no data has been corrected****
Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

	Data of Record	Updated Data
Applicant Type		

Corrected ADS 1.0

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is		
Name of the Deceased or Legally Incapacitated Inventor		
Applicant is an Organization		
Name		
Organization Name		
Address 1		
Address 2		
City,State/Province,Postal Code		
Country		
Phone Number		
Fax Number		
Email Address		

Assignee Information including Non-Applicant Assignee Information

****If no data is shown, no data has been corrected****
Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office

	Data of Record	Updated Data
Order		
Applicant is an Organization		
Name		

Organization Name		
Mailing Address		
Address 1		
Address 2		
City,State/Province,Postal Code		
Country		
Phone Number		
Fax Number		
Email Address		

Signature

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b).

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Jamie J. Zheng/	Registration Number	51,167
First Name	Jamie J.	Last Name	Zheng

Electronic Patent Application Fee Transmittal

Application Number:	15857519
Filing Date:	28-Dec-2017
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	
Filer:	Jamie Jie Zheng/Theresa Asmus
Attorney Docket Number:	129980-5023US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
PROCESSING FEE, EXCEPT PROV. APPLS.	1830	1	140	140
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**140**

Electronic Acknowledgement Receipt	
EFS ID:	34269783
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	
Customer Number:	79141
Filer:	Jamie Jie Zheng/Theresa Asmus
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023US
Receipt Date:	09-NOV-2018
Filing Date:	28-DEC-2017
Time Stamp:	19:51:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$140
RAM confirmation Number	111318INTEFSW00006155500310
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet to update/ correct info	CorrectedADS.pdf	72565 1e2f63799851d7af03bd3bec05559bd7129e4a50	no	5
Warnings:					
Information:					
2	Request under Rule 48 correcting inventorship	129980-5023US_Request-148fwDec_efile.pdf	222777 0be4a394126d445bd22bbaf52709a3a3194e4232	no	2
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30635 65906496dbe8d087e3f73029816559e11845511e	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	325977		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed November 9, 2018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Netlist, Inc.	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	BANSAL, Gurtej
For:	*MEMORY MODULE WITH DATA BUFFERING*	Attorney Docket No.:	129980-5023-US

REQUEST FOR CORRECTION OF NAME UNDER 37 C.F.R. § 1.48(f)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants respectfully request that inventorship be corrected in pending U.S. Patent Application No. 15/857,519 to correct inventor Jefferey C. Solomon's name.

Pursuant to Section 1.48(f), the following are enclosed:

- a Supplemental Application Data Sheet;
- Declaration executed by inventor Jefferey C. Solomon.; and
- processing fee set forth in 37 CFR 1.17(i).

The Commissioner has been authorized through the electronic filing system to charge any additional fees or credit any overpayment associated with this communication to Deposit Account No. 50-0310 (order no. 129980-5023-US).

Respectfully submitted,

Date: November 9, 2018

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

DB2/ 35379201.1

Customer No. 79141
Attorney Docket No.: NETL.018P2C7

Modified PTO/AIA/01 (06-12)

DECLARATION FOR UTILITY OR DESIGN APPLICATION

Title of Invention	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE

As a below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 13/971,231 filed on August 20, 2013.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Note to Inventor: 37 C.F.R. § 1.63(c) states: "A person may not execute an oath or declaration for an application unless that person has reviewed and understands the contents of the application, including the claims, and is aware of the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56."

First Inventor (Legal Name): Jefferey C. Solomon

Signature: Jeffrey C. Solomon Date (Optional): 10-14-2013

Second Inventor (Legal Name): Jayesh R. Bhakta

Signature: Jayesh Bhakta Date (Optional): 10-14-2013

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/857,519	12/28/2017	Jefferey C. Solomon	129980-5023US

CONFIRMATION NO. 9826

79141
Morgan Lewis Bockius LLP (PA)-J. Zheng
1400 Page Mill Road
Palo Alto, CA 94304

37 CFR 1.48(f)
ACKNOWLEDGEMENT LETTER

OC000000103788393

Date Mailed: 11/16/2018

NOTICE OF ACCEPTANCE OF REQUEST UNDER 37 CFR 1.48(f)

This is in response to the applicant's request under 37 CFR 1.48(f) submitted on 11/09/2018.

The request under 37 CFR 1.48(f) to correct the inventorship, to correct or update the name of an inventor, or to correct the order of names of joint inventors is accepted.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/hsarwari/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/857,519	12/28/2017	2139	1880	129980-5023US	12	1

CONFIRMATION NO. 9826

UPDATED FILING RECEIPT

79141
Morgan Lewis Bockius LLP (PA)-J. Zheng
1400 Page Mill Road
Palo Alto, CA 94304

OC000000103788391

Date Mailed: 11/16/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jefferey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 14/715,486 05/18/2015 PAT 9858215
which is a CON of 13/971,231 08/20/2013 PAT 9037774
which is a CON of 13/287,081 11/01/2011 PAT 8516188
which is a CON of 13/032,470 02/22/2011 PAT 8081536
which is a CON of 12/955,711 11/29/2010 PAT 7916574
which is a CON of 12/629,827 12/02/2009 PAT 7881150
which is a CON of 12/408,652 03/20/2009 PAT 7636274
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7289386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7286436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004
and claims benefit of 60/590,038 07/21/2004

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

MEMORY MODULE WITH DATA BUFFERING

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor

community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Address to:
Mail Stop RCE
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Electronically filed	January 11, 2019
Application Number	15/857,519
Filing Date	December 28, 2017
First Named Inventor	Jefferey C. Solomon
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket No.	129980-5023-US

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application. Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application.

1. Submission required under 37 C.F.R. § 1.114

NOTE: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

a. ☐ Previously submitted. If a final Office Action is outstanding, any amendments filed after the final Office Action may be considered as a submission.
   - i. ☐ Request for non-entry of amendment: Please **do not** entered the amendment submitted on _____
   - ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed _____
   - iii. ☐ Other _____

b. ☒ Enclosed
   - i. ☒ Amendment/Reply
   - ii. ☐ Affidavit(s)/Declaration(s)
   - iii. ☒ Information Disclosure Statement (IDS)
   - iv. ☐ Other _____

2. Miscellaneous

a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R. § 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 C.F.R. § 1.17(i) required)

b. ☐ Other _____

3. Fees — The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.

a. ☒ The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023).
   - i. ☒ (1st request) RCE fee required under 37 C.F.R. § 1.17(e)(1), estimated to be **$1300 (large entity)** or $650 (small entity)
   - ii. ☐ (2nd or subsequent request) RCE fee required under 37 C.F.R. § 1.17(e)(2), estimated to be $1900 (large entity) or $950 (small entity)
   - iii. ☐ Extension of time fee required under 37 C.F.R. §§ 1.136 and 1.17, estimated to be $ for a month(s) extension, the request for which is being made herewith
   - iv. ☐ Other _____

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print/Type)	Jamie J. Zheng	*Registration No. (Attorney/Agent)*	51,167
Signature		*Date*	January 11, 2019

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or by facsimile transmitted to fax no. 1-703- to the U.S. Patent and Trademark Office on the date indicated below.

Name (Print/Type)		*Registration No. (Attorney/Agent)*	
Signature		*Date*	1/11/2019

Electronically filed January 11, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Netlist, Inc.	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	BANSAL, Gurtej
For:	*MEMORY MODULE WITH DATA BUFFERING*	Attorney Docket No.:	129980-5023-US
		Date:	January 11, 2019

AMENDMENT AND REQUEST FOR CONTINUED EXAMINATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

In response to the Notice of Allowance dated October 11, 2018, Applicant files herewith an Amendment and a Request for Continued Examination.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US).

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a data bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output first data and first data strobes and the second memory command to cause the memory module to receive or output second data and second data strobes the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks, each rank of the plurality of ranks having a same bit width as the memory module, wherein the plurality of ranks include a first rank selected to receive or output the first data and first data strobes in response to the first memory command, and a second rank ~~is~~ selected to receive or output the second data and second data strobes in response to the second memory command;

a data buffer coupled between ~~the~~ at least one first memory integrated circuit in the first rank and the data bus, and between at least one second memory integrated circuit in the second rank and the data bus; and

logic coupled to the data buffer and configured to respond to the first memory command by providing first control signals to the data buffer to enable communication of respective bits of the first data and respective data strobes of the first data strobes between the ~~at least one first memory integrated circuit~~ memory devices and the memory controller through the data buffer, wherein the logic is further configured to respond to the second memory command by providing second control signals to the data buffer to enable communication of respective bits of the second data and respective strobes of the second data strobes between the memory devices ~~at least one second memory integrated circuit~~ and the memory controller through the data buffer, the first data

including a first data burst and the second data including a second data burst following the first data burst on the data bus;

wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits; and

wherein the first data and the first data strobes, and the second data and the second data strobes, are communicated between the memory devices and the memory controller at a predetermined data rate.

2. (Previously Presented) The memory module of claim 1, wherein each of the plurality memory integrated circuits has a corresponding load, and wherein the data buffer is configured to isolate the loads of both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory controller.

3. (Currently Amended) The memory module of claim 1, wherein the logic is coupled to the printed circuit board and is further configured to respond to the first read/write memory command by outputting a first set of command signals and to respond to the second read/write command by outputting a second set of command signals, the first read/write memory command ~~set of command signals~~ including a first set of input chip select signals corresponding to respective ~~ones~~ ranks of the plurality of ranks and the second ~~set of command signals~~ read/write memory command including a second set of input chip select signals corresponding to respective ~~ones~~ ranks of the plurality of ranks, the first set of command signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals, the second set of command signals including a second plurality of registered chip select signals corresponding to respective ones of the second plurality of input chip select signals, the first set of registered chip select signals including a first registered chip select signal having an active signal value while the rest of the first set of registered chip select signals each has a non-active signal value, the second set of registered chip select signals including a second registered chip select signal having an active signal value while the rest of the second set of registered chip select signals each has a non-active signal value, and wherein the first rank is configured to receive the first registered chip select signal and the second rank is configured to receive the second registered chip select signal.

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Original) The memory module of claim 1, further comprising an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits.

9. (Currently Amended) The memory module of claim 1, wherein the memory module is further coupled to the memory controller using an on-die-termination (ODT) bus, wherein each of the plurality of memory integrated circuits ~~devices~~ includes an ODT circuit, the memory module further comprising a termination circuit external to any of the plurality of memory integrated circuits~~devices~~, wherein the termination circuit is coupled to the ODT bus and to the ODT circuit of at least one of the plurality of memory integrated circuits~~devices~~, wherein the termination circuit is configured to provide external termination of at least one of the plurality of memory integrated circuits ~~devices~~ in response to an ODT signal on the ODT bus, and wherein the ODT circuit of the at least one of the plurality of memory integrated circuits ~~devices~~ is disabled.

10. (Currently Amended) The memory module of claim 1, wherein the data buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring at the predetermined data rate the respective bits of the first data and respective data strobes of the first data strobes, or the respective bits of the second data and respective data strobes of the second data strobes, through the data buffer.

11. (Original) The memory module of claim 1, wherein the logic is further configured to determine the overall CAS latency.

12. (Currently Amended) The memory module of claim 1, wherein the logic is further configured to enable communication of the first data and the first data strobes or the second data

and the second data strobes at the predetermined data rate between the memory module and the memory controller in accordance with the overall CAS latency.

13. (Previously Presented) The memory module of claim 1, wherein each of the plurality of ranks is 72-bit wide, wherein the plurality of memory integrated circuits include 36 4-bit wide memory integrated circuits configured in 18 pairs, wherein the at least one first memory integrated circuit includes a first pair of memory integrated circuits configured to communicate a respective byte of the first data, and wherein the at least one second memory integrated circuit includes a second pair of memory integrated circuits configured to communicate a respective byte of the second data.

14. (Previously Presented) The memory module of claim 13, wherein the first pair of memory integrated circuits are configured to simulate an 8-bit wide memory device, and the second pair of memory integrated circuits are configured to simulate another 8-bit wide memory device.

15. (Previously Presented) The memory module of claim 13, further comprising an SPD device programmed with data to characterize each pair of memory integrated circuits as a virtual 8-bit wide memory device.

16. (Previously Presented) The memory module of claim 1, wherein the data buffer includes switches each coupled between a respective data or strobe pin of the at least one first memory device and a corresponding signal line in the data bus, and between a respective data or strobe pin of the at least one second memory device and the corresponding signal line in the data bus, and wherein the first control signals include control signals for enabling the switches and the second control signals include control signals for enabling the switches.

17. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to read/write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to respond to a first read/write memory command by outputting a first set of command signals, the first read/write memory command including a first plurality of input chip select signals, the first set of command signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals, the first plurality of registered chip select signals including a first registered chip select signal having an active signal value while the rest of the first plurality of registered chip select signals each has a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of ranks, each rank of the plurality of ranks having a same data width as the memory module, wherein the plurality of ranks correspond to, and are configured to receive, respective ones of the first plurality of registered chip select signals, wherein a first rank in the plurality of ranks receiving the first chip select signal is selected to receive or output a first burst of data and a first burst of data strobes in response to the first read/write command~~, wherein each of the memory devices is 4 bits wide, and wherein each of the plurality of ranks is 72 bits wide and include 18 memory devices configured in pairs~~;

at least one buffer coupled between data and strobe signal lines in the memory bus and corresponding data and strobe pins of the memory devices in each of the plurality of ranks, the at least one buffer including a set of signal paths each between a respective data or strobe signal line in the memory bus and a corresponding data or strobe pin of each of a set of memory devices, the set of memory devices including one memory device in each of the plurality of ranks; and

wherein the logic is further configured to, in response to the first read/write memory command, output control signals to the at least one buffer to enable the set of signal paths so as to allow communication of the first burst of data and the first burst of data strobes between the ~~first rank~~ memory devices and the memory controller through the at least one buffer; and

wherein the memory module has an overall CAS latency and the set of signal paths are enabled in accordance with the overall CAS latency ~~greater than an actual operational CAS latency of each of the memory devices~~.

18. (Currently Amended) The memory module of claim 17, wherein each of the ~~4-bit-wide~~ memory devices has a corresponding load, and the at least one buffer is configured to isolate the loads of the memory devices from the memory bus.

19. (Currently Amended) The memory module of claim 17, wherein the first burst of data includes ~~include~~ a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein the set of signal paths are enabled during a time period when the set of consecutively transmitted data bits are successively communicated through the at least one buffer.

20. (Currently Amended) The memory module of claim 17, wherein the logic is further configured to respond to a second read/write memory command by outputting a second set of command signals, the second set of command signals including a second plurality of chip select signals corresponding to respective ranks of the plurality of ranks, the second plurality of chip select signals including a second chip select signal having the active signal value while the rest of the second plurality of chip select signals each has a non-active signal value, wherein a second rank different from the first rank is configured to receive the second chip select signal and is selected to output or receive a second burst of data and a second burst of data strobes in response to the second read/write command, wherein the logic is further configured to, in response to the second read/write memory command, output control signals to the at least one buffer to enable the set of signal paths so as to allow communication of the second burst of data and the second burst of strobes between the ~~second rank~~ memory devices and the memory controller through the at least one buffer, the second burst of data following the first burst of data on the memory bus.

21. (Currently Amended) The memory module of claim 17, wherein each of the memory devices is 4-bits wide, and wherein each of the plurality of ranks is 72-bits wide and include 18 memory devices configured in pairs, and wherein each pair of 4-bit-wide memory devices are configured to simulate an 8-bit-wide memory device.

22. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to read/write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to respond to a read/write memory command by outputting a set of command signals, the read/write memory command including a plurality of input chip select signals, the set of command signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals, the plurality of registered chip select signals including one registered chip select signal having an active signal value while the rest of the plurality of registered chip select signals each has a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of ranks each having a same data width as the memory module, wherein the plurality of ranks correspond to, and are configured to receive, respective ones of the plurality of registered chip select signals, wherein a first rank receiving the registered chip select signal having the active signal value is selected to receive or output a first burst of data and a first burst of data strobes in response to the read/write command~~, wherein each of the memory devices is 4 bits wide, and have a set of data pins and one or more data strobe pins, and wherein each of the plurality of ranks is 72 bits wide and include 18 memory devices configured in pairs~~;

a plurality of configurable circuit components ~~switches~~ each coupled between a respective data or strobe signal line in the memory bus and a corresponding data or strobe pin in each of the plurality of ranks; and

wherein the logic is further configured to, in response to the read/write memory command, output control signals for configuring the plurality of configurable circuit components ~~enabling the switches~~ to allow communication of the first burst of data and the first burst of data strobes between the ~~first rank~~ memory devices and the memory controller; and

wherein the memory module has an overall CAS latency and the set of configurable circuit components are configured to allow communication of the first burst of data in accordance with the overall CAS latency ~~greater than an actual operational CAS latency of each of the memory devices~~.

23. (Currently Amended) The memory module of claim 22, wherein the first burst of data ~~include~~ includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein the plurality of configurable circuit components are enabled during a

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time period when the set of consecutively transmitted data bits are successively communicated through the plurality of configurable circuit components.

24. (Currently Amended) The memory module of claim 22, wherein the logic is further configured to respond to a subsequent read/write memory command by outputting subsequent set of command signals, the subsequent set of command signals including a subsequent plurality of chip select signals corresponding to respective ranks of the plurality of ranks, the subsequent plurality of chip select signals including one subsequent chip select signal having the active signal value while the rest of the subsequent plurality of chip select signals each has a non-active signal value, wherein a second rank different from the first rank is configured to receive the subsequent chip select signal having the active signal value and is selected to output or receive a second burst of data and a second burst of data strobes in response to the subsequent read/write command, wherein the logic is further configured to, in response to the second read/write memory command, output control signals for configuring the plurality of configurable circuit components ~~enabling the switches~~ to allow communication of the second burst of data and the second burst of data strobes between the ~~second rank~~ memory devices and the memory controller.

25. (New) The memory module of claim 17, wherein the overall CAS latency has at least one more clock cycle than an actual operational CAS latency of each of the memory devices.

26. (New) The memory module of claim 17, wherein the data buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring respective bits of the first data and respective data strobes of the first data strobes at a certain rate through the data buffer.

27. (New) The memory module of claim 17, wherein the logic is further configured to determine the overall CAS latency.

28. (New) The memory module of claim 17, wherein the first data and the first data strobes are communicated between the memory devices and the memory controller at a predetermined data rate.

29. (New) The memory module of claim 20, wherein the set of signal paths are disabled after communication of the first burst of data and first burst of data strobes through the at least one buffer and before communication of the second burst of data and the second burst of data strobes through the at least one buffer.

30. (New) The memory module of claim 22, wherein the overall CAS latency has at least one more clock cycle than an actual operational CAS latency of each of the memory devices.

31. (New) The memory module of claim 22, wherein the first data and the first data strobes are communicated between the memory devices and the memory controller at a predetermined data rate.

32. (New) The memory module of claim 24, wherein the plurality of configurable circuit components are disabled after communication of the first burst of data and first burst of data strobes through the at least one buffer and before communication of the second burst of data and the second burst of data strobes through the at least one buffer.

REMARKS

This Amendment is in response to the Notice of Allowance dated October 11, 2018.

Claims 1, 3, 9-10, 12, 17- 24 are amended, and new claims 25-32 are presented. No new matter is added.

Support for the amendments can be found in at least paragraph [0057]-[0058], [0107] of the Specification and FIGS. 6A and 6B.

Filed herewith is an Information Disclosure Statement.

CONCLUDING REMARKS

In light of the above amendments and remarks, the Applicant respectfully requests that the amendments be entered. The Examiner is invited to call the undersigned attorney at (650) 843-4000, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: January 11, 2019

/Jamie J. Zheng/ 51,167

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Electronic Patent Application Fee Transmittal

Application Number:	15857519
Filing Date:	28-Dec-2017
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Filer:	Jamie Jie Zheng/S. Olivier
Attorney Docket Number:	129980-5023US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	8	100	800
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
RCE- 1ST REQUEST	1801	1	1300	1300
		Total in USD ($)		**2100**

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EFS ID:	34838815
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980_5023US_RCE_AMEND.pdf	266457 a77d443120c5627c093f0b6a908265bc5a06659b	yes	12

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Request for Continued Examination (RCE)	1	1
Response After Final Action	2	2
Claims	3	11
Applicant Arguments/Remarks Made in an Amendment	12	12

Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32213 f0b697fad344716aa32a1fec3069b5e700d43e79	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	298670		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 11, 2019*	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	1	of	4	Attorney Docket Number	***129980-5023-US***

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.[1]	Document Number Number - Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code[3] – Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's reply to Patent Owner's Response, filed December 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Deposition Transcript of Carl Sechen, filed December 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Supplemental Declaration of Harold S. Stone, filed December 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Xilinx CoolRunner XPLA3 CPLD product specification (2000), filed December 15, 201
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBIT 2003, 'Synchronous DRAM Architectures, Organization, and Alternative Technologies,' filed January 18, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Xilinx Programmable Logic Design Quick Start Handbook (2004), filed December 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Xilinx Xilinx TQFP package datasheet (2000), filed December 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Xilinx Xilinx VQFP package datasheet (2002), filed December 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed January 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Motion for Observations, filed January 9, 2018

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 11, 2019*	
				Application Number	***15/857,519***
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				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	2	of	4	Attorney Docket Number	***129980-5023-US***

		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBIT 2004, filed January 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Response to Patent Owners Motion for Observations, filed January 23, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Opposition to Petittioner's Motion to Exclude, filed January 23, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Reply in Support of Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed January 30, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Updated Exhibit List, filed February 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Updated Exhibit List, filed February 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBIT 2005, filed February 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Hearing Transcript, filed February 14, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Final Written Decision, filed February 14, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioners' Reply to Patent Owner's Response, filed February 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Oral Testimony of R. Jacob Baker in Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (May 11, 2017), filed February 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing Fast components and Slow components, filed February 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing 4:1 MUX/DeMUX and 4 ranks of memory, filed February 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing 4:1 MUX/DeMUX and 4 ranks of memory, filed February 6, 2018

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 11, 2019*	
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				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	3	of	4	Attorney Docket Number	***129980-5023-US***

		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing 4:1 MUX/DeMUX and 4 ranks of memory (corrected Ex. 1035), filed February 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Excerpts from Brent Keeth and R. Jacob Baker, DRAM Circuit Design: A Tutorial (IEEE Press 2001), filed February 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Motion to Exclude, filed February 28, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioner's Opposition to Patent Owner's Motion to Exclude, filed March 14, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Reply to Opposition to Motion to Exclude, filed March 21, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Hearing Transcript, filed April 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Termination Decision Document, filed July 7, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Objections to Evidence, filed November 14, 2017
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Supplemental Objections to Evidence, filed November 14, 2017
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Reply to Patent Owner's Response, filed February 26, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Google, Inc. et al. v. Netlist, Inc., Appeal 2014-00777, filed February 26, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Submission on Propriety of Petitioners Reply, filed March 20, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Response to Patent Owner's Submission on Propriety of Petitioner's Reply and Supplemental Stone Declaration 1, filed March 27, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Response to Patent Owner's Motion for Observations, filed April 2, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Reply to Patent Owner's Response, filed February 26, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Opposition to Petitioner's Motion to Exclude, filed April 2, 2018

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 11, 2019*	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	4	of	4	Attorney Docket Number	***129980-5023-US***

		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Reply in Support of its Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed April 9, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Objections to Petitioner's Demonstratives, filed April 20, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Final Written Decision, filed July 18, 2018

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International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/Edith Fuentes
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023US
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Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	2017-12-15_IPR2017-00549-16-Petitioners-Reply_to_Patent-Owners-Response.pdf	8999103 9a39187a6e2a373e06cd89f961cbc8c52bb283bb	no	33
Warnings:					

Information:					
2	Non Patent Literature	IPR2017-00549_Exhibit-1024_Oral-Deposition_Carl-Sechen_Dec-2017.pdf	718822 ca5d8bf38eafeb4f3e0071d818b3578dc54d3d37	no	242
Warnings:					
Information:					
3	Non Patent Literature	IPR2017-00549_Exhibit-1025_Supplemental_Declaration-of-Harold-Stone_Dec-2017.pdf	1269407 22c9275eb6b56d848d79571871022aa32bc29741	no	31
Warnings:					
Information:					
4	Non Patent Literature	IPR2017-00549_Exhibit-1026_Xilinx_TQFP-package-datasheet-2000.pdf	1948816 56ec6722177bc4ed18a290fdfd67a79ae988e8e3	no	11
Warnings:					
Information:					
5	Non Patent Literature	2018-01-18-IPR2017-00549-Exhbit-2003-Synchronous-DRAM.pdf	6967250 57f6f81a356925d420f212d210121534e2c7d1b4	no	22
Warnings:					
Information:					
6	Non Patent Literature	2017-12-15_IPR2017-00549-1028-Xilinx-TQFP-package-datasheet_2000.pdf	375901 27d981673757cb09927f6a543b43e8a50ac9167a	no	1
Warnings:					
Information:					
7	Non Patent Literature	2017-12-15_IPR2017-00549-1029-Xilinx-VQFP-package-datasheet-2002.pdf	411724 f008486033cbfe943050b318739afaccc84f2cd5	no	1
Warnings:					
Information:					
8	Non Patent Literature	2018-01-09-IPR2017-00549_Motion-to-Exclude_Paper-18.pdf	186720 e71c814098d4f1c437b4f91d81b6702ad75cd10b	no	11
Warnings:					
Information:					

9	Non Patent Literature	2018-01-09_IPR2017-00549-PO-Motion-for-Observations-Paper-21.pdf	127169 207e1e2eb41999221ec4cdcb4e5d86de29f2d33e	no	8
Warnings:					
Information:					
10	Non Patent Literature	IPR2017-00549_Exhibit-2004-Deposition-Harold-Stone.pdf	1416130 7f543bb70abb3577481b54ea98ff9e0b2b5d33b3	no	294
Warnings:					
Information:					
11	Non Patent Literature	2018-01-23-IPR2017-00549_Petitioners-Response-to-Motion-for-Observations-Paper-22.pdf	126763 aad08f1755aea14dd73724b47a14a2722368b4a1	no	8
Warnings:					
Information:					
12	Non Patent Literature	2018-01-23_IPR2017-00549-PO-Opposition-to-Motion-to-Exclude-Paper-23.pdf	179208 da355233d4c4440b0673dbe6ebcd391cb153ed4b	no	14
Warnings:					
Information:					
13	Non Patent Literature	2018-01-30-IPR2017-00549-Reply-ISO-Motion-to-Exclude-Paper-25.pdf	183516 524ee435473874bb6b71f56fe5da132f9e254e75	no	9
Warnings:					
Information:					
14	Non Patent Literature	2018-02-09_IPR2017-00549_Petitioners-Updated-Exhibit-List-P26.pdf	117582 0e75f7ebf1765b40d526c130256487adba4be2d5	no	5
Warnings:					
Information:					
15	Non Patent Literature	2018-02-09_IPR2017-00549-PO-Updated-Exhibit-List-P27.pdf	102594 8c01695aa046198bc6059c796ba2731439a8863a	no	3
Warnings:					
Information:					

16	Non Patent Literature	IPR2017-00549_Exhibit-1027_Xilinx-Programmable-Logic-Design-Quick-Start-Handbook-2004.pdf	8375782 d6b9d698378b5608cfa3c6131a8233dc11a23a34	no	206
Warnings:					
Information:					
17	Non Patent Literature	2018-02-09_IPR2017-00549-Exhibit-2005.pdf	2838565 a7634c557278da3350516337de0404744661f5a5	no	31
Warnings:					
Information:					
18	Non Patent Literature	2018-02-14-IPR2017-00549-29_Hearing-Transcript.pdf	470003 15c5d75cf98f63c54d1ec173de03264d63f1dcf1	no	4
Warnings:					
Information:					
19	Non Patent Literature	2018-05-03_IPR2017-00549-30_Final-Written-Decision.pdf	5547801 04ad202b26bd4693bcf77301695778b5a18e6d50	no	16
Warnings:					
Information:					
20	Non Patent Literature	2018-02-06_IPR2017-00577_Petitioners-reply_Paper-16.pdf	1825448 2bd18ce6d5faceeefbd00bec35bf14b6ace34aa7	no	42
Warnings:					
Information:					
21	Non Patent Literature	2018-02-6_IPR2017-00577_Exhibit_1033-Oral_testimony-of_R-Jacob_Baker.pdf	11168252 8bf370a2222240b2608affe7bbdff812a87a26f7	no	54
Warnings:					
Information:					
22	Non Patent Literature	2018-02-6_IPR2017-00577_Exhibit_1034-Annotated_Version_Halbert_Figure_4.pdf	309677 61363f42f526bda06c3e7935331cc542e804edff	no	1
Warnings:					
Information:					

23	Non Patent Literature	2018-02-6_IPR2017-00577_Exhibit_1035-Annotated_Version_Halbert_Figure_4.pdf	311503 7413cc7f2f3dc20c812f36120e1175ad07c3d6f9	no	1
Warnings:					
Information:					
24	Non Patent Literature	2018-02-6_IPR2017-00577_Exhibit_1036-Annotated_Version_Halbert_Figure_4.pdf	331285 8f0022a4181d45c13374d594f907cf734b5b632c	no	1
Warnings:					
Information:					
25	Non Patent Literature	2018-02-6_IPR2017-00577_Exhibit_1038-Excerpts-from-Brent-Keeth.pdf	19037023 2e8766b2f764dcb5a36e12f813e713961a23f0d7	no	42
Warnings:					
Information:					
26	Non Patent Literature	2018-02-28_IPR2017-00577_PO_Motion_to_Exclude_Paper-20.pdf	147661 2a073bca7c158dff266602d6c2d5eb52c16f5ce1	no	12
Warnings:					
Information:					
27	Non Patent Literature	2018-03-14-IPR2017-00577-Opposition-to-PO_Motion-to-Exclude-Paper-21.pdf	193258 e183aa844f3e987b3fa2afdd90d4b07242e2f7d5	no	12
Warnings:					
Information:					
28	Non Patent Literature	2018-03-21_IPR2017-00577_PO_Reply-to-Pet-Opp-to-PO_Mtn-to-Exclude_Paper-22.pdf	130642 dc567e943ae72eaec60e180a1c7d208348dab8e9	no	9
Warnings:					
Information:					
29	Non Patent Literature	2017-04-02-IPR2017-00577_Hearing-Order-Paper-23.pdf	122236 bac01c36dd2969e0aed6cee065746c6d0de0cab2d	no	5
Warnings:					
Information:					

30	Non Patent Literature	2017-07-07-IPR2017-00577_Decision-Insitution.pdf	373760 a42356f83ac65be6703c7dff4b1a87b904a00b57	no	22
Warnings:					
Information:					
31	Non Patent Literature	2017-11-14_IPR2017-00667-16_Petitioners-Objections-to-Evidence.pdf	1463778 a41c01437cc0bdac312528e8715e76f3c80daa46	no	6
Warnings:					
Information:					
32	Non Patent Literature	2018-02-15_IPR2017-00667-18-Petitioners-supp-objections-to-evidence.pdf	955177 6eba83dbb8556e49737ef5022b0e6c401d9c8fb4	no	5
Warnings:					
Information:					
33	Non Patent Literature	2018-02-26_IPR2017-00667-19_Petitioners_Reply-Patent-Owners_Response.pdf	9719550 a0246f59e4df8bd43fd4baee8185344aaf957f17	no	38
Warnings:					
Information:					
34	Non Patent Literature	2018-02-26_IPR2017-00667-1032_Google-v-Netlist-Appeal-2014-00777.pdf	5005824 5eb728a1435cd437d32cd02c541abf7477847b07	no	24
Warnings:					
Information:					
35	Non Patent Literature	2018-03-27-IPR2017-00668-28-Petitioners-Response-To-PO-Submission-On-Pro.pdf	1005204 ba0e0932719184b527a8a0f1674a65f5ac73472d	no	5
Warnings:					
Information:					
36	Non Patent Literature	2018-04-02-IPR2017-00668-29-Petitioners-Response-to-PatentOwners-Motion.pdf	5348775 fc565ff69806c93ecbc2fffecc4c7d2194591bc8	no	18
Warnings:					
Information:					

37	Non Patent Literature	2018-04-02-IPR2017-00668-31-POs-Opposition-to-Petitioners-Motion-to-Excl.pdf	5305336 1c58989c4c461346e8d07b3bf4b5d4f4f8e127c7	no	19
Warnings:					
Information:					
38	Non Patent Literature	2018-04-09-IPR2017-00668-33-Petitioners-Reply-ISO-its-Motiont-to-Exclude.pdf	2155349 ea732f1bcfce7e11e435d9f1aad481688b906b18	no	9
Warnings:					
Information:					
39	Non Patent Literature	2018-04-20-IPR2017-00668-34-POs-Objections-to-Petitioners-Demonstrative.pdf	475947 b73904762fc30f220253b19921dd0a86e4ce09f3	no	4
Warnings:					
Information:					
40	Non Patent Literature	2018-07-18_IPR2017-00668_36-Final-Written-Decision.pdf	16760902 da5a146bac457cd76261036e20405f9037b206e7	no	46
Warnings:					
Information:					
41		129980-5023US_IDS.pdf	544997 9299b0c2551bbe1358b2c898afdde01767b3fe2f	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	4
	Information Disclosure Statement (IDS) Form (SB08)	5	8

Warnings:	
Information:	
Total Files Size (in bytes):	123054440

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed January 11, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Solomon et al.	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	Bansal, Gurtej
For:	MEMORY MODULE WITH DATA BUFFERING	Attorney Docket No.:	129980-5023-US

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☐ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

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2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☒ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☐ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial No. , filed on , of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☒ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. **14/715,486**, filed on **May 18, 2015**; **13/971,231** , filed on **August 20, 2013**; **13/287,081** , filed on **November 1, 2011**;

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13/032,470 , filed on **February 22, 2011**; **12/955,711** , filed on **November 29, 2010**; **12/629,827** , filed on **December 2, 2009**; **12/408,652** , filed on **March 20, 2009**; **11/335,875** , filed on **January 19, 2006**; **11/173,175** , filed on **July 1, 2005**; **11/075,395** , filed on **March 7, 2005**, are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: January 11, 2019

51,167

Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/857,519	Filing Date 12/28/2017	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $80 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $420 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT	01/11/2019	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 28	Minus	** 20	= 8		x $100 =	800
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	800

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/TAMMY D MCBETH BROWN/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 16, 2019*	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	1	of	3	Attorney Docket Number	***129980-5023-US***

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.[1]	Document Number Number - Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		9,606,907 B2	03-28-2017	Lee et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code[3] – Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Xilinx Xilinx CS280 package datasheet (1999), filed December 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Demonstratives, filed February 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Supplemental Mandatory Notices, filed April 19, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing 4:1 MUX/DeMUX and 4 ranks of memory (corrected Ex. 1035), filed February 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Deposition Transcript of R. Jacob Baker (Jan. 12, 2018), filed February 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Objections to Evidence, filed February 13, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Request for Oral Argument, filed February 28, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Deposition of Carl Sechen, Ph.D. taken December 8, 2017, filed February 26, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Deposition of Carl Sechen, Ph.D. taken February 8, 2018, filed February 26, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Objections to Evidence, filed March 5, 2018

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 16, 2019*	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	2	of	3	Attorney Docket Number	***129980-5023-US***

		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Motion to Exclude, filed March 19, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Motion for Observations, filed March 19, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Request for Oral Argument, filed March 19, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Exhibit 2007, Deposition of Harold S. Stone, filed March 19, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Submission on Propriety of Petitioners Reply, filed March 20, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Updated Mandatory Notices, filed April 2, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Reply in Support of its Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed April 2, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Objection to Petitioner's Demonstratives, filed April 20, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Hearing Transcript, filed April 24, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Final Written Decision, filed July 18, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Objections to Evidence, filed November 14, 2017
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Notice of Deposition of Carl Sechen, filed January 30, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Supplemental Objections to Evidence, filed February 15, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Reply to Patent Owner's Response, filed February 26, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Objections to Evidence, filed March 5, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Motion for Observations, filed March 19, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Request for Oral Argument, filed March 19, 2018

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 16, 2019*	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	3	of	3	Attorney Docket Number	***129980-5023-US***

		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Submission on Propriety of Petitioner's Reply, filed March 20, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Response to Patent Owner's Submission on Propriety of Petitioner's Reply and Supplemental Stone Declaration, filed March 27, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Response to Patent Owner's Motion for Observations, filed April 2, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Hearing Transcript, filed April 24, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petition, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Preliminary Response, filed April 10, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Decision Granting Institution of Inter Partes Review, entered June 29, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Petition, filed December 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Petitioner's Power of Attorney, filed December 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, File History of U.S. Patent No.9606907, filed December 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Declaration of Dr. Harold Stone, filed December 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Curriculum Vitae of Dr. Harold Stone, filed December 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Patent Owner's Preliminary Response, filed May 7, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Decision Granting Institution of Inter Partes Review, entered August 6, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00365, Petition, filed December 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00365, Patent Owner's Preliminary Response, filed December 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00365, Decision Granting Institution of Inter Partes Review, entered August 6, 2018

Examiner Signature		Date Considered	

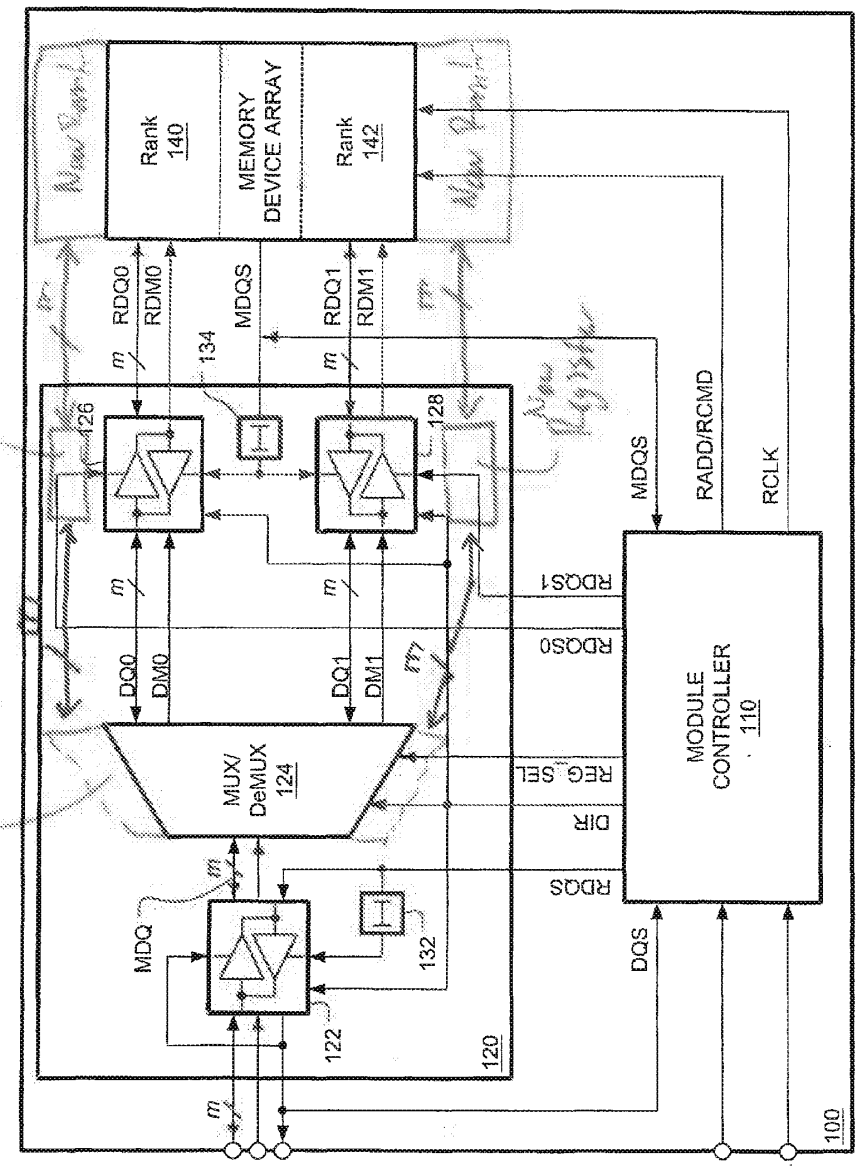


Fig. 4

EXHIBIT 1036
WIT. Dalal
DATE 11/2/18
DATE RCVD 5DR FMR CRR

Electronic Acknowledgement Receipt

EFS ID:	34878877
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/Edith Fuentes
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023US
Receipt Date:	16-JAN-2019
Filing Date:	28-DEC-2017
Time Stamp:	21:30:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5023US_IDS.pdf	513918 87fc89b58ea34cb58f912a9ecc816dc9b23a808d	yes	7

	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Transmittal Letter		1	4	
	Information Disclosure Statement (IDS) Form (SB08)		5	7	
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2	Non Patent Literature	IPR2017-00549_Exhibit-1030_Xilinx-CS280-package-datasheet-1999.pdf	112750 df5482157d8ed6e6940e3eef158a1df23ba20916	no	1
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3	Non Patent Literature	2018-02-06_IPR2017-00577_Exhibit-1036-Correct-Ex-1035-Anno-Vers-Halbert-Fig-4-Shng-4-1-MUX_DeMUX.pdf	220754 c4ed0f79ab92a779816f83e604512f6c85e881b0	no	1
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4	Non Patent Literature	2017-10-31_IPR2017-00577_Petitioner-Objections-to-Evidence_Paper-13.pdf	126498 252efb5ddd9f738dc51d296ee73bd9b00bb301d1	no	6
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5	Non Patent Literature	2018-02-28_IPR2017-00577_PO_Request_for_Oral_Argument-Paper-19.pdf	109567 7cf990e6eae82e4ec5bcdc99f508197d02360531	no	3
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6	Non Patent Literature	2018-02-26-IPR2017-00667-1029-Deposition-of-Carl-Sechen-Ph-D-taken-December-8-2017.pdf	11553863 d695914a272dc5f6c72a0f5aaac53c14867fe494	no	242
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7	Non Patent Literature	2018-03-05-IPR2017-00667-Patent-Owners-Objections-to-Evidence-.pdf	150003 d78a19fd6f9ac99f55cf87220c8af1c58fc6777d	no	6
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8	Non Patent Literature	2018-03-19-IPR2017-00667-Petitioners-Motion-to-Exclude-.pdf	197336 3597251567fa3a8822f0b41df322c0e14fac6a1b	no	17
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9	Non Patent Literature	2018-03-18-IPR2017-00667-PO-Motion-for-Observations-.pdf	208978 61df325a7aa8647e822236a87804b90b97d87fce	no	14
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10	Non Patent Literature	2018-03-18-IPR2017-00667-PO-Request-for-Oral-Argument-.pdf	141105 a27433aef1b69076a4709e44b72ac74bc2b34b74	no	5
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11	Non Patent Literature	2018-03-19-IPR2017-00667-Exhibit-2007-Deposition-of-Harold-S-Stone.pdf	1501118 010cf19f1c41763ed18291e6f0a64f47525b20f6	no	268
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12	Non Patent Literature	2018-03-20-IPR2017-00667-PO-Sbumission-on-Proprietary-of-Petitioners-Reply.pdf	111855 ce324c989078ce054725ac92a270ac51f59305cb	no	4
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13	Non Patent Literature	2018-04-02-IPR2017-00667-Petitioners-Updated-Mandatory-Notices-.pdf	116554 eefad3f1b0cdd2dc9d881455b109e48b8fd59ee8	no	4
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14	Non Patent Literature	2018-04-09-IPR2017-00667-Petitioners-Reply-Supp-Motion-Exclude-Inadmiss-Test-POs-Expert-C-Sechen.pdf	165783 b9c9bdd35c7d0336d45c8fa6f0d3d85b4df8a6e3	no	9
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15	Non Patent Literature	2018-04-20-IPR2017-00667-Patent-Owners-Objections-to-Petitioners-Demonstratives.pdf	232527 7a91bfb1269be53db61fe3ecf0402091ed1870a6	no	4
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18	Non Patent Literature	2018-04-19-IPR2017-00549-28_Patent-Owner-Supplemental-Mandatory-Notices.pdf	5685552 a150dd633730d1d2b6ca15e1055948475ff7e949	no	116
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19	Non Patent Literature	2018-02-18-IPR2017-00667-1030-Deposition-of-Carl-Sechen-Ph-D-taken-February-8-2018.pdf	12536607 15258857f19485c7ca34606408659fa52e428d2e	no	236
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20	Non Patent Literature	2018-02-06_IPR2017-00577_Exhibit-1039-Deposition-Transcript-of-R-Jacob.pdf	11923932 a5ffdac0f7c14f37d9368a83839754c524b9fe91	no	266
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21	Non Patent Literature	IPR2017-00667-Final_Written_Decision_2018-07-18-.pdf	1053580 12dc731181ab747df5231186afa6270da60c787e	no	44
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22	Non Patent Literature	2014-11-14-IPR2017-00668-Petitioners-Objections-to-Evidence-.pdf	124523 9500519511419383 93e198124c46033a59099888	no	6
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23	Non Patent Literature	2018-01-30-IPR2017-00668-Notice-of-Deposition-of-Carl-Sechen-.pdf	98596 9ba97a5df102461406876a120ad26ab79fc8fb23	no	3
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28	Non Patent Literature	2018-03-19-IPR2017-00668-PO-Request-for-Oral-Argument-.pdf	113518 ab4ebe8191ff49d6ccf5c6e6e561b8e01bf8b9f4	no	4
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29	Non Patent Literature	2018-03-20-IPR2017-00668-Patent-Owners-Submission-on-Propriety-of-Petitioners-Reply-.pdf	111854 928ff29ff8c1ba22b29344702576fdcc4c586cc9	no	4
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30	Non Patent Literature	2018-03-27-IPR2017-00668-Petitioners-Resp-PO-Subm-Propriety-Petitioners-Reply-And-Supp-Stone-Dec.pdf	112087 a66d5cc0f75334ab4fb9894616961857f6010baf	no	5
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35	Non Patent Literature	IPR2018-00363_Granting-Institution-of-IPR.pdf	605787 2cdd235dad0953122cb9d1c788ea0f27a741865f	no	33
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40	Non Patent Literature	2018-05-07-IPR2018-00364-Patent-Owners-Preliminary-Response.pdf	1859038 6c15098a112b13d8bb7253cb11d0b096d348cdf8	no	47
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42	Non Patent Literature	2017-12-27-IPR2018-00364-1002-File-History-of-U-S-Patent-No-9606907-Part1.pdf	15362888 3037006e5e9fc1e372cd19dd8a60a9a716cb5b89	no	216
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		Total Files Size (in bytes):	120400438		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed January 16, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Solomon et al.	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	Bansal, Gurtej
For:	MEMORY MODULE WITH DATA BUFFERING	Attorney Docket No.:	129980-5023-US

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☐ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

Petitioners
Ex. 1054, p. 349

2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☒ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☐ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial No. , filed on , of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☒ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. **14/715,486**, filed on **May 18, 2015**; **13/971,231** , filed on **August 20, 2013**; **13/287,081** , filed on **November 1, 2011**;

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13/032,470 , filed on **February 22, 2011**; **12/955,711** , filed on **November 29, 2010**; **12/629,827** , filed on **December 2, 2009**; **12/408,652** , filed on **March 20, 2009**; **11/335,875** , filed on **January 19, 2006**; **11/173,175** , filed on **July 1, 2005**; **11/075,395** , filed on **March 7, 2005**, are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: January 16, 2019

Jamie J. Zheng 51,167 (Reg. No.)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 16, 2019*	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	1	of	3	Attorney Docket Number	***129980-5023-US***

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.[1]	Document Number Number - Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		7,334,150 B2	02-19-2008	Ruckerbauer et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code[3] – Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petition, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Declaration of Dr. Harold Stone, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1022, Decision Denying Institution of Inter Partes Review, entered December 16, 2014
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1023, Decision Denying Institution of Inter Partes Review, entered March 9, 2015
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1024, Excepts from the Hearing in Certain Memory Modules and Components Thereof, and Products Containing Same, filed May 8, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1025, Complainant Netlist, Inc., Initial Post-Hearing Brief , filed May 30, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1026, Respondents' Post-Hearing Brief , filed May 30, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1027, Demonstrative-Graphics-from-hynix-post-hearing-brief, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1028, Netlist-reply-post-hearing-brief, filed December 22, 2017

Examiner Signature		Date Considered	

DB2/ 35764686.1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 16, 2019*	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	2	of	3	Attorney Docket Number	***129980-5023-US***

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1029, Respondent's Reply Post-Hearing Brief, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1030, High-Quality Versions of Demonstrative-Graphics-from-hynix-reply-post-hearing-brief, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1031, Institution of the '185 patent, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1032, Final Written Decision, Diablo Techs., Inc v. Netlist Inc., Paper No. 33, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1033, Decision, Netlist Inc., v. Diablo Techs., Inc., filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1034, Netlist's Infringement Claim Chart of , filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1035, Stone, H.S. Microcomputer Interfacing, Reading, MA Addison Wesley, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1039, Intel E7525 Memory Controller Hub (MCH) Chipset Datasheet, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1040, Initial Determination, Certain Memory Modules and Components Thereof, and Products Containing Same, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1041, MEMORY-SYSTEMS-Cache-DRAM-Disk, Bruce Jacobs et al., filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1042, Direct DRAM Datasheet, Bruce Jacobs et al., filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Notice of Accorded Filing Date, filed January 10, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Preliminary Response, filed April 10, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Granting Institution of Inter Partes Review, entered June 29, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Objection to Petition Evidence, filed July 16, 2018

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 16, 2019*	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	3	of	3	Attorney Docket Number	***129980-5023-US***

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Order 37 C.F.R. 42.5, filed August 2, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Mehran Arjomand,' filed July 30, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Michael D. Hatcher,' filed July 30, 2018

Examiner Signature		Date Considered	

Electronic Acknowledgement Receipt

EFS ID:	34879186
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/Edith Fuentes
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023US
Receipt Date:	16-JAN-2019
Filing Date:	28-DEC-2017
Time Stamp:	21:35:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5023US_IDS-w-Special-Transmittal.pdf	290736 f7da8f47a256c0a10db1ef96f36e1449cf5918b1	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	2
	Information Disclosure Statement (IDS) Form (SB08)	3	5
Warnings:			
Information:			
	Total Files Size (in bytes):	290736	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed January 16, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Solomon et al.	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	Bansal, Gurtej
For:	MEMORY MODULE WITH DATA BUFFERING	Attorney Docket No.:	129980-5023-US

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 27 references. Copies of foreign documents and/or their translation and non-patent literature were submitted on commonly-owned U.S. Pat. App. No. 15/470,856, filed March 27, 2017, which is accessible via PAIR.

Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

Petitioners
Ex. 1054, p. 358

This Information Disclosure Statement is being filed with the filing of a Request for Continued Examination, and presumably no fee is required. The Commissioner is authorized to charge any required fees to Deposit Account No. 50-0310 (order no. 129980-5023-US).

Respectfully submitted,

Date: January 16, 2019

Jamie J. Zheng 51,167
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(650) 843-4000

Electronically filed February 21, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Netlist, Inc.	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	BANSAL, Gurtej
For:	*MEMORY MODULE WITH DATA BUFFERING*	Attorney Docket No.:	129980-5023-US
		Date:	February 21, 2019

PRELIMINARY AMENDMENT AFTER RCE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

Applicant files herewith a Preliminary Amendment in the above-referenced patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US).

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system at a specified data rate via a data bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first burst of data and a first burst of data strobes and the second memory command to cause the memory module to receive or output a second burst of data and a second burst of data strobes, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks, each rank of the plurality of ranks having a same bit width as the memory module, wherein the plurality of ranks include a first rank selected to receive or output the first burst of data and the first burst of data strobes at the specified data rate in response to the first memory command, and a second rank ~~is~~ selected to receive or output the second burst of data and the second burst of data strobes at the specified data rate in response to the second memory command;

[[a]] at least one data buffer including a set of signal paths coupled between ~~at least one first memory integrated circuit in~~ the first rank and the data bus, and between ~~at least one second memory integrated circuit in~~ the second rank and the data bus; and

logic coupled to the at least one data buffer and configured to respond to the first memory command by providing first control signals to the at least one data buffer, wherein the at least one data buffer in response to the first control signals is configured to enable the set of signal paths to transfer ~~to enable communication of~~ respective bits of the first burst of data and respective data strobes of the first burst of data strobes at the specified data rate between the first rank ~~memory devices~~ and the memory controller through the set of signal paths in the at least one data buffer, wherein the logic is further configured to respond to the second memory command by providing

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second control signals to the at least one data buffer, and wherein the at least one data buffer in response to the second control signals is configured to enable the set of signal paths to transfer ~~to enable communication of~~ respective bits of the second burst of data and respective strobes of the second burst of data strobes at the specified data rate between the ~~memory devices~~ second rank and the memory controller through the set of signal paths in the at least one data buffer~~, the first data including a first data burst and the second data including a second data burst following the first data burst on the data bus;~~

wherein the at least one data buffer adds at least one clock cycle time delay for data transfer between the plurality of memory integrated circuits and the memory controller so that ~~the memory module has~~ an overall CAS latency of the memory module is at least one clock cycle greater than an actual operational CAS latency of each of the plurality of memory integrated circuits~~; and~~

~~wherein the first data and the first data strobes, and the second data and the second data strobes, are communicated between the memory devices and the memory controller at a predetermined data rate~~.

2. (Currently Amended) The memory module of claim 1, wherein each of the plurality memory integrated circuits has a corresponding load, and wherein the at least one data buffer is configured to isolate the loads of ~~both the at least one first memory integrated circuit and the at least one second memory integrated circuit~~ the plurality of memory integrated circuits from the memory controller.

3. (Currently Amended) The memory module of claim 1, wherein the logic is coupled to the printed circuit board and is further configured to respond to the first ~~read/write~~ memory command by outputting a first set of registered command signals and to subsequently respond to the second ~~read/write~~ memory command by outputting a second set of registered command signals, the first ~~read/write~~ memory command ~~including~~ having associated therewith a first set of input chip select signals corresponding to respective ranks of the plurality of ranks and the second ~~read/write~~ memory command ~~including~~ having associated therewith a second set of input chip select signals corresponding to respective ranks of the plurality of ranks, the first set of registered command signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals, the second set of registered command signals including a second plurality of registered chip select signals corresponding to respective ones of

the second plurality of input chip select signals, the first set of registered chip select signals including a first registered chip select signal each having an active signal value ~~while the rest of the first set of~~ and one or more other registered chip select signals each ~~has~~ having a non-active signal value, the second set of registered chip select signals including a second registered chip select signal each having an active signal value ~~while the rest of the second set of~~ and one or more other registered chip select signals each ~~has~~ having a non-active signal value, and wherein the first rank is configured to receive the first registered chip select signal and the second rank is configured to receive the second registered chip select signal.

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Currently Amended) The memory module of claim 1, further comprising an SPD device that reports ~~an~~ the overall CAS latency of the memory module to the memory controller~~, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits~~.

9. (Previously Presented) The memory module of claim 1, wherein the memory module is further coupled to the memory controller using an on-die-termination (ODT) bus, wherein each of the plurality of memory integrated circuits includes an ODT circuit, the memory module further comprising a termination circuit external to any of the plurality of memory integrated circuits, wherein the termination circuit is coupled to the ODT bus and to the ODT circuit of at least one of the plurality of memory integrated circuits, wherein the termination circuit is configured to provide external termination of at least one of the plurality of memory integrated circuits in response to an ODT signal on the ODT bus, and wherein the ODT circuit of the at least one of the plurality of memory integrated circuits is disabled.

10. (Currently Amended) The memory module of claim 1, wherein the at least one data buffer comprises combinatorial logic, registers, and logic pipelines to time data transfers through the at

least one data buffer~~, and is configured to register an additional clock cycle for transferring at the predetermined data rate the respective bits of the first data and respective data strobes of the first burst of data strobes, or the respective bits of the second burst of data and respective data strobes of the second burst of data strobes, through the data buffer~~.

11. (Currently Amended) The memory module of claim 1, wherein the logic is further configured to determine the overall CAS latency of the memory module.

12. (Currently Amended) The memory module of claim 1, wherein the set of signal paths are enabled in accordance with the overall CAS latency of the memory module~~ logic is further configured to enable communication of the first burst of data and the respective strobes of the first burst of data strobes, or the respective bits of the second burst of data and the respective strobes of the second burst of data strobes, at the predetermined specified data rate between the memory module and the memory controller in accordance with the overall CAS latency~~.

13. (Currently Amended) The memory module of claim 1, wherein each of the plurality of ranks is 72-bit wide, wherein each rank of the plurality of memory integrated circuits ~~include~~ includes 18~~-36~~ 4-bit wide memory integrated circuits configured in 9~~-18~~ pairs, wherein ~~the at least one first memory integrated circuit includes~~ a first pair of memory integrated circuits in the first rank is configured to communicate a respective byte of the first burst of data, and wherein ~~the at least one second memory integrated circuit includes~~ a second pair of memory integrated circuits in the second rank is configured to communicate a respective byte of the second burst of data.

14. (Previously Presented) The memory module of claim 13, wherein the first pair of memory integrated circuits are configured to simulate an 8-bit wide memory device, and the second pair of memory integrated circuits are configured to simulate another 8-bit wide memory device.

15. (Previously Presented) The memory module of claim 13, further comprising an SPD device programmed with data to characterize each pair of memory integrated circuits as a virtual 8-bit wide memory device.

16. (Currently Amended) The memory module of claim 3 [[1]], wherein the data buffer includes a set of circuit components configurable to enable the set of signal paths in response to

the first set of control signals and subsequently in response to the second set of control signals ~~switches each coupled between a respective data or strobe pin of the at least one first memory device and a corresponding signal line in the data bus, and between a respective data or strobe pin of the at least one second memory device and the corresponding signal line in the data bus, and wherein the first control signals include control signals for enabling the switches and the second control signals include control signals for enabling the switches~~.

17. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to read/write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to ~~respond to~~ receive a first set of input command signals associated with a first read/write memory command and to output ~~by outputting~~ a first set of registered command signals in response to the first set of input command signals, the first set of input command signals ~~read/write memory command~~ including a first plurality of input chip select signals, the first set of registered command signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals, the first plurality of registered chip select signals including a first registered chip select signal having an active signal value ~~while the rest of the first plurality of~~ and one or more other registered chip select signals each ~~has~~ having a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of ranks, each rank of the plurality of ranks having a same data width as the memory module, wherein the plurality of ranks ~~correspond to, and~~ are configured to receive[[,]] respective ones of the first plurality of registered chip select signals, wherein a first rank in the plurality of ranks receiving the first registered chip select signal having the active signal value is selected to receive or output a first burst of data and a first burst of data strobes associated with ~~in response to~~ the first read/write command;

at least one buffer coupled between data and strobe signal lines in the memory bus and corresponding data and strobe pins of the memory devices in each of the plurality of ranks, the at

least one buffer including a set of signal paths between the memory bus and the memory devices ~~each between a respective data or strobe signal line in the memory bus and a corresponding data or strobe pin of each of a set of memory devices, the set of memory devices including one memory device in each of the plurality of ranks~~; and

wherein the logic is further configured to, in response to the first read/write memory command, output first control signals to the at least one buffer, and wherein the at least one buffer is configured in response to the first control signals to enable the set of signal paths to transfer ~~so as to allow communication of~~ the first burst of data and the first burst of data strobes between the memory devices and the memory controller through the at least one buffer; and

wherein ~~the memory module has an overall CAS latency and~~ the set of signal paths are enabled in accordance with ~~the~~ an overall CAS latency of the memory module, and wherein the at least one buffer adds at least one clock cycle time delay for data transfer through the at least one buffer such that the overall CAS latency of the memory module is at least one clock cycle greater than an actual operational CAS latency of each of the plurality of memory devices.

18. (Previously Presented) The memory module of claim 17, wherein each of the memory devices has a corresponding load, and the at least one buffer is configured to isolate the loads of the memory devices from the memory bus.

19. (Currently Amended) The memory module of claim 17, wherein the first burst of data includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein the set of signal paths are enabled ~~during~~ for a time period when the set of consecutively transmitted data bits are successively ~~communicated~~ transferred through the at least one buffer.

20. (Currently Amended) The memory module of claim 17, wherein the logic is further configured to respond to a second set of input command signals associated with a second read/write memory command by outputting a second set of registered command signals, the second set of input command signals including a second plurality of input chip select signals, the second set of registered command signals including a second plurality of registered chip select signals corresponding to respective ones of the second plurality of input chip select signals, the second plurality of registered chip select signals including a second registered chip select signal

having the active signal value ~~while the rest of the second plurality of~~ and one or more other registered chip select signals each ~~has~~ having the ~~a~~ non-active signal value, wherein a second rank different from the first rank ~~is~~ includes memory devices configured to receive the second registered chip select signal having the active signal value and is selected to output or receive a second burst of data and a second burst of data strobes associated with ~~in response to~~ the second read/write command, wherein the logic is further configured to, in response to the second read/write memory command, output second control signals to the at least one buffer, and wherein the at least one buffer is configured in response to the second control signals to enable the set of signal paths to transfer ~~so as to allow communication of~~ the second burst of data and the second burst of data strobes between the memory devices and the memory controller through the at least one buffer~~, the second burst of data following the first burst of data on the memory bus~~.

21. (Previously Presented) The memory module of claim 17, wherein each of the memory devices is 4-bits wide, and wherein each of the plurality of ranks is 72-bits wide and ~~include~~ includes 18 memory devices configured in pairs, and wherein each pair of 4-bit-wide memory devices are configured to simulate an 8-bit-wide memory device.

22. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to read/write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured ~~to respond~~ to receive a set of input command signals associated with a read/write memory command ~~by outputting~~ and to output a set of registered command signals in response to the set of input command signals, the ~~read/write memory command~~ set of input command signals including a plurality of input chip select signals, the set of registered command signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals, the plurality of registered chip select signals including [[one]] a registered chip select signal having an active

signal value ~~while the rest of the plurality of~~ and one or more other registered chip select signals each ~~has~~ having a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of ranks, each rank of the plurality of ranks having a same data width as the memory module, wherein the plurality of ranks ~~correspond to, and~~ are configured to receive[[,]] respective ones of the plurality of registered chip select signals, wherein a first rank receiving the registered chip select signal having the active signal value is selected to receive or output a first burst of data and a first burst of data strobes ~~in response to~~ associated with the read/write command;

a plurality of configurable circuit components to enable or disable a set of signal paths between ~~a~~ respective data or strobe signal ~~line~~ lines in the memory bus and ~~a~~ corresponding data or strobe ~~pin~~ pins of the memory devices ~~in each of the plurality of ranks~~; and

wherein the logic is further configured to, in response to the read/write memory command, output first control signals, ~~for configuring~~ wherein the plurality of configurable circuit components are configured in response to the first control signals to enable the set of signal paths to transfer ~~to allow communication of~~ the first burst of data and the first burst of data strobes between the memory devices and the memory controller; and

wherein ~~the memory module has an overall CAS latency and~~ the set of signal paths are enabled ~~configurable circuit components are configured to allow communication of the first burst of data~~ in accordance with ~~the~~ an overall CAS latency of the memory module; and

wherein the memory module registers at least one additional clock cycle time for data transfer between the memory controller and the memory devices such that the overall CAS latency of the memory module is at least one clock cycle greater than an actual operational CAS latency of each of the plurality of memory devices.

23. (Currently Amended) The memory module of claim 22, wherein the first burst of data includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein the set of signal paths ~~plurality of configurable circuit components~~ are enabled during a time period when the set of consecutively transmitted data bits are successively ~~communicated~~ transferred through the plurality of configurable circuit components.

24. (Currently Amended) The memory module of claim 22, wherein the logic is further configured to respond to a subsequent set of input command signals associated with a subsequent

read/write memory command by outputting a subsequent set of registered command signals, the subsequent set of input command signals including a subsequent plurality of input chip select signals, the subsequent set of registered command signals including a subsequent plurality of registered chip select signals corresponding to respective ones of the subsequent plurality of input chip select signals, the subsequent plurality of registered chip select signals including ~~one subsequent~~ a subsequently registered chip select signal having the active signal value ~~while the rest of the subsequent plurality of~~ and one or more other registered chip select signals each ~~has a~~ having the non-active signal value, wherein a second rank different from the first rank is configured to receive the subsequently registered ~~subsequent~~ chip select signal having the active signal value and is selected to output or receive a second burst of data and a second burst of data strobes ~~in response to~~ associated with the subsequent read/write command, wherein the logic is further configured to, in response to the subsequent ~~second~~ read/write memory command, output second control signals, ~~for configuring~~ wherein the plurality of configurable circuit components are configured to enable the set of signal paths in response to the second control signals to transfer ~~allow communication of~~ the second burst of data and the second burst of data strobes between the memory devices and the memory controller.

25. (Currently Amended) The memory module of claim 17, wherein the memory devices are organized in four ranks and the first set of input command signals include four chip select signals, one for each of the four ranks ~~overall CAS latency has at least one more clock cycle than an actual operational CAS latency of each of the memory devices~~.

26. (Currently Amended) The memory module of claim 17, wherein the at least one data buffer comprises combinatorial logic, registers, and logic pipelines ~~, and is configured to register an additional clock cycle for transferring respective bits of the first data and respective data strobes of the first data strobes at a certain rate~~ to time data transfers through the at least one data buffer.

27. (Previously Presented) The memory module of claim 17, wherein the logic is further configured to determine the overall CAS latency.

28. (Currently Amended) The memory module of claim 17, wherein the first burst of data and the first burst of data strobes are communicated between the memory devices and the memory controller at a ~~predetermined~~ specified data rate.

29. (Currently Amended) The memory module of claim 17 ~~20~~, wherein the first burst of data is transferred in a plurality of cycles including a first cycle and a second cycle, wherein the first control signals include a first subset of control signals for the first cycle and a subsequent second subset of control signals for the second cycle, wherein the set of signal paths are enabled in response to the first subset of control signals and subsequently in response to the second subset of control signals ~~set of signal paths are disabled after communication~~ of the first burst of data ~~and first burst of data strobes through the at least one buffer and before communication of the second burst of data and the second burst of data strobes through the at least one buffer~~.

30. (Currently Amended) The memory module of claim ~~22, wherein the overall CAS latency has at least one more clock cycle than an actual operational CAS latency of each of the memory devices~~ 20, wherein:

the first set of input command signals including a first input command signal indicating that the first read/write command is a read memory command;

the second set of input command signals including a second input command signal indicating that the second read/write command is a write memory command;

the set of signal paths are enabled a first number of clock cycles after the first input command signal is received by the logic; and

the set of signal paths are enabled a second number of clock cycles after the second input command signal is received by the logic, the second number being different from the first number.

31. (Currently Amended) The memory module of claim 22, wherein the first burst of data and the first burst of data strobes are ~~communicated~~ transferred between the first rank of the memory devices and the memory controller at a ~~predetermined~~ specified data rate.

32. (Currently Amended) The memory module of claim 22 ~~24~~, wherein the first burst of data is transferred in a plurality of cycles including a first cycle and a second cycle, wherein the first control signals include a first subset of control signals for the first cycle and a subsequent second subset of control signals for the second cycle, wherein the plurality of configurable circuit components are configured to enable the set of signal paths in response to the first subset of control signals and subsequently in response to the second subset of control signals ~~disabled after communication of the first burst of data and first burst of data strobes through the at least one~~

~~buffer and before communication of the second burst of data and the second burst of data strobes through the at least one buffer~~.

REMARKS

This Amendment is in response to the Notice of Allowance dated October 11, 2018 and is filed with a Request for Continued Examination.

Claims 1-3, 8, 10-13, 16-17, 19-20, 22-26, and 28-32 are amended. No new matter is added.

Support for the amendments can be found in at least paragraphs [0053], [0056]-[0058], [0107], [0117], and FIGS. 6A and 6B.

CONCLUDING REMARKS

In light of the above amendments and remarks, the Applicant respectfully requests that the amendments be entered. The Examiner is invited to call the undersigned attorney at (650) 843-4000, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: February 21, 2019

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
Phone: (650) 843-4000

Electronic Acknowledgement Receipt

EFS ID:	35219521
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023US
Receipt Date:	21-FEB-2019
Filing Date:	28-DEC-2017
Time Stamp:	21:13:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980_5023US_PRE_AMEND.pdf	182245 1ff64d5025b62a2ff99f3989bfa891149b78a5b8	yes	13

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Claims	2	12
	Applicant Arguments/Remarks Made in an Amendment	13	13
Warnings:			
Information:			
	Total Files Size (in bytes):	182245	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 04/09/2019
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER
BANSAL, GURTEJ

ART UNIT	PAPER NUMBER
2139	

DATE MAILED: 04/09/2019

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/857,519	12/28/2017	Jefferey C. Solomon	129980-5023US	9826

TITLE OF INVENTION: MEMORY MODULE WITH DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	07/09/2019

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
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Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 04/09/2019
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/857,519	12/28/2017	Jefferey C. Solomon	129980-5023US	9826

TITLE OF INVENTION: MEMORY MODULE WITH DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	07/09/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
BANSAL, GURTEJ	2139	711-105000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/857,519	12/28/2017	Jefferey C. Solomon	129980-5023US	9826

79141 7590 04/09/2019

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER	
BANSAL, GURTEJ	
ART UNIT	**PAPER NUMBER**
2139	

DATE MAILED: 04/09/2019

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	**Application No.** 15/857,519	**Applicant(s)** Solomon et al.	
	Examiner GURTEJ BANSAL	**Art Unit** 2139	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to Applicant's amendment dated 02/21/2019.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-3 and 8-32 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information , please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 1/11/2019; 1/16/2019; 1/16/2019.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/857,519	Solomon et al.
	Examiner	Art Unit
	GURTEJ BANSAL	2139

CPC							
Symbol						Type	Version
G06F	/	13	/	1673		F	2013-01-01
G11C	/	5	/	04		I	2013-01-01
G06F	/	13	/	00		I	2013-01-01
G06F	/	12	/	00		I	2013-01-01
G06F	/	13	/	4243		I	2013-01-01
G06F	/	13	/	4282		I	2013-01-01
G11C	/	7	/	1072		I	2013-01-01
G11C	/	15	/	00		I	2013-01-01
Y02D	/	10	/	14		A	2018-01-01
Y02D	/	10	/	151		A	2018-01-01

CPC Combination Sets								
Symbol						Type	Set	Ranking	Version
	/		/						

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	28	
/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	29 March 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	9A

U.S. Patent and Trademark Office — Part of Paper No.: 20190329

Petitioners
Ex. 1054, p. 380

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/857,519	Solomon et al.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

INTERNATIONAL CLASSIFICATION					
CLAIMED					
G06F	/	12	/	00	
NON-CLAIMED					
	/		/		

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	28	
/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	29 March 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	9A

U.S. Patent and Trademark Office — Part of Paper No.: 20190329

Petitioners
Ex. 1054, p. 381

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/857,519	Solomon et al.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	5	10	15	19	20	28								
2	2	6	11	22	20	21	29								
8	3	7	12	16	21	23	30								
	4	10	13	24	22	27	31								
	5	11	14	25	23	28	32								
	6	12	15	26	24										
	7	9	16	17	25										
3	8	13	17	18	26										
4	9	14	18	19	27										

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	28	
/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	29 March 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	9A

U.S. Patent and Trademark Office — Part of Paper No.: 20190329

Petitioners
Ex. 1054, p. 382

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/857,519	Solomon et al.
	Examiner	Art Unit
	GURTEJ BANSAL	2139

CPC - Searched*		
Symbol	Date	Examiner
G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc.	09/27/2018	GB

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Inventor Search in PE2E	09/27/2018	GB
Text Search in EAST (See Attached)	09/27/2018	GB
NPL Search in Google Scholar (See Attached)	09/27/2018	GB
Updated Text Search in EAST (See Attached)	03/29/2019	GB
NPL Search in Google Scholar (See Attached)	03/29/2019	GB

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc.	09/27/2018	GB
	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc.	03/31/2019	GB

/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	

Petitioners
Ex. 1054, p. 383

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 11, 2019*	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	1	of	4	Attorney Docket Number	***129980-5023-US***

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.[1]	Document Number Number - Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code[3] – Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's reply to Patent Owner's Response, filed December 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Deposition Transcript of Carl Sechen, filed December 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Supplemental Declaration of Harold S. Stone, filed December 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Xilinx CoolRunner XPLA3 CPLD product specification (2000), filed December 15, 201
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBIT 2003, 'Synchronous DRAM Architectures, Organization, and Alternative Technologies,' filed January 18, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Xilinx Programmable Logic Design Quick Start Handbook (2004), filed December 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Xilinx Xilinx TQFP package datasheet (2000), filed December 15, 2017
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		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed January 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Motion for Observations, filed January 9, 2018

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/29/2019

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 11, 2019*	
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				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	2	of	4	Attorney Docket Number	***129980-5023-US***

		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBIT 2004, filed January 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Response to Patent Owners Motion for Observations, filed January 23, 2018
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		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Reply in Support of Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed January 30, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Updated Exhibit List, filed February 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Updated Exhibit List, filed February 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBIT 2005, filed February 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Hearing Transcript, filed February 14, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Final Written Decision, filed February 14, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioners' Reply to Patent Owner's Response, filed February 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Oral Testimony of R. Jacob Baker in Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (May 11, 2017), filed February 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing Fast components and Slow components, filed February 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing 4:1 MUX/DeMUX and 4 ranks of memory, filed February 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing 4:1 MUX/DeMUX and 4 ranks of memory, filed February 6, 2018

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/29/2019

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Sheet	3	of	4	Attorney Docket Number	***129980-5023-US***

		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing 4:1 MUX/DeMUX and 4 ranks of memory (corrected Ex. 1035), filed February 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Excerpts from Brent Keeth and R. Jacob Baker, DRAM Circuit Design: A Tutorial (IEEE Press 2001), filed February 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Motion to Exclude, filed February 28, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioner's Opposition to Patent Owner's Motion to Exclude, filed March 14, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Reply to Opposition to Motion to Exclude, filed March 21, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Hearing Transcript, filed April 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Termination Decision Document, filed July 7, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Objections to Evidence, filed November 14, 2017
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Supplemental Objections to Evidence, filed November 14, 2017
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Reply to Patent Owner's Response, filed February 26, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Google, Inc. et al. v. Netlist, Inc., Appeal 2014-00777, filed February 26, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Submission on Propriety of Petitioners Reply, filed March 20, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Response to Patent Owner's Submission on Propriety of Petitioner's Reply and Supplemental Stone Declaration 1, filed March 27, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Response to Patent Owner's Motion for Observations, filed April 2, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Reply to Patent Owner's Response, filed February 26, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Opposition to Petitioner's Motion to Exclude, filed April 2, 2018

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/29/2019

DB2/ 35753493.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 11, 2019*	
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				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	4	of	4	Attorney Docket Number	***129980-5023-US***

		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Reply in Support of its Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed April 9, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Objections to Petitioner's Demonstratives, filed April 20, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Final Written Decision, filed July 18, 2018

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/29/2019

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

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Dual-port buffer-to-**memory** interface

JB Halbert, JM Dodd, C Lam, RM Bonella - US Patent 6,742,098, 2004 - Google Patents

... 00—Interconnection of, or transfer of information or other signals between, **memories**, input/output ... data **strobe** RDQS low in turn, thereby signaling to the primary **memory** controller that ... DO_a2 (note that with multiple **strobes** coming from multiple devices, each **strobe** may be ...

Cited by 361 Related articles All 2 versions

Dual-port buffer-to-**memory** interface

JB Halbert, JM Dodd, C Lam, RM Bonella... - US Patent ..., 2006 - Google Patents

... 00—Interconnection of, or transfer of information or other signals between, **memories**, input/output ... data **strobe** RDQS low in turn, thereby signaling to the primary **memory** controller that ... DO_a2 (note that with multiple **strobes** coming from multiple devices, each **strobe** may be ...

Cited by 133 Related articles All 2 versions

System and method for dynamic **rank** specific timing adjustments for double data rate (DDR) components

DA Thompson, DS McGinnis, JF Zumkehr - US Patent 7,127,584, 2006 - Google Patents

... of whole clock pulse to make gross adjustments between **ranks** within the DDR **memory** ... The DQS_OFFSET parameter represents a fine adjustment for the data **strobe** signal to account for ... For example, **memories** are typically arranged in multiple **ranks** of components, which are ...

Cited by 42 Related articles All 2 versions

Memory-module board layout for use with **memory** chips of different data widths

HHD Nguyen, M Burlington - US Patent 7,414,312, 2008 - Google Patents

... Additional chip-selects or module-selects could be used, and the **memory** module could have 3 or ... select, other signals could be used such as an address or a data **strobe** signal. Some **memories** may have more than one chip select input, and some combination of these chip ...

Cited by 76 Related articles All 2 versions

Write clock and data window tuning based on **rank** select

PA LaBerge, J Dodd - US Patent 6,804,764, 2004 - Google Patents

... 00—Interconnection of, or transfer of information or other signals between, **memories**, input/output ... synchronous." Source synchronous systems deliver data along with a clock or **strobe** signal on the ... computer **memory** sub-system with multiple slots or **ranks** of **memory**, each **rank** ...

Cited by 204 Related articles All 2 versions

Memory technology test apparatus

JM Jeddeloh - US Patent 7,020,815, 2006 - Google Patents

... These **memories** differ from conventional **memory** systems, which rely on the system clock to latch ... In one embodiment, the **strobe** is edge-aligned with data for reads and center ... The **memory** interface 122 provides the physical interface for clocks, data masks, **strobes**, **rank** selects ...

Cited by 16 Related articles All 2 versions

Circuit for providing chip-select signals to a plurality of **ranks** of a DDR **memory** module

JR Bhakta, JC Solomon - US Patent 8,081,537, 2011 - Google Patents

... FIG. 3A schematically illustrates an exemplary **memory** module which doubles number of **ranks** in accordance with certain embodiments described herein. FIG ... FIG. 5 shows an exemplary timing diagram in which the last data **strobe** of **memory** device "a" collides with the pre ...

Cited by 40 Related articles All 3 versions

Circuit for providing chip-select signals to a plurality of **ranks** of a DDR **memory** module

JR Bhakta, JC Solomon - US Patent 8,081,535, 2011 - Google Patents

... FIG. 3A schematically illustrates an exemplary **memory** module which doubles number of **ranks** in accordance with certain embodiments described herein. FIG ... FIG. 5 shows an exemplary timing diagram in which the last data **strobe** of **memory** device "a" collides with the pre ...

Cited by 37 Related articles All 3 versions

Multi-**rank** partial width **memory** modules

SN Rajan, MJS Smith - US Patent 8,130,560, 2012 - Google Patents

Connect public, paid and private patent data with Google Patents Public Datasets Multi-**rank** partial width **memory** modules. Download PDF Info. Publication number US8130560B1. Authority US Grant status Grant. Patent type …

Cited by 53 Related articles All 3 versions

On-die termination snooping for 2T applications in a **memory** system implementing non-self-terminating ODT schemes

PA LaBerge - US Patent 7,516,281, 2009 - Google Patents

… G06F13/00—Interconnection of, or transfer of information or other signals between, **memories**, input/output … Data which is to be read from the **memory** arrays 22 is output through the I/O … The data **strobe** generator 32 is operable to produce data **strobes** for upper and lower bytes …

Cited by 47 Related articles All 2 versions

Related searches

ranks **of a ddr** memory **module**

multi-rank **partial width** memory **modules**

multi-rank **dual inline** memory **module**

multi-rank memory **module**

Google 1 2 3 4 5 6 7 8 9 10 Next

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 16, 2019*	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	1	of	3	Attorney Docket Number	***129980-5023-US***

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.[1]	Document Number Number - Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		9,606,907 B2	03-28-2017	Lee et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code[3] – Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

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		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Xilinx Xilinx CS280 package datasheet (1999), filed December 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Demonstratives, filed February 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Supplemental Mandatory Notices, filed April 19, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing 4:1 MUX/DeMUX and 4 ranks of memory (corrected Ex. 1035), filed February 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Deposition Transcript of R. Jacob Baker (Jan. 12, 2018), filed February 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Objections to Evidence, filed February 13, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Request for Oral Argument, filed February 28, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Deposition of Carl Sechen, Ph.D. taken December 8, 2017, filed February 26, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Deposition of Carl Sechen, Ph.D. taken February 8, 2018, filed February 26, 2018
		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Objections to Evidence, filed March 5, 2018

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/29/2019

DB2/ 35761840.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 16, 2019*	
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				Art Unit	*2139*
				Examiner Name	*Bansal, Gurtej*
Sheet	2	of	3	Attorney Docket Number	*129980-5023-US*

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		Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Hearing Transcript, filed April 24, 2018
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		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Objections to Evidence, filed November 14, 2017
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Notice of Deposition of Carl Sechen, filed January 30, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Supplemental Objections to Evidence, filed February 15, 2018
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Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/29/2019

DB2/ 35761840.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 16, 2019*	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	3	of	3	Attorney Docket Number	***129980-5023-US***

		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Submission on Propriety of Petitioner's Reply, filed March 20, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Response to Patent Owner's Submission on Propriety of Petitioner's Reply and Supplemental Stone Declaration, filed March 27, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Response to Patent Owner's Motion for Observations, filed April 2, 2018
		Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Hearing Transcript, filed April 24, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petition, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Preliminary Response, filed April 10, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Decision Granting Institution of Inter Partes Review, entered June 29, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Petition, filed December 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Petitioner's Power of Attorney, filed December 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, File History of U.S. Patent No.9606907, filed December 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Declaration of Dr. Harold Stone, filed December 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Curriculum Vitae of Dr. Harold Stone, filed December 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Patent Owner's Preliminary Response, filed May 7, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Decision Granting Institution of Inter Partes Review, entered August 6, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00365, Petition, filed December 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00365, Patent Owner's Preliminary Response, filed December 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00365, Decision Granting Institution of Inter Partes Review, entered August 6, 2018

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/29/2019

DB2/ 35761840.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	3717	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2011/07/03 21:54
S2	75	365/189.2.ccls.	USPAT	OR	OFF	2011/07/03 21:54
S3	104	365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:27
S4	6392	abstract$3 with (DRAM DIMM memory)	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:40
S5	48	abstracted adj2 (DRAM DIMM memory)	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:40
S6	109	abstracted adj2 (DRAM DIMM memory) or aDRAM	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:42
S7	1	"7515453".pn.	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:00
S8	771	interface same (DDR2 and (DDR or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:17
S9	504	interface with (DDR2 and (DDR or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:18
S10	5	365/189.2.ccls. and (DDR2 and (DDR or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:19
S11	10	365/189.2.ccls. and (DDR and (DDR2 or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:24
S12	1	"20070088995".pn.	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:29
S13	241	CKE with precharge	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:48
S14	0	365/189.2.ccls and CKE with precharge	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:48
S15	111	CKE with precharge same power	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:48
S16	36	silent with alarm with clock	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:54
S17	0	silent with alarm with clock and lark.in.	US-	OR	OFF	2011/07/05

			PGPUB; USPAT			21:54
S18	0	silent with alarm with clock and hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:54
S19	4	alarm with clock and hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:55
S20	0	julia-hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:58
S21	2	julia.in. and hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:59
S22	16	lark.as.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:00
S23	629	precharge same power and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:01
S24	3	precharge same power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:03
S25	1	self with refresh and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:08
S26	3	pre$1charge with power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:09
S27	11	pre$1chargesame power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:09
S28	3	pre$1charge same power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:09
S29	55	pre$1charge same power and CKE and DRAM same DDR same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:22
S30	59	pre$1charge same power and CKE and DRAM same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:25
S31	73	pre$1charge same power and CKE and DDR same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:26
S32	89	refresh same power and CKE and DDR same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:17
S33	10	365/189.2.ccls. and (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:27
S34	54	SPD and (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:29
S35	16	SPD same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:29
S36	0	module with transmit same (pre$1charge	US-	OR	OFF	2011/07/06

		refresh) and CKE	PGPUB; USPAT			00:45
S37	19	memory with transmit same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:45
S38	23	configure same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:48
S39	14	configure with (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:48
S40	1	DDR with DRAM and tCKE with timing with memory	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:52
S41	273	intelligent adj3 (buffer or register)	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:01
S42	9	intelligent adj3 (buffer or register) and pre$charge	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:01
S43	298	SPD same2 (pre$1charge refresh)	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:03
S44	197	SPD same (pre$1charge refresh)	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:03
S45	59	SPD same2 (pre$1charge refresh) and DDR same DRAM	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:03
S46	38	SPD same (pre$1charge refresh) and DDR same DRAM	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:04
S47	3	SPD same (pre$1charge refresh) and DDR same DRAM and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:05
S48	59	SPD same2 (pre$1charge refresh) and DDR same DRAM	US-PGPUB; USPAT	OR	OFF	2011/07/06 10:59
S49	1	SPD same pre$1charge with power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:01
S50	25	SPD same self adj refresh	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:01
S51	0	SPD same self adj refresh and DDR	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:04
S52	2	SPD same self adj refresh and DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:04
S53	22	SPD same self adj refresh same power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:07
S54	2	SPD same self adj refresh and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:24
S55	0	SPD same self adj refresh and tCKE	US-	OR	OFF	2011/07/06

			PGPUB; USPAT			11:26
S56	0	SPD same pre$1charge and tCKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:27
S57	2617837	SPD swith power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:29
S58	578	SPD with power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:29
S59	16	SPD with power same (self adj refresh self$1refresh pre adj charge pre$charge)	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:30
S60	21	SPD same self adj refresh and (pre$1charge or pre adj charge)	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:37
S61	1	"20050246558".pn.	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:41
S62	2	SPD same power with management with mode	US-PGPUB; USPAT	OR	OFF	2011/07/06 12:40
S63	13	365/189.2.ccls. and CS	USPAT	OR	OFF	2011/07/06 12:55
S64	21	365/189.2.ccls. and CS	US-PGPUB; USPAT	OR	OFF	2011/07/06 12:55
S65	171	DIMM same CS	US-PGPUB; USPAT	OR	OFF	2011/07/06 13:00
S66	53	365/189.2.ccls. and (tRP tRCD TWL tRFC timing tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:34
S67	7	365/189.2.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:34
S68	1631	"365".clas. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S69	0	365/189.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S70	446	365/189.$.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S71	36	365/189.$.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR) and DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S72	1	365/189.$.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR) same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:37
S73	3	burst with plurality with DIMM	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:43
S74	0	burst with each with DIMM	US-PGPUB;	OR	OFF	2011/07/06 14:44

			USPAT			
S75	6	burst with multiple with DIMM	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:44
S76	6	burst with multiple with DIMM and read	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:46
S77	5	burst with multiple with DIMM same read	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:47
S78	11	burst with DIMMs same read	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:47
S79	0	365/189.2.ccls. and CKE with (high and low)	USPAT	OR	OFF	2011/07/06 16:19
S80	529	CKE with (high and low)	USPAT	OR	OFF	2011/07/06 16:20
S81	17	CKE with (high and low) and DDR2	USPAT	OR	OFF	2011/07/06 16:20
S82	0	365/189.2.ccls. and CKE with (high and low)	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:20
S83	44	CKE with (high and low) and DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:21
S84	87	CKE with (high and low) same pre$1charge	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:24
S85	0	CKE with (high and low) same pre$1charge same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:24
S86	0	CKE with (high and low) same self adj refresh same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:25
S87	0	CKE with ((high and low) or assert) same self adj refresh same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:25
S88	0	CKE with ((high and low) or assert) same pre$1fetch same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:25
S89	0	CKE with (high or low or assert) same pre$1fetch same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:26
S90	0	CKE with (high or low or assert) same pre$1fetch same2 SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:26
S91	2	CKE with (high or low or assert) same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:26
S92	10	SPD same2 CKE with (high or low or assert)	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:27
S93	1	"20090216936".pn.	US-PGPUB; USPAT	OR	OFF	2012/01/20 18:08
S94	1	"20090216939".pn.	US-	OR	OFF	2012/01/20

			PGPUB; USPAT			18:17
S95	152	buffer with DRAM with protocol	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:25
S96	152	buffer$3 with DRAM with protocol	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:37
S97	572	buffer with $1RAM with protocol	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:38
S98	1	"20030131160".pn.	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:47
S99	1729	buffer with $1RAM with (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:48
S100	626	buffer with DRAM with (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:48
S101	124	buffer with chip with DRAM with (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:51
S102	185	buffer near5 DRAM near5 (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:14
S103	499	buffer with DRAM with type	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:18
S104	51	buffer with DRAM with type with (multiple different tim$3 various)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:19
S105	224	buffer with DRAM with DDR	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:21
S106	3	buffer with DRAM with (timing signal) with adjust	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:32
S107	146	buffer with DRAM with (timing signal) with delay	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:32
S108	31	buffer with DRAM with (timing signal) with DDR$1	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:32
S109	70	buffer with DRAM with (timing signal protocol) and buffer with DDR$1 with (timing signal protocol)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:37
S110	118	buffer with DRAM with (timing signal protocol) and buffer with SDRAM with (timing signal protocol)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:48
S111	36	buffer with DRAM with SDRAM with interface	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:52
S112	48	buffer with DRAM with (SDRAM DDR2 DDR3) with interface	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:52
S113	73	interface with buffer with DRAM with	US-	OR	OFF	2012/01/21

		(DDR$1 SDRAM)	PGPUB; USPAT			02:03
S114	141	interface same buffer with DRAM with (DDR$1 SDRAM)	US-PGPUB; USPAT	OR	OFF	2012/01/21 02:10
S115	2	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/15 14:11
S116	64	DIMM with DRAM and CS with (DIMM DRAM) and buffer with (DIMM DRAM)	US-PGPUB; USPAT	OR	OFF	2013/01/15 14:12
S117	1	"5918229".pn.	US-PGPUB; USPAT	OR	OFF	2013/01/18 14:08
S118	1	"20060184942".pn.	US-PGPUB; USPAT	OR	OFF	2013/01/18 14:35
S119	130	(different multiple distinct) with file adj locking	US-PGPUB; USPAT	OR	OFF	2013/01/18 17:46
S120	0	abstracted with DIMM and DRAM	USPAT	OR	OFF	2013/01/21 13:21
S121	0	abstracted with DIMM	USPAT	OR	OFF	2013/01/21 13:21
S122	2	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 13:21
S123	56	US-5278796-$.DID. OR US-5282177-$.DID. OR US-5384745-$.DID. OR US-1241995-$.DID. OR US-5388265-$.DID. OR US-5467455-$.DID. OR US-5498886-$.DID. OR US-5598376-$.DID. OR US-5610864-$.DID. OR US-5675549-$.DID. OR US-5692202-$.DID. OR US-5706247-$.DID. OR US-5757703-$.DID. OR US-5949254-$.DID. OR US-6034916-$.DID. OR US-6034918-$.DID. OR US-6035365-$.DID. OR US-6330683-$.DID. OR US-6631086-$.DID. OR US-6754129-$.DID. OR US-6970968-$.DID. OR US-20030002262-$.DID. OR US-20040196732-$.DID. OR US-20050149662-$.DID. OR US-7172005-$.DID. OR US-20050259504-$.DID. OR US-20080025108-$.DID. OR US-20080025136-$.DID. OR US-5241266-$.DID. OR US-5843799-$.DID. OR US-5966727-$.DID. OR US-20060026484-$.DID. OR US-20080239858-$.DID. OR US-20080115006-$.DID. OR US-20070288686-$.DID. OR US-7120727-$.DID. OR US-7472220-$.DID. OR US-6317352-$.DID. OR US-6317381-$.DID. OR US-20010019509-$.DID. OR US-3800292-$.DID. OR US-4069452-$.DID. OR US-4323965-$.DID. OR US-4334307-$.DID. OR US-4345319-$.DID. OR US-4392212-$.DID. OR US-4525921-$.DID. OR US-4566082-$.DID. OR US-4646128-$.DID. OR US-4592019-$.DID. OR US-	US-PGPUB; USPAT	OR	OFF	2013/01/21 17:23

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S136	2185	DRAM with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:35
S137	31	DRAM with DIMM and DIMM with virtual$5	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:35
S138	43	DRAM with DIMM and CS with module	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:39
S139	43	virtual with DIMM and DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:49
S140	57	buffer with CS and DIMM with DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:16
S141	2	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:22
S142	37	virtual$5 near3 DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:22
S143	29	virtual$5 near3 DIMM and DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:22
S144	541	(plurality multiple) with DIMM with single	US-PGPUB; USPAT	OR	ON	2013/01/21 23:25
S145	200	(plurality multiple) near3 DIMM with single	US-PGPUB; USPAT	OR	ON	2013/01/21 23:25
S146	170	(plurality multiple) near3 DIMM with single and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/21 23:25
S147	132	logical with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/21 23:35
S148	112	logical with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/21 23:35
S149	334	(group) with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/22 00:47
S150	55	emulat$3 with DIMM and DRAM	US-	OR	ON	2013/01/22

			PGPUB; USPAT			00:52
S151	71	virtual with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/22 09:39
S152	10	(plurality multiple) with virtual with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/22 09:40
S153	47	(plurality multiple) with (virtual logical emulat$3) with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/22 09:40
S154	1	"7133960".pn.	US-PGPUB; USPAT	OR	ON	2013/01/22 09:42
S155	17	rank with (appear$3) with DIMM	USPAT	OR	OFF	2013/01/30 13:21
S159	180	(virtual logical abstract$3) with DIMM	US-PGPUB; USPAT	OR	ON	2013/02/18 23:49
S160	22	(virtual logical abstract$3) adj DIMM	US-PGPUB; USPAT	OR	ON	2013/02/18 23:49
S161	344	(virtual logical abstract$3) adj RAM	US-PGPUB; USPAT	OR	ON	2013/02/19 00:01
S162	98	(virtual logical abstract$3) adj DRAM	US-PGPUB; USPAT	OR	ON	2013/02/19 00:01
S168	2	"201100052062".pn. "5910010".pn. "5222014".pn.	US-PGPUB; USPAT	OR	OFF	2013/04/16 23:55
S169	18	US-20030110339-$.DID. OR US-20030174569-$.DID. OR US-20040049624-$.DID. OR US-20050044302-$.DID. OR US-20060277355-$.DID. OR US-20080130364-$.DID. OR US-20080282084-$.DID. OR US-20080282341-$.DID. OR US-20090049266-$.DID. OR US-20090070520-$.DID. OR US-20090063865-$.DID. OR US-20090063896-$.DID. OR US-20090089480-$.DID. OR US-6047361-$.DID. OR WO-199725674-$.DID. OR KR-2005120344-$.DID. OR US-3201318-$.DID. OR KR-1020087019582-$.DID. OR US-1201321-$.DID. OR US-6201324-$.DID. OR US-4201331-$.DID. OR US-9201340-$.DID. OR US-182013D-$.DID.	US-PGPUB; USPAT	OR	OFF	2013/07/24 15:48
S170	105	(virtual logical abstract$3) adj DRAM	US-PGPUB; USPAT	OR	ON	2013/07/24 15:59
S171	60	emulat$3 with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/07/24 15:59
S172	4337	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/07/24 16:02

S173	3	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/07/24 16:04
S178	1054	buffer with data with CS	US-PGPUB; USPAT	OR	OFF	2017/04/26 15:45
S179	1637	buffer with DIMM	US-PGPUB; USPAT	OR	OFF	2017/04/26 15:49
S180	100	buffer and fan$4 with (rank dimm)	US-PGPUB; USPAT	OR	OFF	2017/04/26 16:14
S181	249	buffer same parallel with (rank dimm)	US-PGPUB; USPAT	OR	OFF	2017/04/26 16:26
S182	112	buffer same parallel with (ranks dimms)	US-PGPUB; USPAT	OR	OFF	2017/04/26 16:26
S183	60	daisy with chain with DIMM same buffer	US-PGPUB; USPAT	OR	OFF	2017/04/27 00:11
S184	9041	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	US-PGPUB; USPAT	OR	OFF	2017/04/30 15:23
S189	1	bust with rank$1 with select$3	US-PGPUB; USPAT	OR	OFF	2017/08/17 00:07
S190	38	burst with rank$1 with select$3	US-PGPUB; USPAT	OR	OFF	2017/08/17 00:07
S191	38	burst with rank with select$3	US-PGPUB; USPAT	OR	ON	2017/08/17 08:16
S192	141	burst same rank$1 same select$3	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:16
S193	113	buffer same parallel with (ranks dimms)	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:34
S194	5288	G06F13/1673.cpc. G011C7/1072.cpc. G011C15/00.cpc. G06F13/4282.cpc. G06F13/4243.cpc.	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:36
S195	299	DIMM same CS	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:46
S196	322	DIMM same (CS chip$1select)	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:46
S197	83	DIMM with DRAM and CS with (DIMM) and buffer with (DIMM DRAM)	US-PGPUB; USPAT	OR	OFF	2017/08/17 09:29
S198	195	DIMM with rank with select$3	US-PGPUB; USPAT	OR	OFF	2017/08/17 10:08
S200	35	DIMM same rank same burst	US-PGPUB; USPAT	OR	OFF	2017/08/17 15:23

S204	69	ranks same dimm same strobe	US-PGPUB; USPAT	OR	OFF	2018/09/27 12:55
S205	154	ranks same dimm same strobe	US-PGPUB; USPAT	OR	ON	2018/09/27 12:55
S206	150	(virtual logical abstract$3) adj DRAM	US-PGPUB; USPAT	OR	ON	2018/09/27 13:51
S207	355	DIMM same (CS chip$1select)	US-PGPUB; USPAT	OR	OFF	2018/09/27 14:01
S208	153	greater with CAS with latency	US-PGPUB; USPAT	OR	OFF	2018/09/27 20:45
S209	1	greater with CAS with latency with actual	US-PGPUB; USPAT	OR	OFF	2018/09/27 20:46
S210	375	(great$3 increas$3) with CAS with latency	US-PGPUB; USPAT	OR	OFF	2018/09/27 21:32
S211	7	(great$3 increas$3) with CAS with latency same DIMM	US-PGPUB; USPAT	OR	OFF	2018/09/27 21:32
S212	11706	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc.	US-PGPUB; USPAT	OR	OFF	2018/09/27 21:56
S216	210	virtual with DIMM	US-PGPUB; USPAT	OR	ON	2019/03/29 16:20
S217	7	(great$3 increas$3) with CAS with latency same DIMM	US-PGPUB; USPAT	OR	OFF	2019/03/29 19:38

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	5558	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc.	USPAT	OR	OFF	2019/03/31 13:43
L2	0	strobes.clm. and ranks.clm. and bits.clm.	USPAT	OR	OFF	2019/03/31 13:43
L3	0	L1 and L2	USPAT	OR	OFF	2019/03/31 13:43
S156	4194	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/01/30 13:35
S157	1321	emulated.clm.	USPAT	OR	OFF	2013/01/30 13:45
S158	3	S156 and S157	USPAT	OR	OFF	2013/01/30 13:45
S163	4205	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/02/19 00:04
S164	1330	emulated.clm.	USPAT	OR	OFF	2013/02/19 00:04
S165	4205	711/5.ccls. 711/105.ccls. 711/167.ccls.	USPAT	OR	OFF	2013/02/19

		365/189.2.ccls.				00:04
S166	1330	emulated.clm.	USPAT	OR	OFF	2013/02/19 00:04
S167	3	S165 and S166	USPAT	OR	OFF	2013/02/19 00:04
S174	4343	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/07/24 16:04
S175	4343	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/07/24 16:06
S176	1399	emulated.clm.	USPAT	OR	OFF	2013/07/24 16:06
S177	4	S175 and S176	USPAT	OR	OFF	2013/07/24 16:06
S185	4964	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	USPAT	OR	OFF	2017/04/30 15:24
S186	6228	data.clm. adj path.clm.	USPAT	OR	OFF	2017/04/30 15:28
S187	120	S185 and S186	USPAT	OR	OFF	2017/04/30 15:28
S188	8	S185 and S186 and rank.clm.	USPAT	OR	OFF	2017/04/30 15:28
S199	5127	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	USPAT	OR	OFF	2017/08/17 10:17
S201	5127	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	USPAT	OR	OFF	2017/08/17 15:22
S202	0	S201 and buffer.clm. and rank.clm. and burst.clm.	USPAT	OR	OFF	2017/08/17 15:22
S203	8	DIMM with rank with selection	USPAT	OR	OFF	2017/08/17 15:23
S213	4948	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc.	USPAT	OR	OFF	2018/09/27 23:32
S214	0	strobes.clm. and ranks.clm. and bits.clm.	USPAT	OR	OFF	2018/09/27 23:33
S215	0	S213 and S214	USPAT	OR	OFF	2018/09/27 23:33

3/31/2019 1:43:47 PM
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 16, 2019*	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	1	of	3	Attorney Docket Number	***129980-5023-US***

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.[1]	Document Number Number - Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		7,334,150 B2	02-19-2008	Ruckerbauer et al.	

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Examiner Initials	Cite No.	Foreign Patent Document Country Code[3] – Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petition, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Declaration of Dr. Harold Stone, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1022, Decision Denying Institution of Inter Partes Review, entered December 16, 2014
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1023, Decision Denying Institution of Inter Partes Review, entered March 9, 2015
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1024, Excepts from the Hearing in Certain Memory Modules and Components Thereof, and Products Containing Same, filed May 8, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1025, Complainant Netlist, Inc., Initial Post-Hearing Brief , filed May 30, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1026, Respondents' Post-Hearing Brief , filed May 30, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1027, Demonstrative-Graphics-from-hynix-post-hearing-brief, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1028, Netlist-reply-post-hearing-brief, filed December 22, 2017

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/29/2019

DB2/ 35764686.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 16, 2019*	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	2	of	3	Attorney Docket Number	***129980-5023-US***

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1029, Respondent's Reply Post-Hearing Brief, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1030, High-Quality Versions of Demonstrative-Graphics-from-hynix-reply-post-hearing-brief, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1031, Institution of the '185 patent, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1032, Final Written Decision, Diablo Techs., Inc v. Netlist Inc., Paper No. 33, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1033, Decision, Netlist Inc., v. Diablo Techs., Inc., filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1034, Netlist's Infringement Claim Chart of , filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1035, Stone, H.S. Microcomputer Interfacing, Reading, MA Addison Wesley, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1039, Intel E7525 Memory Controller Hub (MCH) Chipset Datasheet, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1040, Initial Determination, Certain Memory Modules and Components Thereof, and Products Containing Same, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1041, MEMORY-SYSTEMS-Cache-DRAM-Disk, Bruce Jacobs et al., filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1042, Direct DRAM Datasheet, Bruce Jacobs et al., filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Notice of Accorded Filing Date, filed January 10, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Preliminary Response, filed April 10, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Granting Institution of Inter Partes Review, entered June 29, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Objection to Petition Evidence, filed July 16, 2018

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/29/2019

DB2/ 35764686.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 16, 2019*	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	3	of	3	Attorney Docket Number	***129980-5023-US***

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Order 37 C.F.R. 42.5, filed August 2, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Mehran Arjomand,' filed July 30, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Michael D. Hatcher,' filed July 30, 2018

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/29/2019

DB2/ 35764686.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				***Electronically filed April 17, 2019***	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	1	of	3	Attorney Docket Number	***129980-5023-US***

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.[1]	Document Number Number - Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code[3] – Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1044, 'Deposition Transcript of R. Jacob Baker (Jan. 26, 2019),' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1045, 'Deposition Transcript of R. Jacob Baker (Jan. 12, 2018) in IPR2017-00577 concerning the parent to the '907 Patent,' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1047, 'Certified translation of the Examination Decision issued by the State Intellectual Property Office of the P.R.C. (dated 5/30/18),' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Reply to Patent Owner's Response, filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1043, 'Chart comparing text in Dr. Baker's declaration [Ex. 2002] with identical text in Patent Owner's Response [Paper No. 14],' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1046, 'Final Office Action concerning U.S. Patent Application No. 15/470,856 (dated 7/27/18),' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1048, 'Certified translation of the Preliminary Opinion issued by the German Patent and Trademark Office (dated 1/8/19),' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Request for Oral Argument, filed February 19, 2019

Examiner Signature		Date Considered	

DB2/ 36282888.1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed April 17, 2019*	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	2	of	3	Attorney Docket Number	***129980-5023-US***

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Objections To Reply Evidence, filed February 19, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Request For Oral Argument, filed February 19, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Motion To Exclude, filed February 19, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Corrected Petitioners' Reply to Patent Owner's Response, filed February 20, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Opposition to Patent Owner's Motion to Exclude, filed March 5, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Sur-Reply To Petitioner's Corrected Reply, filed March 8, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Reply To Petitioner's Opposition To Motion To Exclude, filed March 12, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 3002, 'Patent Owner's Request for Sur Reply,' filed March 1, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Order - Trial Hearing, filed March 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1043, 'Deposition Transcript of R. Jacob Baker (Feb. 9, 2019),' filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1044, 'Declaration of R. Jacob Baker in IPR2017-00577 concerning the parent to the '907 Patent (Oct. 25, 2017),' filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1045, 'Deposition Transcript of R. Jacob Baker in IPR2017-00577 concerning the parent to the '907 Patent (Jan. 12, 2018),' filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1046, 'Final Written Decision in IPR2017-00577 invalidating all challenged claims to the parent to the '907 Patent (July 5, 2018),' filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1048, 'U.S. Patent No. 7,133,960,' filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Reply to Patent Owner's Response, filed February 22, 2019

Examiner Signature		Date Considered	

DB2/ 36282888.1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				***Electronically filed April 17, 2019***	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	3	of	3	Attorney Docket Number	***129980-5023-US***

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Objections To Reply Evidence, filed March 1, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Request for Oral Argument, filed March 4, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Request For Oral Argument, filed March 4, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Motion To Exclude, filed March 4, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Opposition to Patent Owner's Motion to Exclude, filed March 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Sur-Reply To Petitioner's Reply, filed March 15, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Reply To Petitioner's Opposition To Motion To Exclude, filed March18, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Order, Trial Hearing, filed March 22, 2019

Examiner Signature		Date Considered	

Electronic Patent Application Fee Transmittal	
Application Number:	15857519
Filing Date:	28-Dec-2017
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Filer:	Jamie Jie Zheng/Edith Fuentes
Attorney Docket Number:	129980-5023US
Filed as Large Entity	

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	240	240
		Total in USD ($)		**240**

Electronic Acknowledgement Receipt	
EFS ID:	35759083
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/Edith Fuentes
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023US
Receipt Date:	17-APR-2019
Filing Date:	28-DEC-2017
Time Stamp:	20:51:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$240
RAM confirmation Number	041819INTEFSW00006453500310
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	IPR2018-00362_EXHIBITS_1044_Deposition_Transcript_of_R_Jacob_Baker_2019FEB11-.pdf	8446617 77e29a059a6e4841b2821e1be925dafa84532e53	no	212
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2	Non Patent Literature	IPR2018-00362_EXHIBITS_1045_Deposition_Transcript_of_R_Jacob_Baker-.pdf	12015889 0bff85400c8950d85d5d55ad6b073858e144de79	no	264
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3	Non Patent Literature	IPR2018-00362_EXHIBITS_1047_Certified_translation_of_the_Examination.pdf	10386527 8320ca684efa47e5c5e6722befdff72e7f19a67d	no	22
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5	Non Patent Literature	IPR2018-00362_EXHIBITS_1043_Chart_comparing_text_in_Dr_Bakers.pdf	15737824 ca17762e06e4bb545725877bf53b3eb07c95ca15	no	29
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6	Non Patent Literature	IPR2018-00362_EXHIBITS_1046_Final_Office_Action_7_27_18.pdf	2742762 e395aafe5dce61fe05c51772ed33a6b6a24ae8dc	no	51
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7	Non Patent Literature	IPR2018-00362_EXHIBITS_1048_Certified_translation_of_the_Preliminary_Opinion.pdf	5463098 0a1e4376e727097faec7050ce3ba49068fcf2e88	no	10
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8	Non Patent Literature	IPR2018-00362_Petitioners_Request_for_Oral_Argument_2019FEB19.pdf	614581 3f795727760ce67d69d50cc806bb03dba1ea8378	no	4
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9	Non Patent Literature	IPR2018-00362_Patent_Owner_Objections_To_Reply_Evidence_2019FEB19.pdf	1407134 9312e7d353e7c92838f1d3ae5d4b5cc07c77ccac	no	6
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11	Non Patent Literature	IPR2018-00362_Patent_Owner_Motion_To_Exclude_2019FEB19.pdf	4618914 92e19ae21b7d52ad8a9a35b27bbe0637ff88ae11	no	17
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12	Non Patent Literature	IPR2018-00362_Corrected_Petitioners_Reply_to_Patent_Owners_Response_2019FEB20.pdf	10602824 86152696a048bda14c91c2cab7a304aeb2713463	no	62
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13	Non Patent Literature	IPR2018-00362_Petitioners_Opposition_to_Patent_Owners_Motion_to_Exclude_2019MAR5.pdf	5419069 44e378a0ba1a734def29307f3195172bd99b7fe9	no	19
Warnings:					
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14	Non Patent Literature	IPR2018-00362_Patent_Owners_Sur-Reply_To_Petitioners_Corrected_Reply_2019MAR8.pdf	2319854 715bb6807f448fe4ca3190c398dcca897e0249cb	no	10
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16	Non Patent Literature	IPR2018-00362_EXHIBITS_3002_Patent-Owners-Request-for-Sur-Reply.pdf	1725122 be8c358e42feca1a812c13ffb5fb30b5e5d69ec3	no	5
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17	Non Patent Literature	IPR2018-00362_Order_Trial_Hearing_2019MAR22.pdf	951936 0ff2a8e11d12ebd08f895e6f309439980d2eca1e	no	4
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Information:					
18	Non Patent Literature	IPR2018-00363_EXHIBITS_1043_Deposition_Transcript_of_R_Jacob_Baker-.pdf	4592765 e9072c499d09014ba58d9d52b4ac0a19b80918d1	no	118
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Information:					
19	Non Patent Literature	IPR2018-00363_EXHIBITS_1044_Declaration_of_R_Jacob_Baker-.pdf	5188350 93d348f304a324d9fd0c5421fc48d853f56b17bc	no	104
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20	Non Patent Literature	IPR2018-00363_EXHIBITS_1045_Deposition_Transcript_of_R_Jacob_Baker-.pdf	11519730 5f4d9c5a4dd2b18cf6be5e23d6f4438295e09b25	no	266
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21	Non Patent Literature	IPR2018-00363_EXHIBITS_1046_Final_Written_Decision.pdf	14852137 162af07007b579396de6d94405ef9c6ad46a50e4	no	41
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22	Non Patent Literature	IPR2018-00363_EXHIBITS_1048_US_Patent_No_7133960.pdf	593133 deff3f807e66c8c73bc99b1283ef89df1efbcbe1	no	8
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23	Non Patent Literature	IPR2018-00363_Petitioners_Reply_to_Patent_Owners_Response_filed_2019FEB22.pdf	14209501 a5448cee9aa9dc8ad6312096fb93da7f4bf81061	no	47
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24	Non Patent Literature	IPR2018-00363_Patent_Owners_Objections_To_Reply_Evidence_filed_2019MAR1.pdf	1572980 711bbe92af8c9118f8f9331c723ab08c018ebe76	no	7
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25	Non Patent Literature	IPR2018-00363_Petitioners_Request_for_Oral_Argument_filed_2019MAR4.pdf	611627 391be1bea473e536cda9648c43431827a17b6ea8	no	4
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26	Non Patent Literature	IPR2018-00363_Patent_Owners_Request_For_Oral_Argument_filed_2019MAR4.pdf	842261 f1eaf6be9ac9004fcc0df2f579dd73ab9512d277	no	5
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27	Non Patent Literature	IPR2018-00363_Patent_Owners_Motion_To_Exclude_filed_2019MAR4.pdf	5379502 8396b4e52a4404d352a2d083eaf0cf3a56c45bee	no	20
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28	Non Patent Literature	IPR2018-00363_Petitioners_Opposition_to_Patent_Owners_Motion_to_Exclude_filed_2019MAR11.pdf	6406131 f74a417bc69eef03401582f8fa5ec1b3a2886061	no	21
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31	Non Patent Literature	IPR2018-00363_Order-Trial_Hearing_filed_2019MAR22-.pdf	133213 84084968d3059cea47db77d4c4785e7e57d41efa	no	4
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32		129980-5023US_IDS.pdf	342130 82b73a685ab2e3c321461ab7922a717b4614c3cd	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
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	Information Disclosure Statement (IDS) Form (SB08)	5	7

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Warnings:					
Information:					
		Total Files Size (in bytes):	166532496		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed April 17, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Solomon et al.	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	Bansal, Gurtej
For:	MEMORY MODULE WITH DATA BUFFERING	Attorney Docket No.:	129980-5023-US

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☐ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☒ The Certification Statement in Item 5 below is applicable.

4b. ☒ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US).

4c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

5. ☒ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☒ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☐ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☐ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial No. , filed on , of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

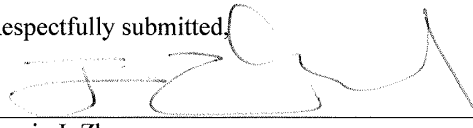
9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: April 17, 2019



51,167

Jamie J. Zheng (Reg. No.)

MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

Petitioners
Ex. 1054, p. 433

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/857,519	12/28/2017	Jefferey C. Solomon	129980-5023US	9826

79141 7590 04/25/2019

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER	
BANSAL, GURTEJ	

ART UNIT	PAPER NUMBER
2139	

NOTIFICATION DATE	DELIVERY MODE
04/25/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

padocketingdepartment@morganlewis.com
vskliba@morganlewis.com

UNITED STATES DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR/ PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
15/857,519	12/28/2017	Solomon et al.	129980-5023US

	EXAMINER	
Morgan, Lewis & Bockius LLP (PA)(J. Zheng) 1400 Page Mill Road Palo Alto, CA 94304	GURTEJ BANSAL	
	ART UNIT	PAPER
	2139	20190420

DATE MAILED: _____

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

IDS dated 04/17/2019 has not been considered. Applicant has indicated a replacement IDS will be submitted with an RCE and therefore asked the Examiner not to consider the references in the IDS dated 04/17/2019

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

PTO-90C (Rev.04-03)

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed April 17, 2019*	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	1	of	3	Attorney Docket Number	***129980-5023-US***

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.[1]	Document Number Number - Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code[3] – Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1044, 'Deposition Transcript of R. Jacob Baker (Jan. 26, 2019),' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1045, 'Deposition Transcript of R. Jacob Baker (Jan. 12, 2018) in IPR2017-00577 concerning the parent to the '907 Patent,' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1047, 'Certified translation of the Examination Decision issued by the State Intellectual Property Office of the P.R.C. (dated 5/30/18),' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Reply to Patent Owner's Response, filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1043, 'Chart comparing text in Dr. Baker's declaration [Ex. 2002] with identical text in Patent Owner's Response [Paper No. 14],' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1046, 'Final Office Action concerning U.S. Patent Application No. 15/470,856 (dated 7/27/18),' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1048, 'Certified translation of the Preliminary Opinion issued by the German Patent and Trademark Office (dated 1/8/19),' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Request for Oral Argument, filed February 19, 2019

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed April 17, 2019*	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	2	of	3	Attorney Docket Number	***129980-5023-US***

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Objections To Reply Evidence, filed February 19, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Request For Oral Argument, filed February 19, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Motion To Exclude, filed February 19, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Corrected Petitioners' Reply to Patent Owner's Response, filed February 20, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Opposition to Patent Owner's Motion to Exclude, filed March 5, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Sur-Reply To Petitioner's Corrected Reply, filed March 8, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Reply To Petitioner's Opposition To Motion To Exclude, filed March 12, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 3002, 'Patent Owner's Request for Sur Reply,' filed March 1, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Order - Trial Hearing, filed March 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1043, 'Deposition Transcript of R. Jacob Baker (Feb. 9, 2019),' filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1044, 'Declaration of R. Jacob Baker in IPR2017-00577 concerning the parent to the '907 Patent (Oct. 25, 2017),' filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1045, 'Deposition Transcript of R. Jacob Baker in IPR2017-00577 concerning the parent to the '907 Patent (Jan. 12, 2018),' filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1046, 'Final Written Decision in IPR2017-00577 invalidating all challenged claims to the parent to the '907 Patent (July 5, 2018),' filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1048, 'U.S. Patent No. 7,133,960,' filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Reply to Patent Owner's Response, filed February 22, 2019

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed April 17, 2019*	
				Application Number	***15/857,519***
				Filing Date	***December 28, 2017***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***Bansal, Gurtej***
Sheet	3	of	3	Attorney Docket Number	***129980-5023-US***

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Objections To Reply Evidence, filed March 1, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Request for Oral Argument, filed March 4, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Request For Oral Argument, filed March 4, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Motion To Exclude, filed March 4, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Opposition to Patent Owner's Motion to Exclude, filed March 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Sur-Reply To Petitioner's Reply, filed March 15, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Reply To Petitioner's Opposition To Motion To Exclude, filed March18, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Order, Trial Hearing, filed March 22, 2019

Examiner Signature		Date Considered	

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Address to:
Mail Stop RCE
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Electronically filed	May 17, 2019
Application Number	15/857,519
Filing Date	December 28, 2017
First Named Inventor	Jefferey C. Solomon
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket No.	129980-5023-US

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application. Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application.

1. Submission required under 37 C.F.R. § 1.114

NOTE: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

a. ☐ Previously submitted. If a final Office Action is outstanding, any amendments filed after the final Office Action may be considered as a submission.
   - i. ☐ Request for non-entry of amendment: Please **do not** entered the amendment submitted on _____
   - ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed _____
   - iii. ☐ Other _____

b. ☒ Enclosed
   - i. ☒ Amendment/Reply
   - ii. ☐ Affidavit(s)/Declaration(s)
   - iii. ☒ Information Disclosure Statement (IDS)
   - iv. ☐ Other _____

2. Miscellaneous

a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R. § 1.103(c) for a period of _____ months.
(Period of suspension shall not exceed 3 months; Fee under 37 C.F.R. § 1.17(i) required)

b. ☐ Other _____

3. Fees — The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.

a. ☒ The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US).
   - i. ☐ (1st request) RCE fee required under 37 C.F.R. § 1.17(e)(1), estimated to be $1300 (large entity) or $650 (small entity)
   - ii. ☒ (2nd or subsequent request) RCE fee required under 37 C.F.R. § 1.17(e)(2), estimated to be **$1900 (large entity)** or $950 (small entity)
   - iii. ☐ Extension of time fee required under 37 C.F.R. §§ 1.136 and 1.17, estimated to be $ for a month(s) extension, the request for which is being made herewith
   - iv. ☒ Other Pay for extra claims

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print/Type)	Jamie J. Zheng	*Registration No. (Attorney/Agent)*	51,167
Signature	/Jamie J. Zheng/	*Date*	May 17, 2019

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or by facsimile transmitted to fax no. 1-703- to the U.S. Patent and Trademark Office on the date indicated below.

Name (Print/Type)		*Registration No. (Attorney/Agent)*	
Signature		*Date*	

DB2/ 36573157.1

Electronic Patent Application Fee Transmittal

Application Number:	15857519
Filing Date:	28-Dec-2017
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Filer:	Jamie Jie Zheng/S. Olivier
Attorney Docket Number:	129980-5023US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	5	100	500
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
RCE- 2ND AND SUBSEQUENT REQUEST	1820	1	1900	1900
		Total in USD ($)		**2400**

Electronic Acknowledgement Receipt	
EFS ID:	36026619
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023US
Receipt Date:	17-MAY-2019
Filing Date:	28-DEC-2017
Time Stamp:	19:38:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$2400
RAM confirmation Number	052019INTEFSW00005548500310
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	2008_00362_Exhibit_2001.pdf	3138922 ec343abfd232683b87a644853c291e299b0456af	no	33
Warnings:					
Information:					
2	Non Patent Literature	2018_00362_Exhibit_2004.pdf	2294146 4d18f1610cd306640cd16632d30fa09d2193c64c	no	24
Warnings:					
Information:					
3	Non Patent Literature	Exhibit_2001_Halbert_Fig_4_annotated.pdf	963566 e6d0f71f3dbb9958ee9960162 57f657d56079804	no	2
Warnings:					
Information:					
4	Non Patent Literature	Exhibit_2002.pdf	3773601 a27634a665c9343fe9053f31e241d29c233d047b	no	100
Warnings:					
Information:					
5	Non Patent Literature	Exhibit_2002_Baker_Declaration.pdf	23890899 3f9bd2175c1ef14dd9b6e08455a498108f9e8e62	no	85
Warnings:					
Information:					
6	Non Patent Literature	Exhibit_2003_Deposition_of_Harold_Stone_with_errata.pdf	8299910 667fb6e88279e3deb2c5dbb13e3678a10b49c4f7	no	160
Warnings:					
Information:					

7	Non Patent Literature	Exhibit_2003_Deposition_of_Harold_Stone_with_errata_1.pdf	8131708 af8fe9fc69b2f8919174f6502becf8b20cee0a7	no	160
Warnings:					
Information:					
8	Non Patent Literature	Exhibit_2004_Inter_Partes_Review_ITC.pdf	2160684 2af2a9c4774a92856087b44bde9787bfc803382b	no	24
Warnings:					
Information:					
9	Non Patent Literature	Exhibit_2005_ITC_Claim_Construction_Order.pdf	7298115 26b02e6ca404bcc66c334d75e09171a934a3696f	no	144
Warnings:					
Information:					
10	Non Patent Literature	Exhibit_2006_Deposition_Transcript_R_Jacob_Baker.pdf	11649864 669314faa239aaeea48465f81585e6196ea5b94b	no	266
Warnings:					
Information:					
11	Non Patent Literature	Exhibit_2007_Halbert_Fig_4_annotated_v2.pdf	1253688 c51385a70da1b749447fde2d5a05c823fac92a04	no	1
Warnings:					
Information:					
12	Non Patent Literature	Exhibit_2008_Deposition_of_Harold_S_Stone.pdf	18578968 b84e230bb6b31d5648d0501078974d3d9d259306	no	243
Warnings:					
Information:					
13	Non Patent Literature	Exhibit_2009_Declaration_of_Harold_S_Stone.pdf	5538644 731e8f0adb81b505d93f03724e65d3df86a1dafa	no	109
Warnings:					
Information:					

14	Non Patent Literature	IPR2018_00362_PO_Preliminary_Response.pdf	2848321 acca2f9b0787a827474f01c4ebb33a451c0cb700	no	47
Warnings:					
Information:					
15	Non Patent Literature	Exhibit_2005_ITC_Inter_Partes_Review.pdf	8074477 489819ecf684517fbd2754ef29ac19cdb192c798	no	144
Warnings:					
Information:					
16		129980_5023US_IDS.pdf	288156 15f9d799ef5928c3d4dba0279019ad9b6ca3740d	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Information Disclosure Statement (IDS) Form (SB08)	5	8
	Transmittal Letter	1	4

Warnings:					
Information:					
17		129980_5023US_RCE_AMD.pdf	351215 949bc8ee76ff1ae07d627fa6c6c753114677601f	yes	15

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Applicant Arguments/Remarks Made in an Amendment	15	15
	Claims	3	14
	Preliminary Amendment	2	2
	Request for Continued Examination (RCE)	1	1

Warnings:
This is not a USPTO supplied RCE SB30 form.
Information:

18	Fee Worksheet (SB06)	fee-info.pdf	32294 35127f8b4a753b4fabc54a1ea951222cf421d4de	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	108567178	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed May 17, 2019	
				Application Number	15/857,519
				Filing Date	December 28, 2017
				First Named Inventor	Jefferey C. Solomon
				Art Unit	2139
				Examiner Name	Bansal, Gurtej
Sheet	1	of	4	Attorney Docket Number	129980-5023US

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		7,024,518 B2	04-04-2006	Halbert et al.	
		7334150 B2	02-19-2008	Ruckerbauer et al.	
		2006/0248969 A1	11-09-2006	Seo et al.	

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1044, 'Deposition Transcript of R. Jacob Baker (Jan. 26, 2019),' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1045, 'Deposition Transcript of R. Jacob Baker (Jan. 12, 2018) in IPR2017-00577 concerning the parent to the '907 Patent,' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1047, 'Certified translation of the Examination Decision issued by the State Intellectual Property Office of the P.R.C. (dated 5/30/18),' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Reply to Patent Owner's Response, filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1043, 'Chart comparing text in Dr. Baker's declaration [Ex. 2002] with identical text in Patent Owner's Response [Paper No. 14],' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1046, 'Final Office Action concerning U.S. Patent Application No. 15/470,856 (dated 7/27/18),' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1048, 'Certified translation of the Preliminary Opinion issued by the German Patent and Trademark Office (dated 1/8/19),' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Request for Oral Argument, filed February 19, 2019

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed May 17, 2019	
				Application Number	15/857,519
				Filing Date	December 28, 2017
				First Named Inventor	Jefferey C. Solomon
				Art Unit	2139
				Examiner Name	Bansal, Gurtej
Sheet	2	of	4	Attorney Docket Number	129980-5023US

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Objections To Reply Evidence, filed February 19, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Request For Oral Argument, filed February 19, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Motion To Exclude, filed February 19, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Corrected Petitioners' Reply to Patent Owner's Response, filed February 20, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Opposition to Patent Owner's Motion to Exclude, filed March 5, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Sur-Reply To Petitioner's Corrected Reply, filed March 8, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Reply To Petitioner's Opposition To Motion To Exclude, filed March 12, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 3002, 'Patent Owner's Request for Sur Reply,' filed March 1, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Order - Trial Hearing, filed March 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364 EXHIBITS 1043, 'Deposition Transcript of R. Jacob Baker (Feb. 9, 2019),' filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1044, 'Declaration of R. Jacob Baker in IPR2017-00577 concerning the parent to the '907 Patent (Oct. 25, 2017),' filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1045, 'Deposition Transcript of R. Jacob Baker in IPR2017-00577 concerning the parent to the '907 Patent (Jan. 12, 2018),' filed February 22, 2019

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed May 17, 2019	
				Application Number	15/857,519
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				First Named Inventor	Jefferey C. Solomon
				Art Unit	2139
				Examiner Name	Bansal, Gurtej
Sheet	3	of	4	Attorney Docket Number	129980-5023US

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1046, 'Final Written Decision in IPR2017-00577 invalidating all challenged claims to the parent to the '907 Patent (July 5, 2018),' filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1048, 'U.S. Patent No. 7,133,960,' filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Reply to Patent Owner's Response, filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Objections To Reply Evidence, filed March 1, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Request for Oral Argument, filed March 4, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Request For Oral Argument, filed March 4, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Motion To Exclude, filed March 4, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Opposition to Patent Owner's Motion to Exclude, filed March 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Sur-Reply To Petitioner's Reply, filed March 15, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Reply To Petitioner's Opposition To Motion To Exclude, filed March18, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Order, Trial Hearing, filed March 1, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1003: Declaration of Dr. Harold Stone, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Supplemental Mandatory Notices, filed September 17, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2003: Deposition of Harold S. Stone, Ph. D, October 5, 2018, filed October 19, 2018

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed May 17, 2019	
				Application Number	15/857,519
				Filing Date	December 28, 2017
				First Named Inventor	Jefferey C. Solomon
				Art Unit	2139
				Examiner Name	Bansal, Gurtej
Sheet	4	of	4	Attorney Docket Number	129980-5023US

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2004: United States International Trade Commission, Inv. No. 337-TA-1089, Joint List of Claim Terms for Construction and Proposed Constructions, filed October 19, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2002: Declaration of R. Jacob Baker, Ph.D, P.E., filed October 19, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2005: United States International Trade Commission, Inv. No. 337-TA-1089, Order No. 17: Construing Terms of the Asserted Patents, filed October 19, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Response, filed October,19, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1011: JEDEC Standard DDR2 SDRAM Specification, JESD79-2B (January 2005), filed December 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Patent Owner's Objections to Petition Evidence, filed August 21, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Patent Owner's Supplemental Mandatory Notices, filed September 17, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Patent Owner's Response, filed November 16, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Exhibit 2001: Annotated Fig. 4 of U.S. Patent No. 7024518 - Halbert, filed November 16, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Exhibit 2002: Declaration of R. Jacob Baker, Ph.D, P.E., filed November 16, 2018

Examiner Signature		Date Considered	

Electronically filed May 17, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jefferey Solomon et al	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	Bansal, Gurtej
For:	MEMORY MODULE WITH DATA BUFFERING	Attorney Docket No.:	129980-5023US

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☐ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

Petitioners
Ex. 1054, p. 451

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☒ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☒ This Information Disclosure Statement replaces a prior Information Disclosure Statement submitted on April 23, 2019, in which inadvertent omissions were made despite a bona fide attempt to comply with 37 C.F.R. §1.98. Copies of publications listed on Form PTO-1449 enclosed in the prior Information Disclosure Statement submitted on April 23, 2019 are not being submitted again herewith.

7c. ☒ Copies of the publications listed on the attached Form PTO-1449 that were not listed on Form PTO-1449 enclosed in the prior Information Disclosure Statement submitted on April 23, 2019, or previously cited in prior application Serial No. 14/715,486, filed on May 18, 2015, 13/971,231, filed on August 20, 2013, 13/287,081, filed on November 1, 2011, 13/032,470, filed on February 22, 2011, 12/955,711, filed on November 29, 2010, 12/629,827, filed on December 2, 2009, 12/408,652, filed on March 20, 2009, 11/335,875, filed on January 19, 2006, 11/173,175, filed on July 1, 2005, and 11/075,395 filed on March 7, 2005, of which this application claims priority under 35 U.S.C. §120, are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023US).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: May 17, 2019

/Jamie J. Zheng/ 51,167
Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
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(650) 843-4000

REMARKS

This Amendment is in response to the Notice of Allowance dated April 19, 2019 and is filed with a Request for Continued Examination.

Claims 1, 3, 9-10, 12-13, 16-17, 18-20, 22-27, 29-30 and 32 are amended. New claims 33-37 are presented. No new matter is added.

Support for the amendments can be found in at least paragraphs [0040], [0053], [0056]-[0058], [0072], [0107], [0117], [0157]-[0158], and FIGS. 6A and 6B.

Applicant files herewith an Information Disclosure Statement, which replaces and corrects errors in the Information Disclosure Statement filed on April 23, 2019.

CONCLUDING REMARKS

In light of the above amendments and remarks, the Applicant respectfully requests that the amendments be entered. The Examiner is invited to call the undersigned attorney at (650) 843-4000, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: May 17, 2019

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
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Phone: (650) 843-4000

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system at a specified data rate via a N-bit wide data bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first burst of data and a first burst of data strobes and the second memory command to cause the memory module to receive or output a second burst of data and a second burst of data strobes, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, ~~each rank of the plurality of ranks having a same bit width as the memory module,~~ wherein the plurality of N-bit wide ranks include a first rank ~~selected~~ configured to receive or output the first burst of data and the first burst of data strobes at the specified data rate in response to the first memory command, and a second rank ~~selected~~ configured to receive or output the second burst of data and the second burst of data strobes at the specified data rate in response to the second memory command;

at least one data buffer ~~including a set of signal paths~~ coupled between the plurality of N-bit wide ranks ~~first rank~~ and the N-bit wide data bus~~, and between the second rank and the data bus~~; and

logic coupled to the at least one data buffer and configured to respond to the first memory command by providing first control signals to the at least one data buffer and to subsequently respond to the second memory command by providing second control signals to the at least one data buffer, wherein the at least one data buffer includes logic pipelines ~~in response to the first control signals is~~ configured to enable data transfers via the set of signal paths in response to the first control signals and subsequently in response to the second control signals, wherein ~~to transfer~~ respective bits of the first burst of data and respective data strobes of the first burst of data strobes

are transferred at the specified data rate between the first rank and the N-bit wide data bus ~~memory controller~~ through ~~the set of signal paths in~~ the at least one data buffer, ~~wherein the logic is further configured to respond to the second memory command by providing second control signals to the at least one data buffer,~~ and wherein ~~the at least one data buffer in response to the second control signals is configured to enable the set of signal paths to transfer~~ respective bits of the second burst of data and respective data strobes of the second burst of data strobes are transferred at the specified data rate between the second rank and the N-bit wide data bus ~~memory controller~~ through ~~the set of signal paths in~~ the at least one data buffer;

wherein the data transfers through the at least one data buffer are registered data transfers, and the at least one data buffer ~~adds at least one clock cycle~~ is configured to add a predetermined amount of time delay for each registered data transfer through the at least one data buffer ~~between the plurality of memory integrated circuits and the memory controller~~ so that an overall CAS latency of the memory module is ~~at least one clock cycle~~ greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.

2. (Previously Presented) The memory module of claim 1, wherein each of the plurality memory integrated circuits has a corresponding load, and wherein the at least one data buffer is configured to isolate the loads of the plurality of memory integrated circuits from the memory controller.

3. (Currently Amended) The memory module of claim 1, wherein the logic is coupled to the printed circuit board and is further configured to receive from the memory controller a first set of input address and control signals associated with the first memory command and to respond to the first memory command by outputting a first set of registered ~~command~~ address and control signals, and wherein the logic is further configured to subsequently receive from the memory controller a second set of input address and control signals associated with the second memory command and to respond to the second memory command by outputting a second set of registered ~~command~~ address and control signals, the first ~~memory command having associated therewith~~ set of input address and control signals including a first set of input chip select signals corresponding to respective ranks of the plurality of ranks and the second set of input address and control signals including ~~memory command having associated therewith~~ a second set of input chip select signals corresponding to respective ranks of the plurality of ranks, the first set of registered ~~command~~

address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals, the second set of registered address and control ~~command~~ signals including a second plurality of registered chip select signals corresponding to respective ones of the second plurality of input chip select signals, the first set of registered chip select signals including a first registered chip select signal ~~each~~ having an active signal value and one or more other registered chip select signals each having a non-active signal value, the second set of registered chip select signals including a second registered chip select signal ~~each~~ having an active signal value and one or more other registered chip select signals each having a non-active signal value, and wherein the logic ~~first rank~~ is configured to ~~receive~~ output the first registered chip select signal to the first rank and to output ~~the second rank is configured to receive~~ the second registered chip select signal to the second rank.

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Previously Presented) The memory module of claim 1, further comprising an SPD device that reports the overall CAS latency of the memory module to the memory controller.

9. (Currently Amended) The memory module of claim 1, wherein the memory module is ~~further coupled to~~ configured to receive from the memory controller ~~using~~ an on-die-termination (ODT) ~~bus~~signal, wherein each of the plurality of memory integrated circuits includes an ODT circuit, the memory module further comprising a termination circuit external to any of the plurality of memory integrated circuits, wherein the termination circuit is ~~coupled to~~configured to receive the ODT ~~bus~~ signal and is coupled to the ODT circuit of at least one of the plurality of memory integrated circuits, wherein the termination circuit is configured to provide external termination of at least one of the plurality of memory integrated circuits in response to ~~an~~ the ODT signal ~~on the ODT bus~~, and wherein the ODT circuit of the at least one of the plurality of memory integrated circuits is disabled.

10. (Currently Amended) The memory module of claim 1, wherein the ~~at least one data buffer comprises combinatorial logic, registers, and~~ logic pipelines are further configured to control timing of the registered ~~to time~~ data transfers through the at least one data buffer.

11. (Previously Presented) The memory module of claim 1, wherein the logic is further configured to determine the overall CAS latency of the memory module.

12. (Currently Amended) The memory module of claim 1, wherein the registered data transfers through the at least one data buffer ~~the set of signal paths~~ are enabled in accordance with the overall CAS latency of the memory module.

13. (Currently Amended) The memory module of claim 1, wherein each rank of the plurality of ranks is 72-bit wide, wherein each rank of the plurality of memory integrated circuits includes 18 4-bit wide memory integrated circuits configured in 9 pairs, wherein a first pair of memory integrated circuits in the first rank is configured to communicate a respective byte of the first burst of data in each time interval of a first plurality of time intervals, and wherein a second pair of memory integrated circuits in the second rank is configured to communicate a respective byte of the second burst of data in each time interval of a second plurality of time intervals.

14. (Previously Presented) The memory module of claim 13, wherein the first pair of memory integrated circuits are configured to simulate an 8-bit wide memory device, and the second pair of memory integrated circuits are configured to simulate another 8-bit wide memory device.

15. (Previously Presented) The memory module of claim 13, further comprising an SPD device programmed with data to characterize each pair of memory integrated circuits as a virtual 8-bit wide memory device.

16. (Currently Amended) The memory module of claim 1 ~~3~~, wherein respective bits of the first burst of data and respective data strobes of the first burst of data strobes are transferred through the at least one data buffer during respective time intervals of a first plurality of time intervals, and wherein respective bits of the second burst of data and respective data strobes of the second burst of data strobes are transferred through the at least one data buffer during respective time intervals of a second plurality of time intervals~~the data buffer includes a set of~~

~~circuit components configurable to enable the set of signal paths in response to the first set of control signals and subsequently in response to the second set of control signals~~.

17. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to ~~read/write~~read or write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to receive a first set of input ~~command~~ address and control signals associated with a first ~~read/write~~read or write memory command and to output a first set of registered ~~command~~ address and control signals in response to the first set of input ~~command~~ address and control signals, the first set of input ~~command~~ address and control signals including a first plurality of input chip select signals, the first set of registered ~~command~~ address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals, the first plurality of registered chip select signals including a first registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, ~~each rank of the plurality of ranks having a same data width as the memory module,~~ wherein the plurality of ranks are configured to receive respective ones of the first plurality of registered chip select signals, wherein a first rank in the plurality of ranks receiving the first registered chip select signal having the active signal value is ~~selected~~ configured to receive or output a first burst of data and a first burst of data strobes associated with the first ~~read/write~~ read or write command;

at least one data buffer coupled between data and strobe signal lines in the N-bit wide memory bus and corresponding data and strobe pins of the memory devices in each of the plurality of N-bit wide ranks, the at least one data buffer including logic pipelines configured to control data transfers through the at least one data buffer ~~a set of signal paths between the memory bus and the memory devices~~; and

wherein the logic is further configured to, in response to the first ~~read/write~~read or write memory command, output first control signals to the at least one data buffer, and wherein the logic pipelines are ~~at least one buffer is~~ configured to respond ~~in response~~ to the first control signals ~~to enable the set of signal paths~~ by enabling the at least one data buffer to transfer the first burst of data and the first burst of data strobes ~~between the memory devices and the memory controller~~ through the at least one data buffer in accordance with an overall CAS latency of the memory module; and

~~wherein the set of signal paths are enabled in accordance with an overall CAS latency of the memory module, and~~ wherein the data transfers through the at least one data buffer are registered data transfers and the at least one data buffer ~~adds at least one clock cycle~~ is configured to add a predetermined amount of time delay for each registered data transfer through the at least one data buffer such that the overall CAS latency of the memory module is ~~at least one clock cycle~~ greater than an actual operational CAS latency of each of the ~~plurality of~~ memory devices.

18. (Currently Amended) The memory module of claim 17, wherein each of the memory devices has a corresponding load, and the at least one data buffer is configured to isolate the loads of the memory devices from the memory bus.

19. (Currently Amended) The memory module of claim 17, wherein the first burst of data includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein ~~the set of signal paths are enabled for a time period when~~ the logic pipelines are configured to enable the at least one data buffer to successively transfer the set of consecutively transmitted data bits ~~are successively transferred~~ through the at least one data buffer in response to the first control signals.

20. (Currently Amended) The memory module of claim 17, wherein the logic is further configured to respond to a second set of input ~~command~~ address and control signals associated with a second ~~read/write~~read or write memory command by outputting a second set of registered ~~command~~ address and control signals, the second set of input ~~command~~ address and control signals including a second plurality of input chip select signals, the second set of registered ~~command~~ address and control signals including a second plurality of registered chip select signals corresponding to respective ones of the second plurality of input chip select signals, the

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Ex. 1054, p. 461

second plurality of registered chip select signals including a second registered chip select signal having the active signal value and one or more other registered chip select signals each having the non-active signal value, wherein a second rank different from the first rank includes memory devices configured to receive the second registered chip select signal having the active signal value and is ~~selected~~configured to output or receive a second burst of data and a second burst of data strobes associated with the second ~~read/write~~read or write command, wherein the logic is further configured to, in response to the second ~~read/write~~read or write memory command, output second control signals to the at least one data buffer, and wherein the logic pipelines are ~~at least one buffer is~~ configured ~~in response~~ to respond to the second control signals ~~to enable the set of signal paths~~ by enabling the at least one data buffer to transfer the second burst of data and the second burst of data strobes between the memory devices and the memory controller through the at least one data buffer in accordance with the overall CAS latency of the memory module.

21. (Previously Presented) The memory module of claim 17, wherein each of the memory devices is 4-bits wide, and wherein each of the plurality of ranks is 72-bits wide and includes 18 memory devices configured in pairs, and wherein each pair of 4-bit-wide memory devices are configured to simulate an 8-bit-wide memory device.

22. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to ~~read/write~~read or write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to receive a set of input ~~command~~ control and address signals associated with a ~~read/write~~ first read or write memory command via the memory bus and to output a set of registered ~~command~~ control and address signals in response to the set of input ~~command~~ control and address signals, the set of input ~~command~~ control and address signals including a plurality of input chip select signals, the set of registered ~~command~~ control and address signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals, the plurality of registered chip select

signals including a registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, ~~each rank of the plurality of ranks having a same data width as the memory module,~~ wherein the plurality of ranks are configured to receive respective ones of the plurality of registered chip select signals, wherein a first rank receiving the registered chip select signal having the active signal value is ~~selected~~ configured to receive or output a first burst of data and a first burst of data strobes associated with the read/write command;

logic pipelines controlled by the logic and configured to enable data transfers between the memory devices and the memory bus;

~~a plurality of configurable circuit components to enable or disable a set of signal paths~~ circuitry between respective data ~~or~~ and data strobe signal lines in the memory bus and corresponding data ~~or~~ and data strobe pins of the memory devices, wherein the circuitry is controlled by the logic pipelines and configured to transfer the first burst of data and the first burst of data strobes between the first rank and the memory bus; and

~~wherein the logic is further configured to, in response to the read/write memory command, output first control signals, wherein the plurality of configurable circuit components are configured in response to the first control signals to enable the set of signal paths to transfer the first burst of data and the first burst of data strobes between the memory devices and the memory controller; and~~

wherein the ~~set of signal paths~~ data transfers between the memory devices and the memory bus are registered data transfers and are enabled by the logic pipelines in accordance with an overall CAS latency of the memory module; and

wherein the ~~memory module registers at least one additional clock cycle~~ circuitry is configured to add a predetermined amount of time delay for each data transfer between the memory controller and the memory devices such that the overall CAS latency of the memory module is ~~at least one clock cycle~~ greater than an actual operational CAS latency of each of the ~~plurality of~~ memory devices.

23. (Currently Amended) The memory module of claim 22, wherein the first burst of data includes a set of consecutively transmitted data bits for each data signal line in the memory bus,

and wherein the circuitry includes a set of signal paths that are enabled before a first data bit of the set of consecutively transmitted data bits is ~~during a time period when the set of consecutively transmitted data bits are successively~~ transferred through the circuitry and disabled after a last data bit of the set of consecutively transmitted data bits is transferred through the circuitry ~~plurality of configurable circuit components~~.

24. (Currently Amended) The memory module of claim 22, wherein the logic is further configured to respond to a subsequent set of input ~~command~~ address and control signals associated with a subsequent ~~read/write~~read or write memory command by outputting a subsequent set of registered ~~command~~ address and control signals, the subsequent set of input ~~command~~ address and control signals including a subsequent plurality of input chip select signals, the subsequent set of registered ~~command~~ address and control signals including a subsequent plurality of registered chip select signals corresponding to respective ones of the subsequent plurality of input chip select signals, the subsequent plurality of registered chip select signals including a subsequently registered chip select signal having the active signal value and one or more other registered chip select signals each having the non-active signal value, wherein a second rank different from the first rank is configured to receive the subsequently registered chip select signal having the active signal value and is ~~selected~~ configured to output or receive a second burst of data and a second burst of data strobes associated with the subsequent ~~read/write~~read or write command, wherein the logic pipelines are ~~is~~ further configured to enable data transfers between the memory devices and the data and data strobe signal lines, in response to the subsequent read/write memory command, ~~output second control signals, wherein the plurality of configurable circuit components are configured to enable the set of signal paths in response to the second control signals~~ and wherein the circuitry is further configured to transfer the second burst of data and the second burst of data strobes between the second rank and the memory bus ~~memory devices and the memory controller~~.

25. (Currently Amended) The memory module of claim 17, wherein the memory devices are organized in four ranks and the first set of input ~~command~~ address and control signals include four chip select signals, one for each of the four ranks.

26. (Currently Amended) The memory module of claim 17, wherein the ~~at least one data~~

~~buffer comprises combinatorial logic, registers, and~~ logic pipelines are further configured to time the registered data transfers through the at least one data buffer.

27. (Currently Amended) The memory module of claim 17, wherein the logic is further configured to ~~determine~~ report the overall CAS latency to the memory controller in response to a mode register set command received from the memory controller.

28. (Previously Presented) The memory module of claim 17, wherein the first burst of data and the first burst of data strobes are communicated between the memory devices and the memory controller at a specified data rate.

29. (Currently Amended) The memory module of claim 17, wherein the first burst of data is transferred through the at least one data buffer in a plurality of ~~cycles~~time intervals including at least a first ~~cycle~~time interval and a ~~second~~ last ~~cycle~~time interval, ~~wherein the first control signals include a first subset of control signals for the first cycle and a subsequent second subset of control signals for the second cycle,~~ wherein the at least one data buffer includes a set of signal paths that are enabled before the first time interval ~~in response to the first subset of control signals~~ and subsequently disabled after the last time interval ~~in response to the second subset of control signals of the first burst of data~~.

30. (Currently Amended) The memory module of claim 20, wherein:

~~the first set of input command signals including a first input command signal indicating that~~ the first read or write memory ~~read/write~~ command is a read memory command;

~~the second set of input command signals including a second input command signal indicating that~~ the second read or write memory ~~second read/write~~ command is a write memory command;

the ~~set of signal paths are~~ at least one data buffer is enabled to transfer the first burst of data and the first burst of data strobes a first number of ~~clock cycles~~ time intervals after the ~~first input~~ read memory command ~~signal~~ is received by the logic; and

the ~~set of signal paths are~~ at least one data buffer is enabled to transfer the second burst of data and the second burst of data strobes a second number of ~~clock cycles~~time intervals after the ~~second input~~ write memory command ~~signal~~ is received by the logic, the second number being different from the first number.

31. (Previously Presented) The memory module of claim 22, wherein the first burst of data and the first burst of data strobes are transferred between the first rank of the memory devices and the memory controller at a specified data rate.

32. (Currently Amended) The memory module of claim 22, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay ~~first burst of data is transferred in a plurality of cycles including a first cycle and a second cycle, wherein the first control signals include a first subset of control signals for the first cycle and a subsequent second subset of control signals for the second cycle, wherein the plurality of configurable circuit components are configured to enable the set of signal paths in response to the first subset of control signals and subsequently in response to the second subset of control signals~~.

33. (New) The memory module of claim 32, wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the first rank is configured receive or output a respective set of bits of the first burst of data on both edges of each of a respective set of data strobes of the first burst of data strobes.

34. (New) The memory module of claim 17, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.

35. (New) The memory module of claim 34, wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the first rank is configured receive or output a respective set of bits of the first burst of data on both edges of each of a respective set of data strobes of the first burst of data strobes.

36. (New) The memory module of claim 1, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the

memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.

37. (New) The memory module of claim 36, wherein the memory integrated circuits are dynamic random access memory integrated circuits configured to operate synchronously with the clock signal, wherein each memory integrated circuit in the first rank is configured receive or output a respective set of bits of the first burst of data on both edges of each of a respective set of data strobes of the first burst of data strobes, and wherein each memory integrated circuit in the second rank is configured receive or output a respective set of bits of the second burst of data on both edges of each of a respective set of data strobes of the second burst of data strobes.

Electronically filed May 17, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Netlist, Inc.	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	BANSAL, Gurtej
For:	*MEMORY MODULE WITH DATA BUFFERING*	Attorney Docket No.:	129980-5023-US
		Date:	May 17, 2019

AMENDMENT AND REQUEST FOR CONTINUED EXAMINATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

Applicant files herewith an Amendment and Request for Continued Examination in the above-referenced patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US).

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/857,519	Filing Date 12/28/2017	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)			
FOR	NUMBER FILED	NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $80 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $420 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT	05/17/2019	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 33	Minus	** 28	= 5		x $100 =	500
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	500

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	SLIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/KIMBERLY D COOPER/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronically filed May 28, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Netlist, Inc.	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	BANSAL, Gurtej
For:	*MEMORY MODULE WITH DATA BUFFERING*	Attorney Docket No.:	129980-5023-US
		Date:	May 28, 2019

PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

Applicant files herewith an Amendment in the above-referenced patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US).

Electronic Acknowledgement Receipt

EFS ID:	36133487
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023US
Receipt Date:	28-MAY-2019
Filing Date:	28-DEC-2017
Time Stamp:	18:18:56
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980_5023US_PRE_AMEND.pdf	181202 f00b3adfefc21ed734ef629cb68caf5bd5cea30e	yes	13

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Applicant Arguments/Remarks Made in an Amendment	13	13
	Claims	2	12
	Preliminary Amendment	1	1
Warnings:			
Information:			
	Total Files Size (in bytes):	181202	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS

Claims 1-2, 9-10, 12-13, 16-20, 22-26, 28-31, 33, 35, and 37 are amended. No new matter is added.

Support for the amendments can be found throughout the specification and the accompanying drawings.

CONCLUDING REMARKS

In light of the above amendments and remarks, the Applicant respectfully requests that the amendments be entered. The Examiner is invited to call the undersigned attorney at (650) 843-4000, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: May 28, 2019

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
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Phone: (650) 843-4000

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system at a specified data rate via a N-bit wide data bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first burst of N-bit wide data signals and a first burst of data strobes and the second memory command to cause the memory module to receive or output a second burst of N-bit wide data signals and a second burst of data strobes, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks include a first rank configured to receive or output the first burst of N-bit wide data signals and the first burst of data strobes at the specified data rate in response to the first memory command, and a second rank configured to receive or output the second burst of N-bit wide data signals and the second burst of data strobes at the specified data rate in response to the second memory command;

~~at least one data buffer~~circuitry coupled between the plurality of N-bit wide ranks and the N-bit wide data bus; and

logic coupled to the circuitry ~~at least one data buffer~~and configured to respond to the first memory command by providing first control signals to the circuitry ~~at least one data buffer~~and to subsequently respond to the second memory command by providing second control signals to the circuitry ~~at least one data buffer~~, wherein the ~~at least one data bufferincludes logic pipelines~~ circuitry is configured to enable data transfers through the circuitry ~~via the set of signal paths~~ in response to the first control signals and subsequently in response to the second control signals, wherein respective ~~bits~~ N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred at the specified data rate between the first rank and the N-bit wide data bus through the circuitry ~~at least one data buffer~~,

and wherein respective N-bit wide data signals ~~bits~~ of the second burst of N-bit wide data signals and respective data strobes of the second burst of data strobes are transferred at the specified data rate between the second rank and the N-bit wide data bus through the circuitry ~~at least one data buffer~~;

wherein the data transfers through the circuitry ~~at least one data buffer~~ are registered data transfers enabled in accordance with an overall CAS latency of the memory module, and the circuitry ~~at least one data buffer~~ is configured to add a predetermined amount of time delay for each registered data transfer through the circuitry ~~at least one data buffer~~ so that the ~~an~~ overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.

2. (Currently Amended) The memory module of claim 1, wherein each of the plurality memory integrated circuits has a corresponding load, and wherein the circuitry ~~at least one data buffer~~ is configured to isolate the loads of the plurality of memory integrated circuits from the memory controller.

3. (Previously Presented) The memory module of claim 1, wherein the logic is coupled to the printed circuit board and is further configured to receive from the memory controller a first set of input address and control signals associated with the first memory command and to respond to the first memory command by outputting a first set of registered address and control signals, and wherein the logic is further configured to subsequently receive from the memory controller a second set of input address and control signals associated with the second memory command and to respond to the second memory command by outputting a second set of registered address and control signals, the first set of input address and control signals including a first set of input chip select signals corresponding to respective ranks of the plurality of ranks and the second set of input address and control signals including a second set of input chip select signals corresponding to respective ranks of the plurality of ranks, the first set of registered address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals, the second set of registered address and control signals including a second plurality of registered chip select signals corresponding to respective ones of the second plurality of input chip select signals, the first set of registered chip select signals including a first registered chip select signal having an active signal value and one or more other

registered chip select signals each having a non-active signal value, the second set of registered chip select signals including a second registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value, and wherein the logic is configured to output the first registered chip select signal to the first rank and to output the second registered chip select signal to the second rank.

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Previously Presented) The memory module of claim 1, further comprising an SPD device that reports the overall CAS latency of the memory module to the memory controller.

9. (Currently Amended) The memory module of claim 1, wherein the memory module is configured to receive from the memory controller an on-die-termination (ODT) signal, wherein each of the plurality of memory integrated circuits includes an ODT circuit, the memory module further comprising a termination circuit external to any of the plurality of memory integrated circuits, wherein the termination circuit is configured to receive the ODT signal and is coupled to the ODT circuit of at least one of the plurality of memory integrated circuits, wherein the termination circuit is configured to provide external termination ~~of~~ for the at least one of the plurality of memory integrated circuits in response to the ODT signal, and wherein the ODT circuit of the at least one of the plurality of memory integrated circuits is disabled.

10. (Currently Amended) The memory module of claim 1, wherein the circuitry includes logic pipelines ~~are further~~ configured to enable the data transfers through the circuitry in response to the first control signals and subsequently in response to the second control signals ~~control timing of the registered data transfers through the at least one data buffer~~.

11. (Previously Presented) The memory module of claim 1, wherein the logic is further configured to determine the overall CAS latency of the memory module.

12. (Currently Amended) The memory module of claim 1, wherein N is 64 or 72 ~~the registered data transfers through the at least one data buffer are enabled in accordance with the overall CAS latency of the memory module~~.

13. (Currently Amended) The memory module of claim 1, wherein each rank of the plurality of ranks is 72-bit wide, wherein each rank of the plurality of N-bit wide ranks ~~memory integrated circuits~~ includes 18 4-bit wide memory integrated circuits configured in 9 pairs, wherein a first pair of memory integrated circuits in the first rank is configured to communicate a respective byte of the first burst of N-bit wide data signals in each time interval of a first plurality of time intervals, and wherein a second pair of memory integrated circuits in the second rank is configured to communicate a respective byte of the second burst of N-bit wide data signals in each time interval of a second plurality of time intervals.

14. (Previously Presented) The memory module of claim 13, wherein the first pair of memory integrated circuits are configured to simulate an 8-bit wide memory device, and the second pair of memory integrated circuits are configured to simulate another 8-bit wide memory device.

15. (Previously Presented) The memory module of claim 13, further comprising an SPD device programmed with data to characterize each pair of memory integrated circuits as a virtual 8-bit wide memory device.

16. (Currently Amended) The memory module of claim 1, wherein the respective ~~bits~~ N-bit wide data signals of the first burst of N-bit wide data signals and the respective data strobes of the first burst of data strobes are transferred through the ~~at least one data buffer~~circuitry during respective time intervals of a first plurality of time intervals, and wherein the respective N-bit wide data signals ~~bits~~ of the second burst of N-bit wide data signals and the respective data strobes of the second burst of data strobes are transferred through the ~~at least one data buffer~~circuitry during respective time intervals of a second plurality of time intervals.

17. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to receive a first set of input address and control signals associated with a first read or write memory command and to output a first set of registered address and control signals in response to the first set of input address and control signals, the first set of input address and control signals including a first plurality of input chip select signals, the first set of registered address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals, the first plurality of registered chip select signals including a first registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of ranks are configured to receive respective ones of the first plurality of registered chip select signals, wherein a first rank in the plurality of ranks receiving the first registered chip select signal having the active signal value is configured to receive or output a first burst of N-bit wide data signals and a first burst of data strobes associated with the first read or write command;

~~at least one data buffer~~circuitry coupled between data and strobe signal lines in the N-bit wide memory bus and corresponding data and strobe pins of ~~the~~ memory devices in each of the plurality of N-bit wide ranks~~, the at least one data buffer including logic pipelines configured to control data transfers through the at least one data buffer~~; and

wherein the logic is further configured to, in response to the first read or write memory command, output first control signals to the circuitry ~~at least one data buffer~~, and wherein the circuitry is configured to enable data transfers between the first rank and the memory bus through the circuitry in response ~~logic pipelines are configured to respond~~ to the first control signals ~~by enabling the at least one data buffer to transfer~~ so that respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred through the circuitry ~~at least one data buffer~~ in accordance with an overall CAS latency of the memory module; and

wherein the data transfers between the first rank and the memory bus through the circuitry ~~at least one data buffer~~ are registered data transfers and the circuitry ~~at least one data buffer~~ is

configured to add a predetermined amount of time delay for each registered data transfer through the circuitry ~~at least one data buffer~~ such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

18. (Currently Amended) The memory module of claim 17, wherein each of the memory devices has a corresponding load, and the circuitry ~~at least one data buffer~~ is configured to isolate the loads of the memory devices from the memory bus.

19. (Currently Amended) The memory module of claim 17, wherein the first burst of N-bit wide data signals includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein ~~the logic pipelines are configured to enable the at least one data buffer to successively transfer~~ the set of consecutively transmitted data bits are successively transferred through the circuitry ~~at least one data buffer~~ in response to the first control signals.

20. (Currently Amended) The memory module of claim 17, wherein the logic is further configured to respond to a second set of input address and control signals associated with a second read or write memory command by outputting a second set of registered address and control signals, the second set of input address and control signals including a second plurality of input chip select signals, the second set of registered address and control signals including a second plurality of registered chip select signals corresponding to respective ones of the second plurality of input chip select signals, the second plurality of registered chip select signals including a second registered chip select signal having the active signal value and one or more other registered chip select signals each having the non-active signal value, wherein a second rank different from the first rank ~~includes memory devices~~ is configured to receive the second registered chip select signal having the active signal value and ~~is configured~~ to output or receive a second burst of N-bit wide data signals and a second burst of data strobes associated with the second read or write command, wherein the logic is further configured to, in response to the second read or write memory command, output second control signals to the circuitry ~~at least one data buffer~~, and wherein the ~~logic pipelines are configured to respond~~ circuitry is configured to enable registered data transfers between the second rank and the memory bus through the circuitry in response to the second control signals ~~by enabling the at least one data buffer to transfer~~ so that the second burst of N-bit wide data signals and the second burst of data strobes

are transferred between the second rank ~~the memory devices~~ and the memory controller through the circuitry ~~at least one data buffer~~ in accordance with the overall CAS latency of the memory module.

21. (Previously Presented) The memory module of claim 17, wherein each of the memory devices is 4-bits wide, and wherein each of the plurality of ranks is 72-bits wide and includes 18 memory devices configured in pairs, and wherein each pair of 4-bit-wide memory devices are configured to simulate an 8-bit-wide memory device.

22. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to receive a set of input control and address signals associated with a first read or write memory command via the memory bus and to output a set of registered control and address signals in response to the set of input control and address signals, the set of input control and address signals including a plurality of input chip select signals, the set of registered control and address signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals, the plurality of registered chip select signals including a registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of ranks are configured to receive respective ones of the plurality of registered chip select signals, wherein a first rank receiving the registered chip select signal having the active signal value is configured to receive or output a first burst of N-bit wide data signals and a first burst of data strobes associated with the read/write command;

~~logic pipelines controlled by the logic and configured to enable data transfers between the memory devices and the memory bus;~~

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circuitry between ~~respective~~ data and data strobe signal lines in the memory bus and corresponding data and data strobe pins of the memory devices, wherein the circuitry includes ~~is controlled by the~~ logic pipelines ~~and~~ configured to enable data transfers between the first rank and the memory bus in response to the first read or write memory command, wherein respective N-bit wide data signals of ~~transfer~~ the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred between the first rank and the memory bus through the circuitry in accordance with an overall CAS latency of the memory module; and

wherein the data transfers between the first rank ~~memory devices~~ and the memory bus are registered data transfers ~~and are enabled by the logic pipelines in accordance with an overall CAS latency of the memory module~~; and

wherein the circuitry is configured to add a predetermined amount of time delay for each data transfer between the memory controller and the memory devices such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

23. (Currently Amended) The memory module of claim 22, wherein the first burst of N-bit wide data signals includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein the circuitry includes a set of signal paths that are enabled before a first data bit of the set of consecutively transmitted data bits is transferred through the circuitry and disabled after a last data bit of the set of consecutively transmitted data bits is transferred through the circuitry.

24. (Currently Amended) The memory module of claim 22, wherein the logic is further configured to respond to a subsequent set of input address and control signals associated with a subsequent read or write memory command by outputting a subsequent set of registered address and control signals, the subsequent set of input address and control signals including a subsequent plurality of input chip select signals, the subsequent set of registered address and control signals including a subsequent plurality of registered chip select signals corresponding to respective ones of the subsequent plurality of input chip select signals, the subsequent plurality of registered chip select signals including a subsequently registered chip select signal having the active signal value and one or more other registered chip select signals each having the non-active signal value, wherein a second rank different from the first rank is configured to receive

the subsequently registered chip select signal having the active signal value and ~~is configured~~ to output or receive a second burst of N-bit wide data signals and a second burst of data strobes associated with the subsequent read or write command, wherein the ~~logic pipelines are~~ circuitry is further configured to enable registered data transfers between the memory devices and the memory bus ~~data and data strobe signal lines,~~ in response to the subsequent read/write memory command~~, and wherein the circuitry is further configured to transfer~~ so that the second burst of N-bit wide data signals and the second burst of data strobes are transferred between the second rank and the memory bus through the circuitry.

25. (Previously Presented) The memory module of claim 17, wherein the memory devices are organized in four ranks and the first set of input address and control signals include four chip select signals, one for each of the four ranks.

26. (Currently Amended) The memory module of claim 17, wherein the circuitry includes logic pipelines ~~are further~~ configured to enable the data transfers between the first rank and the memory bus through the circuitry in response to the first control signals~~time the registered data transfers through the at least one data buffer~~.

27. (Previously Presented) The memory module of claim 17, wherein the logic is further configured to report the overall CAS latency to the memory controller in response to a mode register set command received from the memory controller.

28. (Currently Amended) The memory module of claim 17, wherein the first burst of N-bit wide data signals and the first burst of data strobes are ~~communicated~~ transferred between first rank of the memory devices and the memory controller at a specified data rate.

29. (Currently Amended) The memory module of claim 20~~17~~, wherein the first burst of N-bit wide data signals is transferred through the ~~at least one data buffer~~circuitry in a plurality of time intervals including at least a first time interval and a last time interval, wherein the ~~at least one data buffer~~circuitry includes a set of signal paths that are enabled before the first time interval and subsequently disabled after the last time interval.

30. (Currently Amended) The memory module of claim 29~~20~~, wherein:

the first read or write memory command is a read memory command;

the second read or write memory command is a write memory command;

the set of signal paths are ~~at least one data buffer is~~ enabled to transfer the first burst of N-bit wide data signals and the first burst of data strobes a first number of time intervals after the read memory command is received by the logic; and

the set of signal paths are ~~at least one data buffer is~~ enabled to transfer the second burst of N-bit wide data signals and the second burst of data strobes a second number of time intervals after the write memory command is received by the logic, the second number being different from the first number.

31. (Currently Amended) The memory module of claim 22, wherein the first burst of N-bit wide data signals and the first burst of data strobes are transferred between the first rank of the memory devices and the memory controller at a specified data rate.

32. (Previously Presented) The memory module of claim 22, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.

33. (Currently Amended) The memory module of claim 32, wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the first rank is configured receive or output a respective set of bits of the first burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the first burst of data strobes.

34. (Previously Presented) The memory module of claim 17, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.

35. (Currently Amended) The memory module of claim 34, wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the first rank is configured receive or output a

respective set of bits of the first burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the first burst of data strobes.

36. (Previously Presented) The memory module of claim 1, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.

37. (Currently Amended) The memory module of claim 36, wherein the memory integrated circuits are dynamic random access memory integrated circuits configured to operate synchronously with the clock signal, wherein each memory integrated circuit in the first rank is configured receive or output a respective set of bits of the first burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the first burst of data strobes, and wherein each memory integrated circuit in the second rank is configured receive or output a respective set of bits of the second burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the second burst of data strobes.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/857,519	Filing Date 12/28/2017	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

	(Column 1)		(Column 2)			
FOR	NUMBER FILED		NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A		N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A		N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A		N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =		*		x $80 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =		*		x $420 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).					
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))						
* If the difference in column 1 is less than zero, enter "0" in column 2.					TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT	05/28/2019	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 33	Minus	** 33	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	SLIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/KIMBERLY D COOPER/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/857,519	12/28/2017	Jefferey C. Solomon	129980-5023US	9826

79141 7590 06/10/2019

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER	
BANSAL, GURTEJ	

ART UNIT	PAPER NUMBER
2139	

NOTIFICATION DATE	DELIVERY MODE
06/10/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

padocketingdepartment@morganlewis.com
vskliba@morganlewis.com

Applicant-Initiated Interview Summary	**Application No.** 15/857,519	**Applicant(s)** Solomon et al.	
	Examiner GURTEJ BANSAL	**Art Unit** 2139	**AIA (FITF) Status** No

All participants (applicant, applicants representative, PTO personnel):

(1) GURTEJ BANSAL. (3) _____.

(2) JAMIE ZHENG. (4) _____.

Date of Interview: 05 June 2019.

Type: ☑ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☑ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☐103 ☑Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: 1.

Identification of prior art discussed: N/A.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Applicant indicated that an RCE has been filed in this application and that a preliminary amendment has been made. Examiner discussed the amendment with the Applicant to understand the scope and the intended language of the claimed invention..

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiners responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicants correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,-
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicants record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiners version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, Interview Record OK on the paper recording the substance of the interview along with the date and the examiners initials.

Electronically filed July 9, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jefferey C. Solomon	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	BANSAL, GURTEJ
For:	*MEMORY MODULE WITH DATA BUFFERING*	Atty. Docket No.:	129980-5023-US

INTERVIEW SUMMARY

The Applicant's representatives thank Examiner BANSAL, for the opportunity to discuss this application in a telephonic interview with Jamie J. Zheng (51,167) on June 5, 2019. Applicant indicated that an RCE has been filed in this application and that a preliminary amendment has been made.

Examiner discussed the amendment with the Applicant to understand the scope and the intended language of the claimed invention. No specific agreement was reached.

Respectfully submitted,

Date: July 9, 2019

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
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Petitioners
Ex. 1054, p. 489

Electronic Acknowledgement Receipt

EFS ID:	36535917
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023US
Receipt Date:	09-JUL-2019
Filing Date:	28-DEC-2017
Time Stamp:	20:30:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant summary of interview with examiner	129980-5023-US_Int_Sum.pdf	94979 4449243b2129629347a8a10826851e776550468a	no	1
Warnings:					

Information:	
Total Files Size (in bytes):	94979

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/857,519	12/28/2017	Jefferey C. Solomon	129980-5023US	9826

79141 7590 08/08/2019

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EXAMINER	
BANSAL, GURTEJ	

ART UNIT	PAPER NUMBER
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08/08/2019	ELECTRONIC

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padocketingdepartment@morganlewis.com
vskliba@morganlewis.com

Applicant-Initiated Interview Summary	**Application No.** 15/857,519	**Applicant(s)** Solomon et al.	
	Examiner GURTEJ BANSAL	**Art Unit** 2139	**AIA (FITF) Status** No

All participants (applicant, applicants representative, PTO personnel):

(1) GURTEJ BANSAL. (3) _____.

(2) JAMIE ZHENG. (4) _____.

Date of Interview: 26 July 2019.

Type: ☑ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☑ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☐103 ☑Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: 1.

Identification of prior art discussed: N/A.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Applicant called to check on the status of the claims and discuss the claims as presented in the preliminary amendment. Examiner indicated that the preliminary amendment along with RCE has been received. Examiner also indicated should any questions arise with the amendment that the Examiner would contact the Applicant for clarification..

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiners responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicants correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,-
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicants record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiners version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, Interview Record OK on the paper recording the substance of the interview along with the date and the examiners initials.

Electronically filed August 20, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jefferey C. Solomon	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	Bansal, Gurtej
For:	MEMORY MODULE WITH DATA BUFFERING	Attorney Docket No.:	129980-5023-US

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUBSTANCE OF INTERVIEW

Applicant thanks Examiner Gurtej Bansal for discussing the application during a telephonic interview with Applicant's counsel Jamie Zheng (Reg. No. 51,167) on July 26, 2019. In the interview, Applicant inquired about the status of the application. Examiner indicated that the recently submitted preliminary amendment along with a request for continued examination (RCE) has been received. Examiner also indicated that Examiner would contact Applicant for clarification should any questions arise with the preliminary amendment.

Respectfully submitted,

Date: August 20, 2019

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

Petitioners
Ex. 1054, p. 495

Electronic Acknowledgement Receipt

EFS ID:	36930446
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023US
Receipt Date:	20-AUG-2019
Filing Date:	28-DEC-2017
Time Stamp:	18:18:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant summary of interview with examiner	129980-5023US_INT_SUM.pdf	118627 bcfe4630eb728e2e417d43f5b2b168e75845d762	no	1
Warnings:					

Information:	
Total Files Size (in bytes):	118627

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 22, 2019	
				Application Number	15/857,519
				Filing Date	December 28, 2017
				First Named Inventor	Jefferey C. Solomon
				Art Unit	2139
				Examiner Name	Bansal, Gurtej
Sheet	1	of	1	Attorney Docket Number	129980-5023US

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 29, 'Termination Decision Document,' filed June 27,2019, 94 pgs
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 30, 'Record of Oral Hearing,' filed June 27,2019, 131 pgs

Examiner Signature		Date Considered	

Electronic Acknowledgement Receipt

EFS ID:	36957044
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/Lamesha Robertson
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023US
Receipt Date:	22-AUG-2019
Filing Date:	28-DEC-2017
Time Stamp:	20:22:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980_5023US_IDS.pdf	265221 a7039329cfb600c5d251e49a3c604af403cf1da2	yes	5

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	4	
	Information Disclosure Statement (IDS) Form (SB08)		5	5	
Warnings:					
Information:					
2	Non Patent Literature	PAPER_29.pdf	21688255 e1ab49b9b1c0f85542ae55d05bdad3144e9919c3	no	94
Warnings:					
Information:					
3	Non Patent Literature	PAPER_30.pdf	25864067 00a52c402fc5f144d1c7393b5db2352ac7297754	no	131
Warnings:					
Information:					
		Total Files Size (in bytes):	47817543		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed August 22, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jefferey Solomon et al	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	Bansal, Gurtej
For:	MEMORY MODULE WITH DATA BUFFERING	Attorney Docket No.:	129980-5023US

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☐ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

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☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☒ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☐ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☐ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial No. , filed on , of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

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9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023US).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: August 22, 2019

Jamie Zheng 51,167
(Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 09/06/2019
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER
BANSAL, GURTEJ

ART UNIT	PAPER NUMBER
2139	

DATE MAILED: 09/06/2019

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/857,519	12/28/2017	Jefferey C. Solomon	129980-5023US	9826

TITLE OF INVENTION: MEMORY MODULE WITH DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	12/06/2019

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 09/06/2019
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/857,519	12/28/2017	Jefferey C. Solomon	129980-5023US	9826

TITLE OF INVENTION: MEMORY MODULE WITH DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	12/06/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
BANSAL, GURTEJ	2139	711-105000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

Petitioners
Ex. 1054, p. 506

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/857,519	12/28/2017	Jefferey C. Solomon	129980-5023US	9826

79141 7590 09/06/2019

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER	
BANSAL, GURTEJ	
ART UNIT	**PAPER NUMBER**
2139	

DATE MAILED: 09/06/2019

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Petitioners
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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	**Application No.** 15/857,519	**Applicant(s)** Solomon et al.	
	Examiner GURTEJ BANSAL	**Art Unit** 2139	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to Applicant's amendment dated 05/28/2019.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-3 and 8-37 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information , please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 05/17/2019; 08/22/2019.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/857,519	Solomon et al.
	Examiner	Art Unit
	GURTEJ BANSAL	2139

CPC - Searched*		
Symbol	Date	Examiner
G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc.	09/27/2018	GB

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Inventor Search in PE2E	09/27/2018	GB
Text Search in EAST (See Attached)	09/27/2018	GB
NPL Search in Google Scholar (See Attached)	09/27/2018	GB
Updated Text Search in EAST (See Attached)	03/29/2019	GB
NPL Search in Google Scholar (See Attached)	03/29/2019	GB
Updated Text Search in EAST (See Attached)	09/01/2019	GB
Updated NPL Search in Google Scholar (See Attached)	09/01/2019	GB

/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	

Petitioners
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/857,519	Solomon et al.
	Examiner	Art Unit
	GURTEJ BANSAL	2139

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc.	09/27/2018	GB
	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc.	03/31/2019	GB
	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc.	09/01/2019	GB

/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	

Petitioners
Ex. 1054, p. 511

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/857,519	Solomon et al.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

CPC							
Symbol						**Type**	**Version**
G06F	/	13	/	1673		F	2013-01-01
G11C	/	5	/	04		I	2013-01-01
G06F	/	13	/	00		I	2013-01-01
G06F	/	12	/	00		I	2013-01-01
G06F	/	13	/	4243		I	2013-01-01
G06F	/	13	/	4282		I	2013-01-01
G11C	/	7	/	1072		I	2013-01-01
G11C	/	15	/	00		I	2013-01-01

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	33	
/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	01 September 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	9A

U.S. Patent and Trademark Office — Part of Paper No.: 20190901

Petitioners
Ex. 1054, p. 512

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/857,519	Solomon et al.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

INTERNATIONAL CLASSIFICATION				
CLAIMED				
G06F	/	12	/	00

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	33	
/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	01 September 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	9A

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/857,519	Solomon et al.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	6	10	17	19	22	28	14	37						
2	2	7	11	25	20	26	29								
3	3	8	12	18	21	27	30								
	4	9	13	28	22	31	31								
	5	10	14	29	23	32	32								
	6	11	15	30	24	33	33								
	7	12	16	19	25	23	34								
4	8	15	17	20	26	24	35								
5	9	16	18	21	27	13	36								

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	33	
/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	01 September 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	9A

U.S. Patent and Trademark Office — Part of Paper No.: 20190901

Petitioners
Ex. 1054, p. 514

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed May 17, 2019	
				Application Number	15/857,519
				Filing Date	December 28, 2017
				First Named Inventor	Jefferey C. Solomon
				Art Unit	2139
				Examiner Name	Bansal, Gurtej
Sheet	1	of	4	Attorney Docket Number	129980-5023US

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		7,024,518 B2	04-04-2006	Halbert et al.	
		7334150 B2	02-19-2008	Ruckerbauer et al.	
		2006/0248969 A1	11-09-2006	Seo et al.	

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1044, 'Deposition Transcript of R. Jacob Baker (Jan. 26, 2019),' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1045, 'Deposition Transcript of R. Jacob Baker (Jan. 12, 2018) in IPR2017-00577 concerning the parent to the '907 Patent,' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1047, 'Certified translation of the Examination Decision issued by the State Intellectual Property Office of the P.R.C. (dated 5/30/18),' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Reply to Patent Owner's Response, filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1043, 'Chart comparing text in Dr. Baker's declaration [Ex. 2002] with identical text in Patent Owner's Response [Paper No. 14],' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1046, 'Final Office Action concerning U.S. Patent Application No. 15/470,856 (dated 7/27/18),' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1048, 'Certified translation of the Preliminary Opinion issued by the German Patent and Trademark Office (dated 1/8/19),' filed February 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Request for Oral Argument, filed February 19, 2019

Examiner Signature	/GURTEJ BANSAL/	Date Considered	09/01/2019

DB2/ 22684197.4

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed May 17, 2019	
				Application Number	15/857,519
				Filing Date	December 28, 2017
				First Named Inventor	Jefferey C. Solomon
				Art Unit	2139
				Examiner Name	Bansal, Gurtej
Sheet	2	of	4	Attorney Docket Number	129980-5023US

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Objections To Reply Evidence, filed February 19, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Request For Oral Argument, filed February 19, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Motion To Exclude, filed February 19, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Corrected Petitioners' Reply to Patent Owner's Response, filed February 20, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Opposition to Patent Owner's Motion to Exclude, filed March 5, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Sur-Reply To Petitioner's Corrected Reply, filed March 8, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Reply To Petitioner's Opposition To Motion To Exclude, filed March 12, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 3002, 'Patent Owner's Request for Sur Reply,' filed March 1, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Order - Trial Hearing, filed March 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364 EXHIBITS 1043, 'Deposition Transcript of R. Jacob Baker (Feb. 9, 2019),' filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1044, 'Declaration of R. Jacob Baker in IPR2017-00577 concerning the parent to the '907 Patent (Oct. 25, 2017),' filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1045, 'Deposition Transcript of R. Jacob Baker in IPR2017-00577 concerning the parent to the '907 Patent (Jan. 12, 2018),' filed February 22, 2019

Examiner Signature	/GURTEJ BANSAL/	Date Considered	09/01/2019

DB2/ 22684197.4

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed May 17, 2019	
				Application Number	15/857,519
				Filing Date	December 28, 2017
				First Named Inventor	Jefferey C. Solomon
				Art Unit	2139
				Examiner Name	Bansal, Gurtej
Sheet	3	of	4	Attorney Docket Number	129980-5023US

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1046, 'Final Written Decision in IPR2017-00577 invalidating all challenged claims to the parent to the '907 Patent (July 5, 2018),' filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1048, 'U.S. Patent No. 7,133,960,' filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Reply to Patent Owner's Response, filed February 22, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Objections To Reply Evidence, filed March 1, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Request for Oral Argument, filed March 4, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Request For Oral Argument, filed March 4, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Motion To Exclude, filed March 4, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Opposition to Patent Owner's Motion to Exclude, filed March 11, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Sur-Reply To Petitioner's Reply, filed March 15, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Reply To Petitioner's Opposition To Motion To Exclude, filed March18, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Order, Trial Hearing, filed March 1, 2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1003: Declaration of Dr. Harold Stone, filed December 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Supplemental Mandatory Notices, filed September 17, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2003: Deposition of Harold S. Stone, Ph. D, October 5, 2018, filed October 19, 2018

Examiner Signature	/GURTEJ BANSAL/	Date Considered	09/01/2019

DB2/ 22684197.4

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed May 17, 2019	
				Application Number	15/857,519
				Filing Date	December 28, 2017
				First Named Inventor	Jefferey C. Solomon
				Art Unit	2139
				Examiner Name	Bansal, Gurtej
Sheet	4	of	4	Attorney Docket Number	129980-5023US

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2004: United States International Trade Commission, Inv. No. 337-TA-1089, Joint List of Claim Terms for Construction and Proposed Constructions, filed October 19, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2002: Declaration of R. Jacob Baker, Ph.D, P.E., filed October 19, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2005: United States International Trade Commission, Inv. No. 337-TA-1089, Order No. 17: Construing Terms of the Asserted Patents, filed October 19, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Response, filed October,19, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1011: JEDEC Standard DDR2 SDRAM Specification, JESD79-2B (January 2005), filed December 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Patent Owner's Objections to Petition Evidence, filed August 21, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Patent Owner's Supplemental Mandatory Notices, filed September 17, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Patent Owner's Response, filed November 16, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Exhibit 2001: Annotated Fig. 4 of U.S. Patent No. 7024518 - Halbert, filed November 16, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Exhibit 2002: Declaration of R. Jacob Baker, Ph.D, P.E., filed November 16, 2018

Examiner Signature	/GURTEJ BANSAL/	Date Considered	09/01/2019

DB2/ 22684197.4

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Memory **rank** decoder for a multi-**rank** Dual Inline Memory Module (**DIMM**)

[PDF] googleapis.com

S Raghuram - US Patent 7,266,639, 2007 - Google Patents

... SUMMARY OF THE INVENTION Accordingly it is the object of the present invention to provide a memory **rank** decoder for a Multi-**Rank** Dual Inline Memory Module (**DIMM**) which allows an increased number (M) of memory **ranks** within the memory chips of dual ...

Cited by 140 Related articles All 4 versions

Increasing the number of **ranks** per channel

[PDF] googleapis.com

L Warnes, D Carr, MB Calhoun, AR Mandle - US Patent 8,539,145, 2013 - Google Patents

... connector, only if the quad **rank DIMM** has the same number of pins as the lower **ranked DIMM** ... 1B illustrates an embodiment of the system 100 that has the number of **ranks** per channel ... All eight **CS** signals are bussed to the two 16 **rank DIMMs** to get the encoding/decoding that ...

Cited by 12 Related articles All 2 versions

Emulation of abstracted **DIMMs** using abstracted DRAMs

MJS Smith, SN Rajan, DT Wang - US Patent 8,438,328, 2013 - Google Patents

One embodiment of the present invention sets forth an abstracted memory subsystem comprising abstracted memories, which each may be configured to present memory-related characteristics onto a memory system interface. The characteristics can be presented on the memory ...

Cited by 78 Related articles All 4 versions

Emulation of abstracted **DIMMS** using abstracted DRAMS

[PDF] googleapis.com

MJS Smith, SN Rajan, DT Wang - US Patent 8,631,193, 2014 - Google Patents

One embodiment of the present invention sets forth an abstracted memory subsystem comprising abstracted memories, which each may be configured to present memory related characteristics onto a memory system interface. The characteristics can be presented on the memory ...

Cited by 67 Related articles All 4 versions

Load reduction system and method for **DIMM**-based memory systems

[PDF] googleapis.com

C Haywood, G Raghavan, C Xu - US Patent 8,275,936, 2012 - Google Patents

... arrangement of 64 or 72 data bits using DRAM chips in parallel is termed a '**rank**' 16. The DRAM chips within a **DIMM** may be connected in a parallel arrangement---which may include stacking of DRAM chips within the same package—to provide additional **ranks** (18) ...

Cited by 19 Related articles All 2 versions

Circuit with flexible portion

JR Bhakta, E Yu, **CS** Chen, RE Flaig - US Patent 7,811,097, 2010 - Google Patents

US7811097B1 - Circuit with flexible portion - Google Patents. Circuit with flexible portion. Download PDF Info. Publication number US7811097B1. US7811097B1 US12/237,162 US23716208A US7811097B1 US 7811097 B1 ...

Cited by 77 Related articles All 2 versions

Circuit with flexible portion

JR Bhakta, E Yu, **CS** Chen, RE Flaig - US Patent 8,033,836, 2011 - Google Patents

US8033836B1 - Circuit with flexible portion - Google Patents. Circuit with flexible portion. Download PDF Info. Publication number US8033836B1. US8033836B1 US12/874,900 US87490010A US8033836B1 US 8033836 B1 ...

Cited by 68 Related articles All 2 versions

Circuit card with flexible connection for memory module with heat spreader

JR Bhakta, E Yu, **CS** Chen, RE Flaig - US Patent 7,442,050, 2008 - Google Patents

... not limited to, dual in-line memory modules (**DIMMs**) such as fully-buffered **DIMMs** (FBDIMMs) ... Example **ranks** compatible with certain embodiments described herein are blocks of memory of a fixed depth ... 16 or 18 "×4" memory components can be used to form a **rank** of memory ...

Cited by 78 Related articles All 2 versions

Circuit with flexible portion

JR Bhakta, E Yu, **CS** Chen, RE Flaig - US Patent 8,287,291, 2012 - Google Patents

... not limited to, dual in-line memory modules (**DIMMs**) such as fully-buffered **DIMMs** (FBDIMMs) ... Example **ranks** compatible with certain embodiments described herein are blocks of memory of a fixed depth ... 16 or 18 "×4" memory components can be used to form a **rank** of memory ...

Cited by 64 Related articles All 2 versions

Apparatus and method for initialization of a double-sided **DIMM** having at least one pair of mirrored pins

[PDF] googleapis.com

KS Bains - US Patent 7,260,691, 2007 - Google Patents

... signals provide a command encoding to issue various commands to the various **ranks** of **DIMM** 300. In one embodiment, the encoding for issuing an MRS command is issued to the **DIMM rank** by driving CAS# signal 304, RAS# signal 306, WE# signal 302 and **CS**# signal 308 ...

Cited by 60 Related articles All 4 versions

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Electronically filed May 28, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Netlist, Inc.	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	BANSAL, Gurtej
For:	*MEMORY MODULE WITH DATA BUFFERING*	Attorney Docket No.:	129980-5023-US
		Date:	May 28, 2019

PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

Applicant files herewith an Amendment in the above-referenced patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US).

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	7	(great$3 increas$3) with CAS with latency same DIMM	US-PGPUB; USPAT	OR	OFF	2019/09/01 19:02
L2	7	(great$3 increas$3) with CAS with latency same DIMM	US-PGPUB; USPAT	OR	OFF	2019/09/01 19:28
L3	28	(plurality multiple) with virtual with DIMM	US-PGPUB; USPAT	OR	ON	2019/09/01 19:32
S1	3717	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2011/07/03 21:54
S2	75	365/189.2.ccls.	USPAT	OR	OFF	2011/07/03 21:54
S3	104	365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:27
S4	6392	abstract$3 with (DRAM DIMM memory)	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:40
S5	48	abstracted adj2 (DRAM DIMM memory)	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:40
S6	109	abstracted adj2 (DRAM DIMM memory) or aDRAM	US-PGPUB; USPAT	OR	OFF	2011/07/03 22:42
S7	1	"7515453".pn.	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:00
S8	771	interface same (DDR2 and (DDR or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:17
S9	504	interface with (DDR2 and (DDR or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:18
S10	5	365/189.2.ccls. and (DDR2 and (DDR or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:19
S11	10	365/189.2.ccls. and (DDR and (DDR2 or DRAM or SRAM or DDR3 or flash))	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:24
S12	1	"20070088995".pn.	US-PGPUB; USPAT	OR	OFF	2011/07/05 19:29
S13	241	CKE with precharge	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:48
S14	0	365/189.2.ccls and CKE with precharge	US-	OR	OFF	2011/07/05

			PGPUB; USPAT			21:48
S15	111	CKE with precharge same power	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:48
S16	36	silent with alarm with clock	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:54
S17	0	silent with alarm with clock and lark.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:54
S18	0	silent with alarm with clock and hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:54
S19	4	alarm with clock and hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:55
S20	0	julia-hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:58
S21	2	julia.in. and hu.in.	US-PGPUB; USPAT	OR	OFF	2011/07/05 21:59
S22	16	lark.as.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:00
S23	629	precharge same power and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:01
S24	3	precharge same power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:03
S25	1	self with refresh and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:08
S26	3	pre$1charge with power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:09
S27	11	pre$1chargesame power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:09
S28	3	pre$1charge same power and CKE and 365/189.2.ccls.	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:09
S29	55	pre$1charge same power and CKE and DRAM same DDR same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:22
S30	59	pre$1charge same power and CKE and DRAM same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:25
S31	73	pre$1charge same power and CKE and DDR same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/05 22:26
S32	89	refresh same power and CKE and DDR same DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:17
S33	10	365/189.2.ccls. and (pre$1charge refresh)	US-	OR	OFF	2011/07/06

		and CKE	PGPUB; USPAT			00:27
S34	54	SPD and (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:29
S35	16	SPD same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:29
S36	0	module with transmit same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:45
S37	19	memory with transmit same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:45
S38	23	configure same (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:48
S39	14	configure with (pre$1charge refresh) and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:48
S40	1	DDR with DRAM and tCKE with timing with memory	US-PGPUB; USPAT	OR	OFF	2011/07/06 00:52
S41	273	intelligent adj3 (buffer or register)	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:01
S42	9	intelligent adj3 (buffer or register) and pre$charge	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:01
S43	298	SPD same2 (pre$1charge refresh)	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:03
S44	197	SPD same (pre$1charge refresh)	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:03
S45	59	SPD same2 (pre$1charge refresh) and DDR same DRAM	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:03
S46	38	SPD same (pre$1charge refresh) and DDR same DRAM	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:04
S47	3	SPD same (pre$1charge refresh) and DDR same DRAM and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 01:05
S48	59	SPD same2 (pre$1charge refresh) and DDR same DRAM	US-PGPUB; USPAT	OR	OFF	2011/07/06 10:59
S49	1	SPD same pre$1charge with power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:01
S50	25	SPD same self adj refresh	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:01
S51	0	SPD same self adj refresh and DDR	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:04
S52	2	SPD same self adj refresh and DDR2	US-	OR	OFF	2011/07/06

			PGPUB; USPAT			11:04
S53	22	SPD same self adj refresh same power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:07
S54	2	SPD same self adj refresh and CKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:24
S55	0	SPD same self adj refresh and tCKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:26
S56	0	SPD same pre$1charge and tCKE	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:27
S57	2617837	SPD swith power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:29
S58	578	SPD with power	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:29
S59	16	SPD with power same (self adj refresh self$1refresh pre adj charge pre$charge)	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:30
S60	21	SPD same self adj refresh and (pre$1charge or pre adj charge)	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:37
S61	1	"20050246558".pn.	US-PGPUB; USPAT	OR	OFF	2011/07/06 11:41
S62	2	SPD same power with management with mode	US-PGPUB; USPAT	OR	OFF	2011/07/06 12:40
S63	13	365/189.2.ccls. and CS	USPAT	OR	OFF	2011/07/06 12:55
S64	21	365/189.2.ccls. and CS	US-PGPUB; USPAT	OR	OFF	2011/07/06 12:55
S65	171	DIMM same CS	US-PGPUB; USPAT	OR	OFF	2011/07/06 13:00
S66	53	365/189.2.ccls. and (tRP tRCD TWL tRFC timing tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:34
S67	7	365/189.2.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:34
S68	1631	"365".clas. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S69	0	365/189.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S70	446	365/189.$.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR)	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:36
S71	36	365/189.$.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS	US-PGPUB;	OR	OFF	2011/07/06 14:36

		tRC tRRD tRTP tWR tWTR) and DDR2	USPAT			
S72	1	365/189.$.ccls. and (tRP tRCD TWL tRFC tCKE tXP tXARD TXRDS tAL tFAW tRAS tRC tRRD tRTP tWR tWTR) same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:37
S73	3	burst with plurality with DIMM	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:43
S74	0	burst with each with DIMM	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:44
S75	6	burst with multiple with DIMM	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:44
S76	6	burst with multiple with DIMM and read	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:46
S77	5	burst with multiple with DIMM same read	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:47
S78	11	burst with DIMMs same read	US-PGPUB; USPAT	OR	OFF	2011/07/06 14:47
S79	0	365/189.2.ccls. and CKE with (high and low)	USPAT	OR	OFF	2011/07/06 16:19
S80	529	CKE with (high and low)	USPAT	OR	OFF	2011/07/06 16:20
S81	17	CKE with (high and low) and DDR2	USPAT	OR	OFF	2011/07/06 16:20
S82	0	365/189.2.ccls. and CKE with (high and low)	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:20
S83	44	CKE with (high and low) and DDR2	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:21
S84	87	CKE with (high and low) same pre$1charge	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:24
S85	0	CKE with (high and low) same pre$1charge same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:24
S86	0	CKE with (high and low) same self adj refresh same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:25
S87	0	CKE with ((high and low) or assert) same self adj refresh same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:25
S88	0	CKE with ((high and low) or assert) same pre$1fetch same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:25
S89	0	CKE with (high or low or assert) same pre$1fetch same SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:26
S90	0	CKE with (high or low or assert) same pre$1fetch same2 SPD	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:26
S91	2	CKE with (high or low or assert) same	US-	OR	OFF	2011/07/06

		SPD	PGPUB; USPAT			16:26
S92	10	SPD same2 CKE with (high or low or assert)	US-PGPUB; USPAT	OR	OFF	2011/07/06 16:27
S93	1	"20090216936".pn.	US-PGPUB; USPAT	OR	OFF	2012/01/20 18:08
S94	1	"20090216939".pn.	US-PGPUB; USPAT	OR	OFF	2012/01/20 18:17
S95	152	buffer with DRAM with protocol	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:25
S96	152	buffer$3 with DRAM with protocol	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:37
S97	572	buffer with $1RAM with protocol	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:38
S98	1	"20030131160".pn.	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:47
S99	1729	buffer with $1RAM with (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:48
S100	626	buffer with DRAM with (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:48
S101	124	buffer with chip with DRAM with (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/20 19:51
S102	185	buffer near5 DRAM near5 (timing calibration)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:14
S103	499	buffer with DRAM with type	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:18
S104	51	buffer with DRAM with type with (multiple different tim$3 various)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:19
S105	224	buffer with DRAM with DDR	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:21
S106	3	buffer with DRAM with (timing signal) with adjust	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:32
S107	146	buffer with DRAM with (timing signal) with delay	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:32
S108	31	buffer with DRAM with (timing signal) with DDR$1	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:32
S109	70	buffer with DRAM with (timing signal protocol) and buffer with DDR$1 with (timing signal protocol)	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:37
S110	118	buffer with DRAM with (timing signal	US-	OR	OFF	2012/01/21

		protocol) and buffer with SDRAM with (timing signal protocol)	PGPUB; USPAT			00:48
S111	36	buffer with DRAM with SDRAM with interface	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:52
S112	48	buffer with DRAM with (SDRAM DDR2 DDR3) with interface	US-PGPUB; USPAT	OR	OFF	2012/01/21 00:52
S113	73	interface with buffer with DRAM with (DDR$1 SDRAM)	US-PGPUB; USPAT	OR	OFF	2012/01/21 02:03
S114	141	interface same buffer with DRAM with (DDR$1 SDRAM)	US-PGPUB; USPAT	OR	OFF	2012/01/21 02:10
S115	2	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/15 14:11
S116	64	DIMM with DRAM and CS with (DIMM DRAM) and buffer with (DIMM DRAM)	US-PGPUB; USPAT	OR	OFF	2013/01/15 14:12
S117	1	"5918229".pn.	US-PGPUB; USPAT	OR	OFF	2013/01/18 14:08
S118	1	"20060184942".pn.	US-PGPUB; USPAT	OR	OFF	2013/01/18 14:35
S119	130	(different multiple distinct) with file adj locking	US-PGPUB; USPAT	OR	OFF	2013/01/18 17:46
S120	0	abstracted with DIMM and DRAM	USPAT	OR	OFF	2013/01/21 13:21
S121	0	abstracted with DIMM	USPAT	OR	OFF	2013/01/21 13:21
S122	2	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 13:21
S123	56	US-5278796-$.DID. OR US-5282177-$.DID. OR US-5384745-$.DID. OR US-1241995-$.DID. OR US-5388265-$.DID. OR US-5467455-$.DID. OR US-5498886-$.DID. OR US-5598376-$.DID. OR US-5610864-$.DID. OR US-5675549-$.DID. OR US-5692202-$.DID. OR US-5706247-$.DID. OR US-5757703-$.DID. OR US-5949254-$.DID. OR US-6034916-$.DID. OR US-6034918-$.DID. OR US-6035365-$.DID. OR US-6330683-$.DID. OR US-6631086-$.DID. OR US-6754129-$.DID. OR US-6970968-$.DID. OR US-20030002262-$.DID. OR US-20040196732-$.DID. OR US-20050149662-$.DID. OR US-7172005-$.DID. OR US-20050259504-$.DID. OR US-20080025108-$.DID. OR US-20080025136-$.DID. OR US-5241266-$.DID. OR US-5843799-$.DID. OR US-5966727-$.DID. OR US-20060026484-$.DID. OR US-20080239858-$.DID. OR US-20080115006-$.DID. OR US-	US-PGPUB; USPAT	OR	OFF	2013/01/21 17:23

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S132	83	DIMM with CS and DIMM with DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 21:55
S133	3	("20050038924" | "20080052462" | "6681301").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/01/21 22:03
S134	104	US-20050289292-$.DID. OR US-20050289317-$.DID. OR US-20060002201-$.DID. OR US-6986118-$.DID. OR US-20060010339-$.DID. OR US-6992501-$.DID. OR US-6992950-$.DID. OR US-20060248387-$.DID. OR US-20060041730-$.DID. OR US-7000062-$.DID. OR US-7003618-$.DID. OR US-7003639-$.DID. OR US-20060038597-$.DID. OR US-20060039204-$.DID. OR US-20060039205-$.DID. OR US-20060041711-$.DID. OR US-7007095-$.DID. OR US-7007175-$.DID. OR US-20060044913-$.DID. OR US-20060044909-$.DID. OR US-7010642-$.DID. OR US-7010736-$.DID. OR US-20060049502-$.DID. OR US-20060050574-$.DID. OR US-20060056244-$.DID. OR US-20060062047-$.DID. OR US-20060067141-$.DID. OR US-7024518-$.DID. OR US-7028215-$.DID. OR US-7026708-$.DID. OR US-7028234-$.DID. OR US-20060085616-$.DID. OR US-7033861-$.DID. OR US-7035150-$.DID. OR US-20060087900-$.DID. OR US-20060090054-$.DID. OR US-20060090031-$.DID. OR US-7043599-	US-PGPUB; USPAT; USOCR	OR	OFF	2013/01/21 22:15

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S135	140	US-20060198178-$.DID. OR US-20060203590-$.DID. OR US-20060206738-$.DID. OR US-7119428-$.DID. OR US-20060236165-$.DID. OR US-20060236201-$.DID. OR US-20060233012-$.DID. OR US-7127567-$.DID. OR US-7126399-$.DID. OR US-20060248261-$.DID. OR US-7133960-$.DID. OR US-7136978-$.DID. OR US-20060262586-$.DID. OR US-7149145-$.DID. OR US-7149824-$.DID. OR US-20060294295-$.DID. OR US-20070005998-$.DID. OR US-7173863-$.DID. OR US-20070050530-$.DID. OR	US-PGPUB; USPAT; USOCR	OR	OFF	2013/01/21 22:17

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S136	2185	DRAM with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:35
S137	31	DRAM with DIMM and DIMM with virtual$5	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:35
S138	43	DRAM with DIMM and CS with module	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:39
S139	43	virtual with DIMM and DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 22:49
S140	57	buffer with CS and DIMM with DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:16
S141	2	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:22
S142	37	virtual$5 near3 DIMM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:22
S143	29	virtual$5 near3 DIMM and DRAM	US-PGPUB; USPAT	OR	OFF	2013/01/21 23:22
S144	541	(plurality multiple) with DIMM with single	US-PGPUB; USPAT	OR	ON	2013/01/21 23:25
S145	200	(plurality multiple) near3 DIMM with single	US-PGPUB; USPAT	OR	ON	2013/01/21 23:25
S146	170	(plurality multiple) near3 DIMM with single and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/21 23:25
S147	132	logical with DIMM	US-PGPUB;	OR	ON	2013/01/21 23:35

			USPAT			
S148	112	logical with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/21 23:35
S149	334	(group) with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/22 00:47
S150	55	emulat$3 with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/01/22 00:52
S151	71	virtual with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/22 09:39
S152	10	(plurality multiple) with virtual with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/22 09:40
S153	47	(plurality multiple) with (virtual logical emulat$3) with DIMM	US-PGPUB; USPAT	OR	ON	2013/01/22 09:40
S154	1	"7133960".pn.	US-PGPUB; USPAT	OR	ON	2013/01/22 09:42
S155	17	rank with (appear$3) with DIMM	USPAT	OR	OFF	2013/01/30 13:21
S159	180	(virtual logical abstract$3) with DIMM	US-PGPUB; USPAT	OR	ON	2013/02/18 23:49
S160	22	(virtual logical abstract$3) adj DIMM	US-PGPUB; USPAT	OR	ON	2013/02/18 23:49
S161	344	(virtual logical abstract$3) adj RAM	US-PGPUB; USPAT	OR	ON	2013/02/19 00:01
S162	98	(virtual logical abstract$3) adj DRAM	US-PGPUB; USPAT	OR	ON	2013/02/19 00:01
S168	2	"201100052062".pn. "5910010".pn. "5222014".pn.	US-PGPUB; USPAT	OR	OFF	2013/04/16 23:55
S169	18	US-20030110339-$.DID. OR US-20030174569-$.DID. OR US-20040049624-$.DID. OR US-20050044302-$.DID. OR US-20060277355-$.DID. OR US-20080130364-$.DID. OR US-20080282084-$.DID. OR US-20080282341-$.DID. OR US-20090049266-$.DID. OR US-20090070520-$.DID. OR US-20090063865-$.DID. OR US-20090063896-$.DID. OR US-20090089480-$.DID. OR US-6047361-$.DID. OR WO-199725674-$.DID. OR KR-2005120344-$.DID. OR US-3201318-$.DID. OR KR-1020087019582-$.DID. OR US-1201321-$.DID. OR US-6201324-$.DID. OR US-4201331-$.DID. OR US-9201340-$.DID. OR US-182013D-$.DID.	US-PGPUB; USPAT	OR	OFF	2013/07/24 15:48

S170	105	(virtual logical abstract$3) adj DRAM	US-PGPUB; USPAT	OR	ON	2013/07/24 15:59
S171	60	emulat$3 with DIMM and DRAM	US-PGPUB; USPAT	OR	ON	2013/07/24 15:59
S172	4337	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/07/24 16:02
S173	3	abstracted with DIMM	US-PGPUB; USPAT	OR	OFF	2013/07/24 16:04
S178	1054	buffer with data with CS	US-PGPUB; USPAT	OR	OFF	2017/04/26 15:45
S179	1637	buffer with DIMM	US-PGPUB; USPAT	OR	OFF	2017/04/26 15:49
S180	100	buffer and fan$4 with (rank dimm)	US-PGPUB; USPAT	OR	OFF	2017/04/26 16:14
S181	249	buffer same parallel with (rank dimm)	US-PGPUB; USPAT	OR	OFF	2017/04/26 16:26
S182	112	buffer same parallel with (ranks dimms)	US-PGPUB; USPAT	OR	OFF	2017/04/26 16:26
S183	60	daisy with chain with DIMM same buffer	US-PGPUB; USPAT	OR	OFF	2017/04/27 00:11
S184	9041	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	US-PGPUB; USPAT	OR	OFF	2017/04/30 15:23
S189	1	bust with rank$1 with select$3	US-PGPUB; USPAT	OR	OFF	2017/08/17 00:07
S190	38	burst with rank$1 with select$3	US-PGPUB; USPAT	OR	OFF	2017/08/17 00:07
S191	38	burst with rank with select$3	US-PGPUB; USPAT	OR	ON	2017/08/17 08:16
S192	141	burst same rank$1 same select$3	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:16
S193	113	buffer same parallel with (ranks dimms)	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:34
S194	5288	G06F13/1673.cpc. G011C7/1072.cpc. G011C15/00.cpc. G06F13/4282.cpc. G06F13/4243.cpc.	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:36
S195	299	DIMM same CS	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:46
S196	322	DIMM same (CS chip$1select)	US-PGPUB; USPAT	OR	OFF	2017/08/17 08:46
S197	83	DIMM with DRAM and CS with (DIMM)	US-	OR	OFF	2017/08/17

		and buffer with (DIMM DRAM)	PGPUB; USPAT			09:29
S198	195	DIMM with rank with select$3	US-PGPUB; USPAT	OR	OFF	2017/08/17 10:08
S200	35	DIMM same rank same burst	US-PGPUB; USPAT	OR	OFF	2017/08/17 15:23
S204	69	ranks same dimm same strobe	US-PGPUB; USPAT	OR	OFF	2018/09/27 12:55
S205	154	ranks same dimm same strobe	US-PGPUB; USPAT	OR	ON	2018/09/27 12:55
S206	150	(virtual logical abstract$3) adj DRAM	US-PGPUB; USPAT	OR	ON	2018/09/27 13:51
S207	355	DIMM same (CS chip$1select)	US-PGPUB; USPAT	OR	OFF	2018/09/27 14:01
S208	153	greater with CAS with latency	US-PGPUB; USPAT	OR	OFF	2018/09/27 20:45
S209	1	greater with CAS with latency with actual	US-PGPUB; USPAT	OR	OFF	2018/09/27 20:46
S210	375	(great$3 increas$3) with CAS with latency	US-PGPUB; USPAT	OR	OFF	2018/09/27 21:32
S211	7	(great$3 increas$3) with CAS with latency same DIMM	US-PGPUB; USPAT	OR	OFF	2018/09/27 21:32
S212	11706	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc.	US-PGPUB; USPAT	OR	OFF	2018/09/27 21:56
S216	210	virtual with DIMM	US-PGPUB; USPAT	OR	ON	2019/03/29 16:20
S217	7	(great$3 increas$3) with CAS with latency same DIMM	US-PGPUB; USPAT	OR	OFF	2019/03/29 19:38

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	6105	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc.	USPAT	OR	OFF	2019/09/01 19:58
L5	1	strobes.clm. and ranks.clm. and bits.clm.	USPAT	OR	OFF	2019/09/01 19:58
L6	0	L4 and L5	USPAT	OR	OFF	2019/09/01 19:58
S156	4194	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/01/30 13:35
S157	1321	emulated.clm.	USPAT	OR	OFF	2013/01/30 13:45

S158	3	S156 and S157	USPAT	OR	OFF	2013/01/30 13:45
S163	4205	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/02/19 00:04
S164	1330	emulated.clm.	USPAT	OR	OFF	2013/02/19 00:04
S165	4205	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/02/19 00:04
S166	1330	emulated.clm.	USPAT	OR	OFF	2013/02/19 00:04
S167	3	S165 and S166	USPAT	OR	OFF	2013/02/19 00:04
S174	4343	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/07/24 16:04
S175	4343	711/5.ccls. 711/105.ccls. 711/167.ccls. 365/189.2.ccls.	USPAT	OR	OFF	2013/07/24 16:06
S176	1399	emulated.clm.	USPAT	OR	OFF	2013/07/24 16:06
S177	4	S175 and S176	USPAT	OR	OFF	2013/07/24 16:06
S185	4964	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	USPAT	OR	OFF	2017/04/30 15:24
S186	6228	data.clm. adj path.clm.	USPAT	OR	OFF	2017/04/30 15:28
S187	120	S185 and S186	USPAT	OR	OFF	2017/04/30 15:28
S188	8	S185 and S186 and rank.clm.	USPAT	OR	OFF	2017/04/30 15:28
S199	5127	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	USPAT	OR	OFF	2017/08/17 10:17
S201	5127	G06F13/1684.cpc. G11C5/02.cpc. G11C5/06.cpc. G11C8/18.cpc. G06F13/4027.cpc.	USPAT	OR	OFF	2017/08/17 15:22
S202	0	S201 and buffer.clm. and rank.clm. and burst.clm.	USPAT	OR	OFF	2017/08/17 15:22
S203	8	DIMM with rank with selection	USPAT	OR	OFF	2017/08/17 15:23
S213	4948	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc.	USPAT	OR	OFF	2018/09/27 23:32
S214	0	strobes.clm. and ranks.clm. and bits.clm.	USPAT	OR	OFF	2018/09/27 23:33
S215	0	S213 and S214	USPAT	OR	OFF	2018/09/27 23:33
S218	5558	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc.	USPAT	OR	OFF	2019/03/31 13:43
S219	0	strobes.clm. and ranks.clm. and bits.clm.	USPAT	OR	OFF	2019/03/31 13:43
S220	0	S218 and S219	USPAT	OR	OFF	2019/03/31 13:43

9/ 1/ 2019 7:58:49 PM

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 22, 2019	
				Application Number	15/857,519
				Filing Date	December 28, 2017
				First Named Inventor	Jefferey C. Solomon
				Art Unit	2139
				Examiner Name	Bansal, Gurtej
Sheet	1	of	1	Attorney Docket Number	129980-5023US

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 29, 'Termination Decision Document,' filed June 27,2019, 94 pgs
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 30, 'Record of Oral Hearing,' filed June 27,2019, 131 pgs

Examiner Signature	/GURTEJ BANSAL/	Date Considered	09/01/2019

DB2/ 37159151.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

Electronically filed September 30, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Netlist, Inc.	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	BANSAL, Gurtej
For:	*MEMORY MODULE WITH DATA BUFFERING*	Attorney Docket No.:	129980-5023-US
		Date:	September 30, 2019

AMENDMENT UNDER 35 U.S.C. 312

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

In response to the Notice of Allowance dated September 6, 2019, Applicant files an Amendment under 35 U.S.C. 312 in the above-referenced patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US).

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A memory module operable in a computer system to communicate data with a memory controller of the computer system at a specified data rate via a N-bit wide data bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first burst of N-bit wide data signals and a first burst of data strobes and the second memory command to cause the memory module to receive or output a second burst of N-bit wide data signals and a second burst of data strobes, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks include a first rank configured to receive or output the first burst of N-bit wide data signals and the first burst of data strobes at the specified data rate in response to the first memory command, and a second rank configured to receive or output the second burst of N-bit wide data signals and the second burst of data strobes at the specified data rate in response to the second memory command;

circuitry coupled between the plurality of N-bit wide ranks and the N-bit wide data bus; and

logic coupled to the circuitry and configured to respond to the first memory command by providing first control signals to the circuitry and to subsequently respond to the second memory command by providing second control signals to the circuitry , wherein the circuitry is configured to enable data transfers through the circuitry in response to the first control signals and subsequently in response to the second control signals, wherein respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred at the specified data rate between the first rank and the N-bit wide data bus through the circuitry, and wherein respective N-bit wide data signals of the second burst of N-bit

wide data signals and respective data strobes of the second burst of data strobes are transferred at the specified data rate between the second rank and the N-bit wide data bus through the circuitry;

wherein the data transfers through the circuitry are registered data transfers enabled in accordance with an overall CAS latency of the memory module, and the circuitry is configured to add a predetermined amount of time delay for each registered data transfer through the circuitry so that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.

2. (Previously Presented) The memory module of claim 1, wherein each of the plurality memory integrated circuits has a corresponding load, and wherein the circuitry is configured to isolate the loads of the plurality of memory integrated circuits from the memory controller.

3. (Previously Presented) The memory module of claim 1, wherein the logic is coupled to the printed circuit board and is further configured to receive from the memory controller a first set of input address and control signals associated with the first memory command and to respond to the first memory command by outputting a first set of registered address and control signals, and wherein the logic is further configured to subsequently receive from the memory controller a second set of input address and control signals associated with the second memory command and to respond to the second memory command by outputting a second set of registered address and control signals, the first set of input address and control signals including a first set of input chip select signals corresponding to respective ranks of the plurality of ranks and the second set of input address and control signals including a second set of input chip select signals corresponding to respective ranks of the plurality of ranks, the first set of registered address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals, the second set of registered address and control signals including a second plurality of registered chip select signals corresponding to respective ones of the second plurality of input chip select signals, the first set of registered chip select signals including a first registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value, the second set of registered chip select signals including a second registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value, and

wherein the logic is configured to output the first registered chip select signal to the first rank and to output the second registered chip select signal to the second rank.

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Previously Presented) The memory module of claim 1, further comprising an SPD device that reports the overall CAS latency of the memory module to the memory controller.

9. (Previously Presented) The memory module of claim 1, wherein the memory module is configured to receive from the memory controller an on-die-termination (ODT) signal, wherein each of the plurality of memory integrated circuits includes an ODT circuit, the memory module further comprising a termination circuit external to any of the plurality of memory integrated circuits, wherein the termination circuit is configured to receive the ODT signal and is coupled to the ODT circuit of at least one of the plurality of memory integrated circuits, wherein the termination circuit is configured to provide external termination for the at least one of the plurality of memory integrated circuits in response to the ODT signal, and wherein the ODT circuit of the at least one of the plurality of memory integrated circuits is disabled.

10. (Previously Presented) The memory module of claim 1, wherein the circuitry includes logic pipelines configured to enable the data transfers through the circuitry in response to the first control signals and subsequently in response to the second control signals.

11. (Previously Presented) The memory module of claim 1, wherein the logic is further configured to determine the overall CAS latency of the memory module.

12. (Previously Presented) The memory module of claim 1, wherein N is 64 or 72.

13. (Currently Amended) The memory module of claim 1, wherein each rank of the plurality of ranks is 72-bits ~~72-bit~~ wide, wherein each rank of the plurality of N-bit wide ranks includes 18

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4-bit wide memory integrated circuits configured in 9 pairs, wherein a first pair of memory integrated circuits in the first rank is configured to communicate a respective byte of the first burst of N-bit wide data signals in each time interval of a first plurality of time intervals, and wherein a second pair of memory integrated circuits in the second rank is configured to communicate a respective byte of the second burst of N-bit wide data signals in each time interval of a second plurality of time intervals.

14. (Previously Presented) The memory module of claim 13, wherein the first pair of memory integrated circuits are configured to simulate an 8-bit wide memory device, and the second pair of memory integrated circuits are configured to simulate another 8-bit wide memory device.

15. (Previously Presented) The memory module of claim 13, further comprising an SPD device programmed with data to characterize each pair of memory integrated circuits as a virtual 8-bit wide memory device.

16. (Previously Presented) The memory module of claim 1, wherein the respective N-bit wide data signals of the first burst of N-bit wide data signals and the respective data strobes of the first burst of data strobes are transferred through the circuitry during respective time intervals of a first plurality of time intervals, and wherein the respective N-bit wide data signals of the second burst of N-bit wide data signals and the respective data strobes of the second burst of data strobes are transferred through the circuitry during respective time intervals of a second plurality of time intervals.

17. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to receive a first set of input address and control signals associated with a first read or write memory command and to output a first set of registered address and control signals in response to the first set of input address and control signals, the first set of input address and control signals including a first plurality of input

chip select signals, the first set of registered address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals, the first plurality of registered chip select signals including a first registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks are configured to receive respective ones of the first plurality of registered chip select signals, wherein a first N-bit wide rank in the plurality of N-bit wide ranks receiving the first registered chip select signal having the active signal value is configured to receive or output a first burst of N-bit wide data signals and a first burst of data strobes associated with the first read or write command;

circuitry coupled between data and strobe signal lines in the N-bit wide memory bus and corresponding data and strobe pins of memory devices in each of the plurality of N-bit wide ranks; and

wherein the logic is further configured to, in response to the first read or write memory command, output first control signals to the circuitry, and wherein the circuitry is configured to enable data transfers between the first rank and the memory bus through the circuitry in response to the first control signals so that respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred through the circuitry in accordance with an overall CAS latency of the memory module; and

wherein the data transfers between the first rank and the memory bus through the circuitry are registered data transfers and the circuitry is configured to add a predetermined amount of time delay for each registered data transfer through the circuitry such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

18. (Previously Presented) The memory module of claim 17, wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus.

19. (Previously Presented) The memory module of claim 17, wherein the first burst of N-bit wide data signals includes a set of consecutively transmitted data bits for each data signal line in

the memory bus, and wherein the set of consecutively transmitted data bits are successively transferred through the circuitry in response to the first control signals.

20. (Previously Presented) The memory module of claim 17, wherein the logic is further configured to respond to a second set of input address and control signals associated with a second read or write memory command by outputting a second set of registered address and control signals, the second set of input address and control signals including a second plurality of input chip select signals, the second set of registered address and control signals including a second plurality of registered chip select signals corresponding to respective ones of the second plurality of input chip select signals, the second plurality of registered chip select signals including a second registered chip select signal having the active signal value and one or more other registered chip select signals each having the non-active signal value, wherein a second rank different from the first rank is configured to receive the second registered chip select signal having the active signal value and to output or receive a second burst of N-bit wide data signals and a second burst of data strobes associated with the second read or write command, wherein the logic is further configured to, in response to the second read or write memory command, output second control signals to the circuitry, and wherein the circuitry is configured to enable registered data transfers between the second rank and the memory bus through the circuitry in response to the second control signals so that the second burst of N-bit wide data signals and the second burst of data strobes are transferred between the second rank and the memory controller through the circuitry in accordance with the overall CAS latency of the memory module.

21. (Previously Presented) The memory module of claim 17, wherein each of the memory devices is 4-bits wide, and wherein each of the plurality of ranks is 72-bits wide and includes 18 memory devices configured in pairs, and wherein each pair of 4-bit-wide memory devices are configured to simulate an 8-bit-wide memory device.

22. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to receive a set of input control and address signals associated with a ~~first~~ read or write memory command via the memory bus and to output a set of registered control and address signals in response to the set of input control and address signals, the set of input control and address signals including a plurality of input chip select signals, the set of registered control and address signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals, the plurality of registered chip select signals including a registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks are configured to receive respective ones of the plurality of registered chip select signals, wherein a first N-bit wide rank receiving the registered chip select signal having the active signal value is configured to receive or output a first burst of N-bit wide data signals and a first burst of data strobes associated with the read/write command;

circuitry between data and data strobe signal lines in the memory bus and corresponding data and data strobe pins of the memory devices, wherein the circuitry includes logic pipelines configured to enable data transfers between the first rank and the memory bus in response to the first read or write memory command, wherein respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred between the first rank and the memory bus through the circuitry in accordance with an overall CAS latency of the memory module; and

wherein the data transfers between the first rank and the memory bus are registered data transfers; and

wherein the circuitry is configured to add a predetermined amount of time delay for each data transfer between the memory controller and the memory devices such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

23. (Previously Presented) The memory module of claim 22, wherein the first burst of N-bit wide data signals includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein the circuitry includes a set of signal paths that are enabled before a first data bit of the set of consecutively transmitted data bits is transferred through the circuitry and disabled after a last data bit of the set of consecutively transmitted data bits is transferred through the circuitry.

24. (Currently Amended) The memory module of claim 22, wherein the logic is further configured to respond to a subsequent set of input address and control signals associated with a subsequent read or write memory command by outputting a subsequent set of registered address and control signals, the subsequent set of input address and control signals including a subsequent plurality of input chip select signals, the subsequent set of registered address and control signals including a subsequent plurality of registered chip select signals corresponding to respective ones of the subsequent plurality of input chip select signals, the subsequent plurality of registered chip select signals including a subsequently registered chip select signal having the active signal value and one or more other subsequently registered chip select signals each having the non-active signal value, wherein a second rank different from the first rank is configured to receive the subsequently registered chip select signal having the active signal value and to output or receive a second burst of N-bit wide data signals and a second burst of data strobes associated with the subsequent read or write command, wherein the circuitry is further configured to enable registered data transfers between the memory devices and the memory bus in response to the subsequent read/write memory command so that the second burst of N-bit wide data signals and the second burst of data strobes are transferred between the second rank and the memory bus through the circuitry.

25. (Previously Presented) The memory module of claim 17, wherein the memory devices are organized in four ranks and the first set of input address and control signals include four chip select signals, one for each of the four ranks.

26. (Previously Presented) The memory module of claim 17, wherein the circuitry includes logic pipelines configured to enable the data transfers between the first rank and the memory bus through the circuitry in response to the first control signals.

27. (Previously Presented) The memory module of claim 17, wherein the logic is further configured to report the overall CAS latency to the memory controller in response to a mode register set command received from the memory controller.

28. (Currently Amended) The memory module of claim 17, wherein the first burst of N-bit wide data signals and the first burst of data strobes are transferred between the first N-bit wide rank ~~of the memory devices~~ and the memory controller at a specified data rate.

29. (Previously Presented) The memory module of claim 20, wherein the first burst of N-bit wide data signals is transferred through the circuitry in a plurality of time intervals including at least a first time interval and a last time interval, wherein the circuitry includes a set of signal paths that are enabled before the first time interval and subsequently disabled after the last time interval.

30. (Previously Presented) The memory module of claim 29, wherein:

the first read or write memory command is a read memory command;

the second read or write memory command is a write memory command;

the set of signal paths are enabled to transfer the first burst of N-bit wide data signals and the first burst of data strobes a first number of time intervals after the read memory command is received by the logic; and

the set of signal paths are enabled to transfer the second burst of N-bit wide data signals and the second burst of data strobes a second number of time intervals after the write memory command is received by the logic, the second number being different from the first number.

31. (Currently Amended) The memory module of claim 22, wherein the first burst of N-bit wide data signals and the first burst of data strobes are transferred between the first N-bit wide rank ~~of the memory devices~~ and the memory controller at a specified data rate.

32. (Previously Presented) The memory module of claim 22, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.

33. (Previously Presented) The memory module of claim 32, wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock

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signal, and wherein each memory device in the first rank is configured receive or output a respective set of bits of the first burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the first burst of data strobes.

34. (Previously Presented) The memory module of claim 17, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.

35. (Previously Presented) The memory module of claim 34, wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the first rank is configured receive or output a respective set of bits of the first burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the first burst of data strobes.

36. (Previously Presented) The memory module of claim 1, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.

37. (Previously Presented) The memory module of claim 36, wherein the memory integrated circuits are dynamic random access memory integrated circuits configured to operate synchronously with the clock signal, wherein each memory integrated circuit in the first rank is configured receive or output a respective set of bits of the first burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the first burst of data strobes, and wherein each memory integrated circuit in the second rank is configured receive or output a respective set of bits of the second burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the second burst of data strobes.

REMARKS

This Amendment is in response to the Notice of Allowance dated September 6, 2019.

Claims 13, 17, 22, 24, 28, and 31 are amended to address possible antecedent basis issues. No new matter is added. Also, the amendments do not raise any new issue that would require additional search and examination.

CONCLUDING REMARKS

In light of the above amendments and remarks, the Applicant respectfully requests that the amendments be entered. The Examiner is invited to call the undersigned attorney at (650) 843-4000, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: September 30, 2019

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
Phone: (650) 843-4000

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Ex. 1054, p. 557

PART B - FEE(S) TRANSMITTAL

Electronically filed September 30, 2019

Complete and send this form with applicable fee(s), to: Mail
Mail Stop ISSUE FEE
Commissioner of Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571) 273-2885

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CURRENT CORRESPONDENCE ADDRESS

MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
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(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTY'S DOCKET NO.	CONFIRMATION NO.
15/857,519	12/28/2017	Jefferey C. Solomon	129980-5023-US	9826

TITLE OF INVENTION **MEMORY MODULE WITH DATA BUFFERING**

APPLN. TYPE	ENTITY STATUS	ISSUE FEE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	1000	0	1000	12/06/2019

EXAMINER	ART UNIT	CLASS-SUB CLASS
BANSAL, GURTEJ	2139	711-105000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed

1. **Morgan, Lewis & Bockius LLP**
2.
3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Netlist, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY) Irvine, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☐ Advanced Order - # of Copies ____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above.**)
☐ A check in the amount of the fee(s) enclosed
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☒ The Director is hereby authorized to charge the required fee(s), or credit any overpayment, to Deposit Account Number 50-0310 (order no. 129980-5023-US).

5. **Change in Small Entity Status** (from status indicated above)
☐ a. Applicant certifying micro entity status. See 37 CFR 1.29.
NOTE: Absent a valid certification of Micro Entity (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

☐ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be sign in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date: September 30, 2019

Printed Name: Jamie J. Zheng Registration No. 51,167

Electronic Patent Application Fee Transmittal

Application Number:	15857519
Filing Date:	28-Dec-2017
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Filer:	Jamie Jie Zheng/S. Olivier
Attorney Docket Number:	129980-5023US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1000**

Electronic Acknowledgement Receipt	
EFS ID:	37323987
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023US
Receipt Date:	30-SEP-2019
Filing Date:	28-DEC-2017
Time Stamp:	18:24:25
Application Type:	Utility under 35 USC 111(a)

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Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1000
RAM confirmation Number	E20199TI24466193
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5023US_312_AMEND.pdf	152249 f0b9bc54122c82b368fac6964f4ced7b3658dbde	yes	12
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Amendment after Notice of Allowance (Rule 312)		1	1	
	Claims		2	11	
	Applicant Arguments/Remarks Made in an Amendment		12	12	
Warnings:					
Information:					
2	Issue Fee Payment (PTO-85B)	129980-5023-US_Issue_Fee.pdf	110651 d15743583679862cf361eb6c1c19e2f83b5a2ab2	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30461 94ed3d455056cb575d8bb56870c6a8b4d2a6b582	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	293361		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/857,519	12/28/2017	Jefferey C. Solomon	129980-5023US	9826

79141 7590 10/23/2019

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER	
BANSAL, GURTEJ	

ART UNIT	PAPER NUMBER
2139	

NOTIFICATION DATE	DELIVERY MODE
10/23/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

padocketingdepartment@morganlewis.com
vskliba@morganlewis.com

Response to Rule 312 Communication	Application No.	Applicant(s)	
	15/857,519	Solomon et al.	
	Examiner	Art Unit	AIA (FITF) Status
	GURTEJ BANSAL	2139	No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☑ The amendment filed on 30 September 2019 under 37 CFR 1.312 has been considered, and has been:

a) ☐ entered.

b) ☑ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.

Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

OK TO ENTER: /G.B/

Electronically filed September 30, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Netlist, Inc.	Confirmation No.:	9826
Serial No.:	15/857,519	Art Unit:	2139
Filed:	December 28, 2017	Examiner:	BANSAL, Gurtej
For:	*MEMORY MODULE WITH DATA BUFFERING*	Attorney Docket No.:	129980-5023-US
		Date:	September 30, 2019

AMENDMENT UNDER 35 U.S.C. 312

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

In response to the Notice of Allowance dated September 6, 2019, Applicant files an Amendment under 35 U.S.C. 312 in the above-referenced patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US).

PTO/SB/08a/b(07-09)
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US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	22	of	40

Complete if Known	
Application Number	15/857,519
Filing Date	December 28, 2017
First Named Inventor	Jeffrey C. Solomon
Art Unit	2139
Examiner Name	Bansal, Gurtej
Attorney Docket Number	129980-5023-US

Change(s) applied to document,
/P.K./
11/5/2018

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	5388240 02-1995	~~02-01-1995~~	~~IBM Corporation~~	Olderdissen, et al.
	2.	5463590	10-31-1995	Watanabe	
	3.	5953280	09-14-1999	Matsui	
	4.	6188641	02-13-2001	Uchida	
	5.	6205516	03-20-2001	Usami	
	6.	6480439	11-12-2002	Tokutome et al.	
	7.	7464225	12-09-2008	Tsern	
	8.	7865674	01-04-2011	Gower et al.	
	9.	8089795	01-03-2012	Rajan	
	10.	8130560	03-06-2012	Rajan	
	11.	8189328	05-29-2012	Kanapathippillai	
	12.	8233303	07-31-2012	Best	
	13.	8250295	08-21-2012	Amidi et al.	
	14.	8417870	04-09-2013	Lee et al.	
	15.	8516185	08-20-2013	Lee et al.	
	16.	8516188	08-20-2013	Solomon et al.	
	17.	8756364	06-17-2014	Bhakta et al.	
	18.	20070058409	03-15-2007	Ruckerbauer	
	19.	20080104352	05-01-2008	Talbot	
	20.	20080104352	05-01-2008	Talbot	
	21.	RE36229	06-15-1999	Cady	

US PATENT APPLICATIONS

Examiner Initials *	Cite No. [1]	Application Number	Filing Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	22.	13/411,344	3/2/2012	Lee	Entire Prosecution History
	23.	13/970,606	8/20/2013	Netlist, Inc.	Entire Prosecution History
	24.	13/971,231	8/20/2013	Netlist, Inc.	Entire Prosecution History
	25.	14/229,844	3/29/2014	Netlist, Inc.	Entire Prosecution History
	26.	14/324,990	7/7/2014	Netlist, Inc.	Entire Prosecution History
	27.	14/337,168	7/21/2014	Netlist, Inc.	Entire Prosecution History

NON PATENT LITERATURE DOCUMENTS

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 6 of 40

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Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
Change(s) applied to document, /P.K./ 11/5/2018	137.	7047361	05-16-2006	~~Phison Electronics Corp~~	Chong, et al.
	138.	7054179	05-30-2006	Cogdill et al.	
	139.	7065626	06-20-2006	Schumacher et al.	
	140.	7072231	07-04-2006	Pax	
	141.	7073041	07-04-2006	Dwyer et al.	
	142.	7078793	07-18-2006	Ruckerbauer et al.	
	143.	7120727	10-10-2006	Lee et al.	
	144.	7124260	10-17-2006	LaBerge et al.	
	145.	7127584	10-24-2006	Thompson et al.	
	146.	7130952	10-31-2006	Nanki et al.	
	147.	7133960	11-07-2006	Thompson et al.	
	148.	7133972	11-07-2006	Jeddeloh	
	149.	7142461	11-28-2006	Janzen	
	150.	7149841	12-12-2006	LaBerge	
	151.	7167967	01-23-2007	Bungo et al.	
	152.	7181591	02-20-2007	Tsai	
	153.	7200021	04-03-2007	Raghuram	
	154.	7227910	06-05-2007	Lipka	
	155.	7266639	09-04-2007	Raghuram	
	156.	7272709	09-18-2007	Zitlaw et al.	
	157.	7281079	10-09-2007	Bains et al.	
	158.	7286436	10-23-2007	Bhakta et al.	
	159.	7289386	10-30-2007	Bhakta et al.	
	160.	7346750	03-18-2008	Ishikawa	
	161.	7356639	04-08-2008	Perego et al.	
	162.	7370238	05-06-2008	Billick et al.	
	163.	7437591	10-14-2008	Wong	
	164.	7461182	12-02-2008	Fukushima et al.	
	165.	7471538	12-30-2008	Hofstra	
	166.	7532537	05-12-2009	Solomon et al.	
	167.	7619912	11-17-2009	Bhakta et al.	
	168.	7636274	12-22-2009	Solomon et al.	
	169.	7864627	01-04-2011	Bhakta et al.	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 5 of 40

Complete if Known	
Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	102.	6681301	01-20-2004	Mehta et al.	
	103.	6683372	01-27-2004	Wong et al.	
	104.	6697888	02-24-2004	Halbert et al.	
	105.	6705877	03-16-2004	Li et al.	
	106.	6717885	04-06-2004	Lai	
	107.	6721843	04-13-2004	~~Lexar Media Inc~~	Estakhri
Change(s) applied to document, /P.K./ 11/5/2018	108.	6721860	04-13-2004	Klein	
	109.	6738880	05-18-2004	Lai et al.	
	110.	6742098	05-25-2004	Halbert et al.	
	111.	6754797	06-22-2004	Wu et al.	
	112.	6785189	08-31-2004	Jacobs et al.	
	113.	6788592	09-07-2004	Nakata et al.	
	114.	6807125	10-19-2004	Coteus et al.	
	115.	6807650	10-19-2004	Lamb et al.	
	116.	6813196	11-02-2004	Park et al.	
	117.	6832284	12-14-2004	Perego et al.	
	118.	6834014	12-21-2004	Yoo et al.	
	119.	6854042	02-08-2005	Karabatsos	
	120.	6880094	04-12-2005	LaBerge	
	121.	6889304	05-03-2005	Perego et al.	
	122.	6912615	06-28-2005	Nicolai	
	123.	6912628	06-28-2005	Wicki et al.	
	124.	6925028	08-02-2005	Hosokawa et al.	
	125.	6944694	09-13-2005	Pax	
	126.	6950366	09-27-2005	Lapidus et al.	
	127.	6954281	10-11-2005	Fukuda et al	
	128.	6961281	11-01-2005	Wong et al.	
	129.	6981089	12-27-2005	Dodd et al.	
	130.	6982892	01-03-2006	Lee et al.	
	131.	6982893	01-03-2006	Jakobs	
	132.	6990043	01-24-2006	Kuroda et al.	
	133.	6996686	02-07-2006	Doblar et al.	
	134.	7007130	02-28-2006	Holman	
	135.	7007175	02-28-2006	Chang et al.	
	136.	7046538	05-16-2006	Kinsley et al.	

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Sheet 4 of 40

Complete if Known	
Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	67.	6188641	02-13-2001	Uchida	
	68.	6205516	03-20-2001	Usami	
	69.	6209074	03-27-2001	Dell et al.	
	70.	6226709	05-01-2001	Goodwin et al.	
	71.	6226736	05-01-2001	Niot	
	72.	6233650	05-15-2001	Johnson et al.	
	73.	6247088	06-12-2001	Seo et al.	
	74.	6317352	11-13-2001	Halbert et al.	
Change(s) applied to document, /P.K/ 11/5/2018	75.	6349051	02-19-2002	~~Micron Technology Inc~~	Klein
	76.	6400637	06-04-2002	Akamatsu et al.	
	77.	6408356	06-18-2002	Dell	
	78.	6414868	07-02-2002	Wong et al.	
	79.	6415374	07-02-2002	Faue et al.	
	80.	6438062	08-20-2002	Karabatsos	
	81.	6438062	08-20-2002	Curtis	
	82.	6446158	09-03-2002	Karabatsos	
	83.	6446184	09-03-2002	Dell et al.	
	84.	6453381	09-17-2002	Yuan et al.	
	85.	6470417	10-22-2002	Kolor et al.	
	86.	6480439	11-12-2002	Tokutome et al.	
	87.	6487102	11-26-2002	Halbert et al.	
	88.	6502161	12-31-2002	Perego et al.	
	89.	6518794	02-11-2003	Coteus et al.	
	90.	6526473	02-25-2003	Kim	
	91.	6530007	03-04-2003	Olarig et al.	
	92.	6530033	03-04-2003	Raynham et al.	
	93.	6553450	04-22-2003	Dodd et al.	
	94.	6618320	09-09-2003	Hasegawa et al.	
	95.	6621496	09-16-2003	Ryan	
	96.	6625081	09-23-2003	Roohparvar et al.	
	97.	6625687	09-23-2003	Halbert et al.	
	98.	6636935	10-21-2003	Ware et al.	
	99.	6646949	11-11-2003	Ellis et al.	
	100.	6658509	12-02-2003	Bonella et al.	
	101.	6674684	01-06-2004	Shen	

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Sheet 3 of 40

Complete if Known	
Application Number	*15/857,519*
Filing Date	*December 28, 2017*
First Named Inventor	*Jeffrey C. Solomon*
Art Unit	*2139*
Examiner Name	*Bansal, Gurtej*
Attorney Docket Number	*129980-5023-US*

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
Change(s) applied to document /P.K./ 11/5/2018	34.	5638534	06-10-1997	~~Samsung Electronics Co Ltd~~	Mote, Jr.
	35.	5655153	08-05-1997	~~EMC CORP~~	Sandorfi
	36.	5699542	12-16-1997	Mehta et al.	
	37.	5702984	12-30-1997	Bertin et al.	
	38.	5703826	12-30-1997	Hush et al.	
	39.	5745914	04-28-1998	Connolly et al.	
	40.	5764590	06-09-1998	~~Mitsubishi Electric Corp~~	Iwamoto, et al.
	41.	5784705	07-21-1998	Leung, Wingyu	
	42.	5802395	09-01-1998	Connolly et al.	
	43.	5805520	09-08-1998	Anglada et al.	
	44.	5822251	10-13-1998	Bruce et al.	
	45.	5909388	06-01-1999	~~Siemens Ag~~	Mueller
	46.	5926827	07-20-1999	Dell et al.	
	47.	5926839	07-20-1999	~~IBM~~	Katayama
	48.	5953215	09-14-1999	Karabatsos, Chris	
	49.	5953280	09-14-1999	Watsui	
	50.	5958025	09-28-1999	~~Nippon Electric Co~~	Sonobe
	51.	5959930	09-28-1999	Sakurai	
	52.	5963464	10-05-1999	Dell et al.	
	53.	5966736	10-12-1999	Gittinger et al.	
	54.	5974493	10-26-1999	~~Mitsubishi Electric Corp~~	Okumura, et al.
	55.	6018787	01-25-2000	Ip	
	56.	6044032	03-28-2000	Li	
	57.	6070217	05-30-2000	Connolly et al.	
	58.	6070227	05-30-2000	Rokicki	
	59.	6097652	08-01-2000	Roh	
	60.	6108745	08-22-2000	Gupta et al.	
	61.	6115278	09-05-2000	Deneroff et al.	
	62.	6134638	10-17-2000	Olarig et al.	
	63.	6151271	11-21-2000	Lee	
	64.	6154418	11-28-2000	Li	
	65.	6154419	11-28-2000	Shakkarwar	
	66.	6185654	02-06-2001	Van Doren	

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Sheet 2 of 40

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Filing Date	December 28, 2017
First Named Inventor	Jeffrey C. Solomon
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Attorney Docket Number	129980-5023-US

Change(s) applied to document, /P.K./ 11/5/2018

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	4218740	08-19-1980	~~MOTOROLA INC~~	Bennett, et al.
	2.	4249253	02-03-1981	Gentili et al.	
	3.	4368515	01-11-1983	Nielsen	
	4.	4392212	07-05-1983	Miyasaka et al.	
	5.	4571676	02-18-1986	Mantellina et al.	
	6.	4592011	05-27-1986	Mantellina et al.	
	7.	4633429	12-30-1986	Lewandowski et al.	
	8.	4670748	06-02-1987	Williams	
	9.	4706214	11-10-1987	~~Mitsubishi Denki Kabushiki Kaisha~~	Kassai
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	11.	4958322	09-18-1990	Kosugi et al.	
	12.	4961172	10-02-1990	Shubat et al.	
	13.	4961204	10-02-1990	~~Hitachi Ltd~~	Tanaka, et al.
	14.	4980850	12-25-1990	Morgan	
	15.	5060188	10-22-1991	Zulian et al.	
	16.	5247643	09-21-1993	Shottan	
	17.	5272664	12-21-1993	~~Silicon Graphics Inc~~	Alexander, et al.
	18.	5345412	09-06-1994	Shiratsuchi	
	19.	5357478	10-18-1994	~~Mitsubishi Electric Corp~~	Kikuda, et al.
	20.	5388072	02-07-1995	~~IBM~~	Matick, et al.
	21.	5392252	02-21-1995	~~Visi Technology Inc~~	Rimpo, et al.
	22.	5426753	06-20-1995	Moon	
	23.	5463590	10-31-1995	Watanabe	
	24.	5483497	01-09-1996	Mochizuki et al.	
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	26.	5495435	02-27-1996	Sugahara	
	27.	5513135	04-30-1996	Dell et al.	
	28.	5532954	07-02-1996	Bechtolsheim et al.	
	29.	5541448	07-30-1996	Carpenter	
	30.	5572691	11-05-1996	Koudmani	
	31.	5581498	12-03-1996	Ludwig et al.	
	32.	5590071	12-31-1996	Kolor et al.	
	33.	5602999	02-11-1997	Hyatt; Gilbert P.	

EXAMINER /GURTEJ BANSAL/ DATE CONSIDERED 09/27/2018

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.[1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/857,519	11/26/2019	10489314	129980-5023US	9826

79141 7590 11/06/2019

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Netlist, Inc., Irvine, CA;
Jefferey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

Electronically filed February 14, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent:	Solomon et al.	Confirmation No.:	9826
Patent No.:	10,489,314	Serial No.:	15/857,519
Issued:	November 26, 2019	Filed:	December 28, 2017
For:	MEMORY MODULE WITH DATA BUFFERING	Attorney Docket No:	129980-5023-US

REQUEST FOR CERTIFICATE OF CORRECTION

Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

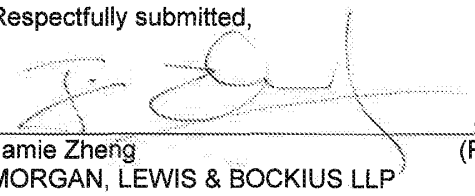
Sir:

Upon review of the subject patent, Patentee's attorney discovered 4 errors on the part of the Applicant. Patentee's attorney requests correction of the issued patent. A Form PTO 1050 Certificate of Correction is enclosed.

The Commissioner is authorized to charge any required fees to our Deposit Account No. 50-0310 (order no. 129980-5023-US).

Respectfully submitted,

Date: February 14, 2020



Jamie Zheng (Reg. No. 51,167)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, California 94304
(650) 843-4000

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.	:	10,489,314
APPLICATION NO.	:	15/857,519
ISSUE DATE	:	November 26, 2019
INVENTOR(S)	:	Solomon et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims, Claim 2, Column 43, Line 2, please delete "plurality memory" and insert --plurality of memory--;

In the Claims, Claim 14, Column 44, Line 39, please delete "configured receive" and insert --configured to receive--;

In the Claims, Claim 14, Column 44, Line 43, please delete "configured receive" and insert --configured to receive--;

In the Claims, Claim 33, Column 48, Lines 45-46, please delete "configured receive" and insert --configured to receive--.

MAILING ADDRESS OF SENDER:
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

Electronic Patent Application Fee Transmittal

Application Number:	15857519
Filing Date:	28-Dec-2017
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Filer:	Jamie Jie Zheng/Deborah Carney
Attorney Docket Number:	129980-5023US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
CERTIFICATE OF CORRECTION	1811	1	150	150

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**150**

Electronic Acknowledgement Receipt	
EFS ID:	38588778
Application Number:	15857519
International Application Number:	
Confirmation Number:	9826
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/Deborah Carney
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023US
Receipt Date:	14-FEB-2020
Filing Date:	28-DEC-2017
Time Stamp:	10:35:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$150
RAM confirmation Number	E20202DA36488969
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	129982-5023US_COC.pdf	69759 5504e3d8cc5c746248fbc4621446762052cc4ace	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30430 232d1a84bef12876a11c1a48ef0b5ecb4d233069	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	100189		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.	: 10,489,314 B2
APPLICATION NO.	: 15/857519
DATED	: November 26, 2019
INVENTOR(S)	: Solomon et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims

Claim 2, Column 43, Line 2, please delete “plurality memory” and insert --plurality of memory--;

Claim 14, Column 44, Line 39, please delete “configured receive” and insert --configured to receive--;

Claim 14, Column 44, Line 43, please delete “configured receive” and insert --configured to receive--;

Claim 33, Column 48, Lines 45-46, please delete “configured receive” and insert --configured to receive--.

Signed and Sealed this
Seventeenth Day of March, 2020

Andrei Iancu
Director of the United States Patent and Trademark Office

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. ƒ 290 and/or 15 U.S.C. ƒ 1116 you are hereby advised that a court action has been filed in the U.S. District Court **Western District of Texas** on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. ƒ 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:21-cv-00431	4/28/2021	Western District of Texas

PLAINTIFF	DEFENDANT
Netlist, Inc.	Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	10,489,314	11/26/2019	Netlist, Inc.
2	9,824,035	11/21/2017	Netlist, Inc.
3	10,268,608	4/23/2019	Netlist, Inc.
4			
5			

In the above´ entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above´ entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1´ Upon initiation of action, mail this copy to Director Copy 3´ Upon termination of action, mail this copy to Director
Copy 2´ Upon filing document adding patent(s), mail this copy to Director Copy 4´ Case file copy