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APPLICATION ELEMENTS
See MPEP Chapter 600 concerning utility patent application contents.

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1. ☐ Fee Transmittal Form *(with duplicate for fee processing)*
2. ☐ Applicant claims Small Entity status, see 37 C.F.R. § 1.27
3. ☒ Specification [Total Pages 57]
4. ☒ Drawing(s) *(35 USC § 113)* [Total Sheets 23]
5. ☒ Oath or Declaration [Total Pages 1]
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ACCOMPANYING APPLICATION PARTS

9. ☐ Assignment Papers *(cover sheet & document(s))*
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10. ☒ 37 CFR § 3.73(c) Statement
    a. ☒ Power of Attorney
11. ☐ English Translation Document *(if applicable)*
12. ☐ Information Disclosure Statement and PTO-1449
    a. ☐ Copies of citations attached
13. ☐ Preliminary Amendment
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16. ☐ Non-Publication Request under 35 U.S.C. § 122 (b)(2)(B)(i)
17. ☐ Other:

Note: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **MUST** be included in an Application Data Sheet (ADS).

(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS: Customer Number 79141

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MEMORY MODULE WITH DATA BUFFERING

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a continuation of U.S. Pat. Appl. No. 15/857,519, filed December 28, 2017, which is a continuation of U.S. Pat. Appl. No. 14/715,486, filed May 18, 2015, (U.S. Pat. No. 9,858,215), which is a continuation of U.S. Pat. Appl. No. 13/971,231, filed August 20, 2013, (Pat. No. 9,037,774), which is a continuation of U.S. Pat. Appl. No. 13/287,081, filed November 1, 2011, (U.S. Pat. No. 8,516,188), which is a continuation of U.S. Pat. Appl. No. 13/032,470, filed February 22, 2011, (U.S. Pat. No. 8,081,536), which is a continuation of U.S. Pat. Appl. No. 12/955,711, filed November 29, 2010, (U.S. Pat. No. 7,916,574), which is a continuation of U.S. Pat. Appl. No. 12/629,827, filed December 2, 2009, (U.S. Pat. No. 7,881,150), which is a continuation of U.S. Pat. Appl. No. 12/408,652, filed March 20, 2009, (U.S. Pat. No. 7,636,274), which is a continuation of U.S. Pat. Appl. No. 11/335,875, filed January 19, 2006, (U.S. Pat. No. 7,532,537), which claims the benefit of U.S. Provisional Appl. No. 60/645,087, filed January 19, 2005 and which is a continuation-in-part of U.S. Pat. Appl. No. 11/173,175, filed July 1, 2005, (U.S. Pat. No. 7,289,386), which claims the benefit of U.S. Provisional Appl. No. 60/588,244, filed July 15, 2004 and which is a continuation-in-part of U.S. Pat. Appl. No. 11/075,395, filed March 7, 2005, (U.S. Pat. No. 7,286,436), which claims the benefit of U.S. Provisional Appl. No. 60/550,668, filed March 5, 2004, U.S. Provisional Appl. No. 60/575,595, filed May 28, 2004, and U.S. Provisional Appl. No. 60/590,038, filed July 21, 2004. U.S. Pat. Appl. Nos. 15/857,519, 14/715,486, 13/287,081, 13/032,470, 12/955,711, 12/629,827, 12/408,652, 11/335,875, 11/173,175, and 11/075,395, and U.S. Provisional Appl. Nos. 60/550,668, 60/575,595, 60/590,038, 60/588,244, and 60/645,087 are each incorporated in its entirety by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules.

2. Description of the Related Art

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[0003] Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the processor of the computer system. Memory modules typically have a memory configuration with a unique combination of rows, columns, and banks which result in a total memory capacity for the memory module.

[0004] For example, a 512-Megabyte memory module (termed a "512-MB" memory module, which actually has 2^{29} or 536,870,912 bytes of capacity) will typically utilize eight 512-Megabit DRAM devices (each identified as a "512-Mb" DRAM device, each actually having 2^{29} or 536,870,912 bits of capacity). The memory cells (or memory locations) of each 512-Mb DRAM device can be arranged in four banks, with each bank having an array of 2^{24} (or 16,777,216) memory locations arranged as 2^{13} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 64 M 8-bit-wide memory locations (actually with four banks of 2^{27} or 134,217,728 one-bit memory cells arranged to provide a total of 2^{26} or 67,108,864 memory locations with 8 bits each) are identified as having a "64 Mb×8" or "64 M×8-bit" configuration, or as having a depth of 64 M and a bit width of 8. Furthermore, certain commercially-available 512-MB memory modules are termed to have a "64 M×8-byte" configuration or a "64 M×64-bit" configuration with a depth of 64 M and a width of 8 bytes or 64 bits.

[0005] Similarly, a 1-Gigabyte memory module (termed a "1-GB" memory module, which actually has 2^{30} or 1,073,741,824 bytes of capacity) can utilize eight 1-Gigabit DRAM devices (each identified as a "1-Gb" DRAM device, each actually having 2^{30} or 1,073,741,824 bits of capacity). The memory locations of each 1-Gb DRAM device can be arranged in four banks, with each bank having an array of memory locations with 2^{14} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 128 M 8-bit-wide memory locations (actually with a total of 2^{27} or 134,217,728 memory locations with 8 bits each) are identified as having a "128 Mb×8" or "128 M×8-bit" configuration, or as having a depth of 128 M and a bit width of 8. Furthermore, certain commercially-available 1-GB memory modules are identified as having a "128 M×8-byte" configuration or a "128 M×64-bit" configuration with a depth of 128 M and a width of 8 bytes or 64 bits.

[0006] The commercially-available 512-MB (64 M×8-byte) memory modules and

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the 1-GB (128 M×8-byte) memory modules described above are typically used in computer systems (e.g., personal computers) which perform graphics applications since such "×8" configurations are compatible with data mask capabilities often used in such graphics applications. Conversely, memory modules with "×4" configurations are typically used in computer systems such as servers which are not as graphics-intensive. Examples of such commercially available "×4" memory modules include, but are not limited to, 512-MB (128 M×4-byte) memory modules comprising eight 512-Mb (128 Mb×4) memory devices.

[0007] The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "×64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "×72" organization.

[0008] The memory capacity of a memory module increases with the number of memory devices. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks. For example, a memory module with four ranks has double the memory capacity of a memory module with two ranks and four times the memory capacity of a memory module with one rank. Rather than referring to the memory capacity of the memory module, in certain circumstances, the memory density of the memory module is referred to instead.

[0009] During operation, the ranks of a memory module are selected or activated by address and command signals that are received from the processor. Examples of such address and command signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support one-rank and two-rank memory modules. By only supporting one-rank and two-rank memory modules, the memory density that can be incorporated in each memory slot is limited.

[0010] Various aspects of the design of a memory module impose limitations on the size of the memory arrays of the memory module. Certain such aspects are particularly important for memory modules designed to operate at higher frequencies. Examples of such aspects include, but are not limited to, memory device (e.g., chip) densities, load fan-out, signal integrity, available rank selects, power dissipation, and thermal profiles.

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SUMMARY OF THE INVENTION

[0011] A memory module is operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller. The memory bus includes address and control signal lines and data signal lines. According to some embodiments, the memory module comprises a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, and memory devices mounted on the printed circuit board.

[0012] In some embodiments, the memory module further comprises logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines, and to output a set of registered address and control signals in response to the set of input address and control signals. The set of input address and control signals includes a plurality of input chip select signals in addition to other input address and control signals. The plurality of input chip select signals includes one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value. The set of registered address and control signals includes a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals, in addition to other registered address and control signals corresponding to respective ones of the other input address and control signals. The plurality of registered chip select signals includes one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value. The logic is further configurable to output data buffer control signals in response to the read or write memory command.

[0013] In some embodiments, the memory devices are arranged in a plurality of N-bit wide ranks. The plurality of ranks are configured to receive respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by one respective N-bit wide rank of the plurality of N-bit-wide ranks. One of the plurality of ranks receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command.

[0014] In some embodiments, the memory module further comprises circuitry

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coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks. The circuitry is configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module. In some embodiments, data transfers through the circuitry are registered for an additional amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

[0015] In some embodiments, the memory module further comprises a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, and the predetermined amount of time delay is at least one clock cycle time delay. In some embodiments, the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the one of the plurality of ranks is configured receive or output a respective set of bits of the first burst of N-bit wide data signals on both edges of each of a respective set of data strobes.

[0016] In some embodiments, the circuitry includes data paths, and the circuitry is configured to enable the data paths in response to the data buffer control signals so that the N-bit wide data signals are transferred via the data paths. In some embodiments, the data paths are disabled when no data signals associated with any memory command are being transferred through the circuitry. In some embodiments, the read or write command is a write memory command, wherein the burst of N-bit wide data signals include a respective series of write data bits received by the circuitry from a respective one of the data signal lines, and wherein the respective series of write data bits are successively transferred via a respective one of the data paths.

[0017] In some embodiments, each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus.

[0018] In some embodiments, the memory module has a specified data rate, and wherein the burst of N-bit wide data signals are transferred through the data paths at the specified data rate.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0019] FIG. 1 schematically illustrates an example memory module in accordance with certain embodiments described herein.

[0020] FIG. 2 schematically illustrates a circuit diagram of two memory devices of a conventional memory module.

[0021] FIGS. 3A and 3B schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two memory devices from the computer system in accordance with certain embodiments described herein.

[0022] FIGS. 4A and 4B schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two ranks of memory devices from the computer system in accordance with certain embodiments described herein.

[0023] FIGS. 5A-5D schematically illustrate example memory modules having a circuit comprising a logic element and one or more switches operatively coupled to the logic element in accordance with certain embodiments described herein.

[0024] FIG. 6A shows an exemplary timing diagram of a gapless read burst for a back-to-back adjacent read condition from one memory device.

[0025] FIG. 6B shows an exemplary timing diagram with an extra clock cycle between successive read commands issued to different memory devices for successive read accesses from different memory devices.

[0026] FIG. 7 shows an exemplary timing diagram in which the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b."

[0027] FIGS. 8A-8D schematically illustrate circuit diagrams of example memory modules comprising a circuit which multiplexes the DQS data strobe signal lines from one another in accordance with certain embodiments described herein.

[0028] FIG. 9A schematically illustrates an example memory module with four ranks of memory devices compatible with certain embodiments described herein.

[0029] FIG. 9B schematically illustrates an example memory module with two

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ranks of memory devices compatible with certain embodiments described herein.

[0030] FIG. 9C schematically illustrates another example memory module in accordance with certain embodiments described herein.

[0031] FIG. 10A schematically illustrates an exemplary memory module which doubles the rank density in accordance with certain embodiments described herein.

[0032] FIG. 10B schematically illustrates an exemplary circuit compatible with embodiments described herein.

[0033] FIG. 11A schematically illustrates an exemplary memory module which doubles number of ranks in accordance with certain embodiments described herein.

[0034] FIG. 11B schematically illustrates an exemplary circuit compatible with embodiments described herein.

[0035] FIG. 12 schematically illustrates an exemplary memory module in which a data strobe (DQS) pin of a first memory device is electrically connected to a DQS pin of a second memory device while both DQS pins are active.

[0036] FIG. 13 is an exemplary timing diagram of the voltages applied to the two DQS pins due to non-simultaneous switching.

[0037] FIG. 14 schematically illustrates another exemplary memory module in which a DQS pin of a first memory device is connected to a DQS pin of a second memory device.

[0038] FIG. 15 schematically illustrates an exemplary memory module in accordance with certain embodiments described herein.

[0039] FIGS. 16A and 16B schematically illustrate a first side and a second side, respectively, of a memory module with eighteen 64 M×4 bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board.

[0040] FIGS. 17A and 17B schematically illustrate an exemplary embodiment of a memory module in which a first resistor and a second resistor are used to reduce the current flow between the first DQS pin and the second DQS pin.

[0041] FIG. 18 schematically illustrates another exemplary memory module

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compatible with certain embodiments described herein.

[0042] FIG. 19 schematically illustrates a particular embodiment of the memory module schematically illustrated by FIG. 18.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Load Isolation

[0043] FIG. 1 schematically illustrates an example memory module **10** compatible with certain embodiments described herein. The memory module **10** is connectable to a memory controller **20** of a computer system (not shown). The memory module **10** comprises a plurality of memory devices **30**, each memory device **30** having a corresponding load. The memory module **10** further comprises a circuit **40** electrically coupled to the plurality of memory devices **30** and configured to be electrically coupled to the memory controller **20** of the computer system. The circuit **40** selectively isolates one or more of the loads of the memory devices from the computer system. The circuit **40** comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module **10**.

[0044] As used herein, the term "load" is a broad term which includes, without limitation, electrical load, such as capacitive load, inductive load, or impedance load. As used herein, the term "isolation" is a broad term which includes, without limitation, electrical separation of one or more components from another component or from one another. As used herein, the term "circuit" is a broad term which includes, without limitation, an electrical component or device, or a configuration of electrical components or devices which are electrically or electromagnetically coupled together (e.g., integrated circuits), to perform specific functions.

[0045] Various types of memory modules **10** are compatible with embodiments described herein. For example, memory modules **10** having memory capacities of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, as well as other capacities, are compatible with embodiments described herein. Certain embodiments described herein are applicable to various frequencies including, but not limited to 100 MHz, 200 MHz, 400 MHz, 800 MHz, and above. In addition, memory modules **10** having widths of 4 bytes, 8 bytes, 16 bytes, 32bytes, or 32bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments

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described herein. In certain embodiments, the memory module **10** comprises a printed circuit board on which the memory devices **30** are mounted, a plurality of edge connectors configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, and a plurality of electrical conduits which electrically couple the memory devices **30** to the circuit **40** and which electrically couple the circuit **40** to the edge connectors. Furthermore, memory modules **10** compatible with embodiments described herein include, but are not limited to, single in-line memory modules (SIMMs), dual in-line memory modules (DIMMs), small-outline DIMMs (SO-DIMMs), unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), fully-buffered DIMM (FBDIMM), rank-buffered DIMMs (RBDIMMs), mini-DIMMs, and micro-DIMMs.

[0046] Memory devices **30** compatible with embodiments described herein include, but are not limited to, random-access memory (RAM), dynamic random-access memory (DRAM), synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., SDR, DDR-1, DDR-2, DDR-3). In addition, memory devices **30** having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein. Memory devices **30** compatible with embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP). Memory devices **30** compatible with embodiments described herein are available from a number of sources, including but not limited to, Samsung Semiconductor, Inc. of San Jose, Calif., Infineon Technologies AG of San Jose, Calif., and Micron Technology, Inc. of Boise, Id. Persons skilled in the art can select appropriate memory devices **30** in accordance with certain embodiments described herein.

[0047] In certain embodiments, the plurality of memory devices **30** comprises a first number of memory devices **30**. In certain such embodiments, the circuit **40** selectively isolates a second number of the memory devices **30** from the computer system, with the second number less than the first number.

[0048] In certain embodiments, the plurality of memory devices **30** are arranged in a first number of ranks. For example, in certain embodiments, the memory devices **30** are arranged in two ranks, as schematically illustrated by FIG. 1. In other embodiments, the memory devices **30** are arranged in four ranks. Other numbers of ranks of the memory devices

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30 are also compatible with embodiments described herein.

[0049] In certain embodiments, the circuit comprises a logic element selected from a group consisting of: a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, and a complex programmable-logic device (CPLD). In certain embodiments, the logic element of the circuit **40** is a custom device. Sources of logic elements compatible with embodiments described herein include, but are not limited to, Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif. In certain embodiments, the logic element comprises various discrete electrical elements, while in certain other embodiments, the logic element comprises one or more integrated circuits.

[0050] In certain embodiments, the circuit **40** further comprises one or more switches which are operatively coupled to the logic element to receive control signals from the logic element. Examples of switches compatible with certain embodiments described herein include, but are not limited to, field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex.

[0051] FIG. 2 schematically illustrates a circuit diagram of two memory devices **30a, 30b** of a conventional memory module showing the interconnections between the DQ data signal lines **102a**, **102b** of the memory devices **30a, 30b** and the DQS data strobe signal lines **104a**, **104b** of the memory devices **30a, 30b**. Each of the memory devices **30a, 30b** has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, however, for simplicity, FIG. 2 only illustrates a single DQ data signal line and a single DQS data strobe signal line for each memory device **30a, 30b**. The DQ data signal lines **102a**, **102b** and the DQS data strobe signal lines **104a**, **104b** are typically conductive traces etched on the printed circuit board of the memory module. As shown in FIG. 2, each of the memory devices **30a, 30b** has their DQ data signal lines **102a**, **102b** electrically coupled to a common DQ line **112** and their DQS data strobe signal lines **104a**, **104b** electrically coupled to a common DQS line **114**. The common DQ line **112** and the common DQS line **114** are electrically coupled to the memory controller **20** of the computer system. Thus, the computer system is exposed to the loads of both memory devices **30a, 30b** concurrently.

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[0052] In certain embodiments, the circuit **40** selectively isolates the loads of at least some of the memory devices **30** from the computer system. The circuit **40** of certain embodiments is configured to present a significantly reduced load to the computer system. In certain embodiments in which the memory devices **30** are arranged in a plurality of ranks, the circuit **40** selectively isolates the loads of some (e.g., one or more) of the ranks of the memory module **10** from the computer system. In certain other embodiments, the circuit **40** selectively isolates the loads of all of the ranks of the memory module **10** from the computer system. For example, when a memory module **10** is not being accessed by the computer system, the capacitive load on the memory controller **20** of the computer system by the memory module **10** can be substantially reduced to the capacitive load of the circuit **40** of the memory module **10**.

[0053] As schematically illustrated by FIGS. 3A and 3B, an example memory module **10** compatible with certain embodiments described herein comprises a circuit **40** which selectively isolates one or both of the DQ data signal lines **102a**, **102b** of the two memory devices **30a, 30b** from the common DQ data signal line **112** coupled to the computer system. Thus, the circuit **40** selectively allows a DQ data signal to be transmitted from the memory controller **20** of the computer system to one or both of the DQ data signal lines **102a**, **102b**. In addition, the circuit **40** selectively allows one of a first DQ data signal from the DQ data signal line **102a** of the first memory device **30a** or a second DQ data signal from the DQ data signal line **102b** of the second memory device **30b** to be transmitted to the memory controller **20** via the common DQ data signal line **112** (see, e.g., triangles on the DQ and DQS lines of FIGS. 3A and 3B which point towards the memory controller). While various figures of the present application denote read operations by use of DQ and DQS lines which have triangles pointing towards the memory controller, certain embodiments described herein are also compatible with write operations (e.g., as would be denoted by triangles on the DQ or DQS lines pointing away from the memory controller).

[0054] For example, in certain embodiments, the circuit **40** comprises a pair of switches **120** *a*, **120** *b* on the DQ data signal lines **102a**, **102b** as schematically illustrated by FIG. 3A. Each switch **120** *a*, **120** *b* is selectively actuated to selectively electrically couple the DQ data signal line **102a** to the common DQ signal line **112**, the DQ data signal line **102b** to the common DQ signal line **112**, or both DQ data signal lines **102a**, **102b** to the common DQ

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signal line **112**. In certain other embodiments, the circuit **40** comprises a switch **120** electrically coupled to both of the DQ data signal lines **102a**, **102b**, as schematically illustrated by FIG. 3B. The switch **120** is selectively actuated to selectively electrically couple the DQ data signal line **102a** to the common DQ signal line **112**, the DQ data signal line **102b** to the common DQ signal line **112**, or both DQ signal lines **102a**, **102b** to the common DQ signal line **112**. Circuits **40** having other configurations of switches are also compatible with embodiments described herein. While each of the memory devices **30a, 30b** has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, FIGS. 3A and 3B only illustrate a single DQ data signal line and a single DQS data strobe signal line for each memory device **30a, 30b** for simplicity. The configurations schematically illustrated by FIGS. 3A and 3B can be applied to all of the DQ data signal lines and DQS data strobe signal lines of the memory module **10**.

[0055] In certain embodiments, the circuit **40** selectively isolates the loads of ranks of memory devices **30** from the computer system. As schematically illustrated in FIGS. 4A and 4B, example memory modules **10** compatible with certain embodiments described herein comprise a first number of memory devices **30** arranged in a first number of ranks **32**. The memory modules **10** of FIGS. 4A and 4B comprises two ranks **32a**, **32b**, with each rank **32a**, **32b** having a corresponding set of DQ data signal lines and a corresponding set of DQS data strobe lines. Other numbers of ranks (e.g., four ranks) of memory devices **30** of the memory module **10** are also compatible with certain embodiments described herein. For simplicity, FIGS. 4A and 4B illustrate only a single DQ data signal line and a single DQS data strobe signal line from each rank **32**.

[0056] The circuit **40** of FIG. 4A selectively isolates one or more of the DQ data signal lines **102a**, **102b** of the two ranks **32a**, **32b** from the computer system. Thus, the circuit **40** selectively allows a DQ data signal to be transmitted from the memory controller **20** of the computer system to the memory devices **30** of one or both of the ranks **32a**, **32b** via the DQ data signal lines **102a**, **102b**. In addition, the circuit **40** selectively allows one of a first DQ data signal from the DQ data signal line **102a** of the first rank **32a** and a second DQ data signal from the DQ data signal line **102b** of the second rank **32b** to be transmitted to the memory controller **20** via the common DQ data signal line **112**. For example, in certain embodiments, the circuit **40** comprises a pair of switches **120** *a*, **120** *b* on the DQ data signal lines **102a**, **102b** as schematically illustrated by FIG. 4A. Each switch **120** *a*, **120** *b* is selectively actuated to

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selectively electrically couple the DQ data signal line **102a** to the common DQ data signal line **112**, the DQ data signal line **102b** to the common DQ data signal line **112**, or both DQ data signal lines **102a**, **102b** to the common DQ data signal line **112**. In certain other embodiments, the circuit **40** comprises a switch **120** electrically coupled to both of the DQ data signal lines **102a**, **102b**, as schematically illustrated by FIG. 4B. The switch **120** is selectively actuated to selectively electrically couple the DQ data signal line **102a** to the common DQ data signal line **112**, the DQ data signal line **102b** to the common DQ data signal line **112**, or both DQ data signal lines **102a**, **102b** to the common DQ data signal line **112**. Circuits **40** having other configurations of switches are also compatible with embodiments described herein.

[0057] In the example embodiments schematically illustrated by FIGS. 3A, **3**B, **4**A, and **4**B, the circuit **40** comprises a logic element which is integral with and comprises the switches **120** which are coupled to the DQ data signal lines and the DQS data strobe signal lines. In certain such embodiments, each switch **120** comprises a data path multiplexer/demultiplexer. In certain other embodiments, the circuit **40** comprises a logic element **122** which is a separate component operatively coupled to the switches **120**, as schematically illustrated by FIGS. 5A-5D. The one or more switches **120** are operatively coupled to the logic element **122** to receive control signals from the logic element **122** and to selectively electrically couple one or more data signal lines to a common data signal line. Example switches compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex. Example logic elements **122** compatible with certain embodiments described herein include, but are not limited to, programmable-logic devices (PLD), application-specific integrated circuits (ASIC), field-programmable gate arrays (FPGA), custom-designed semiconductor devices, and complex programmable-logic devices (CPLD). Example logic elements **122** are available from Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif.

[0058] In certain embodiments, the load isolation provided by the circuit **40** advantageously allows the memory module **10** to present a reduced load (e.g., electrical load, such as capacitive load, inductive load, or impedance load) to the computer system by selectively switching between the two ranks of memory devices **30** to which it is coupled. This

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feature is used in certain embodiments in which the load of the memory module **10** may otherwise limit the number of ranks or the number of memory devices per memory module. In certain embodiments, the memory module **10** operates as having a data path rank buffer which advantageously isolates the ranks of memory devices **30** of the memory module **10** from one another, from the ranks on other memory modules, and from the computer system. This data path rank buffer of certain embodiments advantageously provides DQ-DQS paths for each rank or sets of ranks of memory devices which are separate from one another, or which are separate from the memory controller of the computer system. In certain embodiments, the load isolation advantageously diminishes the effects of capacitive loading, jitter and other sources of noise. In certain embodiments, the load isolation advantageously simplifies various other aspects of operation of the memory module **10**, including but not limited to, setup-and-hold time, clock skew, package skew, and process, temperature, voltage, and transmission line variations.

[0059] For certain memory module applications that utilize multiple ranks of memory, increased load on the memory bus can degrade speed performance. In certain embodiments described herein, selectively isolating the loads of the ranks of memory devices **30** advantageously decreases the load on the computer system, thereby allowing the computer system (e.g., server) to run faster with improved signal integrity. In certain embodiments, load isolation advantageously provides system memory with reduced electrical loading, thereby improving the electrical topology to the memory controller **20**. In certain such embodiments, the speed and the memory density of the computer system are advantageously increased without sacrificing one for the other.

[0060] In certain embodiments, load isolation advantageously increases the size of the memory array supported by the memory controller **20** of the computer system. The larger memory array has an increased number of memory devices **30** and ranks of memory devices **30** of the memory module **10**, with a corresponding increased number of chip selects. Certain embodiments described herein advantageously provide more system memory using fewer chip selects, thereby avoiding the chip select limitation of the memory controller.

[0061] An exemplary section of Verilog code corresponding to logic compatible with a circuit **40** which provides load isolation is listed below in Example 1. The exemplary code of Example 1 corresponds to a circuit **40** comprising six FET switches for providing load isolation to DQ and DQS lines.

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[0062] Example 1

```
//=================================== declarations
  reg                   rasN_R, casN_R, weN_R;
  wire                  actv_cmd_R, pch_cmd_R, pch_all_cmd_R, ap_xfr_cmd_R_R;
  wire                  xfr_cmd_R,mrs_cmd,rd_cmd_R;

//- - - - - - - - - - - - - - - - - - - - - - - - DDR 2 FET
  reg                   brs0N_R;                    // registered chip sel
  reg                   brs1N_R;                    // registered chip sel
  reg                   brs2N_R;                    // registered chip sel
  reg                   brs3N_R;                    // registered chip sel
  wire                  sel;
  wire                  sel_01;
  wire                  sel_23;
  wire                  rd_R1;
  wire                  wr_cmd_R,wr_R1;
  reg                   rd_R2,rd_R3,rd_R4,rd_R5;
  reg                   wr_R2,wr_R3,wr_R4,wr_R5;
  reg                   enfet1,enfet2,enfet3,enfet4,enfet5,enfet6;
  wire                  wr_01_R1,wr_23_R1;
  reg                   wr_01_R2,wr_01_R3,wr_01_R4;
  reg                   wr_23_R2,wr_23_R3,wr_23_R4;
  wire                  rodt0_a,rodt0_b;

//=================================== logic
  always @(posedge clk_in)
        begin
                brs0N_R <= brs0_in_N;    // cs0
                brs1N_R <= brs1_in_N;    // cs1
                brs2N_R <= brs2_in_N;    // cs2
                brs3N_R <= brs3_in_N;    // cs3
                rasN_R  <= brras_in_N ;
                casN_R  <= brcas_in_N ;
                weN_R   <= bwe_in_N ;
        end
assign sel = ~brs0N_R | ~brs1N_R | ~brs2N_R | ~brs3N_R ;
assign sel_01 = ~brs0N_R | ~brs1N_R ;
assign sel_23 = ~brs2N_R | ~brs3N_R ;
assign actv_cmd_R = !rasN_R & casN_R & weN_R; // activate cmd
assign pch_cmd_R = !rasN_R & casN_R & !weN_R ;// pchg cmd
assign xfr_cmd_R = rasN_R & !casN_R;                  // xfr cmd
assign mrs_cmd = !rasN_R & !casN_R & !weN_R ;   // md reg set cmd
assign rd_cmd_R = rasN_R & !casN_R & weN_R ;    // read cmd
assign wr_cmd_R = rasN_R & !casN_R & !weN_R ; // write cmd
//-----------------------------------
assign    rd_R1 = sel & rd_cmd_R;  // rd cmd cyc 1
assign    wr_R1 = sel & wr_cmd_R;  // wr cmd cyc 1
```

```
//-------------------------------------
  always @(posedge clk_in)
          begin
                    rd_R2 <= rd_R1 ;
                    rd_R3 <= rd_R2;


                  rd_R4 <= rd_R3;
                  rd_R5 <= rd_R4;
//                rd0_o_R6 <= rd0_o_R5;
                  wr_R2 <= wr_R1 ;
                  wr_R3 <= wr_R2;
                  wr_R4 <= wr_R3;
                  wr_R5 <= wr_R4;
          end
//-------------------------------------
assign    wr_01_R1 = sel_01 & wr_cmd_R;  // wr cmd cyc 1 for cs 2 & cs3
assign    wr_23_R1 = sel_23 & wr_cmd_R;  // wr cmd cyc 1 for cs 2 & cs3
  always @(posedge clk_in)
          begin
                  wr_01_R2 <= wr_01_R1 ;
                  wr_01_R3 <= wr_01_R2;
                  wr_01_R4 <= wr_01_R3;
                  wr_23_R2 <= wr_23_R1 ;
                  wr_23_R3 <= wr_23_R2;
                  wr_23_R4 <= wr_23_R3;
          end
assign    rodt0_ab = (rodt0)          // odt cmd from sys
                   | (wr_23_R1)       // wr 1st cyc to other rnks (assume single dimm per channel)
                   | (wr_23_R2)       // wr 2nd cyc to other rnks (assume single dimm per channel)
                   | (wr_23_R3)       // wr 3rd cyc to other rnks (assume single dimm per channel)
                   ;
assign    rodt1_ab = (rodt1)          // odt cmd from sys
                   | (wr_01_R1)       // wr 1st cyc to other rnks (assume single dimm per channel)
                   | (wr_01_R2)       // wr 2nd cyc to other rnks (assume single dimm per channel)
                   | (wr_01_R3)       // wr 3rd cyc to other rnks (assume single dimm per channel)
                   ;
```


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```
//-------------------------------------
 always @(posedge clk_in)
        begin
  if (
     |(rd_R2)                          // pre-am rd
     |(rd_R3)                          // 1st cyc of rd brst (cl3)
     |(rd_R4)                          // 2nd cyc of rd brst (cl3)
     |(wr_R1)                          // pre-am wr
     |(wr_R2)                          // wr brst 1st cyc
     |(wr_R3)                          // wr brst 2nd cyc
      ) begin
                enfet1 <= 1'b1;        // enable fet
                enfet2 <= 1'b1;        // enable fet
                enfet3 <= 1'b1;        // enable fet
                enfet4 <= 1'b1;        // enable fet
                enfet5 <= 1'b1;        // enable fet
                enfet6 <= 1'b1;        // enable fet
       end

  else
       begin
                enfet1 <= 1'b0;        // disable fet
                enfet2 <= 1'b0;        // disable fet
                enfet3 <= 1'b0;        // disable fet
                enfet4 <= 1'b0;        // disable fet
                enfet5 <= 1'b0;        // disable fet

                enfet6 <= 1'b0;        // disable fet
     end
end
```

Back-to-Back Adjacent Read Commands

[0063] Due to their source synchronous nature, DDR SDRAM (e.g., DDR1, DDR2, DDR3) memory devices operate with a data transfer protocol which surrounds each burst of data strobes with a pre-amble time interval and a post-amble time interval. The pre-amble time interval provides a timing window for the receiving memory device to enable its data capture circuitry when a known valid level is present on the strobe signal to avoid false triggers of the memory device's capture circuit. The post-amble time interval provides extra time after the last strobe for this data capture to facilitate good signal integrity. In certain embodiments, when the computer system accesses two consecutive bursts of data from the same memory device, termed herein as a "back-to-back adjacent read," the post-amble time interval of the first read command and the pre-amble time interval of the second read command are skipped by design protocol to increase read efficiency. FIG. 6A shows an exemplary timing diagram of this

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"gapless" read burst for a back-to-back adjacent read condition from one memory device.

[0064] In certain embodiments, when the second read command accesses data from a different memory device than does the first read command, there is at least one time interval (e.g., clock cycle) inserted between the data strobes of the two memory devices. This inserted time interval allows both read data bursts to occur without the post-amble time interval of the first read data burst colliding or otherwise interfering with the pre-amble time interval of the second read data burst. In certain embodiments, the memory controller of the computer system inserts an extra clock cycle between successive read commands issued to different memory devices, as shown in the exemplary timing diagram of FIG. 6B for successive read accesses from different memory devices.

[0065] In typical computer systems, the memory controller is informed of the memory boundaries between the ranks of memory of the memory module prior to issuing read commands to the memory module. Such memory controllers can insert wait time intervals or clock cycles to avoid collisions or interference between back-to-back adjacent read commands which cross memory device boundaries, which are referred to herein as "BBARX."

[0066] In certain embodiments described herein in which the number of ranks **32** of the memory module **10** is doubled or quadrupled, the circuit **40** generates a set of output address and command signals so that the selection decoding is transparent to the computer system. However, in certain such embodiments, there are memory device boundaries of which the computer system is unaware, so there are occasions in which BBARX occurs without the cognizance of the memory controller **20** of the computer system. As shown in FIG. 7, the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b," resulting in a "collision window."

[0067] FIGS. 8A-8D schematically illustrate circuit diagrams of example memory modules **10** comprising a circuit **40** which multiplexes the DQS data strobe signal lines **104a**, **104b** of two ranks **32a**, **32b** from one another in accordance with certain embodiments described herein. While the DQS data strobe signal lines **104a**, **104b** of FIGS. 8A-8D correspond to two ranks **32a**, **32b** of memory devices **30**, in certain other embodiments, the circuit **40** multiplexes the DQS data strobe signal lines **104a**, **104b** corresponding to two individual memory devices **30a, 30b**.

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[0068] FIG. 8A schematically illustrates a circuit diagram of an exemplary memory module **10** comprising a circuit **40** in accordance with certain embodiments described herein. In certain embodiments, BBARX collisions are avoided by a mechanism which electrically isolates the DQS data strobe signal lines **104a**, **104b** from one another during the transition from the first read data burst of one rank **32a** of memory devices **30** to the second read data burst of another rank **32b** of memory devices **30**.

[0069] In certain embodiments, as schematically illustrated by FIG. 8A, the circuit **40** comprises a first switch **130a** electrically coupled to a first DQS data strobe signal line **104a** of a first rank **32a** of memory devices **30** and a second switch **130b** electrically coupled to a second DQS data strobe signal line **104b** of a second rank **32b** of memory devices **30**. In certain embodiments, the time for switching the first switch **130a** and the second switch **130b** is between the two read data bursts (e.g., after the last DQS data strobe of the read data burst of the first rank **32a** and before the first DQS data strobe of the read data burst of the second rank **32b**). During the read data burst for the first rank **32a**, the first switch **130a** is enabled. After the last DQS data strobe of the first rank **32a** and before the first DQS data strobe of the second rank **32b**, the first switch **130a** is disabled and the second switch **130b** is enabled.

[0070] As shown in FIG. 8A, each of the ranks **32a**, **32b** otherwise involved in a BBARX collision have their DQS data strobe signal lines **104a**, **104b** selectively electrically coupled to the common DQS line **114** through the circuit **40**. The circuit **40** of certain embodiments multiplexes the DQS data strobe signal lines **104a**, **104b** of the two ranks **32a**, **32b** of memory devices **30** from one another to avoid a BBARX collision.

[0071] In certain embodiments, as schematically illustrated by FIG. 8B, the circuit **40** comprises a switch **130** which multiplexes the DQS data strobe signal lines **104a**, **104b** from one another. For example, the circuit **40** receives a DQS data strobe signal from the common DQS data strobe signal line **114** and selectively transmits the DQS data strobe signal to the first DQS data strobe signal line **104a**, to the second DQS data strobe signal line **104b**, or to both DQS data strobe signal lines **104a**, **104b**. As another example, the circuit **40** receives a first DQS data strobe signal from the first rank **32a** of memory devices **30** and a second DQS data strobe signal from a second rank **32b** of memory devices **30** and selectively switches one of the first and second DQS data strobe signals to the common DQS data strobe signal line **114**.

[0072] In certain embodiments, the circuit **40** also provides the load isolation

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described above in reference to FIGS. 1-5. For example, as schematically illustrated by FIG. 8C, the circuit **40** comprises both the switch **120** for the DQ data signal lines **102a**, **102b** and the switch **130** for the DQS data strobe signal lines **104a**, **104b**. While in certain embodiments, the switches **130** are integral with a logic element of the circuit **40**, in certain other embodiments, the switches **130** are separate components which are operatively coupled to a logic element **122** of the circuit **40**, as schematically illustrated by FIG. 8D. In certain such embodiments, the control and timing of the switch **130** is performed by the circuit **40** which is resident on the memory module **10**. Example switches **130** compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex., and multiplexers, such as the SN74AUC2G53 2:1 analog multiplexer/demultiplexer available from Texas Instruments, Inc. of Dallas, Tex.

[0073] The circuit **40** of certain embodiments controls the isolation of the DQS data strobe signal lines **104a**, **104b** by monitoring commands received by the memory module **10** from the computer system and producing "windows" of operation whereby the appropriate switches **130** are activated or deactivated to enable and disable the DQS data strobe signal lines **104a**, **104b** to mitigate BBARX collisions. In certain other embodiments, the circuit **40** monitors the commands received by the memory module **10** from the computer system and selectively activates or deactivates the switches **120** to enable and disable the DQ data signal lines **102a**, **102b** to reduce the load of the memory module **10** on the computer system. In still other embodiments, the circuit **40** performs both of these functions together.

Command Signal Translation

[0074] Most high-density memory modules are currently built with 512-Megabit ("512-Mb") memory devices wherein each memory device has a 64 M×8-bit configuration. For example, a 1-Gigabyte ("1-GB") memory module with error checking capabilities can be fabricated using eighteen such 512-Mb memory devices. Alternatively, it can be economically advantageous to fabricate a 1-GB memory module using lower-density memory devices and doubling the number of memory devices used to produce the desired word width. For example, by fabricating a 1-GB memory module using thirty-six 256-Mb memory devices with 64 M×4-bit configuration, the cost of the resulting 1-GB memory module can be reduced since the unit cost of each 256-Mb memory device is typically lower than one-half the unit cost of each 512-

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Mb memory device. The cost savings can be significant, even though twice as many 256-Mb memory devices are used in place of the 512-Mb memory devices. For example, by using pairs of 512-Mb memory devices rather than single 1-Gb memory devices, certain embodiments described herein reduce the cost of the memory module by a factor of up to approximately five.

[0075] Market pricing factors for DRAM devices are such that higher-density DRAM devices (e.g., 1-Gb DRAM devices) are much more than twice the price of lower-density DRAM devices (e.g., 512-Mb DRAM devices). In other words, the price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices. This pricing difference often lasts for months or even years after the introduction of the higher-density DRAM devices, until volume production factors reduce the costs of the newer higher-density DRAM devices. Thus, when the cost of a higher-density DRAM device is more than the cost of two lower-density DRAM devices, there is an economic incentive for utilizing pairs of the lower-density DRAM devices to replace individual higher-density DRAM devices.

[0076] FIG. 9A schematically illustrates an exemplary memory module **10** compatible with certain embodiments described herein. The memory module **10** is connectable to a memory controller **20** of a computer system (not shown). The memory module **10** comprises a printed circuit board **210** and a plurality of memory devices **30** coupled to the printed circuit board **210**. The plurality of memory devices **30** has a first number of memory devices **30**. The memory module **10** further comprises a circuit **40** coupled to the printed circuit board **210**. The circuit **40** receives a set of input address and command signals from the computer system. The set of input address and command signals correspond to a second number of memory devices **30** smaller than the first number of memory devices **30**. The circuit **40** generates a set of output address and command signals in response to the set of input address and command signals. The set of output address and command signals corresponds to the first number of memory devices **30**.

[0077] In certain embodiments, as schematically illustrated in FIG. 9A, the memory module **10** further comprises a phase-lock loop device **220** coupled to the printed circuit board **210** and a register **230** coupled to the printed circuit board **210**. In certain embodiments, the phase-lock loop device **220** and the register **230** are each mounted on the printed circuit board **210**. In response to signals received from the computer system, the phase-lock loop device **220** transmits clock signals to the plurality of memory devices **30**, the circuit

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40, and the register **230**. The register **230** receives and buffers a plurality of command signals and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals), and transmits corresponding signals to the appropriate memory devices **30**. In certain embodiments, the register **230** comprises a plurality of register devices. While the phase-lock loop device **220**, the register **230**, and the circuit **40** are described herein in certain embodiments as being separate components, in certain other embodiments, two or more of the phase-lock loop device **220**, the register **230**, and the circuit **40** are portions of a single component. Persons skilled in the art are able to select a phase-lock loop device **220** and a register **230** compatible with embodiments described herein.

[0078] In certain embodiments, the memory module **10** further comprises electrical components which are electrically coupled to one another and are surface-mounted or embedded on the printed circuit board **210**. These electrical components can include, but are not limited to, electrical conduits, resistors, capacitors, inductors, and transistors. In certain embodiments, at least some of these electrical components are discrete, while in other certain embodiments, at least some of these electrical components are constituents of one or more integrated circuits.

[0079] In certain embodiments, the printed circuit board **210** is mountable in a module slot of the computer system. The printed circuit board **210** of certain such embodiments has a plurality of edge connections electrically coupled to corresponding contacts of the module slot and to the various components of the memory module **10**, thereby providing electrical connections between the computer system and the components of the memory module **10**.

[0080] In certain embodiments, the plurality of memory devices **30** are arranged in a first number of ranks **32**. For example, in certain embodiments, the memory devices **30** are arranged in four ranks **32a**, **32b**, **32** *c*, **32** *d*, as schematically illustrated by FIG. 9A. In certain other embodiments, the memory devices **30** are arranged in two ranks **32a**, **32b**, as schematically illustrated by FIG. 9B. Other numbers of ranks **32** of the memory devices **30** are also compatible with embodiments described herein.

[0081] As schematically illustrated by FIGS. 9A and 9B, in certain embodiments, the circuit **40** receives a set of input command signals (e.g., refresh, precharge) and address signals (e.g., bank address signals, row address signals, column address signals, gated column

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address strobe signals, chip-select signals) from the memory controller **20** of the computer system. In response to the set of input address and command signals, the circuit **40** generates a set of output address and command signals.

[0082] In certain embodiments, the set of output address and command signals corresponds to a first number of ranks in which the plurality of memory devices **30** of the memory module **10** are arranged, and the set of input address and command signals corresponds to a second number of ranks per memory module for which the computer system is configured. The second number of ranks in certain embodiments is smaller than the first number of ranks. For example, in the exemplary embodiment as schematically illustrated by FIG. 9A, the first number of ranks is four while the second number of ranks is two. In the exemplary embodiment of FIG. 9B, the first number of ranks is two while the second number of ranks is one. Thus, in certain embodiments, even though the memory module **10** actually has the first number of ranks of memory devices **30**, the memory module **10** simulates a virtual memory module by operating as having the second number of ranks of memory devices **30**. In certain embodiments, the memory module **10** simulates a virtual memory module when the number of memory devices **30** of the memory module **10** is larger than the number of memory devices **30** per memory module for which the computer system is configured to utilize. In certain embodiments, the circuit **40** comprises logic (e.g., address decoding logic, command decoding logic) which translates between a system memory domain of the computer system and a physical memory domain of the memory module **10**.

[0083] In certain embodiments, the computer system is configured for a number of ranks per memory module which is smaller than the number of ranks in which the memory devices **30** of the memory module **10** are arranged. In certain such embodiments, the computer system is configured for two ranks of memory per memory module (providing two chip-select signals CS_0, CS_1) and the plurality of memory modules **30** of the memory module **10** are arranged in four ranks, as schematically illustrated by FIG. 9A. In certain other such embodiments, the computer system is configured for one rank of memory per memory module (providing one chip-select signal CS_0) and the plurality of memory modules **30** of the memory module **10** are arranged in two ranks, as schematically illustrated by FIG. 9B.

[0084] In the exemplary embodiment schematically illustrated by FIG. 9A, the memory module **10** has four ranks of memory devices **30** and the computer system is

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configured for two ranks of memory devices per memory module. The memory module **10** receives row/column address signals or signal bits (A_0-A_{n+1}), bank address signals (BA_0-BA_m), chip-select signals (CS_0 and CS_1), and command signals (e.g., refresh, precharge, etc.) from the computer system. The A_0-A_n row/column address signals are received by the register **230**, which buffers these address signals and sends these address signals to the appropriate ranks of memory devices **30**. The circuit **40** receives the two chip-select signals (CS_0, CS_1) and one row/column address signal (A_{n+1}) from the computer system. Both the circuit **40** and the register **230** receive the bank address signals (BA_0-BA_m) and at least one command signal (e.g., refresh, precharge, etc.) from the computer system.

Logic Tables

[0085] Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using chip-select signals.

TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:
1. CS_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

[0086] In Logic State 1: CS_0 is active low, A_{n+1} is non-active, and Command is active. CS_{0A} is pulled low, thereby selecting Rank **0**.

[0087] In Logic State 2: CS_0 is active low, A_{n+1} is active, and Command is active. CS_{0B} is pulled low, thereby selecting Rank **1**.

[0088] In Logic State 3: CS_0 is active low, A_{n+1} is Don't Care, and Command is active high. CS_{0A} and CS_{0B} are pulled low, thereby selecting Ranks **0** and **1**.

[0089] In Logic State 4: CS_1 is active low, A_{n+1} is non-active, and Command is

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active. CS_{1A} is pulled low, thereby selecting Rank **2**.

[0090] In Logic State 5: CS_1 is active low, A_{n+1} is active, and Command is active. CS_1B is pulled low, thereby selecting Rank **3**.

[0091] In Logic State 6: CS_1 is active low, A_{n+1} is Don't Care, and Command is active. CS_{1A} and CS_1B are pulled low, thereby selecting Ranks **2** and **3**.

[0092] In Logic State 7: CS_0 and CS_1 are pulled non-active high, which deselects all ranks, i.e., CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are pulled high.

[0093] The "Command" column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently.

[0094] Table 2 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using gated CAS signals.

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TABLE 2

CS*	RAS*	CAS*	WE*	Density Bit	A_{10}	Command	CAS0*	CAS1*
1	x	x	x	x	x	NOP	x	x
0	1	1	1	x	x	NOP	1	1
0	0	1	1	0	x	ACTIVATE	1	1
0	0	1	1	1	x	ACTIVATE	1	1
0	1	0	1	0	x	READ	0	1
0	1	0	1	1	x	READ	1	0
0	1	0	0	0	x	WRITE	0	1
0	1	0	0	1	x	WRITE	1	0
0	0	1	0	0	0	PRE-CHARGE	1	1
0	0	1	0	1	0	PRE-CHARGE	1	1
0	0	1	0	x	1	PRE-CHARGE	1	1
0	0	0	0	x	x	MODE REG SET	0	0
0	0	0	1	x	x	REFRESH	0	0

[0095] In certain embodiments in which the density bit is a row address bit, for read/write commands, the density bit is the value latched during the activate command for the selected bank.

Serial-Presence-Detect Device

[0096] Memory modules typically include a serial-presence detect (SPD) device **240** (e.g., an electrically-erasable-programmable read-only memory or EEPROM device) comprising data which characterize various attributes of the memory module, including but not limited to, the number of row addresses the number of column addresses, the data width of the memory devices, the number of ranks, the memory density per rank, the number of memory devices, and the memory density per memory device. The SPD device **240** communicates this data to the basic input/output system (BIOS) of the computer system so that the computer system is informed of the memory capacity and the memory configuration available for use and can configure the memory controller properly for maximum reliability and performance.

[0097] For example, for a commercially-available 512-MB (64 M×8-byte) memory module utilizing eight 512-Mb memory devices each with a 64 M×8-bit configuration, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte **3**: Defines the number of row address bits in the DRAM device in the memory module [13 for the 512-Mb memory device].

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Byte **4**: Defines the number of column address bits in the DRAM device in the memory module [11 for the 512-Mb memory device].

Byte **13**: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 512-Mb (64 M×8-bit) memory device].

Byte **14**: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 512-Mb (64 M×8-bit) memory device].

Byte **17**: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 512-Mb memory device].

[0098] In a further example, for a commercially-available 1-GB (128 M×8-byte) memory module utilizing eight 1-Gb memory devices each with a 128 M×8-bit configuration, as described above, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte **3**: Defines the number of row address bits in the DRAM device in the memory module [14 for the 1-Gb memory device].

Byte **4**: Defines the number of column address bits in the DRAM device in the memory module [11 for the 1-Gb memory device].

Byte **13**: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 1-Gb (128 M×8-bit) memory device].

Byte **14**: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 1-Gb (128 M×8-bit) memory device].

Byte **17**: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 1-Gb memory device].

[0099] In certain embodiments, the SPD device **240** comprises data which characterize the memory module **10** as having fewer ranks of memory devices than the memory module **10** actually has, with each of these ranks having more memory density. For example, for a memory module **10** compatible with certain embodiments described herein having two ranks of memory devices **30**, the SPD device **240** comprises data which characterizes the memory module **10** as having one rank of memory devices with twice the memory density per rank. Similarly, for a memory module **10** compatible with certain embodiments described herein having four ranks of memory devices **30**, the SPD device **240** comprises data which characterizes the memory module **10** as having two ranks of memory devices with twice the

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memory density per rank. In addition, in certain embodiments, the SPD device **240** comprises data which characterize the memory module **10** as having fewer memory devices than the memory module **10** actually has, with each of these memory devices having more memory density per memory device. For example, for a memory module **10** compatible with certain embodiments described herein, the SPD device **240** comprises data which characterizes the memory module **10** as having one-half the number of memory devices that the memory module **10** actually has, with each of these memory devices having twice the memory density per memory device. Thus, in certain embodiments, the SPD device **240** informs the computer system of the larger memory array by reporting a memory device density that is a multiple of the memory devices **30** resident on the memory module **10**. Certain embodiments described herein advantageously do not require system level changes to hardware (e.g., the motherboard of the computer system) or to software (e.g., the BIOS of the computer system).

[00100] FIG. 9C schematically illustrates an exemplary memory module **10** in accordance with certain embodiments described herein. The memory module **10** comprises a pair of substantially identical memory devices **31**, **33**. Each memory device **31**, **33** has a first bit width, a first number of banks of memory locations, a first number of rows of memory locations, and a first number of columns of memory locations. The memory module **10** further comprises an SPD device **240** comprising data that characterizes the pair of memory devices **31**, **33**. The data characterize the pair of memory devices **31**, **33** as a virtual memory device having a second bit width equal to twice the first bit width, a second number of banks of memory locations equal to the first number of banks, a second number of rows of memory locations equal to the first number of rows, and a second number of columns of memory locations equal to the first number of columns.

[00101] In certain such embodiments, the SPD device **240** of the memory module **10** is programmed to describe the combined pair of lower-density memory devices **31**, **33** as one virtual or pseudo-higher-density memory device. In an exemplary embodiment, two 512-Mb memory devices, each with a 128 M×4-bit configuration, are used to simulate one 1-Gb memory device having a 128 M×8-bit configuration. The SPD device **240** of the memory module **10** is programmed to describe the pair of 512-Mb memory devices as one virtual or pseudo-1-Gb memory device.

[00102] For example, to fabricate a 1-GB (128 M×8-byte) memory module, sixteen

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512-Mb (128 M×4-bit) memory devices can be used. The sixteen 512-Mb (128 M×4-bit) memory devices are combined in eight pairs, with each pair serving as a virtual or pseudo-1-Gb (128 M×8-bit) memory device. In certain such embodiments, the SPD device **240** contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: 13 row address bits.

Byte 4: 12 column address bits.

Byte 13: 8 bits wide for the primary virtual 1-Gb (128 M×8-bit) memory device.

Byte 14: 8 bits wide for the error checking virtual 1-Gb (128 M×8-bit) memory device.

Byte 17: 4 banks.

[00103] In this exemplary embodiment, bytes **3**, **4**, and **17** are programmed to have the same values as they would have for a 512-MB (128 M×4-byte) memory module utilizing 512-Mb (128 M×4-bit) memory devices. However, bytes **13** and **14** of the SPD data are programmed to be equal to 8, corresponding to the bit width of the virtual or pseudo-higher-density 1-Gb (128 M×8-bit) memory device, for a total capacity of 1-GB. Thus, the SPD data does not describe the actual-lower-density memory devices, but instead describes the virtual or pseudo-higher-density memory devices. The BIOS accesses the SPD data and recognizes the memory module as having 4 banks of memory locations arranged in 2^{13} rows and 2^{12} columns, with each memory location having a width of 8 bits rather than 4 bits.

[00104] In certain embodiments, when such a memory module **10** is inserted in a computer system, the computer system's memory controller then provides to the memory module **10** a set of input address and command signals which correspond to the number of ranks or the number of memory devices reported by the SPD device **240**. For example, placing a two-rank memory module **10** compatible with certain embodiments described herein in a computer system compatible with one-rank memory modules, the SPD device **240** reports to the computer system that the memory module **10** only has one rank. The circuit **40** then receives a set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices **30** of the memory module **10**.

[00105] Similarly, when a two-rank memory module **10** compatible with certain embodiments described herein is placed in a computer system compatible with either one- or

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two-rank memory modules, the SPD device **240** reports to the computer system that the memory module **10** only has one rank. The circuit **40** then receives a set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices **30** of the memory module **10**.

[00106] Furthermore, a four-rank memory module **10** compatible with certain embodiments described herein simulates a two-rank memory module whether the memory module **10** is inserted in a computer system compatible with two-rank memory modules or with two- or four-rank memory modules. Thus, by placing a four-rank memory module **10** compatible with certain embodiments described herein in a module slot that is four-rank-ready, the computer system provides four chip-select signals, but the memory module **10** only uses two of the chip-select signals.

[00107] In certain embodiments, the circuit **40** comprises the SPD device **240** which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device **240** of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array. In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit **40**. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices **30** from the memory controller **20**. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three. In still other embodiments, the SPD device **240** does not utilize this extra cycle of time.

Memory Density Multiplication

[00108] In certain embodiments, two memory devices having a memory density are

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used to simulate a single memory device having twice the memory density, and an additional address signal bit is used to access the additional memory. Similarly, in certain embodiments, two ranks of memory devices having a memory density are used to simulate a single rank of memory devices having twice the memory density, and an additional address signal bit is used to access the additional memory. As used herein, such simulations of memory devices or ranks of memory devices are termed as "memory density multiplication," and the term "density transition bit" is used to refer to the additional address signal bit which is used to access the additional memory by selecting which rank of memory devices is enabled for a read or write transfer operation.

[00109] For example, for computer systems which are normally limited to using memory modules which have a single rank of 128 M×4-bit memory devices, certain embodiments described herein enable the computer system to utilize memory modules which have double the memory (e.g., two ranks of 128 M×4-bit memory devices). The circuit **40** of certain such embodiments provides the logic (e.g., command and address decoding logic) to double the number of chip selects, and the SPD device **240** reports a memory device density of 256 M×4-bit to the computer system.

[00110] In certain embodiments utilizing memory density multiplication embodiments, the memory module **10** can have various types of memory devices **30** (e.g., DDR1, DDR2, DDR3, and beyond). The circuit **40** of certain such embodiments utilizes implied translation logic equations having variations depending on whether the density transition bit is a row, column, or internal bank address bit. In addition, the translation logic equations of certain embodiments vary depending on the type of memory module **10** (e.g., UDIMM, RDIMM, FBDIMM, etc.). Furthermore, in certain embodiments, the translation logic equations vary depending on whether the implementation multiplies memory devices per rank or multiplies the number of ranks per memory module.

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TABLE 3A

	128-Mb	256-Mb	512-Mb	1-Gb
Number of banks	4	4	4	4
Number of row address bits	12	13	13	14
Number of column address bits for "x 4" configuration	11	11	12	12
Number of column address bits for "x 8" configuration	10	10	11	11
Number of column address bits for "x 16" configuration	9	9	10	10

[00111] Table 3A provides the numbers of rows and columns for DDR-1 memory devices, as specified by JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published February 2004, and incorporated in its entirety by reference herein.

[00112] As described by Table 3A, 512-Mb (128 M×4-bit) DRAM devices have 2^{13} rows and 2^{12} columns of memory locations, while 1-Gb (128 M×8-bit) DRAM devices have 2^{14} rows and 2^{11} columns of memory locations. Because of the differences in the number of rows and the number of columns for the two types of memory devices, complex address translation procedures and structures would typically be needed to fabricate a 1-GB (128 M×8-byte) memory module using sixteen 512-Mb (128 M×4-bit) DRAM devices.

[00113] Table 3B shows the device configurations as a function of memory density for DDR2 memory devices.

TABLE 3B

	Number of Rows	Number of Columns	Number of Internal Banks	Page Size (x4s or x8s)
256 Mb	13	11	4	1 KB
512 Mb	14	11	4	1 KB
1 Gb	14	11	8	1 KB
2 Gb	15	11	8	1 KB
4 Gb	16	11	8	1 KB

Table 4 lists the corresponding density transition bit for the density transitions between the DDR2 memory densities of Table 3B.

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TABLE 4

Density Transition	Density Transition Bit
256 Mb to 512 Mb	A_{13}
512 Mb to 1 Gb	BA_2
1 Gb to 2 Gb	A_{14}
2 Gb to 4 Gb	A_{15}

Other certain embodiments described herein utilize a transition bit to provide a transition from pairs of physical 4-Gb memory devices to simulated 8-Gb memory devices.

[00114] In an example embodiment, the memory module comprises one or more pairs of 256-Mb memory devices, with each pair simulating a single 512-Mb memory device. The simulated 512-Mb memory device has four internal banks while each of the two 256-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 256-Mb memory devices. In certain embodiments, the additional row address bit is translated by the circuit **40** to the rank selection between each of the two 256-Mb memory devices of the pair. Although there are eight total internal banks in the rank-converted memory array, the computer system is only aware of four internal banks. When the memory controller activates a row for a selected bank, the circuit **40** activates the same row for the same bank, but it does so for the selected rank according to the logic state of the additional row address bit A_{13}.

[00115] In another example embodiment, the memory module comprises one or more pairs of 512-Mb memory devices, with each pair simulating a single 1-Gb memory device. The simulated 1-Gb memory device has eight internal banks while each of the two 512-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 512-Mb memory devices. In certain embodiments, the mapped BA_2 (bank **2**) bit is used to select between the two ranks of 512-Mb memory devices to preserve the internal bank geometry expected by the memory controller of the computer system. The state of the BA_2 bit selects the upper or lower set of four banks, as well as the upper and lower 512-Mb rank.

[00116] In another example embodiment, the memory module comprises one or more pairs of 1-Gb memory devices, with each pair simulating a single 2-Gb memory device. Each of the two 1-Gb memory devices has eight internal banks for a total of sixteen internal banks, while the simulated 2-Gb memory device has eight internal banks. In certain embodiments, the additional row address bit translates to the rank selection between the two

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1-Gb memory devices. Although there are sixteen total internal banks per pair of 1-Gb memory devices in the rank-converted memory array, the memory controller of the computer system is only aware of eight internal banks. When the memory controller activates a row of a selected bank, the circuit **40** activates the same row for the same bank, but is does so for the selected rank according to the logic state of the additional row address bit A_{14}.

[00117] The circuit **40** of certain embodiments provides substantially all of the translation logic used for the decoding (e.g., command and address decoding). In certain such embodiments, there is a fully transparent operational conversion from the "system memory" density domain of the computer system to the "physical memory" density domain of the memory module **10**. In certain embodiments, the logic translation equations are programmed in the circuit **40** by hardware, while in certain other embodiments, the logic translation equations are programmed in the circuit **40** by software. Examples 1 and 2 provide exemplary sections of Verilog code compatible with certain embodiments described herein. As described more fully below, the code of Examples 1 and 2 includes logic to reduce potential problems due to "back-to-back adjacent read commands which cross memory device boundaries or "BBARX." Persons skilled in the art are able to provide additional logic translation equations compatible with embodiments described herein.

[00118] An exemplary section of Verilog code compatible with memory density multiplication from 512 Mb to 1 Gb using DDR2 memory devices with the BA_2 density transition bit is listed below in Example 2. The exemplary code of Example 2 corresponds to a circuit **40** which receives one chip-select signal from the computer system and which generates two chip-select signals.

[00119] Example 2

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```
always @(posedge clk__in)
    begin
                cs0N__R <= cs0__in__N;    // cs0
                rasN__R <= ras__in__N;
                casN__R <= cas__in__N;
                weN__R <= we__in__N;
    end
// Gated Chip Selects
assign          pcs0a__1 = (~cs0__in__N & ~ras__in__N & ~cas__in__N)                          // ref,rmd reg set
                | (~cs0__in__N & ras__in__N & cas__in__N)                                     // ref exit, pwr da
                | (~cs0__in__N & ~ras__in__N & cas__in__N & ~we__in__N & a10__in)             // pchg all
                | (~cs0__in__N & ~ras__in__N & cas__in__N & ~we__in__N & ~a10__in & ~ba2__in) // pchg single bnk
                | (~cs0__in__N & ~ras__in__N & cas__in__N & we__in__N       & ~ba2__in)      // activate
                | (~cs0__in__N & ras__in__N & ~cas__in__N             & ~ba2__in)             // xfr
                ;
assign          pcs0b__1 = (~cs0__in__N & ~ras__in__N & ~cas__in__N)                          // ref,rmi reg set
                | (~cs0__in__N & ras__in__N & cas__in__N)                                     // ref exit, pwr da
                | (~cs0__in__N & ~ras__in__N & cas__in__N & ~we__in__N & a10__in)             // pchg all
                | (~cs0__in__N & ~ras__in__N & cas__in__N & ~we__in__N & ~a10__in & ba2__in) // pchg single bnk
                | (~cs0__in__N & ~ras__in__N & cas__in__N & we__in__N       & ba2__in)       // activate
                | (~cs0__in__N & ras__in__N & ~cas__in__N             & ba2__in) // xfr
                ;
//-------------------------------
 always @(posedge clk__in)
    begin
                a4__r <= a4__in ;
                a5__r <= a5__in ;
                a6__r <= a6__in ;
                a10__r <= a10__in ;
                ba0__r <= ba0__in ;
                ba1__r <= ba1__in ;
                ba2__r <= ba2__in ;
                q__mrs__cmd__cyc1  <= q__mrs__cmd ;
    end
////////////////////////////////////////////////////////////
// determine the cas latency
////////////////////////////////////////////////////////////
assign q__mrs__cmd__r = (!rasN__R & !casN__R & !weN__R)
                        & !cs0N__R
                & (!ba0__r & !ba1__r)
                ;       // rmd reg set cmd
    always @(posedge clk__in)
        if (~reset__N)      // hmr
                cl3 <= 1'b1 ;
        else if (q__mrs__cmd__cyc1)   // load mode reg cmd
      begin
                cl3 <= (~a6__r & a5__r & a4__r) ;
      end
    always @(posedge clk__in)
        if (~reset__N)              // reset
```

```
                cl2 <= 1'b0 ;
            else if (q_mrs_cmd_cyc1)   // load mode reg cmd
        begin
                cl2 <= (~a6_r & a5_r & ~a4_r ) ;
        end
      always @(posedge clk_in)
            if (~reset_N)              // reset
                cl4 <= 1'b0 ;
            else if (q_mrs_cmd_cyc1)   // load mode reg cmd
        begin
                cl4 <= (a6_r & ~a5_r & ~a4_r ) ;
        end
  always @(posedge clk_in)
            if (~reset_N)              cl5 <= 1'b0 ;
            else if (q_mrs_cmd_cyc1)   // load mode reg cmd
        begin
                cl5 <= (a6_r & ~a5_r & a4_r ) ;
        end
assign          pre_cyc2_enfet = (wr_cmd_cyc1 & acs_cyc1 & cl3)     // wr brst cl3 preamble
                               ;
assign          pre_cyc3_enfet = (rd_cmd_cyc2 & cl3)                // rd brst cl3 preamble
                               | (wr_cmd_cyc2 & cl3)                // wr brst cl3 1st pair
                               | (wr_cmd_cyc2 & cl4)                // wr brst cl4 preamble
                               ;
assign          pre_cyc4_enfet = (wr_cmd_cyc3 & cl3)                // wr brst cl3 2nd pair
                               | (wr_cmd_cyc3 & cl4)                // wr brst cl4 1st pair
                               | (rd_cmd_cyc3 & cl3)                // rd brst cl3 1st pair
                               | (rd_cmd_cyc3 & cl4)                // rd brst cl4 preamble
                               ;
assign          pre_cyc5_enfet = (rd_cmd_cyc4 & cl3)                // rd brst cl3 2nd pair
                               | (wr_cmd_cyc4 & cl4)                // wr brst cl4 2nd pair
                               | (rd_cmd_cyc4 & cl4)                // rd brst cl4 1st pair
                               ;
// dq
assign          pre_dq_cyc = pre_cyc2_enfet
                   | pre_cyc3_enfet
                   | pre_cyc4_enfet
                   | pre_cyc5_enfet
                   ;
assign          pre_dq_ncyc = enfet_cyc2
                   | enfet_cyc3
                   | enfet_cyc4
                   | enfet_cyc5
                   ;
// dqs
assign          pre_dqsa_cyc = (pre_cyc2_enfet & ~ba2_r)
                   | (pre_cyc3_enfet & ~ba2_cyc2)
                   | (pre_cyc4_enfet & ~ba2_cyc3)
                   | (pre_cyc5_enfet & ~ba2_cyc4)
                   ;
assign          pre_dqsb_cyc = (pre_cyc2_enfet & ba2_r)
                   | (pre_cyc3_enfet & ba2_cyc2)
                   | (pre_cyc4_enfet & ba2_cyc3)
                   | (pre_cyc5_enfet & ba2_cyc4)
                   ;
assign          pre_dqsa_ncyc = (enfet_cyc2 & ~ba2_cyc2)
                   | (enfet_cyc3 & ~ba2_cyc3)
                   | (enfet_cyc4 & ~ba2_cyc4)
                   | (enfet_cyc5 & ~ba2_cyc5)
                   ;
assign          pre_dqsb_ncyc = (enfet_cyc2 & ba2_cyc2)
                   | (enfet_cyc3 & ba2_cyc3)
                   | (enfet_cyc4 & ba2_cyc4)
                   | (enfet_cyc5 & ba2_cyc5)
                   ;
```

```
always @(posedge clk_in)
        begin
                        acs_cyc2 <= acs_cyc1 ;        // cs active
                        ba2_cyc2 <= ba2_r ;
                        ba2_cyc3 <= ba2_cyc2 ;
                        ba2_cyc4 <= ba2_cyc3 ;
                        ba2_cyc5 <= ba2_cyc4 ;
                        ri_cmd_cyc2 <= rd_cmd_cyc1 & acs_cyc1;
                        ri_cmd_cyc3 <= rd_cmd_cyc2 ;
                        ri_cmd_cyc4 <= rd_cmd_cyc3 ;
                        rd_cmd_cyc5 <= rd_cmd_cyc4 ;
                        rd_cmd_cyc6 <= ri_cmd_cyc5 ;
                        rd_cmd_cyc7 <= ri_cmd_cyc6 ;
                        wr_cmd_cyc2 <= wr_cmd_cyc1 & acs_cyc1;
                        wr_cmd_cyc3 <= wr_cmd_cyc2 ;
                        wr_cmd_cyc4 <= wr_cmd_cyc3 ;
                        wr_cmd_cyc5 <= wr_cmd_cyc4 ;
        end
 always @(negedge clk_in)
        begin
                        dq_ncyc <= dq_cyc;
                        dqs_ncyc_a <= dqs_cyc_a;
                        dqs_ncyc_b <= dqs_cyc_b;
        end
// DQ FET enables
assign                  enq_fet1 = dq_cyc | dq_ncyc             ;
assign                  enq_fet2 = dq_cyc | dq_ncyc ;
assign                enq_fet3 = dq_cyc | dq_ncyc               ;
assign                  enq_fet4 = dq_cyc | dq_ncyc ;
assign                  enq_fet5 = dq_cyc | dq_ncyc ;
// DQS FET enables
assign                  ens_fet1a = dqs_cyc_a | dqs_ncyc_a    ;
assign                  ens_fet2a = dqs_cyc_a | dqs_ncyc_a    ;
assign                  ens_fet3a = dqs_cyc_a | dqs_ncyc_a    ;
assign                  ens_fet1b = dqs_cyc_b | dqs_ncyc_b    ;
assign                  ens_fet2b = dqs_cyc_b | dqs_ncyc_b    ;
assign                  ens_fet3b = dqs_cyc_b | dqs_ncyc_b    ;
```

[00120] Another exemplary section of Verilog code compatible with memory density multiplication from 256 Mb to 512 Mb using DDR2 memory devices and gated CAS signals with the row A_{13} density transition bit is listed below in Example 3. The exemplary code of Example 3 corresponds to a circuit **40** which receives one gated CAS signal from the computer system and which generates two gated CAS signals.

[00121] Example 3

```
// latched a13 flags cs0, banks 0-3
   always @(posedge clk_in)
      if (actv_cmd_R & ~rs0N_R & ~bnk1_R & ~bnk0_R )   // activate
      begin
                        1_a13_00 <= a13_r ;
      end
   always @(posedge clk_in)
      if (actv_cmd_R & ~rs0N_R & ~bnk1_R & bnk0_R)      // activate
      begin
                        1_a13_01 <= a13_r ;
      end
   always @(posedge clk_in)
      if (actv_cmd_R & ~rs0N_R & bnk1_R & ~bnk0_R)      // activate
```


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```
    begin
            1_a13_10 <= a13_r ;
    end
  always @(posedge clk_in)
    if (actv_cmd_R & ~rs0N_R & bnk1_R & bnk0_R)      // activate
    begin
            1_a13_11 <= a13_r ;
    end
// gated cas
assign cas_i = ~(casN_R);
assign   cas0_o = ( ~rasN_R & cas_i)
                | ( rasN_R & ~1_a13_00 & ~bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & ~1_a13_01 & ~bnk1_R & bnk0_R & cas_i)
                | ( rasN_R & ~1_a13_10 & bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & ~1_a13_11 & bnk1_R & bnk0_R & cas_i)
                ;
assign   cas1_o = ( ~rasN_R & cas_i)
                | ( rasN_R & 1_a13_00          & ~bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & 1_a13_01          & ~bnk1_R & bnk0_R & cas_i)
                | ( rasN_R & 1_a13_10          & bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & 1_a13_11          & bnk1_R & bnk0_R & cas_i)
                ;
assign          pcas_0_N = ~cas0_o;
assign          pcas_1_N = ~cas1_o;
assign          rd0_o_R1 = rasN_R & cas0_o & weN_R & ~rs0N_R;   // rnk0 rd cmd cyc
assign          rd1_o_R1 = rasN_R & cas1_o & weN_R & ~rs0N_R;   // rnk1 rd cmd cyc
assign          wr0_o_R1 = rasN_R & cas0_o & ~weN_R & ~rs0N_R;  // rnk0 wr cmd cyc
assign          wr1_o_R1 = rasN_R & cas1_o & ~weN_R & ~rs0N_R ;  // rnk1 wr cmd cyc
    always @(posedge clk_in)
        begin
            rd0_o_R2 <= rd0_o_R1 ;
            rd0_o_R3 <= rd0_o_R2;
            rd0_o_R4 <= rd0_o_R3;
            rd0_o_R5 <= rd0_o_R4;
            rd1_o_R2 <= rd1_o_R1 ;
            rd1_o_R3 <= rd1_o_R2;
            rd1_o_R4 <= rd1_o_R3;
            rd1_o_R5 <= rd1_o_R4;
            wr0_o_R2 <= wr0_o_R1 ;
            wr0_o_R3 <= wr0_o_R2;
            wr0_o_R4 <= wr0_o_R3;
            wr1_o_R2 <= wr1_o_R1 ;
            wr1_o_R3 <= wr1_o_R2;
            wr1_o_R4 <= wr1_o_R3;
        end
    always @(posedge clk_in)
        begin
        if (
              (rd0_o_R2 & ~rd1_o_R4)                                  // pre-am rd if no ped on rnk 1
            | rd0_o_R3                                                // 1st cyc of rd brst
            | rd0_o_R4                                                // 2nd cyc of rd brst
            | (rd0_o_R5 & ~rd1_o_R2 & ~rd1_o_R3)                      // post-rd cyc if no ped on rnk 1
            | (wr0_o_R1)                                              // pre-am wr
            | wr0_o_R2 | wr0_o_R3                                     // wr brst 1st & 2nd cyc
            | (wr0_o_R4)                                              // post-wr cyc (chgef9)
            | wr1_o_R1 | wr1_o_R2 | wr1_o_R3 | wr1_o_R4               // rank 1 (chgef9)
            )
                                    en_fet_a <= 1'b1;                 // enable fet
        else
                                    en_fet_a <= 1'b0;                 // disable fet
        end
```

```
always @(posedge clk_in)
        begin
        if (
                (rd1_o_R2 & ~rd0_o_R4)
              | rd1_o_R3
              | rd1_o_R4
              | (rd1_o_R5 & ~rd0_o_R2 & ~rd0_o_R3)
            | (wr1_o_R1)                                    // (chgef8)
            | wr1_o_R2 | wr1_o_R3
  | (wr1_o_R4)                                              // post-wr cyc     (chgef9)
  | wr0_o_R1 | wr0_o_R2 | wr0_o_R3 | wr0_o_R4               // rank 0 (chgef9)
                )
                    eq_let_b <= 1'b1;                       //
        else
                    eq_let_b <= 1'b0;
        end
```

[00122] In certain embodiments, the chipset memory controller of the computer system uses the inherent behavioral characteristics of the memory devices (e.g., DDR2 memory devices) to optimize throughput of the memory system. For example, for each internal bank in the memory array, a row (e.g., 1 KB page) is advantageously held activated for an extended period of time. The memory controller, by anticipating a high number of memory accesses or hits to a particular region of memory, can exercise this feature to advantageously eliminate time-consuming pre-charge cycles. In certain such embodiments in which two half-density memory devices are transparently substituted for a single full-density memory device (as reported by the SPD device **240** to the memory controller), the memory devices advantageously support the "open row" feature.

[00123] FIG. 10A schematically illustrates an exemplary memory module **10** which doubles the rank density in accordance with certain embodiments described herein. The memory module **10** has a first memory capacity. The memory module **10** comprises a plurality of substantially identical memory devices **30** configured as a first rank **32a** and a second rank **32b**. In certain embodiments, the memory devices **30** of the first rank **32a** are configured in pairs, and the memory devices **30** of the second rank **32b** are also configured in pairs. In certain embodiments, the memory devices **30** of the first rank **32a** are configured with their respective DQS pins tied together and the memory devices **30** of the second rank **32b** are configured with their respective DQS pins tied together, as described more fully below. The memory module **10** further comprises a circuit **40** which receives a first set of address and command signals from a memory controller (not shown) of the computer system. The first set of address and command signals is compatible with a second memory capacity substantially equal to one-half of the first memory capacity. The circuit **40** translates the first set of address and command

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signals into a second set of address and command signals which is compatible with the first memory capacity of the memory module **10** and which is transmitted to the first rank **32a** and the second rank **32b**.

[00124] The first rank **32a** of FIG. 10A has 18 memory devices **30** and the second rank **32b** of FIG. 10A has 18 memory devices **30**. Other numbers of memory devices **30** in each of the ranks **32a**, **32b** are also compatible with embodiments described herein.

[00125] In the embodiment schematically illustrated by FIG. 10A, the memory module **10** has a width of 8 bytes (or 64 bits) and each of the memory devices **30** of FIG. 10A has a bit width of 4 bits. The 4-bit-wide ("×4") memory devices **30** of FIG. 10A have one-half the width, but twice the depth of 8-bit-wide ("×8") memory devices. Thus, each pair of "×4" memory devices **30** has the same density as a single "×8" memory device, and pairs of "×4" memory devices **30** can be used instead of individual "×8" memory devices to provide the memory density of the memory module **10**. For example, a pair of 512-Mb 128 M×4-bit memory devices has the same memory density as a 1-Gb 128 M×8-bit memory device.

[00126] For two "×4" memory devices **30** to work in tandem to mimic a "×8" memory device, the relative DQS pins of the two memory devices **30** in certain embodiments are advantageously tied together, as described more fully below. In addition, to access the memory density of a high-density memory module **10** comprising pairs of "×4" memory devices **30**, an additional address line is used. While a high-density memory module comprising individual "×8" memory devices with the next-higher density would also utilize an additional address line, the additional address lines are different in the two memory module configurations.

[00127] For example, a 1-Gb 128 M×8-bit DDR-1 DRAM memory device uses row addresses A_{13}-A_0 and column addresses A_{11} and A_9-A_0. A pair of 512-Mb 128 M×4-bit DDR-1 DRAM memory devices uses row addresses A_{12}-A_0 and column addresses A_{12}, A_{11}, and A_9-A_0. In certain embodiments, a memory controller of a computer system utilizing a 1-GB 128 M×8 memory module **10** comprising pairs of the 512-Mb 128 M×4 memory devices **30** supplies the address and command signals including the extra row address (A_{13}) to the memory module **10**. The circuit **40** receives the address and command signals from the memory controller and converts the extra row address (A_{13}) into an extra column address (A_{12}).

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[00128] FIG. 10B schematically illustrates an exemplary circuit **40** compatible with embodiments described herein. The circuit **40** is used for a memory module **10** comprising pairs of "×4" memory devices **30** which mimic individual "×8" memory devices. In certain embodiments, each pair has the respective DQS pins of the memory devices **30** tied together. In certain embodiments, as schematically illustrated by FIG. 10B, the circuit **40** comprises a programmable-logic device (PLD) **42**, a first multiplexer **44** electrically coupled to the first rank **32a** of memory devices **30**, and a second multiplexer **46** electrically coupled to the second rank **32b** of memory devices **30**. In certain embodiments, the PLD **42** and the first and second multiplexers **44**, **46** are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42**, first multiplexer **44**, and second multiplexer **46** in accordance with embodiments described herein.

[00129] In the exemplary circuit **40** of FIG. 10B, during a row access procedure (CAS is high), the first multiplexer **44** passes the A_{12} address through to the first rank **32**, the second multiplexer **46** passes the A_{12} address through to the second rank **34**, and the PLD **42** saves or latches the A_{13} address from the memory controller. In certain embodiments, a copy of the A_{13} address is saved by the PLD **42** for each of the internal banks (e.g., 4 internal banks) per memory device **30**. During a subsequent column access procedure (CAS is low), the first multiplexer **44** passes the previously-saved A_{13} address through to the first rank **32a** as the A_{12} address and the second multiplexer **46** passes the previously-saved A_{13} address through to the second rank **32b** as the A_{12} address. The first rank **32a** and the second rank **32b** thus interpret the previously-saved A_{13} row address as the current A_{12} column address. In this way, in certain embodiments, the circuit **40** translates the extra row address into an extra column address in accordance with certain embodiments described herein.

[00130] Thus, by allowing two lower-density memory devices to be used rather than one higher-density memory device, certain embodiments described herein provide the advantage of using lower-cost, lower-density memory devices to build "next-generation" higher-density memory modules. Certain embodiments advantageously allow the use of lower-cost readily-available 512-Mb DDR-2 SDRAM devices to replace more expensive 1-Gb DDR-2 SDRAM devices. Certain embodiments advantageously reduce the total cost of the resultant memory module.

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[00131] FIG. 11A schematically illustrates an exemplary memory module **10** which doubles number of ranks in accordance with certain embodiments described herein. The memory module **10** has a first plurality of memory locations with a first memory density. The memory module **10** comprises a plurality of substantially identical memory devices **30** configured as a first rank **32a**, a second rank **32b**, a third rank **32** *c*, and a fourth rank **32** *d*. The memory module **10** further comprises a circuit **40** which receives a first set of address and command signals from a memory controller (not shown). The first set of address and command signals is compatible with a second plurality of memory locations having a second memory density. The second memory density is substantially equal to one-half of the first memory density. The circuit **40** translates the first set of address and command signals into a second set of address and command signals which is compatible with the first plurality of memory locations of the memory module **10** and which is transmitted to the first rank **32a**, the second rank **32b**, the third rank **32** *c*, and the fourth rank **32** *d*.

[00132] Each rank **32a**, **32b**, **32** *c*, **32** *d* of FIG. 11A has 9 memory devices **30**. Other numbers of memory devices **30** in each of the ranks **32a**, **32b**, **32** *c*, **32** *d* are also compatible with embodiments described herein.

[00133] In the embodiment schematically illustrated by FIG. 11A, the memory module **10** has a width of 8 bytes (or 64 bits) and each of the memory devices **30** of FIG. 11A has a bit width of 8 bits. Because the memory module **10** has twice the number of 8-bit-wide ("×8") memory devices **30** as does a standard 8-byte-wide memory module, the memory module **10** has twice the density as does a standard 8-byte-wide memory module. For example, a 1-GB 128 M×8-byte memory module with 36 512-Mb 128 M×8-bit memory devices (arranged in four ranks) has twice the memory density as a 512-Mb 128 M×8-byte memory module with 18 512-Mb 128 M×8-bit memory devices (arranged in two ranks).

[00134] To access the additional memory density of the high-density memory module **10**, the two chip-select signals (CS_0, CS_1) are used with other address and command signals to gate a set of four gated CAS signals. For example, to access the additional ranks of four-rank 1-GB 128 M×8-byte DDR-1 DRAM memory module, the CS_0 and CS_1 signals along with the other address and command signals are used to gate the CAS signal appropriately, as schematically illustrated by FIG. 11A. FIG. 11B schematically illustrates an exemplary circuit **40** compatible with embodiments described herein. In certain embodiments, the circuit **40**

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comprises a programmable-logic device (PLD) **42** and four "OR" logic elements **52**, **54**, **56**, **58** electrically coupled to corresponding ranks **32a**, **32b**, **32** *c*, **32** *d* of memory devices **30**.

[00135] In certain embodiments, the PLD **42** comprises an ASIC, an FPGA, a custom-designed semiconductor device, or a CPLD. In certain embodiments, the PLD **42** and the four "OR" logic elements **52**, **54**, **56**, **58** are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42** and appropriate "OR" logic elements **52**, **54**, **56**, **58** in accordance with embodiments described herein.

[00136] In the embodiment schematically illustrated by FIG. 11B, the PLD **42** transmits each of the four "enabled CAS" ($ENCAS_0a$, $ENCAS_0b$, $ENCAS_1a$, $ENCAS_1b$) signals to a corresponding one of the "OR" logic elements **52**, **54**, **56**, **58**. The CAS signal is also transmitted to each of the four "OR" logic elements **52**, **54**, **56**, **58**. The CAS signal and the "enabled CAS" signals are "low" true signals. By selectively activating each of the four "enabled CAS" signals which are inputted into the four "OR" logic elements **52**, **54**, **56**, **58**, the PLD **42** is able to select which of the four ranks **32a**, **32b**, **32** *c*, **32** *d* is active.

[00137] In certain embodiments, the PLD **42** uses sequential and combinatorial logic procedures to produce the gated CAS signals which are each transmitted to a corresponding one of the four ranks **32a**, **32b**, **32** *c*, **32** *d*. In certain other embodiments, the PLD **42** instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS_0a, CS_0b, CS_1a, and CS_1b) which are each transmitted to a corresponding one of the four ranks **32a**, **32b**, **32** *c*, **32** *d*.

Tied Data Strobe Signal Pins

[00138] For proper operation, the computer system advantageously recognizes a 1-GB memory module comprising 256-Mb memory devices with 64 M×4-bit configuration as a 1-GB memory module having 512-Mb memory devices with 64 M×8-bit configuration (e.g., as a 1-GB memory module with 128 M×8-byte configuration). This advantageous result is desirably achieved in certain embodiments by electrically connecting together two output signal pins (e.g., DQS or data strobe pins) of the two 256-Mb memory devices such that both output signal pins are concurrently active when the two memory devices are concurrently enabled. The DQS or data strobe is a bi-directional signal that is used during both read cycles

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and write cycles to validate or latch data. As used herein, the terms "tying together" or "tied together" refer to a configuration in which corresponding pins (e.g., DQS pins) of two memory devices are electrically connected together and are concurrently active when the two memory devices are concurrently enabled (e.g., by a common chip-select or CS signal). Such a configuration is different from standard memory module configurations in which the output signal pins (e.g., DQS pins) of two memory devices are electrically coupled to the same source, but these pins are not concurrently active since the memory devices are not concurrently enabled. However, a general guideline of memory module design warns against tying together two output signal pins in this way.

[00139] FIGS. 12 and 13 schematically illustrate a problem which may arise from tying together two output signal pins. FIG. 12 schematically illustrates an exemplary memory module **305** in which a first DQS pin **312** of a first memory device **310** is electrically connected to a second DQS pin **322** of a second memory device **320**. The two DQS pins **312**, **322** are both electrically connected to a memory controller **330**.

[00140] FIG. 13 is an exemplary timing diagram of the voltages applied to the two DQS pins **312**, **322** due to non-simultaneous switching. As illustrated by FIG. 13, at time t_1, both the first DQS pin **312** and the second DQS pin **322** are high, so no current flows between them. Similarly, at time t_4, both the first DQS pin **312** and the second DQS pin **322** are low, so no current flows between them. However, for times between approximately t_2 and approximately t_3, the first DQS pin **312** is low while the second DQS pin **322** is high. Under such conditions, a current will flow between the two DQS pins **312**, **322**. This condition in which one DQS pin is low while the other DQS pin is high can occur for fractions of a second (e.g., 0.8 nanoseconds) during the dynamic random-access memory (DRAM) read cycle. During such conditions, the current flowing between the two DQS pins **312**, **322** can be substantial, resulting in heating of the memory devices **310**, **320**, and contributing to the degradation of reliability and eventual failure of these memory devices.

[00141] A second problem may also arise from tying together two output signal pins. FIG. 14 schematically illustrates another exemplary memory module **305** in which a first DQS pin **312** of a first memory device **310** is electrically connected to a second DQS pin **322** of a second memory device **320**. The two DQS pins **312**, **322** of FIG. 14 are both electrically connected to a memory controller (not shown). The DQ (data input/output) pin **314** of the first

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memory device **310** and the corresponding DQ pin **324** of the second memory device **320** are each electrically connected to the memory controller by the DQ bus (not shown). Typically, each memory device **310**, **320** will have a plurality of DQ pins (e.g., eight DQ pins per memory device), but for simplicity, FIG. 14 only shows one DQ pin for each memory device **310**, **320**.

[00142] Each of the memory devices **310**, **320** of FIG. 14 utilizes a respective on-die termination or "ODT" circuit **332**, **334** which has termination resistors (e.g., 75 ohms) internal to the memory devices **310**, **320** to provide signal termination. Each memory device **310**, **320** has a corresponding ODT signal pin **362**, **364** which is electrically connected to the memory controller via an ODT bus **340**. The ODT signal pin **362** of the first memory device **310** receives a signal from the ODT bus **340** and provides the signal to the ODT circuit **332** of the first memory device **310**. The ODT circuit **332** responds to the signal by selectively enabling or disabling the internal termination resistors **352**, **356** of the first memory device **310**. This behavior is shown schematically in FIG. 14 by the switches **342**, **344** which are either closed (dash-dot line) or opened (solid line). The ODT signal pin **364** of the second memory device **320** receives a signal from the ODT bus **340** and provides the signal to the ODT circuit **334** of the second memory device **320**. The ODT circuit **334** responds to the signal by selectively enabling or disabling the internal termination resistors **354**, **358** of the second memory device **320**. This behavior is shown schematically in FIG. 14 by the switches **346**, **348** which are either closed (dash-dot line) or opened (solid line). The switches **342**, **344**, **346**, **348** of FIG. 14 are schematic representations of the operation of the ODT circuits **332**, **334**, and do not signify that the ODT circuits **332**, **334** necessarily include mechanical switches.

[00143] Examples of memory devices **310**, **320** which include such ODT circuits **332**, **334** include, but are not limited to, DDR2 memory devices. Such memory devices are configured to selectively enable or disable the termination of the memory device in this way in response to signals applied to the ODT signal pin of the memory device. For example, when the ODT signal pin **362** of the first memory device **310** is pulled high, the termination resistors **352**, **356** of the first memory device **310** are enabled. When the ODT signal pin **362** of the first memory device **310** is pulled low (e.g., grounded), the termination resistors **352**, **356** of the first memory device **310** are disabled. By selectively disabling the termination resistors of an active memory device, while leaving the termination resistors of inactive memory devices enabled, such configurations advantageously preserve signal strength on the active memory

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device while continuing to eliminate signal reflections at the bus-die interface of the inactive memory devices.

[00144] In certain configurations, as schematically illustrated by FIG. 14, the DQS pins **312**, **322** of each memory device **310**, **320** are selectively connected to a voltage VTT through a corresponding termination resistor **352**, **354** internal to the corresponding memory device **310**, **320**. Similarly, in certain configurations, as schematically illustrated by FIG. 14, the DQ pins **314**, **324** are selectively connected to a voltage VTT through a corresponding termination resistor **356**, **358** internal to the corresponding memory device **310**, **320**. In certain configurations, rather than being connected to a voltage VTT, the DQ pins **314**, **324** and/or the DQS pins **312**, **322** are selectively connected to ground through the corresponding termination resistors **352**, **354**, **356**, **358**. The resistances of the internal termination resistors **352**, **354**, **356**, **358** are selected to clamp the voltages so as to reduce the signal reflections from the corresponding pins. In the configuration schematically illustrated by FIG. 14, each internal termination resistor **352**, **354**, **356**, **358** has a resistance of approximately 75 ohms.

[00145] When connecting the first memory device **310** and, the second memory device **320** together to form a double word width, both the first memory device **310** and the second memory device **320** are enabled at the same time (e.g., by a common CS signal). Connecting the first memory device **310** and the second memory device **320** by tying the DQS pins **312**, **322** together, as shown in FIG. 14, results in a reduced effective termination resistance for the DQS pins **312**, **322**. For example, for the exemplary configuration of FIG. 14, the effective termination resistance for the DQS pins **312**, **322** is approximately 37.5 ohms, which is one-half the desired ODT resistance (for 75-ohm internal termination resistors) to reduce signal reflections since the internal termination resistors **352**, **354** of the two memory devices **310**, **320** are connected in parallel. This reduction in the termination resistance can result in signal reflections causing the memory device to malfunction.

[00146] FIG. 15 schematically illustrates an exemplary memory module **400** in accordance with certain embodiments described herein. The memory module **400** comprises a first memory device **410** having a first data strobe (DQS) pin **412** and a second memory device **420** having a second data strobe (DQS) pin **422**. The memory module **400** further comprises a first resistor **430** electrically coupled to the first DQS pin **412**. The memory module **400** further comprises a second resistor **440** electrically coupled to the second DQS pin **422** and to the first

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resistor **430**. The first DQS pin **412** is electrically coupled to the second DQS pin **422** through the first resistor **430** and through the second resistor **440**.

[00147] In certain embodiments, the memory module **400** is a 1-GB unbuffered Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) high-density dual in-line memory module (DIMM). FIGS. 16A and 16B schematically illustrate a first side **462** and a second side **464**, respectively, of such a memory module **400** with eighteen 64 M×4-bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board (PCB) **460**. In certain embodiments, the memory module **400** further comprises a phase-lock-loop (PLL) clock driver **470**, an EEPROM for serial-presence detect (SPD) data **480**, and decoupling capacitors (not shown) mounted on the PCB in parallel to suppress switching noise on VDD and VDDQ power supply for DDR-1 SDRAM. By using synchronous design, such memory modules **400** allow precise control of data transfer between the memory module **400** and the system controller. Data transfer can take place on both edges of the DQS signal at various operating frequencies and programming latencies. Therefore, certain such memory modules **400** are suitable for a variety of high-performance system applications.

[00148] In certain embodiments, the memory module **400** comprises a plurality of memory devices configured in pairs, each pair having a first memory device **410** and a second memory device **420**. For example, in certain embodiments, a 128 M×72-bit DDR SDRAM high-density memory module **400** comprises thirty-six 64 M×4-bit DDR-1 SDRAM integrated circuits in FBGA packages configured in eighteen pairs. The first memory device **410** of each pair has the first DQS pin **412** electrically coupled to the second DQS pin **422** of the second memory device **420** of the pair. In addition, the first DQS pin **412** and the second DQS pin **422** are concurrently active when the first memory device **410** and the second memory device **420** are concurrently enabled.

[00149] In certain embodiments, the first resistor **430** and the second resistor **440** each has a resistance advantageously selected to reduce the current flow between the first DQS pin **412** and the second DQS pin **422** while allowing signals to propagate between the memory controller and the DQS pins **412**, **422**. In certain embodiments, each of the first resistor **430** and the second resistor **440** has a resistance in a range between approximately 5 ohms and approximately 50 ohms. For example, in certain embodiments, each of the first resistor **430** and the second resistor **440** has a resistance of approximately 22 ohms. Other resistance values

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for the first resistor **430** and the second resistor **440** are also compatible with embodiments described herein. In certain embodiments, the first resistor **430** comprises a single resistor, while in other embodiments, the first resistor **430** comprises a plurality of resistors electrically coupled together in series and/or in parallel. Similarly, in certain embodiments, the second resistor **440** comprises a single resistor, while in other embodiments, the second resistor **440** comprises a plurality of resistors electrically coupled together in series and/or in parallel.

[00150] FIGS. 17A and 17B schematically illustrate an exemplary embodiment of a memory module **400** in which the first resistor **430** and the second resistor **440** are used to reduce the current flow between the first DQS pin **412** and the second DQS pin **422**. As schematically illustrated by FIG. 17A, the memory module **400** is part of a computer system **500** having a memory controller **510**. The first resistor **430** has a resistance of approximately 22 ohms and the second resistor **440** has a resistance of approximately 22 ohms. The first resistor **430** and the second resistor **440** are electrically coupled in parallel to the memory controller **510** through a signal line **520** having a resistance of approximately 25 ohms. The first resistor **430** and the second resistor **440** are also electrically coupled in parallel to a source of a fixed termination voltage (identified by VTT in FIGS. 17A and 17B) by a signal line **540** having a resistance of approximately 47 ohms. Such an embodiment can advantageously be used to allow two memory devices having lower bit widths (e.g., 4-bit) to behave as a single virtual memory device having a higher bit width (e.g., 8-bit).

[00151] FIG. 17B schematically illustrates exemplary current-limiting resistors **430**, **440** in conjunction with the impedances of the memory devices **410**, **420**. During an exemplary portion of a data read operation, the memory controller **510** is in a high-impedance condition, the first memory device **410** drives the first DQS pin **412** high (e.g., 2.7 volts), and the second memory device **420** drives the second DQS pin **422** low (e.g., 0 volts). The amount of time for which this condition occurs is approximated by the time between t_2 and t_3 of FIG. 13, which in certain embodiments is approximately twice the tDQSQ (data strobe edge to output data edge skew time, e.g., approximately 0.8 nanoseconds). At least a portion of this time in certain embodiments is caused by simultaneous switching output (SSO) effects.

[00152] In certain embodiments, as schematically illustrated by FIG. 17B, the DQS driver of the first memory device **410** has a driver impedance R_1 of approximately 17 ohms, and the DQS driver of the second memory device **420** has a driver impedance R_4 of

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approximately 17 ohms. Because the upper network of the first memory device **410** and the first resistor **430** (with a resistance R_2 of approximately 22 ohms) is approximately equal to the lower network of the second memory device **420** and the second resistor **440** (with a resistance R_3 of approximately 22 ohms), the voltage at the midpoint is approximately 0.5*(2.7−0)=1.35 volts, which equals VTT, such that the current flow across the 47-ohm resistor of FIG. 17B is approximately zero.

[00153] The voltage at the second DQS pin **422** in FIG. 17B is given by $V_{DQS2}=2.7*R_4/(R_1+R_2+R_3+R_4)=0.59$ volts and the current flowing through the second DQS pin **422** is given by $I_{DQS2}=0.59/R_4=34$ milliamps. The power dissipation in the DQS driver of the second memory device **420** is thus $P_{DQS2}=34$ mA*0.59 V=20 milliwatts. In contrast, without the first resistor **430** and the second resistor **440**, only the 17-ohm impedances of the two memory devices **410**, **420** would limit the current flow between the two DQS pins **412**, **422**, and the power dissipation in the DQS driver of the second memory device **420** would be approximately 107 milliwatts. Therefore, the first resistor **430** and the second resistor **440** of FIGS. 17A and 17B advantageously limit the current flowing between the two memory devices during the time that the DQS pin of one memory device is driven high and the DQS pin of the other memory device is driven low.

[00154] In certain embodiments in which there is overshoot or undershoot of the voltages, the amount of current flow can be higher than those expected for nominal voltage values. Therefore, in certain embodiments, the resistances of the first resistor **430** and the second resistor **440** are advantageously selected to account for such overshoot/undershoot of voltages.

[00155] For certain such embodiments in which the voltage at the second DQS pin **422** is $V_{DQS2}=0.59$ volts and the duration of the overdrive condition is approximately 0.8 nanoseconds at maximum, the total surge is approximately 0.59 V*1.2 ns=0.3 V-ns. For comparison, the JEDEC standard for overshoot/undershoot is 2.4 V-ns, so certain embodiments described herein advantageously keep the total surge within predetermined standards (e.g., JEDEC standards).

[00156] FIG. 18 schematically illustrates another exemplary memory module **600** compatible with certain embodiments described herein. The memory module **600** comprises a termination bus **605**. The memory module **600** further comprises a first memory device **610**

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having a first data strobe pin **612**, a first termination signal pin **614** electrically coupled to the termination bus **605**, a first termination circuit **616**, and at least one data pin **618**. The first termination circuit **616** selectively electrically terminating the first data strobe pin **612** and the first data pin **618** in response to a first signal received by the first termination signal pin **614** from the termination bus **605**. The memory module **600** further comprises a second memory device **620** having a second data strobe pin **622** electrically coupled to the first data strobe pin **612**, a second termination signal pin **624**, a second termination circuit **626**, and at least one data pin **628**. The second termination signal pin **624** is electrically coupled to a voltage, wherein the second termination circuit **626** is responsive to the voltage by not terminating the second data strobe pin **622** or the second data pin **628**. The memory module **600** further comprises at least one termination assembly **630** having a third termination signal pin **634**, a third termination circuit **636**, and at least one termination pin **638** electrically coupled to the data pin **628** of the second memory device **620**. The third termination signal pin **634** is electrically coupled to the termination bus **605**. The third termination circuit **636** selectively electrically terminates the data pin **628** of the second memory device **620** through the termination pin **638** in response to a second signal received by the third termination signal pin **634** from the termination bus **605**.

[00157] FIG. 19 schematically illustrates a particular embodiment of the memory module **600** schematically illustrated by FIG. 18. The memory module **600** comprises an on-die termination (ODT) bus **605**. The memory module **600** comprises a first memory device **610** having a first data strobe (DQS) pin **612**, a first ODT signal pin **614** electrically coupled to the ODT bus **605**, a first ODT circuit **616**, and at least one data (DQ) pin **618**. The first ODT circuit **616** selectively electrically terminates the first DQS pin **612** and the DQ pin **618** of the first memory device **610** in response to an ODT signal received by the first ODT signal pin **614** from the ODT bus **605**. This behavior of the first ODT circuit **616** is schematically illustrated in FIG. 14 by the switches **672**, **676** which are selectively closed (dash-dot line) or opened (solid line).

[00158] The memory module **600** further comprises a second memory device **620** having a second DQS pin **622** electrically coupled to the first DQS pin **612**, a second ODT signal pin **624**, a second ODT circuit **626**, and at least one DQ pin **628**. The first DQS pin **612** and the second DQS pin **622** are concurrently active when the first memory device **610** and the

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second memory device **620** are concurrently enabled. The second ODT signal pin **624** is electrically coupled to a voltage (e.g., ground), wherein the second ODT circuit **626** is responsive to the voltage by not terminating the second DQS pin **622** or the second DQ pin **624**. This behavior of the second ODT circuit **626** is schematically illustrated in FIG. 14 by the switches **674**, **678** which are opened.

[00159] The memory module **600** further comprises at least one termination assembly **630** having a third ODT signal pin **634** electrically coupled to the ODT bus **605**, a third ODT circuit **636**, and at least one termination pin **638** electrically coupled to the DQ pin **628** of the second memory device **620**. The third ODT circuit **636** selectively electrically terminates the DQ pin **628** of the second memory device **620** through the termination pin **638** in response to an ODT signal received by the third ODT signal pin **634** from the ODT bus **605**. This behavior of the third ODT circuit **636** is schematically illustrated in FIG. 19 by the switch **680** which is either closed (dash-dot line) or opened (solid line).

[00160] In certain embodiments, the termination assembly **630** comprises discrete electrical components which are surface-mounted or embedded on the printed-circuit board of the memory module **600**. In certain other embodiments, the termination assembly **630** comprises an integrated circuit mounted on the printed-circuit board of the memory module **600**. Persons skilled in the art can provide a termination assembly **630** in accordance with embodiments described herein.

[00161] Certain embodiments of the memory module **600** schematically illustrated by FIG. 19 advantageously avoid the problem schematically illustrated by FIG. 12 of electrically connecting the internal termination resistances of the DQS pins of the two memory devices in parallel. As described above in relation to FIG. 14, FIGS. 18 and 19 only show one DQ pin for each memory device for simplicity. Other embodiments have a plurality of DQ pins for each memory device. In certain embodiments, each of the first ODT circuit **616**, the second ODT circuit **626**, and the third ODT circuit **636** are responsive to a high voltage or signal level by enabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by disabling the corresponding termination resistors. In other embodiments, each of the first ODT circuit **616**, the second ODT circuit **626**, and the third ODT circuit **636** are responsive to a high voltage or signal level by disabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by

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enabling the corresponding termination resistors. Furthermore, the switches **672**, **674**, **676**, **678**, **680** of FIG. 18 are schematic representations of the enabling and disabling operation of the ODT circuits **616**, **626**, **636** and do not signify that the ODT circuits **616**, **626**, **636** necessarily include mechanical switches.

[00162] The first ODT signal pin **614** of the first memory device **610** receives an ODT signal from the ODT bus **605**. In response to this ODT signal, the first ODT circuit **616** selectively enables or disables the termination resistance for both the first DQS pin **612** and the DQ pin **618** of the first memory device **610**. The second ODT signal pin **624** of the second memory device **620** is tied (e.g., directly hard-wired) to the voltage (e.g., ground), thereby disabling the internal termination resistors **654**, **658** on the second DQS pin **622** and the second DQ pin **628**, respectively, of the second memory device **620** (schematically shown by open switches **674**, **678** in FIG. 19). The second DQS pin **622** is electrically coupled to the first DQS pin **612**, so the termination resistance for both the first DQS pin **612** and the second DQS pin **622** is provided by the termination resistor **652** internal to the first memory device **510**.

[00163] The termination resistor **656** of the DQ pin **618** of the first memory device **610** is enabled or disabled by the ODT signal received by the first ODT signal pin **614** of the first memory device **610** from the ODT bus **605**. The termination resistance of the DQ pin **628** of the second memory device **620** is enabled or disabled by the ODT signal received by the third ODT signal pin **634** of the termination assembly **630** which is external to the second memory device **620**. Thus, in certain embodiments, the first ODT signal pin **614** and the third ODT signal pin **634** receive the same ODT signal from the ODT bus **605**, and the termination resistances for both the first memory device **610** and the second memory device **620** are selectively enabled or disabled in response thereto when these memory devices are concurrently enabled. In this way, certain embodiments of the memory module **600** schematically illustrated by FIG. 19 provides external or off-chip termination of the second memory device **620**.

[00164] Certain embodiments of the memory module **600** schematically illustrated by FIG. 19 advantageously allow the use of two lower-cost readily-available 512-Mb DDR-2 SDRAM devices to provide the capabilities of a more expensive 1-GB DDR-2 SDRAM device. Certain such embodiments advantageously reduce the total cost of the resultant memory module **600**.

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[00165] Certain embodiments described herein advantageously increase the memory capacity or memory density per memory slot or socket on the system board of the computer system. Certain embodiments advantageously allow for higher memory capacity in systems with limited memory slots. Certain embodiments advantageously allow for flexibility in system board design by allowing the memory module **10** to be used with computer systems designed for different numbers of ranks (e.g., either with computer systems designed for two-rank memory modules or with computer systems designed for four-rank memory modules). Certain embodiments advantageously provide lower costs of board designs.

[00166] In certain embodiments, the memory density of a memory module is advantageously doubled by providing twice as many memory devices as would otherwise be provided. For example, pairs of lower-density memory devices can be substituted for individual higher-density memory devices to reduce costs or to increase performance. As another example, twice the number of memory devices can be used to produce a higher-density memory configuration of the memory module. Each of these examples can be limited by the number of chip select signals which are available from the memory controller or by the size of the memory devices. Certain embodiments described herein advantageously provide a logic mechanism to overcome such limitations.

[00167] Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

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WE CLAIM:

1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory bus including address and control signal lines and data signal lines, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals, the set of input address and control signals including a plurality of input chip select signals and other input address and control signals, the plurality of input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value, the set of registered address and control signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals, the plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value, wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of ranks are configured to receive respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by one respective N-bit wide rank of the plurality of N-bit-wide ranks, wherein one of the plurality of ranks receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command; and

circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit

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wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;

wherein data transfers through the circuitry are registered for an additional amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

2. The memory module of claim 1, wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus.

3. The memory module of claim 1, wherein the first burst of N-bit wide data signals includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein the set of consecutively transmitted data bits are successively transferred through the circuitry in response to the data buffer control signals.

4. The memory module of claim 1, wherein each of the memory devices is 4-bits wide, and wherein each of the plurality of ranks is 72-bits wide and includes 18 memory devices configured in pairs, and wherein each pair of 4-bit-wide memory devices are configured to simulate an 8-bit-wide memory device.

5. The memory module of claim 1, wherein the memory devices are organized in four ranks and the first set of input address and control signals include four chip select signals, one for each of the four ranks.

6. The memory module of claim 1, wherein the circuitry includes logic pipelines configurable to enable the data transfers between the memory devices and the memory bus through the circuitry.

7. The memory module of claim 1, wherein the logic is further configured to report the overall CAS latency to the memory controller in response to a mode register set command received from the memory controller.

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8. The memory module of claim 1, wherein the memory module has a specified data rate, and wherein the burst of N-bit wide data signals are transferred between the one of the plurality of ranks and the memory controller at the specified data rate.

9. The memory module of claim 1, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.

10. The memory module of claim 9, wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the one of the plurality of ranks is configured receive or output a respective set of bits of the first burst of N-bit wide data signals on both edges of each of a respective set of data strobes.

11. The memory module of claim 1, wherein the circuitry includes data paths, and wherein the circuitry is configurable to enable the data paths in response to the data buffer control signals so that the N-bit wide data signals are transferred via the data paths.

12. The memory module of claim 11, wherein the data paths are disabled when no data signals associated with any memory command are being transferred through the circuitry.

13. The memory module of claim 12, wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus.

14. The memory module of claim 12, wherein the memory module has a specified data rate, and wherein the burst of N-bit wide data signals are transferred through the data paths at the specified data rate.

15. The memory module of claim 12, wherein the read or write command is a write memory command, wherein the burst of N-bit wide data signals include a respective series of write data bits received by the circuitry from a respective one of the data signal lines, and wherein the respective series of write data bits are successively transferred via a respective one of the data paths.

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MEMORY MODULE WITH DATA BUFFERING

ABSTRACT OF THE DISCLOSURE

A memory module operable to communicate data with a memory controller via a N-bit wide memory bus comprises memory devices arranged in a plurality of N-bit wide ranks. The memory module further comprises logic configurable to receive a set of input address and control signals associated with a read or write memory command and output registered address and control signals and data buffer control signals. The memory module further comprises circuitry coupled between the memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks. The circuitry is configurable to enable registered transfers of N-bit wide data signals associated with the memory read or write command between the N-bit wide memory bus and the memory devices in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module, which is greater than an actual operational CAS latency of the memory devices.

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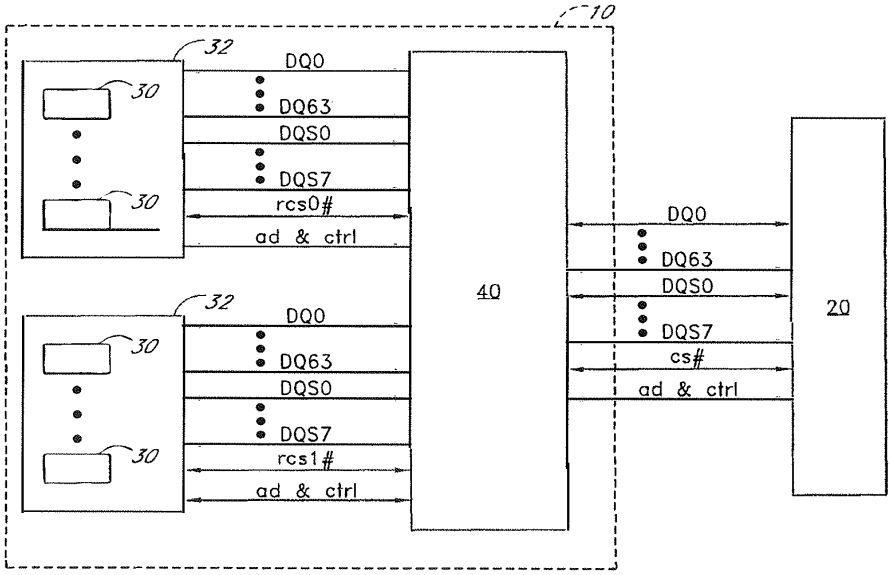

10
32
30
30
DQ0
DQ63
DQS0
DQS7
rcs0#
ad & ctrl
32
30
30
DQ0
DQ63
DQS0
DQS7
rcs1#
ad & ctrl
40
DQ0
DQ63
DQS0
DQS7
cs#
ad & ctrl
20

FIG. 1

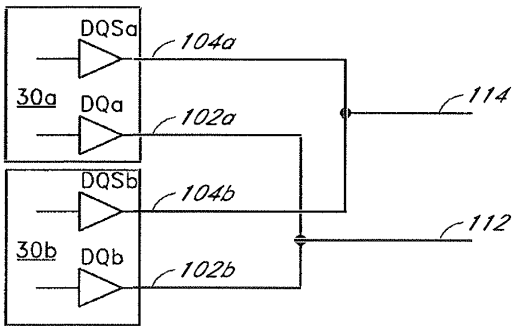


FIG. 2

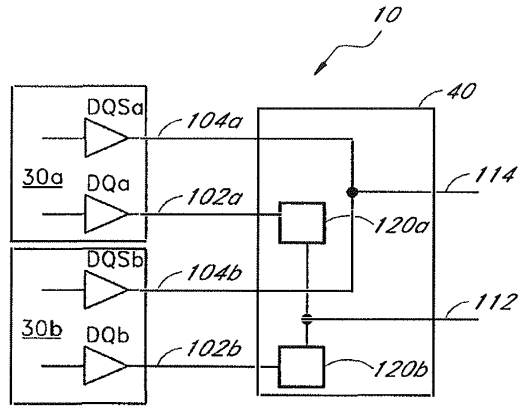

10
40
DQSa
104a
30a
DQa
102a
114
120a
DQSb
104b
112
30b
DQb
102b
120b

FIG. 3A

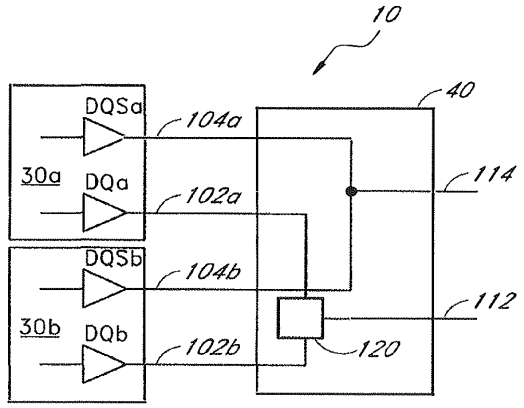

10
40
DQSa
104a
30a
DQa
102a
114
DQSb
104b
112
30b
DQb
102b
120

FIG. 3B

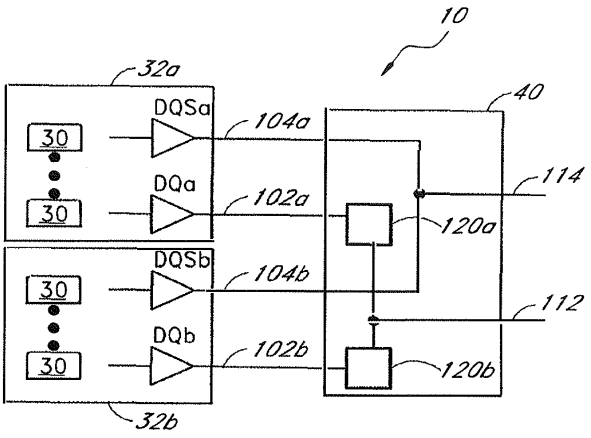

10
32a
DQSa
104a
30
DQa
102a
30
40
114
120a
DQSb
104b
30
112
DQb
102b
30
120b
32b

FIG. 4A

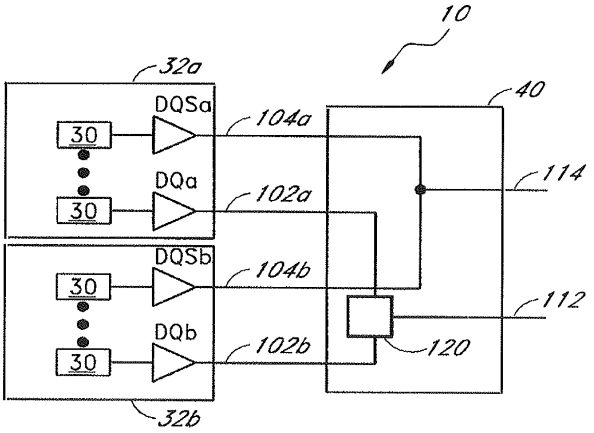

10
32a
40
DQSa
104a
30
114
DQa
102a
30
DQSb
104b
30
112
DQb
102b
30
120
32b

FIG. 4B

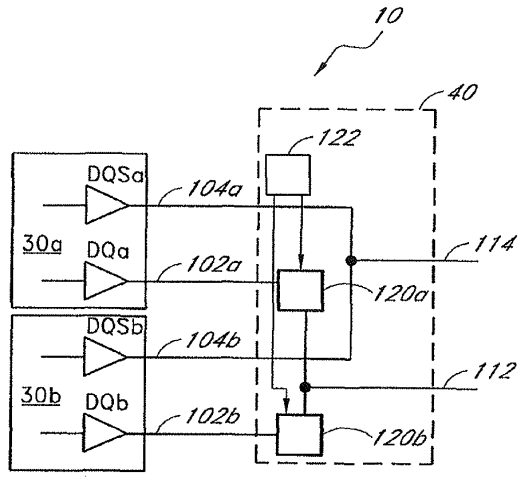

10
40
122
DQSa
104a
30a
DQa
102a
114
120a
DQSb
104b
112
30b
DQb
102b
120b

FIG. 5A

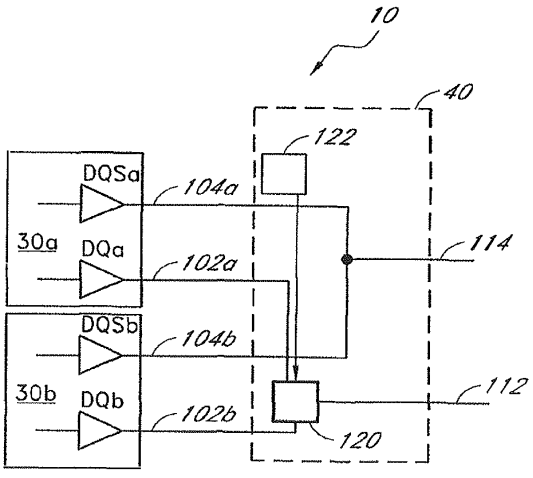

10
40
122
DQSa
104a
30a
DQa
102a
114
DQSb
104b
112
30b
DQb
102b
120

FIG. 5B

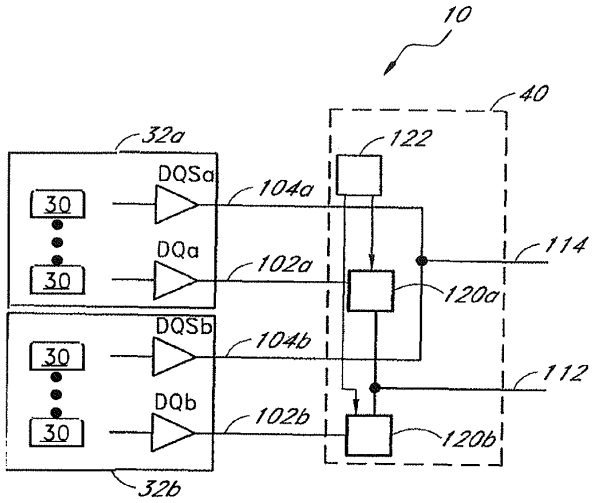

10
40
32a
122
DQSa
104a
30
30
DQa
102a
114
120a
DQSb
104b
30
30
112
DQb
102b
120b
32b

FIG. 5C

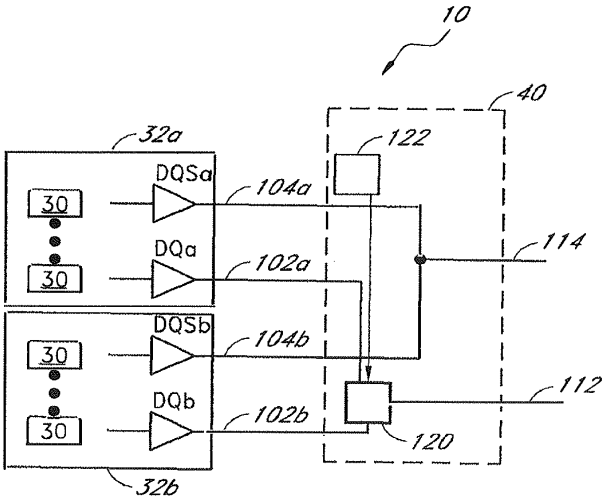

10
40
32a
122
DQSa
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30
DQa
102a
114
DQSb
104b
30
30
112
DQb
102b
120
32b

FIG. 5D

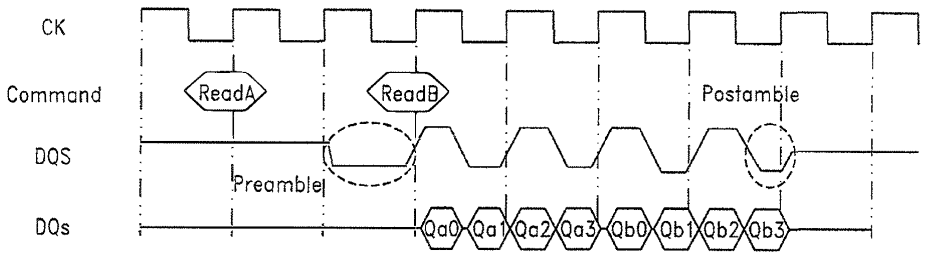

CK
Command
ReadA
ReadB
Postamble
DQS
Preamble
DQs
Qa0
Qa1
Qa2
Qa3
Qb0
Qb1
Qb2
Qb3

FIG. 6A

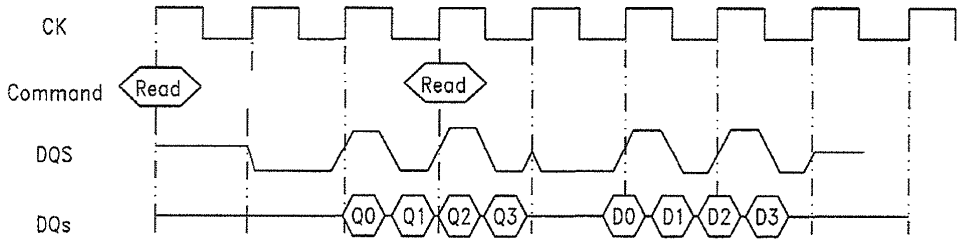

CK
Command
Read
Read
DQS
DQs
Q0
Q1
Q2
Q3
D0
D1
D2
D3

FIG. 6B

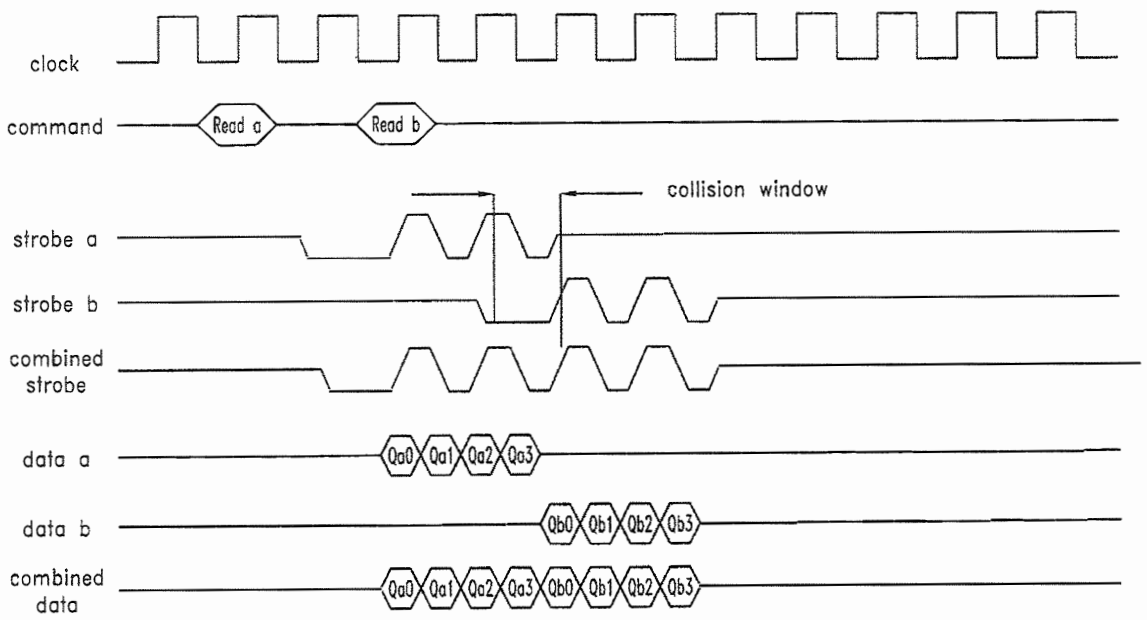

clock
command
Read a
Read b
collision window
strobe a
strobe b
combined strobe
data a
Qa0
Qa1
Qa2
Qa3
data b
Qb0
Qb1
Qb2
Qb3
combined data
Qa0
Qa1
Qa2
Qa3
Qb0
Qb1
Qb2
Qb3

FIG. 7

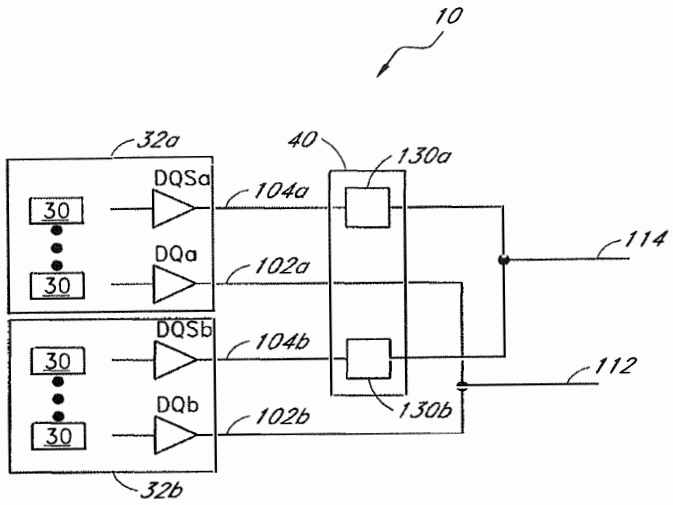

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32a
40
130a
DQSa
104a
30
30
DQa
102a
114
DQSb
104b
30
30
112
DQb
102b
130b
32b

FIG. 8A

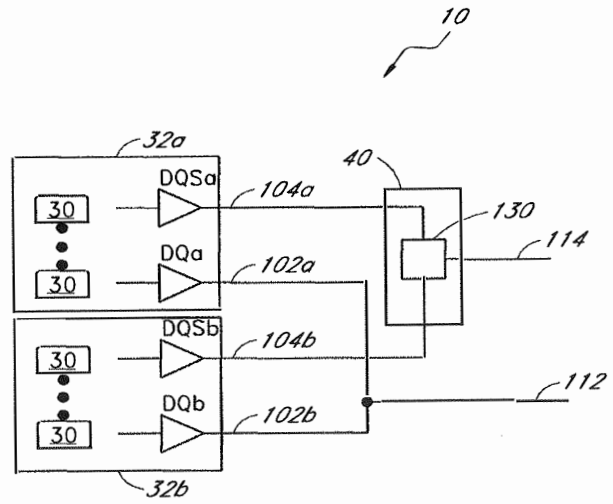

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32a
40
DQSa
104a
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130
114
DQa
102a
DQSb
104b
30
30
112
DQb
102b
32b

FIG. 8B

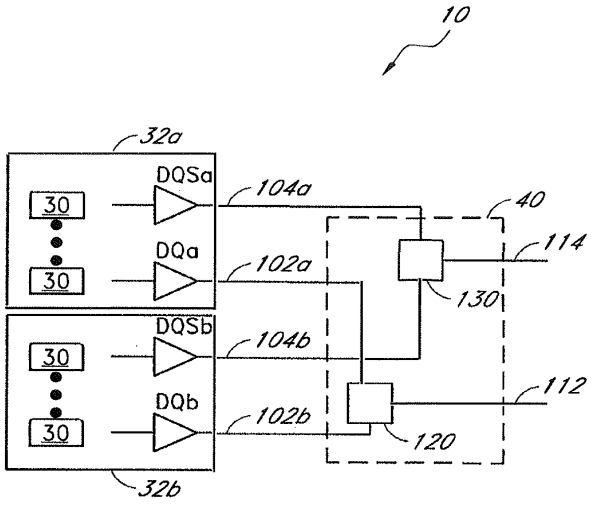

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32a
DQSa
104a
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30
114
DQa
102a
30
130
DQSb
104b
30
112
DQb
102b
30
120
32b

FIG. 8C

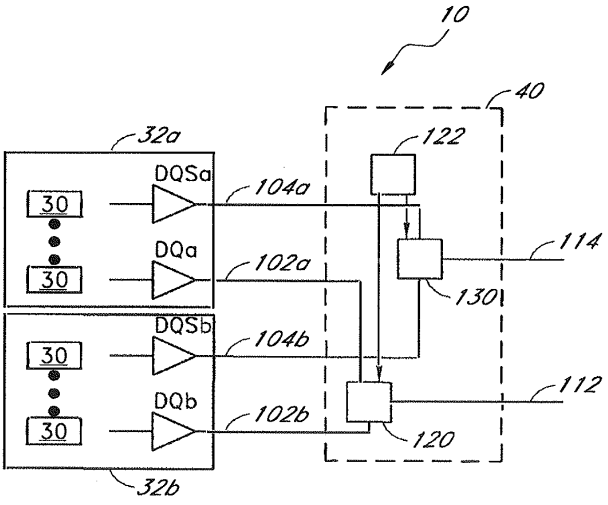

10
40
32a
122
DQSa
104a
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114
DQa
102a
30
130
DQSb
104b
30
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DQb
102b
30
120
32b

FIG. 8D

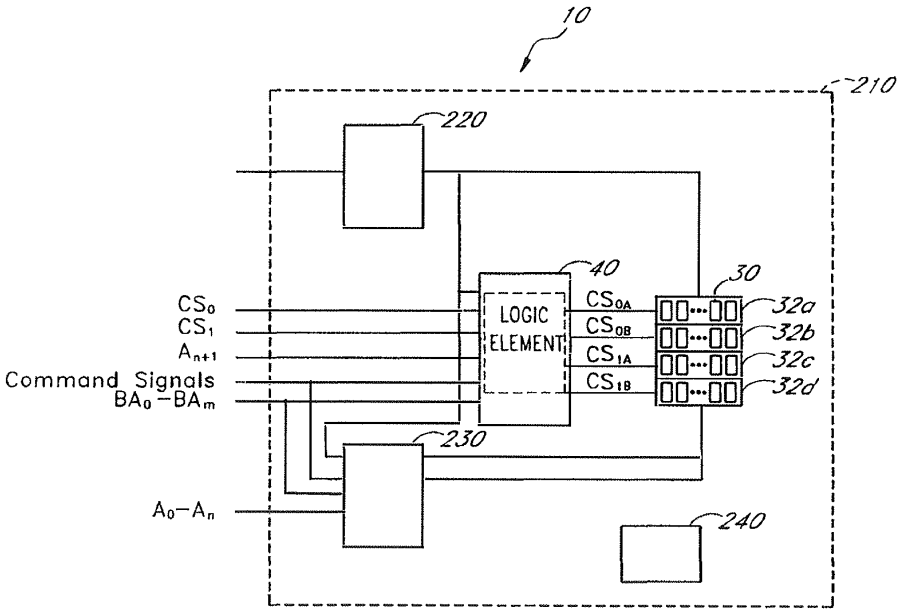

10
210
220
40
30
LOGIC ELEMENT
CS_0
CS_1
A_{n+1}
Command Signals
BA_0-BA_m
CS_{0A}
CS_{0B}
CS_{1A}
CS_{1B}
32a
32b
32c
32d
230
A_0-A_n
240

FIG. 9A

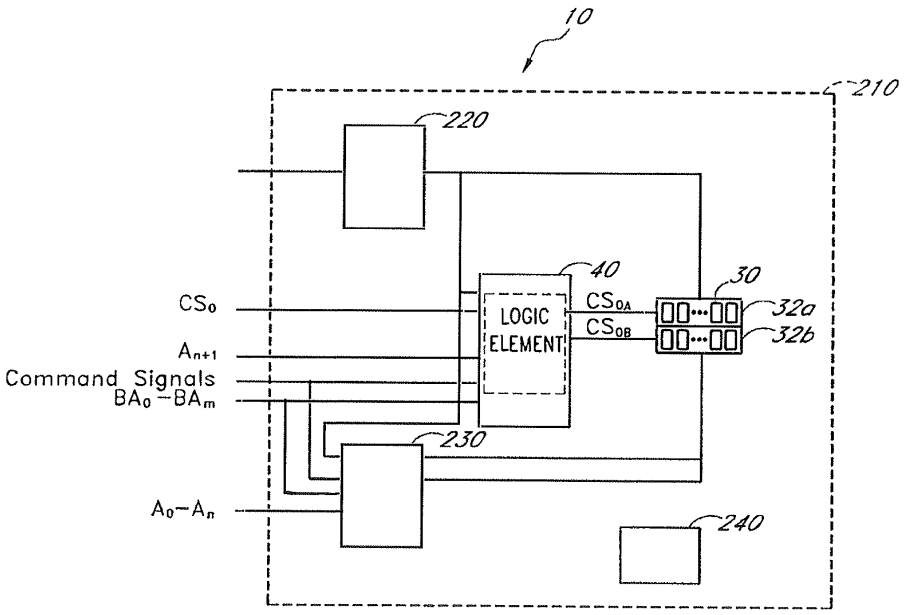

10
210
220
40
30
LOGIC ELEMENT
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230
240
CS0
An+1
Command Signals
BA0 – BAm
A0 – An
CS0A
CS0B

FIG. 9B

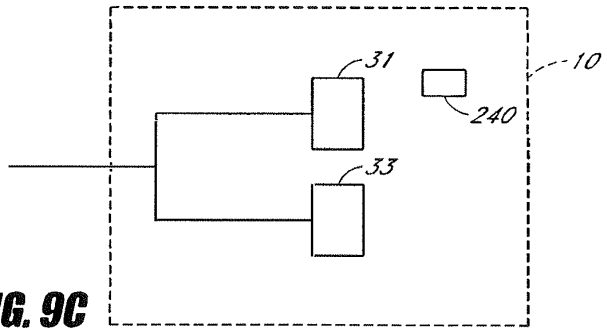


FIG. 9C

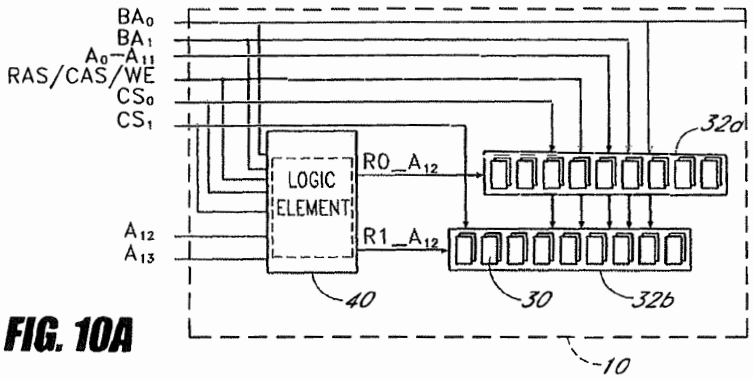


FIG. 10A

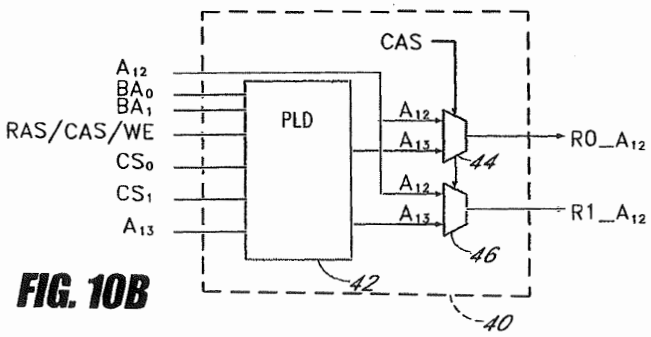


FIG. 10B

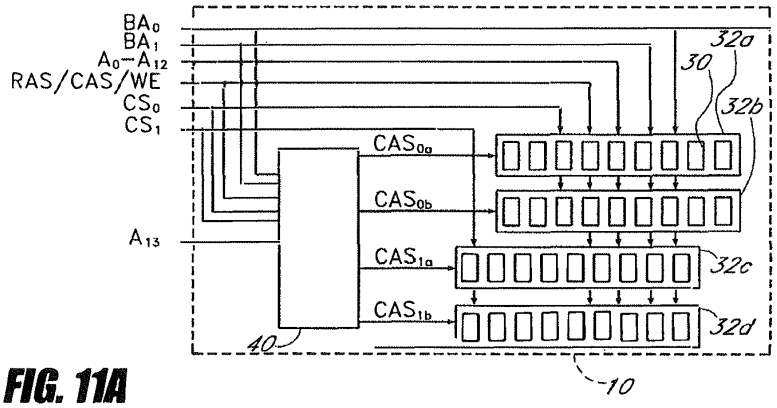


FIG. 11A

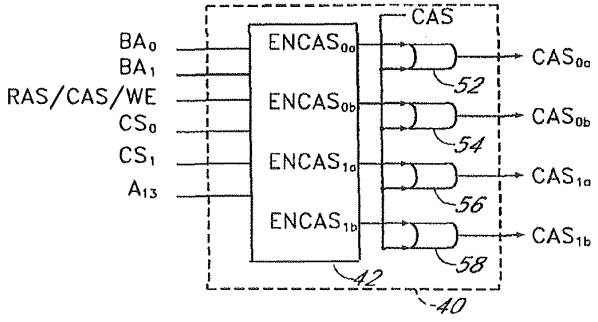


FIG. 11B

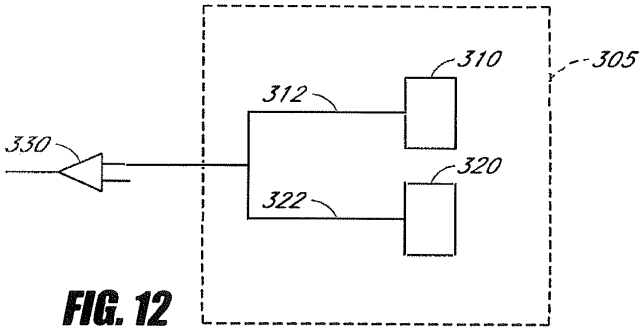


FIG. 12

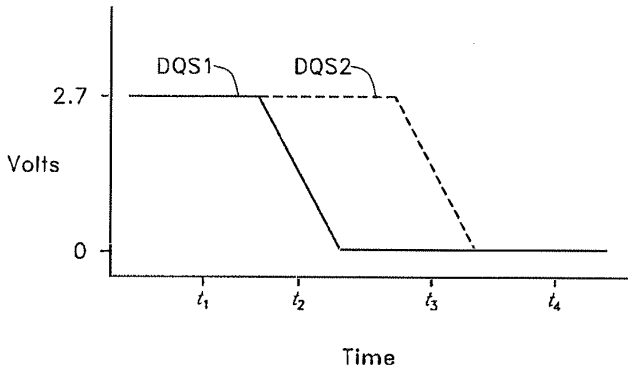


FIG. 13

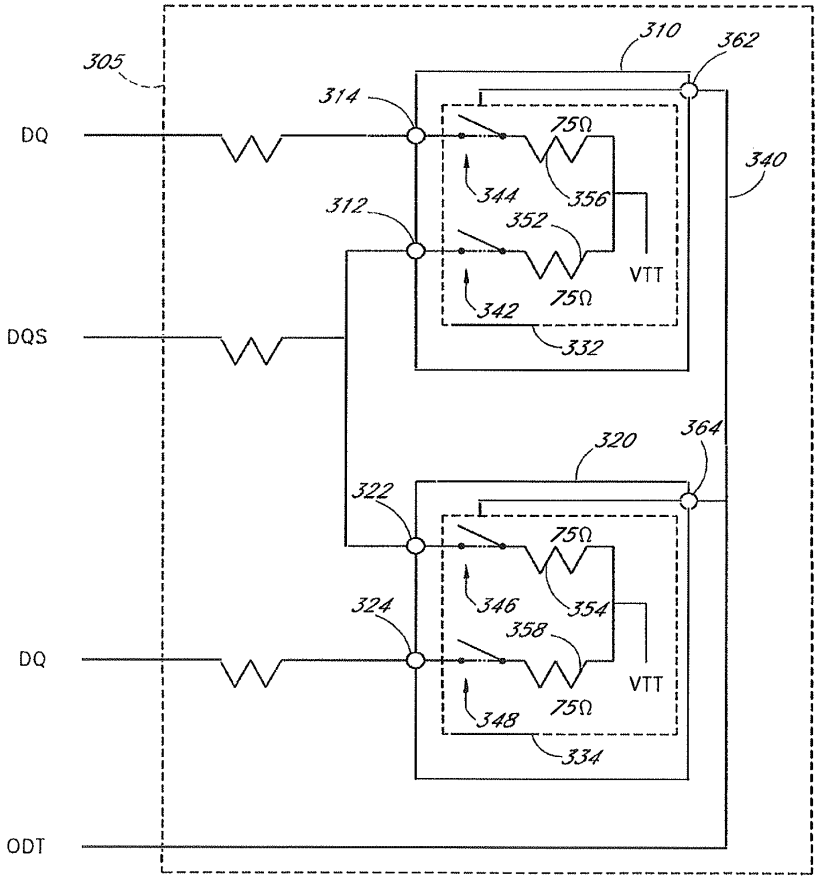

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FIG. 14

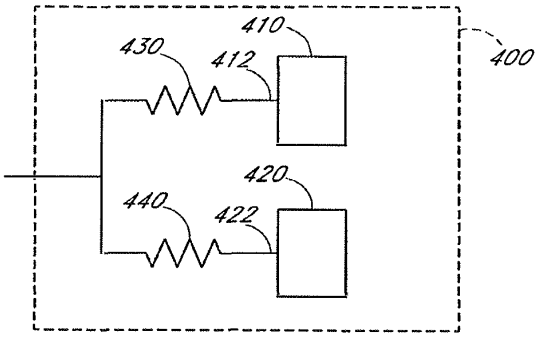


FIG. 15

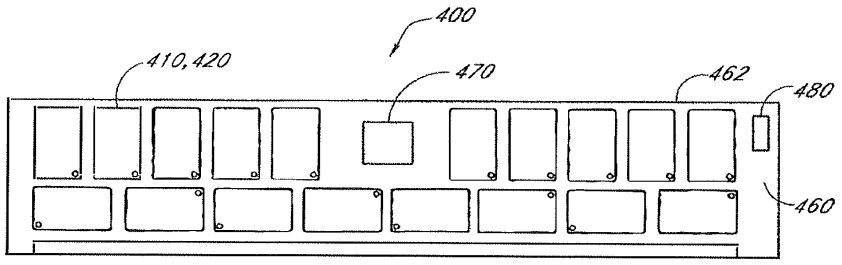


FIG. 16A

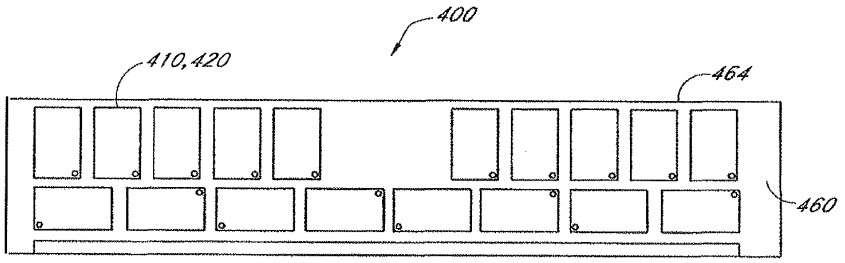


FIG. 16B

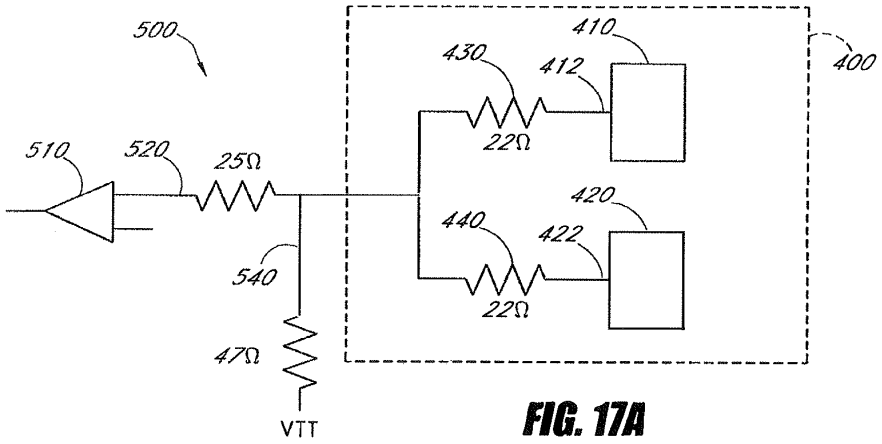


FIG. 17A

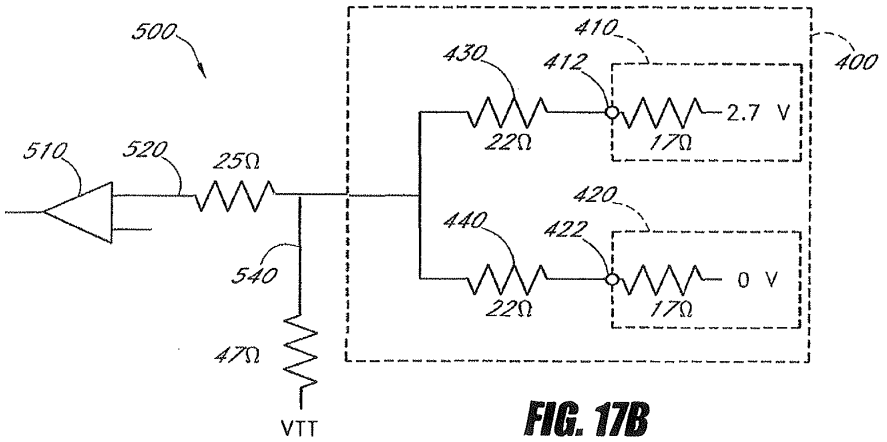


FIG. 17B

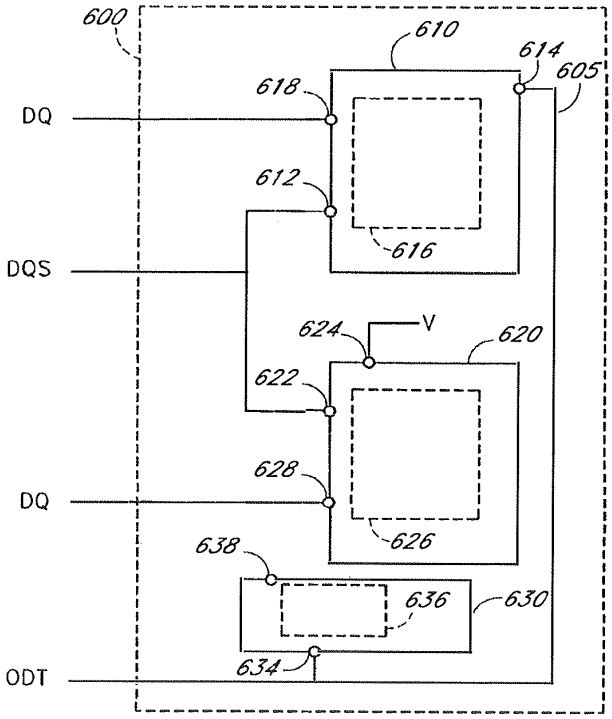

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FIG. 18

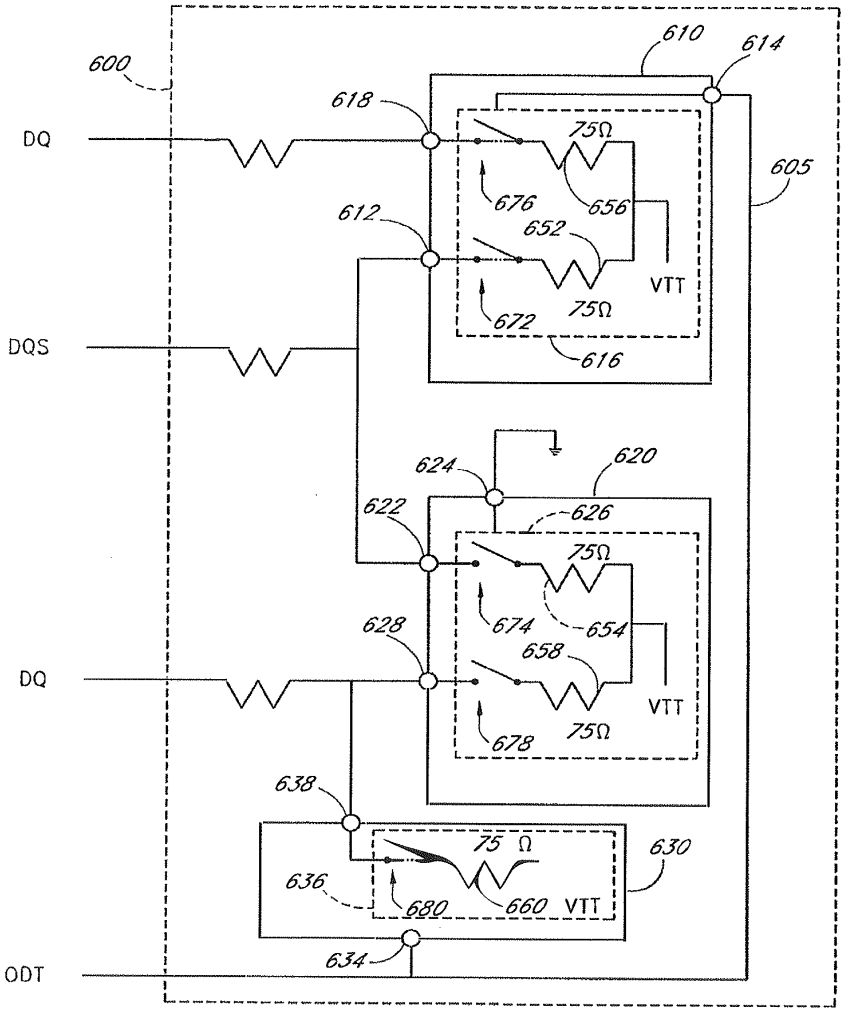

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FIG. 19

Electronically filed November 25, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jefferey C. Solomon	Confirmation No.:	To be assigned
Serial No.:	To be assigned	Art Unit	To be assigned
Filed:	Filed herewith	Examiner:	To be assigned
For:	MEMORY MODULE WITH DATA BUFFERING	Attorney Docket No.:	129980-5023-US01

STATEMENT UNDER 37 C.F.R. § 3.73(c)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Netlist, Inc., a corporation, states that it is the assignee of the entire right, title and interest in the patent application/patent identified above by virtue of an assignment from the inventor(s) of the parent of the patent application/patent identified above.

The assignment was recorded in the United States Patent and Trademark Office on July 17, 2006 at Reel 018104, Frame 0964, or for which a copy thereof is attached.

The undersigned is authorized to act on behalf of the assignee.

Date: November 25, 2019

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

GENERAL POWER OF ATTORNEY BY APPLICANT FOR UNITED STATES PATENT

I hereby revoke all previous powers of attorney given in the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

I hereby appoint the practitioner associated with the following Customer Number :

79141

as my/our attorney or agent, and to transact all business in the United States Patent and Trademark Office in connection with the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

Please recognize or change the **correspondence address** for the application referenced in the attached transmittal letter to the address associated with the above-mentioned **Customer Number**.

I am the Applicant:

- ☐ Inventor or Joint Inventor
- ☐ Legal Representative of a Deceased or Legally Incapacitated Inventor
- ■ Assignee or Person to Whom the Inventor is Under an Obligation to Assign
- ☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is currently being filed in this document)

SIGNATURE of Applicant for Patent

Signature		Date: January 9, 2013
Name	**Gail Sasaki**	
Title	Vice President and Chief Financial Officer	
Company	Netlist, Inc.	

Note: Signature - this form must be signed by the Applicant or a person authorized to act on behalf of Applicant.

Submit multiple forms for more than one signature
Total of __ forms are submitted.

Customer No. 79141
Attorney Docket No.: NETL.018P2C7

Modified PTO/AIA/01 (06-12)

DECLARATION FOR UTILITY OR DESIGN APPLICATION

Title of Invention	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE

As a below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

■ United States application or PCT international application number 13/971,231 filed on August 20, 2013.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Note to Inventor: 37 C.F.R. § 1.63(c) states: "A person may not execute an oath or declaration for an application unless that person has reviewed and understands the contents of the application, including the claims, and is aware of the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56."

First Inventor (Legal Name): Jefferey C. Solomon

Signature: Jeffrey C. Solomon Date (Optional): 10-14-2013

Second Inventor (Legal Name): Jayesh R. Bhakta

Signature: Jayesh Bhakta Date (Optional): 10-14-2013

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5023-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jefferey	C.	Solomon	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	Irvine	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	16 Silver Fir
Address 2	
City	Irvine
State/Province	CA
Postal Code	92604
Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jayesh	R.	Bhakta	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	Cerritos	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	12220 Rose Street
Address 2	
City	Cerritos
State/Province	CA
Postal Code	90703
Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5023-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	79141		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	MEMORY MODULE WITH DATA BUFFERING		
Attorney Docket Number	129980-5023-US01	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	23	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	79141		

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5023-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending			Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)	
	Continuation of	15/857519	2017-12-28	

Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/857519	Continuation of	14/715486	2015-05-18	9858215	2018-01-02

Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14/715486	Continuation of	13/971232	2013-08-20	9037774	2019-05-19

Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/971232	Continuation of	13/287081	2011-11-01	8516188	2013-08-20

Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/287081	Continuation of	13/032470	2011-02-22	8081536	2011-12-20

Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/032470	Continuation of	12/955711	2010-11-29	7916574	2011-03-29

Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/955711	Continuation of	12/629827	2009-12-02	781150	2011-02-01

Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/629827	Continuation of	12/408652	2009-03-20	7636274	2009-12-22

Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/408652	Continuation of	11/335875	2006-01-19	7532537	2009-05-12

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5023-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/335875	Claims benefit of provisional	60/645087	2005-01-19
Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11/335875	Continuation in part of	11/173175	2005-07-01	7289386	2007-10-30

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/173175	Claims benefit of provisional	60/588244	2004-07-15
Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11/173175	Continuation in part of	11/075395	2005-03-07	7286436	2007-10-23

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/075395	Claims benefit of provisional	60/550668	2004-03-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/075395	Claims benefit of provisional	60/575595	2004-05-28
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/075395	Claims benefit of provisional	60/590038	2004-07-21

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5023-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5023-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5023-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Netlist, Inc.		
Mailing Address Information For Applicant:			
Address 1	175 Technology		
Address 2	Suite 150		
City	Irvine	**State/Province**	CA
Country	US	Postal Code	92618
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5023-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/ Jamie J. Zheng /			Date (YYYY-MM-DD)	2019-11-25
First Name	Jamie J.	Last Name	Zheng	Registration Number	51167

Additional Signature may be generated within this form by selecting the Add button. Add

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5023-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	37856763
Application Number:	16695020
International Application Number:	
Confirmation Number:	7514
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023-US01
Receipt Date:	25-NOV-2019
Filing Date:	
Time Stamp:	20:21:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	129980-5023US01_TRANS.pdf	148340 fa5d825ceb8175b300ef0dc81434caca5bac526b	no	1

Warnings:

Information:					
2		129980-5023-US01_APPLN.pdf	3788816 3fcbb6037e41311b7b591ba17a7fba1cd8507c62	yes	57
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	53	
	Claims		54	56	
	Abstract		57	57	
Warnings:					
Information:					
3	Drawings-only black and white line drawings	129980-5023US01_DRAWINGS.pdf	384446 305c6f73bb74edcc1e4743658661e3783ae60ecf	no	23
Warnings:					
Information:					
4		129980-5023US01_STMT_POA.pdf	370705 c6ac5243069de545a7e463f3b8ef1a69325a6b1c	yes	2
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Assignee showing of ownership per 37 CFR 3.73		1	1	
	Power of Attorney		2	2	
Warnings:					
Information:					
5	Oath or Declaration filed	129980-5023-US01_DECL.pdf	68755 7a040447f5849d1ce42a7d29b21b3d6e7d30d6cb	no	1
Warnings:					
Information:					
6	Application Data Sheet	129980-5023US01_ADS.pdf	1257012 214d5e80b3dde8c38cbdce34daaf78ff5495914d	no	10

Warnings:	
Information:	
Total Files Size (in bytes):	6018074

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/695,020	11/25/2019	Jefferey C. Solomon	129980-5023-US01

CONFIRMATION NO. 7514

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

FORMALITIES LETTER

OC000000113322580

Date Mailed: 12/16/2019

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1880** TOTAL FEE BALANCE DUE.

Petitioners
Ex. 1057, p. 98

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/afessehaye/

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/695,020

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	15 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/695,020	11/25/2019	2139	0.00	129980-5023-US01	15	1

CONFIRMATION NO. 7514

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

FILING RECEIPT

OC000000113322579

Date Mailed: 12/16/2019

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Jefferey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: The patent practitioners associated with Customer Number 79141

Domestic Priority data as claimed by applicant

This application is a CON of 15/857,519 12/28/2017 PAT 10489314
which is a CON of 14/715,486 05/18/2015 PAT 9858215
which is a CON of 13/971,232 08/20/2013 ABN
which is a CON of 13/287,081 11/01/2011 PAT 8516188
which is a CON of 13/032,470 02/22/2011 PAT 8081536
which is a CON of 12/955,711 11/29/2010 PAT 7916574
which is a CON of 12/629,827 12/02/2009 PAT 7881150
which is a CON of 12/408,652 03/20/2009 PAT 7636274
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7289386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7286436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004

and claims benefit of 60/590,038 07/21/2004

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 12/13/2019
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/695,020**
Projected Publication Date: To Be Determined - pending completion of Missing Parts
Non-Publication Request: No
Early Publication Request: No
Title

MEMORY MODULE WITH DATA BUFFERING

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

Document Description: Application Data Sheet to update/correct info
Doc Code: ADS.CORR

CORRECTED ADS FORM

Application Number	16695020
Title of Invention	MEMORY MODULE WITH DATA BUFFERING

Inventor Information

****If no data is shown, no data has been corrected****

	Data of Record	Updated Data
Order Number		
Name		
Residence Information		
Residency		
City		
State		
Country of Residence		
Mailing Address of Inventor		
Address 1		
Address 2		
City,State/Province, Postal Code		
Country		

Document Description: Application Data Sheet to update/correct info
Doc Code: ADS.CORR

Application Information

	Data of Record	Updated Data
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	
Attorney Docket Number	129980-5023-US01	
Entity Type	Regular Undiscounted	

Domestic Benefit/National Stage Information

****If no data is shown, no data has been corrected****

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121,365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S. C. 119(e) or 120, and 37 CFR 1.78(a).

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	16695020	
	Continuity Type	CON	
	Prior Application Number	15857519	
	Filing Date (YYYY-MM-DD)	2017-12-28	
	Patent Number	10489314	
	Issue Date (YYYY-MM-DD)	2019-11-26	

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	15857519	
	Continuity Type	CON	
	Prior Application Number	14715486	
	Filing Date (YYYY-MM-DD)	2015-05-18	
	Patent Number	9858215	
	Issue Date (YYYY-MM-DD)	2018-01-02	

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	11335875	
	Continuity Type	CIP	
	Prior Application Number	11173175	
	Filing Date (YYYY-MM-DD)	2005-07-01	
	Patent Number	7289386	
	Issue Date (YYYY-MM-DD)	2007-10-30	

		Data of Record	Updated Data
	Prior Application Status	pending	
	Application Number	11173175	
	Continuity Type	PRO	
	Prior Application Number	60588244	
	Filing Date (YYYY-MM-DD)	2004-07-15	
	Patent Number		
	Issue Date (YYYY-MM-DD)	0001-01-01	

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	11173175	
	Continuity Type	CIP	
	Prior Application Number	11075395	
	Filing Date (YYYY-MM-DD)	2005-03-07	
	Patent Number	7286436	
	Issue Date (YYYY-MM-DD)	2007-10-23	

		Data of Record	Updated Data
	Prior Application Status	pending	
	Application Number	11075395	
	Continuity Type	PRO	
	Prior Application Number	60550668	
	Filing Date (YYYY-MM-DD)	2004-03-05	
	Patent Number		
	Issue Date (YYYY-MM-DD)	0001-01-01	

		Data of Record	Updated Data
	Prior Application Status	pending	
	Application Number	11075395	
	Continuity Type	PRO	
	Prior Application Number	60575595	
	Filing Date (YYYY-MM-DD)	2004-05-28	
	Patent Number		
	Issue Date (YYYY-MM-DD)	0001-01-01	

Document Description: Application Data Sheet to update/correct info
Doc Code: ADS.CORR

		Data of Record	Updated Data
	Prior Application Status	pending	
	Application Number	11075395	
	Continuity Type	PRO	
	Prior Application Number	60590038	
	Filing Date (YYYY-MM-DD)	2004-07-21	
	Patent Number		
	Issue Date (YYYY-MM-DD)	0001-01-01	

		Data of Record	Updated Data
	Prior Application Status	abandoned	
	Application Number	14715486	
	Continuity Type	CON	
	Prior Application Number	~~13971232~~	13971231
	Filing Date (YYYY-MM-DD)	2013-08-20	
	Patent Number		
	Issue Date (YYYY-MM-DD)	0001-01-01	

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	~~13971232~~	13971231
	Continuity Type	CON	
	Prior Application Number	13287081	
	Filing Date (YYYY-MM-DD)	2011-11-01	
	Patent Number	8516188	
	Issue Date (YYYY-MM-DD)	2013-08-20	

Corrected ADS 1.0

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	13287081	
	Continuity Type	CON	
	Prior Application Number	13032470	
	Filing Date (YYYY-MM-DD)	2011-02-22	
	Patent Number	8081536	
	Issue Date (YYYY-MM-DD)	2011-12-20	

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	13032470	
	Continuity Type	CON	
	Prior Application Number	12955711	
	Filing Date (YYYY-MM-DD)	2010-11-29	
	Patent Number	7916574	
	Issue Date (YYYY-MM-DD)	2011-03-29	

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	12955711	
	Continuity Type	CON	
	Prior Application Number	12629827	
	Filing Date (YYYY-MM-DD)	2009-12-02	
	Patent Number	7881150	
	Issue Date (YYYY-MM-DD)	2011-02-01	

Document Description: Application Data Sheet to update/correct info
Doc Code: ADS.CORR

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	12629827	
	Continuity Type	CON	
	Prior Application Number	12408652	
	Filing Date (YYYY-MM-DD)	2009-03-20	
	Patent Number	7636274	
	Issue Date (YYYY-MM-DD)	2009-12-22	

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	12408652	
	Continuity Type	CON	
	Prior Application Number	11335875	
	Filing Date (YYYY-MM-DD)	2006-01-19	
	Patent Number	7532537	
	Issue Date (YYYY-MM-DD)	2009-05-12	

		Data of Record	Updated Data
	Prior Application Status	pending	
	Application Number	11335875	
	Continuity Type	PRO	
	Prior Application Number	60645087	
	Filing Date (YYYY-MM-DD)	2005-01-19	
	Patent Number		
	Issue Date (YYYY-MM-DD)	0001-01-01	

Corrected ADS 1.0

Document Description: Application Data Sheet to update/correct info
Doc Code: ADS.CORR

Foreign Priority Information

****If no data is shown, no data has been corrected****

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

		Data of Record	Updated Data
	Application Number		
	Country		
	Filing Date		
	Access Code		

Applicant Information

****If no data is shown, no data has been corrected****
Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

	Data of Record	Updated Data
Applicant Type		
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is		
Name of the Deceased or Legally Incapacitated Inventor		
Applicant is an Organization		
Name		
Organization Name		
Address 1		

Corrected ADS 1.0

Address 2		
City,State/Province,Postal Code		
Country		
Phone Number		
Fax Number		
Email Address		

Assignee Information including Non-Applicant Assignee Information

****If no data is shown, no data has been corrected****
Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office

	Data of Record	Updated Data
Order		
Applicant is an Organization		
Name		
Organization Name		

Mailing Address

Address 1		
Address 2		
City,State/Province,Postal Code		
Country		
Phone Number		
Fax Number		

Email Address		

Signature

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b).

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/ Jamie J. Zheng /	Registration Number	51167
First Name	Jamie J.	Last Name	Zheng

Electronically filed January 21, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jefferey C. Solomon	Confirmation No.:	7514
Serial No.:	16/695,020	Art Unit:	2139
Filed:	November 25, 2019	Examiner:	TBD
For:	*MEMORY MODULE WITH DATA BUFFERING*	Attorney Docket No.:	129980-5023-US01

MISCELLANEOUS COMMUNICATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants concurrently submit with this Communication a Supplemental Application Data Sheet which has been updated to the extent:

Domestic Benefit/National Stage Information:

1. Correcting priority claim from 13/971,232 to **13/971,231**

No other information on the Application Data Sheet has been changed or added.

Applicants respectfully request an updated filing receipt be mailed to Applicant.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US01).

Respectfully submitted,

Date: January 21, 2020

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)

MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

Electronic Acknowledgement Receipt	
EFS ID:	38357157
Application Number:	16695020
International Application Number:	
Confirmation Number:	7514
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023-US01
Receipt Date:	21-JAN-2020
Filing Date:	25-NOV-2019
Time Stamp:	18:03:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet to update/ correct info	CorrectedADS.pdf	151944 3fdce627e97387150199431 4e4632448ba0f09e3	no	10
Warnings:					

Information:					
2	Miscellaneous Incoming Letter	129980-5023US01_MIS_COMM.pdf	100446 9760f915f2c4ea886cf28d5322cd55e00658b0fb	no	1
Warnings:					
Information:					
			Total Files Size (in bytes):	252390	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/695,020	11/25/2019	Jefferey C. Solomon	129980-5023-US01

CONFIRMATION NO. 7514

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

IMPROPER CFR REQUEST

OC000000114135597

Date Mailed: 01/23/2020

RESPONSE TO REQUEST FOR CORRECTED FILING RECEIPT

Power of Attorney, Claims, Fees, System Limitations, and Miscellaneous

In response to your request for a corrected Filing Receipt, the Office is unable to comply with your request because:

- The ADS submitted on 01/21/2020 was not properly marked up to show the desired changes. For information being changed relative to the information already of record, additions must be shown with underlining, and deletions must be shown with strike-through or brackets. See 37 CFR 1.76(c)(2)

In order to make changes to the information of record, an ADS must be properly signed and properly marked up relative to the current information of record.

Proper signature: The ADS must be signed with a handwritten signature or proper S-signature by:

- A patent practitioner, with the practitioner's registration number accompanying the signature (e.g., immediately below or adjacent to the signature), or
- The applicant, if the applicant is an individual other than the inventor(s) and no power of attorney has been appointed, or
- All of the inventors, if no other applicant has been established and no power of attorney has been appointed.

A proper S-signature consists of only letters and/or Arabic numerals, with appropriate spaces and commas, periods, apostrophes, or hyphens for punctuation contained between a first single forward slash mark before, and a second single forward slash mark after, the S-signature.

Proper markings: The ADS must identify the changes being made with underlining for insertions and strike-through or brackets for text removed. No other markings or indications are acceptable. Where an ADS providing corrected or updated information does not contain all of the sections of the ADS, the entire section in which changes are being made must be included in the ADS. Information of record can generally be found on the latest filing receipt.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/byemane/

Electronically filed February 18, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jefferey C. Solomon	Confirmation No.:	7514
Serial No.:	16/695,020	Art Unit:	2139
Filed:	November 25, 2019	Examiner:	TBD
For:	MEMORY MODULE WITH DATA BUFFERING	Attorney Docket No:	129980-5023-US01

RESPONSE TO THE NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

Mail Stop: MISSING PARTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Notice to File Missing Parts mailed December 16, 2019, enclosed please find:

- a Fee Transmittal Form setting forth the calculation for the statutory basic filing, search and examination fees, together with the surcharge for late submission of the statutory basic filing, search and examination fees due in this matter;
- a copy of the corrected ADS form submitted electronically on January 21, 2020, via EFS, in which the correction of a typographical error in the priority claim is properly marked up relative to the current information of record, and which is properly signed by the undersigned patent practitioner; and
- a copy of the Notice to File Missing Parts.

Applicant respectfully requests that an updated filing receipt be mailed to Applicant.

Petitioners
Ex. 1057, p. 119

February 16, 2020 was a Sunday and Monday February 17, 2020 was a Federal holiday, this response is filed on time on February 18, 2020 pursuant to 37 CFR § 1.7.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US01).

Respectfully submitted,

Date: February 18, 2020

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

UTILITY PATENT APPLICATION FEE TRANSMITTAL *(Only for new nonprovisional applications under 37 CFR § 1.53(b))*	Attorney Docket No.	129980-5023-US01
	First Inventor	Jefferey C. Solomon
	Title	MEMORY MODULE WITH DATA BUFFERING
	Electronically filed	February 18, 2020

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BASIC FILING, SEARCH AND EXAMINATION FEES

Application Type	Filing Fees	Search Fees	Examination Fees	Fees Paid ($)
Utility	$ 300	$ 660	$ 760	$ 1720

EXCESS CLAIM FEES

Type	No. Filed	Less	Extra	Extra Rate ($)	Fee ($)
Total Claims	15	- 20	0	$ 100 each	0
Independent	1	- 3	0	$ 460 each	0
			Surcharge for late filing fee		160

APPLICATION SIZE FEE (Specification and Drawings)

Total Sheets	Extra Sheets	No. of each add'l 50 or fraction thereof	Fee ($)
80 x .75- 100	0 / 50	0 (round up to whole no.) x $400	0

Sub Total	1880
Applicant qualifies for the 50% Reduction for Independent Inventor, Nonprofit Organization or Small Business Concern minus electronic filing discount of $75	
TOTAL FILING FEE	**1880**

Please charge the total filing fee and any other additional fees to Morgan, Lewis & Bockius LLP Deposit Account 50-0310 (order no. 129980-5023-US01).

Respectfully submitted,

Date: February 18, 2020

/ Jamie J. Zheng /

Jamie J. Zheng — 51,167 (Reg. No.)

MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

Electronically filed February 18, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jefferey C. Solomon	Confirmation No.:	7514
Serial No.:	16/695,020	Art Unit	2139
Filed:	November 25, 2019	Examiner:	To be assigned
For:	MEMORY MODULE WITH DATA BUFFERING	Attorney Docket No.:	129980-5023-US01

STATEMENT UNDER 37 C.F.R. § 3.73(c)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

NETLIST, INC., a corporation, states that it is the assignee of the entire right, title and interest in the patent application/patent identified above by virtue of an assignment from the inventor(s) of the parent of the patent application/patent identified above.

The assignment was recorded in the United States Patent and Trademark Office on July 17, 2006 at Reel 018104, Frame 0964, or for which a copy thereof is attached.

The undersigned is authorized to act on behalf of the assignee.

Date: February 18, 2020

/ Jamie J. Zheng / 51,167
Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

Petitioners
Ex. 1057, p. 122

Electronic Acknowledgement Receipt

EFS ID:	38357157
Application Number:	16695020
International Application Number:	
Confirmation Number:	7514
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023-US01
Receipt Date:	21-JAN-2020
Filing Date:	25-NOV-2019
Time Stamp:	18:03:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet to update/ correct info	CorrectedADS.pdf	151944 5fdce627e973871501994314e9632448ba0f29e3	no	10

Warnings:

Information:					
2	Miscellaneous Incoming Letter	129980-5023US01_MIS_COMM.pdf	100446 [redacted]	no	1
Warnings:					
Information:					
		Total Files Size (in bytes):	252390		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed January 21, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jefferey C. Solomon	Confirmation No.:	7514
Serial No.:	16/695,020	Art Unit:	2139
Filed:	November 25, 2019	Examiner:	TBD
For:	*MEMORY MODULE WITH DATA BUFFERING*	Attorney Docket No.:	129980-5023-US01

MISCELLANEOUS COMMUNICATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants concurrently submit with this Communication a Supplemental Application Data Sheet which has been updated to the extent:

Domestic Benefit/National Stage Information:

1. Correcting priority claim from 13/971,232 to **13/971,231**

No other information on the Application Data Sheet has been changed or added.

Applicants respectfully request an updated filing receipt be mailed to Applicant.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US01).

Respectfully submitted,

Date: January 21, 2020

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)

MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

Petitioners
Ex. 1057, p. 125

Document Description: Application Data Sheet to update/correct info
Doc Code: ADS.CORR

CORRECTED ADS FORM

Application Number	16695020
Title of Invention	MEMORY MODULE WITH DATA BUFFERING

Inventor Information

****If no data is shown, no data has been corrected****

	Data of Record	Updated Data
Order Number		
Name		
Residence Information		
Residency		
City		
State		
Country of Residence		
Mailing Address of Inventor		
Address 1		
Address 2		
City,State/Province, Postal Code		
Country		

Document Description: Application Data Sheet to update/correct info
Doc Code: ADS.CORR

Application Information

	Data of Record	Updated Data
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	
Attorney Docket Number	129980-5023-US01	
Entity Type	Regular Undiscounted	

Domestic Benefit/National Stage Information

****If no data is shown, no data has been corrected****

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121,365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S. C. 119(e) or 120, and 37 CFR 1.78(a).

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	16695020	
	Continuity Type	CON	
	Prior Application Number	15857519	
	Filing Date (YYYY-MM-DD)	2017-12-28	
	Patent Number	10489314	
	Issue Date (YYYY-MM-DD)	2019-11-26	

Document Description: Application Data Sheet to update/correct info
Doc Code: ADS.CORR

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	15857519	
	Continuity Type	CON	
	Prior Application Number	14715486	
	Filing Date (YYYY-MM-DD)	2015-05-18	
	Patent Number	9858215	
	Issue Date (YYYY-MM-DD)	2018-01-02	

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	11335875	
	Continuity Type	CIP	
	Prior Application Number	11173175	
	Filing Date (YYYY-MM-DD)	2005-07-01	
	Patent Number	7289386	
	Issue Date (YYYY-MM-DD)	2007-10-30	

		Data of Record	Updated Data
	Prior Application Status	pending	
	Application Number	11173175	
	Continuity Type	PRO	
	Prior Application Number	60588244	
	Filing Date (YYYY-MM-DD)	2004-07-15	
	Patent Number		
	Issue Date (YYYY-MM-DD)	0001-01-01	

Corrected ADS 1.0

Document Description: Application Data Sheet to update/correct info
Doc Code: ADS.CORR

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	11173175	
	Continuity Type	CIP	
	Prior Application Number	11075395	
	Filing Date (YYYY-MM-DD)	2005-03-07	
	Patent Number	7286436	
	Issue Date (YYYY-MM-DD)	2007-10-23	

		Data of Record	Updated Data
	Prior Application Status	pending	
	Application Number	11075395	
	Continuity Type	PRO	
	Prior Application Number	60550668	
	Filing Date (YYYY-MM-DD)	2004-03-05	
	Patent Number		
	Issue Date (YYYY-MM-DD)	0001-01-01	

		Data of Record	Updated Data
	Prior Application Status	pending	
	Application Number	11075395	
	Continuity Type	PRO	
	Prior Application Number	60575595	
	Filing Date (YYYY-MM-DD)	2004-05-28	
	Patent Number		
	Issue Date (YYYY-MM-DD)	0001-01-01	

Corrected ADS 1.0

Document Description: Application Data Sheet to update/correct info
Doc Code: ADS.CORR

	Data of Record	Updated Data
Prior Application Status	pending	
Application Number	11075395	
Continuity Type	PRO	
Prior Application Number	60590038	
Filing Date (YYYY-MM-DD)	2004-07-21	
Patent Number		
Issue Date (YYYY-MM-DD)	0001-01-01	

	Data of Record	Updated Data
Prior Application Status	abandoned	
Application Number	14715486	
Continuity Type	CON	
Prior Application Number	~~13971232~~	13971231
Filing Date (YYYY-MM-DD)	2013-08-20	
Patent Number		
Issue Date (YYYY-MM-DD)	0001-01-01	

	Data of Record	Updated Data
Prior Application Status	patented	
Application Number	~~13971232~~	13971231
Continuity Type	CON	
Prior Application Number	13287081	
Filing Date (YYYY-MM-DD)	2011-11-01	
Patent Number	8516188	
Issue Date (YYYY-MM-DD)	2013-08-20	

Corrected ADS 1.0

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	13287081	
	Continuity Type	CON	
	Prior Application Number	13032470	
	Filing Date (YYYY-MM-DD)	2011-02-22	
	Patent Number	8081536	
	Issue Date (YYYY-MM-DD)	2011-12-20	

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	13032470	
	Continuity Type	CON	
	Prior Application Number	12955711	
	Filing Date (YYYY-MM-DD)	2010-11-29	
	Patent Number	7916574	
	Issue Date (YYYY-MM-DD)	2011-03-29	

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	12955711	
	Continuity Type	CON	
	Prior Application Number	12629827	
	Filing Date (YYYY-MM-DD)	2009-12-02	
	Patent Number	7881150	
	Issue Date (YYYY-MM-DD)	2011-02-01	

Document Description: Application Data Sheet to update/correct info
Doc Code: ADS.CORR

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	12629827	
	Continuity Type	CON	
	Prior Application Number	12408652	
	Filing Date (YYYY-MM-DD)	2009-03-20	
	Patent Number	7636274	
	Issue Date (YYYY-MM-DD)	2009-12-22	

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	12408652	
	Continuity Type	CON	
	Prior Application Number	11335875	
	Filing Date (YYYY-MM-DD)	2006-01-19	
	Patent Number	7532537	
	Issue Date (YYYY-MM-DD)	2009-05-12	

		Data of Record	Updated Data
	Prior Application Status	pending	
	Application Number	11335875	
	Continuity Type	PRO	
	Prior Application Number	60645087	
	Filing Date (YYYY-MM-DD)	2005-01-19	
	Patent Number		
	Issue Date (YYYY-MM-DD)	0001-01-01	

Corrected ADS 1.0

Document Description: Application Data Sheet to update/correct info
Doc Code: ADS.CORR

Foreign Priority Information

****If no data is shown, no data has been corrected****

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

		Data of Record	Updated Data
	Application Number		
	Country		
	Filing Date		
	Access Code		

Applicant Information

****If no data is shown, no data has been corrected****
Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

	Data of Record	Updated Data
Applicant Type		
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is		
Name of the Deceased or Legally Incapacitated Inventor		
Applicant is an Organization		
Name		
Organization Name		
Address 1		

Corrected ADS 1.0

Address 2		
City,State/Province,Postal Code		
Country		
Phone Number		
Fax Number		
Email Address		

Assignee Information including Non-Applicant Assignee Information

****If no data is shown, no data has been corrected****
Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office

	Data of Record	Updated Data
Order		
Applicant is an Organization		
Name		
Organization Name		

Mailing Address

Address 1		
Address 2		
City,State/Province,Postal Code		
Country		
Phone Number		
Fax Number		

Email Address		

Signature

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b).

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/ Jamie J. Zheng /	Registration Number	51167
First Name	Jamie J.	Last Name	Zheng

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/695,020	11/25/2019	Jefferey C. Solomon	129980-5023-US01

CONFIRMATION NO. 7514

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

FORMALITIES LETTER

OC000000113922580

Date Mailed: 12/16/2019

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $(0) previous unapplied payment amount.
- $ **1880** TOTAL FEE BALANCE DUE.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/afessehaye/

Modified PTO/AIA/82B (07-12)

GENERAL POWER OF ATTORNEY BY APPLICANT FOR UNITED STATES PATENT

I hereby revoke all previous powers of attorney given in the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

I hereby appoint the practitioner associated with the following Customer Number

:

79141

as my/our attorney or agent, and to transact all business in the United States Patent and Trademark Office in connection with the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

Please recognize or change the **correspondence address** for the application referenced in the attached transmittal letter to the address associated with the above-mentioned **Customer Number**.

I am the Applicant:

☐ Inventor or Joint Inventor

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor

■ Assignee or Person to Whom the Inventor is Under an Obligation to Assign

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is currently being filed in this document)

SIGNATURE of Applicant for Patent

Signature		Date: January 9, 2013
Name	**Gail Sasaki**	
Title	Vice President and Chief Financial Officer	
Company	Netlist, Inc.	

Note: Signature - this form must be signed by the Applicant or a person authorized to act on behalf of Applicant.

Submit multiple forms for more than one signature
Total of ___ forms are submitted.

Electronic Patent Application Fee Transmittal

Application Number:	16695020
Filing Date:	25-Nov-2019
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Filer:	Jamie Jie Zheng/S. Olivier
Attorney Docket Number:	129980-5023-US01

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	160	160
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1880**

Electronic Acknowledgement Receipt	
EFS ID:	38620957
Application Number:	16695020
International Application Number:	
Confirmation Number:	7514
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023-US01
Receipt Date:	18-FEB-2020
Filing Date:	25-NOV-2019
Time Stamp:	18:54:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1880
RAM confirmation Number	E20202HI55101891
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5023US01_Response_FEE.pdf	898389 317aafa50f6ca3eb1694574584349bc0a9d8eb50	yes	20

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Applicant Response to Pre-Exam Formalities Notice	1	2
	Fee Worksheet (SB06)	3	3
	Miscellaneous Incoming Letter	4	18
	Assignee showing of ownership per 37 CFR 3.73	19	19
	Power of Attorney	20	20

Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	37171 88ef27f7ac522d1ea5d73e6eb127541aba906dfb	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	935560		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/695,020	11/25/2019	Jefferey C. Solomon	129980-5023-US01

CONFIRMATION NO. 7514

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

POA ACCEPTANCE LETTER

OC000000114842617

Date Mailed: 02/21/2020

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/18/2020.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/mteklemichael/

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/695,020	11/25/2019	2139	1880	129980-5023-US01	15	1

CONFIRMATION NO. 7514

UPDATED FILING RECEIPT

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

OC000000114842605

Date Mailed: 02/21/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Jefferey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: The patent practitioners associated with Customer Number 79141

Domestic Priority data as claimed by applicant

This application is a CON of 15/857,519 12/28/2017 PAT 10489314
which is a CON of 14/715,486 05/18/2015 PAT 9858215
which is a CON of 13/971,232 08/20/2013 ABN
which is a CON of 13/287,081 11/01/2011 PAT 8516188
which is a CON of 13/032,470 02/22/2011 PAT 8081536
which is a CON of 12/955,711 11/29/2010 PAT 7916574
which is a CON of 12/629,827 12/02/2009 PAT 7881150
which is a CON of 12/408,652 03/20/2009 PAT 7636274
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7289386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7286436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004

and claims benefit of 60/590,038 07/21/2004

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 12/13/2019
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/695,020**
Projected Publication Date: 05/28/2020
Non-Publication Request: No
Early Publication Request: No
Title

MEMORY MODULE WITH DATA BUFFERING

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/695,020	11/25/2019	2139	1880	129980-5023-US01	15	1

CONFIRMATION NO. 7514

CORRECTED FILING RECEIPT

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304



Date Mailed: 02/25/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Jefferey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: The patent practitioners associated with Customer Number 79141

Domestic Priority data as claimed by applicant

This application is a CON of 15/857,519 12/28/2017 PAT 10489314
which is a CON of 14/715,486 05/18/2015 PAT 9858215
which is a CON of 13/971,232 08/20/2013 ABN
which is a CON of 13/287,081 11/01/2011 PAT 8516188
which is a CON of 13/032,470 02/22/2011 PAT 8081536
which is a CON of 12/955,711 11/29/2010 PAT 7916574
which is a CON of 12/629,827 12/02/2009 PAT 7881150
which is a CON of 12/408,652 03/20/2009 PAT 7636274
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7289386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7286436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004

and claims benefit of 60/590,038 07/21/2004
and said 14/715,486 05/18/2015
is a CON of 13/971,231 08/20/2013 PAT 9037774
which is a CON of 13/287,081 11/01/2011 PAT 8516188
which is a CON of 13/032,470 02/22/2011 PAT 8081536
which is a CON of 12/955,711 11/29/2010 PAT 7916574
which is a CON of 12/629,827 12/02/2009 PAT 7881150
which is a CON of 12/408,652 03/20/2009 PAT 7636274
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which claims benefit of 60/645,087 01/19/2005

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 12/13/2019

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/695,020**

Projected Publication Date: 06/04/2020

Non-Publication Request: No

Early Publication Request: No

Title

MEMORY MODULE WITH DATA BUFFERING

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

Electronically filed March 9, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jefferey C. Solomon	Confirmation No.:	7514
Serial No.:	16/695,020	Art Unit:	2133
Filed:	November 25, 2019	Examiner:	Ruiz, Jared Ian
For:	*MEMORY MODULE WITH DATA BUFFERING*	Attorney Docket No.:	129980-5023-US01

MISCELLANEOUS COMMUNICATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants concurrently submit with this Communication a Corrected Application Data Sheet which has been updated to the extent:

Domestic Benefit/National Stage Information:

1. Correcting priority claim from 13/971,232 to **13/971,231**

No other information on the Application Data Sheet has been changed or added.

Applicants respectfully request an updated filing receipt be mailed to Applicant.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US01).

Respectfully submitted,

Date: March 9, 2020

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

Petitioners
Ex. 1057, p. 153

PTO/AIA/14 (02-18)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5023-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jefferey	C.	Solomon	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Irvine	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	16 Silver Fir		
Address 2			
City	Irvine	State/Province	CA
Postal Code	92604	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jayesh	R.	Bhakta	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Cerritos	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	12220 Rose Street		
Address 2			
City	Cerritos	State/Province	CA
Postal Code	90703	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

PTO/AIA/14 (02-18)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5023-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

☐ An Address is being provided for the correspondence Information of this application.			
Customer Number	79141		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	MEMORY MODULE WITH DATA BUFFERING		
Attorney Docket Number	129980-5023-US01	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	23	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	79141		

PTO/AIA/14 (02-18)
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5023-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	15/857519	2017-12-28

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/857519	Continuation of	14/715486	2015-05-18	9858215	2018-01-02

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14/715486	Continuation of	~~13/971232~~ 13/971231	2013-08-20	9037774	2019-05-19

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/9712~~3~~21	Continuation of	13/287081	2011-11-01	8516188	2013-08-20

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/287081	Continuation of	13/032470	2011-02-22	8081536	2011-12-20

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/032470	Continuation of	12/955711	2010-11-29	7916574	2011-03-29

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/955711	Continuation of	12/629827	2009-12-02	7881150	2011-02-01

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/629827	Continuation of	12/408652	2009-03-20	7636274	2009-12-22

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/408652	Continuation of	11/335875	2006-01-19	7532537	2009-05-12

PTO/AIA/14 (02-18)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5023-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/335875	Claims benefit of provisional	60/645087	2005-01-19

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11/335875	Continuation in part of	11/173175	2005-07-01	7289386	2007-10-30

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/173175	Claims benefit of provisional	60/588244	2004-07-15

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11/173175	Continuation in part of	11/075395	2005-03-07	7286436	2007-10-23

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/075395	Claims benefit of provisional	60/550668	2004-03-05

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/075395	Claims benefit of provisional	60/575595	2004-05-28

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11/075395	Claims benefit of provisional	60/590038	2004-07-21

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

PTO/AIA/14 (02-18)
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5023-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5023-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5023-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Netlist, Inc.		
Mailing Address Information For Applicant:			
Address 1	175 Technology		
Address 2	Suite 150		
City	Irvine	**State/Province**	CA
Country	US	Postal Code	92618
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Approved for use through 11/30/2020. OMB 0651-0032
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5023-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/ Jamie J. Zheng /			Date (YYYY-MM-DD)	March 9, 2020
First Name	Jamie J.	Last Name	Zheng	Registration Number	51167

Additional Signature may be generated within this form by selecting the Add button.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5023-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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Electronic Acknowledgement Receipt

EFS ID:	38813747
Application Number:	16695020
International Application Number:	
Confirmation Number:	7514
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023-US01
Receipt Date:	09-MAR-2020
Filing Date:	25-NOV-2019
Time Stamp:	20:16:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5024US01_MIS_COMM_COR_ADS.pdf	852860 4581db1144f991020fce1070330d164cdf2ede89	yes	11

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Application Data Sheet	2	11
Warnings:			
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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/695,020	11/25/2019	2133	1880	129980-5023-US01	15	1

CONFIRMATION NO. 7514

CORRECTED FILING RECEIPT

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

OC000000115387635

Date Mailed: 03/12/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

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Inventor(s)

Jefferey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: The patent practitioners associated with Customer Number 79141

Domestic Priority data as claimed by applicant

This application is a CON of 15/857,519 12/28/2017 PAT 10489314
which is a CON of 14/715,486 05/18/2015 PAT 9858215
which is a CON of 13/971,231 08/20/2013 PAT 9037774
which is a CON of 13/287,081 11/01/2011 PAT 8516188
which is a CON of 13/032,470 02/22/2011 PAT 8081536
which is a CON of 12/955,711 11/29/2010 PAT 7916574
which is a CON of 12/629,827 12/02/2009 PAT 7881150
which is a CON of 12/408,652 03/20/2009 PAT 7636274
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7289386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7286436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004

and claims benefit of 60/590,038 07/21/2004

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 12/13/2019
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/695,020**
Projected Publication Date: 06/18/2020
Non-Publication Request: No
Early Publication Request: No
Title

MEMORY MODULE WITH DATA BUFFERING

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/695,020	11/25/2019	Jefferey C. Solomon	129980-5023-US01

CONFIRMATION NO. 7514

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Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
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PUBLICATION NOTICE

OC000000117855631

Title:MEMORY MODULE WITH DATA BUFFERING

Publication No.US-2020-0192834-A1
Publication Date:06/18/2020

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				***Electronically filed January 8, 2021***	
				Application Number	***16/695,020***
				Filing Date	***November 25, 2019***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***TBD***
Sheet	1	of	47	Attorney Docket Number	***129980-5023-US01***

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.[1]	Document Number Number - Kind Code[2]	Publication Date YYYY-MM-DD	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	4,218,740	1980-08-19	MOTOROLA INC	
	2.	4,249,253	1981-02-03	Gentili et al.	
	3.	4,368,515	1983-01-11	Nielsen	
	4.	4,392,212	1983-07-05	Miyasaka et al.	
	5.	4,571,676	1986-02-18	Mantellina et al.	
	6.	4,592,011	1986-05-27	Mantellina et al.	
	7.	4,633,429	1986-12-30	Lewandowski et al.	
	8.	4,670,748	1987-06-02	Williams	
	9.	4,706,214	1987-11-10	Mitsubishi Denki Kabushiki Kaisha	
	10.	4,739,473	1988-04-19	Ng	
	11.	4,866,603	1989-09-02	Chiba	
	12.	4,958,322	1990-09-18	Kosugi et al.	
	13.	4,961,172	1990-10-02	Shubat et al.	
	14.	4,961,204	1990-10-02	Hitachi Ltd	
	15.	4,980,850	1990-12-25	Morgan	
	16.	5,060,188	1991-10-22	Zulian et al.	
	17.	5,247,643	1993-09-21	Shottan	
	18.	5,272,664	1993-12-21	Silicon Graphics Inc	
	19.	5,313,624	1994-05-17	Harriman	
	20.	5,345,412	1994-09-06	Shiratsuchi	
	21.	5,357,478	1994-10-18	Kikuda et al	
	22.	5,388,072	1995-02-07	IBM	
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	25.	5,426,753	1995-06-20	Moon	
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	29.	5,495,435	1996-02-27	Sugahara	
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Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 8, 2021*	
				Application Number	***16/695,020***
				Filing Date	***November 25, 2019***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***TBD***
Sheet	2	of	47	Attorney Docket Number	***129980-5023-US01***

	31.	5,532,954	1996-07-02	Bechtolsheim et al.	
	32.	5,537,584	1996-07-16	Miyai et al.	
	33.	5,541,448	1996-07-30	Carpenter	
	34.	5,559,970	1996-09-24	Sharma	
	35.	5,572,691	1996-11-05	Koudmani	
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	39.	5,617,559	1997-04-01	Le et al.	
	40.	5,630,096	1997-05-13	Zuravleff	
	41.	5,638,534	1997-06-10	Samsung Electronics Co Ltd	
	42.	5,649,159	1997-07-15	Le et al.	
	43.	5,655,153	1997-08-05	EMC CORP	
	44.	5,699,542	1997-12-16	Mehta et al.	
	45.	5,702,984	1997-12-30	Bertin et al.	
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	47.	5,717,851	1998-02-10	Yishay et al.	
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	49.	5,729,716	1998-05-17	Lee et al.	
	50.	5,745,914	1998-04-28	Connolly et al.	
	51.	5,764,590	1998-06-09	Mitsubishi Electric Corp	
	52.	5,784,705	1998-07-21	Leung, Wingyu	
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Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 8, 2021*	
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				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***TBD***
Sheet	3	of	47	Attorney Docket Number	***129980-5023-US01***

	64.	5,959,930	1999-09-28	Sakurai	
	65.	5,963,464	1999-10-05	Dell et al.	
	66.	5,966,736	1999-10-12	Gittinger et al.	
	67.	5,973,392	1999-10-26	Senba et al.	
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	69.	6,011,710	2000-01-04	Wiggers	
	70.	6,018,787	2000-01-25	Ip	
	71.	6,044,032	2000-03-28	Li	
	72.	6,061,754	2000-05-09	Cepulis	
	73.	6,070,217	2000-05-30	Connolly et al.	
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	75.	6,097,652	2000-08-01	Roh	
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	81.	6,154,418	2000-11-28	Li	
	82.	6,154,419	2000-11-28	Shakkarwar	
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	95.	6,317,352	2001-11-13	Halbert et al.	
	96.	6,349,051	2002-02-19	Micron Technology Inc	
	97.	6,381,140	2002-04-30	Liao, Sheng-Chi	

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 8, 2021*	
				Application Number	***16/695,020***
				Filing Date	***November 25, 2019***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***TBD***
Sheet	4	of	47	Attorney Docket Number	***129980-5023-US01***

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	99.	6,408,356	2002-06-18	Dell	
	100.	6,414,868	2002-07-02	Wong et al.	
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	113.	6,530,007	2003-03-04	Olarig et al.	
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	344.	Inter Partes Review Case No. IPR2014-00883, Corrected Petition for Inter Partes Review of U.S. Patent No. 8,081,536, filed on July 8, 2014.
	345.	Inter Partes Review of U.S. Patent No. 8,081,536, Case No. IPR2014-00883, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014
	346.	Inter Partes Review of U.S. Patent No. 8,081,536, Case No. IPR2014-00883, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014
	347.	Inter Partes Review Case No. IPR2014-00883, Patent Owner Response, filed May 8, 2015
	348.	Inter Partes Review Case No. IPR2014-00883, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
	349.	Inter Partes Review Case No. IPR2014-00883, Exhibit 1025, 'Professor Carl Sechen Deposition Transcript,' filed June 19, 2015
	350.	Inter Partes Review Case No. IPR2014-00883, Exhibit 1026, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19, 2015
	351.	Inter Partes Review Case No. IPR2014-00883, Petitioner's Request for Oral Argument, filed July 1, 2015

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	352.	Inter Partes Review Case No. IPR2014-00883, Patent Owner's Request for Oral Hearing, filed July 3, 2015
	353.	Inter Partes Review Case No. IPR2014-00883, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015
	354.	Inter Partes Review Case No. IPR2014-00883, Record of Oral Hearing, filed November 16, 2015
	355.	Inter Partes Review Case No. IPR2014-00883, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015
	356.	Inter Partes Review Case No. IPR2014-00883, Netlist Inc.'s Notice of Appeal, filed February 10, 2016
	357.	Inter Partes Review Case No. IPR2014-01011, Exhibit 1007 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan." filed on June 22, 2014.
	358.	Inter Partes Review Case No. IPR2014-01011, Corrected Petition for Inter Partes Review of U.S. Patent No. 7,881,150, filed on July 8, 2014.
	359.	Inter Partes Review of U.S. Patent No. 7,881,150, Case No. IPR2014-01011, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014
	360.	Inter Partes Review of U.S. Patent No. 7,881,150, Case No. IPR2014-01011, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014
	361.	Inter Partes Review of U.S. Patent No. 7,881,150, Case No. IPR2014-01011, Exhibit 3001 to Decision – Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued December 16, 2014
	362.	Inter Partes Review of U.S. Patent No. 7,881,150, Case No. IPR2014-01011, Exhibit 3002 to Decision – Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued December 16, 2014
	363.	Inter Partes Review of U.S. Patent No. 7,881,150, Case No. IPR2014-01011, Exhibit 3003 to Decision – Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued December 16, 2014
	364.	Inter Partes Review of U.S. Patent No. 7,881,150, Case No. IPR2014-01011, Exhibit 3004 to Decision – Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued December 16, 2014
	365.	Inter Partes Review Case No. IPR2014-01011, Patent Owner Response, filed May 8, 2015
	366.	Inter Partes Review Case No. IPR2014-01011, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
	367.	Inter Partes Review Case No. IPR2014-01011, Exhibit 1027, 'Professor Carl Sechen Deposition Transcript,' filed June 19, 2015

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	368.	Inter Partes Review Case No. IPR2014-01011, Exhibit 1028, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19, 2015
	369.	Inter Partes Review Case No. IPR2014-01011, Petitioner's Request for Oral Argument, filed July 1, 2015
	370.	Inter Partes Review Case No. IPR2014-01011, Patent Owner's Request for Oral Hearing, filed July 3, 2015
	371.	Inter Partes Review Case No. IPR2014-01011, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015
	372.	Inter Partes Review Case No. IPR2014-01011, Record of Oral Hearing, filed November 16, 2015
	373.	Inter Partes Review Case No. IPR2014-01011, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015
	374.	Inter Partes Review Case No. IPR2014-01011, Netlist Inc.'s Notice of Appeal, filed February 10, 2016
	375.	Inter Partes Review Case No. IPR2014-01020, Exhibit 1002 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on April 7, 2015.
	376.	Inter Partes Review Case No. IPR2014-01020, Exhibit 1023 to Petition for Inter Partes Review, curriculum vitae of Dr. Srinivasan Jagannathan, filed on April 7, 2015.
	377.	Inter Partes Review Case No. IPR2014-01020, Exhibit 1025 to Petition for Inter Partes Review, "operational," The Pocket Oxford American Dictionary of Current English, Oxford University Press, 2002, filed on April 7, 2015.
	378.	Inter Partes Review Case No. IPR2014-01020, Decision to Institute Inter Partes Review of D U.S. Patent No. 7,881,150, dated October 8, 2015.
	379.	Inter Partes Review Case No. IPR2014-01021, Exhibit 1026 to Petition for Inter Partes Review, curriculum vitae of Dr. Srinivasan Jagannathan, filed on April 7, 2015.
	380.	Inter Partes Review Case No. IPR2014-01021, Corrected Exhibit 1002 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on April 22, 2015.
	381.	Inter Partes Review Case No. IPR2014-01021, Decision to Institute Inter Partes Review of U.S. Patent No. 8,081,536, dated October 8, 2015
	382.	Petition for Inter Partes Review filed on 6/24/2014 for U.S. Patent No. 8,516,185, Case No. IPR2014-01029, and all associated documents including cited references and expert declarations, available at https://ptabtrials.uspto.gov
	383.	Inter Partes Review Case No. IPR2014-01029, Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on June 24, 2014.

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	384.	Inter Partes Review Case No. IPR2014-01029, Exhibit 1008 to Petition for Inter Partes Review, "Declaration of Charles J. Neuhauser, Ph.D. under 37 C.F.R. § 1.68," filed on June 24, 2014.
	385.	Inter Partes Review Case No. IPR2014-01029, Supplemental Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on July 23, 2014.
	386.	Inter Partes Review Case No. IPR2014-01029, Patent Owner's Preliminary Response pursuant to 37 C.F.R. § 42.107, filed on October 17, 2014.
	387.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014.
	388.	Inter Partes Review Case No. IPR2014-01029, Petitioner's Request for Rehearing pursuant to 37 C.F.R. § 42.71, filed on January 15, 2015.
	389.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Request for Rehearing, Issued on March 3, 2015.
	390.	Inter Partes Review Case No. IPR2014-01369, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued March 9, 2014.
	391.	Inter Partes Review Case No. IPR2014-01369, Corrected Petition for Inter Partes Review of Claims 1-19 of U.S. Patent No. 8,516,185, filed on September 22, 2014.
	392.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1008 to Corrected Petition for Inter Partes Review, "Declaration of Dr. Nader Bagherzadeh under 37 C.F.R. § 1.68," filed on September 22, 2014.
	393.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1013 to Corrected Petition for Inter Partes Review, "Webster's II New College Dictionary," filed on September 22, 2014.
	394.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1014 to Corrected Petition for Inter Partes Review, "Standard Dictionary of Electrical and Electronics Terms," IEEE 1988, filed on September 22, 2014.
	395.	Inter Partes Review Case No. IPR2015-0 021, Petition for Inter Partes Review of U.S. Patent No. 8,081,536, filed on April 7, 2015
	396.	Inter Partes Review Case No. IPR2015-01020, Petition for Inter Partes Review of U.S. Patent No. 7,881,150, filed on April 7, 2015.
	397.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Related Matters, filed April 28, 2015
	398.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner Response to Petition, filed February 22, 2016
	399.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016

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	400.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2002, "Videotaped Deposition of Srinivasan Jagannathan, Ph.D on February 12, 2016," filed February 22, 2016
	401.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2003, "Videotaped Deposition of Srinivasan Jagannathan, Ph.D on April 20, 2015," filed February 22, 2016
	402.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Objections to Evidence, filed February 29, 2016
	403.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Reply, filed May 19, 2016
	404.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016
	405.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, May 10, 2016 Deposition of Carl Sechen, filed May 19, 2016
	406.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner Request for Oral Argument, filed June 2, 2016
	407.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER MOTION FOR OBSERVATIONS, filed June 2, 2016
	408.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016
	409.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2007, "Deposition of Dr. Srinivasan Jagannathan on May 25, 2016," filed June 2, 2016
	410.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, ORDER Trial Hearing, filed June 8, 2016
	411.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016
	412.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Response to Motion for Observations, filed June 10, 2016
	413.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Response to Netlist's Submission, filed June 13, 2016
	414.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's Objections to Petitioner's Demonstrative Exhibits, filed June 23, 2016
	415.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's Demonstrative Exhibits, filed June 24, 2016

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	416.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Updated Exhibit List, filed June 24, 2016
	417.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Demonstrative Exhibits, filed June 24, 2016
	418.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Record of Oral Hearing, dated July 26, 2016
	419.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Final Written Decision, issued September 28, 2016
	420.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3001 to Final Decision, issued September 28, 2016
	421.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3001-2 to Final Decision, issued September 28, 2016
	422.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3002 to Final Decision, issued September 28, 2016
	423.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3003 to Final Decision, issued September 28, 2016
	424.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3004 to Final Decision, issued September 28, 2016
	425.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner Response to Petition, filed February 22, 2016
	426.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016
	427.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Objections to Evidence, filed February 29, 2016
	428.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Reply, filed May 19, 2016
	429.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016
	430.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner Request for Oral Argument, filed June 2, 2016
	431.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, PATENT OWNER MOTION FOR OBSERVATIONS, filed June 2, 2016
	432.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016

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	433.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner's SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016
	434.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Response to Motion for Observations, filed June 10, 2016
	435.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Response to Patent Owner's Submission, filed June 13, 2016
	436.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner's Objections to Petitioner's Demonstrative Exhibits, filed June 23, 2016
	437.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner's Demonstrative Exhibits, filed June 24, 2016
	438.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Updated Exhibit List, filed June 24, 2016
	439.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Final Decision, issued September 28, 2016
	440.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Petition for Inter Partes Review, filed December 30, 2016
	441.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Exhibit 1003, "Declaration of Harold S. Stone," filed December 30, 2016
	442.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Exhibit 1008, Declaration of John J. Kelly Regarding Records of Joint Electron Device Engineering Council (JEDEC), filed December 30, 2016
	443.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, DECISION Institution of Inter Partes Review, filed May 15, 2017.
	444.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, Exhibit 2001 (DECLARATION OF PROFESSOR CARL SECHEN), filed September 15, 2017.
	445.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, Patent Owner's Response, filed September 15, 2017.
	446.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, PETITIONERS' OBJECTIONS TO EVIDENCE, filed September 15, 2017.
	447.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Deposition Transcript of Carl Sechen, filed December 15, 2017.
	448.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's reply to Patent Owner's Response, filed December 15, 2017.

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	449.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Supplemental Declaration of Harold S. Stone, filed December 15, 2017.
	450.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Xilinx Xilinx CS280 package datasheet (1999), filed December 15, 2017.
	451.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBIT 2004, filed January 9, 2017.
	452.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Motion for Observations, filed January 9, 2017.
	453.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed January 9, 2017.
	454.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBIT 2003, 'Synchronous DRAM Architectures, Organization, and Alternative Technologies,' filed January 18, 2017.
	455.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Response to Patent Owners Motion for Observations, filed January 23, 2018.
	456.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Opposition to Petitioner's Motion to Exclude, filed January 23, 2018.
	457.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Reply in Support of Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed January 30, 2018.
	458.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Demonstratives, filed February 9, 2018.
	459.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBIT 2005, filed February 9, 2018.
	460.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Updated Exhibit List, filed February 9, 2018.
	461.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Updated Exhibit List, filed February 9, 2018.
	462.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Final Written Decision, filed February 14, 2018.
	463.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Hearing Transcript, filed February 14, 2018.
	464.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Supplemental Mandatory Notices, filed April 19, 2018.

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	465.	Inter Partes Review of U.S. Patent No. 8516185, Case No. IPR2017-00577, Petition for Inter Partes Review, filed January 5, 2017
	466.	Inter Partes Review of U.S. Patent No. 8516185, Case No. IPR2017-00577, Exhibit 1003, "Declaration of Harold S. Stone," filed January 5, 2017
	467.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, DECISION Institution of Inter Partes Review, filed July 7, 2017.
	468.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, SCHEDULING ORDER, filed July 7, 2017.
	469.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2003 (DECLARATION OF R. JACOB BAKER, PH.D., P.E.), filed October 25, 2017.
	470.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2004 (Deposition of HAROLD S. STONE, PH.D.), filed October 25, 2017.
	471.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2005 (Memory Systems: Cache, DRAM, Disk), filed October 25, 2017.
	472.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2006 (PC2100 and PC1600 DDR SDRAM Registered DIMM, Design Specification, Revision 1.3, January 2002), filed October 25, 2017.
	473.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2007 (DRAM CIRCUIT DESIGN: Fundamental and High-Speed Topics), filed October 25, 2017.
	474.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, PATENT OWNER'S RESPONSE, filed October 25, 2017.
	475.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, PETITIONERS' OBJECTIONS TO EVIDENCE, filed October 31, 2017.
	476.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing 4:1 MUX/DeMUX and 4 ranks of memory (corrected Ex. 1035), filed February 6, 2018.
	477.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing 4:1 MUX/DeMUX and 4 ranks of memory, filed February 6, 2018.
	478.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing Fast components and Slow components, filed February 6, 2018.
	479.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Deposition Transcript of R. Jacob Baker (Jan. 12, 2018.), filed February 6, 2018.

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	480.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Excerpts from Brent Keeth and R. Jacob Baker, DRAM Circuit Design: A Tutorial (IEEE Press 2001), filed February 6, 2018.
	481.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Oral Testimony of R. Jacob Baker in Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (May 11, 2017), filed February 6, 2018.
	482.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioners' Reply to Patent Owner's Response, filed February 6, 2018.
	483.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Objections to Evidence, filed February 13, 2018.
	484.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Motion to Exclude, filed February 28, 2018.
	485.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Request for Oral Argument, filed February 28, 2018.
	486.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioner's Opposition to Patent Owner's Motion to Exclude, filed March 14, 2018.
	487.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Reply to Opposition to Motion to Exclude, filed March 21, 2018.
	488.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Hearing Transcript, filed April 6, 2018.
	489.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Termination Decision Document, filed July 7, 2018.
	490.	Inter Partes Review of U.S. Patent No. 7,532,537, Case No. IPR2017-00667, DECISION Institution of Inter Partes Review, filed July 21, 2017.
	491.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Objections to Evidence, filed November 14, 2017.
	492.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Supplemental Objections to Evidence, filed November 14, 2017.
	493.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Deposition of Carl Sechen, Ph.D. taken December 8, 2017, filed February 26, 2018.
	494.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Deposition of Carl Sechen, Ph.D. taken February 8, 2018., filed February 26, 2018.
	495.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Google, Inc. et al. v. Netlist, Inc., Appeal 2014-00777, filed February 26, 2018.

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	496.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Reply to Patent Owner's Response, filed February 26, 2018.
	497.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Objections to Evidence, filed March 5, 2018.
	498.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Exhibit 2007, Deposition of Harold S. Stone, filed March 19, 2018.
	499.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Motion for Observations, filed March 19, 2018.
	500.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Request for Oral Argument, filed March 19, 2018.
	501.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Motion to Exclude, filed March 19, 2018.
	502.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Submission on Propriety of Petitioners Reply, filed March 20, 2018.
	503.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Response to Patent Owner's Submission on Propriety of Petitioner's Reply and Supplemental Stone Declaration 1, filed March 27, 2018.
	504.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Reply in Support of its Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed April 2, 2018.
	505.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Updated Mandatory Notices, filed April 2, 2018.
	506.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Response to Patent Owner's Motion for Observations, filed April 2, 2018.
	507.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Objection to Petitioner's Demonstratives, filed April 20, 2018.
	508.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Hearing Transcript, filed April 24, 2018.
	509.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Final Written Decision, filed July 18, 2018.
	510.	Inter Partes Review of U.S. Patent No. 7,532,537, Case No. IPR2017-00668, DECISION Institution of Inter Partes Review, filed July 21, 2017.
	511.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Objections to Evidence, filed November 14, 2017.
	512.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Notice of Deposition of Carl Sechen, filed January 30, 2018.

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	513.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Supplemental Objections to Evidence, filed February 15, 2018.
	514.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Reply to Patent Owner's Response, filed February 26, 2018.
	515.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Objections to Evidence, filed March 5, 2018.
	516.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Motion for Observations, filed March 19, 2018.
	517.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Request for Oral Argument, filed March 19, 2018.
	518.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Submission on Propriety of Petitioner's Reply, filed March 20, 2018.
	519.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Response to Patent Owner's Submission on Propriety of Petitioner's Reply and Supplemental Stone Declaration, filed March 27, 2018.
	520.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Opposition to Petitioner's Motion to Exclude, filed April 2, 2018.
	521.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Response to Patent Owner's Motion for Observations, filed April 2, 2018.
	522.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Reply in Support of its Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed April 9, 2018.
	523.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Objections to Petitioner's Demonstratives, filed April 20, 2018.
	524.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Hearing Transcript, filed April 24, 2018.
	525.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Final Written Decision, filed July 18, 2018.
	526.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017.-00549, Xilinx CoolRunner XPLA3 CPLD product specification (2000), filed December 15, 2017.
	527.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017.-00549, Xilinx Programmable Logic Design Quick Start Handbook (2004), filed December 15, 2017.
	528.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017.-00549, Xilinx Xilinx TQFP package datasheet (2000), filed December 15, 2017.
	529.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017.-00549, Xilinx Xilinx VQFP package datasheet (2002), filed December 15, 2017.

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	530.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1022, Decision Denying Institution of Inter Partes Review, filed December 16, 2014
	531.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1023, Decision Denying Institution of Inter Partes Review, filed March 9, 2015
	532.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1024, Excepts from the Hearing in Certain Memory Modules and Components Thereof, and Products Containing Same, filed May 8, 2017.
	533.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1025, Complainant Netlist, Inc., Initial Post-Hearing Brief , filed May 30, 2017.
	534.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1026, Respondents' Post-Hearing Brief , filed May 30, 2017.
	535.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Declaration of Dr. Harold Stone, filed December 22, 2017.
	536.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1003: Declaration of Dr. Harold Stone, filed December 22, 2017.
	537.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1027, Demonstrative-Graphics-from-hynix-post-hearing-brief, filed December 22, 2017.
	538.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1028, Netlist-reply-post-hearing-brief, filed December 22, 2017.
	539.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1029, Respondent's Reply Post-Hearing Brief, filed December 22, 2017.
	540.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1030, High-Quality Versions of Demonstrative-Graphics-from-hynix-reply-post-hearing-brief, filed December 22, 2017.
	541.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1031, Institution of the '185 patent, filed December 22, 2017.
	542.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1032, Final Written Decision, Diablo Techs., Inc v. Netlist Inc., Paper No. 33, filed December 22, 2017.
	543.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1033, Decision, Netlist Inc., v. Diablo Techs., Inc., filed December 22, 2017.
	544.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1034, Netlist's Infringement Claim Chart of , filed December 22, 2017.

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	545.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1035, Stone, H.S. Microcomputer Interfacing, Reading, MA Addison Wesley, filed December 22, 2017.
	546.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1039, Intel E7525 Memory Controller Hub (MCH) Chipset Datasheet, filed December 22, 2017.
	547.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1040, Initial Determination, Certain Memory Modules and Components Thereof, and Products Containing Same, filed December 22, 2017.
	548.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1041, MEMORY-SYSTEMS-Cache-DRAM-Disk, Bruce Jacobs et al., filed December 22, 2017.
	549.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1042, Direct DRAM Datasheet, Bruce Jacobs et al., filed December 22, 2017.
	550.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petition, filed December 22, 2017.
	551.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1011: JEDEC Standard DDR2 SDRAM Specification, JESD79-2B (January 2005), filed December 27, 2017.
	552.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Notice of Accorded Filing Date, filed January 10, 2018.
	553.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Preliminary Response, filed April 10, 2018.
	554.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Granting Institution of Inter Partes Review, filed June 29, 2018.
	555.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Objection to Petition Evidence, filed July 16, 2018.
	556.	Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Mehran Arjomand,' filed July 30, 2018.
	557.	Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Michael D. Hatcher,' filed July 30, 2018.
	558.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Order 37 C.F.R. 42.5, filed August 2, 2018.

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	559.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Supplemental Mandatory Notices, filed September 17, 2018.
	560.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2002: Declaration of R. Jacob Baker, Ph.D, P.E., filed October 19, 2018.
	561.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2003: Deposition of Harold S. Stone, Ph. D, October 5, 2018., filed October 19, 2018.
	562.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2004: United States International Trade Commission, Inv. No. 337-TA-1089, Joint List of Claim Terms for Construction and Proposed Constructions, filed October 19, 2018.
	563.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2005: United States International Trade Commission, Inv. No. 337-TA-1089, Order No. 17: Construing Terms of the Asserted Patents, filed October 19, 2018.
	564.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Response, filed October 19, 2018.
	565.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1043, 'Chart comparing text in Dr. Baker's declaration [Ex. 2002] with identical text in Patent Owner's Response [Paper No. 14],' filed February 11, 2019.
	566.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1044, 'Deposition Transcript of R. Jacob Baker (Jan. 26, 2019.),' filed February 11, 2019.
	567.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1045, 'Deposition Transcript of R. Jacob Baker (Jan. 12, 2018) in IPR2017-00577 concerning the parent to the '907 Patent,' filed February 11, 2019.
	568.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1046, 'Final Office Action concerning U.S. Patent Application No. 15/470,856 (dated 7/27/18),' filed February 11, 2019.
	569.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1047, 'Certified translation of the Examination Decision issued by the State Intellectual Property Office of the P.R.C. (dated 5/30/18),' filed February 11, 2019.
	570.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1048, 'Certified translation of the Preliminary Opinion issued by the German Patent and Trademark Office (dated 1/8/19),' filed February 11, 2019.
	571.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Reply to Patent Owner's Response, filed February 11, 2019.
	572.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Motion To Exclude, filed February 19, 2019.

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	573.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Objections To Reply Evidence, filed February 19, 2019.
	574.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Request For Oral Argument, filed February 19, 2019.
	575.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Request for Oral Argument, filed February 19, 2019.
	576.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Corrected Petitioners' Reply to Patent Owner's Response, filed February 20, 2019.
	577.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 3002, 'Patent Owner's Request for Sur Reply,' filed March 1, 2019.
	578.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Opposition to Patent Owner's Motion to Exclude, filed March 5, 2019.
	579.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Sur-Reply To Petitioner's Corrected Reply, filed March 8, 2019.
	580.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Reply To Petitioner's Opposition To Motion To Exclude, filed March 12, 2019.
	581.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Order - Trial Hearing, filed March 22, 2019.
	582.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 30, 'Record of Oral Hearing,' filed June 27, 2019, 131 pgs.
	583.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 29, 'Termination Decision Document,' filed June 27, 2019, 94 pgs.
	584.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petition, filed December 22, 2017.
	585.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Preliminary Response, filed April 10, 2018.
	586.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Decision Granting Institution of Inter Partes Review, filed June 29, 2018.
	587.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1043, 'Deposition Transcript of R. Jacob Baker (Feb. 9, 2019.),' filed February 22, 2019.
	588.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1044, 'Declaration of R. Jacob Baker in IPR2017-00577 concerning the parent to the '907 Patent (Oct. 25, 2017),' filed February 22, 2019.

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	589.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1045, 'Deposition Transcript of R. Jacob Baker in IPR2017-00577 concerning the parent to the '907 Patent (Jan. 12, 2018),' filed February 22, 2019.
	590.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1046, 'Final Written Decision in IPR2017-00577 invalidating all challenged claims to the parent to the '907 Patent (July 5, 2018),' filed February 22, 2019.
	591.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1048, 'U.S. Patent No. 7,133,960,' filed February 22, 2019.
	592.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Reply to Patent Owner's Response, filed February 22, 2019.
	593.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Order, Trial Hearing, filed March 1, 2019.
	594.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Objections To Reply Evidence, filed March 1, 2019.
	595.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Motion To Exclude, filed March 4, 2019.
	596.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Request For Oral Argument, filed March 4, 2019.
	597.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Request for Oral Argument, filed March 4, 2019.
	598.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Opposition to Patent Owner's Motion to Exclude, filed March 11, 2019.
	599.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Sur-Reply To Petitioner's Reply, filed March 15, 2019.
	600.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Reply To Petitioner's Opposition To Motion To Exclude, filed March18, 2019.
	601.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Order, Trial Hearing, filed March 22, 2019.
	602.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Curriculum Vitae of Dr. Harold Stone, filed December 27, 2017.
	603.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Declaration of Dr. Harold Stone, filed December 27, 2017.
	604.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, File History of U.S. Patent No.9606907, filed December 27, 2017.
	605.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Petition, filed December 27, 2017.

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	606.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Patent Owner's Preliminary Response, filed May 7, 2018.
	607.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Decision Granting Institution of Inter Partes Review, filed August 6, 2018.
	608.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Patent Owner's Objections to Petition Evidence, filed August 21, 2018.
	609.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Patent Owner's Supplemental Mandatory Notices, filed September 17, 2018.
	610.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Exhibit 2001: Annotated Fig. 4 of U.S. Patent No. 7024518 - Halbert, filed November 16, 2018.
	611.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Exhibit 2002: Declaration of R. Jacob Baker, Ph.D, P.E., filed November 16, 2018.
	612.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Patent Owner's Response, filed November 16, 2018.
	613.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364 EXHIBITS 1043, 'Deposition Transcript of R. Jacob Baker (Feb. 9, 2019.),' filed February 22, 2019.
	614.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00365, Patent Owner's Preliminary Response, filed December 27, 2017.
	615.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00365, Petition, filed December 27, 2017.
	616.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00365, Decision Granting Institution of Inter Partes Review, filed August 6, 2018.
	617.	Order Granting Request for Inter Partes Reexamination mailed September 8, 2010, for Control No. 95/000,381, filed June 9, 2010, 21 pages.
	618.	Non-Final Action mailed August 27, 2010, for Control No. 95/000,546, filed May 11, 2010, 16 pages.
	619.	Order Granting Request for Inter Partes Reexamination mailed August 9, 2010, for Control No. 95/000,546, filed May 11, 2010, 22 pages.
	620.	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control Nos. 95/000,546 and 95/000,577, mailed February 25, 2015, 25 pages.
	621.	Patent Trial and Appeal Board Decision on Request for Rehearing for Reexamination Control Nos. 95/000,546 and 95/000,577, mailed August 27, 2015, 5 pages.
	622.	Action Closing Prosecution mailed October 1, 2012, for Control Nos. 95/000,546 and 95/000,577, filed May 11, '2010 and October 20, 2010 respectively, 39 pages.

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				Application Number	***16/695,020***
				Filing Date	***November 25, 2019***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***TBD***
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	857.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Diablo Technologies, Inc.'s Invalidity Contentions, dated June 6, 2014.
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	861.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Smart Storage Systems, Inc.'s Invalidity Contentions, dated June 6, 2014
	862.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits E.1-E.7 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.

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				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***TBD***
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	864.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits D-1 to D6 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.
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	869.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Plaintiff Netlist Inc's Opposition to Defendant Inphi Corporation's Motion for Stay Pending Reexaminations and Interference Proceedings Regarding the Patents-In-Suit, filed May 3, 2010 in 23 pages. cited by other.
	870.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. Inphi Corporation, Plaintiff Netlist, Inc's First Amended Complaint For Patent Infringement, filed Dec. 23, 2009 in 8 pages. cited by other.
	871.	US District Court Civil Docket; Netlist Inc. v. Google Inc.; 4:09cv5718; Date filed Dec. 4, 2009. In 10 pages. cited by other.
	872.	U.S. Court of Appeals for the Federal Circuit, Decision on Appeal for Reexamination Control No. 95/001,381, filed November 13, 2015, 14 pages
	873.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Corrected Joint Claim

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				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***TBD***
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	874.	Construction and Prehearing Statement Pursuant to Patent L.R. 4-3, including Exhibit A, filed August 27, 2014, 28 pages.
	875.	Notice of Allowance, U.S. Pat. App. No. 12/504,131, February 12, 2013, 52 pages
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	891.	International Search Report and Written Opinion, PCT Application No. PCT/US2011/059209, January 31, 2013

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Electronic Acknowledgement Receipt

EFS ID:	41600916
Application Number:	16695020
International Application Number:	
Confirmation Number:	7514
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5023-US01
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Filing Date:	25-NOV-2019
Time Stamp:	20:31:35
Application Type:	Utility under 35 USC 111(a)

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	129980-5023US_IDS_Transmittal_2021-01-08.pdf	124198 72f25075dbbc965ac3ae924b85e3084e9c3f702d	no	4

Warnings:

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2	Information Disclosure Statement (IDS) Form (SB08)	129980-5023US01_IDS_List_Form_1449_2021-01-08.pdf	388380 250df85c35f8f59c2da345a14596c9993bbe8a5e	no	47
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed January 8, 2021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jefferey C. Solomon	Confirmation No.:	7514
Serial No.:	16/695,020	Art Unit:	2139
Filed:	November 25, 2019	Examiner:	TBD
For:	MEMORY MODULE WITH DATA BUFFERING	Attorney Docket No:	129980-5023-US01

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☐ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☐ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☒ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

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4d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☒ Copies of foreign patent documents and publications listed on Form PTO-1449 from prior application Serial No. **15/857,519**, filed on **December 28, 2017**; **14/715,486**, filed on **May 18, 2015**; **13/971,231** , filed on **August 20, 2013**; **13/287,081** , filed on **November 1, 2011**; **13/032,470** , filed on **February 22, 2011**; **12/955,711** , filed on **November 29, 2010**; **12/629,827** , filed on **December 2, 2009**; **12/408,652** , filed on **March 20, 2009**; **11/335,875** , filed on **January 19, 2006**; **11/173,175** , filed on **July 1, 2005**; **11/075,395** , filed on **March 7, 2005**, of which this application claims

priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5023-US01).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: January 8, 2021

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 03/30/2021

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER
BANSAL, GURTEJ

ART UNIT	PAPER NUMBER
2139	

DATE MAILED: 03/30/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/695,020	11/25/2019	Jefferey C. Solomon	129980-5023-US01	7514

TITLE OF INVENTION: MEMORY MODULE WITH DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	06/30/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

Petitioners
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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 03/30/2021
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/695,020	11/25/2019	Jefferey C. Solomon	129980-5023-US01	7514

TITLE OF INVENTION: MEMORY MODULE WITH DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	06/30/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
BANSAL, GURTEJ	2139	711-105000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

Petitioners
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/695,020	11/25/2019	Jefferey C. Solomon	129980-5023-US01	7514

79141 7590 03/30/2021

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER	
BANSAL, GURTEJ	
ART UNIT	**PAPER NUMBER**
2139	

DATE MAILED: 03/30/2021

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Petitioners
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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	**Application No.** 16/695,020	**Applicant(s)** Solomon et al.	
	Examiner GURTEJ BANSAL	**Art Unit** 2139	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to claims as filed dated 11/25/2019.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-15 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☑ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 01/08/2021.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

Allowable Subject Matter

1. Claims 1-15 are allowed.

2. The following is an examiner's statement of reasons for allowance:

Claim 1 recites the limitation, "the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module; wherein data transfers through the circuitry are registered for an additional amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices."

Said limitations are taught by the specification as originally filed. Said limitations, in combination with the other recited limitations, are not taught or suggested by the prior art of record.

Claims 2-15 depend from independent claim 1 and are considered allowable for at least the same reasons are recited above.

Janzen (US 2003/0018845) appears to be the closest prior art and teaches a memory device having a number of ranks having different burst order addressing for read and write operations. However, does not teach the limitation, "the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in

accordance with an overall CAS latency of the memory module; wherein data transfers through the circuitry are registered for an additional amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices."

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to GURTEJ BANSAL whose telephone number is (571)270-5588. The examiner can normally be reached on M-F 8am-5pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571)-272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

Notice of References Cited	Application/Control No. 16/695,020	Applicant(s)/Patent Under Reexamination Solomon et al.	
	Examiner GURTEJ BANSAL	Art Unit 2139	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20030018845-A1	01-2003	Janzen, Jeffery W.	G11C7/103	711/1
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
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	S					
	T					

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	U	
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	W	
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/695,020	Solomon et al.
	Examiner	Art Unit
	GURTEJ BANSAL	2139

CPC - Searched*		
Symbol	Date	Examiner
G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc. G11C5/04.cpc. G11C7/1072.cpc. G11C15/00.cpc.	03/25/2021	GB
G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc. G11C5/04.cpc. G11C7/1072.cpc. G11C15/00.cpc. with text limiting	03/25/2021	GB

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Text Search in EAST (See Attached)	03/25/2021	GB
NPL Search in Google Scholar (See Attached)	03/25/2021	GB
Inventor Search in PE2E	03/25/2021	GB

/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	

Petitioners
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/695,020	Solomon et al.
	Examiner	Art Unit
	GURTEJ BANSAL	2139

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc . G06F13/4243.cpc. G06F13/4282.cpc. G11C5/04. cpc. G11C7/1072.cpc. G11C15/00.cpc.	03/25/2021	GB

/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	

Petitioners
Ex. 1057, p. 234

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/695,020	Solomon et al.
	Examiner	Art Unit
	GURTEJ BANSAL	2139

CPC							
Symbol						Type	Version
G06F	/	13	/	1673		F	2013-01-01
G11C	/	5	/	04		I	2013-01-01
G06F	/	13	/	00		I	2013-01-01
G06F	/	12	/	00		I	2013-01-01
G06F	/	13	/	4243		I	2013-01-01
G06F	/	13	/	4282		I	2013-01-01
G11C	/	7	/	1072		I	2013-01-01
G11C	/	15	/	00		I	2013-01-01
Y02D	/	10	/	00		A	2018-01-01

CPC Combination Sets								
Symbol						Type	Set	Ranking	Version
	/		/						

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	15	
/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	25 March 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	9A

U.S. Patent and Trademark Office — Part of Paper No.: 20210325

Petitioners
Ex. 1057, p. 235

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/695,020	Solomon et al.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

INTERNATIONAL CLASSIFICATION				
CLAIMED				
G06F	/	12	/	00

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	15	
/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	25 March 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	9A

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Petitioners
Ex. 1057, p. 236

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
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	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	15	
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(Primary Examiner)	(Date)	1	9A

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Application No: 16/695,020

Foreign Priority claimed: ○ Yes ◉ No

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Verified and Acknowledged: /GURTEJ BANSAL/ Examiner's Signature | Initials

Title: MEMORY MODULE WITH DATA BUFFERING

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/25/2019	711	2139	129980-5023-US01
RULE			

APPLICANTS

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INVENTORS

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Jayesh R. Bhakta, Cerritos, CA, UNITED STATES

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IF REQUIRED, FOREIGN LICENSE GRANTED**

12/13/2019

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 8, 2021*	
				Application Number	***16/695,020***
				Filing Date	***November 25, 2019***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***TBD***
Sheet	1	of	47	Attorney Docket Number	***129980-5023-US01***

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				Art Unit	*2139*
				Examiner Name	*TBD*
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				First Named Inventor	*Jefferey C. Solomon*
				Art Unit	*2139*
				Examiner Name	*TBD*
Sheet	3	of	47	Attorney Docket Number	*129980-5023-US01*

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				Art Unit	*2139*
				Examiner Name	*TBD*
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				Art Unit	*2139*
				Examiner Name	*TBD*
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				Art Unit	***2139***
				Examiner Name	***TBD***
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	375.	Inter Partes Review Case No. IPR2014-01020, Exhibit 1002 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on April 7, 2015.
	376.	Inter Partes Review Case No. IPR2014-01020, Exhibit 1023 to Petition for Inter Partes Review, curriculum vitae of Dr. Srinivasan Jagannathan, filed on April 7, 2015.
	377.	Inter Partes Review Case No. IPR2014-01020, Exhibit 1025 to Petition for Inter Partes Review, "operational," The Pocket Oxford American Dictionary of Current English, Oxford University Press, 2002, filed on April 7, 2015.
	378.	Inter Partes Review Case No. IPR2014-01020, Decision to Institute Inter Partes Review of D U.S. Patent No. 7,881,150, dated October 8, 2015.
	379.	Inter Partes Review Case No. IPR2014-01021, Exhibit 1026 to Petition for Inter Partes Review, curriculum vitae of Dr. Srinivasan Jagannathan, filed on April 7, 2015.
	380.	Inter Partes Review Case No. IPR2014-01021, Corrected Exhibit 1002 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on April 22, 2015.
	381.	Inter Partes Review Case No. IPR2014-01021, Decision to Institute Inter Partes Review of U.S. Patent No. 8,081,536, dated October 8, 2015
	382.	Petition for Inter Partes Review filed on 6/24/2014 for U.S. Patent No. 8,516,185, Case No. IPR2014-01029, and all associated documents including cited references and expert declarations, available at https://ptabtrials.uspto.gov
	383.	Inter Partes Review Case No. IPR2014-01029, Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on June 24, 2014.

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				First Named Inventor	***Jefferey C. Solomon***
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	384.	Inter Partes Review Case No. IPR2014-01029, Exhibit 1008 to Petition for Inter Partes Review, "Declaration of Charles J. Neuhauser, Ph.D. under 37 C.F.R. § 1.68," filed on June 24, 2014.
	385.	Inter Partes Review Case No. IPR2014-01029, Supplemental Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on July 23, 2014.
	386.	Inter Partes Review Case No. IPR2014-01029, Patent Owner's Preliminary Response pursuant to 37 C.F.R. § 42.107, filed on October 17, 2014.
	387.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014.
	388.	Inter Partes Review Case No. IPR2014-01029, Petitioner's Request for Rehearing pursuant to 37 C.F.R. § 42.71, filed on January 15, 2015.
	389.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Request for Rehearing, Issued on March 3, 2015.
	390.	Inter Partes Review Case No. IPR2014-01369, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued March 9, 2014.
	391.	Inter Partes Review Case No. IPR2014-01369, Corrected Petition for Inter Partes Review of Claims 1-19 of U.S. Patent No. 8,516,185, filed on September 22, 2014.
	392.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1008 to Corrected Petition for Inter Partes Review, "Declaration of Dr. Nader Bagherzadeh under 37 C.F.R. § 1.68," filed on September 22, 2014.
	393.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1013 to Corrected Petition for Inter Partes Review, "Webster's II New College Dictionary," filed on September 22, 2014.
	394.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1014 to Corrected Petition for Inter Partes Review, "Standard Dictionary of Electrical and Electronics Terms," IEEE 1988, filed on September 22, 2014.
	395.	Inter Partes Review Case No. IPR2015-0 021, Petition for Inter Partes Review of U.S. Patent No. 8,081,536, filed on April 7, 2015
	396.	Inter Partes Review Case No. IPR2015-01020, Petition for Inter Partes Review of U.S. Patent No. 7,881,150, filed on April 7, 2015.
	397.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Related Matters, filed April 28, 2015
	398.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner Response to Petition, filed February 22, 2016
	399.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016

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	400.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2002, "Videotaped Deposition of Srinivasan Jagannathan, Ph.D on February 12, 2016," filed February 22, 2016
	401.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2003, "Videotaped Deposition of Srinivasan Jagannathan, Ph.D on April 20, 2015," filed February 22, 2016
	402.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Objections to Evidence, filed February 29, 2016
	403.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Reply, filed May 19, 2016
	404.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016
	405.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, May 10, 2016 Deposition of Carl Sechen, filed May 19, 2016
	406.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner Request for Oral Argument, filed June 2, 2016
	407.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER MOTION FOR OBSERVATIONS, filed June 2, 2016
	408.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016
	409.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2007, "Deposition of Dr. Srinivasan Jagannathan on May 25, 2016," filed June 2, 2016
	410.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, ORDER Trial Hearing, filed June 8, 2016
	411.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016
	412.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Response to Motion for Observations, filed June 10, 2016
	413.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Response to Netlist's Submission, filed June 13, 2016
	414.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's Objections to Petitioner's Demonstrative Exhibits, filed June 23, 2016
	415.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's Demonstrative Exhibits, filed June 24, 2016

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	416.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Updated Exhibit List, filed June 24, 2016
	417.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Demonstrative Exhibits, filed June 24, 2016
	418.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Record of Oral Hearing, dated July 26, 2016
	419.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Final Written Decision, issued September 28, 2016
	420.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3001 to Final Decision, issued September 28, 2016
	421.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3001-2 to Final Decision, issued September 28, 2016
	422.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3002 to Final Decision, issued September 28, 2016
	423.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3003 to Final Decision, issued September 28, 2016
	424.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3004 to Final Decision, issued September 28, 2016
	425.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner Response to Petition, filed February 22, 2016
	426.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016
	427.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Objections to Evidence, filed February 29, 2016
	428.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Reply, filed May 19, 2016
	429.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016
	430.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner Request for Oral Argument, filed June 2, 2016
	431.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, PATENT OWNER MOTION FOR OBSERVATIONS, filed June 2, 2016
	432.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016

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	433.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner's SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016
	434.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Response to Motion for Observations, filed June 10, 2016
	435.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Response to Patent Owner's Submission, filed June 13, 2016
	436.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner's Objections to Petitioner's Demonstrative Exhibits, filed June 23, 2016
	437.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner's Demonstrative Exhibits, filed June 24, 2016
	438.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Updated Exhibit List, filed June 24, 2016
	439.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Final Decision, issued September 28, 2016
	440.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Petition for Inter Partes Review, filed December 30, 2016
	441.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Exhibit 1003, "Declaration of Harold S. Stone," filed December 30, 2016
	442.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Exhibit 1008, Declaration of John J. Kelly Regarding Records of Joint Electron Device Engineering Council (JEDEC), filed December 30, 2016
	443.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, DECISION Institution of Inter Partes Review, filed May 15, 2017.
	444.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, Exhibit 2001 (DECLARATION OF PROFESSOR CARL SECHEN), filed September 15, 2017.
	445.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, Patent Owner's Response, filed September 15, 2017.
	446.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, PETITIONERS' OBJECTIONS TO EVIDENCE, filed September 15, 2017.
	447.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Deposition Transcript of Carl Sechen, filed December 15, 2017.
	448.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's reply to Patent Owner's Response, filed December 15, 2017.

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	449.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Supplemental Declaration of Harold S. Stone, filed December 15, 2017.
	450.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Xilinx Xilinx CS280 package datasheet (1999), filed December 15, 2017.
	451.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBIT 2004, filed January 9, 2017.
	452.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Motion for Observations, filed January 9, 2017.
	453.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed January 9, 2017.
	454.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBIT 2003, 'Synchronous DRAM Architectures, Organization, and Alternative Technologies,' filed January 18, 2017.
	455.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Response to Patent Owners Motion for Observations, filed January 23, 2018.
	456.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Opposition to Petitioner's Motion to Exclude, filed January 23, 2018.
	457.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Reply in Support of Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed January 30, 2018.
	458.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Demonstratives, filed February 9, 2018.
	459.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBIT 2005, filed February 9, 2018.
	460.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Updated Exhibit List, filed February 9, 2018.
	461.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Updated Exhibit List, filed February 9, 2018.
	462.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Final Written Decision, filed February 14, 2018.
	463.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Hearing Transcript, filed February 14, 2018.
	464.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Supplemental Mandatory Notices, filed April 19, 2018.

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	465.	Inter Partes Review of U.S. Patent No. 8516185, Case No. IPR2017-00577, Petition for Inter Partes Review, filed January 5, 2017
	466.	Inter Partes Review of U.S. Patent No. 8516185, Case No. IPR2017-00577, Exhibit 1003, "Declaration of Harold S. Stone," filed January 5, 2017
	467.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, DECISION Institution of Inter Partes Review, filed July 7, 2017.
	468.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, SCHEDULING ORDER, filed July 7, 2017.
	469.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2003 (DECLARATION OF R. JACOB BAKER, PH.D., P.E.), filed October 25, 2017.
	470.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2004 (Deposition of HAROLD S. STONE, PH.D.), filed October 25, 2017.
	471.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2005 (Memory Systems: Cache, DRAM, Disk), filed October 25, 2017.
	472.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2006 (PC2100 and PC1600 DDR SDRAM Registered DIMM, Design Specification, Revision 1.3, January 2002), filed October 25, 2017.
	473.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2007 (DRAM CIRCUIT DESIGN: Fundamental and High-Speed Topics), filed October 25, 2017.
	474.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, PATENT OWNER'S RESPONSE, filed October 25, 2017.
	475.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, PETITIONERS' OBJECTIONS TO EVIDENCE, filed October 31, 2017.
	476.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing 4:1 MUX/DeMUX and 4 ranks of memory (corrected Ex. 1035), filed February 6, 2018.
	477.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing 4:1 MUX/DeMUX and 4 ranks of memory, filed February 6, 2018.
	478.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing Fast components and Slow components, filed February 6, 2018.
	479.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Deposition Transcript of R. Jacob Baker (Jan. 12, 2018.), filed February 6, 2018.

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	480.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Excerpts from Brent Keeth and R. Jacob Baker, DRAM Circuit Design: A Tutorial (IEEE Press 2001), filed February 6, 2018.
	481.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Oral Testimony of R. Jacob Baker in Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (May 11, 2017), filed February 6, 2018.
	482.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioners' Reply to Patent Owner's Response, filed February 6, 2018.
	483.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Objections to Evidence, filed February 13, 2018.
	484.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Motion to Exclude, filed February 28, 2018.
	485.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Request for Oral Argument, filed February 28, 2018.
	486.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioner's Opposition to Patent Owner's Motion to Exclude, filed March 14, 2018.
	487.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Reply to Opposition to Motion to Exclude, filed March 21, 2018.
	488.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Hearing Transcript, filed April 6, 2018.
	489.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Termination Decision Document, filed July 7, 2018.
	490.	Inter Partes Review of U.S. Patent No. 7,532,537, Case No. IPR2017-00667, DECISION Institution of Inter Partes Review, filed July 21, 2017.
	491.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Objections to Evidence, filed November 14, 2017.
	492.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Supplemental Objections to Evidence, filed November 14, 2017.
	493.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Deposition of Carl Sechen, Ph.D. taken December 8, 2017, filed February 26, 2018.
	494.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Deposition of Carl Sechen, Ph.D. taken February 8, 2018., filed February 26, 2018.
	495.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Google, Inc. et al. v. Netlist, Inc., Appeal 2014-00777, filed February 26, 2018.

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	496.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Reply to Patent Owner's Response, filed February 26, 2018.
	497.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Objections to Evidence, filed March 5, 2018.
	498.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Exhibit 2007, Deposition of Harold S. Stone, filed March 19, 2018.
	499.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Motion for Observations, filed March 19, 2018.
	500.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Request for Oral Argument, filed March 19, 2018.
	501.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Motion to Exclude, filed March 19, 2018.
	502.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Submission on Propriety of Petitioners Reply, filed March 20, 2018.
	503.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Response to Patent Owner's Submission on Propriety of Petitioner's Reply and Supplemental Stone Declaration 1, filed March 27, 2018.
	504.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Reply in Support of its Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed April 2, 2018.
	505.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Updated Mandatory Notices, filed April 2, 2018.
	506.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Response to Patent Owner's Motion for Observations, filed April 2, 2018.
	507.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Objection to Petitioner's Demonstratives, filed April 20, 2018.
	508.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Hearing Transcript, filed April 24, 2018.
	509.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Final Written Decision, filed July 18, 2018.
	510.	Inter Partes Review of U.S. Patent No. 7,532,537, Case No. IPR2017-00668, DECISION Institution of Inter Partes Review, filed July 21, 2017.
	511.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Objections to Evidence, filed November 14, 2017.
	512.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Notice of Deposition of Carl Sechen, filed January 30, 2018.

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				First Named Inventor	***Jefferey C. Solomon***
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	513.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Supplemental Objections to Evidence, filed February 15, 2018.
	514.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Reply to Patent Owner's Response, filed February 26, 2018.
	515.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Objections to Evidence, filed March 5, 2018.
	516.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Motion for Observations, filed March 19, 2018.
	517.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Request for Oral Argument, filed March 19, 2018.
	518.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Submission on Propriety of Petitioner's Reply, filed March 20, 2018.
	519.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Response to Patent Owner's Submission on Propriety of Petitioner's Reply and Supplemental Stone Declaration, filed March 27, 2018.
	520.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Opposition to Petitioner's Motion to Exclude, filed April 2, 2018.
	521.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Response to Patent Owner's Motion for Observations, filed April 2, 2018.
	522.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Reply in Support of its Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed April 9, 2018.
	523.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Objections to Petitioner's Demonstratives, filed April 20, 2018.
	524.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Hearing Transcript, filed April 24, 2018.
	525.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Final Written Decision, filed July 18, 2018.
	526.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017.-00549, Xilinx CoolRunner XPLA3 CPLD product specification (2000), filed December 15, 2017.
	527.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017.-00549, Xilinx Programmable Logic Design Quick Start Handbook (2004), filed December 15, 2017.
	528.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017.-00549, Xilinx Xilinx TQFP package datasheet (2000), filed December 15, 2017.
	529.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017.-00549, Xilinx Xilinx VQFP package datasheet (2002), filed December 15, 2017.

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				First Named Inventor	***Jefferey C. Solomon***
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	530.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1022, Decision Denying Institution of Inter Partes Review, filed December 16, 2014
	531.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1023, Decision Denying Institution of Inter Partes Review, filed March 9, 2015
	532.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1024, Excepts from the Hearing in Certain Memory Modules and Components Thereof, and Products Containing Same, filed May 8, 2017.
	533.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1025, Complainant Netlist, Inc., Initial Post-Hearing Brief , filed May 30, 2017.
	534.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1026, Respondents' Post-Hearing Brief , filed May 30, 2017.
	535.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Declaration of Dr. Harold Stone, filed December 22, 2017.
	536.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1003: Declaration of Dr. Harold Stone, filed December 22, 2017.
	537.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1027, Demonstrative-Graphics-from-hynix-post-hearing-brief, filed December 22, 2017.
	538.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1028, Netlist-reply-post-hearing-brief, filed December 22, 2017.
	539.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1029, Respondent's Reply Post-Hearing Brief, filed December 22, 2017.
	540.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1030, High-Quality Versions of Demonstrative-Graphics-from-hynix-reply-post-hearing-brief, filed December 22, 2017.
	541.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1031, Institution of the '185 patent, filed December 22, 2017.
	542.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1032, Final Written Decision, Diablo Techs., Inc v. Netlist Inc., Paper No. 33, filed December 22, 2017.
	543.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1033, Decision, Netlist Inc., v. Diablo Techs., Inc., filed December 22, 2017.
	544.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1034, Netlist's Infringement Claim Chart of , filed December 22, 2017.

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	545.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1035, Stone, H.S. Microcomputer Interfacing, Reading, MA Addison Wesley, filed December 22, 2017.
	546.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1039, Intel E7525 Memory Controller Hub (MCH) Chipset Datasheet, filed December 22, 2017.
	547.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1040, Initial Determination, Certain Memory Modules and Components Thereof, and Products Containing Same, filed December 22, 2017.
	548.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1041, MEMORY-SYSTEMS-Cache-DRAM-Disk, Bruce Jacobs et al., filed December 22, 2017.
	549.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1042, Direct DRAM Datasheet, Bruce Jacobs et al., filed December 22, 2017.
	550.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petition, filed December 22, 2017.
	551.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1011: JEDEC Standard DDR2 SDRAM Specification, JESD79-2B (January 2005), filed December 27, 2017.
	552.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Notice of Accorded Filing Date, filed January 10, 2018.
	553.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Preliminary Response, filed April 10, 2018.
	554.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Granting Institution of Inter Partes Review, filed June 29, 2018.
	555.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Objection to Petition Evidence, filed July 16, 2018.
	556.	Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Mehran Arjomand,' filed July 30, 2018.
	557.	Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Michael D. Hatcher,' filed July 30, 2018.
	558.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Order 37 C.F.R. 42.5, filed August 2, 2018.

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	559.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Supplemental Mandatory Notices, filed September 17, 2018.
	560.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2002: Declaration of R. Jacob Baker, Ph.D, P.E., filed October 19, 2018.
	561.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2003: Deposition of Harold S. Stone, Ph. D, October 5, 2018., filed October 19, 2018.
	562.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2004: United States International Trade Commission, Inv. No. 337-TA-1089, Joint List of Claim Terms for Construction and Proposed Constructions, filed October 19, 2018.
	563.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2005: United States International Trade Commission, Inv. No. 337-TA-1089, Order No. 17: Construing Terms of the Asserted Patents, filed October 19, 2018.
	564.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Response, filed October 19, 2018.
	565.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1043, 'Chart comparing text in Dr. Baker's declaration [Ex. 2002] with identical text in Patent Owner's Response [Paper No. 14],' filed February 11, 2019.
	566.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1044, 'Deposition Transcript of R. Jacob Baker (Jan. 26, 2019.),' filed February 11, 2019.
	567.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1045, 'Deposition Transcript of R. Jacob Baker (Jan. 12, 2018) in IPR2017-00577 concerning the parent to the '907 Patent,' filed February 11, 2019.
	568.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1046, 'Final Office Action concerning U.S. Patent Application No. 15/470,856 (dated 7/27/18),' filed February 11, 2019.
	569.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1047, 'Certified translation of the Examination Decision issued by the State Intellectual Property Office of the P.R.C. (dated 5/30/18),' filed February 11, 2019.
	570.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1048, 'Certified translation of the Preliminary Opinion issued by the German Patent and Trademark Office (dated 1/8/19),' filed February 11, 2019.
	571.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Reply to Patent Owner's Response, filed February 11, 2019.
	572.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Motion To Exclude, filed February 19, 2019.

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	573.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Objections To Reply Evidence, filed February 19, 2019.
	574.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Request For Oral Argument, filed February 19, 2019.
	575.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Request for Oral Argument, filed February 19, 2019.
	576.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Corrected Petitioners' Reply to Patent Owner's Response, filed February 20, 2019.
	577.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 3002, 'Patent Owner's Request for Sur Reply,' filed March 1, 2019.
	578.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Opposition to Patent Owner's Motion to Exclude, filed March 5, 2019.
	579.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Sur-Reply To Petitioner's Corrected Reply, filed March 8, 2019.
	580.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Reply To Petitioner's Opposition To Motion To Exclude, filed March 12, 2019.
	581.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Order - Trial Hearing, filed March 22, 2019.
	582.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 30, 'Record of Oral Hearing,' filed June 27, 2019, 131 pgs.
	583.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 29, 'Termination Decision Document,' filed June 27, 2019, 94 pgs.
	584.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petition, filed December 22, 2017.
	585.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Preliminary Response, filed April 10, 2018.
	586.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Decision Granting Institution of Inter Partes Review, filed June 29, 2018.
	587.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1043, 'Deposition Transcript of R. Jacob Baker (Feb. 9, 2019.),' filed February 22, 2019.
	588.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1044, 'Declaration of R. Jacob Baker in IPR2017-00577 concerning the parent to the '907 Patent (Oct. 25, 2017),' filed February 22, 2019.

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	589.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1045, 'Deposition Transcript of R. Jacob Baker in IPR2017-00577 concerning the parent to the '907 Patent (Jan. 12, 2018),' filed February 22, 2019.
	590.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1046, 'Final Written Decision in IPR2017-00577 invalidating all challenged claims to the parent to the '907 Patent (July 5, 2018),' filed February 22, 2019.
	591.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1048, 'U.S. Patent No. 7,133,960,' filed February 22, 2019.
	592.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Reply to Patent Owner's Response, filed February 22, 2019.
	593.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Order, Trial Hearing, filed March 1, 2019.
	594.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Objections To Reply Evidence, filed March 1, 2019.
	595.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Motion To Exclude, filed March 4, 2019.
	596.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Request For Oral Argument, filed March 4, 2019.
	597.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Request for Oral Argument, filed March 4, 2019.
	598.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Opposition to Patent Owner's Motion to Exclude, filed March 11, 2019.
	599.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Sur-Reply To Petitioner's Reply, filed March 15, 2019.
	600.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Reply To Petitioner's Opposition To Motion To Exclude, filed March18, 2019.
	601.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Order, Trial Hearing, filed March 22, 2019.
	602.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Curriculum Vitae of Dr. Harold Stone, filed December 27, 2017.
	603.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Declaration of Dr. Harold Stone, filed December 27, 2017.
	604.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, File History of U.S. Patent No.9606907, filed December 27, 2017.
	605.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Petition, filed December 27, 2017.

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	606.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Patent Owner's Preliminary Response, filed May 7, 2018.
	607.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Decision Granting Institution of Inter Partes Review, filed August 6, 2018.
	608.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Patent Owner's Objections to Petition Evidence, filed August 21, 2018.
	609.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Patent Owner's Supplemental Mandatory Notices, filed September 17, 2018.
	610.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Exhibit 2001: Annotated Fig. 4 of U.S. Patent No. 7024518 - Halbert, filed November 16, 2018.
	611.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Exhibit 2002: Declaration of R. Jacob Baker, Ph.D, P.E., filed November 16, 2018.
	612.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Patent Owner's Response, filed November 16, 2018.
	613.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364 EXHIBITS 1043, 'Deposition Transcript of R. Jacob Baker (Feb. 9, 2019.),' filed February 22, 2019.
	614.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00365, Patent Owner's Preliminary Response, filed December 27, 2017.
	615.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00365, Petition, filed December 27, 2017.
	616.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00365, Decision Granting Institution of Inter Partes Review, filed August 6, 2018.
	617.	Order Granting Request for Inter Partes Reexamination mailed September 8, 2010, for Control No. 95/000,381, filed June 9, 2010, 21 pages.
	618.	Non-Final Action mailed August 27, 2010, for Control No. 95/000,546, filed May 11, 2010, 16 pages.
	619.	Order Granting Request for Inter Partes Reexamination mailed August 9, 2010, for Control No. 95/000,546, filed May 11, 2010, 22 pages.
	620.	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control Nos. 95/000,546 and 95/000,577, mailed February 25, 2015, 25 pages.
	621.	Patent Trial and Appeal Board Decision on Request for Rehearing for Reexamination Control Nos. 95/000,546 and 95/000,577, mailed August 27, 2015, 5 pages.
	622.	Action Closing Prosecution mailed October 1, 2012, for Control Nos. 95/000,546 and 95/000,577, filed May 11, '2010 and October 20, 2010 respectively, 39 pages.

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	623.	Patent Owner's Appeal Brief for Reexamination Control Nos. 95/000,546 and 95/000,577, filed October 2, 2013, 46 pages
	624.	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control Nos. 95/000,546 and 95/000,577, mailed February 25, 2015, 25 pages.
	625.	Patent Trial and Appeal Board Decision on Request for Rehearing for Reexamination Control Nos. 95/000,546 and 95/000,577, mailed August 27, 2015, 5 pages.
	626.	Order Granting Request for Inter Partes Reexamination mailed January 18, 2011, for Control No. 95/000,577, filed October 20, 2010, 17 pages.
	627.	Portion of Request for Inter Partes Reexamination of U.S. Patent No. 7,289,386, corresponding to Reexam Control No. 95/000,577, in 184 pages. cited by other.
	628.	Order Granting Request for Inter Partes Reexamination mailed January 18, 2011, for Control No. 95/000,578, filed October 20, 2010, 14 pages.
	629.	Portion of Request for Inter Partes Reexamination of U.S. Patent No. 7,619,912, corresponding to Reexam Control No. 95/000,578, in 66 pages. cited by other.
	630.	Patent Owner's Response to Office Action mailed November 13, 2012 for Reexamination Control Nos. 95/000,578; 95/000,579, and 95/001,339, filed January 14, 2013, 96 pages.
	631.	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control Nos. 95/000,578; 95/000,579; and 95/001,339, mailed May 31, 2016, 106 pages.
	632.	Order Granting Request for Inter Partes Reexamination mailed January 14, 2011, for Control No. 95/000,579, filed October 21, 2010, 12 pages.
	633.	Portion of Request for Inter Partes Reexamination of U.S. Patent No. 7,619,912, corresponding to Reexam Control No. 95/000,579, in 32 pages. cited by other.
	634.	Examiner's Determination after Board Decision on Appeal for Reexamination Control No. 95/001,337, mailed September 11, 2015, 16 pages.
	635.	Non-Final Action Closing Prosecution mailed March 12, 2012, for Control No. 95/001,337, filed April 19, 2010, 33 pages.
	636.	Non-Final Action mailed September 27, 2011, for Control No. 95/001,337, filed April 19, 2010, 19 pages.
	637.	Order Granting Request for Inter Partes Reexamination mailed August 27, 2010, for Control No. 95/001,337, filed April 19, 2010, 21 pages.
	638.	Right of Appeal Notice mailed June 22, 2012, for Control No. 95/001,337, filed June 4 2010, 34 pages.
	639.	Non-Final Action Closing Prosecution mailed September 1, 2010, for Control No. 95/001,339, filed April 10, 2010, 17 pages.

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				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***TBD***
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A 6.4-Gb/s near-ground single-ended transceiver for dual-**rank** **DIMM** memory interface systems

M Bucher, RT Kollipara, B Su... - IEEE Journal of Solid ..., 2013 - ieeexplore.ieee.org

... a point-to-two point configuration for a dual-**rank** system [4]. Additional **ranks** could be ... et al.: 6.4-GB/S NEAR-GROUND SINGLE-ENDED TRANSCEIVER FOR DUAL-**RANK** **DIMM** MEMORY INTERFACE ... goal was to keep this under 10 nS or comparable to the **CAS** **latency** of the ...

☆ 99 Cited by 20 Related articles All 3 versions

A 1.0-ns/1.0-V delay-locked loop with racing mode and countered **CAS** **latency** controller for DRAM interfaces

HW Lee, H Choi, BJ Shin, KH Kim... - IEEE journal of solid ..., 2012 - ieeexplore.ieee.org

... on 667-DDR2 by 39% when the server is in idle state [1]. **DIMM** based DDR3 ... al., "A 1.6-Gb/s/pin double data rate SDRAM with wave- pipelined **CAS** **latency** control," IEEE ... loop using power noise management technique with unregulated power supply for pseudo-**rank** DRAM in ...

☆ 99 Cited by 32 Related articles All 6 versions

A DDR2 controller for BEE3

C Thacker - Microsoft Research, 2009 - aitia.ac.upc.edu

... which reduce the loading on the address and control lines at the expense of an extra cycle of **CAS** **latency** ... Each **DIMM** consists of two **ranks**, for a total of four **ranks** per controller ... Note that the controller uses location 0 in **rank** 1 during calibration, so user logic should not make ...

☆ 99 Cited by 13 Related articles »

Fully-buffered **DIMM** memory architectures: Understanding mechanisms, overheads and scaling

B Ganesh, A Jaleel, D Wang... - 2007 IEEE 13th ..., 2007 - ieeexplore.ieee.org

... DD0 RAS DD3 **CAS** DD1 DD2 D2 D1 D3 Southbound bus ... Typically, single-**rank** configurations have higher **latencies** due to insufficient number of memory banks to distribute requests to ... Adding more **ranks** in these system helps reduce the **DIMM**-based queueing delays ...

☆ 99 Cited by 104 Related articles All 13 versions »

Analysis of Memory Performance: Mixed **Rank** Performance Across Microarchitectures

M Bouache, JL Glover, J Boukhobza - International Conference on High ..., 2016 - Springer

... section, we are giving a background about the memory architecture, **ranking**, different types ... QRDIMMs (Quad **Ranked** **DIMMs**) are generally not recommended for best performance ... memory RAS (Row Access Select) modes [12]: Independent Channel Mode, **Rank** Sparing Mode ...

☆ 99 Cited by 1 Related articles All 3 versions

DECO: **DIMM** controller efficient for ECC operations

W Jang - Electronics Letters, 2014 - IET

... **DIMM**. **DIMMs** consist of two **ranks** and each **rank** includes nine syn- chronous dynamic random access memories (SDRAMs). Reversely ... command. The **DIMM** generates 9 byte ECC words after the **CAS** **latency** (CL) from the first **CAS** command ...

☆ 99 Cited by 1 Related articles All 7 versions »

Minimizing DRAM **rank** switching overhead for improved timing bounds and performance

L Ecco, A Kostrzewa, R Ernst - 2016 28th Euromicro ..., 2016 - ieeexplore.ieee.org

... If both **CAS** commands are of the same type, the cal- culations are simpler: for tRDRD dr, the ... tRTRS = 2 cycles, which, as described in Table II, is only valid for a dual-**rank** module with a ... In [15], [20], a TDM schedule is used to alternate be- tween the **ranks** and, consequently, the ...

☆ 99 Cited by 15 Related articles

Petitioners
Ex. 1057, p. 287

PRET DRAM controller: Bank privatization for predictability and temporal isolation

J Reineke, I Liu, HD Patel, S Kim... - 2011 Proceedings of the ..., 2011 - ieeexplore.ieee.org

... right side of Fig- ure 1 depicts a high-level view of the dual-**ranked** dual in ... sharing of I/O mechanisms within a device, consec- utive accesses to the same **rank** are more ... We later exploit this subtle difference by restricting consecutive accesses to different **ranks** to achieve more ...

☆ 99 Cited by 220 Related articles All 13 versions »

Decoupled **DIMM**: building high-bandwidth memory system using low-speed DRAM devices

H Zheng, J Lin, Z Zhang, Z Zhu - ACM SIGARCH Computer Architecture ..., 2009 - dl.acm.org

... which for DDR3 systems includes BA0-BA2 (banks address), A0-A13 (row/column address), RAS (Row Address Strobe), **CAS** (Column Address ... hit **latency** MSHR entries Inst:8, Data:32, L2:64 Memory 4/2/1-channels, 2-**DIMMs**/channel, 2-**ranks**/**DIMM**, 8-banks/**rank**, 9-devices ...

☆ 99 Cited by 91 Related articles All 13 versions

Duo: Exposing on-chip redundancy to **rank**-level ecc for high reliability

SL Gong, J Kim, S Lym, M Sullivan... - ... Symposium on High ..., 2018 - ieeexplore.ieee.org

... write **latency** = 10ns ... to maintain the 12.5% redundancy level; only a single ×4 redundant device will be available with a 32-bit wide **rank** and a ... This poses a challenge in achieving high reliability as seen today with ×8 DDR4-generation **ranks**, which cannot provide true SDDC ...

☆ 99 Cited by 10 Related articles All 5 versions

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L7	190	CS with buffer with RANK	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 01:25
L8	5,794	CAS with latency	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 01:35
L9	2,116	CAS with latency with memory	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 01:35
L10	1,704	CAS adj latency with memory	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 01:35
L11	221	CAS adj latency with memory with (DIMM module rank)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 01:35
L12	503	grundy.in.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 01:41
L13	1,171	CS with dimm	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 01:43
L14	18,887	CS with rank	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 01:47
L15	95	CS with rank same burst	US-PGPUB;	OR	ON	2021/03/25 01:47

			USPAT; EPO; IBM_TDB			
L16	130	(US-4218740-$ | US-4249253-$ | US-4368515-$ | US-4392212-$ | US-4571676-$ | US-4592011-$ | US-4633429-$ | US-4670748-$ | US-4706214-$ | US-4739473-$ | US-4866603-$ | US-4958322-$ | US-4961172-$ | US-4961204-$ | US-4980850-$ | US-5060188-$ | US-5247643-$ | US-5272664-$ | US-5313624-$ | US-5345412-$ | US-5357478-$ | US-5388072-$ | US-5388240-$ | US-5392252-$ | US-5426753-$ | US-5463590-$ | US-5483497-$ | US-5485589-$ | US-5495435-$ | US-5513135-$ | US-5532954-$ | US-5537584-$ | US-5541448-$ | US-5559970-$ | US-5572691-$ | US-5581498-$ | US-5590071-$ | US-5602999-$ | US-5617559-$ | US-5630096-$ | US-5638534-$ | US-5649159-$ | US-5655153-$ | US-5699542-$ | US-5702984-$ | US-5703826-$ | US-5717851-$ | US-5724604-$ | US-5729716-$ | US-5745914-$ | US-5764590-$ | US-5784705-$ | US-5802395-$ | US-5802541-$ | US-5805520-$ | US-5822251-$ | US-5905401-$ | US-5909388-$ | US-5926827-$ | US-5926839-$ | US-5953215-$ | US-5953280-$ | US-5958025-$ | US-5959930-$ | US-5963464-$ | US-5966736-$ | US-5973392-$ | US-5974493-$ | US-6011710-$ | US-6018787-$ | US-6044032-$ | US-6061754-$ | US-6070217-$ | US-6070227-$ | US-6097652-$ | US-6108745-$ | US-6115278-$ | US-6134638-$ | US-6141245-$ | US-6151271-$ | US-6154418-$ | US-6154419-$ | US-6173357-$ | US-6185654-$ | US-6188641-$ | US-6205516-$ | US-6209074-$ | US-6223650-$ | US-6226709-$ | US-6226736-$ | US-6233650-$ | US-6247088-$ | US-6260127-$ | US-6262938-$ | US-6317352-$ | US-6349051-$ | US-6381140-$ | US-6400637-$ | US-	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 01:50

		6408356-$ | US-6414868-$ | US-6415374-$ | US-6438062-$ | US-6446158-$ | US-6446184-$ | US-6453381-$ | US-6470417-$ | US-6480439-$ | US-6487102-$ | US-6502161-$ | US-6518794-$ | US-6526473-$ | US-6530007-$ | US-6530033-$ | US-6546476-$ | US-6553449-$ | US-6553450-$ | US-6618320-$ | US-6618791-$ | US-6621496-$ | US-6625081-$ | US-6625687-$ | US-6636446-$ | US-6636935-$ | US-6646949-$ | US-6658509-$ | US-6674684-$ | US-6681301-$ | US-6683372-$ | US-6697888-$ | US-6704910-$).DID.				
L17	27,800	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc. G11C5/04.cpc. G11C7/1072.cpc. G11C15/00.cpc.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 02:16
L18	0	(G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc. G11C5/04.cpc. G11C7/1072.cpc. G11C15/00.cpc.) with CAS with latency	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 02:19
L19	1,288	(G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc. G11C5/04.cpc. G11C7/1072.cpc. G11C15/00.cpc.) and CAS with latency	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 02:19
L20	80	(G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc. G11C5/04.cpc. G11C7/1072.cpc. G11C15/00.cpc.) and CAS with latency same rank	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 02:19
L21	2,861	CS with rank and @pd<="20060101"	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 02:39
L22	99	CS with rank with memory and @pd<="20060101"	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 02:39
S1	18,362	G06F3/0683.cpc. G06F3/0604.cpc. G06F3/0655.cpc.	US-PGPUB; USPAT;	OR	ON	2021/03/17 11:52

			EPO; IBM_TDB			
S2	31,786	memory adj bank	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/17 11:57
S3	579	S1 and S2	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/17 11:57
S4	5,003	memory adj bank with controller	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/17 20:41
S5	416	memory adj bank with controller with (switch mux multiplexer)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/17 20:57
S6	502	grundy.in.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/17 21:03
S7	27	DIMM with memory with controller with MUX	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/17 21:47
S8	107	RAM with memory with controller with MUX	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 00:23
S9	1	RAM with tiles same memory with controller same mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 00:42
S10	1	RAM with tiles same memory with controller same switch	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 00:44

S11	63	RAM with bank same memory with controller same switch	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 00:52
S12	4,598,109	memory controller with memory adj bank	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 00:57
S13	2,379	memory adj controller with memory adj bank	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 00:58
S14	221	memory adj controller with memory adj bank same (switch mux)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 00:58
S15	621	memory adj controller with RAM same (switch mux)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 01:12
S16	0	"tile.clm" and "bansal.xa"	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 01:24
S17	0	tile and bansal.xa.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 01:24
S18	8	tile and bansal.xp.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 01:24
S19	4,598,512	memory controller with (MUX Switch) with RAM	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 01:33
S20	220	memory adj controller with (MUX Switch) with RAM	US-PGPUB; USPAT;	OR	ON	2021/03/18 01:33

			EPO; IBM_TDB			
S21	103	memory adj controller with (MUX Switch) with DIMM	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 01:44
S22	30,028	(MUX switch) with RAM	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 01:59
S23	352	(MUX switch) with banks with RAM	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 01:59
S24	30,028	(MUX switch) with RAM	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 02:11
S25	426	memory adj controller same (MUX switch) with RAM	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 02:12
S26	25	power adj island and (MUX switch) with RAM	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 02:21
S27	64	DIMM with mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 03:07
S28	502	grundy.in.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 10:33
S29	426	memory adj controller same RAM with (switch mux)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 10:49

S30	4,750	controller same bank with (switch mux)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 10:55
S31	5,010	parallel with memory with bank	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 11:10
S32	686	parallel with memory with bank and mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 11:10
S33	3,316	parallel with memory with bank and (mux switch$3)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 11:10
S34	226	parallel with RAM with bank and mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 17:58
S35	1	parallel with RAM with bank with mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 17:58
S36	50	RAM with bank with mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 17:58
S37	2,070	RAM with mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 18:00
S38	209	RAM with mux with controller	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 18:00
S39	36	DIMM with mux with controller	US-PGPUB; USPAT;	OR	ON	2021/03/18 18:00

			EPO; IBM_TDB			
S40	184	DIMM with switch with controller	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 18:02
S41	336	pipelin$3 and bank with mux same controller	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/19 03:09
S42	556	controller with memory adj bank same (switch mux)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/19 03:17
S43	955	bank with select$3 with mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/19 03:26
S44	43	rank with select$3 with mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/19 03:49
S45	618	ram with select$3 with mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/19 03:53
S47	8	DIMM with mux with CS	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/23 17:51
S48	300	memory with mux with CS	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/23 17:55
S49	703	RAM with tiles and (mux switch)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/23 18:36

S50	121	RAM with tiles same2 (mux switch)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/23 18:36
S51	48	Die with mux with controller	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/23 18:39
S52	209	RAM with mux with controller	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/23 18:42
S53	369	MRAM with compar$3 with flash	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/23 18:44
S54	5,539	(switch mux) with parallel with memory	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/23 21:46
S55	437	(switch mux) with parallel with memory with (die chip plane dimm)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/23 21:47

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L23	13,642	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc. G11C5/04.cpc. G11C7/1072.cpc. G11C15/00.cpc.	USPAT	OR	ON	2021/03/25 03:03
L24	114	burst.clm. and CAS.clm. and latency.clm.	USPAT	OR	ON	2021/03/25 03:04
L25	29	L23 and L24	USPAT	OR	ON	2021/03/25 03:04

3/25/2021 3:06:42 AM
C:\Users\gbansal\Documents\EAST\Workspaces\16695020.wsp

Electronically filed June 17, 2021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jefferey C. SOLOMON	Confirmation No.:	7514
Serial No.:	16/695,020	Art Unit:	2139
Filed:	25-Nov-2019	Examiner:	BANSAL, Gurtej
For:	MEMORY MODULE WITH DATA BUFFERING	Attorney Docket No.:	129980-5023-US01

AMENDMENT UNDER 37 C.F.R. § 1.312

Mail Stop: Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is filed under 37 C.F.R. § 1.312 for the above identified patent application, and is filed after a Notice of Allowance dated March 30, 2020.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. 129980-5023-US01).

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Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory bus including address and control signal lines and data signal lines, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals, the set of input address and control signals including a plurality of input chip select signals and other input address and control signals, the plurality of input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value, the set of registered address and control signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals, the plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value, wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks correspond to ~~are configured to receive~~ respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices in one respective N-bit wide rank of the plurality of N-bit-wide ranks, wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the

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other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command; and

circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;

wherein data transfers through the circuitry are registered for an ~~additional~~ amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

2. (Original) The memory module of claim 1, wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus.

3. (Currently Amended) The memory module of claim 1, wherein the [[first]] burst of N-bit wide data signals includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein the set of consecutively transmitted data bits are successively transferred through the circuitry in response to the data buffer control signals.

4. (Currently Amended) The memory module of claim 1, wherein each of the memory devices is 4-bits wide, and wherein each of the plurality of ranks is 64-bits or 72-bits wide and includes 16 or 18 memory devices configured in pairs~~, and wherein each pair of 4-bit-wide memory devices are configured to simulate an 8-bit-wide memory device~~.

5. (Currently Amended) The memory module of claim 1, wherein the memory devices are organized in four ranks and the [[first]] set of input address and control signals include four chip select signals, one for each of the four ranks.

6. (Original) The memory module of claim 1, wherein the circuitry includes logic pipelines configurable to enable the data transfers between the memory devices and the memory bus through the circuitry.

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7. (Original) The memory module of claim 1, wherein the logic is further configured to report the overall CAS latency to the memory controller in response to a mode register set command received from the memory controller.

8. (Currently Amended) The memory module of claim 1, wherein the memory module has a specified data rate, and wherein the burst of N-bit wide data signals are transferred between the one of the plurality of N-bit wide ranks and the memory controller at the specified data rate.

9. (Original) The memory module of claim 1, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.

10. (Currently Amended) The memory module of claim 9, wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the one of the plurality of N-bit wide ranks is configured to receive or output a respective set of bits of the ~~first~~ burst of N-bit wide data signals on both edges of each of a respective set of data strobes.

11. (Currently Amended) The memory module of claim 1, wherein the circuitry includes data paths, and wherein the circuitry is configurable to enable the data paths in response to the data buffer control signals so that the burst of N-bit wide data signals are transferred via the data paths.

12. (Original) The memory module of claim 11, wherein the data paths are disabled when no data signals associated with any memory command are being transferred through the circuitry.

13. (Original) The memory module of claim 12, wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus.

14. (Original) The memory module of claim 12, wherein the memory module has a specified data rate, and wherein the burst of N-bit wide data signals are transferred through the data paths at the specified data rate.

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15. (Original) The memory module of claim 12, wherein the read or write command is a write memory command, wherein the burst of N-bit wide data signals include a respective series of write data bits received by the circuitry from a respective one of the data signal lines, and wherein the respective series of write data bits are successively transferred via a respective one of the data paths.

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REMARKS

This amendment is filed after the Notice of Allowance dated March 30, 2021, which allowed claims 1-15.

Claims 1, 3-5, 8, and 10-11 been amended to address minor issues of clarity. No new matter is added, and the amendments should not require additional search or examination.

The Examiner is invited to call the undersigned attorney at (650) 521-4828, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: June 17, 2021

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)

Customer No. 79141

Phone: (650) 521-4828

Petitioners
Ex. 1057, p. 303

Electronic Acknowledgement Receipt	
EFS ID:	43010800
Application Number:	16695020
International Application Number:	
Confirmation Number:	7514
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5023-US01
Receipt Date:	17-JUN-2021
Filing Date:	25-NOV-2019
Time Stamp:	03:19:38
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5023-US01_312_Amendment.pdf	123602 2550b35eec548731fdccc473a1708c1fc2338f2c	yes	6

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment after Notice of Allowance (Rule 312)	1	1
	Claims	2	5
	Abstract	6	6
Warnings:			
Information:			
	Total Files Size (in bytes):	123602	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Patent Application Fee Transmittal

Application Number:	16695020
Filing Date:	25-Nov-2019
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Filer:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023-US01

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1200	1200

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1200**

Electronic Acknowledgement Receipt	
EFS ID:	43143194
Application Number:	16695020
International Application Number:	
Confirmation Number:	7514
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5023-US01
Receipt Date:	30-JUN-2021
Filing Date:	25-NOV-2019
Time Stamp:	21:36:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1200
RAM confirmation Number	E20216TL37170395
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	129980-5023-US01_Issue-Fee-Payment_2021-06-30.pdf	311477 2cec4f25f4f23fa90754045 15a836ce46f670721	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30502 3020f0bcc9cbc4cd2290356da3453a24a02d5348	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	341979		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 03/30/2021
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Jamie J. Zheng	(Typed or printed name)
/Jamie J. Zheng/	(Signature)
2021-06-30	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/695,020	11/25/2019	Jefferey C. Solomon	129980-5023-US01	7514

TITLE OF INVENTION: MEMORY MODULE WITH DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	06/30/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
BANSAL, GURTEJ	2139	711-105000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 USCH Law, PC
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Netlist, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Irvine, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ☑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ☑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

☑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 60-3916

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Jamie J. Zheng/ Date 2021-06-30

Typed or printed name Jamie J. Zheng Registration No. 51167

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Petitioners
Ex. 1057, p. 310

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 03/30/2021

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER
BANSAL, GURTEJ

ART UNIT	PAPER NUMBER
2139	

DATE MAILED: 03/30/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/695,020	11/25/2019	Jefferey C. Solomon	129980-5023-US01	7514

TITLE OF INVENTION: MEMORY MODULE WITH DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	06/30/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

Petitioners
Ex. 1057, p. 311

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/695,020	11/25/2019	Jefferey C. Solomon	129980-5023-US01	7514

79141 7590 07/09/2021

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER
BANSAL, GURTEJ

ART UNIT	PAPER NUMBER
2139	

NOTIFICATION DATE	DELIVERY MODE
07/09/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com

Response to Rule 312 Communication	Application No.	Applicant(s)	
	16/695,020	Solomon et al.	
	Examiner	Art Unit	AIA (FITF) Status
	GURTEJ BANSAL	2139	No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☑ The amendment filed on 17 June 2021 under 37 CFR 1.312 has been considered, and has been:

a) ☐ entered.

b) ☑ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.

Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	

OK TO ENTER: /G.B/

Electronically filed June 17, 2021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jefferey C. SOLOMON	Confirmation No.:	7514
Serial No.:	16/695,020	Art Unit:	2139
Filed:	25-Nov-2019	Examiner:	BANSAL, Gurtej
For:	MEMORY MODULE WITH DATA BUFFERING	Attorney Docket No.:	129980-5023-US01

AMENDMENT UNDER 37 C.F.R. § 1.312

Mail Stop: Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is filed under 37 C.F.R. § 1.312 for the above identified patent application, and is filed after a Notice of Allowance dated March 30, 2020.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. 129980-5023-US01).

Petitioners
Ex. 1057, p. 314

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 8, 2021*	
				Application Number	*16/695,020*
				Filing Date	*November 25, 2019*
				First Named Inventor	*Jefferey C. Solomon*
				Art Unit	*2139*
				Examiner Name	*TBD*
Sheet	6	of	47	Attorney Docket Number	*129980-5023-US01*

Change(s) applied to document, /S.B./ 4/28/2021

	166.	7,007,175	2006-02-28	Chang et al.	
	167.	7,024,518	2006-04-04	Halbert et al.	
	168.	7,046,538	2006-05-16	Kinsley et al.	
	169.	7,047,361	2006-05-16	~~Phison Electronics Corp~~	Chong et al.
	170.	7,054,179	2006-05-30	Cogdill et al.	
	171.	7,065,626	2006-06-20	Schumacher et al.	
	172.	7,072,231	2006-07-04	Pax	
	173.	7,073,041	2006-07-04	Dwyer et al.	
	174.	7,078,793	2006-07-18	Ruckerbauer et al.	
	175.	7,093,066	2006-08-15	Klein	
	176.	7,120,727	2006-10-10	Lee et al.	
	177.	7,124,260	2006-10-17	LaBerge et al.	
	178.	7,127,584	2006-10-24	Thompson et al.	
	179.	7,130,308	2006-10-31	Haddock et al.	
	180.	7,130,952	2006-10-31	Nanki et al.	
	181.	7,133,960	2006-11-07	Thompson et al.	
	182.	7,133,972	2006-11-07	Jeddeloh	
	183.	7,142,461	2006-11-28	Janzen	
	184.	7,149,841	2006-12-12	LaBerge	
	185.	7,167,967	2007-01-23	Bungo et al.	
	186.	7,181,591	2007-02-20	Tsai	
	187.	7,191,302	2007-03-13	Usami	
	188.	7,200,021	2007-04-03	Raghuram	
	189.	7,225,303	2007-05-29	Choi	
	190.	7,227,910	2007-06-05	Lipka	
	191.	7,254,036	2007-08-07	Pauley et al.	
	192.	7,266,639	2007-09-04	Raghuram	
	193.	7,272,709	2007-09-18	Zitlaw et al.	
	194.	7,281,079	2007-10-09	Bains et al.	
	195.	7,286,436	2007-10-23	Bhakta et al.	
	196.	7,289,386	2007-10-30	Bhakta et al.	
	197.	7,334,150	2008-02-19	Ruckerbauer et al.	
	198.	7,346,750	2008-03-18	Ishikawa	
	199.	7,356,639	2008-04-08	Perego et al.	

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/25/2021

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 8, 2021*	
				Application Number	*16/695,020*
				Filing Date	*November 25, 2019*
				First Named Inventor	*Jefferey C. Solomon*
				Art Unit	*2139*
				Examiner Name	*TBD*
Sheet	5	of	47	Attorney Docket Number	*129980-5023-US01*

Change(s) applied to document, /S.B./ 4/28/2021

	132.	6,705,877	2004-03-16	Li et al.		
	133.	6,717,855	2004-04-06	Underwood		
	134.	6,717,885	2004-04-06	Lai		
	135.	6,721,843	2004-04-13	~~Lexar Media Inc~~ Estakhri		
	136.	6,721,860	2004-04-13	Klein		
	137.	6,738,880	2004-05-18	Lai et al.		
	138.	6,742,098	2004-05-25	Halbert et al.		
	139.	6,747,887	2004-06-08	Halbert et al.		
	140.	6,754,797	2004-06-22	Wu et al.		
	141.	6,785,189	2004-08-31	Jacobs et al.		
	142.	6,788,592	2004-09-07	Nakata et al.		
	143.	6,807,125	2004-10-19	Coteus et al.		
	144.	6,807,650	2004-10-19	Lamb et al.		
	145.	6,813,196	2004-11-02	Park et al.		
	146.	6,832,284	2004-12-14	Perego et al.		
	147.	6,832,303	2004-12-14	Tanaka		
	148.	6,834,014	2004-12-21	Yoo et al.		
	149.	6,854,042	2005-02-08	Karabatsos		
	150.	6,880,094	2005-04-12	LaBerge		
	151.	6,889,304	2005-05-03	Perego et al.		
	152.	6,912,615	2005-06-28	Nicolai		
	153.	6,912,628	2005-06-28	Wicki et al.		
	154.	6,925,028	2005-08-02	Hosokawa et al.		
	155.	6,944,694	2005-09-13	Pax		
	156.	6,948,084	2005-09-20	Manapat et al		
	157.	6,950,366	2005-09-27	Lapidus et al.		
	158.	6,954,281	2005-10-11	Fukuda et al		
	159.	6,961,281	2005-11-01	Wong et al.		
	160.	6,981,089	2005-12-27	Dodd et al.		
	161.	6,982,892	2006-01-03	Lee et al.		
	162.	6,982,893	2006-01-03	Jakobs		
	163.	6,990,043	2006-01-24	Kuroda et al.		
	164.	6,996,686	2006-02-07	Doblar et al.		
	165.	7,007,130	2006-02-28	Holman		

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/25/2021

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 8, 2021*	
				Application Number	***16/695,020***
				Filing Date	***November 25, 2019***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***TBD***
Sheet	3	of	47	Attorney Docket Number	***129980-5023-US01***

Change(s) applied to document, /S.B./ 4/28/2021

	64.	5,959,930	1999-09-28	Sakurai		
	65.	5,963,464	1999-10-05	Dell et al.		
	66.	5,966,736	1999-10-12	Gittinger et al.		
	67.	5,973,392	1999-10-26	Senba et al.		
	68.	5,974,493	1999-10-26	~~Mitsubishi Electric Corp~~	Okumura et al.	
	69.	6,011,710	2000-01-04	Wiggers		
	70.	6,018,787	2000-01-25	Ip		
	71.	6,044,032	2000-03-28	Li		
	72.	6,061,754	2000-05-09	Cepulis		
	73.	6,070,217	2000-05-30	Connolly et al.		
	74.	6,070,227	2000-05-30	Rokicki		
	75.	6,097,652	2000-08-01	Roh		
	76.	6,108,745	2000-08-22	Gupta et al.		
	77.	6,115,278	2000-09-05	Deneroff et al.		
	78.	6,134,638	2000-10-17	Olarig et al.		
	79.	6,141,245	2000-10-31	Bertin		
	80.	6,151,271	2000-11-21	Lee		
	81.	6,154,418	2000-11-28	Li		
	82.	6,154,419	2000-11-28	Shakkarwar		
	83.	6,173,357	2011-01-09	Ju		
	84.	6,185,654	2001-02-06	Van Doren		
	85.	6,188,641	2001-02-13	Uchida		
	86.	6,205,516	2001-03-20	Usami		
	87.	6,209,074	2001-03-27	Dell et al.		
	88.	6,223,650	2001-05-15	Johnson		
	89.	6,226,709	2001-05-01	Goodwin et al.		
	90.	6,226,736	2001-05-01	Niot		
	91.	6,233,650	2001-05-15	Johnson et al.		
	92.	6,247,088	2001-06-12	Seo et al.		
	93.	6,260,127	2001-07-10	Olarig et al.		
	94.	6,262,938	2001-07-17	Lee		
	95.	6,317,352	2001-11-13	Halbert et al.		
	96.	6,349,051	2002-02-19	~~Micron Technology Inc~~	Klein	
	97.	6,381,140	2002-04-30	Liao, Sheng-Chi		

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/25/2021

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 8, 2021*	
				Application Number	***16/695,020***
				Filing Date	***November 25, 2019***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***TBD***
Sheet	2	of	47	Attorney Docket Number	***129980-5023-US01***

	31.	5,532,954	1996-07-02	Bechtolsheim et al.	
	32.	5,537,584	1996-07-16	Miyai et al.	
	33.	5,541,448	1996-07-30	Carpenter	
	34.	5,559,970	1996-09-24	Sharma	
	35.	5,572,691	1996-11-05	Koudmani	
	36.	5,581,498	1996-12-03	Ludwig et al.	
	37.	5,590,071	1996-12-31	Kolor et al.	
	38.	5,602,999	1997-02-11	Hyatt; Gilbert P.	
	39.	5,617,559	1997-04-01	Le et al.	
	40.	5,630,096	1997-05-13	Zuravleff	
Change(s) applied to document, /S.B./ 4/28/2021	41.	5,638,534	1997-06-10	~~Samsung Electronics Co Ltd~~	Mote, Jr.
	42.	5,649,159	1997-07-15	Le et al.	
	43.	5,655,153	1997-08-05	~~EMC CORP~~ Sandorfi	
	44.	5,699,542	1997-12-16	Mehta et al.	
	45.	5,702,984	1997-12-30	Bertin et al.	
	46.	5,703,826	1997-12-30	Hush et al.	
	47.	5,717,851	1998-02-10	Yishay et al.	
	48.	5,724,604	1998-03-03	Moyer	
	49.	5,729,716	1998-05-17	Lee et al.	
	50.	5,745,914	1998-04-28	Connolly et al.	
	51.	5,764,590	1998-06-09	~~Mitsubishi Electric Corp~~	Iwamoto et al.
	52.	5,784,705	1998-07-21	Leung, Wingyu	
	53.	5,802,395	1998-09-01	Connolly et al.	
	54.	5,802,541	1998-09-01	Reed	
	55.	5,805,520	1998-09-08	Anglada et al.	
	56.	5,822,251	1998-10-13	Bruce et al.	
	57.	5,905,401	1999-05-18	Sher	
	58.	5,909,388	1999-06-01	~~Siemens Ag~~ Mueller	
	59.	5,926,827	1999-07-20	Dell et al.	
	60.	5,926,839	1999-07-20	~~IBM~~ Katayama	
	61.	5,953,215	1999-09-14	Karabatsos, Chris	
	62.	5,953,280	1999-09-14	Matsui	
	63.	5,958,025	1999-09-28	~~Nippon Electric Co~~ Sonobe	

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/25/2021

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 8, 2021*	
				Application Number	***16/695,020***
				Filing Date	***November 25, 2019***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***TBD***
Sheet	1	of	47	Attorney Docket Number	***129980-5023-US01***

Change(s) applied to document, /S.B./ 4/28/2021

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.[1]	Document Number Number - Kind Code[2]	Publication Date YYYY-MM-DD	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	4,218,740	1980-08-19	~~MOTOROLA INC~~ Bennett et al.	
	2.	4,249,253	1981-02-03	Gentili et al.	
	3.	4,368,515	1983-01-11	Nielsen	
	4.	4,392,212	1983-07-05	Miyasaka et al.	
	5.	4,571,676	1986-02-18	Mantellina et al.	
	6.	4,592,011	1986-05-27	Mantellina et al.	
	7.	4,633,429	1986-12-30	Lewandowski et al.	
	8.	4,670,748	1987-06-02	Williams	
	9.	4,706,214	1987-11-10	Mitsubishi Denki ~~Kabushiki Kaisha~~	Kassai
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Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/25/2021

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 41 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

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