Paper No. 2

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,

Petitioners,

v.

NETLIST, INC.,

Patent Owner.

Case IPR2023-01142
Patent 9,858,215

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,858,215

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EXHIBIT LIST

Exhibit #	Description
1001	U.S. Patent No. 9,858,215 (issued January 2, 2018)
1002	File History of U.S. Patent No. 9,858,215 (filed May 18, 2015)
1003	Declaration of Dr. Andrew Wolfe
1004	Curriculum Vitae of Dr. Andrew Wolfe
1005	U.S. Provisional Application No. 60/645,087 (filed Jan. 19, 2005)
1006	U.S. Provisional Application No. 60/588,244 (filed July 15, 2004)
1007	U.S. Provisional Application No. 60/550,668 (filed March 5, 2004)
1008	U.S. Provisional Application No. 60/575,595 (filed May 28, 2004)
1009	U.S. Provisional Application No. 60/590,038 (filed July 21, 2004)
1010	File History of U.S. Patent No. 7,286,436 (filed March 7, 2005)
1011	U.S. Patent No. 7,286,436 (issued Oct. 23, 2007)
1012	U.S. Patent No. 7,289,386 (issued Oct. 30, 2007)
1013	Affirmance of the Examiner's Decision on Reexamination of '386 Patent (Feb. 25, 2015)
1014	Reexamination Certificate for '386 Patent (Aug. 19, 2016)
1015	U.S. Patent No. 7,619,912 (issued Nov. 17, 2009)
1016	Decision on Reexamination of '912 Patent (June 6, 2016); Decision Under 37 C.F.R. § 41.77(f) (July 27, 2018); and Decision on Rehearing (Jan. 31, 2019)
1017	Reexamination Certificate for '912 Patent (Feb. 8, 2021)
1018	Petition for *Inter Partes* Review of U.S. Patent No. 7,619,912 (Feb. 17, 2022)

Exhibit #	Description
1019	Patent Owner Preliminary Response to Petition for *Inter Partes* Review of U.S. Patent No. 7,619,912 (July 21, 2022)
1020	Declaration of Michael C. Brogioli, Ph.D. in Support of Patent Owner Preliminary Response to Petition for *Inter Partes* Review of U.S. Patent No. 7,619,912 (July 21, 2022)
1021	Reply to Patent Owner Preliminary Response to Petition for *Inter Partes* Review of U.S. Patent No. 7,619,912 (Aug. 26, 2022)
1022	Sur-Reply to Patent Owner Preliminary Response to Petition for *Inter Partes* Review of U.S. Patent No. 7,619,912 (Sept. 9, 2022)
1023	Decision Granting Institution of *Inter Partes* Review of U.S. Patent No. 7,619,912 (Oct. 19, 2022)
1024	Patent Owner's Request for Rehearing of Decision Granting Institution of *Inter Partes* Review of U.S. Patent No. 7,619,912 (Nov. 2, 2022)
1025	Order of *Sua Sponte* Director Review of Decision Granting Institution of *Inter Partes* Review of U.S. Patent No. 7,619,912 (Jan. 5, 2023)
1026	U.S. Patent No. 7,864,627 (issued Jan. 4, 2011)
1027	Decision on Appeal of Reexamination of '627 Patent (May 30, 2016); Decision Under 37 C.F.R. § 41.77(f) (May 31, 2018)
1028	Reexamination Certificate for '627 Patent (Nov. 5, 2018)
1029	U.S. Patent No. 8,756,364 (issued June 17, 2014)
1030	IPR2017-00549 Final Written Decision ('364 Patent) (May 3, 2018)
1031	IPR Certificate for '364 Patent (May 26, 2020)
1032	U.S. Patent No. 7,532,537 (issued May 12, 2009)
1033	IPR2017-00667 Final Written Decision ('537 Patent) (July 18, 2018)

Exhibit #	Description
1034	IPR2017-00668 Final Written Decision (’537 Patent) (July 18, 2018)
1035	IPR Certificate for ’537 Patent (Apr. 27, 2020)
1036	U.S. Patent No. 7,636,274 (issued Dec. 22, 2009)
1037	Decision on Appeal of Reexamination of ’274 Patent (May 9, 2017)
1038	Reexamination Certificate for ’274 Patent (Nov. 5, 2018)
1039	U.S. Patent No. 7,881,150 (issued Feb. 1, 2011)
1040	IPR2014-00882 Final Written Decision on Remand (’150 Patent) (March 29, 2018)
1041	IPR2014-01011 Final Written Decision on Remand (’150 Patent) (March 29, 2018)
1042	IPR2015-01020 Final Written Decision (’150 Patent) (Sept. 28, 2016)
1043	IPR Certificate for ’150 Patent (Mar. 6, 2019)
1044	File History of U.S. Patent No. 7,916,574 (filed Nov. 29, 2010)
1045	U.S. Patent No. 7,916,574 (issued Mar. 29, 2011)
1046	U.S. Patent No. 8,081,536 (issued Dec. 20, 2011)
1047	IPR2014-00883 Final Written Decision on Remand (’536 Patent) (March 29, 2018)
1048	IPR2015-01021 Final Written Decision (’536 Patent) (Sept. 28, 2016)
1049	IPR Certificate for ’536 Patent (Mar. 11, 2019)
1050	File History of U.S. Patent No. 8,516,188 (filed Nov. 1, 2011)
1051	U.S. Patent No. 8,516,188 (issued Aug. 20, 2013)

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1052	File History of U.S. Patent No. 9,037,774 (filed Aug. 20, 2013)
1053	U.S. Patent No. 9,037,774 (issued May 19, 2015)
1054	File History of U.S. Patent No. 10,489,314 (filed Dec. 28, 2017)
1055	U.S. Patent No. 10,489,314 (issued Nov. 26, 2019)
1056	Decisions Granting Institution of *Inter Partes* Reviews of U.S. Patent No. 10,489,314 (Nov. 1, 2022)
1057	File History of U.S. Patent No. 11,093,417 (filed Nov. 25, 2019)
1058	U.S. Patent No. 11,093,417 (issued Aug. 17, 2021)
1059	File History of U.S. Patent Application No. 17/403,832 (filed Aug. 16, 2021)
1060	JEDEC JESD79 standard for DDR SDRAM (June 2000)
1061	[intentionally omitted]
1062	JEDEC JESD21-C design specification for DDR SDRAM Registered DIMM (January 2002)
1063	[intentionally omitted]
1064	JEDEC JESD79-2 standard for DDR2 SDRAM (Sept. 2003)
1065	Declaration of Julie Carlson (JESD79-2)
1066	JEDEC JESD21-C design specification for DDR2 SDRAM Registered DIMM, Rev. 3.2 (Oct. 4, 2005)
1067	[intentionally omitted]
1068	Harold S. Stone, Microcomputer Interfacing (1982)
1069	Bruce Jacob, *Synchronous DRAM Architectures, Organizations, and Alternative Technologies* (Dec. 10, 2002)

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1070	Bruce Jacob et al., Memory Systems: Cache, DRAM, Disk (2008)
1071	U.S. Patent No. 7,363,422 to Perego et al. (filed Jan. 28, 2004)
1072	U.S. Patent No. 7,155,627 to Matsui (filed Aug. 22, 2003)
1073	U.S. Patent Application Publication No. 2006/0277355 to Ellsberry et al. (filed June 1, 2005)
1074	IPR2018-00362 Final Written Decision (June 27, 2019) ('907 Patent)
1075	U.S. Patent No. 9,606,907 (all claims cancelled)
1076	Decision Granting Institution of *Inter Partes* Review of U.S. Patent No. 10,949,339 (Oct. 19, 2022) (child of U.S. Patent No. 9,606,907, Exhibit 1075)
1077	U.S. Patent Application Publication No. 2002/0112119 to Halbert et al. (published Aug. 15, 2002)
1078	U.S. Patent No. 7,024,518 to Halbert et al. (filed Mar. 13, 2002)
1079	U.S. Patent Application Publication No. 2006/0117152 to Amidi et al. (filed Jan. 5, 2004)
1080	U.S. Patent No, 8,250,295 to Amidi et al. (filed Jan. 5, 2004)
1081	U.S. Patent. No. 5,513,135 to Dell et al. (issued Apr. 30, 1996)
1082	U.S. Patent Application Publication No. 2003/0039151 to Matsui (published Feb. 27, 2003)
1083	[intentionally omitted]
1084	[intentionally omitted]
1085	Amended Complaint in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. filed Aug. 15, 2022)
1086	Waiver of Service in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. filed Aug. 31, 2022)

Exhibit #	Description
1087	[intentionally omitted]
1088	Amended Complaint in *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:22-cv-00294 (E.D. Tex. filed Aug. 15, 2022)
1089	Micron's Answer in *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:22-cv-00294 (E.D. Tex. filed Sept. 7, 2022)
1090	[intentionally omitted]
1091	*Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation* (June 21, 2022)
1092	Federal Court Management Statistics (Mar. 31, 2022), *available at* <https://www.uscourts.gov/statistics/table/na/federal-court-management-statistics/2022/03/31-1>

CLAIM LISTING

Ref. #	Listing of Challenged Claims
1.a.1	1. A memory module
1.a.2	operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller,
1.a.3	the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst,
1.a.4	the memory module comprising:
1.b	a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;
1.c	a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command;
1.d.1	a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank,
1.d.2	wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and
1.d.3	wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command;
1.e	a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus; and

Ref. #	Listing of Challenged Claims
1.f.1	logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data bust between the at least one first memory integrated circuit and the memory controller through the buffer,
1.f.2	wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.
2	The memory module of claim 1, wherein the buffer is configured to isolate both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory controller.
3	The memory module of claim 1, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.
4	The memory module of claim 1, further comprising an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits.
5	The memory module of claim 1, wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits.
6	The memory module of claim 1, further comprising determining a latency value, wherein the communication of the first data burst between the at least one first memory integrated circuit and the memory controller is enabled in accordance with the latency value.

Ref. #	Listing of Challenged Claims
7	The memory module of claim 1, wherein the memory module is further coupled to the memory controller using an on-die-termination (ODT) bus, wherein each of the plurality of memory devices includes an ODT circuit, the memory module further comprising a termination circuit external to any of the plurality of memory devices, wherein the termination circuit is coupled to the ODT bus and to the ODT circuit of at least one of the plurality of memory devices, wherein the termination circuit is configured to provide external termination of the at least one of the plurality of memory devices in response to an ODT signal on the ODT bus, and wherein the ODT circuit in the at least one of the plurality of memory devices is disabled.
8	The memory module of claim 1, wherein the buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the first data burst or the second data burst through the buffer.
9	The memory module of claim 1, wherein the first memory command includes at least one first chip select signal and the second memory command includes at least one second chip select signal.
10	The memory module of claim 9, wherein the memory module produces at least third and fourth chip select signals in response to the first memory command, the third chip select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the fourth chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.

Ref. #	Listing of Challenged Claims
11	The memory module of claim 10, wherein the memory module produces at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first [sic: second] memory command, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an active value to cause the at least one second memory integrated circuit to receive or output data signals in response to the second memory command.
12	The memory module of claim 1, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory bus, and wherein the buffer is configured to prevent the first burst of data strobe signals and the second burst of data strobe signals from colliding with each other.
13	The memory module of claim 12, wherein each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval, and wherein the buffer is configured to combine the first burst of data strobe signals into a combined burst of data strobe signals that does not include the post-amble interval of the first burst of data strobe signals and the preamble interval of the second burst of data strobe signals.
14	The memory module of claim 1, wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is selected to communicate data with the memory controller.

Ref#	Listing of Challenged Claims
15	The memory module of claim 14, the at least one of the circuit components is configured to provide the first data path in response to the first control signals, and is configured to provide the second data path in response to the second control signals.
16	The memory module of claim 1, wherein the logic is configured to enable the communication of the first data burst between the at least one first memory integrated circuit and the memory controller in accordance with a latency value.
17	The memory module of claim 16, wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the first data burst through the buffer.
18	The memory module of claim 16, wherein the logic is further configured to determine the latency value.
19	The memory module of claim 16, wherein the logic is further configured to enable the communication of the second data burst between the at least one second memory integrated circuit and the memory controller in accordance with the latency value.
20	The memory module of claim 19, wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the second data burst through the buffer.
21.a	A method of operating a memory module coupled to a memory controller via a memory bus, the memory module comprising memory integrated circuits arranged in ranks and mounted on a printed circuit board having a plurality of edge connections coupled to the memory bus, the memory integrated circuits including at least one first memory integrated circuits including at least one second memory integrated circuit in a second rank, the method comprising:
21.b	receiving at one or more circuits coupled to the printed circuit board a first set of input command and address signals representing a first memory command from the memory controller via the memory bus, the first memory command to cause the memory module to receive or output a first data burst;

Ref. #	Listing of Challenged Claims
21.c	generating a first set of output command and address signals in response to the first set of input command and address signals, the first set of output command and address signals selecting the first rank to receive or output the first data burst;
21.d	receiving at the one or more circuits a second set of input command and address signals representing a second memory command from the memory controller via the memory bus, the second memory command to cause the memory module to receive or output a second data burst;
21.e	generating a second set of output command and address signals in response to the second set of input command and address signals, the second set of output command and address signals selecting the second rank to receive or output the second data burst;
21.f	in response to the first memory command, providing first control signals to a buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer; and
21.g	in response to the second memory command, providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.
22	The method of claim 21, further comprising isolating the at least one first memory integrated circuit and the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory system.

Ref. #	Listing of Challenged Claims
23	The method of claim 21, wherein the first set of input command and address signals include at least one input chip-select signal, the method further comprising generating a first chip select signal and a second chip select signal in response to the first set of input command and address signals, the first chip-select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the second chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.
24	The method of claim 21, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of the memory integrated circuits.
25	The method of claim 21, further comprising reporting an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of the memory integrated circuits.
26	The method of claim 21, wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is caused to communicate data with the memory controller.
27	The method of claim 21, wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits.

Ref. #	Listing of Challenged Claims
28	The method of claim 21, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein the memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory bus, the method further comprising combining the first burst of data strobe signals and the second burst of data strobes to form a third burst of data strobe signals on the memory bus.
29	The method of claim 28, wherein each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval, and wherein the third burst of data strobes does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals.

I. PETITIONERS' MANDATORY NOTICES

A. Real Parties-in-Interest (37 C.F.R. §42.8(b)(1))

The real parties in interest are the Petitioners Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC.

B. Related Matters (37 C.F.R. §42.8(b)(2))

The following judicial or administrative matters would affect, or be affected by, a decision in this proceeding concerning U.S. Patent No. 9,858,215.

The following proceedings are currently pending:

- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. amended complaint filed Aug. 15, 2022)
- *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:22-cv-00294 (E.D. Tex. amended complaint filed Aug. 15, 2022)
- *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2022-00615 (U.S. Patent No. 7,619,912)
- *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2023-00203 (U.S. Patent No. 7,619,912)
- *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2022-00639 (U.S. Patent No. 10,949,339)
- *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2022-00744 (U.S. Patent No. 10,489,314)

- *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2022-00745 (U.S. Patent No. 10,489,314)
- *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2023-00454 (U.S. Patent No. 11,093,417)
- U.S. Application No. 17/403,832

The following proceedings have concluded:

- *Inter partes* Reexamination Nos. 95/000,578; 95/000,579; and 95/001,339 of U.S. Patent No. 7,619,912
- *Inter partes* Reexamination Nos. 95/000,546 and 95/000,577 of U.S. Patent No. 7,289,386
- *Inter partes* Reexamination No. 95/001,758 of U.S. Patent No. 7,864,627
- *Inter partes* Reexamination No. 95/001,337 of U.S. Patent No. 7,636,274
- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00549 (U.S. Patent No. 8,756,364)
- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00667 (U.S. Patent No. 7,532,537)
- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00668 (U.S. Patent No. 7,532,537)

- *Diablo Technologies, Inc. v. Netlist, Inc.*, IPR2014-00882 (U.S. Patent No. 7,881,150)
- *Diablo Technologies, Inc. v. Netlist, Inc.*, IPR2014-01011 (U.S. Patent No. 7,881,150)
- *SanDisk Corp. v. Netlist, Inc.*, IPR2015-01020 (U.S. Patent No. 7,881,150)
- *Diablo Technologies, Inc. v. Netlist, Inc.*, IPR2014-00883 (U.S. Patent No. 8,081,536)
- *SanDisk Corp. v. Netlist, Inc.*, IPR2015-01021 (U.S. Patent No. 8,081,536)
- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2018-00362 (U.S. Patent No. 9,606,907)
- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2018-00363 (U.S. Patent No. 9,606,907)

C. Lead and Back-up Counsel (37 C.F.R. §42.8(b)(3))

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D. Service Information (37 C.F.R. §42.8(b)(4))

Service information is provided in the designation of counsel above. Petitioners consents to service of all documents via electronic mail to Winston-IPR-NetList@winston.com.

II. INTRODUCTION

Petitioners respectfully request trial on claims 1-29 of U.S. Patent No. 9,858,215 ("215 Patent") (EX1001) based on grounds not considered during prosecution.

III. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW

A. Standing (§42.104(a))

The 215 Patent is available for IPR and Petitioners are not barred or estopped from requesting IPR on the grounds identified below.

B. Identification of Challenge (§42.104(b))

Petitioners challenge claims 1-29 of the 215 Patent as follows:

Ground	Claims Challenged	35 U.S.C.	References
1	1-29	§103(a)	Perego + JESD79-2
2	1-29		Ground 1 + Ellsberry
3	1-29		Ground 1 + Halbert
4	1-29		Ground 1 + Matsui2

Petitioners' proposed claim constructions and the precise reasons why the claims are unpatentable are provided below. The evidence relied upon is listed above, beginning on page viii.

IV. RELEVANT INFORMATION CONCERNING THE CONTESTED PATENT

A. Effective Filing Date of the 215 Patent: No Earlier Than July 1, 2005

The prior art in Grounds 1, 3, and 4 (Perego, JESD79-2, Halbert, and Matsui2) all predate March 5, 2004, the filing date of the 215 Patent's earliest provisional application. But Ellsberry (Ground 2 only) is also prior art because the

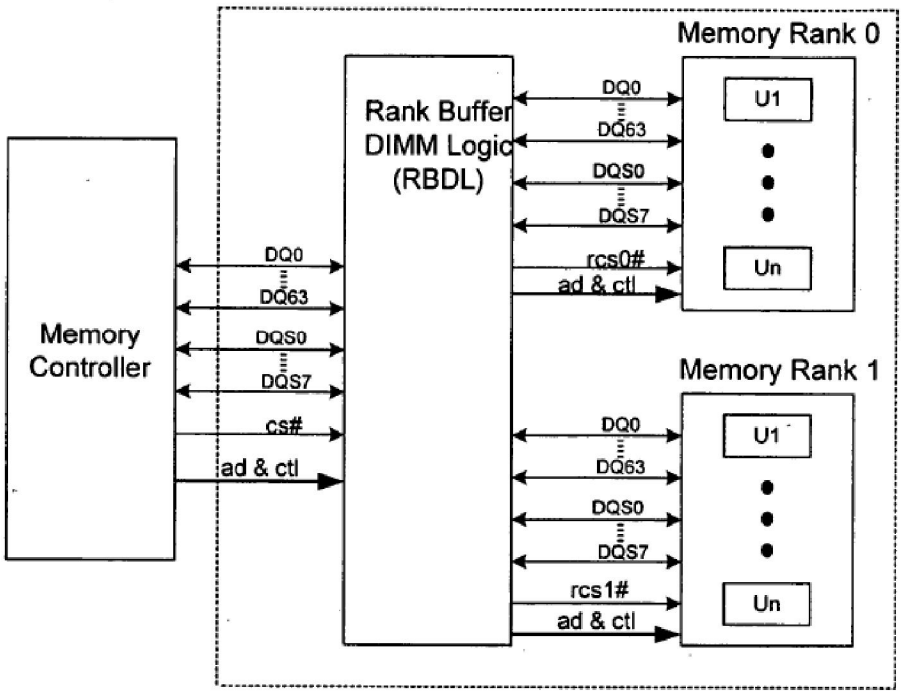
215 Patent's claims lack §112 support from any application filed before July 1, 2005, the filing date of the continuation-in-part application that resulted in U.S. Patent No. 7,289,386 ("386 Patent") (EX1012). EX1003, ¶¶51-67.

To secure the 215 Patent, Netlist amended independent claims 1 and 21 (and thus all claims) to require "provid[ing] [first/second] control signals to the ***buffer*** to enable communication of the [first/second] data burst between the at least one [first/second] memory integrated circuit and the memory controller through the ***buffer***[.]"[1] EX1002, pp.390-91, 393, 513; EX1001, 37:51-62, 40:17-27. However, no application filed prior to July 1, 2005 provided §112 support for these limitations. EX1003, ¶¶58-66.

Of the five provisional applications and the one non-provisional application filed prior to July 1, 2005, only one provisional application (U.S. Provisional Application No. 60/645,087 ("087 Provisional") (EX1005)) discloses a "Buffer" (RBDL) through which data (DQ0-DQ63) is communicated:

[1] All emphasis in quotes, and color highlighting in figures, has been added unless otherwise noted.

FIGURE 1:



Block Diagram: Rank Buffered DIMM Memory Sub-system

EX1005, Fig.1; EX1003, ¶¶58-60. But the 087 Provisional fails to disclose different first/second control signals to the buffer for enabling the communication of data bursts through the buffer in response to memory commands. EX1003, ¶61. The 087 Provisional does not mention any "data burst" or "control signals," much less the specific control signals required by the claims. *Id.* The 087 Provisional also does not name all the inventors listed on the 215 Patent. EX1005, p.1.

Although the 087 Provisional refers to "a data path multiplexer/demultiplexer" that provides separate DQ/DQS paths for each rank, it fails to disclose how the multiplexer/demultiplexer specifically enables data bursts through the data buffer in response to memory commands, what its control signals

are, and how those control signals differ for the first/second memory commands. EX1005, [0005], [0008], [0017]; EX1003, ¶62. And a POSITA would have recognized that the buffer need not use different first/second control signals, even if the second memory commands are directed to different ranks, because, for example, the data could be sent to both of the ranks, and a chip-select signal (e.g., rcs0#, rcs1#) could be used to target one of those ranks. EX1003, ¶¶63-64 (citing EX1005, [0009], [0012], Fig.1; EX1064, p.6). A POSITA would have also recognized that data transfer through the buffer does not necessarily happen in response to memory commands as required by the 215 Patent claims and instead could be controlled by other means, such as the "preamble" on the DQS strobe lines. EX1003, ¶65 (citing EX1064, pp.26 (t_{RPRE}), 30 (t_{WPRE}), 65).

Although the claims of the 215 Patent are obvious in light of the prior art, as explained below, that does not mean the 087 Provisional in light of that prior art provides §112 support for the claims of the 215 Patent: "[A] description that merely renders the invention *obvious* does not satisfy the [written description] requirement[.]" *Ariad Pharms., Inc. v. Eli Lilly & Co*., 598 F.3d 1336, 1352 (Fed. Cir. 2010) (en banc); *see also Rivera v. ITC*, 857 F.3d 1315, 1322 (Fed. Cir. 2017).

Accordingly, the claims of the 215 Patent are not entitled to a priority date before July 1, 2005, making Ellsberry prior art for Ground 2.

B. Person of Ordinary Skill in the Art ("POSITA")

A POSITA in the field of the 215 Patent in 2004 or 2005 would have had an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field. EX1003, ¶48. Additional training can substitute for educational or research experience, and vice versa. *Id.* A POSITA would have been familiar with various standards of the day including the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with the memory controller of a computer system. *Id.* Specifically, he or she would have been knowledgeable about the JEDEC DDR and DDR2 SDRAM standards used to standardize the functioning of memory devices, and the JEDEC 21-C standard used to standardize different possibilities for the physical layout of memory devices on a module as well as different possibilities for density and organization of the memory devices to achieve a given memory capacity. *Id.*; *see also id.* ¶¶49-50 (citing EX1001, 5:63-6:11, 21:7-22:7, 34:26-33 (referring to JEDEC standards); EX1060, EX1062, EX1064, EX1066). He or she would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs (Application-Specific Integrated Circuits) and CPLDs (Complex Programmable

Logic Devices) and more low-level circuits such as tri-state buffers, flip flops and registers. *Id.* ¶48.

C. Background Technology

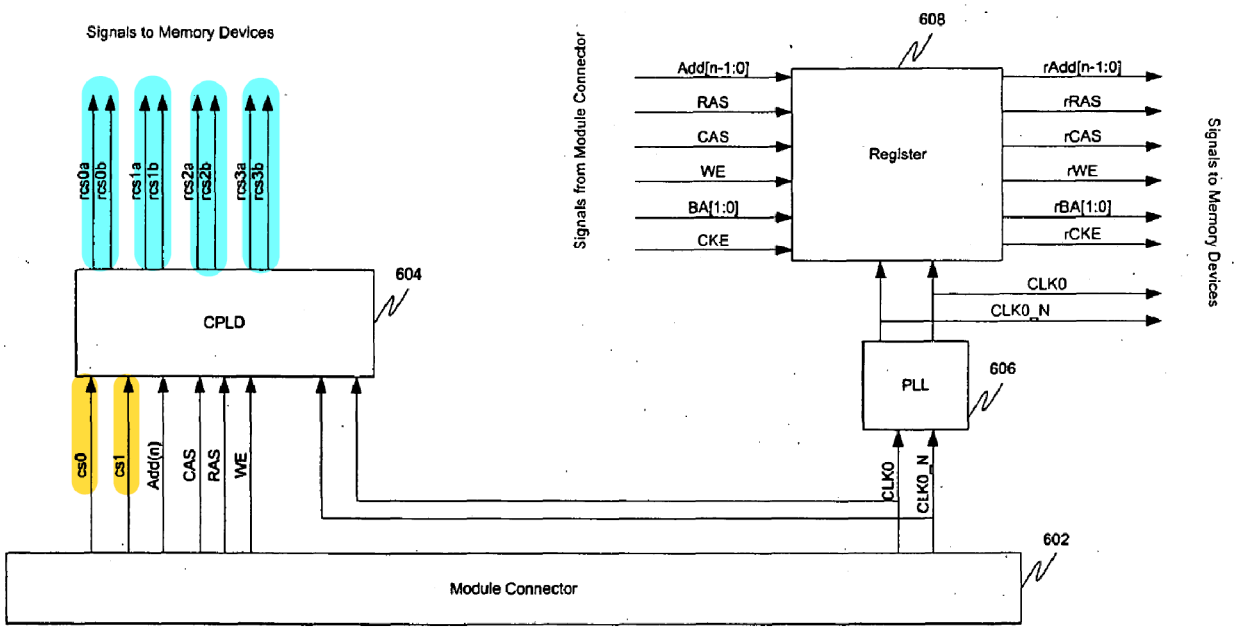
1. JEDEC Standards

"For over 50 years, JEDEC has been the global leader in developing and publishing open standards for the microelectronics industry." EX1065, ¶4. The 215 Patent refers to various JEDEC standards, including for RDIMM memory modules and DDR SDRAM memory devices. EX1001, 5:63-6:11, 21:7-22:7, 34:26-33. A POSITA would have been familiar with these JEDEC standards. EX1003, ¶¶169-170; EX1060 (DDR); EX1062 (RDIMM for DDR); EX1064 (DDR2); EX1066 (RDIMM for DDR2). The prior art also refers to these JEDEC standards. *Id.* (citing EX1071, 3:67-4:3, 8:1-9, 10:54-59; EX1073, [0046], [0050]).

2. Rank Multiplication

A POSITA also would have been familiar with "rank multiplication," which permitted replacing one rank of expensive high-density memory with two or more ranks of less expensive low-density memory without any change to the overall performance or memory capacity of the memory module — thus enabling significant cost savings. EX1003, ¶¶171-174; EX1079, ¶[0008]; EX1001, 13:51-14:4 ("cost savings can be significant").

A POSITA would have understood how to implement rank multiplication. EX1003, ¶172. For example, Amidi (EX1079), which is prior art, teaches that rank multiplication involves mapping address signals (e.g., Add(n)) and chip-select signals (e.g., cs0 and cs1, yellow, for two ranks of high-density memory devices) received from a system memory controller complying with the JEDEC standard into *more* chip-select signals (e.g., rcs0 to rcs3, blue) to control the higher number of ranks (e.g., four ranks) of less expensive, lower density memory devices on the memory module:



Row Address Decoding
FIG.6A

EX1079, [0041], [0050]-[0052], FIG. 6A; EX1003, ¶172. Another example of prior art that teaches rank multiplication is Ellsberry, discussed below (pp.20-22). EX1003, ¶173.

Given the significant cost savings from rank multiplication, POSITAs were motivated to implement the technique in a wide range of memory modules. EX1003, ¶¶171, 174.

D. The 215 Patent

1. Technical Overview

The 215 Patent concerns "rank multiplication," discussed directly above. EX1003, ¶¶68-73. The 215 Patent purports to describe "devices and methods for improving the performance, the memory capacity, or both, of memory modules." EX1001, 1:42-45. As shown below, a memory module (10) includes "a circuit 40 [red] electrically coupled to the plurality of memory devices 30 [green, blue] and configured to be electrically coupled to the memory controller 20 of the computer system." *Id.*, 5:24-27, Fig.1 (below).

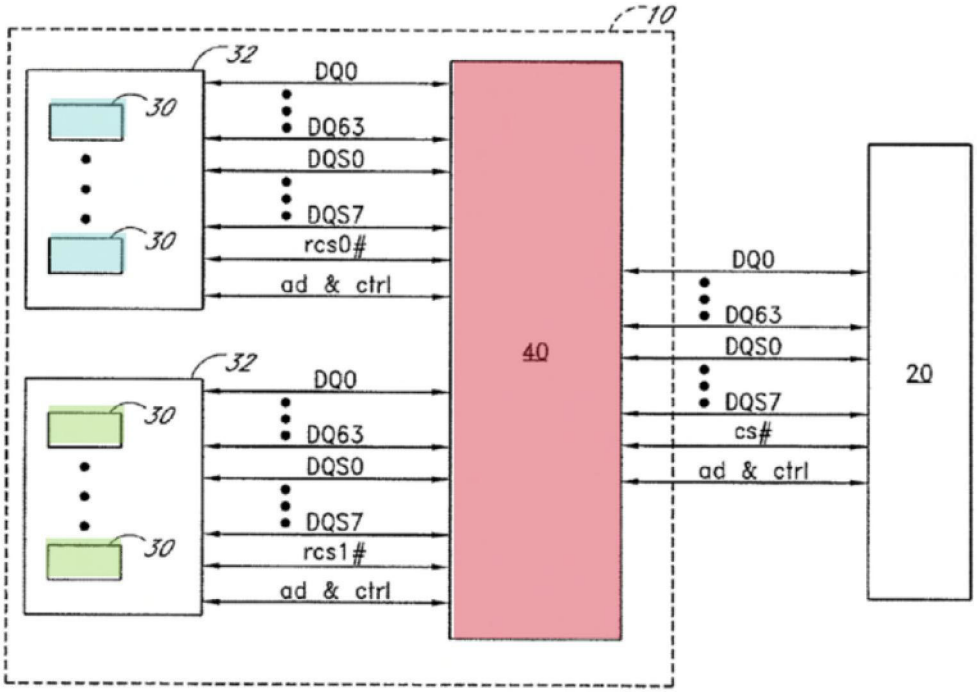


FIG. 1

"DRAM devices of a memory module are generally arranged as ranks or rows of memory" (e.g., the two ranks 32, green and blue, in Figure 1 above). *Id.*, 2:41-45, 6:30-34, 12:13-17, Fig.1. "[T]he ranks...are selected or activated by address and command signals," including "rank-select signals [(cs#)], also called chip-select signals," *id.*, 2:59-63, which are JEDEC-standard signals for DDR (sometimes called DDR-1) and DDR-2 memory devices, EX1003, ¶69; EX1060, p.7; EX1064, p.6. The 215 Patent's embodiments are compatible with such memory devices. EX1001, 6:4-8, 21:7-10.

The 215 Patent purportedly improves a memory module's capacity because the "circuit 40 selectively isolates one or more of the loads of the memory devices from the computer system...[and] comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module 10." EX1001, 5:24-32, Fig.1 (above); *see also id.*, 9:17-64. The computer system sees a memory module with higher-density memory devices (a system memory domain), while the physical configuration of the module (a physical memory domain) is different. EX1003, ¶71; EX1001, 15:42-46. As shown above in Figure 1, the memory controller (20) issues commands to a single "virtual" rank using a single chip-select signal ("cs#"), while the module actually has two ranks, each having its own chip-select signals ("rcs0#" and "rcs1#"). EX1003, ¶71. Signal collision is prevented by selectively connecting the system data bus to only one of the ranks that form the "virtual" higher density memory device. *Id.*, ¶72; EX1001, 12:5-43, Fig.7.

When the buffer circuit (40) registers the data transfers, an extra clock cycle is added to the natural CAS latency of the individual memory devices ("equivalent to a registered DIMM") and "advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices 30 from the memory controller 20." EX1001, 20:22-46; EX1003, ¶73.

2. Prosecution History

During prosecution of the 215 Patent, the Examiner never issued a rejection. *See generally* EX1002. Instead, the claims were allowed after amendments following Examiner interviews. EX1003, ¶¶112-116; EX1002, pp.280-94, 389-98, 412-36.

The 215 Patent is related to a number of earlier applications. EX1003, ¶¶74-120. Hundreds of claims from those earlier applications, all related to "rank multiplication," have been canceled in recent years as a result of reexaminations and IPRs. *Id.* ¶¶89-95, 99, 171 (citing EX1012-EX1017, EX1026-EX1043, EX1046-EX1049). In addition, IPRs were recently instituted against the 912 and 314 patents, which are in the same family as the 215 Patent. *See* EX1023;[2] EX1056, pp.22, 50.

V. OVERVIEW OF THE PRIOR ART

A. Perego (EX1071)

U.S. Patent No. 7,363,422 ("Perego"), filed January 28, 2004, and published September 23, 2004, is prior art under §102(a), (e). EX1071; EX1003, ¶135. Perego teaches a memory system 305 including a memory controller 310 connected to multiple buffered memory modules 330a-330n, such as memory module 340,

[2] This decision is being reviewed. EX1024-EX1025.

which includes a buffer device (350, red) and multiple groups of memory devices (360, green and blue). EX1071, Abstract, Fig.3B, 4:63-5:15; EX1003, ¶137.

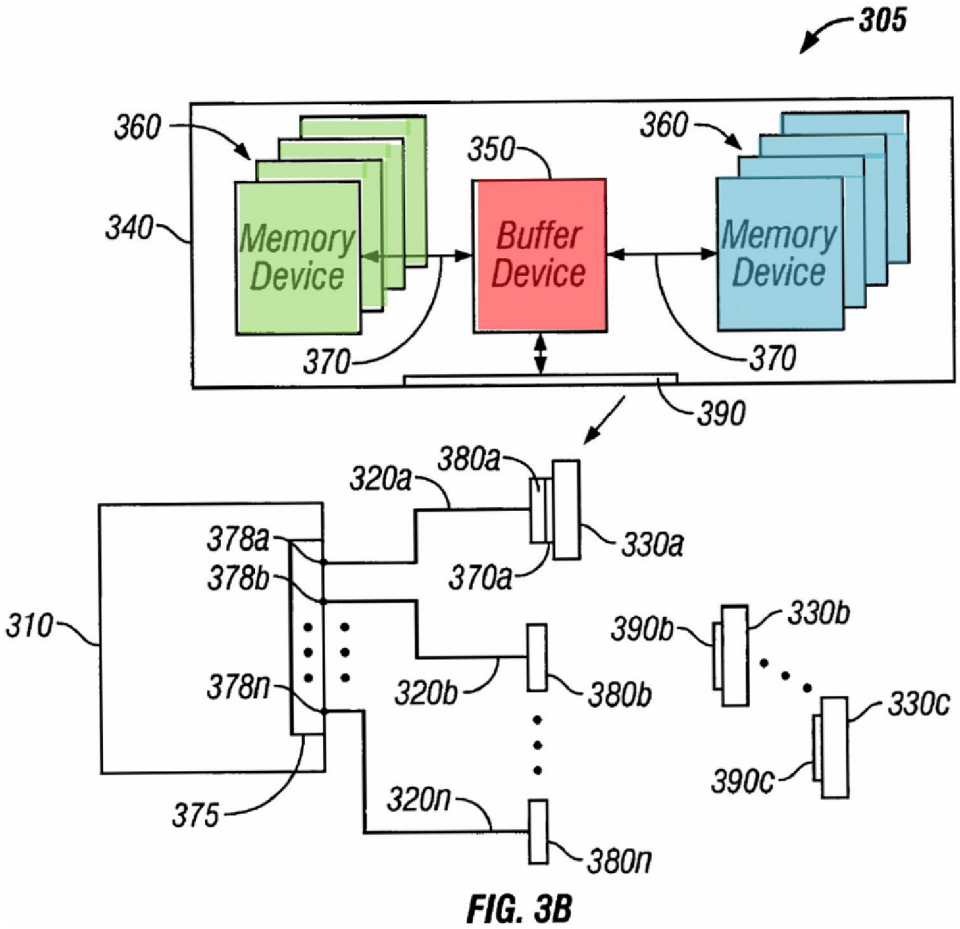


FIG. 3B

EX1071, Fig.3B. "Buffer device 350 provides a high degree of system flexibility. New generations of memory devices may be phased in with controller 310.... Similarly, new generations of controllers may be phased in...while retaining backward compatibility with existing generations of memory devices." *Id.*, 6:34-

43; *see also id.* Fig.3C (below, showing configurable width buffered module 395); EX1003, ¶¶138-139.

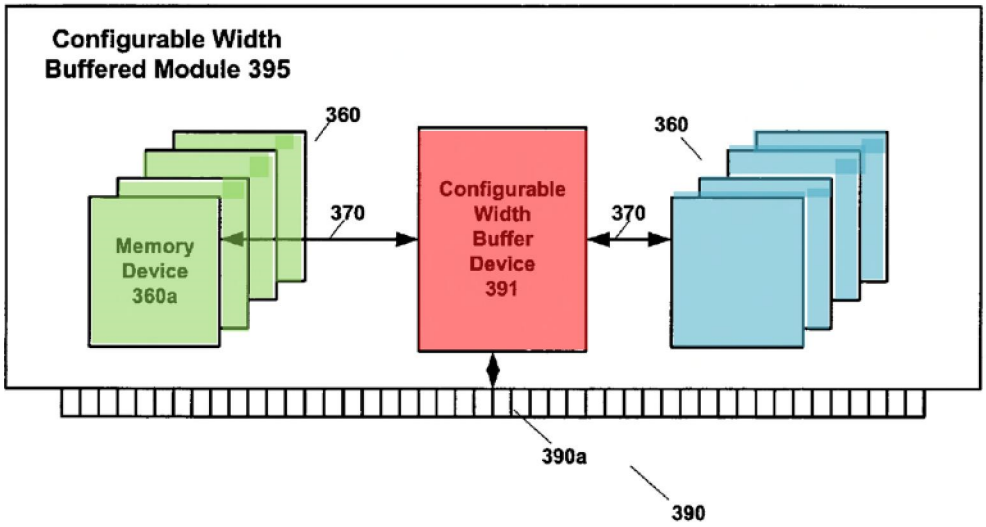


Fig. 3C

The buffer device (red, above and below) includes programmable interfaces 520a and 520b, which accommodate different numbers and types of memory devices, while configurable width interface 590 communicates with the memory controller. *Id*., 13:6-10, 13:60-14:15; EX1003, ¶140.

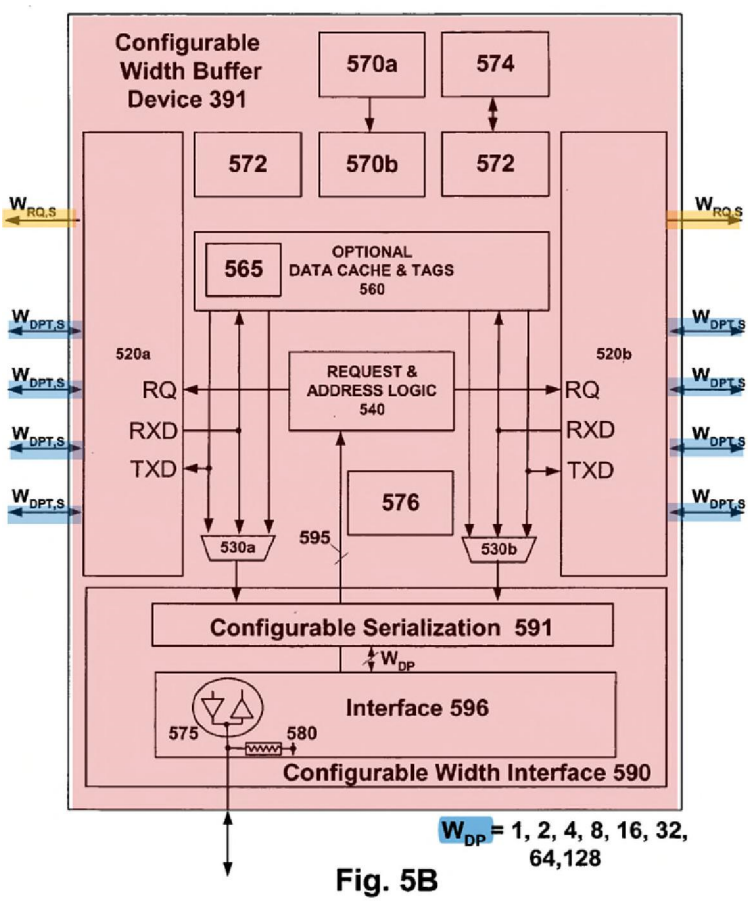


Fig. 5B

EX1071, Fig.5B. Configurable width interface 590 can include two input and output latches 597f-m (blue, below) for each data connection. *Id.*, 17:22-26, 17:61-67; EX1003, ¶141.

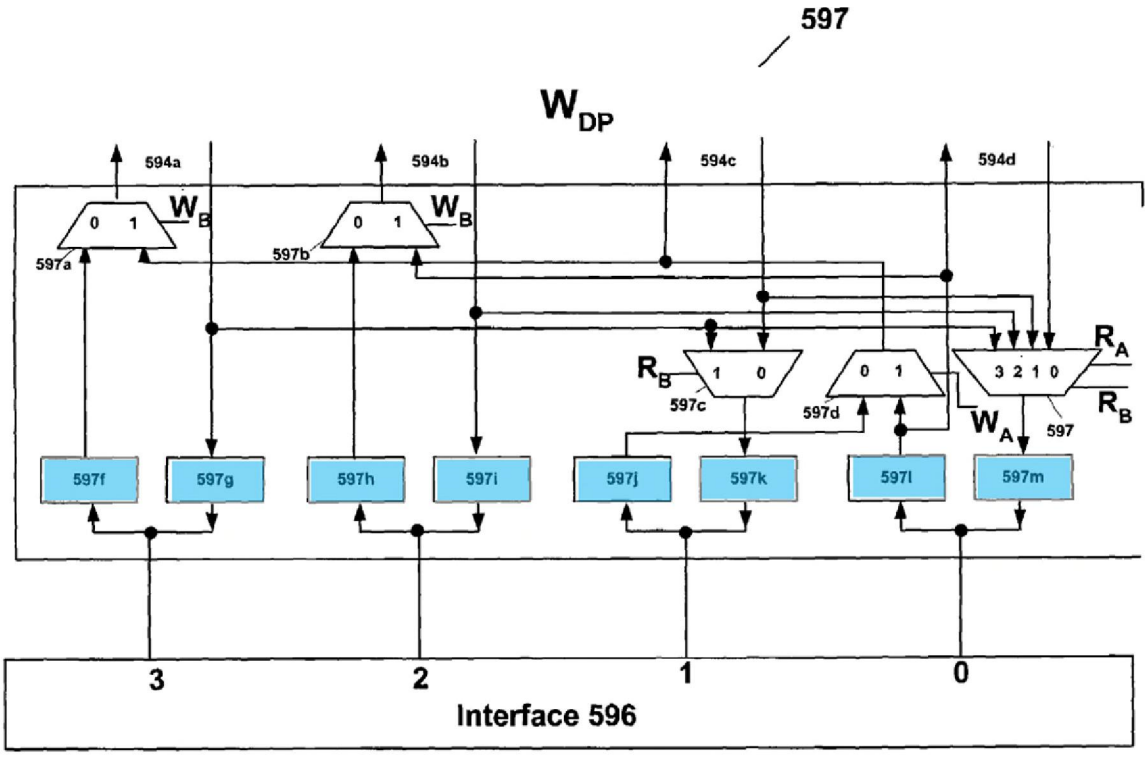


Fig. 5C

EX1071, Fig.5C. Perego's buffer device (red, above) also includes a serial interface 574 and operations circuit 572 to provide information to the system memory controller for initialization and proper configuration and operation of the system, including access latency values. *Id.*, 12:20-34, Figs.5A-5B; EX1003, ¶142.

B. JESD79-2 (EX1064)

The DDR2 SDRAM Specification (JESD79-2), published in September 2003, is prior art under §102(a), (b). EX1064; EX1065, ¶¶6-11; EX1003, ¶143. It

is a JEDEC standard for second generation double data rate (DDR2) memory devices. EX1064, p.Cover-1; EX1003, ¶144. JESD79-2 describes, for example, the signals used to execute read and write commands in ranks of memory devices. EX1064, pp.6, 24-33, 49; EX1003, ¶145. JESD79-2 also describes CAS latencies and adding additional clock cycles of latency when executing read and write commands. EX1064, pp.24-25; EX1003, ¶145.

C. Ellsberry (EX1073)

U.S. Patent Publication No. 2006/0277355 ("Ellsberry"), filed June 1, 2005, is prior art at least under §102(e) as explained above (pp.5-8). EX1073; EX1003, ¶146; *see also* EX1023, pp.24-26 (recognizing Ellsberry as prior art in proceeding against family member of 215 Patent). The Board analyzed Ellsberry extensively in a Final Written Decision against Netlist, *see* EX1074, and thus the issues decided against Netlist in that Decision are now binding against Netlist, *see, e.g.*, *VirnetX Inc. v. Apple, Inc.*, 909 F.3d 1375, 1377-78 (Fed. Cir. 2018); *MaxLinear, Inc. v. CF CRESPE LLC,* 880 F.3d 1373, 1376-77 (Fed. Cir. 2018).

Ellsberry implements "rank multiplication" (discussed above, pp.10-12) by "making two smaller-capacity memory devices emulate a single higher-capacity memory device." EX1073, Abstract; EX1003, ¶149. In particular, Ellsberry's memory module has "[a] control unit [red, below] and memory bank switch [purple, below]...to selectively control write and/or read operations...[and]

selectively rout[e] data to and from the memory devices," thus allowing "a plurality of memory devices [blue and green, below] [to] appear as a single memory device to the operating system." *Id.*

Figures 10-13 of Ellsberry illustrate different memory module configurations "that can be built using combinations of the control unit and bank switch." EX1073, ¶[0052]; *see also* EX1074, pp.77-81 (Final Written Decision discussing relationship of Figures 2, 5-6, and 10-13).

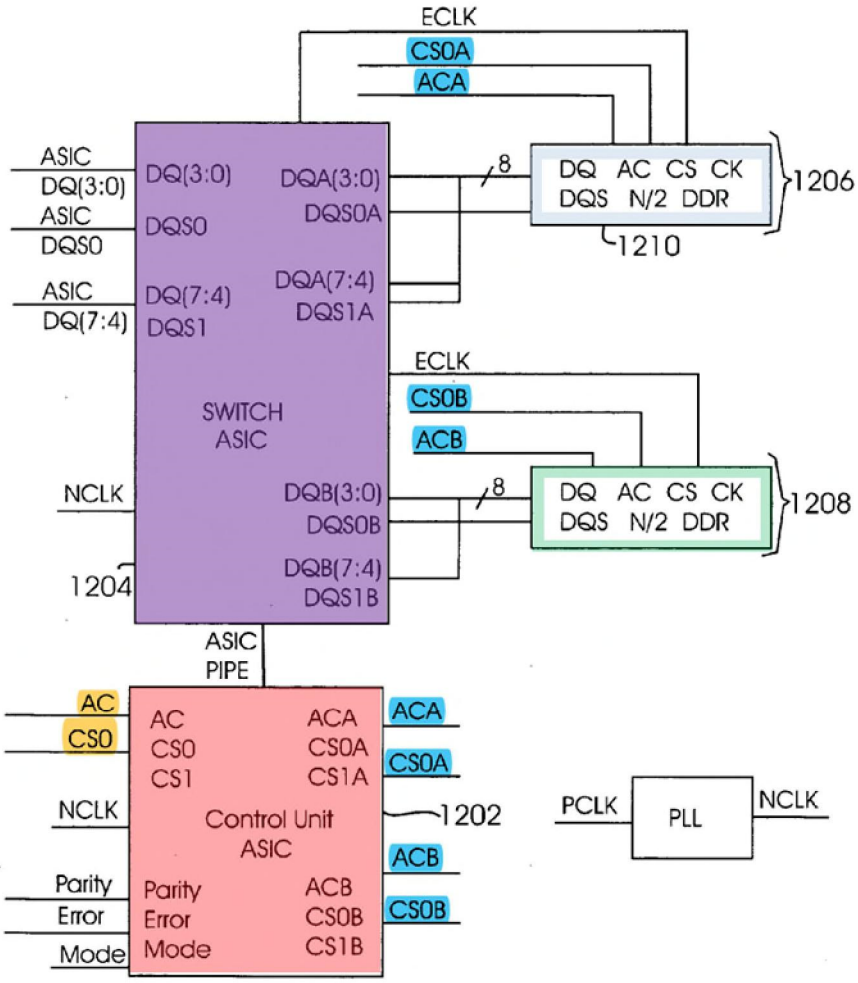


Fig. 12

EX1073, Fig.12. For example, "FIG. 12 illustrates...one control unit 1202 [(red)] and one bank switch 1204 [(purple)]...to control two memory banks 1206 [(light blue frame)] & 1208 [(light green frame)], each memory bank having one memory device 1210." *Id.* ¶[0055], Fig.12; EX1003, ¶150. The control unit (1202, red) receives a single chip-select signal (CS0, orange) to control a single memory rank, and generates two chip-select signals (CS0A and CS0B, blue) for two memory ranks. *Id.*

D. Halbert (EX1078)

U.S. Patent No. 7,024,518 ("Halbert"), filed March 13, 2002, is prior art at least under §102(e). EX1078; EX1003, ¶151. Halbert discloses "a new memory module architecture" that can be used in "a typical memory system" such as Figure 1 below. EX1078, Abstract, 1:31-2:46, Fig.1 (below); EX1003, ¶¶153-156.

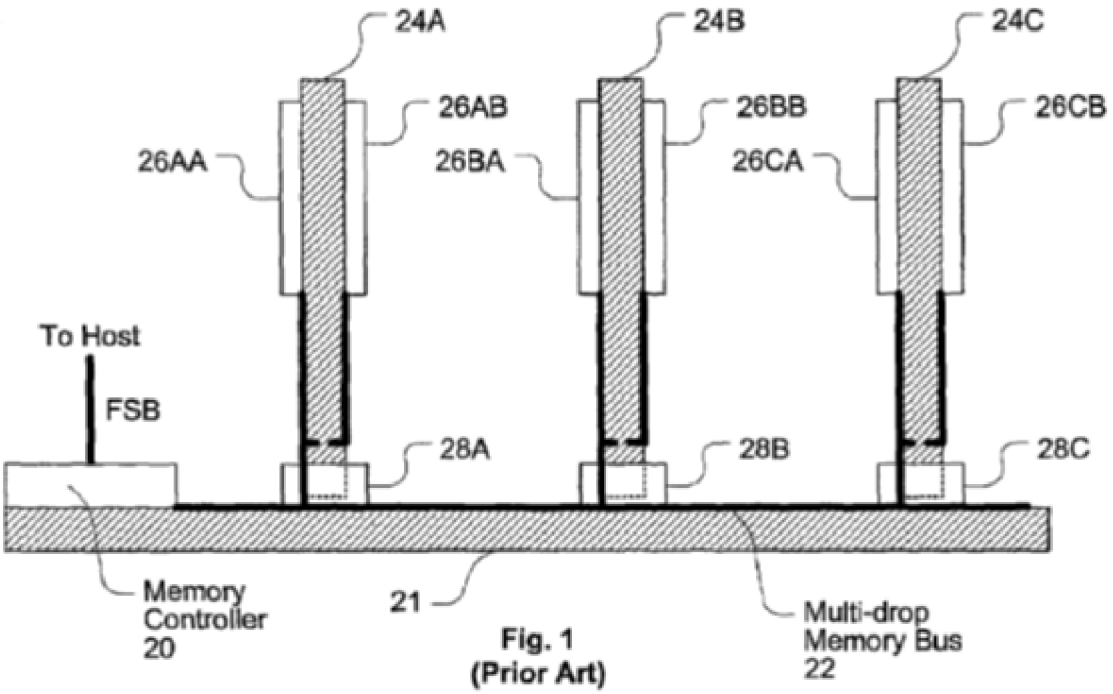
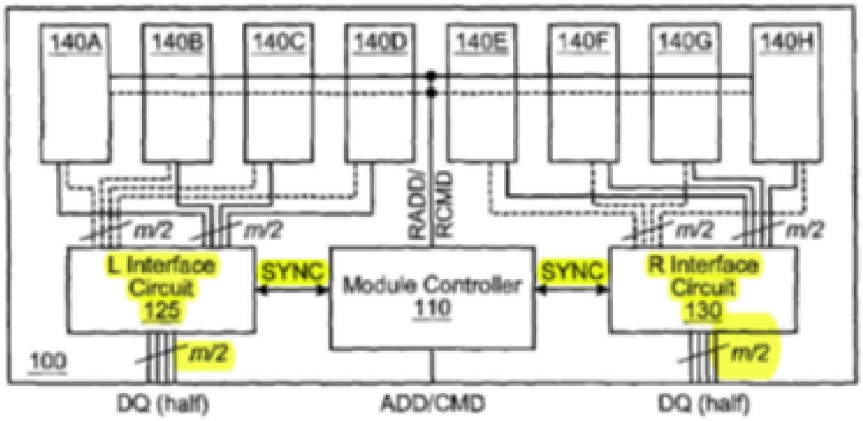


Fig. 1
(Prior Art)

Halbert's proposed memory module (below) can "allow the memory devices to be isolated from the full capacitive loading effects of the system memory data bus," EX1078, 3:60-4:2, while being "compatible with an existing memory controller/bus and with existing memory devices," *id.*, 3:48-57; *see also id.*, 3:42-4:35, 6:1-4.

Fig. 7



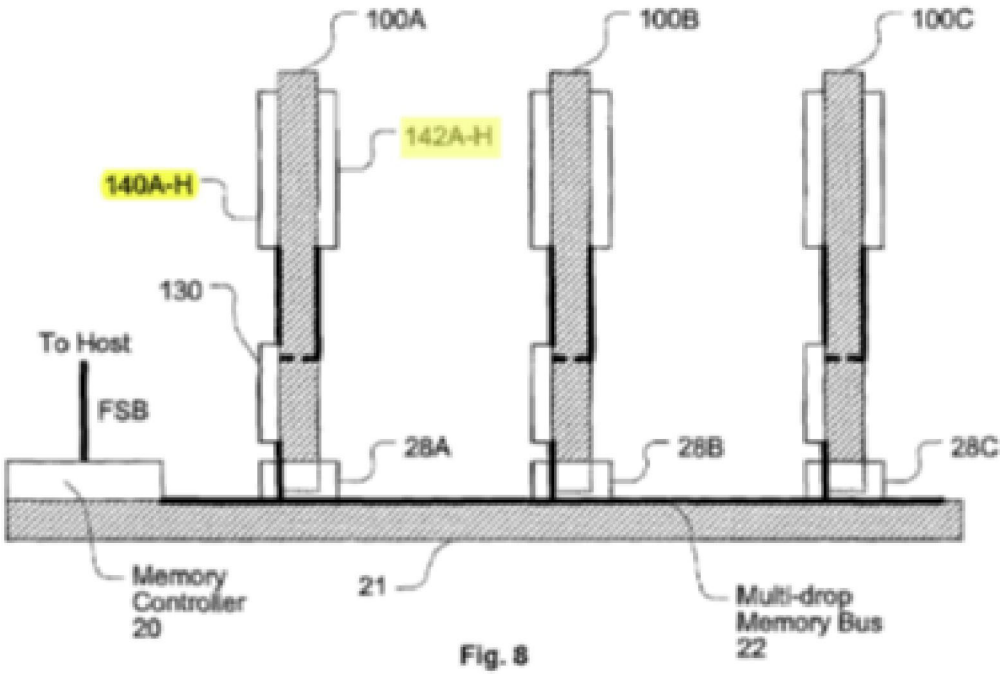
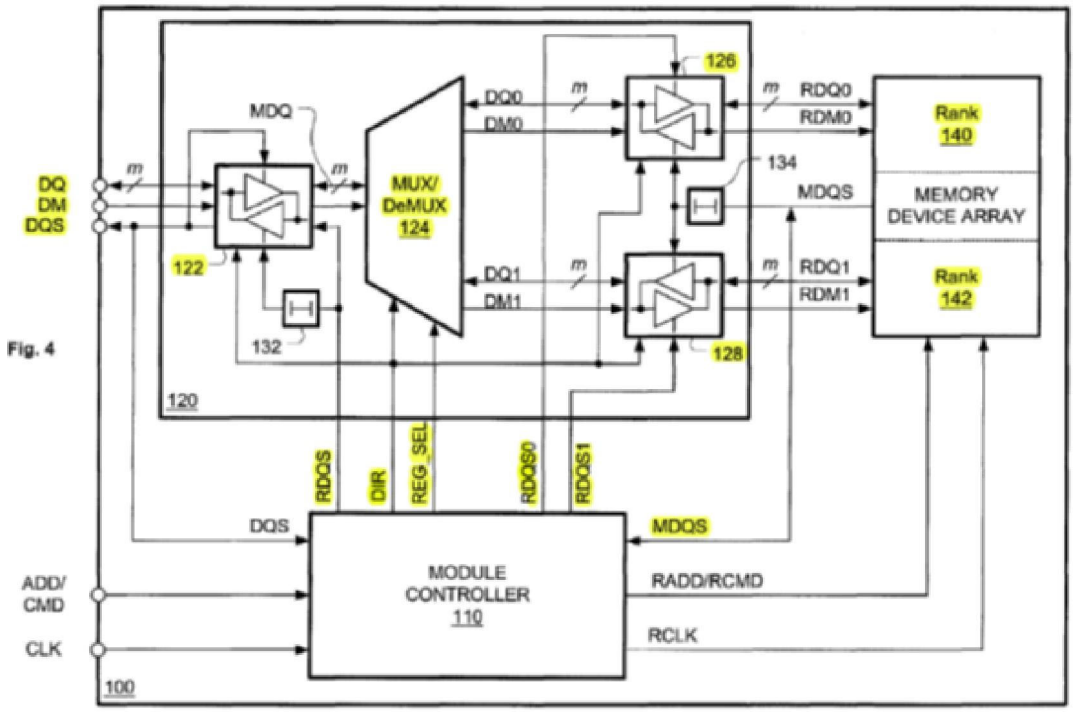


Fig. 8

Id., 7:31-61, Figs.7-8; EX1003, ¶¶157-158.

Halbert's module 100 (above and below) includes a module controller 110 that registers the address and command signals (ADD/CMD), and controls data interface circuits 125 and 130 (above) that communicate data between the system memory bus 22 and memory devices in ranks 140 and 142. EX1078, 4:36-5:65, 7:31-61, Fig.4; EX1003, ¶159. Interface circuits 125 and 130 (above) can each be

implemented as data interface circuit 120 in Figure 4 (below), except with half the number of data signal lines. *Id.*, 7:37-40; EX1003, ¶160.

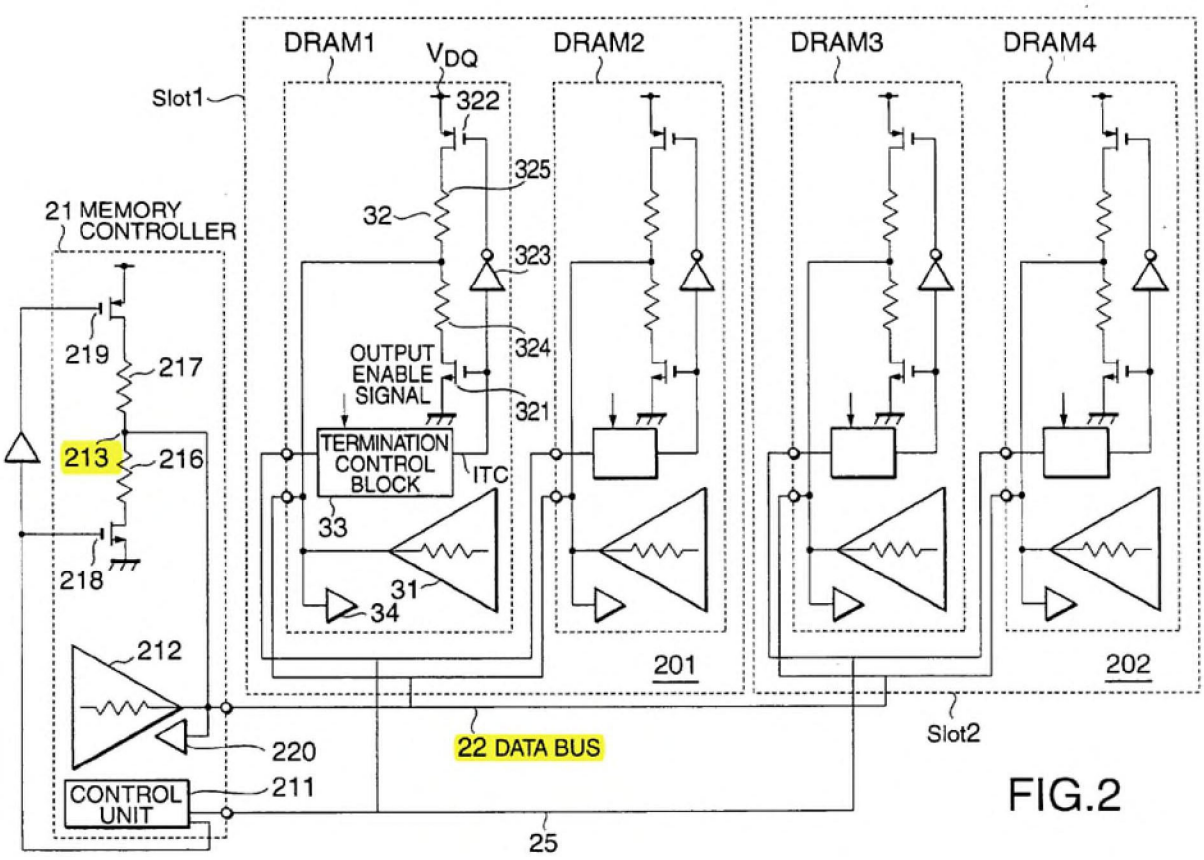


EX1078, Fig.4. Interface circuit 120 has a multiplexer/demultiplexer 124 that selectively directs data signals through registers 126 or 128 to or from rank 140 or 142, respectively. *Id.*, 5:6-22; EX1003, ¶¶161-164.

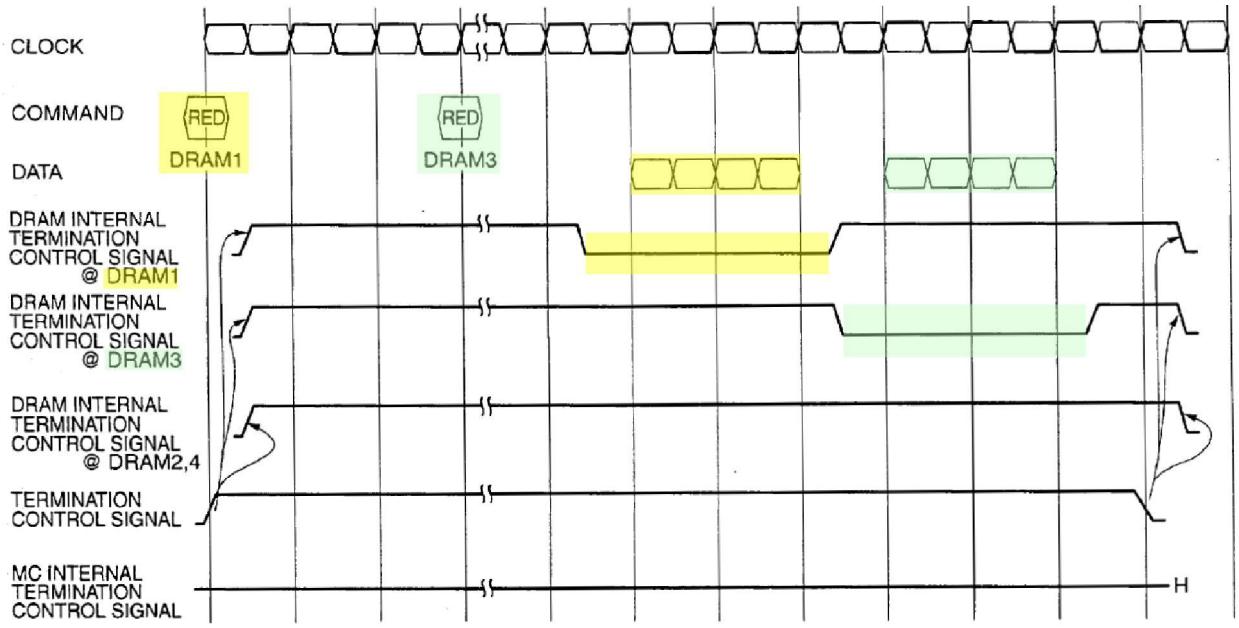
E. Matsui2 (EX1082)

U.S. Patent Publication No. 2003/0039151 ("Matsui2"), filed August 23, 2002, and published February 27, 2003, is prior art at least under §102(a), (b), and (e). EX1082; EX1003, ¶165. Matsui2 discloses a termination circuit 213 that interfaces with DRAM memory devices and provides external termination for data signals received on data bus 22. *E.g.*, EX1082, [0037]. "[A] termination circuit

213 [can] be put into an operating state in case [sic] where the data are read from the DRAM1, the DRAM2, the DRAM3, and the DRAM4," *id.*, [0037], Fig.2, and the termination circuit is turned off and on for read and write operations as shown, for example, in Figure 5 below, *id.*, Figs.5-7, 9. EX1003, ¶¶167-168.



EX1082, Fig.2.



Id., Fig.5.

VI. CLAIM CONSTRUCTION

Except for the term "rank," discussed below, Petitioners contend for purposes of this proceeding that no further construction is needed. While Netlist appears to have interpreted some of the other claim terms unduly broadly for purposes of infringement, *see, e.g.*, EX1085, pp.31-45; EX1088, pp.30-43, even though a narrower interpretation may be more reasonable, the claims are obvious under either interpretation, so no further construction is needed. EX1003, ¶133.

A. "rank"

A POSITA would have understood that "rank" refers to "an independent set of one or more memory devices on a memory module that act together in response

to command signals, including chip-select signals, to read or write the full bit-width of the memory module." EX1003, ¶126. This is consistent with the claim language (e.g., claim 1's "including at least one [first/second] memory integrated circuit in the [first/second] rank[,]" EX1001, 37:32-38); the specification (e.g., "The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width....[T]he ranks of a memory module are selected or activated by....rank-select signals, also called chip-select signals," *id.*, 2:59-62); and the JEDEC standard, EX1064, p.6 ("Chip Select:…. $\overline{CS}$ provides for external ***Rank*** selection on systems with multiple ***Ranks***."). EX1003, ¶¶124-128.

As already recognized by the Board, the term "bank" (or "physical bank") was also sometimes used to refer to what is now typically called a "rank." EX1003, ¶129; EX1048, pp.13-14, 20, 28 (invalidating claims to "ranks" based on prior-art "banks"); *compare* EX1060, p.7 (chip-select for "bank"), *with* EX1064, p.6 (chip-select for "[r]ank"); *see also* EX1062, pp.6, 10-16 (chip-selects for "physical banks"). Thus a POSITA would understand that "bank" and "physical bank" could mean the same thing as "rank" (given the "chip-select signal"):

10.2.2 Rank

Figure 10.5 shows a memory system populated with 2 ranks of DRAM devices. Essentially, a *rank* of memory is a *"bank"* of one or more DRAM devices that operate in lockstep in response to a given command. However, the word *bank* has already been used to describe the number of independent DRAM arrays within a DRAM device. To lessen the confusion associated with overloading the nomenclature, the word *rank* is now used to denote a set of DRAM devices that operate in lockstep to respond to a given command in a memory system.

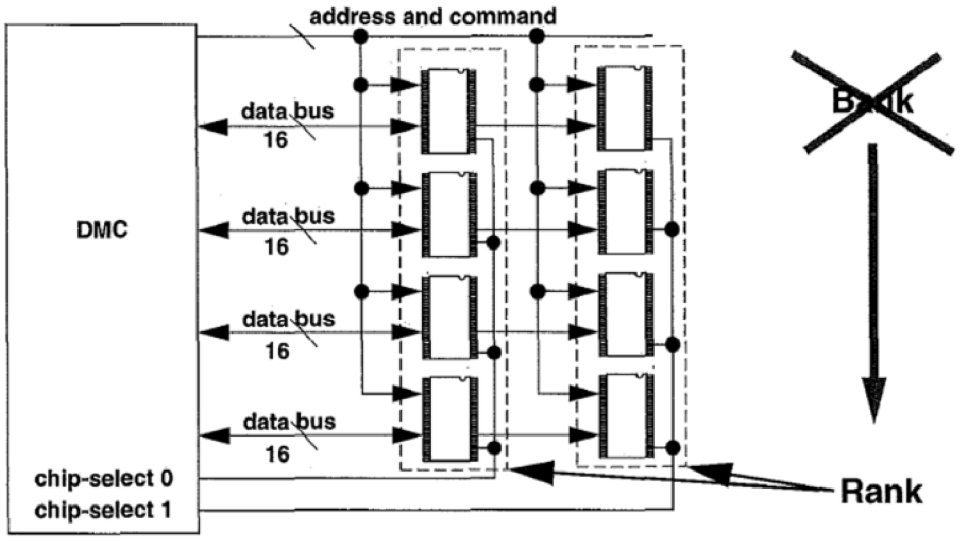


FIGURE 10.5: Memory system with 2 ranks of DRAM devices.

EX1070, p.413; *see also* EX1069, pp.4 n.3, 9; EX1003, ¶129.

A "rank" comprises "one or more DRAM devices." EX1003, ¶¶127, 130-131; EX1001, 37:32-38 ("at least one"); EX1070, p.413; EX1023, pp.28-33 (rejecting Netlist's argument to the contrary). Consistent with the claim language ("at least one"), the 215 Patent describes an embodiment with one memory device in each "rank." EX1001, 16:66-17:8; EX1003, ¶130. In this embodiment, the bit

width of the "rank" would be the same as the bit width of the memory device, for example 16 bits. EX1003, ¶130. The 215 Patent explains that "memory devices...having bit widths of 4, 8, 16, 32, as well as other bit widths[] are compatible." EX1001, 6:9-11.

VII. ARGUMENT

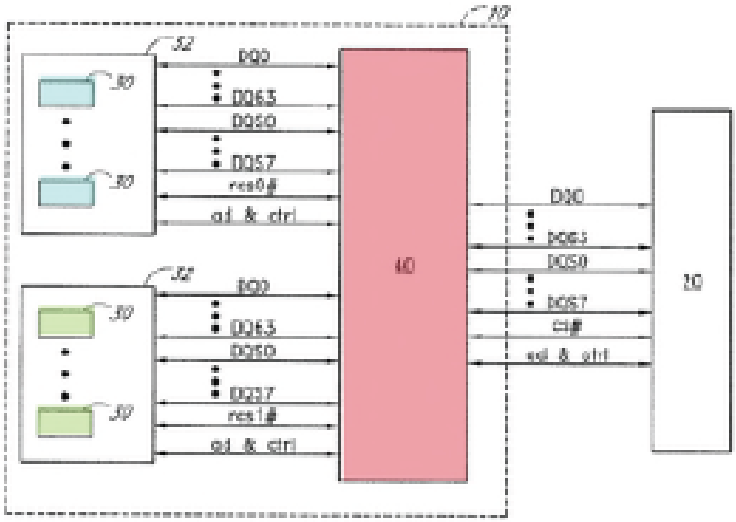
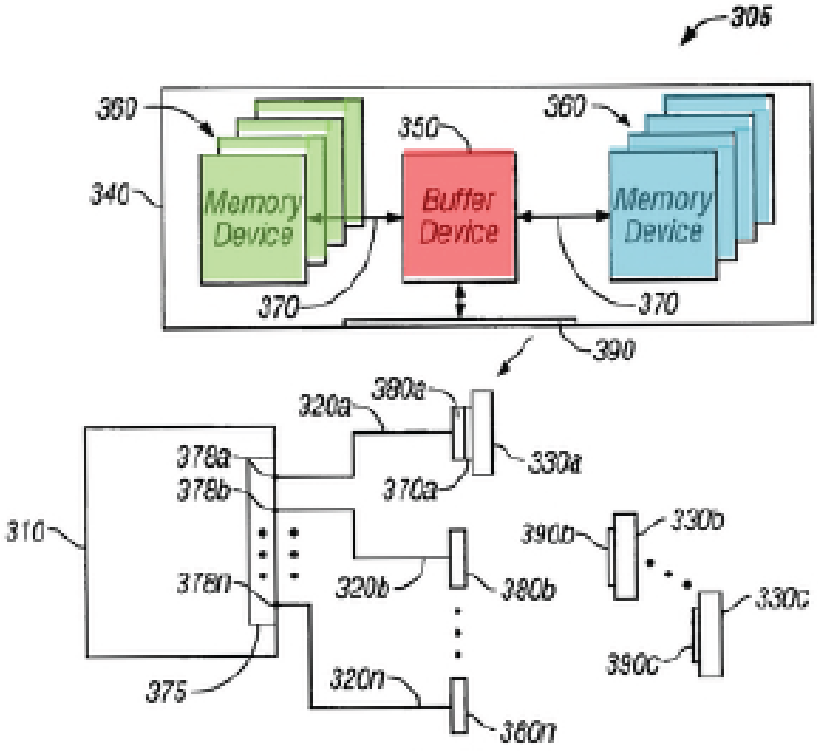
A. Ground 1

Ground 1 renders obvious claims 1-29.

1. Ground 1 combination: Perego (EX1071) and JESD79-2 (EX1064)

Ground 1 combines Perego (EX1071) with JESD79-2 (EX1064). EX1003, ¶¶182-192.

As shown below, Perego is similar to the 215 Patent, which discloses a "circuit 40" (red) that "selectively ***isolates*** the loads of some (e.g., one or more) of the ranks" (blue and green) "of the memory module 10 from the computer system." EX1001, 7:16-22. Perego similarly discloses a "buffer device 350" (red) that "transceives and ***provides isolation*** between...signals interfacing to the plurality of memory devices 360[]" (blue and green). EX1071, 6:12-15.

215 Patent	 FIG. 1
Perego	 FIG. 3B

The 215 Patent explains that its circuit 40 can be part of the same component as a register 230, EX1001, 14:54-58, that "receives and buffers a plurality of command signals and address signals...and transmits corresponding signals to the appropriate memory devices 30," *id.*, 14:46-51. As explained below, Perego similarly explains that its buffer device 350 can perform these functions. *See, e.g.*, EX1071, 5:6-15, 6:12-33, 13:18-24, Figs.5A-5B; *see also* claim elements [1.c] (pp.48-54), [1.e] (pp.73-76); EX1003, ¶¶249-260, 304-311.

Both Perego and the 215 Patent disclose that their memory modules can use DDR2 memory devices. EX1071, 3:62-4:12, 8:1-4 ("DDR"), 10:54-67 ("DDR2"); EX1001, 6:4-:11 ("DDR-1, DDR-2"), 21:7-10 ("DDR1, DDR2"). As discussed above (pp.9-10), the JEDEC standard for DDR2 memory devices is JESD79-2 (EX1064).

Accordingly, A POSITA would have been motivated to combine the teachings of JESD79-2 with the memory module described in Perego. EX1003, ¶183. A POSITA would have known about and been familiar with the JEDEC Standards, including JESD79-2 as discussed above (pp.9-10), and would have recognized the relevance of these standards given Perego's references to using DDR2 memory devices. *Id.* For example, JESD79-2 discloses specific ways to issue read and write commands to DDR2 memory devices, including using "row address strobe, column address strobe, etc., and address lines" as referenced in

Perego, EX1071, 9:58-60. *See, e.g.*, EX1064, pp.6, 24-33, 49. Accordingly, a POSITA would have been motivated to consult JESD79-2—including its details regarding memory transactions, such as read and write operations, for JEDEC-compliant memory devices—to implement Perego's system with JEDEC-compatible memory devices. EX1003, ¶183.

Furthermore, Perego discloses "exploit[ing] features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices," EX1071, 6:34-43, which would have motivated a POSITA to turn to JESD79-2 to implement Perego's system in a way that is compatible with existing generations of memory devices (specifically DDR2 memory devices). EX1003, ¶184. A POSITA would have also recognized that applying JESD79-2's teachings to Perego would have resulted in a predictable variation of Perego, which would improve similar devices in the same way and not yield unexpected results or challenges in implementation. *Id.*

In applying the teachings of JESD79-2 to Perego, a POSITA would have been knowledgeable about other JEDEC standards, as noted above (pp.9-10). These standards would have included, for example, JESD21-C, which had standardized a registered DIMM format for DDR memory devices, specifying the input and output signals and their functions on the memory module, and the corresponding assignments for socket/connector pins. EX1003, ¶¶185-188;

EX1062, pp.1, 5-9; EX1066, pp.1, 4-8. Indeed, Perego discloses an upgradeable memory system that includes interfaces for DIMM and other removable memory modules, EX1071, 1:58-2:6 (discussing DIMM format disclosed by U.S. Patent No. 5,513,135, EX1081), along with a need for "flexible and cost effective upgrade capabilities," EX1071, 2:26-29, 6:34-43. EX1003, ¶185. A POSITA would have therefore been motivated to implement Perego's memory modules in a registered DIMM format with DDR memory devices that fits into DIMM connectors and uses DIMM module input signals, according to JEDEC standards, including JESD21-C and JESD79-2. EX1003, ¶¶185-188. Perego also discloses that its module includes the functionality of a serial presence detect (SPD) consistent with "conventional DIMM modules" to store information used to configure memory devices upon system startup, EX1071, 12:20-34, and which "provides the configurable width buffer and/or module capabilities to the memory system," *id.*, Abstract. A POSITA would therefore have understood that Perego's module would be compatible with JEDEC's SPD requirements, *e.g.*, EX1062, pp.68-70; EX1066, pp.94-96, to allow the system memory controller to read, understand, and properly initialize and use Perego's module. EX1003, ¶189.

For at least these reasons, a POSITA would have been aware of JESD79-2 and related JEDEC standards and understood their disclosure, and would have been motivated to combine JESD79-2 with Perego in order to implement Perego's

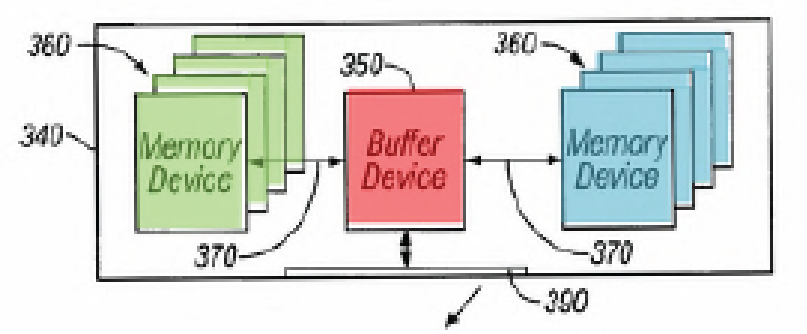
modules using JEDEC-compliant memory devices, such as DDR2 memory devices, to allow these modules to be used in JEDEC-compliant memory systems, such as those using DIMM modules of the format described by JESD21-C. EX1003, ¶190. A POSITA would have understood that the combination of Perego and JESD79-2 merely used familiar elements according to known methods described in Perego and the JEDEC standards, including JESD79-2, yielding predictable results, namely memory modules like Perego's including memory devices operating according to the familiar JEDEC standards. EX1003, ¶191.

2. Independent Claim 1

a) [1.a] Preamble

(1) [1.a.1] Memory Module

To the extent the preamble is limiting, Ground 1 teaches "*[a] memory module*," e.g., Perego's memory subsystem 340, buffered module 395, and memory modules 400, 450, and 470, as shown in Figures 3B (partially below) and 3C-4C (below). EX1071, 1:21-23, 6:57-60, 7:30-33, 9:26-33, Title, Abstract. EX1003, ¶¶212-216.



[Fig. 3B]

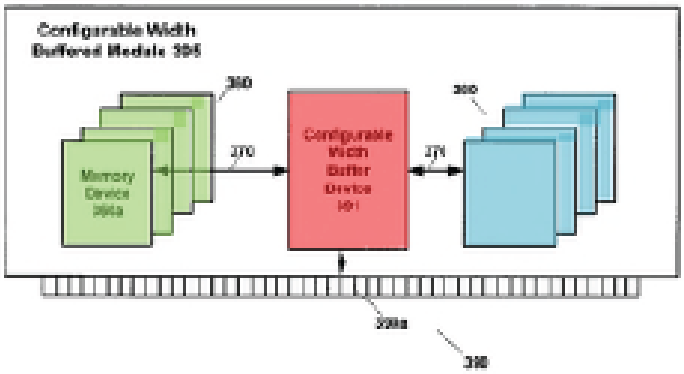


Fig. 3C

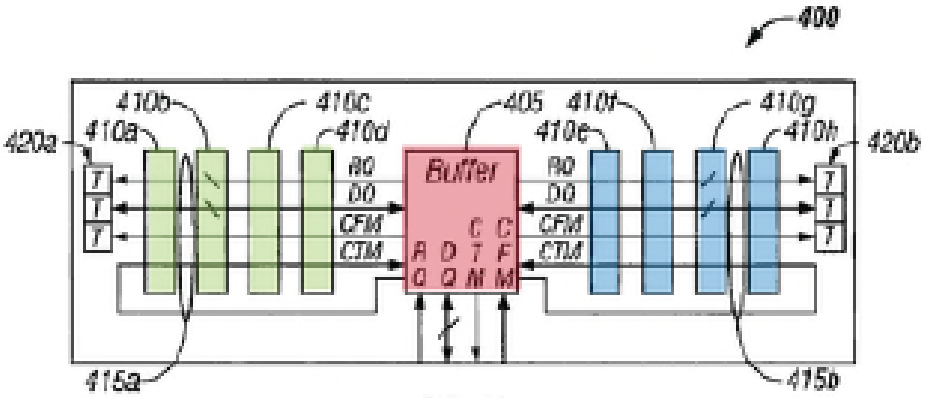


FIG. 4A

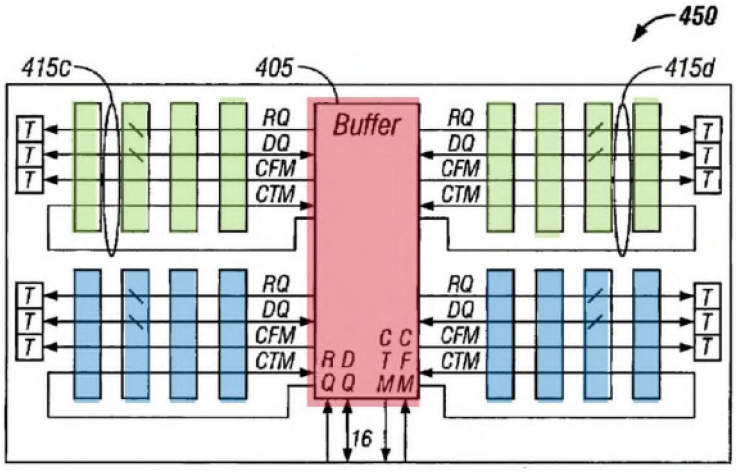


FIG. 4B

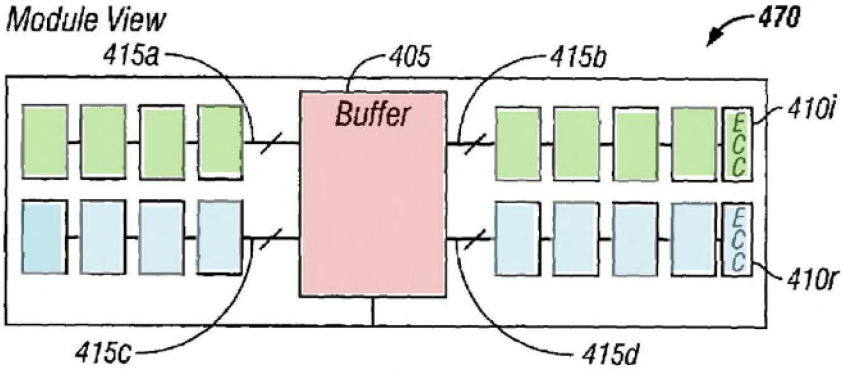


FIG. 4C

(2) [1.a.2] Operable in a Computer System

Ground 1 teaches that the memory module is "*operable in a computer system*," e.g., Perego's teachings of a "personal computer or server" including memory system 305 (below). EX1071, 3:13-22, 4:65-5:15; EX1003, ¶¶219-220. Perego's module provides "upgrade flexibility," EX1071, 3:23-28, 6:34-37, and thus is compatible with prior-art computers using a traditional bus for data, address, and control signals consistent with the JEDEC standards, *id.*, 1:34-40,

2:22-25 ("bussed approaches...permit[]...upgradeability"), Figs.1, 2A-2B; EX1064, p.6; EX1062, p.6; EX1066, p.6. EX1003, ¶¶221-222.

Ground 1 also teaches "*to communicate data* [through a respective link, e.g., 320a] *with a memory controller* [e.g., memory controller 310] *of the computer system via a memory bus* [e.g., in link 320a, which communicates "data, addressing and control information" between memory controller 310 and memory subsystem 340] *in response to memory commands* [e.g., read and write commands that comply with JESD79-2, EX1064, pp.24-33, 49] *received from the memory controller* [e.g., through the link 320a]." *See, e.g.*, EX1071, Fig.3B (below), 3:13-22, 4:65-5:15; EX1003, ¶¶219-228.

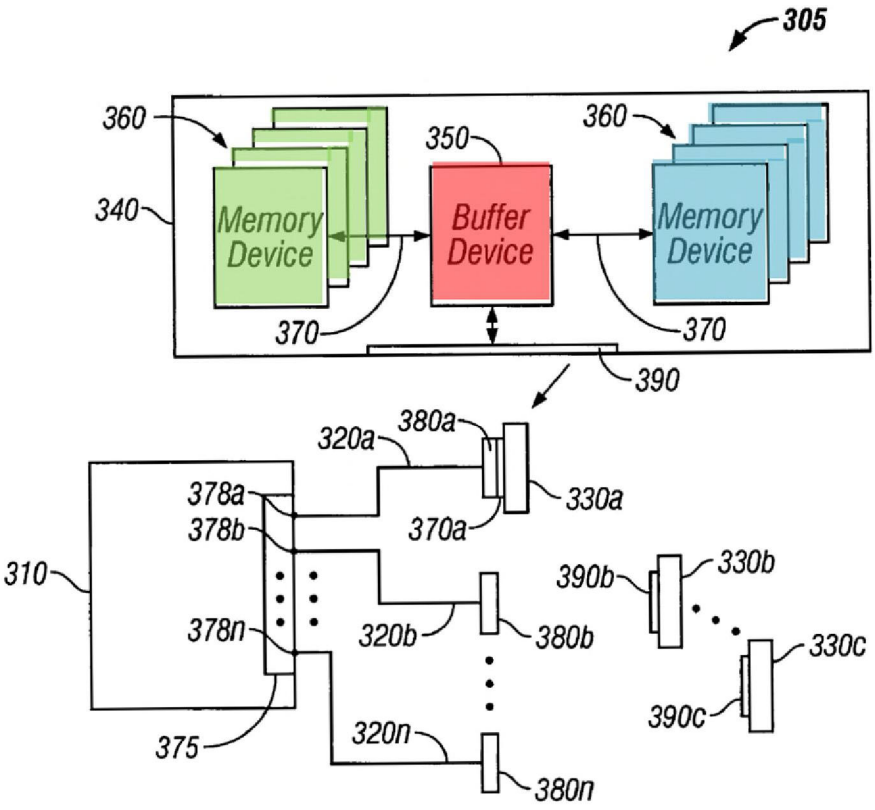


FIG. 3B

More specifically, Perego discloses that its "*memory bus*" (e.g., in link 320a) can have a data width of W_{DP}=16, 32, 64, or 128 bits "*to communicate data with a memory controller* [310] *of the computer system*." EX1071, Figs.4A-4B ("DQ" data lines), Figs.5A-5B (below), 3:41-47 ("one or more busses"), 5:6-24 ("bus"), 11:8-12, 14:16-51; EX1003, ¶¶220-224. A POSITA would have understood that a data width of W_{DP}=64 corresponds to the 64-bit data width of a JEDEC-compliant registered DIMM module. EX1062, p.5; EX1003, ¶224.

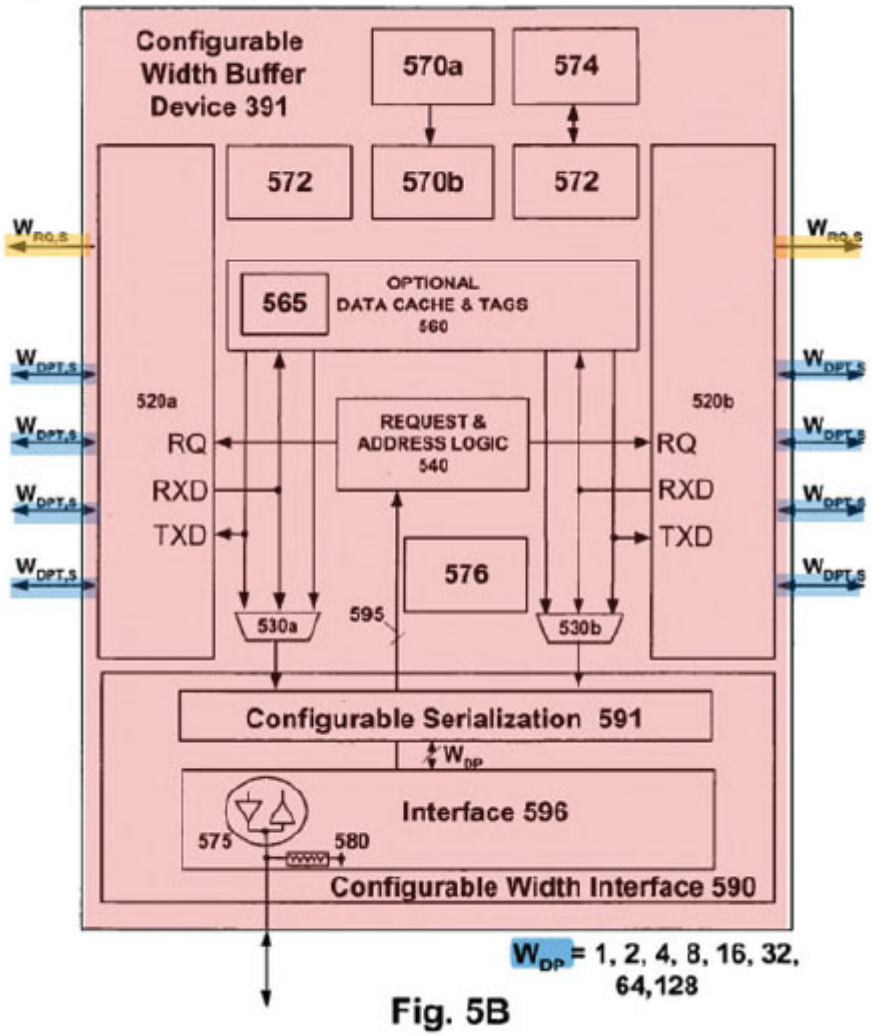

Configurable Width Buffer Device 391
570a
574
572
570b
572
OPTIONAL DATA CACHE & TAGS 560
565
520a
520b
REQUEST & ADDRESS LOGIC 540
RQ
RXD
TXD
RQ
RXD
TXD
576
595
530a
530b
Configurable Serialization 591
Interface 596
575
580
Configurable Width Interface 590
W_DP = 1, 2, 4, 8, 16, 32, 64,128

Fig. 5B

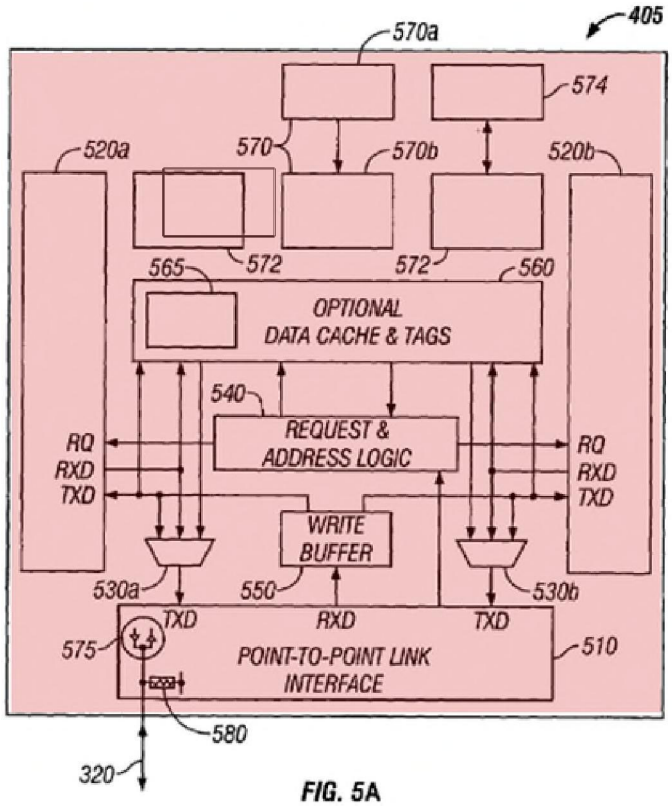


FIG. 5A

Further, a POSITA would have understood that Perego's module and corresponding memory devices communicate data "*in response to memory commands received from the memory controller.*" EX1003, ¶¶225-227. For example, Perego discloses that "[i]n a normal memory read operation" memory devices 360 transmit data in response to controller 310 "transmit[ting]...signals to one or more, or all of memory devices 360." EX1071, 6:15-25, Fig.3B; *see also id.*, 3:62-4:12 (describing memory devices storing and retrieving data "as part of a write or read command"). Perego's disclosure of "control lines (RQ) transport[ing] control (e.g., read, write, precharge...) information," EX1071, 9:50-60, and the use of "row address strobe [RAS], column address strobe [CAS], etc.,"

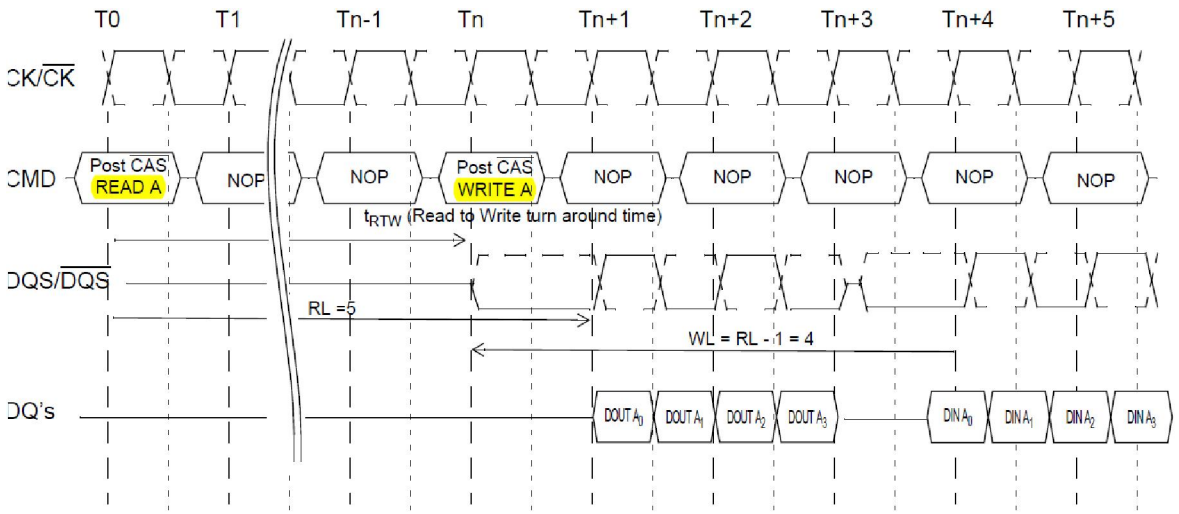
id., 9:58-60 also teaches that such control information includes read and write commands from the memory controller. EX1003, ¶226. A POSITA would also have understood from their own knowledge of JEDEC standards, including JESD79-2, the specific ways to issue read and write commands to Perego's DDR2 memory devices, and would have been motivated to apply those teachings. EX1003, ¶227; EX1064, pp.24-33 (Section 2.2.4, "Read and Write Access Modes"); *id.*, pp.6, 49 & n.1 (showing Chip Select "CS," Row Address Strobe "$\overline{\text{RAS}}$," and Column Address Strobe "$\overline{\text{CAS}}$" signals used to convey memory read and write commands).

(3) [1.a.3] Memory Commands

Ground 1 teaches "*the memory commands including a first memory command* [e.g., write or read] *and a subsequent second memory command* [e.g., subsequent write or read], *the first memory command to cause the memory module to receive* [for a write command] *or output* [for a read command] *a first data burst* [according to the JESD79-2 standard] *and the second memory command to cause the memory module to receive or output a second data burst* [according to the JESD79-2 standard]." EX1003, ¶¶229-239.

Perego discloses using DDR SDRAM devices that store or retrieve data in response to "a write or read command," EX1071, 3:64-4:12, 8:1-4, 10:56-58, and a POSITA would have understood from JESD79-2 that a first write or read

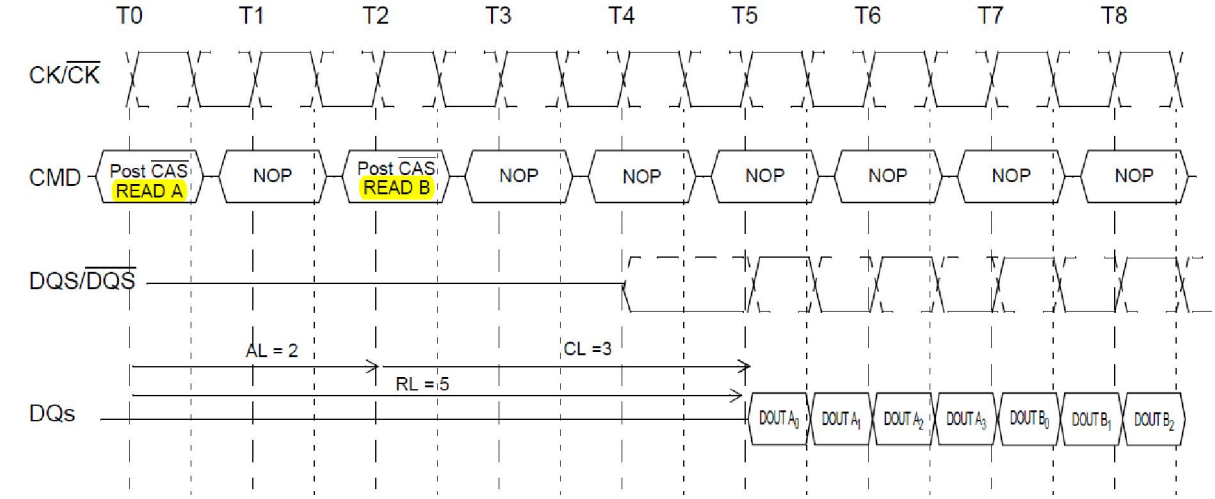
command can be followed by a "*subsequent*" second write or read command, EX1064, pp.24-33; EX1003, ¶¶232, 237, as shown below:



The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation.

Figure 26 — Burst Read Followed by Burst Write: RL = 5, WL = (RL-1) = 4, BL = 4

EX1064, p.28 (read command, write command).



The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 27 — Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

Id. (read command, read command). In Perego's module, the subsequent memory operations can be directed to different subsets of the memory devices. EX1071, 7:56-59; EX1003, ¶237.

Furthermore, a POSITA would have understood that the data for a read or write command can be transmitted or received in "*burst[s]*," EX1003, ¶233; EX1064, pp.25-32, as shown below by JESD79-2:

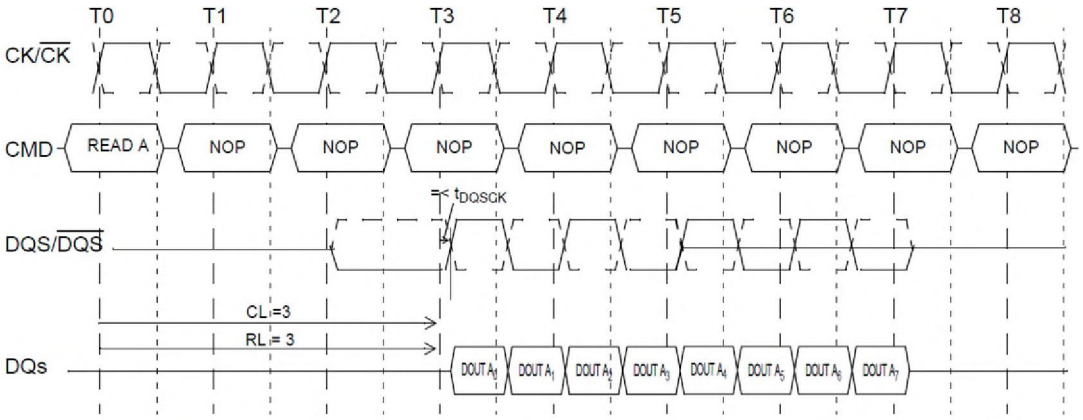


Figure 25 — Burst Read Operation: RL = 3 (AL = 0 and CL = 3, BL = 8)

EX1064, p.27.

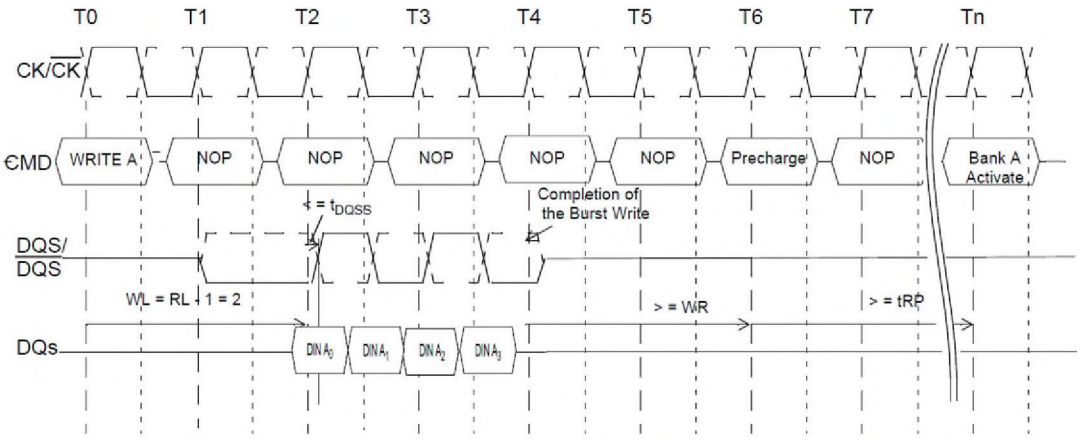
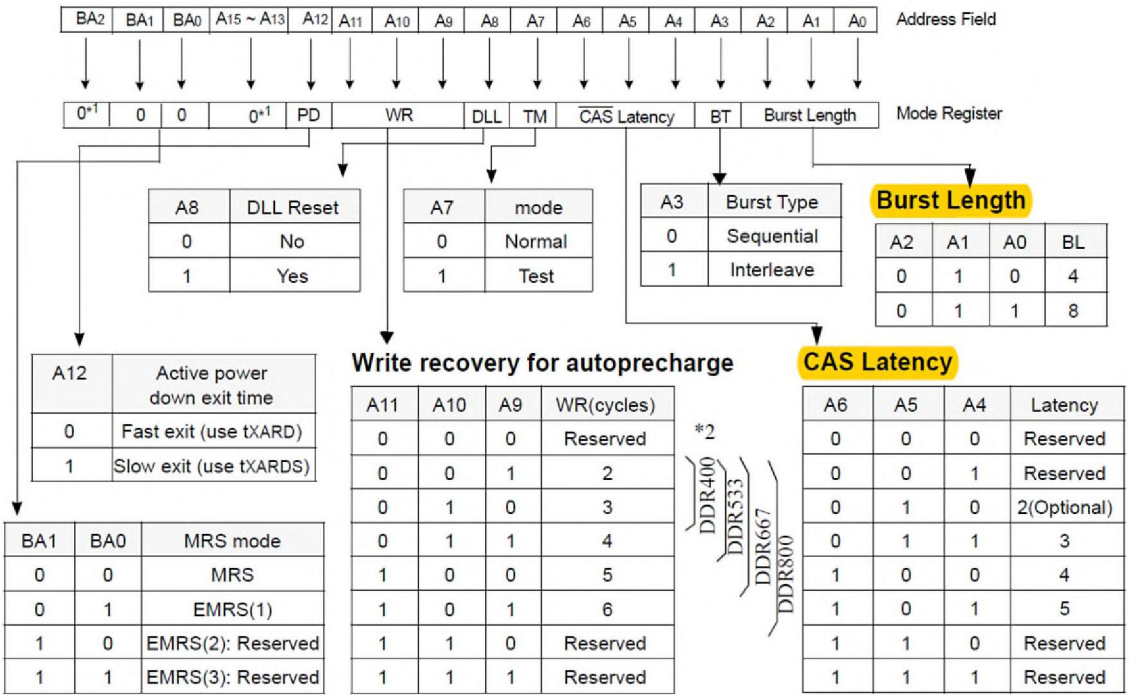


Figure 31 — Burst Write Operation: RL = 3, WL = 2, tWR = 2 (AL=0, CL=3), BL = 4

Id., p.30. A POSITA would have also understood that the memory controller can program latencies and burst lengths by mode register commands, so that data communication between the memory controller and the memory module is synchronized, EX1003, ¶¶233-235, as also shown in JESD79-2:



EX1064, p.12. Accordingly, a POSITA would have understood that Perego's modules were designed to perform multiple read and write operations and output or receive corresponding bursts of data signals, and would have been motivated to apply the teachings of JESD79-2 to Perego's module. EX1003, ¶238.

(4) [1.a.4] Comprising

Ground 1 teaches "*the memory module* [above, pp.35-37] *comprising*" [below, pp.46-80].

b) [1.b] Printed Circuit Board

Ground 1 teaches "*a printed circuit board* [PCB] *having a plurality of edge connections* [edge connectors 390] *configured to be electrically coupled to a corresponding plurality of contacts of a module slot* [e.g., mating connectors or sockets 380] *of the computer system.*" EX1003, ¶¶243-248. For example, Perego's memory modules "are incorporated onto individual substrates (e.g., ***PCBs***)...that include connectors 390a-390c" with "a plurality of contacts, conducting elements or pins," EX1071, 5:56-6:11, 7:39-41, as shown below:

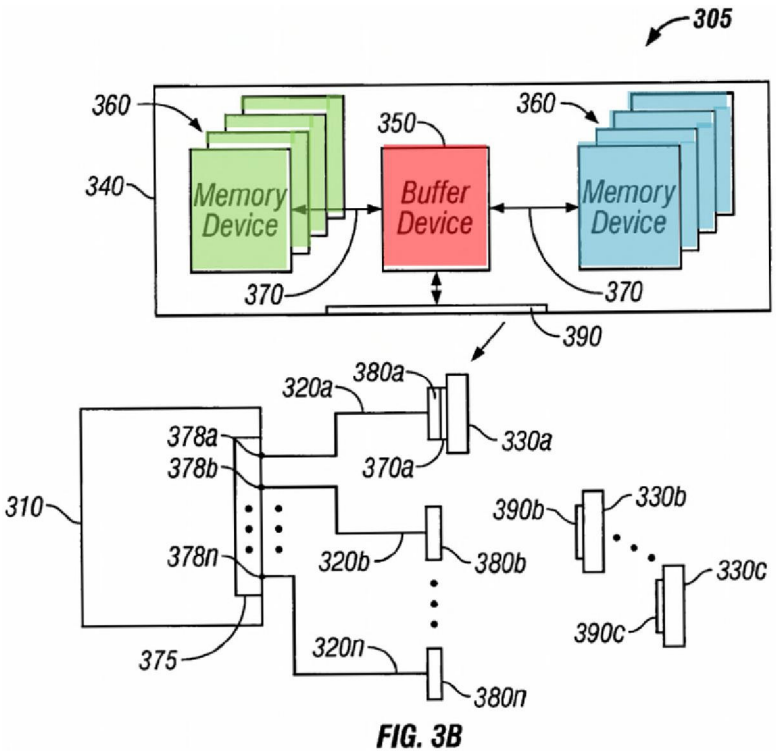


FIG. 3B

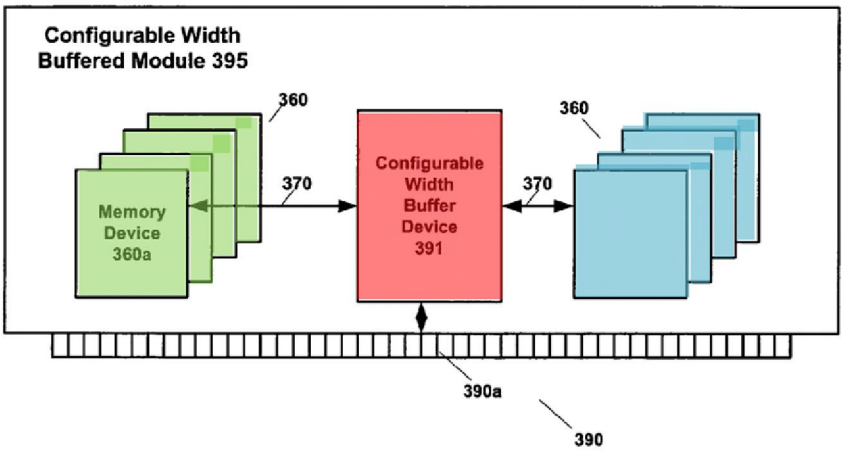


Fig. 3C

Id., Figs.3B-3C. Moreover, a POSITA would have understood from Perego that its module can be implemented in a standard DIMM format, EX1003, ¶247; EX1071, 6:34-43, 3:25-28; EX1069, p.2, and that such a DIMM format also uses a "*printed*

circuit board" (PCB) with "*edge connections*" to couple to the socket of the memory system, EX1003, ¶247; EX1062, pp.29 (describing mounting on "PCB"), 66 (describing "DIMM printed circuit board" with "PCB edge connector contacts").

c) [1.c] Register

Ground 1 teaches "*a register* [e.g., in Perego's buffer device (350)] *coupled to the printed circuit board* [from [1.b] (pp.46-48)] *and configured to receive and buffer first command and address signals representing the first memory command* [from [1.a.3] (pp.42-46)]*, and to receive and buffer second command and address signals representing the second memory command* [from [1.a.3] (pp.42-46)]." EX1003, ¶¶249-260. Perego's buffer device (350) is shown below:

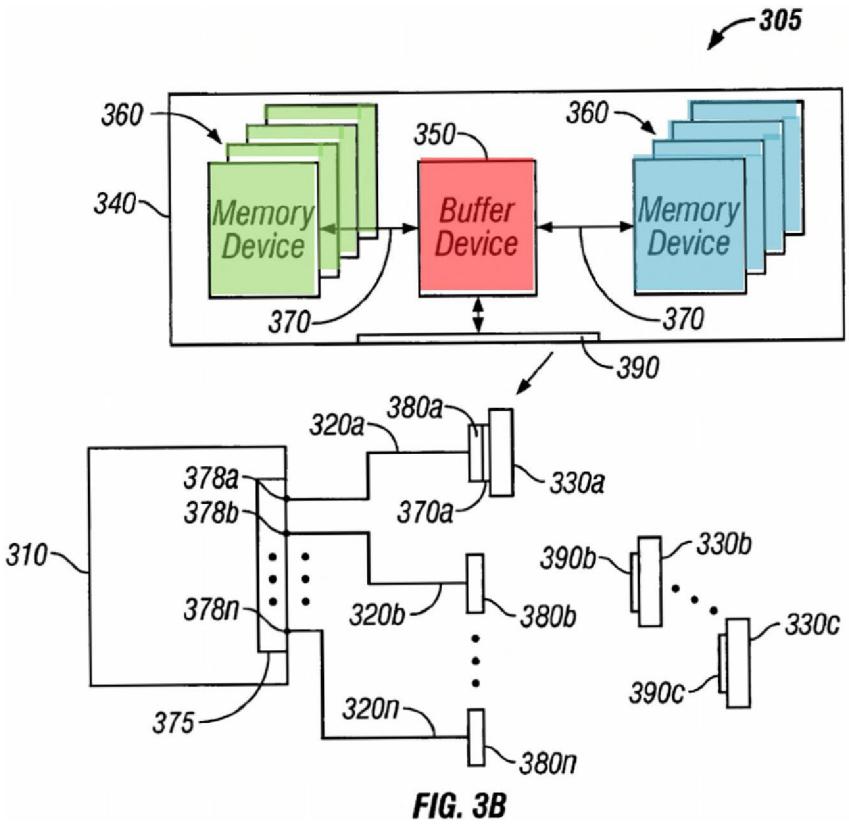
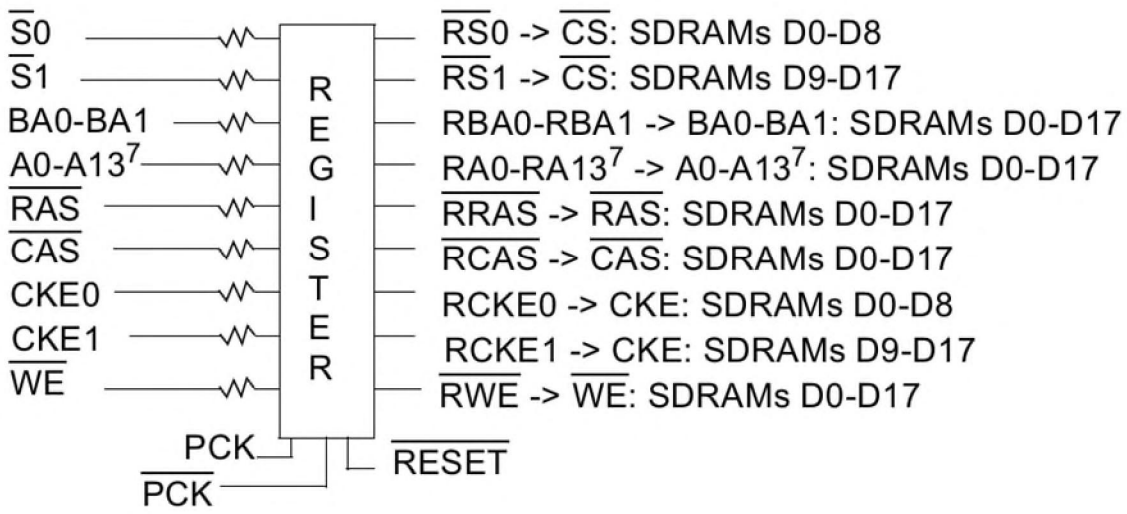


FIG. 3B

EX1071, Fig.3B. A POSITA would understand that this buffer device (shown above and below in red) includes a "*register*" to "buffer or register" first/second command and address signals representing first/second memory commands (read or write commands received on link 320). EX1003, ¶¶251-252; EX1071, 5:6-15, 6:12-33, Figs.5A-5B. A POSITA would have understood that this register, after receiving address (e.g., BA0-BA1, A0-A13) and control signals (e.g., S0-S1, RAS, CAS, WE), provides "*register[ed]*" address (e.g., RBA0-RBA1, RA0-RA-13) and control signals (e.g., RS0-RS1, RRAS, RCAS, RWE) to the memory devices at least because Perego's buffer device can operate similarly to a JEDEC-compliant

registered DIMM, EX1062, p.12, shown immediately below. EX1003, ¶¶254-255; EX1071, 6:15-30; *see also id.*, 13:54-59, Fig.5C (showing that interface 596 includes registers, similar to latches 597f-m, for interfacing with the system memory bus).



EX1062, p.12.

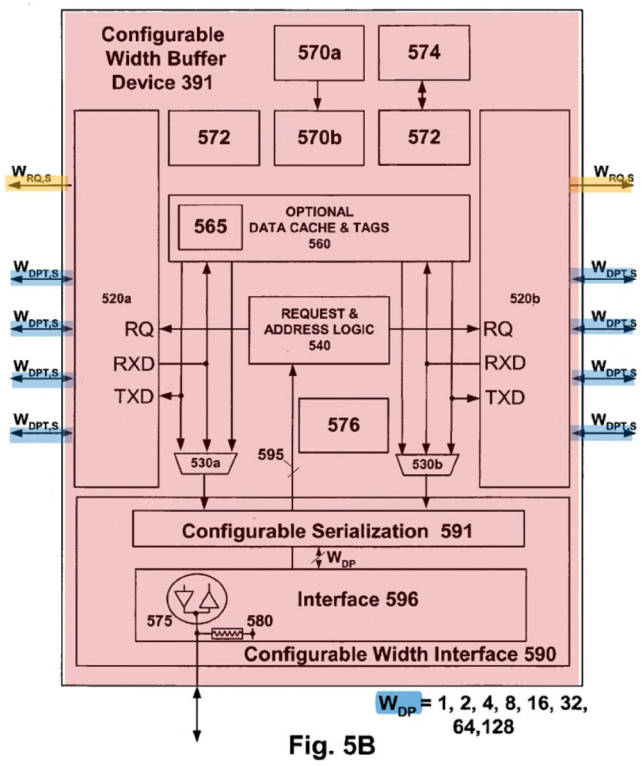


Fig. 5B

EX1071, Fig. 5B

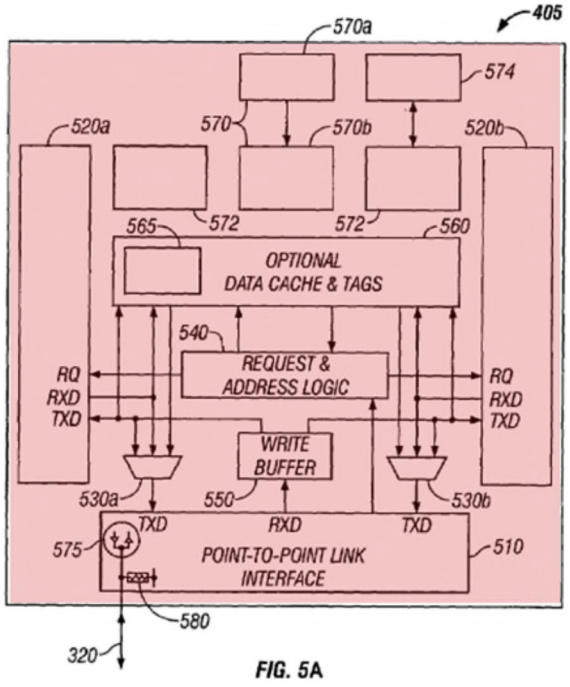


FIG. 5A

EX1071, Fig.5A. Perego's buffer (red above) includes request and address logic 540 for decoding "control information and address information," among other tasks. *Id.*, 13:54-59; *see also id.* at 6:12-15, 11:8-12. A POSITA would have understood that this information represents "*command and address signals*" based at least on Perego's disclosure that its module can use DDR SDRAM devices, EX1071, 8:1-4, 10:56-59, which respond to read and write commands and corresponding address information, EX1064, pp.26, 29, 49. EX1003, ¶253.

Perego also discloses control lines (RQ) between the system controller and the memory module that send "read, write" commands and corresponding "address" signals. EX1071, 9:50-60, Figs.4A-4B (below); EX1003, ¶256.

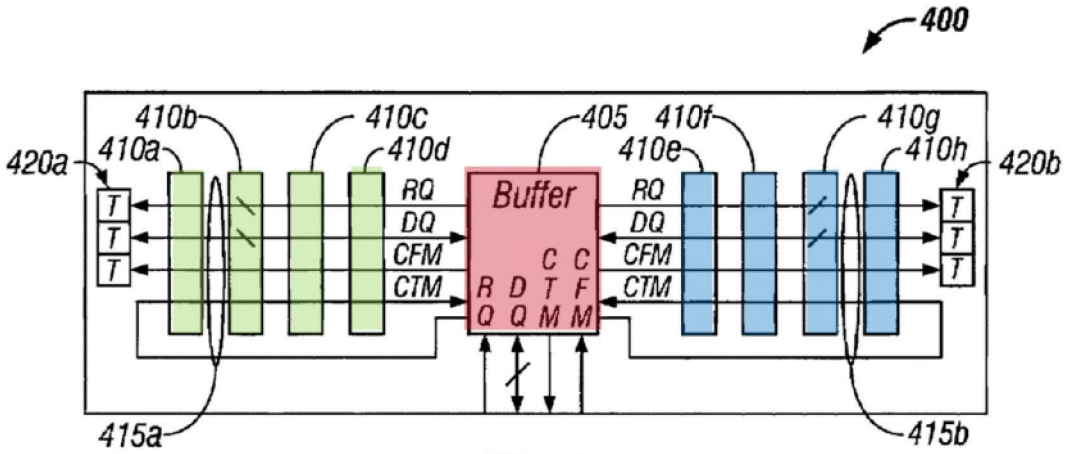


FIG. 4A

EX1071, Fig.4A.

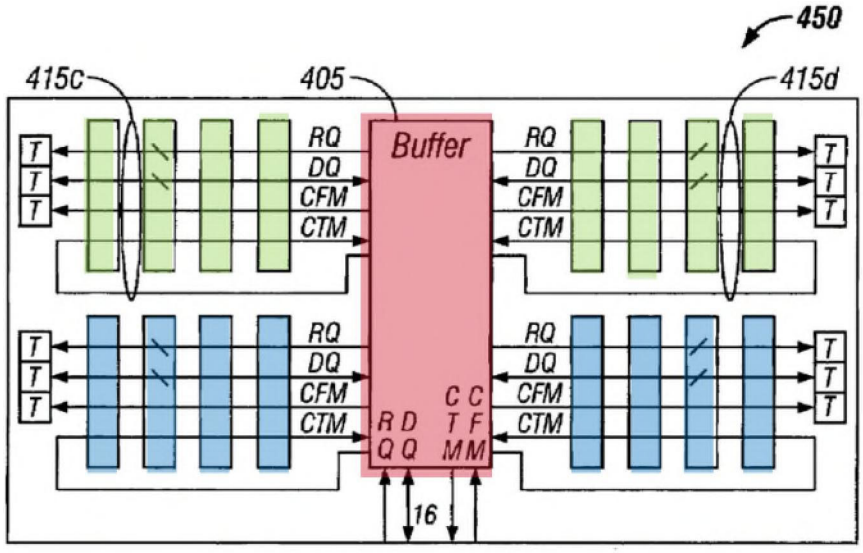


FIG. 4B

Id., Fig.4B.

A POSITA also would have understood that "*command and address signals*" representing a respective memory command would be received from the

memory controller because the receiving of command and address information is naturally associated with a memory command. EX1003, ¶¶256-258.

d) [1.d] Ranks

(1) [1.d.1] Memory Integrated Circuits

Ground 1 teaches "*a plurality of memory integrated circuits* [e.g., 360, 410, below] *mounted on the printed circuit board* [from [1.b] (pp.46-48)] *and arranged in a plurality of ranks including a first rank* [green, below] *and a second rank* [blue, below], *the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank.*" EX1003, ¶¶261-282.

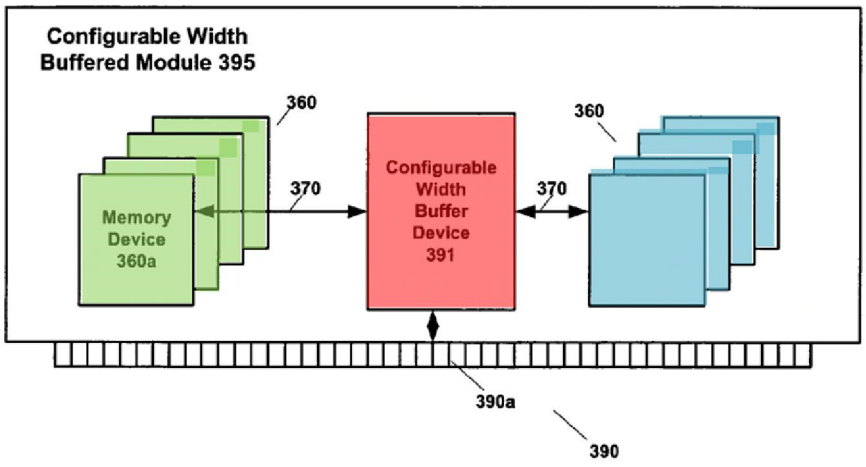


Fig. 3C

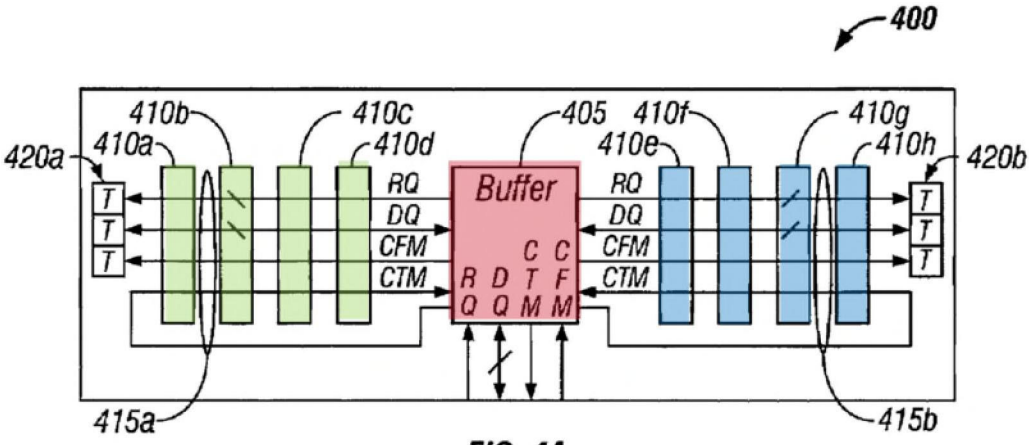

400
410b
410a
420a
410c
410d
405
410f
410e
410g
410h
420b
Buffer
RQ
DQ
CFM
CTM
C C
R D T F
Q Q M M
T
415a
415b

FIG. 4A

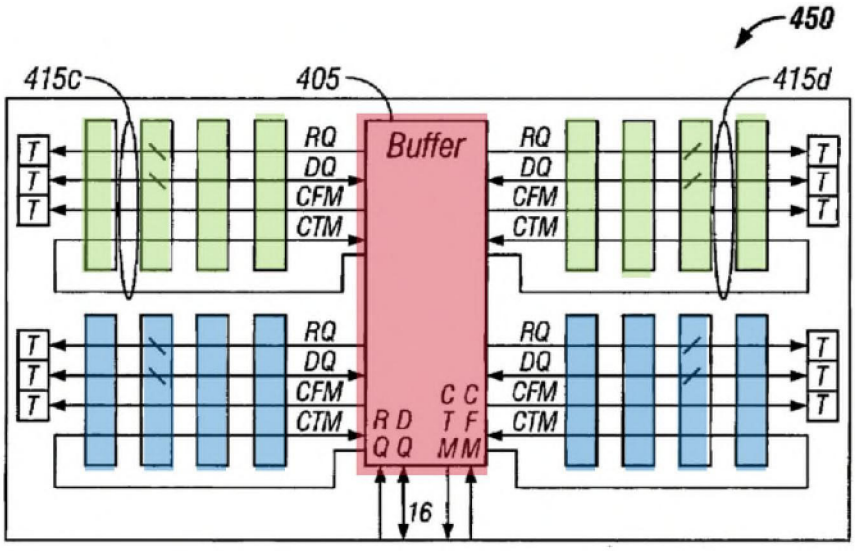

450
415c
405
415d
Buffer
RQ
DQ
CFM
CTM
C C
R D T F
Q Q M M
T
16

FIG. 4B

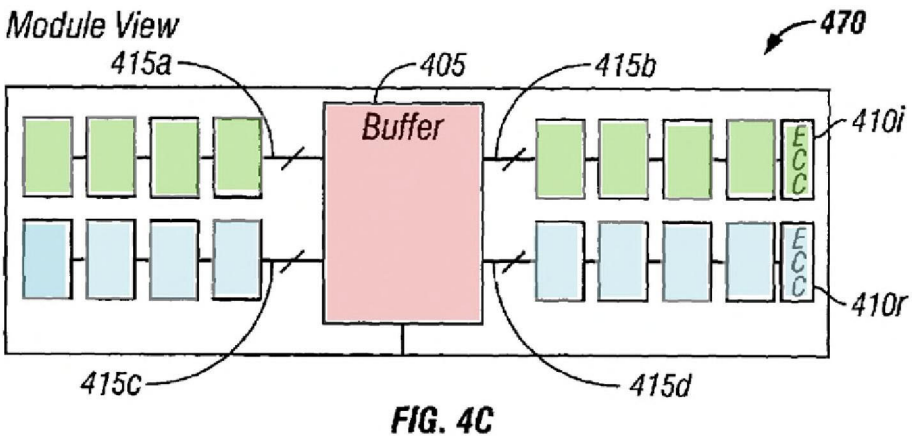


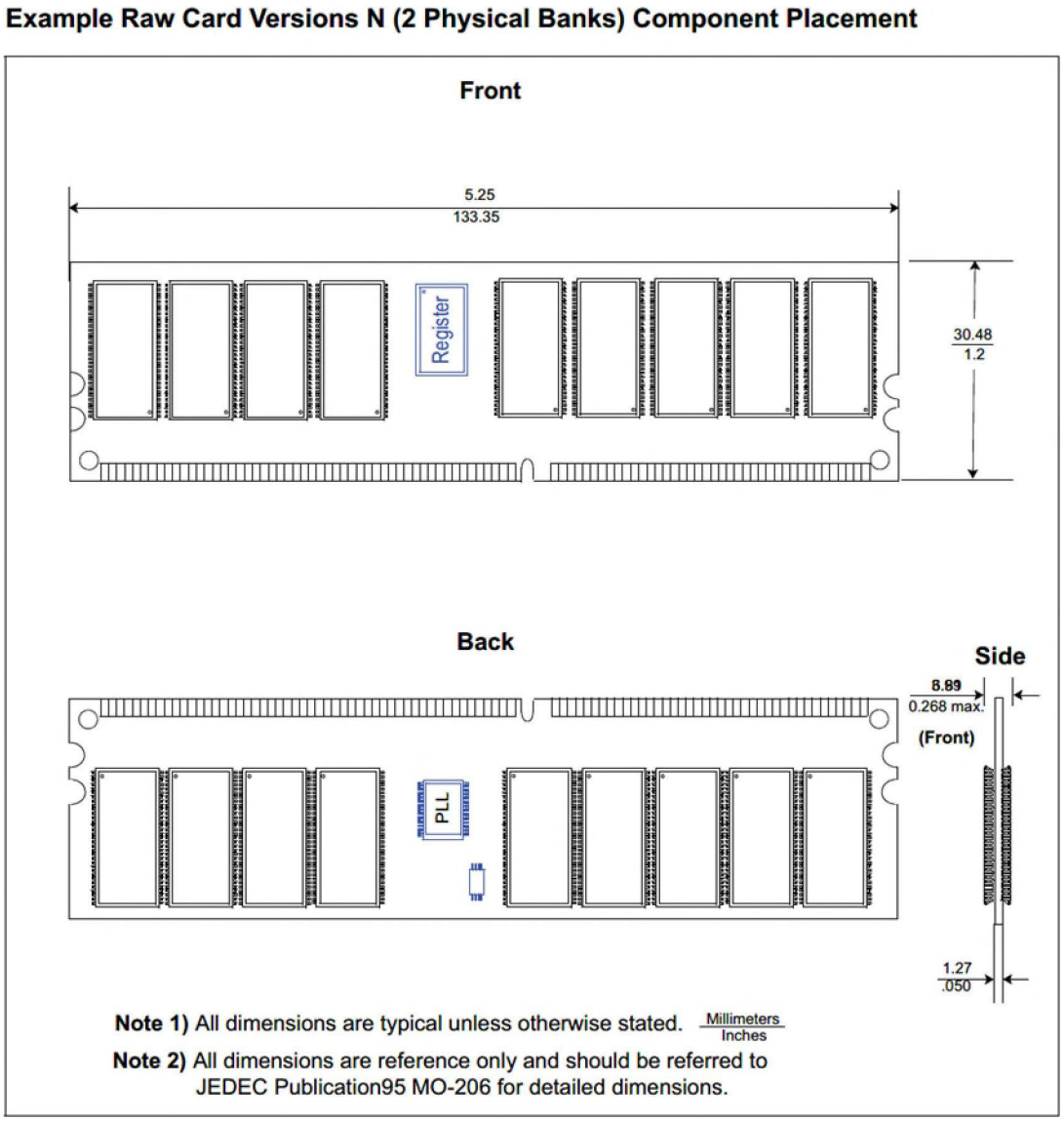
FIG. 4C

EX1071, Figs.3C, 4A-4C.

Perego's "*memory integrated circuits*" 360 and 410, which can include DDR or DDR2 SDRAM devices, are shown above. EX1071, 3:62-4:3, 8:1-4, 10:56-58; EX1003, ¶264. Perego discloses "grouping memory devices into multiple independent target subsets (i.e. more ***independent banks***)," EX1071, 15:37-45, which renders obvious the claim limitation "*rank[s]*" as properly construed (pp.27-30). EX1003, ¶263.

As explained above for [1.b] (pp.46-48), Perego's "memory module" includes a "*printed circuit board*" (PCB), which Perego explains is a "a substrate package housing or structure having a plurality of memory devices employed with a connector interface," EX1071, 4:19-22, consistent with the standard DIMM format (below) that includes "*a plurality of memory integrated circuits mounted on the printed circuit board*," EX1062, pp.29, 35 (below, illustrating DDR SDRAM

devices "surface mounted" on both sides of a PCB in a DIMM format); EX1071, 2:4-6 ("DIMM"). EX1003, ¶265.



Perego also teaches "*a plurality of memory integrated circuits ... arranged in a plurality of ranks*" with "*at least one...memory integrated circuit*" in each "*rank*." EX1003, ¶266. For example, Perego teaches that "interfaces 520a and 520b [below] may be programmed to connect to 16'x4' width memory devices,

8‘x8’ width memory devices or 4‘x16’ width memory devices,” EX1071, 14:10-15, Figs.5A-5B, resulting in a “*rank*” with a bit-width of 64 bits, consistent with the standard DIMM layout shown above, *see, e.g.*, EX1062, p.13 (describing a “x64 DIMM, populated as two physical banks [i.e., “*ranks*,” *see* pp.27-30] of [eight] x8 DDR SDRAMs [i.e., D0-D7, and D8-D15]”). The terms ‘x4’, ‘x8’ and ‘x16’—pronounced “by four,” “by eight,” and “by sixteen”—refer to the data width of a single memory device, EX1069, p.1, so eight ‘x8’ memory devices results in a total bit-width of 64 bits. EX1003, ¶266.

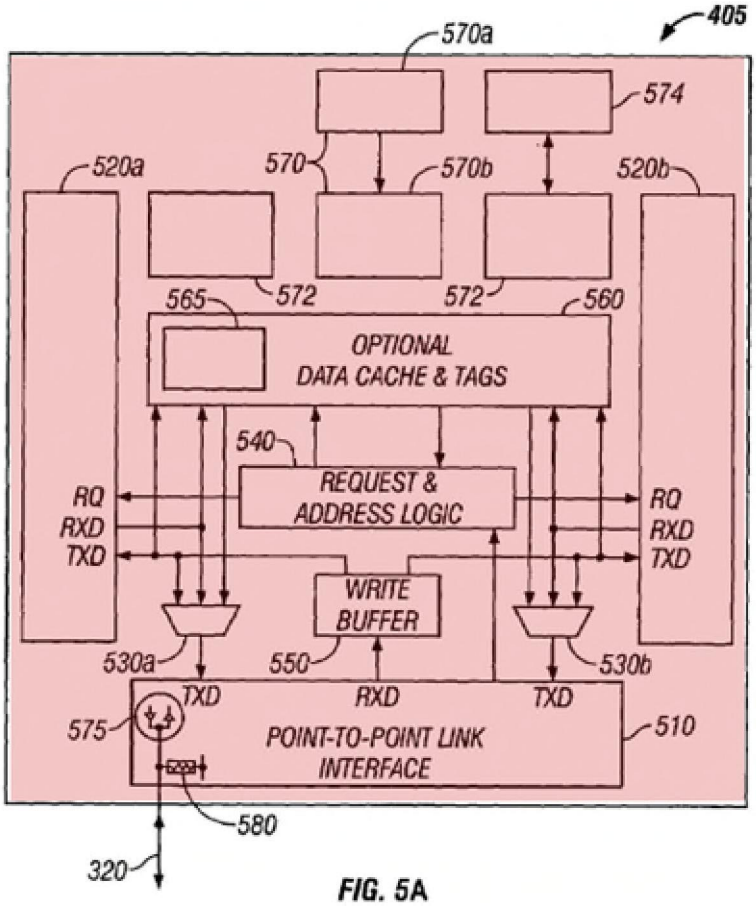


FIG. 5A

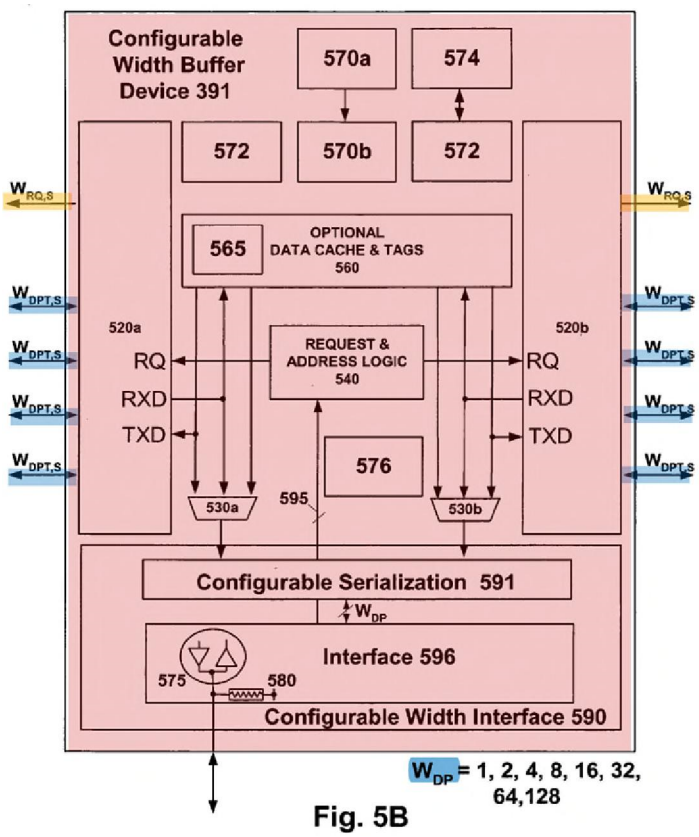


Fig. 5B

Perego teaches that the data width accessed in a memory transaction (W_A), and the data width of the buffer interfacing with the memory controller (W_{DP}), can both be the same (e.g., both 64 bits), such that the ratio W_A/W_{DP}=1:1. EX1071, 14:16-40, 17:22-28 ("1:1"), Fig.5C; EX1003, ¶267. A POSITA would understand that W_A refers to the bit-width of each "*rank*" of memory devices (e.g., 64 bits can be read or written at a time) when only "***one***" of the "one or more channels 370" (shown below) is used for a read or write operation. EX1071, 6:12-24, 14:23-27, Fig.3C; EX1003, ¶¶268-269. Accordingly, when Perego's buffer device has two

channels, and each channel is connected to one rank, Perego's module includes two ranks of memory devices (green and blue below). EX1003, ¶269.

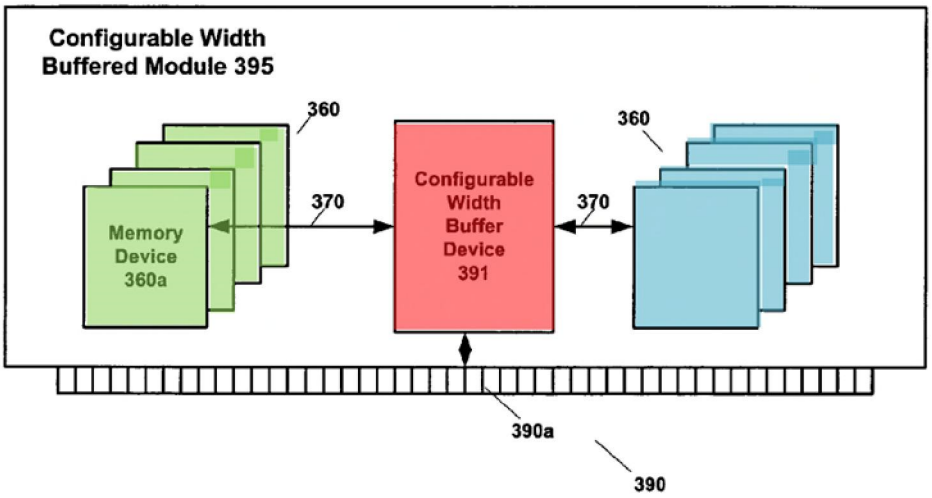


Fig. 3C

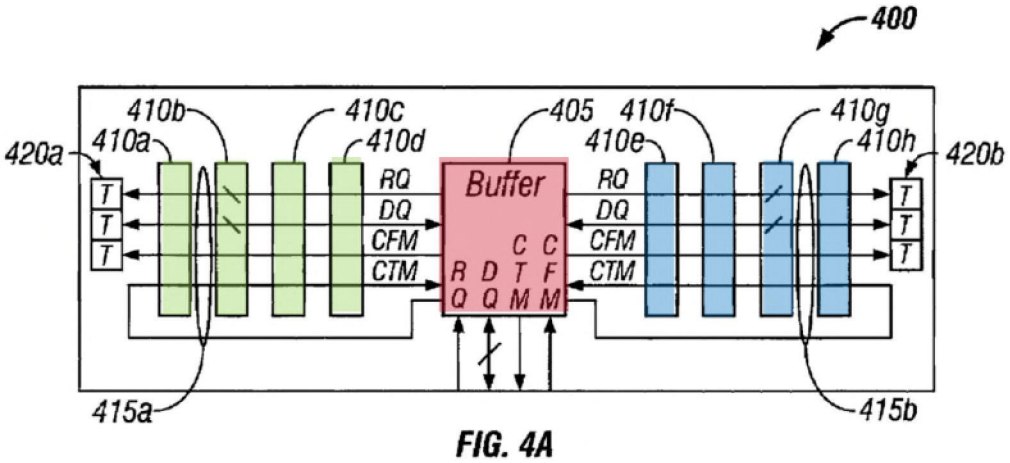


FIG. 4A

EX1071, Figs.3C, 4A.

Furthermore, Perego discloses that "[a]ny number of channels 415a-415d, for example[] two channels 415c and 415d may transfer information

simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations." *Id.*, 21:16-20. In such an implementation, shown below, a POSITA would understand that the memory devices coupled to channels 415c/d form one rank (green, "*first rank*"), and the memory devices coupled to channels 415a/b form another rank (blue, "*second rank*"). EX1003, ¶270; EX1071, Fig.4B (below); *see also id.* Fig.4C (further below, using different channel numbering, with 415a/b referring to the top channels and 415c/d referring to the bottom channels). Indeed, Netlist has previously conceded that Perego discloses two such "*ranks*" (e.g., 415a/b and 415c/d, shown below). EX1019, p.43; EX1020, ¶¶93-94; EX1003, ¶271.

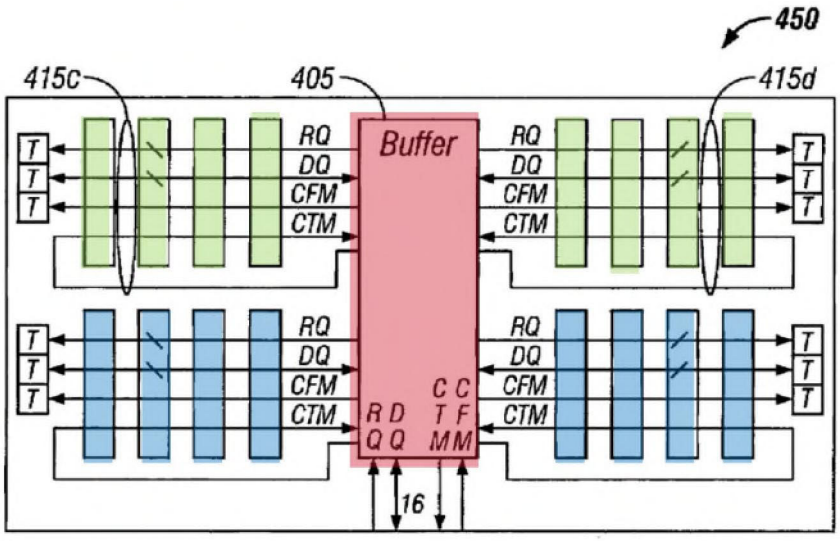


FIG. 4B

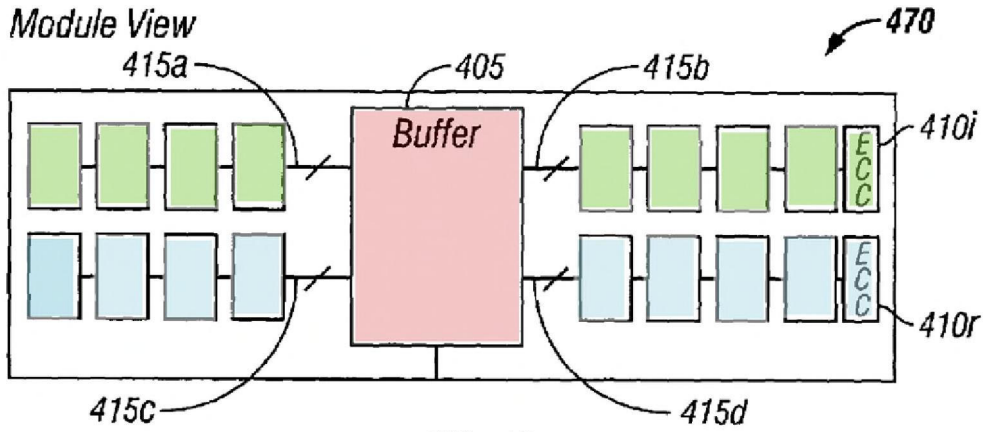


FIG. 4C

EX1071, Figs.4B-4C.

As shown above, each "*rank*" (green, blue) includes "*at least one...memory integrated circuit.*" EX1071, 15:37-45, Figs.3B (memory devices 360), 4A-4C (memory devices 410); EX1003, ¶272.

Finally, it would have been obvious to a POSITA to arrange Perego's DDR memory devices into "*ranks*," and a POSITA would have been motivated to do so, in light of the JEDEC standards. EX1003, ¶¶273-275; EX1064, p.6 ("Chip Select...provides for external ***Rank*** selection on systems with multiple ***Ranks***"); EX1062, p.13 (showing "x64 DIMM" with two "*ranks*," referred to as "physical banks," *see* pp.27-30, each with eight x8 memory devices, and each with its own chip-select signal, RS0 and RS1). Implementing such ranks in Perego's module would have been well within the level of ordinary skill. EX1003, ¶274 (citing, e.g., EX1072, Fig.1 (Matsui1, below, showing details of wiring DDR SDRAMs to a central buffer in DIMM format)).

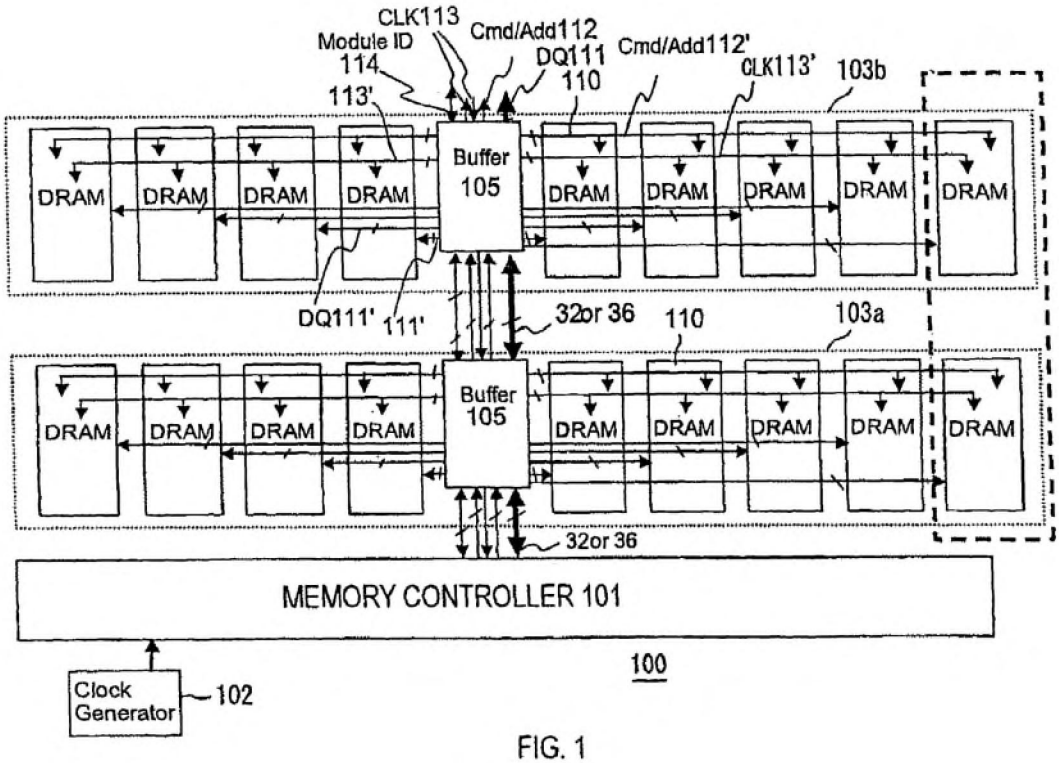


FIG. 1

(2) [1.d.2]-[1.d.3] First and Second Rank

Ground 1 teaches "*wherein the first rank* [green, below] *is selected to receive* [in response to a write command] *or output* [in response to a read command] *the first data burst* [from [1.a.3] (pp.42-46)] *in response to the first memory command* [from [1.a.3] (pp.42-46)] *and is not selected to communicate data with the memory controller in response to the second memory command* [from [1.a.3] (pp.42-46)]" and "*wherein the second rank* [blue, below] *is selected to receive or output the second data burst* [from [1.a.3] (pp.42-46)] *in response to the second memory command* [from [1.a.3] (pp.42-46)] *and is not selected to*

communicate data with the memory controller in response to the first memory command [from [1.a.3] (pp.42-46)]." EX1003, ¶¶283-303.

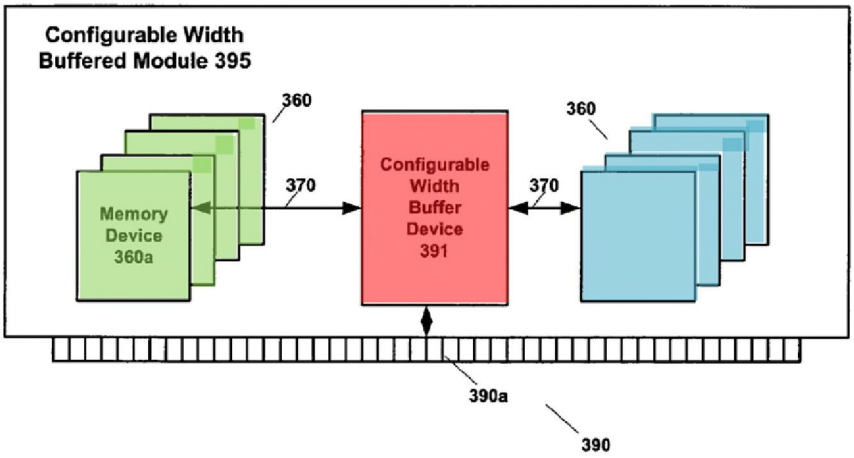


Fig. 3C

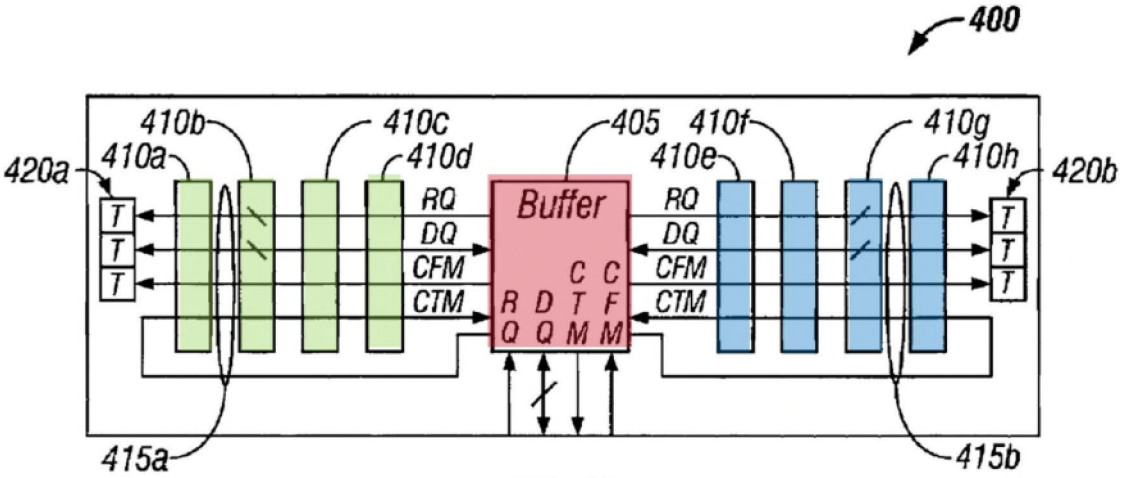


FIG. 4A

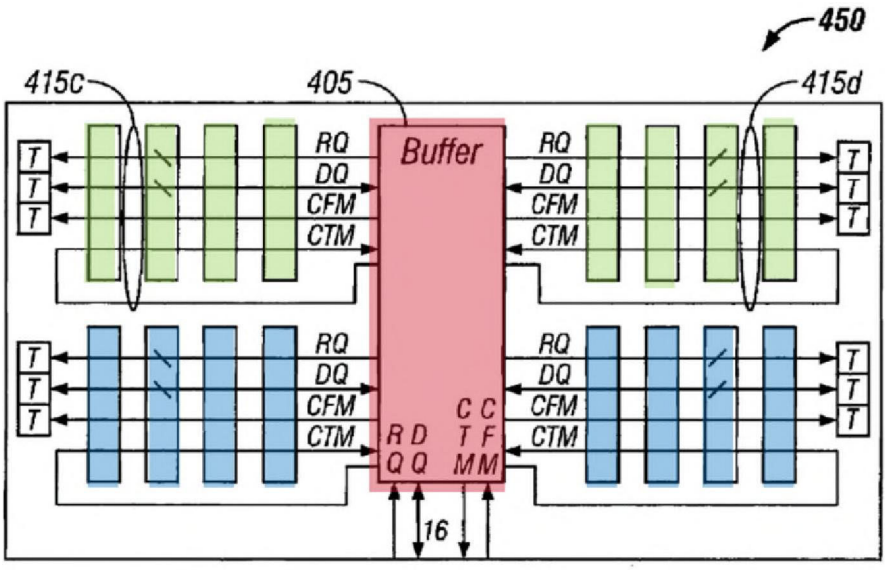


FIG. 4B

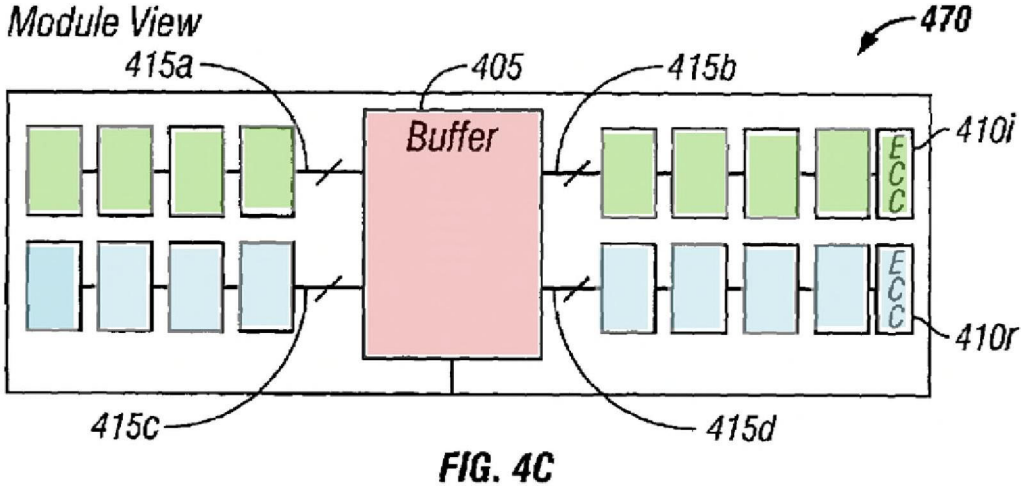


FIG. 4C

EX1071, Figs.3C, 4A-4C.

Perego's buffer device (red, above and below) responds to a read or write command by selecting a target subset of memory devices, e.g., a "*rank*," and routes the data through a corresponding "datapath" to that rank of memory devices (e.g., green or blue above) and not the other rank(s) of memory devices. EX1003,

¶¶285-286, 299-302; EX1071, 6:21-22 ("Buffer device 350...receives the data via ***one***...of channels 370."), 11:56-61 ("route data"), 15:31-45 ("datapath" to "target subset" of memory devices), 21:16-20 (other memory devices "remain in a ready or standby state until called upon to perform memory access operations"), Figs.5A-5B.

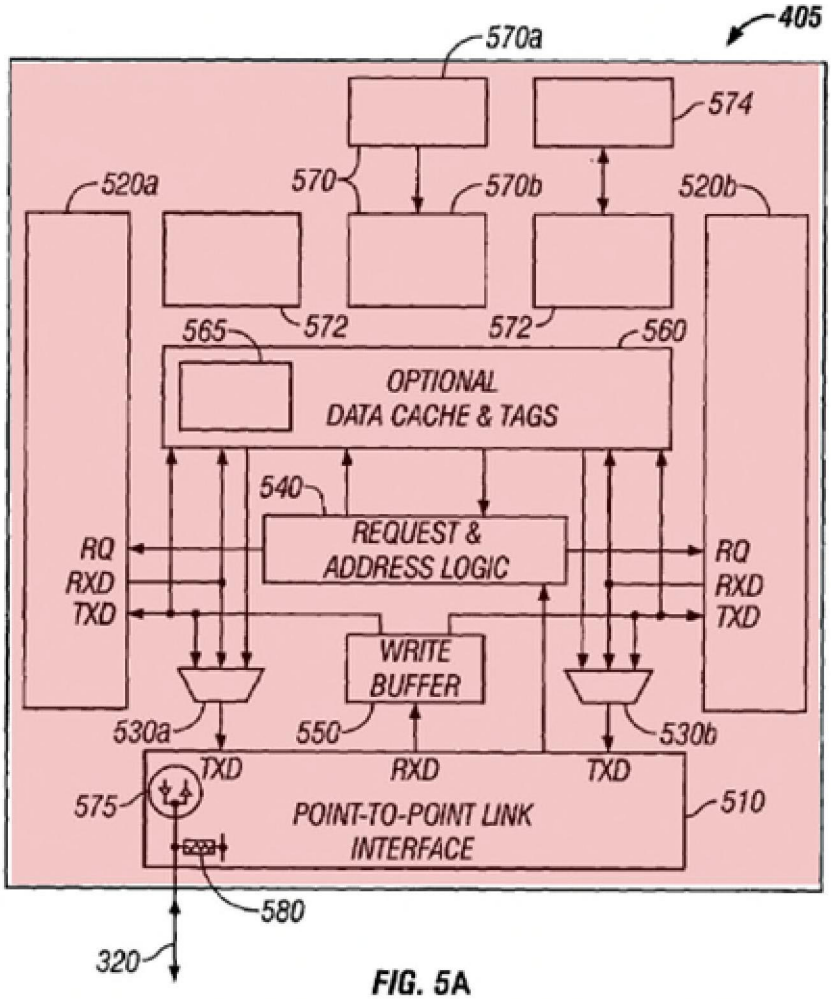


FIG. 5A

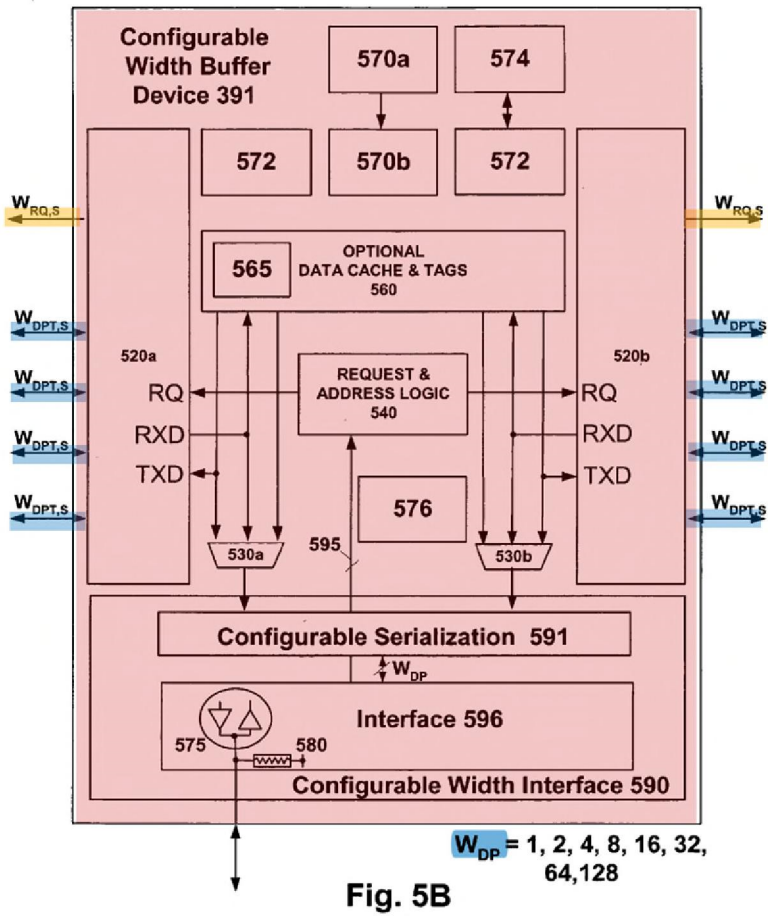
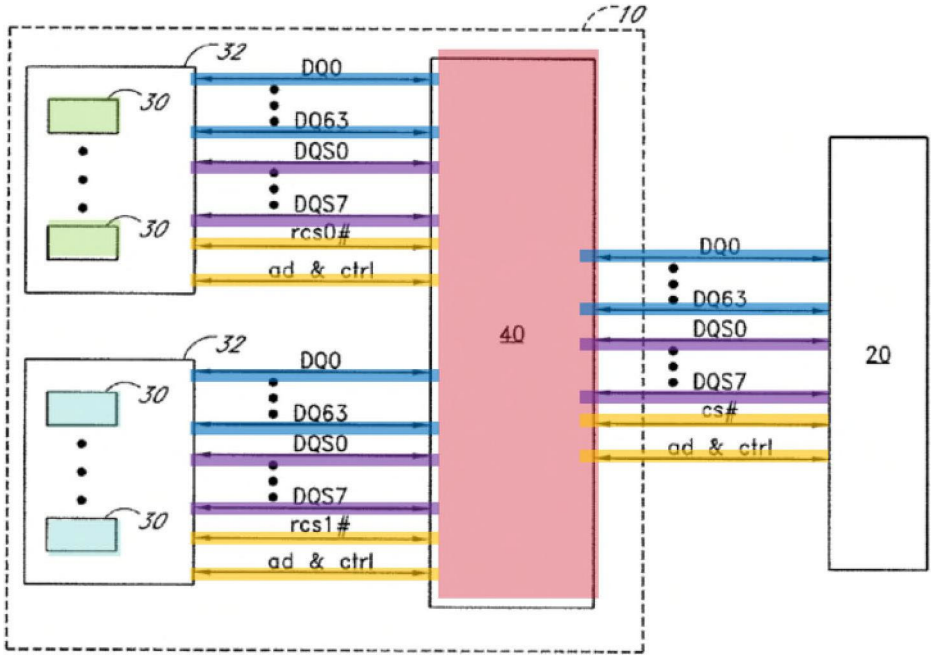


Fig. 5B

EX1071, Figs.5A-5B.

Perego's disclosure above satisfies the express claim language requiring that the second rank is ***not*** selected to communicate data with the memory controller in response to the first memory command while the first rank is receiving or outputting the data signals (and vice versa), *see* EX1003, ¶¶288, 295, consistent with [1.f.1]-[1.f.2] below (pp.76-80), *see* EX1003, ¶296, and consistent with the 215 Patent's disclosure that different ranks (green and blue, below) are on different

"forks" of the data path (blue DQ data lines, and purple DQS strobe lines, below, from buffer 40, red), *see* EX1003, ¶297:



EX1001, Fig.1. As shown above and below, the 215 Patent discloses that data and strobe signals output or received by one rank are ***not*** received or output by the other rank because they are on separate data paths, thus avoiding collisions. EX1003, ¶298; EX1001, 13:36-49; *see also id.* Fig.8C (below).

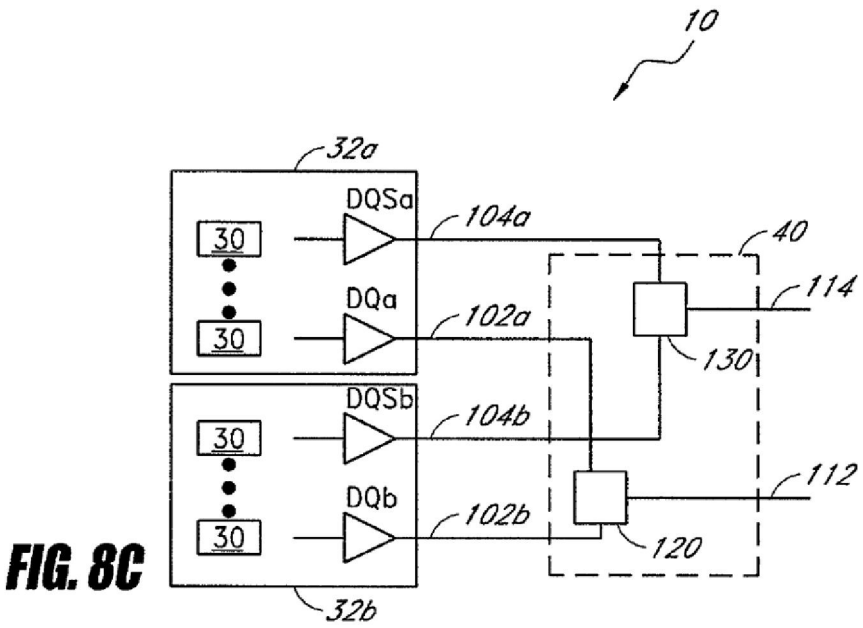
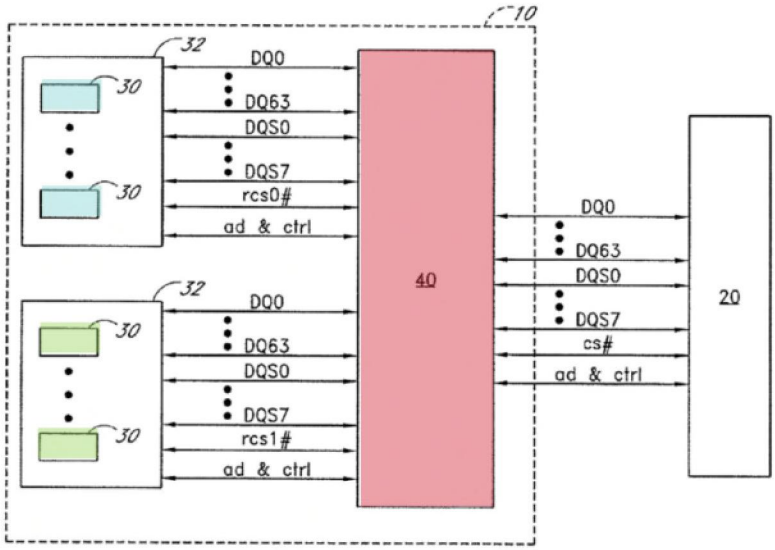


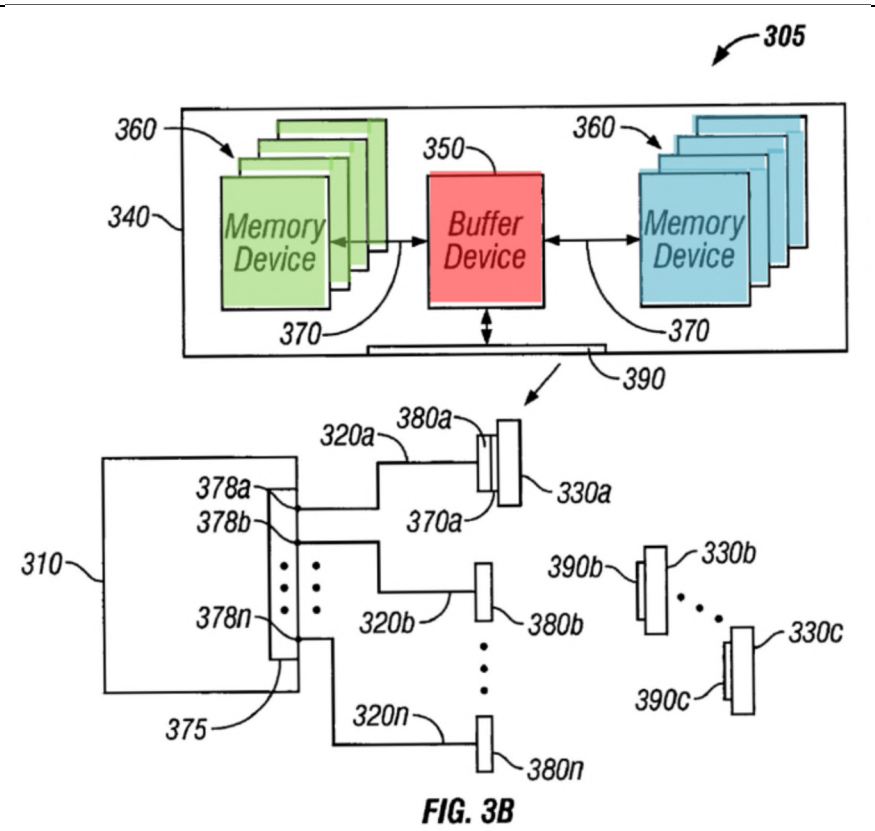
FIG. 8C

Like the 215 Patent, Perego teaches a separate data path for each rank (e.g., green, blue) as discussed above (pp.64-67).

In district court, Netlist appears to advance an unduly broad construction permitting the two ranks to ***share*** the same data lines on the module (rather than being on separate "forks"). *See* EX1085, pp.39-41; EX1003, ¶289. This arrangement was also well known and is similar to the arrangement disclosed in the prior-art JEDEC standards. *See, e.g.*, EX1062, p.16 (showing two ranks connected to chip-select signals RS0 and RS1, respectively, where the memory devices in the two ranks, e.g., D0 and D18, are connected to the same DQS data strobes and the same DQ data signals); EX1064, pp.4-5 (similar, for stacked memory device, with chip-select signals CS0 and CS1); EX1003, ¶290. A

POSITA would have recognized that Perego also renders obvious this limitation under Netlist's broader construction. EX1003, ¶291. Indeed, Perego discloses the same memory module structure as the 215 Patent:

215 Patent (EX1001, Fig.1)	 FIG. 1

Perego (EX1071), Fig. 3B	 FIG. 3B

Thus, if the primary embodiment shown in Figure 1 of the 215 Patent (above) is not excluded from the scope of the claim, Perego satisfies the claim because Perego similarly discloses a separate data channel to each rank (e.g., 370 above) and that one rank is selected to communicate data while the other rank(s) are not, as discussed above (pp.64-67). EX1003, ¶¶291-292.

If Netlist argues that the claim requires a single data channel to both ranks (as in the prior-art JESD21-C standard, *see, e.g.*, EX1062, p.16), Perego discloses that implementation as well, where a single channel is used to access two memory devices (e.g., 652 and 653, below) in two different ranks (green and blue, below)

coupled to the same data lines (e.g., DQ3 and DQ4). EX1003, ¶¶293-294; EX1071, 10:14-15, Fig.5E.

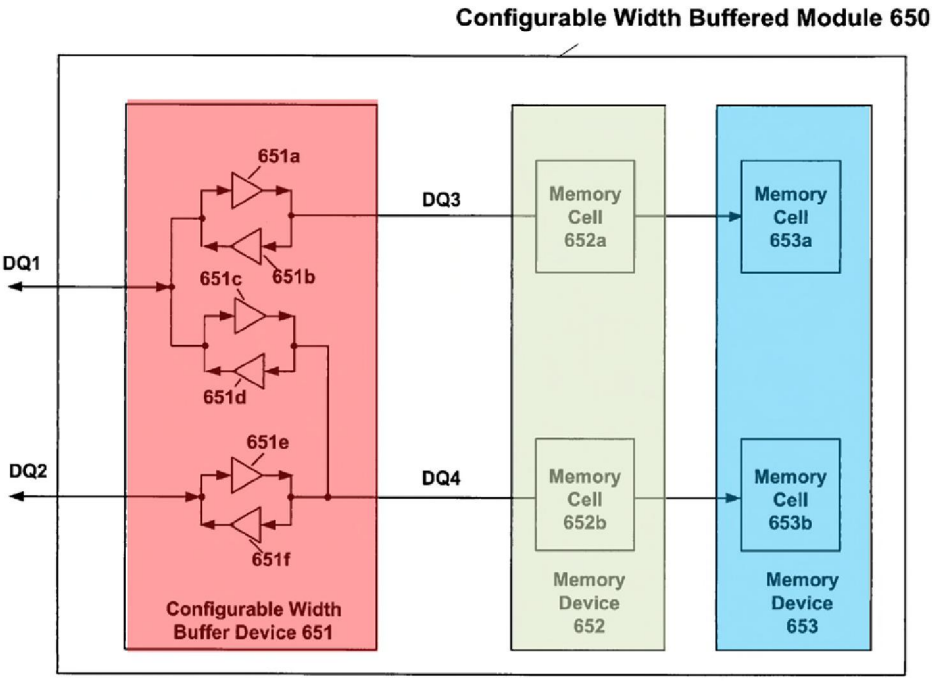


Fig. 5E

EX1071, Fig.5E. In this arrangement, a POSITA would have understood that, because the data lines are shared by multiple SDRAM memory devices, each rank of memory devices would receive a separate chip-select signal that selects the memory devices in that rank, similar to the prior-art JEDEC standard. EX1062, p.16 (showing a two-rank module having two chip-select signals, RS0 and RS1, each coupled to a respective rank of memory devices); EX1069, pp.2-3 (similar); EX1003, ¶294.

e) [1.e] Buffer

Ground 1 teaches "*a buffer*[3] [red, below, including circuitry in Perego's buffer device (e.g., buffer device 391 in Figures 3C/5B, and buffer device 405 in Figures 4A-4B, 5A) for buffering and/or routing data signals in interfaces 520a and 520b, multiplexers 530a and 530b, and interfaces 510 or 590] *coupled between the at least one first memory integrated circuit* [in the "*first*" rank from [1.d.1] (pp.54-63), e.g., a rank coupled to interface 520a] *and the memory bus* [from [1.a.2] (pp.37-42), coupled to interface 510 or 590]*, and between the at least one second memory integrated circuit* [in the "*second*" rank from [1.d.1] (pp.54-63), e.g., a rank coupled to interface 520b] *and the memory bus.*" EX1003, ¶¶304-311.

[3] The intrinsic evidence shows that the "*buffer*" does not need to be a physically separate component from the "*register*" in [1.c] (pp.48-54). EX1003, ¶306; EX1001, 37:27-31 (claim 1, "a register...configured to...buffer"), 38:35-39 (claim 8, "the buffer comprises...registers"), 9:26-31 (memory module 10 operates as having a "buffer"), 14:37-57 ("register 230 [in memory module 10]...buffers"), 16:12-14 (same), Fig.1; *see also id.* 5:38-43, 6:48-51.

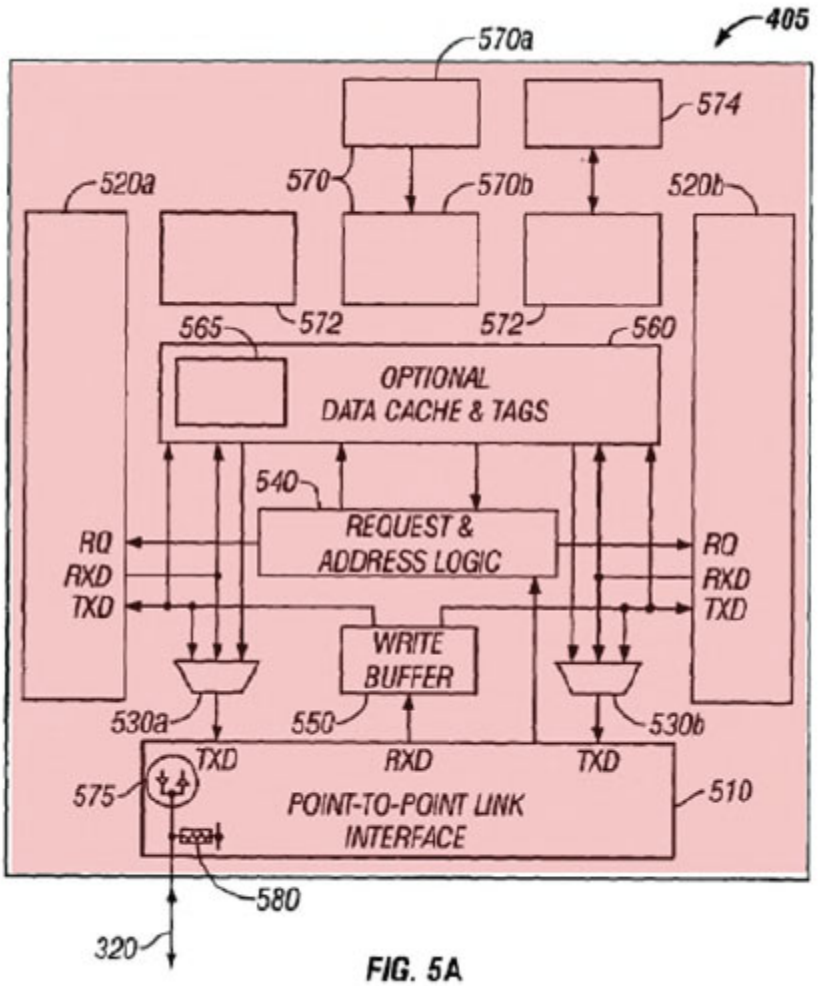

405
570a
574
520a
570
570b
520b
565
572
572
560
OPTIONAL
DATA CACHE & TAGS
540
REQUEST &
ADDRESS LOGIC
RQ
RXD
TXD
RQ
RXD
TXD
WRITE
BUFFER
530a
550
530b
TXD
RXD
TXD
575
POINT-TO-POINT LINK
INTERFACE
510
580
320

FIG. 5A

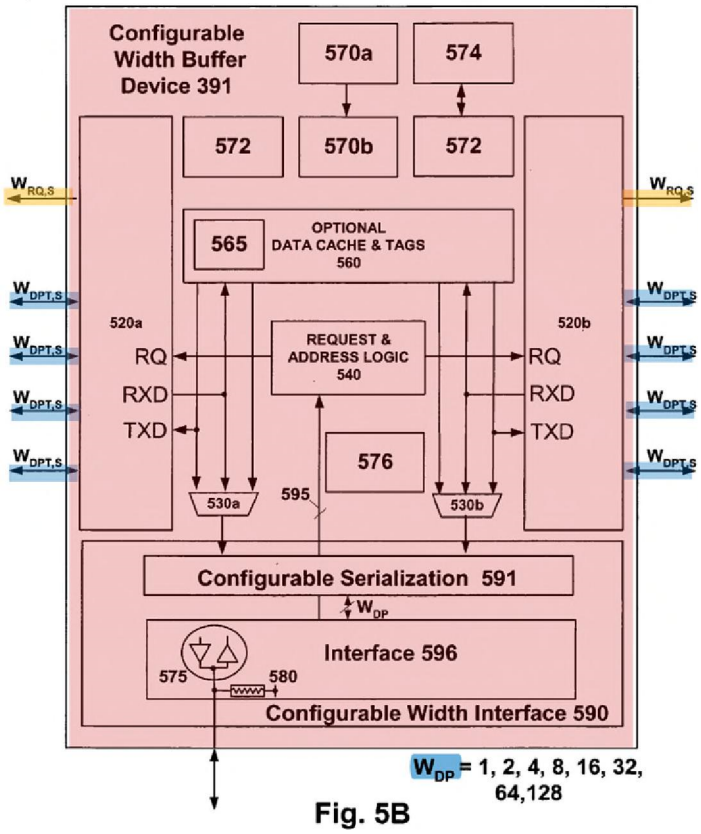


Fig. 5B

Perego's "*buffer*" device (red, above) "isolate[es]" signals, including data signals, thus isolating the memory controller from signals interfacing with the memory devices. *See, e.g.*, EX1071, Figs. 5A-5B (above), 4:38-42 ("buffer device...isolating data...signals"), 6:12-15 (buffer device 350 in Figs.3A-3B), 11:1-7 (buffer device 405 in Fig.5A), 13:6-10 (buffer device 391 in Fig.5B); *see also id.*, 7:30-34, 10:59-67 (buffer device 391/405 from Figs.5A-5B can be the buffer device in memory systems 300/305 in Figs.3A-3B); EX1003, ¶¶308-309.

Furthermore, a POSITA would have understood that the circuitry for handling data signals in interfaces 520a/b, multiplexers 530a/b, and interface 510

or 590, is a "*buffer*" because it includes data buffers, e.g., transceivers 575 in interface 510 or 590, and transceivers in interfaces 520a/b, which can include latches (e.g., blue, below) that buffer the data signals. EX1071, 13:18-24, 14:65-15:2, Fig.5C (below, showing input/output latches 597f-m for data signals), 17:61-63, 18:65-19:3; EX1003, ¶310.

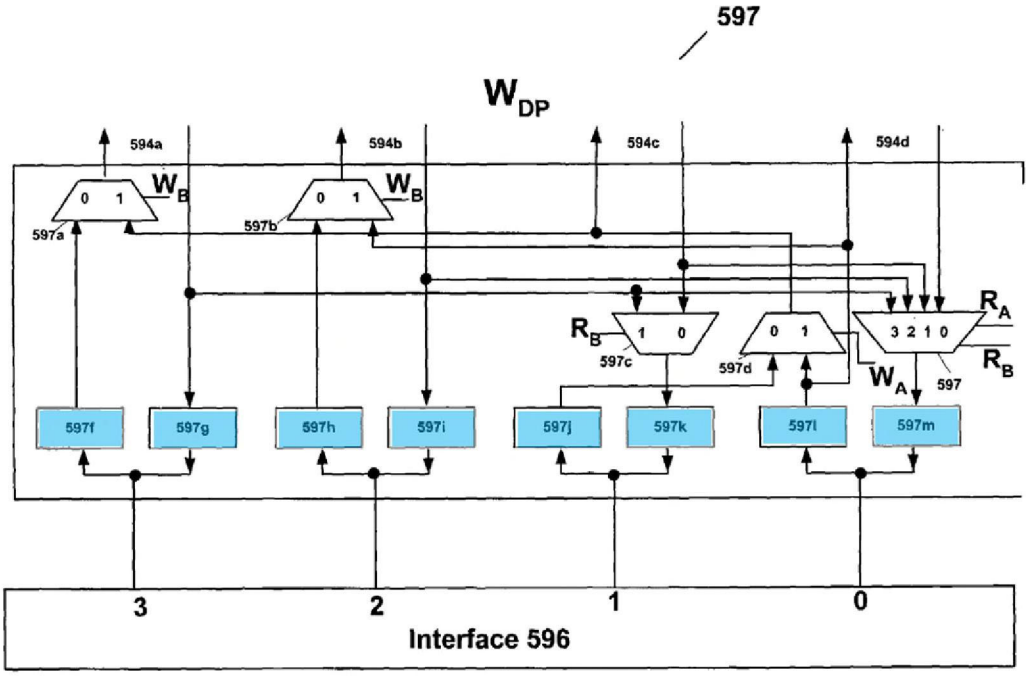


Fig. 5C

f) [1.f.1]-[1.f.2] Logic

Ground 1 teaches "*logic* [e.g., request & address logic 540; logic in the interface to the system memory controller (interface 590 or 510); logic in interfaces 520a/520b to the memory devices; and logic in computation block 565, all shown below in Figs.5A-5B] *coupled to the buffer* [from [1.e] (pp.73-76)] *and*

configured to respond to the first memory command [write or read, from [1.a.3] (pp.42-46)] *by providing first control signals to the buffer to enable communication of the first data bust between the at least one first memory integrated circuit* [in the "*first*" rank] *and the memory controller* [310] *through the buffer*," and "*wherein the logic is further configured to respond to the second memory command* [e.g., subsequent write or read, from [1.a.3] (pp.42-46)] *by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals* [e.g., because the "*first*" rank is selected to receive or output a "*first*" data burst, and the "*second*" rank is selected to receive or output the "*second*" data burst, where the "*first*" and "*second*" ranks are coupled to different channels of Perego's buffer device as explained for [1.d.1]-[1.d.2] (pp.54-72)]." EX1003, ¶¶312-324.

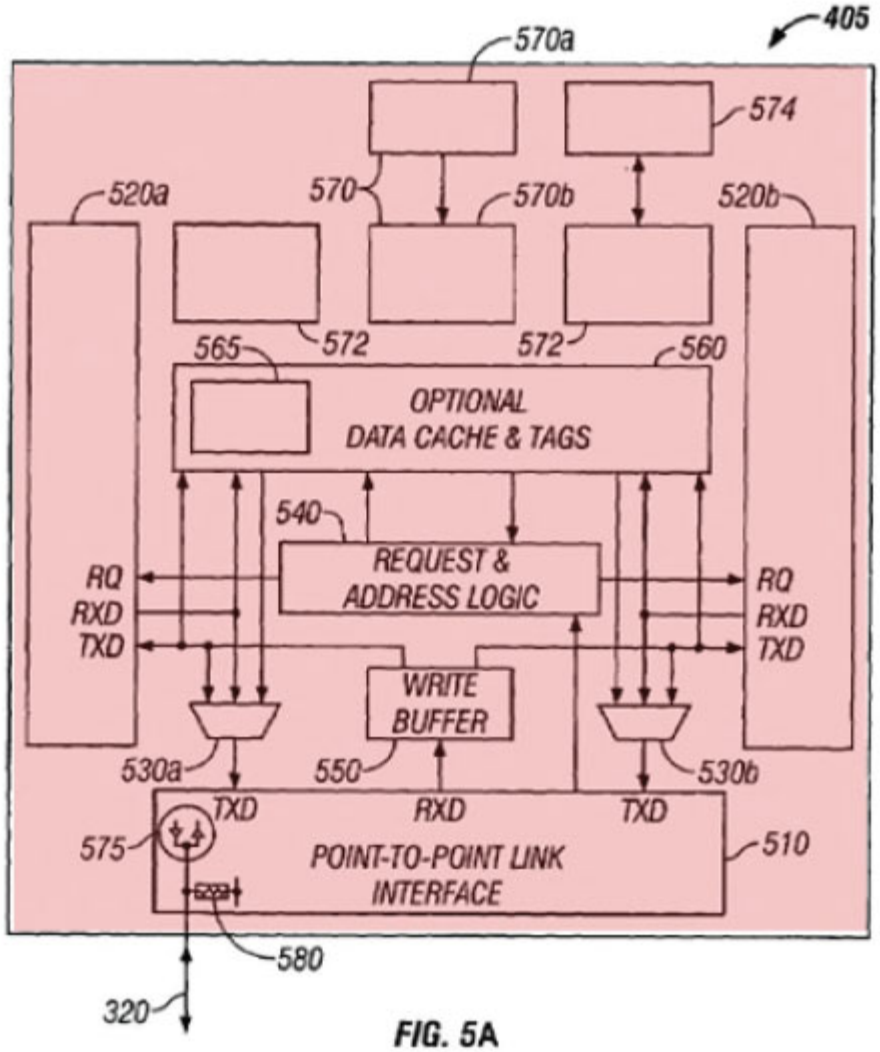

405
570a
574
520a
570
570b
520b
565
572
572
560
OPTIONAL
DATA CACHE & TAGS
540
REQUEST &
ADDRESS LOGIC
RQ
RXD
TXD
RQ
RXD
TXD
WRITE
BUFFER
530a
550
530b
TXD
RXD
TXD
575
POINT-TO-POINT LINK
INTERFACE
510
580
320

FIG. 5A

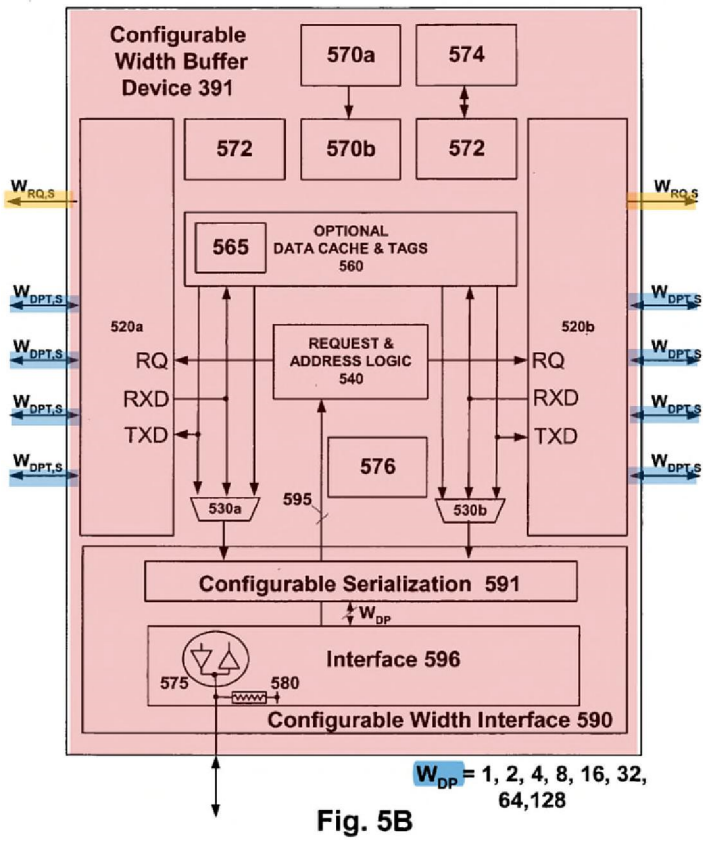


Fig. 5B

As explained for [1.a.2]-[1.a.3] (pp.37-46) and [1.d.2]-[1.d.3] (pp.63-72), Perego's data bursts are selectively routed through the buffer device to/from the targeted "*rank*" of memory devices and to/from the memory controller, and a POSITA would have understood that the buffer device's logic sends "*control signals*" to interfaces 520a/b to activate only the channel transferring the data burst between the memory controller and the targeted rank. EX1003, ¶¶315-317; EX1071, 11:56-61 ("route data"), 6:15-25 ("data via one or more of channels 370"), 12:9-12 (computation block 565), 13:54-59 (request & address logic 540),

21:16-20 (other channels "remain in a ready or standby state"), 15:40-45 (not using all channels "reduce[s] power consumption").

Furthermore, a POSITA would have understood that, because interfaces 520a/b, 510, and 590 include transceivers (e.g., 575), and because multiplexer/demultiplexer circuit 597 (e.g., in 591) contains "multiplexing logic and demultiplexing logic," Perego's buffer device includes logic that sends "*control signals*" to the transceivers, multiplexing/demultiplexing circuits, and to the input and output latches to selectively activate those circuit elements of the buffer according to the targeted rank and direction of the read and write operations. EX1003, ¶¶318-319; EX1071, 14:62-15:6 ("The address…will determine which target subset of channels 370 will be utilized for the data transfer…"), 17:41-44 ("multiplexing logic is used during read operations, and the demultiplexing logic is used during write operations"), 17:6162, Figs.5A-5B. For example, the targeted rank can be determined by the logic using the address information, in addition to the input chip-select signals, when Perego's module implements rank multiplication (as discussed above, pp.10-12). EX1003, ¶319; EX1071, 14:63-65, 15:34-40.

3. Claim 2

Ground 1 teaches "*[t]he memory module of claim 1, wherein the buffer* [from [1.e] (pp.73-76)] *is configured to isolate both the at least one first memory*

integrated circuit and the at least one second memory integrated circuit from the memory bus [from [1.a.2] (pp.37-42)] *when the memory module is not being accessed by the memory controller*." EX1003, ¶¶325-331. For example, as explained for [1.e] (pp.73-76), Perego's "*buffer*" "isolate[es]" the memory controller from the data signals interfacing with the memory devices, EX1071, 6:12-15, and only "access[es]" the targeted memory devices, *id.*, 15:31-45, with all other "memory devices...in a ready or standby state until called upon to perform memory access operations," *id.*, 21:16-20, making it obvious to "*isolate*" all the memory devices "*when the memory module is not being accessed by the memory controller*," EX1003, ¶¶328-330. Such isolation also would have been obvious because Perego discloses the advantages of isolation, including "reduced power" and "power savings." EX1071, 15:31-45, 20:42-47; EX1003, ¶330.

4. Claim 3

Ground 1 teaches "*[t]he memory module of claim 1, wherein the memory module has an overall CAS latency* [e.g., 4 clock cycles] *greater than an actual operational CAS latency of each of the plurality of memory integrated circuits* [e.g., 3 clock cycles]," so that the buffer has enough time (e.g., 1 clock cycle) to perform its functions. EX1003, ¶¶332-338. Under the JEDEC standards, "an additional clock cycle" is added to the "CAS latency" of the memory devices to leave enough time for the register on the DIMM to perform its functions. *See*

EX1062, p.68 n.1; EX1064, pp.12 ("CAS Latency" of 2, 3, 4, or 5 clock cycles), 14 (permitting additional "Additive Latency" of 1 clock cycle); EX1003, ¶¶334-336. It would have been obvious to add one additional clock cycle to Perego for the same reason, i.e., so that the memory module complies with the timing of the JEDEC standards, and so the buffer has enough time to perform its functions (including latching the data signals for interfaces 520a/b with 597f-m, blue, below) using "internal" clock circuit 570a-b (purple, below). EX1003, ¶¶335-337; EX1071, 18:65-19:3, 17:61-63, 12:65-13:5, Figs.5B-5C.

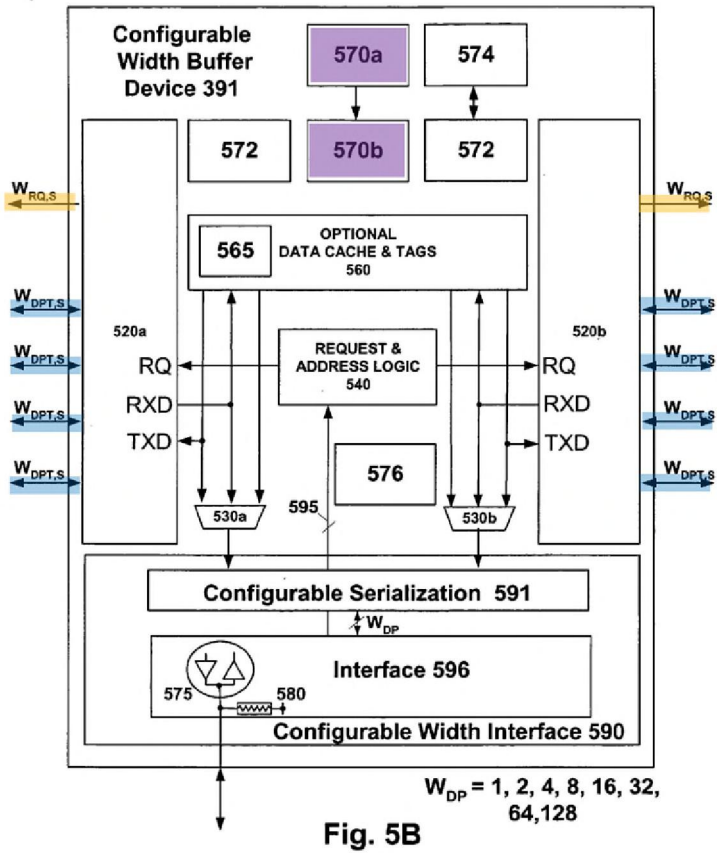


Fig. 5B

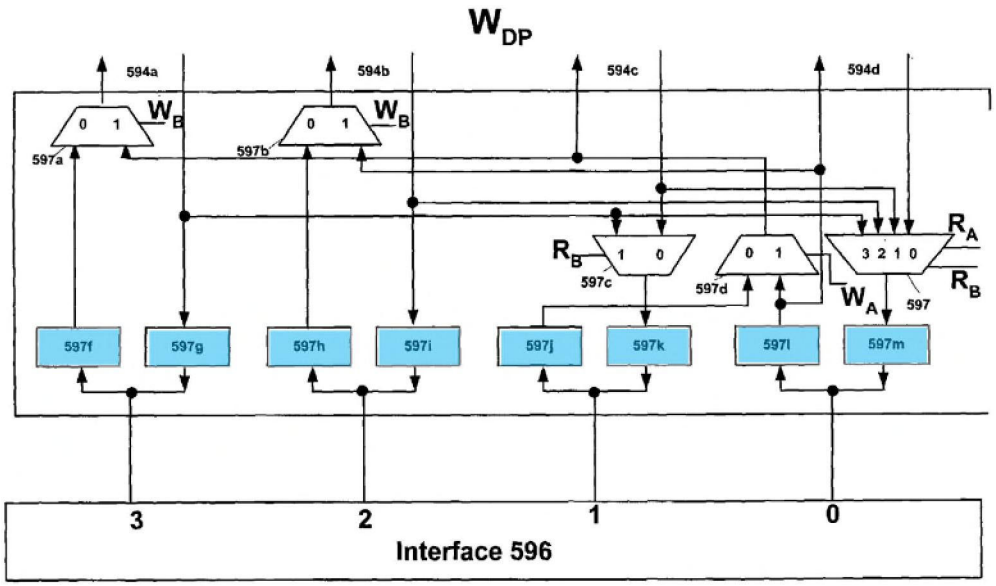


Fig. 5C

5. Claim 4

Ground 1 teaches "*[t]he memory module of claim 1, further comprising an SPD device* [which is standard on JEDEC-compliant memory modules, EX1071, Abstract ("SPD"), 12:20-34 ("serial presence detect (SPD)"), 15:52-53 ("SPD"); EX1062, p.68 ("Serial Presence Detect")] *that reports an overall CAS latency of the memory module to the memory controller* [e.g., during initialization, EX1071, 12:20-34 ("latency values"), 15:52-53, 16:1-5, Abstract]*, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits* [as explained for claim 3 (pp.81-83)]." EX1003, ¶¶354-358.

6. Claim 5

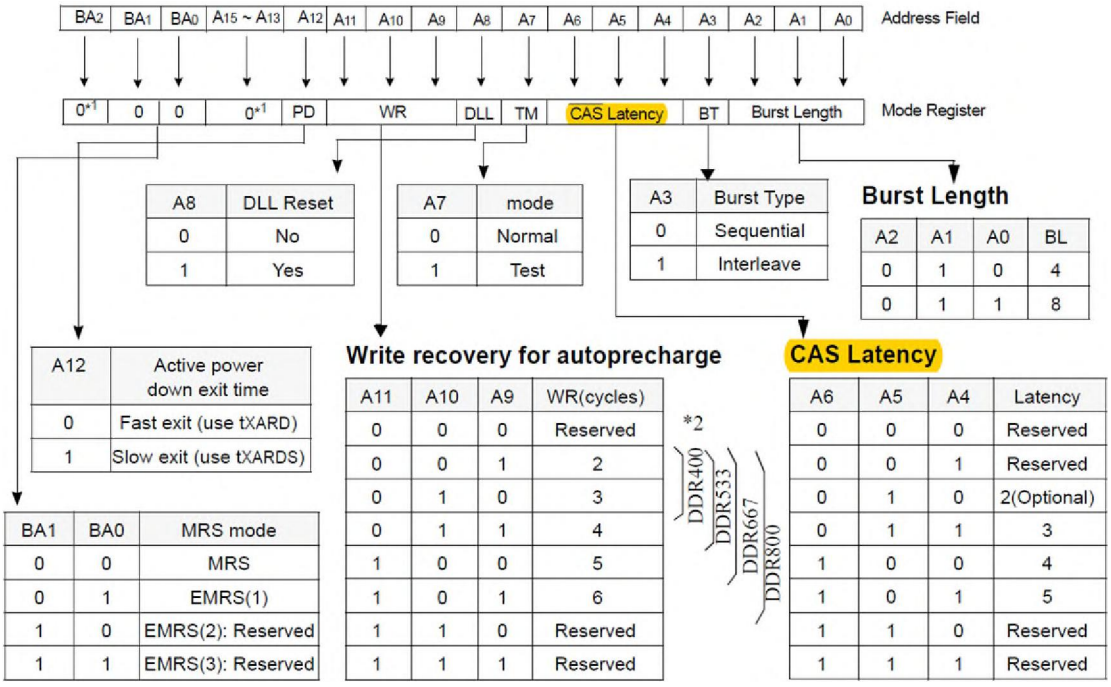
Ground 1 teaches "*[t]he memory module of claim 1, wherein the memory module is a dual in-line memory module (DIMM)* [as discussed for [1.b] (pp.46-48)]*, and wherein the plurality of memory integrated circuits are double-data-rate* [DDR or DDR2, *see* EX1060/EX1062, EX1064/EX1066] *dynamic random access memory (DRAM) circuits* [as discussed for [1.d.1] (pp.54-63)]." EX1003, ¶¶364-368; *see also* EX1073, [0046] ("SDRAM DDR1 and DDR2"), [0052] ("DIMMs"); EX1078, 2:8-9 ("DIMM"), 9:56-59 ("(DDR) SDRAM").

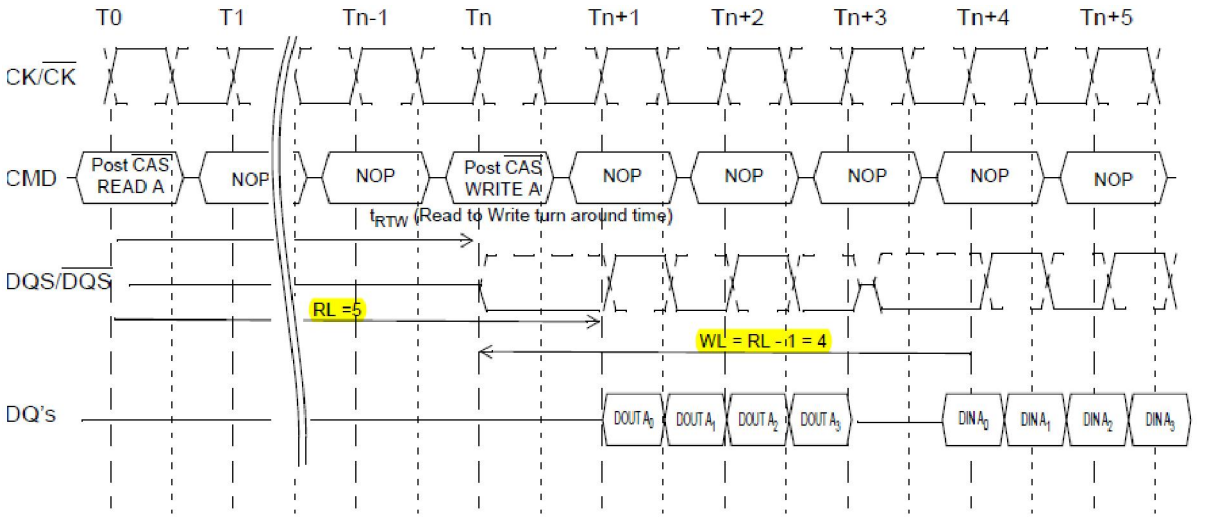
7. Claim 6

Ground 1 teaches "*[t]he memory module of claim 1, further comprising determining a latency value* [as discussed for claims 3-4 (pp.81-83)]*, wherein the communication of the first data burst between the at least one first memory integrated circuit and the memory controller is enabled in accordance with the latency value* [e.g., per the JESD79-2 standard, as discussed below]." EX1003, ¶¶369-381.

Perego discloses providing "access latency values" to the memory controller during initialization, EX1071, 12:20-34, Fig.5B, and a POSITA would have known from the JEDEC standards (including JESD79-2, shown below) that the data transfers in Perego's memory module are enabled in accordance with these "access latency values," including CAS latency (expressed in terms of an integer number

of clock cycles), which are programmed during initialization by the memory controller and used to properly time burst operations to comply with the JEDEC standards, *see* EX1064, pp.12 (first below, showing CAS latency), 14 (Additive Latency), 26 (Read Latency (RL)=Additive Latency (AL), if any, plus CAS Latency (CL)), 28 (second below, showing timing of burst in accordance with latency values). EX1003, ¶¶373-378.





The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation.

Figure 26 — Burst Read Followed by Burst Write: RL = 5, WL = (RL-1) = 4, BL = 4

The Board has previously concluded, in finding claims unpatentable from a family member of the 215 Patent, that it would have been obvious to a POSITA to enable data communications in accordance with a CAS latency value to ensure proper data transfer. *See* EX1030, pp.3 (last limitation), 7-14. That finding is now binding against Netlist, as explained above (p.20).

Furthermore, as discussed above for claims 3-4 (pp.81-83), a POSITA would have understood that any scheduled data transfer to or from the memory module must account for the latency of the ***entire*** module, including the latency of the memory devices combined with the latency added by the buffer device (red, below, which sits between the memory devices and the memory controller). EX1003, ¶¶379-380.

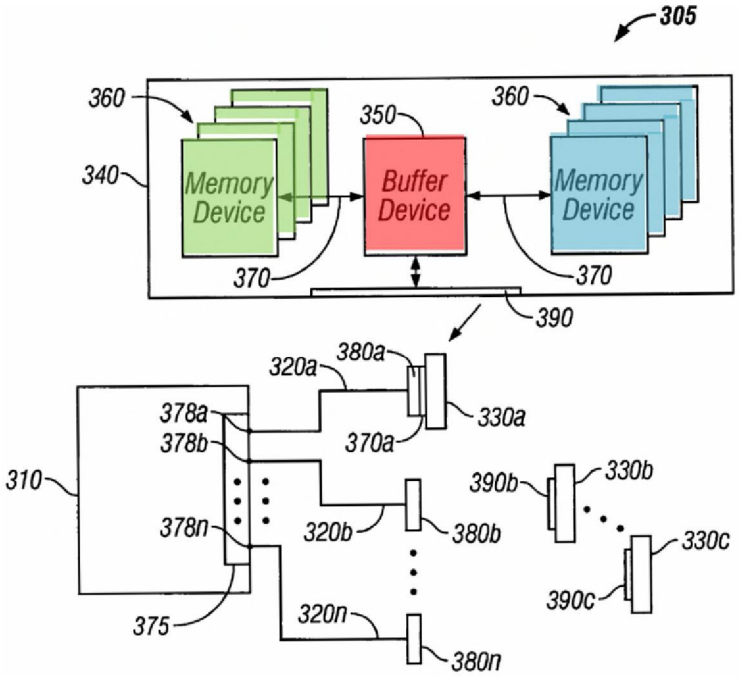


FIG. 3B

8. Claim 7

a) [7.a] On-Die-Termination (ODT) Bus

Ground 1 teaches "*[t]he memory module of claim 1, wherein the memory module is further coupled to the memory controller using an on-die-termination (ODT) bus* [e.g., per the JESD79-2 standard, as discussed below]." EX1003, ¶¶383-388.

When implementing Perego with DDR2 memory devices, as discussed above for [1.d.1] (pp.54-63), it would be obvious to include an ODT bus because that is a standard way for the memory controller to control the ODT circuit in DDR2 memory devices to turn on/off termination resistance for signals, including data (DQ) and strobe (DQS) signals, according to JEDEC standards, including

JESD79-2 (shown below). EX1064, p.6 (first below), pp.18-22 ("On Die Termination"); EX1066, p.7 (second below); EX1003, ¶¶383-386.

1.2 Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, and $\overline{DM}$ signal for x4x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, UDM, and $\overline{LDM}$ signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.

Registered DIMM Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0	IN	Positive Edge	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM PLL.
$\overline{CK0}$	IN	Negative Edge	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM PLL.
CKE[1:0]	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
$\overline{S}$[3:0]	IN	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. These input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When both $\overline{S}$[0:1] are high, all register outputs (except CKE, ODT and Chip select) remain in the previous state. For modules supporting 4 ranks, $\overline{S}$[2:3] operate similarly to $\overline{S}$[0:1] for a second set of register outputs.
ODT[1:0]	IN	Active High	On-Die Termination control signals
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	IN	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.

Perego describes the importance of proper signal termination, which would further motivate a POSITA to couple the memory module to an ODT bus. EX1071, 11:26-36, 9:34-38; EX1003, ¶386.

b) [7.b] ODT Circuit

Ground 1 teaches "*wherein each of the plurality of memory devices including an ODT circuit,*" e.g., when using DDR2 memory devices, as explained for [7.a] (pp.87-88). EX1003, ¶¶389-391.

c) [7.c] Termination Circuit

Ground 1 teaches "*the memory module further comprising a termination circuit* [e.g., circuitry, logic and termination elements, such as termination 580 (below), in the buffer device] *external to any of the plurality of memory devices, wherein the termination circuit is coupled to the ODT bus* [from [7.a] (pp.87-88)] *and to the ODT circuit* [from [7.b] (p.89)] *of at least one of the plurality of memory devices*." EX1003, ¶¶392-397.

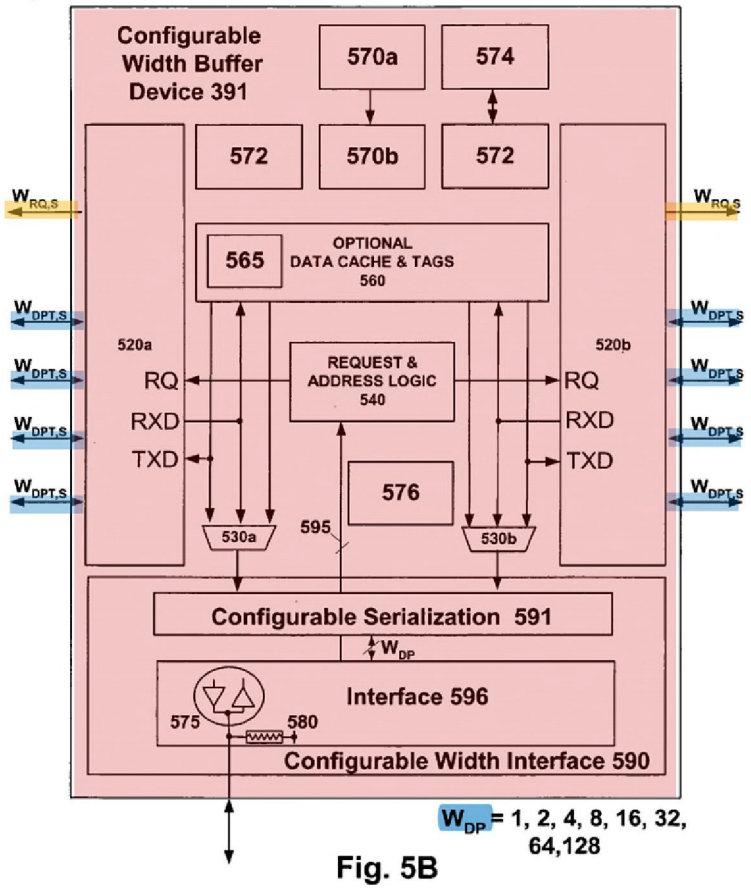


Fig. 5B

A POSITA would understand that the "*termination circuit*" in the buffer (red, above) is coupled to the "*ODT bus*" (to receive ODT signals from the memory controller) and to the "*ODT circuit*" of the DDR2 memory devices, in order to set the termination state in the DDR2 memory devices. EX1003, ¶¶393-395; EX1072 (Matsui1), Fig.19 (below, showing that a POSITA would understand that the termination circuit for the signals from the memory devices would be in the buffer device when it is what interfaces with the memory devices).

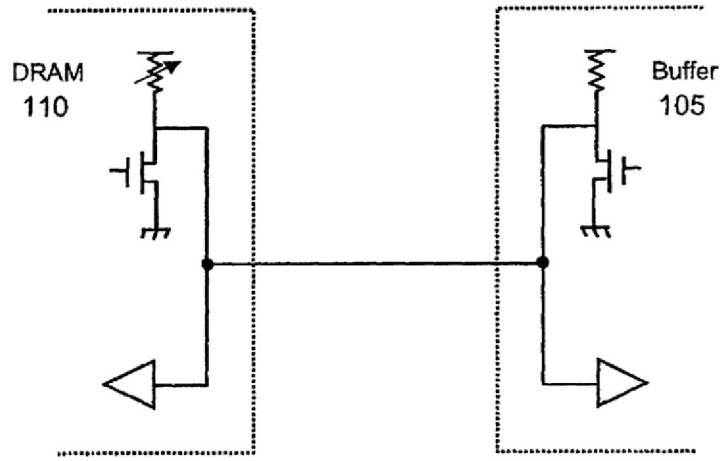


FIG. 19

A POSITA would have been motivated to control the "*ODT circuit*" in the DDR2 memory devices, as discussed above, to avoid reflections that would degrade the quality of the signals. EX1071, 9:6-12 ("to help reduce voltage reflections"); EX1068, pp.viii ("terminations can remove or reduce reflections"), 54-71 (discussing reflections); EX1003, ¶396.

d) [7.d] External Termination

Ground 1 teaches "*wherein the termination circuit* [from [7.c] (pp.89-91)] *is configured to provide external termination of the at least one of the plurality of memory devices* [e.g., the DDR2 memory devices coupled to interfaces 520a/b of the buffer, red, below] *in response to an ODT signal on the ODT bus* [from [7.a] (pp.87-88)]." EX1003, ¶¶398-404. A POSITA would have understood from Perego that the "*termination circuit*" is on the data path and is controlled in response to the "*ODT signal*" to properly terminate active signals on the corresponding channel connecting to the DDR2 memory devices (e.g., to reduce reflections, as discussed

for [7.c] (pp.89-91)). EX1071, 8:51-9:12, 5:4-6, 16:1721, 9:6-9, Fig.5B (below); EX1003, ¶¶400-402.

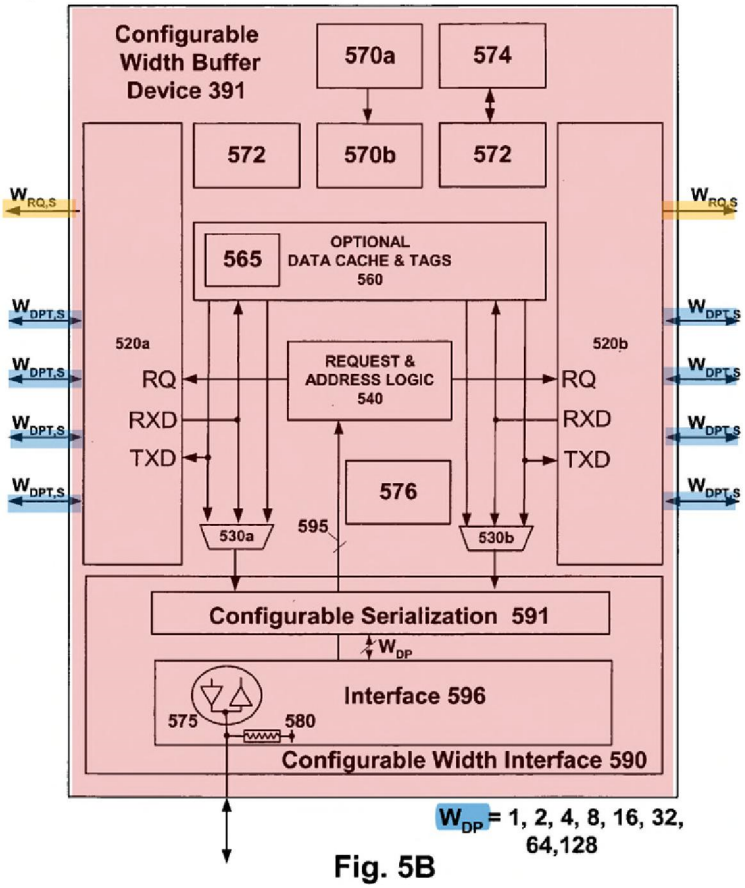


Fig. 5B

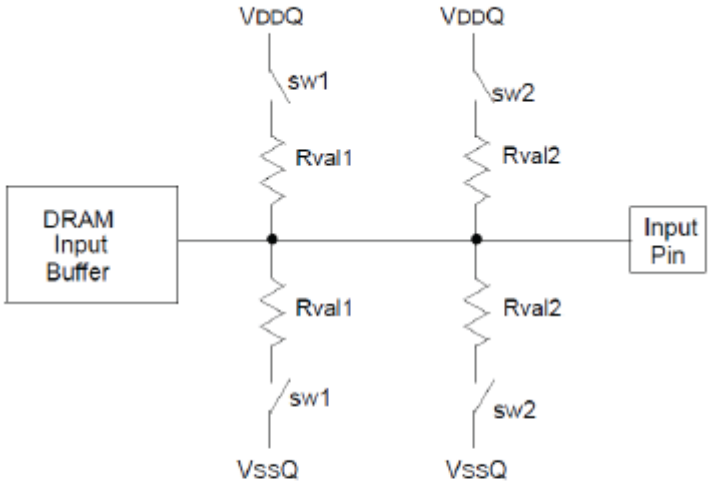
e) [7.e] ODT Circuit Disabled

Ground 1 teaches "*wherein the ODT circuit* [from [7.b] (p.89)] *in the at least one of the plurality of memory devices is disabled* [e.g., because that memory device is actively driving the data signal, or to optimize signal integrity]." EX1003, ¶¶405-410. The JESD79-2 standard allows each "*ODT circuit*" to be

"independently turn[ed] on/off" to "improve signal integrity of the memory channel," as shown below. EX1064, pp.18-19.

2.2.2.4 ODT (On Die Termination)

On Die Termination (ODT) is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQS/$\overline{\text{DQS}}$, RDQS/$\overline{\text{RDQS}}$, and DM signal for x4x8 configurations via the ODT control pin. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{\text{UDQS}}$, LDQS/$\overline{\text{LDQS}}$, UDM, and LDM signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

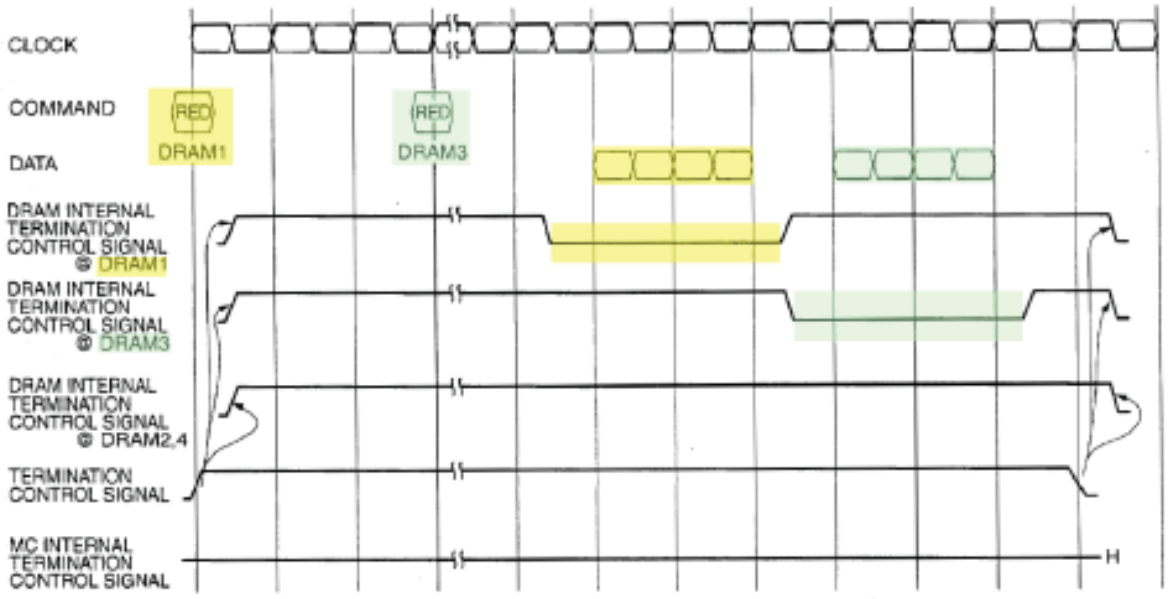


Switch sw1 or sw2 is enabled by ODT pin.
Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.
Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

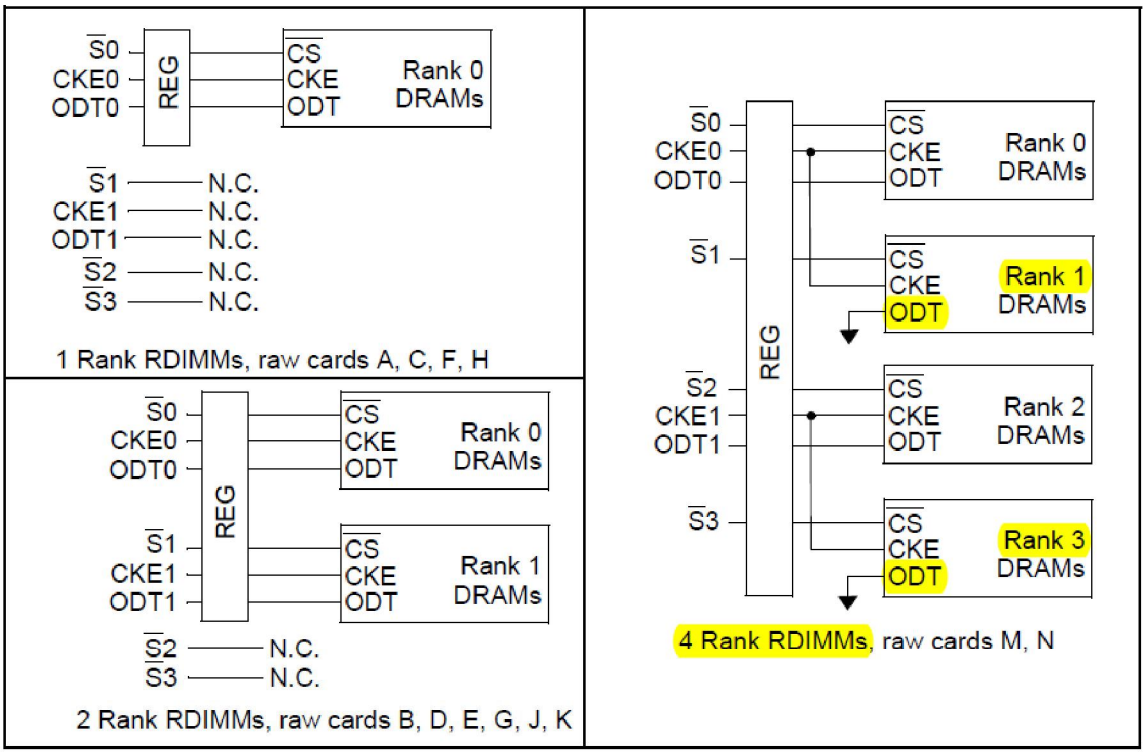
For example, a POSITA would understand that ODT would be turned off when a memory device is actively driving the data signal, or when turning off ODT for some memory devices would optimize the data signal, as shown below.

EX1003, ¶¶408-409; EX1071, 9:5-12; EX1082 (Matsui2), Fig.5 (first below); EX1066, p.106 (second below).



TERMINATION CONTROL UPON READ OPERATION OF DRAM1/3

FIG.5



Simulation and testing indicate that best signal integrity on the data, mask, and strobe bus is obtained when ODT is programmed for 75 Ω for ranks 0 and 2 of DDR2 SDRAMs via the mode register set command EMRS(1) and both ODT0 and ODT1 RDIMM signals are asserted during cycles requiring termination from the slot containing the 4 rank RDIMM, providing an effective 37.5 Ω termination impedance during these cycles. Since ODT for ranks 1 and 3 are disabled via the ODT pins on these ranks, programming via EMRS(1) is a don't-care for these ranks.

9. Claim 8

Ground 1 teaches "*[t]he memory module of claim 1, wherein the buffer comprises combinatorial logic* [e.g., to properly route the data through the buffer, EX1071, 11:56-61, 16:29-32, 17:22-18:9, 18:48-54, including when performing "rank multiplication" (discussed above, pp.10-12), *id.*, 13:49-59, 14:63-65, 15:34-40, 20:35-40, as discussed for [1.c] and [1.f.1]-[1.f.2] (pp.48-54, 76-80)]*, registers* [e.g., to latch data signals, as discussed for claim 3 (pp.81-83)]*, and logic pipelines* [e.g., to handle the sequence of commands and corresponding latencies associated

with data transfers, EX1064, pp.23-25, 49]*, and is configured to register an additional clock cycle for transferring the first data burst or the second data burst through the buffer* [as discussed for claims 3-4 (pp.81-83)]." EX1003, ¶¶411-419. A POSITA would understand that to properly route the data through the buffer (e.g., based on address signals when performing "rank multiplication," discussed above, pp.10-12), combinatorial logic and logic pipelines would be required, because the JEDEC standards specify that a read or write operation includes at least two steps: a Bank Activate command (with bank and row addresses), EX1064, pp.23, 49, and then a Read or Write command (with bank and column addresses) followed by the actual transfer of data with pre-defined latencies, id. pp.24-25, 49. EX1003, ¶¶415, 418.

10. Claim 9

Ground 1 teaches "*[t]he memory module of claim 1, wherein the first memory command* [e.g., write or read, from [1.a.2]-[1.a.3] (pp.37-46)] *includes at least one first chip select signal* [per the JEDEC standard for write and read commands, EX1064, pp.6 (first below), 49 (second below)] *and the second memory command* [e.g., subsequent write or read, from [1.a.2]-[1.a.3] (pp.37-46)] *includes at least one second chip select signal* [e.g., for the same reason, and because each rank uses different chip-select signals (e.g., S0 and S1 for a two-rank module), EX1062, p.12 (third below); EX1069, pp.2-3]." EX1003, ¶¶420-426.

1.2 Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, and $\overline{DM}$ signal for x4x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, $\overline{UDM}$, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.

Table 10 — Command truth table.

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1,2
Refresh (REF)	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1,7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.

NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

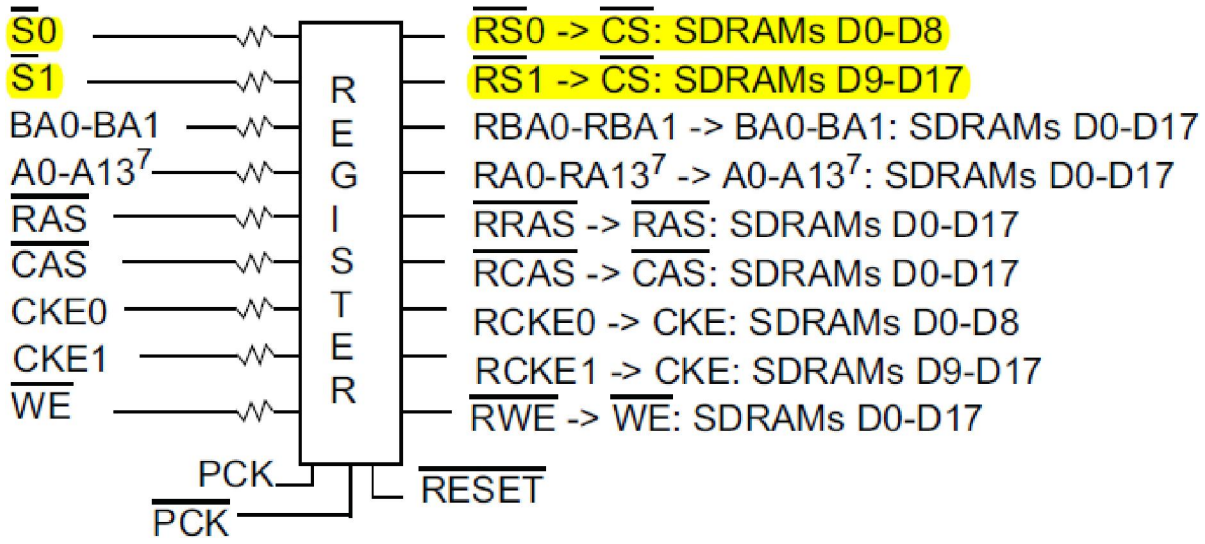
NOTE 3 Burst reads or writes at BL=4 cannot be terminated or interrupted. See sections "Reads interrupted by a Read" and "Writes interrupted by a Write" in section 2.2.4 for details.

NOTE 4 The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined in section 2.2.7.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See section 2.2.2.4.

NOTE 6 "X" means "H or L (but a defined logic level)".

NOTE 7 Self refresh exit is asynchronous.



11. Claim 10

Ground 1 teaches "*[t]he memory module of claim 9, wherein the memory module produces at least third and fourth chip select signals* [e.g., based on the address signals when performing "rank multiplication" (discussed above, pp.10-12), *see* EX1071, 14:63-65, 15:37-40] *in response to the first memory command* [e.g., write or read, from [1.a.2]-[1.a.3] (pp.37-46)]*, the third chip select signal being provided to the at least one first memory integrated circuit* [e.g., in the green rank below] *and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command* [e.g., Perego's buffer (red) sends to the targeted (green) rank a write or read command, which according to the JESD79-2 standard would include an active chip-select signal (e.g., Low or "L"), EX1064, pp.6, 49 (second below), and the buffer routes the data to/from that rank as discussed for [1.d.2]-[1.d.3] (pp.63-72)],

the fourth chip-select signal being provided to the at least one second memory integrated circuit [e.g., in the blue rank below] *and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command* [e.g., Perego's buffer (red) sends to the non-targeted (blue) rank a non-active chip-select signal (e.g., High or "H"), which according to the JESD79-2 standard would prevent that rank from reading or writing any data, EX1064, pp.6, 49 (second below), and the use of separate data paths for each rank as shown below would prevent any data being routed to/from the non-targeted rank as discussed for [1.d.2]-[1.d.3] (pp.63-72)]." EX1003, ¶¶427-442; EX1069, pp.2-4, 9 (explaining the "chip-select" signal is only sent to the targeted "rank" of memory devices); EX1062, p.13 (showing that each "*rank*," called "physical bank," *see* pp.27-30, receives a separate chip-select signal (e.g., RS0 and RS1)); EX1068 (Stone), pp.89-90 (explaining importance of avoiding bus conflicts).

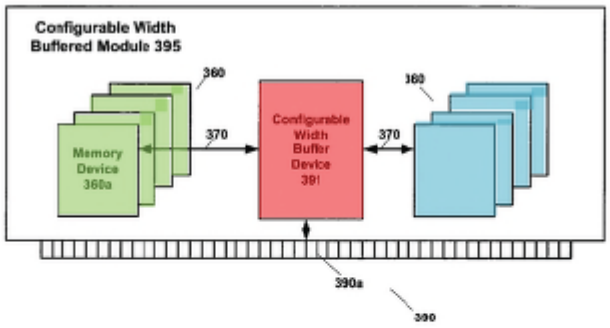


Fig. 3C

Table 10 — Command truth table.

Function	CKE		CS	RAS	CAS	WE	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1,2
Refresh (REF)	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1,7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					

12. Claim 11

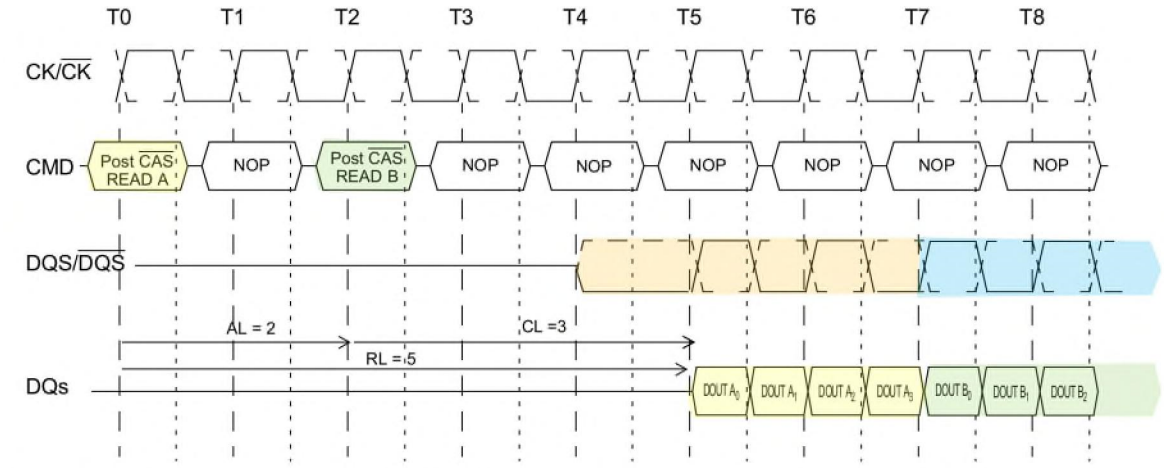
Ground 1 teaches, for the same reasons provided directly above for claim 10 (pp.99-101), "*[t]he memory module of claim 10, wherein the memory module produces at least fifth and sixth chip select signals* [e.g., based on the address signals when performing "rank multiplication"] *in response to the second memory command* [e.g., subsequent write or read, from [1.a.2]-[1.a.3] (pp.37-46)]*, the fifth chip select signal being provided to the at least one first memory integrated circuit* [e.g., in the green rank above] *and having a non-active value* [e.g., "H" per the JEDEC standard above] *to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first [sic: second]*[4] *memory command* [as explained above for the non-targeted rank]*, the sixth chip select signal being provided to the at least one second memory integrated circuit* [e.g., in the blue rank above] *and having an active value* [e.g., "L" per the JEDEC standard above] *to cause the at least one second memory integrated circuit to receive or output data signals in response to the second memory command* [as explained above for the targeted rank]." EX1003, ¶¶443-450.

[4] The claim language, as written, referring to the earlier "*first*" command, is not operational because it contradicts [1.a.3] (pp.42-46) and [1.d.2] (pp.63-72). EX1003, ¶445.

13. Claim 12

a) [12.a] First Memory Command

Ground 1 teaches "*[t]he memory module of claim 1, wherein the first memory command* [from [1.a.2]-[1.a.3] (pp.37-46), directed to the first rank, from [1.d.2]-[1.d.3] (pp.63-72)] *is a first read command* [e.g., READ A, yellow, below] *and the second memory command* [from [1.a.2]-[1.a.3] (pp.37-46), directed to the second rank, from [1.d.2]-[1.d.3] (pp.63-72)] *is a second read command* [e.g., READ B, green, below]*, wherein the first read command and the second read command are back to back adjacent read commands* [e.g., a "Seamless Burst" under the JESD79-2 standard, below, from the virtual rank that was created by "rank multiplication" from the first and second ranks (discussed above, pp.10-12; *see also* EX1071, 14:63-65, 15:37-40)]." EX1003, ¶¶452-457; EX1064, pp.24 ("seamless burst"), 28 (below). In the example below, the back-to-back read commands are "adjacent" because the data burst corresponding to the second read command is output immediately after the first one without the preamble in the strobe signals. The JEDEC standards allow such back-to-back adjacent read commands on a module "regardless of same or different banks as long as the banks are activated." EX1064, p.28.



The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 27 — Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

b) [12.b] First Burst of Data Strobe Signals

Ground 1 teaches, for the same reasons provided directly above for [12.a] (pp.103-104), "*wherein the memory module outputs the first data burst* [e.g., DOUT A0-A3, yellow, above] *together with a first burst of data strobe signals* [e.g., DQS T4-T7, orange, above] *in response to the first read command* [e.g., READ A, yellow, above]*, wherein memory module outputs the second data burst* [e.g., DOUT B0, B1, B2,..., green, above)] *together with a second burst of data strobe signals* [e.g., DQS T7-..., blue, above] *in response to the second read command* [e.g., READ B, green, above]*, wherein the second data burst follows the first data burst on the memory bus* [e.g., a "Seamless Burst" under the JESD79-2 standard, above]." EX1003, ¶¶458-463. Under the JEDEC standards, a POSITA would have understood that writing or reading data to/from DDR memory devices requires a "complement data strobe signal" (DQS/DQS) together with the data

signals on the DQ data lines, as shown above and also below in yellow. EX1064, p.27 (below); EX1071, 14:4-10; EX1069, p.2 n.2; EX1003, ¶460.

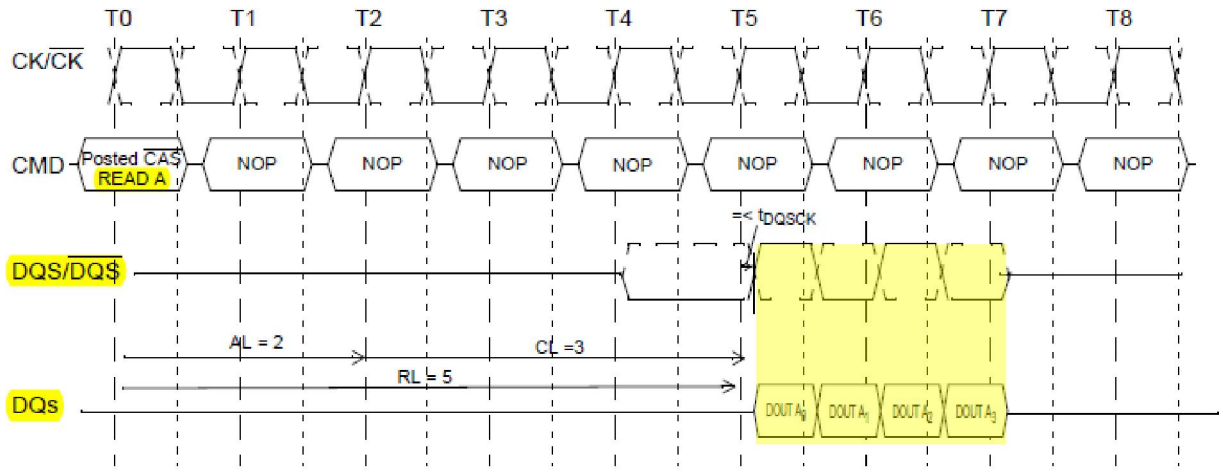


Figure 24 — Burst Read Operation: RL = 5 (AL = 2, CL = 3, BL = 4)

c) [12.c] Buffer Configured to Prevent Collisions

Ground 1 teaches "*wherein the buffer is configured to prevent the first burst of data strobe signals and the second burst of data strobe signals from colliding with each other*." EX1003, ¶¶464-472. For example, as discussed for [1.d.2]-[1.d.3] (pp.63-72), Ground 1 teaches using different data paths (or "channels") for the different ranks, meaning the "*first*" and "*second*" "*data strobe signals*" would be received with different interfaces of the buffer device (e.g., 520a vs. 520b), and would be isolated from each other, thus preventing collisions. EX1003, ¶¶466, 468-469; EX1071, 4:38-42, 6:12-15. Perego also discloses that its buffer "may employ a configurable datapath router within interface 591," EX1071, 15:34-37,

which would also prevent collisions, because the data and the corresponding strobe signals would be received only from the target rank at a time. EX1003, ¶467.

14. Claim 13

a) [13.a] Pre-Amble and Post-Amble Intervals

Ground 1 teaches "*[t]he memory module of claim 12, wherein each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval* [e.g., JESD79-2's $t_{RPRE,}$ below] and a post-amble interval [e.g., JESD79-2's $t_{RPST,}$ below]." EX1064, pp.26 (first below), 65 (second below); EX1003, ¶¶474-477.

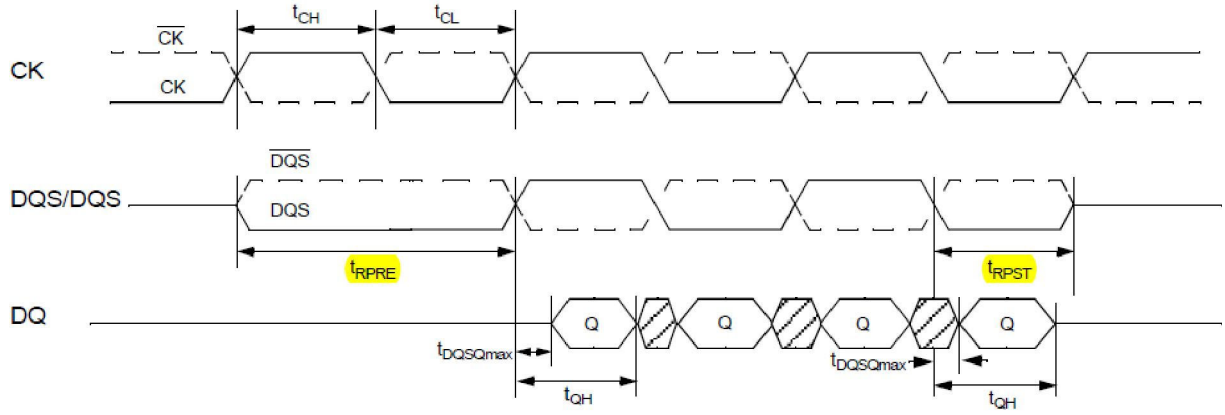


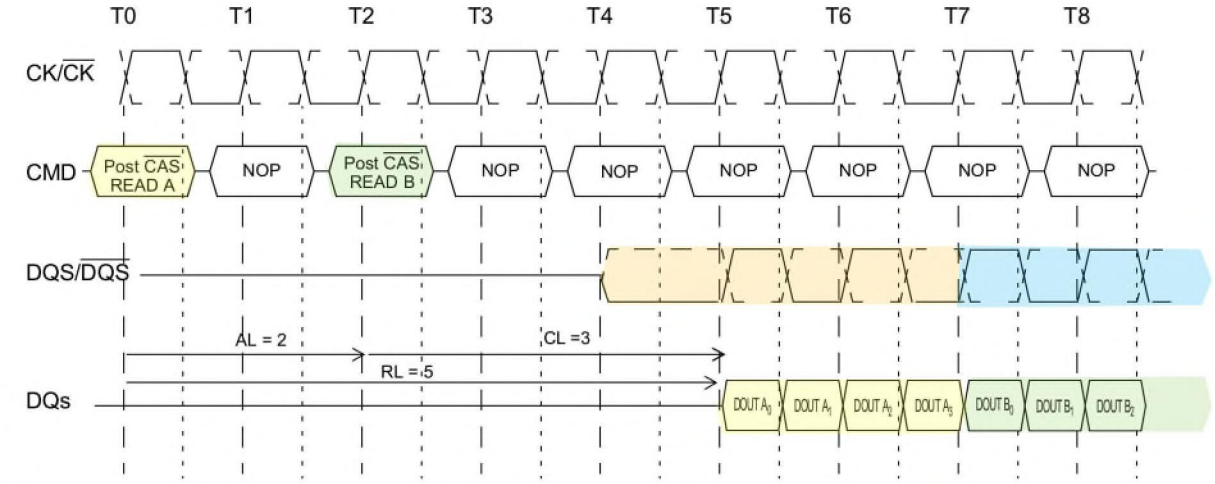
Figure 23 — Data Output (Read) Timing

Read preamble	tRPRE
Read postamble	tRPST

b) [13.b] Combined Burst of Data Strobe Signals

Ground 1 teaches, for the same reasons provided above for claim 12 (pp.103-106), "*wherein the buffer is configured to combine the first burst of data*

strobe signals [e.g., orange DQS, at T4-T7, below] *and the second burst of data strobe signals* [e.g., blue DQS, at T7-, below] *into a combined burst of data strobe signals that does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals* [e.g., at T7 below, resulting in a "Seamless Burst" from the virtual rank that was created by "rank multiplication" from the first and second ranks (discussed above, pp.10-12; *see also* EX1071, 14:63-65, 15:37-40)]." EX1064, p.28 (below); EX1003, ¶¶478-482.



The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 27 — Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

15. Claim 14

Ground 1 teaches, as explained above for [1.d.2]-[1.d.3], [1.e.], [1.f.1]-[1.f.2] (pp.63-80), "*[t]he memory module of claim 1, wherein the buffer includes circuit components* [e.g., in multiplexers 530a and 530b, and interfaces 520a, 520b and 510 or 590 (and respective transceivers in those interfaces), shown below]

configurable to provide a first data path [e.g., to interface 520a for the channel 370 to the first rank, green, below] *or a second data path* [e.g., to interface 520b for the channel 370 to the second rank, blue, below] *depending on whether the first rank or the second rank is selected to communicate data with the memory controller*." EX1003, ¶¶483-488.

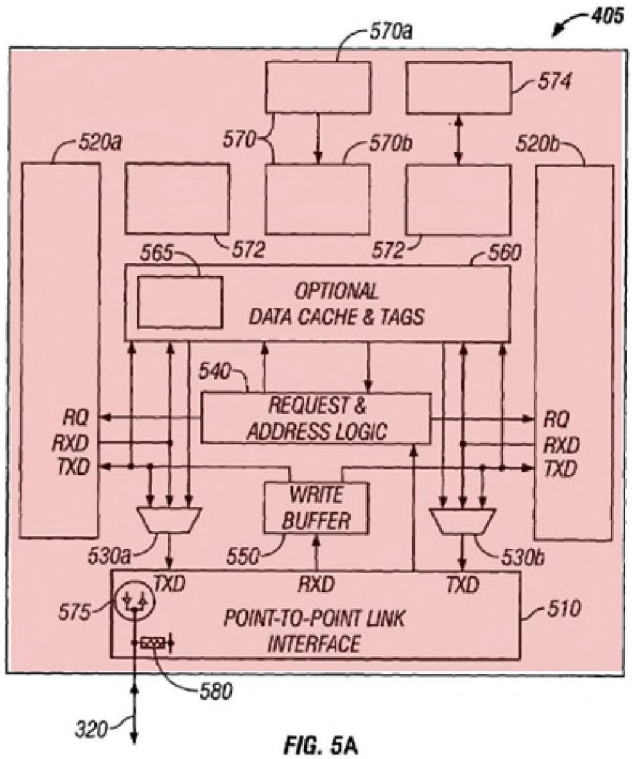


FIG. 5A

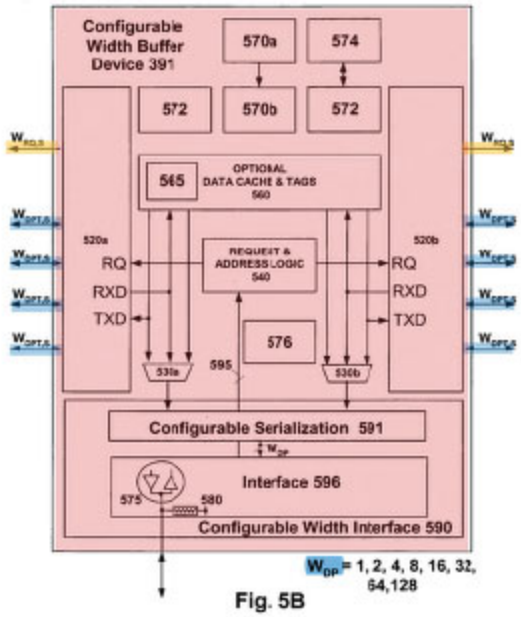

Configurable Width Buffer Device 391
570a
574
572
570b
572
565
OPTIONAL DATA CACHE & TAGS 560
520a
520b
REQUEST & ADDRESS LOGIC 540
RQ
RXD
TXD
RQ
RXD
TXD
576
595
Configurable Serialization 591
Interface 596
575
580
Configurable Width Interface 590
W_{OP} = 1, 2, 4, 8, 16, 32, 64,128

Fig. 5B

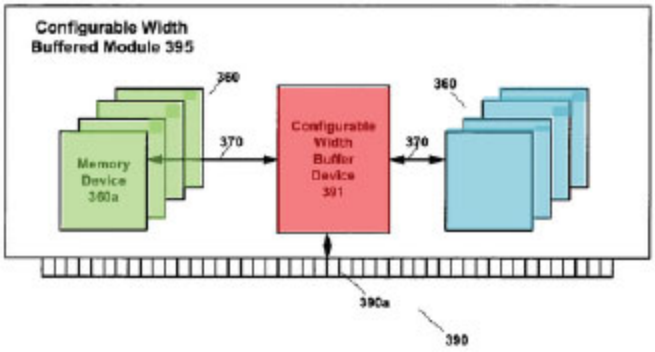

Configurable Width Buffered Module 395
360
370
Memory Device 360a
Configurable Width Buffer Device 391
370
360
390a
390

Fig. 3C

16. Claim 15

Ground 1 teaches, as explained above for [1.d.2]-[1.d.3], [1.e.], [1.f.1]-[1.f.2] (pp.63-80), "*[t]he memory module of claim 14, the*[5] *at least one of the circuit components* [from claim 14 (pp.107-109)] *is configured to provide the first data path* [from claim 14 (pp.107-109)] *in response to the first control signals* [from [1.f.1] (pp.76-80)]*, and is configured to provide the second data path* [from claim 14 (pp.107-109)] *in response to the second control signals* [from [1.f.2] (pp.76-80)]." EX1003, ¶¶489-494.

17. Claims 16-29

The limitations of claims 16-29 are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Ground 1 for at least the same reasons discussed above:

This limitation...	...is substantially similar to this limitation...	...and thus obvious for at least the same reasons above and as discussed in EX1003:
[16]	[1.f.1], [6]	¶¶495-498 (¶¶312-324, 369-381)
[17]	[8]	¶¶499-502 (¶¶411-419)
[18]	[1.f.1], [6]	¶¶503-508 (¶¶312-324, 369-381)

[5] This lacks antecedent basis, so this analysis assumes the claim refers to one or more "*circuit components*" from Claim 14. EX1003, ¶491.

This limitation...	...is substantially similar to this limitation...	...and thus obvious for at least the same reasons above and as discussed in EX1003:
[19][6]	[6]	¶¶509-514 (¶¶369-381)
[20]	[8]	¶¶515-518 (¶¶411-419)
[21.a.1]	[1.a.1]-[1.a.2]	¶¶520-522 (¶¶212-228)
[21.a.2]	[1.a.2]	¶¶523-525 (¶¶217-228)
[21.a.3]	[1.d.1]	¶¶526-528 (¶¶261-282)
[21.a.4]	[1.b]	¶¶529-531 (¶¶243-248)
[21.a.5]	[1.d.1]	¶¶532-535 (¶¶261-282)
[21.a.6][7]	—	¶¶536-538
[21.b]	[1.c], [1.a.2]-[1.a.3]	¶¶539-541 (¶¶249-260, 217-239)
[21.c]	[1.c], [1.d.2], [10]	¶¶542-544 (¶¶249-260, 283-303, 427-442)
[21.d]	[1.c], [1.a.2]-[1.a.3]	¶¶545-547 (¶¶249-260, 217-239)
[21.e]	[1.c], [1.d.2], [11]	¶¶548-550 (¶¶249-260, 283-303, 443-450)
[21.f]	[1.f.1]	¶¶551-553 (¶¶312-324)

[6] A POSITA would have understood that both of the "*first*" and "*second*" data bursts would be communicated in accordance with the latency value. EX1003, ¶¶512-514.

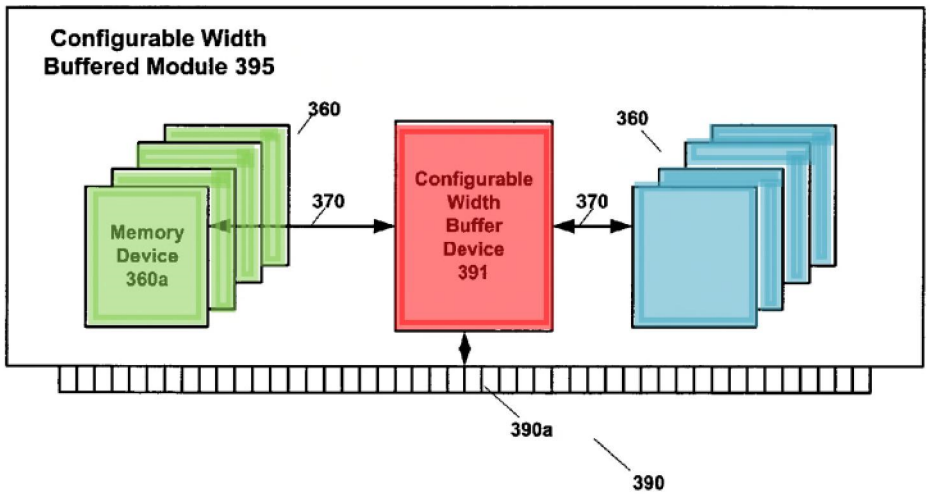
[7] This limitation is merely "the method comprising...."

This limitation...	...is substantially similar to this limitation...	...and thus obvious for at least the same reasons above and as discussed in EX1003:
[21.g]	[1.f.2]	¶¶554-556 (¶¶312-324)
[22]	[2]	¶¶557-561 (¶¶325-331)
[23.a]	[9]	¶¶563-565 (¶¶420-426)
[23.b]	[10]	¶¶566-568 (¶¶427-442)
[24]	[3]	¶¶569-572 (¶¶332-353)
[25]	[4]	¶¶573-576 (¶¶354-363)
[26]	[14]	¶¶577-580 (¶¶483-488)
[27]	[5]	¶¶581-584 (¶¶364-368)
[28.a]	[12.a]	¶¶586-588 (¶¶452-457)
[28.b]	[12.b]	¶¶589-591 (¶¶458-463)
[28.c]	[13.b]	¶¶592-594 (¶¶478-482)
[29.a]	[13.a]	¶¶596-598 (¶¶474-477)
[29.b]	[13.b]	¶¶599-601 (¶¶478-482)

B. Ground 2

1. Ground 2 combination: Ground 1 + Ellsberry (EX1073)

Ground 2 combines Ground 1 (Perego + JESD79-2) with the teachings of Ellsberry (EX1073). EX1003, ¶¶193-200. As shown below, Perego and Ellsberry disclose memory modules with a similar structure:

EX1071, Fig.3C (Perego)	 Fig. 3C

EX1073, Fig.10 (Ellsberry)

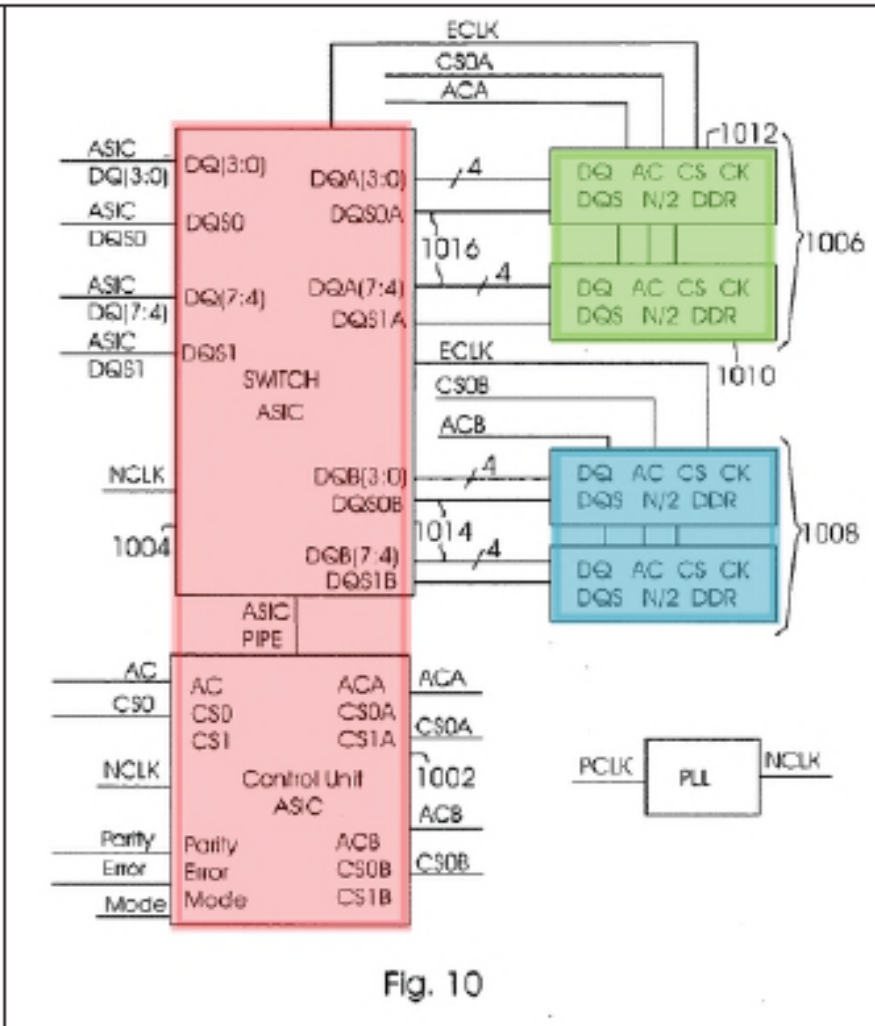


Fig. 10

Ellsberry (introduced above, pp.20-22) is analogous art because it is directed to efficiently organizing and using memory systems, including expanding memory module capacity. EX1073, Abstract, [0026]; EX1003, ¶193. Ellsberry also uses DDR and DDR2 SDRAM memory devices with memory modules in a DIMM format, like Perego and the 215 Patent, and expressly incorporates by reference the corresponding JEDEC standards, including JESD79-2 (EX1064). EX1073, [0023], [0046], [0053], Claim 10; EX1003, ¶¶194, 196. Ellsberry also teaches "rank

multiplication" (discussed above, pp.10-12), like Perego (as discussed for [1.f.1]-[1.f.2] (pp.76-80)) and the 215 Patent (pp.12-14). EX1003, ¶196; EX1073, [0026] ("two separate SDRAM DDR devices...emulate a single, two-times capacity, SDRAM DDR device" "without the need for additional chip select lines on the main memory bus"), Figs.7A-7F.

A POSITA would have been motivated to combine Ground 1 with Ellsberry because they would have recognized the relevance of the JEDEC standards, including JESD79-2, to both Perego and Ellsberry. EX1003, ¶195. A POSITA also would have been motivated to make the combination given Ellsberry's detailed description of how to implement "rank multiplication" using JEDEC-compliant memory devices, thus providing significant cost savings (discussed above, pp.10-12) that could be applied to Perego's module. EX1003, ¶196.

A POSITA would have recognized that both Ellsberry and Perego buffer the data signals on the module, advantageously reducing the load on the data lines. EX1003, ¶198. Perego discloses a centralized buffer for the data signals, like the preferred embodiment of the 215 Patent, while Ellsberry discloses distributed data buffers, and a POSITA would have understood that these implementations were known alternatives for data buffering. *Id.*; EX1078, 10:1-6 (recognizing these alternatives). Therefore, a POSITA would have been motivated to look at

analogous art like Ellsberry for details about implementing memory modules with data buffering, such as Perego. EX1003, ¶198.

A POSITA would have recognized that applying Ellsberry's teachings to Ground 1 (Perego+JESD79-2) would have resulted in a predictable variation, improving similar devices in the same way and not yielding unexpected results or challenges. EX1003, ¶¶197, 199. Furthermore, a POSITA would have recognized that, because both Perego and Ellsberry disclose buffering data signals and using JEDEC-compliant memory devices, they provide alternative, predictable solutions for operating memory modules with data buffering capabilities in accordance with the JEDEC standards. EX1003, ¶199. Therefore, it would have been at least obvious to a POSITA to try the proposed combination. *Id*.

2. Claims 1-29

Ground 2 renders obvious claims 1-29 for at least the same reasons provided above for Ground 1 (pp.30-112), given that Ground 2 incorporates Ground 1.

3. Claims 1-2, 9-11, 14-15

Ground 2 further renders obvious claims 1 (pp.35-80), 2 (pp.80-81), 9 (pp.96-99), 10 (pp.99-101), 11 (pp.102-102), 14 (pp.107-109), and 15 (p.110).

Ellsberry teaches "rank multiplication," just like the 215 Patent, where two "*ranks*" of memory devices on the memory module (green and blue, below, which

Ellsberry calls "banks") emulate a single, higher-density rank. EX1073, Abstract, Figs.2, 5-6, 8B n.3, 10-13; EX1076, pp.21-22; EX1003, ¶280.

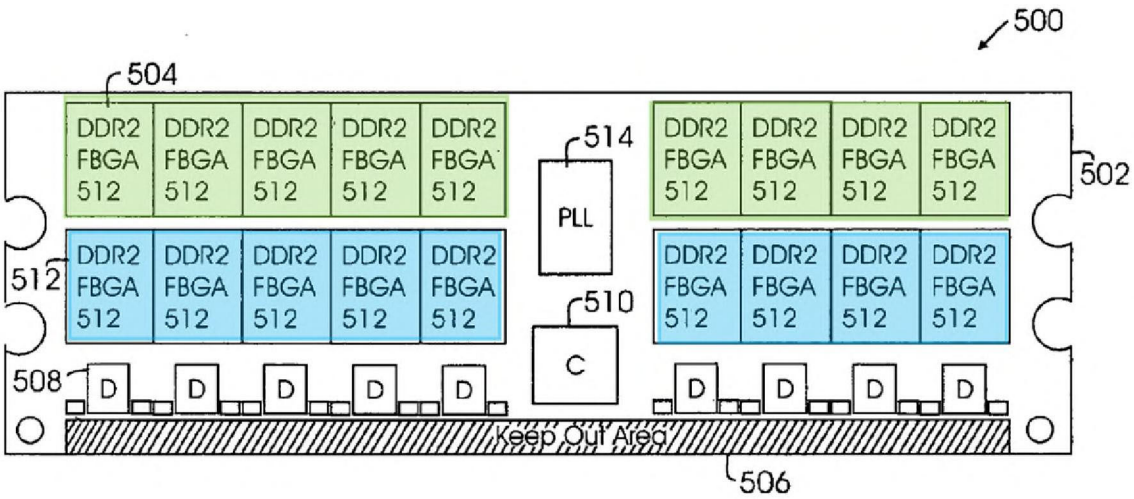
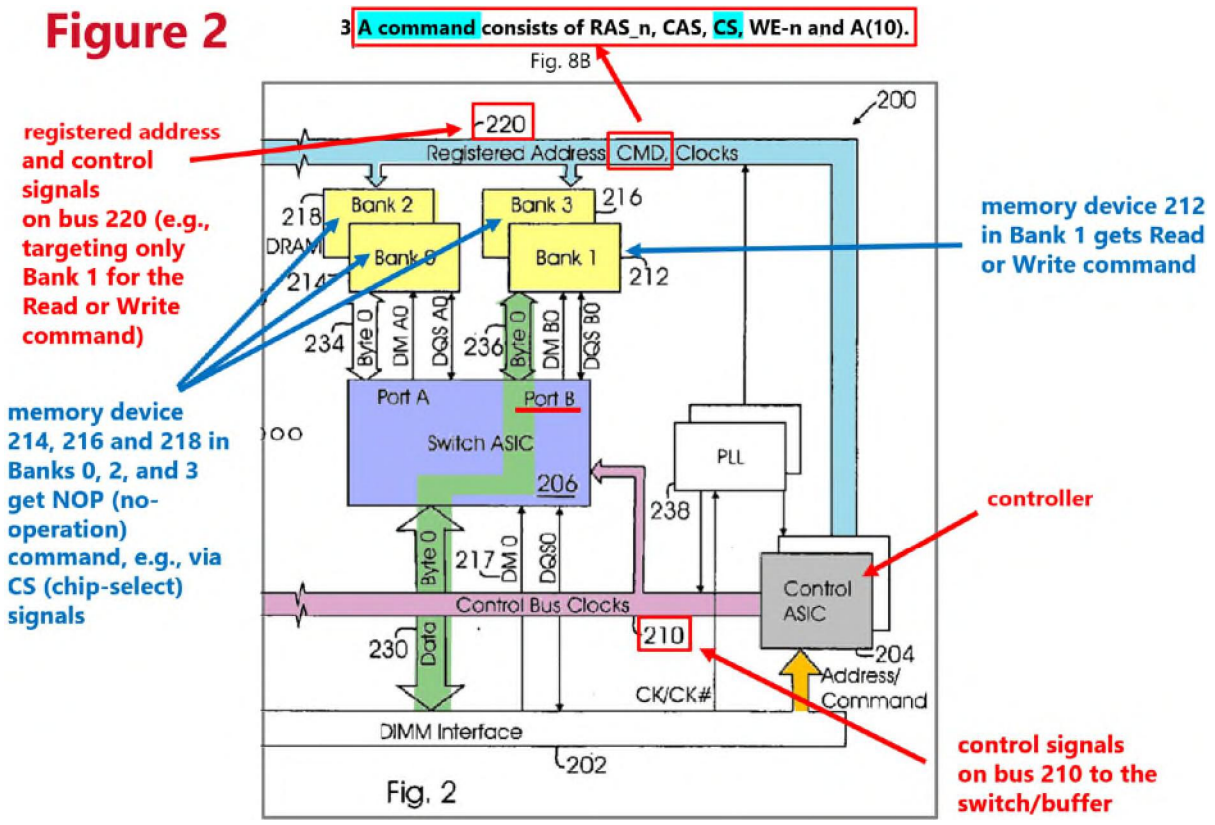


Fig. 5

For example, as shown below, "Bank 0" and "Bank 1" are two different "*memory integrated circuit[s]*" in two different "*ranks*" connected to two different "*data paths*" (234 to Port A vs. 236 to Port B) together emulating a single, higher-density memory device in a single rank. EX1073, Abstract, [0011], [0036], claim 1, Figs.2, 4, 7A-7F, 8A-8B, 10-13. EX1003, ¶¶291-292.



As shown above, Ellsberry's "Control ASIC" (204, grey) includes a "*register*" (see 220, blue, "Registered") and a part of the "*buffer*" that includes "*logic*," which provides "*control signals*" on 210 (purple) to the data "*buffer[s]*" (Switch ASICs, blue) that "*isolate*" the memory devices from the memory controller, where the "*logic*" uses the received address information and chip-select signals associated with a read or write "*memory command*" (as shown in Figures 7A-7F) to (i) cause the "*buffer*" to choose either the "*first data path*" (e.g., Port A connected to one rank) or the "*second data path*" (e.g., Port B connected to another rank), as shown in Figures 2 and 8A, and to (ii) generate additional "*chip select signals*" (as shown in Figures 10-13, e.g., CS0A and CS0B) so that only the targeted rank (e.g., Bank

1) gets an "*active*" "*chip select signal*" on 220 (as part of the read or write command) while all the other ranks get a "*non-active*" "*chip select signal*" on 220 (i.e., a NOP or "Deselect" command). EX1003, ¶¶319, 424, 429, 438-439, 446450, 485, 492; EX1073, [0010], [0012], [0031], [0036], Figs.2-4, 7A-7F, 8A-8B, 10-13, Claim 1; EX1060, p.13, n.9 ("DESELECT and NOP are functionally interchangeable"); EX1064, p.48 (similar); EX1074, pp.31-37 (Final Written Decision finding that Ellsberry discloses sending NOP commands to the non-targeted ranks), 52-56 ("Isolation").

4. Claims 3-4, 6, 8

Ground 2 further renders obvious claims 3-4 (pp.81-83), 6 (pp.84-87), and 8 (pp.95-96). EX1003, ¶¶349-353, 359-363, 369-381, 415. Ellberry teaches that the command from the memory controller setting the CAS latency for the DDR memory devices should be modified so that it is one clock cycle less than specified by the memory controller:

Command	Mode	Addr	P Bank	DDR A		DDR B	
				Command	Addr	Command	Addr
MRS	X	X	X	MRS	1	MRS	1
EMRS	X	X	X	EMRS	2	EMRS	2

NOTES: 1. if cl_mode. = subtract; cl = cl - 1 to DDRs

2. ods squelch-based on ODS setting, rtt squelch-based on REFF setting, ocd squelch-default, dqs_n enable, rdqs disable, out squelch - enable

EX1073, [0044], Figs.8A-8B; EX1003, ¶351.

For claims 3 and 8, a POSITA would have been motivated to set the CAS latency of the memory devices to be one clock cycle shorter so that the buffer in Perego and Ellsberry's memory modules has enough time (given the additional clock cycle) to perform its functions (including latching the data signals) and still comply with the timing expected by the memory controller. EX1003, ¶¶351-352, 415.

For claim 4, Ellsberry teaches the use of an "*SPD*" that "reports" to the "host system" the "configuration" of the module, including features that are "emulated." EX1073, [0034]; EX1003, ¶¶360-361. Given the need for one extra clock cycle for the buffer on the module to perform its functions, as discussed directly above, a POSITA would have been motivated to configure the SPD to report to the memory controller a CAS latency that is one clock cycle more (e.g., 4 clock cycles) than an actual operational CAS latency of the memory devices (e.g., 3 clock cycles), since otherwise the one-clock-cycle-shorter CAS latency may not be feasible for the memory devices (e.g., 2 clock cycles may not work). EX1003, ¶362; EX1064, p.12 (CAS Latency of "2" is only "Optional," not required).

For claim 6, a POSITA would have understood that any scheduled data transfer to and from the memory module should respect the latency of the entire module, including the latency of the memory devices combined with the latency

added by the buffer device, as taught above by Ellsberry, in order to perform memory operations efficiently and without errors. EX1003, ¶380.

5. Claim 5

Ground 2 further renders obvious claim 5 (p.84). *See* EX1073, [0046] ("SDRAM DDR1 and DDR2"), [0052] ("DIMMs"); EX1003, ¶367.

6. Claim 7

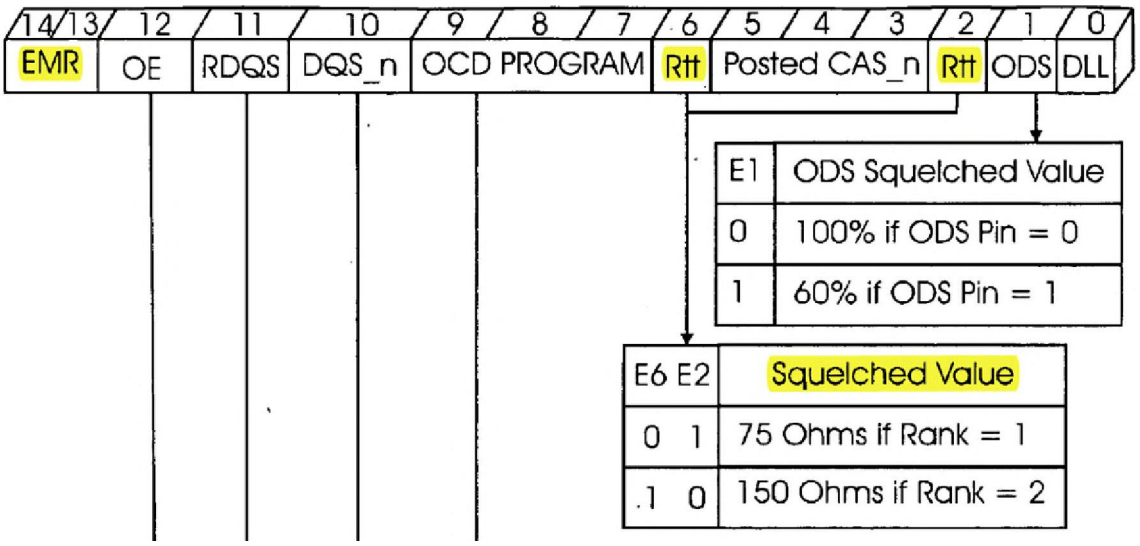
Ground 2 further renders obvious claim 7 (pp.87-95) concerning the use of "*on-die-termination (ODT)*" in the memory devices along with "*external termination*."

Ellsberry expressly discloses using the "Rtt" setting in JESD79-2 that configures the "*ODT*" circuitry in DDR memory devices. EX1073, [0044], Figs.8A-8B, 9 (partially below); EX1064, pp.14, 18-19 (further below); EX1003, ¶396.

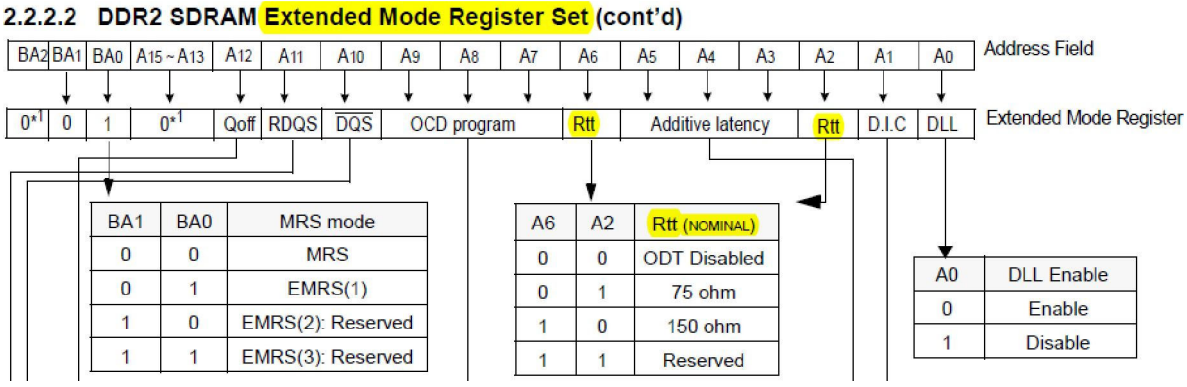
Command	Mode	Addr	P Bank	DDR A		DDR B	
				Command	Addr	Command	Addr
MRS	X	X	X	MRS	1	MRS	1
EMRS	X	X	X	EMRS	2	EMRS	2

NOTES: 1. if cl_mode. = subtract; cl = cl - 1 to DDRs

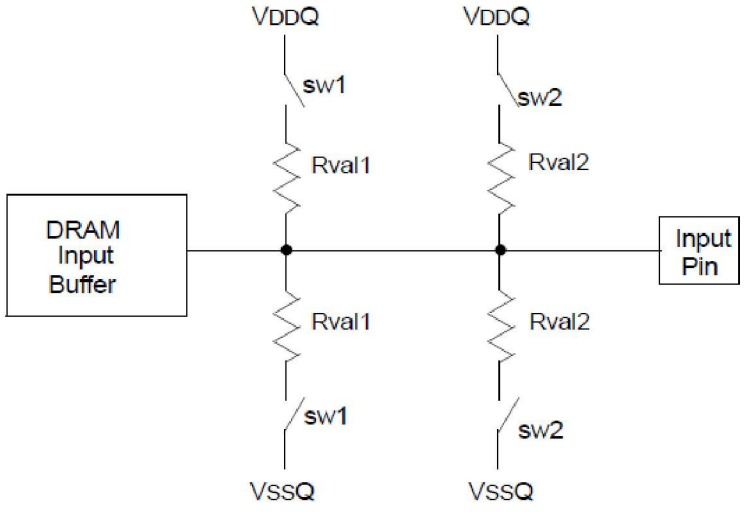
2. ods squelch-based on ODS setting, rtt squelch-based on REFF setting, ocd squelch-default, dqs_n enable, rdqs disable, out squelch - enable


14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
EMR
OE
RDQS
DQS_n
OCD PROGRAM
Rtt
Posted CAS_n
Rtt
ODS
DLL
E1 ODS Squelched Value
0 100% if ODS Pin = 0
1 60% if ODS Pin = 1
E6 E2 Squelched Value
0 1 75 Ohms if Rank = 1
1 0 150 Ohms if Rank = 2

....


2.2.2.2 DDR2 SDRAM Extended Mode Register Set (cont'd)
BA2 BA1 BA0 A15~A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
Address Field
0*1 0 1 0*1 Qoff RDQS DQS OCD program Rtt Additive latency Rtt D.I.C DLL
Extended Mode Register
BA1 BA0 MRS mode
0 0 MRS
0 1 EMRS(1)
1 0 EMRS(2): Reserved
1 1 EMRS(3): Reserved
A6 A2 Rtt (NOMINAL)
0 0 ODT Disabled
0 1 75 ohm
1 0 150 ohm
1 1 Reserved
A0 DLL Enable
0 Enable
1 Disable

2.2.2.4 ODT (On Die Termination) (cont'd)



Switch sw1 or sw2 is enabled by ODT pin.
Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.
Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

Given that Ellsberry teaches "squelch[ing]" the "Rtt" value from the memory controller used to configure *ODT*, as shown above, a POSITA would have understood that a *termination circuit* on the memory module would be coupled to the *ODT circuit* of the memory devices to properly control their ODT circuits. EX1003, ¶396.

7. Claims 12-13

Ground 2 further renders obvious claims 12-13 (pp.103-107) concerning avoiding collisions of the post-amble and pre-amble of "*data strobe signals*" during "*back to back adjacent read commands*" from two different ranks.

Ellsberry discloses that its data "*buffer(s)*" (blue Switch ASICs above, p.118, and Figure 4 below) uses two bidirectional drivers 402 and 404 to interface with respective data buses 234 (connected to the rank(s) of memory devices on Port A) and 236 (connected to the rank(s) of memory devices on Port B), each including corresponding data (DQ) and data strobe (DQS) signals. EX1073, [0045], Fig.4 (below); EX1003, ¶470.

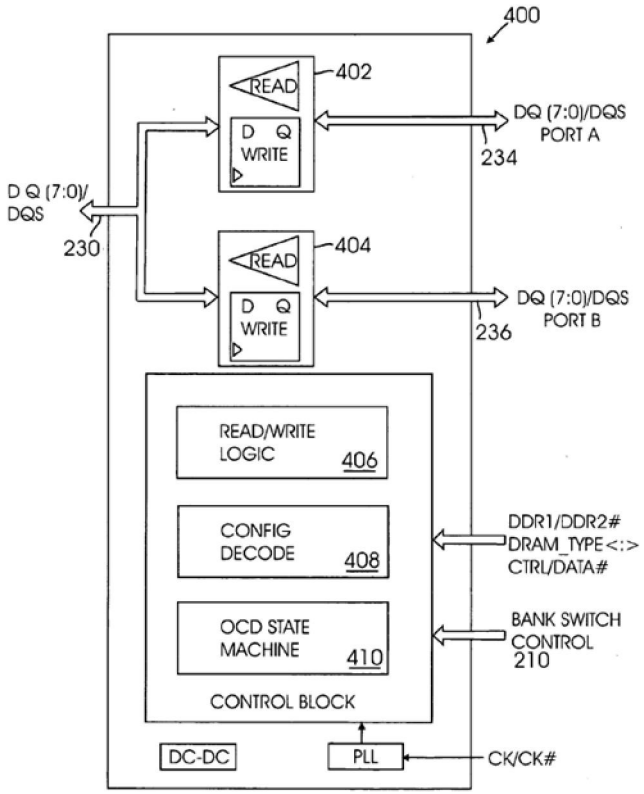
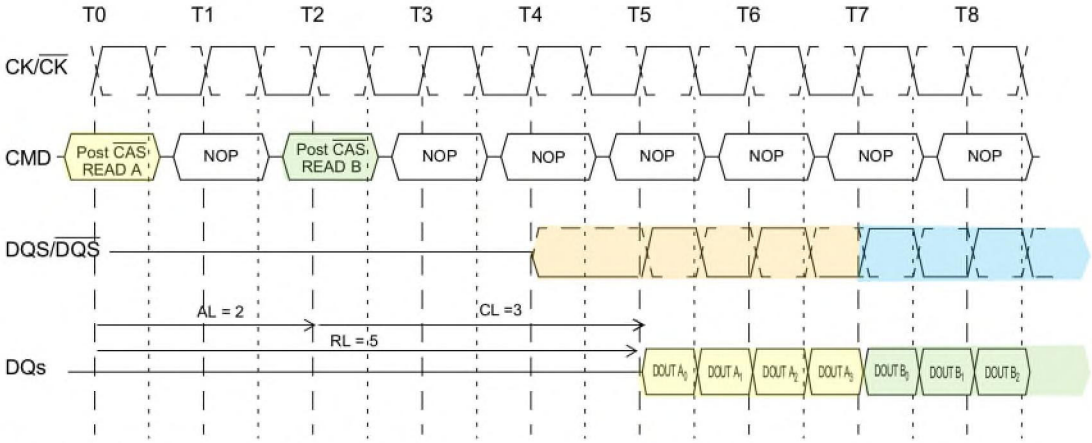


Fig. 4

A POSITA would have been motivated to follow Ellsberry's teaching that, in case of a read command, the data from the target rank is driven by either—but not both—of the drivers 402/404 on data bus 230, and their understanding that

(1) driving the bus via only one of the drivers is required to avoid disastrous conflicts that would result in data loss and potentially burning out the drivers, and (2) using separate drivers for the two ranks avoids collisions. EX1073, [0033], [0045]; EX1068, pp.89-90; EX1003, ¶¶470-471. Thus, in the case of "*back to back adjacent read commands*" from two different ranks, there would be no collisions because the driver connected to the first rank (e.g., 402) would stop driving the DQ data and DQS strobe signals onto bus 230 at T7 (in the example from JESD79-2 below), meaning the *post-amble* from the *first burst of data strobe signals* would not be driven onto bus 230, and the driver connected to the second rank (e.g., 404) would start driving the DQ and DQS signals onto bus 230 at T7, meaning the *pre-amble* of the *second burst of data strobe signals* would not be driven onto bus 230. EX1003, ¶¶471, 479.



The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 27 — Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

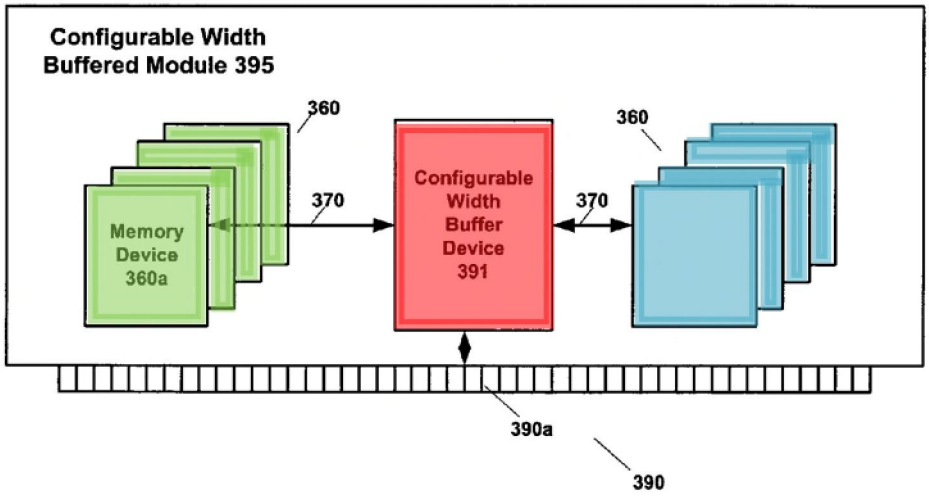
8. Claims 16-29

The limitations of claims 16-29 are substantially identical to earlier limitations, as shown in the table above (pp.110-112), and thus they are obvious in light of Ground 2 for at least the same reasons discussed above.

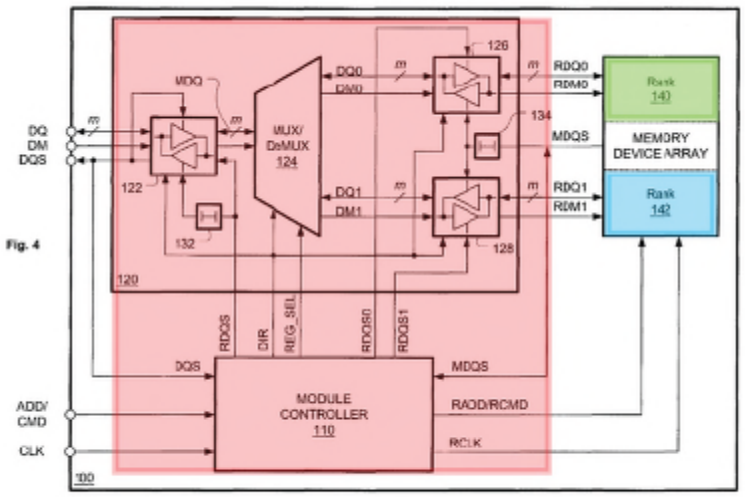
C. Ground 3

1. Ground 3 Combination: Ground 1 + Halbert (EX1078)

Ground 3 combines Ground 1 (Perego + JESD79-2) with the teachings of Halbert (EX1078). EX1003, ¶¶201-205. As shown below, Perego and Halbert disclose memory modules with a similar structure:

EX1071, Fig.3C (Perego)	 Fig. 3C

EX1078, Fig.4 (Halbert)



Halbert (introduced above, pp.22-25) is analogous art because it is directed to efficiently organizing and using memory systems, including expanding DIMM-formatted memory modules by using one or more buffers (red) to isolate the memory devices (green, blue) from the memory controller. EX1078, 1:16-19, 3:58-4:8; EX1003, ¶201. Halbert also discloses using DDR memory devices, EX1078, 9:55-59, similar to the DDR2 memory devices standardized by JESD79-2. EX1003, ¶201.

A POSITA would have been motivated to look at analogous art like Halbert for details about implementing memory modules with data buffering like Perego. EX1003, ¶202. For example, a POSITA would have been motivated to use Halbert's rank-based arrangements in Perego's module (by itself or as modified in

view of JESD79-2) since they "allow the memory devices to be isolated from the full capacitive loading effects of the system memory data bus...[and] avoid arrangements of competing memory banks that load each other, as is the case with a dual-bank DIMM." EX1078, 3:67-4:5; EX1003, ¶281.

A POSITA would have recognized that the combination would have resulted in a predictable variation, which would improve similar devices like Perego in the same way and not yield unexpected results or challenges. EX1003, ¶203. For example, a POSITA would have understood that buffering both address/command and data signals on the module allows advantageously operating multiple memory ranks, and permits "rank multiplication" (discussed above, pp.10-12) to enable significant cost savings. EX1003, ¶204.

2. Claims 1-29

Ground 3 renders obvious claims 1-29 for at least the same reasons provided above for Ground 1 (pp.30-112), given that Ground 3 incorporates Ground 1.

3. [1.d.2]-[1.d.3]

Ground 3 further renders obvious [1.d.2]-[1.d.3] (pp.63-72), concerning the "*first*" and "*second*" "*rank*," given Halbert's disclosure of different ranks on different data paths. EX1003, ¶¶277-282. Specifically, as shown below, Halbert teaches a memory module including two memory "*ranks*" 140 (green) and 142 (blue) on separate data paths, and buffering circuitry (red) (which includes a

module controller 110 and a data interface circuit 120) that interfaces with the two ranks on one side (right), and with the system memory bus on the other side (left). EX1078, 4:36-39, 4:49-59, 5:6-11, Fig.4 (below); EX1003, ¶¶278-279.

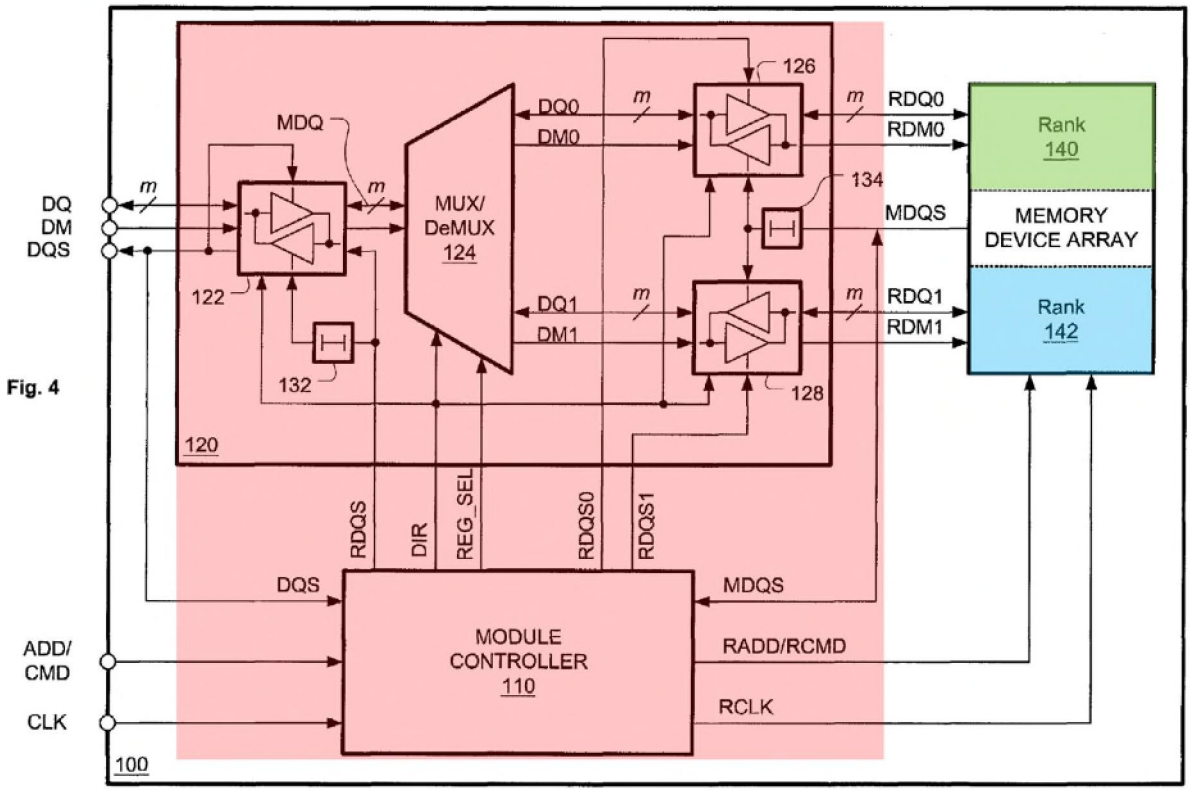


Fig. 4

4. Claim 3

Ground 3 further renders obvious claim 3 (pp.81-83) requiring the "*overall CAS latency*" of the module to be greater than that of the memory devices (e.g., by at least one clock cycle), as shown by Figures 3 and 5 of Halbert below. EX1003, ¶¶339-348; EX1078, 2:46-58 ("one-clock cycle delay"), Fig.3 (first below), 4:60-62, 5:6-11, Fig.4 (above), 5:66-6:65, Fig.5 (second below); *see also* EX1060, p.10 ("Read Latency").

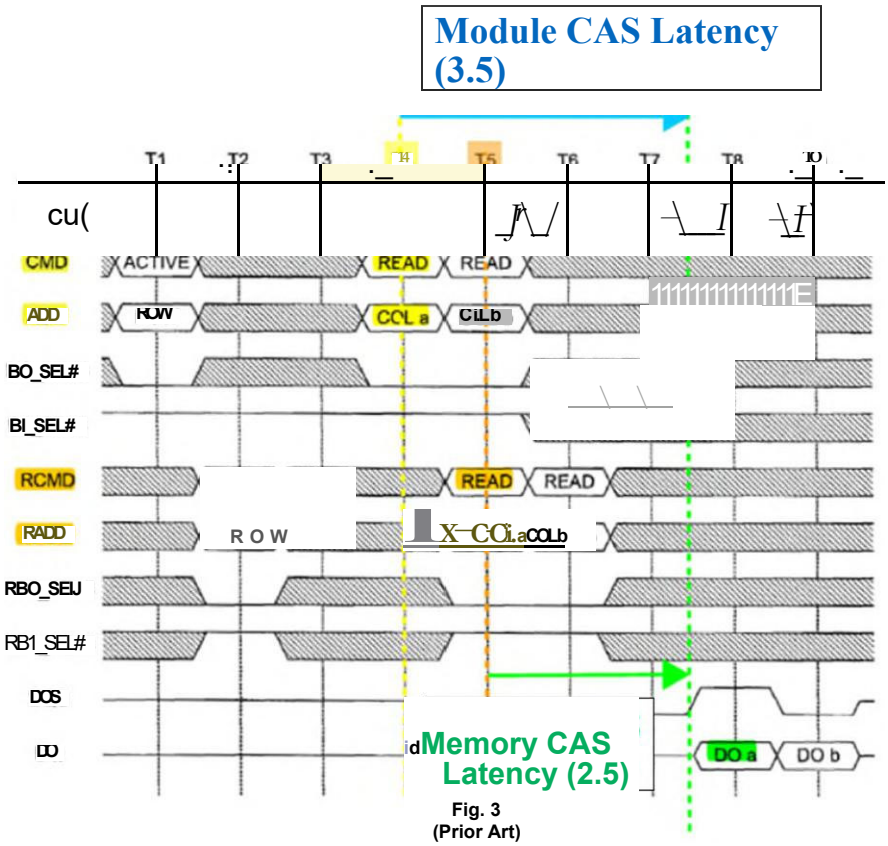
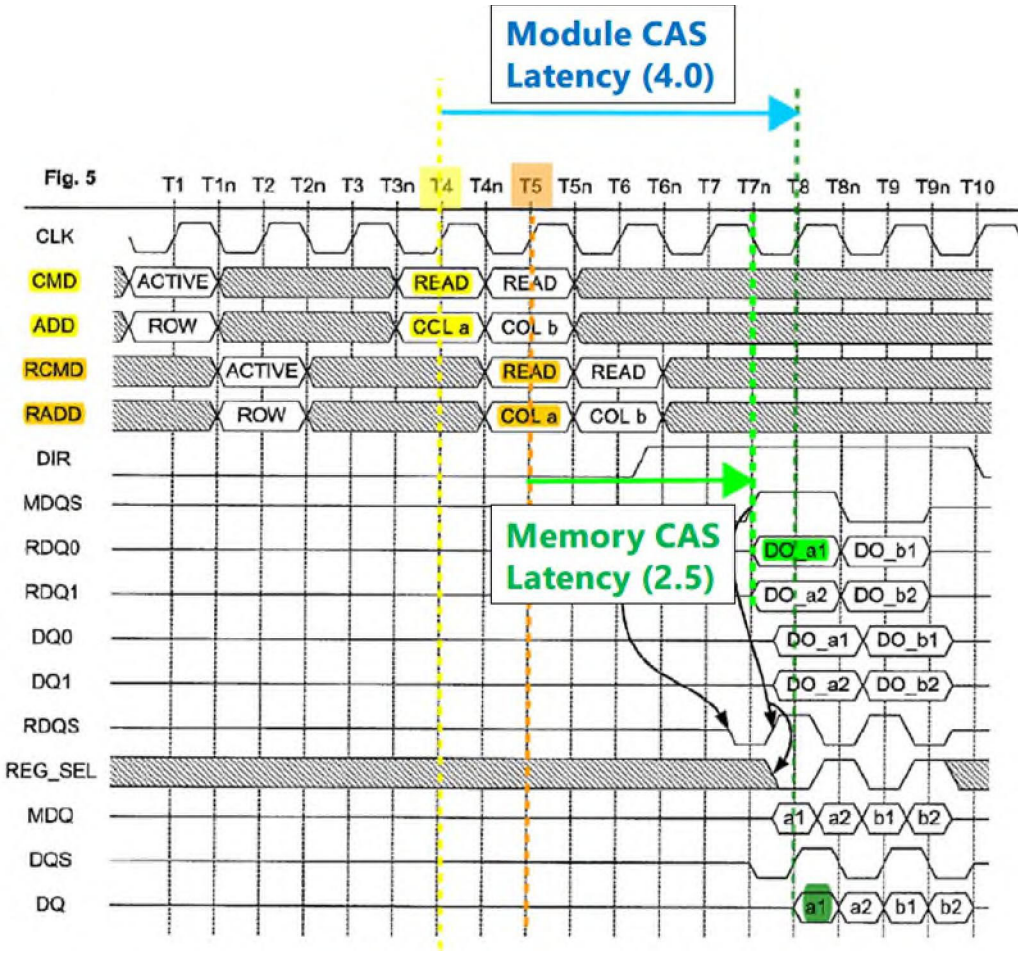


Fig. 3
(Prior Art)



5. Claim 5

Ground 3 further renders obvious claim 5 (p.84). *See* EX1078, 2:8-9 ("DIMM"), 9:56-59 ("(DDR) SDRAM"); EX1003, ¶367.

D. Ground 4

1. Ground 4 combination: Ground 1 + Matsui2 (EX1082)

Ground 4 combines Ground 1 (Perego + JESD79-2) with the teachings of Matsui2 (EX1082). EX1003, ¶¶206-209.

Matsui2 (introduced above, pp.25-27) is analogous art because it is directed to solving the problem of efficiently organizing and using memory systems,

including at high speeds. EX1082, [0001]; EX1003, ¶206. Like Perego and the 215 Patent, Matsui2 uses DDR SDRAM memory devices, EX1082, [0002], so a POSITA would have been motivated to look to Matsui2 to implement Perego's module with DDR memory devices in accordance with the JEDEC standards for DDR, like JESD79-2. EX1003, ¶206.

In particular, because Matsui2 is directed to "reading data from the memory devices at high speed by effectively preventing reflection between the data bus and each memory device," EX1082, [0011]-[0012], a POSITA would have been motivated to look at Matsui2 in order to permit Perego's module to operate at similar high speeds with DDR memory devices. EX1003, ¶207. A POSITA would have recognized that applying the Matsui2's teachings about termination circuits to the Perego+JESD79-2 combination would have resulted in a predictable variation, which would improve similar devices in the same way and not yield unexpected results or challenges. EX1003, ¶208.

2. Claims 1-29

Ground 4 renders obvious claims 1-29 for at least the same reasons provided above for Ground 1 (pp.30-112), given that Ground 4 incorporates Ground 1.

3. Claim 7

Ground 4 further renders obvious claim 7 (pp.87-95), especially [7.d] (pp.91-92) and [7.e] (pp.92-95) discussed below.

a) [7.d]

Matsui2 discloses a termination circuit 213 that interfaces with memory devices and provides external termination for data signals received on data bus 22 from the memory devices. EX1082, [0037], Fig.2 (below), Figs.5-7, 9 (showing that termination circuit 213 is turned on and off for performing read and write operations); EX1003, ¶403. A POSITA would have been motivated to use such termination circuits in Perego's interfaces 520a and 520b to reduce reflections on the signal lines in the channels connecting those interfaces to the memory devices. EX1071, 9:6-9, 11:29-31; EX1068, pp.viii ("remove...reflections"), 57 ("no reflected wave"); EX1003, ¶¶402-403.

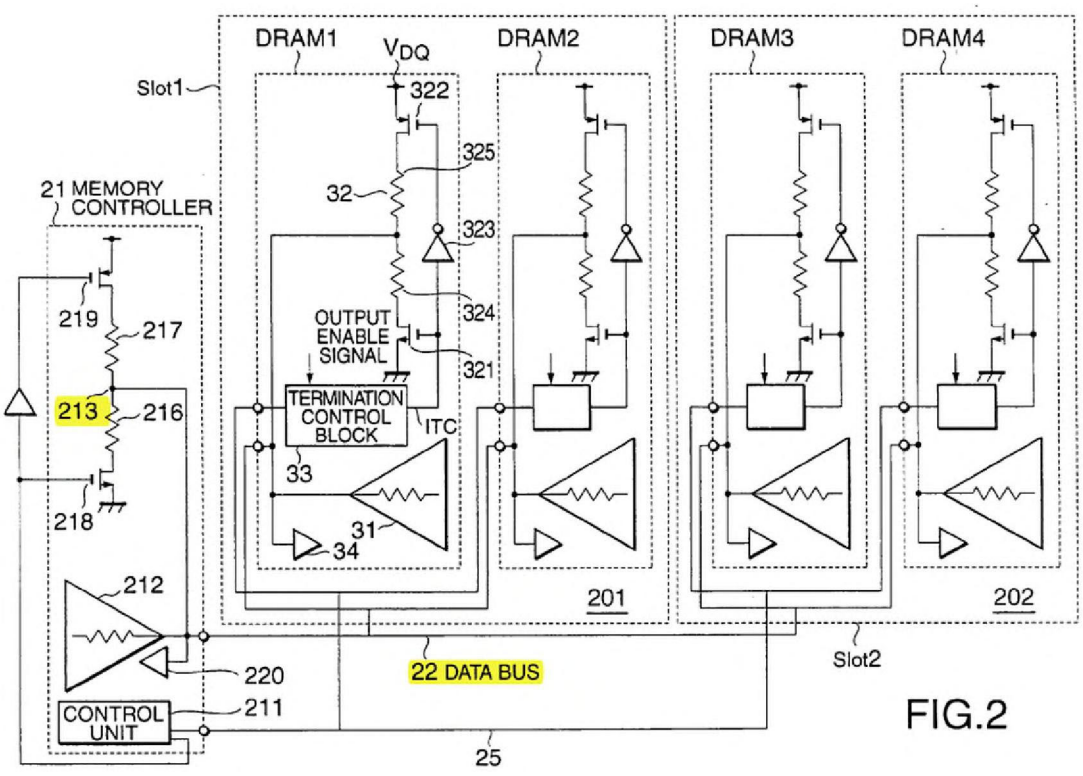
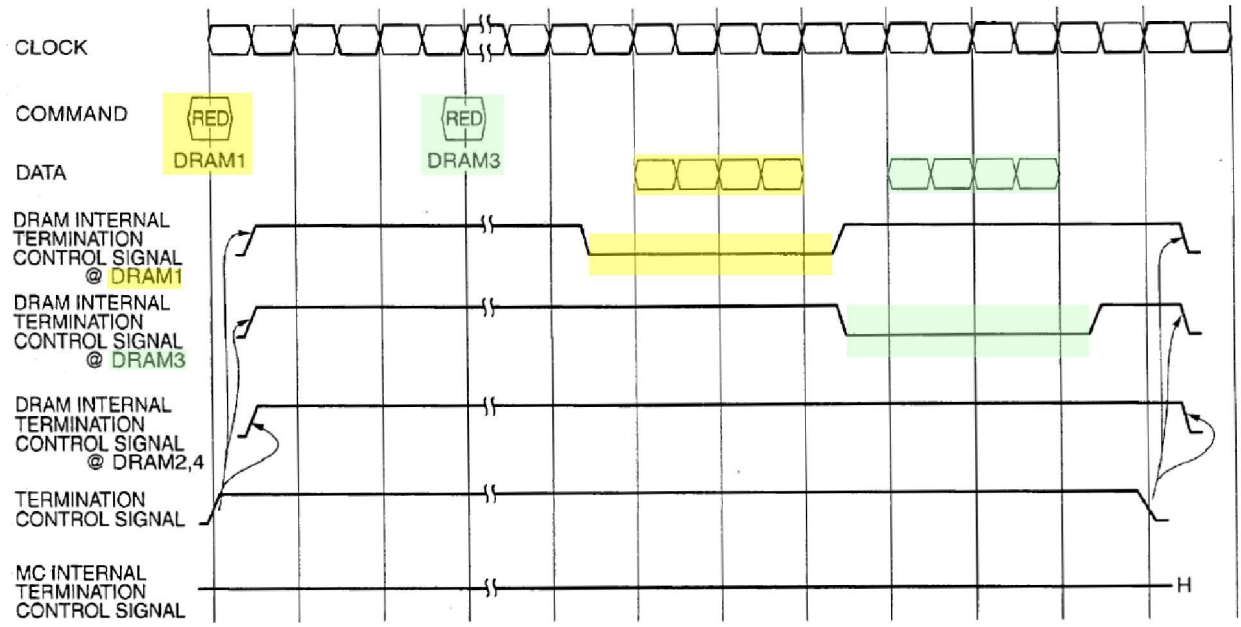


FIG.2

b) [7.e]

Matsui2 discloses turning on and off the termination of DRAM devices for read operations. EX1082, Fig.5 (below); EX1003, ¶408.



TERMINATION CONTROL UPON READ OPERATION OF DRAM1/3

FIG.5

A Skilled Artisan would have also understood that the ODT circuit of a memory device may be turned off (disabled) when that memory device is driving the data signal line (as shown above) and that it is the termination element in the interface circuit 520 that is matched to the impedance of the transmission line in order to properly terminate the signal driven by the memory device. EX1003, ¶408.

VIII. SECONDARY CONSIDERATIONS

As discussed above (pp.10-14), the 215 Patent discloses and claims "rank multiplication" as the solution to expensive, high-density memory devices. But others also immediately recognized and solved the same problem. As shown above, the 215 Patent is remarkably similar to Ellsberry (EX1073), and both were filed within one month of each other. Amidi (EX1079) and Perego (EX1071) also recognized and solved the same problem in the 18 months before the 215 Patent, as discussed above. Such "simultaneous invention" is a secondary consideration of obviousness. EX1003, ¶¶602-603; EX1023, pp.39-40. Indeed, hundreds of claims from this family of patents — all directed to "rank multiplication" — have been found invalid, providing ample evidence of widespread "simultaneous invention" of the subject matter and claims of the 215 Patent. *Id.* ¶¶89-95, 99, 171 (citing EX1012-EX1017, EX1026-EX1043, EX1046-EX1049).

IX. OTHER CONSIDERATIONS

A. §325(d)

Advanced Bionics and §325(d) do not support discretionary denial because the Examiner did not consider the Grounds discussed above. Although Ellsberry and family members of Perego and Halbert were disclosed by Netlist during prosecution, they were buried in IDSs with hundreds of other references, and there is no evidence that the Examiner substantively considered those references either alone or as part of the Grounds presented here. EX1002, pp.122-25, 157, 252,

328-31, 345, 358, 522-27. Denial under §325(d) is thus unwarranted. *E.g.*, *HTC Corp. v. Motiva Patents, LLC*, IPR2019-01666, Paper 9, at 6-10 (PTAB Apr. 3, 2020). Denial is also unwarranted because to the extent the Examiner considered Ellsberry or the family members of Perego or Halbert, the Examiner materially erred for the reasons explained above. Indeed, the Board has instituted *inter partes* reviews against family members of the 215 Patent based on grounds applying Perego and Ellsberry (*see* EX1023) and Halbert's publication (*see* EX1030, EX1056).

B. *Fintiv*

The *Fintiv* factors and the Interim *Fintiv* Guidance (EX1091) favor institution. The Board should not exercise its discretion because, as shown above, the merits of this petition are compelling. EX1091, pp.4-5. Furthermore, Samsung Electronics Co., Ltd. ("Samsung") filed a petition against the 215 Patent (IPR2023-00455 ("Samsung IPR")) within five months of Netlist's complaint asserting the 215 Patent against Samsung and Petitioners in the Eastern District of Texas. EX1085; EX1088. Petitioners have filed this copycat petition and a motion for joinder to the Samsung IPR within the one-year statutory bar. Both Netlist's litigations are still in their early stages, with the Claim Construction hearing scheduled for October 5, 2023—almost three months after an Institution Decision will have issued in the Samsung IPR. Thus, the *Fintiv* factors favor institution.

EX1091, pp.3, 8-9; EX1092, p.35 (showing a median 24.2-month time-to-trial); *Samsung Elecs. Co. v. Staton Techiya, LLC*, IPR2022-00324, Paper 13, at 12 (PTAB July 11, 2022) (applying the median). Moreover, should the Board grant institution of the Samsung IPR, the Board should not discretionarily deny institution of this petition because it will have been determined that the unpatentability challenge presented in this petition is compelling. EX1091, pp.4-5.

C. Discretionary Denial Under *General Plastic* Is Unwarranted

General Plastic does not support denying institution. This petition will not tax the Board's resources or ability to meet the statutory deadline for a final determination because Petitioners filed this petition and motion for joinder timely, advancing the same grounds and relying upon the same evidence and expert declaration as the Samsung IPR; Petitioners agree to be subject to the Samsung IPR schedule and take an understudy role only.

X. CONCLUSION

Petitioners therefore respectfully request that Trial be instituted and that claims 1-29 be canceled as unpatentable.

Dated: July 28, 2023

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CERTIFICATE OF COMPLIANCE

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. §42.24 because it contains 13,999 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. §42.24.

Dated: July 28, 2023

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CERTIFICATE OF SERVICE

I hereby certify that on this 28th day of July, 2023, a copy of this Petition, including all exhibits, has been served in its entirety by FedEx Express on the following counsel of record for Patent Owner:

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