UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SMA SOLAR TECHNOLOGY AMERICA, LLC,
Petitioner,
v.

TIGO ENERGY, INC.,
Patent Owner.

Patent 9,966,848
Filing Date: December 28, 2016
Issue Date: May 8, 2018
Title: SYSTEMS AND METHODS FOR ENHANCED EFFICIENCY AUXILIARY POWER SUPPLY MODULE

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Inter Partes Review No.: IPR2023-01175

Declaration of Douglas Holberg

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I. INTRODUCTION

1) I have been engaged by SMA Solar Technology America, LLC to opine on the patentability or otherwise of U.S. Patent No. 9,966,848 (—the '848 Patent), entitled —SYSTEMS AND METHODS FOR ENHANCED EFFICIENCY AUXILIARY POWER SUPPLY MODULE. My opinions are set forth herein. I submit this Declaration on behalf of SMA Solar Technology America, LLC in connection with its request for *inter partes* review of the '848 Patent.

A. Education and Relevant Experience

2) My education includes a B.S. in Electrical Engineering from Texas A&M University in 1977, followed by a M.S. in Electrical Engineering from the University of Texas at Austin in 1989. I earned a Ph.D. in Electrical Engineering from the University of Texas at Austin in 1992.

3) I have over 40 years of experience in the electronics field. During that time, I have worked for several different electronics companies including: Mostek, Texas Micro Engineering (acquired by Crystal Semiconductor), Crystal Semiconductor, Cirrus Logic, Cygnal Integrated Products, and Silicon Laboratories. I joined Silicon Laboratories when they acquired Cygnal, which I co-founded in 1999.

4) I am a named inventor on 43 U.S. granted patents. I have held a variety of engineering positions throughout my career, from circuit designer, design manager, Director of Engineering, Chief Technology Officer (CTO), Vice President (V.P.)

of Engineering, and V.P. of Technology. In addition to my engineering experience, I also have served as an adjunct faculty member at the University of Texas, where I taught CMOS analog and mixed-signal design for six years.

5) I am the co-author of the textbook —CMOS Analog Circuit Design, the first edition of which published 1987. As explained in the Preface of the second edition, published in 2002, the objective of the textbook is to teach the fundamentals and background that are necessary to understand how a —circuit works. It is now available in third edition and published in English and Chinese (first and second edition). This textbook is widely used throughout the world by new and experienced engineers in industry and by students in the classroom.

6) Upon graduating from Texas A&M University, I went to work for Mostek Corporation designing integrated circuits for telecommunications applications. I designed an integrated dual tone multi frequency (DTMF) generator. I received my first patent for this integrated DTMF generator. After leaving Mostek, I joined a startup company, Texas Micro Engineering, as the second employee. At Texas Micro Engineering, I designed, among other things, a dual-channel (atrium-ventricle) pacemaker sense amplifier/filter using discrete-time switched-capacitor technology.

7) While enrolled in the Masters/Ph.D. program at the University of Texas at Austin, I worked on the application of bipolar technology to dynamic random access

memory (DRAM) sense-amplifier architectures and circuit-simulation algorithms. While at The University of Texas at Austin, I also designed and laid out the mask set (The Holberg Mask Set) still in use by the fabrication class/lab.

8) Upon graduating with a Ph.D. in Electrical Engineering, I went to work for Crystal Semiconductor/Cirrus Logic, where I designed high frequency synthesizers for hard-disk read-channel applications. I managed a group designing charge-coupled device (CCD) interface circuits for digital camera applications, as well as television encoder chips and CMOS imagers.

9) Upon leaving Cirrus, I started a company called Cygnal Integrated Products that developed mixed-signal microcontrollers. At Cygnal, I was the founder, CTO), V.P. of Engineering, and an individual contributor. While at Cygnal, I designed analog-to-digital converters (ADCs), Vbe temperature sensors, input/output (I/O) cells/pads (both design and layout), as well as many additional miscellaneous circuits. My company was later purchased by Silicon Labs, where I remained employed as a manager of the microcontroller group, followed by the position of V.P. of Technology.

10) I have significant experience with the technology described in the ‘848 patent, including resistors, capacitors, diodes, inductors, transistors, transformers, oscillators, operational amplifiers, comparators, general integrated-circuit technology, analog/digital mixed-signal circuits, device analysis and modeling,

floor-planning, and layout of integrated circuits, and the tools used to design, and verify integrated circuits (CAD tools). In addition, I have experience with device modeling and characterization, which has been applied throughout my career.

11) My analyses set forth in this declaration are informed by my experience in the field of electrical engineering, including analog circuitry, ADCs, and digital circuits. Based on my above-described experience, I believe that I am considered to be an expert in the field.

12) The ‘848 Patent is entitled ―Systems and Methods for Enhanced Efficiency Auxiliary Power Supply Module. Prior to reviewing the ‘848 Patent, I was well familiar with the subject matter described and claimed therein. I am well familiar with circuits generally, such as disclosed in the ‘848 Patent.

B. Materials Considered

13) The analysis that I provide in this Declaration is based on my education and experience as an engineer, and upon my knowledge of CMOS integrated circuit design, as well as the documents I have considered, including the ‘848 Patent (Ex.1001). I have reviewed the prosecution history for the ‘848 Patent (Ex.1006).

14) I have reviewed various publications from the prior art at the time of the alleged invention of the ‘848 Patent. These publications, along with other materials I have reviewed, include those listed below:

15) Certified English Translation of German Publication DE3725476 (Mieth) (Ex. 1002).

16) U.S. Patent No. 6,246,592 (Balogh) (Ex. 1003).

17) The IEEE Standard Dictionary of Electrical and Electronics Terms, Sixth Edition 1996 (Ex. 1004).

18) U.S. Patent No. 6,798,177 (Liu) (Ex. 1005).

19) File wrapper of U.S. Patent No. 9,966,848 (Ex. 1006).

20) Allen, Philip E., and Douglas R. Holberg. "CMOS Analog Circuit Design" (2002) ("CMOS") (Ex. 1009).

21) Solibro GmbH CIGS THIN FILM SOLAR MODULE SL2 ("Solibro") (Ex. 1010).

22) MITSUBISHI ELECTRIC PHOTOVOLTAIC MODULE ("ME") (Ex. 1011).

23) US Patent application No. 2007/0001653 (Xu) (Ex. 1012).

24) U.S. Patent Publication No. 2006/0207192 (Durham) (Ex. 1013).

25) Arias et al., "A Modular PV Regulator Based on Microcontroller with Maximum Power Point Tracking," IEEE, IAS 2004. (Ex. 1014).

26) U.S. Patent No. 4,617,529 (Suzuki) (Ex. 1015).

II. LEGAL PRINCIPLES USED IN MY ANALYSIS

27) I understand that in writing this Declaration I am obliged to follow existing applicable law. I have therefore been asked to apply the following legal principles to my analysis, and I have done so.

A. Person Having Ordinary Skill in the Art

28) I understand that my assessment of the claims of the ‘848 Patent must be undertaken from the perspective of what would have been known or understood by a person having ordinary skill in the art, reading the ‘848 Patent on its relevant filing date and in light of the specification and file history of that patent. I often refer to such a person as a ―PHOSITA in this Declaration.

29) I am informed and understand that various factors can be considered in determining a person having ordinary skill in the art (PHOSITA). I am informed and understand that those factors include: (1) the educational level of the inventor(s);

30) (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) the rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the field.

31) I understand that SMA Solar Technology America, LLC proposed in the Petition that a person having ordinary skill in the art (―PHOSITA) in the field of the ‘848 Patent in 2009 would have a bachelor’s degree in electrical engineering, or a similar discipline and at least two years of experience designing circuits.

32) I agree with this level of ordinary skill for the ‘848 Patent. Based on my experience, I understand and know of the capabilities of a person of this skill level as of the time the ‘848 Provisional Patent Application was filed. (i.e., the priority application to which the ‘848 Patent claims its earliest priority) in 2009. I am

familiar with how a PHOSITA would have understood and used the terminology found in the '848 Patent at the time of its filing, and with the state of the art at that time.

33) My analysis and opinions regarding the claims of the '848 Patent have been based on the perspective of a PHOSITA as defined above as of September 2, 2009, the alleged earliest priority date to which the application which later issued as the '848 Patent claimed priority. As described above and as shown in my CV, I have extensive experience in the field of electronics in the relevant timeframe.

B. The Prior Art

34) I understand that applicable patent law provides categories of information that constitute prior art that may be used to anticipate patent claims or to render them obvious. I understand that for a reference to qualify as prior art to a particular patent claim under the relevant law, that reference must have been made, known, used, published, or patented, or must have been the subject of a patent application by another person, before the priority date of the patent, and in this matter, must satisfy one of the standards of pre-AIA 35 U.S.C. § 102.

C. Claim Construction Standard

35) In making this Declaration, I have been asked to review the terms in the '848 Patent claims to determine what a PHOSITA would have understood those terms to have meant at the time of the alleged invention. In addition, I have been informed that, in an *inter partes* review proceeding, the claim terms under

consideration are to be construed using the same claim construction standard used in a civil action under 35 U.S.C. § 282(b), which is articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. I further understand that under the *Phillips* standard, the claim terms are given their ordinary and customary meaning, as would be understood by a PHOSITA at the time of the invention, consistent with the specification and the prosecution history. My opinions regarding the meaning of claim terms of the '848 Patent are based on the construction of the claim terms using the *Phillips* standard in view of the specification and the prosecution history of the '848 Patent.

D. Anticipation

36) I understand that to be valid, a patent claim must be —novel, and that a claim is invalid if it is —anticipated by a single prior art reference. I further understand that a reference anticipates if it discloses each and every element of the claim and enables a PHOSITA to make and use the claimed invention without undue experimentation.

E. Obviousness

37) I also understand that even if a claim of a patent is not anticipated, that claim is still invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious to a PHOSITA at the time the invention was made.

38) I understand further that the condition "at the time the invention was made" in an obviousness determination is imposed to rule out impermissible hindsight. Accordingly, permissible reasoning takes into account only knowledge which was within the level of ordinary skill in the art at the time the claimed invention was made and does not include knowledge gleaned from the applicant's disclosure in the patent under analysis. I also understand that an opining expert is required to analyze prior art from the perspective of a PHOSITA and may not simply provide his or her own personal conclusions.

39) I also understand that an obviousness determination includes several factual inquiries, including: (1) determining the scope and content of the prior art;

40) (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the pertinent art; and (4) taking into consideration any secondary indicia (objective evidence) of non-obviousness.

41) I also understand that such objective evidence of non-obviousness may include: (1) a long felt but unsolved need that was satisfied by the claimed invention; (2) commercial success attributable to the claimed invention; (3) unexpected results achieved by the claimed invention; (4) praise by experts of the claimed invention with factual support; (5) taking of licenses under the patent by others for reasons related to the alleged non-obviousness of the claimed invention;

42) (6) the failure of others; (7) the teaching away of others; (8) skepticism by experts; and (9) evidence that competitors in the marketplace have copied the invention instead of using the prior art. I also understand that, in order to establish non-obviousness, there must be a demonstrated relationship, or nexus, between any such secondary indicia and the claimed invention, i.e., there must be objective evidence of non-obviousness attributable to the claimed invention.

43) I further understand that near simultaneous invention by two or more equally talented inventors working independently may or may not be an indication of obviousness when considered in light of all the circumstances.

44) I understand that a conclusion of obviousness can be based on a combination of multiple prior art references. I understand that rationales that may support a conclusion of obviousness include:

(A) Combining prior art elements according to known methods to yield predictable results;

(B) Simply substituting one known element for another to obtain predictable results;

(C) Using known techniques to improve similar devices (methods, or products) in the same way;

(D) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(E) Using an —obvious to try solution, i.e., choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(F) Applying known work in one field of endeavor to yield variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art;

(G) Applying some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference disclosures to arrive at the claimed invention.

45) I further understand that an analysis of obviousness should recognize that market demand, rather than scientific literature, often drives design trends.

46) I also understand that if a technique has been used to improve one device, and if a PHOSITA would recognize the technique would improve similar devices in the same way, then using that technique would be obvious to a PHOSITA unless actual application of that technique is beyond his or her skill.

47) I also understand that practical and common-sense considerations should guide an analysis of obviousness, because familiar items may have obvious uses beyond their primary purposes. I further understand that applying common sense does not require a —specific hint or suggestion in a particular reference. Rather, applying common sense requires a reasoned explanation that avoids conclusory generalizations and false deductions.

48) I also understand that, when addressing a problem, a PHOSITA will often be able to fit together the disclosures of multiple publications. In this regard, I understand that an analysis of obviousness may consider inferences and creative steps that a PHOSITA would normally employ.

49) I also understand that a particular combination of prior art may be proven obvious merely by showing that it was obvious for a PHOSITA to try that combination. For example, when there is a design need or a market pressure to solve a problem, and/or there exists a finite number of identified, predictable solutions with a reasonable expectation of success, a PHOSITA has good reason to pursue the known options within his or her technical grasp. I understand that if this leads to anticipated success, it is likely that the result is not of innovation but of ordinary skill and common sense.

50) I also understand that a combination of familiar elements according to known methods is presumed to be obvious when that combination does no more than yield predictable results. Work known in one field of endeavor may prompt variations of that work for use in either the same field or a different field, based on design incentives and other market forces. If a technique has been used to improve some device, and a PHOSITA can implement a predictable variation of that technique, then that variation is likely unpatentable.

51) I further understand that to be proper for use in an analysis of obviousness, a reference must teach art that is analogous to the claimed invention. I also understand that under a correct analysis, any need or problem known in the field of endeavor at the time of the invention and addressed by the claimed invention can provide a reason for combining the elements in the manner claimed.

52) I understand that a claim can be obvious in light of a single reference, without the need to combine references, if the elements of the claim that are not found explicitly or inherently in that single reference can be supplied by the common sense or technical knowledge of a PHOSITA. For example, combining two embodiments disclosed adjacent to each other in a prior art patent likely does not require a leap of inventiveness.

53) I also understand that a claimed invention may be obvious if it merely involves simple substitution of one known element for another to obtain predictable results.

54) I understand further that, in an analysis of obviousness, two items of prior art need not be like two puzzle pieces that must fit together perfectly. For example, a claimed invention may be found obvious if a PHOSITA would view rearrangement as an obvious matter of design choice.

55) I also understand that an analysis of obviousness requires a comparison between the properly construed claim language and the prior art on a limitation-by-limitation basis.

III. BACKGROUND OF THE TECHNOLOGY

56) Comparators are a widely used component that detects and indicates the relationship between its two inputs. A symbol for a comparator is shown in Fig. 1 below, but can be illustrated in other ways as well.

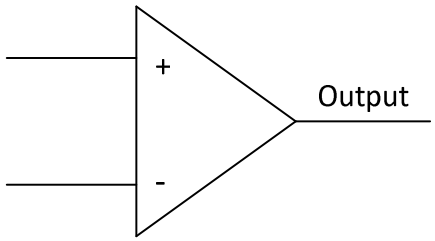


Fig. 1

57) The inputs are characterized as the positive input and the negative input. Sometimes also referred to as the non-inverting and inverting inputs, respectively. A comparator generally has, but is not limited to, a single output that indicates the relationship between the input signals at the positive and negative inputs. If the positive input is greater than the negative input, then the output of the comparator will be high. Alternatively, if the positive input is less than the negative input, then the output of the comparator is low. Theoretically for an ideal comparator, if the inputs are equal, the output is indeterminate. The ideal transfer curve for a comparator is shown in Fig. 2 below. (Ex. 1009, Fig 8.1-4).

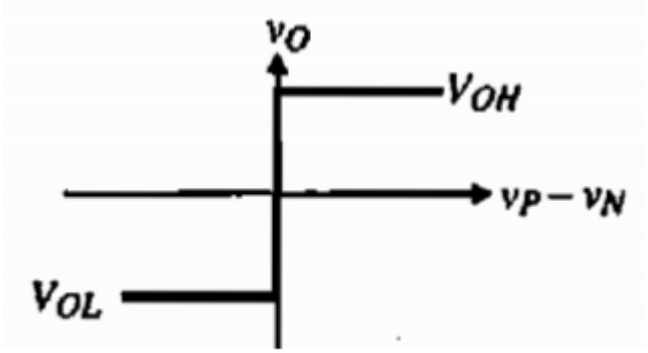


Fig. 2

58) Comparators, like all electronic devices, are subject to noise—both internal and external noise. When comparators are intrinsically noisy, or are placed in a noisy environment they can "chatter" when the input is close to the switching threshold (comparator threshold) (Ex. 1009, 462). This is illustrated in Fig. 3 below. (Ex. 1009, Fig 8.4-6a).

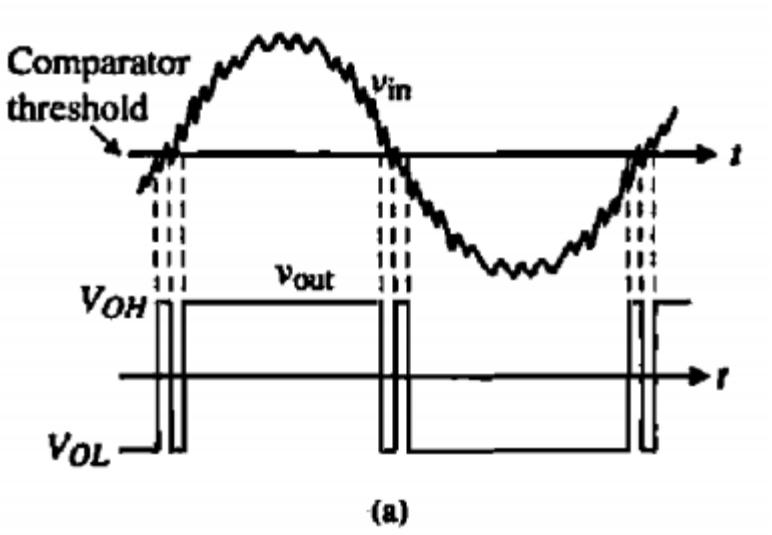


Fig. 3

59) As seen in Fig. 3, due to the noise on v_{in} (the positive input terminal of the comparator), at the comparator threshold, the noise of the signal bounces above and below the threshold, causing the signal at the output (vout) to switch quickly or "chatter" between V_{OH} and V_{OL}, in some instances, multiple times depending upon the frequency of the noise on the input signal. One of the methods to avoid this "chatter" on a comparator output is to add hysteresis to the transfer function curve of the comparator. To add hysteresis, the trip threshold of the comparator is varied based on the state of the comparator. This can be understood as follows. When the input signal to the comparator is rising, the state of the comparator does not change until the input signal reaches a positive trip point threshold (V_{TRP}^{+} as shown in Fig. 4 below). Once the state has changed due to the input signal exceeding the threshold, the trip-point threshold is reduced to a negative trip point so that the state of the comparator output does not change until the input signal falls below the negative trip point (V_{TRP}^{-}. as shown in Fig. 4 below). This is illustrated in Fig. 4 below (Ex. 1009, Fig. 8.4-5).

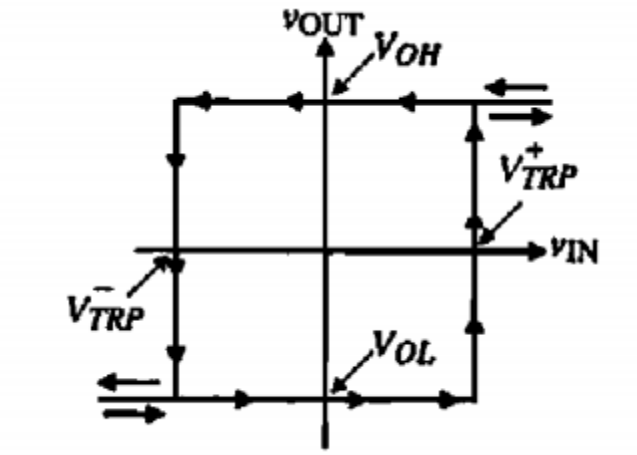


Fig. 4

60) As shown, the input signal, v_{IN}, starting from the left is low causing v_{OUT} to be low (V_{OL} or the "first state"). As v_{IN} increases to the right, a positive trip point is reached, V_{TRP}^{+}. At that point V_{OUT} goes high (V_{OH} or the "second state"). V_{IN} can continue increasing with no change in state. As v_{IN} starts decreasing, the output, v_{OUT}, remains high (second state) until it reaches a negative trip point threshold V_{TRP}^{-} (which is lower than the initial positive trip point V_{TRP}^{+}) causing the comparator output, v_{OUT}, to go low (first state).

61) Once hysteresis is introduced to the comparator, the "chatter" effect is removed as long as the noise amplitude on the signal is less than the difference of the positive and negative trip voltages (i.e., keeping the noise less than the hysteresis "window"). This is illustrated in Fig. 5 below (Ex. 1009, Fig. 8.4-6b) where the "chatter" on the output signal of the comparator no longer exists.

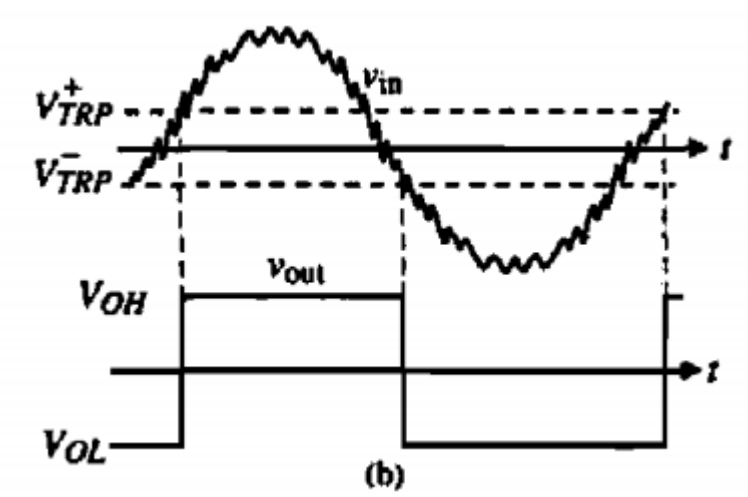


Fig. 5

62) When the signals at the positive and negative inputs cross (e.g., when the positive input becomes greater than the negative input), the state of the comparator output changes (e.g., goes from a low state to a high state in this case). This transition does not happen instantaneously—there is some intrinsic delay. This delay is generally referred to as propagation delay as illustrated in Fig. 6 below (Ex. 1009, Fig. 8.1-9). In fact, nothing in real-world circuitry happens instantaneously, i.e., without delay.

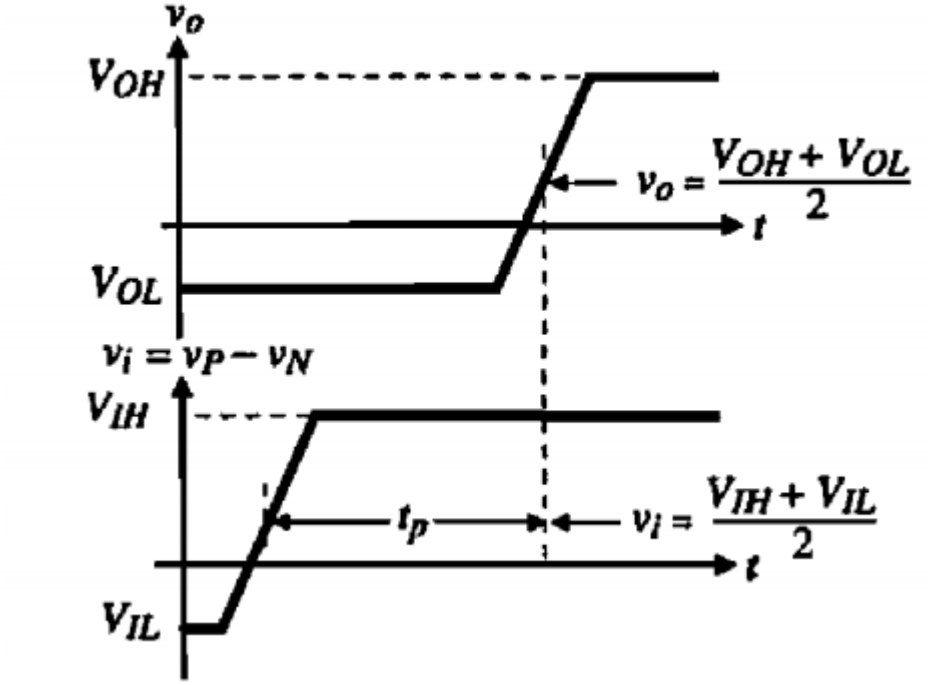


Fig. 6

63) As can be seen in the figure, if the midpoint of the transition is taken as the reference point between the low state and high state of both the input signal and the output signal, respectively, it is clear that a delay of t_p represents the time delay between the transition at the comparator input and the corresponding signal transition at the comparator output. This delay, t_p, represents a delay associated with the various internal circuitry of the comparator to effectuate the corresponding signal transition at the output in response to the transition at the comparator input.

IV. OVERVIEW OF THE '848 PATENT

A. Brief Description

64) The '848 patent is directed to a power supply in a solar power supply system. Ex.1001,1:50-51. The Fig. 7, below, shows a power supply having a first stage 401 and a second stage 402—buck converters. The first stage 401 receives an input voltage from a photovoltaic ("PV") panel and outputs a first voltage at a first output. The second stage 402 is connected to the first stage 401 and receives its input from the first stage 401. Ex.1001,1:51-56. The second stage 402 operates in two states: (1) a first, deactivated state, and (2) a second, enabled state. In the second state the second stage 402 generates a second voltage at a second output using the first voltage to supply power (a voltage) to a micro-controller. Ex.1001,8:41-48.

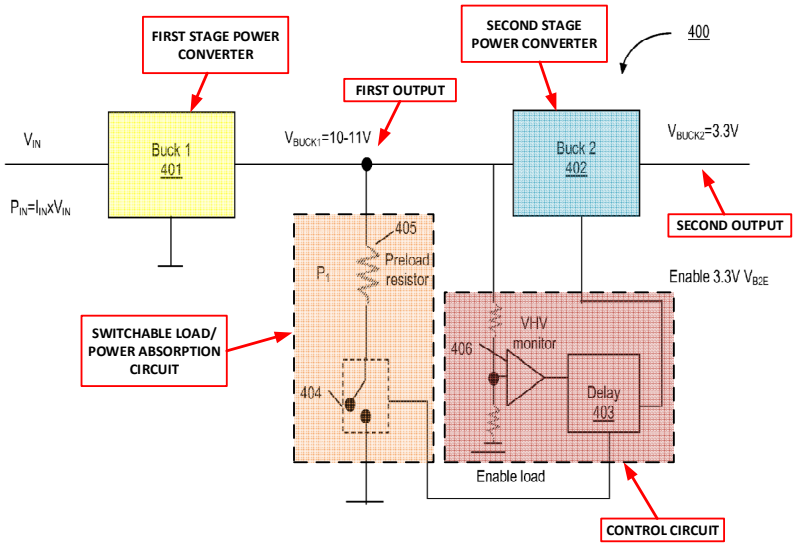


Figure 4

Fig. 7

65) The power supply includes a control circuit (406,403) to prevent false start problems when the solar panel is providing insufficient power. Ex.1001,8:19-22. The control circuit, in the first state, connects a preload resistor 405 to the first output by closing a switch 404 via a first control signal to emulate the load of the second stage 402 on the first stage output prior to activating the second stage 402 via a second control signal. Ex.1001,8:22-23,8:35-37. If the first stage output voltage exceeds a threshold, the control circuit disconnects the preload resistor 405 by opening the switch 404 via the first control signal. Ex.1001,8:41-45. The control circuit employs a delay 403 to delay the second control signal with respect to the first control signal to ensure the second stage operation remains disabled

until after the switch 404 is opened, thus providing a "break before make condition," wherein the switch 404 opens before the second stage 402 is enabled in the second state. Ex.1001,8:40-48.

66) In another embodiment shown in Fig. 8, (Figure 3 of Ex.1001), a capacitor 326 is connected to the input of the second stage 311/402. Ex.1001,9:32-34.

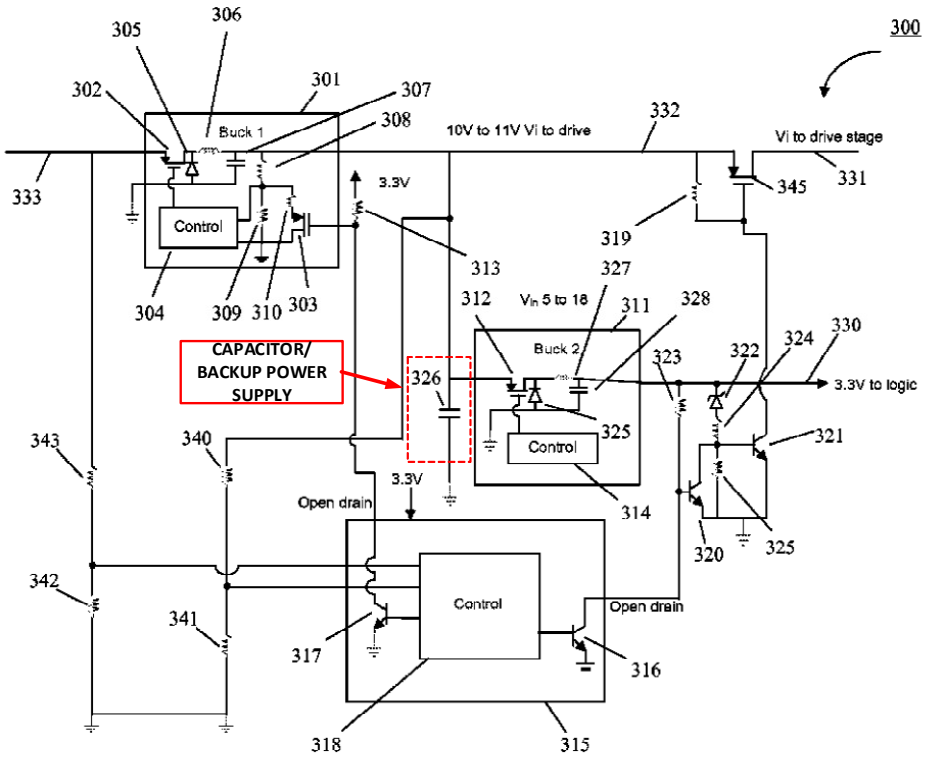


Fig. 8

67) Capacitor 326 operates as a backup power supply to keep the second stage 311/402 running longer when the first stage 401cannot provide power. Thus, in the first state, the capacitor 326 is charged and absorbs power, and when the first stage 401 is inoperative/unstable, the capacitor provides power to keep the second stage 402 running to provide the second voltage at the second output. Ex.1001,4:60-66.

B. Earliest Priority Date for the Claims

68) The ’848 patent was filed as App. No. 15/392,960 on December 28, 2016, as a continuation of App. No. 14/822,227 (issued as Patent No. 9,584,021), filed on August 10, 2015, which is a continuation of App. No. 12/787,205 (issued as Patent No. 9,143,036) filed on May 25, 2010, which claims priority to U.S. App. No. 61/275,734, filed on September 2, 2009, and U.S. App. No. 61/336,743, filed on January 26, 2010. Ex.1001,P.1;Ex.1006,P.93. At least 61/275,734, and arguably 61/336,743, do not provide support under 35 U.S.C. §112, first paragraph, for the claimed subject matter. I do not rely on prior art published in the time period between the priority dates and the non-provisional filing date of May 25, 2010, but reserve the right to challenge the priority date of the ‘848 Patent.

69) No substantive Office Actions were issued in the ’960 application. An allowance was issued on December 19, 2017. Subsequent to the allowance, an amendment under 37 C.F.R. §1.312 was filed to address an informality. Ex.1006,P.3.

70) The earliest alleged priority date for the ’848 patent claims is September 2, 2009. Each reference in the grounds for unpatentability predates this date and constitutes available prior art under 35 U.S.C. § 311(b).

V. OVERVIEW OF PRIOR ART

A. DE3725476 (Mieth) (Ex.1002)

71) Mieth discloses a circuit and associated method that supplies power to an electrical load such as a micro-controller from a solar generator. See Fig. 9 below. Ex.1002, 8:8-9, Fig. 1.

72) For electrical energy sources that exhibit variability in performance, such as a solar converter (due to the time of day or weather conditions), depending on the power provided by the energy source, the circuit arrangement operates in two different states. Ex.1002, 1:23-28; 5:22-27. In a first state, at lower source voltages, a preliminary load is switched "in" to the circuit, while disabling a downstream auxiliary power supply circuit. In a second state, at higher source voltages, the preliminary load is switched "out" of the circuit arrangement, and the power from the solar generator is fed to the auxiliary power supply circuit (*e.g.*, power supply apparatus 19). *Id.* 1:28-34; claim 1, 2:10-34.

73) As given below, Fig. 9 shows the solar generator 1 that provides a direct current to a first stage capacitor 2, providing a first voltage at a first output in response to a direct current input.

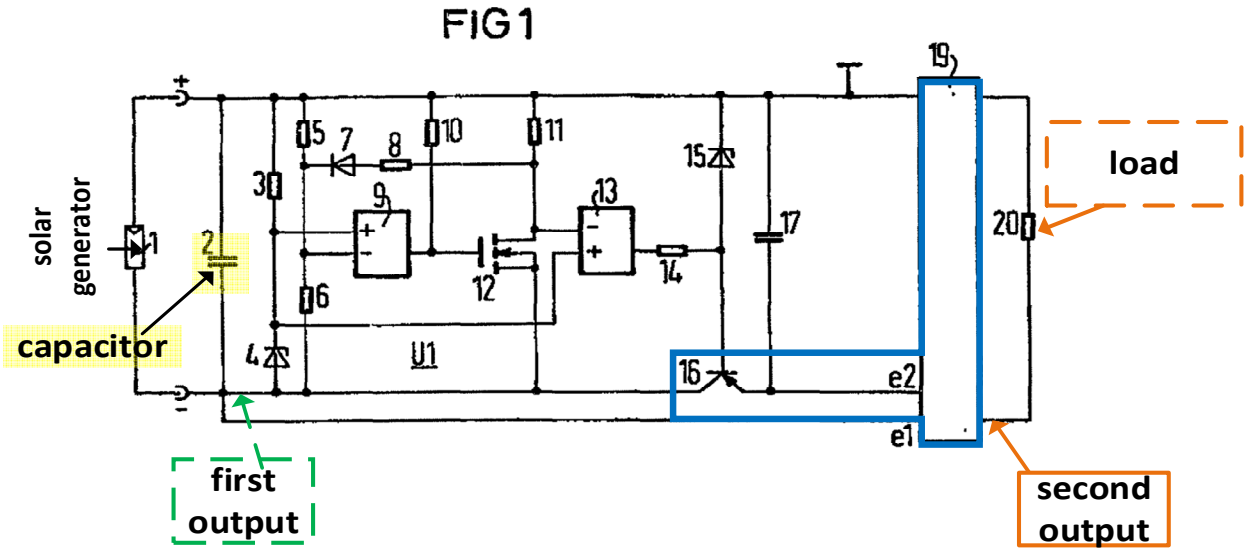


Fig. 9

74) The circuit arrangement includes two comparators, a first comparator 9, and a second comparator 13, that operate in one of two states. In the first state, with a low voltage at the first output, the first comparator 9 switches "in" the preliminary load, while the state of the second comparator 13 results in the power supply apparatus 19 being disabled. *Id.* 6:14-23; 9:15-32.

75) Fig. 10 highlights the first state at low input voltages, where first comparator 9 is "high" and preliminary switchable load 11 (i.e., resistor 11), is switched "in" due to transistor 12 being "on" (i.e., conducting).

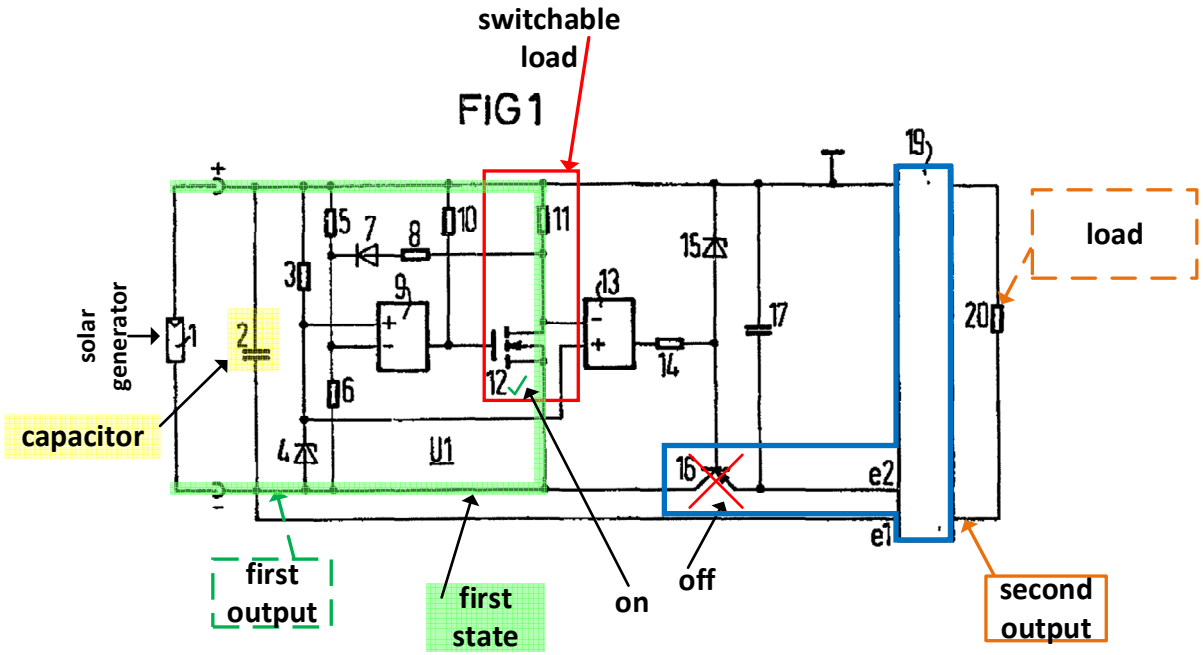


Fig. 10

76) Further, in the first state, second comparator 13 output is "high", causing the pnp bipolar transistor 16 to be "off" (i.e., non-conducting), and power supply apparatus 19 to be disabled. *Id.* 12:12-19.

77) Fig. 11 illustrates the second state when power provided by solar generator 1 is high (the magnitude of the voltage across capacitor 2 is high), thus the magnitude of the first voltage at the first output is high. With higher magnitude input voltages, the voltage at the negative input of first comparator 9 exceeds the reference voltage at the positive input terminal, causing the first comparator output to transition "low" and turning off transistor 12 (i.e., "switching out" switchable load, resistor 11).

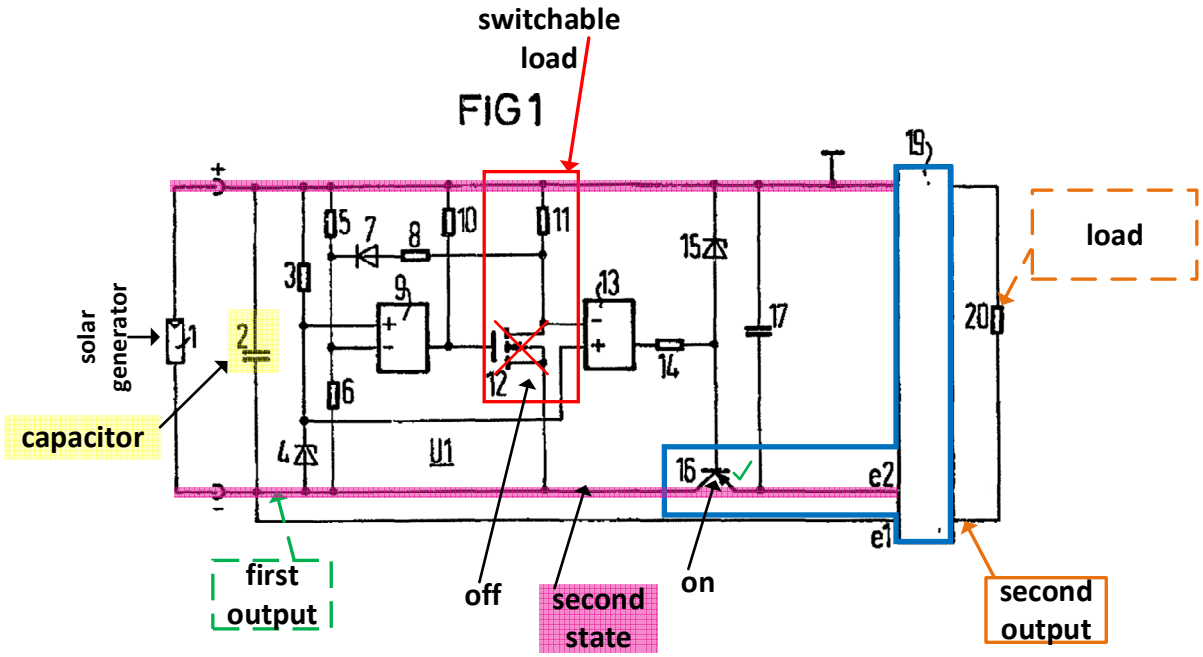


Fig. 11

78) With transistor 12 off, the negative input of second comparator 13 gets pulled high, causing second comparator 13 output to go "low," turning on transistor 16 (pnp bipolar transistor). *Id.* 12:21-30. With transistor 16 conducting, the first output is passed to the e2 input of auxiliary power converter 19, enabling it to provide the second output to load 20. *Id.* 9:15-32. Auxiliary power converter 19 is also connected to solar generator 1 via supply voltage input e1. Ex.1002 8:29-35. Mieth does not discuss the function of supply voltage input e1, a PHOSITA would understand that supply voltage input e1 may provide additional functionality to the circuit of Mieth, perhaps, for a product or particular implementation that is extraneous to the detailed description.

79) In addition, Mieth discloses a “break before make” operation between the first and second states, wherein an exit from the first state (preliminary load 11 is “switched in”) is concluded before the second state (where auxiliary power converter 19 is enabled) is initiated. This “break before make” operability is facilitated by the cascaded first and second comparators 9 and 13. When the first voltage at the first output goes low (relative to the positive terminal of the PV), first comparator 9 output changes state to turn off the transistor 12. Only after transistor 12 stops conducting does second comparator 13 output transition from “high” to “low” in order to turn on transistor 16. Thus when transistor 12 shuts off, the voltage at the negative input terminal of second comparator 13 rises and exceeds the reference voltage at the positive input terminal, causing output of the second comparator 13 to transition low. Transistor 16 is a pnp-type transistor, and is activated or turned “on” when the voltage at its base terminal that connects to the output of the second comparator 13 is low. Because comparator 9 must change state before the output of transistor 12 (the negative input of comparator 13) changes state and comparator 13 changes state only after its negative input changes state, there is an intrinsic delay built into the cascaded comparator arrangement to ensure that the first control signal that disables preliminary load 11 always occurs before the second control signal that enables power supply apparatus 19. Thus, Mieth teaches a delay between first and second control signals.

80) Mieth includes a hysteresis circuit comprising comparator 9, voltage divider resistors 5, 6, 8, 11, and diode 7. *Id.* 12:21-30. The hysteresis function is provided by the positive feedback via resistor 8 and diode 7. *Id.* Using the nomenclature shown in the Fig. 12 below, Mieth's hysteresis will be analyzed.

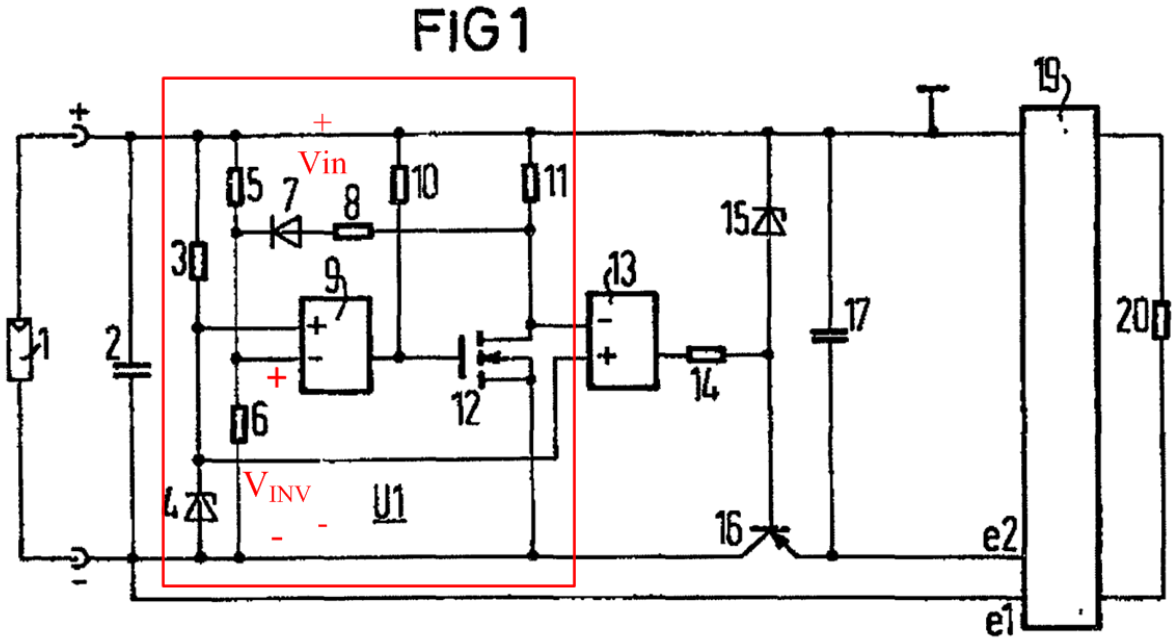


Fig. 12

81) Mieth incorporates a diode 7 in the hysteresis circuit so that the hysteresis feedback is applied in only one state (when the output of comparator 9 is low causing drain of transistor 12 to be high). Thus, in the first state where $Vin\frac{R6}{R5+R6} < V_{ZENER}$, the drain of transistor 12 is low, so diode 7 does not conduct.

When *Vin* increases so that when $Vin\frac{R6}{R5+R6} > V_{ZENER}$, the output of the comparator

goes low and the drain of transistor 12 goes high so that diode 7 is conducting and as a result changes the voltage at the inverting input of comparator 9 to:

$$\frac{Vin\left(\frac{R6}{R5}+\frac{R6}{R8+R11}\right)-V_{DIODE}\frac{R6}{R8+R11}}{1+\frac{R6}{R5}+\frac{R6}{R8+R11}}=V_{INV}$$

82) Ignoring the forward voltage of the diode (setting $V_{DIODE}=0$) this expression simplifies to:

$$Vin\frac{R6}{R_{EQ}+R6}=V_{INV}$$

where:

$$R_{EQ}=\frac{R5(R8+R11)}{R5+R8+R11}$$

83) Thus there are two thresholds. The upper threshold is given by:

$$Vin=\frac{R5+R6}{R6}V_{ZENER}$$

84) and the lower threshold given by:

$$Vin=\frac{R_{EQ}+R6}{R6}V_{ZENER}$$

85) The hysteresis curve resulting from this circuit arrangement is shown in Fig. 13 below.

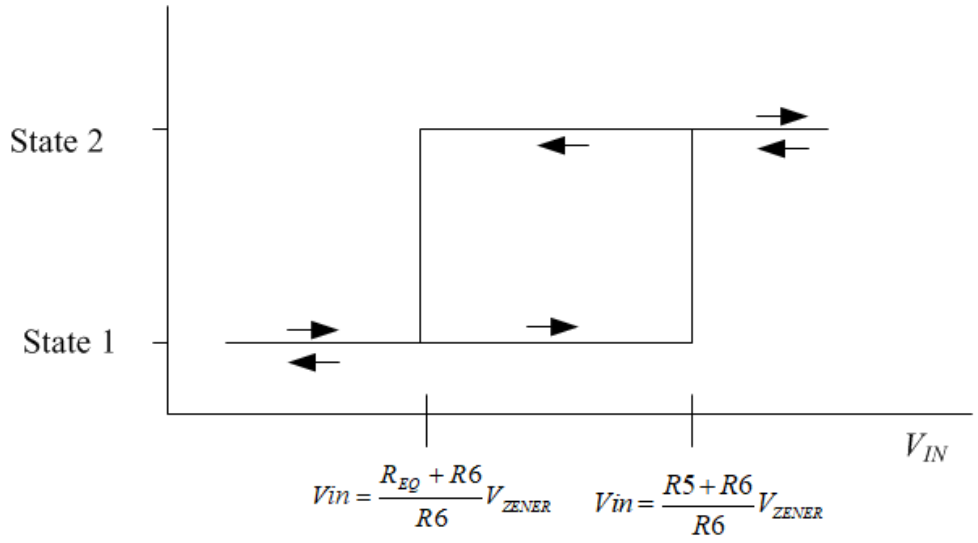


Fig. 13

B. U.S. Patent No. 6,246,592 (Balogh) (Ex.1003)

86) Balogh is a United States patent that issued on June 12, 2001. Balogh discloses that cascaded power converter arrangements that include two or more power converters are well known. Ex.1003, 1:21-22. Balogh further discloses that cascaded converters are commonly used to provide large input to output voltage conversion ratios (step-up or step-down). *Id.* 1:25-28. Solar power applications often employ individual modules with voltages as high as 75-80V under some operation conditions, and as low as 10V in other instances, while still providing enough power to operate a load such as a microcontroller. Ex. 1010; Ex. 1011. Consequently, solar power applications including cascaded power converter systems having large input to output voltage conversion ratios can be advantageous.

87) It is well known in the art that improved efficiency can be achieved by cascading buck converters when there is a large ratio of input to output voltage as described in Patent application: US 2007/0001653 (hereafter "Xu"). Ex. 1012. Xu states: "The present invention provides a two-stage power delivery system that employs cascaded buck stages. For high input-to-output voltage ratios, each cascaded buck stage has a more suitable (i.e., larger) duty cycle that results in a much lower total power loss than in a single-stage buck." Ex. 1012, ¶6. Xu teaches using cascaded buck converters where the input is in the range from 6 to 24 volts and an output voltage on the order of 1 volt. *Id.* ¶18. Thus, as will be discussed in greater detail *infra*, Xu provides a teaching that a PHOSITA would readily consider a cascaded converter arrangement in various solar applications, such as the application taught in Mieth.

88) Balogh discloses multiple cascaded buck converter arrangements in prior art Figs.1B-1D, respectively. One example of a conventional, cascaded converter arrangement provided in Fig. 1D thereof is illustrated in Fig. 14 below.

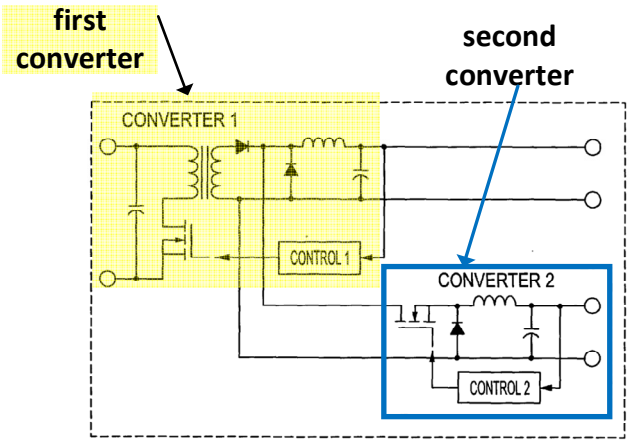


FIG. 1D
PRIOR ART

Fig. 14

89) In Fig. 14, an isolated DC-DC converter (converter 1) feeds a post regulator circuit (converter 2) to form first and second step-down (buck) converter stages, respectively. In one example, the first converter is a transformer-coupled input power converter that steps down the input voltage to an intermediate voltage. Ex.1003, 1:61-66; 3:8-13. The second converter is a buck power converter. *Id.*, 1:62-63.

C. U.S. Patent No. 6,798,177 (Liu) (Ex.1005)

90) Liu is a United States patent that published on September 28, 2004. Liu discloses a multi-stage converter circuit that employs a storage capacitor in between, and in parallel with, two cascaded converter stages. As shown in Fig. 15 below (which corresponds to Fig. 5 of Liu), the multi-stage converter circuit includes an input stage 50, a storage or reservoir capacitor 58, and output stage 60. Output stage 60 connects to a power amplifier ("PA") 68 as a load. Ex.1005, Fig.5, 4:25-28.

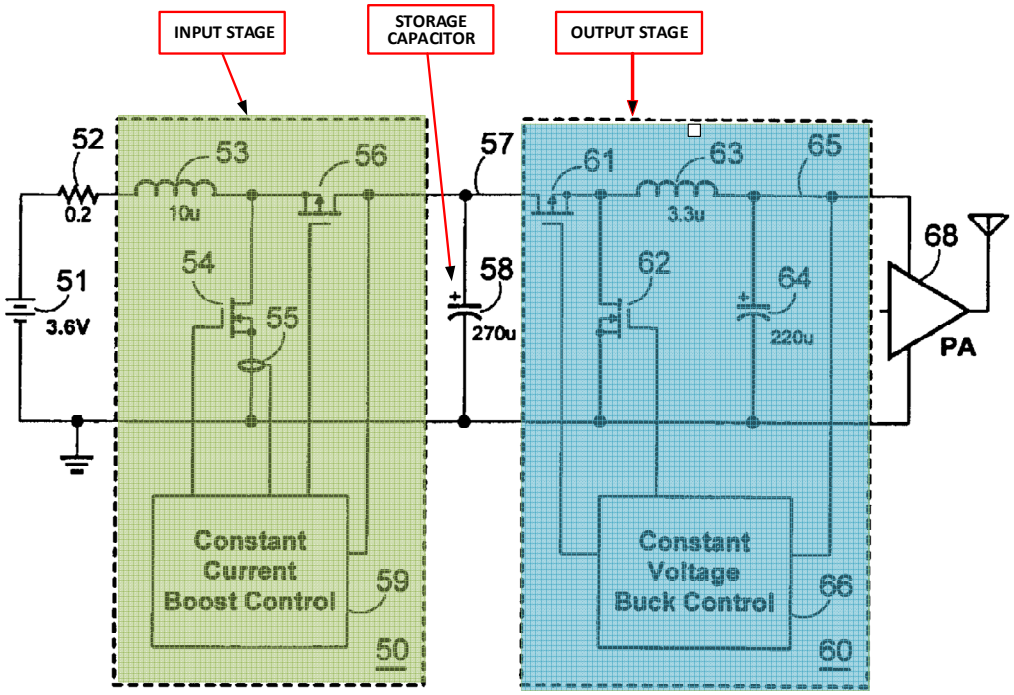


FIG. 5

Fig. 15

91) The input stage 50 operates to charge the storage capacitor 58 and thus increase the voltage across the capacitor. The output stage 60 operates to down-convert the voltage on the reservoir capacitor 58 to an output voltage, for example, 3.4V, needed by the PA 68, which the output stage 60 regulates. *Id.*, 4:36-50. During operation the storage or reservoir capacitor 58 supplies energy to the PA 68, such that if the input stage 50 ceases operating, the output stage continues powering the PA 68 for some further period of time. *Id.*.

VI. SUMMARY OF ARGUMENT

92) The ’848 patent claims a method to supply power, an apparatus that supplies power, and a power supply. The prior art herein is replete with this power supply. Mieth teaches most elements of the ’848 patent’s independent claims. For independent claim elements arguably not taught by Mieth, Balogh teaches first stage power converter features and cascaded first and second stages such as step-down power converters.

93) Liu discloses a capacitor as part of a power absorption circuit between cascaded power converters. Adding these features to Mieth’s system to supply power would have been obvious, and yields the alleged invention claimed in the ’848 patent.

94) In sum, as demonstrated by a preponderance of the evidence, including this prior art, the ’848 patent claims are unpatentable as being anticipated and/or obvious in view of the cited prior art.

VII. SPECIFIC GROUNDS FOR UNPATENTABILITY

A. Ground A: Anticipation of claims 1, 4, 5, 7-10, 13, 14, and 16-18 in view of Mieth

1. Independent Claim 1

95) With reference to the claim listing appendix, Mieth discloses elements [1A] – [1H].

i. [1A]: "An apparatus, comprising:"

96) Mieth (Ex.1002) discloses a circuit that supplies power to an electrical load from a solar generator. Ex.1002 (Mieth), 8:8-9. A PHOSITA understands that a "circuit" is a species of the genus term "apparatus." Thus, Mieth teaches [1A].

ii. [1B]: "a first stage power converter to generate a first output from a direct current input;"

97) There is no explicit definition of "first stage power converter" in the '848 patent specification, thus a PHOSITA, would construe "a first stage power converter" to be one or more circuit elements that converts one type or level of a voltage or current waveform to another. As such, the solar generator 1 of Mieth supplies a ***direct current input*** (dashed-red) to the capacitor 2. The supplied current charges the capacitor resulting in a voltage across its terminals. As specified in the claim, the first stage power converter merely generates a first output from a direct current input. The capacitor 2 performs that recited function and thus constitutes "***a first stage power converter***" as shown in Fig. 16 below. The "first stage power converter" of Mieth is a parallel capacitor 2 which converts the direct current input into a ***first output*** (dashed-green) as shown.

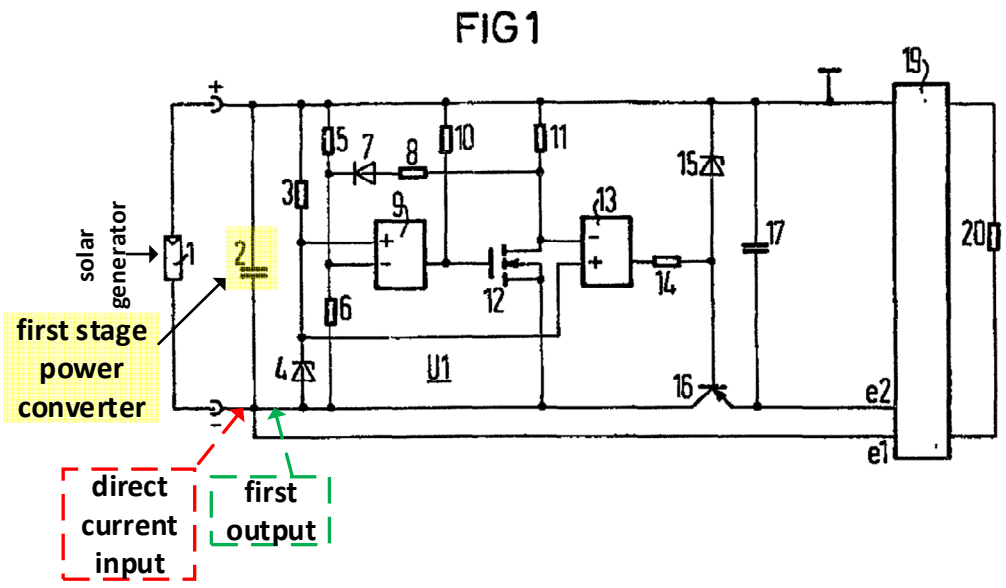


Fig. 16

98) Thus, Mieth teaches [1B].

iii. [1C]: "a second stage power converter connected to the first stage power converter to convert the first output to a second output"

99) In Mieth, a power supply apparatus 19 connected to a bipolar transistor 16 (second stage power converter-blue) together constitutes ***a second stage power converter connected*** (green) coupled to capacitor 2 that forms the first output (dashed-green), as illustrated below in Fig. 17. As stated above in ¶97, the capacitor 2 is a first stage power converter according to the claim language. The first stage power converter is connected (green) to the second stage power converter (blue), as shown in Fig. 17.

100) Still referring to the figure below, the power supply apparatus 19 ***is powered*** by way of auxiliary voltage input e2 which is coupled to the first output when the

bipolar transistor 16 is conducting. Ex.1002, 8:29-35. According to Mieth, the power supply apparatus 19 is a DC-DC voltage converter or a charging converter and outputs a voltage and current to power a load 20. *Id.* Thus. the power supply apparatus 19 is a power converter, and as a power converter, power supply apparatus 19 receives the first output and ***converts the first output to a second output*** (orange) as shown below in Fig. 17. As shown, the second output is provided by the second stage power converter 16/19 to the load 20.

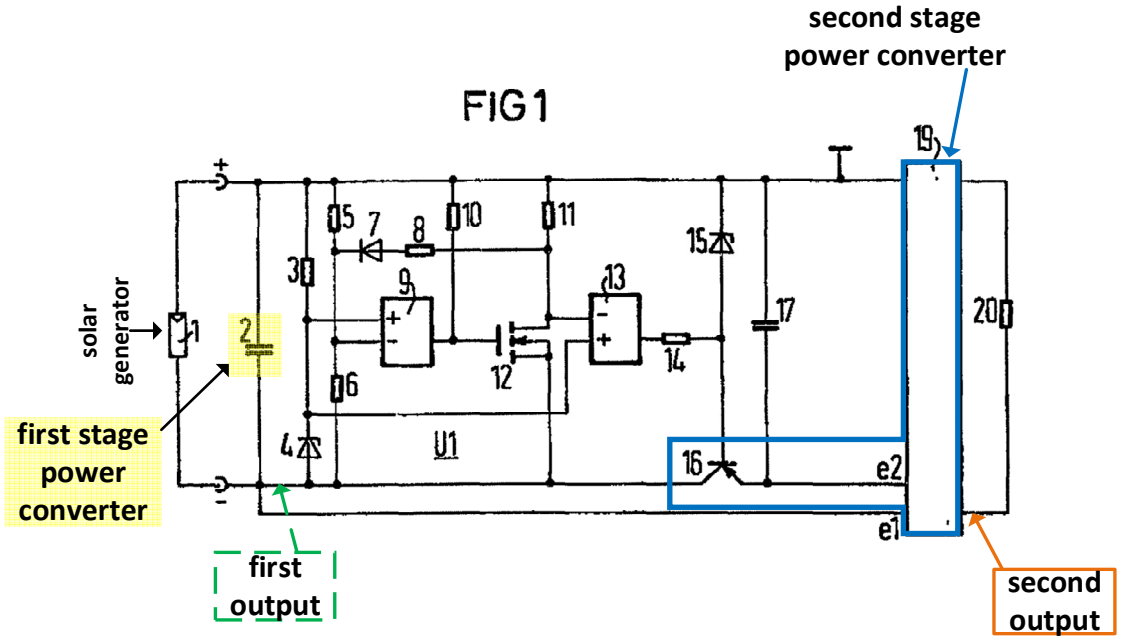


Fig. 17

101) Thus, Mieth discloses [1C].

iv. [1D]: "a micro-controller;"

102) Mieth discloses a circuit as shown below in Fig. 18. Mieth discloses a capacitor 2 (yellow) in parallel with the solar generator 1, and a power supply apparatus 19 connected to a bipolar transistor 16 (blue). Ex.1002, 9:5-9, 11:14-16. The capacitor 2 receives direct current from the solar generator 1, and provides a first output.

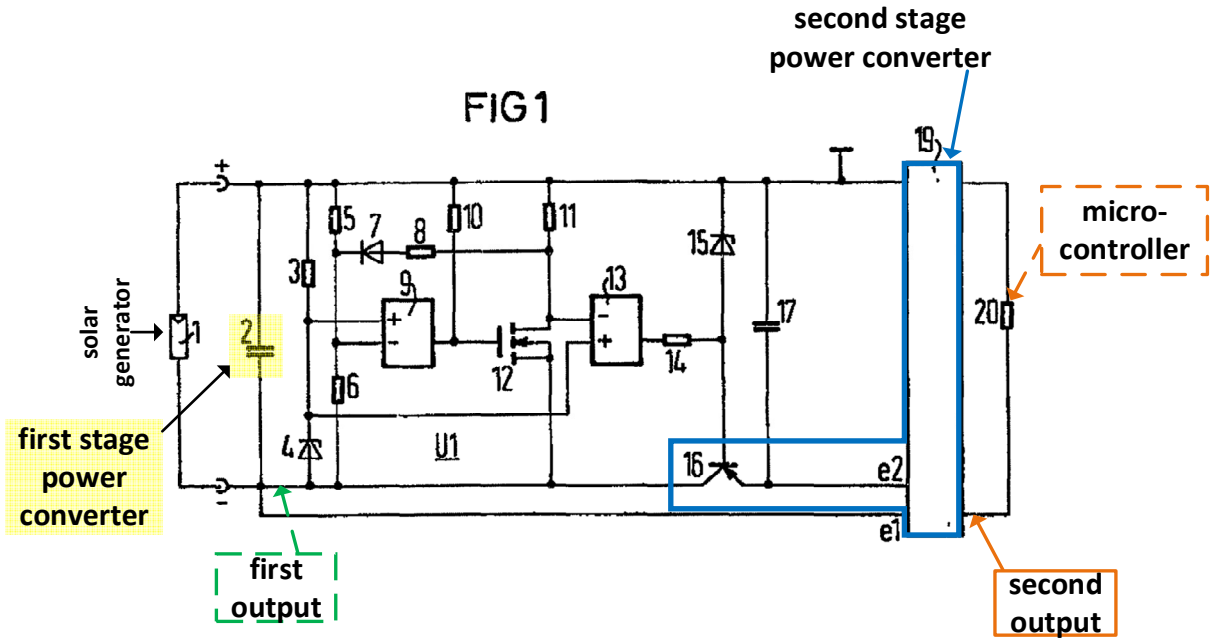


Fig. 18

103) The power supply apparatus 19 of Mieth is a DC-DC voltage converter or a charging converter and outputs a voltage and current to power a load 20 as shown in Fig. 18. A PHOSITA understands that the load 20 is a generic term, and can be or include a micro-controller. Ex.1014, 1180, Fig.5. As such, the load 20 is analogous to the claimed micro-controller (dashed-orange) as both the load 20

draws power from the second output and the micro-controller of the '848 patent draws power from the second output.

104) Thus, Mieth teaches [1D].

v. [1E]: "a power absorption circuit"

105) Mieth discloses that the first output (dashed-green) of capacitor 2 is connected to a field-effect transistor 12 that is connected to a preliminary load 11 as shown in Fig. 19. Ex.1002,10:5-14

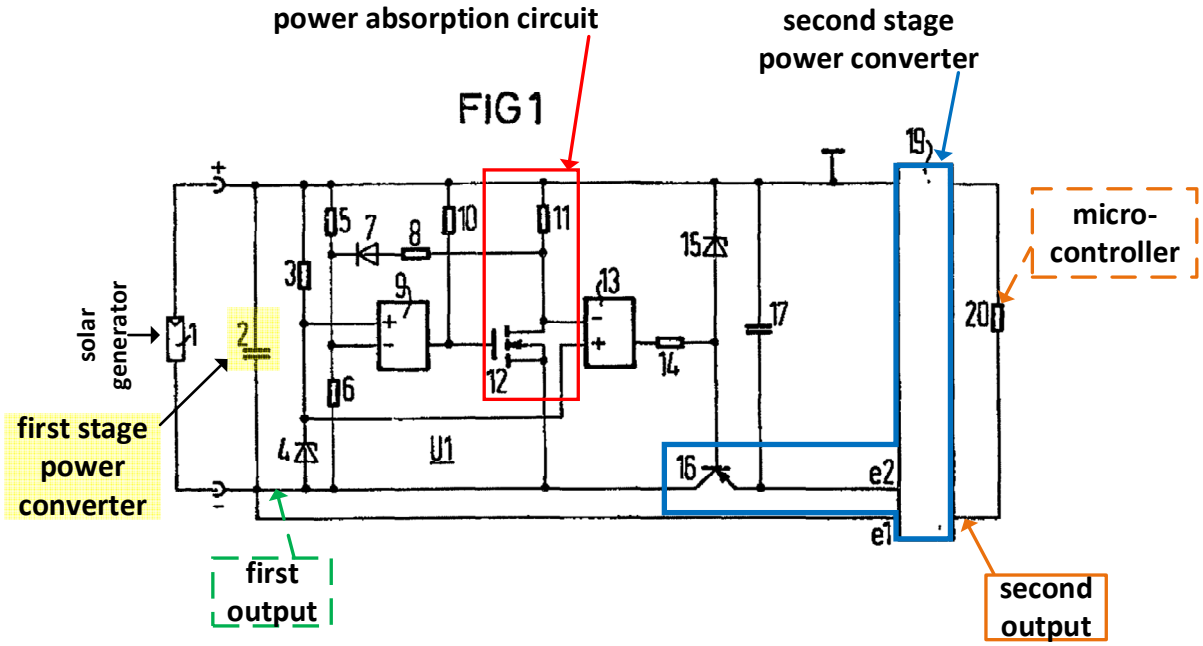


Fig. 19

106) Mieth describes the preliminary load 11 as consuming power from the solar generator 1, and thus a PHOSITA would understand that the preliminary load absorbs power. Ex.1002,11:14-25. Thus, the field-effect transistor 12, which

operates as a switch, and the preliminary load 11 in combination are analogous to the claimed ***power absorption circuit*** (red).

107) Thus, Mieth teaches [1E].

vi. [1F]: "a control circuit coupled with the first stage power converter and the second stage power converter, the control circuit powered by the first output to control the second stage power converter"

108) Mieth discloses a first comparator 9 that turns the transistor 12 "on" or "off" as shown in Fig. 20 below. Ex.1002,9:34-10-14

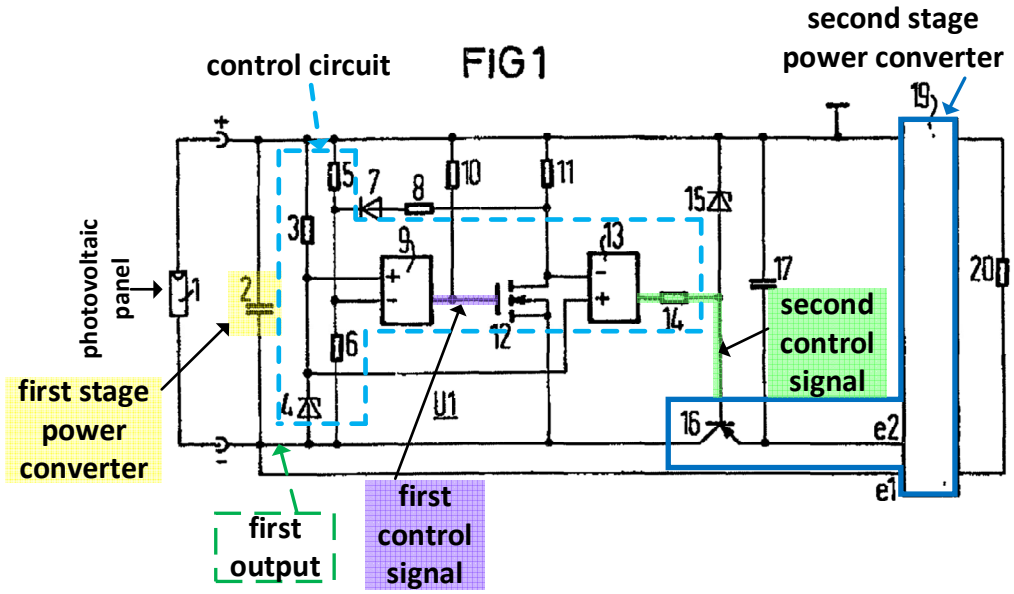


Fig. 20

109) First comparator 9 compares a reference voltage from a reference voltage generator to a representative voltage from a voltage divider. Ex.1002,9:34-10:3. The reference voltage generator is defined by the Zener diode 4. *Id.* The voltage

divider is defined by the voltage divider of resistors 5 and 6 and the representative voltage is representative of the first output (dashed-green) of capacitor 2 (first stage power converter-yellow). *Id.* First comparator 9 compares the representative voltage and the reference voltage to determine if the representative voltage exceeds a value defined by the reference voltage, and outputs a first control signal (highlighted-purple) to transistor 12 based on the comparison. Ex.1002,12:12-26.

110) A PHOSITA understands that a control circuitry (dashed-blue) that controls transistor 12, which includes first comparator 9, voltage divider 5, 6 and reference input generator 3, 4, which are powered by the first output from the capacitor 2, is analogous to the claimed **a *control circuit coupled with the first stage power converter*** and the claimed ***the control circuit powered by the first output***. Ex.1002,9:34-10:3.

111) The first control signal output from first comparator 9 controls transistor 12, and the output of transistor 12 is used by second comparator 13 to generate a second control signal (highlighted-green). Ex.1002,11:4-12,12:12-19. The second control signal output from second comparator 13 operates transistor 16, turning the transistor "on" or "off" which connects or disconnects power supply apparatus 19 to or from the first output. *Id.* When the first control signal is low, transistor 12 is "off" and second comparator 13 outputs a low voltage which turns transistor 16 "on," connecting the power supply apparatus 19 to the first output of capacitor 2.

Ex.1002,12:12-30. When the first control signal is high, transistor 12 is "on" which connects preliminary load 11 to the first output of capacitor 2, and second comparator 13 outputs a high voltage which turns transistor 16 "off," disconnecting power supply apparatus 19 from the first output of capacitor 2. Ex.1002,9:15-23,12:12-30.

112) Since first comparator 9 generates the first control signal that controls transistor 12 and second comparator 13 to then control transistor 16/power supply apparatus 19 by the second control signal, Mieth discloses the claimed ***to control the second stage power converter***. Furthermore, the first comparator 9 couples to transistor 16/power supply apparatus 19 through transistor 12 and the second comparator 13, and is analogous to the claimed ***a control circuit coupled with . . . the second stage power converter***.

113) Thus, Mieth teaches [1F].

vii. [1G]: "wherein; when the second stage power converter is in a first mode of not providing the second output to power the micro-controller, the control circuit monitors a voltage of the first output powering the power absorption circuit and signals the second stage power converter to remain in the first mode during a time period in which the voltage is below a threshold"

114) As shown in Fig. 21, Mieth can be configured in a first mode (highlighted-pink) where transistor 16 is "off" and power supply apparatus 19 (second stage power converter-blue) is disconnected from the first output of capacitor 2 (first stage

power converter-highlighted-yellow). Ex.1002,12:12-30.

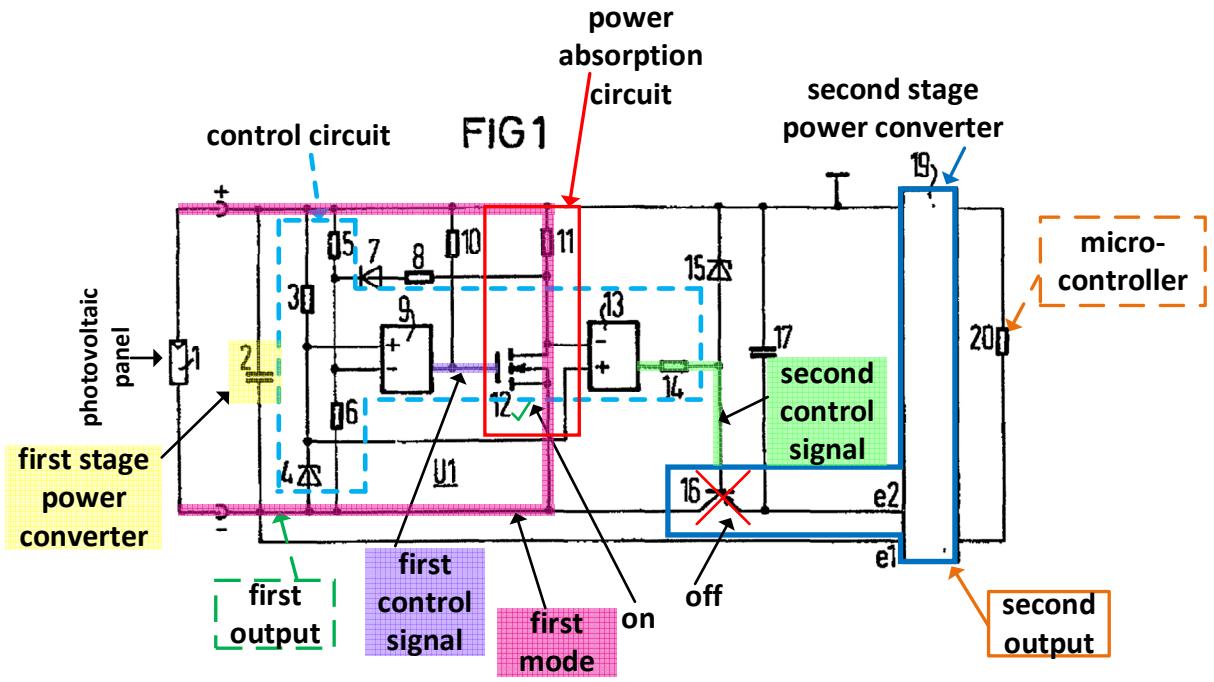


Fig. 21

115) When transistor 16 is "off," power supply apparatus 19 is disconnected from the first output (dashed-green) of capacitor 2, and load 20 (micro-controller-dashed-orange) is not powered by the second output (orange). Ex.1002,8:29-35,9:9-13,9:23-32. Transistor 16 being off and power supply apparatus 19 disconnected from the first output of capacitor 2, resulting in load 20 not powered by the second output is analogous to the claim feature ***when the second stage power converter is in a first mode of not providing the second output to power the micro-controller.***

116) Furthermore, in the first mode, transistor 12 is turned "on" and the first output powers preliminary load 11 (power absorption circuit-red). Ex.1002,10:5-14. First comparator 9 (part of the control circuit-dashed-blue) turns transistor 12 "on"

based on a comparison of a reference voltage (*i.e.,* reference voltage generator defined by Zener diode 4) and a representative voltage (voltage at the junction of resistors 5 and 6) representative of the first output voltage. Ex.1002,9:34-10:3. First comparator 9 that connects preliminary load 11 to the first output through control of transistor 12 based on the representative voltage of the first output is analogous to the claimed ***the control circuit monitors a voltage of the first output powering the power absorption circuit***.

117) The representative voltage at first comparator 9 is compared to a "predefined minimum value," (*e.g.*, associated with a threshold voltage) and during a time period when the representative voltage is lower than the predefined minimum value, the first control signal from first comparator 9 is a high voltage which turns transistor 12 "on." Ex.1002,11:4-12,12:12-26. The time period when the representative voltage is lower than the predefined minimum value is analogous to the claimed ***during a time period in which the voltage is below a threshold***.

118) When transistor 12 is "on," preliminary load 11 is connected to the first output of capacitor 2, which signals a high voltage to second comparator 13, which signals a high voltage to transistor 16, turning power supply apparatus 19 "off," which disables the second output from powering load 20. Ex.1002,9:15-23,12:12-30. Therefore, first comparator 9 turning transistor 12 "on" signals power supply apparatus 19 to be turned "off" through transistor 16, thereby disabling the second

output from powering the load, which is analogous to the claimed ***signals the second stage power converter to remain in the first mode***.

119) As such, Mieth teaches [1G].

viii. [1H]: "when the voltage is above the threshold, the control circuit signals the second stage power converter to enter a second mode of providing the second output to power the micro-controller"

120) As discussed in accordance with [1G] in ¶¶114-118, in the first mode, the preliminary load 11 and the field-effect transistor 12 (*i.e.,* power absorption circuit-red) are powered by the first output of capacitor 2 (*i.e.*, first stage power converter-highlighted-yellow). Mieth further discloses that when voltages from the solar generator 1 (as represented at the negative input terminal of first comparator 9) are above a predefined minimum value (as represented at the positive input terminal of first comparator 9), the auxiliary voltage input e2 of the power supply apparatus 19 is connected to the first output of the solar generator 1. Ex.1002,9:23-26. As shown in Fig. 22 below, when the predefined minimum value is satisfied, the circuit of Mieth operates in a ***second mode*** (highlighted-pink) where the bipolar transistor 16 is "on" or conducting, causing the first output (dashed-green) of capacitor 2 to be connected to e2 thereby powering the power supply apparatus 19.

Ex.1002,10:16-29.

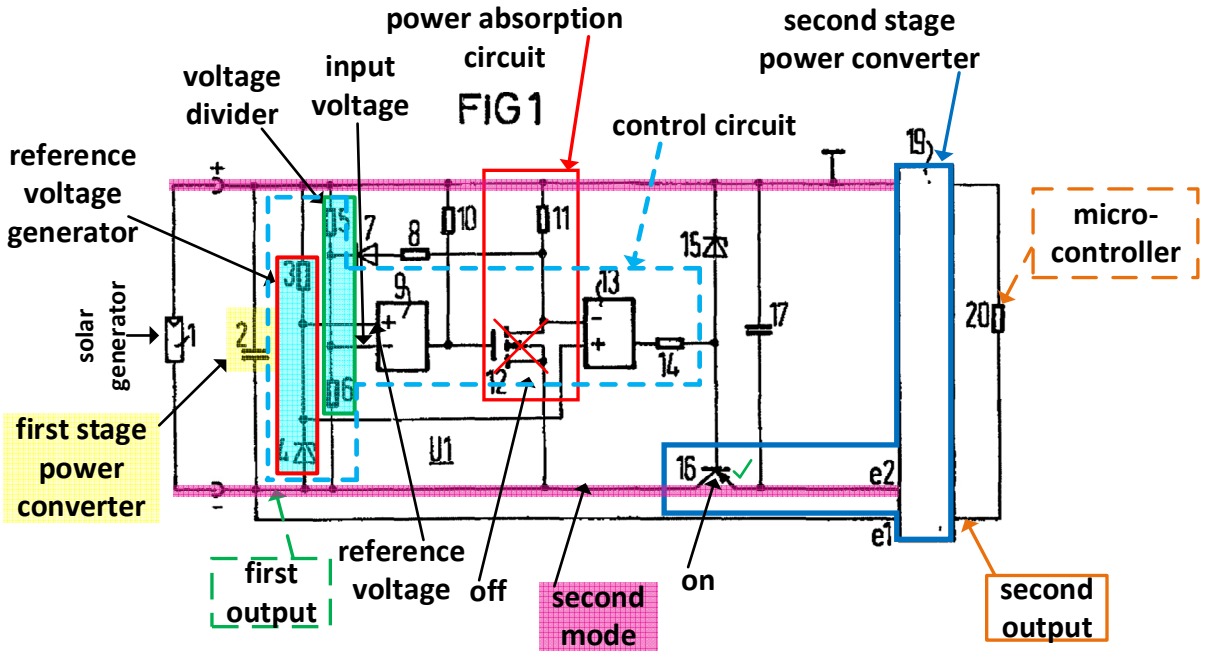


Fig. 22

121) Furthermore, in the second mode, the field-effect transistor 12 is "off" or non-conducting, thereby disconnecting the preliminary load 11 from the first output. *Id*. As discussed in ¶¶114-118, the first comparator 9 of the control circuit compares a reference voltage from a reference voltage generator (highlighted-teal-outlined-red) to a representative voltage from a voltage divider (highlighted-teal-outlined-green) to determine if the representative voltage exceeds a value defined by the reference voltage. Ex.1002,12:12-26. While in the first mode, when the first output of capacitor 2 rises and the representative voltage at the output of voltage divider 5, 6 is above the value (*i.e.,* "predefined minimum value" as quoted by Mieth), the circuit disconnects the preliminary load 11 from the first output by

configuring the field-effect transistor 12 to an "off" state. *Id*. The output of voltage divider 5, 6 rising above the value is analogous to the claimed ***when the voltage is above the threshold***.

122) The bipolar transistor 16 connecting the power supply apparatus 19 to the first output resulting in the second output of the power supply apparatus 19 powering the load 20 is analogous to the claimed ***the control circuit signals the second stage power converter to enter a second mode of providing the second output to power the micro-controller.***.

123) Thus, Mieth discloses element [1H].

124) As Mieth discloses each and every element [1A]-[1H], Mieth anticipates claim 1.

2. Dependent Claim 4

125) Claim 1 is disclosed by Mieth. See paragraphs 96-124. Claim 4 depends from claim 1 and requires, "wherein the power absorption circuit comprises a switchable load." Ex.1001, claim 4.

126) As discussed in detail in paragraphs 105-107, Mieth discloses a preliminary load 11 and a field-effect transistor 12 which operates as a switch as shown in

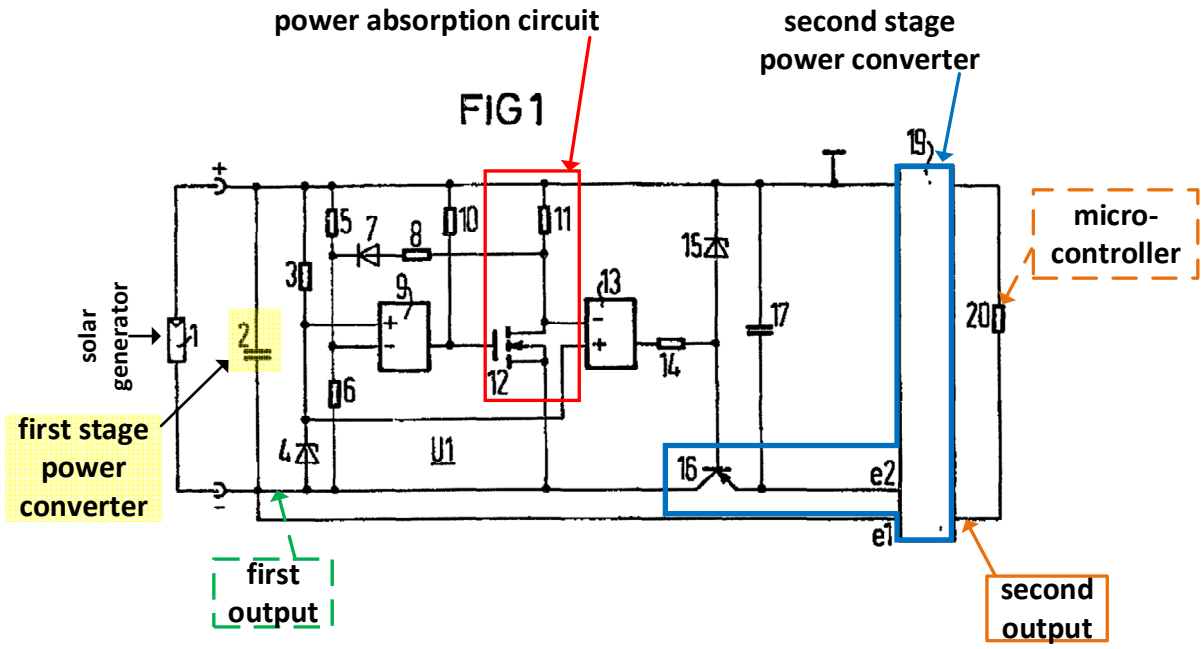


Fig. 19. Ex.1002,10:5-14. The preliminary load 11 is a resistor which is a load. Since the preliminary load 11 is connected or disconnected from the fist output based on the first mode or the second mode by the field-effect transistor 12, as discussed in ¶¶114-119, the preliminary load 11 and the field-effect transistor 12 are analogous to the claimed ***switchable load***.

127) Thus, Mieth discloses claim 4.

3. Dependent Claim 5

128) Claim 4 is disclosed by Mieth. *Supra*, 125-127, Claim 5 depends from claim 4 and requires [5A], "wherein the control circuit signals the switchable load to be in a first state to consume the first output when the second stage power converter is in the first mode." Ex.1001, claim 5.

129) As described in ¶¶114-119 and shown below in Fig. 23, Mieth teaches the claimed ***first mode*** where the power supply apparatus 19 (*i.e.,* second stage power converter-blue) is disconnected from the claimed ***first output***.

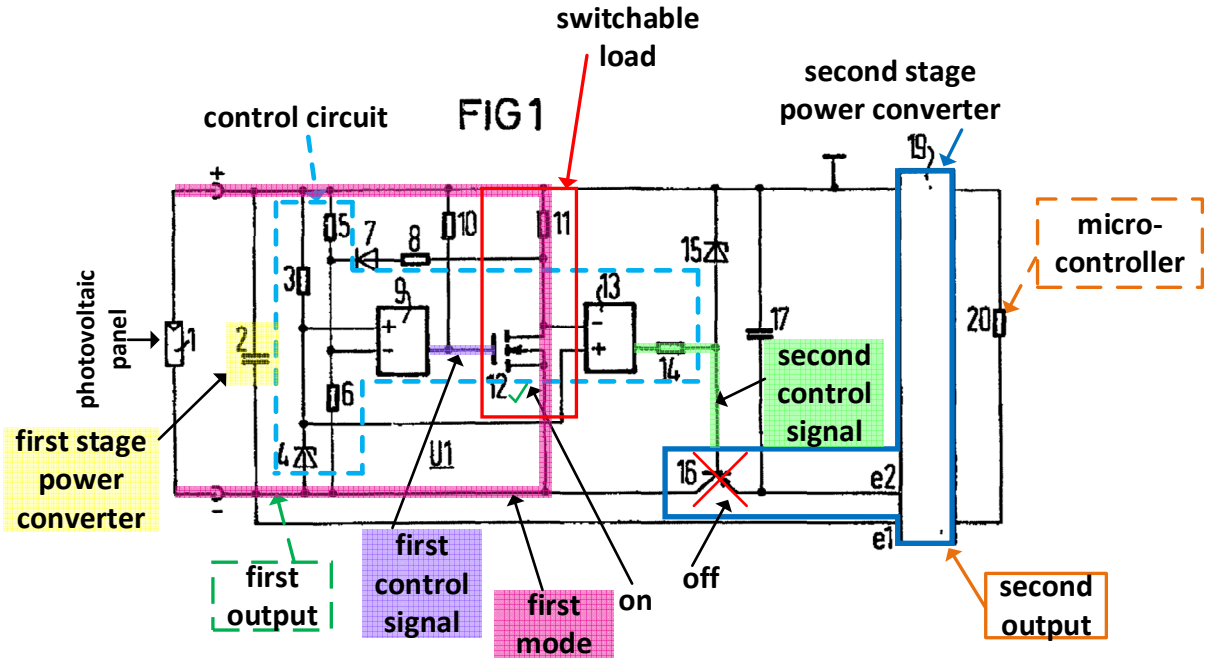


Fig. 23

130) In the first mode, the first comparator 9 of the control circuit turns transistor 12 "on" by a first control signal (highlighted-purple) associated with the voltage comparison performed by comparator 9. Ex.1002,9:34-10:3,11:4-12,12:12-26. When the transistor 12 is "on," the preliminary load 11 is connected to the first output to consume the first output. *Id.* As discussed in ¶¶125-127, the transistor 12 and preliminary load 11 are analogous to the claimed ***switchable load***, and the condition where the preliminary load 11 is connected to the first output is analogous to the claimed ***first* state**. *Id.* Thus, the first control signal from

comparator 9 that turns transistor 12 "on" thereby connecting the preliminary load 11 to the first output is analogous to the claimed ***the control circuit signals the switchable load to be in a first state to consume the first output***. The preliminary load 11 is connected to the first output while the power supply apparatus 19 is disconnected from the first output during the first mode which is analogous to the claimed ***when the second stage power converter is in the first mode.***¶¶114-119.

131) Thus, Mieth teaches [5A].

132) Claim 5 further requires [5B], "and to be in a second state not to consume the first output when the voltage is above the threshold." Ex.1001, claim 5. As shown in Fig. 24, Mieth teaches the claimed second state, where the preliminary load 11 and transistor 12 are disconnected and not consuming the first output when the voltage at the output of voltage divider 5, 6 is above the claimed threshold.

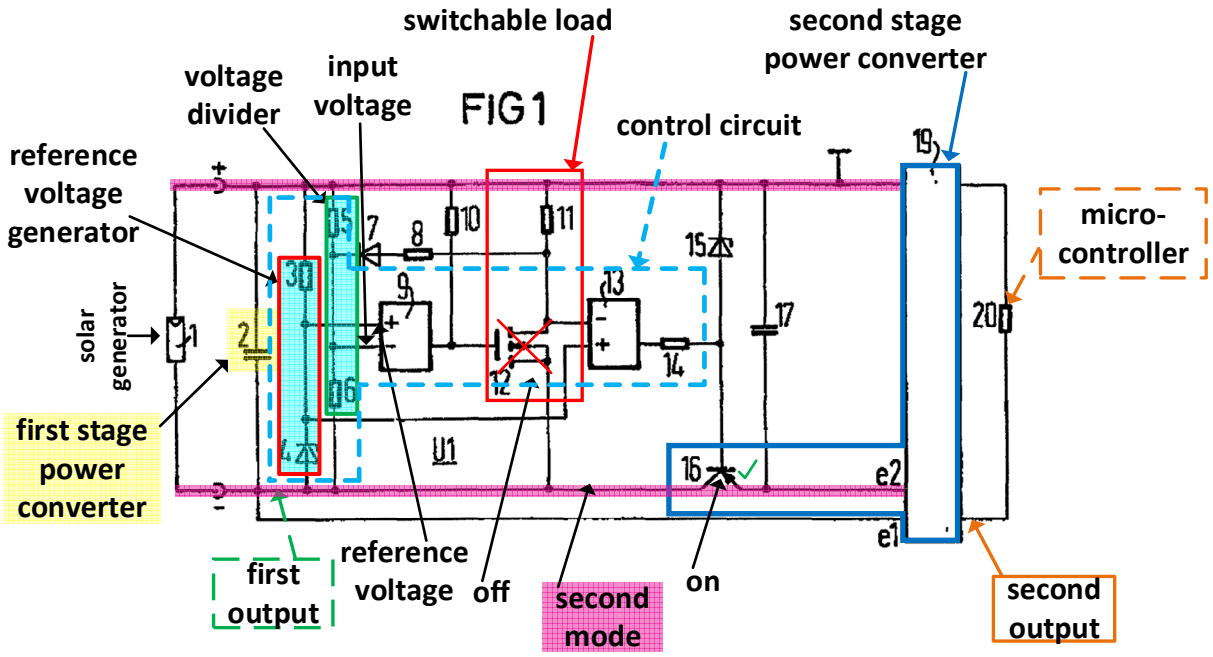


Fig. 24

133) Mieth discloses that when voltages from the solar generator 1 are above a predefined minimum value (which is analogous to the claimed ***threshold***), the auxiliary voltage input e2 of the power supply apparatus 19 is connected to the first output of the solar generator 1, described previously as the second mode. Ex.1002,9:23-26; ¶¶120-124 The first comparator 9 of the control circuit compares a reference voltage from a reference voltage generator (highlighted-teal-outlined-red) to a representative voltage from a voltage divider (highlighted-teal-outlined-green) to determine if the representative voltage exceeds the predetermined minimum value defined by the reference voltage. Ex.1002,12:12-26. When the first output of capacitor 2 rises and the representative voltage at the output of

voltage divider 5, 6 is above the predefined minimum value, the control circuit disconnects the preliminary load 11 from the first output by configuring the field-effect transistor 12 to an "off" state. *Id*. The transistor 12 turning "off" and disconnecting the preliminary load 11 from the first output is analogous to the claimed ***to be in a second state not to consume the first output***. The voltage at the output of voltage divider 5, 6 rising above the value is analogous to the claimed ***when the voltage is above the threshold***.

134) Thus, Mieth teaches claim [5B] and every element of claim 5.

4. Dependent Claim 7

135) Claim 5 is disclosed by Mieth. Supra, ¶¶128-134. Claim 7 depends from claim 5 and requires [7A], "wherein the switchable load comprises: a resistive device." Ex.1001, claim 7. As shown below in Fig. 25, preliminary load 11 can be a resistor. Ex.1002,12:14-20 ("preliminary load formed by the resistor 11"). Since the preliminary load 11 can be a resistor, and a resistor is a resistive device, preliminary load 11 of Mieth is analogous to element [7A] the switchable load comprises: a resistive device.

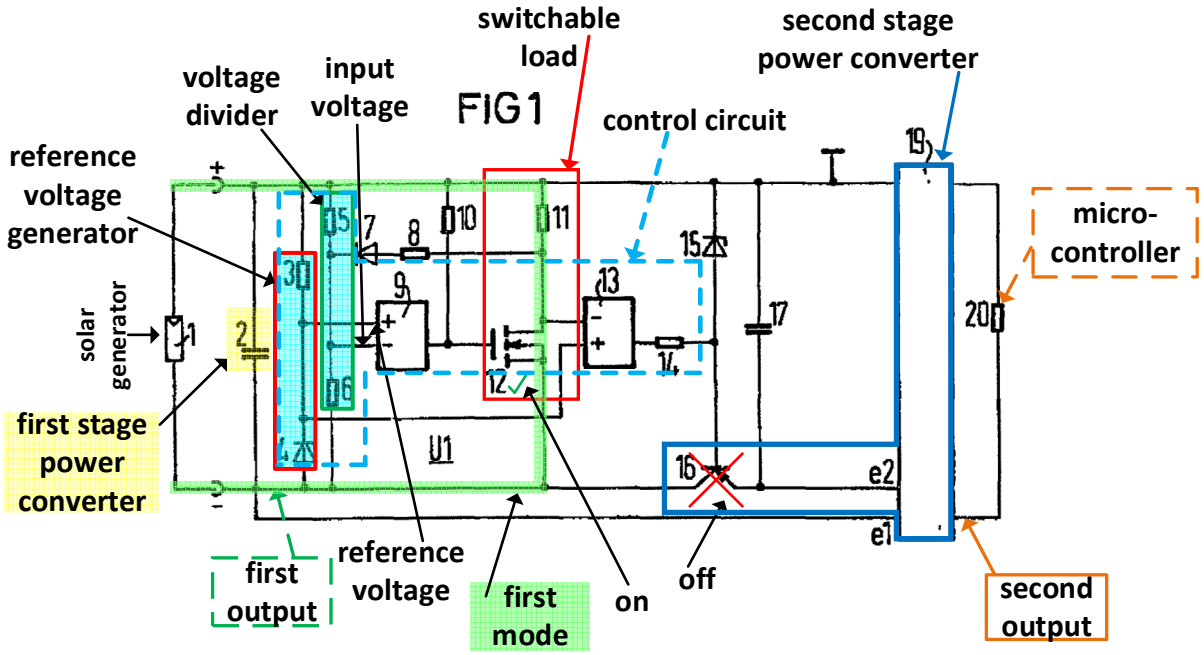


Fig. 25

136) Claim 7 further requires [7B], "a switching device connected to the resistive device." Ex.1001, claim 7. As shown in Fig. 25, the field-effect transistor 12 is connected to the preliminary load 11. *Supra*, ¶¶128-134. Mieth describes the field-effect transistor 12 as an electronic switch, and thus a PHOSITA would understand that the field-effect transistor 12 is a switching device. Ex.1002,10:5-14. As such, the field-effect transistor 12 connected to resistor 11 is analogous to the claimed, ***switching device connected to the resistive device*** of [7B].

137) Claim 7 further requires [7C] further recites, "wherein the switching device is turned on in the first state to connect the resistive device to the first output and turned off in the second state to disconnect the resistive device from the first

output." As discussed above in ¶¶114-124, and ¶¶128-134 the control circuit of Mieth is configured to operate in two different modes: (1) a first mode associated with "low" first output voltages, where the switchable load is connected to and consumes the first output, and the second output is not powered, and (2) a second mode associated with "high" first output voltages, where the switchable load is disconnected, and power from the first output connects to the second power converter which, in response, powers the micro-controller via the second output.

138) As stated in ¶¶114-119, feature [1G], in the first mode, for "low" first output voltages, transistor 12 is turned "on" by the first comparator 9 and loads the first output with the preliminary load 11 (analogous to the switchable load-red). Ex.1002,9:15-32,10:5-14. In the first mode, the first comparator 9 compares the reference voltage at the positive input terminal of the first comparator 9 to the representative voltage at the negative input terminal of the first comparator 9. Ex.1002,9:34-10:3.

139) In the first mode, the representative voltage is less than the reference voltage in magnitude (*i.e.,* a "low" voltage condition at the first output), and the first comparator 9 turns on the transistor 12 and powers the preliminary load 11 and field-effect transistor 12 by the first output. Ex.1002,12:12-19. Thus, the control circuit and transistor 12 are analogous to feature [7C], ***wherein the switching***

device is turned on in the first state to connect the resistive device to the first output.

140) Mieth further discloses that when voltages from the solar generator 1 (as represented at the negative input terminal of first comparator 9) are above a predefined minimum value (*i.e.*, relatively "high" first output voltages), the control circuit transitions the circuit to the second mode, where the auxiliary voltage input e2 of the power supply apparatus 19 is connected to the first output of the solar generator 1. Ex.1002,9:23-26. As shown in Fig. 26 below, when the predefined minimum value is exceeded, the circuit of Mieth operates in the second mode (highlighted-pink) where the first output (dashed-green) is connected to e2 to power the power supply apparatus 19. Ex.1002,10:16-29.

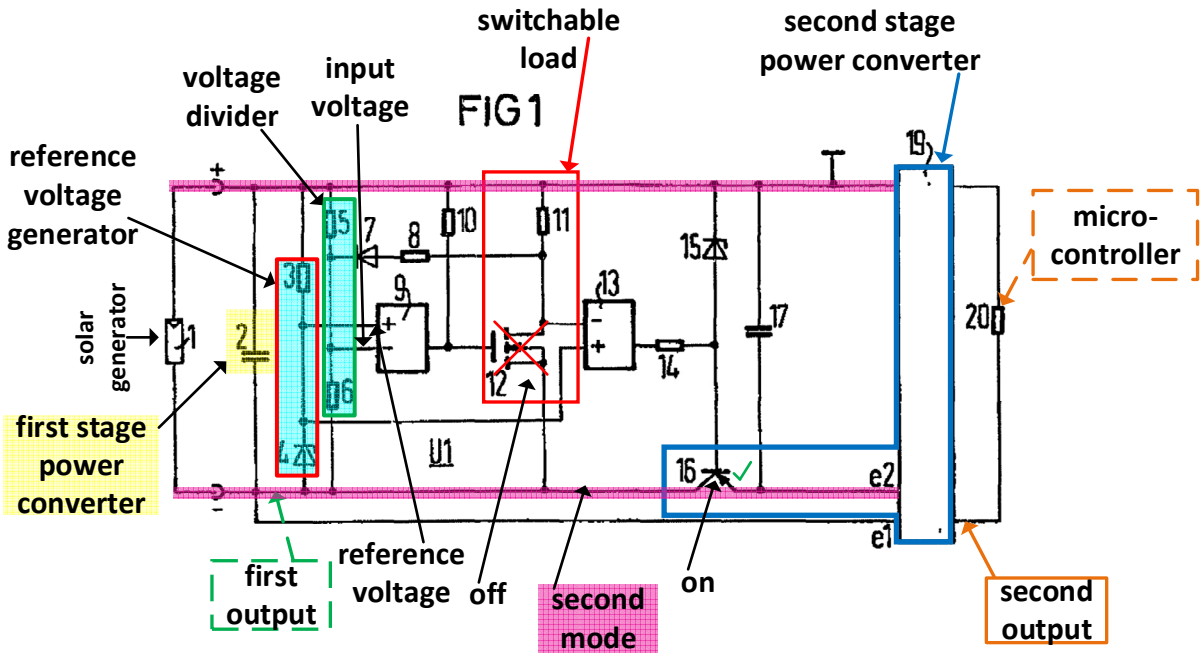


Fig. 26

141) Furthermore, in the second mode, the field-effect transistor 12 is "off" or non-conducting, thereby disconnecting the preliminary load 11 from the first output. *Id*. As discussed in ¶¶114-119 and ¶¶120-124, the first comparator 9 compares the reference voltage to the representative voltage to determine if the representative voltage exceeds a threshold defined by the reference voltage. Ex.1002,12:12-26. While in the first mode, when the first output rises in magnitude and the representative voltage exceeds the threshold (*i.e.,* "predefined minimum value" as quoted by Mieth), the time period of the first mode ends, and the control circuit disconnects the preliminary load 11 from the first output by configuring the field-effect transistor 12 to an "off" state, which results in the preliminary load 11 (*i.e.,* the switchable load) not consuming the first output in the second state. Thus, the control circuit of Mieth teaches the remaining claim feature [7C] ***wherein the switching device is... turned off in the second state to disconnect the resistive device from the first output.*** *Id*.

142) Thus, Mieth teaches all the features of claim 7.

5. Dependent Claim 8

143) Claim 5 is disclosed by Mieth. *Supra,* ¶¶128-134 Claim 8 depends from claim 5 and requires "wherein the control circuit delays a first signal instructing the switching device to change from the first state to the second state to generate a second delayed signal that instructs the second stage to change from the first mode

to the second mode." Ex.1001, claim 8. It is noted that there is no antecedence for the feature "first stage" rendering claim 8 indefinite. Further analysis is provided construing the feature "first stage" as the "first stage power converter" from claim 1.

144) In the first mode, the output of the first comparator 9 (*i.e.,* the claimed first signal-highlighted-purple), which controls the field-effect transistor 12 (switching device-highlighted-teal), is "high," turning transistor 12 "on" (*i.e.,* the claimed first state for the switchable load) Ex.1002,12:21-30; Ex.1002, Fig. 27.

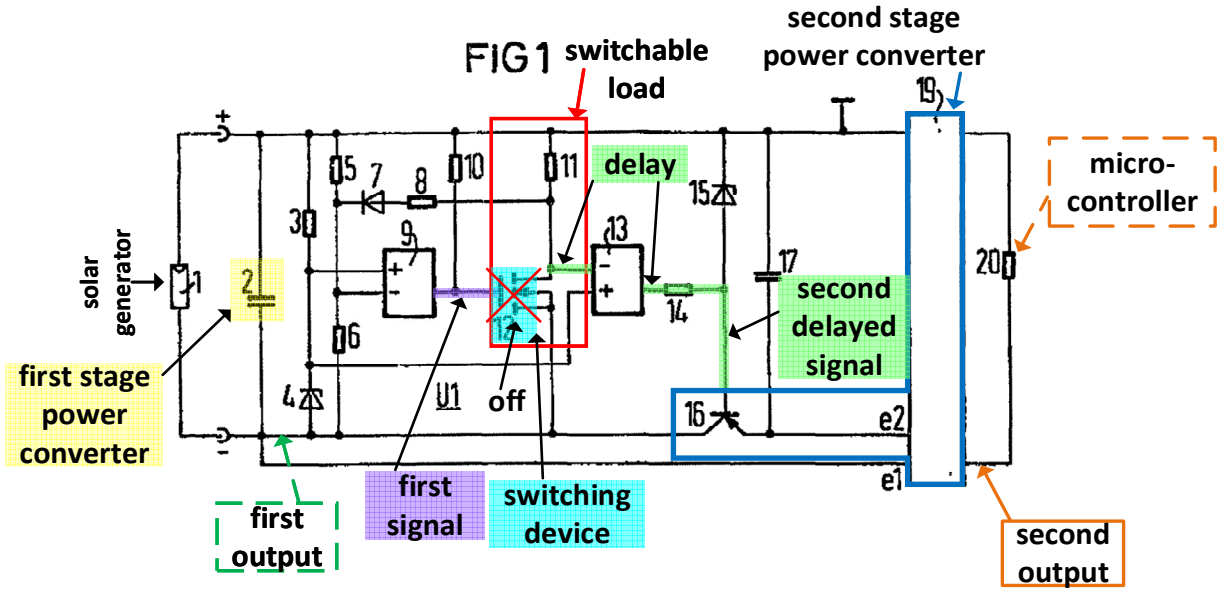


Fig. 27

145) When the first output reaches a high voltage, the output of the first comparator 9 turns the transistor 12 "off" (*i.e.,* when the output voltage at the first output reaches the desired level, the representative voltage at the negative input of comparator 9 exceeds the predefined minimum value – analogous to the claimed second state).

Ex.1002,10:16-29,12:21-30. The circuit signal from the first comparator 9 that feeds the gate of the transistor 12 of Mieth is analogous to **the *first signal*** of claim 8.

146) Mieth discloses delaying the first signal from the first comparator 9 to generate a second delayed signal at the output of the second comparator 13 to enable the second stage power converter to power the load 20. Mieth discloses that the field-effect transistor 12 and the second comparator 13 delays the first signal from the first comparator 9 to generate a second delayed signal (highlighted-green) that turns on the bipolar transistor 16. More particularly, the second comparator 13 outputs the second delayed signal based on an output from the field-effect transistor 12, where the output from the field-effect transistor 12 (*i.e.,* the drain terminal thereof) is itself based on the first signal. *Id*. As such, the state of the second delayed signal is dictated by the state of the first signal, and the transition of the second delayed signal to activate bipolar transistor 16 is delayed with respect to the transition of the first signal by the propagation delays of the transistor 12 and the second comparator 13 which is analogous to the claimed ***delays the first signal***. The second comparator 13 generates the second delayed signal based on the first signal which is analogous to the claimed ***to generate a second delayed signal***, and the second delayed signal controls the bipolar transistor 16 which operates as a switch to selectively pass the first output to the second stage power converter 19 at

the e2 terminal. Upon the second stage power converter 19 being powered by the first output via bipolar transistor 16 at e2, the second stage power converter 19 provides the second output that powers the load 20, which is the micro-controller (see ¶103). This circuit functionality is analogous to claim 8 that recites, ***instructing the switching device to change from the first state to the second state . . . that instructs the second stage to change from the first mode to the second mode.***

147) Furthermore, if it is contended that the *delaying the first signal* should be defined by a specific delay circuitry rather than the intrinsic switching and delay characteristics of comparator 13 and switch 12, a PHOSITA would have known to add a capacitor (optionally with a series resistor to form an RC delay circuit) parallel to resistor 11 according to customary practices in the art at the time of filing. Further, or in alternative, one or more buffer circuits or delay elements could be interposed between the second comparator output and the base of bipolar transistor 16 to define a larger delay period, as is well known and customary in the general knowledge of a PHOSITA. Ex.1015,3:53-63,Fig.3

148) Thus, Mieth teaches all the features of claim 8.

6. Dependent Claim 9

149) Claim 9 depends from claim 8. With reference to the claim listing appendix, Mieth discloses elements [9A]-[9B] as provided below

i. [9A]: "wherein the control circuit comprises: a hysteresis amplifier coupled to the first output to generate the first signal."

150) A PHOSITA understands hysteresis is a positive feedback loop between the output of a device and an input of a device, such as an amplifier or comparator, to mitigate instability in switched signals (see ¶¶56-63). A PHOSITA would further understand that an amplifier can be configured as a comparator, and thus the first comparator 9 can be an amplifier.

151) As shown in Fig. 28 below, Mieth discloses a capacitor 2 (highlighted-yellow) that outputs a first output (dashed-green) analogous to the claimed first output, and the first comparator 9 (dashed-blue) that is analogous to the claimed hysteresis amplifier that outputs a first signal (highlighted-purple) analogous to the claimed first signal of [9A] as discussed further below.

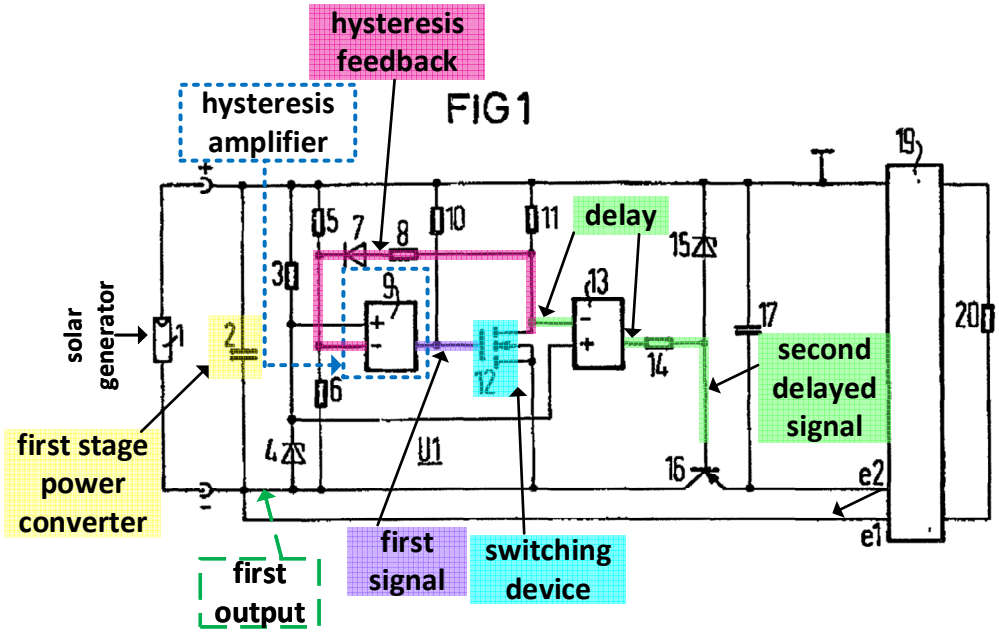


Fig. 28

152) The first comparator 9 is configured with hysteresis where the hysteresis feedback path (highlighted-pink) from the output of the switching device (field-effect transistor 12) is connected to the negative input of the first comparator 9 through resistor 8 and diode 7. Ex.1002,9:34-38. Furthermore, Mieth recites that "[h]ysteresis is achieved by means of the resistor 8." Ex.1002,12:26-27. Specifically, when the switch 12 is off, the series circuit comprising resistors, 8, 11 and diode 7 are in parallel with resistor 5 forming a voltage divider with resistor 6. When the switch 12 is on, diode 7 is off and no current flows through resistor 8 leaving only resistors 5 and 6 to form the voltage divider. In this way the first comparator 9 and associated circuitry exhibit hysteretic behavior. Since the first comparator 9 can be an amplifier with a positive feedback loop, the first comparator 9 is the same as the claimed ***hysteresis amplifier***. The first output of

the capacitor 2 is represented at the negative input of the first comparator 9 through a voltage divider defined by resistors 5 and 6 in addition to resistors 8 and 11 and diode 7 when first comparator 9 output is low, and the first comparator 9 outputs the first signal, which is analogous to the claimed ***hysteresis amplifier coupled to the first output to generate the first signal***. Ex.1002,9:34-38.

153) Thus, Mieth teaches [9A].

ii. [9B]: "a delay circuit coupled to the first signal to generate the second delayed signal."

154) The above Fig. 28 further illustrates the field-effect transistor 12 (switching device-highlighted-teal) and the second comparator 13 that delays the first signal (highlighted-purple) from first comparator 9 to generate a second delayed signal (highlighted-green). Ex.1002,Fig.1,11:4-12.

155) The delay circuit operates when the first signal goes low, causing transistor 12 to turn "off," and pulling the drain terminal thereof high due to lack of current flowing through resistor 11. With the drain terminal connected to the negative input terminal of the second comparator 13, the drain terminal going high causes the output of the second comparator 13 to go low (*i.e.,* the second delayed signal), which activates the bipolar transistor 16. The propagation delays from the first signal through the transistor 12 and the second comparator 13 constitute ***a delay circuit*** that delays the second signal with respect to the first signal. That is, when

the first signal goes low, the second signal goes low thereafter by a delay time period dictated by the transistor 12 and the second comparator 13.

156) Since, the field-effect transistor 12 and the second comparator 13 are coupled together and delay the first signal to generate the second signal at the output of the second comparator 13, the field-effect transistor 12 and the second comparator 13 are analogous to the claimed ***delay circuit coupled to the first signal to generate the second delayed signal***. However, if it is argued that the *delay circuit* should be defined by further specific circuitry rather than the intrinsic switching characteristics of second comparator 13 and switch 12, delay elements discussed in accordance with claim 8 in ¶¶143-148 can be implemented.

157) Thus, Mieth discloses [9B] and all elements of claim 9.

7. Independent Claim 10

158) With reference to the claim listing appendix, Mieth discloses Elements [10A]-[10H]. As explained below, a PHOSITA would have been motivated by Mieth to arrive at the alleged invention of claim 10.

i. [10A]: "A method to supply power, the method comprising:"

159) Mieth (Ex.1002) discloses a circuit that supplies power to an electrical load from a solar generator 1. Ex.1002(Mieth),8:8-9. A PHOSITA would understand that when the circuit of Mieth supplies power to the electrical load, the circuit is

performing a method to supply power to the electrical load. Thus, Mieth teaches [10A].

ii. [10B]: "providing a first stage power converter to generate a first output from a direct current input"

160) [10B] is analogous to [1B], and thus Mieth discloses [10B] for at least the same reasons Mieth discloses [1B] as described in §VII.A.1.ii.

iii. [10C]: "wherein the first stage power converter is coupled to a power absorption circuit"

161) The power absorption circuit of [10C] is analogous to the power absorption circuit of [1E], and thus Mieth discloses the power absorption circuit of [10C] for at least the same reasons Mieth discloses the power absorption circuit of [1E] as described in §VII.A.1.v. [10C] requires that the *first stage power converter is coupled to the power absorption circuit*. As described in ¶¶102-107, Mieth discloses that the first output of the capacitor 2 (first stage power converter) is connected to the field-effect transistor 12 and preliminary load 11 (power absorption circuit), which is analogous to the claimed ***first stage power converter is coupled to a power absorption circuit***. As such, Mieth teaches [10C] for the same reasons described in ¶¶105-107.

iv. [10D]: "providing a second stage power converter connected to the first stage power converter to convert the first output to a second output"

162) [10D] is analogous to [1C], and thus Mieth discloses [10D] for at least the same reasons Mieth discloses [1C] as described in ¶¶99-101.

v. [10E]: "wherein the second stage power converter is coupled to a micro-controller;"

163) The micro-controller of [10E] is analogous to the micro-controller of [1D], and thus Mieth discloses the micro-controller of [10E] for at least the same reasons Mieth discloses the micro-controller of [1D] as described in ¶¶102-107. [10E] requires *wherein the second stage power converter is coupled to a micro-controller*. As described in ¶¶102-107. and ¶¶120-124., Mieth discloses that the power supply apparatus 19 (second stage power converter) is coupled to a load 20 (micro-controller) and provides a second output to the micro-controller, which is the same as the claimed ***second stage power converter is coupled to a micro-controller***. As such, Mieth teaches [10E] for the same reasons described in ¶¶102-107. and ¶¶120-124.

vi. [10F]: "powering, by the first output, a control circuit that is coupled with the first stage power converter and the second stage power converter"

164) [10F] is analogous to [1F], and thus Mieth discloses [10E] for at least the same reasons Mieth discloses [1F] as described in ¶¶108-113.

vii. [10G]: "controlling, by the control circuit powered by the first output, the second stage power converter, by: when the second stage power converter is in a first mode of not providing the second output to power the micro-controller, monitoring a voltage of the first output powering the power absorption circuit and signaling the second stage power

converter to remain in the first mode during a time period in which the voltage is below a threshold; and"

165) [10G] is analogous to [1G], and thus Mieth discloses [10G] for at least the same reasons Mieth discloses [1G] as described in ¶¶114-119.

viii. 10H]: "when the voltage is above the threshold, signaling the second stage power converter to enter a second mode of providing the second output to power the micro-controller"

166) [10H] is analogous to [1H], and thus Mieth discloses [10H] for at least the same reasons Mieth discloses [1H] as described in ¶¶120-124.

8. Dependent Claim 13

167) Claim 13 is taught by Mieth. *Supra*, ¶¶158-166. Claim 13 depends from claim 10 and requires, "further comprising: providing, in the power absorption circuit, a switchable load." Ex.1001, claim 13. Claim 13 is analogous to claim 4, and thus Mieth discloses claim 13 for at least the same reason Mieth discloses claim 4 as described in ¶¶125-127.

9. Dependent Claim 14

168) Claim 13 is taught by Mieth. *Supra*, ¶167. Claim 14 depends from claim 13 and requires, "wherein the control circuit signals the switchable load to be in a first state to consume the first output when the second stage power converter is in the first mode and to be in a second state not to consume the first output when the voltage is above the threshold." Ex.1001, claim 14. Claim 14 is analogous to

claim 5, and thus Mieth discloses claim 14 for at least the same reason Mieth discloses claim 5 as described in ¶¶128-134.

10. Dependent Claim 16

169) Claim 14 is taught by Mieth. *Supra*, ¶168. Claim 16 depends from claim 14 and requires, "further comprising: providing, in the switchable load: a resistive device; and a switching device connected to the resistive device, wherein the switching device is turned on in the first state to connect the resistive device to the first output and turned off in the second state to disconnect the resistive device from the first output." Ex.1001, claim 16. Claim 16 is analogous to claim 7, and thus Mieth discloses claim 16 for at least the same reason Mieth discloses claim 7 as described in ¶¶135-142.

11. Dependent Claim 17

170) Claim 14 is taught by Mieth. *Supra*, ¶168. Claim 17 depends from claim 14 and requires, "further comprising: delaying, by the control circuit, a first signal instructing the switching device to change from the first state to the second state to generate a second delayed signal that instructs the second stage to change from the first mode to the second mode." Ex.1001, claim 17. Claim 17 is analogous to claim 8, and thus Mieth discloses claim 17 for at least the same reason Mieth discloses claim 8 as described in ¶¶143-148.

12. Dependent Claim 18

171) Claim 17 is taught by Mieth. *Supra*, ¶170. Claim 18 depends from claim 17 and requires, "further comprising: providing, in the control circuit, a hysteresis amplifier coupled to the first output to generate the first signal; and providing a delay circuit coupled to the first signal to generate the second delayed signal." Ex.1001, claim 18. Claim 18 is analogous to claim 9, and thus Mieth discloses claim 18 for at least the same reason Mieth discloses claim 9 as described in ¶¶149-157.

B. Ground B: Obviousness of claims 1, 4, 5, 7-10, 13, 14, and 16-20 in view of Mieth and Balogh

172) With reference to the claim listing appendix, Mieth is believed to disclose all the elements of claims 1, 4-5, 7-10, 13-14, and 16-18. To the extent it is argued that Mieth does not teach the first stage power converter (e.g., elements [1B] and [10B]), Balogh discloses a first stage power converter as set forth in elements [1B] and [10B]. Further, as explained below, a PHOSITA would have been motivated to combine together Mieth and Balogh to arrive at the alleged invention of claims 1, 4, 5, 7-10, 13, 14, and 16-20.

1. Independent Claim 1

i. [1B]: "a first stage power converter to generate a first output from a direct current input"

173) A PHOSITA understands that solar generators generate a direct current. Ex.1013, ¶21. As such, the solar generator 1 of Mieth supplies a ***direct current input*** (dashed-red) to the capacitor 2 as shown in Fig. 29 below, and generates a first output.

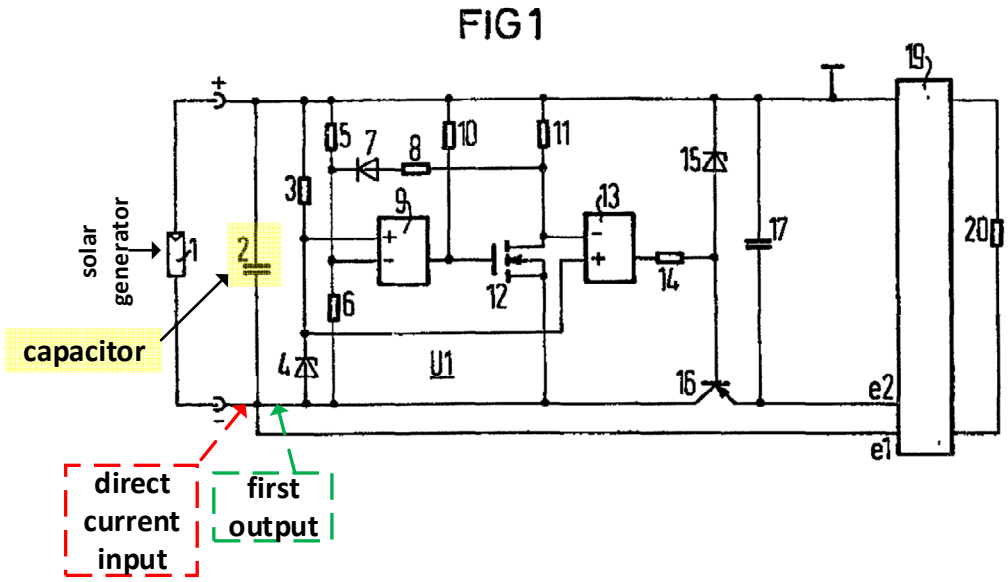


Fig. 29

174) Balogh discloses cascaded converter arrangements (*e.g.*, Ex.1003(Balogh), Figs.1B-1D), and states that cascaded arrangements using first and second buck converters are employed in circuit applications that require large input/output conversion ratios. Ex.1003,1:21-27. It is known to a PHOSITA that photovoltaic panels or modules can realize high input voltages, and such high input voltages need large input/output conversion ratios to step down the input voltage.

Ex.1003,1:21-27. Even a single photovoltaic module can see a voltage as high as 80V, which may necessitate a large input/output conversion ratio. Ex.1010; Ex.1011. Balogh teaches, in Fig 1D (Fig. 30 below), a cascaded converter arrangement using *a first stage transformer-coupled input power converter that steps down an input voltage to an intermediate voltage*, followed by a second stage buck output power converter that further steps down the intermediate voltage to a final voltage. Ex.1003,1:62-66. Thus, Balogh clearly discloses ***a first stage power converter***, as recited in element [1B] and shown in Fig. 30 below.

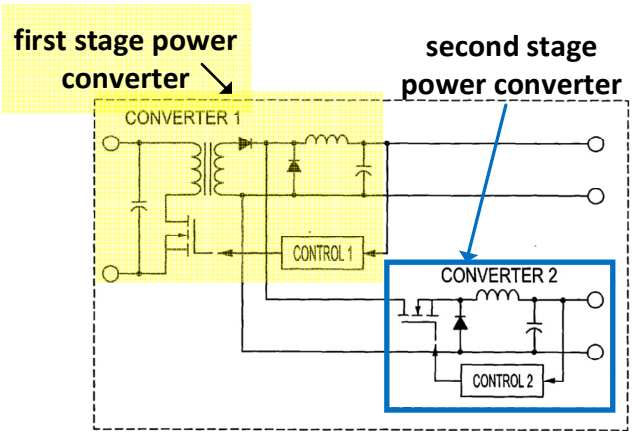


FIG. 1D
PRIOR ART

Fig. 30

175) Mieth states that applications having photovoltaic energy sources or wind energy sources often provide varying levels of input voltage that can create difficulties when serving as an input to a power converter. Ex.1002,5:22-38. Mieth further teaches the use of a switchable load in situations where an input voltage to a power

converter varies, such as the voltage from a photovoltaic system that will vary depending upon the time of day, or weather conditions. *Id.*

176) A PHOSITA is motivated to combine the cascaded power converter architecture of Balogh with Mieth. Balogh discloses the first stage power converter to replace the capacitor 2 of Mieth and configure two cascaded power converters with the switchable load feature of Mieth for DC applications with high input voltages. Mieth is directed towards solar generators that generate up to 36 volts. Ex.1002,12:21-26. Balogh discloses higher DC voltages relative to Mieth, for example, 48V with large step-down ratios, for example, 48V to 1.5V. Ex.1003, 10:45-52. In other prior art examples, solar panel modules can have 80V output voltages requiring large step-down ratios. Ex.1010; Ex.1011. As such, a PHOSITA would have known and been motivated to combine the cascaded power converter architecture of Balogh with Mieth for high DC applications (e.g., 48V or 80V solar panel modules) to realize an appropriate intermediate voltage for the power supply apparatus 19 (*i.e.,* second stage power converter) of Mieth.

177) The combination of Mieth-Balogh involves combining known prior art elements (Mieth's switchable load and step-down converter and Balogh's cascaded step down converter architecture) according to known methods to yield predictable results, i.e., a cascaded step-down power converter having a switchable load at the second power converter input that is selectively employed based on the output

voltage of the first stage step-down power converter. A PHOSITA would have had the skills, knowledge, and motivation to carry out the combination. A PHOSITA would have reasonably expected success in combining Mieth and Balogh as no significant modifications are required to implement. A PHOSITA would have appreciated the benefit of adapting the high DC voltage stepped down to an intermediate voltage of Balogh to situations with a variable input voltage to a power converter as shown in Mieth. As understood by a PHOSITA, there are no undue technical hurdles to applying Mieth with Balogh or vice-versa, as such a combination would have been a simple modification to Mieth's system, readily accomplished by a PHOSITA. Accordingly, Mieth in combination with Balogh is proper and teaches element [1B].

178) Specifically, while the capacitor 2 discussed above in ¶¶ 97-101 (see Fig. 17 above) provides the recited function of the first stage power converter as recited in the claims, and the bipolar transistor 16/power supply apparatus 19 is analogous to the claimed second stage power converter, Balogh discloses a cascaded converter arrangement having an isolated DC-DC converter in its first stage that is explicitly set forth as a first stage power converter that also receives a direct current input and provides a first output. Ex.1003, 10:45-52.

179) Balogh's isolated DC-DC converter (analogous to the first stage power converter-yellow) and post regulator circuit are cascaded step-down converters and are shown in Fig. 30, Ex.1003,2:61-64.

180) Based on Balogh, a PHOSITA would understand that cascaded converters are commonly used to provide input to output power conversion that is not optimally implemented in a single converter. Ex.1003,1:25-28. Thus, the purpose of the first stage power converter and the second stage power converter was previously described by Balogh, that is, to provide input-to-output power conversion that is not optimally implemented in a single converter, for example, in high DC voltage applications. Ex.1003,10:45-52. Balogh's DC-DC converter can replace the capacitor 2 of Mieth to provide a first output to be consumed by the switchable load or to power the second stage power converter, and the claimed second stage power converter uses the first output from the first stage to power the micro-controller, which is not optimally implemented by a single converter (e.g. the first stage power converter or the second stage power converter alone). As such, a PHOSITA, at the time of filing, would know that the capacitor 2 of Mieth could be replaced by the DC-DC converter of Balogh, and combined with the power supply apparatus 19 of Mieth to form a cascaded converter architecture as disclosed by Balogh.

181) In addition, it is well known in the art that improved efficiency can be achieved by cascading buck power converters when there is a large ratio of input to output voltage as described in Patent application: US 2007/0001653 (hereafter "Xu"). Ex. 1012. Xu states: "The present invention provides a two-stage power delivery system that employs cascaded buck stages. For high input-to-output voltage ratios, each cascaded buck stage has a more suitable (i.e., larger) duty cycle that results in a much lower total power loss than in a single-stage buck." Ex. 1012, ¶6.

182) In addition, Xu reflects further general knowledge of a PHOSITA that cascaded converters advantageously improve circuit efficiency. Ex.1012. Xu states that in some applications where there is a lower input-to-output voltage ratio, for example, like in Mieth, the first stage power converter can be configured with a duty cycle of one so that it operates as a well-known L-C filter for the subsequent second stage, thereby being substantially similar to Mieth's capacitor 2 input stage. For at least these reasons, it would have been obvious for a PHOSITA to combine Balogh with Mieth in view of the general knowledge of a PHOSITA, as shown by the teaching of Xu, where large output/input ratios are more efficient when implemented with cascaded buck converters.

183) Thus, Xu provides a teaching that a PHOSITA would readily consider a cascaded converter arrangement in various solar applications, such as the application taught in Mieth. As such, a PHOSITA, at the time of filing, would know that the

capacitor 2 of Mieth could be replaced readily by the first stage power converter of Balogh, and combined with the power supply apparatus 19 of Mieth to form a cascaded converter architecture as disclosed by Balogh.

184) Thus, Balogh discloses [1B], and in combination with Mieth.

ii.[1A]-[1H] are disclosed by Mieth-Balogh

185) As discussed in ¶¶95-124 Mieth discloses claim 1. As discussed in ¶¶173-184, Mieth in combination with Balogh disclose feature [1B], thus Mieth-Balogh also teach all the elements [1A]-[1H] of claim 1. Additionally, for the same reasons, Mieth-Balogh teach all of claims 4, 5, and 7-9.

2. Independent Claim 10

i.[10B]: "providing a first stage power converter to generate a first output from a direct current input"

186) [10B] is analogous to [1B], and thus Mieth-Balogh disclose [10B] for at least the same reasons Mieth-Balogh disclose [1B] as described in ¶¶173-185.

ii. [10A]-[10H] are disclosed by Mieth-Balogh

187) As discussed in ¶¶158-166 Mieth discloses claim 1. As discussed in ¶186 , Mieth in combination with Balogh discloses feature [10B], thus Mieth-Balogh also teach all the elements [10A]-[10H] of claim 1. Additionally, Mieth teaches claims 13-14, and 16-18 as discussed in §VII.A.8-§VII.A.12; therefore for the same reasons, Mieth-Balogh teaches claims 13-14, and 16-18.

3. Independent Claim 19

188) With reference to the claim listing appendix, Mieth and Balogh disclose elements [19A]-[19J]. As explained below, a PHOSITA would have been motivated to combine together Mieth and Balogh to arrive at the alleged invention of claim 19.

i. [19A]: "A power supply for use in a solar electric production system"

189) Mieth (Ex.1002) discloses a circuit that supplies power to an electrical load from a solar generator. Ex.1002, 8:8-9. A PHOSITA would understand that a solar generator is a solar electric production system. Thus, Mieth teaches [19A].

ii. [19B]: "the power supply comprising: a first stage power converter"

190) As shown below in Fig. 31, Mieth discloses a circuit with a capacitor 2 (yellow) in parallel with a solar generator. Ex.1002,9:5-9. As discussed in accordance with [1B], the capacitor 2 is analogous to the claimed ***first stage power converter***. ¶¶97-98.

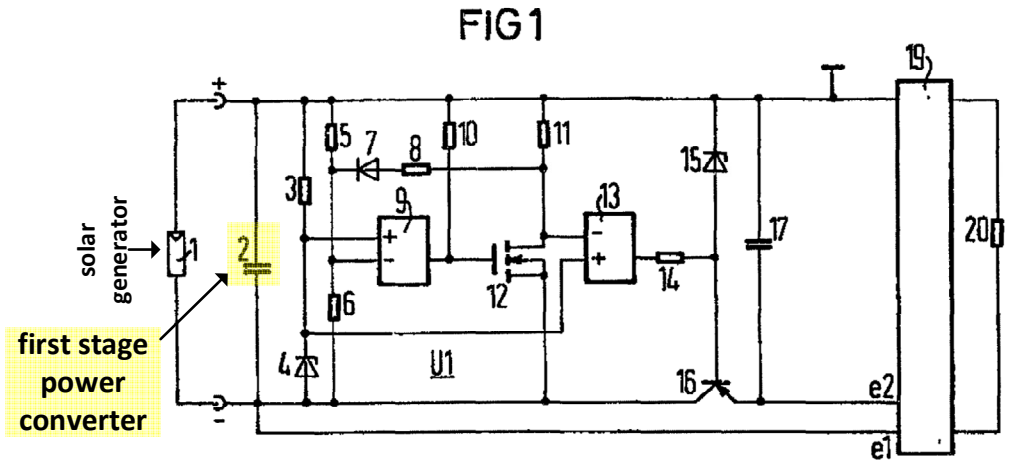


Fig. 31

191) Thus, Mieth teaches [19B]. Additionally, the combination of Mieth and Balogh disclose the first stage power converter of [19B] as discussed in further detail in ¶¶194-197.

iii. [19C]: "having: an input connected to a first voltage from a photovoltaic panel"

192) Mieth discloses a solar generator 1 which a PHOSITA would understand includes the claimed ***photovoltaic panel***. Mieth further discloses that the solar generator 1 provides an output voltage which is analogous to the claimed ***a first voltage from a photovoltaic panel***. Ex.1002,4:37-5:7. Furthermore, as seen in Fig. 32, the capacitor 2 is connected to the solar generator 1 and thus ***an input*** of the capacitor 1 (*i.e.,* first stage power converter) is connected to the output voltage (*i.e.,* first

voltage) of the solar generator 1.

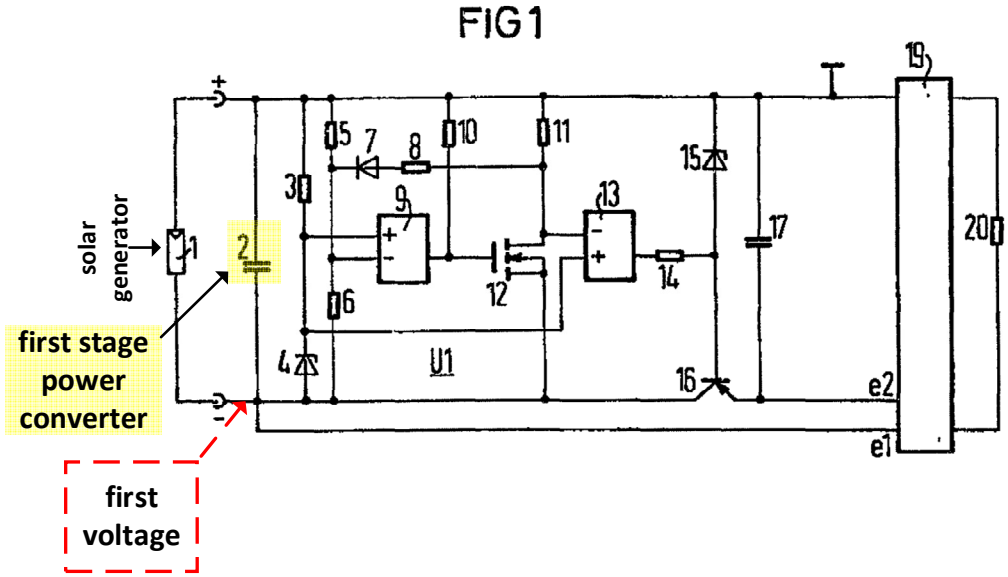


Fig. 32

193) Thus, Mieth teaches [19C]. Additionally, the combination of Mieth and Balogh disclose the features of [19C] as discussed in further detail in ¶¶194-197.

iv. [19D]: "an output providing a second voltage different from the first voltage from the photovoltaic panel"

194) Mieth does not disclose that the capacitor 2 (first stage power converter) outputs a second voltage that differs from the first voltage. However, Balogh discloses cascaded converter arrangements as illustrated below in Fig. 33 (Ex. 1003), where

converter 1 is analogous to the claimed first stage power converter. Ex.1003,2:54-64.

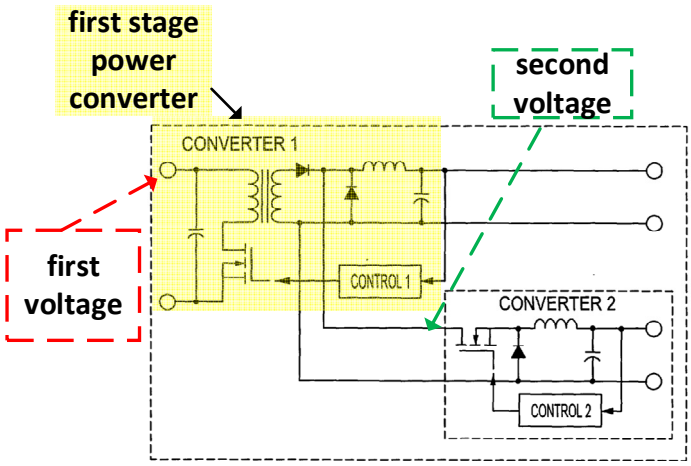


FIG. 1D
PRIOR ART

Fig. 33

195) Converter 1 of Balogh is a DC/DC converter that converts a first voltage at the input of converter 1 to a second voltage at the output of converter 1 that is different than the first voltage, which is analogous to the claimed ***an output providing a second voltage different from the first voltage from the photovoltaic panel***. As Balogh states (Ex.1003,1:29-36) a buck converter is characterized where the "output voltage is lower than the input voltage" thus the output voltage is different from the input voltage. Specifically, the first voltage input to converter 1 passes through the transformer of converter 1 which can step down the voltage to the second voltage seen at the output of converter 1.

196) A PHOSITA is motivated to combine the cascaded power converter architecture of Balogh with Mieth as described in accordance with claim 1 in ¶¶173-185. That is, Balogh discloses converter 1 which is a first stage power converter that can replace the capacitor 2 of Mieth and configure two cascaded power converters with the switchable load features of Mieth for DC applications with high input voltages for solar generator applications.

197) Thus, Mieth-Balogh teach [19D].

v. [19E]: "a second stage power converter connected to the output of the first stage power converter,"

198) [19E] is analogous to the features of [1C] that recite, "a second stage power converter connected to the first stage power converter." [19E] differs in reciting that the second stage power converter is connected to the ***output*** of the first stage power converter. Mieth, as seen below in Fig. 34, discloses that the power supply apparatus 19 (analogous to the second stage power converter, or see also converter 2 of Balogh's Fig. 1D) is connected at the output of capacitor 2 (analogous to the first stage power converter, or see also converter 1 of Balogh's Fig. 1D).

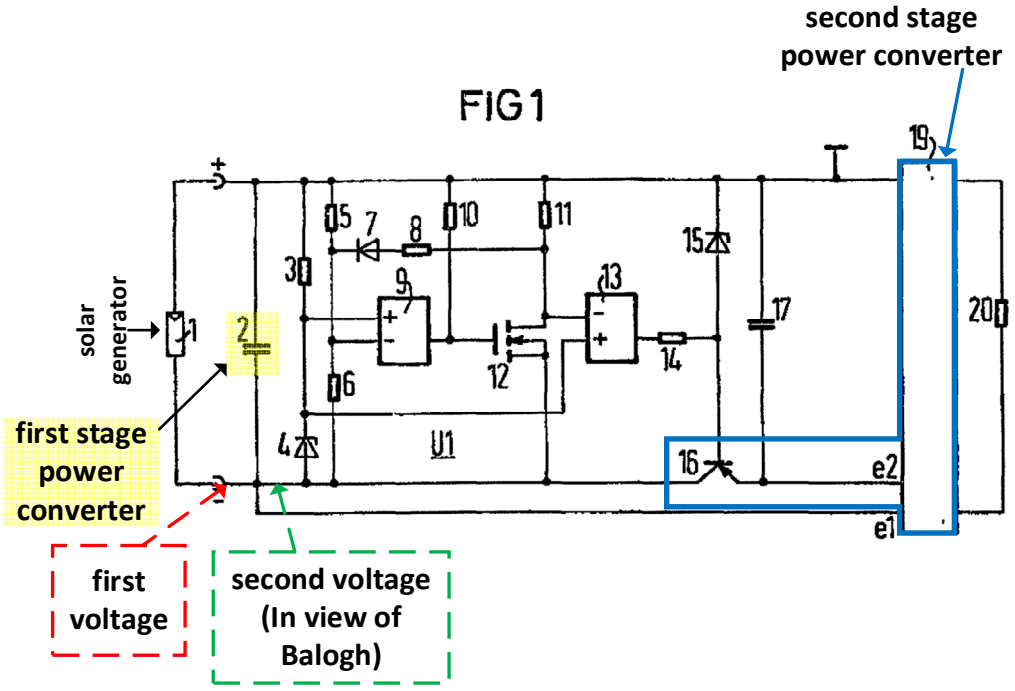


Fig. 34

199) Thus Mieth discloses [19E] for at least the same reasons Mieth discloses [1C] as described in ¶¶99-101.

vi. [19F]: "the second stage power converter supplying power at a third voltage to a micro-controller of the photovoltaic panel; and"

200) Mieth discloses that the power supply apparatus 19 connected to the bipolar transistor 16 (blue-second stage power converter) generates an output voltage to a load 20. Ex.1002,11:14-16,12:21-30. As shown in Fig. 35, the output of the power supply apparatus 19 is analogous to the claimed ***supplying power at a third voltage***. Ex.1002,8:29-35. The load 20 of Mieth receives the output of the power supply apparatus 19. *Id.* A PHOSITA would understand that a load in a circuit can

be or include a micro-controller, as such, the load 20 is analogous to the claimed ***micro-controller*** (dashed-orange).

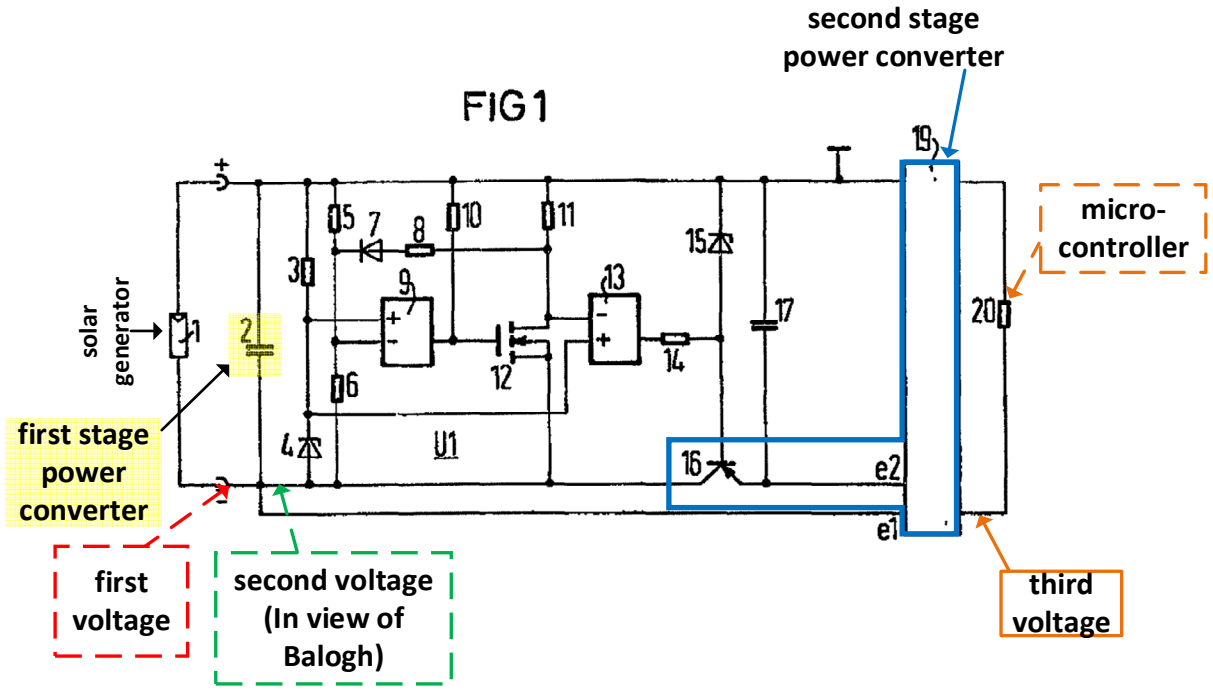


Fig. 35

201) A PHOSITA would understand that the micro-controller can reside with or be connected to circuitry associated with the solar generator 1 of Mieth which includes the claimed photovoltaic panel, which is analogous to the claimed ***a micro-controller of the photovoltaic panel.***

202) Thus Mieth discloses [19F].

vii. [19G]: "a control circuit coupled to the first stage power convert and the second stage power converter and powered by the output of the first stage power converter"

203) [19G] is analogous to [1F], and thus Mieth discloses [19G] for at least the same reasons Mieth discloses [1F] as described in ¶¶108-113.

viii. [19H]: "wherein after the first stage power converter is turned on, the control circuit instructs the second stage power converter to: not supply the power at the third voltage to the micro-controller before a determination that the output of the first stage power converter has been stable for a predetermined period of time; and"

204) Mieth-Balogh disclose a first stage power converter, either the capacitor 2 of Mieth or converter 1 of Balogh (*e.g.*, as discussed in ¶187. The first stage power converter of Mieth or Balogh are ***turned on*** when connected to and receiving the first voltage from the solar generator 1 as seen in Fig. 36. A PHOSITA would understand the claimed "turned on" condition can be met when the solar generator 1 is generating DC power that powers the first stage power converter. As such, Mieth-Balogh disclose the claimed ***wherein after the first stage power converter is turned on***.

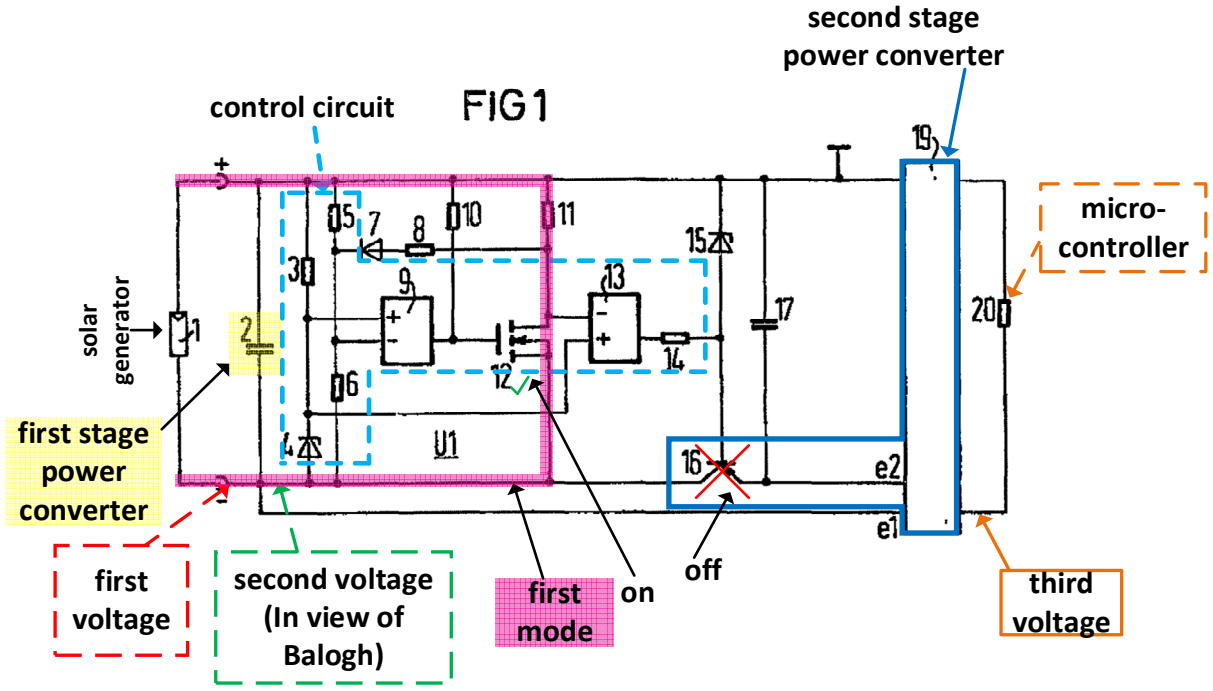


Fig. 36

205) Mieth discloses a switchable load between the first stage and second stage power converter that is connected to the first stage power converter when the output of the first stage power converter does not meet a stable criteria according to a voltage threshold Ex.1002,5:22-38. As the input voltage magnitude is ramping (in Mieth, going negative with respect to positive terminal of the solar generator), initially (before current begins to flow in zener diode 4) the voltage at the positive input of the comparator is greater than the voltage at the negative input thus causing the output of comparator 9 to go high, turning on transistor 12 and thus turning on the switchable load. During this period where the voltage magnitude is ramping (and below the voltage threshold established by regulator circuit 3,4 and

the voltage divider 5,6) and transistor 12 is on, comparator 13 output is high, turning off transistor 16. Thus, during this period (before the threshold is reached) the circuitry instructs transistor 16 to not supply power to the micro-controller. As such, when the first stage powers on, the circuit of Mieth is configured for the first mode as described in [1G]. Details regarding the voltage threshold of Mieth are discussed in accordance with ¶¶108-119 above. As described above, the power supply apparatus 19 of Mieth does not supply power to the load 20 when the first stage power converter is turned on, which is analogous to the claimed ***not supply the power at the third voltage to the micro-controller***.

206) Mieth discloses hysteresis by the circuit configuration of the first comparator 9, to mitigate instability in switching signals as discussed in ¶¶149-157. The operation of hysteresis within Mieth is analogous to the claimed ***a determination that the output . . . has been stable***. Neither the claim language nor the '848 specification provide a clear definition of "stable" or "stability" which is necessary to understand the meaning of claim feature [19H]. The IEEE dictionary defines "stability" as such: "Stability: An aspect of system behavior associated with systems having the general property that the bounded input perturbations result in bounded output perturbations." Ex. 1004, page 1029. In the context of the '848 specification, these "perturbations" per the IEEE dictionary are analogous to the oscillations referred to in Ex. 1002, 9:67-10:1: "…positive hysteresis is introduced

in order to prevent oscillations." The '848 specification gives further clarification starting at Ex. 1001, 8:67-9:1: "The reason this hysteresis modification is used is that at very low light conditions (where the sunlight is very dim for instance), solar panels can provide voltages that are high enough for turning on, but cannot ultimately provide sufficient power for the circuit that is to be powered by the buck converter (**402**). Therefore, identifying a simple threshold for voltage Vbuck**1** does not stop unsuccessful turn-on attempts, if no hysteresis is employed in delay circuit (**403**)" A PHOSITA would understand this to mean that small variations at Vbuck1 would cause large variations at the output of Vbuck2 because it would be turning on and off—oscillating. As per the IEEE definition, the output of Vbuck1 is bounded by small perturbations while the output of Vbuck2 goes rail to rail—essentially unbounded. The solution to these oscillations is to provide hysteresis to the signal path. The specification goes on to say "One way to prevent such attempts is to permit the system of circuit (**400**) to turn on only when it can stay on with the available given power. Power is measured by measuring the voltage on resistor P**1** (**405**) (plus any losses from the switch (**404**)) as represented by Vbuck**1**. In one embodiment, the delay circuit (**403**) can be omitted from the circuit (**400**), since this approach can also work with zero delay because of positive hysteresis." Ex. 1001, 9:14-9:21.

207) Seemingly, the '848 specification teaches that stability is maintained by virtue of the hysteresis—not the delay. It is incidental that the hysteresis function is provided in the delay block because, the '848 specification states that the approach works with zero delay.

208) Nothing in the '848 specification describes a circuit that measures stability—nothing that determines that stability has been achieved is disclosed by the '848 specification. Only a circuit that ENABLES stability is described and that is the hysteresis circuit. According to the '848 specification, to achieve stability, a hysteresis circuit is required. Given this, I interpret the claim language: "*a determination that the output of the first stage power converter has been* ***stable for a predetermined period of time*****"** to simply mean that the output of the first stage power converter has reached the upper threshold of the hysteresis of the comparator, instructing the second stage power converter to turn on after a predetermined delay. Mieth achieves this with his hysteresis comparator followed by the propagation delays of the signal path.

209) Furthermore, as shown in Fig. 36 above, the feedback from the output of the first comparator 9 back to the input of first comparator 9 through resistor 8 and diode 7, and the time it takes the first comparator 9 to compare its inputs define a period of time that is analogous to the claimed ***stable for a predetermined period of time***.

That is, the predetermined period of time in Mieth is intrinsic to delays of the circuit elements associated with hysteresis for the first comparator 9.

210) In addition, while not required by the claim language nor described as necessary in the detailed description of the '848 Patent, if it is contended that the feature ***stable for a predetermined period of time*** should be defined by specific delay circuitry rather than the intrinsic switching and delay characteristics of comparator 9 and associated circuitry, a PHOSITA would have known to interpose one or more buffer circuits or delay elements to affect a predetermined period of time. Such would be customary practices in the art at the time of filing.

211) Thus Mieth discloses [19H].

ix. [19I]: "supply the power at the third voltage to the micro-controller after the determination that the output of the first stage power converter has been stable for the predetermined period of time"

212) Mieth discloses a second mode that is analogous to feature [19I] as discussed in accordance with [1H]. ¶¶120-124. As shown in Fig. 37 below, in the second mode, the second stage power supply provides power at the third voltage to the load 20 (*i.e.,* micro-controller).

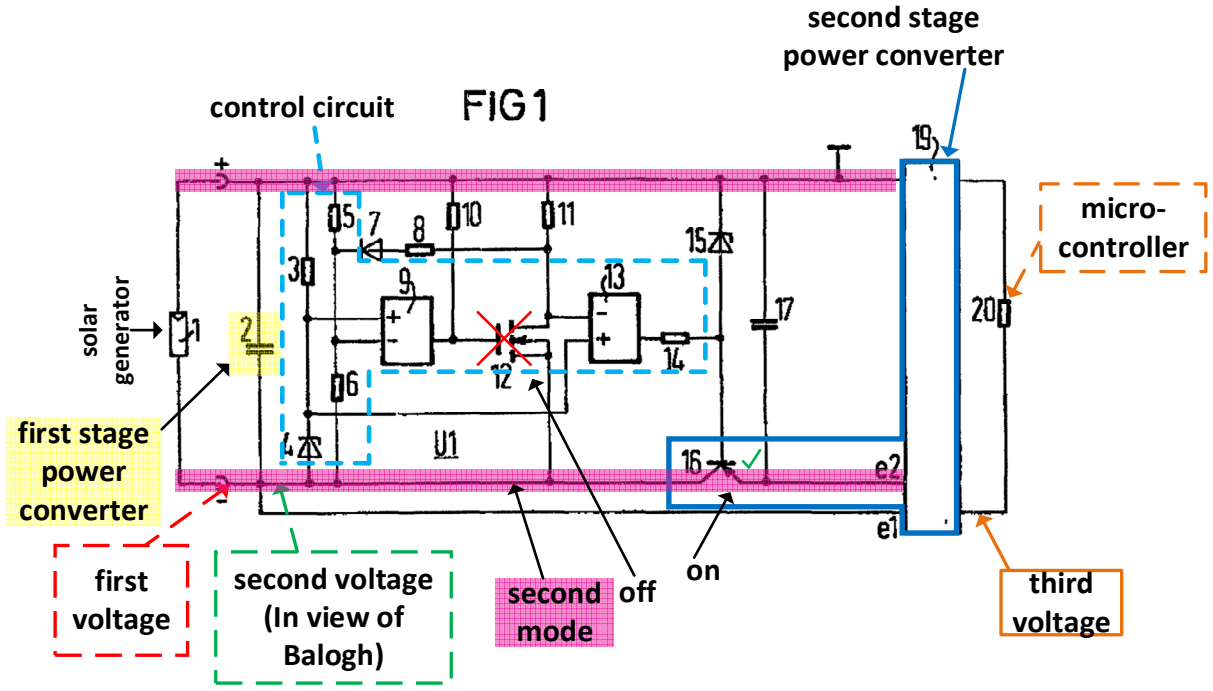


Fig. 37

213) As described in ¶¶120-124, in the second mode, the bipolar transistor 16 is "on" causing the output of the power supply apparatus 19 to power the load 20, which is analogous to the claimed ***supply the power at the third voltage to the micro-controller.***

214) As discussed in ¶¶204-211, the output of Mieth's first stage power converter (either capacitor 2 or in view of Balogh's converter 1) is determined to be stable by the hysteresis of comparator 9 for a predetermined period of time when the representative voltage at the first comparator 9 meet or exceed the predefined minimum value.

215) Thus Mieth discloses [19I], and Mieth-Balogh disclose every feature of claim 19.

4. Dependent Claim 20

216) Claim 19 is taught Mieth and Balogh. *Supra,* ¶¶188-215. Claim 20 depends from claim 19 and requires, "wherein the first stage power converter is a first step-down converter, and the second stage power converter is a second step-down converter." Ex.1001, claim 20. As discussed in *Supra,* ¶¶173-185, a PHOSITA would have been motivated to combine the cascaded power converter architecture of Balogh with the switchable load features of Mieth. As discussed in *Supra* ¶¶190-199., and Fig. 34 above, Mieth-Balogh disclose a capacitor 2 (highlighted-yellow) which is analogous to the claimed ***first stage power converter*** and disclose power supply apparatus 19 connected to the bipolar transistor 16 (blue) which is analogous to the claimed ***second stage power converter***. The power supply apparatus 19 is a DC-DC voltage converter or charging converter which a PHOSITA would understand can step-down DC power and is analogous to the claimed ***second stage power converter is a second step-down converter***. Ex.1002,8:29-35. Balogh teaches a first stage power converter and a second stage power converter that can each comprise step-down converters as seen in Fig. 33 above. Ex.1003,1:29-36. Balogh teaches that a cascaded arrangement can include a first buck converter and a second buck converter where a buck converter steps an input voltage down to an output voltage that is lower than the input voltage. *Id.* It would be obvious to a PHOSITA to modify the capacitor 2 of Mieth with the step-down converter from

Balogh to realize the claimed ***first stage power converter is a first step-down converter***. Thus, Mieth-Balogh disclose claim 20.

C. Ground C: Obviousness of claims 2, 3, 6, 11, 12, and 15 in view of Mieth and Liu, or over Mieth-Balogh, and further in view of Liu

1. Dependent Claim 2

217) Claim 1 is taught by Mieth. *Supra*, ¶¶95-124. Claim 2 depends from claim 1 and requires, "wherein the power absorption circuit includes a capacitor coupled to the first output." Ex.1001, claim 2.

218) Mieth discloses transistor 12 connected to preliminary load 11 to form the claimed ***power absorption circuit coupled to the first output*** as discussed in ¶¶114-119. Additionally, Liu (Ex.1005) discloses a capacitor as a power absorption circuit coupled to the first output, and a PHOSITA is motivated to combine Mieth and Liu for the following reasons.

219) As shown in Fig. 38 below, Liu discloses cascaded DC voltage converters with an input stage 50 separated from an output stage 60 by a reservoir capacitor 58. Ex.1005,4:25-35.

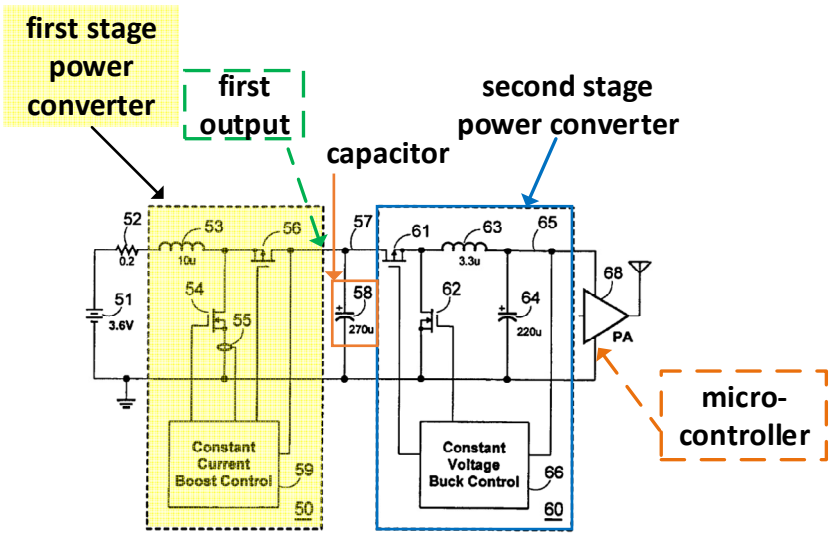


Fig. 38

220) Input stage 50 up-converts the voltage from battery 51 to charge reservoir capacitor 58, and output stage 60 down converts the voltage of reservoir capacitor 58 to power a power amplifier ("PA") 68. Ex.1005,4:36-43. Since input stage 50 (highlighted-yellow) converts an input voltage to an output voltage, input stage 50 is analogous to the claimed first stage power converter of claim 1, and the output (dashed-green) of input stage 50 is analogous to the claimed ***first output*** of claim 2. Since reservoir capacitor 58 (orange) is charged from the first output of input stage 50, reservoir capacitor 58 absorbs the first output of input stage 50 and is analogous to the claimed ***power absorption circuit includes a capacitor coupled to the first output***. Thus, Mieth-Liu or Mieth-Balogh-Liu teach claim 2.

221) The combination of Mieth-Liu involves combining known prior-art elements (combining Mieth's resistive load between converters with Liu's capacitive load between converters) according to known methods to yield predictable results, a cascaded power converter having a capacitive load at the second power converter input. A PHOSITA has the skills, knowledge, and motivation to carry out the combination. A PHOSITA would reasonably expect success in combining Mieth and Liu, and there is no undue technical hurdles in combining Mieth with Liu, as the combination is a simple modification to Mieth's system. *Id*.

2. Dependent Claim 3

222) Claim 2 is taught by Mieth-Liu. *Supra*, ¶¶217-221. Claim 3 depends from claim 2 and requires, "wherein the voltage above the threshold allows the capacitor to power the second stage to operate the micro-controller for at least a predetermined period of time in absence of power input from the first stage during the predetermined period of time." Ex.1001, claim 3. Neither claims 3, 2, or 1 provide antecedence for "first stage" or "second stage" and thus the terms are indefinite. For purposes of analysis, "first stage" and "second stage" are interpreted to mean "first stage power converter" and "second stage power converter," respectively.

223) The claimed ***voltage above the threshold*** is analogous to feature [1H] discussed in ¶¶120-124, and thus is disclosed by Mieth.

224) Liu (Fig. 38 above) teaches that reservoir capacitor 58 provides most of the energy to PA 68 through output stage 60 for a period of time when battery 51 cannot supply power to the PA 68. Ex.1005,1:8-12,4:43-51. A PHOSITA understands that capacitor 58 provides power to the PA 68 for a predetermined period of time by sizing the capacitor appropriately. Furthermore, while Liu shows PA 68 powered by reservoir capacitor 58 through output stage 60, a PHOSITA understands that reservoir capacitor 58 and output stage 60 could power another load such as the claimed ***micro-controller*** through a second stage power converter. Thus, capacitor 58 that can provide power to the PA 68 for a period of time is analogous to the claimed ***capacitor to power the second stage to operate the micro-controller for at least a predetermined period of time in absence of power input from the first stage during the predetermined period of time***.

225) Liu discloses cascaded power converters with a capacitor that provides power to a load through a second power converter for a period of time without incoming power from a first power converter. Ex.1005,4:36-43. Mieth teaches use of a power absorption circuit when an input voltage to a power converter varies, such as the voltage from a photovoltaic system that varies depending upon time of day, or weather conditions. Mieth disconnects the switchable load between first stage and second stage power converters when the input voltage to the first stage power converter meets a stable criteria according to a voltage threshold. *Id.* A PHOSITA

is motivated to combine the two-stage converter and capacitor of Liu with the power absorption circuit of Mieth, as the capacitor provides a more stable power source to Mieth's load for a predetermined time period when the power absorption circuit is disconnected from the circuit or voltage from the photovoltaic system is varying due to dynamic conditions. *Id.* Additionally or alternatively, a PHOSITA would be motivated to combine the two-stage converter of Balogh with the capacitor of Liu and power absorption circuit of Mieth.

226) A PHOSITA is motivated to employ known means in the art, as taught in Liu, to modify the circuit of Mieth (e.g., Fig. 22 above) such that when the representative voltage connected to comparator 9 is below the predefined minimum value according to the first output, the capacitor of Liu powers load 20 (*i.e.,* micro-controller) through power supply apparatus 19 (*i.e.,* the second stage power converter) for a predetermined period of time, ***which is analogous to claim 3***. Therefore, both Mieth and Liu, or Mieth, Balogh, and Liu, provide an express motivation to combine together to improve a cascaded power converter system by including a capacitor in the power absorption circuit. *Id.*

227) Thus, Mieth-Liu or Mieth-Balogh-Liu disclose claim 3.

3. Dependent Claim 6

228) Claim 5 is taught by Mieth alone, or by a combination of Mieth-Balogh. *Supra*, ¶¶128-134. Claim 6 depends from claim 5 and requires, "wherein, when the

switchable load is in the second state, the voltage above the threshold is sufficient to power the second state to operate the micro-controller for at least a predetermined period of time during which the direct current input to the first stage power converter has diminishing power." Ex.1001, claim 6. It is unclear what the claim means by reciting ***power the second state to operate the micro-controller***, as the second state described by claims 5-6 is related to the claimed switchable load and not the micro-controller. In fact, in the second state, the switchable load does not consume the first output and is conceivably disconnected from the first output. Thus claim 6 is indefinite. For purposes of analysis the feature is interpreted as *powering the second stage* rather than *powering the second state*, to operate the micro-controller.

229) Fig. 39 below illustrates Mieth in the second mode. As taught by Mieth, when voltages from the solar generator 1 (as represented at the negative input terminal of first comparator 9) are above a predefined minimum value (as represented at the positive input terminal of first comparator 9)(*i.e.,* relatively "high" first output voltages), the control circuit transitions the circuit to the second mode, wherein the auxiliary voltage input e2 of the power supply apparatus 19 is connected to the first output of the solar generator 1. Ex.1002,9:23-26. As shown in Fig. 39 below, when the predefined minimum value is satisfied (*i.e.,* the voltage associated with the first output exceeds the claimed threshold), the circuit of Mieth operates in the

second mode (highlighted-pink) where the field-effect transistor 12 is "off" or non-conducting, thereby disconnecting the preliminary load 11 from the first output. *Id.*

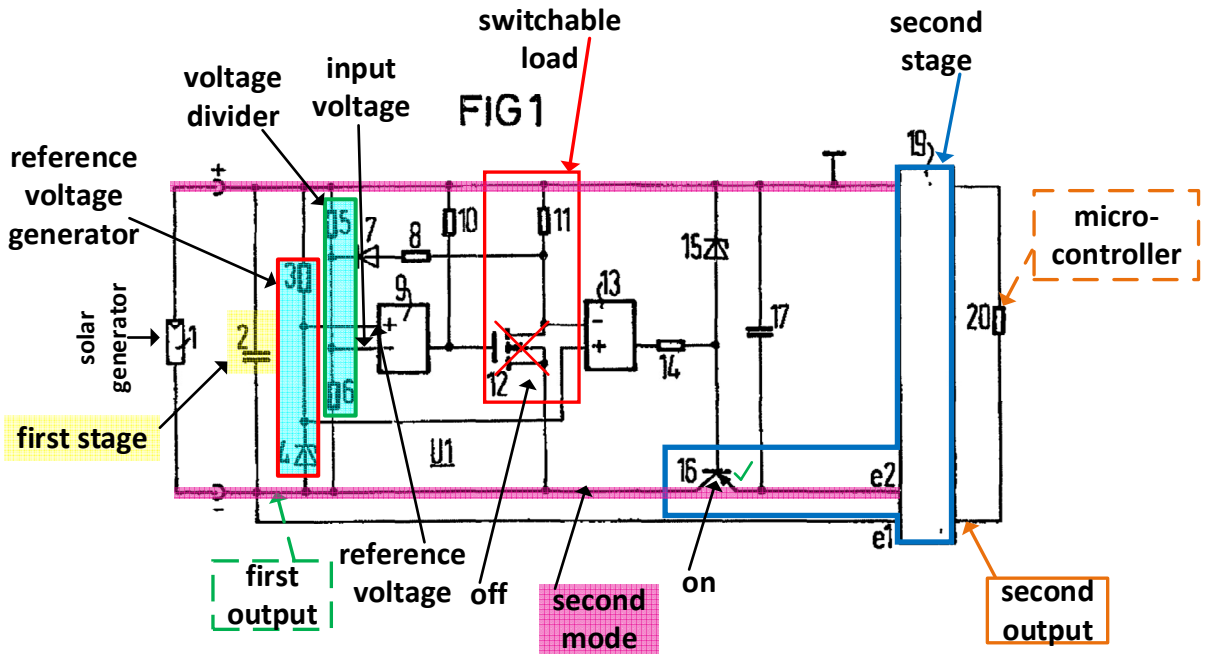


Fig. 39

230) As discussed in ¶¶99-101, the first comparator 9 compares the reference voltage from the reference voltage generator (highlighted-teal-outlined-red) to the representative voltage from the voltage divider (highlighted-teal-outlined-green) to determine if the representative voltage exceeds a threshold defined by the reference voltage. Thus, according to Mieth, *the design of the reference voltage generator dictates the magnitude of the threshold that triggers the exit from the first state and entry into the second state.* Ex.1002,12:12-26.

231) As shown above, upon the control circuit of Mieth causing the circuitry to exit the first mode and enter the second mode, the first output is large enough that the threshold defined by the reference voltage generator is exceeded, and the first output is passed to the e2 terminal of the second stage power converter 19.

232) More particularly, when the voltage representative of the first output exceeds the threshold, the transistor 12 is shut "off," pulling its output node (connected to the negative input terminal of the second comparator 13) high due to resistor 11. This causes the output of the second comparator 13 to go low, thus turning bipolar transistor 16 "on," and passing the first output to the e2 terminal to power the second stage power converter 19, which, in turns provides the second output to the load 20.

233) Claim 6 requires that when the direct current input to the first stage power converter has diminishing power, the threshold is sufficient for the second stage power converter to operate the micro-controller for at least a predetermined period of time. Ex.1001, claim 6. The '848 patent does not define or provide any context for what constitutes the predetermined period of time for the claim feature. In the second state (or second mode), when the direct current input to the first stage power converter has diminishing power, the first output will begin to decrease. As the second stage power converter has a range of input voltages at which it may operate effectively to provide the second output to the load 20 (micro-controller),

Mieth's control circuit is operable to allow the second stage power converter 19 to operate the load for a predetermined period of time despite a decreasing first output voltage, as no minimum time period is set forth by the claim, nor provided as an example in the detailed description of the '848 patent. Thus, Mieth discloses this feature.

234) If Mieth standing alone is not deemed to provide adequate support for the feature of claim 6, Liu discloses use of a reservoir capacitor 58 between first and second stage power converters, so that if the first stage power converter is inoperable or otherwise deficient (*e.g.,* diminishing power), the capacitor provides auxiliary power to the second stage power converter to power the micro-controller for the predetermined period of time.

235) Mieth discloses transistor 12 connected to preliminary load/resistor 11 to form a power absorption circuit coupled to the first output, as, during the first mode, power from the first output is at least partially consumed by the preliminary load/resistor 11. Ex.1002,9:34-10:3,11:4-12,12:12-26. Mieth does not disclose that preliminary load/resistor 11 includes a capacitor. However, Liu discloses a capacitor as a power absorption circuit coupled to the first output and feeding a second stage power converter, and a PHOSITA is motivated to combine Mieth and Liu for at least the following reasons.

236) As shown in Fig. 40, Liu discloses cascaded DC voltage converters with an input stage (or first stage power converter) 50 separated from an output stage (or a second stage power converter) 60 by a reservoir capacitor 58. Ex.1005,4:25-35.

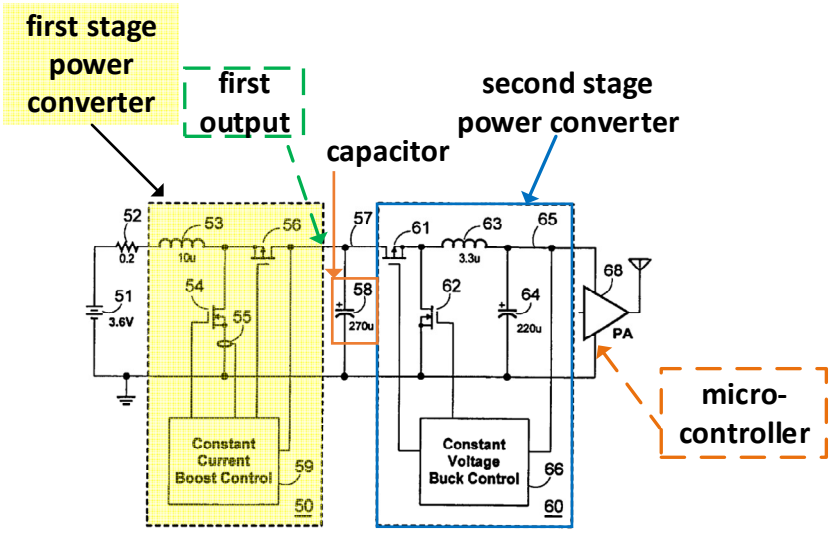


Fig. 40

237) The first stage power converter 50 converts the voltage from battery 51 to charge reservoir capacitor 58, and second stage power converter 60 down converts the voltage of reservoir capacitor 58 to power a power amplifier ("PA") 68. Ex.1005,4:36-43. Since first stage power converter 50 (highlighted-yellow) converts an input voltage to an output voltage, input stage 50 is analogous to the claimed first stage power converter of claim 1, and the output (dashed-green) of first stage power converter 50 is analogous to the claimed ***first output*** of claim 3. Since the reservoir capacitor 58 (orange) is charged from the first output of the first stage power converter 50, reservoir capacitor 58 absorbs the first output of the first

stage power converter 50, and as the capacitor 58 charges, in combination with Mieth, the voltage at the voltage divider eventually exceeds the "predefined condition" which causes the control circuit of Mieth to transition from the first state (lower first output voltages) to the second state (higher first output voltages).

238) Liu teaches that reservoir capacitor 58 provides most of the energy to PA 68 through output stage 60 for a period of time when battery 51 cannot supply power to the PA 68. Ex.1005,1:8-12,4:43-51. A PHOSITA understands that capacitor 58 provides power to the PA 68 for a predetermined period of time by sizing the capacitor appropriately. Furthermore, while Liu shows PA 68 powered by reservoir capacitor 58 through the second stage power converter 60, a PHOSITA understands that reservoir capacitor 58 and output stage 60 could power another load (as opposed to the PA 68) such as the claimed ***micro-controller***. *Id*. Thus, capacitor 58 that can provide power to the PA 68 for a period of time is analogous to the claimed ***voltage above the threshold is sufficient to power the second state to operate the micro-controller for at least a predetermined period of time during which the direct current input to the first stage power converter has diminishing power.***

239) Liu discloses cascaded power converters with a capacitor that provides power to a load through a second power converter for a period of time without incoming power from a first power converter. Ex.1005,4:36-43. Mieth teaches use of a

power absorption circuit when an input voltage to a power converter varies, such as the voltage from a photovoltaic system that varies depending upon time of day, or weather conditions. Ex.1002,5:22-38. Mieth in view of Balogh disconnects the switchable load between first stage and second stage power converters when the input voltage to the first stage power converter meets a stable criteria according to a voltage threshold. *Id.* A PHOSITA is motivated to combine the capacitor of Liu with the power absorption circuit (*i.e.,* the switchable load 11/12) of Mieth, as the capacitor provides a more stable power source to Mieth's load (*i.e.,* the micro-controller) for a predetermined time period when the power absorption circuit is disconnected from the circuit or voltage from the photovoltaic system is varying due to dynamic conditions. *Id.*

240) A PHOSITA is motivated to employ known means in the art, as taught in Liu, to modify the circuit of Mieth (e.g., Fig. 39) such that when Mieth is in the second state and the monitored voltage connected to first comparator 9 falls below the predefined minimum value (*i.e.,* the "predefined threshold") according to the first output, the capacitor of Liu powers load 20 (*i.e.,* micro-controller) through power supply apparatus 19 (*i.e.,* the second stage power converter) for a predetermined period of time, ***which is analogous to claim 6***. Therefore, both Mieth and Liu provide an express motivation to combine together to improve a cascaded power converter system by including a capacitor in the power absorption circuit. *Id.*

241) If it is argued that Mieth does not teach a first stage power converter, Mieth may be combined with Balogh to provide such feature, as set forth in ¶¶173-184. Further, Liu may be combined with a combination of Mieth-Balogh for at least the reasons above in ¶¶217-221.

242) Thus, Mieth-Liu, or alternatively Mieth-Balogh-Liu disclose claim 3.

4. Dependent Claim 11

243) Claim 10 is taught by Mieth alone, or by a combination of Mieth-Balogh. *Supra*, ¶¶158-187. Claim 11 depends from claim 10 and requires, "further comprising: providing, in the power absorption circuit, a capacitor coupled to the first output" Ex.1001, claim 11. Claim 11 is analogous to claim 2, and thus Mieth-Liu or Mieth-Balogh-Liu discloses claim 11 for at least the same reasons Mieth-Liu or Mieth-Balogh-Liu discloses claim 2 as described in ¶¶217-221.

5. Dependent Claim 12

244) Claim 11 is taught by Mieth-Liu or Mieth-Balogh-Liu. *Supra*, ¶243. Claim 12 depends from claim 11 and requires, "wherein the voltage above the threshold allows the capacitor to power the second stage to operate the micro-controller for at least a predetermined period of time in absence of power input from the first stage during the predetermined period of time." Ex.1001, claim 12. Claim 12 is analogous to claim 3, and thus Mieth-Liu or Mieth-Balogh-Liu discloses claim 12

for at least the same reasons Mieth-Liu or Mieth-Balogh-Liu discloses claim 3 as described in ¶¶222-227.

6. Dependent Claim 15

245) Claim 14 is taught by Mieth alone, or by a combination of Mieth-Balogh. Supra, ¶¶168-187. Claim 15 depends from claim 14 and requires, "wherein, when the switchable load is in the second state, the voltage above the threshold is sufficient to power the second state to operate the micro-controller for at least a predetermined period of time during which the direct current input to the first stage power converter has diminishing power." Ex.1001, claim 15. Claim 15 is analogous to claim 6, and thus Mieth-Liu or Mieth-Balogh-Liu discloses claim 15 for at least the same reasons Mieth-Liu or Mieth-Balogh-Liu discloses claim 6 as described in ¶¶228-242.

VIII. CONCLUDING STATEMENT

Under penalty of perjury, all statements made herein of my own knowledge are true, and I believe that all statements made herein on information and belief to be true. I have been warned and I am aware that willful false statements are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code. In signing this Declaration, I understand that the Declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may

be subject to cross-examination in the case and that cross-examination will take place in the United States. If cross examination is required of me, I undertake to appear within the United States during the time allotted for cross-examination, and within the limits of my ability so to do. I declare under penalty of perjury that the foregoing is true and correct.

Executed on July 11, 2023.



Douglas Holberg

IX. CLAIM LISTING APPENDIX

U.S. Patent No. 9,966,848 - Avrutsky	
Claim Element Designation	**Claim Element**
Claim 1	
[1A]	An apparatus, comprising:
[1B]	a first stage power converter to generate a first output from a direct current input;
[1C]	a second stage power converter connected to the first stage power converter to convert the first output to a second output;
[1D]	a micro-controller;
[1E]	a power absorption circuit; and
[1F]	a control circuit coupled with the first stage power converter and the second stage power converter, the control circuit powered by the first output to control the second stage power converter,
[1G]	wherein; when the second stage power converter is in a first mode of not providing the second output to power the micro-controller, the control circuit monitors a voltage of the first output powering the power absorption circuit and signals the second stage power converter to remain in the first mode during a time period in which the voltage is below a threshold; and
[1H]	when the voltage is above the threshold, the control circuit signals the second stage power converter to enter a second mode of providing the second output to power the micro-controller
Claim 2: The apparatus of claim 1, wherein the power absorption circuit comprises a capacitor coupled to the first output.	
Claim 3: The apparatus of claim 2, wherein the voltage above the threshold allows the capacitor to power the second stage to operate the micro-controller for at least a predetermined period of time in absence of power input from the first stage during the predetermined period of time.	
Claim 4: The apparatus of claim 1, wherein the power absorption circuit comprises a switchable load.	
Claim 5	
[5A]	The apparatus of claim 4, wherein the control circuit signals the switchable load to be in a first state to consume the first output when the second stage power converter is in the first mode

[5B]	and to be in a second state not to consume the first output when the voltage is above the threshold.
Claim 6: The method of claim 5, wherein, when the switchable load is in the second state, the voltage above the threshold is sufficient to power the second state to operate the micro-controller for at least a predetermined period of time during which the direct current input to the first stage power converter has diminishing power.	
Claim 7	
[7A]	The apparatus of claim 5, wherein the switchable load comprises: a resistive device; and
[7B]	a switching device connected to the resistive device
[7C]	wherein the switching device is turned on in the first state to connect the resistive device to the first output and turned off in the second state to disconnect the resistive device from the first output.
Clam 8: The apparatus of claim 5, wherein the control circuit delays a first signal instructing the switching device to change from the first state to the second state to generate a second delayed signal that instructs the second stage to change from the first mode to the second mode.	
Claim 9:	
[9A]	The apparatus of claim 8, wherein the control circuit comprises: a hysteresis amplifier coupled to the first output to generate the first signal; and
[9B]	a delay circuit coupled to the first signal to generate the second delayed signal.
Claim 10	
[10A]	A method to supply power, the method comprising:
[10B]	providing a first stage power converter to generate a first output from a direct current input,
[10C]	wherein the first stage power converter is coupled to a power absorption circuit;
[10D]	providing a second stage power converter connected to the first stage power converter to convert the first output to a second output,
[10E]	wherein the second stage power converter is coupled to a micro-controller;
[10F]	powering, by the first output, a control circuit that is coupled with the first stage power converter and the second stage power converter; and

[10G]	controlling, by the control circuit powered by the first output, the second stage power converter, by: when the second stage power converter is in a first mode of not providing the second output to power the micro-controller, monitoring a voltage of the first output powering the power absorption circuit and signaling the second stage power converter to remain in the first mode during a time period in which the voltage is below a threshold; and
[10H]	when the voltage is above the threshold, signaling the second stage power converter to enter a second mode of providing the second output to power the micro-controller.
Claim 11: The method of claim 10, further comprising: providing, in the power absorption circuit, a capacitor coupled to the first output.	
Claim 12: The method of claim 11, wherein the voltage above the threshold allows the capacitor to power the second stage to operate the micro-controller for at least a predetermined period of time in absence of power input from the first stage during the predetermined period of time.	
Claim 13: The method of claim 10, further comprising: providing, in the power absorption circuit, a switchable load.	
Claim 14: The method of claim 13, wherein the control circuit signals the switchable load to be in a first state to consume the first output when the second stage power converter is in the first mode and to be in a second state not to consume the first output when the voltage is above the threshold.	
Claim 15: The method of claim 14, wherein, when the switchable load is in the second state, the voltage above the threshold is sufficient to power the second state to operate the micro-controller for at least a predetermined period of time during which the direct current input to the first stage power converter has diminishing power.	
Claim 16: The method of claim 14, further comprising: providing, in the switchable load: a resistive device; and a switching device connected to the resistive device, wherein the switching device is turned on in the first state to connect the resistive device to the first output and turned off in the second state to disconnect the resistive device from the first output.	
Claim 17: The method of claim 14, further comprising: delaying, by the control circuit, a first signal instructing the switching device to change from the first state to the second state to generate a second delayed signal that instructs the second stage to change from the first mode to the second mode.	
Claim 18: The method of claim 17, further comprising: providing, in the control circuit, a hysteresis amplifier coupled to the first output to generate the first	

signal; and providing a delay circuit coupled to the first signal to generate the second delayed signal.	
Claim 19	
[19A]	A power supply for use in a solar electric production system,
[19B]	the power supply comprising: a first stage power converter
[19C]	having: an input connected to a first voltage from a photovoltaic panel; and
[19D]	an output providing a second voltage different from the first voltage from the photovoltaic panel;
[19E]	a second stage power converter connected to the output of the first stage power converter,
[19F]	the second stage power converter supplying power at a third voltage to a micro-controller of the photovoltaic panel; and
[19G]	a control circuit coupled to the first stage power converter and the second stage power converter and powered by the output of the first stage power converter
[19H]	wherein after the first stage power converter is turned on, the control circuit instructs the second stage power converter to: not supply the power at the third voltage to the micro-controller before a determination that the output of the first stage power converter has been stable for a predetermined period of time; and
[19I]	supply the power at the third voltage to the micro-controller after the determination that the output of the first stage power converter has been stable for the predetermined period of time.
Claim 20: The power supply of claim 19, wherein the first stage power converter is a first step-down converter, and the second stage power converter is a second step-down converter.	