

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Hayato Nakanishi
U.S. Patent No.: 7,259,736 Attorney Docket No.: 54108-0002IP1
Issue Date: August 21, 2007
Appl. Serial No.: 10/712,381
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Title: ELECTRO-OPTICAL DEVICE, ACTIVE-MATRIX SUB-
STRATE, AND ELECTRONIC APPARATUS

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Patent Trial and Appeal Board
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**DECLARATION OF DAVID K. LIU IN SUPPORT OF PETITION FOR IN-
TER PARTES REVIEW OF UNITED STATES PATENT NO. 7,259,736
PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

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EXHIBITS

EX-1001	U.S. Patent No. 7,259,736 to Hayato Nakanishi (“the ’736 patent”)
EX-1002	Excerpts from the Prosecution History of the ’736 Patent (“the Prosecution History”)
EX-1003	Declaration of Dr. David K. Liu
EX-1004	U.S. Patent No. 5,831,699 (“Wright”)
EX-1005	Prosecution History of JP2002-348622 (“the Foreign Counterpart Prosecution History”)
EX-1006	Certified Translation of Pages 1-10, 50-58 from the Foreign Counterpart Prosecution History
EX-1007	Certified Translation of Pages 63-79 from the Foreign Counterpart Prosecution History
EX-1008	JPH11185654A to Yukio Masuda et al (“Masuda”)
EX-1009	Certified Translation of Masuda
EX-1010	JP2002-278504A to Mitsuo Inoue et al (“Inoue”)
EX-1011	Certified Translation of Inoue
EX-1012	KR960012168A to Yang-Ho Kwon (“Kwon”)
EX-1013	Certified Translation of Kwon
EX-1014	Sarma et al., “Flat Panel Displays for Portable Systems,” 13 <i>Journal of VLSI Signal Processing Systems</i> 165-190 (1996)

- EX-1015 Complaint, *Element Capital Commercial Company PTE. Ltd. v. BOE Technology Group Co., Ltd. et al.*, Case No. 2:22-cv-0118-JRG (E.D. Tex.)
- EX-1016 Docket Control Order, *Element Capital Commercial Company PTE. Ltd. v. BOE Technology Group Co., Ltd. et al.*, Case No. 2:22-cv-0118-JRG (E.D. Tex.)
- EX-1017 Plaintiff's Infringement Contentions, served on January 5, 2023 in *Element Capital Commercial Company PTE. Ltd. v. BOE Technology Group Co., Ltd. et al.*, Case No. 2:22-cv-0118-JRG (E.D. Tex.)
- EX-1018 2023-05-31 Email from Patent Owner to Petitioner
- EX-1019 2023-06-29 Email Thread Between Patent Owner and Petitioner Memorializing Agreement re Second IPR Petition
- EX-1020 U.S. Published App. No 2003/0090447 to Hajime Kimura ("Kimura")

I, David K. Liu, Ph.D., do hereby declare as follows:

I. ASSIGNMENT

1. I have been retained as a technical expert by counsel on behalf of BOE Technology Group Co., Ltd. and Beijing BOE Display Technology Co., Ltd. (“Petitioner”). I understand that Petitioner is requesting that the Patent Trial and Appeal Board institute an *inter partes* review (“IPR”) proceeding with respect to U.S. Patent No. 7,259,736 (“the ’736 patent”).

2. I have been asked to provide my independent analysis of the ’736 patent in light of certain prior art references.

3. I am not, and never have been, an employee of Petitioner. I received no compensation for this Declaration beyond my normal hourly compensation based on my time actually spent analyzing the ’736 patent, the prior art cited below, and issues related thereto, and I will not receive any added compensation based on the outcome of any IPR or other proceeding involving the ’736 patent.

4. My analysis here is based on my years of education, research and experience, as well as my investigation and study of relevant materials, including those cited here. I may rely upon these materials, my knowledge and experience, and/or additional materials to rebut arguments raised by the Patent Owner. Further, I may also consider additional documents and information in forming any necessary opinions, including documents that may not yet have been provided to me.

5. My analysis of the materials produced in this proceeding is ongoing and I will continue to review any new material as it is provided. This declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated here based on new information and on my continuing analysis of the materials already provided.

II. QUALIFICATIONS AND BACKGROUND INFORMATION

6. I have personal knowledge or have developed knowledge of these technologies based upon education, training, or experience, of the matters set forth herein.

7. A detailed description of my professional qualifications, including a listing of my specialties/expertise and professional activities, is contained in my curriculum vitae, a copy of which is provided as Appendix A. Below is a short summary of my professional qualifications.

A. Educational Background

8. I received a Bachelor of Science degree in Electrical Engineering from the University of California, Berkeley, in 1983. I received Master of Science and Ph.D. degrees in Electrical Engineering from Stanford University in 1985 and 1989, respectively.

B. Professional Experience

9. From 1989 to 1992, I was a member of technical staff at Texas Instruments, Inc. At Texas Instruments, my job responsibilities included process integration, device modeling, high-voltage CMOS process integration, and investigating novel source-side injection mechanisms for Flash EPROM channel hot-electron programming.

10. From 1992 to 1995, I was a member of the technical staff at Advanced Micro Devices, Inc. (AMD) where I was a key contributor in optimizing Flash cell and periphery devices in AMD's CMOS-based 0.5um and 0.35um Flash EPROM technology. My job responsibilities at AMD also included process integration, device modeling, and development of triple-well process technology for accommodate x-decoder transistors and high voltage transistors for negative gate erase operation. While at AMD, I was awarded a Spotlight Award for developing a method of manufacturing a self-aligned source (SAS) etch for a NOR flash memory.

11. I spent the next five years of my career in managerial and director roles at several California-based semiconductor companies. I was responsible for increasing yield and for leading teams of engineers working to develop next-generation memory devices.

12. In 2000, I co-founded Progressant Technologies in Fremont, California. Progressant Technologies developed IP for negative differential resistance transistor technology and was eventually acquired by Synopsys, Inc.

13. From 2000 to 2004, I was a Senior Manager at Xilinx, Incorporated, where I was responsible for developing nonvolatile memory process technology for flash and CPLD product applications, as well as advanced CMOS process technology (specifically 75nm CMOS technology node, a half node version between 90nm and 65nm). The flash memory products I developed at Xilinx are used as the configuration memory for the FPGA, with the configuration interface between them being the JTAG interface.

14. From 2004 to 2007, I was a Senior Scientist at Maxim Integrated Products where I was responsible for developing Embedded Non-volatile Memory process technology for Power Management product applications.

15. Since 2007, I have served as a technical consultant where I have provided expert advice regarding Flash memory technology, CMOS process technology, and semiconductor device physics.

16. I have 20 years of experience as an engineer and engineering manager/director of Complementary Metal Oxide Semiconductor (CMOS) technology development. During my career, I have worked at some of the leading technology companies in the world, such as Texas Instruments, Advanced Micro Devices, Altera Corporation (now a subsidiary of Intel Corp.), and Xilinx. At these companies, my work focused on various aspects of CMOS and semiconductor technology.

17. I hold over 95 U.S. patents, a large number of which are directed to

logic CMOS processes technology and high voltage CMOS process technology.

The vast majority of my patents are in the area of CMOS process technology and memory architecture. As such, I am intimately familiar with the implementation of integrated process flows that essentially are repetitive sequences of modules, each composed of a layer patterning step followed by selective deposition and etching of various semiconductor materials, with the area of selectivity dictated by the layer patterning.

III. OVERVIEW OF CONCLUSIONS FORMED

18. The analysis and conclusions set forth in this Declaration are informed by my educational background and experiences in the field (see Section II).

19. Additionally, as part of my independent analysis for this Declaration, I have considered the following: the background knowledge/technologies that were commonly known to a person of ordinary skill in the art at the time of alleged invention (“POSITA”) before the earliest claimed priority date for the ’736 patent (11/29/2002); my own knowledge and experiences gained from my work experience in the field and related disciplines; and my experience in working with others involved in this field and related disciplines.

20. In addition, I have reviewed the ’736 patent (EX-1001), relevant excerpts of the prosecution history of the ’736 patent (EX-1002), and relevant ex-

cerpts of the prosecution history of the '736 patent's Japanese counterpart application and certified translation thereof (EX-1005, EX-1006, EX-1007). I have also reviewed at least the following prior art references:

- JPH11185654A to Yukio Masuda et al ("Masuda") and certified translation thereof (EX-1008, EX-1009)
- U.S. Pub. Patent. No. 2003/0090447 ("Kimura") (EX-1020)
- JP2002-278504A to Mitsuo Inoue et al ("Inoue") and certified translation thereof (EX-1010, EX-1011)
- KR960012168A to Yang-Ho Kwon ("Kwon") and certified translation thereof (EX-1012, EX-1013)

21. I have also reviewed some cited supporting references and documentation including:

- U.S. Patent No. 5,831,699 ("Wright") (EX-1004)
- Sarma et al., "Flat Panel Displays for Portable Systems," 13 Journal of VLSI Signal Processing Systems 165-190 (1996) (EX-1014)

22. Counsel has informed me that I should consider these materials through the lens of one of ordinary skill in the art related to the '736 patent at the time of the earliest possible priority date of the '736 patent, and I have done so during my review of these materials. Counsel has informed me that the earliest possi-

ble priority date to which the challenged claims of '736 patent are entitled is November 29, 2002 ("Critical Date"), and I have therefore used that Critical Date in my analysis below.

23. Any figures that appear within this document have been prepared with the assistance of Counsel and reflect my understanding of the '736 patent and the prior art discussed below.

24. Although this Declaration refers to certain portions of the cited references for the sake of brevity, it should be understood that these citations are examples, and that one of ordinary skill in the art would have viewed the references cited herein in their entireties and, for reasons detailed later, in combination with other references cited herein or cited within those references themselves. The references used in this Declaration, therefore, should be viewed as being cited and analyzed herein in their entireties.

25. This declaration explains the conclusions that I have formed based on my analysis. To summarize those conclusions, based upon my knowledge and experience and my review of the prior art publications listed above, I believe that:

- Claims 18 and 33 are anticipated by, and obvious over JPH11185654A ("Masuda") (Ground 1A)
- Claims 18, 23, 33, and 35 are obvious over Masuda in view of U.S. Pub. Patent App. No. 2003/0090447 ("Kimura") (Ground 1B)

IV. LEVEL OF ORDINARY SKILL IN THE ART

26. Based on my knowledge and experience in the field and my review of the '736 patent and its file history, I believe that a person of ordinary skill in the art at the time of alleged invention ("POSITA") would have had at least a Master's degree in electrical engineering, physics, or a related field, and at least two years of relevant work experience in the field of integrated circuit design and manufacturing. Additional education can remedy lack of work experience and vice versa.

27. Based on my experience, I have a good understanding of the capabilities of one of ordinary skill. Furthermore, I possess those capabilities myself.

V. LEGAL STANDARDS

28. I have been informed by counsel of certain legal principles applicable to a patentability analysis and I have applied these principles as listed below.

A. Claim Construction

29. I have been informed by Counsel and understand that the best indicator of claim meaning is its usage in the context of the patent specification as understood by one of ordinary skill. I further understand that the words of the claims should be given their plain meaning unless that meaning is inconsistent with the patent specification or the patent's history of examination before the Patent Office. Counsel has also informed me, and I understand that, the words of the claims should be interpreted as they would have been interpreted by one of ordinary skill

at the time the invention was made (not today). Because I do not know at what date the invention as claimed was made, I have used the earliest priority date of the '736 patent as the point in time for claim interpretation purposes. That date was November 29, 2002.

B. Legal Standards for Anticipation

30. I have been informed by Counsel and understand that documents and materials that qualify as prior art can render a patent claim unpatentable as anticipated. I am informed by Counsel and understand that all prior art references are to be looked at from the viewpoint of a person of ordinary skill in the art.

31. I am informed by Counsel and understand that a challenged claim is unpatentable as “anticipated” under 35 U.S.C. § 102 if it is determined that all the limitations of the claim are described in a single prior art reference. I am informed by Counsel and understand that, to anticipate a claim, a prior art reference must disclose, either expressly or inherently, each and every limitation of that claim and enable one of ordinary skill in the art to make and use the invention.

32. I have been informed by Counsel and understand that in an inter partes review, “the petitioner shall have the burden of proving a proposition of unpatentability,” including a proposition of anticipation, “by a preponderance of the evidence.” 35 U.S.C. § 316(e).

C. Legal Standards for Obviousness

33. I have been informed by Counsel and understand that documents and materials that qualify as prior art can render a patent claim unpatentable as obvious. I am informed by Counsel and understand that all prior art references are to be looked at from the viewpoint of a person of ordinary skill in the art at the time of the invention, and that this viewpoint prevents one from using his or her own insight or hindsight in deciding whether a claim is obvious.

34. I have been informed by Counsel and understand that a claim is unpatentable for obviousness under 35 U.S.C. § 103 (in the pre-AIA form of that statute that applies to the '736 Patent) "if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." I am informed by Counsel and understand that obviousness may be based upon a combination of references. I am informed by Counsel and understand that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. However, I am informed by Counsel and understand that a patent claim composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.

35. I am informed by Counsel and understand that when a patented invention is a combination of known elements, a court must determine whether there

was an apparent reason to combine the known elements in the fashion claimed by the patent at issue by considering the teachings of prior art references, the effects of demands known to people working in the field or present in the marketplace, and the background knowledge possessed by a person having ordinary skill in the art.

36. I am informed by Counsel and understand that a patent claim composed of several limitations is not proved obvious merely by demonstrating that each of its limitations was independently known in the prior art. I am informed by counsel and understand that identifying a reason those elements would be combined can be important because inventions in many instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. I am informed by Counsel and understand that it is improper to use hindsight in an obviousness analysis, and that a patent's claims should not be used as a "roadmap."

37. I am informed by Counsel and understand that an obviousness inquiry requires consideration of the following factors: (1) the scope and content of the prior art; (2) the differences between the claims and the prior art; (3) the level of ordinary skill in the pertinent art; and (4) any objective indicia of non-obviousness, such as commercial success, long-felt but unresolved need, failure of others, industry recognition, copying, and unexpected results. I understand that the foregoing

factors are sometimes referred to as the “Graham factors.”

38. I have been informed by Counsel and understand that an obviousness evaluation can be based on a combination of multiple prior art references. I understand that the prior art references themselves may provide a suggestion, motivation, or reason to combine, but that the nexus linking two or more prior art references is sometimes simple common sense. I have been informed by Counsel and understand that obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references may be supplied by the direction of the marketplace.

39. I have been informed by Counsel and understand that if a technique has been used to improve one device, and a person of ordinary skill at the time of invention would have recognized that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

40. I have been informed by Counsel and understand that practical and common sense considerations should guide a proper obviousness analysis, because familiar items may have obvious uses beyond their primary purposes. I have been informed by Counsel and understand that a person of ordinary skill looking to overcome a problem will often be able to fit together the teachings of multiple

prior art references. I have been informed by Counsel and understand that obviousness analysis therefore takes into account the inferences and creative steps that a person of ordinary skill would have employed at the time of invention.

41. I have been informed by Counsel and understand that a proper obviousness analysis focuses on what was known or obvious to a person of ordinary skill at the time of invention, not just the patentee. Accordingly, I understand that any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed. I have been informed by Counsel and understand that a claim can be obvious in light of a single reference, without the need to combine references, if the elements of the claim that are not found explicitly or inherently in the reference can be supplied by the common sense of one of skill in the art.

42. I have been informed by Counsel and understand that secondary indicia of non-obviousness may include (1) a long felt but unmet need in the prior art that was satisfied by the invention of the patent; (2) commercial success of processes covered by the patent; (3) unexpected results achieved by the invention; (4) praise of the invention by others skilled in the art; (5) taking of licenses under the patent by others; (6) deliberate copying of the invention; (7) failure of others to find a solution to the long felt need; and (8) skepticism by experts. I understand

that evidence of secondary indicia of non-obviousness, if available, should be considered as part of the obviousness analysis.

43. I have been informed by Counsel and understand that there must be a relationship between any such secondary considerations and the invention, and that contemporaneous and independent invention by others is a secondary consideration supporting an obviousness determination.

44. In summary, my understanding is that prior art teachings are properly combined where one of ordinary skill having the understanding and knowledge reflected in the prior art and motivated by the general problem facing the inventor, would have been led to make the combination of elements recited in the claims. Under this analysis, the prior art references themselves, or any need or problem known in the field of endeavor at the time of the invention, can provide a reason for combining the elements of multiple prior art references in the claimed manner.

45. I have been informed by Counsel and understand that in an *inter partes* review, “the petitioner shall have the burden of proving a proposition of unpatentability,” including a proposition of obviousness, “by a preponderance of the evidence.” 35 U.S.C. § 316(e).

VI. TECHNOLOGY BACKGROUND

46. Electronic displays generally work by providing a matrix of “pixels,” each of which emit light. EX-1014 at 6. By controlling the light emitted by each

pixel, these displays can generate images. *See id.* For color displays, each pixel typically comprises “sub-pixels” each of which is responsible for emitting light of a particular color on command. *See, e.g., id.* at 20-21. Prior to the ’736 patent, there were a variety of display technologies. *Flat Panel Displays for Portable Systems* by Kalluri R. Sarma and Tayo Akinwande, *Journal of VLSI Signal Processing Systems* 13, 165-190 (1996) provides a helpful overview of various types of these display technologies. EX-1014. Some of these display technologies are relevant to the ’736 patent and to the prior art discussed.

47. An “electroluminescent display,” also known in the art as an “EL” display or “ELD,” creates light by using electrodes to apply a voltage or current to a material that emits light under these conditions, as electroluminescent material is material that emits light when excited by an electric voltage or current. The Sarma paper describes an ELD that “creates light by the excitation of a powder phosphor or a thin-film phosphor layer.” *See id.* at 4-5. For color displays “red, green, and blue phosphor layers” can be used. *See id.*

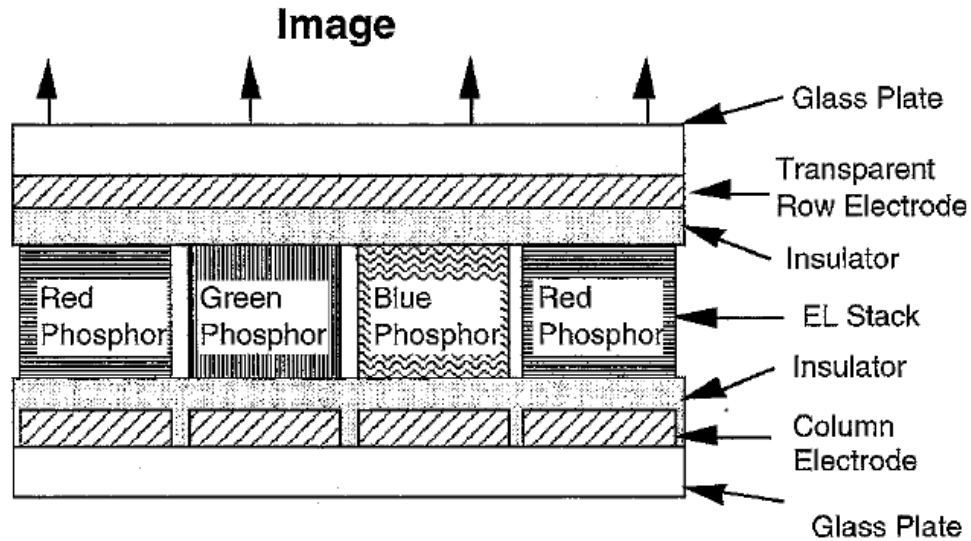


Figure 1. Device structure of the electroluminescent display (ELD).

48. A plasma display operates “by glow discharge of a noble gas.” EX-1014 at 5. It features gas that is “confined between the transparent row and column electrodes.” *Id.* “When a high voltage is applied between the electrodes, the intersection produces a plasma from which light is emitted,” through a secondary excitation of the phosphor’s electrons. *Id.*

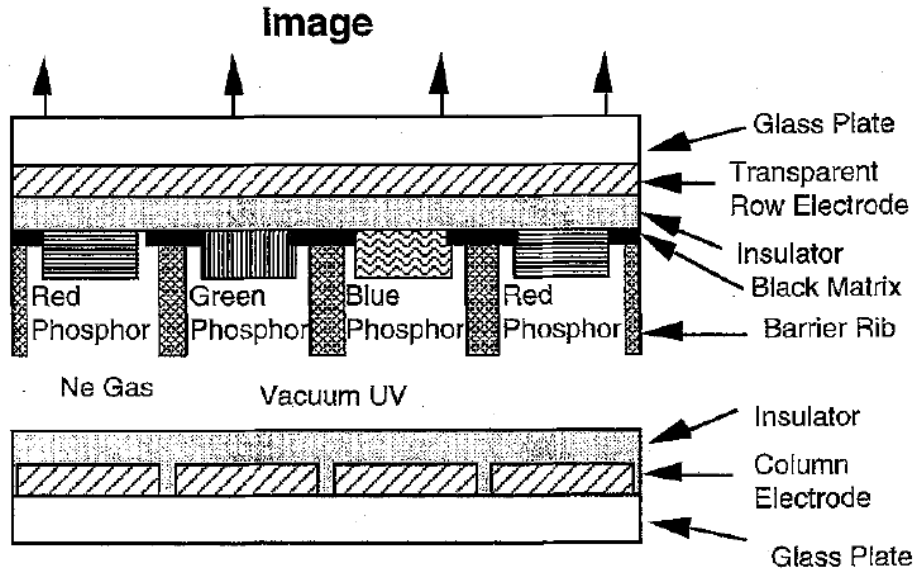


Figure 2. Device structure and operating principles of plasma display panels.

49. A “field emitter display”, also known in the art as “FED” features “sharp cones that emit electrons . . . in the presence of a high electric field.” EX-1014 at 19-20. Those electrons “bombard the phosphor [layer] and create a luminous image which is seen by the viewer.” *Id.*

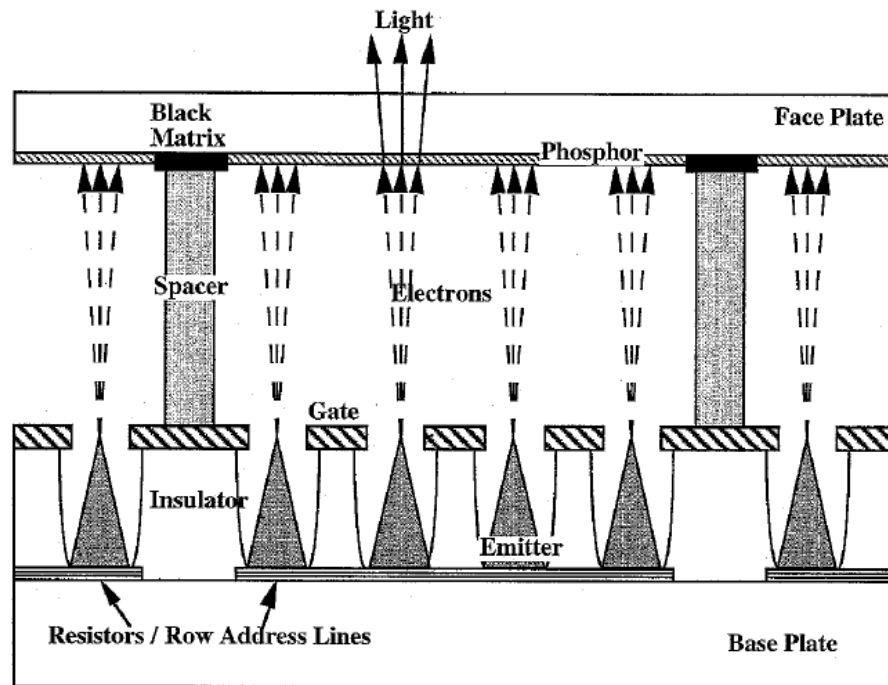


Figure 15. Device structure and operating principles of a field emitter display (FED).

50. To address specific pixels in a display, active matrix technology may be implemented, which utilizes active transistors to drive specific electro-optical elements. *See* EX-1014 at 11-13. An active matrix display generally consists of a matrix of pixels, generating light (luminescence) upon electrical activation, that have been deposited or integrated onto thin-film transistor arrays (arrays of unit driving circuits), with these “TFT” array functioning as a series of control and data input to control the current flowing to each pixel. *See id.* In other words, each pixel comprises a pixel circuit, which in turn comprises an electro-optical element and a driving transistor, which supplies power to the electro-optical element. *See id.*

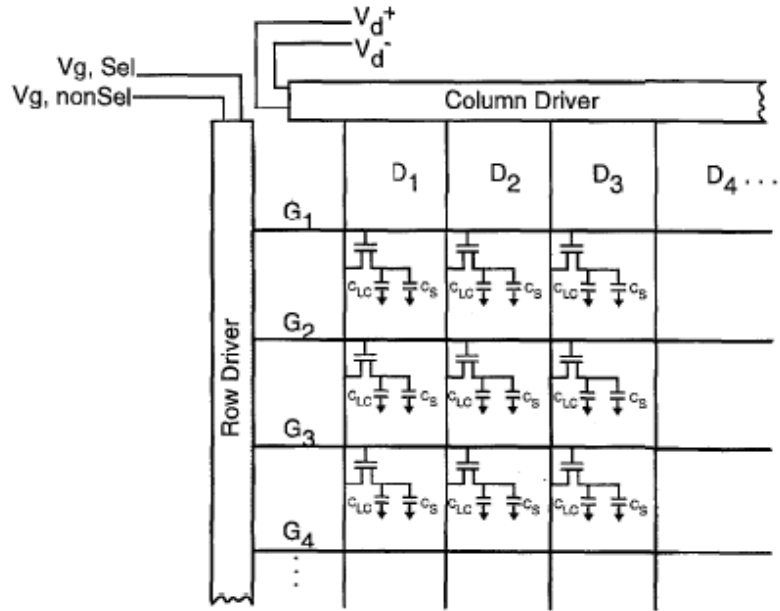


Figure 7. Schematic of a TFT active matrix array.

Id. at Fig. 7.

51. Each of the plurality of pixel circuits in an active matrix display is arranged to correspond to the intersection of a data line and a control line (gate signal line or scan line):

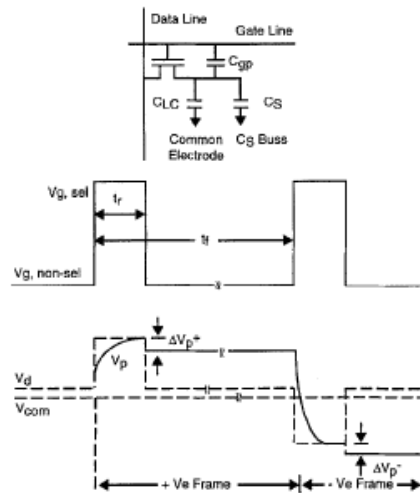


Figure 10. Electrical equivalent of a TFT-LCD pixel, and its operation.

Id. at Fig. 10.

52. The current flowing through an electro-optical device in an “active matrix” arrangement is fundamentally controlled by circuitry associated with each pixel. *See id.* at 11-13, Fig. 7.

53. An active matrix system stands in contrast to a passive matrix system. *See id.* at 2. For example, a passive matrix LCD system utilizes a set of multiplexed electrodes that are made of a conductive film, usually indium-tin oxide or ITO, with the electrodes arranged in a row and column formation placed above and below the LCD layer. *See id.* at 9-11. The rows and columns are then connected to integrated circuits to control the columns and the rows of electrodes. *See id.* Active matrix LCD systems have a similar construction to the passive implementation. *See id.* Like a passive matrix system, an active LCD matrix uses a semi-transparent conductive grid to supply the drive current. *See id.* The difference is that the active matrix system has driving transistors built into each pixel. *See id.* Due to the many advantages offered by the active matrix system, a POSITA would have looked to various teachings in the field that offer an improved active matrix system in implementing a display panel device. This would not only include LCD or plasma displays, but OLED and other self-emission type of display devices. This endeavor would also include looking into various teachings that would im-

prove upon or mitigate the variations introduced by the inherent device characteristics variations of TFT transistors implemented in non-single crystalline silicon.

54. Many measurements characterize the quality of the image from a display device, with viewing angle and contrast ratio as two common metrics that are often used to compare the quality of the display device. *See id.* at 3, 6, 23. The contrast ratio measures the luminance of the display between on state and off state, with the off state being the black state. *See id.* It is essentially a measure of the brightness on a full white state vs. the darkness on a black state. *See id.* This ratio is mainly impacted and degraded by the reflective ambient light off the display panel. *See id.* The other quality metric, the viewing angle, is a measure of the variation in contrast ratio under different directional viewing. *See id.*

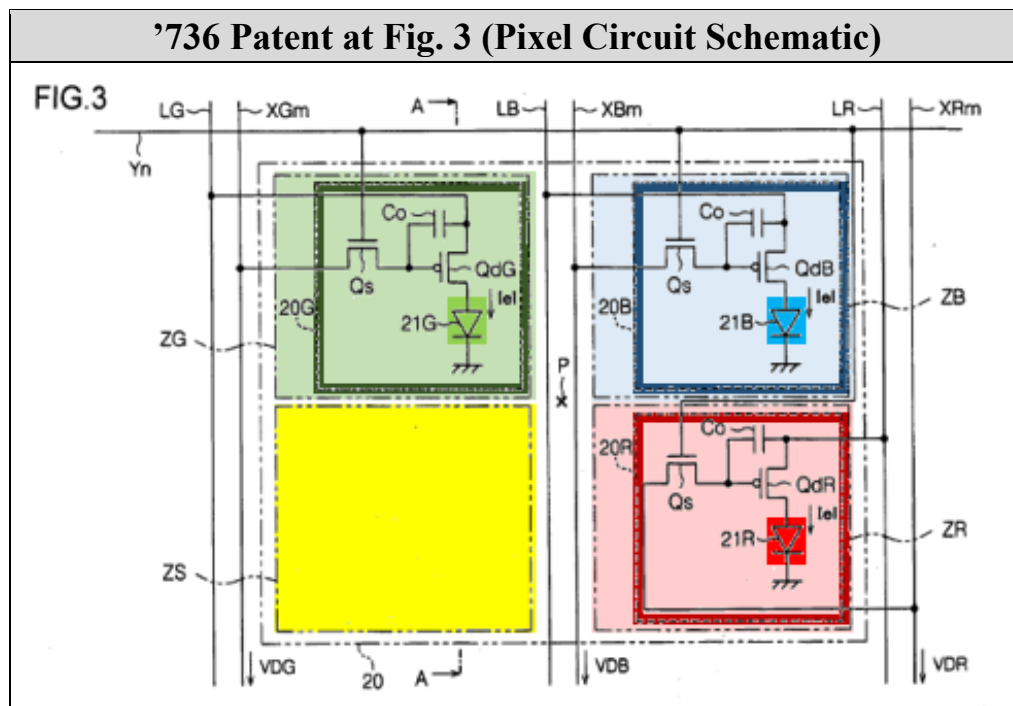
55. Given that the contrast ratio is a function of the black state, it was apparent to a POSITA at the time of the '736 patent that for a given pixel area (with sub-pixels of different color regions), the contrast ratio would be enhanced with a larger area of black region, or light absorbing region; with the light absorbing region stemming from having an anti-reflective property. *See, e.g., id.* at 17 (“Reflection of the ambient light from the display panel reduces the contrast ratio.”). This was known to help reduce the ambient reflected light that may reflected off the surface of the display device panels. *See id.* This reduction of the reflective light can be achieved through the application of an anti-reflective coating on the

area of a pixel, including both areas that are utilized by the optical regions of the sub pixels within a pixel, as well as the peripheral area (e.g., areas that are not utilized by the optical regions of the sub-pixels) of such a pixel. *See id.*

VII. THE '736 PATENT

A. Overview of the '736 Patent

56. The pattern of display pixels for an exemplary first embodiment is illustrated in Figure 3 of the '736 patent:



'736 Patent File History at Fig. 3 (annotated to show “[pixel/dummy] forming regions,” “pixel circuits,” and “organic EL (electroluminescent) elements”).¹

¹ I use the '736 patent's original November 14, 2003, filing's figures rather than the '736 patent's figures. EX-1002 at 31-37. The '736 patent apparently issued

57. The pattern features green (“ZG”), blue (“ZB”), and red (“ZR”) “pixel forming regions,” and a “dummy forming region” (“ZS”) laid out in a square lattice. *See* EX-1001 at 7:58-62. Each pixel region features a “pixel circuit” (20G, 20B, and 20R for green, blue, and red, respectively) to drive an “organic EL (electroluminescent) element” (21G, 21B, and 21R). *See id.* at 7:44-48. The dummy region, in contrast, lacks pixel circuits or elements and instead features an “anti-reflection member made of black polyimide or the like.” *Id.* at 8:1-5. The ’736 patent concludes that the formation of the dummy forming regions ZS can ensure that black is displayed on the display panel portion 12, and as a result, the contrast ratio of the display is enhanced. *Id.* at 8:4-8.

58. As mentioned earlier, the contrast ratio is a measure of the brightness in an on state versus the darkness in a black state. A POSITA would have found it obvious that for a given pixel area (with sub-pixels of different color regions), the contrast ratio would be enhanced with a sub-pixel area of a black region, or light absorbing region; particularly with the light absorbing region having an anti-reflective property. *See* EX-1014 at 3, 6, 23. The black region acting as the ineffective

with the wrong figures, which pertain to unrelated U.S. application no. 10/721,381 and not the ’736 patent (U.S. application no. 10/712,381).

region for the pixel, contrast ratio between white and black can be enhanced.

59. An “electro-optical element” as disclosed in the ’736 patent, is a component that uses its electro-optical effect to display colored light for a pixel; with the electro-optical effect referring to the use of electrical signal to modulate the optical properties and behavior. *See* EX-1001 at 2:5-14. As such, liquid crystal elements, organic EL (electroluminescent) elements, electrophoresis elements, electron emitting elements, and plasma emission elements, among others, all fall in this category being an electro-optical element. *See id.* at 1:11-14, 3:62-64, 16:42-47. Relatedly, a “light-emitting film” is a material within an electro-optical element that emits light. *See id.* at 5:26-28 (“In this case, the EL element is constituted by an organic EL element[,], the light-emitting layer of which is made of organic material.”).

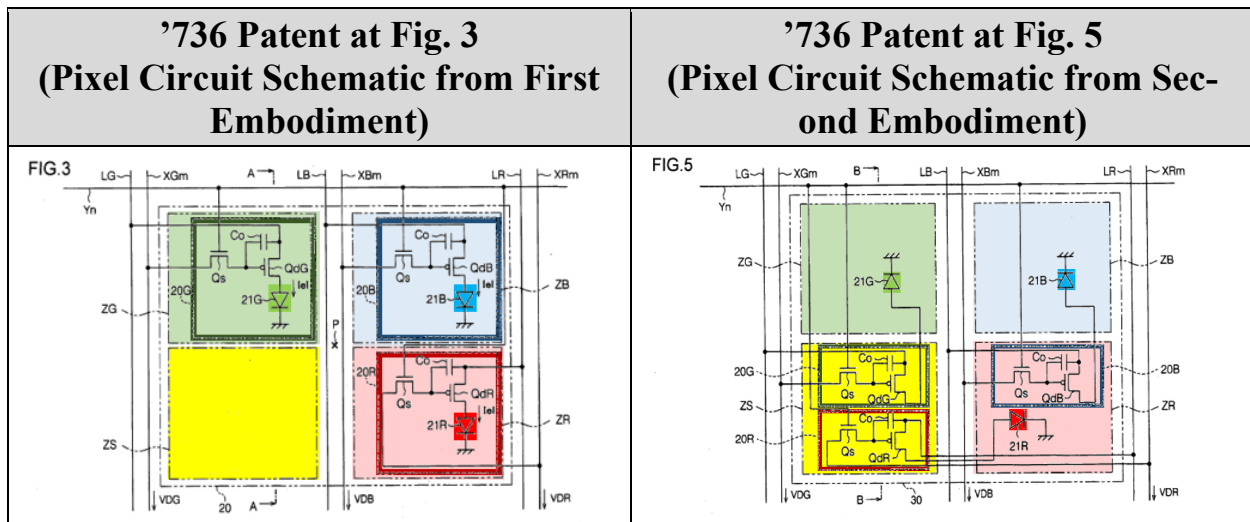
60. An “effective optical region” as well as a “light emitting region” and an “element forming region”—terms coined by the ’736 patent—encompass where a particular electro-optical element is placed. *See id.* at 1:53-62 (using terminology “effective optical regions”), 4:6-16 (using terminology “light-emitting regions”), 5:29-39 (using terminology “element forming regions”), 7:58-8:8 (describing figure 3 as depicting “pixel forming regions” that each have an “organic EL element”). The ’736 patent discloses that “a first effective optical region or a first

light emitting region and a second effective optical region or a second light emitting region recited in the claims correspond to, for example, two pixel forming regions selected from the green, blue, and red pixel forming regions ZG, ZB, and ZR in [the first] exemplary embodiment.” *Id.* at 12:13-19; *see also id.* at 12:32-38 (“[F]irst element forming regions, second element forming regions, and non-element-forming regions recited in the claims correspond to, for example, . . . the green, blue, and red pixel-forming regions ZG, ZB, and ZR, and the dummy forming region ZS, respectively.”). These terms are not standard terms of the art, but are used in the ’736 patent to describe the physical or geographical regions within the pixel display array of the display device that contains the electro-optical elements and their light emitting films.

61. The ’736 patent does not limit the types of display technology to which its allegedly novel pixel pattern may apply. For example, it states that the pixel circuits it describes may be embodied in LED or FED (i.e., field emission display) technology. *See* EX-1001 at 16:42-47.

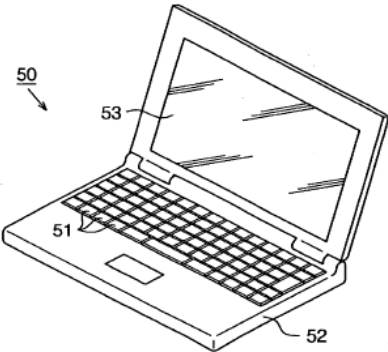
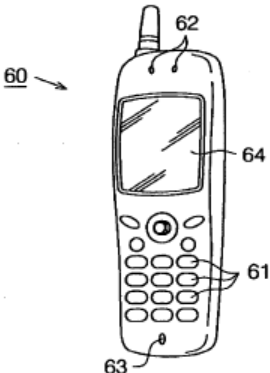
62. The ’736 patent also discloses a second embodiment. The second embodiment is similar to the first except that the green and red pixel circuits are relocated from their original locations to the non-luminous / non-element-forming region and the blue pixel circuit is relocated from its original location to the red light-emitting / element forming region. *See* EX-1001 at 13:42-63. Relocating the

circuits in this manner allegedly allows the “aperture ratios in the green pixel forming region ZG and the blue pixel forming region ZB” to be increased. EX-1001 at 13:52-53. For example, the patent states that the “formation of the pixel [circuits²], which control the green and red organic EL elements 21G and 21R, in the dummy forming region ZS can reduce the area of the pixel circuit 30.” *Id.* at 15:24-28.



63. The '736 patent also discloses a third embodiment. This third embodiment generally involves implementing the concepts discussed above in a “mobile personal computer” or a “portable telephone.” See EX-1001 at 15:30-60.

² The patent’s reference to “pixel elements” rather than “pixel circuits” in this section appears to be a typo. See EX-1001 at 13:42-45, 13:58-63.

'736 Patent at Fig. 7 (Mobile Personal Computer)	'736 Patent at Fig. 8 (Portable Telephone)
	

B. United States Patent Office Proceedings

64. During prosecution of the application that ultimately issued as the '736 patent, the claims were rejected in an office action that issued September 12, 2006, in light of U.S. 5,831,699 to Wright. EX-1002 at 241-250; EX-1004. The Examiner argued that Wright disclosed ineffective optical regions (highlighted in yellow below) that were sandwiched by effective optical regions (highlighted in red below). *See* EX-1002 at 241-250. The Examiner did not treat claim 1 and 3's "effective optical regions" any differently from claim 16's light-emitting regions" or from claim 26 and 27's "element forming regions." *See id.* at 25-28, 245-246. Likewise, the Examiner did not treat claim 1 and 3's "ineffective optical regions" any differently from claim 16's "non-luminous regions" or claim 26 and 27's "non-element-forming regions." *See id.*

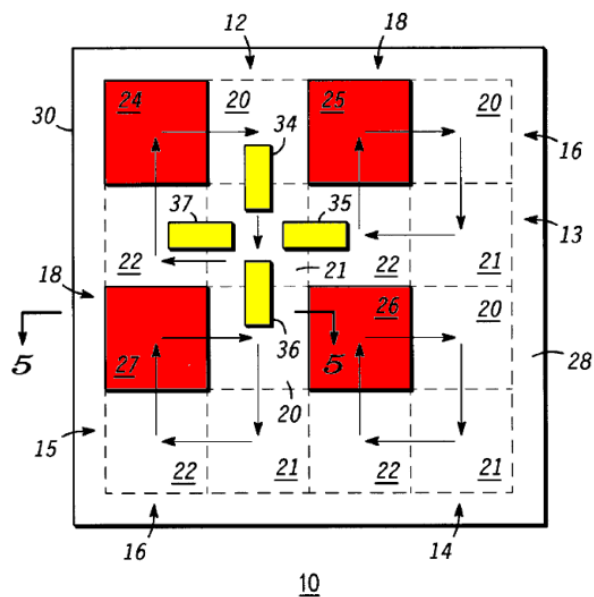


FIG. 1

EX-1004 at Fig. 1.

65. To overcome the Wright reference, the Applicant amended the claims that ultimately issued as claims 3, 18, and 33 to further require that the “whole” ineffective optical region / non-luminous region / non-element-forming region must be sandwiched. *See* EX-1002 at 258-259. Based on the image above, the Applicant appears to have used the word “whole” to mean that no part of the ineffective optical region extends beyond the effective optical regions that sandwich the ineffective optical region. A notice of allowance issued April 9, 2007, which stated that none of the cited references “teaches the whole ineffective optical regions being arranged so as to be sandwiched by two of the first effective optical regions and so as to be sandwiched by two of the second effective optical regions.” *Id.* at 279.

C. Japanese Patent Office Proceedings

66. During prosecution of the '736 patent's priority Japanese application—JP2002-348622—the Japanese Patent Office identified the Masuda (EX-1008, EX-1009 (translation)) and Inoue (EX-1010, EX-1011 (translation)) references as prior art. *See, e.g.*, EX-1006 at 14 (identifying Masuda (H11-185654) in search report). Moreover, the JPO rejected claims that were essentially the same as claims of the '736 patent that issued before the USPTO, including challenged claims 18 and 33. *See* EX-1007 (relying on Masuda and Inoue in office action rejection). The differences between the claims that the JPO rejected and the claims that the USPTO allowed are minor at best. For example, a “substrate” is a component used in just about any display device:

Claims Anticipated by Masuda According to the JPO	Issued Claims of the '736 Patent
3. An electro-optical device, comprising: a plurality of first effective optical regions provided with a first electro-optical element; a plurality of second effective optical regions provided with a second electro-optical element; and	3. An electro-optical device comprising: a substrate; a plurality of first effective optical regions provided above the substrate, first electro-optical elements being provided in the first effective optical regions; a plurality of second effective optical regions provided above the substrate, second electro-optical elements being provided in the second effective optical

a plurality of non-effective optical regions in which electro-optical elements are not provided; wherein each of the plurality of non-effective optical regions is interposed between two first effective optical regions of the plurality of first effective optical regions and simultaneously interposed between two second effective optical regions of the plurality of second effective optical regions.	regions; and a plurality of ineffective optical regions provided above the substrate, no electro-optical elements being provided in the ineffective optical regions, each of the whole ineffective optical regions being arranged so as to be sandwiched by two of the first effective optical regions and so as to be sandwiched by two of the second effective optical regions.
16. An electro-optical device, comprising on a substrate: a plurality of first light emitting regions on which a first light emitting film is formed; a plurality of second light emitting regions on which a second light emitting film is formed; and a plurality of non-light-emitting regions on which the light-emitting film is not formed; wherein each of the plurality of non-light-emitting regions is interposed between two first light-emitting regions of the plurality of first light-emitting regions, and simultaneously interposed between	18. An electro-optical device, comprising: a substrate; a plurality of first light-emitting regions provided above the substrate, first light-emitting films being provided in the first light-emitting regions; a plurality of second light-emitting regions provided above the substrate, second light-emitting films being provided in the second light emitting regions; and a plurality of non-luminous regions provided above the substrate, no light-emitting films being provided in the non-luminous regions, each of the whole non-luminous regions is arranged so as to be sandwiched by two of the first light-emitting regions and so as to be sandwiched

two second light-emitting regions of the plurality of second light-emitting regions.	by two of the second light-emitting regions.
27. An active matrix substrate, comprising on a substrate: a plurality of first element forming regions where the first electro-optic elements are formed; a plurality of second element forming regions where the second electro-optic elements are formed; and a plurality of non-element forming regions in which electro-optical elements are not formed; wherein each of the plurality of non-element forming regions is interposed between two first element forming regions of the plurality of first element forming regions, and simultaneously interposed between two second element forming regions, of the plurality of second element forming regions.	33. An active matrix substrate comprising: a substrate; a plurality of first element forming regions provided above the substrate, first electro-optical elements being provided in the first element forming regions; a plurality of second element forming regions provided above the substrate, second electro-optical elements being provided in the second element forming regions; and a plurality of non-element-forming regions provided above the substrate, no electro-optical elements being provided in the non-element-forming regions, each of the whole non-element-forming regions being arranged so as to be sandwiched by two of the first element forming regions and so as to be sandwiched by two of the second element forming regions.

EX-1006 at 5-11; EX-1007 at 1-2; EX-1001 at 16:55-18:27.

67. In lieu of disputing that these limitations were disclosed by Masuda and Inoue, the Applicant amended the claims to include requirements that reflect

the second embodiment's teachings regarding moving one pixel circuit from one effective optical region to either a different effective optical region or to an ineffective optical region:

(2) Details of the Invention in the Present Application

As described in the Scope of Patent Claims through the procedural amendment filed with the same date as this written opinion, the invention of the present application is:

"[Claim 1]

An electro-optical device wherein:
a plurality of first effective optical regions provided with a first electro-optical element,
a plurality of second effective optical regions provided with a second electro-optical element,
and
a plurality of non-effective optical regions wherein no electro-optical element is provided
are disposed on a substrate, wherein:
each of the plurality of non-effective optical regions is arranged interposed between two of the plurality of first effective optical regions and also arranged interposed between two of the second effective optical regions; and
of the pluralities of first effective optical regions and second effective optical regions, in at least one first effective optical region and second effective optical region, an electronic circuit is formed for driving an aforementioned electro-optical element that is formed in the other first effective optical region and second effective optical region.

[Claim 2]

An electro-optical device wherein:
a plurality of first effective optical regions provided with a first electro-optical element,
a plurality of second effective optical regions provided with a second electro-optical element,
and
a plurality of non-effective optical regions wherein no electro-optical element is provided
are disposed on a substrate, wherein:
each of the plurality of non-effective optical regions is arranged interposed between two of the plurality of first effective optical regions and also arranged interposed between two of the second effective optical regions; and
in an aforementioned non-effective optical region, an electronic circuit is formed for driving an aforementioned electro-optical element that is formed in at least one of the first effective optical regions and the second effective optical regions.

EX-1007 at 3-4 (underlining reflects language introduced by amendment).

68. The new requirements of claim 1 of the Japanese counterpart are reflected in claims 23 and 35 that are challenged in this petition.

VIII. SUMMARY OF THE CITED PRIOR ART

A. Overview of Masuda

69. JPH11185654A (“Masuda”) is a Japanese patent application that published on July 9, 1999. It relates to a display panel and aims to “improve image quality by reducing visual interference . . . due to differences in luminosity.” EX-1009 at [Problem]. Luminosity, in this context, refers to the brightness of pixels that form the display panel. “Differences in luminosity” refer to the problem that certain pixels may appear brighter than others, depending on how they are arranged in a pattern. Masuda teaches that rearranging a pixel’s colors in a display can improve these differences in luminosity, and therefore, image quality.

70. Masuda uses the images below (which have been annotated to identify various pixels) to explain this concept. It claims that conventional patterns featured red, green, and blue pixels lined in a “stripe arrangement” as shown in figure 3(a). EX-1009 at [0017]. This stripe arrangement, however, may feature poor “resolution in the horizontal direction” and problematic “vertical stripes.” *Id.*

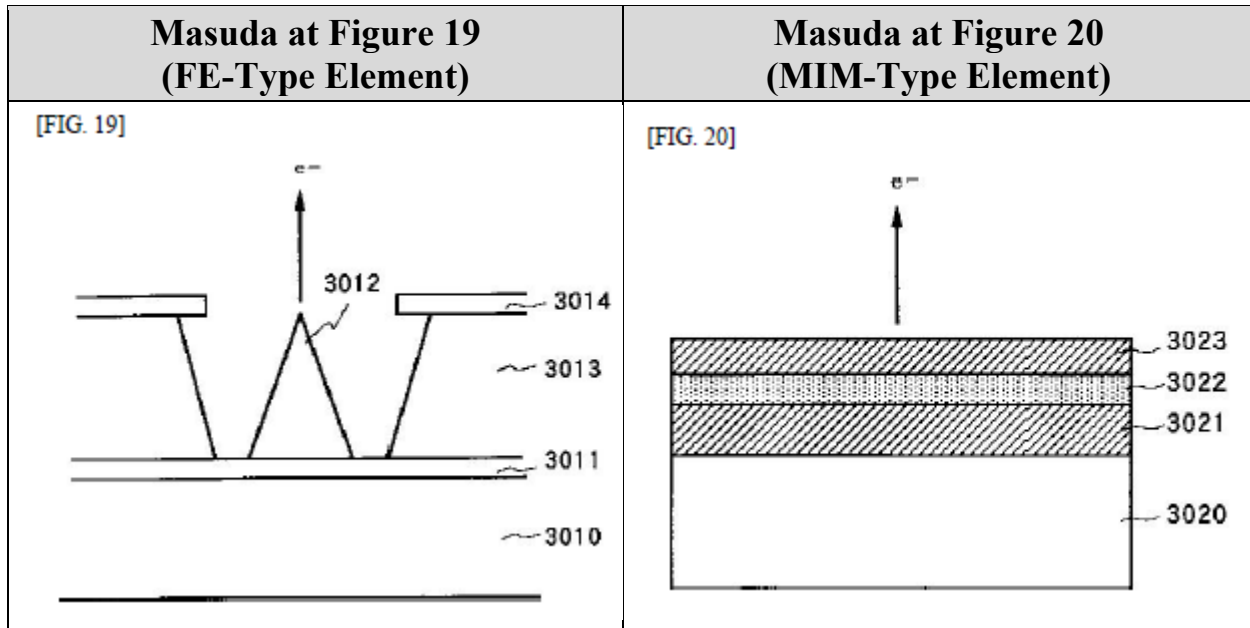
71. A “checkerboard arrangement,” as shown by figure 3(b), has better resolution because the pixels are not arranged in a stripe pattern. *Id.* at [0018]. However, one of the pixels in this checkerboard pattern (green in this instance) will outnumber the two (red and blue in this instance). This would ordinarily cause the green pixels to have higher luminosity than the red and blue pixels. Masuda states

that to compensate for this difference in luminosity, “the green outputs of the two elements are each limited to half in order to . . . achieve a color balance.” *Id.* at [0020].

72. Masuda offers a third pixel pattern, which it claims solves this problem of “difference in luminosity.” *Id.* at [0021]-[0022]. Rather than having a particular color element, such as green, repeat twice in a given pixel, Masuda proposes that instead a “non-display element” be used. *Id.* Thus, in a given pixel, there will be equal numbers of color elements (one green, one red, and one blue), which would reduce “differences in luminosity” across the colors.

Masuda at Figure 3(a) (conventional “stripe arrangement”)	Masuda at Figure 3(b) (conventional “checkerboard arrangement”)	Masuda at Figure 5 (improved arrangement with “non-dis- play elements”)
 (a)	 (b)	

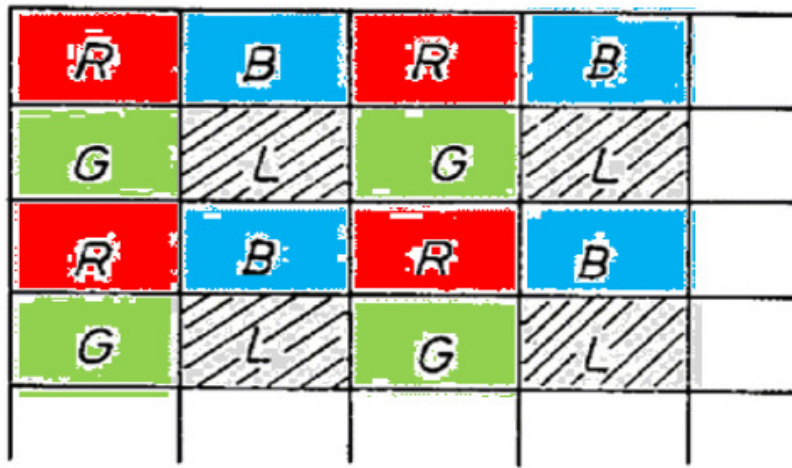
73. Masuda discloses “electron emitting element” types of displays, such as those with “field emission-type emitting elements” (“FE-type”) or alternatively, “metal/insulating layer/metal-type emitting elements” (“MIM-type”). *Id.* at [0002]. Both types of technology feature elements that emit electrons that strike fluorescent material, which in turn produces light. *Id.* at [0015].



74. A POSITA would have understood that Masuda’s specific checker-board pixel pattern could be useful for many different types of color displays—not just FE-types of displays. As discussed above, color displays are and were based on the principle that elements that emit different colors (such as red, green, and blue) could be arranged into pixels, and a collection of pixels would form a display. A particular image could be displayed by setting each color within each pixel to particular values. The “differences in luminosity” problem can be caused by having more of one color element than another, which is a problem that is independent of the particular technology used to implement those color elements.

75. For example, KR960012168A to Kwon discloses a “plasma display device” featuring red, blue, green and “black” pixels (indicated by the letters R, B, G, and L, respectively, in Kwon’s highlighted figure 4 reproduced below:

도면4



EX-1013 at Fig. 4; *see also id.* at Abstract (recognizing that the same pattern of red, blue, green, and a “black” pixel “has the advantage of being able to make the luminance between pixels uniform and improve the contrast”).

B. Overview of Kimura

76. U.S. Pub. App. No. 2003/0090447 (“Kimura”) is a United States patent application that was filed September 18, 2002 and published on May 15, 2003. It generally “relates to an active matrix display device in which a transistor is provided in each pixel to control light emission of the pixel.” EX-1020 at [0001]. It primarily pertains to an active matrix display devices that uses organic light emitting diode pixels (or “OLEDs”). *See id.* at [0003], [0071]-[0072]. Kimura discloses shortcomings in convention methods for driving pixels—including both ana-

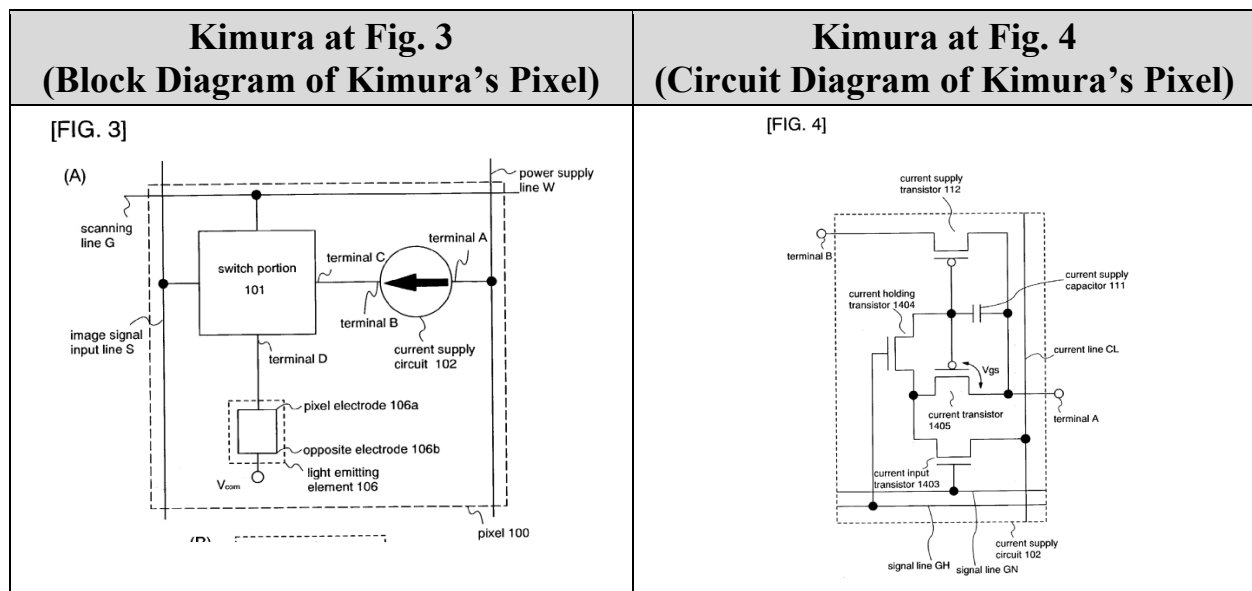
log and digital methods and including both voltage-based and current-based methods. *See e.g., id.* at [0009]-[0011] (addressing “voltage writing type analog method”); *id.* at [0012]-[0014] (addressing “voltage writing type digital driving method”); *id.* at [0015]-[0036] (addressing “current writing type analog method”); *id.* at [0038]-[0041] (addressing “voltage writing type digital driving method”). For example, with respect to the “voltage writing type analog method,” Kimura discloses that “the current flowing in the OLED 3006 fluctuates greatly due to changes in drain current caused by fluctuation in current characteristic of the driving TFT 3004 [or thin film transistor].” *Id.* at [0010], Fig. 30. As another example, Kimura discloses that “a problem of conventional display devices in which driving TFTs operate in a linear range, typically, voltage writing type digital method display devices, is that the amount of current actually flows is varied even when a constant voltage is applied between two electrodes of an OLED.” *Id.* at [0037]; *see also* [0042] (addressing shortcoming of “conventional current writing type analog driving method”). Kimura seeks to improve this driving circuitry to achieve “low-cost display device with a reduced size in which a light emitting element can emit light at a constant luminance irrespective of a change in current characteristic due to degradation or the like, which is fast in writing signals in pixels, and which is capable of displaying in precise gray scales.” *Id.* at [0051].

77. Kimura improves upon conventional driving methods by introducing a

“current supply circuit . . . for causing a fixed current flow.” *Id.* at [0071]. A

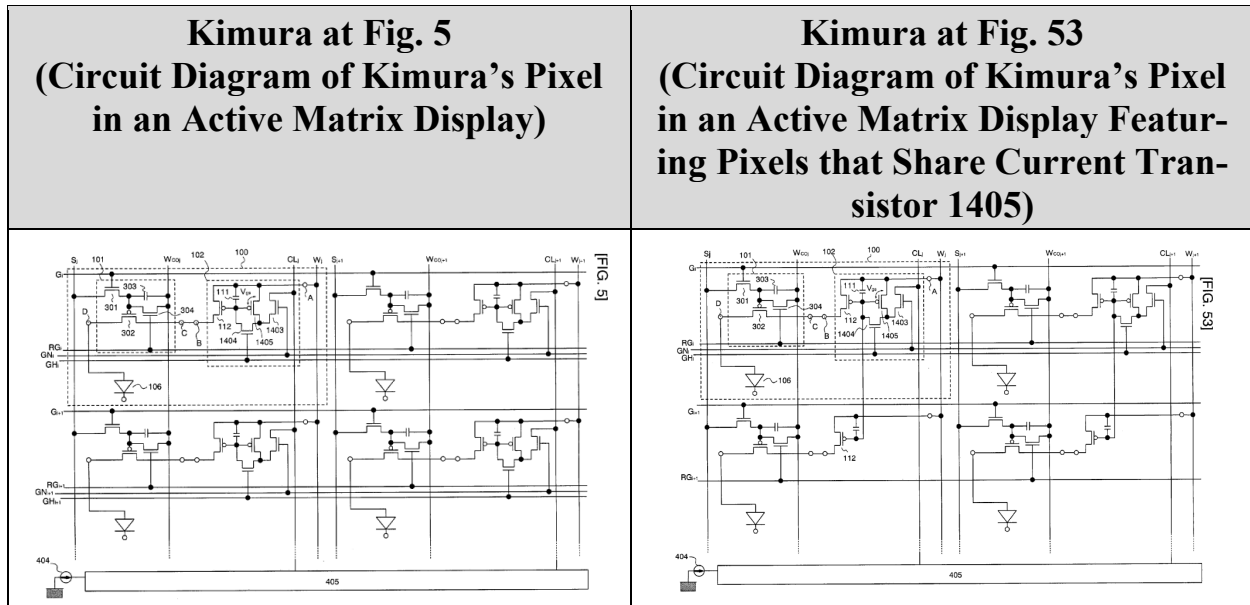
“switch portion” selectively allows the current supply circuit to power an OLED.

Id. “When the switch portion is ON, a constant current determined by the current supply circuit flows in the light emitting element and light is emitted. When the switch portion is OFF, the light emitting element receives no current flow and does not emit light.” *Id.* at [0074]. Kimura teaches that this current supply circuit can be implemented using a “current mirror circuit method” in which “one transistor serves as the current supply transistor 112 and the other serves as a current transistor.” *Id.* at [0180]-[0183]. In this method, the constant current “that flows in the current transistor 1405” determines the current that flows in the current supply transistor 112.” *Id.* at [0265]. This driving method is represented in both block and circuit schematic form in the figures reproduced below:



78. Fig. 3 and Fig. 4 of Kimura would convey to a POSITA that transistor 1405 essentially determines the current that flows in the current supply transistor 112 in that “a constant current according to the current I_0 ’ that flows in the current transistor 1405 flows in the current supply transistor 112.” *Id.* at [0265]. The current that flows through the current supply transistor 112 determines the current that is supplied to drive the OLED element (the electro-optical element). A POSITA would understand that this essentially makes the transistor 1405 the key component of the electronic circuit that drives the electro-optical element. Transistors 1403 and 1404 are also involved in this driving process and also constitute part of the “circuit” that drives the electro-optical element.

79. Kimura identifies this driving method of using a current supply circuit as its “Embodiment Mode 1.” *See id.* at [0184]-[0294]. As part of that embodiment mode, the driving circuitry can be replicated for each pixel in an active matrix display, as shown in figure 5 below. Kimura further discloses a variation of Embodiment Mode 1, which it identifies as “Embodiment 10.” *See id.* at [0466]-[0470]. “This embodiment shows an example of sharing among plural pixels the current transistor 1405, which is placed in each pixel in the pixel structure shown in FIG. 5 in accordance with Embodiment Mode 1.” *Id.* at [0467].



C. Overview of Kimura-Masuda Combination

80. A POSITA would have been motivated to combine the teachings of Kimura and Masuda to implement an organic EL display device (i.e., the display technology disclosed by Kimura) featuring the checkerboard pattern with a non-display element (as disclosed in Masuda).

81. Both references relate to display technology and are concerned with the same problem of reducing variations in luminance across pixels. A POSITA implementing Kimura's display would have been motivated to incorporate the pixel pattern taught by Masuda to further that goal. Kimura aims to provide "a light emitting element can emit light at a constant luminance irrespective of a change in current characteristic due to degradation or the like." EX-1020 at [0051], [0084]. But Kimura does not restrict how color forming pixels must be

laid out. *See id.* at [0290] (noting that light emitting elements can emit red, green, or blue light, but not restricting the order in which those colors must be implemented in, for example, the array depicted by figure 53). A POSITA implementing Kimura's organic EL device would have been motivated to look for complementary techniques to further reduce brightness variation. Masuda describes such a technique by describing how color forming pixels may be laid out, including "self-illuminated" pixels like those disclosed in Kimura. *See* EX-1009 at [0015] (disclosing "self-illuminated" pixels that are superior to liquid crystal displays that were popular in past years); EX-1020 at [0003] (discussing OLED light elements, which are also self-illuminating).

82. Masuda's pixel pattern reduces "the difference in luminosity between columns or difference in luminosity between rows." EX-1009 at [0021]. Masuda teaches that "[t]ypically, when primary color display elements are arranged in two rows and two columns and one desired color is repeated in spatial additive color mixing, it is necessary to consider the luminosity values of the individual elements in arranging the primary color display elements." *Id.* at [0024]. In other words, to create a repeating 2x2 square matrix of colored sub-pixels, one color would ordinarily need to be re-used, which would cause that particular color to have a greater luminosity than the other colors. The problem with such an arrangement is that the output of the repeated element (e.g., green in Masuda Figure 3(b)) must be "limited

to half in order to . . . achieve a color balance.” *Id.* at [0020]. Such a conventional arrangement would also have the effect of causing the viewer to perceive alternating red and blue horizontal or vertical lines. *Id.* at [0019]. Masuda’s improved checkerboard pattern includes “one element that does not contribute to the image display” and places the “the primary color display element that has the highest luminosity value and the primary color display element that has the second-highest luminosity value . . . at opposite corner positions” thereby minimizing “maximum luminosity difference between rows or columns.” *Id.* at [0022], [0027]. This pattern reduces the “stripe” phenomenon. Moreover, Masuda’s checkerboard pattern solves the same directional viewing problem that the ’736 patent seeks to address. The ’736 patent states that by arranging same-color elements “at regular intervals in the column and row directions with one forming region interposed therebetween, it is possible to reduce *directional viewing variation* that occurs between the column direction and the row direction of the display panel.” EX-1001 at 12:61-67; *see also id.* at Abstract; *id.* at 4:21-30 (referencing first or second light-emitting films “arranged so as to [not] be adjacent to each other”). A POSITA would have recognized that Masuda’s pattern also addresses this problem in the same way. Masuda advocates for a “checkerboard” pattern rather than a “stripe” pattern for laying out pixels. *See* EX-1009 at [0017]-[0022]. In the “stripe” pattern, same color pixels are adjacent to one another, which may cause the human

eye to perceive vertical or horizontal lines that are not intended to be displayed.

See id. By instead implementing a “checkerboard” pattern, as Masuda suggests, those colors are more evenly distributed, which reduces the risk that the human eye will perceive lines because luminosity across pixels is more evenly distributed.

See id. Because the “line” problem would be more pronounced in at large viewing angles, Masuda’s checkerboard solution has the same benefit of improving directional viewing variation, as mentioned by the ’736 patent. *See id.*

83. Masuda’s Figure 21 quantifies luminosities by row and column for different possible arrangements of R, B, G, and “non-display” elements. *Id.* at [0028]. “[T]he minimum value among the maximum luminosity differences between columns and rows will be 0.40, where this occurs when the red (R) and green (G) are arranged at opposite corner positions.” *Id.*

[FIG. 21]

				Sum of Luminosity for Each Row and Column				Maximum Luminosity Difference between Rows or Columns
				First Row	Second Row	Third Row	Fourth Row	
m11	m12	m21	m22	行・列ごとの輝度和				行間・列間の最大輝度差
				1行目	2行目	3行目	4行目	
R	G	B	x	0.89	0.11	0.41	0.59	0.78
R	G	x	B	0.89	0.11	0.30	0.70	0.78
R	B	G	x	0.41	0.59	0.89	0.11	0.78
R	B	x	G	0.41	0.59	0.30	0.70	0.40
R	x	G	B	0.30	0.70	0.89	0.11	0.78
R	x	B	G	0.30	0.70	0.41	0.59	0.40
G	R	B	x	0.89	0.11	0.70	0.30	0.78
G	R	x	B	0.89	0.11	0.59	0.41	0.78
G	B	R	x	0.70	0.30	0.89	0.11	0.78
G	B	x	R	0.70	0.30	0.59	0.41	0.40
G	x	R	B	0.59	0.41	0.89	0.11	0.78
G	x	B	R	0.59	0.41	0.70	0.30	0.40
B	R	G	x	0.41	0.59	0.70	0.30	0.40
B	R	x	G	0.41	0.59	0.11	0.89	0.78
B	G	R	x	0.70	0.30	0.41	0.59	0.40
B	G	x	R	0.70	0.30	0.11	0.89	0.78
B	x	R	G	0.11	0.89	0.41	0.59	0.78
B	x	G	R	0.11	0.89	0.70	0.30	0.78
x	R	G	B	0.30	0.70	0.59	0.41	0.40
x	R	B	G	0.30	0.70	0.11	0.89	0.78
x	G	R	B	0.59	0.41	0.30	0.70	0.40
x	G	B	R	0.59	0.41	0.11	0.89	0.78
x	B	R	G	0.11	0.89	0.30	0.70	0.78
x	B	G	R	0.11	0.89	0.59	0.41	0.78

Id. at Fig. 21.

84. A POSITA would have recognized that Masuda's pixel pattern could have been implemented in Kimura's display by arranging Kimura's blue, green, and red organic EL elements as shown below and simply omitting any EL element in the fourth spot of the pixel pattern, as shown below. Omitting the EL element can be accomplished by not including the light emitting film to the driving circuit

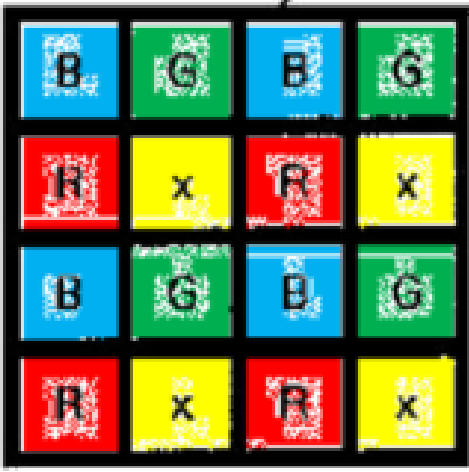
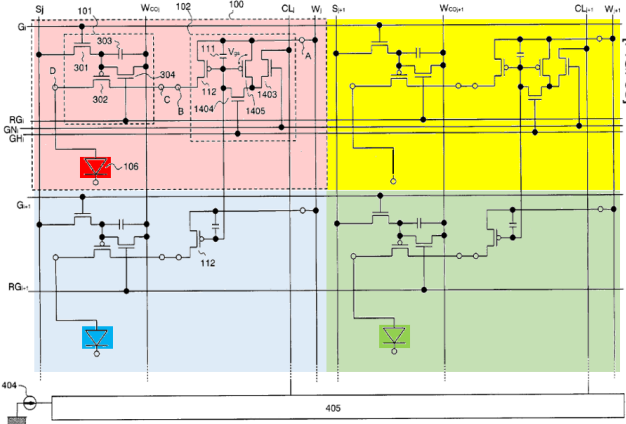
(not forming any EL film). The non-display regions as implemented in the combination would lack electro-optical elements and light-emitting films since, per Masuda, such regions do not emit light.

85. A POSITA arranging Kimura's pixels in Masuda's pattern would have amounted to an application of known techniques to create expected results. Kimura contemplates having colored sub-pixels to form a composite pixel from the perspective of the human eye. This is shown by EX-1020 at Fig. 53 for example, which depicts four sub-pixels next to one another. It further requires that the pixels be laid out in a matrix. EX-1020 at [0001]. But it does not restrict how the colors must be arranged with respect to one another to form the display. A POSITA would recognize that *some* arrangement of pixels must be because the pixels must be organized in some manner in order to form an image. This would have motivated a POSITA employ a known pixel geometry, such as the one disclosed in Masuda.

86. As discussed above, the technique of having one non-luminous / non-element-forming region as part of a checkerboard pattern of sub-pixels was known in the art, as demonstrated by both Masuda and Kwon. *See, e.g.*, EX-1013 at Abstract (referencing red, blue, green, and "black" pixels); Fig. 4. A POSITA using that pattern to implement Kimura would have amounted to simply applying a

known technique to achieve an expected result (a display with less luminous variation across pixels).

87. A POSITA arranging Kimura's pixels in Masuda's pattern would have had a reasonable expectation of success in combining the two references. The problem of luminosity variance due to repeating colors and Masuda's solution is independent of the display technology used. While Masuda generally describes FE-type and MIM-type displays (EX-1009 at [0042]), how to lay out pixels is an issue in any type of display, including an organic EL displays like Kimura. The Kwon reference, for example, confirms that Masuda's improved checkerboard pattern was generally known in the art and could be used in plasma-type displays. *See* EX-1013 at Fig. 4, Abstract. A POSITA would have no reason to doubt that the same pattern would be equally successful in an organic EL display, such as that disclosed by Inoue. Below is reproduced a modified version of Kimura figure 53, which implements Masuda's color pattern and omits an electro-optical element in the top-right region.

Masuda at Fig. 5 (pattern with non-display elements)	Kimura Pixel Pattern of Fig. 53 Modified to Incorporate Teachings of Masuda
	

IX. GROUND 1A

88. In my opinion, Masuda anticipates claims 18 and 33. Additionally, in my opinion, Masuda renders obvious claims 18 and 33.

A. Claims 18 and 33

89. Masuda discloses an “Image Displaying Device Having [a] Display Panel,” which is an “electro-optical device.” *See* EX-1009 at Title; *see also id.* at [0001], [0021], [0101].

90. Masuda discloses a “substrate 1001,” which is a “substrate” as claimed by the ’736 patent. *See* EX-1009 at [0034]; *see also id.* at [0004]-[0005], [0008]-[0010] (discussing structure of field emission displays), [0031]-[0035], Fig. 4, Fig. 19, Fig. 20. A “substrate” in an image display generally refers to a layer upon which light emitting elements are formed. The ’736 patent does not use the

term “substrate” in any different sense.

91. Implementing Masuda’s teachings on an “active matrix substrate” would have been obvious to a POSITA. Masuda does not restrict itself to a particular display technology, instead noting a variety of display technologies in the field. *See, e.g.* EX-1009 at [0002]-[0016] (noting a variety of techniques, including hot cathode elements, cold cathode elements, field emission-type elements, metal-type emitting elements, and liquid crystal elements), Claim 1 (broadly claiming a “display panel for displaying a color image wherein primary color display elements are arranged in a matrix”). Because active matrix is but one of two primary techniques for driving pixels, a POSITA would have found it obvious to apply Masuda’s teachings to a device based on active matrix technology that uses an active matrix pixels disposed on a substrate. *See* EX-1014 at 9-11.

92. Masuda discloses “electro-optical elements” with “light-emitting films.” Masuda discloses “image displaying devices that use combinations of surface conduction-type emitting elements and fluorescent materials that emit light through exposure to an electron beam.” EX-1009 at [0015]. As discussed above, electron-emitting type displays, such as Masuda, featured elements that emit electrons. When these electrons strike a fluorescent material of a particular color, the fluorescent materials emit light. These elements’ fluorescent material thus constitutes a light-emitting film. *See, e.g. id.* at [0037] (characterizing the fluorescent

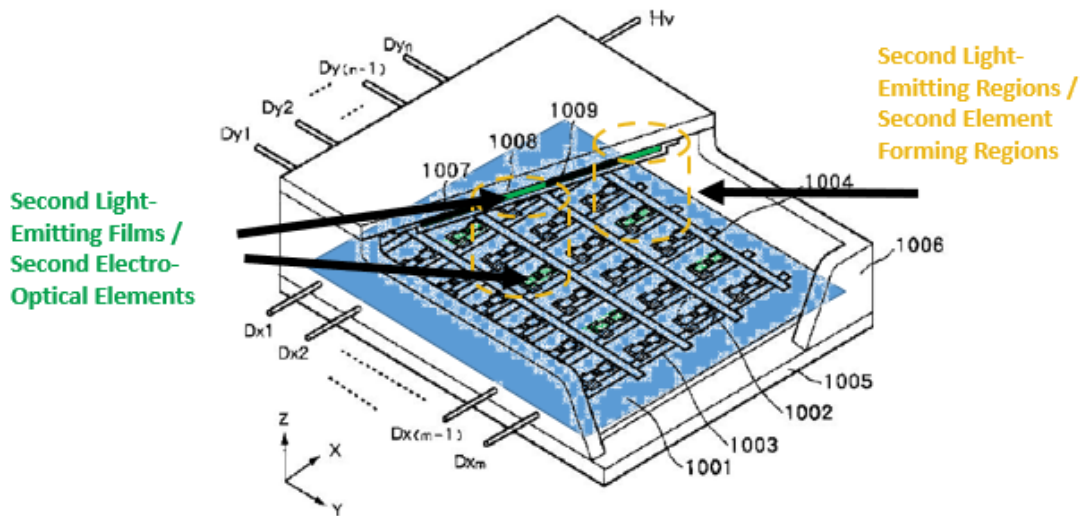
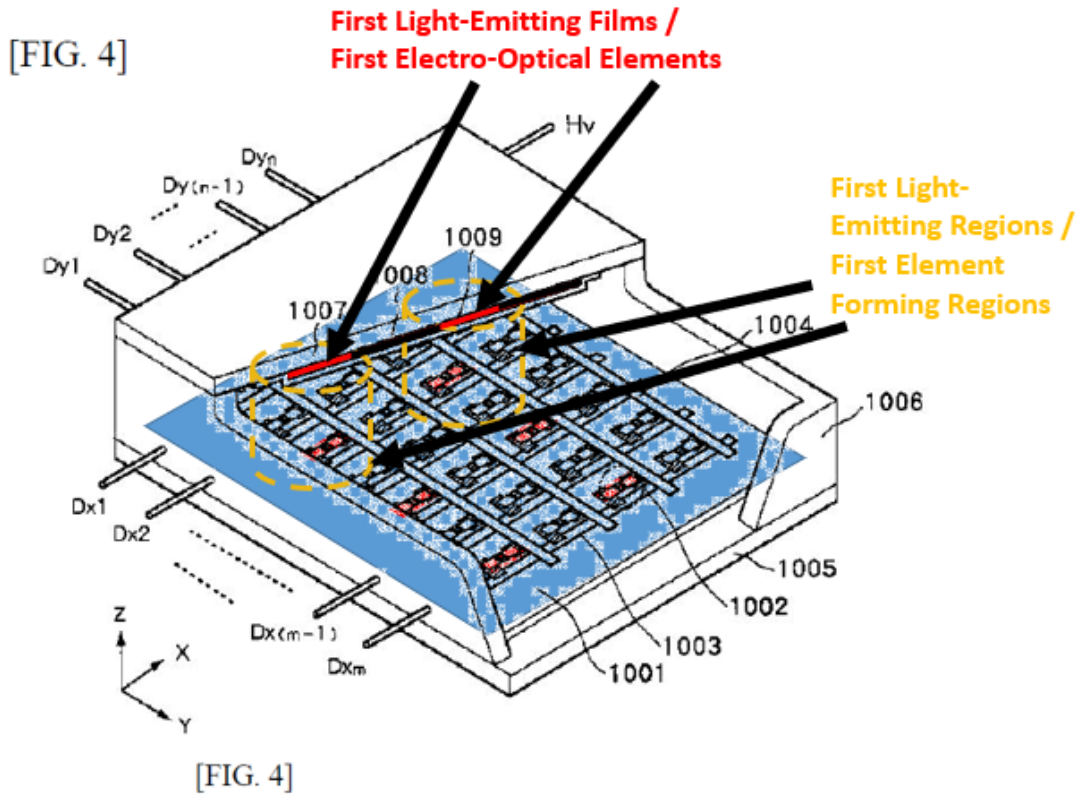
material as a “film”). Additionally, the combination of Masuda’s electron-emitting elements and fluorescent material that they strike constitute an “electro-optical element” because they convert electrical signals (by being driven by electrodes) into optical energy (by emitting light).

93. Masuda’s electro-optical elements and their light-emitting films are provided in “light-emitting regions” / “element forming regions.” Neither “light-emitting regions” nor “element forming regions” is a term of art, and the ’736 patent apparently coined these phrases to refer to a region that includes a particular electro-optical element. Because the element emits light, the optical region is “light-emitting.” Additionally, regions in which these elements are formed constitute “element forming” regions. Thus, the regions in Masuda encompassing particular electro-optical elements are light-emitting / element forming regions. *See* EX-1009 at [0022]-[0026] (referencing “primary color display elements”), [0036].

94. Masuda’s light-emitting / element forming regions are provided above a substrate. As discussed above, display devices include a “substrate,” which generally refers to a layer upon which light emitting elements are formed. *See* EX-1009 at [0032]-[0037].

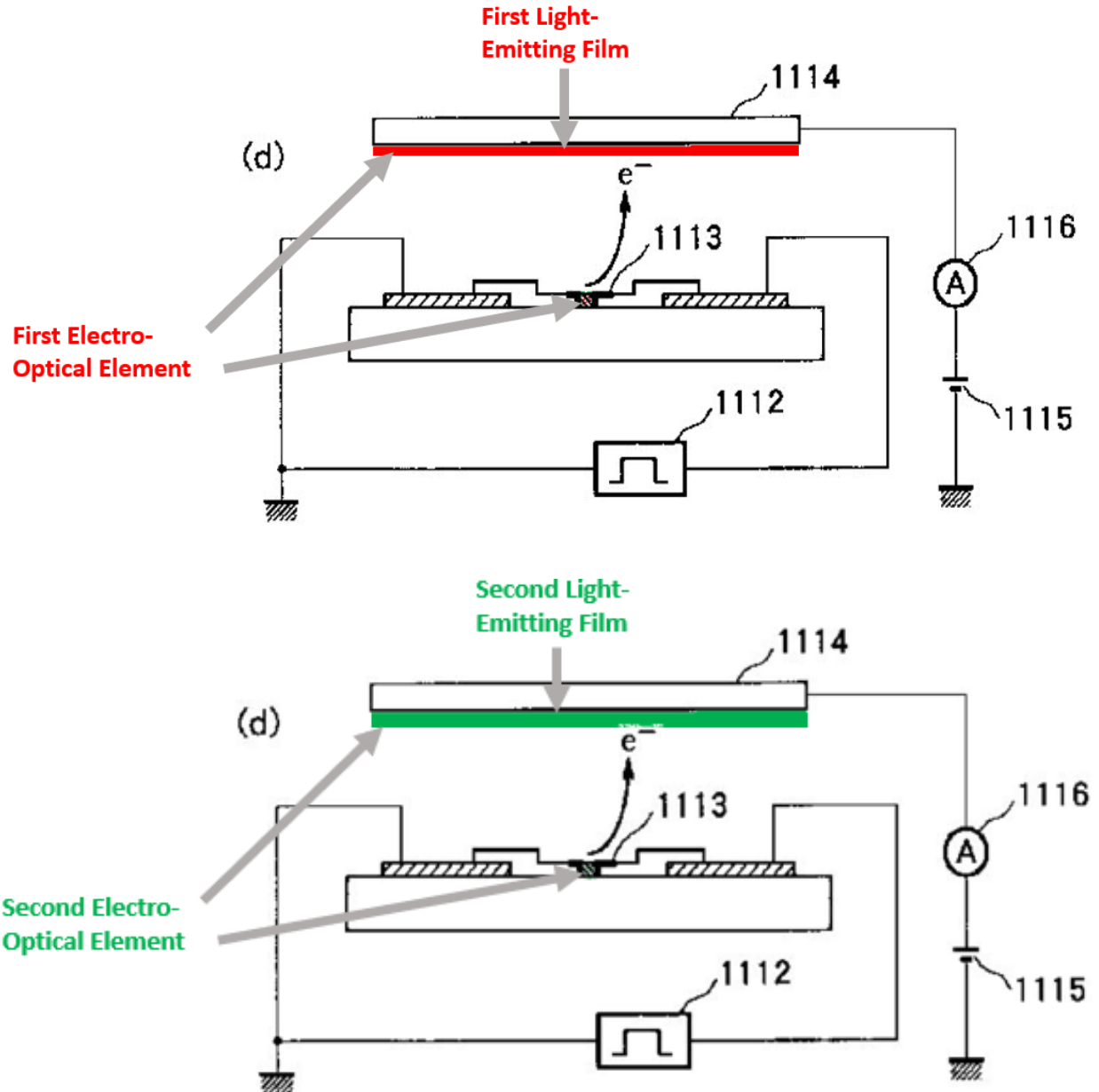
95. Two versions of Masuda’s Figure 4 are reproduced and highlighted below to identify first and second light-emitting / element forming and first and second electro-optical elements with their respective first and second light-emitting

films. The “first” and “second” monikers, in the ’736 patent, each generally refer to collections of a particular color. The top image identifies the substrate (1001) (in blue), red fluorescent material (1008) (in red), and corresponding electron emitting elements (1002) (in red) when laid out in Masuda’s improved checkerboard pattern. The bottom image identifies the substrate (1001) (in blue), green fluorescent material (1008) (in green), and corresponding electron emitting elements (1002) (in green) when laid out in Masuda’s improved checkerboard pattern.



96. Two versions of Masuda's Figure 7(d) are reproduced and highlighted below to show a cross sectional view of electro-optical elements with their respective light-emitting films. In the first version, the red highlights identify an electron emitting portion (identified in other figures as 1105) and its red light-emitting film.

See EX-1009 at [0061]-[0067] (explaining process of creating electron-emitting components). In some embodiments, the “fluorescent face of the display panel is used as the anode electrode 1114.” *Id.* at [0075]. A POSITA would understand that in such embodiments, the fluorescent material would be deposited on the anode electrode so that the anode would attract electrons, causing them to strike the fluorescent material. As discussed above, this fluorescent material is a “light-emitting film” because it emits light when struck by electrons. A POSITA would have understood the light-emitting film in the ’736 patent to be broad enough in nature to encompass this material. EX-1001 at 16:42-47 (“[A]lthough the pixel circuits 20 and 30 are embodied as electronic circuits to provide preferable advantages, they maybe embodied as electronic circuits to drive electro-optical elements, for example, light-emitting elements, such as LED or FED, other than the organic EL elements 21G, 21B, and 21R.”). In any event, red fluorescent material is located above the electron-emitting element so that electrons ejected by the electron-emitting element strike the fluorescent material, causing it to emit light. The second version uses green highlights to identify corresponding components of green electro-optical elements.



97. Two versions of Masuda's Figure 5 are reproduced and highlighted below to identify first (red) and second (green) light-emitting / element forming regions when laid out in Masuda's improved checkerboard pattern.

First Light-Emitting Regions /
First Element Forming Regions



1010: Black Conductive Material
R: Red Fluorescent Body
G: Green Fluorescent Body
B: Blue Fluorescent Body
x: Non-Display Element

R : 赤色蛍光体
G : 緑色蛍光体
B : 青色蛍光体
X : 非表示要素

Second Light-Emitting Regions /
Second Element Forming Regions



1010: Black Conductive Material
R: Red Fluorescent Body
G: Green Fluorescent Body
B: Blue Fluorescent Body
x: Non-Display Element

R : 赤色蛍光体
G : 緑色蛍光体
B : 青色蛍光体
X : 非表示要素

98. Masuda discloses “non-luminous” / “non-element-forming” regions “provided above the substrate” that have no “light-emitting films” or “electro-optical elements.” It teaches an improved checkerboard pattern that includes “one element that does not contribute to the image display,” also referred to as a “non-display element.” EX-1009 at [0022], [0027]-[0029]. This “non-display” element constitutes a non-luminous / non-element-forming region. Neither “non-luminous region” nor “non-element-forming region” is a term of art, but rather these phrases appear to have been coined by the ’736 patent to describe a region of the pixel pattern that is similar, geometrically and structurally, to effective optical regions, except that a non-luminous / non-element-forming region does not emit light. Masuda’s “non-display” elements perform the same function—i.e., they increase contrast, since contrast ratio generally relates to the luminance ratio between the

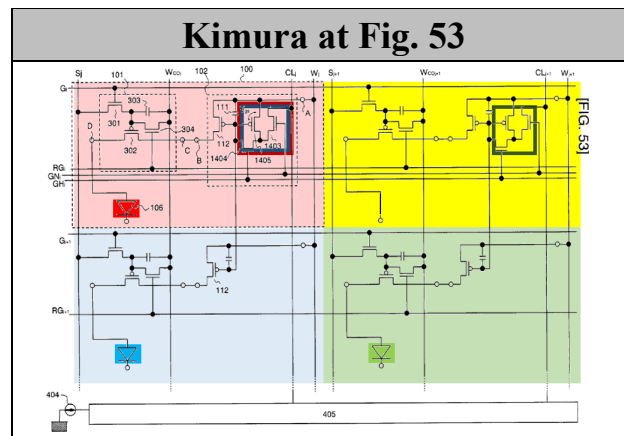
brightest white and darkest black, thereby reducing differences in luminosity and by extension directional viewing variation. A POSITA would have understood that Masuda's "non-display" elements have no electro-optical elements or light-emitting films. If they did, they would emit light, and therefore cease to be non-luminous / non-element-forming regions. For example, including phosphor material in non-luminous / non-element-forming regions would needlessly risk unintentional light emission if stray electrons from adjacent sub-pixels struck that material. If there is no phosphor material (i.e., light-emitting film) for a given non-luminous / non-element-forming regions, there is also no electro-optical element because phosphor is necessary for the region to emit optical light. Moreover, a POSITA would have recognized that omitting electro-optical elements and light-emitting films in those regions would not make the display more costly. Finally, these non-luminous / non-element-forming regions are provided above a substrate for the reasons explained above.

99. Masuda discloses that each of the whole non-luminous / non-element-forming regions are sandwiched by two first light-emitting / element forming regions and by two second light-emitting / element forming regions. As shown by the annotated version of the '736 patent Figure 2 and the annotated version of Masuda Figure 5 below, Masuda's "non-luminous" / "non-element-forming" regions are sandwiched in the same way that the '736 "non-luminous" / "non-element-

60

102. The Kimura-Masuda combination renders obvious “a substrate.” *See supra* Ground 1, Claims 18 and 33. Kimura’s organic EL pixels are “formed on a glass or other insulating substrate.” *See* EX-1020 at [0050].

103. The Kimura-Masuda combination renders obvious “electro-optical elements” with “light-emitting films.” *See supra* Ground 1, Claims 18 and 33. Kimura discloses organic light-emitting diodes (OLEDs), which are electro-optical elements. Those OLEDs feature a “light emitting layer” in an “organic compound layer,” which is a light-emitting film. *See id.* at [0072]. Kimura’s Figure 53 depicts two EL electro-optical elements, an example of which is shown by the figure below, which has been annotated to show that it could emit red light, consistent with Kimura’s teachings.



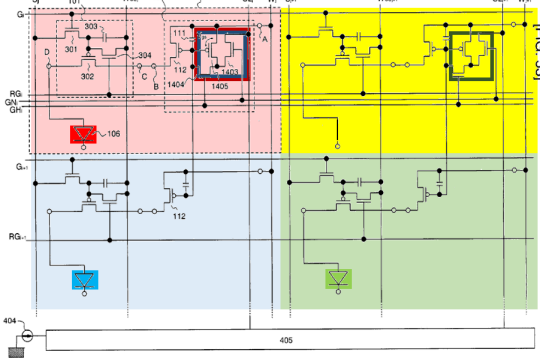
104. The Kimura-Masuda combination renders obvious that electro-optical elements are provided in “light-emitting regions” / “element forming regions.” *See supra* Ground 1, Claims 18 and 33. As shown by the annotated figure 53 above, Kimura discloses circuitry that drives the organic EL elements. The region that encompasses a given element constitutes a light-emitting / element forming region.

105. The Kimura-Masuda combination renders obvious that the light-emitting / element forming regions are provided “above a substrate.” *See supra* Ground 1, Claims 18 and 33. Kimura discloses that “pixels are generally formed on a glass or other insulating substrate.” EX-1020 at [0050].

106. The Kimura-Masuda combination renders obvious “non-luminous regions” / “non-element-forming regions.” *See supra* Ground 1, Claims 18 and 33. As discussed above, this combination features Kimura’s OLEDs laid out in a pattern that aligns with Masuda’s checkerboard pattern that includes a “non-display” element. This non-display element, as discussed in my treatment above of Masuda, constitutes a non-luminous / non-element-forming region. The table below shows how Kimura’s display would implement Masuda’s checkerboard pattern.

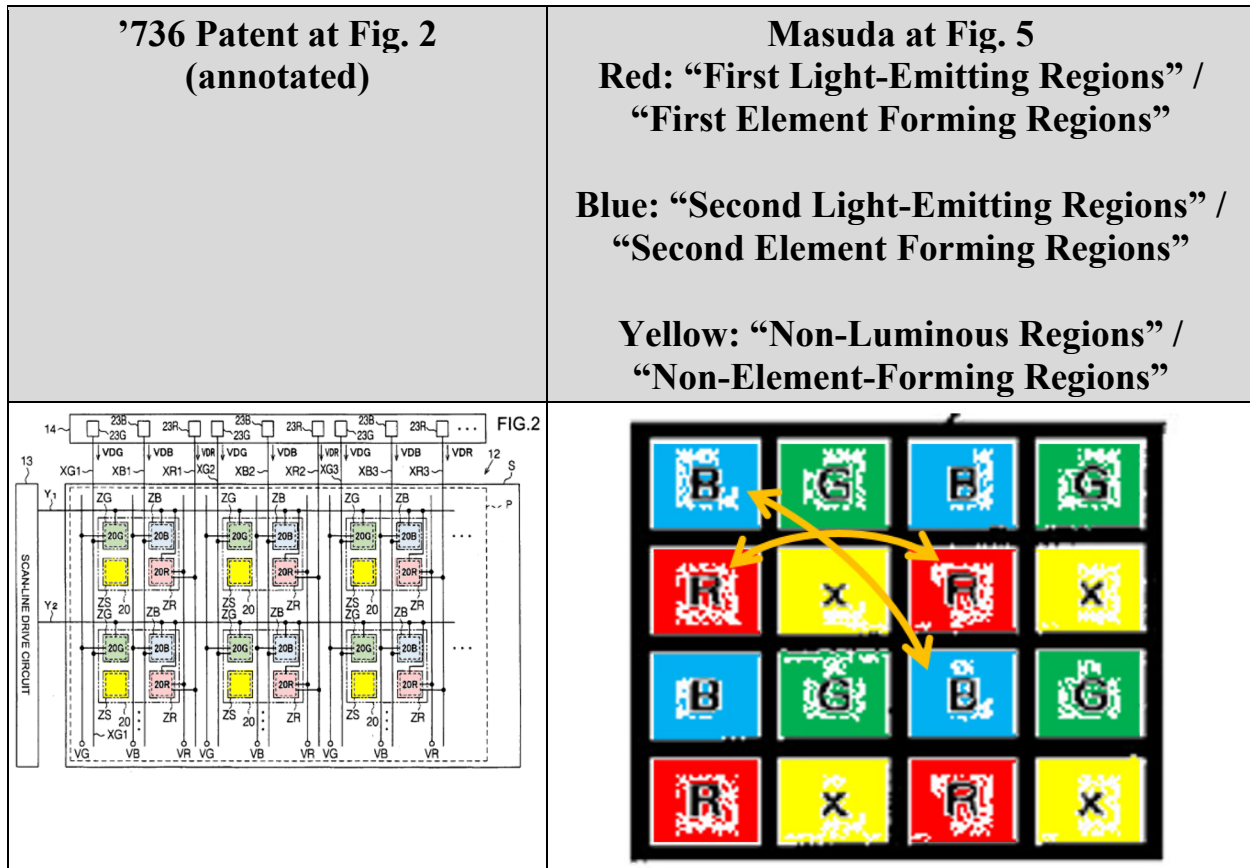
107. Additionally, the Kimura-Masuda combination renders obvious that those non-luminous / non-element-forming regions lack electro-optical elements and light-emitting films. *See supra* Ground 1, Claims 18 and 33. As shown by the

figure on the right-hand side of the table, in order to implement a “non-display” element, the OLED and its light-emitting film would have been omitted in the relevant region. Similar to my discussion above regarding Masuda alone, in the combination of Kimura with Masuda, a POSITA would have found it obvious to omit the OLED to ensure that “non-display” elements do not emit light, as intended. Moreover, a POSITA would have recognized that omitting this element would not increase cost.

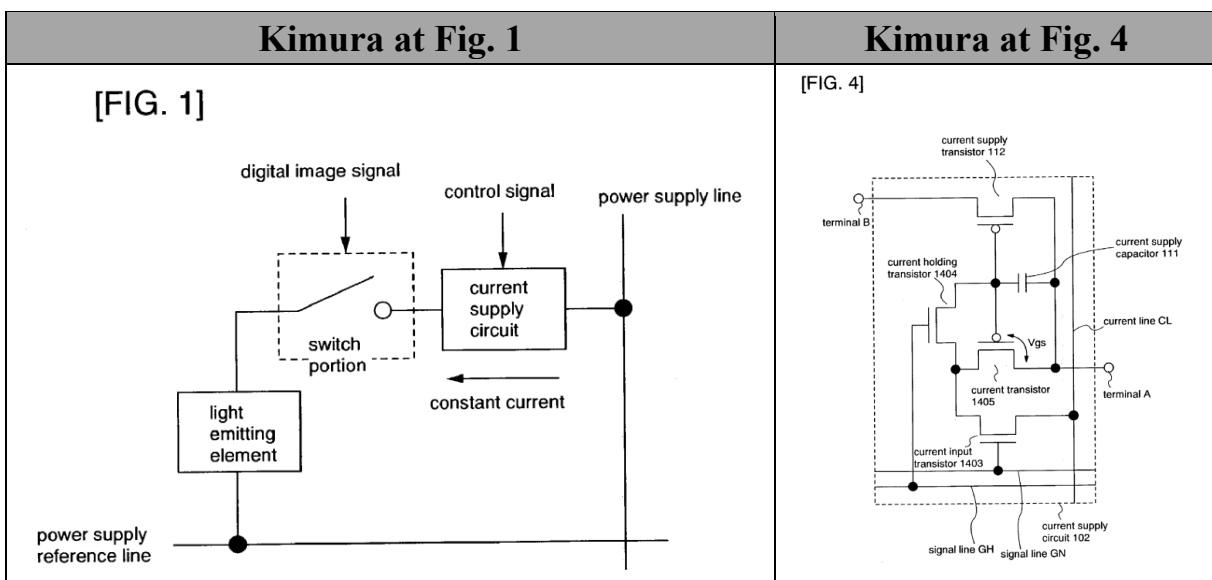
Masuda at Fig. 5 (non-display element)	Kimura Pixel Pattern of Fig. 53 Modified to Incorporate Teachings of Masuda
Non-Luminous Regions / Non-Element-Forming Regions 	

108. The Kimura-Masuda combination renders obvious that each of the whole non-luminous / non-element-forming regions would be sandwiched by two sets of light-emitting / element forming regions. *See supra* Ground 1, Claims 18 and 33. As shown by the annotated figures below, Masuda’s checkerboard pattern,

which as discussed above could be implemented using Kimura's OLED elements, features non-luminous / non-element-forming regions that are sandwiched by red light-emitting / element forming regions and blue light-emitting / element forming regions.



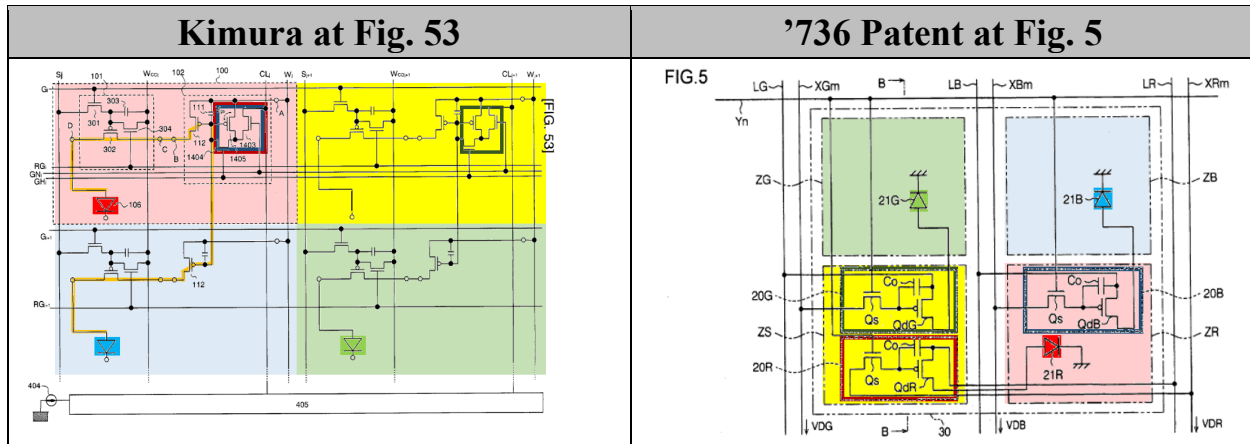
forming regions has an electronic circuit to drive the electro-optical element that is provided in another first or second element forming region.” As discussed above, Kimura discloses improved pixel driving circuitry that, in one embodiment, uses a current mirror method. *See* EX-1020 at [0179]-[0182], [1085]-[0191], Fig. 4. This method drives a pixel using a “current transistor 1405,” which generates current that is “mirrored” by a “current supply transistor 112.” *Id.* at [0185].



110. In one embodiment, the “current transistor 1405” is shared by two adjacent pixels in the same column. EX-1020 at [0468]-[0469]. As discussed earlier under the Overview of Kimura, Paragraph 78, at least this shared transistor constitutes a “circuit” that drives both pixels, but is only located in the light-emitting / element forming region that has one of the pixels. In other words, this shared transistor “control[s] light emission” of both the first (red) and second (blue) light-

emitting films per claim 23. In yet other words, this shared transistor and accompanying transistors 1403 and 1404 “drive” the first (red) and second (blue) electro-optical elements per claim 35.

111. Kimura’s figure 53 has been annotated below to show how its pixel array would implement Masuda’s pattern and to show that the blue electro-optical element and the red electro-optical element share current transistor 1405 along with transistors 1403 and 1404 (indicated by the red and blue concentric squares). Orange shows the path by which current generated by that current transistor 1405 drives both the blue and red electro-optical elements. As also shown in that annotated figure, the current transistor 1405 resides in the red light-emitting / element forming region. This matches the salient features of the ’736 patent’s second embodiment, in the sense that in both figures, one light-emitting / element forming region contains circuitry that drives the light-emitting film/electro-optical element in another light-emitting / element forming region as shown by the annotated version of ’736 patent figure 5 shown below. In Kimura figure 53, the red region has the circuitry that drives the blue region’s electro-optical device. In the ’736 patent figure 5, the red region has the circuitry that drives the blue region’s electro-optical device.



112. Kimura states that sharing this transistor “makes it possible to reduce in number transistors and signal lines per pixel” thereby achieving “a display device having high aperture ratio.” *Id.* The '736 patent's second embodiment allegedly provides the same benefit. *See* EX-1001 at 13:52-53 (alleging that arranging the pixel circuit's “formation positions” in the manner shown in figure 5 allows the “aperture ratios in the green pixel forming region ZG and the blue pixel forming region ZB” to be increased).

XI. CONCLUSION

113. I reserve the right to supplement my opinions to address any information obtained, or positions taken, based on any new information introduced throughout this proceeding.

114. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements are made with the

knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both (under Section 1001 of Title 18 of the United States Code).



By: _____

David K. Liu, Ph.D.

July 7, 2023

APPENDIX A

DAVID KUAN-YU LIU, Ph.D.

42063 Benbow Drive, Fremont, CA 94539 • (510) 770-9449 or (510) 579-5029

www.davidkyliu.com davidkyliu@comcast.net

PROFESSIONAL PROFILE

- Technical expert with over 20 years of industrial experience in the development of advanced CMOS devices and process technology, with special emphasis on non-volatile semiconductor memory devices and process technology, and high-voltage semiconductor devices, with additional 12 years of experience serving as expert consultant.
 - Named inventor on 99 US patents.
- Consultant and expert witness for past 15 years in semiconductor intellectual property evaluation and patent litigation, with deposition experience and successful ITC trial testifying experience.
- Successful track record in transitioning products from development phase to high-volume manufacturing phase, both as an individual contributor and as manager/director.
- Co-founder of an LLC in the development and licensing of intellectual property with emphasis on embedded flash memory technology.
- Co-founder of a semiconductor memory start-up company (Progressant Technologies, Inc.); participated in its successful sale to Synopsys, Inc.
- Fluent in Mandarin Chinese (native language) and English; over 10 years experience as real-time translator of church sermons and proficient in written translation.

EDUCATION

Stanford University, Palo Alto, California

Ph.D., Electrical Engineering (1989)

Thesis: Physics and Technology of Novel Conductivity-Modulated Power MOSFET's

M.S., Electrical Engineering (1985)

Coursework in integrated-circuit technology, semiconductor device physics, computer modeling of semiconductor devices and fabrication processes, and solid-state physics

University of California, Berkeley, California

B.S., Electrical Engineering (1983)

Certificate of Distinction (awarded annually to the top EECS graduate)

KEY EXPERT WORK EXPERIENCE:

Case:	Netlist, Inc. vs. Samsung Electronics Co. Ltd. et al.,
Jurisdiction:	Civil Action No. 2:21-cv-00463 Eastern District of Texas
Work Product:	Expert relating to memory modules.
Nature of Case:	Civil action.
Counsel:	Retained by Fish & Richardson (Contact: Tony Nguyen)
Date:	8/22 – Current

Case: **Vervain, LLC vs. *Micron Technology* & related IPR Petition**
Jurisdiction: Action No. 6:21-cv-00487-ADA
Western District of Texas
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 4 patents, all 4 petitions instituted, and deposed on both initial declaration and reply declaration.
Counsel: Retained by Orrick, Herrington & Sutcliffe LLP (Contact: Jared Bobrow)
Date: 8/21 – Current

Case: **Monterey Research vs. *Qualcomm* PTAB Matter**
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Jones Day (Contact: David Cochran)
Date: 12/21 – Current

Case: ***Semiconductor Energy Laboratory Co., OLED Patent Matters***
Jurisdiction: Action No. 8:21-cv-00554-JAK-ADS
Central District of California
Work Product: Expert for infringement on 3 patents relating to OLED driver circuit and layout, responsibilities include source code viewing, GDS layers viewing, and claim charts review.
Nature of Case: Civil action.
Counsel: Retained by Fish & Richardson (Contact: Bryan Basso)
Date: 9/21 – 4/22

Case: ***Apple Inc. IPR Petition for U.S. Patents 6,622,108 & 6,807,505***
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Erise IP (Contact: Paul Hart)
Date: 8/21 – 9/21

Case: ***Texas Instruments IPR Petition***
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: Josh Griswold)
Date: 9/20 – 4/21

Case: ***Micron Technology vs. UMC/JinHua***
Jurisdiction: Case No. 4:17-CV-06932-MMC
United States District Court for the Northern District of California
Work Product: Testifying expert, trade secret documents review, and declaration submission.
Nature of Case: Trade secret contention of Micron confidential documents.
Counsel: Retained by Jones Day (Contact: Randy Kay)
Date: 3/17 – Current

Case: ***SK Hynix vs. BitMicro***
Jurisdiction: Investigation No. 337-TA-1097
United States International Trade Commission
Work Product: Testifying expert for non-infringement on 2 patents, issued expert rebuttal report, deposition taken, issued witness statement.
Nature of Case: ITC infringement case concerning module stacking of SDRAM.
Counsel: Retained by Fish Richardson (Contact: Joseph Colaanni)
Date: 11/18 – 4/19

Case: ***Rohm Company IPR Petition***
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: Matt Colvin)
Date: 4/18 – 8/18

Case: ***Apple Inc., vs. Qualcomm Incorporated***
Jurisdiction: Case No. 3:17-CV-02402
United States District Court for the Southern District of California
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration, 2 depositions taken.
Counsel: Fish & Richardson (Contact: Tony Nguyen)
Date: 1/18 – 5/19

Case: ***Macronix vs. Toshiba***
Jurisdiction: Investigation No. 337-TA-1046
United States International Trade Commission
Work Product: Testifying expert for infringement and non-invalidity on 2 patents, claim construction analysis, technical tutorial, database viewing for evidence gathering, issuing expert report and expert rebuttal report, deposition taken for 2 patents, issued witness statement and rebuttal witness statement, testified in ITC court on both infringement and invalidity.
Nature of Case: ITC infringement case concerning advanced NAND Flash memory.
Counsel: Retained by Fish Richardson (Contact: David Barken)
Date: 4/17 – 10/18

Case: *Novatek Microelectronics Corp. IPR Petition*
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Kroub, Silbersher & Kolmykov PLLC (Contact: Sergey Kolmykov)
Date: 2/17 – 4/17

Case: *Taiwan Semiconductor Manufacturing Company IPR Petition*
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: John Goetz)
Date: 7/15 – 4/17

Case: *Triune Systems, LLC vs. Wayne Chen, et al.,*
Jurisdiction: Case No. 296-03209-2013,
District Court of Collin County, TX
Work Product: Testifying expert, database viewing, expert report, video-taped testimony
Nature of Case: Defending against trade secret contention.
Counsel: Retained by Gordon & Rees LLP (Contact: Robert Bragalone)
Date: 5/15 – 9/15

Case: *Macronix vs. Spansion*
Jurisdiction: Investigation No. 337-TA-922
United States International Trade Commission
Work Product: Testifying expert, claim construction analysis, technical tutorial, database viewing for evidence gathering, expert report, expert rebuttal report.
Nature of Case: ITC infringement case concerning Flash memory cell
Counsel: Retained by Fish Richardson (Contact: David Barken)
Date: 9/14 – 1/15

Case: *Macronix vs. Spansion*
Jurisdiction: Investigation No. 337-TA-909
United States International Trade Commission
Work Product: Database viewing for evidence gathering, support technical content of expert report, support technical content against rebuttal report.
Nature of Case: ITC infringement case concerning Flash memory cell
Counsel: Retained by Winston & Strawn (Contact Michael Murray)
Date: 5/14 – 1/15

Case: ***Keranos, LLC v. Analog Devices et. al.***
Jurisdiction: Civil Case No. 2:10-CV-00207
United States District Court for the Eastern District of Texas
Work Product: Claim Chart Generation and Claim Construction
Nature of Case: Patent infringement case concerning split gate Flash memory cell
Counsel: Retained by Agility IP (Contact Michelle Breit)
Date: 2/09 – 2/14

Case: ***Silicon Storage Technology, Inc. v. Xicor, LLC***
Jurisdiction: Civil Case No. CV 10-01515
United States District Court for the Northern District of California
Work Product: Expert report and declarations
Nature of Case: Matter concerning United States Reissue Patent RE38,370 on the process of flash memory cell.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 6/11 – 10/11

Case: ***Fast Memory Erase, LLC v. Spansion et.al.***
Jurisdiction: Civil Case No. 3:10CV-481
United States District Court for the Northern District of Texas
Work Product: Declarations
Nature of Case: Defending Motion for Attorney Fees.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/10 – 6/10

Case: ***Fast Memory Erase, LLC v. Spansion et.al.***
Jurisdiction: Civil Case No. 3-08cv0977M
United States District Court for the Northern District of Texas
Work Product: Testifying expert: issuing expert report, declarations, and deposition taken.
Nature of Case: Patent infringement case concerning minimizing source current during erase of Flash memory cell.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/09 – 5/10

EXPERIENCE:

10/07 to present: **Technical Consultant/Expert Witness**

Serving as a technical consultant and advisor in the area of semiconductor device and process technologies. Expert witness in ITC cases and district court cases, with successful testifying experience in trial hearing. Depositions taken at least 6 times for both litigation cases and IPR petitions. Experienced in source code viewings of circuit schematics and GDS layouts; seasoned in reverse engineering of integrated circuits, as well as techniques for de-processing and analyzing semiconductor chips. Responsibilities including gathering and reviewing of evidence, issuing declaration on claim construction, giving technical tutorial, issuing expert report and expert rebuttal report. Technical consultant for evaluating numerous flash memory and CMOS image sensor patent portfolios for licensing and acquisition consideration. Assessed qualitative merits of each patent portfolio and identified potential infringers and potential licensees. Generated numerous claim charts against potential infringers based on published patents, technical papers and datasheets, and reverse engineering reports.

10/07 to 4/11: **Jonker, LLC**

Inventor and Partner. Developed an intellectual property (IP) portfolio (7 U.S. patents granted and 3 U.S. patent applications pending) on zero-cost CMOS-logic-compatible embedded flash memory. Successfully negotiated the acquisition of this IP portfolio by a major semiconductor company.

8/04 to 10/07: **Maxim Integrated Products, San Jose, California**

Senior Scientist. Responsible for developing embedded non-volatile memory process technology for battery management products. Duties included supervising the development of integrated process flows at the 0.35 μ m and 0.18 μ m CMOS technology nodes. Analyzed and solved process-related reliability issues.

5/00 to 8/04: **Xilinx, Incorporated, San Jose, California**

Senior Manager. Responsible for developing non-volatile memory process technology for flash and CPLD products, as well as advanced CMOS process technology (75nm node). Duties included supervising the development of integrated non-volatile memory process flows at multiple CMOS technology nodes to meet product application requirements. Analyzed and solved process-related reliability issues.

2/00 to 5/00 **Progressant Technologies, Fremont, California**

Co-Founder. Facilitated IP development and sale of the company to Synopsys, Inc.

9/98 to 2/00

Programmable Silicon Solutions, Sunnyvale, California

Director of Process Engineering. Responsible for developing a fully logic compatible embedded flash memory technology for WSMC (a semiconductor foundry). Developed a new integrated process flow to implement a proprietary flash cell in a high-performance logic process, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement. Applied interpersonal skills to align the goals of the foundry technology development group to that of PSS. Participated in the strategic planning of a technology roadmap and foundry strategy for the company.

9/97 to 9/98

AMIC Technology, Santa Clara, California

Director of Flash Technology. Responsible for developing 0.35μm ETOX-based flash memory technology. Prepared the business plan and technology roadmap. Developed a new integrated process flow, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement.

5/96 to 9/97

Altera Corp., San Jose, California

Device Engineering Manager. Responsible for technology development, process integration, and foundry interface for 0.35μm generation of logic and EEPROM programmable logic device technology. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, and product yield enhancement.

7/95 to 5/96

Information Storage Devices, San Jose, California

Technology Development Manager/Program Manager. Led a project team of 10 in technology development, process integration, and first product introduction, with a new foundry. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, resolution of sorting issues and yield enhancement.

5/92 to 7/95

Advanced Micro Devices, Sunnyvale, California

Member of Technical Staff. Led the development of low-energy/DINOR-type flash EPROM technology. Key individual contributor in optimizing the process and design of flash cell and periphery devices in AMD's 0.5μm and 0.35μm flash EPROM technologies. Duties included process integration, device modeling, and development of triple-well technology and high-voltage transistors for negative gate erase operation.

1/89 to 4/92

Texas Instruments, Dallas, Texas

Member of Technical Staff. Research and development of 16Mb generation of flash EPROM technology, as well as a new generation of antifuse-based FPGAs. Duties included process integration, device modeling, high-voltage CMOS process integration, and investigation of a novel source-side injection mechanism for EPROM channel hot-electron programming.

AWARDS/HONORS

U.C. Berkeley Certificate of Distinction Award, 1983

AEA Faculty Development Fellowship, 1983-1985

AMD Spotlight Award, 1995

PATENTS

1. U.S. Patent 5,106,773, "Programmable Gate Array and Methods for Its Fabrication" (with K.-L. Chen and H. Tigelaar), issued April 21, 1992.
2. U.S. Patent 5,166,557, "Gate Array with Built-in Programmable Circuitry" (with K.-L. Chen), issued November 24, 1992.
3. U.S. Patent 5,202,576, "Asymmetrical Non-Volatile Memory Cell, Arrays, and Methods for Fabricating the Same" (with M. Wong), issued April 13, 1993.
4. U.S. Patent 5,219,782, "Sublithographic Antifuse and method for Manufacturing" (with K.-L. Chen), issued June 15, 1993.
5. U.S. Patent 5,250,464, "Method of Making a Low Capacitance, Low Resistance Sidewall Antifuse Structure" (with M. Wong), issued October 5, 1993.
6. U.S. Patent 5,264,384, "Method of Making a Non-Volatile Memory Cell" (with C. Kaya), issued November 23, 1993.
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