

**UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD**

BOE TECHNOLOGY GROUP CO., LTD.,
BEIJING BOE DISPLAY TECHNOLOGY CO., AND
MOTOROLA (WUHAN) MOBILITY TECHNOLOGIES
COMMUNICATION CO., LTD.,
Petitioner

v.

ELEMENT CAPITAL COMMERCIAL COMPANY PTE. LTD,
Patent Owner.

IPR2023-01178
U.S. PATENT NO. 7,259,736

DECLARATION OF DR. ARIS SILZARS

Declaration

I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

By: 
Aris Silzars, Ph.D.

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I, Dr. Aris Silzars, do hereby declare:

1. I am making this declaration at the request of Element Capital Commercial Company PTE. LTD in the matter of the BOE Technology Group Co., Ltd., Beijing BOE Display Technology Co., and Motorola (Wuhan) Mobility Technologies Communication Co., Ltd., petition for *inter partes* review of IPR2023-01178.

2. I am being compensated for my work in this matter at my standard hourly rate of \$350 for consulting services. My compensation in no way depends on the outcome of this proceeding or the content of my testimony.

3. In preparing this Declaration, I considered the following materials:

- (a) U.S. Patent No. 7,259,736 (“’736 patent”) (EX-1001);
- (b) Excerpts from the Prosecution History of the ’736 Patent (“Prosecution History”) (EX-1002)
- (c) Declaration of Dr. David K. Liu (EX-1003)
- (d) U.S. Patent No. 5,831,699 (“Wright”) (EX-1004)
- (e) Prosecution History of JP2002-348622 (“Foreign Counterpart Prosecution History”) (EX-1005)
- (f) Certified Translation of Pages 1-10, 50-58 from the Foreign Counterpart Prosecution History (EX-1006)

- (g) Certified Translation of Pages 63-79 from the Foreign Counterpart Prosecution History (EX-1007)
- (h) JPH11185654A (“Masuda”) (EX-1008)
- (i) Certified Translation of Masuda (EX-1009)
- (j) JP2002-278504A (“Inoue”) (EX-1010)
- (k) Certified Translation of Inoue (EX-1011)
- (l) KR960012168A (“Kwon”) (EX-1012)
- (m) Certified Translation of Kwon (EX-1013)
- (n) Sarma et al., “Flat Panel Displays for Portable Systems,” 13 *Journal of VLSI Signal Processing Systems* 165-190 (1996) (EX-1014)
- (o) Complaint, *Element Capital Commercial Company PTE. Ltd. v. BOE Technology Group Co., Ltd. et al.*, Case No. 2:22-cv-0118-JRG (EDTEX) (EX-1015)
- (p) U.S. Patent Application Publication No. 2003/0090447 (“Kimura”) (EX-1020)
- (q) The Petition filed by the Petitioner.
- (r) Certificate of Correction of U.S. Patent No. 7,259,736 (EX-2004)

- (s) Ernst Lueder, “Liquid Crystal Displays: Addressing Schemes and Electro-Optical Effects,” 161-245 (2001) (EX-2005)
- (t) Jiun-Haw Lee, et al., “Introduction to Flat Panel Displays,” 233-254 (2008) (EX-2006)
- (u) Amal Ghosh, et al., “Short Course S-1: Fundamentals of OLEDs,” 63-81 (2004) (EX-2007)
- (v) Achintya K. Bhowmik, et al., “Mobile Displays: Technology and Applications,” 39-43 (2008) (EX-2008)
- (w) Ernst Lueder, “Fundamentals of Passive- and Active-Addressed Liquid-Crystal Displays,” 13 (1998) (EX-2009)
- (x) Louis D. Silverstein, “Color in Electronic Displays,” 75-77 (1999) (EX-2010)

I. Professional Background

4. Information concerning my professional qualifications, experience, and publications, and the matters in which I have served as an expert, are set forth in my current curriculum vitae (EX-2003).

5. I received my Bachelor of Arts degree in Physics in 1963 from Reed College in Portland, Oregon. I received my Master of Arts degree in Physics in 1965

from the University of Utah. I received my Doctoral degree in Electrical Engineering in 1969 from the University of Utah.

6. I have been an active participant in the development of display device technologies and products that use displays since 1974. I have managed research groups as large as 350 technologists in creating and implementing display device technologies and high performance electronic circuits into products based on these technologies.

7. I have participated in numerous technical conference activities (including Program and General Chair of the International Society for Information Display symposium – the preeminent annual international conference on display technology) and made numerous presentations on display applications and on the technology evolution of those products. I was President of the Society for Information Display (“SID”) from 2000 to 2002. With over 7000 members, SID is the premier organization for professionals and academics in the fields of display research, design, manufacturing, applications, standards development, and marketing.

8. Since 1995, I have been an independent industry consultant with a broad client base and continue to be active and knowledgeable regarding all new display device-related technologies. My area of expertise encompasses the fields of

information display technology, liquid crystal, OLED, and LED displays, digital integrated circuits and systems, mechanical design, and packaging for electronic products and semiconductor technology.

9. I have authored over 100 publications, most related to display device technology. I am also a named inventor on seventeen patents, most of which are related to or in the field of display device technology. In my many years of engineering, manufacturing, and product development experience, I have personally been involved in the design of large segmented LED displays, including obtaining three patents on which I am a co-inventor.

II. '736 Patent Technologies

10. Below I describe the state of display device technology as of the '736 patent's filing date, and summarize the development of technologies underlying the features recited in claims 23 and 35 of the '736 patent.

11. There are three distinct methods for operating two-dimensional (flat panel) displays. *See* EX-2005 at 3-5. They differ in their structure and in their function. *See* EX-2005 at 3-5. The technologies and design methods used for one are not readily transferable to the others. The three types are characterized by how the individual elements (cells) are stimulated – addressed. *See* EX-2005 at 3-5. In

other words, they are characterized by how the light emitting material is controlled to change the brightness of each segment or cell.

12. The simplest is known as segment addressed. *See, e.g.*, EX-2005 at 3. This type of display is characterized by a direct electrical connection to each pixel. *See* EX-2005 at 3. These displays are typically used for clocks and other limited information applications. Segmented displays are limited in complexity by the number and density of wiring interconnections that can be accommodated on the substrate. *See* EX-2005 at 3.

13. The next level of complexity and information content is provided by what are called passive matrix displays. *See, e.g.*, EX-2005 at 3-4; EX-2007 at 11-15. These displays have rows and columns and are addressed by briefly stimulating each cell to change its light emission characteristics. *See* EX-2005 at 3-4; EX-2007 at 11-15. After a particular cell is stimulated it may have an extended relaxation time to hold the image while the other cells are being addressed.

14. The third and most complex type of flat-panel display is known as active matrix displays. *See, e.g.*, EX-2005 at 4-5; EX-2007 at 11-15. That is the technology that is described in the '736 patent and that is the addressing method used in essentially all higher resolution and larger screen size flat panel displays.

15. The figures below are schematic illustrations for describing passive matrix addressing (FIG. A) and active matrix addressing (FIG. B). EX-2005 at FIGS. 10.2 and 10.3.

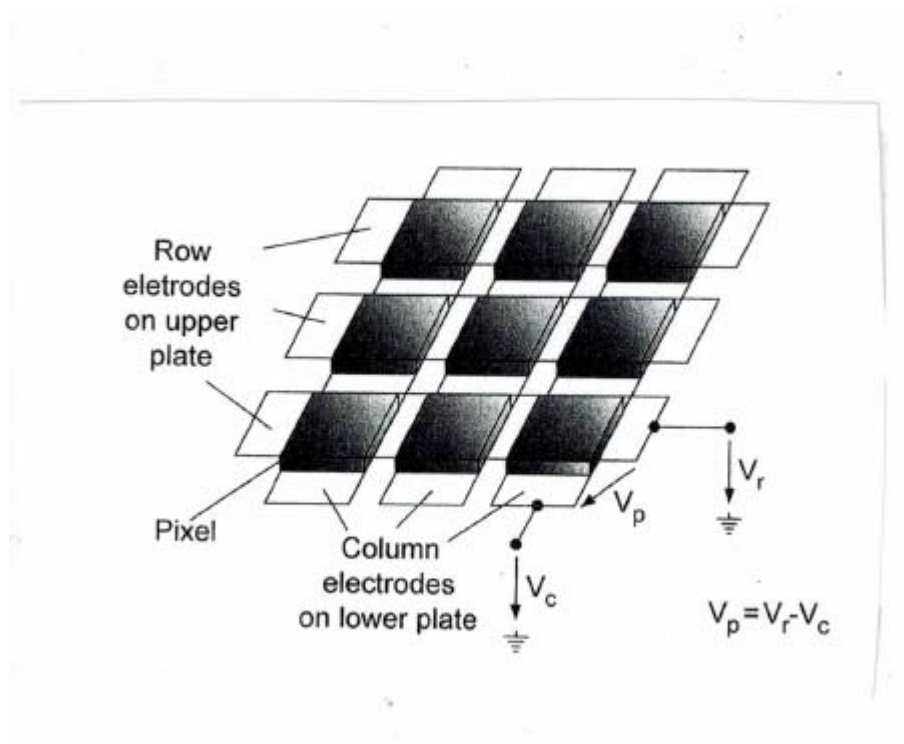


FIG. A (Passive Matrix)

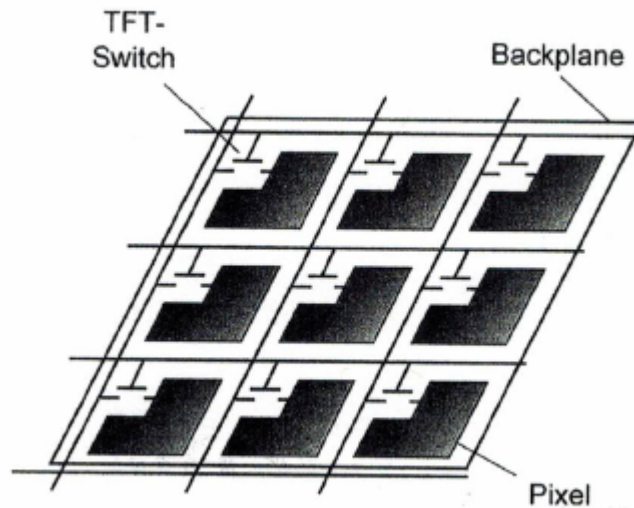


FIG. B (Active Matrix)

16. Passive matrix displays require a structure that places the rows on one substrate and the columns on an opposite substrate. *See* EX-2005 at 3-4. Both rows and columns have varying voltages applied in a particular time sequence to address the cells. *See* EX-2005 at 3-4; EX-2007, 12. There is no common electrode. *See* EX-2005 at 3-4. On the other hand, in an active matrix display there is a common electrode on one substrate while all of the active addressing circuitry is placed on an opposing substrate. *See* EX-2005 at 6-7. All the row and column connections in an active matrix display are thus on one substrate with only a common voltage reference is on the opposing substrate. *See* EX-2005 at 6-7. As a result, the structure and

method of operation are entirely different for these two types of LC displays and the methods used to design and manufacture one type are not readily applicable to the other.

17. The need to have rows on one substrate and columns on another for the passive matrix displays has yet other consequences in how the conductive patterns are placed as compared to active matrix displays. In a passive matrix display, the row and column conductors are integral with the pixel electrodes, i.e. there are no intervening elements. *See* EX-2005 at 4. In contrast, in an active matrix display, the pixel electrodes are isolated from the row and column addressing lines by thin film transistors (TFTs) placed in the area of each pixel that does not interfere with the light emission. *See* EX-2005 at 6-7. The row and column electrodes for addressing the pixels are placed in the narrow spaces between the pixels or underneath the emitting areas. *See, e.g.,* EX-2005 at 6-7. Thus, the location, width, and constituent materials of the rows and columns are substantially different in an active matrix display. Furthermore, an active matrix display has a supplemental capacitor for each pixel. *See* EX-2005 at 6-7. These capacitors are used to store additional charge and provide stability and emission uniformity for the display. *See* EX-2005 at 6-7. Such capacitors are not used in passive matrix displays. *See, e.g.,* EX-2007 at 11-13.

18. Because the active matrix displays use thin-film transistors and supplemental capacitors, the cell response is proportional to the total charge that is placed at each pixel location during the addressing period. Since passive matrix displays do not have such a charge storage mechanism, they are more susceptible to variations in electrode resistance and the voltage drops that can be introduced by such resistance variations.

19. Additionally, since passive matrix displays do not have a charge storage capability, there is a major limitation in the visual performance that can be achieved as compared to active matrix displays. Both passive and active matrix displays are addressed by the sequential scanning of the rows while charge is supplied to each pixel by the columns. The number of rows (resolution) that must be scanned determines the amount of time available in each frame to provide the electrical charge to each pixel. For example, for a 1,000 row display, the charging time per row is $1/1,000$ of the frame time duration.

20. In a passive matrix display, once this charge has been provided, the only way to retain the image for the rest of the frame is by the relaxation time of the emission control material. In an LCD display that would be the relaxation time of the liquid crystal material itself. In an FED, it would be the decay time of the phosphor screen. This results in the image fading as other rows are addressed.

21. On the other hand, in an active matrix display, when a row is active and the charge is supplied from the column electrodes, there is a gating transistor that turns on and off during the charging period to retain the image. The charge that flows during this charging period is fed into the pixel and into a supplemental capacitor. *See, e.g.*, EX-2009 at 3. Once the brief charging period is complete, the gating transistor turns off and the charge on the pixel and supplemental capacitor are retained for the duration of the frame and the pixel continues to operate at the desired brightness level. There is no image decay as with a passive matrix display. The implementation of this storage mechanism has allowed for the development of high resolution full color displays that now dominate the market for nearly every application, such as large screen flat panel televisions, full color computer monitors, cell phones, and the like that produce highly readable images under various ambient conditions.

III. Relevant Legal Standards

22. I have been asked to provide my opinions as to whether claims 23 and 35 of the '736 patent would have been obvious to a person of ordinary skill in the art ("POSITA") at the time of the filing date of the '736 patent.

23. I am an engineer by training and profession. The opinions I express in this declaration involve the application of my technical knowledge and experience to the evaluation of certain prior art with respect to the '736 patent. In addition, I understand that the following legal principles apply.

24. It is my understanding that, in determining whether claims of the '736 patent are obvious in this proceeding, the claim terms are generally given their ordinary and customary meaning as understood by a POSITA. A POSITA would read the claim terms in the context of the entire patent specification in which they appear, as well as the prosecution history of the patent.

25. It is my understanding that a claim is anticipated under 35 U.S.C. § 102 if each and every element and limitation of the claim is found, either expressly or inherently, in a single prior art reference. I also understand that a reference must disclose all claimed elements as arranged in the claim, although identical terminology need not be used in the reference and claim elements.

26. It is my understanding that a claim is unpatentable under 35 U.S.C. § 103 if the claimed subject matter as a whole would have been obvious to a POSITA in the art at the time of the alleged invention. I also understand that an obviousness analysis takes into account the scope and content of the prior art, the differences

between the claimed subject matter and the prior art, and the level of ordinary skill in the art at the time of the invention.

27. In determining the scope and content of the prior art, it is my understanding that a reference is considered relevant prior art if it falls within the field of the inventor's endeavor. In addition, a reference is prior art if it is reasonably pertinent to the particular problem with which the inventor was involved. A reference is reasonably pertinent if it logically would have commended itself to an inventor's attention in considering his problem. If a reference relates to the same problem as the claimed invention, that supports use of the reference as prior art in an obviousness analysis.

28. To assess the differences between prior art and the claimed subject matter, it is my understanding that 35 U.S.C. § 103 requires the claimed invention to be considered as a whole. This "as a whole" assessment involves showing that one of ordinary skill in the art at the time of invention, confronted by the same problems as the inventor and with no knowledge of the claimed invention, would have selected the elements from the prior art and combined them in the claimed manner.

29. It is my further understanding that several rationales may be applied for combining references or modifying a reference to show obviousness of claimed

subject matter. These rationales include: combining prior art elements according to known methods to yield predictable results; simple substitution of one known element for another to obtain predictable results; a predictable use of prior art elements according to their established functions; applying a known technique to a known device (method or product) ready for improvement to yield predictable results; choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify a prior art reference or to combine prior art teachings to arrive at the claimed invention.

IV. Person of Ordinary Skill in the Art

30. It is my understanding that when interpreting the claims of the '736 patent, I must do so based on the perspective of one of ordinary skill in the art at the relevant priority date. My understanding is that the earliest claimed priority date of the '736 patent is November 29, 2002.

31. It is my opinion that one of ordinary skill in the art in the field of display device technology in the 2002 time period, would have had at least a Master's degree in electrical engineering, physics, or a related field, and at least two years of relevant work experience in the field of display device technology. Additional education can remedy lack of work experience and vice versa.

32. I am a person of at least ordinary skill in the art and was so at the time of the invention of the '736 patent.

V. Overview Of The Subject U.S. Patent No. 7,259,736

33. The '736 patent was assigned to Seiko Epson Corporation, the principal named inventor is Hayato Nakanishi. The patent is titled "Electro-Optical Device, Active-Matrix Substrate, and Electronic Apparatus."

34. The '736 patent is directed towards an electro-optical device that is an active matrix, organic light-emitting diode ("OLED") display. In particular, the '736 patent aims to reduce image distortions and color irregularities caused by directional viewing variations that occur in active matrix OLED displays due to pixel circuits having different shapes and/or different pitches in the column direction (data-line direction) and the row direction (scan-line direction) of a display panel portion. *See* EX-1001 at col. 1, lines 23-24.

35. As described in the "Background of the Invention" section of the '736 patent, active matrix displays include a display panel that has a plurality of pixels arranged in a matrix, where each of the pixels has a respective pixel circuit including electro-optical elements and driving transistors. When the pixel circuits have different shapes and/or pitches in the column and row directions of the display, directional viewing variations may occur which results in image distortions and

color irregularities. Example relevant portions of the '736 patent are reproduced below:

One type of driving system for a related art display having liquid-crystal elements, organic EL (electroluminescent) elements, electrophoresis elements, electron emitting elements, or the like is an active matrix drive system. An active-matrix drive system display includes a display panel that has a plurality of pixels in a matrix. The pixels have respective pixel circuits, each of which is constituted by electro-optical elements and driving transistors for supplying drive power to the electro-optical elements.

EX-1001 at 1:11-22.

When the pixel circuits have different shapes and/or different pitches in the column direction (data-line direction) and the row direction (scan-line direction) of the display panel portion, directional viewing variation occurs between the column direction and the row direction of the display panel. As a result, an image displayed on the display panel portion may be distorted in the column direction (data-line direction) or the row direction (scan-line direction). In particular, for a full-color

display, color irregularities occur in addition to the distortion of the image in the column and row directions. Thus, the display quality of the display is reduced.

EX-1001 at 1:23-34.

36. In order to achieve reduced image distortions and color irregularities caused by directional viewing variations, the '736 patent discloses an arrangement where, for each pixels, a dummy forming region is provided together with the red, green, and blue pixel forming regions in a square lattice. Specifically, the dummy forming region is a region that is a non-light emitting region, while the red, green, and blue pixel forming regions are regions that comprise organic EL elements for emitting light in red, green, and blue colors, respectively. Example relevant portions of the '736 patent are reproduced below:

As shown in FIG. 3, in a region where each pixel circuit 20 is formed, a pixel forming region ZG for green, a pixel forming region ZB for blue, a pixel forming region ZR for red, and a dummy forming region ZS are provided in a square lattice. The green pixel forming region ZG has the green pixel circuit 20G and the organic EL element 21G therein emits green light. The blue pixel forming region ZB has the blue pixel circuit

20B and the organic EL element 21B therein emits blue light. The red pixel forming region ZR has the red pixel circuit 20R and the organic EL element 21R therein emits red light. In the dummy forming region ZS, none of the pixel circuits 20G, 20B, and 20R is formed, but an anti-reflection member made of black polyimide or the like is formed in this exemplary embodiment. Thus, black is displayed in the dummy forming region ZS. Thus, the formation of the dummy forming regions ZS can ensure that black is displayed on the display panel portion 12. As a result, the contrast ratio of the display 10 can be enhanced.

EX-1001 at 7:58-8:8.

37. In order to reduce the directional viewing variations, the dummy forming regions are arranged so as to be sandwiched by the green pixel forming regions in the vertical direction (column direction), and to be sandwiched by the red pixel forming regions in the horizontal direction (row direction). Example relevant portions of the '736 patent are reproduced below:

With regard to the arrangement of the forming regions ZG, ZB, ZR, and ZS (pixel circuits 20G, 20B, and 20R) allotted in a square lattice in this exemplary embodiment ... That is, except for the pixel circuits 20 that

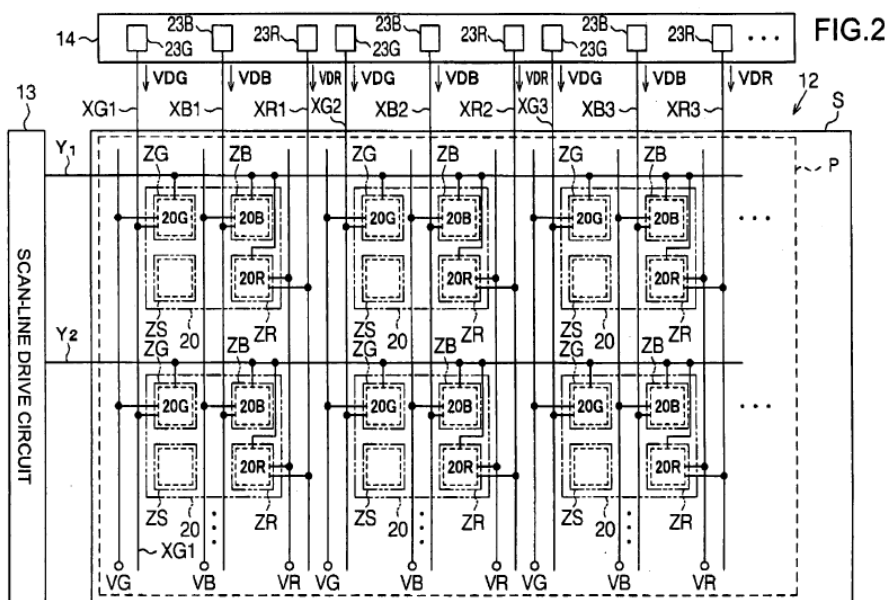
are located at the top, bottom, left, and right edges, the dummy forming regions ZS of the pixel circuits 20 are arranged so as to be sandwiched by the green pixel forming regions ZG in the vertical direction (column direction). The dummy forming regions ZS are also arranged so as to be sandwiched by the red pixel forming regions ZR in the horizontal direction (row direction). The green pixel forming region ZG, the blue pixel forming region ZB, the red pixel forming region ZR, and the dummy forming region ZS, which are formed in a square lattice, constitute one pixel region. As a result, the green, blue, and red organic EL elements 21G, 21B, and 21R can be arranged in regular directions and at regular intervals in the column and row directions of the display panel portion 12. Thus, this arrangement can reduce directional viewing variation that occurs between the column direction and the row direction of the display panel portion 12, which makes it possible to suppress the distortion of an image displayed on the display panel portion 12.

EX-1001 at 8:19-47.

The display 10 of this exemplary embodiment can provide the following advantages. (1) In this exemplary embodiment, in each pixel region of the display panel portion 12, the green pixel forming region ZG having the green pixel circuit 20G including the green organic EL element 21G, is allotted to the upper left side, and the blue pixel forming region ZB having the blue pixel circuit 20B including the blue organic EL element 21B, is allotted to the upper right side. Also, the dummy forming region ZS that does not have any of the color pixel circuits but has the anti-reflection member, is allotted to the lower left side, and the red pixel forming region ZR having the red pixel circuit 20R including the red organic EL element 21R, is allotted to the lower right side. Further, in the adjacent pixel circuits 20, except for the pixel circuits 20 that are located at the top, bottom, left, and right edges, the green pixel forming regions ZG, the blue pixel forming regions ZB, the red pixel forming regions ZR, and the dummy forming regions ZS are arranged in a positional relationship in which another forming region is provided between two adjacent same-color forming regions. Thus, since two adjacent same-color organic EL elements 21G, 21B, and 21R are arranged at regular intervals in the column and row directions with

one forming region interposed therebetween, it is possible to reduce directional viewing variation that occurs between the column direction and the row direction of the display panel portion 12.

EX-1001 at 12:41-67.



EX-2004 at FIG. 2; *see also* FIGS. 3 and 5.

VI. Prosecution History of the Subject U.S. Patent No. 7,259,736

38. I have reviewed the file history of U.S. Patent Application No. 10/712381 (the “Patent Application”), from which the ‘736 patent issued.

39. The claims of the Patent Application were allowed after the Applicant filed an Amendment to specify aspects related to ineffective optical regions, non-luminous regions, and non-element forming regions in claims corresponding to

independent claims 3, 18, and 33 of the '736 patent. EX-1002 at 258-268 and 279. For example, the Examiner agreed during an interview that anticipation rejections under 35 U.S.C. § 102 would be withdrawn upon amending the claims to specify that each of the “whole” ineffective optical regions are arranged so as to be sandwiched by two of the first effective optical regions and so as to be sandwiched by two of the second effective optical regions. EX-1002 at 256 and 267. The Applicant then amended claims 3, 16, and 27 of the Patent Application to specify the “whole” feature. EX-1002 at 258-265 and 267.

VII. Summary of Alleged Prior Art

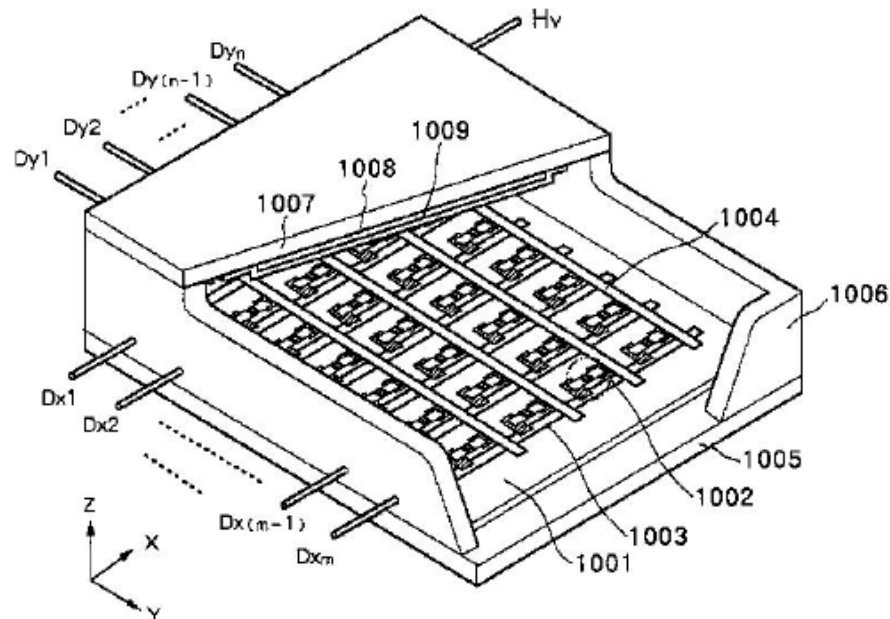
A. JPH11185654A

40. JPH11185654A (“Masuda”) is a Japanese patent application publication that published on July 9, 1999.

41. Masuda is directed towards passive matrix display panels that include field emission display technology. Specifically, the field emission display technology includes cold cathode elements, as parts of primary color display elements, that emit electrons to a fluorescent (e.g., phosphor) material to emit light to produce a color display. EX-1009 at [0001]-[0002], [0034], and [0042]; EX-2006 at 3-24.

42. Masuda describes that the cold cathode elements are to be particularly used as a multi-electron beam source, and that the cold cathode elements include surface conduction-type emitting elements, electric field emission-type elements (“FE-type”), and metal/insulating layer/metal-type emitting elements (“MIM-type”). EX-1009 at [0002], [0034], and [0042]. In other words, the field emission display technology of Masuda includes electron emitters of the surface conduction-type, the FE-type, or the MIM-type.

43. Referring to FIG. 4 of Masuda, reproduced below, the multi-electron beam source, implemented by the cold cathode elements (conduction-type emitting elements 1002) that are arranged in a matrix, are controlled to emit electrons towards a fluorescent film 1008 that is above the cold cathode elements and coated with fluorescent (e.g., phosphor) materials of the three primary colors of red, green, and blue. EX-1009 at [0033]-[0036]. The emitted electrons cause the fluorescent film to emit red, green, and/or blue light, thus implementing primary color display elements of pixels. EX-1009 at [0033]-[0036].

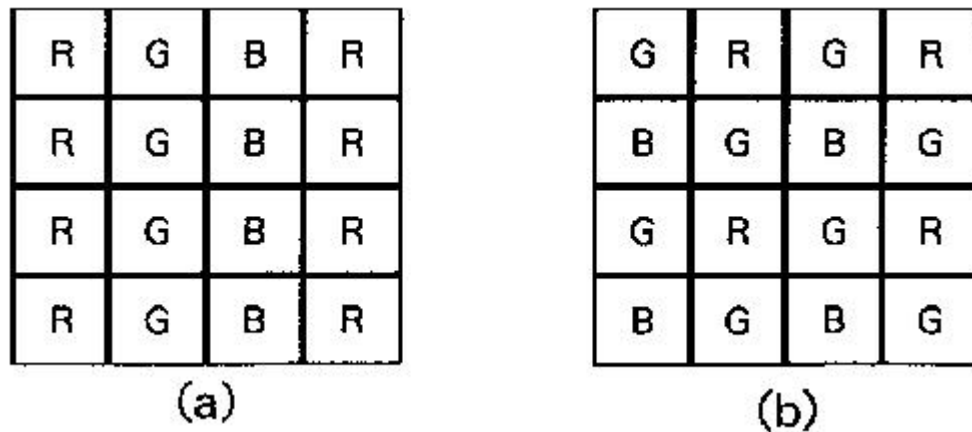


EX-1009 (“Masuda”) at FIG. 4

44. Masuda particularly aims to improve image quality and performance of passive matrix displays utilizing field emission display technology that include the cold cathode elements, as parts of color display elements, by arranging the color display elements in a particular checkerboard arrangement. EX-1009 at [0018].

45. Masuda contends that the checkerboard arrangements of FIG. 3 of Masuda, reproduced below, improve resolution but causes viewers to perceive visual interference of red and blue horizontal (or vertical) stripes on the display due to the red and blue display elements being lined up in a respective row (or column), thereby reducing image quality. EX-1009 at [0018]-[0019]. Further, Masuda contends that such an arrangement requires the green color output of green display elements to be

limited to half in order to achieve color balance, which limits the maximum performance of the display elements. EX-1009 at [0020].



EX-1009 (“Masuda”) at FIG. 3

46. Masuda contends that the visual interference of horizontal (or vertical) stripes is particularly caused by a difference in luminosity between rows (or columns) of the color display elements, which in turn, is caused by inherent luminosity differences between the different primary colors arranged in said rows (or columns) of the color display elements; green having a luminosity value of 0.59, red having a luminosity value of 0.30, and blue having a luminosity value of 0.11. EX-1009 at [0021]-[0022], [0026].

47. In an attempt to avoid such visual interference, Masuda describes that the passive matrix displays, which include the cold cathode elements as parts of the display elements, include a particular checkerboard arrangement in which a red color

display element, a green color display element, a blue color display element, and a non-display element are arranged in a repeated, two-row and two-column arrangement, with the two brightest colors (*i.e.*, Green (0.59) and Red (0.30)) being arranged at opposite corner positions as shown FIGS. 1-2 of Masuda, reproduced below. EX-1009 at [0022] and [0028]-[0030].

[FIG. 1]

B	G
R	x

EX-1009 (“Masuda”) at FIG. 1

[FIG. 2]

B	R
G	x

EX-1009 (“Masuda”) at FIG. 2

48. As shown above, in such two-row and two-column, checkerboard arrangements, the two primary color display elements that have the highest luminosity values (e.g., the red display element (R) and the green display element (G)) are in opposite corners from each other, which Masuda contends achieves a minimum value among maximum luminosity differences between columns and rows. EX-1009 at [0022] and [0028]-[0030]. By reducing the luminosity differences between the columns and rows, Masuda contends that the visual interference caused by horizontal stripes or vertical stripes is reduced. EX-1009 at [0021].

49. Notably, the field emission display technology in Masuda of using cold cathode elements to emit electrons to a fluorescent (e.g., phosphor) material to implement color display elements was never implemented in commercial display products, and such display technology can only include a small numbers of pixels since such display technology does not implement storing an image in one row while other rows are being addressed. Thus, a display implementing such display technology would have limited resolution. In addition, displays, if implementing the field emission display technology, would not be an active matrix display. The reason is that the tip of the emitter of cold cathode element pulls electrons in a highly nonlinear process. *See* EX-1009 at [0091]-[0092], [0095], FIG. 12.

B. US2003/0090447

50. US2003/0090447 (“Kimura”) is a United States patent application publication that published on May 15, 2003.

51. Kimura is directed towards an improvement to active matrix (“AM”) organic light emitting diode (“OLED”) displays of reducing variation in luminance of light emission of the active matrix OLED display by controlling electrical current flowing into a current supply circuit of the active matrix display. *See* EX-1020 at [0001]-[0084].

52. As noted in Kimura, active matrix OLED displays include a light emitting element and a transistor for controlling light emission of the light emitting element, where the active matrix OLED displays can utilize a voltage writing type analog method, a voltage writing type digital method, or a current writing type analog method to control the amount of current flowing in to the OLED in order to control the luminance of the OLED. EX-1020 at [0003]-[0004], [0008], [0015].

53. However, Kimura describes that active matrix OLED displays utilizing the voltage writing type analog method have problems of variation in luminance of the OLED due to (a) fluctuations in threshold voltage of the driving TFT or (b) variations in an amount of current actually flowing despite a constant voltage applied between two electrodes of the OLED due to changes in environment temperature,

degradation of the OLED, and the like. EX-1020 at [0010] (describing problems of the voltage writing type analog driving method), [0037] and [0041] (describing problems of the voltage writing type digital driving method).

54. Kimura notes that the current writing type analog driving method may instead be utilized in order to alleviate the above problems. EX-1020 at [0026], [0042], [0045]. However, Kimura further notes that active matrix OLED displays utilizing current writing type analog method have significant drawback of it being difficult to write a signal current quickly, having a strong possibility to emit light at an inaccurate luminance, and causing reduction in contrast. EX-1020 at [0046]-[0049], [0051].

55. More particularly, Kimura describes that active matrix OLED displays utilizing the current writing type analog method include a storage capacitor that is configured to hold electric charges/voltages. EX-1020 at [0046]. However, the process to hold a given level of electric charges in the storage capacitor takes longer as the signal current becomes smaller because of cross capacitance of wirings, which causes difficulty in writing a signal current quickly. Further, the small signal current increases the influence of noises, which increases the possibility that the light cannot be emitted at an accurate luminance. EX-1020 at [0046]-[0047]. In addition, Kimura

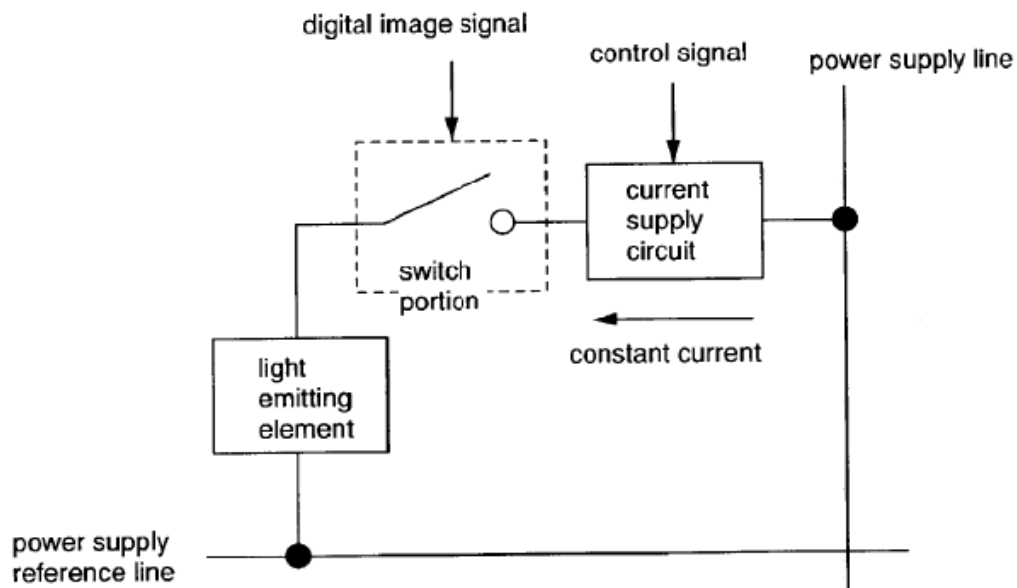
describes that active matrix OLED displays utilizing the current writing type analog method include a current mirror circuit and a pair of TFTs. EX-1020 at [0048]. However, the pair of TFTs may not have the same current characteristic in the current mirror circuit, which causes fluctuations in threshold voltage of the TFTs that leads to a reduction in contrast. EX-1020 at [0048]-[0049].

56. To avoid such issues, Kimura describes a configuration that involves at least one switch portion that is configured to switch between an ON state that allows for a constant current to flow to the light emitting element (i.e., OLED) to emit light and an OFF state that prevents the constant current from flowing into the light emitting element, based on a digital video signal. *See, e.g.*, EX-1020 at [0071]-[0077]. Since the switch portion(s) allow for the emission of light to be switched on and off by simply changing between ON and OFF states based on the video signal, signal current can be written more quickly. *See, e.g.*, EX-1020 at [0079]. Further, since the switch portion(s) allow for the current to be cut completely in the OFF state, accurate grey scale display can be obtained which improves the contrast. *See, e.g.*, EX-1020 at [0079].

57. Kimura describes that a basic structure of such configuration includes, for each pixel, a current supply circuit, the switch portion, and the light emitting

element as shown in Fig. 1 of Kimura (reproduced below). EX-1020 at [0070]-[0071].

[FIG. 1]



EX-1020 ("Kimura") at FIG. 1

VIII. Ground IB – Claims 23 and 35 Are Not Rendered Obvious Under 35

U.S.C. § 103 By Kimura In View Of Masuda

58. As discussed below, it would not have been obvious, before the effective filing date of the '736 patent, for a POSITA to modify the configuration of Kimura with the checkerboard pattern of Masuda to describe all features of claims 23 and 35 of the '736 patent.

59. For example, (1) Masuda is not analogous art of the '736 patent, (2) a POSITA would not have considered combining Kimura and Masuda, as the references describe significantly different and incompatible technologies, and Kimura already effectively achieves its purpose of reducing variation in luminance of light emission without having the problem indicated in Masuda of visual interference caused by horizontal stripes or vertical stripes, and (3) modification of Kimura in which the configuration for enabling a constant current to flow in a light emitting element of Kimura is replaced with the checkerboard pattern of Masuda would cause Kimura to be unsatisfactory for its intended purpose of reducing variation in luminance of light emission of an active matrix OLED display.

A. Masuda Is Not Analogous Art

60. The '736 patent and Masuda are not within the same field of endeavor because the '736 patent and Masuda are directed toward substantially and fundamentally different types of displays.

61. As explained above, Masuda is directed towards passive matrix display panels that utilize field emission display technology by including cold cathode elements, as parts of primary color display elements, that emit electrons into a vacuum enclosure to a fluorescent (e.g., phosphor) material to produce a color display. EX-1009 at [0001]-[0002], [0034], and [0042]. Specifically, Masuda is

directed to the field of endeavor of passive matrix displays utilizing such field emission display technology.

62. In contrast, the invention defined by claims 23 and 35 of the '736 patent are directed towards the field of endeavor of an active matrix display.

63. Specifically, active matrix displays are displays having electronic circuits that are in element forming regions and drive electro optical elements. For example, the '736 patent describes active matrix displays as follows:

An active matrix substrate according to an aspect of the present invention includes a plurality of element forming regions that are provided above a substrate and that have electrodes for connection with electronic elements, and a wiring region that is provided above the substrate and that has wires to supply various electrical signals to the electronic elements via the electrodes.

EX-1001 at 5:29-35.

In the active matrix substrate of an aspect of the present invention, each of the first and second element forming regions may have an electronic circuit to drive the first or second electro-optical element that is provided therein.

EX-1001 at 6:1-4.

In the active matrix substrate of an aspect of the present invention, at least one of the first element forming regions and the second element forming regions may have an electronic circuit to drive the electro-optical element that is provided in another first or second element forming region.

EX-1001 at 6: 10-14.

64. Claim 23 includes the feature of “at least one of the first and second light-emitting regions having an electronic circuit to control light emission of the first or second light-emitting film provided in another first or second light-emitting region,” which specifies that the invention defined by claim 23 includes an electronic circuit that is within a light-emitting region and controls a light-emitting film. Accordingly, the invention defined by claim 23 is directed towards the field of endeavor of an active matrix display.

65. Claim 35 includes the feature of “at least one of the first and second element forming regions has an electronic circuit to drive the electro-optical element that is provided in another first or second element forming region,” which specifies that the invention defined by claim 35 includes an electronic circuit that is within an element forming region and drives an electro-optical element. Accordingly, the

invention defined by claim 35 is directed towards the field of endeavor of an active matrix display.

66. The general structure and method of operation for passive matrix displays and active matrix displays are substantially different. Specifically, as mentioned previously, passive matrix displays require a structure that places the rows on one substrate and the columns on an opposite substrate, where rows and columns have varying voltages applied in a particular time sequence to address the cells without the use of common electrode. *See* EX-2005 at 3-4. On the other hand, active matrix displays require a structure that has all the row and column connections on one substrate, where a common electrode is used on one substrate while all of the active addressing circuitry is placed on an opposing substrate. *See* EX-2005 at 6-7.

67. The specific structures, such as the location, width, and constituent materials of the rows and columns for passive matrix displays and active matrix displays are also substantially different. Specifically, as mentioned previously, since the passive matrix displays require a structure that places the rows on one substrate and the columns on an opposite substrate, the row and column conductors are integral with the pixel electrodes. *See* EX-2005 at 3-4. In this regard, the rows and columns should also be formed without having any intervening elements. On the other hand, active matrix displays isolate the pixel electrodes from the row and

column addressing lines by a thin film transistors (TFTs), which is placed in the area of each pixel that does not interfere with the light emission. *See* EX-2005 at 6-7. The row and column electrodes for addressing the pixels are then placed in the narrow spaces between the pixels or underneath the emitting areas. *See, e.g.*, EX-2005 at 6-7.

68. At least in view of the above, Masuda, which is directed towards the field of endeavor of passive matrix displays (particularly, passive matrix displays utilizing field emission technology) is not from the same field of endeavor of the invention defined by claims 23 and 35 of the '736 patent, which are directed towards the field of endeavor of an active matrix display.

69. Additionally, Masuda is not reasonably pertinent to the problem faced by the inventor of the '736 patent.

70. The '736 patent is directed towards the problem of how to reduce, with respect to electro-optical devices that utilize active matrix displays, image distortions and color irregularities caused by directional viewing variations. Such directional viewing variations occur specifically in electro-optical devices utilizing active matrix displays in which pixels circuits have different shapes and/or pitches in the column and row directions. Example relevant portions of the '736 patent are reproduced below:

One type of driving system for a related art display having liquid-crystal elements, organic EL (electroluminescent) elements, electrophoresis elements, electron emitting elements, or the like is an active matrix drive system. An active-matrix drive system display includes a display panel that has a plurality of pixels in a matrix. The pixels have respective pixel circuits, each of which is constituted by electro-optical elements and driving transistors for supplying drive power to the electro-optical elements. 1:11-22

EX-1001 at 1:11-22.

When the pixel circuits have different shapes and/or different pitches in the column direction (data-line direction) and the row direction (scan-line direction) of the display panel portion, directional viewing variation occurs between the column direction and the row direction of the display panel. As a result, an image displayed on the display panel portion may be distorted in the column direction (data-line direction) or the row direction (scan-line direction). In particular, for a full-color display, color irregularities occur in addition to the distortion of the image in the column and row directions. Thus, the display quality of the display is reduced. 1:23-34

EX-1001 at 1:23-34

71. The directional viewing variations, related to the problem of image distortions and color irregularities mentioned in the '736 patent, pertains to a gradual decrease in brightness or contrast of a display as you move away from being directly in front of the display.

72. In contrast, Masuda is directed to the problem of, at the time of the alleged invention of Masuda, passive matrix displays utilizing such field emission display technology having visual interference caused by horizontal stripes or vertical stripes due to differences in luminosity between rows or differences in luminosity between columns in such passive matrix displays. EX-1009 at [0021].

73. The problem of Masuda of the interference effects of horizontal and vertical stripes is different from the problem of directional viewing variation effects mentioned in the '736 patent because the horizontal and vertical stripes may be perceived at all viewing positions, and because the interference effects of horizontal and vertical stripes is strongly affected by the particular image being displayed whereas the directional viewing variation effects are not related to any specific image.

74. Also, at the time of the alleged invention of Masuda and the filing date of the '736 patent, passive matrix displays had limited resolution, due to low pixel

density, which resulted in the problem of the visual interference caused by horizontal stripes or vertical stripes. *See, e.g.*, EX-1011 at 4 (“Because of these problems, the PM type is currently manufactured as products with a screen size of no more than a few inches and 10,000 pixels or so.”); EX-2008 at 3-7 (describing relationship between visual interference and resolution). The low pixel density is related to the fact that, in passive matrix displays, the addition of more rows/columns of pixels means that there is less time to stimulate the pixels and because passive matrix displays have no mechanism for storing an image in a row while other rows are being written. *See, e.g.*, EX-2009 at 3 (“The shortcomings of passive matrix addressing ... are overcome by active matrix addressing. In this mode an electronic switch is placed in each pixel providing ... the means to store videoinformation on capacitors”). With such constraints, the maximum resolution of passive matrix displays is significantly limited.

75. In contrast, at the time of the alleged invention of Masuda and the filing date of the ‘736 patent, active matrix displays included a mechanism for storing an image in a row while others rows are being written and achieved much greater resolution than passive matrix displays, which avoids the problem mentioned in Masuda. *See* EX-2005 at 6-7; EX-2007 at 14; EX-2008 at 3-7 (describing relationship between visual interference and resolution); EX-2009 at 3 (“The

shortcomings of passive matrix addressing ... are overcome by active matrix addressing. In this mode an electronic switch is placed in each pixel providing ... the means to store videoinformation on capacitors”).

76. At least in view of the above, the ‘736 patent and Masuda are not within the same field of endeavor, and Masuda is not reasonably pertinent to the problem faced by the inventor of the ‘736 patent. Thus, Masuda is not analogous art with respect to the ‘736 patent.

B. A POSITA Would Not Have Looked Towards Masuda To Modify Kimura

77. A person of skill in the art would not have found it obvious to combine Masuda with Kimura, nor look from one to the other for guidance.

78. As described above, passive matrix displays, such as described in Masuda, and active matrix displays, such as described in Kimura, are entirely different.

79. With Masuda’s diametrically different mode of operation and configuration that is limited in the number of pixels and quality of the image that can be implemented, a POSITA working on an active matrix display design would

never consider the passive matrix field emission display technology proposed by Masuda.

80. In view of the above, Kimura and Masuda describe incompatible display technologies such that a POSITA would not look towards one of such references in attempt to improve the other.

81. Second, as described above, Masuda is directed to solving a problem of visual interference caused by horizontal stripes or vertical stripes that is not a problem of active matrix displays due to active matrix displays being capable of greater resolution than passive matrix displays. *See* EX-2008 at 3-7 (describing relationship between visual interference and resolution); EX-2010 at 3-5. Thus, the problem of Masuda is not a problem in Kimura, which describes an improvement for active matrix displays, and the solution of Masuda is not applicable to Kimura.

82. At least in view of the above, a POSITA would not have considered combining Kimura and Masuda, as the references describe significantly different and incompatible technologies, and Kimura already effectively achieves its purpose of reducing variation in luminance of light emission without having the problem indicated in Masuda of visual interference caused by horizontal stripes or vertical stripes, which are alleged in Masuda to be caused by differences in luminosity between columns or rows of pixels.

**C. Modifying Kimura By Masuda Would Make Kimura
Unsatisfactory For Its Intended Purpose**

83. As described above, Kimura is intended to provide a configuration that reduces variation in luminance of active matrix displays, which Kimura achieves by maintaining current flowing in the light emitting element constant. EX-1020 at [0077].

84. By attempting to solve variation in luminance by implementing a checkerboard arrangement of Masuda in the configuration of Kimura, instead of maintaining current flowing in the light emitting element constant, the variation in luminance in Kimura would be substantially increased. For example, the solution of Masuda of having a checkerboard pattern of primary color display elements and a non-display element does not address the problem solved in Kimura of variation in luminance of the OLED that is caused by fluctuating current flowing into the OLED due to fluctuating threshold voltage of the driving TFT, or variations in an amount of current actually flowing despite a constant voltage applied between two electrodes of the OLED due to changes in environment temperature, degradation of the OLED, and the like. EX-1020 at [0010], [0037], and [0041]. That is, the solution of Masuda

does not provide any mechanism for ensuring that variation in luminance of an OLED is reduced when the current flowing into the OLED fluctuates.

85. In view of the above, a modification of Kimura in which the configuration for keeping the current flowing in the light emitting element constant of Kimura is replaced with the checkerboard pattern of Masuda would cause Kimura to be unsatisfactory for its intended purpose of reducing variation in luminance of light emission of the active matrix display.

86. At least for these reasons, it would not have been obvious for a POSITA to modify Kimura with the checkerboard pattern of Masuda.

D. There is no Motivation to Combine Masuda with Kimura

87. As described above, the problem to be solved by Masuda is related to a difference in luminosity that is caused by inherent luminosity differences between the different primary colors; green having a luminosity value of 0.59, red having a luminosity value of 0.30, and blue having a luminosity value of 0.11. EX-1009 at [0021]-[0022], and [0026]. The particular checkerboard arrangement proposed by Masuda is specifically designed to address the above problem by having a red color display element, a green color display element, a blue color display element, and a non-display element arranged in a repeated, two-row and two-column arrangement, with the two brightest colors (*i.e.*, Green (0.59) and Red (0.30)) being arranged at

opposite corner positions. EX-1009 at [0022] and [0028]-[0030]. With such arrangement, color-dependent brightness variations are not eliminated, but are reduced. EX-1009 at [0028].

88. As such, the checkerboard pixel arrangement proposed by Masuda does not address problems related to all forms of differences in luminosity generally. Rather, the checkerboard pixel arrangement proposed by Masuda only attempts to address the difference in luminosity when such difference in luminosity is specifically caused by inherent luminosity differences between the different colors, *i.e.*, when such difference in luminosity is color-dependent. That is, Masuda's pixel arrangement does not reduce variation in pixel luminance *generally*, but reduces only color-dependent variations in pixel luminance.

89. Such a problem of difference in luminosity that is caused by inherent luminosity differences between the different primary colors does not exist in Kimura. In particular, Kimura already achieved balanced light emission luminance among light emitting elements of different colors by controlling the length of the lighting period, by controlling reference current values inputted into the pixels of different colors, and by controlling the gate length-gate width ratio of a current supply transistor. EX-1020 at [0290]. That is, the brightness of each pixel is explicitly

controlled to achieve balanced light emission luminance, rather than being left at their natural luminosity characteristics of color.

90. It should be noted that, as further described above, the problem to be solved by Kimura related to variation of brightness is caused by fluctuating threshold voltage of the driving TFT, or variations in an amount of current actually flowing despite a constant voltage applied between two electrodes of the OLED due to changes in environment temperature, degradation of the OLED, and the like, rather than being caused by the inherent luminosity differences between the different primary colors. EX-1020 at [0010], [0037], and [0041].

91. In view of the above, the variation of brightness problem in Kimura would continue to exist under any pixel arrangement, including Masuda's. Thus, there is no motivation to use the pixel arrangement of Masuda to address the above problem in Kimura.

92. Additionally, while the Petition contends that Kimura "does not describe the specific arrangement of colored pixels (pixel geometries)" and therefore "would have led a POSITA to consider known pixel geometries, like Masuda, to understand how Kimura's colored pixels may be arranged" (Petition at 57), Kimura *does* describe a specific pixel arrangement. That is, Kimura describes a 4x4 arrangement of pixel regions in which "four pixels [are] on the i-th (i is a natural

number) row and j-th (j is a natural number) column, the (i+1)-th row and j-th column, the i-th row and (j+1)-th column, and the (i+1)-th row and (j+1)-th column.” EX-1020 at [0201], [0468], and Figs. 3 and 53. Thus, a POSITA would have understood from Kimura how pixels would have been arranged in Kimura’s configuration, and would not need to look elsewhere to determine the pixel arrangement of Kimura.

93. Even if Kimura was silent with respect to a specific arrangement of pixels, it would not have been obvious for a POSITA to modify Kimura with the specific checkerboard pixel arrangement of Masuda, at least for the reasons discussed above.

IX. Summary

94. The combination of the Kimura and Masuda references fail to render claims 23 and 35 of the ‘736 patent obvious for all the reasons explained above.