

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner

U.S. Patent No. 7,697,369

**DECLARATION OF R. JACOB BAKER,
UNDER 37 C.F.R. § 1.68 IN SUPPORT OF PETITION FOR
INTER PARTES REVIEW**

TABLE OF CONTENTS

I.	Introduction.....	4
II.	Qualifications and Professional Experience	6
III.	Level of Ordinary Skill in the Art	9
IV.	Relevant Legal Standards	10
V.	Background.....	12
	A. Memory Systems.....	12
	B. Strobe Signals.....	12
	C. Synchronous and Asynchronous Memory	13
VI.	Overview of the '369 Patent.....	14
VII.	Claim Construction.....	18
VIII.	Identification of how the Claims are Unpatentable.....	19
	A. Ground 1: Claims 1, 6, 10, 14, 15, 16, 17, 18, 19, 25, 26, and 27 are Obvious in View of Lee	19
	1. Summary of Lee.....	19
	2. Claim 1	24
	3. Claim 6.....	39
	4. Claim 10.....	42
	5. Claim 14.....	44
	6. Claim 15.....	46
	7. Claim 16.....	47
	8. Claim 17.....	48
	9. Claim 18.....	48

10.	Claim 19.....	48
11.	Claim 25.....	48
12.	Claim 26.....	51
13.	Claim 27.....	58
B.	Ground 2: Claims 2, 7, and 11 are Obvious in View of Lee and JEDEC	58
1.	Summary of JEDEC	58
2.	Motivation to Combine Lee and JEDEC	60
3.	Claim 2.....	64
4.	Claim 7.....	68
5.	Claim 11.....	68
IX.	Conclusion	70

I, R. Jacob Baker, do hereby declare as follows:

I. INTRODUCTION

1. I am making this declaration at the request of Western Digital Technologies, Inc. in the matter of the *Inter Partes* Review of U.S. Patent No. 7,697,369 (“the ’369 patent”) to Koshizuka *et al.*

2. I am being compensated for my work in this matter at my standard hourly rate. I am also being reimbursed for reasonable and customary expenses associated with my work and testimony in this investigation. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

3. I have been asked to provide my opinions regarding whether claims 1, 2, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 25, 26, and 27 (“the Challenged Claims”) of the ’369 patent are unpatentable as they would have been obvious to a person having ordinary skill in the art (“POSITA”) at the time of the alleged invention, in light of the prior art. It is my opinion that all of the limitations of the challenged claims would have been obvious to a POSITA.

4. In the preparation of this declaration, I have studied:

- a. the ’369 patent, EX1001;
- b. the prosecution history of the ’369 patent (“’369 File History”), EX1002;

- c. U.S. Patent Publication No. 2004/0022095 to Lee *et al.* (“Lee”), EX1005;
- d. JEDEC Standard: Double Data Rate (DDR) SDRAM Specification, JESD79C (March 2003) (“JEDEC”), EX1007.

5. In forming the opinions expressed below, I have considered:

the documents listed above;

High Performance Memories: New Architecture DRAMs and SRAMs Evolution and Function, Betty Prince (1999) (“Prince”), EX1006;

U.S. Patent No. 6,026,465 to Mills *et al.* (“Mills”), EX1008;

U.S. Patent No. 6,956,409 to Streif *et al.* (“Streif”), EX1009;

U.S. Patent Publication No. 2006/0064561 to Simeral *et al.* (“Simeral”), EX1010.

the relevant legal standards, including the standard for obviousness, and any additional authoritative documents as cited in the body of this declaration; and

my own knowledge and experience based upon my work in the field of optical communication as described below, as well as the following materials.

6. Unless otherwise noted, all emphasis in any quoted material has been added.

II. QUALIFICATIONS AND PROFESSIONAL EXPERIENCE

7. My complete qualifications and professional experience are described in my *Curriculum Vitae*, a copy of which can be found in Exhibit 1004. The following is a brief summary of my relevant qualifications and professional experience.

8. I presently serve as a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas (UNLV). All of my opinions stated in this declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience in designing, developing, researching, and teaching regarding integrated circuit design and memory system design.

9. I have been teaching electrical engineering at UNLV since 2012. Prior to this position, I was a Professor of Electrical and Computer Engineering at Boise State University from 2000. Prior to my position at Boise State University, I was an Associate Professor of Electrical Engineering between 1998 and 2000 and Assistant Professor of Electrical Engineering between 1993 and 1998 at the University of Idaho. I have been teaching electrical engineering since 1991.

10. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno in 1993. I also received a MS and BS in Electrical Engineering from UNLV in 1988 and 1986, respectively.

11. As described in my CV, I am a licensed Professional Engineer and have extensive industry experience in circuit design, fabrication, and manufacture of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, Phase-Change Random Access Memory (PCRAM) chips, and CMOS Image Sensors (CISs) at Micron Technology, Inc. (“MTI”) in Boise, Idaho. I spent considerable time working on the development of flash memory chips while at MTI. My efforts resulted in more than a dozen patents relating to flash memory. One of my projects at MTI included the development, design, and testing of circuit design techniques for a multi-level cell (MLC) flash memory using signal processing. This effort resulted in higher-density memories for use in solid-state drives and flash memory cards having an ATA interface that are ubiquitous in consumer electronics, including cameras and data storage systems. Further, the use of higher-density memory can result in fewer changes in the flash translation layer for logical-to-physical addressing, less need for garbage collection, and larger data segments that can improve a computing system’s performance. Another project I worked on at MTI focused on the design of buffers for high-speed double-data rate DRAM, which resulted in around 10 U.S. patents in buffer design. Among many other experiences, I led the development of the delay locked loop (DLL) in the late 1990s so that MTI DRAM products could transition to the DDR memory protocol, used in mobile and non-mobile (server, desktop, cell phones, tablets, etc.)

computing systems as main computer memory, for addressing and controlling accesses to memory via interprocess communications (IPC) with the memory controller (MC). Further, I did consulting work at Sun Microsystems and then Oracle on the design of memory modules during 2009 and 2010. This work entailed the design of low-power, high-speed, and wide interconnection methods with the goal of transmitting data to/from the memory module and the MC at higher speeds.

12. I have taught courses in integrated circuit design (analog, digital, mixed-signal, memory circuit design, etc.), linear circuits, microelectronics, communication systems, power electronics, and fiber optics. As a professor, I have been the main advisor to over 100 Master's and Doctoral students.

13. I am the author of several books covering the area of integrated circuit design including: DRAM Circuit Design: Fundamental and High-Speed Topics (two editions), CMOS Circuit Design, Layout, and Simulation (four editions), and CMOS Mixed-Signal Circuit Design (two editions). I have authored, and coauthored, more than 100 papers and presentations in the areas of solid-state circuit design, and I am the named inventor on over 150 granted U.S. patents.

14. I have received numerous awards for my work, including the Frederick Emmons Terman (the "Father of Silicon Valley") Award. The Terman Award is bestowed annually upon an outstanding young electrical/computer

engineering educator in recognition of the educator's contributions to the profession.

15. I am a Fellow of the IEEE for contributions to memory circuit design. I have also received the IEEE Circuits and Systems Education Award (2011).

16. I have received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001), all from Boise State University. I have also received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor award four of the years I have been at UNLV.

17. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art.

III. LEVEL OF ORDINARY SKILL IN THE ART

18. I understand there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including (1) the levels of education and experience of persons working in the field at the time of the invention; (2) the sophistication of the technology; (3) the types of problems encountered in the field; and (4) the prior art solutions to those problems.

19. A person of ordinary skill in the art ("POSITA") in the field of the '369 patent, as of its earliest possible filing date of June 8, 2006, would have been

someone knowledgeable and familiar with the memory system arts that are pertinent to the '369 patent. A POSITA would have been familiar with the field of memory systems including memory controllers, during the 2000s. That person would have a bachelor's degree in electrical engineering, or equivalent training, and approximately two years of experience working in the field of memory systems. Lack of work experience can be remedied by additional education, and vice versa.

20. For purposes of this Declaration, in general, and unless otherwise noted, my statements and opinions, such as those regarding my experience and the understanding of a POSITA generally (and specifically related to the references I consulted herein), reflect the knowledge that existed in the field as of the priority date of the '369 patent. Unless otherwise stated, when I provide my understanding and analysis below, it is consistent with the level of a POSITA prior to the priority date of the '369 patent.

IV. RELEVANT LEGAL STANDARDS

21. I am not an attorney. In preparing and expressing my opinions and considering the subject matter of the '369 patent, I am relying on certain basic legal principles that counsel have explained to me. These principles are discussed below.

22. I understand that prior art to the '369 patent includes patents and

printed publications in the relevant art that predate the priority date of the alleged invention recited in the '369 patent. For purposes of this Declaration, I am applying June 8, 2006 as the earliest possible priority date of the '369 patent.

23. I have been informed that a claimed invention is unpatentable under 35 U.S.C. § 103 if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. I have also been informed by counsel that the obviousness analysis takes into account factual inquiries including the level of ordinary skill in the art, the scope and content of the prior art, and the differences between the prior art and the claimed subject matter.

24. I have been informed by counsel that the Supreme Court has recognized several rationales for combining references or modifying a reference to show obviousness of claimed subject matter. Some of these rationales include the following: (a) combining prior art elements according to known methods to yield predictable results; (b) simple substitution of one known element for another to obtain predictable results; (c) use of a known technique to improve a similar device (method, or product) in the same way; (d) applying a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e) choosing from a finite number of identified, predictable solutions, with a

reasonable expectation of success; and (f) some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

V. BACKGROUND

A. Memory Systems

25. Memory systems typically include a memory controller and the memory itself. “In a conventional mobile processing system, the memory and the memory controller are, typically, interconnected in a point-to-point fashion.” EX1005, Lee, [0006]. Memory systems perform both read and write operations. For a write operation, the memory controller receives data from an external source and then transmits that data to the memory for storage. During a read operation, the memory transmits data to the memory controller, which then passes that data to an external device that is requesting that data.

B. Strobe Signals

26. When transmitting data between the memory controller and the memory, strobe signals are used to inform the receiving system when to sample the incoming data. For example, during a write operation, the memory controller sends the write data signal along with a write data strobe signal. The memory then uses the received write data strobe signal to know when to sample the data from the data

signal being received.

27. Similarly, during the read operation, the memory transmits data to the controller along with a read data strobe signal. As will be explained in detail below, it was also known to have the memory generate the read data strobe signal in response to a strobe signal from the controller.

C. Synchronous and Asynchronous Memory

28. Memory may be either synchronous or asynchronous. *See* Prince, 17-18. An example of synchronous memory is Synchronous Dynamic Random-Access Memory (SDRAM). *See* Prince, 23. An example of asynchronous memory is Static Random-Access Memory (SRAM). *See* Prince, 21.

29. In synchronous memory systems, transfer of data between the controller and memory is synchronized with the system clock signal. *See* EX1005, Lee, [0005]. The clock signal can be provided to the memory device in different ways, such as from a separate clock crystal used for other components of the computer system, or from the memory controller. For example, when the controller writes to memory, it sends a data signal to the memory along with a strobe signal that is synchronized with the system clock. Similarly, during a read operation, the memory transmits data along with a strobe signal synchronized with the system clock.

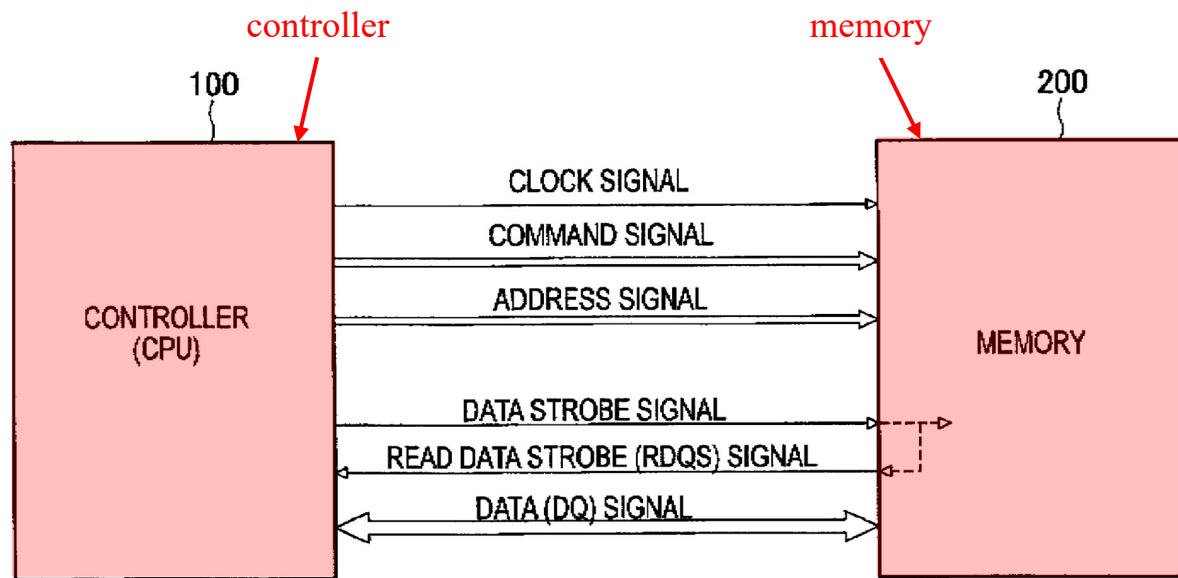
30. Asynchronous memory, however, is not synchronized with the system

clock. *See* EX1005, Lee, [0028]. For example, when the controller writes to memory it sends a data signal to the memory along with a strobe signal. That strobe signal does not have to be synchronized with the system clock. Similarly, in a read operation, the memory transmits data along with a strobe signal that is not necessarily synchronized with the system clock.

31. Thus, both asynchronous and synchronous memory make use of strobe signals in a similar manner but differ by whether the strobe signals are synchronized with the system clock. In other words, both types of memory use strobe signals that are synchronized with the data signals. But synchronization of the strobe signal with the data signal is distinct from the concept of “synchronous memory,” which refers to synchronizing the strobe signal with the system clock.

VI. OVERVIEW OF THE '369 PATENT

32. The '369 patent generally “relates to a system having a controller and a memory and, more particularly, to a data sending/receiving operation between the controller and the memory.” '369 patent, 1:6-8. Fig. 1 of the '369 patent, shown below, illustrates “a controller 100 and a memory 200.” '369 patent, 3:7-8.



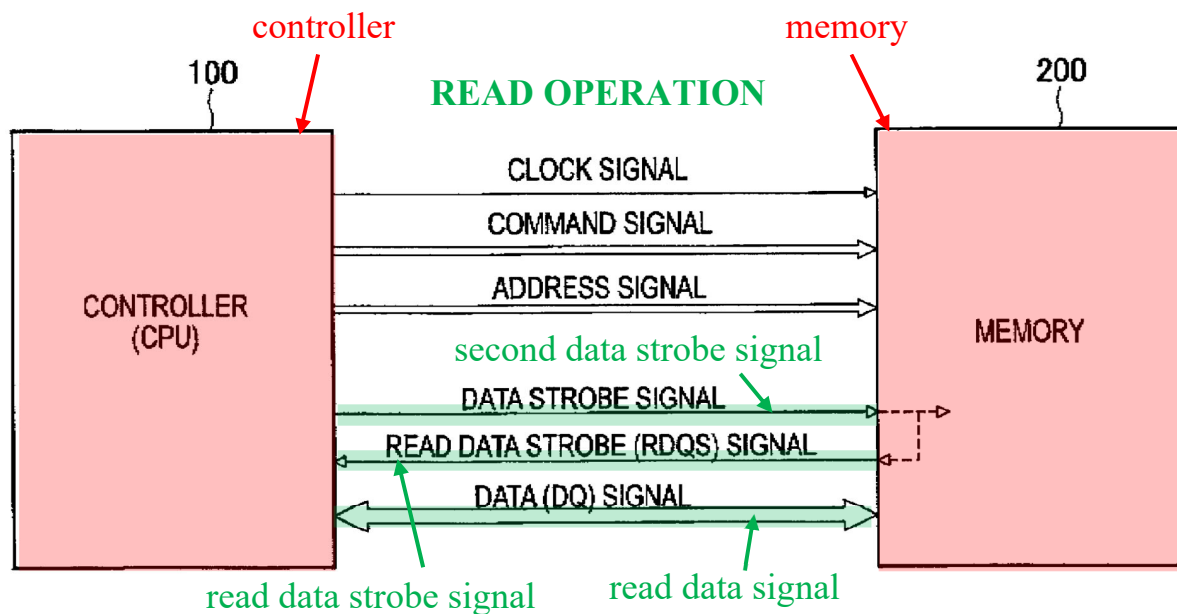
'369 patent, Fig. 1 (annotated).

33. The background section of the '369 patent explains that “[i]n a conventional data sending/receiving operation between the controller and the memory, either the controller or the memory who serves as a sender generates a data strobe.” ’369 patent, 1:9-11. For example, during the write operation—where the controller transmits data to the memory—the controller generates the strobe signal. During the read operation—where the memory transmits data to the controller—the memory generates the strobe signal.

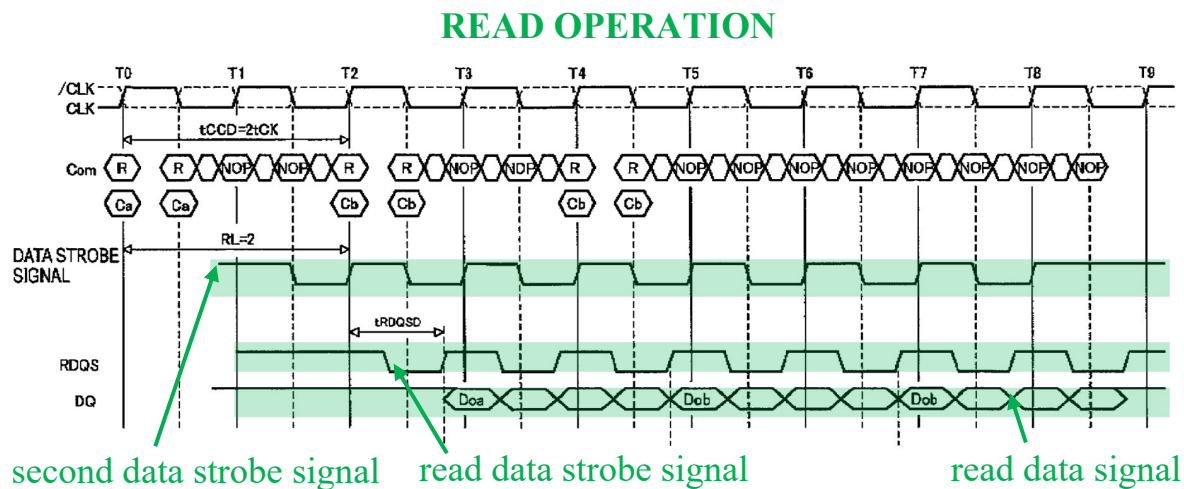
34. The purported novelty of the '369 patent is that during the read operation, the memory generates the read data strobe signal in response to a strobe signal from the controller: “The memory 200 is adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal and

to send out the read data signal synchronized with the read data strobe signal.”

'369 patent, 3:22-25. Claim 1, for example, recites this concept as follows: “the memory being adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal.” The read operation is illustrated in Figs. 1 and 8 as shown below.

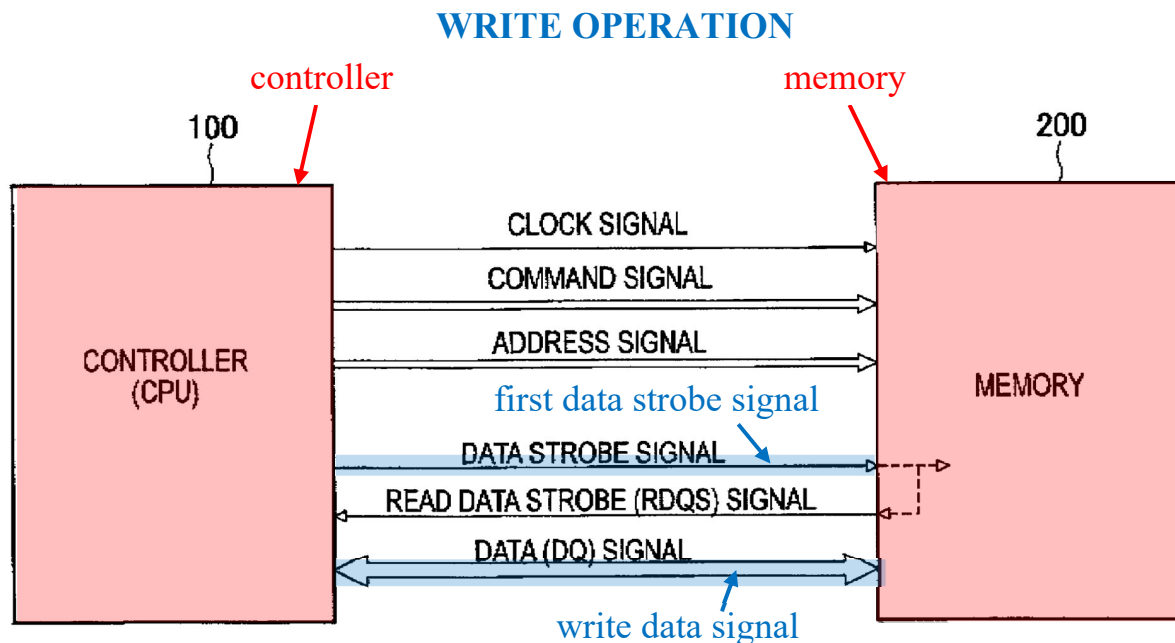


'369 patent, Fig. 1 (annotated).



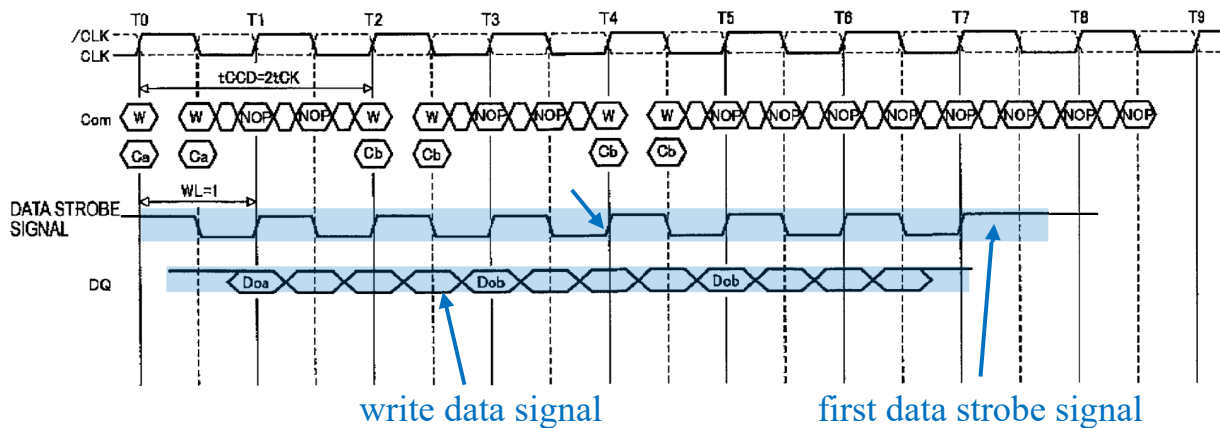
'369 patent, Fig. 8 (annotated).

35. The '369 patent also describes and claims a conventional write operation. During the write operation, "[t]he controller 100 is adapted to send out a first data strobe signal and a write data signal." '369 patent 3:12-14. The write operation is illustrated in Figs. 1 and 6 as shown below.



'369 patent, Fig. 1 (annotated).

WRITE OPERATION



'369 patent, Fig. 6 (annotated).

36. As I will explain in detail below, the '369 patent describes and claims nothing more than well-known techniques for using data strobe signals during read and write operations. In particular, the concept of having the memory send a data strobe signal in response to a strobe signal from the controller was well known at the time the '369 patent was filed.

VII. CLAIM CONSTRUCTION

37. It is my understanding that in order to properly evaluate the '369 patent, the terms of the claims must first be interpreted. It is my understanding that for the purposes of this *inter partes* review, the claims are to be construed under the so-called *Phillips* standard, under which claim terms are given their ordinary and customary meaning as would be understood by one of ordinary skill in the art in light of the specification and prosecution history, unless the inventor has set forth a special meaning for a term. I do not believe any of the terms require express

construction.

VIII. IDENTIFICATION OF HOW THE CLAIMS ARE UNPATENTABLE

38. I have been asked to provide my opinion as to whether the Challenged Claim of the '369 patent would have been obvious in view of the prior art. The discussion below provides a detailed analysis of how the prior art references identified below teach the limitations of the Challenged Claims of the '369 patent.

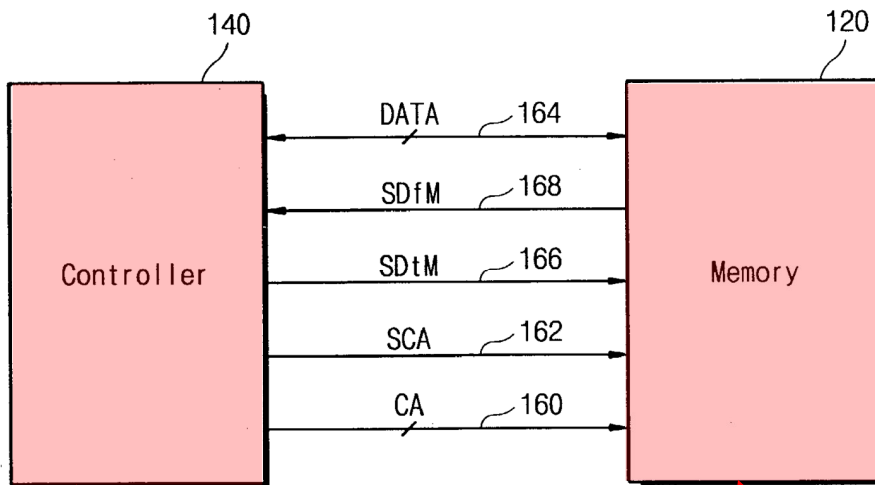
39. As part of my analysis, I have considered the scope and content of the prior art and any differences between the alleged invention and the prior art. I describe in detail below the scope and content of the prior art, as well as any differences between the alleged invention and the prior art, on an element-by-element basis for each Challenged Claims of the '369 patent.

40. As described in detail below, the alleged invention of the Challenged Claims are anticipated by the prior art and would have been obvious in view of the teachings of the prior art as well as the knowledge of a POSITA.

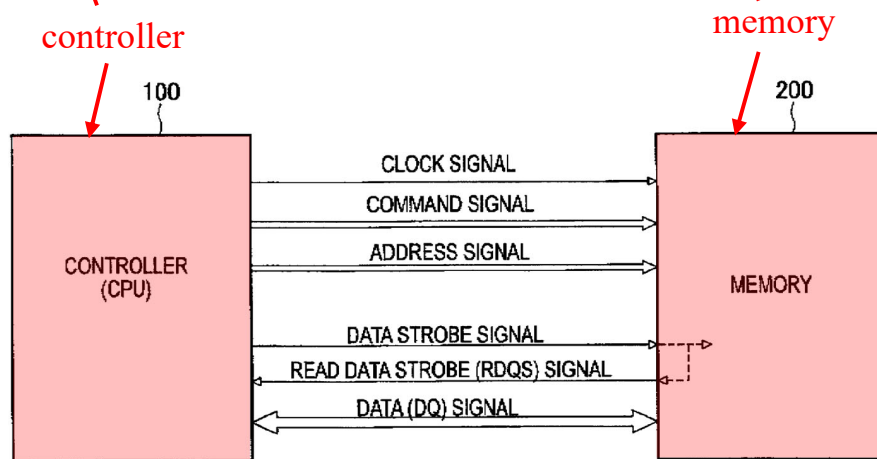
A. Ground 1: Claims 1, 6, 10, 14, 15, 16, 17, 18, 19, 25, 26, and 27 are Obvious in View of Lee

1. Summary of Lee

41. Lee, like the '369 patent, relates to “a system that performs data transmission between a memory and a memory controller.” EX1005, Lee, [0002]. Below is a comparison between Fig. 1 of Lee and Fig. 1 of the '369 patent, which both illustrate data and strobe signals sent between a memory and a controller.

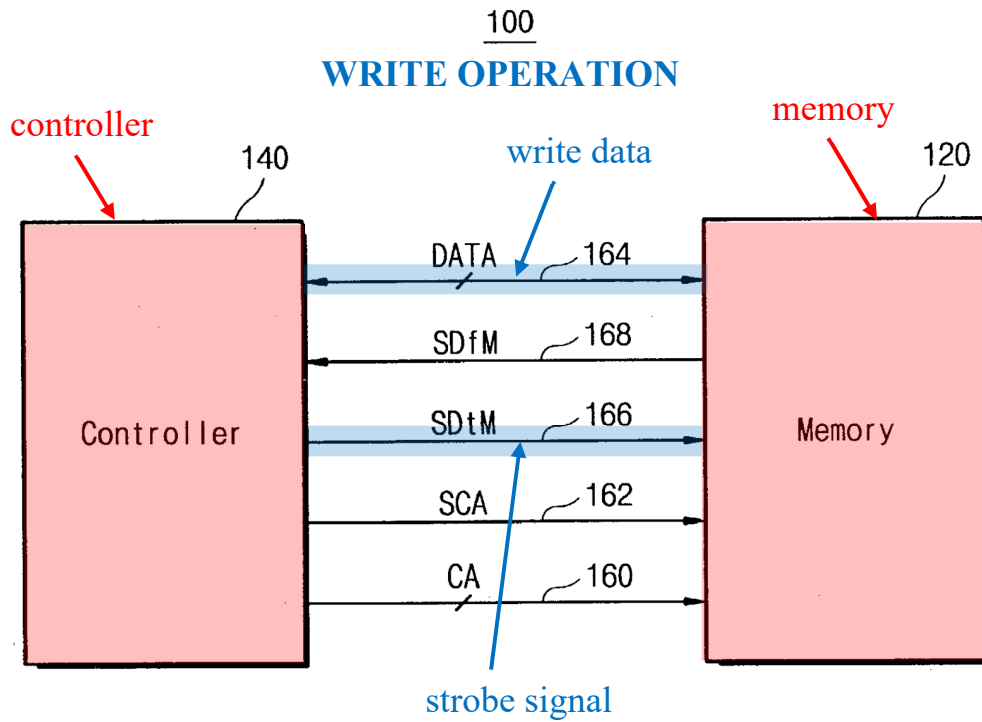


Lee, Fig. 1 (annotated).

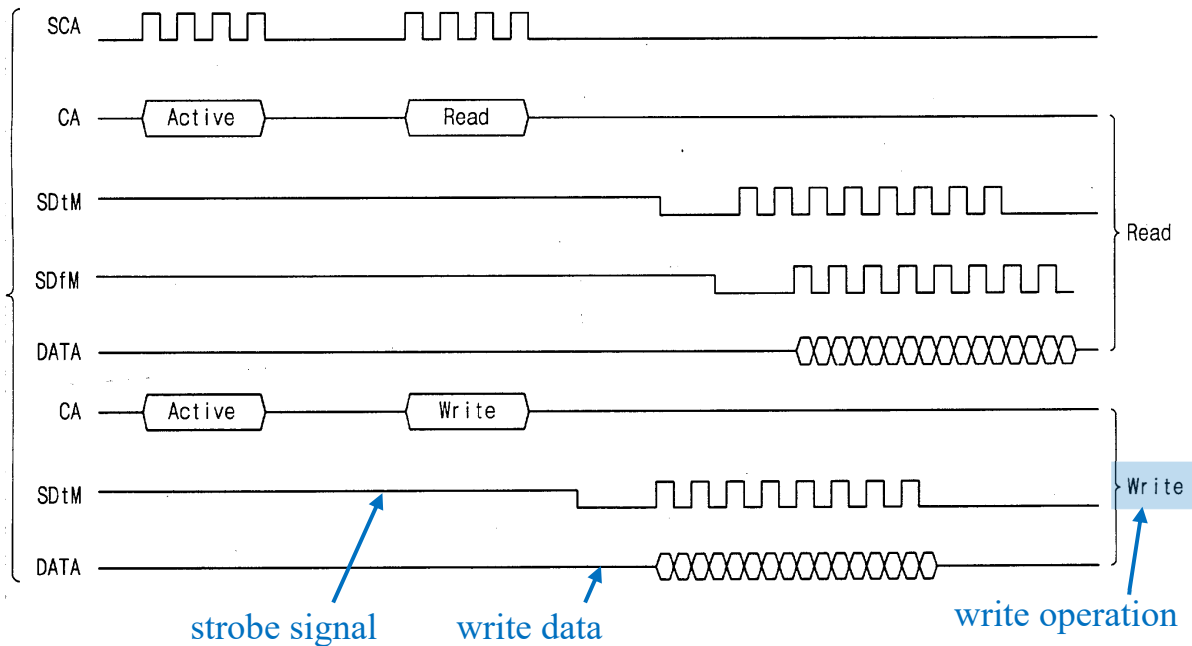


'369 patent, Fig. 1 (annotated).

42. Lee further describes the read and write operations that make use of strobe signals in the same way as the '369 patent. *See* EX1005, Lee, [0020]-[0021]. For the write operation, “the write data DATA is sent to the memory 120 from the memory controller 140 together with the second strobe signal SDtM based on the source synchronous interface.” EX1005, Lee, [0020]. The write operation is shown in the annotated Figs. 1 and 2 below.



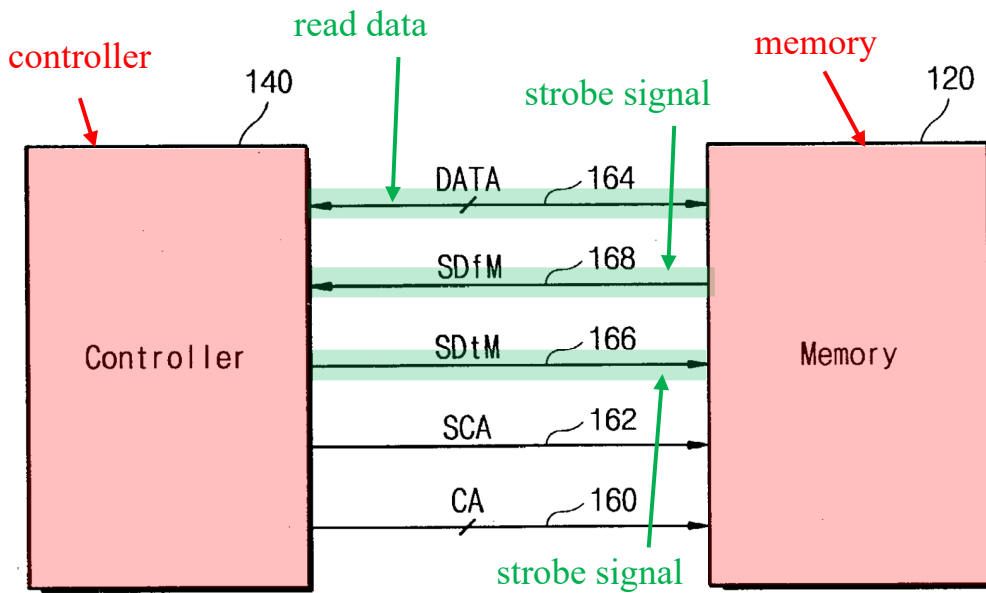
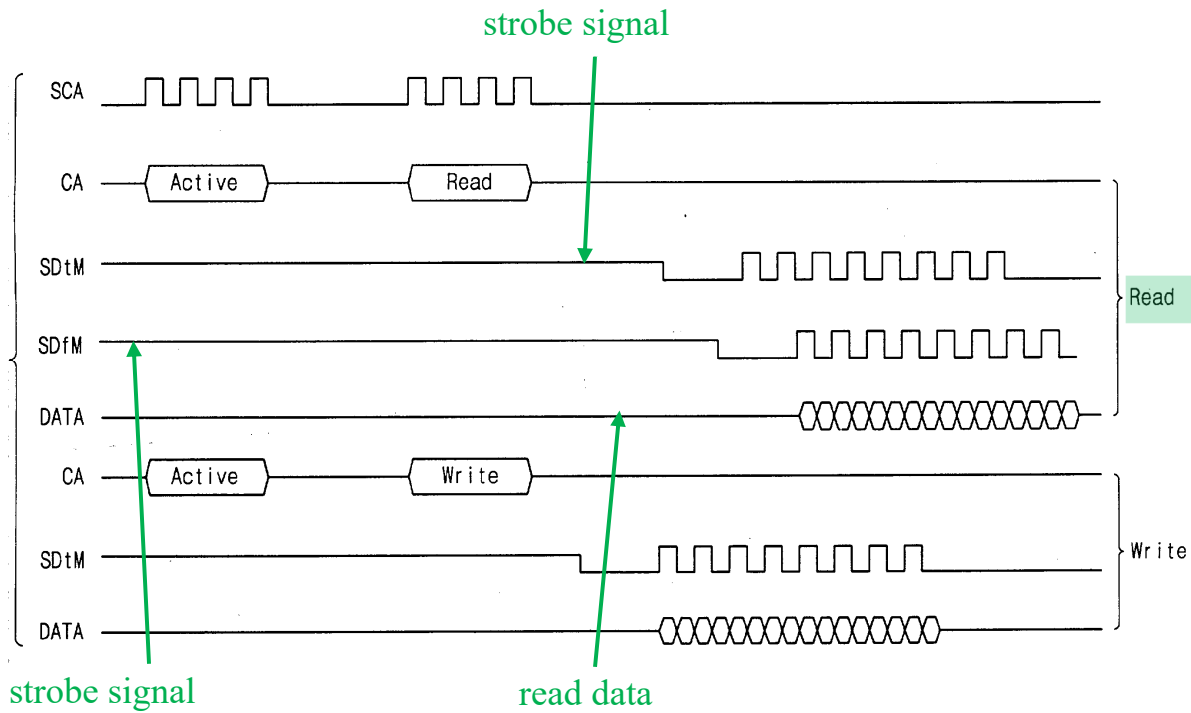
Lee, Fig. 1 (annotated).



Lee, Fig. 2 (annotated).

43. Lee's read operation also uses strobe signals in the same way as the '369 patent. For the read operation, "[t]he read data that is read from the memory 120 is sent to the memory controller 140 together with the third strobe signal SDfM." EX1005, Lee, [0021]. The third strobe signal is generated in response to a signal from the controller: "the memory controller 140 transfers to the memory 120 the second strobe signal SDtM as a transmission synchronous or reference signal at a time when it wants to receive data read out from the memory 120. The memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM." EX1005, Lee, [0021]. The read operation is shown in the annotated Figs. 1 and 2 below.¹

¹ I note that while Lee illustrates the timing for both read and write operations in the same figure, a POSITA would have recognized that read and write operations generally do not occur simultaneously.

100**READ OPERATION****Lee, Fig. 1 (annotated).****Lee, Fig. 2 (annotated).**

44. Accordingly, Lee describes the same read and write operations involving a controller and memory that are described in the '369 patent. Importantly, Lee's read operation corresponds to the purported novelty of the '369 patent: a memory that transmits a read data strobe signal responsive to a strobe signal from the controller. The analysis below explains how each claim element of the challenged claims is rendered obvious by Lee.

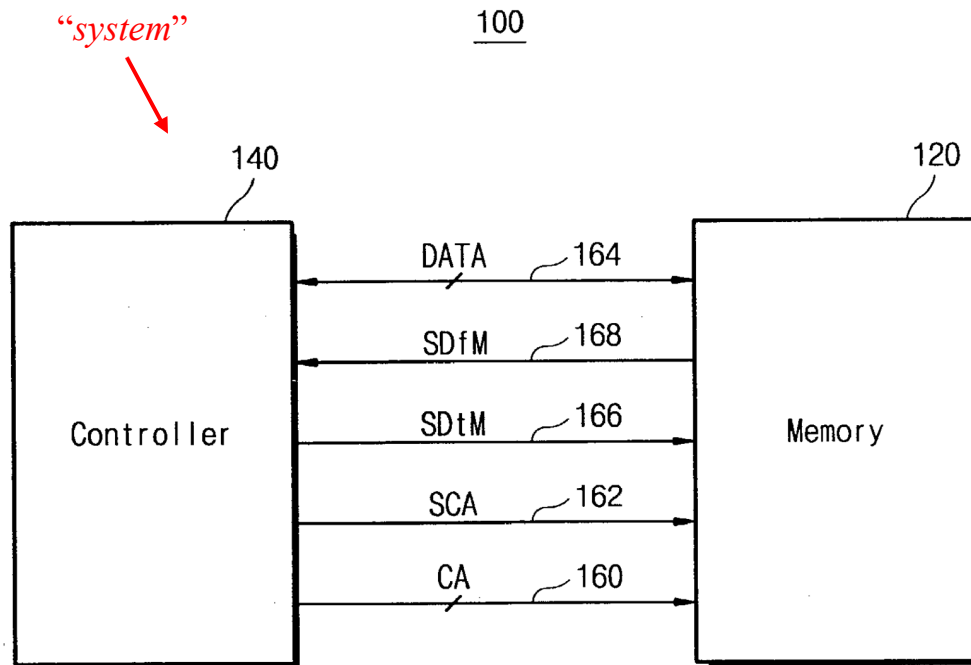
2. Claim 1

[1.0] *A system comprising:*

45. Lee describes a system for data transmission between controller and a memory: "The present invention is related to electronic devices, and, in particular, to **a system** that performs data transmission between a memory and a memory controller." EX1005, Lee, [0002].

A block diagram of a system according to certain embodiments of the present invention is illustrated in FIG. 1. Referring to FIG. 1, **a memory system 100 according to particular embodiments the present invention includes a memory 120 and a memory controller 140.** The memory 120 is an asynchronous memory, and can be implemented using non-volatile memories (e.g., FRAM, EEPROM, EPROM, and so on) and volatile memories (e.g., DRAM, SRAM, and so on). With the memory system 100, data transmission between the memory 120 and the memory controller 140 is carried out by a source synchronous interface.

EX1005, Lee, [0017].



Lee, Fig. 1 (annotated).

46. Thus, because Lee describes a memory system that performs data transmission between a memory and a memory controller, Lee renders obvious a “system” as claimed.

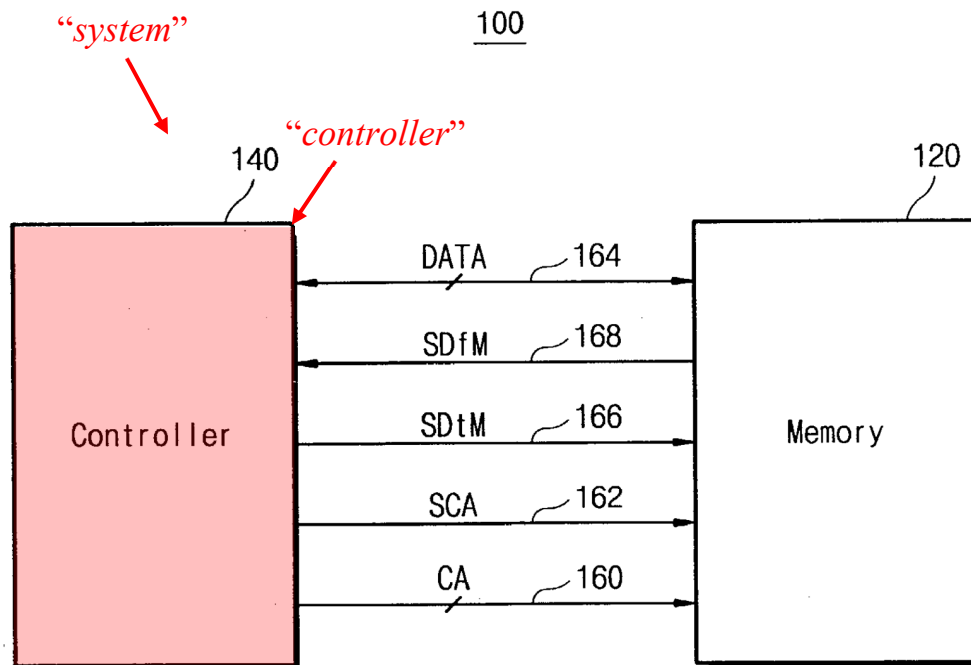
[1.1] a controller adapted to send out a first data strobe signal and a write data signal in a write operation,

47. First, Lee’s system includes a controller 120 (“controller”).

A block diagram of a system according to certain embodiments of the present invention is illustrated in FIG. 1. Referring to FIG. 1, **a memory system 100 according to particular embodiments the present invention includes a memory 120 and a memory controller 140**. The memory 120 is an asynchronous memory, and can be implemented

using non-volatile memories (e.g., FRAM, EEPROM, EPROM, and so on) and volatile memories (e.g., DRAM, SRAM, and so on). With the memory system 100, data transmission between the memory 120 and the memory controller 140 is carried out by a source synchronous interface.

EX1005, Lee, [0017].



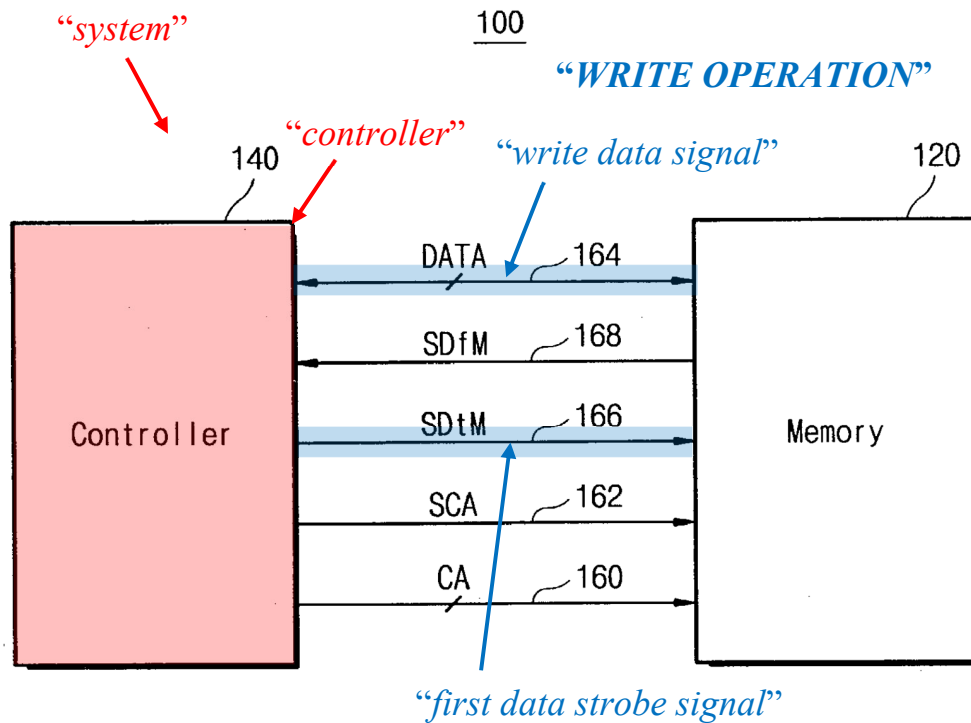
Lee, Fig. 1 (annotated).

48. **Second**, Lee describes the write operation in which the controller transmits strobe signal SDtM (*"first data strobe signal"*) over line 166 and data (*"write data signal"*) over line 164.

For a write operation, in addition to the command/address information CA, the memory controller 140 transfers data DATA to the memory 120 via a data bus 164, and transfers, as a transmission

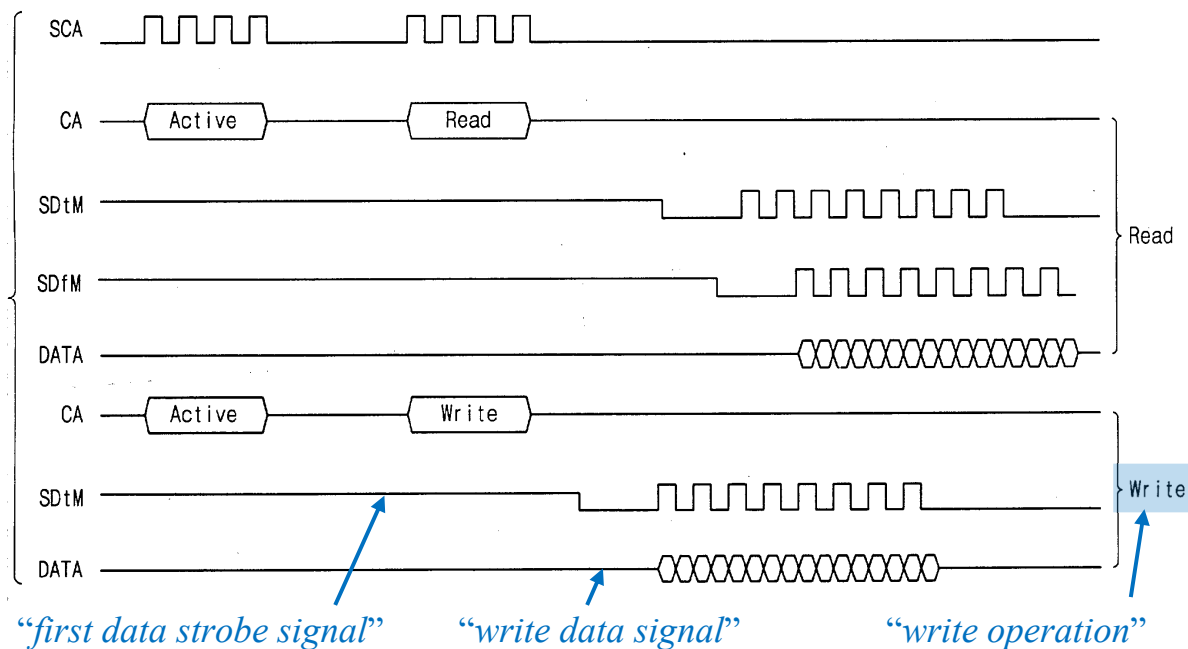
synchronous signal, the second strobe signal SDtM to the memory 120 via a signal line 166. In particular, for a write operation, the write data DATA is sent to the memory 120 from the memory controller 140 together with the second strobe signal SDtM based on the source synchronous interface. The memory 120 latches the write data DATA in response to the second strobe signal SDtM.

EX1005, Lee, [0020].



Lee, Fig. 1 (annotated).

49. Lee further describes the signals of the write operation in Fig. 2 as shown below.



Lee, Fig. 2 (annotated).

A write operation from the memory controller 140 to the memory 120 is also illustrated in the lower portion of FIG. 2. During a write operation where data is written to the memory 120, first, an active command Active' (e.g., a row address) is sent to the memory controller 140 from the memory 120. The active command Active' is sent to the memory 120 by the memory controller 140 toggling the first strobe signal SCA during a predetermined time, for example, when the active command Active' is on the control bus 160 (illustrated as CA in FIG. 2). That is, the memory controller 140 loads the active command Active' on the control bus 160 and toggles the first Strobe Signal SCA while the command is on the control bus 160. The memory 120 latches the active command Active in response to toggling of the first strobe signal SCA. The memory controller 140 subsequently loads the write command Write (e.g., a column address) on the control bus 160 and

toggles the first strobe signal SCA while the write command Write is on the control bus 160. The memory 120 latches the write command Write in response to toggling of the first strobe signal SCA.

The data to be written is then sent from the memory controller 140 to the memory 120. Data transmission is accomplished by toggling the second strobe Signal SDtM. That is, the memory controller 160 loads the write data DATA on the data bus 166 and toggles the second strobe signal SDtM while the write data DATA is on the data bus 166. The memory 120 latches the write data DATA in response to the second strobe signal SDtM. The latched write data may be stored in a memory cell array (not shown) utilizing conventional techniques. For example, the latched data may be stored in the memory cell array via a write circuit (e.g., a write driver circuit).

EX1005, Lee, [0026]-[0027].

50. Thus, because Lee describes a controller 140 that transmits a strobe signal SDtM and a data signal over lines 166 and 164 respectively, Lee renders obvious “*a controller adapted to send out a first data strobe signal and a write data signal in a write operation*” as claimed.

[1.2] the write data signal being synchronized with the first data strobe signal,

51. Lee explains that the data signal is synchronous with the data strobe signal SDtM: “For a write operation ... the memory controller 140 transfers data DATA to the memory 120 via a data bus 164, and transfers, **as a transmission synchronous signal**, the second strobe signal SDtM to the memory 120 via a

signal line 166.” EX1005, Lee, [0020]. A POSITA would have further recognized that the very purpose of a strobe signal is to instruct the receiving system when to sample the transmitted data. *See* EX1005, Lee, [0027] (“The memory 120 latches the write data DATA in response to the second strobe signal SDtM”). A POSITA would thus understand that the strobe signal is synchronized with the data signal. I further note that synchronization of the strobe signal does not necessarily make the memory “synchronous memory” because it is not necessarily synchronized with the system clock. *See* EX1005, Lee, [0028].

52. Thus, because Lee describes the strobe signal as a transmission synchronous signal, Lee renders obvious “*the write data signal being synchronized with the first data strobe signal*” as claimed.

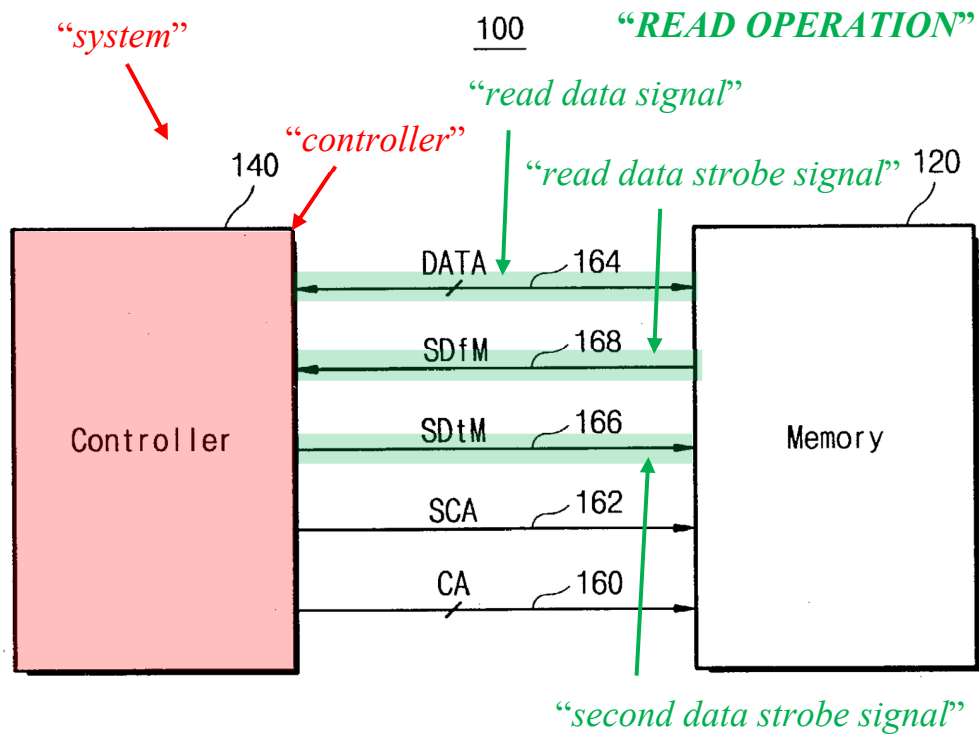
[1.3] *the controller being adapted, in a read operation, to send out a second data strobe signal and to receive a read data signal in synchronization with a read data strobe signal,*

53. First, Lee describes a read operation in which the memory transmits strobe signal SDfM (“*read data strobe signal*”) over line 168 and data (“*read data signal*”) over line 164 in response to the SDtM signal (“*second data strobe signal*”).

For a read operation, in addition to the command/address information CA, **the memory controller 140 transfers to the memory 120 the second strobe signal SDtM as a transmission synchronous or reference signal at a time when it wants to receive data read out**

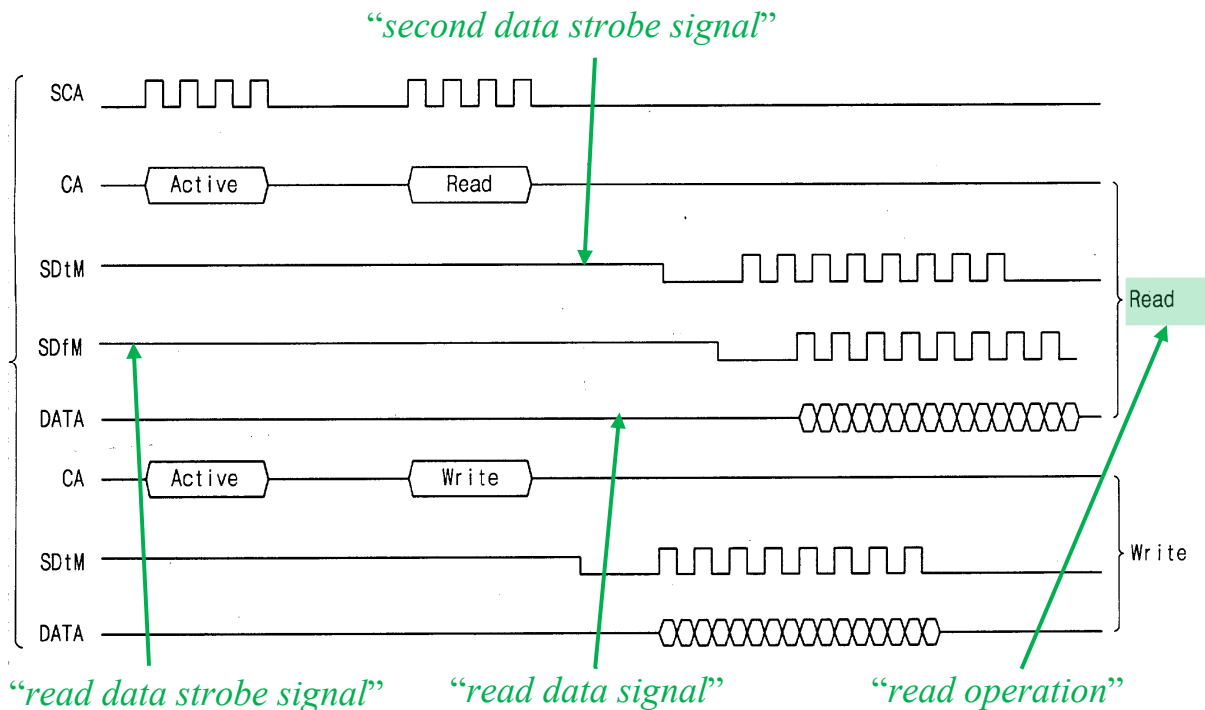
from the memory 120. The memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM. The read data that is read from the memory 120 is sent to the memory controller 140 together with the third strobe signal SDfM. Therefore, during the read operation the memory controller 140 receives the read data DATA from the memory 120 together with the third strobe signal SDfM at a required time, by sending the second strobe signal SDtM to the memory 120 after it transmits the command and address information to the memory 120.

EX1005, Lee, [0021].



Lee, Fig. 1 (annotated).

54. Lee further describes the signals of the write operation in Fig. 2 as shown below.



Lee, Fig. 2 (annotated).

Data transmission operations according to some embodiments of the present invention are illustrated in FIG. 2. The upper portion of FIG. 2, labeled Read, illustrates an operation for reading data from a memory 120 and sending the data to a memory controller 140. To read data from the memory 120, an active command Active (e.g., a row address) is sent to the memory 120 from the memory controller 140. This is accomplished by toggling the first strobe signal SCA during a predetermined time, for example, when the active command Active has been placed on the CA bus. Such operations are illustrated in FIG.2, as the memory controller 140 loads the active command Active on a control bus 160 (identified as CA in FIG. 2) and toggles the first strobe signal SCA while the active command Active is on the control bus 160. The memory 120 latches the active command Active in response to

toggling of the first strobe signal SCA. The memory controller 140 the loads the read command Read (e.g., a column address) on the control bus 160 and toggles the first strobe signal SCA while the read command Read is on the control bus 160. The memory 120 latches the read command Read in response to toggling of the first strobe signal SCA. EX1005, Lee, [0024].

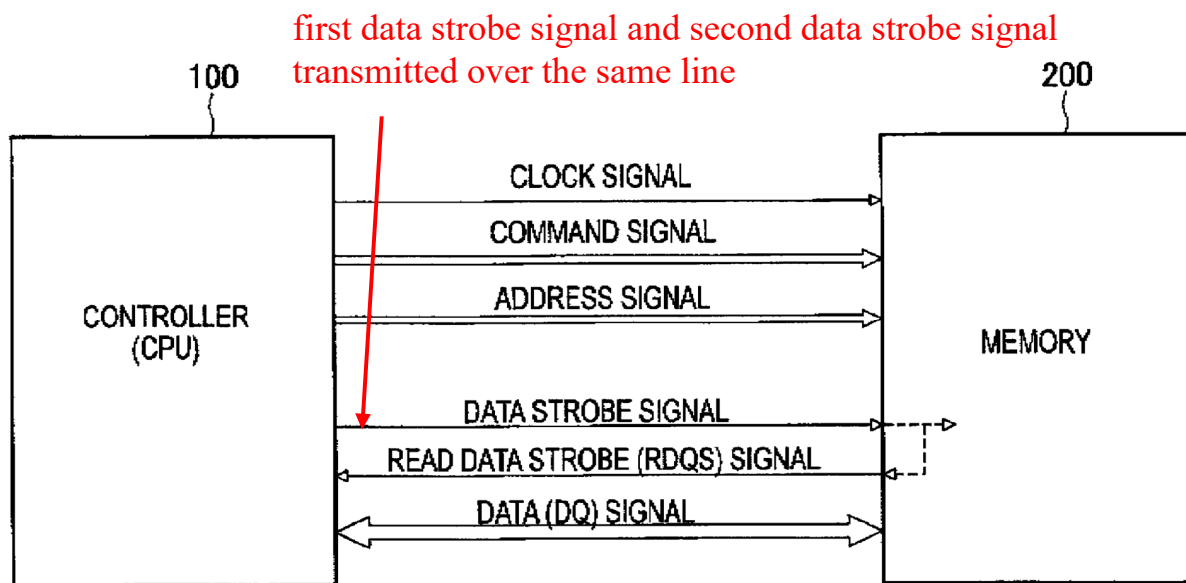
55. Lee further describes what it describes as “conventional operations” in which the memory generates the strobe signal SDfM (“*read data strobe signal*”) in response to receipt of the strobe signal SDtM (“*second data strobe signal*”).

Responsive to receipt of the active command Active and the read command Read, **the data stored in the memory 120 may be read from memory utilizing conventional read operations.** For example, data stored in a memory cell array (not shown) is read out via a read circuit (e.g., a sense amplifier circuit). The read data is transferred to the memory controller 140 from the memory 120 via a data bus 166, based on the control of the memory controller 140. **To send data read from the memory 120 to the memory controller 140, first, the memory controller 140 transfers the second strobe signal SDtM to the memory 120. The memory 120 generates the third strobe signal SDfM in response to the received second strobe signal SDtM.** The third strobe signal SDfM, as illustrated in FIG. 2, may have the same wave form as the second strobe signal SDtM delayed by a predetermined time. The memory 120 loads data on the data bus 166 (illustrated as DATA in FIG. 2) in response to the second strobe signal SDtM and outputs the third strobe signal SDfM while the data is loaded

on the data bus 166. The memory controller 140 latches data DATA loaded on the data bus 166 in response to the third strobe signal SDfM.

EX1005, Lee, [0025].

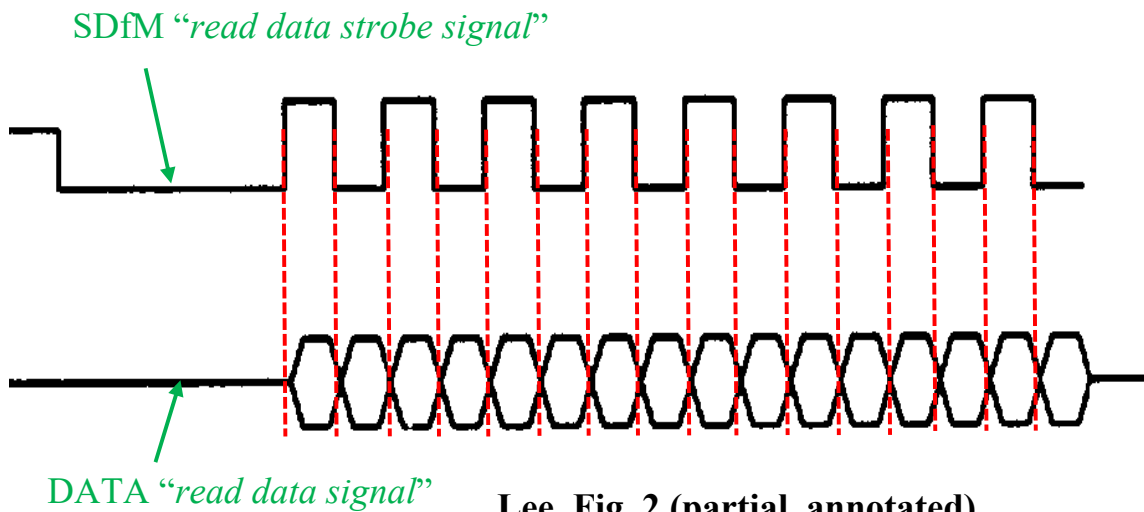
56. Note that the SDtM signal of the read operation (“*second data strobe signal*”) is different than the SDtM signal of the write operation (“*first data strobe signal*”) because they are sent at different times. In other words, while both SDtM signals traverse the same line they are distinct signals because they are sent at different times during different types of operations. The ’369 patent describes the claimed “*first data strobe signal*” and “*second data strobe signal*” similarly being transmitted over the same transmission line. See ’369 patent, Fig. 1.



’369 patent, Fig. 1 (annotated).

57. Second, like the write operation, the SDfM signal (“*read data strobe signal*”) is in synchronization with the read data signal. As can be seen in the

annotated figure below, the rising and falling times of the strobe signal SDfM are synchronized with the switching of the data signal.



58. Accordingly, a POSITA would have understood that the SDfM signal is “in synchronization with” the read DATA signal. Again, a POSITA would have understood that synchronization is done for the purpose of telling the receiving component—in this case the memory—when to sample the data: “The memory controller 140 latches data DATA loaded on the data bus 166 in response to the third strobe signal SDfM.” EX1005, Lee, [0025].

59. Thus, because Lee describes that during a read operation, the memory sends a data signal and a data strobe signal responsive to a signal from the controller, Lee renders obvious “*the controller being adapted, in a read operation, to send out a second data strobe signal and to receive a read data signal in synchronization with a read data strobe signal*” as claimed.

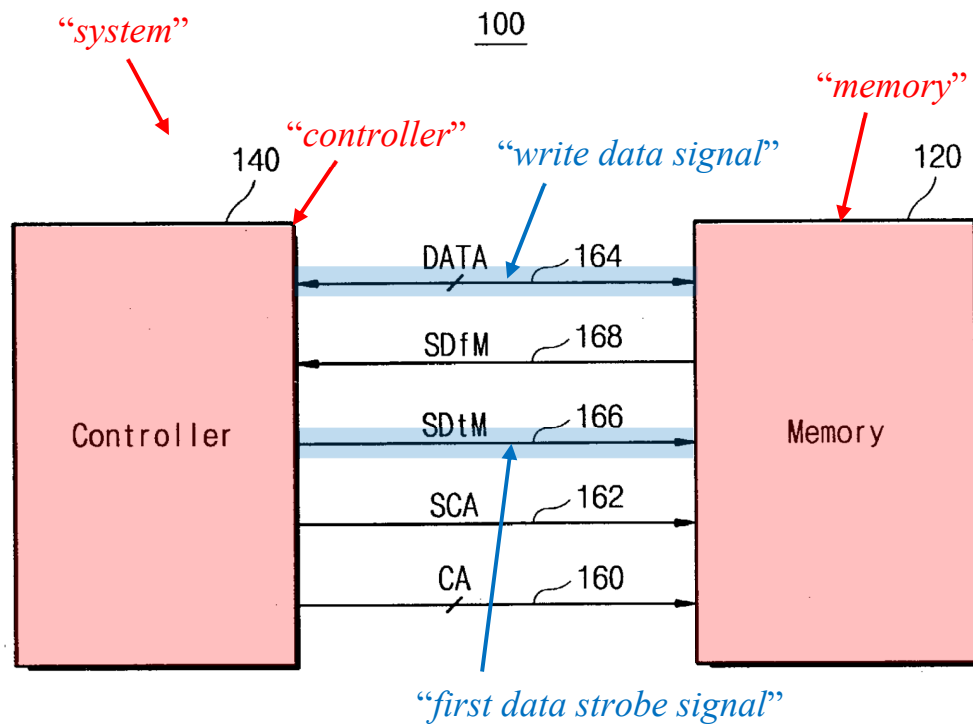
[1.4] *the read data strobe signal being received by the controller in response to the second data strobe signal; and*

60. Lee explains that the SDfM signal is received by the controller in response to transmitting the SDtM signal: “The memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM.” EX1005, Lee, [0021]; *see also* EX1005, Lee, [0024] (“The memory 120 generates the third strobe signal SDfM in response to the received second strobe signal SDtM”).

61. Thus, because Lee’s strobe signal SDfM is received in response to the strobe signal SDtM, Lee renders obvious “*the read data strobe signal being received by the controller in response to the second data strobe signal*” as claimed.

[1.5] *a memory adapted to receive the write data signal in synchronization with the first data strobe signal in the write operation,*

62. First, Lee’s system includes a memory 120 (“memory”), as described above at [1.0] and [1.1].



Lee, Fig. 1 (annotated).

63. **Second**, as described above at [1.2], Lee describes the write operation in which the memory receives strobe signal SDtM (*"first data strobe signal"*) over line 166 and data (*"write data signal"*) over line 164.

64. Thus, because Lee describes a memory that receives the write data signal along with a strobe signal, Lee renders obvious *"a memory adapted to receive the write data signal in synchronization with the first data strobe signal in the write operation"* as claimed.

[1.6] the memory being adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal and to send the read data signal synchronized with the read data strobe signal.

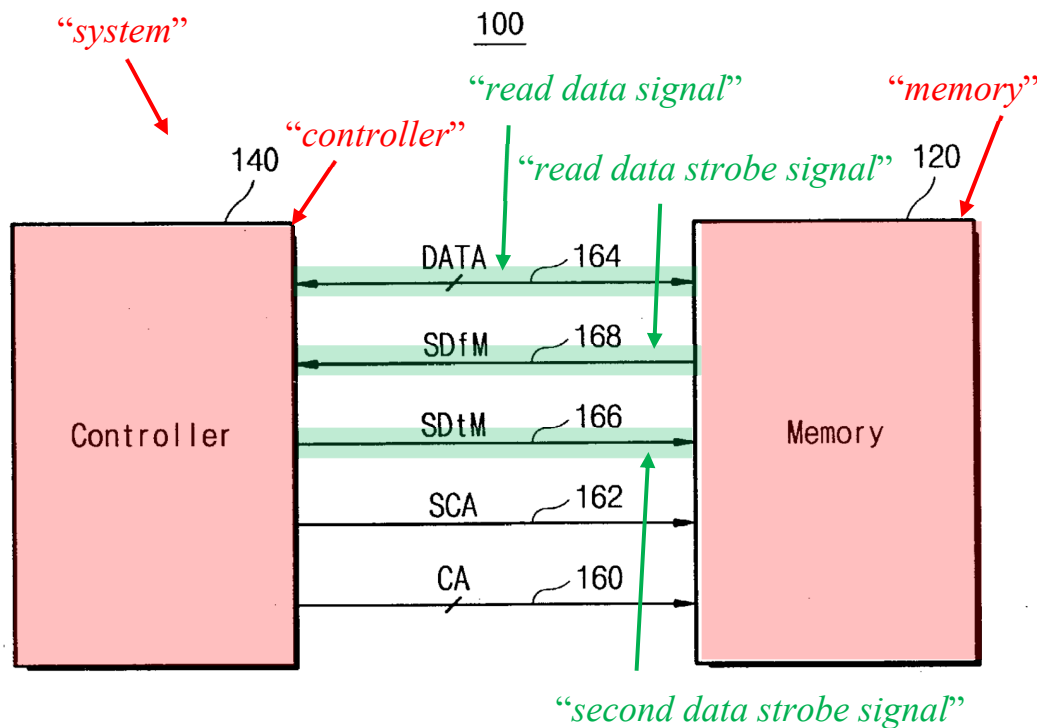
65. As explained above at [1.3] and [1.4], Lee describes a read operation

in which the memory transmits strobe signal SDfM (“*read data strobe signal*”) over line 168 and data (“*read data signal*”) over line 164 in response to receiving the SDtM signal (“*second data strobe signal*”).

For a read operation, in addition to the command/address information CA, **the memory controller 140 transfers to the memory 120 the second strobe signal SDtM as a transmission synchronous or reference signal at a time when it wants to receive data read out from the memory 120. The memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM.**

The read data that is read from the memory 120 is sent to the memory controller 140 together with the third strobe signal SDfM. Therefore, during the read operation the memory controller 140 receives the read data DATA from the memory 120 together with the third strobe signal SDfM at a required time, by sending the second strobe signal SDtM to the memory 120 after it transmits the command and address information to the memory 120.

EX1005, Lee, [0021]; *see also* EX1005, Lee [0025].



Lee, Fig. 1 (annotated).

66. Thus, because Lee's memory system transmits the strobe signal SDfM in response to the SDtM signal, Lee renders obvious *"the memory being adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal and to send the read data signal synchronized with the read data strobe signal"* as claimed.

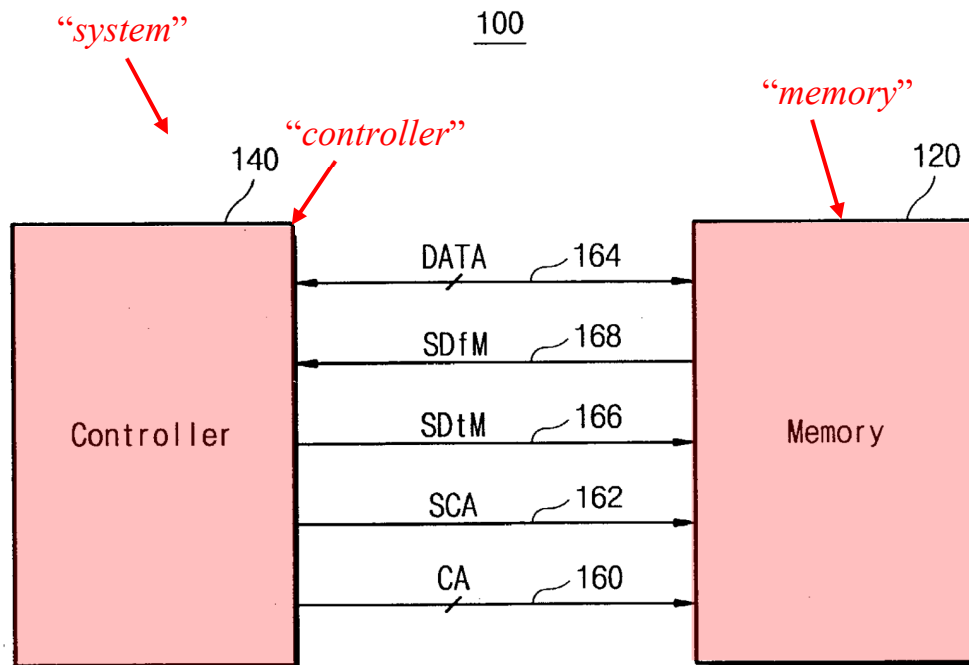
3. Claim 6

[6.0] *A controller for use in a system, the system including a memory,*

67. Lee describes a memory system 100 ("system") that includes a controller 140 ("controller") and a memory 120 ("memory").

A block diagram of a system according to certain embodiments of the present invention is illustrated in FIG. 1. Referring to FIG. 1, **a memory system 100** according to particular embodiments the present invention includes **a memory 120** and **a memory controller 140**. The memory 120 is an asynchronous memory, and can be implemented using non-volatile memories (e.g., FRAM, EEPROM, EPROM, and so on) and volatile memories (e.g., DRAM, SRAM, and so on). With the memory system 100, data transmission between the memory 120 and the memory controller 140 is carried out by a source synchronous interface.

EX1005, Lee, [0017].



Lee, Fig. 1 (annotated).

68. Thus, because Lee describes a memory system with a controller and a memory, Lee renders obvious a “*controller for use in a system, the system*”

including a memory” as claimed.

[6.1] the controller being adapted to send out a first data strobe signal and a write data signal to the memory in a write operation, the write data signal being synchronized with the first data strobe signal,

69. For the reasons explained above at [1.1] and [1.2], Lee renders obvious “*the controller being adapted to send out a first data strobe signal and a write data signal to the memory in a write operation, the write data signal being synchronized with the first data strobe signal*” as claimed.

[6.2] the controller being adapted to send out a second data strobe signal to the memory and to receive a read data signal in synchronization with a read data strobe signal from the memory in a read operation,

70. For the reasons explained above at [1.3], Lee renders obvious “*the controller being adapted to send out a second data strobe signal to the memory and to receive a read data signal in synchronization with a read data strobe signal from the memory in a read operation*” as claimed.

[6.3] the read data strobe signal received by the controller corresponding to the second data strobe signal in the read operation.

71. As explained above at [1.4], Lee’s SDfM signal is received by the controller in response to transmitting the SDtM signal: “The memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM.” EX1005, Lee, [0021]. Because the SDfM signal (“*read data strobe signal*”) is received “in response to” the SDtM signal of the read operation (“*second data strobe signal*”), the SDfM signal *corresponds* to the SDtM signal.

The SDfM signal also corresponds to the SDtM signal in that it has the same form:

“The third strobe signal SDfM, as illustrated in FIG. 2, may have the same wave form as the second strobe signal SDtM.” EX1005, Lee, [0025].

72. Thus, Lee renders obvious “*the read data strobe signal received by the controller corresponding to the second data strobe signal in the read operation*” as claimed.

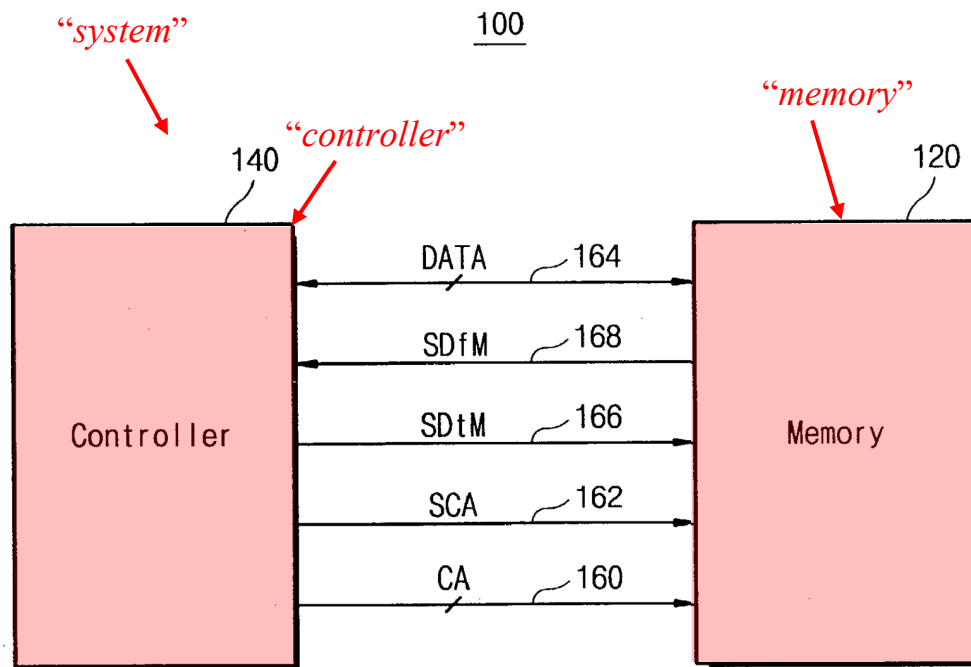
4. Claim 10

[10.0] *A memory for use in a system, the system including a controller,*

73. Lee describes a memory system 100 (“system”) that includes a controller 140 (“controller”) and a memory 120 (“memory”).

A block diagram of a system according to certain embodiments of the present invention is illustrated in FIG. 1. Referring to FIG. 1, **a memory system 100** according to particular embodiments the present invention includes **a memory 120** and **a memory controller 140**. The memory 120 is an asynchronous memory, and can be implemented using non-volatile memories (e.g., FRAM, EEPROM, EPROM, and so on) and volatile memories (e.g., DRAM, SRAM, and so on). With the memory system 100, data transmission between the memory 120 and the memory controller 140 is carried out by a source synchronous interface.

EX1005, Lee, [0017].



Lee, Fig. 1 (annotated).

74. Thus, Lee renders obvious a “*memory for use in a system, the system including a controller*” as claimed.

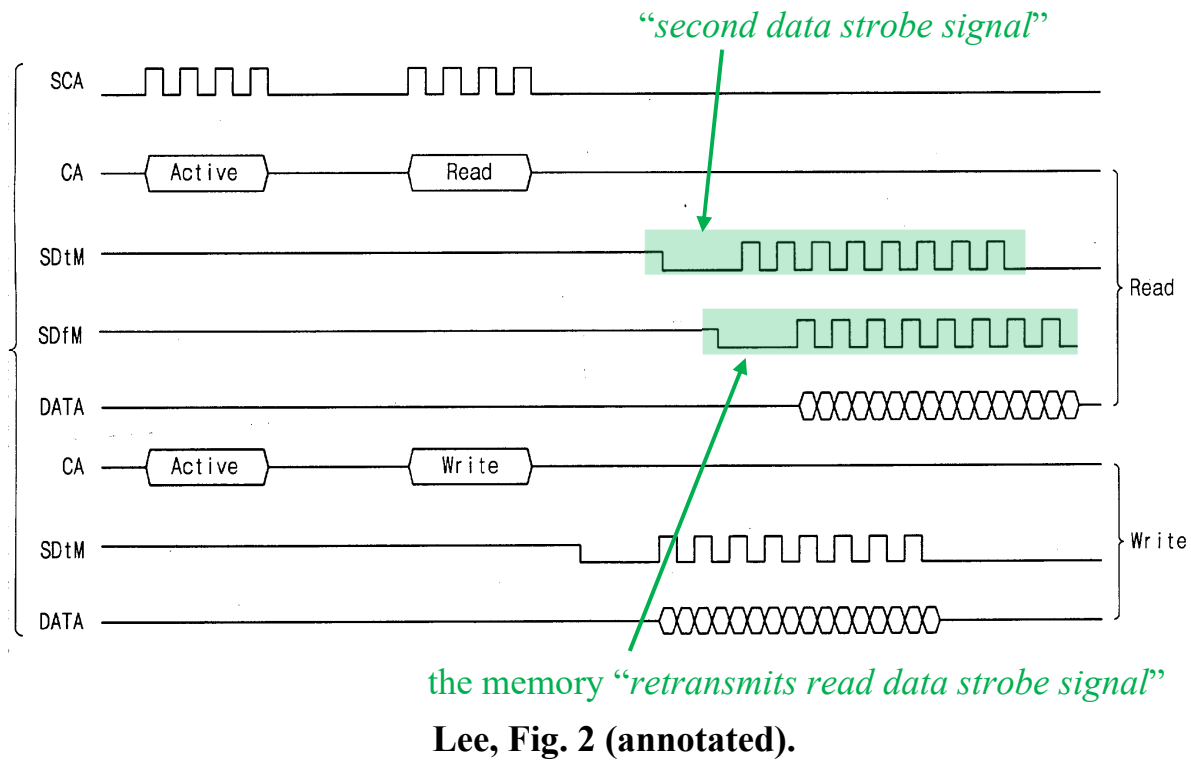
[10.1] *the controller outputting a data strobe signal in a read operation, the memory being adapted to send out a read data strobe signal to the controller in response to the data strobe signal and to send out a read data signal synchronized with the read data strobe signal in a read operation.*

75. For the reasons explained above at [1.3], [1.4], and [1.6], Lee renders obvious “*the controller outputting a data strobe signal in a read operation, the memory being adapted to send out a read data strobe signal to the controller in response to the data strobe signal and to send out a read data signal synchronized with the read data strobe signal in a read operation*” as claimed.

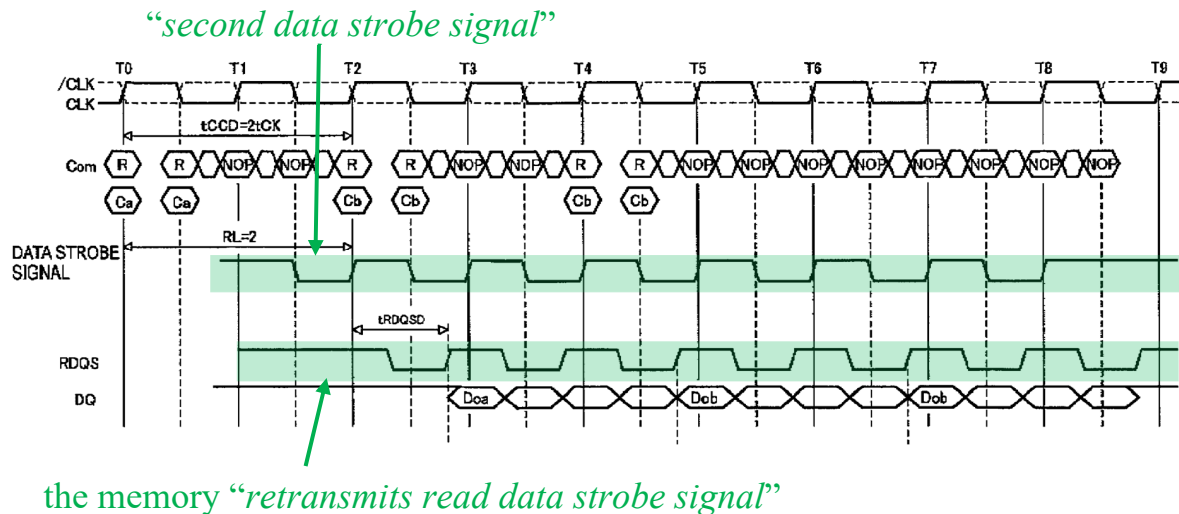
5. Claim 14

[14.1] *The system of claim 1, wherein in the read operation the memory retransmits the second data strobe signal as the read data strobe signal.*

76. Lee explains that “The memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM.” EX1005, Lee, [0021]. Lee also explains that “[t]he third strobe signal SDfM, as illustrated in FIG. 2, **may have the same wave form** as the second strobe signal SDtM delayed by a predetermined time.” EX1005, Lee, [0025]. Thus, by generating the third strobe signal SDfM (“*read data strobe signal*”) that has the same wave form as the received the SDtM signal (“*second data strobe signal*”), the memory system is *retransmitting* the SDtM signal as the SDfM signal. As shown in the figure below, the SDfM signal is identical to the SDtM signal in shape.



77. Notably, Lee describes retransmitting the strobe signal with at least the same level of specificity as the '369 patent, the specification of which does not provide any further explanation as to what it means to "retransmit" the second strobe signal as the read data strobe signal. What Lee explains and illustrates is thus similar to how the '369 patent illustrates the "retransmitted" read data strobe signal.



’369 Patent, Fig. 8 (annotated).

78. Thus, because Lee describes transmitting the strobe signal SDfM with the same waveform as the received SDtM signal, Lee renders obvious “*wherein in the read operation the memory retransmits the second data strobe signal as the read data strobe signal*” as claimed.

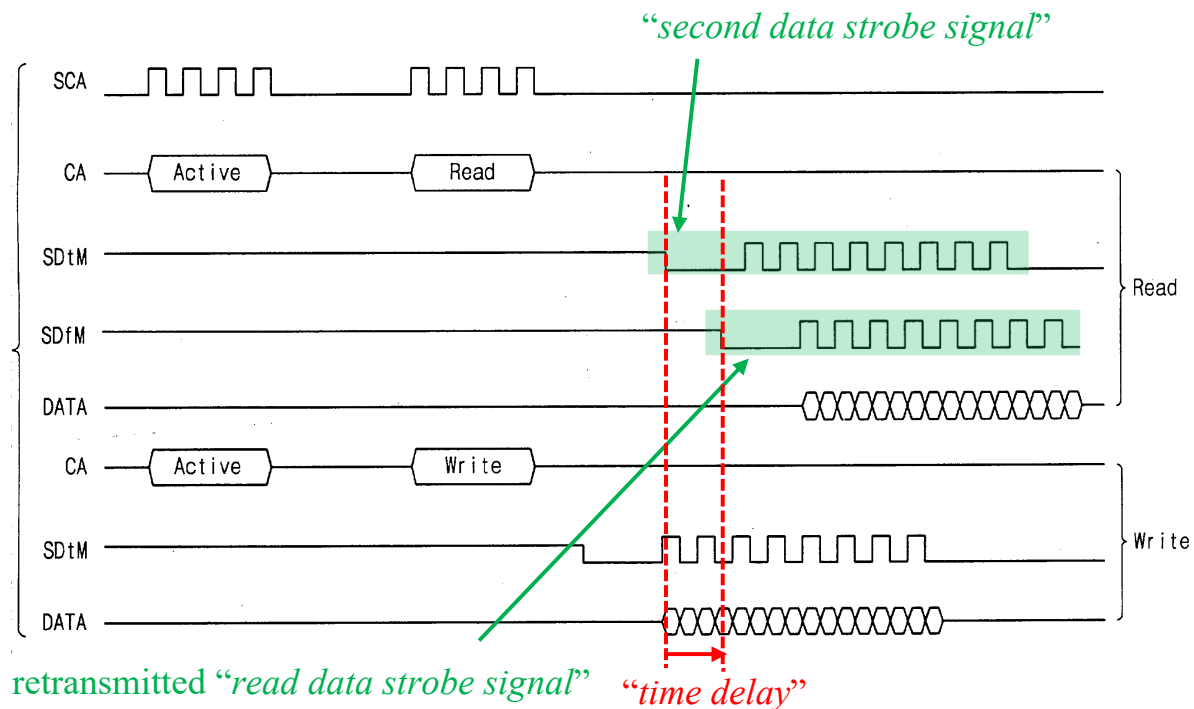
6. Claim 15

[15.1] The system of claim 14, wherein in the read operation the memory retransmits the second data strobe signal with a time delay as the read data strobe signal.

79. Lee explains that “[t]he memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM.” EX1005, Lee, [0021]. Lee also explains that “[t]he third strobe signal SDfM, as illustrated in FIG. 2, **may have the same wave form** as the second strobe signal SDtM **delayed by a predetermined time.**” EX1005, Lee, [0025]. Thus, by generating the third strobe signal SDfM (“*read data strobe signal*”) with the same wave form as the SDtM

signal (“second data strobe signal”) with a predetermined delay, the memory system is *retransmitting* the SDtM signal as the SDfM signal with a time delay.

The time delay can be seen in the figure below.



Lee, Fig. 2 (annotated).

80. Thus, because Lee describes transmitting the strobe signal SDfM with the same wave form as the received SDtM signal with a predetermined delay, Lee renders obvious “*wherein in the read operation the memory retransmits the second data strobe signal with a time delay as the read data strobe signal*” as claimed.

7. Claim 16

[16.1] *The controller of claim 6, wherein in the read operation the controller receives a read data signal from the memory which is a retransmission of the second data strobe signal.*

81. See [14.1].

8. Claim 17

[17.1] *The controller of claim 16, wherein in the read operation the controller receives a read data signal from the memory which is a retransmission of the second data strobe signal with a time delay.*

82. See [15.1].

9. Claim 18

[18.1] *The memory of claim 10, wherein in the read operation the read data strobe signal is a retransmission of the received data strobe signal.*

83. See [14.1].

10. Claim 19

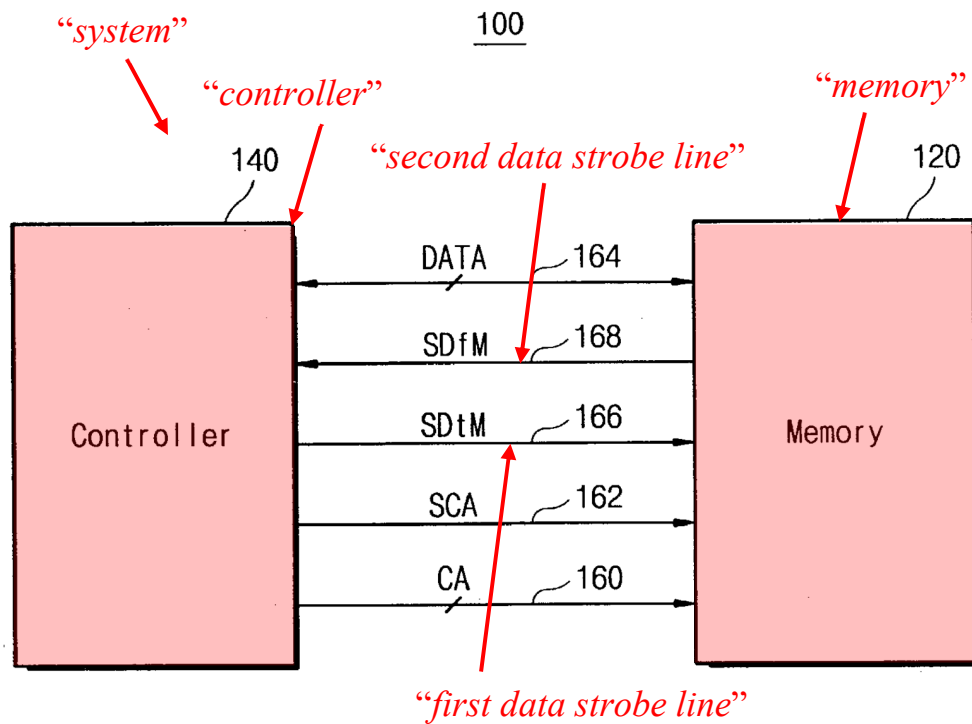
[19.1] *The memory of claim 18, wherein in the read operation the read data strobe signal is a retransmission of the received data strobe signal with a time delay.*

84. See [15.1].

11. Claim 25

[25.1] *The system according to claim 1, further comprising first and second data strobe lines each provided between the controller and the memory, the first data strobe line transferring the first data strobe signal in the write operation from the controller to the memory, the first data strobe line transferring the second data strobe signal in the read operation from the controller to the memory, and the second data strobe line transferring the read data strobe signal in the read operation from the memory to the controller.*

85. First, as explained above at [1.1] and [1.3], Lee's system includes signal lines 166 and 168 ("*first and second data strobe lines*") between the memory and the controller.



EX1005, Lee, Fig. 1 (annotated).

86. **Second**, as explained above at [1.1], the signal line 166 carries the SDtM signal of the write operation (*"the first data strobe line transferring the first data strobe signal in the write operation from the controller to the memory"*): "For a write operation ... the memory controller 140 transfers data DATA to the memory 120 via a data bus 164, and transfers, as a transmission synchronous signal, the second strobe signal SDtM to the memory 120 via a signal line 166." EX1005, Lee, [0020].

87. **Third**, as explained at [1.3], the signal line 166 also carries the SDtM signal of the read operation (*"the first data strobe line transferring the second data strobe signal in the read operation from the controller to the memory"*): "For a

read operation ... the memory controller 140 transfers to the memory 120 the second strobe signal SDtM.” EX1005, Lee, [0020]. *See also* EX1005, Lee, [0021] (“SDtM to the memory 120 **via a signal line 166.**”).

88. Fourth, as also explained at [1.3], the SDfM signal is sent from the memory to the controller during the read operation (*“the second data strobe line transferring the read data strobe signal in the read operation from the memory to the controller”*): “Therefore, during the read operation the memory controller 140 receives the read data DATA from the memory 120 together with the third strobe signal SDfM at a required time.” EX1005, Lee, [0021]. Further, the SDfM signal is sent over line 168. EX1005, Lee, [0033] (“the third strobe signal SDfM transferred via the signal line 168.”).

89. Thus, because Lee’s system includes signal lines 166 and 168 between the memory controller, and the signal lines carry the strobe signals of the read and write operations, Lee renders obvious *“further comprising first and second data strobe lines each provided between the controller and the memory, the first data strobe line transferring the first data strobe signal in the write operation from the controller to the memory, the first data strobe line transferring the second data strobe signal in the read operation from the controller to the memory, and the second data strobe line transferring the read data strobe signal in the read operation from the memory to the controller”* as claimed.

12. Claim 26

[26.0] A controller comprising a first terminal, a second terminal, and a third terminal,

90. First, Lee describes a memory system 100 that includes a controller 140 (“*controller*”) and a memory 120.

A block diagram of a system according to certain embodiments of the present invention is illustrated in FIG. 1. Referring to FIG. 1, **a memory system 100** according to particular embodiments the present invention includes **a memory 120** and **a memory controller 140**. The memory 120 is an asynchronous memory, and can be implemented using non-volatile memories (e.g., FRAM, EEPROM, EPROM, and so on) and volatile memories (e.g., DRAM, SRAM, and so on). With the memory system 100, data transmission between the memory 120 and the memory controller 140 is carried out by a source synchronous interface.

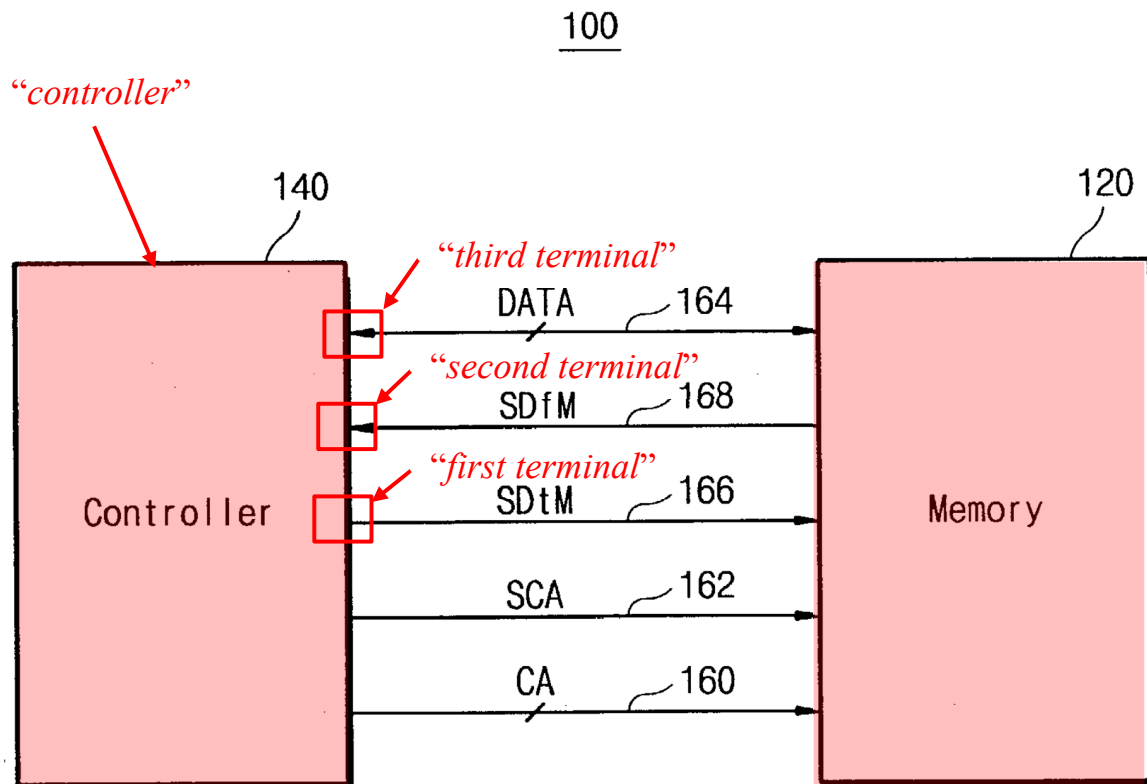
EX1005, Lee, [0017].

91. Lee explains that communication between a memory and a controller uses “pins.”

As is known to those of skill in the art, a memory typically provides external communications with, for example, a memory controller or chipset, **via pins (e.g., data pins, address pins, control pins, power pins, and so on)**. In a conventional mobile processing system, the memory and the memory controller are, typically, interconnected in a point-to-point fashion.

EX1005, Lee, [0006].

92. A POSITA would have understood that the pins for the communication lines 164, 166, and 168 may be referred to as terminals as well. Such terminals are shown in the annotated Fig. 1 below.



Lee, Fig. 1 (annotated).

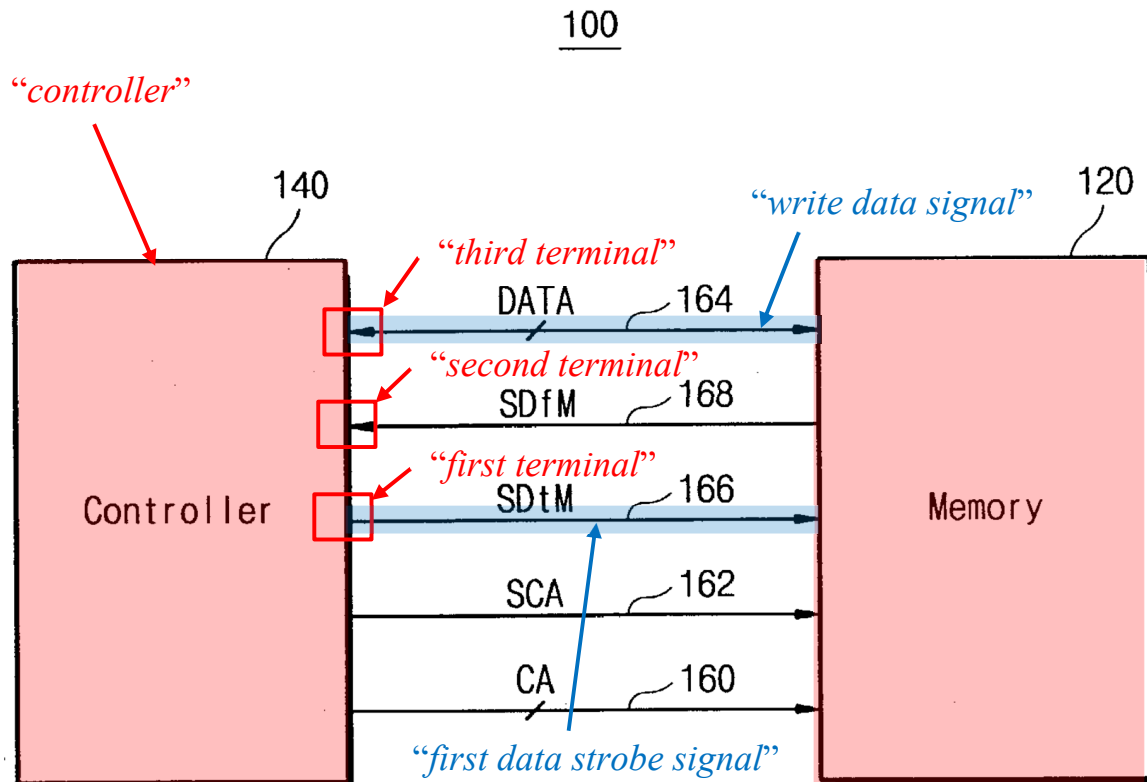
93. Thus, because Lee's controller includes pins for communicating with the memory, Lee renders obvious a "*controller comprising a first terminal, a second terminal, and a third terminal*" as claimed.

[26.1] the controller being adapted to produce a first data strobe signal at the first terminal and a write data signal at the third terminal in a write operation, the write data signal being synchronized with the first data strobe signal,

94. First, Lee describes the write operation in which the controller transmits strobe signal SDtM (“*first data strobe signal*”) over line 166 (“*first terminal*”) and data (“*write data signal*”) over line 164 (“*third terminal*”).

For a write operation, in addition to the command/address information CA, the memory controller 140 transfers data DATA to the memory 120 via a data bus 164, and transfers, as a transmission synchronous signal, the second strobe signal SDtM to the memory 120 via a signal line 166. In particular, for a write operation, the write data DATA is sent to the memory 120 from the memory controller 140 together with the second strobe signal SDtM based on the source synchronous interface. The memory 120 latches the write data DATA in response to the second strobe signal SDtM.

EX1005, Lee, [0020].



Lee, Fig. 1 (annotated).

95. Second, Lee explains that the data signal is synchronous with the data strobe signal SDtM: “For a write operation ... the memory controller 140 transfers data DATA to the memory 120 via a data bus 164, and transfers, as a transmission synchronous signal, the second strobe signal SDtM to the memory 120 via a signal line 166.” EX1005, Lee, [0020].

96. Thus, because Lee describes a controller 140 that transmits a strobe signal SDtM and a data signal over lines 166 and 164 respectively, Lee renders obvious “the controller being adapted to produce a first data strobe signal at the

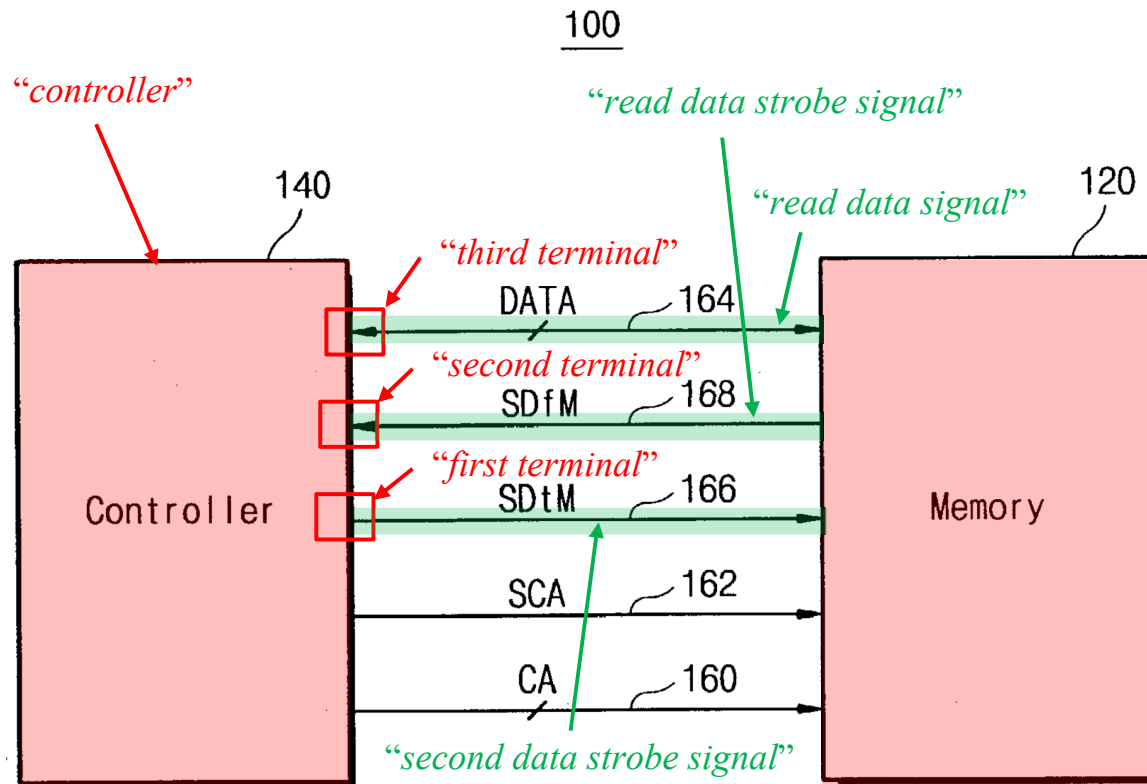
first terminal and a write data signal at the third terminal in a write operation, the write data signal being synchronized with the first data strobe signal” as claimed.

[26.2] the controller being adapted to produce a second data strobe signal at the first terminal and to receive a read data signal at the third terminal in synchronization with a read data strobe signal arriving at the second terminal from outside of the controller in a read operation.

97. First, consistent with the discussion above at [1.3], Lee describes a read operation in which the memory (which is “*from outside the controller*”) transmits strobe signal SDfM (“*read data strobe signal*”) over line 168 (“*second terminal*”) and data (“*read data signal*”) over line 164 (“*third terminal*”) in response to the SDtM signal (“*second data strobe signal*”).

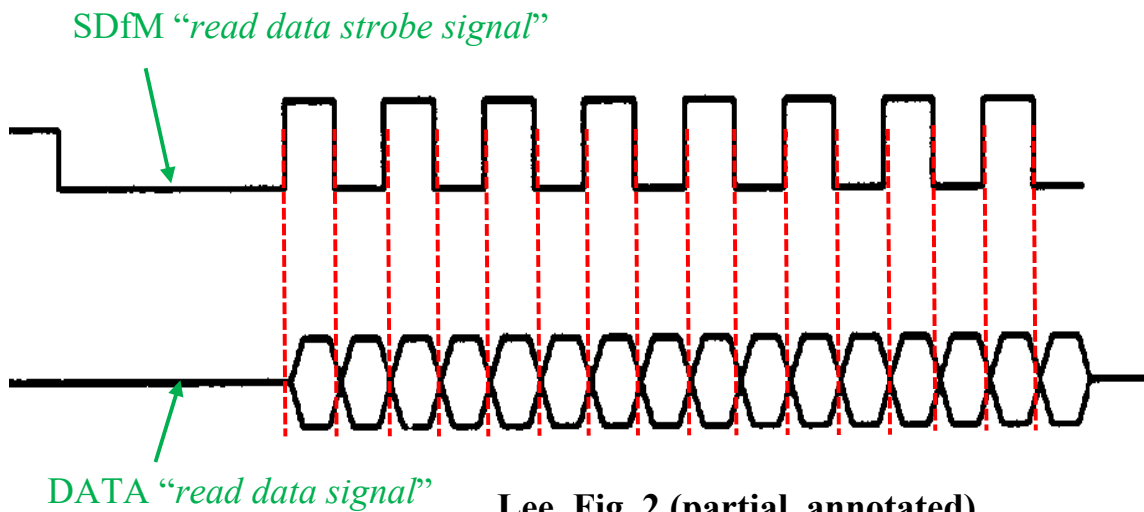
For a read operation, in addition to the command/address information CA, **the memory controller 140 transfers to the memory 120 the second strobe signal SDtM as a transmission synchronous or reference signal at a time when it wants to receive data read out from the memory 120. The memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM.** The read data that is read from the memory 120 is sent to the memory controller 140 together with the third strobe signal SDfM. Therefore, during the read operation the memory controller 140 receives the read data DATA from the memory 120 together with the third strobe signal SDfM at a required time, by sending the second strobe signal SDtM to the memory 120 after it transmits the command and address information to the memory 120.

EX1005, Lee, [0021].



Lee, Fig. 1 (annotated).

98. **Second**, like the write operation, the SDfM signal (*"read data strobe signal"*) is in synchronization with the read data signal. As can be seen in the annotated figure below, the rising and falling times of the strobe signal SDfM are synchronized with the switching of the data signal.



99. Accordingly, a POSITA would have understood that the SDfM signal is “in synchronization with” the read DATA signal. Again, a POSITA would have understood that synchronization is done for the purpose of telling the receiving component—in this case the memory—when to sample the data: “The memory controller 140 latches data DATA loaded on the data bus 166 in response to the third strobe signal SDfM.” EX1005, Lee, [0025].

100. Thus, because Lee describes memory that transmits a data signal over line 164 and a strobe signal SDfM over line 168 responsive to a strobe signal SDtM over line 166, Lee renders obvious “the controller being adapted to produce a second data strobe signal at the first terminal and to receive a read data signal at the third terminal in synchronization with a read data strobe signal arriving at the second terminal from outside of the controller in a read operation” as claimed.

13. Claim 27

[27.1] *The controller according to claim 26, wherein the read data strobe signal is generated outside of the controller in response to the second data strobe signal.*

101. Lee explains that the SDfM signal is generated by the memory (“*outside of the controller*”): “The memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM.” EX1005, Lee, [0021]. Furthermore, as explained above at [1.3] and [1.4], the strobe signal SDfM (“*read data strobe signal*”) is generated “in response to” receiving the strobe signal SDtM (“*second data strobe signal*”).

102. Thus, because Lee’s memory generates the strobe signal SDfM in response to the strobe signal SDtM, Lee renders obvious “*the read data strobe signal being received by the controller in response to the second data strobe signal*” as claimed.

B. Ground 2: Claims 2, 7, and 11 are Obvious in View of Lee and JEDEC

103. As I will explain below, it would have been obvious to a POSITA to implement Lee’s the SCA signal as a continuous clock signal, consistent with the JEDEC standard for memory systems.

1. Summary of JEDEC

104. The Joint Electron Device Engineering Council (JEDEC) is a standard setting body in the electronics industry. The JEDEC Solid State Technology

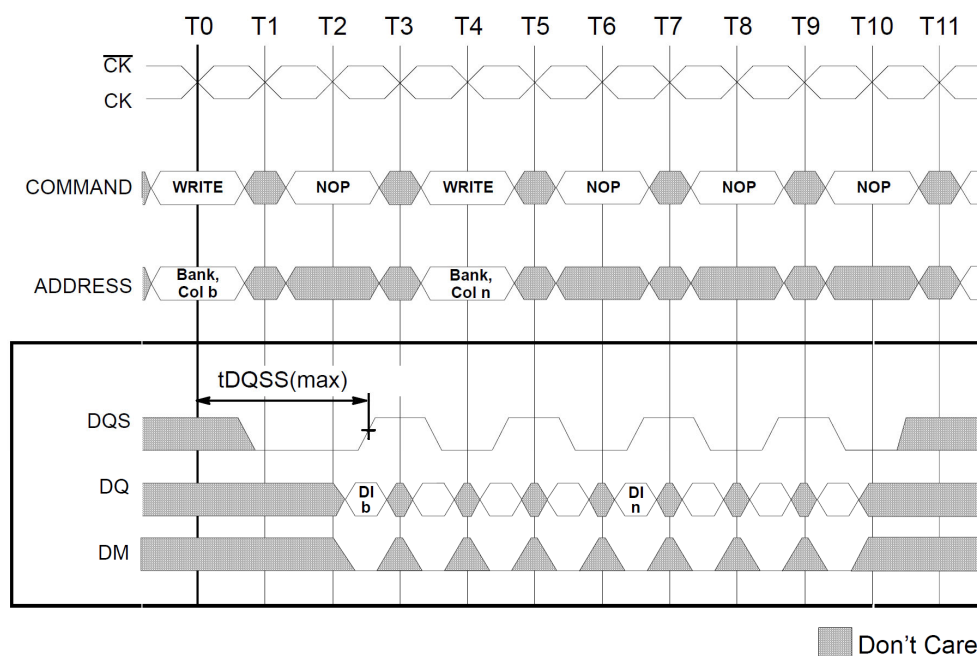
Association produces standards related to memory devices. For example, version JESD79C (EX1007, “JEDEC”) describes standards for Double Data Rate (DDR) SDRAM. JEDEC, 1. The JEDEC Standard: Double Data Rate (DDR) SDRAM Specification, JESD79C is an industry standards document that is dated March of 2003. The metadata of Exhibits 1007 indicates a creation date of March 31, 2003 and a modified date of April 30, 2003.

105. Exhibit 1007 was obtained from the Internet Archive at the following URL: “<https://web.archive.org/web/20030609052112/http://www.jedec.org/download/search/JESD79C.pdf>”. The availability of the JEDEC standard from the Internet Archive shows that the standards document was readily available at the JEDEC website (www.jedec.org). Furthermore, POSITAs at the time the ’369 patent was filed would have been familiar with various industry standards for memory systems, including JEDEC and ONFI (Open NAND Flash Interface). POSITAs would have relied on publicly available standards documents, such as JESD79C for memory system design.

106. Furthermore, various patents, which predate the filing of the ’369 patent, refer to the JESD79C standards document. EX1009, Streif, 3:17-20 (“The JEDEC DDR SDRAM technical standard is published in a document entitled “JEDEC Standard—Double Data Rate (DDR) SDRAM Specification—JESD79C (Revision of JESD79B),” published March 2003, which is herein included by

reference”); EX1010, Simeral, [0009] (“DDR is defined in the JEDEC specification JESD79C, adopted in September, 2003”).

107. The JEDEC standard describes using a clock signal CK that is synchronized with command signals. As shown in the figure below, the CK signal is a continuous clock signal that is synchronized with the command signal.



JEDEC, 34.

2. Motivation to Combine Lee and JEDEC

108. A POSITA would have found it obvious to implement Lee’s SCA signal in any of a variety of known and suitable ways—in either a synchronous or asynchronous manner. Lee’s SCA signal is used to latch command/address information: “That is, the command/address information CA is transferred to the memory 120 from the memory controller 140 together with the first strobe signal

SCA based on the source synchronous interface. The memory 120 latches the command/address information CA in response to the first strobe signal SCA.”

EX1005, Lee, [0019]. Lee further explains that the SCA signal is applied intermittently: The SCA signal “can be implemented using a clock signal that is toggled only during a desired period, for example, when data is on the CA bus or the DATA bus.” EX1005, Lee, [0035]. Using such an intermittent signal is an example of asynchronous memory. *See supra*, V.C.

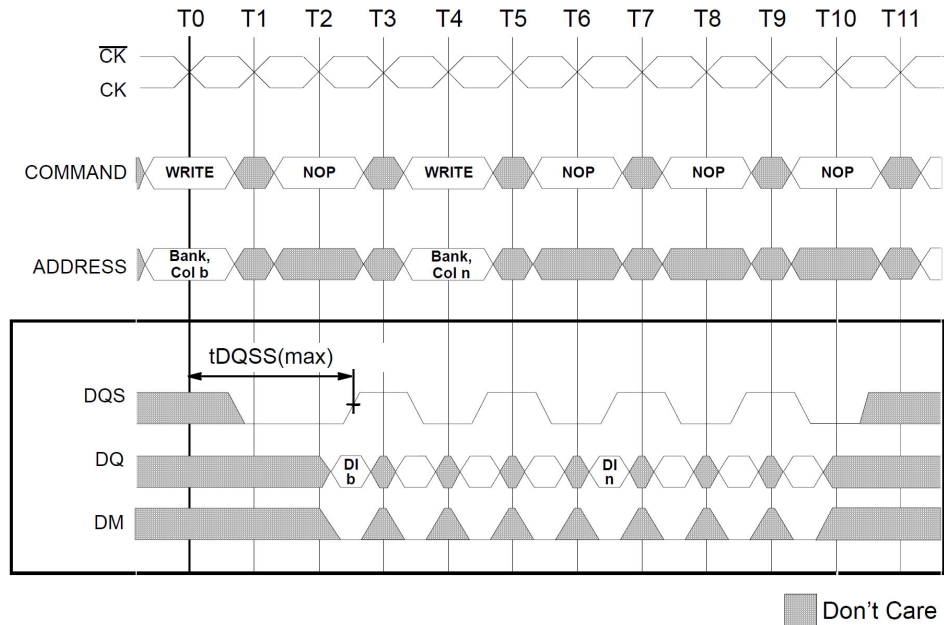
109. While Lee describes using the SCA signal, which is an intermittent strobe signal such as is often used in asynchronous memory, a POSITA would have found it obvious to implement to use a continuous clock signal, such as is often used in synchronous memory. Lee provides evidence that it was known to use either synchronous or asynchronous memory. As Lee explains, “the amount of current consumed by a memory system in a standby state results from the clock signal used to synchronize operations **of a synchronous memory**.” EX1005, Lee, [0034]. Lee chooses to use an asynchronous memory. “[A]ccording to embodiments of the present invention, as illustrated for example in FIG. 3, the strobe signals, such as SCA and SDtM, that are used as transmission references or synchronous signals, are used in the memory 120 only as a latch enable or latching signal.” EX1005, Lee, [0034]. “This means that the memory 120 performs read and write operations **in an asynchronous manner**, for example, using a delay

chain as a state machine.” EX1005, Lee, [0034].

110. A POSITA would have understood that there are design tradeoffs between using a synchronous device interface based on a continuous clock signal, and an asynchronous device interface with a non-continuous strobe signal. For example, asynchronous memory can provide the benefit of less power consumption, as explained by Lee. *See* EX1005, Lee, [0034]. Synchronous memory—using a continuous clock—provides the benefit of higher bandwidth capabilities. *See*, Prince, 5. Indeed, POSITAs used systems that had the capability to switch between synchronous and asynchronous modes. *See generally* EX1008, Mills, title, abstract. Accordingly, a POSITA implementing a memory system according to Lee’s teachings would have found it obvious to use either synchronous or asynchronous memory, as either was a suitable option depending on the characteristics considered most important. If a POSITA wanted to design the system that emphasized power conservation, they could choose Lee’s asynchronous option. If a POSITA wanted to design the memory system that emphasized high bandwidth, they could choose the synchronous option. These are well-known options to a POSITA. That is, any modifications to Lee to accommodate a synchronous option, such as changing Lee’s input latches to registers, are well-known and extremely common skills of a POSITA.

111. POSITAs knew how to implement memories using a continuous clock

because industry standards defined how to do so. The JEDEC standard is an example. As explained above, the JEDEC standard defines the use of a continuous clock signal that is transmitted from the controller to the memory.



JEDEC, 34.

112. As can be seen from the figure above, the command and address lines are synchronized with the clock signal CK . Accordingly, a POSITA would have found it obvious to implement Lee's SCA signal using a continuous clock, consistent with the JEDEC standard. The results of using a standardized process such as the one described in the JEDEC standard would have been predictable because standardized techniques are heavily vetted: "JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Council level and subsequently reviewed and approved by the

EIA General Counsel.” EX1007, JEDEC, 2. For this reason, a POSITA also would have had a reasonable expectation of success. Further still, there is a general familiarity and ease-of-design in the art using synchronous devices and a continuous clock, as evidenced by the JEDEC Standard, that would motivate a POSITA to use a continuous clock for the memory device of Lee.

113. Thus, the combination of Lee and JEDEC is merely a substitute of one known element (Lee’s intermittent SCA signal) with another (standardized continuous clock) to obtain predictable results.

3. Claim 2

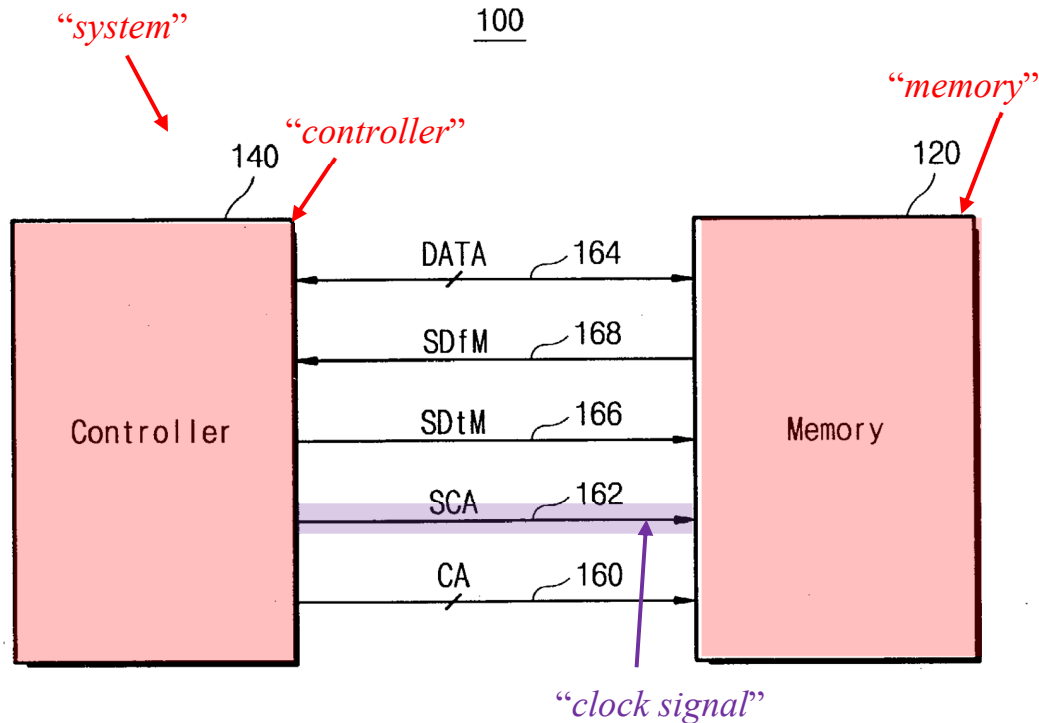
[2.1] *The system according to claim 1, wherein the controller is further adapted to produce a clock signal and to send the clock signal to the memory, each of the first and the second data strobe signals and the read data strobe signal being independent of and separated from the clock signal.*

114. First, Lee’s memory controller produces the SCA signal (“*clock signal*”) which is sent from the controller to the memory.

As is further illustrated in FIG. 1, the memory controller 140 sends command/address information CA for a read/write operation to the memory 120 via a control bus 160. **The memory controller 140 sends the first strobe signal SCA as a transmission reference or synchronous signal to the memory 120 via a signal line 162.** That is, the command/address information CA is transferred to the memory 120 from the memory controller 140 together with the first strobe signal SCA based on the source synchronous interface. The memory 120

latches the command/address information CA in response to the first strobe signal SCA.

EX1005, Lee, [0019]. Fig. 2 below shows Lee's SCA signal, which could be implemented as a continuous clock signal as described at VIII.B.2.



Lee, Fig. 1 (annotated).

115. Lee explains that the SCA signal can be implemented using a clock signal:

According to embodiments of the present invention, **the strobe signals SCA and SDtM can be provided by any method known to those of skill in the art that provide the signal as described herein. For example, a strobe signal can be implemented using a clock signal that is toggled only during a desired period, for example, when data**

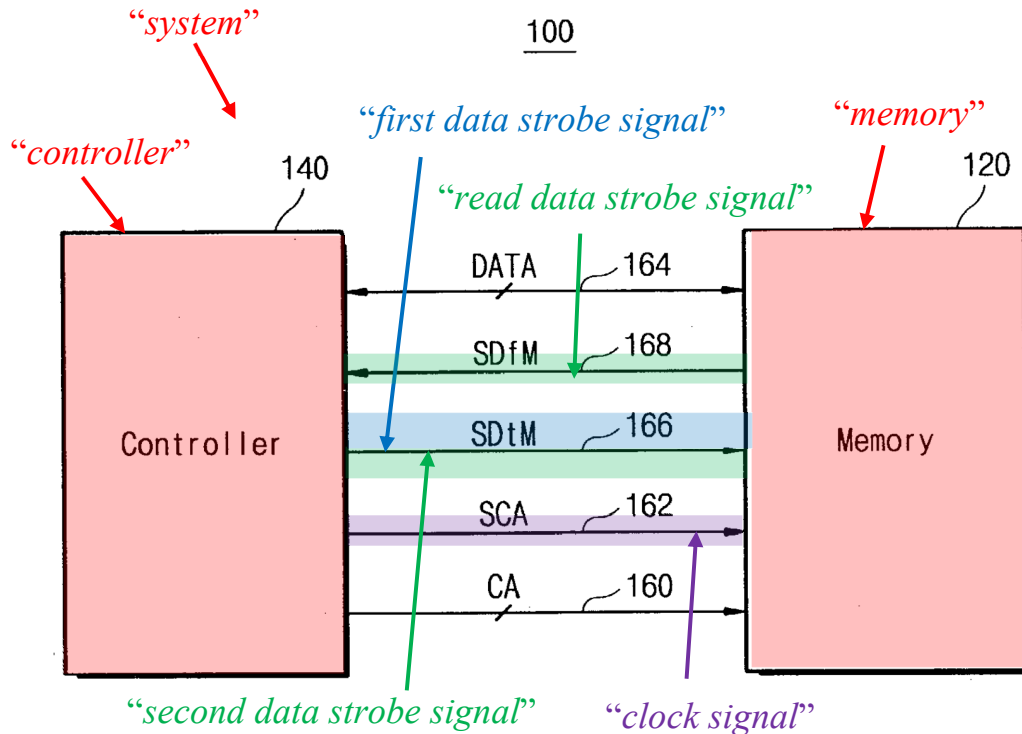
is on the CA bus or the DATA bus. Alternatively, the strobe signal can be implemented so as to have a preamble interval and a valid interval. For example, as illustrated in FIG. 2, a strobe signal is set to a low level (or a high level) during the preamble interval so that the driver and/or the input buffer is activated, and is toggled during the valid interval. At this time, a latch latches information loaded on the control/data bus in response to the toggled strobe signal, as valid information.

EX1005, Lee, [0035]. Thus, a POSITA would understand that the SCA signal *is* a “*clock signal*” during the above-described desired period. It would have been obvious to modify Lee to use a continuous clock, as discussed above at VIII.B.2. Also, if the Patent Owner points to how Lee uses latches instead of registers on the inputs, this is describing how the SCA signal is being used by the device, and not whether the SCA signal is a “*clock signal*.”

116. Furthermore, Lee’s controller is “*adapted to produce*” the SCA signal because the controller *generates* the SCA signal: “In FIG. 3, input/output interface circuits of a memory controller 140 are illustrated, however, additional function of the memory controller may be provided, for example, **to control the generation of** the signals SDtM CON, **SCA CON**, and CA CON.” EX1005, Lee, [0029].

117. Second, Lee’s SCA signal is independent from the other signals SDtM and SDfM, given that the SCA signal is sent across a different transmission line. Specifically, the SCA signal is sent over line 162, while SDtM (“*first data strobe signal*” in the write operation and “*second data strobe signal*” in the read

operation) signals are sent over line 166 and the SDfM signal (“*read data strobe signal*”) is sent over line 168. Fig. 2 below shows Lee’s system with the SCA signal implemented as a clock signal per the JEDEC standards, as described at VIII.B.2



Lee, Fig. 1 (annotated).

118. The SCA signal in Lee serves the same function as the clock signal described in the '369 patent. In Lee, the SCA signal is used to let the memory know when to sample data from the command/address lines: “That is, the command/address information CA is transferred to the memory 120 from the memory controller 140 together with the first strobe signal SCA based on the source synchronous interface. The memory 120 latches the command/address

information CA in response to the first strobe signal SCA.” EX1005, Lee, [0019].

119. Similarly, the ‘369 patent itself explains that “the internal clock signal is sent to the memory 200 via the buffer as the clock signal.” ’369 patent, 4:8-9. The memory system, “upon receiving the clock signal” then sends the “clock signal to circuits for command/address and so on.” ’369 patent, 4:66-5:1; *see also* Fig. 3. A POSITA would have thus understood that the SCA signal in Lee is analogous to the clock signal recited in claim 2.

120. Thus, because Lee’s controller generates and sends the SCA signal to the memory, and the SCA signal may be implemented as a clock signal that is independent from the data transfer strobe signals, Lee renders obvious “*wherein the controller is further adapted to produce a clock signal and to send the clock signal to the memory, each of the first and the second data strobe signals and the read data strobe signal being independent of and separated from the clock signal*” as claimed.

4. Claim 7

[2.1] *The controller according to claim 6, wherein the controller is further adapted to produce a clock signal and to send the clock signal to the memory, each of the first and the second data strobe signals and the read data strobe signal being independent of and separated from the clock signal.*

121. *See* [2.1].

5. Claim 11

[11.1] *The memory according to claim 10, the controller being further adapted to*

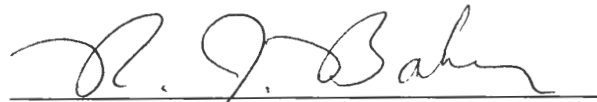
send out a clock signal and to send the clock signal to the memory, wherein each of the data strobe signal and the read data strobe signal is independent of and separated from the clock signal.

122. See [2.1].

IX. CONCLUSION

123. This declaration and my opinions herein are made to the best of my knowledge and understanding, and based on the material available to me, at the time of signing this declaration. I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: July 13, 2023


R. Jacob Baker, Ph.D., P.E.