

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

LONGITUDE LICENSING LTD.,
Patent Owner.

IPR2023-01200
Patent 7,697,369 B2

Before RICHARD M. LEBOVITZ, DAVID C. McKONE, and
KEVIN C. TROCK, *Administrative Patent Judges*.

TROCK, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Western Digital Technologies, Inc. (“Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting *inter partes* review of claims 1, 2, 6, 7, 10, 11, 14–19, and 25–27 (the “challenged claims”) of U.S. Patent No. 7,697,369 B2 (Ex. 1001, “the ’369 patent”). Longitude Licensing LTD. (“Patent Owner”) (Paper 4, 1) did not file a Preliminary Response.

The Board has authority to determine whether to institute *inter partes* review. *See* 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). Under 35 U.S.C. § 314(a), we may not authorize an *inter partes* review unless the information in the petition and the preliminary response “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

For the reasons stated below, we determine that Petitioner has established a reasonable likelihood that it would prevail with respect to at least one claim. We therefore institute *inter partes* review as to all of the challenged claims of the ’369 patent and all of the asserted grounds of unpatentability in the Petition.

II. BACKGROUND

A. Related Matters

Petitioner identifies the following district court proceedings involving the ’369 patent:

1. *Longitude Licensing Limited v. ASUSTeK Computer Inc. et al.*, Case No. 8-23-cv-00033 (C.D. Cal.) (filed Jan. 9, 2023).
2. *Longitude Licensing Limited v. Lenovo Group Limited et al.*, Case No. 8-23-cv-00035 (C.D. Cal.) (filed Jan. 9, 2023).

3. *Longitude Licensing Limited v. Acer Inc. et al.*, Case No. 8-23-cv-00036 (C.D. Cal.) (filed Jan. 9, 2023).

4. *Longitude Licensing Limited v. HP Inc.*, Case No. 8-23-cv-00038 (C.D. Cal.) (filed Jan. 9, 2023).

5. *Longitude Licensing Limited v. Amazon.com, Inc.*, Case No. 8-23-cv-00039 (C.D. Cal.) (filed Jan. 9, 2023) (“Amazon Action”).

6. *Longitude Licensing Limited v. Dell Technologies Inc. et al.*, Case No. 8-22-cv-02312 (C.D. Cal.) (filed Dec. 23, 2022¹).
Pet. 69–70.

Each of the above actions (with the exception of the Amazon Action with respect to Petitioner) is stayed pending the resolution of the Amazon Action. Ex. 1011.

Patent Owner identifies the same six related matters. Paper 4, 1–2.

B. Real Parties-in-Interest

Petitioner identifies Western Digital Technologies, Inc. as the real party-in-interest. Pet. 68. Petitioner states that (1) the six cases identified above involve Petitioner’s customers as defendants, (2) Petitioner submits that Petitioner is the only real party-in-interest (“RPI”), and (3) “regardless of whether any defendant should be named as an RPI, no RPI analysis is necessary because there are no time bar or estoppel implication for any defendant.” *Id.*

Patent Owner identifies Longitude Licensing LTD. as the real party-in-interest. Paper 4, 1.

¹ Petitioner incorrectly identified the filing date as Dec. 23, 2023.

Based on the current record, we determine that Petitioner has established compliance with the statutory requirement under 35 U.S.C. § 312(a)(2) to identify all real parties in interest.

C. The '369 Patent

The '369 patent is entitled “System with Controller and Memory.” Ex. 1001, code (54). The patent “relates to a system having a controller and a memory and, more particularly, to a data sending/receiving operation between the controller and the memory.” *Id.* at 1:6–8.

The '369 patent explains that “[i]n a conventional data sending/receiving operation between the controller and the memory, either the controller or the memory who serves as a sender generates a data strobe signal which is synchronized with a clock signal.” *Id.* at 1:9–12. The patent further explains “[i]t is an object of the ['369] invention to provide a system based on a new protocol which is different from the above-described conventional techniques.” *Id.* at 1:25–27.

Figure 1 of the '369 patent, reproduced below, is a schematic block diagram of a system according to one embodiment. *Id.* at 2:12–14.

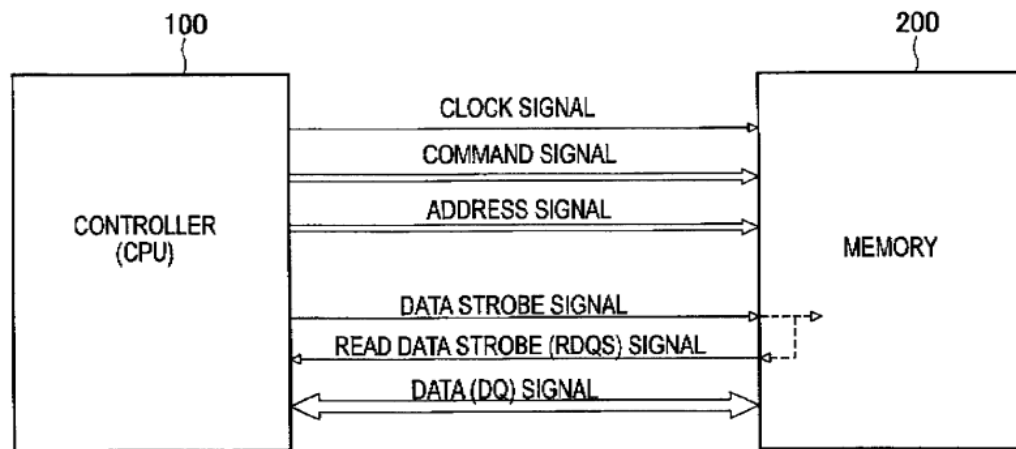


Figure 1, shown above, depicts controller 100 and memory 200. *Id.* at 3:6–11. Controller 100 outputs a clock signal, command signal, and address

signal to memory 200. *Id.* Controller 100 also outputs and receives data (DQ) signal to/from memory 200. *Id.*

In a write operation, controller 100 sends out a first data strobe signal and also sends out a write data signal over the DQ signal line, as shown in Figure 1, above. *See id.* at 3:12–25. In a write operation, memory 200 receives the write data signal in synchronization with the first data strobe signal. *Id.*

In a read operation, controller 100 sends out a second data strobe signal and receives a read data signal over the DQ signal line in synchronization with a read data strobe (RDQS) signal. *Id.* The RDQS signal corresponds to the second data strobe signal. *Id.* The '369 patent explains that “memory 200 is adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal and to send out the read data signal synchronized with the read data strobe signal.” *Id.*

The '369 patent describes the following advantages:

In the system according to the first embodiment, the write/read operations to/from the memory 200 are controlled by the data strobe signal outputted from the controller 100. The write and the read operations can be carried out without the use of and independently from the clock signal. Therefore, it is not necessary for the memory 200 to produce the data strobe signal from the clock signal nor to make the read data strobe signal synchronize with the clock signal.

Id. at 3:37–44.

D. Illustrative Claim

The '369 patent has 27 claims. Claims 1, 6, 10, and 26 are the independent claims challenged. Claim 1 is illustrative of the claimed subject matter and is reproduced below, with bracketed annotations added:

1. [1.0] A system comprising:
 - [1.1] a controller adapted to send out a first data strobe signal and a write data signal in a write operation, [1.2] the write data signal being synchronized with the first data strobe signal, [1.3] the controller being adapted, in a read operation, to send out a second data strobe signal and to receive a read data signal in synchronization with a read data strobe signal, [1.4] the read data strobe signal being received by the controller in response to the second data strobe signal; and
 - [1.5] a memory adapted to receive the write data signal in synchronization with the first data strobe signal in the write operation, [1.6] the memory being adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal and to send the read data signal synchronized with the read data strobe signal.

Ex. 1001, 8:15–30.

E. Prior Art References and Other Evidence

Petitioner relies on the following references:

1. Lee, US Patent Application Publication No. 2004/0022095 A1 (February 5, 2004), (Ex. 1005, “Lee”).
2. JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, March 2003,² (Ex. 1007, “JEDEC”).

In addition to these references, Petitioner relies on a Declaration of R. Jacob Baker, Ph.D. Ex. 1003.

² Petitioner contends JEDEC was publicly available as of at least June 9, 2003. Pet. 17.

F. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability. Pet. 16.

Claim(s) Challenged	Basis 35 U.S.C. §	Reference(s)
1, 6, 10, 14, 15, 16, 17, 18, 19, 25, 26, 27	103(a) ³	Lee
2, 7, 11	103(a)	Lee, JEDEC

III. ANALYSIS

A. Applicable Legal Standards

A claim is unpatentable as obvious under 35 U.S.C. § 103 “if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a) (2006). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) so-called “secondary considerations,” including commercial success, long-felt but unsolved needs, failure of others, and unexpected results. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). At this stage, neither party has presented any evidence on the fourth *Graham* factor.

³ Because the application from which the ’369 patent issued was filed before March 16, 2013 (Ex. 1001, code (22)), citations to 35 U.S.C. § 103 are to the pre-AIA version. Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29.

B. Level of Ordinary Skill in the Art

According to Petitioner, a person of ordinary skill in the pertinent art would have had a working knowledge of the memory system art that is pertinent to the '369 patent, including memory systems and memory controllers. A [person of ordinary skill in the art] would have had a bachelor's degree in electrical engineering, or an equivalent, and approximately two years of professional experience relating to field of memory systems. Lack of professional experience can be remedied by additional education, and vice versa.

Pet. 15 (citing Ex. 1003 ¶¶ 18–20).

Petitioner's definition appears consistent with the level of technology described by the '369 patent and the applied prior art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (prior art itself may reflect an appropriate level of skill). Therefore, for the purpose of this decision, we adopt Petitioner's formulation.

C. Claim Construction

For this *inter partes* review, the Board applies the same claim construction standard as that applied in federal courts. *See* 37 C.F.R. § 42.100(b) (2023). Under this standard, claim terms “are generally given their ordinary and customary meaning” as understood by a person of ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc) (citations omitted). “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Extrinsic evidence is “less significant than the intrinsic record in

determining ‘the legally operative meaning of claim language.’” *Phillips*, 415 F.3d at 1317 (citation omitted).

Petitioner contends no claim term requires express construction. Pet. 15 (citing Ex. 1003).

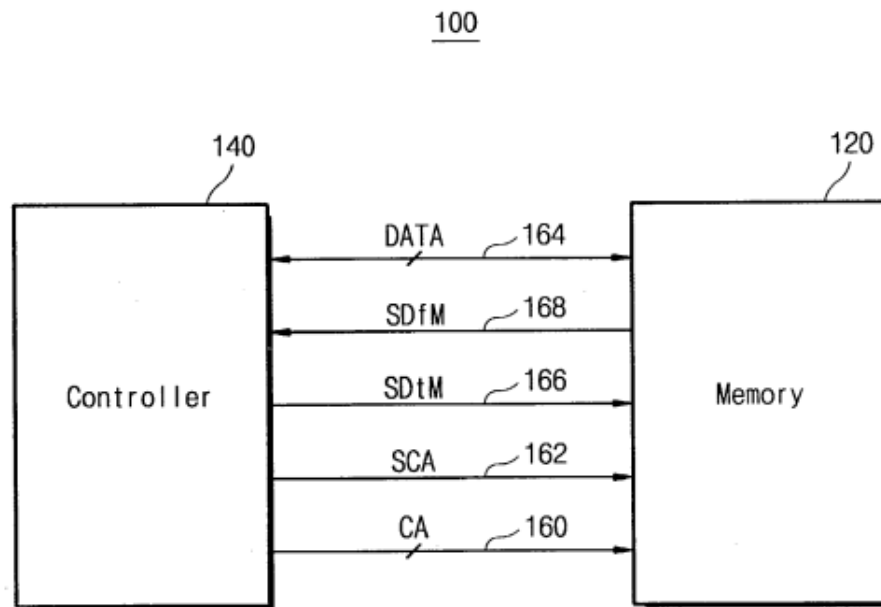
Only those terms that are in controversy need be construed, and only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017); *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999). For purposes of this Decision and based on this preliminary record, we determine that no claim terms require express construction at this stage of the proceeding.

D. Prior Art References

1. Lee (Ex. 1005)

Lee is a patent application publication titled “Asynchronous Memory Using Source Synchronous Transfer and System Employing the Same.” Ex. 1005, code (54). Lee “is related to electronic devices, and, in particular, to a system that performs data transmission between a memory and a memory controller.” *Id.* ¶ 2.

Lee’s Figure 1, reproduced below, is a block diagram of systems according to embodiments of the Lee invention. *Id.* ¶ 11.



Lee's Figure 1, shown above, depicts memory system 100 which includes memory 120 and memory controller 140. *Id.* ¶ 17.

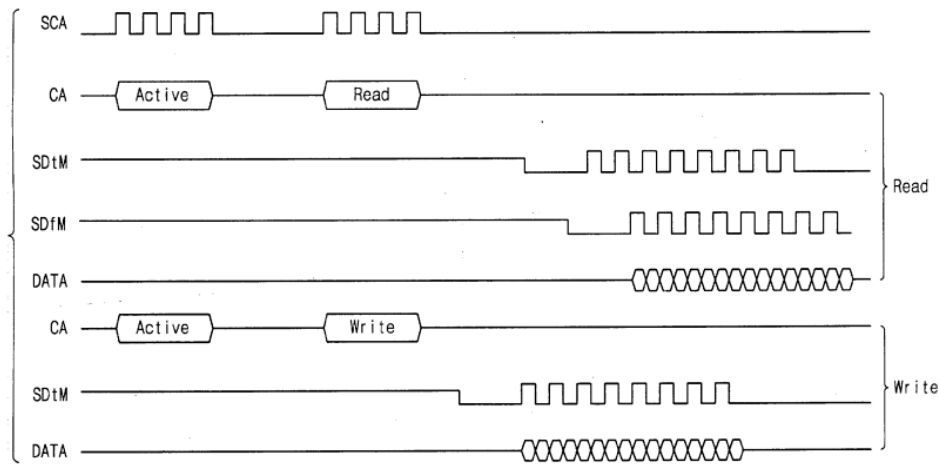
In a write operation, write data DATA is sent to memory 120 from memory controller 140 together with a second strobe signal SDtM. *Id.* ¶ 20.

In a read operation, Lee's system works as follows:

For a read operation, in addition to the command/address information CA, the memory controller **140** transfers to the memory **120** the second strobe signal SDtM as a transmission synchronous or reference signal at a time when it wants to receive data read out from the memory **120**. The memory **120** internally generates a third strobe signal SDfM in response to the second strobe signal SDtM. The read data that is read from the memory **120** is sent to the memory controller **140** together with the third strobe signal SDfM.

Id. ¶ 21.

Lee's Figure 2, reproduced below, is a timing diagram of data transmission operations according to embodiments of the Lee invention. *Id.* ¶ 12.



Lee's Figure 2, shown above, depicts read and write signal transmission operations between memory controller 140 and memory 120. *Id.* ¶¶ 24–26. During a write operation where data is written to memory 120, Lee explains that

first, an active command 'Active' (e.g., a row address) is sent to the memory controller 140 from the memory 120. The active command 'Active' is sent to the memory 120 by the memory controller 140 toggling the first strobe signal SCA during a predetermined time, for example, when the active command 'Active' is on the control bus 160 (illustrated as CA in FIG. 2). That is, the memory controller 140 loads the active command 'Active' on the control bus 160 and toggles the first strobe signal SCA while the command is on the control bus 160. The memory 120 latches the active command 'Active' in response to toggling of the first strobe signal SCA. The memory controller 140 subsequently loads the write command 'Write' (e.g., a column address) on the control bus 160 and toggles the first strobe signal SCA while the write command 'Write' is on the control bus 160. The memory 120 latches the write command 'Write' in response to toggling of the first strobe signal SCA.

EX. 1005 ¶ 26.

Similarly, with respect to a read operation, Lee explains that data stored in a memory cell array (not shown) is read out via a read circuit (e.g., a sense amplifier circuit). The read data is

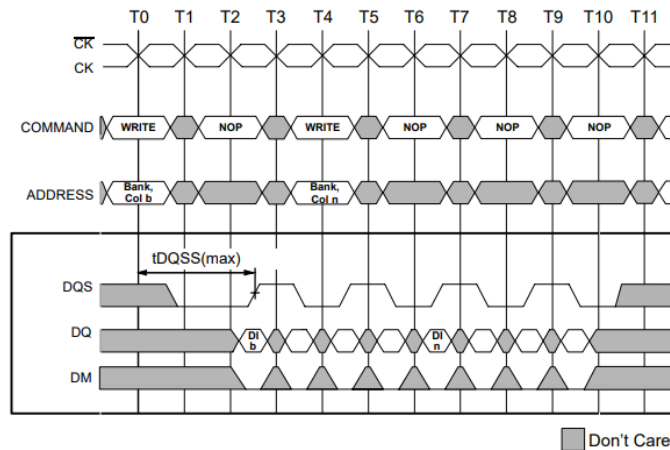
transferred to the memory controller 140 from the memory 120 via a data bus 166, based on the control of the memory controller 140. To send data read from the memory 120 to the memory controller 140, first, the memory controller 140 transfers the second strobe signal SDtM to the memory 120. The memory 120 generates the third strobe signal SDfM in response to the received second strobe signal SDtM. The third strobe signal SDfM, as illustrated in FIG. 2, may have the same waveform as the second strobe signal SDtM delayed by a predetermined time. The memory 120 loads data on the data bus 166 (illustrated as DATA in FIG. 2) in response to the second strobe signal SDtM and outputs the third strobe signal SDfM while the data is loaded on the data bus 166. The memory controller 140 latches data DATA loaded on the data bus 166 in response to the third strobe signal SDfM.

Ex. 1005 ¶ 25.

2. *JEDEC (Ex. 1007)*

JEDEC is a standard of the Joint Electron Device Engineering Council entitled Double Data Rate (DDR) SDRAM Specification. Ex. 1007, 1; Ex. 1003 ¶ 104. A DDR SDRAM is a high-speed dynamic random-access memory. Ex. 1007, 7. JEDEC states that “JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Council level and subsequently reviewed and approved by the EIA [Electronic Industries Alliance] General Counsel.” *Id.* at 1–2.

JEDEC Figure 22, reproduced below, is a timing diagram for WRITE bursts. *Id.* at 37, 40.



JEDEC Figure 22, shown above, depicts clock CK and command and address signals. *Id.* at 7, 40.

E. Obviousness Based on Lee (Ground 1)

Petitioner contends that claims 1, 6, 10, 14–19, and 25–27 would have been rendered obvious by Lee. Pet. 20–57. Petitioner provides a detailed claim analysis, supported by the testimony of Dr. Baker. *See* Pet. 20–57; Ex. 1003 ¶¶ 41–102. Patent Owner has not filed a preliminary response. We discuss the evidence and the arguments provided by Petitioner with respect to independent claim 1.

1. Independent Claim 1

a) [1.0] A system comprising:

For the preamble, Petitioner points out that “Lee describes a system for data transmission between [a] controller and a memory.” Pet. 26–27 (citing Ex. 1005 ¶ 2). According to Petitioner, “Lee further describes ‘a memory system 100 . . . [that] includes a memory 120 and a memory controller 140.” Pet. 27 (citing Ex. 1005 ¶ 17). “[B]ecause Lee describes a memory system that performs data transmission between a memory and a memory controller,” Petitioner asserts, “Lee renders obvious a ‘system’ as claimed.” Pet. 27 (citing Ex. 1003 ¶¶ 45–46).

On this preliminary record, we determine that Petitioner has shown sufficiently for purposes of institution that Lee meets the subject matter recited in the preamble of claim 1.

b) *[1.1] a controller adapted to send out a first data strobe signal and a write data signal in a write operation,*

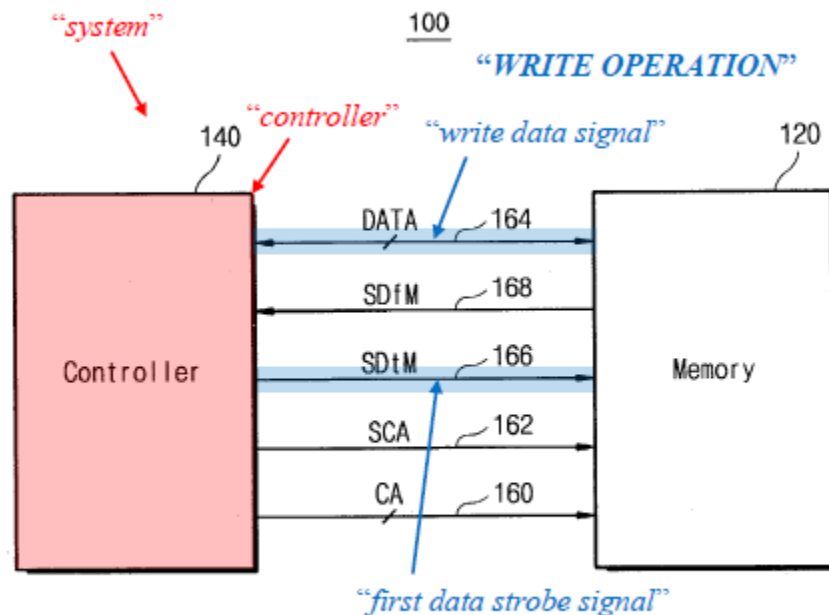
For this limitation, Petitioner asserts that “Lee’s system includes a controller 120 (*‘controller’*): ‘[A] memory system 100 according to particular embodiments the present invention includes a memory 120 and a memory controller 140.’” Pet. 28 (citing Ex. 1005 ¶ 17). Petitioner explains that

Lee describes a write operation in which the controller transmits strobe signal SDtM (“first data strobe signal”) over line 166 and data (“write data signal”) over line 164. Lee explains that during a write operation, “the memory controller 140 transfers data DATA to the memory 120 via a data bus 164, and transfers, as a transmission synchronous signal, the second strobe signal SDtM to the memory 120 via a signal line 166.”

Pet. 28 (citing Ex. 1005 ¶ 20).

Petitioner provides annotated Figure 1 from Lee, shown below.

Pet. 28.



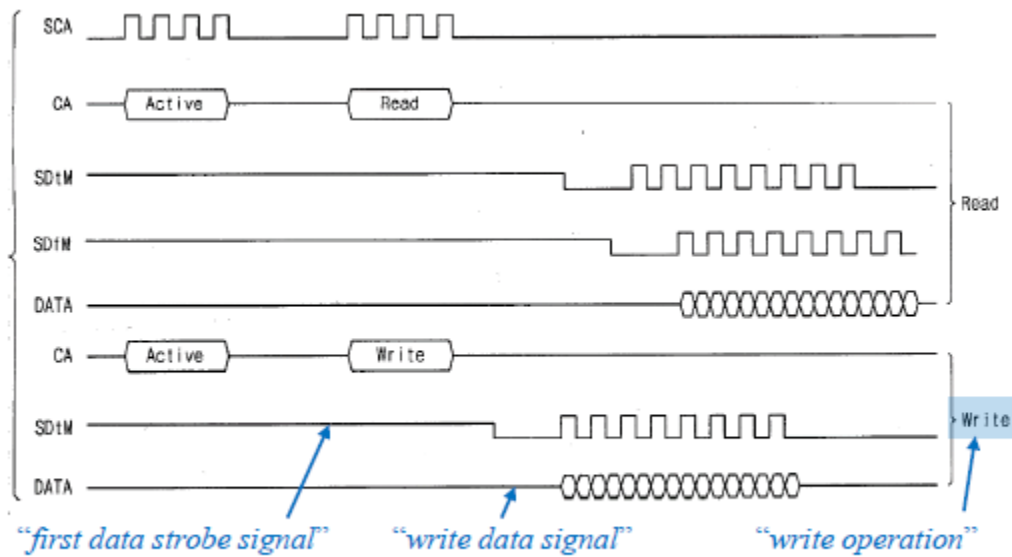
EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 48.

Petitioner's annotated Figure 1 from Lee, shown above, is a block diagram depicting controller 140 in communication with memory 120. Pet. 29. According to Lee, during a write operation

memory controller 140 transfers data DATA to the memory 120 via a data bus 164, and transfers, as a transmission synchronous signal, the second strobe signal SDtM to the memory 120 via a signal line 166. In particular, for a write operation, the write data DATA is sent to the memory 120 from the memory controller 140 together with the second strobe signal SDtM based on the source synchronous interface. The memory 120 latches the write data DATA in response to the second strobe signal SDtM.

Ex. 1005 ¶ 20. Petitioner identifies (in blue) SDtM 166 as the recited "first data strobe signal" and DATA 164 as the recited "write data signal." Pet. 29.

Petitioner also provides annotated Figure 2 from Lee, shown below.
Pet. 30.



EX1005, Lee, Fig. 2 (annotated); EX1003, ¶ 49.

Petitioner's annotated Figure 2 from Lee, shown above, is a timing diagram of data transmission operations depicting read and write operations. Petitioner identifies (in blue) SDtM as the recited "first data strobe signal" and DATA as the recited "write data signal" for the recited "write operation." Pet. 30. According to Petitioner, in Lee "[d]uring the write operations, 'data to be written is then sent from the memory controller 140 to the memory 120. Data transmission is accomplished by toggling the second strobe signal SDtM.'" Pet. 30 (citing Ex. 1005 ¶ 27).

"Thus," Petitioner argues, "because Lee describes a controller 140 that transmits a strobe signal SDtM and a data signal over lines 166 and 164 respectively, Lee renders obvious 'a controller adapted to send out a first data strobe signal and a write data signal in a write operation' as claimed." Pet. 30 (citing Ex. 1003 ¶¶ 47–50). Petitioner's arguments are supported by the testimony of Dr. Baker.

On this preliminary record, we determine that Petitioner has shown sufficiently for purposes of institution that Lee’s description of memory controller 140 transferring data to memory 120 via data bus 164 and transferring strobe signal SDtM to memory 120 via signal line 166 during a write operation meets the recited “*controller adapted to send out a first data strobe signal and a write data signal in a write operation,*” of claim 1.

c) [1.2] *the write data signal being synchronized with the first data strobe signal,*

For this limitation, Petitioner asserts “Lee explains that the data signal is synchronous with the data strobe signal SDtM: ‘For a write operation . . . the memory controller 140 transfers data DATA to the memory 120 via a data bus 164, and transfers, *as a transmission synchronous signal,* the second strobe signal SDtM to the memory 120 via a signal line 166.’” Pet. 30–31 (citing Ex. 1005 ¶ 20).

Petitioner argues that a person of ordinary skill in the art “would have further recognized that the very purpose of a strobe signal is to instruct the receiving system when to sample the transmitted data.” Pet. 31 (citing Ex. 1005 ¶ 27 (“The memory 120 latches the write data DATA in response to the second strobe signal SDtM”). Petitioner asserts that “Lee’s asynchronous memory still uses strobe signals that are synchronized with their corresponding data signals.” *Id.* According to Petitioner, a person of ordinary skill in the art “would have thus understood that the strobe signal is synchronized with the data signal.” *Id.*

“Thus,” Petitioner argues, “because Lee describes the strobe signal as a transmission synchronous signal, Lee renders obvious ‘*the write data signal being synchronized with the first data strobe signal*’ as claimed.” Pet.

31 (citing Ex. 1003 ¶¶ 51–52). Petitioner’s arguments are supported by the testimony of Dr. Baker.

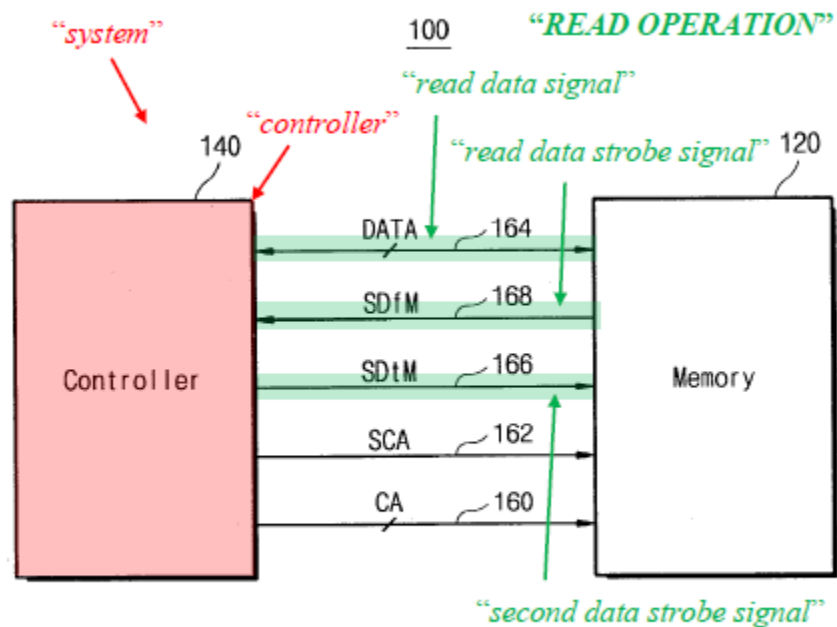
On this preliminary record, we determine that Petitioner has shown sufficiently for purposes of institution that Lee’s description of a write operation where memory controller 140 transfers data to memory 120 via data bus 164, and transfers as a transmission synchronous signal, strobe signal SDtM to memory 120 via signal line 166 meets the recited “*write data signal being synchronized with the first data strobe signal*,” of claim 1.

d) [1.3] the controller being adapted, in a read operation, to send out a second data strobe signal and to receive a read data signal in synchronization with a read data strobe signal,

For this limitation, Petitioner asserts that “Lee describes a read operation in which the memory transmits strobe signal SDfM (“*read data strobe signal*”) over line 168 and data (“*read data signal*”) over line 164 in response to the SDtM signal (“*second data strobe signal*”).” Pet. 31–32. According to Petitioner, “Lee explains that during a read operation, ‘the memory controller 140 transfers to the memory 120 the second strobe signal SDtM as a transmission synchronous or reference signal at a time when it wants to receive data read out from the memory 120.’” *Id.* at 32 (quoting Ex. 1005 ¶ 21). Petitioner argues that “Lee’s controller thus ‘*send[s] out a second data strobe signal*.’” Pet. 32. Petitioner explains that “[t]he controller then receives data in synchronization with a read strobe signal: ‘Therefore, during the read operation the memory controller 140 receives the read data DATA from the memory 120 together with the third strobe signal SDfM at a required time,’” as Petitioner asserts that SDfM is the recited “*read data strobe signal*.” Pet. 32 (quoting Ex. 1005 ¶ 21). “Lee’s

controller,” Petitioner argues, “thus ‘receive[s] a read data signal in synchronization with a read data strobe signal.’” Pet. 32.

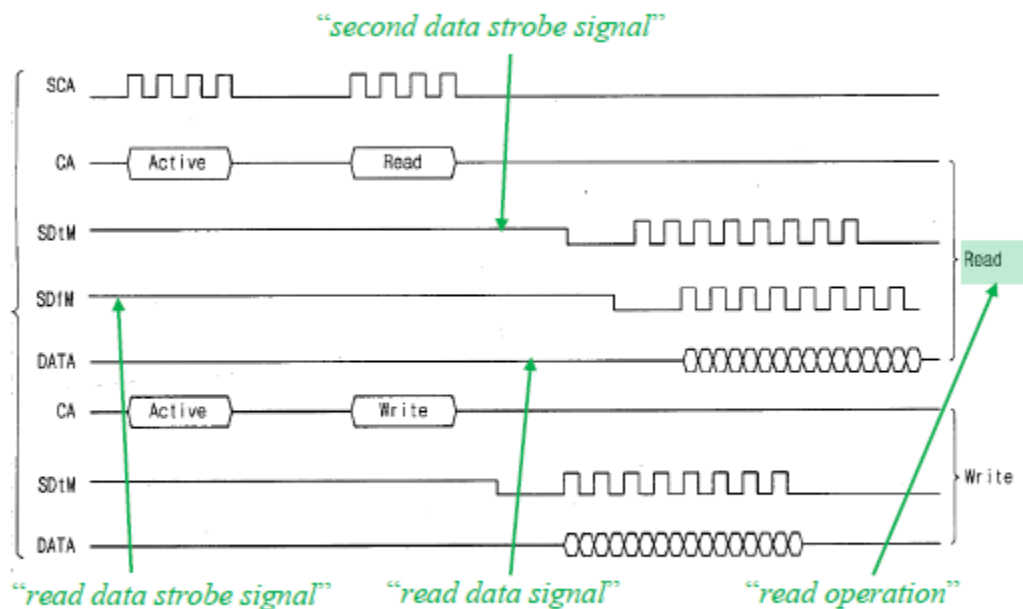
To illustrate this operation, Petitioner provides an annotated Figure 1 from Lee, shown below. Pet. 33.



EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 53.

Petitioner’s annotated Figure 1 from Lee, shown above, is a block diagram depicting controller 140 in communication with memory 120 during a “read operation.” Pet. 33. Petitioner identifies (in green) SDtM 166 as the recited “second data strobe signal,” SDfM 168 as the recited “read data strobe signal,” and DATA 164 as the recited “read data signal.” *Id.*

Petitioner also provides an annotated Figure 2 from Lee, shown below. Pet. 34.

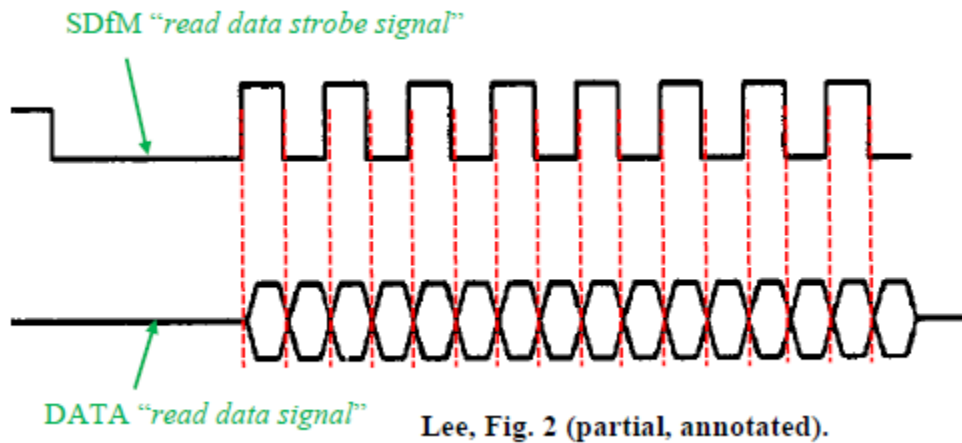


EX1005, Lee, Fig. 2 (annotated); EX1003, ¶ 54.

Petitioner’s annotated Figure 2 from Lee, shown above, is a timing diagram of data transmission operations depicting read and write operations. Petitioner identifies (in green) SDtM as the recited “second data strobe signal,” SDfM as the recited “read data strobe signal,” and DATA as the recited “read data signal” for the recited “read operation.” Pet. 34.

Petitioner points out that “Lee’s read operations are described as “conventional read operations.” Pet. 34 (citing Ex. 1005 ¶ 25). According to Petitioner, “[s]uch conventional read operations include the memory generating the strobe signal SDfM (*‘read data strobe signal’*) in response to receipt of the strobe signal SDtM (*‘second data strobe signal’*).” Pet. 34. According to Petitioner, Lee explains that “[t]o send data read from the memory 120 to the memory controller 140, first, the memory controller 140 transfers the second strobe signal SDtM to the memory 120. The memory 120 generates the third strobe signal SDfM *in response* to the received second strobe signal SDtM.” Pet. 34 (quoting Ex. 1005 ¶ 25).

Dr. Baker testifies that “the SDfM signal (“*read data strobe signal*”) is in synchronization with the read data signal.” Ex. 1003 ¶ 57. To illustrate this, Dr. Baker provides an annotated, partial view of Lee’s Figure 2, shown below. *Id.*



Dr. Baker’s annotated, partial view of Lee’s Figure 2, shown above, identifies (in green) SDfM as the recited “read data strobe signal,” and DATA as the recited “read data signal,” showing that “the rising and falling times of the strobe signal SDfM are synchronized with the switching of the data signal.” *Id.*

Based on this figure, Dr. Baker testifies that a person of ordinary skill in the art “would have understood that the SDfM signal is ‘*in synchronization with*’ the read DATA signal,” and such a person “would have understood that synchronization is done for the purpose of telling the receiving component—in this case the memory—when to sample the data.” Ex. 1003 ¶ 58 (citing Ex. 1005 ¶ 25).

“Thus,” Petitioner argues, “because Lee describes that during a read operation, the memory sends a data signal and a data strobe signal (which are synchronized) responsive to a signal from the controller, Lee renders

obvious ‘*the controller being adapted, in a read operation, to send out a second data strobe signal and to receive a read data signal in synchronization with a read data strobe signal*’ as claimed.” Pet. 36 (citing Ex. 1003 ¶¶ 53–59). Petitioner’s arguments are supported by the testimony of Dr. Baker.

On this preliminary record, we determine that Petitioner has shown sufficiently for purposes of institution that Lee’s description of a read operation where memory controller 140 transfers to memory 120 strobe signal SDtM as a transmission synchronous or reference signal at a time when it wants to receive data read out from the memory 120; and memory 120 generates strobe signal SDfM in response to the received strobe signal SDtM; and memory controller 140 receives read data DATA from memory 120 together with strobe signal SDfM, meets the recited “*controller being adapted, in a read operation, to send out a second data strobe signal and to receive a read data signal in synchronization with a read data strobe signal,*” of claim 1.

e) [1.4] *the read data strobe signal being received by the controller in response to the second data strobe signal;*

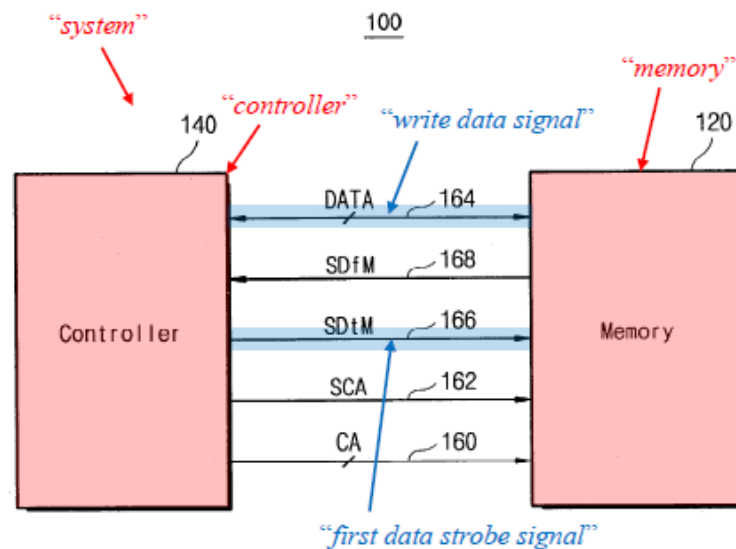
For this limitation, Petitioner points out that “Lee explains that the SDfM signal is received by the controller in response to transmitting the SDtM signal: ‘The memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM.’” Pet. 37 (quoting Ex. 1005 ¶ 21; *see also* Ex. 1005 ¶ 24. “Thus,” Petitioner argues, “because Lee’s strobe signal SDfM is received in response to the strobe signal SDtM, Lee renders obvious “*the read data strobe signal being received by the controller in response to the second data strobe signal*” as claimed. Pet. 37

(citing Ex. 1003 ¶¶ 60–61). Petitioner’s arguments are supported by Dr. Baker’s testimony.

On this preliminary record, we determine that Petitioner has shown sufficiently for purposes of institution that Lee’s description of memory controller 140 transferring strobe signal SDtM to memory 120, wherein memory 120 generates strobe signal SDfM in response to received strobe signal SDtM meets the recited “*read data strobe signal being received by the controller in response to the second data strobe signal,*” of claim 1.

f) [1.5] *a memory adapted to receive the write data signal in synchronization with the first data strobe signal in the write operation,*

For this limitation, Petitioner asserts that Lee describes a “write operation in which the memory receives strobe signal SDtM (“*first data strobe signal*”) over line 166 and data (“*write data signal*”) over line 164.” Pet. 38. To illustrate this operation, Petitioner provides an annotated version of Lee’s Figure 1, shown below. Pet. 38.



EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 62.

Petitioner's annotated Figure 1 from Lee, shown above, is a block diagram depicting controller 140 in communication with memory 120. Petitioner identifies (in blue) SDtM 166 as the recited "first data strobe signal" and DATA 164 as the recited "write data signal." *Id.*

Lee explains in particular that "[f]or a write operation . . . memory controller 140 transfers data DATA to the memory 120 via a data bus 164, and transfers, as a transmission synchronous signal, the second strobe signal SDtM to the memory 120 via a signal line 166." Ex. 1005 ¶ 20.

"Thus," Petitioner argues, "because Lee describes a memory that receives the write data signal along with a strobe signal, Lee renders obvious *"a memory adapted to receive the write data signal in synchronization with the first data strobe signal in the write operation"* as claimed. *Id.* (citing Ex. 1003 ¶¶ 62–64). Petitioner's arguments are supported by Dr. Baker's testimony.

On this preliminary record, we determine that Petitioner has shown sufficiently for purposes of institution that Lee's description of memory controller 140 transferring DATA to memory 120 via data bus 164, and also transferring, as a transmission synchronous signal, strobe signal SDtM to memory 120 via signal line 166, meets the recited *"memory adapted to receive the write data signal in synchronization with the first data strobe signal in the write operation,"* of claim 1.

g) [1.6] *the memory being adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal and to send the read data signal synchronized with the read data strobe signal.*

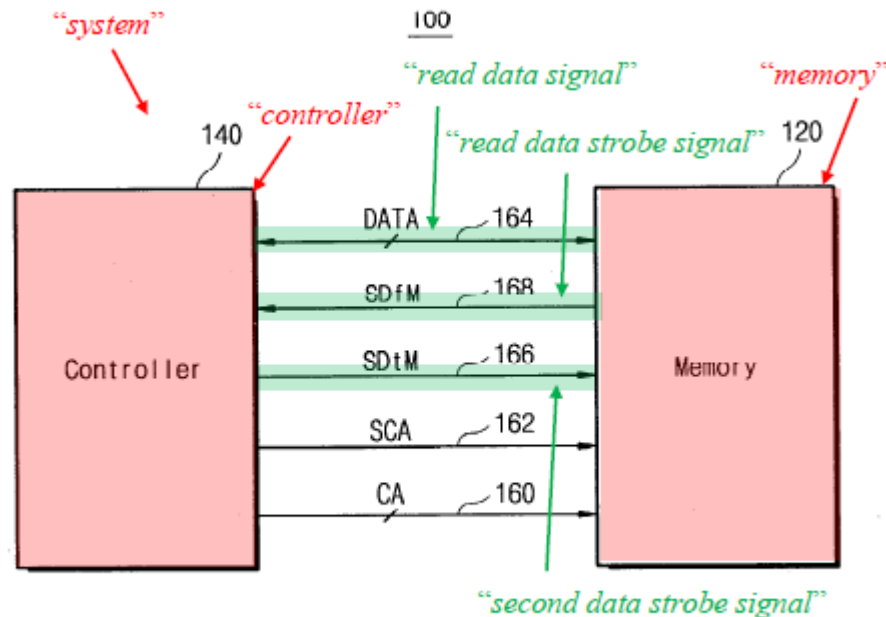
For this limitation, Petitioner asserts that

Lee describes a read operation in which the memory transmits strobe signal SDfM (*"read data strobe signal"*) over line 168 and

data (“*read data signal*”) over line 164. In Lee’s read operation, “the memory controller 140 transfers to the memory 120 the second strobe signal SDtM as a transmission synchronous or reference signal at a time when it wants to receive data read out from the memory 120.” EX1005, Lee, [0021]. These signals are transmitted by the memory in response to receiving the SDtM signal (“*second data strobe signal*”). “The memory 120 internally generates a third strobe signal SDfM *in response to* the second strobe signal SDtM. The read data that is read from the memory 120 is sent to the memory controller 140 together with the third strobe signal SDfM.”

Pet. 39 (citing Ex. 1005 ¶ 21; *see also* Ex. 1005 ¶ 25).

To illustrate this operation, Petitioner provides an annotated version of Lee’s Figure 1, shown below. Pet. 40.



EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 65.

Petitioner’s annotated Figure 1 from Lee, shown above, depicts controller 140 in communication with memory 120 during a read operation. *Id.* Petitioner identifies (in green) signal SDtM 166 as the recited “second

data strobe signal,” signal SDfM 168 as the recited “read data strobe signal,” and DATA 164 as the recited “read data signal.” *Id.*

Petitioner argues that “because Lee’s memory system transmits the strobe signal SDfM in response to the SDtM signal, Lee renders obvious “*the memory being adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal and to send the read data signal synchronized with the read data strobe signal*” as claimed. Pet. 40 (citing Ex. 1003 ¶¶ 65–66). Petitioner’s arguments are supported by Dr. Baker’s testimony.

On this preliminary record, we determine that Petitioner has shown sufficiently for purposes of institution that Lee’s description of memory controller 140 transferring to memory 120 strobe signal SDtM as a transmission synchronous or reference signal, wherein memory 120 generates strobe signal SDfM in response to strobe signal SDtM, and read data that is read from memory 120 is sent to memory controller 140 together with strobe signal SDfM meets the recited “*memory being adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal and to send the read data signal synchronized with the read data strobe signal,*” of claim 1.

2. Conclusion as to Independent Claim 1

We have considered Petitioner’s evidence and arguments that the limitations of claim 1 are met by the teachings of Lee. Based on this preliminary record, we are persuaded that Petitioner has demonstrated sufficiently for purposes of institution that the teachings of Lee meet the limitations of independent claim 1.

3. *Independent Claims 6, 10, and 26*

Petitioner also contends that independent claims 6, 10, and 26 would have been rendered obvious by Lee. Pet. 40–44, 51–57. Petitioner provides a detailed claim analysis, supported by the testimony of Dr. Baker. *See* Pet. 40–44, 51–57; Ex. 1003 ¶¶ 67–75, 90–100.

We have considered Petitioner’s evidence and arguments with respect to independent claims 6, 10, and 26. Because we determine that Petitioner demonstrates a reasonable likelihood of prevailing in its challenge to independent claim 1, we institute *inter partes* review as to all other challenges in the Petition, including Petitioner’s challenges to claims 6, 10, and 26. *See PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018).

4. *Dependent Claims 14, 15, 16, 17, 18, 19, 25, and 27*

Petitioner contends that dependent claims 14, 15, 16, 17, 18, 19, 25, and 27 would have been rendered obvious by Lee. Pet. 44–51, 57. Petitioner provides a detailed claim analysis, supported by the testimony of Dr. Baker. *See* Pet. 44–51, 57; Ex. 1003 ¶¶ 76–89, 101, 102.

We have considered the evidence and arguments with respect to dependent claims 2, 7, and 11. Because we determine that Petitioner demonstrates a reasonable likelihood of prevailing in its challenge to independent claim 1 under 35 U.S.C. § 103(a) as obvious over Lee, we are instituting an *inter partes* review on that challenge and we also institute *inter partes* review as to all challenges in the Petition, including Petitioner’s challenges to dependent claims 14, 15, 16, 17, 18, 19, 25, and 27. *See PGS Geophysical*, 891 F.3d at 1360 (Fed. Cir. 2018).

F. Obviousness Based on Lee and JEDEC (Ground 2)

Petitioner contends that dependent claims 2, 7, and 11 are unpatentable under 35 U.S.C. § 103 as obvious over the combined teachings of Lee and JEDEC. Pet. 57–68. Petitioner provides a detailed claim analysis, supported by the testimony of Dr. Baker. *See* Pet. 63–68; Ex. 1003 ¶¶ 103–122. Petitioner also provides an explanation of a rationale to combine the teachings of Lee and JEDEC in the manner described in the Petition. Pet. 59–63 (citing Ex. 1003 ¶¶ 108–13).

We have considered the evidence and arguments with respect to dependent claims 2, 7, and 11. Because we determine that Petitioner demonstrates a reasonable likelihood of prevailing in its challenge to independent claim 1 under 35 U.S.C. § 103(a) as obvious over Lee, we are instituting an *inter partes* review on that challenge and we also institute *inter partes* review as to all challenges in the Petition, including Petitioner’s challenges to claims 2, 7, and 11. *See PGS Geophysical* 891 F.3d at 1360 (Fed. Cir. 2018).

IV. CONCLUSION

For the foregoing reasons, we determine that there is a reasonable likelihood that Petitioner would prevail with respect to at least one of the claims challenged in the Petition. We therefore institute trial as to all challenged claims on all grounds asserted in the Petition.

V. ORDER

Upon consideration of the record before us, it is

ORDERED that *inter partes* review of claims 1, 2, 6, 7, 10, 11, 14–19, and 25–27 of the ’369 patent is instituted on all grounds in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

IPR2023-01200
Patent 7,697,369 B2

PETITIONER:

David O'Dell
Calmann Clements
Hong Shi
HAYNES AND BOONE, LLP
david.odell.ipr@haynesboone.com
calmann.clements.ipr@haynesboone.com
hong.shi.ipr@haynesboone.com

FOR PATENT OWNER:

James Milkey
Qi Tong
RUSS AUGUST & KABAT
jmilkey@raklaw.com
ptong@raklaw.com