

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

LONGITUDE LICENSING LTD.,
Patent Owner.

Case IPR2023-01200
U.S. Patent No. 7,697,369 B2

PATENT OWNER'S RESPONSE

TABLE OF CONTENTS

I.	Introduction	1
II.	Summary of Prior Art References	3
	A. United States Patent Application 2004/0022095 to Lee (Ex. 1005)	3
	B. JEDEC Standard JESD79C for DDR SDRAM (“JEDEC”) (Ex. 1007)	7
III.	Level of Ordinary Skill in the Art	12
IV.	Claim Construction.....	12
V.	The Petition’s Ground 2 fails.	13
VI.	Conclusion.....	21

TABLE OF AUTHORITIES

Cases

<i>ATD Corp. v. Lydall, Inc.</i> , 159 F.3d 534 (Fed. Cir. 1998).....	20
<i>Belden Inc. v. Berk–Tek LLC</i> , 805 F.3d 1064 (Fed. Cir. 2015).....	13, 20
<i>Cheese Sys., Inc. v. Tetra Pak Cheese & Powder Sys., Inc.</i> , 725 F.3d 1341 (Fed. Cir. 2013).....	20
<i>Galderma Labs., L.P. v. Tolmar, Inc.</i> , 737 F.3d 731 (Fed. Cir. 2013).....	17
<i>In re Fulton</i> , 391 F.3d 1195 (Fed. Cir. 2004).....	17
<i>KSR Int’l Co. v. Teleflex, Inc.</i> , 550 U.S. at 398 (2007)	20
<i>Meiresonne v. Google, Inc.</i> , 849 F.3d 1379 (Fed. Cir. 2017).....	17
<i>Pers. Web Techs., LLC v. Apple, Inc.</i> , 848 F.3d 987 (Fed. Cir. 2017).....	13, 19
<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005).....	12
<i>Plas-Pak Indus., Inc. v. Sulzer Mixpac AG</i> , 600 F. App’x 755 (Fed. Cir. 2015).....	14
<i>Shenzhen Liown Electronics Co. v. Disney Enterprises, Inc.</i> , IPR2015-01656, Paper 7 (Feb. 8, 2016).....	12
<i>Virtek Vision Int’l ULC v. Assembly Guidance Sys., Inc.</i> , 97 F.4th 882 (Fed. Cir. 2024).....	14
<i>Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.</i> , 200 F.3d 795 (Fed. Cir. 1999).....	12

Statutes

35 U.S.C. § 103(a)	2
--------------------------	---

Patent Owner's Exhibits List

Exhibit No.	Description
2001	Declaration of Brian D. Ledahl in Support of Motion for <i>Pro Hac Vice</i> Admission
2002	Declaration of Paul A. Kroeger in Support of Motion for <i>Pro Hac Vice</i> Admission
2003	Declaration of Bruce Jacob in Support of Patent Owner's Response Re: <i>Inter Partes</i> Review of U.S. Patent No. 7,697,369
2004	Deposition Transcript of Dr. R. Jacob Baker dated April 5, 2024

I. Introduction

Petitioner Western Digital Technologies, Inc. (“WD” or “Petitioner”) presents two grounds of unpatentability for the challenged claims of U.S. 7,367,369 (the “’369 Patent”) (Ex. 1001). Ground 1 challenges claims 1, 6, 10, 14, 15, 16, 17, 18, 19, 25, 26, and 27 as obvious over Lee alone and Ground 2 challenges claims 2, 7, and 11 as obvious over the combination of Lee and JEDEC. Pet. at 16. This Patent Owner Response addresses Ground 2 only.

Unlike the claims challenged in Ground 1, each of claims 2, 7, and 11 require that the controller be adapted to produce (1) a clock signal; and (2) send the clock signal to the memory. Claim 2 is exemplary and is reproduced below:

The system according to claim 1, *wherein the controller is further adapted to produce a clock signal and to send the clock signal to the memory*, each of the first and the second data strobe signals and the read data strobe signal being independent of and separated from the clock signal.

'369 Patent, Claim 2. Petitioner's Ground 2 fails because it provides no motivation to combine Lee and JEDEC that renders the clock signal limitations obvious.¹

Lee teaches an asynchronous memory that, by definition, does not receive a system clock. Specifically, Lee seeks to “*avoid*” “*the need for a continuous clock*” and reduce “the current consumed by the memory 120 when not performing a read or write operation ... over a similar memory that utilizes a continuous clock.” Ex. 1005, Lee ¶ [0028] (emphasis added). It expressly avoids the clock tree structure in “conventional ... synchronous memory” “that produces a clock signal” “*irrespective of whether an operation is being performed*” and thus produces the same current in a “standby” and “non standby state” *Id.* ¶ [0005]. It further refers to such a “low power mode” as being “beneficial.” *Id.* ¶ [0004].

In contrast, the JEDEC standard describes the first-generation Double Data Rate *Synchronous* DRAM (DDR SDRAM). JEDEC requires that a system clock signal be delivered to the memory device. Indeed, Petitioner, and its expert Dr. Jacob

¹ The Board's Institution Decision did not make any finding as to whether Petitioner had shown a reasonable likelihood of prevailing on this Ground. Institution Decision, Paper 6 at 28. Instead, the Board noted “[b]ecause we determine that Petitioner demonstrates a reasonable likelihood of prevailing in its challenge to independent claim 1 under 35 U.S.C. § 103(a) as obvious over Lee, we are instituting an *inter partes* review on that challenge and we also institute *inter partes* review as to all challenges in the Petition, including Petitioner's challenges to claims 2, 7, and 11.” *Id.*

Baker, use the JEDEC standard for its disclosure of a continuous clock signal that is provided to the memory.

The Petition's proposed combination of Lee and the JEDEC standard is to make one of Lee's signals a "continuous clock signal" in manner expressly eschewed by Lee. Moreover, this would frustrate the intended purpose of Lee's invention of allowing for a memory with a low power mode. The Petition's attempt to refer to this combination as a simple design choice ignores the clear teaching of Lee that sought to preclude the use of a continuous clock.

Accordingly, the Petition does not present a proper motivation to combine Lee and JEDEC and its Ground 2 fails. For this reason, the Petition fails to show that claims 2, 7, and 11 of the '369 Patent are unpatentable.

II. Summary of Prior Art References

A. United States Patent Application 2004/0022095 to Lee (Ex. 1005)

Lee is entitled "asynchronous memory using source-synchronous transfer and system employing same." Lee, Ex. 1005. A POSITA understands that "source synchronous transfer" simply means that a data-strobe signal is transmitted along with the data signal. Ex. 2003, Jacob Decl., ¶ 88; Ex. 1005, Lee ¶ [0018] ("A Source synchronous interface is an interface where data is sent from a transmitter to a receiver together with a clock signal, which is used within a receive interface to latch the accompanying data."). Lee describes a general interface that can be used for

different memory types (e.g., DRAMs, SRAMs, MROMs, PROMs, etc. Ex. 2003, Jacob Decl., ¶ 88; Ex. 1005, Lee ¶[0003].

Lee indicates that one of the most important aspects of the invention is that it enables a low-power system:

Various memory configurations have been utilized in conventional mobile processing Systems Such as Personal Communication Service (PCS), cellular, or Personal Digital Assistant (PDA). Such memory systems include non-volatile and volatile memories. *Because mobile processing systems typically operate using a power supply voltage supplied from a battery, low-power operation of the memory system included in the mobile processing system may be beneficial. In particular, because mobile processing systems may spend much of their operational time in a standby state, memory systems that may provide low-power operation while the mobile processing system is in the standby state may also be beneficial.*

Ex. 1005, Lee ¶ [0004] (emphasis added); Jacob Decl., ¶ 88. Lee teaches that use of a conventional, continually produced, clock signal is the primary impediment of such “beneficial” “low power operations”:

The standby current generated in a conventional memory, such as a synchronous memory, having a clock tree structure may be

substantially the same as that in a non-standby state. This may be the case because the clock signal is used as a transmission reference signal for synchronous memory operations and, therefore, ***the clock signal is, typically, internally produced irrespective of whether an operation is being performed by the synchronous memory.***

Ex. 1005, Lee ¶ [0005] (emphasis added); Jacob Decl., ¶ 89. Indeed, the benefits of foregoing the use of a continuous clock by using Lee's invention are taught throughout the disclosure of Lee. Ex. 1005, Lee ¶ [0028] ("The memory 120 operates in an asynchronous fashion, for example, a fashion using a conventional technique that utilizes a delay chain as a state machine. Furthermore, as is seen from the discussion above, the Strobe Signals SCA and SDtM that are used as transmission synchronous signals are only toggled when a transfer is occurring. ***Thus, the need for a continuous clock may be avoided and the current consumed by the memory 120 when not performing a read or write operation may be reduced over a similar memory that utilizes a continuous clock.***") (emphasis added); *Id.* ¶ [0034] ("As is discussed above, typically, the amount of current consumed by a memory system in a standby state results from the clock signal used to synchronize operations of a synchronous memory.... However, according to embodiments of the present invention, as illustrated for example in FIG. 3, the strobe signals, such as SCA and SDtM, that are used as transmission references or Synchronous Signals, are used in

the memory 120 only as a latch enable or latching Signal. *That is, the strobe signals SCA and SDtM are not used as a reference signal (e.g., a clock signal)* for a memory operation. Accordingly, certain embodiments of the present invention may be capable of reducing the standby current consumed in the memory 120 as no clocks need be generated or utilized as a reference Signal for the operations to the memory array.”) (emphasis added).

In summary, a POSITA understands that Lee teaches that the clock signal in synchronous memory systems is problematic, and this includes memory systems such as Synchronous DRAM and Double Data Rate Synchronous DRAM (SDRAM and DDR SDRAM). Ex. 2003, Jacob Dec. ¶ 90. It discloses that, in these synchronous memory systems, the clock signal enters the memory device itself, and the memory device cannot turn the clock off. *Id.* The clock signal is delivered throughout the chip by way of the memory device’s internal clock tree to all of the internal registers and components that run in time with the clock. *Id.* Consequently, the entire chip beats in time with the clock, and that beating dissipates power. *Id.* Lee indicates that the power dissipation level is such that when the memory chip is supposed to be in a standby state (i.e., functionally idle and preferentially dissipating no power at all), it is in fact generating current, and therefore dissipating power, “substantially the same as that in a non-standby state.” Ex. 1005, Lee ¶ [0005].

Accordingly, Lee's invention does *not* deliver the repeating, uninterrupted clock signal to the memory device. Ex. 2003, Jacob Dec. ¶ 91. The invention provides for a source synchronous interface with strobe signals accompanying the data, but there is no traditional "system clock" signal delivered to the memory device. *Id.* Note that this invention is unlike the well-known memory systems of the day, SDRAM and DDR SDRAM, and is in keeping with Lee's observation that those synchronous memory systems, in which the clock is delivered to the memory device, cannot reach low power levels due to the clock. *Id.* Even Lee's patent claims support this: they reference only 'an asynchronous memory,' and the word 'clock' is not found in the claims at all. Ex. 1005, Lee at 11-12.

B. JEDEC Standard JESD79C for DDR SDRAM ("JEDEC") (Ex. 1007)

In contrast to Lee, JEDEC requires that a system clock signal be delivered to the memory device. JEDEC Standard JESD79C for DDR SDRAM ('JEDEC') describes the first-generation Double Data Rate Synchronous DRAM (DDR SDRAM). Ex. 2003, Jacob Decl., ¶ 92. The following figure illustrates the package interface and shows that the DDR SDRAM receives a differential clock signal, comprising the CK and CK-bar signals, over pins 45 and 46, respectively:

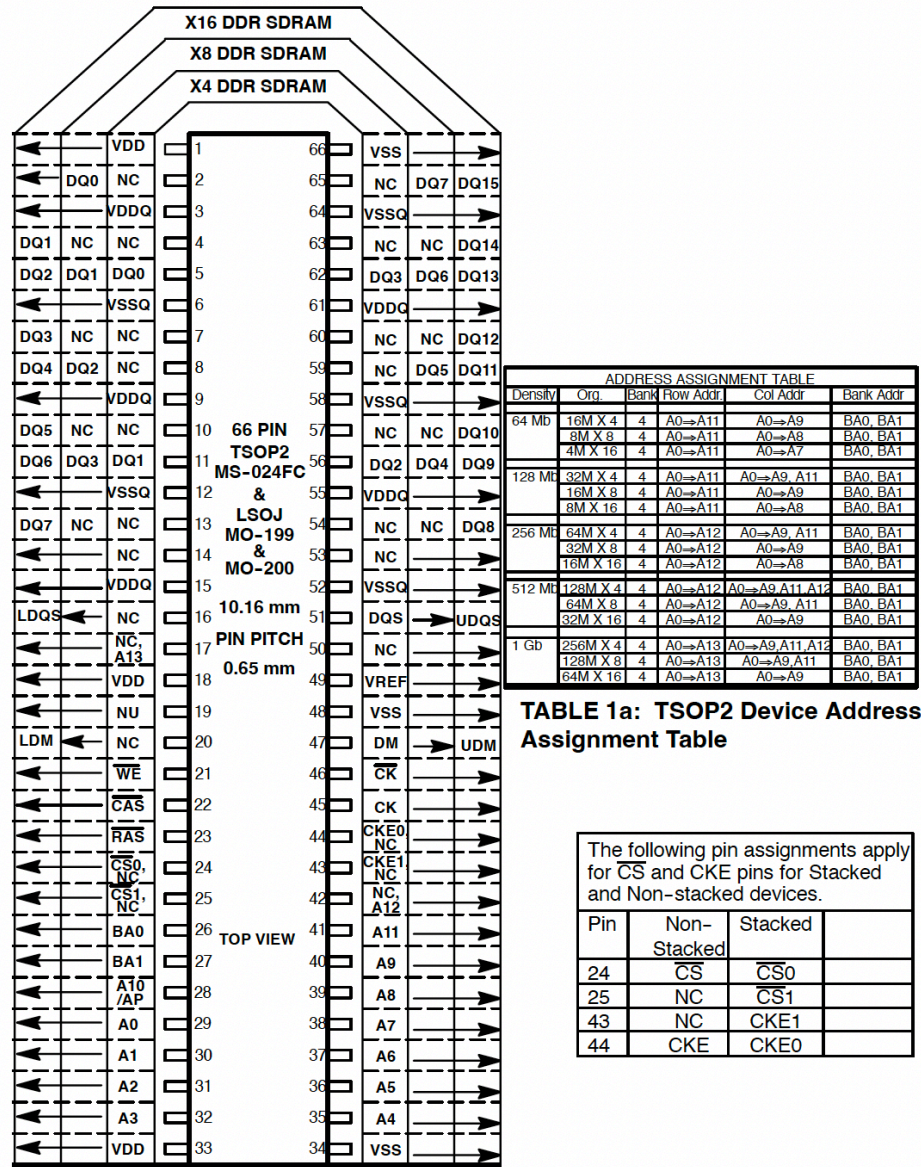
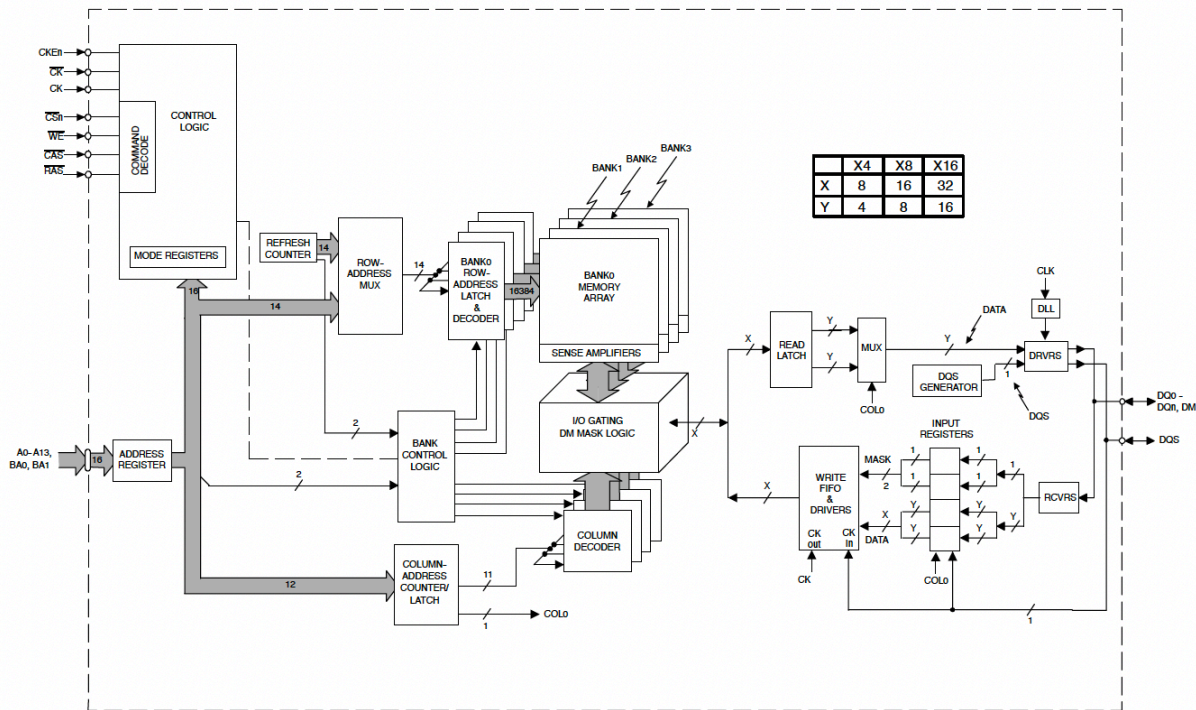


Figure 1
64 Mb Through 1Gb DDR SDRAM (X4, X8, & X16) IN TSOP2 & LSOJ

Ex. 1007, JEDEC at 9. The DRAM's block diagram shown in Figure 3 provides that the DDR SDRAM receives a differential clock signal, comprising the CK and CK bar signals:



Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note 2: DM is a unidirectional signal (input only) but is internally loaded to match the load of the bidirectional DQ and DQS signals.

Note 3: Not all address inputs are used on all densities.

FIGURE 3: FUNCTIONAL BLOCK DIAGRAM OF DDR SDRAM

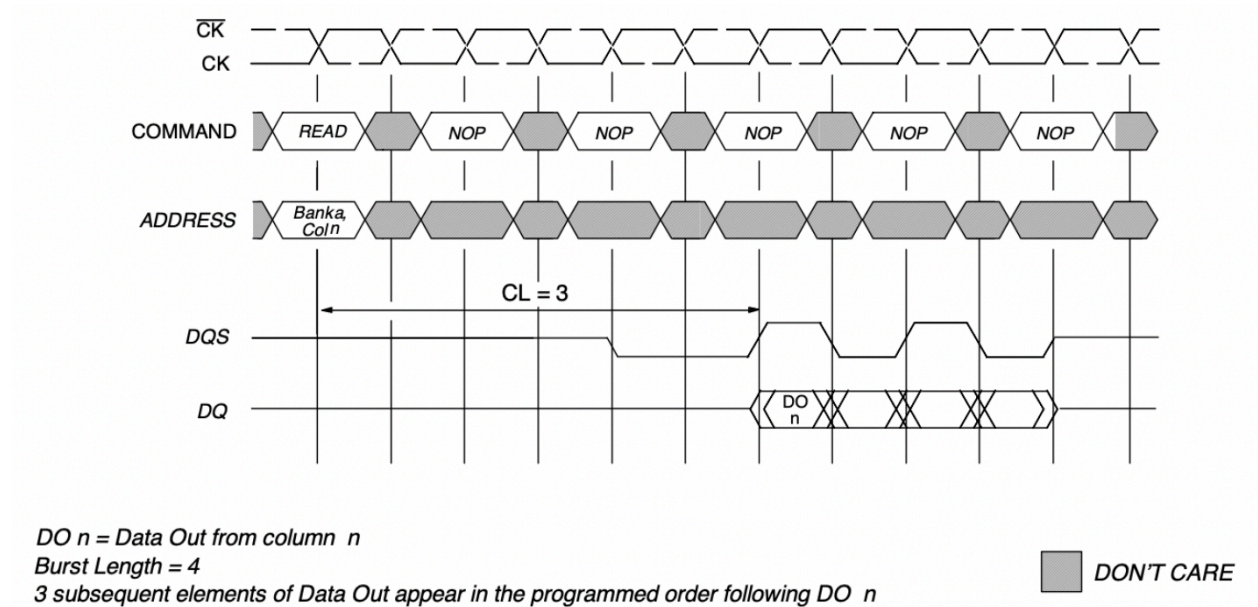
Ex. 1007, JEDEC at 11. The signals are part of the DRAM interface, shown in the upper left-hand corner of the diagram. Ex. 2003, Jacob Decl., ¶ 94.

As shown in Table 2, the commands and addresses are captured by the clock signal:

TABLE 2: PIN DESCRIPTIONS

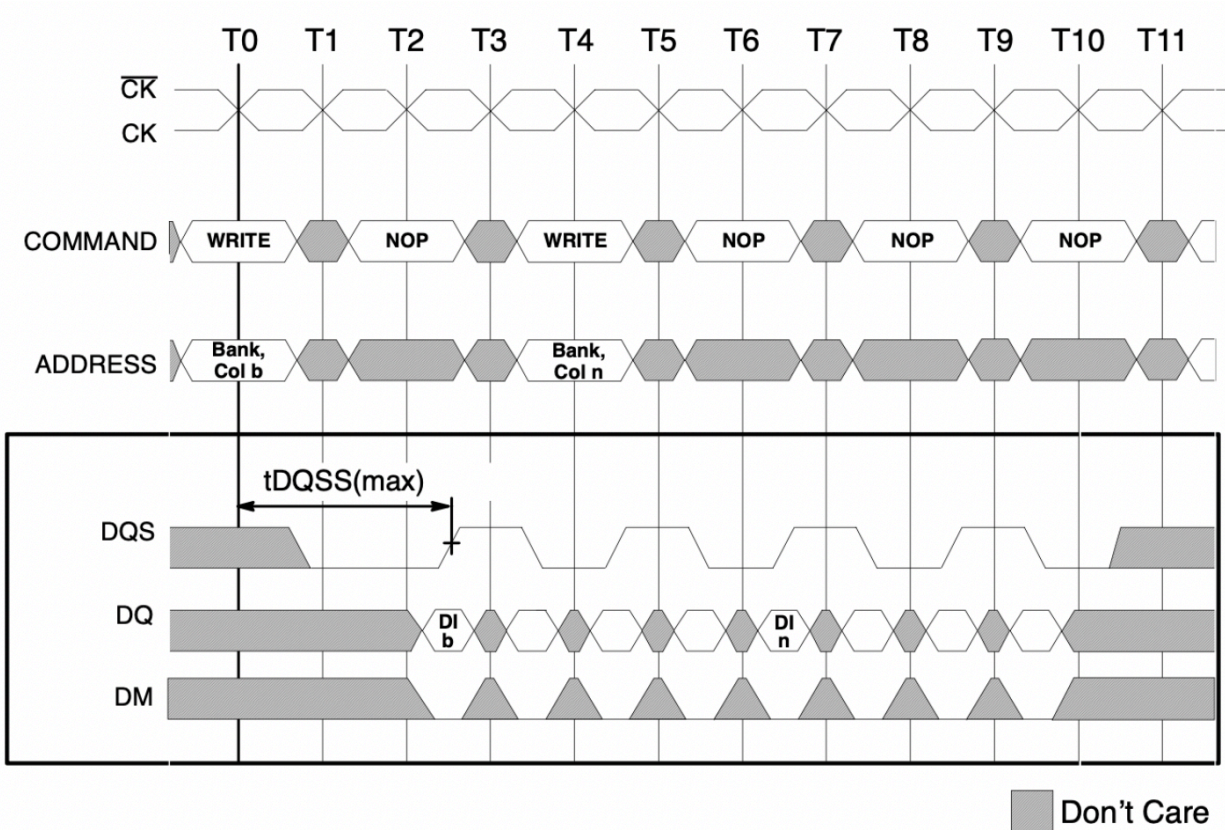
SYMBOL	TYPE	DESCRIPTION
CK, $\overline{\text{CK}}$	Input	Clock: CK and $\overline{\text{CK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{\text{CK}}$. Output (read) data is referenced to the crossings of CK and $\overline{\text{CK}}$ (both directions of crossing).

Ex. 1007, JEDEC at 12. The following shows the timing for a DDR SDRAM read operation:



Ex. 1007, JEDEC at 30. As described in the table above, the READ command on the COMMAND bus and the address on the ADDRESS bus are both captured using the clock signal. Ex. 2003, Jacob Decl., ¶ 97. The DRAM interprets the command to be a read operation. *Id.* It then delivers the data corresponding to the address onto the data bus several clock cycles later. *Id.* The data is driven onto the DQ bus by the DDR SDRAM, and at the same time the DRAM drives the DQS strobe along with the data signal, so that the memory controller can capture the data using the strobe. *Id.*

The following Figure from JEDEC shows the timing for a DDR SDRAM write operation:



Ex. 1007, JEDEC at 40. The WRITE command on the COMMAND bus and the address on the ADDRESS bus are both captured by the clock signal at time T0. Ex. 2003, Jacob Decl., ¶ 99. The DRAM interprets the command to be a write operation. It knows to expect the data when the DQS strobe signal goes high — the figure above shows this as starting at a delay of $t_{DQSS(max)}$ after T0. *Id.* The rising and falling edges of the DQS signal are used to capture the data values into a buffer. *Id.* The DRAM then delivers the data to the corresponding address (shown as **Bank, Col b**) in the memory array. *Id.*

As the timing diagrams show, and as the specification indicates, the commands and addresses are captured by the system clock, which is part of the DRAM interface, and the data bits are captured by the DQS data strobe. Ex. 2003, Jacob Decl., ¶100.

III. Level of Ordinary Skill in the Art

The Petition proposes that a person of ordinary skill in the art in the field of the '369 Patent “would have had a bachelor’s degree in electrical engineering, or an equivalent, and approximately two years of professional experience relating to field of memory systems.” Pet. at 15. For purposes of this IPR, Patent Owner does not challenge that definition. Ex. 2003, Jacob Decl., ¶21.

IV. Claim Construction

The Board does not construe any claim terms unnecessary to resolve the parties’ dispute. *Shenzhen Liown Electronics Co. v. Disney Enterprises, Inc.*, IPR2015-01656, Paper 7 at 10 (Feb. 8, 2016) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). The Petition states that “Petitioner contends no claim term requires express construction.” Pet. 5. For purposes of this IPR, Patent Owner agrees that no express construction of any term is necessary. Accordingly, the claim terms should be interpreted in accordance with the ordinary and customary meaning as understood by one of ordinary skill in the art. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005).

V. The Petition’s Ground 2 fails.

The Petition’s Ground 2 is based on combining Lee with JEDEC to incorporate JEDEC’s teaching of a continuous clock signal to meet the requirements of claims. Specifically, the Petition contends that “[a] POSITA would have found it obvious for Lee’s SCA signal to be implemented as a continuous clock signal consistent with the JEDEC standard for memory systems.” Pet. at 57. This ground fails as it fails to show a motivation to combine. Specifically, no motivation to combine the references exist as the proposed combination would render Lee inoperable for its intended purpose of achieving low power operation.

As the Board is no doubt aware, an obvious combination requires evidence that a POSITA would have been motivated to combine the references. *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993–94 (Fed. Cir. 2017) (“reasoning [that] seems to say no more than that a skilled artisan, once presented with the two references, would have understood that they could be combined ... is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention”); *Belden Inc. v. Berk–Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.”). As the Federal Circuit recently reaffirmed a finding of obviousness requires the existence of “a motivation

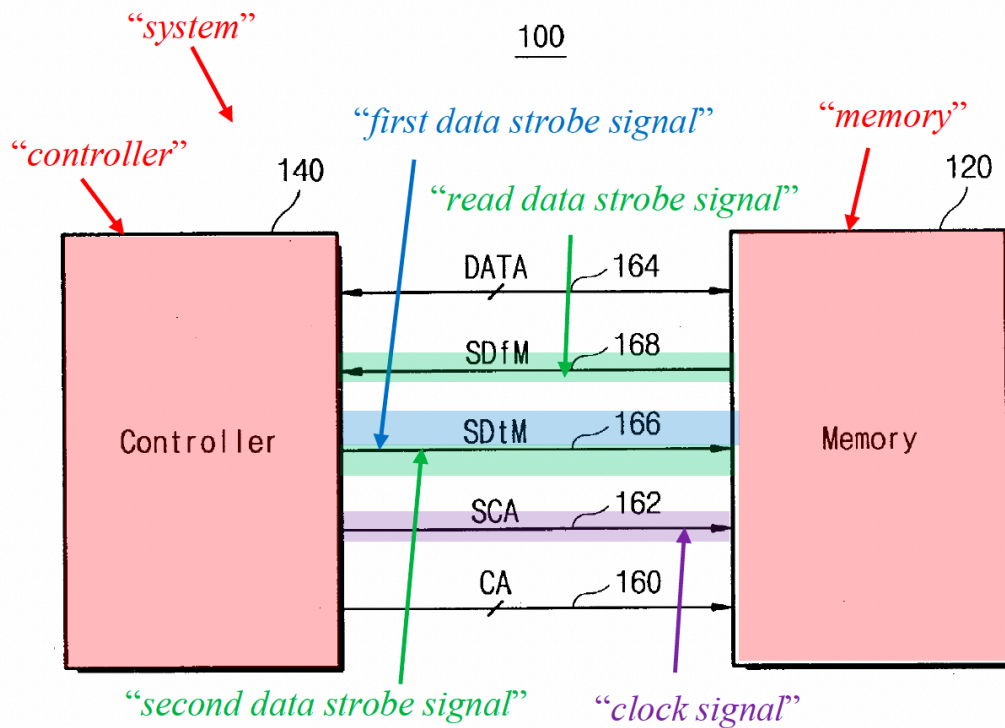
to combine various prior art references in order for a skilled artisan to make the claimed invention.” *Virtek Vision Int'l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882, 887 (Fed. Cir. 2024) (“It does not suffice to simply be known. A reason for combining must exist.”).

No motivation to combine exists where the proposed combination would render the primary reference inoperable for the intended purpose. *See Plas-Pak Indus., Inc. v. Sulzer Mixpac AG*, 600 F. App’x 755, 760 (Fed. Cir. 2015) (affirming the Board’s finding that a combination of references would render the reference “‘inoperable for its intended purpose,’ and a person of ordinary skill would thus not have been motivated to pursue the combination”). When a substitution such as the would “defeat[] the purpose of” the system being modified, that “substitution is illogical” and cannot provide the basis for an obviousness determination. *In re Schweickert*, 676 F. App’x 988, 994 (Fed. Cir. 2017); *see also Plas-Pak*, 600 F. App’x at 760 (affirming the Board’s finding that a combination of references would render the reference “‘inoperable for its intended purpose,’ and a person of ordinary skill would thus not have been motivated to pursue the combination”).

As noted above Lee teaches an asynchronous memory that, by definition, does not receive a system clock. Specifically, Lee seeks to “*avoid*” “*the need for a continuous clock*” and reduce “the current consumed by the memory 120 when not performing a read or write operation ... over a similar memory that utilizes a

continuous clock.” Ex. 1005, Lee ¶ [0028] (emphasis added). It expressly avoids the clock tree structure in “conventional ... synchronous memory” “that produces a clock signal” “*irrespective of whether an operation is being performed*” and thus produces the same current in a “standby” and “non standby state” *Id.* ¶ [0005]. It further refers to such a “low power mode” as being “beneficial.” *Id.* ¶ [0004].

Accordingly, introducing the continuous clock—which Lee seeks to avoid—by using Petitioner’s proposed combination with JEDEC would render Lee inoperable for its intended purpose because it would remove the lower power operability. Ex. 2003, Jacob Decl., ¶¶ 101-110. Indeed, the specific combination of Lee and JEDEC urged by Petitioner and its expert was eschewed by Lee as frustrating its purpose of reducing power consumption. The Petition and Dr. Baker base their combination on implementing Lee’s SCA signal “as a continuous clock signal”:



Combination of Lee and JEDEC
(annotated based on EX1005, Lee, Fig. 1); EX1003, ¶ 117.

Pet. at 64-65 (“A POSITA would have found it obvious to substitute Lee’s SCA signal using a clock signal”). Ex 1003, Baker Decl., ¶¶114-118. Lee, specifically provides, however, *“the strobe signals SCA and SDtM are not used as a reference signal (e.g., a clock signal) for a memory operation.”* Ex. 1005, Lee ¶ [0034]. Dr. Baker notes that Paragraph 35 of Lee provides that “SCA ... can be implemented using a clock signal that is toggled only during the desired period.” Ex 1003, Baker Decl., ¶115. However, such disclosure by its clear terms does not endorse the use of a “continuous clock” but one that “is toggled only during the desired period.” Again,

Petitioner’s proposed combination would leave the clock always “toggled on” and thus frustrate the intended purpose of Lee.² Ex. 2003, Jacob Decl., ¶107-110.

Being faced with this contradiction, the Petition and Dr. Baker seek to refer to the use of a continuous clock as a “design tradeoff”:

A POSITA would have understood that there are design tradeoffs between using synchronous and asynchronous memories. For example, asynchronous memory can provide the benefit of less power consumption, as explained by Lee. See EX1005, Lee, [0034]. Synchronous memory—using a clock signal for sampling information—provides the benefit of higher bandwidth capabilities. See EX.1006 (Prince), 5. Indeed, POSITAs used systems that had the capability to switch between synchronous and asynchronous modes.

² Lee’s teaching of avoiding a continuous clock rises to the level of teaching away from using Petitioner’s combination. In re Brandt, 886 F.3d 1171, 1178 (Fed. Cir. 2018) (“A prior art reference evidences teaching away if it ‘criticize[s], discredit[s], or otherwise discourage[s] the solution claimed.’”) (*In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004)); *Meiresonne v. Google, Inc.*, 849 F.3d 1379, 1382 (Fed. Cir. 2017) (“A reference teaches away ‘when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken’”) (quoting *Galderma Labs., L.P. v. Tolmar, Inc.*, 737 F.3d 731, 738 (Fed. Cir. 2013)). However, as the combination clearly renders Lee inoperable for its intended purpose of providing a low power mode by avoiding a continuous clock, the Board need not reach this determination.

See generally EX1008, Mills, title, abstract. Accordingly, a POSITA implementing a memory system according to Lee's teachings would have found it obvious to use either synchronous or asynchronous memory, as either was a known option, and would choose between the two based on their specific design/power considerations.... If a POSITA wanted to design the system for power conservation, they would likely choose Lee's asynchronous option. If a POSITA wanted to design the memory system for high bandwidth, they would likely choose the synchronous option. EX1003, ¶ 110.

Petition at 59-60; *also*, Baker Decl., ¶110. However, the Prince (Ex. 1006) reference Petitioner and Dr. Baker cite refutes that this is a mere design choice. Instead, it notes that asynchronous memory requires "more expensive technology" to have "equivalent speed" as synchronous memory:

For processors of 50 MHz and above the most cost-effective solution for 586 class systems is the synchronous SRAM, since *an asynchronous SRAM must be in a more expensive technology, such as BiCMOS, to have an equivalent speed with an otherwise identical synchronous SRAM*. Above 66 MHz a synchronous burst pipelined part is preferred to an equivalent technology synchronous flowthrough

part because of the reduced access time of the pipelined burst part at essentially the same cost.

Ex. 1006 at 6. *See also* Ex. 2004, Baker Tr. at 24:10-14 (Prince is “writing that asynchronous SRAM must be in a more expensive technology”).

Here, Lee teaches a new asynchronous memory design. Ex. 2003, Jacob Decl., ¶ 88.³ Yet, Petitioner and Dr. Baker contend that a POSITA being presented with such teaching and looking to design a more expensive form of memory, would nonetheless combine it with teaching concerning synchronous memory and do it in a way that frustrates the purpose and fundamental teaching of Lee.

Moreover, Petitioner’s contention that “[a] POSITA would have understood that there are design tradeoffs between using synchronous and asynchronous memories” does not show a reason to combine Lee and JEDEC. *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993–94 (Fed. Cir. 2017) (“[R]easoning [that] seems to say no more than that a skilled artisan, once presented with the two references, would have understood that they could be combined ... is not enough: it does not imply a motivation to pick out those two references and combine them to

³ As Dr. Jacob explains in his declaration, Dr. Baker has not defined “asynchronous memory” consistent with the understanding of a POSITA. Ex. 2003, Jacob Decl., ¶¶ 75-85. A synchronous memory device does not merely synchronize various signals with the system clock, it receives the system clock. *Id.* An asynchronous memory does not receive a system clock as is taught by Lee.

arrive at the claimed invention”). Instead, this is strongly suggestive of improper hindsight reasoning. *See KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. at 398, 421 (2007) (“A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning.”). And the fact that the Petition may, with the benefit of hindsight, cobble together a combination of known elements that might, when arranged in a specific way, teach the invention, is not evidence of obviousness, “because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.” *Id.* at 418–19; *Cheese Sys., Inc. v. Tetra Pak Cheese & Powder Sys., Inc.*, 725 F.3d 1341, 1352 (Fed. Cir. 2013) (“Obviousness ‘cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention.’”) (quoting *ATD Corp. v. Lydall, Inc.*, 159 F.3d 534, 546 (Fed. Cir. 1998)). “[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention” (*Belden*, 805 F.3d at 1073 (Fed. Cir. 2015) (emphases in original)) and the Petition ultimately provides no coherent reason why a POSITA *would have been motivated to make* the specific combination of Lee and JEDEC it alleges.

Accordingly, the Petition does not demonstrate a reasonable likelihood of prevailing with respect to Ground 2.

VI. Conclusion

Because the Petition fails to provide evidence that a POSITA would have been motivated to combine Lee and JEDEC its Ground 2 fails. Accordingly, the Petition fails to show that claims 2, 7, and 11 of the '369 Patent are unpatentable.

Date: May 3, 2024

Respectfully submitted,
/ James A. Milkey /
James A. Milkey, Reg. No. 79,503
Russ, August & Kabat
12424 Wilshire Blvd., 12th Floor
Los Angeles, CA 90025

Counsel for Patent Owner

CERTIFICATION REGARDING WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner certifies that there are 3,915 words in the paper excluding the portions exempted under 37 C.F.R. §42.24(a)(1).

Date: May 3, 2024

Respectfully submitted,
/ James A. Milkey /
James A. Milkey, Reg. No. 79,503
Russ, August & Kabat
12424 Wilshire Blvd., 12th Floor
§Los Angeles, CA 90025

Attorney for Patent Owner

CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e)(1))

The undersigned hereby certifies that the above document was served on May 3, 2024, by filing this document through the Patent Trial and Appeal Case Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

David O'Dell
Hong Shi
david.odell.ipr@haynesboone.com
hong.shi.ipr@haynesboone.com
HAYNES AND BOONE, LLP

Date: May 3, 2024

/ James A. Milkey /

RUSS AUGUST & KABAT
12424 Wilshire Blvd., 12th Fl.
Los Angeles, CA 90025
(310) 826-7474

James A. Milkey, Reg. No. 79,503
Reg. No. 79,503
Attorney for Patent Owner