

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

LONGITUDE LICENSING LTD.,
Patent Owner

IPR2023-01200
Patent No. 7,697,369 B2

PETITIONER'S REPLY

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PETITIONER'S EXHIBIT LIST

Updated: July 26, 2024

EX1001	U.S. Patent No. 7,697,369
EX1002	Prosecution History of U.S. 7,697,369
EX1003	Declaration of R. Jacob Baker under 37 C.F.R. § 1.68
EX1004	<i>Curriculum Vitae</i> of R. Jacob Baker
EX1005	U.S. Patent Publication No. 2004/0022095 to Lee et al. ("Lee")
EX1006	<i>High Performance Memories: New Architecture DRAMs and SRAMs Evolution and Function</i> , Betty Prince (1999) ("Prince")
EX1007	JEDEC Standard: Double Data Rate (DDR) SDRAM Specification, JESD79C (March 2003) ("JEDEC")
EX1008	U.S. Patent No. 6,026,465 to Mills et al. ("Mills")
EX1009	U.S. Patent No. 6,956,409 to Streif et al. ("Streif")
EX1010	U.S. Patent Publication No. 2006/0064561 to Simeral et al. ("Simeral")
EX1011	Order Granting Motion to Stay (Lenovo) (05-16-23)
EX1012	Order Granting Western Digital's Motion to Intervene (Amazon) (05-16-23)
EX1013	Director Vidal Memo re: Discretionary Denials, June 22, 2022
EX1014 (NEW)	U.S. Patent No. 6,336,159 ("the '159 Patent")
EX1015 (NEW)	Deposition Transcript of Dr. Bruce L. Jacob, June 27, 2024

I. Introduction

The Petition and the record as a whole provide detailed reasons why the cited art renders the challenged claims of the '369 Patent obvious. There are two Grounds in the Petition (Paper 2), Ground 1 challenges claims 1, 6, 10, 14, 15, 16, 17, 18, 19, 25, 26, and 27 as obvious over Lee (EX1005) alone and Ground 2 challenges claims 2, 7, and 11 as obvious over the combination of Lee in view of JEDEC (EX1007). Petition at 16. The Patent Owner Response (Paper 16, "POR") does not contest Ground 1, and only contests Ground 2 on the basis of insufficient reasons to combine Lee and JEDEC, including that either Lee teaches away from the combination or that the combination renders Lee inoperable for its intended purpose. None of the arguments in the POR adequately refute the evidence of record.

In summary, both the '369 Patent and the prior art reference Lee are directed to a technique called "source-synchronous" operation, which is discussed below. Source-synchronous operation is a well-known and prior art process. See e.g., Deposition of Patent Owner's Expert, Dr. Jacob (EX1015, "Jacob Depo"), 11:4-18; Declaration of Dr. Jacob (EX2003, "Jacob Decl."), ¶¶ 31-32. The alleged inventive concept of both the '369 Patent and Lee is to modify the conventional source-synchronous operation by adding an additional strobe signal used to

transfer data during read operations, hereinafter referred to as the “turnaround strobe”.¹ Source-synchronous operation using a turnaround strobe is the subject matter of Ground 1 (e.g., claim 1) of the present IPR, was discussed in the Institution Decision, and the fact that this operation is also (and previously) taught by Lee is not challenged by the Patent Owner. POR, 1; Institution Decision (Paper 6), 18-22.

While the ‘369 Patent and Lee both describe the same source-synchronous operation for the transfer of data signals, they are different in that the primary embodiment of the ‘369 Patent uses “synchronous” memory, which uses a clock for the transfer of address and control signals, while the primary embodiment of Lee uses “asynchronous” memory which does not use a clock for the transfer of address and control signals. However, there are multiple reasons why it would be obvious to use Lee’s source-synchronous operation with synchronous memory, many of which were spelled out in the Petition and which will be further discussed

¹ The term “turnaround strobe” was not used in the Petition, but was used by the Patent Owner’s expert, Dr. Jacob, during deposition and is adopted herein as a shortcut way to describe the modified source-synchronous operation of the ‘369 Patent. EX2003, Jacob Decl., 14:17-18, *see generally*, pp. 13-15.

below. As for the Patent Owner's argument that Lee either teaches away from using synchronous memory (and a clock) or that the combination of Lee and JEDEC render Lee inoperable for its intended purpose by using synchronous memory, those arguments fail for multiple reasons set forth below. For one, Lee is clear that asynchronous memory is an example application, or use, for its source-synchronous operation. Thus as described in the Petition and further discussed below, a POSITA would find it obvious to use Lee's source-synchronous operation with synchronous memories (memories using a clock signal), thereby rendering unpatentable the claims identified in Ground 2 of the Petition.

II. Claim Construction

No express claim construction necessary.

III. Source-Synchronous Operation and Turnaround Strobe

As discussed above, both the '369 Patent and the Lee prior art reference are directed to a well-known practice of memory systems called *source-synchronous* operation. Interestingly, both the '369 Patent and Lee incorporate by reference

prior art patents that describe source-synchronous operation.² Patent Owner's expert, Dr. Jacob, also describes the well-known, conventional, prior-art source-synchronous operation in his declaration. Jacob Decl., ¶¶ 31-32.

The alleged inventive concept of the '369 Patent is a process that PO's expert Dr. Jacob refers to as a "turnaround strobe" process. *See* fn1, *supra*. Relevant portions of claim 1 of the '369 Patent are reproduced below with the strobe and data signals used in a conventional source-synchronous read operation colored in [blue](#), and the additional turnaround strobe colored in [green](#).

1. A system comprising:
 - a controller ... being adapted, in a **read operation**, to send out [a second data strobe signal](#) ...; and
 - a memory ... being adapted, in the **read operation**, to output the [read data strobe signal](#) [in response to the second data strobe signal](#)

² The '369 Patent incorporates by reference U.S. Pat. No. 6,789,209B1 in which "[d]ata signals are sent out from the sender is synchronized with the data strobe signal." '369 Patent, 1:12-17. Lee incorporates by reference U.S. Pat. No. 6,336,159 titled "Method and Apparatus for Transferring Data in Source-Synchronous Protocol and Transferring Signals in Common Clock Protocol in Multiple Agent Processing System." Lee, ¶[0018].

and to send the read data signal synchronized with the read data strobe signal.

‘369 Patent, claim 1. The Petition further discusses this purported novelty of the ‘369 Patent, including how this turnaround strobe was amended and emphasized during prosecution in order to obtain allowance of the patent. Petition, 11-14.

This turnaround strobe process also describes the inventive concept of the prior art reference Lee. The same color coding is applied below with the strobe and data signals used in a conventional source-synchronous read operation colored in blue, and the additional turnaround strobe colored in green.

For a **read operation**, in addition to the command/address information CA, the memory controller 140 transfers to the memory 120 the second strobe signal SDtM as a transmission synchronous or reference signal at a time when it wants to receive data read out from the memory 120. The memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM. The read data that is read from the memory 120 is sent to the memory controller 140 together with the third strobe signal SDfM. Therefore, during the read operation the memory controller 140 receives the read data DATA from the memory 120 together with the third strobe signal SDfM at a required time, by sending the second strobe signal SDtM to the memory 120 after it transmits the command and address information to the memory 120.

Lee, ¶[0021].

It is noted that none of the discussion above describes or refers to synchronous or asynchronous memory, neither does it describe a clock or the absence thereof.

IV. Ground 2: It Would be Obvious to Use a Clock in Lee's Source Synchronous Memory System

There are multiple reasons identified in the Petition, and additional reasons discussed below, why a POSITA would combine the teachings of Lee and JEDEC to teach a source-synchronous memory operation, including a clock signal, as recited in claim 2 of the '369 Patent, as well as the remaining claims identified in Ground 2 of the Petition.³ Furthermore, although Lee discusses some of the benefits of using asynchronous memory, Lee is not limited to asynchronous

³ It is noted that there are other elements in the claims of Ground 2 which are clearly shown in the Petition and which were not contested in the Patent Owner Response. Therefore, the present discussion will focus on the clock signal sent to the memory, as recited in claim 2 of the '369 Patent and discussed in the POR.

memory, neither does Lee teach away from using synchronous memory nor would Lee be inoperable for its intended purpose by using synchronous memory.⁴

A. Reasons to Use a Clock Signal in Lee's Memory System

The Petition listed multiple reasons to combine the teaching of JEDEC, which describes a synchronous DRAM (SDRAM) that uses a clock signal, in the memory system of Lee. These include:

1. Increased bandwidth

Synchronous memory—using a clock signal for sampling information—provides the benefit of higher bandwidth capabilities. Petition, 60-61, citing EX.1006 (Prince), 5. Increased bandwidth, as compared to reduced power, was a well-known design choice for a POSITA, as explained by Petitioner's expert Dr. Baker. EX1003, ¶110 (“If a POSITA wanted to design the system that emphasized power conservation, they could choose Lee's asynchronous option. If a POSITA wanted to design the memory system that emphasized high bandwidth, they could choose the synchronous option.”)

⁴ For the sake of the present discussion, referring to “synchronous memory” means using a “clock signal,” as that term is recited in the claims.

The Patent Owner addresses this argument in its Response, noting that “asynchronous memory requires ‘more expensive technology’ to have ‘equivalent speed’ as synchronous memory.” POR, 18, citing Prince, 5; see also, Jacob Decl., ¶70. It is clear that for a given processing technology, synchronous memory is faster than asynchronous memory. To drive this point home, the Prince textbook gives an example:

The conclusion is that a 15 ns asynchronous SRAM⁵ could give 0 wait states to about 40 MHz, while a 9 ns burst SSRAM in the same 0.5 micron technology could give 0 wait states to 66 MHz and a 7 ns pipelined burst SSRAM could give 0 wait states over 75 MHz.

Prince, 18. Thus in summary, an asynchronous memory (SRAM) can run at a slower 40 MHz speed, while a synchronous memory (SSRAM) using the same 0.5 micron fabrication technology can run at a faster 66 or 75 MHz speed. Thus, a POSITA would have reason to combine the teachings of Lee and JEDEC to produce a system with higher bandwidth.

The POR also accuses the reasons listed in the Petition, including synchronous and asynchronous having design tradeoffs, as being improper

⁵ SRAM is static random access memory; SSRAM is synchronous SRAM.

hindsight. POR, 20. However, the Petition did not just merely state that synchronous devices existed, but rather stated several specific reasons, and motivations, to combine the teaching of Lee with the synchronous device of JEDEC. A “motivation to combine may be found explicitly or implicitly in market forces; design incentives; the ‘interrelated teachings of multiple patents’; ‘any need or problem known in the field of endeavor at the time of invention and addressed by the patent’; and the background knowledge, creativity, and common sense of the person of ordinary skill.” *Zup v. Nash Mfg.*, 896 F.3d 1365, 1371, (Fed. Cir. 2018) (quoting *Plantronics, Inc. v. Aliph, Inc.*, 724 F.3d 1343, 1354 (Fed. Cir. 2013) (citing *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1328 (Fed. Cir. 2009) (quoting *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418-421 (2007))).

This leads us to the next reason to combine described in the Petition.

2. *Reduced cost to fabricate*

Continuing with the discussion above, a synchronous memory fabricated using an older semiconductor technology can achieve similar bandwidth as an asynchronous memory fabricating using a newer, and more costly, semiconductor technology. See above. Therefore, another reason to combine the teachings of Lee and JEDEC is to save cost.

To the extent the PO argues that using asynchronous memory with source-synchronous operation makes the memory run faster, that is not the case, nor is it technically supported by any evidence from either Lee or PO's expert. The inventive concept of adding a turnaround strobe to a source-synchronous memory system, such as is taught in Lee, allows the controller to control, and potentially delay, when the memory device will respond with its read data and read data strobe. *See* Lee, ¶[0021].

3. Industry Standard

Another reason to use clocked memory with Lee is that synchronous memory—using a clock signal for sampling control and address information—had an industry standard describing its use and operation. *See* Petition, 61, *see also*, Baker Decl. 111 (The JEDEC standard for synchronous DRAM describes the use of a continuous clock signal that is transmitted from the controller to the memory); Jacob Decl., ¶¶94-100. Thus, the very existence of the JEDEC Standard (JEDEC, EX10007) would teach, motivate, and enable a POSITA to use and design memories with a clock.

Additional reasons to use synchronous memory features, including a clock signal, in Lee's memory system are also provided by Patent Owner's expert, Dr. Bruce Jacob. These include:

4. *Synchronous memories have predictable timing, have less skew, faster turnaround on requests, and support high-bandwidth operations such as burst mode*

Dr. Jacob provides an historical account of "The Evolution of DRAM from Asynchronous to Synchronous" in his declaration. Jacob Decl., ¶¶62-70. This account describes how memory devices were asynchronous in the mid-1970s but eventually evolved to become synchronous. *Id.* The account also describes many benefits that synchronous memory provides over asynchronous memory. For example, SDRAM provides more predictable timing, and less skew:

[B]y associating all data and control transfer with a clock signal, the timing of events is made more predictable. Such a scheme, by definition, has less skew. Reduction in skew means that the system can potentially achieve faster turnaround on requests, thereby yielding higher throughput.

Jacob Decl., ¶70. In another example:

Synchronous DRAMs support the concept of a *burst mode*; SDRAM devices have a programmable register that holds a burst length ... which reduces the command bandwidth used.

Jacob Decl., ¶70.

These benefits recognized by PO's expert describe additional reasons for a POSITA to use synchronous memory features, such as described in JEDEC, in their designs, including in Lee's memory system.

5. *Reduced cost and simplicity of design*

During his deposition, PO's expert Dr. Jacob provided even more reasons to use synchronous memory over asynchronous memory, including design cost savings and simplicity of design.

Well, I gave that characterization of synchronous versus asynchronous. Honestly, I don't know exactly why the industry transitioned. If we're talking about DRAMs. I don't know why the industry transitioned from one to the other.

Presumably, it was -- it was cost-saving reasons. And simpler design meant less -- less money spent. I'm guessing. I think that's what the transition was about. But I -- I didn't -- I don't think I expressed the opinion on why the industry did it. But I do know that synchronous designs tend to be simpler than asynchronous designs because you are

now having things all happen on a clock. And so the – the movement of data and commands through the system looks more like the movement of traffic through a city with regular stoplights at the end of every block. And so it's more regular, it's more predictable. And therefore, it's easier to design.

You give up some amount of latency in doing it, but you -- you know, in that you have longer latencies. But the tradeoff is simplicity. So, you know, I think that's -- that's the benefits, but again, I don't know exactly why the industry transitioned from one to the other.

Jacob Decl., 22:10 – 23:8; see generally, pp. 22-25. Cost savings and simpler designs provided by Dr. Jacob are universal motivations known in memory system design, and are additional reasons why a POSITA would use a synchronous memory features, such as described in JEDEC, in Lee's memory system. *See Intel Corp. v. PACT XPP SCHWEIZ AG*, 61 F. 4th 1373, 1380 (holding that “universal” motivations known in a particular field to improve technology provide “a motivation to combine prior art references *even absent any hint of suggestion* in the references themselves.”) (emphasis original).

B. Lee does not *teach away* from using synchronous memory, neither does synchronous memory render Lee inoperable for its intended purpose

The bulk of the POR is spent arguing that Lee either teaches away from using a clock, or synchronous memory, or that the combination of Lee and JEDEC's synchronous memory renders Lee inoperable for its intended purpose. The POR's basis for this argument is from four paragraphs in Lee, reproduced below in their entirety:

[0004] Various memory configurations have been utilized in conventional mobile processing systems such as Personal Communication Service (PCS), cellular, or Personal Digital Assistant (PDA). Such memory systems include non-volatile and volatile memories. Because mobile processing systems typically operate using a power supply voltage supplied from a battery, low-power operation of the memory system included in the mobile processing system may be beneficial. In particular, because mobile processing systems may spend much of their operational time in a standby state, memory systems that may provide low-power operation while the mobile processing system is in the standby state may also be beneficial.

[0005] The standby current generated in a conventional memory, such as a synchronous memory, having a clock tree structure may be substantially the same as that in a non-standby state. This may be the case because the clock signal is used as a transmission reference

signal for synchronous memory operations and, therefore, the clock signal is, typically, internally produced irrespective of whether an operation is being performed by the synchronous memory.

[0028] The memory 120 operates in an asynchronous fashion, for example, a fashion using a conventional technique that utilizes a delay chain as a state machine. Furthermore, as is seen from the discussion above, the strobe signals SCA and SDtM that are used as transmission synchronous signals are only toggled when a transfer is occurring. Thus, the need for a continuous clock may be avoided and the current consumed by the memory 120 when not performing a read or write operation may be reduced over a similar memory that utilizes a continuous clock.

[0034] As is discussed above, typically, the amount of current consumed by a memory system in a standby state results from the clock signal used to synchronize operations of a synchronous memory. If the memory uses the clock signal as an operation reference signal, the clock signal, typically, continues to be generated even while in the standby state. Thus, internal circuits that use or generate the clock signals continue to operate and consume current. However, according to embodiments of the present invention, as illustrated for example in FIG. 3, the strobe signals, such as SCA and SDtM, that are used as transmission references or synchronous signals, are used in the memory 120 only as a latch enable or latching signal. That is, the strobe signals SCA and SDtM are not used as a reference signal (e.g.,

a clock signal) for a memory operation. This means that the memory 120 performs read and write operations in an asynchronous manner, for example, using a delay chain as a state machine. Accordingly, certain embodiments of the present invention may be capable of reducing the standby current consumed in the memory 120 as no clocks need be generated or utilized as a reference signal for the operations to the memory array.

Lee, ¶¶ [0004], [0005], [0028], [0034], underlining added.

None of these four paragraphs, nor the rest of Lee, teaches away from using synchronous memory or otherwise supports PO's argument that combining Lee with JEDEC's synchronous memory renders Lee inoperable for its intended purpose. Reasons include:

1. Lee is merely stating potential benefits of using asynchronous memory in his memory system

In the above-recited paragraphs, Lee is clearly stating that asynchronous memory “*may*” be beneficial in mobile applications, or that using its source synchronous operation “*may*” avoid a need for a continuous clock, or that current consumption “*may*” be reduced. *Id.* ¶¶ [0004], [0005], [0028]. Paragraph [0034] is clearly limited to “certain embodiments.” The case law is clear that “the teaching away inquiry does not focus on whether a person of ordinary skill in the

art would have merely favored one disclosed option over another disclosed option.” *Bayer Pharma AG v. Watson Labs. Inc.*, 874 F.3d 1316, 1327 (Fed. Cir. 2017). Likewise, “the fact that the motivating benefit comes at the expense of another benefit, however, should not nullify its use as a basis to modify the disclosure of one reference with the teachings of another. Instead, the benefits, both lost and gained, should be weighed against one another.” *Winner Int’l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 (2000); see also, *Medchem v. Rolabo*, 437 F.3d 1157, 1165 (2006).

The reasons to combine listed above provide many benefits and reasons why a POSITA would indeed choose to use synchronous memory instead of asynchronous memory in Lee’s memory system, which does not render Lee’s memory system inoperable for its intended purpose.

2. *Lee does not impose an intended purpose of only using asynchronous memory as asserted by Patent Owner, and does not clearly discourage using synchronous memory*

The paragraphs from Lee listed above clearly state that asynchronous memory “may” provide low-power operation and be beneficial in mobile applications, or that absence of a clock signal “may” reduce current consumption

in some embodiments. These potential benefits do impose an alleged “intended purpose” to produce Lee’s invention with only asynchronous memory. As also discussed above, Lee’s inventive concept was a source-synchronous process with a turnaround strobe, which can be used with asynchronous memory and can also be used with synchronous memory.

Patent Owner’s attempt to cast one of Lee’s potential benefits as its intended purpose of providing “a low power mode by avoiding a continuous clock” (POR, 17 n2) is contrary to *Plas-Pak*, the case relied by Patent Owner. *See, Plas-Pak Indus., Inc. v. Sulzer Mixpac AG*, 600 F. App’x 755, 760 (Fed. Cir. 2015). In *Plas-Pak*, the Court find the prior art reference’s intended purpose of “dispensing fluid materials directly into cracks” based on description directed at “the invention,” not just a specific embodiment. *Plas-Pak Indus.*, 600 F. App’x 755 at 759 (citing statements of prior art references including “***This invention*** relates to...”).

Here, as discussed above at III, like the ’369 Patent, Lee’s invention and its intended purpose is directed at a memory system with a source-synchronous process with a turnaround strobe, which can be used with asynchronous memory and can also be used with synchronous memory. Lee, [0002] (“***The present invention*** is related to electronic devices, and, in particular, to a system that

performs data transmission between a memory and a memory controller.” Lee, [0002]; *see also* Lee, Abstract (“A memory for storing data information and/or a controller for controlling read/write operations of the memory based on a source synchronous interface.”); also *compare* claim 5 (claiming “[a] system comprising: a memory...”) and claim 12 (claiming “[a] system comprising: an asynchronous memory...”). Accordingly, Lee’s invention can be used with asynchronous memory and can also be used with synchronous memory, and Petitioner’s Ground 2 combination does not render Lee inoperable for its intended purpose.

Furthermore, the Federal Circuit has ruled that “[a] statement that a particular combination is not a preferred embodiment does not teach away absent clear discouragement of that combination.” *Syntex (U.S.A.) LLC v. Apotex, Inc.*, 407 F.3d 1371, 1380 (Fed. Cir. 2005) (citing *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994); *In re Fulton*, 391 F.3d at 1195, 1199–1200 (Fed. Cir. 2004)); *In re Ethicon, Inc.*, 844 F.3d 1344, 1351 (Fed. Cir. 2017) (“Although [the primary prior art reference] states that a ‘bioabsorbable polymer is probably more desirable,’ . . . , this statement, absent clear discouragement from use, does not compel a finding that [the prior art reference] teaches away from using VDF:HFP as a stent coating.” (citation omitted)). As discussed above, Lee’s invention, a source-synchronous

process with a turnaround strobe, can be implemented with either synchronous or asynchronous memory, and benefits exist for either implementation.

3. *Lee's inventive concept works with synchronous memory*

As discussed above, the inventive concept of Lee was to modify a source-synchronous memory system by adding a turnaround strobe from the controller to the memory during read operations. The memory would respond to the turnaround strobe by providing a read data strobe and read data back to the memory controller. *See supra*, pp. 7-10; *see also*, Lee, ¶[0021].

As also discussed above, source-synchronous operations are not limited to asynchronous memories. JEDEC is a specific example of a source synchronous memory system that utilizes synchronous memory. U.S. Patent No 6,336,159, which is incorporated by reference in Lee (¶[0018]), is another example of a source synchronous memory system that utilizes synchronous memory. The '159 Patent describes:

a system that transmits data using a source synchronous protocol while transmitting control signals using a common clock protocol in order to increase the bandwidth of transmitting data without a corresponding increase in the number of signals transmitted

Ex1014, 1:49-54, underlining added.

In *Chemours Company FC, LLC v. Daikin Industries, Ltd.*, 4 F.4th 1370, 1376 (Fed. Cir. 2021), the court found that a reference teaches away when the modification of the reference would destroy the “inventive concept” or “basic objective” of the reference. The present case is distinguished from *Chemours* because Lee’s inventive concept of a source-synchronous memory system with turnaround strobe works with synchronous or asynchronous memory.

4. *Lee’s use of asynchronous memory in a mobile application is merely an embodiment*

Lee’s use of asynchronous memory, without a clock signal, is merely one embodiment of his invention – and not even his first-mentioned embodiment.

Lee’s SUMMARY OF THE INVENTION section lists a series of different embodiments of his invention. This section of Lee begins at ¶ 7, which discusses “certain embodiments of the present invention” utilizing a “source synchronous interface.” The description in this paragraph has no reference to clock signals (or absence thereof) or to asynchronous memory. Instead, it merely refers to “memory.” The next paragraph of the summary section begins: “In still further embodiments of the present invention, a memory ...” ¶ 8. Similarly, this

paragraph does not refer to clock signals (or absence thereof) or to asynchronous memory. The third paragraph of the summary section begins: “In accordance with further embodiments of the present invention, communications with an asynchronous memory ...” ¶ 9. This third paragraph is the first time in the summary section that “asynchronous memory” is mentioned.

In Lee's DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS section, Lee first warns that “this invention should not be construed as limited to the embodiments set forth herein.” Lee, ¶ [0016]. In the next paragraph of this section, Lee clearly recites an embodiment using an asynchronous memory 120, with reference to Fig. 1 of the document. Lee, ¶ [0017]. However, in the very next paragraph of this section, Lee recites an embodiment using synchronous memory. Specifically, Lee incorporates by reference U.S. Patent No 6,336,159. Lee, ¶[0018] which describes:

a system that transmits data using a source synchronous protocol while transmitting control signals using a common clock protocol in order to increase the bandwidth of transmitting data without a corresponding increase in the number of signals transmitted

EX1014, 1:49-54.

So, it is clear that Lee teaches multiple embodiments of his invention, and that only some, but not all, of the embodiments are directed to asynchronous memory. So when Lee refers to “a memory device”, it is proper to interpret this term to cover both synchronous and asynchronous memory. Thus, Lee not only does not teach away from using synchronous memory, but actually and specifically teaches using synchronous memory.

5. *Some of Lee's claims cover synchronous memory*

Lee includes a listing of 25 claims, some of which show that Lee clearly contemplates covering both types of memory, asynchronous and synchronous. For example, consider independent claims 5 and 12 of Lee, which start as follows:

5. A system comprising: a memory ...

12. A system comprising: an asynchronous memory ...

It is noted that claim 5 never refers to “asynchronous” memory, neither does it refer to a clock (or lack thereof). The different claim terminology in these two claims highlights the fact that Lee is not limiting his invention to asynchronous memory, at least not in claim 5.

Also, U.S. Patent No. 6,336,159, which is incorporated by reference into Lee (¶[0018]), describes “a memory”, which is referring to synchronous memory. See discussion above, citing EX1014, 1:49-54. So when claim 5 of the ‘369 Patent refers to “a memory”, the specification of the patent supports that it could be either asynchronous memory or synchronous memory using a common clock protocol.

This discussion is consistent with the longstanding presumption of claim differentiation that “[i]n the absence of evidence to the contrary, we must presume that the use of these different terms in the claims connotes different meanings.” *CAE Screenplates Inc. v. Heinrich Fiedler GmbH*, 224 F.3d 1308, 1317 (Fed. Cir. 2000); *see also, Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 810 (Fed. Cir. 2021). Also, the fact that Lee’s specification refers to both synchronous and asynchronous memory would lead a POSITA to understand that Lee’s use of the term “memory” would cover both. *Nobel Biocare Services AG v. Intradent USA, Inc.*, 903 F.3d 1365, 1381 (Fed. Cir. 2018) (aff’g PTAB anticipation decision and construction; “there is a strong presumption against a claim construction that excludes a disclosed embodiment.”)⁶ Thus, since claim 5 of the ‘369 Patent uses the term “a

⁶ It is noted that Petitioner is not proposing a claim construction here, but rather how a POSITA should construe the term “memory device” in Lee’s claims.

memory” and claim 12 uses the term “an asynchronous memory”, these terms should be construed differently, and more specifically, that claim 5’s “memory” should cover both asynchronous memory and synchronous memory. This is further evidence that Lee is actually *operable* using synchronous memory for its intended purpose.

V. Conclusion

None of Patent Owner’s arguments withstand scrutiny. For the reasons stated above and the evidence as a whole, the Board should find the challenged claims unpatentable.

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Respectfully submitted,

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VI. Certificate of Word Count

Pursuant to 37 C.F.R. § 42.24, the undersigned attorney for the Petitioner declares that the argument section of this Petition (Sections I-V) has a total of 4,851 words, according to the word count tool in Microsoft Word™.

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VII. Certificate of Service

Date of service July 26, 2024

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Documents served **Petitioner's Reply;
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