

**UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD**

**WESTERN DIGITAL TECHNOLOGIES, INC.,)
)
Petitioner,)
)
vs.)
)
LONGITUDE LICENSING LTD.,)
)
Patent Owner.)
_____)**

CERTIFIED COPY

**Patent No.
7,697,369 B2**

**DEPOSITION OF
BRUCE L. JACOB, PH.D.
REMOTELY HELD VIA VIDEOCONFERENCE TECHNOLOGY
JUNE 27, 2024**

**REPORTED BY:
LYNETTE MARIE NELSON,
CA CSR No. 11585, OR CSR No. 250121,
TN LCR No. 896, RPR, CRR, CCRR, CRG,
REALTIME SYSTEMS ADMIN.
JOB NO. 24-138548
Ref #: IPR2023-01200, CM#52414.16**

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Petitioner,)
vs.) Patent No.
LONGITUDE LICENSING LTD.,) 7,697,369 B2
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DEPOSITION OF BRUCE L. JACOB, PH.D.,
taken by the Petitioner, commencing at the hour of
10:00 a.m. on Thursday, June 27, 2024, held remotely via
videoconference, before Lynette Marie Nelson, Certified
Shorthand Reporter in and for the State of California,
Oregon, and Tennessee.

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APPEARANCES:

For the Petitioner:
HAYNES AND BOONE, LLP
BY: DAVID M. O'DELL, ESQ.
2801 N. Harwood Street, Suite 2300
Dallas, Texas 75201
(214)651-5000
david.odell@haynesboone.com

For the Patent Owner:
RUSS AUGUST & KABAT
BY: PAUL A. KROEGER, ESQ.
12424 Wilshire Boulevard, 12th Floor
Los Angeles, California 90025
pkroeger@raklaw.com

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I N D E X

WITNESS: BRUCE L. JACOB, PH.D.	PAGE
EXAMINATION	
BY MR. O'DELL	5

E X H I B I T S

NONE

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REMOTE DEPOSITION; THURSDAY, JUNE 27, 2024,
10:00 A.M. EASTERN STANDARD TIME

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BRUCE L. JACOB, Ph.D.,
HAVING BEEN DULY SWORN BY THE CERTIFIED SHORTHAND
REPORTER, WAS EXAMINED AND TESTIFIED AS FOLLOWS:

EXAMINATION

BY MR. O'DELL:

Q. Thank you for being here today, Dr. Jacob.

I'd like to start with some informalities that
we seem to go over every time but get them on record.

First of all, when you need a break, need to
hit the head, as you say, let me know and we'll break;
and I'll do the same, too, if I need to hit the head.

For the deposition, I plan to go over three
documents. And hopefully you got a note of those.

The first document is the -- your declaration,
the declaration of Dr. Jacob. It's Exhibit 2003.

A. Okay.

Q. The second document is U.S. Patent
No. 7,697,369. It's Exhibit 1001. And I will refer to
this as the '369 patent.

A. Cool, yes.

Q. And the third document is U.S. Publication

1 No. 2004/0022095A1, which is Exhibit 1005, and I will
2 refer to that as Lee, L-E-E.

3 A. Okay.

4 Q. Have you read and do you have each of these
5 documents?

6 A. I have read and I do have them in front of me
7 and I've got them electronically and I also have hard
8 copies in front of me.

9 Q. Great. Me, too, by the way. So I don't always
10 trust electronics.

11 So, as you know, you've done this before,
12 please do not communicate with others while we are on
13 record unless, of course, it's on record.

14 Please wait for me to finish my question before
15 you answer, and I'll try to give you the same courtesy.
16 I'll try my best to wait for you to complete your answer
17 before I move on.

18 A. Okay.

19 Q. Please answer -- please answer all questions
20 unless the -- your counsel instructs you not to answer.
21 So even if your counsel objects, you still answer unless
22 your counsel says do not answer.

23 A. Okay.

24 Q. As you know, please answer verbally. Please do
25 not do hand waving. Of course you want to not do that

1 so that the Zoom -- you don't get --

2 A. You don't want explosions?

3 Q. There we go.

4 A. I have no idea how to turn it off. I have no

5 idea.

6 Q. Well, I think it provides a little levity to an

7 otherwise boring conversation. So that's -- anyway.

8 I'm going to talk about a POSITA, P-O-S-I-T-A,

9 or person having ordinary skill in the art, at or around

10 the year 2006. And that is the earliest priority date

11 which is a Japanese filing of the '365 -- '369 patent.

12 Does that make sense?

13 A. It does.

14 Q. So we're not talking about a POSITA today.

15 We're not talking about a POSITA in 1995. But although

16 I understand you gave a little background, which is

17 helpful, but we're saying what would a POSITA say in

18 2006. Okay.

19 All right. Well, let's move on to the real

20 stuff.

21 So did you write the declaration by yourself?

22 A. Yes, I did. There's a section of legalese that

23 I didn't write --

24 Q. Yeah.

25 A. -- but all of the technical stuff I wrote.

1 Q. Starting with your qualifications at
2 paragraph 11 of your declaration, would you consider
3 yourself an expert in the memory system design area
4 around the year 2006?

5 A. Yes. Mm-hmm.

6 Q. Turning to paragraph 31 of your declaration,
7 this is a picture of -- I'm going to jump right in, by
8 the way.

9 A. Okay.

10 Q. Turning to paragraph 31 of your declaration.

11 A. All righty. I'm there.

12 Q. All right. This is a picture of a source
13 synchronous timing; right?

14 A. Yes, it is.

15 Q. Can you explain what's going on in the data
16 write operation and then the data read operation and
17 tell me more about source synchronous.

18 A. Sure.

19 This is just -- this is at a very high-level
20 depiction of source synchronous. It's leaving out a lot
21 of the details, but the idea is that you send a strobe
22 signal along with a data signal so that the receiving
23 side receives the -- the strobe and the data in
24 synchronous, you know -- they're in sync with each
25 other. They receive them at the same time. So -- as

1 opposed to using, for instance, a global clock to latch
2 the data in which you can't guarantee a certain amount
3 of alignment between the global clock and the -- and the
4 data because they're coming from different places.

5 So -- so in the data write operation, the
6 strobe is coming from the controller. The data is
7 coming from the controller so they both routed along the
8 circuit board with each other so that they -- the two
9 signals take a parallel track and take the same amount
10 of distance to go from the controller to the memory
11 device so they have the same, you know, latency there.
12 So they arrive in sync with each other.

13 And then the data read operation is just
14 reversed.

15 Q. So kind of, in short, whoever is providing data
16 also provides the strobe signal so that they arrive,
17 whatever the length of propagation is, at the same time?

18 A. Yes. Yes.

19 Q. Or close to.

20 A. Yeah. The idea is that when -- if you're
21 dealing with -- with frequencies, you know, tens of
22 megahertz, it's less of an issue, but as soon as you get
23 up into the hundreds of megahertz and certainly once you
24 get into the gigahertz ranges, even short amounts of
25 wire introduce skews that you need to account for and --

1 and this is the easiest way to account for it.

2 You send the two signals in parallel with each
3 other. And when one takes a right turn, the other takes
4 a right turn. They're routed together on the circuit
5 board so that they're always going to be in sync with
6 each other.

7 There are further mechanisms that you use to
8 bring them even tighter in sync with each other. But
9 this was -- this is a high-level depiction of the idea.

10 Q. Can a source synchronous system still use a
11 clock for things other than data?

12 A. To do what?

13 Q. To sample -- to sample -- can a source
14 synchronous system still use a clock to sample, for
15 example, control information?

16 A. Can -- so the question is, if you have a source
17 synchronous data delivery system, can that system use,
18 for instance, the system clock to sample commands and
19 addresses --

20 Q. Yes.

21 A. -- is that the question?

22 And the answer is yes, the system can do that.

23 Q. That's what the '369 patent does; right?

24 A. One of these guys does that. I believe it's
25 the '369. Let me make sure, I'll just look at this, the

1 timing diagrams.

2 Yes, yes, yes. Yes. Yes. That's how the '369
3 works.

4 Q. Did -- I'm going to not use his surname. I
5 don't know what the sex of the inventor is. Did
6 Koshizuka, K-O-S-H-I-Z-U-K-A, who is the inventor of the
7 '369 patent, invent and patent source synchronous timing
8 with his '369 patent?

9 A. I believe not. One of these guys actually
10 calls out where source synchronous clocking came from.

11 Okay. So, in fact, no, he says, for instance,
12 this is in the second paragraph of the first column
13 somewhere around line 12 or so, he says data signals are
14 sent out from the sender -- it says is synchronized,
15 that's bad grammar, but he's saying in synchronization
16 with the data strobe signal as disclosed in U.S. Patent
17 No. 6789209. So right there, he's describing -- he's
18 well aware of source synchronous clocking in prior art.

19 Q. What is the difference between your basic
20 description of source synchronous operations at
21 paragraph 31 of your declaration and the claimed
22 invention of the -- Claim 1 of the '369 patent?

23 If it helps, we can look at Claim 1 of the
24 '369 patent.

25 A. I'm going to pull up the electronic version

1 because it's bigger.

2 Q. Maybe I can ask this question more simply.

3 What improvement did Koshizuka provide to
4 source synchronous operation?

5 A. I'm not sure that -- that he's claiming to
6 improve upon source synchronous clocking. My
7 understanding from a high level was that the '369
8 patent, the main idea, is embodied in Figure 10 where
9 what he's got is two -- two different memories that
10 operate at very different speeds and they don't even
11 have to be like multiples of each other. These two
12 different memories that are -- that have different
13 bandwidths and different speeds and so forth can all
14 share the same control signals. And that's -- that's --
15 that would simplify the design of a system pretty
16 significantly rather than having a controller that has
17 to have a set of pins for each separate memory.

18 And this -- this could be -- you could envision
19 this extending to three different memories at three
20 different speeds. So I think I view it as that's the
21 main contribution from this patent.

22 I did not read the -- the claims in terms of,
23 hey, how -- to what degree did he improve upon source
24 synchronous clocking, but if you want, I can look
25 through the -- the claim for a bit and see if he does

1 claim to have improved upon source synchronous clocking.

2 Q. So -- and I will. But let me -- let me say
3 this differently.

4 When I look at Claim 1 of the '369 patent, I
5 don't see the two different speed memories as shown in
6 Figure 10. But what I do see that's different from your
7 drawings of source synchronous memory or memory systems
8 is that in a read operation, there's actually two strobe
9 signals: One from the controller to the memory device
10 and then another back from the memory device to the
11 controller along with the data.

12 A. Aah, I see what you're getting at. Okay. So
13 then now I see what you're getting at.

14 So the difference -- and it's just -- all
15 right. So if you look at my diagram for the data read
16 operation, we've got the strobe signal just something
17 called strobe signal that's coming out of a transmitter
18 circuit inside the memory device. It's got an amplifier
19 on the memory device side and it's sent across the
20 circuit board to the memory controller.

21 I don't show you where the strobe signal comes
22 from. And there are a lot of places a strobe signal
23 could come from. It could -- it could be generated
24 locally from an oscillator. It could be taken from, you
25 know, some other signal, you know, for instance, if the

1 memory were receiving a clock signal, it could gate the
2 clock signal onto the strobe line to produce a strobe.
3 Or -- and this is what the '369 patent does, it could do
4 a turnaround clock, a turnaround strobe, where it's --
5 it's receiving an incoming strobe signal from the
6 controller and it simply turns it right around and
7 transmits it right back to the controller.

8 And then at the same time that it's sending out
9 the pulses of the strobe, it's delivering each pulse of
10 the data and so -- so it's basically timing the delivery
11 of the data with the pulses of the strobe that are
12 coming in.

13 So -- so in a sense, you could look at that as
14 the memory controller is dictating to the memory device
15 the timing of the data.

16 Q. Okay.

17 A. And they call that turnaround clocks or
18 turnaround strobes a lot of times.

19 Q. And in the claim, if I'm not paraphrasing your
20 answer, your very complete answer correctly, please
21 correct me. But in the claim around line 19 of Claim 1
22 of the '369 patent, it refers to a second data strobe
23 signal being sent by the controller. And then to
24 receive a read data signal in synchronization with a
25 read data strobe signal, that's the difference between

1 what would be considered conventional source synchronous
2 operation?

3 A. Well, it's -- it's not necessarily -- yeah.
4 That's different from the way I depicted it in my -- in
5 my declaration.

6 Q. Okay.

7 Okay. I know you write about this in
8 paragraph 62. But tell me the difference between
9 synchronous and asynchronous memory systems.

10 You give a description of this, you have a
11 section heading directed to this. But in your words
12 here today, what's the difference between synchronous
13 and asynchronous memory systems?

14 A. So if you're applying the term to memory
15 systems as a whole, it's a little too broad.

16 Q. Okay.

17 A. But -- but if we limit it to DRAMs, for
18 example, I get to it in paragraph 61. And this is just
19 lifted straight out of my book that I wrote in 2005
20 regarding DRAM specifically, if the clock drives the
21 DRAMs directly, the DRAMs are called synchronous DRAMs.
22 If the clock does not drive the DRAMs directly, the
23 DRAMs are called asynchronous DRAMs.

24 In a synchronous DRAM, in "a" synchronous DRAM,
25 steps internal to the DRAM happen in time with one or

1 more edges of this clock.

2 In an asynchronous DRAM, operative steps
3 internal to the DRAM happen when the memory controller
4 commands the DRAM to act and those commands typically
5 happen in time with one or more edges of the system
6 clock. So . . .

7 Q. Okay. Okay. Thank you.

8 Let's turn to paragraph 36 of your declaration,
9 which describes the -- I'm about to say a bunch of
10 letters, okay? -- DDR SDRAM. And we often refer to that
11 last word as SDRAM. Okay?

12 All right. Let me start, and then one other
13 word that I'm going to say is JEDEC, all capitalized,
14 J-E-D-E-C. It's just -- it's just a word.

15 All right. So let me start over here.

16 A. I like that definition. "It's just a word."

17 Q. What do you call the word like "NASA," you
18 know, it stands for something.

19 A. Yeah, it's an acronym.

20 Q. Acronym. Thank you.

21 A. But I love it, "it's just a word." There's a
22 whole bunch of people involved in the organization. But
23 I love it.

24 You can question their efficiency and their
25 means and then their results, but I love that. "It's

1 just a word."

2 Q. I was part of JEDEC back in the '90s. I'm
3 insulting my own --

4 A. Yeah, yeah. Oh, I attended some of the
5 meetings and, oh my gosh, it's like -- it's basically
6 the whole organization as far as DRAM is concerned, it's
7 like Intel and everybody else is just -- they're not
8 even participants, they're audience members watching
9 what's going on because Intel is saying this is what's
10 going to happen.

11 Q. Yeah.

12 A. I imagine things have changed since, but it was
13 eye-opening. Anyway, sorry to --

14 Q. So I'm going to start over this question.
15 Hopefully it will make sense now.

16 Let's turn to paragraph 36 of your declaration
17 which describes the DDR SDRAM interface from 2003.

18 This appears to be consistent with the JEDEC
19 standard provided in the position at Exhibit 1007;
20 right?

21 A. I believe that I used the same document that
22 Baker referenced. I think I used the same version. I
23 tried to.

24 Q. Are the figures at the bottom of this
25 paragraph, I believe it's on page 19 of your

1 declaration, describing source synchronous timing?

2 A. Yes. For the data signal, they do.

3 Q. What is the relationship between DQS and CK or
4 clock?

5 A. I don't understand the question. What do you
6 mean, what is the relation?

7 Q. I see a vertical line that goes between the
8 transition of clock and the transition of DQS. In this
9 figure, from paragraph 36 of your declaration, is DQS
10 aligned with clock?

11 A. In the top figure, it happens to be. And
12 that's -- that is a read -- that's a read operation. In
13 the bottom figure, it is not aligned with the clock and
14 that's a write operation. So the strobe does not have
15 to be aligned with the clock.

16 Q. In the read operation part of the figure, is
17 DQS continuous?

18 A. No. Well, it depends on what you mean by
19 "continuous." You mean like a continuous periodic
20 noninterrupted clock signal? You know, something that
21 repeats forever?

22 Q. Yes.

23 A. Okay. Yeah, then no, it's not that. I mean,
24 you could say it's continuous over a defined interval or
25 something. It depends on your definition of continuous.

1 But no, it doesn't repeat forever. It just repeats for
2 a short bit.

3 Q. So in this top figure of the read operation at
4 paragraph 36 of your declaration, we would call the
5 clock signal continuous but the DQS signal would not be
6 continuous?

7 A. I would not call it continuous. But again, you
8 could say continuous over an interval or something. But
9 no, you'd say that the DQS signal is not continuous but
10 the clock is.

11 Q. Would it make more sense if I said that the
12 clock was free running?

13 A. You could say that. Yes.

14 Q. Okay. Okay.

15 If, in the read operation here in the top of
16 figure of paragraph 36 of your declaration, if DQS was
17 continuous for the entire -- just was free running,
18 would you say that it's essentially the same as clock,
19 CK?

20 A. It -- I would say it's essentially the same in
21 that it's free running. It would be performing a
22 different function. You know, it's one of those things
23 where you can't make a globally -- you can't make a
24 global statement say they're identical. If both of them
25 are free running, then certainly both of them are free

1 running similar in that regard.

2 Q. And they're aligned to each other?

3 A. In this example, if you chose to align DQS with
4 the clock, then they would be aligned with each other.

5 Q. Paragraph 46 of your declaration, this
6 paragraph is referring to an SRAM cache?

7 A. Yes, it's referring to the -- what's labeled
8 Figure 5.1 out of my book that's on page 23.

9 Q. Is the read/write signal in this -- referred to
10 in this paragraph a clock signal?

11 A. Usually read/write is not a clock signal
12 because it's usually, you know -- it's -- for example,
13 could be high if it's a write, low if it's a read, or
14 the other way around depending if it's active high or
15 active low. And I'm guessing since it's ends in a "B,"
16 it's a bar.

17 But no, that would not -- that would be a
18 control signal that determines whether or not you're
19 reading or writing.

20 Q. Okay. Referring to paragraph 62.

21 A. Okay. I'm there.

22 Q. Do synchronous memory devices facilitate higher
23 speed and performance microprocessors?

24 A. In general, not necessarily. I mean, they --
25 in general, the reason that people move to synchronous

1 devices is because they simplify system design. But
2 they don't necessarily give you any better bandwidth,
3 for instance, in the -- I think it was the 1980s, IBM
4 had asynchronous toggle mode that had just insane
5 bandwidth and it was asynchronous. So the main -- the
6 main reason for going to synchronous is that it
7 simplifies the interface between communicating devices.

8 Q. Have you ever heard of a pipeline memory?

9 A. I have.

10 Q. Can a pipeline memory -- let me give some more
11 background to this.

12 A pipeline memory is a synchronous memory; is
13 that your understanding?

14 A. Well, there is pipeline burst EDO, and I'm not
15 sure if that was -- I don't think that was synchronous,
16 was it?

17 I think pipeline burst EDO was -- I don't think
18 that was considered synchronous. A pipeline memory, you
19 don't necessarily have to have a system clock delivered
20 to the -- to the DRAM to make it pipeline. But in SRAM
21 designs, it may be different. I'm not -- I haven't
22 built pipelined SRAMs so I'm not sure about that. So it
23 kind of depends on what kind of device you're talking
24 about.

25 Q. So you said earlier that there was a move from

1 asynchronous to synchronous memories actually before the
2 time of this '369 patent, which provided the benefit of
3 more simple design. I'm not quoting you exactly if you
4 can correct me on that. Is that correct?

5 A. I'm sorry.

6 Q. So you said -- you said earlier that there was
7 a transition from asynchronous to synchronous memories
8 because it simplified the interface between the
9 controller and the memory device; is that correct?

10 A. Well, I gave that characterization of
11 synchronous versus asynchronous. Honestly, I don't know
12 exactly why the industry transitioned. If we're talking
13 about DRAMs. I don't know why the industry transitioned
14 from one to the other.

15 Presumably, it was -- it was cost-saving
16 reasons. And simpler design meant less -- less money
17 spent. I'm guessing. I think that's what the
18 transition was about. But I -- I didn't -- I don't
19 think I expressed the opinion on why the industry did
20 it. But I do know that synchronous designs tend to be
21 simpler than asynchronous designs because you are now
22 having things all happen on a clock. And so the -- the
23 movement of data and commands through the system looks
24 more like the movement of traffic through a city with
25 regular stoplights at the end of every block. And so

1 it's more regular, it's more predictable. And
2 therefore, it's easier to design.

3 You give up some amount of latency in doing it,
4 but you -- you know, in that you have longer latencies.
5 But the tradeoff is simplicity. So, you know, I think
6 that's -- that's the benefits, but again, I don't know
7 exactly why the industry transitioned from one to the
8 other.

9 Q. So can you tell me why having a simplified
10 interface or the simplicity that you were just
11 describing is a positive thing or is a benefit?

12 A. It means that nonexperts can design systems and
13 get them to work. So if you go back to the 1980s and
14 the early 1990s, there were people who could make really
15 fast DRAMs, but they were experts at it and they were
16 few and far between. And it was difficult -- from
17 what -- what they told me, it was difficult for them to
18 get other companies to go out and build parts that met
19 their specifications, like, there were a lot of
20 manufacturers who were capable of building DIMMs, but
21 they didn't know much about parasitics. So they could
22 build DIMMs that worked at, say, 50 megahertz or below,
23 but if you wanted to go to, like, 66 megahertz and
24 100 megahertz and so forth, these manufactures didn't
25 know how to do it. And this is why you kind of see

1 around that time, you know, early '90s and in particular
2 with the move to the synchronous DRAMs, they started
3 moving towards a JEDEC specification that was not nearly
4 a pin-out. Previously, the JEDEC specifications were
5 just pin-outs basically. Here's the DRAM, these pins
6 contain -- these pins are the ones that, you know, match
7 up with these signals. So like clock comes -- not
8 clock. They didn't have clocks.

9 CAS comes in here, RAS comes in here, address
10 pin zero is here, address pin one is here, data one,
11 data zero, and so forth. Power is here. Ground is
12 here. They basically said here is the pin-out of the
13 DRAM. And that was what a JEDEC specification looked
14 like.

15 But starting in the mid-1990s, they started to
16 include more specifications like what the parasitics
17 should look like, what the capacitance of these things
18 should look like, what's the -- you know, the impedance
19 measurements and so forth so that you could guarantee a
20 certain level of performance, and evidently there were a
21 bunch of manufacturers out there who was unaware of any
22 of these processes and so they had to be educated if
23 that makes sense.

24 And I think that moving to the synchronous
25 model made it easier to instruct these people on how to

1 build working parts that would work correctly at high
2 speeds. But this is -- this is my guess from, you know,
3 just putting together little bits and pieces that I saw.
4 Nobody's ever come out and said this is what it was all
5 about. This is my guess after watching what happened.

6 Q. Your guess is probably pretty good. I mean,
7 you wrote the textbook and you've got the -- the
8 background. You were an expert in the art at the time.

9 MR. O'DELL: So Lynette, he said the word "CAS"
10 and "RAS." That's more acronyms, C-A-S and R-A-S.

11 THE STENOGRAPHER: Thank you.

12 THE WITNESS: Thank you for that clarification.

13 MR. O'DELL: I'm going to say something funny,
14 this is kind of off the record.

15 (Discussion held off record.)

16 MR. O'DELL: All right. I would like to take a
17 little break. Maybe we can all hit the head, I'm going
18 to refresh some of my notes and I think we've answered a
19 lot of my questions already.

20 I do have more questions to go, but I'd like to
21 kind of reorganize and reidentify that. So why don't we
22 take a little ten-minute break. Is that okay?

23 MR. KROEGER: Sure.

24 (A recess was taken.)

25

1 BY MR. O'DELL:

2 Q. All right. I'm going to refer to the Lee prior
3 reference.

4 A. Okay.

5 Q. Paragraph 4 and 5 of Lee talks about a mobile
6 processing systems and clock signals. Are you familiar
7 with that -- those two paragraphs or would you like to
8 read them again to refresh your memory?

9 A. Well, I'll read them briefly. I'm familiar
10 with them. But . . .

11 Q. Okay.

12 A. Yeah, he's just explaining why having low power
13 is good.

14 Q. Okay.

15 A. And why clocks are bad.

16 Q. Would you agree that for mobile applications,
17 some may find it desirable to use asynchronous memory
18 devices?

19 A. Certainly. I think that's -- that's a good
20 statement.

21 Q. Do you think that in other applications, it may
22 be desirable to use synchronous memory devices?

23 A. Depending upon the application, you would
24 choose to use one or the other. And it all depends on
25 the application. He's just talking about what he wants

1 to accomplish.

2 Q. Mm-hmm.

3 Do you know if mobile devices in 2006, which is
4 the priority date of the '369 patent, were using
5 synchronous memory devices?

6 A. I would imagine it depends upon the mobile
7 device. And I -- and I -- I don't know offhand -- I
8 don't know if you can say generally across the board
9 everybody is doing one or the other. I'm certainly
10 not -- everyone was not doing either one or the other.
11 It was something where there would be a mix, I believe,
12 by mid-2000s.

13 Q. Why would some entities use a synchronous
14 device when a synchronous device consumes more power?

15 A. I don't know. You would have to give me a
16 specific instance, you know. It could be cost reasons,
17 because, you know, by then SDRAM was more common. And
18 also, it depends upon the instance that we're talking
19 about.

20 A designer makes choices based on lots of
21 things, you know. They've got to not exceed certain --
22 certain quantities and they can't go over certain dollar
23 amount, they can't exceed a certain power amount and so
24 forth. And they -- they make their decisions based on
25 all of that.

1 Q. Keeping Lee open -- I don't know if you can do
2 this, keeping Lee open, look at paragraph 102 of your
3 declaration.

4 A. Paragraph 102 of my declaration.

5 Right. So 102 says Lee specifically says that
6 the memory devices when they receive the nonstop system
7 clock generate current and therefore dissipate power,
8 quote, irrespective of whether an operation is being
9 performed by the synchronous memory, end quote, and that
10 the power levels achieved in the standby state which
11 should be near to zero because the chip is functionally
12 idle at that point instead, quote, may be substantially
13 the same as that in a non-standby state, end quote.

14 And then I quote Lee paragraph 5.

15 Q. Do you agree with that discussion of Lee?

16 A. Well, I -- I'm not sure what you're asking.

17 Q. Does his analysis -- do you agree with his
18 analysis of synchronous and asynchronous memory?

19 A. Well, certainly if you've got a clock running,
20 it dissipates a whole lot of power. The rule of thumb
21 in -- for instance, in microprocessor designs is that
22 the clock tree and all of the latches that it drives
23 generally counts for 33 percent of the power, roughly
24 one-third of the power. So if you have a clock that's
25 running, it's -- it's a good estimate that that's

1 accounting for a third of your power.

2 Q. Let's look at Figure 2 of Lee.

3 Okay?

4 A. All right. The timing diagram?

5 Q. Yes.

6 A. Okay. I'm there.

7 Q. In your opinion, would a person of ordinary
8 skill in the art in 2006 consider Lee's SCA strobe
9 signal a clock?

10 A. It -- it depends upon your definition of clock,
11 you know. People often say let's clock in the data,
12 let's clock in this. It's something where you'd have to
13 figure it out from context what they mean. Sometimes
14 when you use a strobe to -- you know, to clock in
15 something, people will call it a clock. And actually, I
16 think I've got a little discussion of that in my -- in
17 my "Background" section where I say, you know, there's
18 some -- when you know it's one thing, you call it a
19 strobe; when you know it's the other, you call it a
20 clock. And sometimes you can use clock to mean both a
21 strobe and a clock.

22 So it's -- it's -- this is -- engineers love to
23 use terms however they -- however they use them. And
24 they frequently give you something that you gotta figure
25 out from context. So I can envision scenarios where

1 people would call that a clock. But it's clear that
2 it's not a free-running uninterrupted signal.

3 Q. So some people may say that this SCA strobe
4 signal on Figure 2 of Lee is a clock but not a
5 free-running clock?

6 A. Right. They might call it a clock just like I
7 said, you know, engineers frequently call strobes
8 clocks. But if we go by the patent's definition and so
9 forth -- not definition, but the patent's usage of the
10 term and -- and Lee's discussion, it's clearly not a
11 free-running clock signal.

12 Q. So would you say that the SCA strobe signal of
13 Figure 2 of Lee is not a clock as recited in Claim --
14 let's say Claim 2 of the '369 patent?

15 A. Right. I would -- I would not think that that
16 would satisfy Claim 2.

17 Q. Why is that?

18 A. Because when you -- when you read the
19 '369 patent, he's -- he's making a pretty clear
20 distinction between strobes and a free-running clock and
21 he shows a free-running clock that's used for sampling
22 the commands and addresses. So -- so it's clear when he
23 says clock, he means a free-running clock.

24 Q. We talked about this briefly in other context,
25 but let's turn to paragraph 69 of your declaration.

1 A. Okay. I'm there.

2 Q. You say that a synchronous DRAM memory device
3 that transfers data and control with a clock signal is
4 more predictable and has less skew.

5 Can you explain what that means?

6 A. Where did I -- are you reading that from my --

7 Q. I summarized it.

8 A. You paraphrased that. Okay. I see what you're
9 saying.

10 But I said that by associating all data and
11 control transfer with a clock signal, the timing events
12 is made more predictable. Such a scheme, by definition,
13 has less skew.

14 So when you make things happen with the clock,
15 then the receiving device knows that everything is
16 either going to happen on the beat of the clock or it's
17 not going to happen.

18 So whereas asynchronous devices, things happen
19 whenever the controller says they're going to happen.
20 Meaning like I send a signal to you, it's like
21 literally, I'm pulling the strings of a marionette. I'm
22 in an asynchronous device, I'm controlling the internal
23 structures of the device and so things happen when I,
24 the controller, say so. And so the device has to be
25 designed to be able to tolerate that. And it's hard to

1 test -- it's hard to predict, it's hard to know exactly
2 what's going to happen and when.

3 Whereas if everything happens on the beat of
4 the clock, then the only time that you need to be
5 looking for things is on the beat of the clock. So by
6 definition, that's more predictable.

7 And skew means -- but it's -- literally means
8 the predictability of timing. So that's why I said such
9 a scheme, by definition, has less skew, because you've
10 made everything predictable, therefore you've reduced
11 the amount of skew in the system.

12 MR. O'DELL: I'm going to take about a
13 two-minute review. I don't think we need to go off
14 record because I don't believe I have any more
15 questions, but I want to confirm that. I want to review
16 my notes to make sure I didn't miss something. But I
17 don't think we need to break unless someone wants a
18 break.

19 MR. KROEGER: Okay.

20 MR. O'DELL: I am through with my questioning
21 on cross. I leave this open for redirect if so desired.

22 MR. KROEGER: I don't have any questions. So I
23 think we're good.

24 MR. O'DELL: Okay.

25 (Deposition was concluded at 11:02 a.m.)

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Note: If you are adding to your testimony, print the exact words you want to add. If you are deleting from your testimony, print the exact words you want to delete. Specify with "Add" or "Delete" and sign this form.

DEPOSITION OF: BRUCE L. JACOB, Ph.D.

CASE: WESTERN DIGITAL TECHNOLOGIES V LONGITUDE LICENSING

DATE OF DEPOSITION: JUNE 27, 2024

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Declaration Under Penalty of Perjury

I, **BRUCE L. JACOB, Ph.D.**, the witness herein,
declare under penalty of perjury that I have read the
foregoing in its entirety; and that the testimony
contained therein, as corrected by me, is a true and
accurate transcription of my testimony elicited at said
time and place.

Executed this _____ day of _____ 20____, at
_____, _____.
(city) (state)

BRUCE L. JACOB, Ph.D.

1 **REPORTER'S CERTIFICATE**

2 **-000-**

3 I, LYNETTE M. NELSON, CA CSR No. 11585, OR CSR
4 No. 250121, TN LCR No. 896, RPR, CRR, CCRR, CRG, duly
5 licensed and qualified in and for the State of
6 California, Oregon, and Tennessee, do hereby certify
7 that there came before me on the 27TH day of JUNE, 2024,
8 via web videoconference, the following named person,
9 to-wit BRUCE L. JACOB, Ph.D., who was duly sworn to
10 testify the truth, the whole truth, and nothing but the
11 truth of knowledge touching and concerning the matters
12 in controversy in this case; and that he was thereupon
13 examined under oath and his examination reduced to
14 typewriting under my supervision; that the deposition is
15 a true record of the testimony given by the witness.

16 I further certify that pursuant to FRCP Rule
17 30(e)(1) that the signature of the deponent:

18 () Was requested by the deponent or a party
19 before the completion of the deposition;

20 (X) was not requested by the deponent of a
21 party before the completion of the deposition.

22 I further certify that I am neither attorney or
23 counsel for, nor related to or employed by any of the
24 parties to the action in which this deposition is taken,
25 and further that I am not a relative, employee of any

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attorney or counsel employed by the parties hereto, or
financially interested in the action.

CERTIFIED TO BY ME on this 10TH day of JULY, 2024.



LYNETTE M. NELSON,
CA CSR No. 11585, OR CSR No. 250121,
TN LCR No. 896, RPR, CRR, CCRR, CRG,
REALTIME SYSTEMS ADMIN.

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