

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

LONGITUDE LICENSING LTD.,
Patent Owner.

Case IPR2023-01200
U.S. Patent No. 7,697,369 B2

PATENT OWNER'S SUR-REPLY

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I. Introduction

The Petition relies on the modification of the Lee reference to use a synchronous memory in combination with the JEDEC standard, but Petitioner's Reply cannot escape Lee's clear teaching that "*the need for a continuous clock*" [as used in synchronous memory] should be *avoid[ed]*" to reduce "the current consumed by the memory 120 when not performing a read or write operation ... over a similar memory that utilizes a continuous clock." Ex. 1005, Lee ¶ [0028] (emphasis added). This teaching reflects Lee's fundamental purpose and inventive concept: using asynchronous memory with source synchronous transfer to improve power consumption over conventionally known synchronous memory such as the JEDEC standard. As explained in the POR, this teaching is fatal to Petitioner's Ground 2 which seeks to combine Lee with the JEDEC standard to use a synchronous and continuous clock with Lee in direct contravention of its inventive concept and fundamental purpose.

Faced with such an inherent contradiction, Petitioner's Reply resorts to mischaracterizing and misrepresenting Lee to claim that a POSITA would do what Lee expressly forbids – use synchronous memory. First, Petitioner erroneously contends that Lee's inventive concept involves only a "turnaround strobe" in a "source synchronous process" based on one cherry-picked paragraph of Lee. In fact, Lee's inventive concept involves the use of "asynchronous memory," something

made clear by multiple paragraphs of Lee, every embodiment of its invention, and indeed, by its title: “Asynchronous Memory Using Source Synchronous Transfer And System Employing Same.” Ex. 1005, Lee at 1 (emphasis added).

Petitioner next resorts to claiming a POSITA would nonetheless have combined the references in spite of Lee’s teaching largely because synchronous memory, such as that defined by JEDEC, was known in the art. In other words, Petitioner shows only that a POSITA *could* have combined the references, not that he or she *would* have done so as legally required. Moreover, Petitioner ignores that its only expressed modification of Lee – using the SCA signal as a clock signal – runs directly counter to Lee’s teaching and is based on impermissible hindsight.

Finally, Petitioner’s arguments that its combination would not frustrate Lee’s intended purpose are based on a misreading of Lee. Petitioner’s contention that Lee is not limited to “asynchronous memory” and would work just as well with synchronous memory is simply fabricated attorney argument. Every embodiment of Lee uses asynchronous memory in accordance with its fundamental purpose of achieving a low power mode. Further, a POSITA would understand that all of Lee’s claims are limited to “asynchronous memory” as expressly defined in the specification. The use of synchronous memory is simply inconsistent with Lee’s teaching. Lee teaches away from using synchronous memory as Petitioner contends.

Accordingly, as explained below and in the POR, the Petition does not present a proper motivation to combine Lee and JEDEC. Consequently, its Ground 2 fails. For this reason, the Petition fails to show that claims 2, 7, and 11 of the '369 Patent are unpatentable.

II. The Manner In Which A Clock Is Used By The Memory Is Key To The Inventions Of Both The '369 Patent and Lee

Petitioner's reply first characterizes the inventive concept of both Lee and the '369 Patent as concerning solely use of a "turnaround strobe" in connection with "source-synchronous operation" divorced from how a clock is used with the memory. Reply at 7-10. However, as explained in the POR and in Dr. Jacob's declaration, "source synchronous transfer" simply means that a data-strobe signal is transmitted along with the data signal. POR at 3; Ex. 2003, Jacob Decl., ¶ 88. Lee makes clear that the term "source synchronous interface" refers to the interface that provides "data transmission between the memory 120 and the memory controller 140" and was known in the art. Ex. 1005, Lee ¶ [0017]; Ex. 1005, Lee ¶ [0018] ("A Source synchronous interface is an interface where data is sent from a transmitter to a receiver together with a clock signal, which is used within a receive interface to latch the accompanying data."). Accordingly, "source synchronous transfer," by itself is not the inventive concept of Lee.

Instead, Lee’s inventive concept involves using asynchronous memory with source synchronous transfer. “Asynchronous memory,” as taught by Lee and understood in the art, is one that does not receive a continuous system clock, unlike a synchronous memory which does receive a system clock. Ex. 2003, Jacob Decl., ¶¶ 85. *See also id.* at ¶ 62, 75-84. Lee’s inventive concept involves using asynchronous memory with a source synchronous interface as a way to conserve power in a manner not previously known in the art. Ex. 1005, Lee ¶¶ [0003], [0005], [0028], [0034]. As Dr. Jacob opines – and Petitioner does not dispute – the decision to use asynchronous memory with a source synchronous interface “represents a complete transformation of the interface.” Ex. 2003, Jacob Decl., ¶ 85.

Petitioner discounts Lee’s teaching of asynchronous memory by cherry-picking a single paragraph of Lee (Lee ¶ [0021]) and noting that “none of the discussion” in this one paragraph “describes or refers to synchronous or asynchronous memory, neither does it describe a clock or the absence thereof.” Reply at 10. Petitioner can only make this statement by avoiding the substantial teaching of Lee that use of asynchronous memory is beneficial because it allows for a lower power mode of operation. Ex. 1005, Lee ¶ [0005] (in “*conventional memory, such as a synchronous memory* the clock signal is, typically, internally produced irrespective of whether an operation is being performed by the synchronous memory”) (emphasis added); *Id.* ¶ [0028] (“The memory 120 operates

in an asynchronous fashion *Thus, the need for a continuous clock may be avoided and the current consumed by the memory 120 when not performing a read or write operation may be reduced over a similar memory that utilizes a continuous clock.*”) (emphasis added); *Id.* ¶ [0034] (“according to embodiments of the present invention, as illustrated for example in FIG. 3, the strobe signals ... *are not used as a reference signal (e.g., a clock signal)* for a memory operation”) (emphasis added).

Curiously, Petitioner also attempts to discount the use of a synchronous clock in the ‘369 Patent by focusing on claim 1. Reply at 8-9. However, Petitioner’s Ground 2, the only ground at issue, is directed to claims 2, 7, and 11, each of which require the use of a synchronous clock:

The system according to claim [1, 6, 10] wherein the controller is further adapted to produce a clock signal and to send the clock signal to the memory, each of the first and second data strobe signals and the read data strobe signal being independent of and separated from the clock signal.

Ex. 1001, ‘369 Patent at 21-22. Furthermore, the use of synchronous memory is specifically taught by the ‘369 Patent. *Id.* at 4:55-5:5 (“the memory 200 ... has ... “an internal clock generating section 230 The internal clock generating section 230 generates an internal clock signal upon receiving the clock signal and sends out the internal clock signals to circuits for command/address and so on. As shown in

Fig. 3, the input/output operation of the memory 200 is carried out based on the data strobe signal received from the controller 100 and is completely separated from the clock signal.”).

For the reasons explained in the POR and below, Lee’s requirement of asynchronous memory is fatal to Petitioner’s ground 2, as Petitioner’s proposed combination with the JEDEC standard requires the use of synchronous memory in a manner directly contrary to Lee’s intended purpose and manner of operation.

III. Petitioner Fails To Provide Any Reason That One Of Skill In The Art *Would Have Combined Lee and JEDEC As Proposed*

Petitioner’s reply posits myriad examples as to why a POSITA might have combined Lee and the JEDEC standard: (1) “increased bandwidth;” (2) “reduced costs to fabricate;” (3) “industry standard;” (4) purported benefits of synchronous memories; and (5) “reduced costs and simplicity of design.” Reply at 11-17. None of these reasons show that a POSITA *would* have combined LEE and JEDEC. At most they show that a POSITA could have combined the references, merely because they were known in the art, which is insufficient as matter of law. *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993–94 (Fed. Cir. 2017) (“reasoning [that] seems to say no more than that a skilled artisan, once presented with the two references, would have understood that they could be combined ... is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at

the claimed invention”); *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.”); *Virtek Vision Int'l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882, 887 (Fed. Cir. 2024) (“It does not suffice to simply be known. A reason for combining must exist.”).

In terms of the purported benefits of using synchronous memories, such as increased bandwidth, Petitioner once again fails to provide a reason that a POSITA would have chosen these benefits over the low-power benefits of asynchronous memory described by Lee. This is especially true as Lee teaches its benefits are preferable over conventional, synchronous, memories. Ex. 1005, Lee ¶ [0005] (in “*conventional memory, such as a synchronous memory* the clock signal is, typically, internally produced irrespective of whether an operation is being performed by the synchronous memory”) (emphasis added); *Id.* ¶ [0028] (“The memory 120 operates in an asynchronous fashion *Thus, the need for a continuous clock may be avoided and the current consumed by the memory 120 when not performing a read or write operation may be reduced over a similar memory that utilizes a continuous clock.*”) (emphasis added); *Id.* ¶ [0034] (“according to embodiments of the present invention, as illustrated for example in

FIG. 3, the strobe signals ... *are not used as a reference signal (e.g., a clock signal)* for a memory operation”) (emphasis added).

Petitioner refers to the use of synchronous or asynchronous memories as “design tradeoffs” but comes forward with no evidence to rebut Dr. Jacob’s opinion that using synchronous memory “represents a complete transformation of the interface.” Ex. 2003, Jacob Decl., ¶ 85. Moreover, Petitioner ignores that the specific combination of Lee and JEDEC it contends a POSITA would have used is, in fact, taught away by Lee. Specifically, the Petition contends that “[a] POSITA would have found it obvious to substitute Lee’s SCA signal using a clock signal,” Ex 1003, Baker Decl., ¶¶114-118. Lee, however, notes that *“the strobe signals SCA and SDtM are not used as a reference signal (e.g., a clock signal)* for a memory operation.” Ex. 1005, Lee ¶ [0034]. Petitioner cannot explain why a POSITA would have ignored this clear teaching that is 180 degrees contrary to Petitioner’s proposed combination.

Indeed, Petitioner’s only justification for using the SCA in Lee as a clock signal is because “[t]he SCA signal in the combination of Lee and JEDEC serves the same function as the clock signal described in the ’369 Patent.” Petition at 66. In other words, **the Petition uses the teaching of the patent as a roadmap** to justify its obviousness arguments – a prima facie example of hindsight reasoning. *Otsuka Pharm. Co. v. Sandoz, Inc.*, 678 F.3d 1280, 1296 (Fed. Cir. 2012) (“[t]he inventor’s

own path itself never leads to a conclusion of obviousness; that is hindsight. What matters is the path that the person of ordinary skill in the art would have followed, as evidenced by the pertinent prior art.”); *Life Techs., Inc. v. Clontech Labs., Inc.*, 224 F.3d 1320, 1325 (Fed. Cir. 2000) (“[T]he path that leads an inventor to the invention is expressly made irrelevant to patentability by statute.”); *Heidelberger Druckmaschinen AG v. Hantscho Com. Prod., Inc.*, 21 F.3d 1068, 1072 (Fed. Cir. 1994) (“The motivation to combine references cannot come from the invention itself.”).

Finally, with regard to Petitioner’s claims of cost benefits, neither party’s expert offered the opinion that asynchronous memory was more expensive than synchronous memory. *See* Ex. 2004, Baker Depo. Tr. at 22:7-25:19 (declining to offer opinion as to whether asynchronous RAM was more or less expensive as of the priority date); Reply at 16-17 citing Jacob Depo Tr. at 22:10-23:8 (stating he had “no opinion” as to why the industry transitioned from synchronous to asynchronous memory). Thus, Petitioner simply has no evidence of any cost savings from using synchronous memory as taught by the purported combination of JEDEC with Lee.

Accordingly, the Petition is devoid of any reason as to why a POSITA would have combined Lee and JEDEC to arrive at the claimed invention. For this reason alone, Ground 2 fails.

IV. Lee Teaches Away From Synchronous Memory And Using Synchronous Memory Would Render Lee Inoperable For Its Intended Purpose

The remainder of Petitioner's Reply hand waves over Lee's clear teaching that its invention should only be used with asynchronous memory to avoid the use of a continuous clock and achieve low power benefits. Reply at 20-29. In sum, Petitioner argues that Lee's use of asynchronous memory is only an exemplary embodiment that would work equally well with synchronous memory. *Id.* This argument fails to survive even a cursory reading of Lee.

First, Lee's teaching is clear that the invention requires the use of asynchronous memory. The only memory taught by Lee, memory 120, is asynchronous. Ex. 1005, Lee at ¶ [0017] (“[t]he memory 120 is an asynchronous memory”). Furthermore, asynchronous memory is used in every one of Lee's embodiments. *Id.* at ¶ [0036] (“the memory 120' and the memory controller 140' in FIG. 4 are substantially identical to those of memory 120 and memory controller 140 discussed in FIG. 3”); *Id.* at ¶ [0036] (“the memory 120” and the memory controller 140” in FIG. 5 are substantially identical to those of memory 120 and memory controller 140 discussed in Fig. 3”). And, indeed, Lee's title confirms this is the case: “***asynchronous memory*** using source synchronous transfer.” *Id.* at 1.

Nowhere does Lee discuss the use synchronous memory, except to distinguish its invention over “conventional memory.” Ex1005, Lee ¶ [005]. Moreover, Lee has

no suggestion that similar benefits of low power can be obtained using such synchronous memory. Indeed, Lee specifically refers to synchronous memory as the “conventional memory” that it is seeking to improve:

The standby current generated in a *conventional memory, such as a Synchronous memory*, having a clock tree structure may be substantially the same as that in a non-standby state. This may be the case because the clock signal is used as a transmission reference signal for synchronous memory operations and, therefore, the clock signal is, typically, internally produced irrespective of whether an operation is being performed by the synchronous memory.

Ex1005, Lee ¶ [005]. Accordingly, Petitioner’s contention that Lee’s “inventive concept ... can be used with asynchronous memory and can also be used with synchronous memory” lacks merit. Petition at 23.

Petitioner latches onto the fact that one of Lee’s independent claims (claim 5) does not use the word “asynchronous.” Petition at 23, 27-28. However, the claims do claim the “memory” and “memory controller” described in Figs. 3-5. Thus, a POSITA would clearly understand that the memory is limited to “asynchronous memory” based on the specification’s clear teaching. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005) (“the specification “is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.”) (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)).

Petitioner invokes claim differentiation in an attempt to broaden claim 5 and its dependents (as the other independent claims refer to “asynchronous memory”) to cover synchronous memory. However, that doctrine “cannot be relied upon to ‘broaden claims beyond their correct scope.’” *Wenger Mfg., Inc. v. Coating Mach. Sys., Inc.*, 239 F.3d 1225, 1233 (Fed. Cir. 2001) (quoting *Kraft Foods, Inc. v. Int'l Trading Co.*, 203 F.3d 1362, 1368 (Fed.Cir.2000)); *InterDigital Commc'ns, LLC v. Int'l Trade Comm'n*, 690 F.3d 1318, 1331 (Fed. Cir. 2012) (“the doctrine of claim differentiation does not permit enlarging a claim term beyond its presentation in the specification”) (Newman, J. dissenting). Again, Lee provides no written description, enablement, or other analysis of using anything but asynchronous memory, and a POSITA would recognize that its claims are so limited.

Equally frivolous is Petitioner’s claim that Lee “recites an embodiment using synchronous memory” because it “incorporates by reference U.S. Patent No. 6,336,159.” Reply at 26. In fact, Lee only incorporates U.S. Patent No. 6,336,159 for its discussion of “source synchronous interfaces.” Ex. 1005, Lee ¶ [0018] (“Source synchronous interfaces are disclosed in U.S. Patent 6,336,159 ... the disclosures of which are incorporated herein by reference.”). This incorporation is merely an example of the conventional memory structure Lee sought to improve, not an assertion that “Lee’s inventive concept works with synchronous memory” as Petitioner maintains. Reply at 24.

In sum, Lee sought to improve conventionally-known source synchronous data transfer systems, such as the JEDEC standard, by using asynchronous memory to achieve low-power benefits and avoid the need of a continuous clock. Lee's intended purpose would be frustrated by using synchronous memory, and Lee taught away from using such. For this reason, a POSITA would not have been motivated to combine Lee with the JEDEC standard and the Petition does not demonstrate a reasonable likelihood of prevailing with respect to Ground 2.

V. Conclusion

Because the Petition fails to provide evidence that a POSITA would have been motivated to combine Lee and JEDEC its Ground 2 fails. Accordingly, the Petition fails to show that claims 2, 7, and 11 of the '369 Patent are unpatentable.

Date: August 29, 2024

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CERTIFICATION REGARDING WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner certifies that there are 2,975 words in the paper excluding the portions exempted under 37 C.F.R. §42.24(a)(1).

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CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e)(1))

The undersigned hereby certifies that the above document was served on August 29, 2024, by filing this document through the Patent Trial and Appeal Case Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

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