

Inter Partes Review U.S. Patent No. 7,697,369

Western Digital Technologies, Inc. v. Longitude Licensing LTD, IPR2023-01200

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IPR2023-01200

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Claim 1 of '369 Patent

The inventive concept of the '369 Patent is to modify the conventional source-synchronous operation by adding an additional strobe signal used to transfer data during read operations, what PO's expert refers to as a "turnaround strobe"

Pet. Reply, 5-8; see *also*, Pet., 14
(discussing prosecution history)

1. A system comprising:
a controller adapted to send out a first data strobe signal and a write data signal in a write operation, the write data signal being synchronized with the first data strobe signal, the controller being adapted, in a read operation, to send out a second data strobe signal and to receive a read data signal in synchronization with a read data strobe signal, the read data strobe signal being received by the controller in response to the second data strobe signal; and
a memory adapted to receive the write data signal in synchronization with the first data strobe signal in the write operation, the memory being adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal and to send the read data signal synchronized with the read data strobe signal.

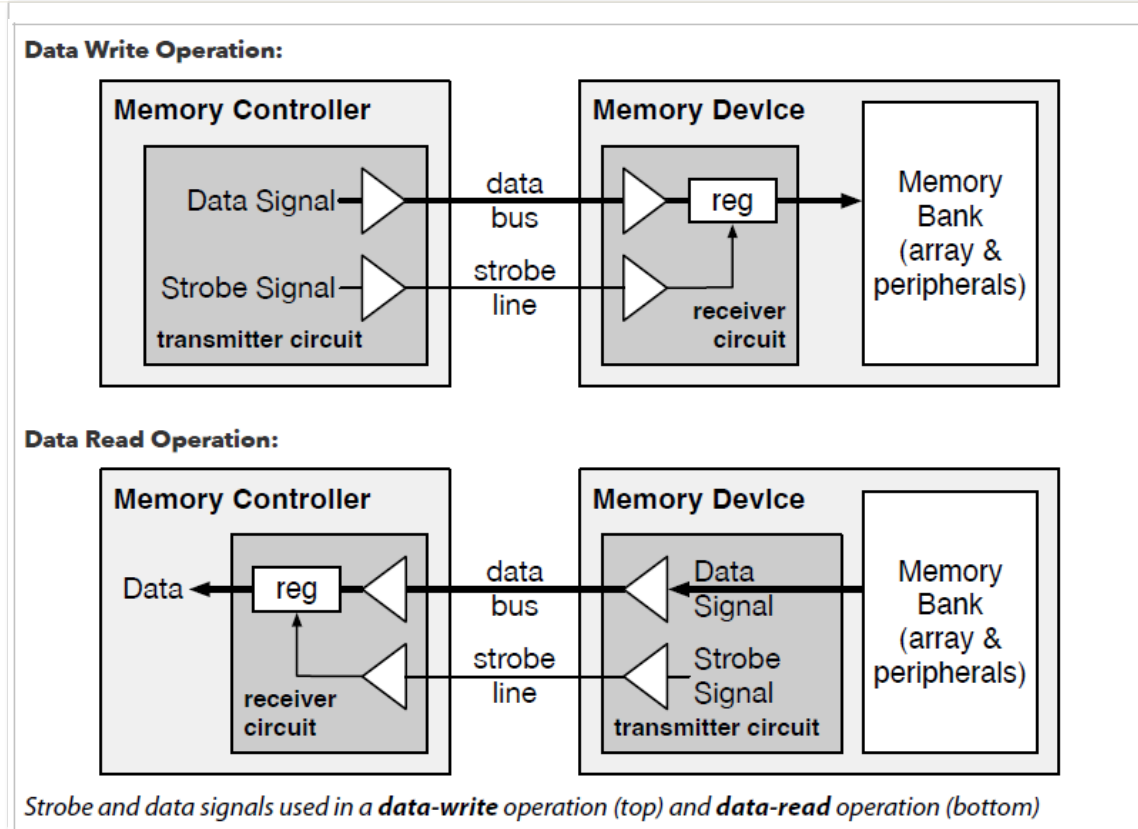
Source synchronous
write operation

Source synchronous
read operation

Turnaround strobe

EX1001, claim 1

“Source-Synchronous” – strobe and data are synchronized

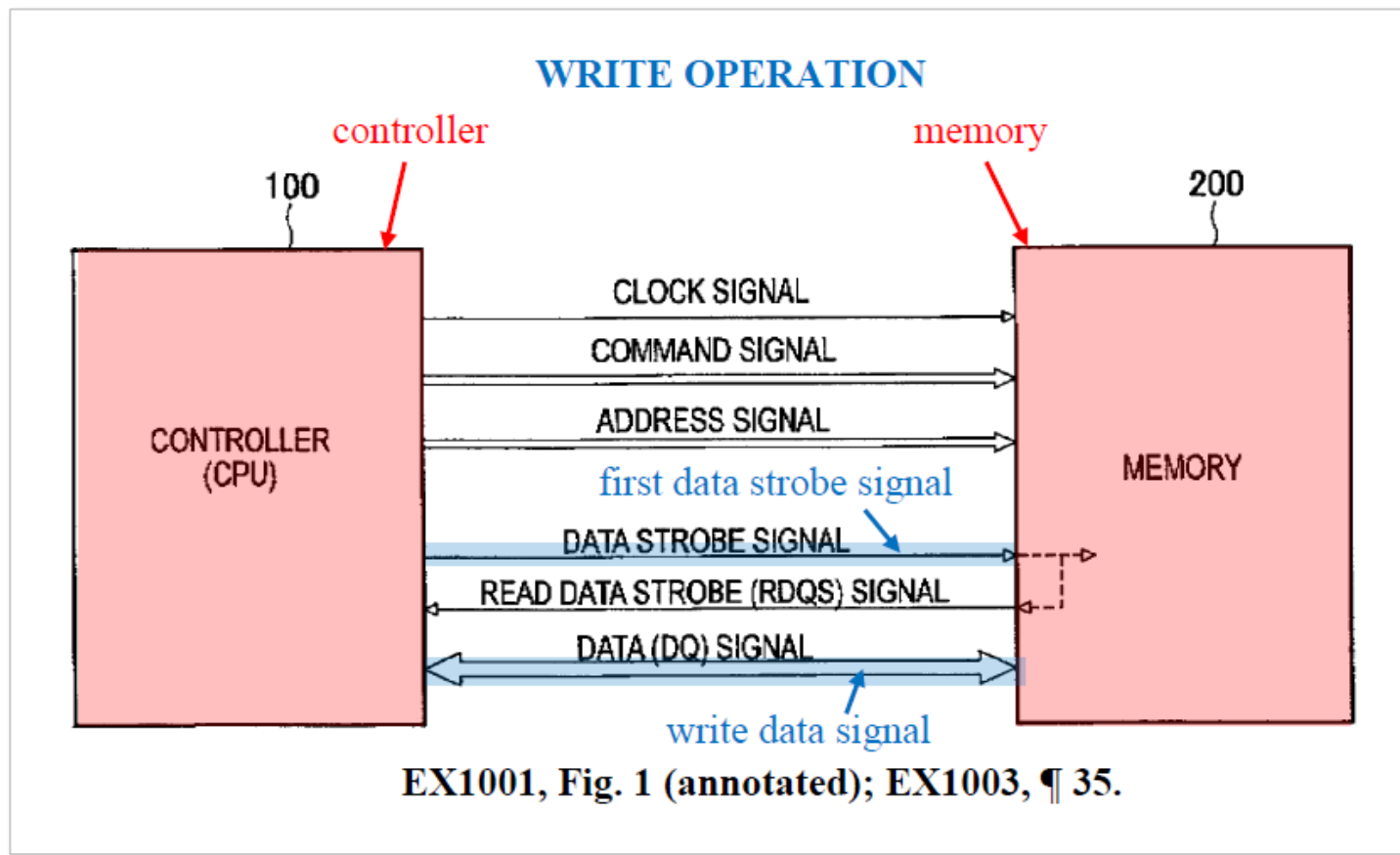


(32) The figures above illustrate a *source-synchronous* timing arrangement: the strobe and data are transmitted from the same source along with each other, which will ensure that they remain synchronized with one another, an arrangement that makes it easier to capture the data correctly at the receiving end. The top example

Ex. 2003, Jacob Decl., 16-17

The '369 Patent

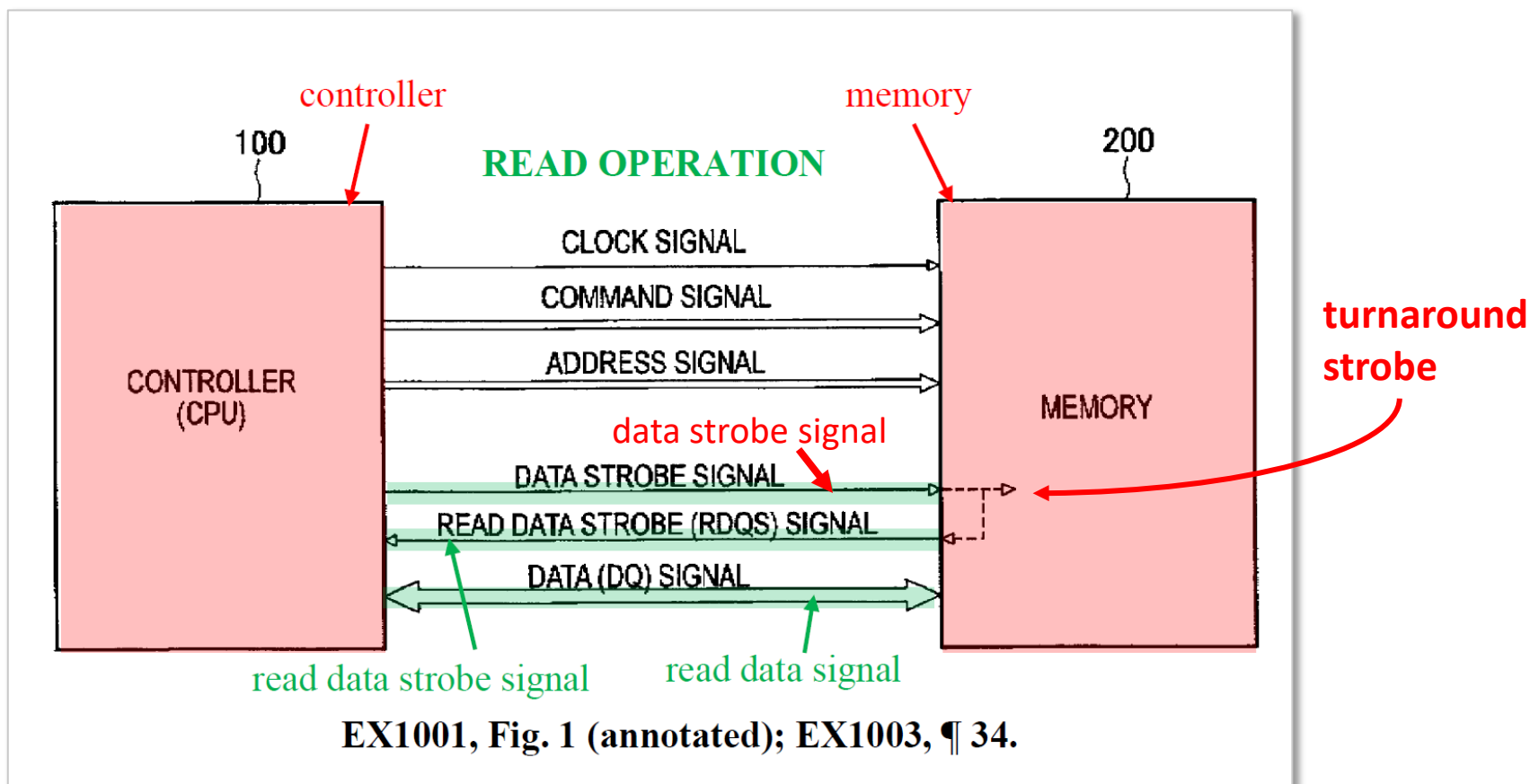
A source synchronous write operation



Pet., 13

The '369 Patent

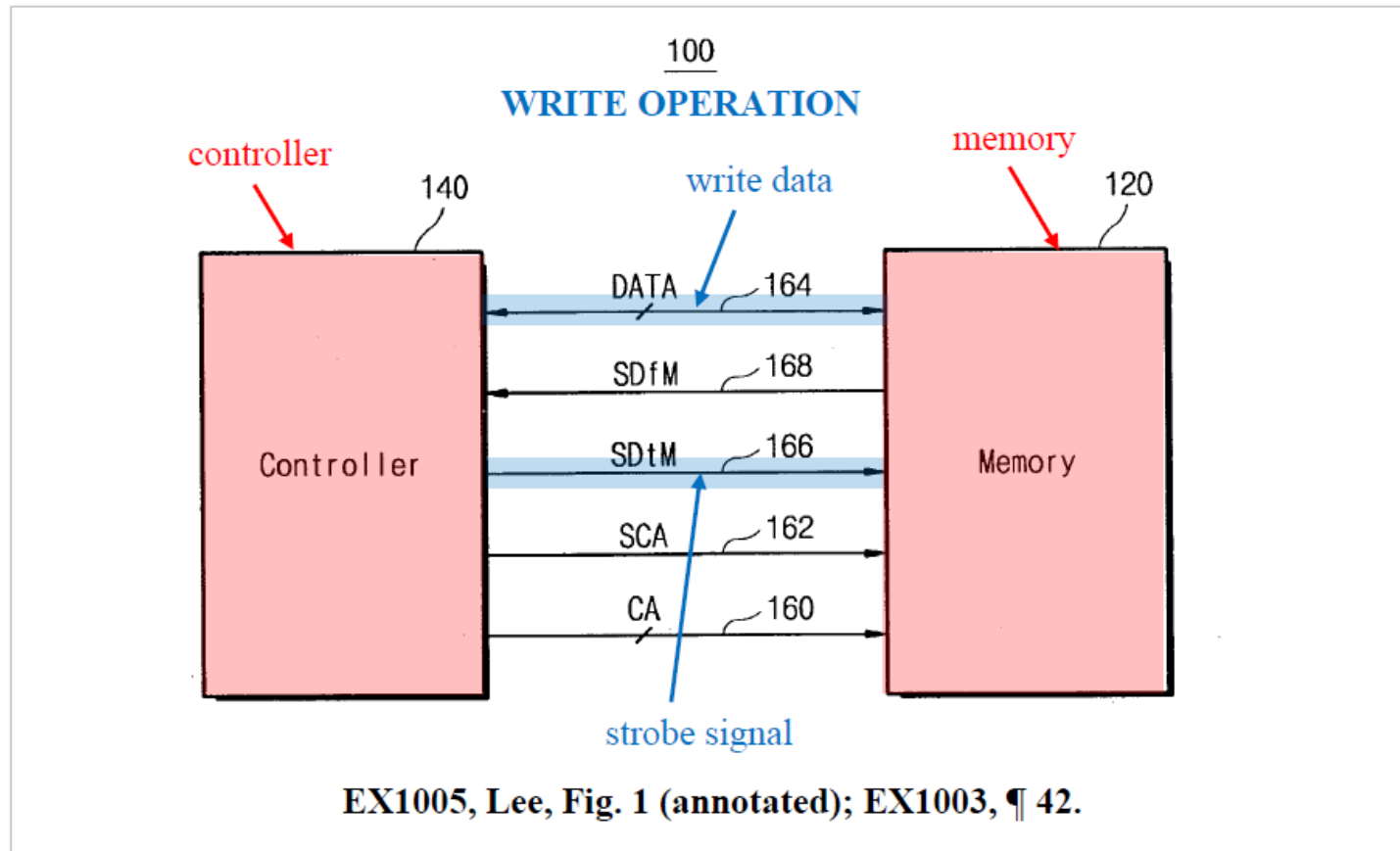
A source synchronous read operation with turnaround strobe (**DATA STROBE SIGNAL**)



Pet., 12; Pet. Reply, 8

Prior Art Reference Lee

A source synchronous write operation*

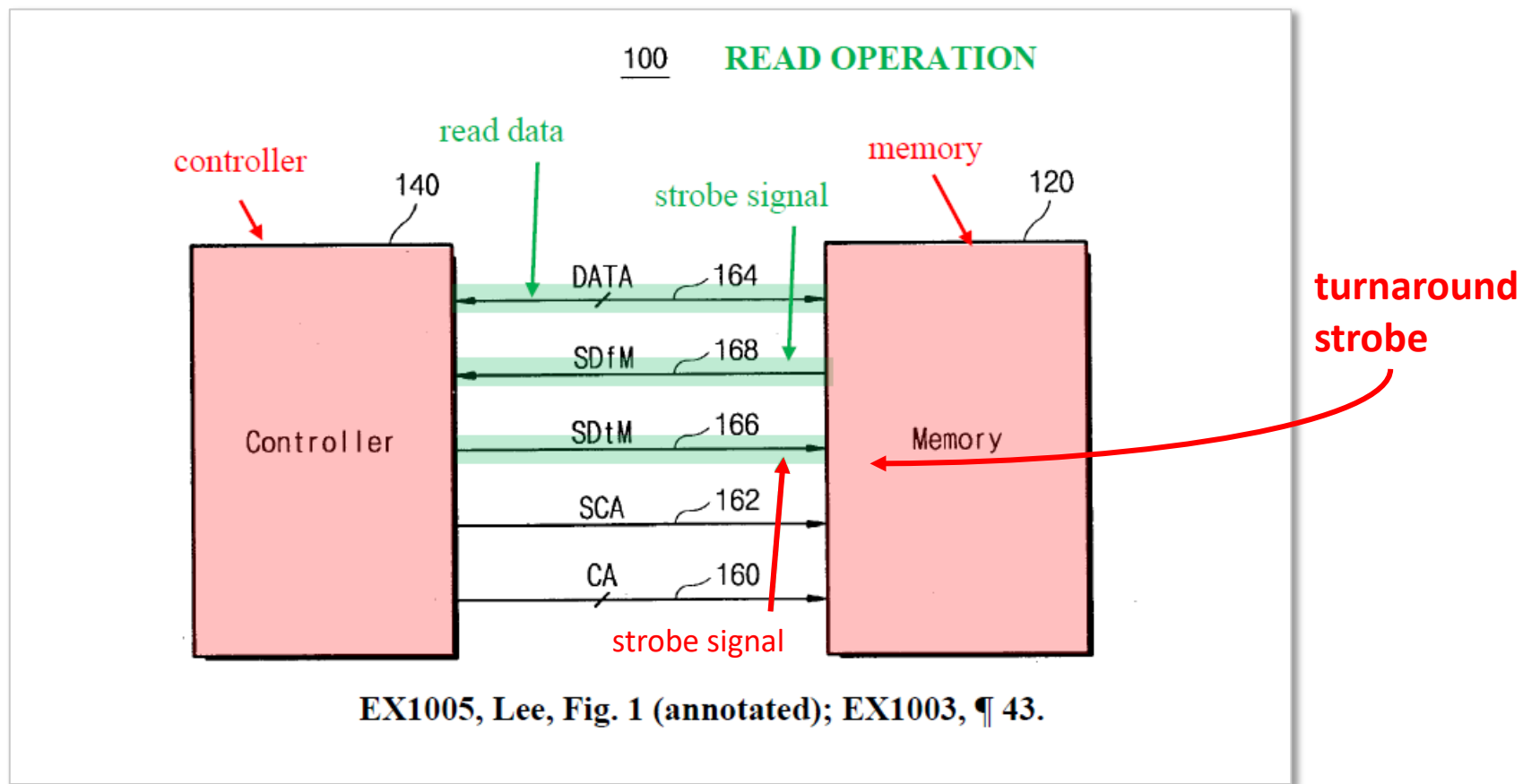


Pet., 23

* Note that Lee describes source synchronous operation at ¶¶[0017], [0018].

Prior Art Reference Lee

A source synchronous read operation with turnaround strobe (SDtM)



Pet., 25; Pet. Reply, 9

Instituted Claims and Grounds

Grounds	Claims	Basis
#1	1, 6, 10, 14, 15, 16, 17, 18, 19, 25, 26, and 27	Obvious under 35 U.S.C. § 103 (Pre-AIA) over Lee
#2	2, 7, and 11	Obvious under 35 U.S.C. § 103 (Pre-AIA) over Lee and JEDEC

Pet., 16; Inst. Dec., 7.

Patent Owner does not contest Ground #1. See POR, 1, 13. Thus, only Ground #2 remains at issue.

Claim 2 of '369 Patent

Claim 2 (and similarly claims 7 and 11) adds a **clock signal**, which is “independent of and separated from” the strobe signals

1. A system comprising:
 - a controller adapted to send out a first data strobe signal and a write data signal in a write operation, the write data signal being synchronized with the first data strobe signal, the controller being adapted, in a read operation, to send out a second data strobe signal and to receive a read data signal in synchronization with a read data strobe signal, the read data strobe signal being received by the controller in response to the second data strobe signal; and
 - a memory adapted to receive the write data signal in synchronization with the first data strobe signal in the write operation, the memory being adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal and to send the read data signal synchronized with the read data strobe signal.
2. The system according to claim 1, wherein the controller is further adapted to produce a clock signal and to send the clock signal to the memory, each of the first and the second data strobe signals and the read data strobe signal being independent of and separated from the clock signal.

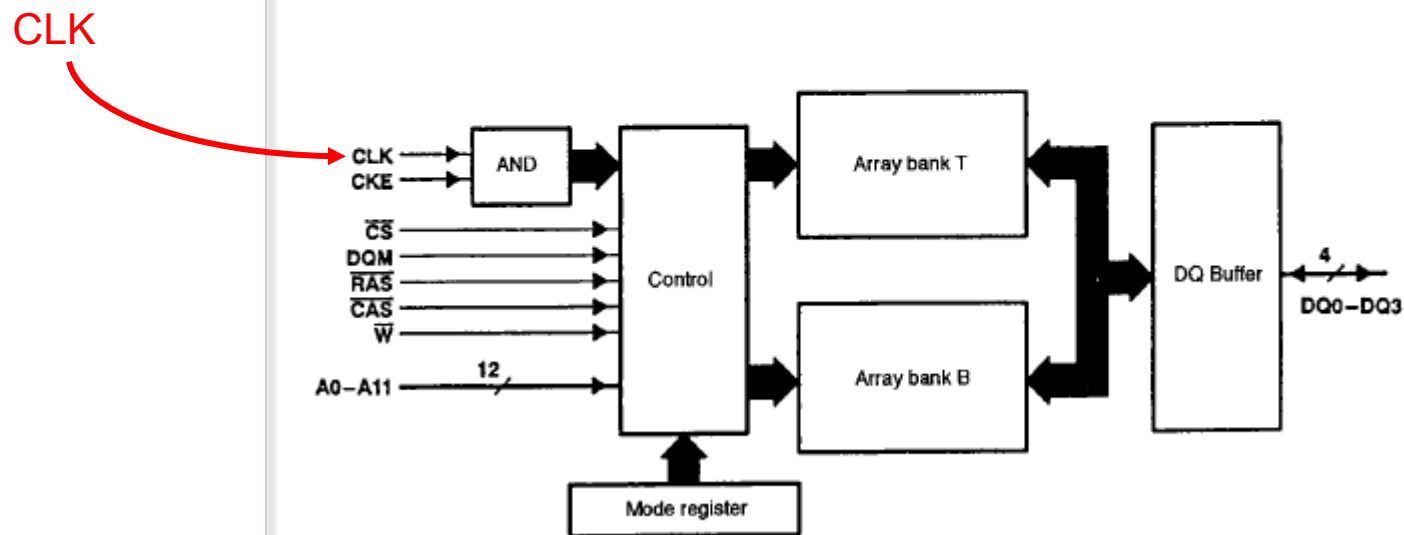
Clock signal

A Clock Signal – Synchronous Memory

Synchronous memory uses a system clock (CLK) to improve bandwidth

Pet., 60-61 and Pet. Reply, 11-13.

New interface architectures are also being used to improve the bandwidth of the RAMs. The most common is the synchronous interface. Making a memory synchronous puts it under the control of the system clock. "Wait states", during which the processor must wait for the output data from the RAM, can be reduced or eliminated. With a synchronous RAM the input addresses can be latched into the memory, freeing the processor to perform other tasks until the data is available after a known number of cycles. While the intrinsic speed of the RAM does not increase by the addition of a synchronous interface, the effective speed in the system increases since the processor no longer waits for the RAM to operate.



EX.1006 (Prince Textbook), 5, cited and discussed at Pet., 60-61 and Pet. Reply, 11-13.

The Remaining Issue to be Decided

Patent Owner argues:

- “Lee teaches an asynchronous memory.” PO Resp., 2, 14.
- “[T]o combine Lee with the JEDEC standard to use a synchronous and continuous clock with Lee [is] in direct contravention of [Lee’s] inventive concept and fundamental purpose.” PO Sur-Reply, 2.

Petitioner responds:

- Although asynchronous memories may use less power, synchronous memory provides higher bandwidth than asynchronous memories. Pet., 60-61.
 - There are more reasons to combine a clock, as taught in JEDEC, to Lee’s system. Pet. Reply, 11-17.
- Lee is not limited to asynchronous memory. Pet. Reply, 18-29.

Lee does not *require* asynchronous memory

When Lee discusses asynchronous memory, it is described that it “may be beneficial” in mobile applications, and that it is limited to “certain embodiments”

[0004] Various memory configurations have been utilized in conventional mobile processing systems such as Personal Communication Service (PCS), cellular, or Personal Digital Assistant (PDA). Such memory systems include non-volatile and volatile memories. Because mobile processing systems typically operate using a power supply voltage supplied from a battery, low-power operation of the memory system included in the mobile processing system may be beneficial. In particular, because mobile processing systems may spend much of their operational time in a standby state, memory systems that may provide low-power operation while the mobile processing system is in the standby state may also be beneficial.

[0005] The standby current generated in a conventional memory, such as a synchronous memory, having a clock tree structure may be substantially the same as that in a non-standby state. This may be the case because the clock signal is used as a transmission reference signal for synchronous memory operations and, therefore, the clock signal is, typically, internally produced irrespective of whether an operation is being performed by the synchronous memory.

[0034] As is discussed above, typically, the amount of current consumed by a memory system in a standby state results from the clock signal used to synchronize operations of a synchronous memory. If the memory uses the clock signal as an operation reference signal, the clock signal, typically, continues to be generated even while in the standby state. Thus, internal circuits that use or generate the clock signals continue to operate and consume current. However, according to embodiments of the present invention, as illustrated for example in FIG. 3, the strobe signals, such as SCA and SDtM, that are used as transmission references or synchronous signals, are used in the memory 120 only as a latch enable or latching signal. That is, the strobe signals SCA and SDtM are not used as a reference signal (e.g., a clock signal) for a memory operation. This means that the memory 120 performs read and write operations in an asynchronous manner, for example, using a delay chain as a state machine. Accordingly, certain embodiments of the present invention may be capable of reducing the standby current consumed in the memory 120 as no clocks need be generated or utilized as a reference signal for the operations to the memory array.

Lee, ¶¶[0004]-[0005], [0034], cited and emphasized as in Pet. Reply, 18-20

Lee's inventive concept and fundamental purpose does not require asynchronous memory

Lee's SUMMARY OF THE INVENTION section describes multiple embodiments, most of which refer generally to "memory," and not "asynchronous memory."

Asynchronous memory is mentioned for the first time in the third paragraph of the summary, in accordance with "further embodiments."

SUMMARY OF THE INVENTION

[0007] In accordance with certain embodiments of the present invention, there is provided systems, memories and/or methods of communicating with a memory that utilize a source synchronized interface. In some embodiments of the present invention, a memory is stores data information and a controller is controls read and write operations to/from utilizing the source synchronous interface. In some embodiments of the present invention, during write operations, the controller transfers to the memory a command and an address together with a first strobe signal and the memory latches the command and address in response to the first strobe signal. During the read operations, the memory responds to a second strobe signal from the controller to generate a third strobe signal, and the controller receives data from the memory in response to the third strobe signal.

[0008] In still further embodiments of the present invention, a memory is provided that includes a first interface circuit that latches the command and address in response to the first strobe signal and a second interface circuit that outputs read data in response to the second strobe signal. The data with the signal is transferred via the read data buses.

[0009] In accordance with further embodiments of the present invention, communications with an asynchronous memory are provided by receiving at the asynchronous memory a command, an address and a first strobe signal. The command and the address are each received at least partially concurrently with the first strobe signal. Data stored in the asynchronous memory is read from the memory based on the received command and the receive address. A second strobe signal is received at the asynchronous memory and a third strobe signal is generated in response to receipt of the second strobe signal. The data read from the asynchronous memory and the third strobe signal are output from the asynchronous memory. Furthermore, the data read from the asynchronous memory and the third strobe signal are at least partially concurrently output.

Lee, ¶¶[0007]-[0009], highlighting added; cited and emphasized in Pet. Reply, 25-26.

Lee's inventive concept and fundamental purpose does not require asynchronous memory

Lee's DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS section warns the reader not to limit the invention to the “embodiments set forth herein.”

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0016] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. However, this invention should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout. It also will be understood that when an element is referred to as being “connected” or “coupled” to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being “directly connected” or “directly coupled” to another element, there are no intervening elements present.

Lee, ¶[0016], highlighting added; cited and emphasized in Pet. Reply, 26

Lee's inventive concept and fundamental purpose does not require asynchronous memory

Lee's DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS section, through USP 6,336,159's incorporation by reference, teaches using a clock

[0018] A source synchronous interface is an interface where data is sent from a transmitter to a receiver together with a clock signal, which is used within a receive interface to latch the accompanying data. Source synchronous interfaces may remove the limit of the time of flight on wire between a transmitter and a receiver and may not require controlled clock skew between the transmitter and the receiver. Source synchronous interfaces are disclosed in U.S. Pat. No. 6,311,285 entitled "METHOD AND APPARATUS FOR SOURCE SYNCHRONOUS TRANSFERS AT FREQUENCIES INCLUDING ODD FRACTION OF A CORE FREQUENCY" and U.S. Pat. No. 6,336,159 entitled "METHOD AND APPARATUS FOR TRANSFERRING DATA IN SOURCE-SYNCHRONOUS PROTOCOL AND TRANSFERRING SIGNALS IN COMMON CLOCK PROTOCOL IN MULTIPLE AGENT PROCESSING SYSTEM," the disclosures of which are incorporated herein by reference as if set forth fully herein.

Lee, ¶[0018], cited in Pet. Reply, 26-27

The '159 patent describes: "a system that transmits data using a source synchronous protocol while transmitting control signals using a common clock protocol in order to increase the bandwidth of transmitting data without a corresponding increase in the number of signals transmitted." EX1014, 1:49-54, cited in Pet. Reply, 26.

Lee's inventive concept and fundamental purpose does not require asynchronous memory

Lee's CLAIMS recite different systems, some of which refer generally to "memory," and others that refer specifically to "asynchronous memory."

5. A system comprising:

- a **memory** configured to store data information and further configured to latch command and address information in response to receipt of a first strobe signal, to latch write data in response to receipt of a second strobe signal for a write operation and to generate a third strobe signal in response to receiving the second strobe signal and output read data and the generated third strobe signal for a read operation; and
- a controller configured to control the read and write operations of the memory, the controller being further configured to transfer to the memory the command and address information together with the first strobe signal, transfer write data to the memory together with the second strobe for a write operation and transfer the second strobe to the memory and receive the read data together with the third strobe output from the memory for a read operation

12. A system comprising:

- an **asynchronous memory** having a first interface circuit which receives a command and an address in response to a first strobe signal, a second interface circuit that receives data in response to a second strobe signal, and a strobe signal generator circuit that generates a third strobe signal in response to the second strobe signal; and
- a memory controller that generates the first and the second strobe signals and receives data from the asynchronous memory in response to the third strobe signal.

Lee claim section, highlighting added; cited and emphasized in Pet. Reply, 23, 27

Conclusion

- Lee's inventive concept, like the '369 patent, is a source synchronous memory system utilizing a turnaround strobe.
- Lee discusses that asynchronous memory “may be beneficial” in mobile applications, but Lee never requires asynchronous memory.
- Lee repeatedly uses the general term “memory” to describe its invention. It refers to asynchronous memory with respect to “certain embodiments” or only in some (not all) claims.

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Reasons to Combine Lee and JEDEC

- Synchronous memories provide the following benefits over asynchronous memories:
 - “Increased bandwidth”
 - “Reduced cost to fabricate”
 - “Industry standard”
 - “Predictable timing, ... less skew, faster turnaround requests, and support high-bandwidth operations such as burst mode”
 - “Reduced cost and simplicity of design”

Pet. Reply, 11-17, citing Petition and PO’s expert, Dr. Jacob