

IPR2023-01200 (’369 Patent)

**WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,
v.
LONGITUDE LICENSING LTD.,
Patent Owner.**

Patent Owner’s Demonstratives

Served October 11, 2024
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IPR2023-01200
Longitude Licensing Ltd.
Ex. 2005, Page 1 of 26

'369 Patent

U.S. Patent 7,697,369 (Ex. 1001)


 US007697369B2

(12) **United States Patent**
Koshizuka

(10) **Patent No.:** US 7,697,369 B2
 (45) **Date of Patent:** Apr. 13, 2010

(54) **SYSTEM WITH CONTROLLER AND MEMORY**

(75) **Inventor:** Atsuo Koshizuka, Tokyo (JP)

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(21) **Appl. No.:** 11/759,862

(22) **Filed:** Jun. 7, 2007

(65) **Prior Publication Data**
 US 2007/0291577 A1 Dec. 20, 2007

(30) **Foreign Application Priority Data**
 Jun. 8, 2006 (JP) 2006-160204

(51) **Int. Cl.**
 G11C 5/00 (2006.01)

(52) **U.S. Cl.**
 365/233.1; 365/230.06

(58) **Field of Classification Search**
 365/233.1; 365/230.06

See application file for complete search history.

(56) **References Cited**
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(10) **Patent No.:** US 7,697,369 B2
 (45) **Date of Patent:** Apr. 13, 2010

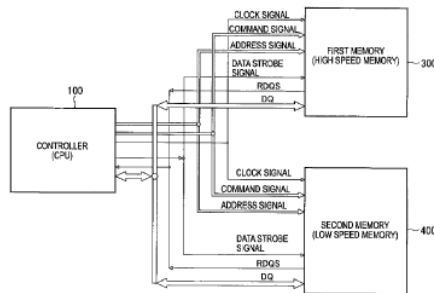
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ABSTRACT
 According to the system of the present invention, data (DQ) signals are outputted/received between a controller 100 and a memory 200 based on a data strobe signal sent out from the controller 100. The data strobe signal is independently and completely separated from a clock signal. The data strobe signal has a frequency different from a clock signal. Therefore, the memory 200 is not required to generate a read data strobe signal in synchronization with the clock signal.

27 Claims, 16 Drawing Sheets



EX1001 / Page 1 of 22
Western Digital Technologies, Inc.

Ex. 1001

- Entitled “System With Controller and Memory”
- Atsuo Koshizuka
- Application Filed June 7, 2007

'119 Patent Claims 2, 7, 11

The system according to claim [1, 6, 10] wherein the controller is further adapted to produce a clock signal and to send the clock signal to the memory, each of the first and second data strobe signals and the read data strobe signal being independent of and separated from the clock signal.

Ex. 1001, '369 Patent at 21-22

Ex. 1001, '119 Patent at 5:26-6:3.

The Claims at Issue Require a Synchronous Clock

The system according to claim [1, 6, 10] wherein the ***controller is further adapted to produce a clock signal and to send the clock signal to the memory***, each of the first and second data strobe signals and the read data strobe signal being independent of and separated from the clock signal.

Ex. 1001, '369 Patent at 21-22

Use of a Synchronous Clock is Key to the Invention of the '369 Patent

the memory 200 ... has ... an internal clock generating section 230 ***The internal clock generating section 230 generates an internal clock signal upon receiving the clock signal and sends out the internal clock signals to circuits for command/address and so on.*** As shown in Fig. 3, the input/output operation of the memory 200 is carried out based on the data strobe signal received from the controller 100 and is completely separated from the clock signal.

Ex. 1001, '369 Patent at 4:55-5:5
(emphasis added)

The Petition's Second Challenge

Ground No. 2:

**Claims 2, 7, and 11 Are Not Obvious Over The Combination of
Lee and JEDEC**

Lee Seeks to Enable a Low Power System By Foregoing A Continuous Clock

Various memory configurations have been utilized in conventional mobile processing Systems Such as Personal Communication Service (PCS), cellular, or Personal Digital Assistant (PDA). Such memory systems include non-volatile and volatile memories. *Because mobile processing systems typically operate using a power supply voltage supplied from a battery, low-power operation of the memory system included in the mobile processing system may be beneficial. In particular, because mobile processing systems may spend much of their operational time in a standby state, memory systems that may provide low-power operation while the mobile processing system is in the standby state may also be beneficial.*

Ex. 1005, Lee ¶ [0004]

Lee Seeks to Enable a Low Power System By Foregoing A Continuous Clock

The standby current generated in a conventional memory, such as a synchronous memory, having a clock tree structure may be substantially the same as that in a non-standby state.

This may be the case because the clock signal is used as a transmission reference signal for synchronous memory operations and, therefore, ***the clock signal is, typically, internally produced irrespective of whether an operation is being performed by the synchronous memory.***

Ex. 1005, Lee ¶ [0005]

Lee's Low Power Mode Requires An Asynchronous Clock

The memory 120 operates in an asynchronous fashion, for example, a fashion using a conventional technique that utilizes a delay chain as a state machine. Furthermore, as is seen from the discussion above, the Strobe Signals SCA and SDtM that are used as transmission synchronous signals are only toggled when a transfer is occurring. ***Thus, the need for a continuous clock may be avoided and the current consumed by the memory 120 when not performing a read or write operation may be reduced over a similar memory that utilizes a continuous clock.***

Ex. 1005, Lee ¶ [0028]

Lee's Low Power Mode Requires An Asynchronous Clock

As is discussed above, typically, the amount of current consumed by a memory system in a standby state results from the clock signal used to synchronize operations of a synchronous memory.... However, according to embodiments of the present invention, as illustrated for example in FIG. 3, the strobe signals, such as SCA and SDtM, that are used as transmission references or Synchronous Signals, are used in the memory 120 only as a latch enable or latching Signal. ***That is, the strobe signals SCA and SDtM are not used as a reference signal (e.g., a clock signal)*** for a memory operation. Accordingly, certain embodiments of the present invention may be capable of reducing the standby current consumed in the memory 120 as no clocks need be generated or utilized as a reference Signal for the operations to the memory array.”

Ex. 1005, Lee ¶ [0034]

Lee Expressly Claims Asynchronous Memory Systems

What is claimed is:

1. An asynchronous semiconductor memory device comprising:

- a memory array configured to store data information;
- a first interface circuit configured to latch command and address information in response to a first strobe signal received by the asynchronous memory device;
- a read circuit configured to read data information from the memory array in response to the latched command and address information;
- a signal generator circuit configured to generate a third strobe signal based on a second strobe signal received by the asynchronous semiconductor memory device; and
- a second interface circuit configured to latch data read from the array by the read circuit in response to the second strobe signal and output the latched data read from the array and the generated third strobe signal at least partially concurrently with the output of the latched data read from the array.

12. A system comprising:

- an asynchronous memory having a first interface circuit which receives a command and an address in response to a first strobe signal, a second interface circuit that receives data in response to a second strobe signal, and a strobe signal generator circuit that generates a third strobe signal in response to the second strobe signal; and
- a memory controller that generates the first and the second strobe signals and receives data from the asynchronous memory in response to the third strobe signal.

17. A system comprising:

an asynchronous memory; and

a memory controller that generates first and second strobe signals,

wherein the asynchronous memory includes:

- a memory array that stores data information;
- a first interface circuit that latches command and address information in response to the first strobe signal;
- a read circuit that reads data from the array in response to the latched command and address information;
- a signal generator circuit that delays the second strobe signal to generate a third strobe signal; and
- a second interface circuit that latches data read by the read circuit in response to the second strobe signal, the latched data in the second interface circuit being transferred to the memory controller together with the third strobe signal.

Ex. 1005, Lee at 11-12.

Lee is Entitled “Asynchronous Memory Using Source Synchronous Transfer And System Employing Same



US 2004/0022095A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2004/0022095 A1**

Lee

(43) **Pub. Date: Feb. 5, 2004**

(54) **ASYNCHRONOUS MEMORY USING
SOURCE SYNCHRONOUS TRANSFER AND
SYSTEM EMPLOYING THE SAME**

Publication Classification

(51) **Int. Cl.⁷** **G11C 29/00**

(52) **U.S. Cl.** **365/200**

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(21) **Appl. No.: 10/396,933**

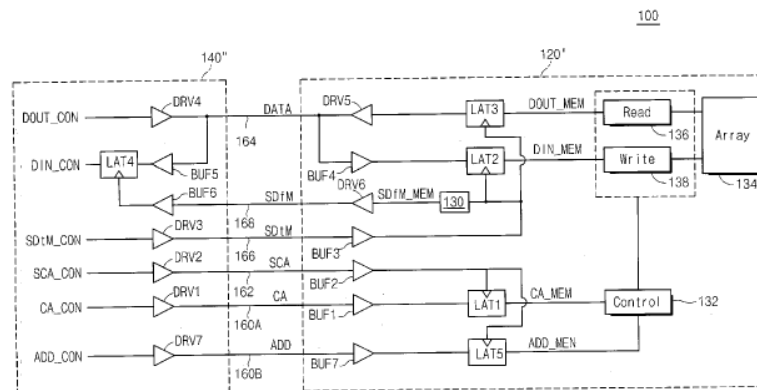
(22) **Filed: Mar. 25, 2003**

(30) **Foreign Application Priority Data**

Jul. 30, 2002 (KR) 2002-44982

(57) **ABSTRACT**

A memory for storing data information and/or a controller for controlling read/write operations of the memory based on a source synchronous interface are provided. During the read/write operations, a command and an address are provided to the memory together with the first strobe signal. The memory may latch the command and address in response to the first strobe signal. During a read operation, the memory responds to a received second strobe signal to generate a third strobe signal. The memory outputs data from the memory and the third strobe signal, for example, so that the output data may be latched with the third strobe signal by the memory controller.



Ex. 1005 at 1.

A POSITA Understands that Claim 5 of Lee is Limited to Asynchronous Memory Based On the Specification's Teaching



“[T]he specification ‘is always highly relevant to the claim construction analysis. Usually, it is dispositive; it ***is the single best guide to the meaning of a disputed term.***”

Phillips v. AWH Corp., 415 F.3d 1303, 1313 (Fed. Cir. 2005)

Lee Does Not Recite An Embodiment Using Synchronous Memory By Incorporating By Reference U.S. Patent No. 9,336,159

- Lee defines source synchronous transfer as the interface that the interface that provides “data transmission between the memory 120 and the memory controller 140” and was known in the art. Ex. 1005, Lee ¶ [0017].
- *See also* ex. 1005, Lee ¶ [0018] (“A Source synchronous interface is an interface where data is sent from a transmitter to a receiver together with a clock signal, which is used within a receive interface to latch the accompanying data.”).

Source Synchronous Transfer Is Irrelevant to the Inventive Concept of Lee

- Lee only incorporates U.S. Patent No. 6,336,159 for its discussion of “source synchronous interfaces.”
 - Ex. 1005, Lee ¶ [0018] (“Source synchronous interfaces are disclosed in ... U.S. Patent 6,336,159 ... the disclosures of which are incorporated herein by reference.”).
- Lee defines source synchronous transfer as the interface that the interface that provides “data transmission between the memory 120 and the memory controller 140” and was known in the art. Ex. 1005, Lee ¶ [0017];
 - Ex. 1005, Lee ¶ [0018] (“A Source synchronous interface is an interface where data is sent from a transmitter to a receiver together with a clock signal, which is used within a receive interface to latch the accompanying data.”).

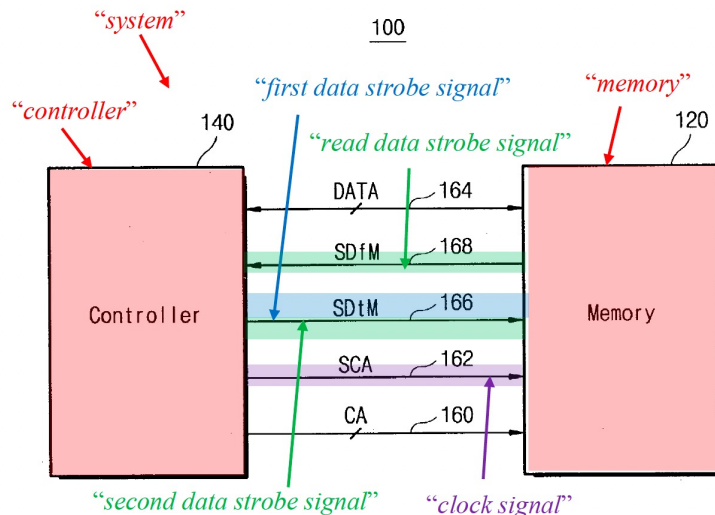
Petitioner's Proposed Combination Seeks To Implement the JEDEC Standards Teaching of a Continuous Clock Into Lee

“A POSITA would have found it obvious for Lee’s SCA signal to be implemented as a continuous clock signal consistent with the JEDEC standard for memory systems.”

Pet. at 57

Petitioner's Proposed Combination Would Frustrate Lee's Fundamental Purpose

Petitioner's Combination (Pet. at 64-65)



Combination of Lee and JEDEC
(annotated based on EX1005, Lee, Fig. 1); EX1003, ¶ 117.

"A POSITA would have found it obvious to substitute Lee's SCA signal using a clock signal"

Lee

"the strobe signals SCA and SDtM are not used as a reference signal (e.g., a clock signal) for a memory operation."

Ex. 1005, Lee ¶ [0034].

Any Combination Cannot Defeat the Purpose of the System Being Modified



When a substitution such as the would “defeat[] the purpose of” the system being modified, that “substitution is illogical” and cannot provide the basis for an obviousness determination.

In re Schweickert, 676 F. App'x 988, 994 (Fed. Cir. 2017)

Lee Teaches Away From Using The Continuous Clock of The Combination



“A prior art reference evidences teaching away if it ‘criticize[s], discredit[s], or otherwise discourage[s] the solution claimed.’”

In re Brandt, 886 F.3d 1171, 1178 (Fed. Cir. 2018)

Petitioner Presents No Evidence That a POSITA *Would* Have Combined Lee and JEDEDC



“[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.”

Belden Inc. v. Berk-Tek LLC, 805 F.3d 1064, 1073 (Fed. Cir. 2015)

Petitioner Presents No Evidence That a POSITA *Would Have* Combined Lee and JEDEDC

Petitioner fails to show that a POSITA would have chosen the benefits of increased bandwidth over the low-power benefits of asynchronous memory.

- Lee teaches its memory preferable over conventional, synchronous memory systems.
- Ex. 1005, Lee ¶ [0005] (in “**conventional memory, such as a synchronous memory** ... the clock signal is, typically, internally produced irrespective of whether an operation is being performed by the synchronous memory”)
- *Id.* ¶ [0028] (“The memory 120 operates in an asynchronous fashion **Thus, the need for a continuous clock may be avoided and the current consumed by the memory 120 when not performing a read or write operation may be reduced over a similar memory that utilizes a continuous clock.**”)
- *Id.* ¶ [0034] (“according to embodiments of the present invention, as illustrated for example in FIG. 3, the strobe signals ... **are not used as a reference signal (e.g., a clock signal)** for a memory operation”)

Petitioner Presents No Evidence That a POSITA *Would* Have Combined Lee and JEDED

- Petitioner wrongly asserts the use of synchronous or asynchronous memories are design tradeoffs.
- Petitioner fails to rebut Dr Jacob's opinions that using synchronous memory "represents a complete transformation of the interface." Ex. 2003, Jacob Decl., ¶ 85.

Petitioner's Justification for Using the SCA in Lee as Clock Signal Using the '369 Patent Teaching as a Roadmap

“The SCA signal in the combination of Lee and JEDEC serves the same function as the clock signal described in the '369 Patent.”

Petition at 66.

Petitioner Presents No Evidence That a POSITA *Would* Have Combined Lee and JEDEDC



“The inventor's own path itself never leads to a conclusion of obviousness; that is hindsight. What matters is the path that the person of ordinary skill in the art would have followed, as evidenced by the pertinent prior art.”

Otsuka Pharm. Co. v. Sandoz, Inc., 678 F.3d 1280, 1296 (Fed. Cir. 2012)

Neither Expert Presented Evidence of Cost Benefits From Using Asynchronous or Synchronous Memory

- Petitioner's Expert, Dr. Baker, declined to offer an opinion that asynchronous memory was more expensive than synchronous memory.
 - Ex. 2004, Baker Depo. Tr. at 22:7-25:19
- Patent Owner's Expert Dr. Jacob had "no opinion" on the topic
 - Ex. 1015, Jacob Depo Tr. at 22:10-23:8