

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,

Petitioner

v.

LONGITUDE LICENSING LTD.,

Patent Owner.

IPR 2023-01200

Patent 7,697,369 B2

Record Of Oral Hearing

Held: October 23, 2024

Before RICHARD M. LEBOVITZ, DAVID C. McKONE, and
KEVIN C. TROCK, Administrative Patent Judges.

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P-R-O-C-E-E-D-I-N-G-S

1:00 p.m.

JUDGE TROCK: Okay, this is Judge Trock, can everybody hear me? Great, thank you. Thank you for your patience. All right, let's get started. We're here on IPR 2023-01200 concerning U.S. Patent 7697369. With me today on the panel are Judges McKone and Lebovitz. This is in the matter of Western Digital Technologies versus Longitude Licensing Limited. Let's start with appearances from Petitioner.

MR.O'DELL: Hello Board, my name is David O'Dell, I'm the lead counsel on this case and I represent Petitioner, Western Digital. With me today is my co-counsel Hong Shi.

JUDGE TROCK: Good day, Mr. O'Dell.

MR. O'DELL: Good day.

JUDGE TROCK: How about appearances for Patent Owner?

MR. LEDAHL: Thank you, Your Honor, Brian Ledahl for the Patent Owner, and with me on the hearing today is lead counsel for the Patent Owner James Milkey.

JUDGE TROCK: Good day Mr. Ledahl.

MR. LEDAHL: Thank you.

JUDGE TROCK: I appreciate your patience on the technical difficulties I've been having. We're here today to hear the parties' arguments in this matter, our primary concern is your opportunity to be heard. If you are experiencing technical difficulties, please let us know right away so that we can get those resolved. The parties have requested 30 minutes per side for this argument today, we will start with Petitioner. Petitioner, do you want to reserve any of your time for rebuttal?

1 MR. O'DELL: Yes, I would like to reserve 10 minutes for rebuttal, so
2 20 minutes for this initial presentation.

3 JUDGE TROCK: Thank you, and Patent Owner I'm going to ask you
4 the same question now, do you want to reserve any of your time for rebuttal?

5 MR. LEDAHL: Yes, I would like to reserve five minutes for sur-
6 rebuttal time.

7 JUDGE TROCK: Okay, and that will give you 25 minutes on your
8 principle argument. So, we have all the exhibits of record, and what I'm
9 going to request is that when you make your presentation that if you're
10 going to use an exhibit please identify it by page number and by document
11 number so that we can follow along with you. Give us a moment to catch
12 up, because we have all the exhibits and the papers of record before us on
13 our computers. Please identify yourself for the court reporter each time you
14 speak, speak slowly, if you're not speaking, please mute your microphone so
15 there isn't any interference. At the end of the session, the court reporter may
16 have some questions with respect to spelling, we will stay on the line for you
17 so that you can take care of that, and if there are no other questions from
18 counsel, you feel ready to get started, then Petitioner, the floor is yours.

19 MR. O'DELL: All right, thank you very much. I am going to share
20 my screen, and this will be the presentation that we filed, I believe, two days
21 ago. Is that showing okay? Judge Trock, do you see --

22 JUDGE TROCK: Yes, I have it.

23 MR. O'DELL: Okay great, thank you. All right, ready to start. My
24 name is David O'Dell, I represent the petitioner, Western Digital, I have
25 slide one of my presentation up on the screen today, and we are talking
26 about the patentability of the 369 Patent. Turning to slide two of the

1 presentation, I would like to briefly discuss the 369 Patent and the prior art,
2 as well as some of the terminology that we use in the briefing to make sure
3 that everything is clear. I believe that we will then move on to what is the
4 single issue to be decided by this board.

5 All right, Claim 1 of the 369 Patent describes a system with a
6 controller and a memory. In a system such as this, data is written from the
7 controller to the memory, and data is read from the memory to the controller.
8 A conventional process for writing and reading data is a so-called source
9 synchronous operation, and I'm going to discuss this briefly in the next
10 slide, in which the device driving the data, be it the controller or the
11 memory, also drives the strobe signals so that the device receiving the data
12 can know that the data on the bus is good and valid.

13 Source synchronous operations is old and is actually used not only in
14 the patent but in both prior art references, Lee and JEDEC, the JEDEC
15 standard. The inventive concept of the 369 Patent is the addition of another
16 strobe used during read operation, which the Patent Owner's expert calls a
17 turnaround strobe, it's the claimed second strobe signal. And I think a
18 turnaround strobe is a nice tag, we're find with that term used by the Patent
19 Owner's expert to kind of identify this. So you'll see in our papers that we
20 kind of adopted his terminology there, a turnaround strobe. As discussed in
21 this petition, this concept of a turnaround strobe is why the original examiner
22 allowed this patent, this red underlined portion of the claim was the part that
23 was amended and argued to obtain allowance of the claim and the patent.

24 Turning to slide three, again I'm using the Patent Owner's expert, one
25 to avoid any dispute and second, it's perfectly clear. This is source
26 synchronous operation, it's an old process. And again, when you're

1 transferring data, the device transferring the data also sends a strobe signal.
2 So here in the data write operation, the memory controller rides the data on
3 the data bus, and the strobe signal on the strobe line, so that the memory
4 device receives it, the strobe allows the memory device, hey, the data on the
5 data bus is good. And likewise, in the read operation this goes the other way
6 from the memory device. So this is, source synchronous operation is a way
7 to notify the recipient that the data on the data bus is good.

8 On slide four, actually, let me go to slide five of the presentation.
9 And here is where the turnaround stroke comes in. so in a read operation, it
10 is the memory device that is driving data and the data strobe, read data
11 strobe. What the invention of the 369 Patent was to add another stroke, here
12 I've labeled it as the turnaround stroke, and this allows the controller to
13 control when the memory device is to drive the data, this allows the
14 controller to be in control, and that's the invention of the 369 Patent. So the
15 controller sends out this data strobe signal here, this is from their patent, and
16 this dotted line here is what was shown in their patent, it's the turnaround
17 strobe. Once the memory gets this turnaround strobe, the claimed second
18 data strobe, it can then send out the read data strobe and drive the data on the
19 data bus.

20 And this is uncontested, but Lee describes the same thing, and turning
21 to slide seven of the presentation, here's a read operation in Lee where read
22 data and a strobe signal from the memory device is started when it receives
23 this turnaround strobe, SDTM, from the controller. This is not being
24 contested. On slide eight, I have the grounds that we presented in the
25 petition, ground one is for the majority of the claims, and ground two is for
26 dependent Claims 2, 7, and 11, and I believe the parties are in agreement that

1 Claims 2, 7, and 11 are essentially the same except for the corresponding
2 base claim. And so going forward, I'll use Claim 2 as being representative.

3 Turning to slide nine, here I have Claims 1 and 2, and in Claim 2, the
4 system of Claim 1 is adapted to further produce a clock signal. The clock
5 signal, according to the claim and its general understanding is independent
6 of the read data strobe signals, and all of the strobe signals used in
7 transferring data described, all three of the strobe signals. The clock signal,
8 turning to slide 10, using a clock signal is what people in the art refer to as
9 synchronous memory. And so I want to be clear that source synchronous
10 operation does not imply that there's a clock signal, a free running clock
11 signal, but a synchronous memory does. A synchronous memory is a
12 memory that's controlled by a free running clock.

13 Here I have on slide 10 a picture from a textbook, this prior art. It
14 talks about this new architecture called synchronous interface, and having a
15 synchronous interface improves the bandwidth of the system, it actually
16 allows a second read to start while the first read is occurring. And here in
17 the picture, you can see that a clock signal identified by the signal CLK is
18 provided to the control and address signals of the memory device. And if
19 you see on the right, the data signals are not being controlled by the clock
20 signal, it is the control and address signals. JEDEC describes the same
21 thing, but JEDEC is a standard document, and it's the commonly accepted
22 standard for most memory devices, very popular, and it's
23 more detailed in its drawing, and so I've kind of chosen this drawing due to
24 its simplicity.

1 JUDGE McKONE: This is Judge McKone, I have a quick question.
2 JEDEC, is that a standard for synchronous memory or asynchronous
3 memory or both?

4 MR. O'DELL: It's a standard for synchronous memory only.

5 JUDGE McKONE: Okay.

6 MR. O'DELL: So, yes. Turning to slide 11, the sole point that I
7 believe this Board needs to address is the combination of Lee with JEDEC,
8 and more specifically whether Lee -- that it would be obvious to modify Lee
9 to include a clock as described in the JEDEC standard. Okay, so Lee
10 teaches an asynchronous memory, it does. And as we've discussed the term,
11 an asynchronous memory does not have a clock. So the question before the
12 Board is whether it would be obvious to modify Lee to include a clock. And
13 the Patent Owner argues that to combine Lee with the JEDEC standard, to
14 use a synchronous and continuous clock with Lee is in direct contravention
15 of Lee's invented concept and fundamental purpose. They also argue that
16 Lee teaches away from using a clock signal, or said differently, teaches
17 away from using synchronous memory.

18 In our response, and this is going to be the whole subject of this
19 discussion, although asynchronous memories may use less power,
20 synchronous memories provide higher bandwidth than asynchronous
21 memories, and that there are many reasons to modify Lee to use a clock and
22 be a synchronous memory. And we presented five or six reasons, and I have
23 those listed at the end of the presentation. I don't think the reasons to
24 combine are being argued against, instead I think that Patent Owner is solely
25 relying on this contravened Lee's invented concept, or Lee teaches away
26 from using synchronous memory. I will agree that Lee has a primary

1 embodiment that is asynchronous memory, so that's not disputed, the
2 question is whether Lee teaches away from using synchronous memory or a
3 clock.

4 JUDGE TROCK: This is Judge Trock, can you hear me?

5 MR. O'DELL: Yes.

6 JUDGE TROCK: So I have a question with respect to these rationales
7 to combine Lee and JEDEC. Which of those rationales are included in the
8 petition?

9 MR. O'DELL: Okay, yes, I am going to jump to the -- just a second.
10 So I believe several of these are described in the petition, including the first
11 three, but Patent Owner's expert provided additional reasons that were using
12 -- Patent Owner's expert discussed the benefits of using synchronous
13 memory, which we added in the reply. So the petition described that
14 synchronous memory has increased bandwidth and reduced cost to fabricate,
15 and it's an industry standard. And that is --

16 JUDGE TROCK: Okay, so this is Judge Trock again. I'm in your
17 petition pages 60, 61, I see higher bandwidth capabilities, I'm not seeing
18 reduced cost to fabricate, I'm not seeing the industry standard, can you give
19 me a citation for that?

20 MR. O'DELL: Okay.

21 JUDGE TROCK: I mean you clearly describe the JEDEC standard in
22 here, but I'm trying to discern whether you've used that as a rationale to
23 combine these two references.

24 MR. O'DELL: So on page 61 of the petitions, POSITAs knew how to
25 implement memories using the clock signals and registers, because industry
26 standards defined how to do so. And so that was the argument here, that the

1 JEDEC standard, which is an industry standard for synchronous memories,
2 said this was a known standard.

3 JUDGE TROCK: Right, that's an argument, sure, I understand that,
4 that's an argument that you can do it, that's not an argument that you'd want
5 to.

6 MR. O'DELL: Yes.

7 JUDGE TROCK: I'm looking for the want to arguments.

8 MR. O'DELL: So the primary argument presented in the petition, and
9 I might have to look at this further, was that synchronous memory provides
10 increased bandwidth.

11 JUDGE TROCK: Right, I've got that at the top of page 61, right,
12 bottom of 60, top of 61, that's pretty clear. I'm just asking for these
13 additional ones. We can address this later on if you want, when we come
14 back for your rebuttal, if you want to take time while Patent Owner is
15 presenting and come up with those citations for me I'd appreciate it.

16 MR. O'DELL: Okay, yes, for now let's say that increased bandwidth
17 is certainly sufficient enough to motivate the combination, because a faster
18 computer is often a desirable thing to have.

19 JUDGE McKONE: This is Judge McKone, just so I understand
20 exactly what we're discussing here, what is the precise combination of Lee
21 and JEDEC that you're proposing?

22 MR. O'DELL: I don't have a slide for that, but the combination
23 would be to add a clock signal. So Lee uses this strobe signal, SCA, strobe,
24 control, and address, and the petition says that instead of using this strobe
25 signal, it would be obvious to use a clock signal.

1 JUDGE McKONE: Okay, so we're starting with Lee's device and
2 scheme, and Lee describes an asynchronous memory, so we're replacing the
3 memory 120 in Lee with a synchronous memory in JEDEC, and then we're
4 feeding that memory all these signals, except that SCA is now replaced with
5 a clock, is that now your combination?

6 MR. O'DELL: So I wouldn't say there's a wholesale replacement of
7 the memory 120 with JEDEC's memory, but the concept of using a clock
8 signal in Lee's memory is being replaced from this SCA signal, this strobe
9 control address signal.

10 JUDGE McKONE: Okay, so I'm a little bit confused here. So if we
11 start with Lee's memory which is asynchronous, you're saying we would
12 feed a clock signal to the asynchronous memory?

13 MR. O'DELL: Right, and the memory would of course have a clock
14 reception circuit, yes.

15 JUDGE McKONE: Why would we send a clock to an asynchronous
16 memory when the whole point of an asynchronous memory is it doesn't
17 work with the clock?

18 MR. O'DELL: So this would convert the memory to be a
19 asynchronous memory.

20 JUDGE McKONE: Is that the only difference between a synchronous
21 memory and an asynchronous memory, or is asynchronous memory different
22 technology which would make it higher bandwidth?

23 MR. O'DELL: So the difference -- just a second. I am back to slide
24 10. The addition of a synchronous memory is having this clock, it's
25 actually, in this figure it's showing a clock signal and a clock enable, CKE,
26 that you add that to the memory.

1 JUDGE McKONE: And that's the only thing you have to add, the
2 silicone is the same otherwise?

3 MR. O'DELL: This is beyond the scope of the briefing, but for the
4 sake and purpose of this discussion, yes.

5 JUDGE TROCK: Okay so this is Judge Trock. So your slide 10,
6 that's coming out of Prince, right, that's not coming out of JEDEC?

7 MR. O'DELL: Right.

8 JUDGE TROCK: So can you give us something from JEDEC that
9 will show us what your combination is?

10 MR. O'DELL: Yes.

11 JUDGE TROCK: And I'm assuming the clock is going to be on the
12 controller side, is that right?

13 MR. O'DELL: The clock is driven by the controller to the memory
14 device. So JEDEC provides timing diagrams and requirements, and here we
15 have a clock for the command and address signals.

16 JUDGE TROCK: So this is 59 in your petition, for purposes of the
17 record.

18 MR. O'DELL: Yes, thank you for saying that. So in 59 of the
19 petition, it shows Exhibit 1007 of JEDEC, Figure 22, where a clock signal is
20 used to control the command and address information, and that would be in
21 replace of the SCA strobe signal that is used in an asynchronous memory.

22 JUDGE McKONE: JEDEC, you said it describes the standard for
23 using synchronous memory, right?

24 MR. O'DELL: Yes.

1 JUDGE McKONE: So am I correct in assuming that the signaling
2 that is shown here in JEDEC's Figure 22 is signaling and controlling that's
3 optimized for use with a synchronous memory?

4 MR. O'DELL: The memory core will be unchanged, it's the
5 interface, the synchronous interface, in that the command and address
6 signals are sampled in response to a clock signal instead of a strobe signal.

7 JUDGE MCKONE: Okay, so JEDEC describes how at least the
8 design or the standard felt was the best way to access a synchronous
9 memory?

10 MR. O'DELL: JEDEC describes a synchronous memory by adding
11 the clock signals. The clock signal is fed into a register, but the strobe signal
12 is also fed into a register, so I don't know how much difference there is
13 between an asynchronous memory and a synchronous memory other than
14 the control and address functions are sampled in response to a continuous
15 clock or a non-continuous strobe signal.

16 JUDGE TROCK: You got about one minute left on your time.

17 MR. O'DELL: Okay, thank you.

18 JUDGE McKONE: I'm just wondering, if JEDEC tells us the
19 standard way of accessing a synchronous memory, why are we going to use
20 Lee's different scheme that is optimized for use with asynchronous
21 memory?

22 MR. O'DELL: Well let's address that. First of all, Lee is not
23 necessarily optimized, Lee has an embodiment that shows asynchronous
24 memory, and the arguments being made by the Patent Owner is Lee says
25 well, in mobile applications it may be beneficial to use asynchronous
26 memory. That to be implies it may not be, and it may not be beneficial in

1 mobile applications and Lee does not speak to other applications. Lee also
2 in its summary, the first two paragraphs of the summary describes source
3 synchronous interface which is used generally with memory, it's not until
4 the third paragraph of the summary that Lee discusses using asynchronous
5 memory in some of the embodiments. Lee describes embodiments that uses
6 synchronous memory -- yes, I'm sorry?

7 JUDGE TROCK: Sorry Mr. O'Dell, I'm just letting you know you're
8 out of time and you're going into your rebuttal time.

9 MR. O'DELL: Okay, that's okay with me. Lee describes an
10 embodiment here, this incorporated by reference 159, that is a synchronous
11 memory and uses a common clock protocol, which it recognizes provides
12 increased bandwidth. And finally, Lee's claims, he has some claims to a
13 system comprising a memory which I believe is a genus that covers both
14 asynchronous and synchronous memory, and yes, he has claims also directed
15 to asynchronous memory. So I believe that Lee certainly describes an
16 asynchronous memory, yes, but Lee is clear that he is open ended to his
17 invention of a turnaround strobe, which I believe is what Lee's invention is,
18 this source synchronous operation with the turnaround strobe, the same
19 invention of the 369, only Lee was first. This turnaround strobe can work
20 with memory in general, which would include both synchronous and
21 asynchronous, and it works with asynchronous memory, which is Lee's
22 preferred embodiment, his primary embodiment. So I believe that Lee
23 describes a preference for using asynchronous memory that may be a
24 preference, may be beneficial. Those are the words he uses, 'may be,' not
25 must be, may be, but he is open ended to being synchronous or

1 asynchronous and his spec identifies synchronous memory, it's in the spec.
2 So, anyway.

3 JUDGE TROCK: So Mr. O'Dell, this is Judge Trock again. So I
4 want to direct you to Lee paragraph 34 and ask you how to interpret this
5 paragraph. So 34 is discussing Figure 3, and towards the bottom third of 34,
6 Lee says memory 120, that's the principle memory that's described in Lee,
7 performs read and write operations in asynchronous manner, and then
8 towards the end of that paragraph it says in memory 120 as no clocks need
9 be generated or utilized as a reference signal for the operations to the
10 memory array. So that seems on its face pretty definitive that Lee's memory
11 120 is asynchronous and it does not, expressly is not going to use clocks.

12 MR. O'DELL: It is correct, memory 120 is asynchronous. Lee
13 describes an asynchronous memory, and Lee mentions the benefits, the low
14 operation power of -- and I have slide 12 of my presentation up on the
15 screen, which has that paragraph 34, and in certain embodiments it may be
16 capable of reducing the standby current. You know, typically it may be able
17 to be used, Lee certainly describes asynchronous memory -- so yes, Lee
18 describes an asynchronous memory, but Lee also mentions and covers
19 synchronous memory.

20 JUDGE TROCK: Right, so I don't want to put words in your mouth,
21 but are you saying then that someone of ordinary skill in the art at the time
22 of the invention, you would give up this power savings just in order to take
23 this bandwidth and use the clock signal from JEDEC, is that your argument?

24 MR. O'DELL: Yes, the synchronous memories are higher bandwidth,
25 the systems are faster, and that is often the desire of memory system
26 designers, to have a fast system, and the claims in Lee is not limited to

1 mobile applications, which admittedly like to have low power. Low power
2 is important in mobile applications. Speed is also important in mobile
3 applications, so.

4 JUDGE McKONE: Is the speed or the addition of making them faster
5 because there's a clock signal, is that the only thing that's different is if you
6 add a clock signal then it's faster and higher bandwidth?

7 MR. O'DELL: Yes, because by having a clock, you can start the next
8 operation, say a read operation while the first operation is still being
9 completed. So the controller gives a first address to the memory, the
10 memory starts to respond with data from the first address, but during that
11 time, the controller is working up a clock, it's giving a second address, so
12 it's called a pipeline, so you can actually move things faster through the
13 system by starting the next read operation. And Prince talks about that, we
14 talk about that when we cite Prince. Yes, the synchronous d RAM, while it
15 may consume more power, it does provide higher bandwidth, both Prince
16 says that and Lee says that in his incorporation by reference of the
17 synchronous d RAM into its spec.

18 JUDGE McKONE: Now if we accept your argument that a skilled
19 artisan would have combined the teachings of JEDEC and Lee because
20 JEDEC is a standard, why wouldn't we use JEDEC's standard set of
21 commands as shown in Figure 22 of JEDEC, why would we instead use
22 Lee's commands with the addition of a clock?

23 MR. O'DELL: So the combination being presented to add a clock is
24 taught by JEDEC into Lee's system, converting Lee's primary embodiment
25 120 from an asynchronous memory a synchronous memory. And JEDEC
26 also teaches a source synchronous operation, so another combination could

1 have been adding Lee's turnaround strobe to JEDEC. Everything else in
2 JEDEC is fine with the claim, it's a source synchronous memory transfer
3 operation with a clock signal used for the control and address signals. I
4 certainly want to answer all the questions but I'm trying to reserve as few
5 minutes as possible for my rebuttal.

6 JUDGE TROCK: You're down to about three minutes for your
7 rebuttal.

8 MR. O'DELL: Okay, then I will end it here and save the rest of my
9 three minutes for rebuttal.

10 JUDGE TROCK: Thank you, Mr. O'Dell.

11 MR. O'DELL: Thank you.

12 JUDGE TROCK: Patent Owner, the floor is yours.

13 MR. LEDAHL: Thank you, Your Honor, I'm going to also share my
14 screen if I may. It may take me just a moment here. So I think, we heard a
15 number of things that Petitioner argued here that I think are certainly not in
16 the petition, and don't really align with the reality of the argument here. I
17 think perhaps the most -- I'm sorry, I'm having difficulty getting it to allow
18 me to share my screen. But if you have the presentation, I'm looking at, I'd
19 like to start with slide 18, which I think is the clearest example of why the
20 argument that we just heard is inconsistent with the teachings of the
21 reference.

22 So in slide 18, we contrast Petitioner's combination, which was
23 described at pages 64 to 65 of the petition, and there the combination was,
24 and I think Mr. O'Dell said exactly the same thing in his presentation a few
25 moments ago, that a person of skill in the art would have found it obvious to
26 substitute Lee's, and he specifically said the SCA signal using a clock

1 signal. That's what they said in the petition. What does Lee say about that?
2 Well on paragraph 34 of Lee, which we were looking at just a moment ago,
3 the reference says the strobe signals, SCA, and SDtM are not used as a
4 reference signal, e.g. a clock signal for a memory operation.

5 So Petitioner's argument is that a person of skill in the art would read
6 Lee and then decide to do exactly the opposite of what Lee teaches a person
7 should do in implementing Lee's teaching. That's far from a motivation to
8 combine, and this suggestion that there would somehow be some theoretical
9 bandwidth improvement, I think a number of the questions spoke to this, and
10 I don't think Petitioner, certainly didn't point to anything in the petition that
11 shows how this clearly hindsight based combination would somehow
12 improve the bandwidth of Lee's memory simply by adding a clock. That's
13 an assertion that was made here, but there's no showing of how that would
14 be implemented or how simply adding a clock signal to Lee, this kind of
15 Rube Goldberg approach that is proposed would suddenly make that
16 asynchronous memory faster or have more bandwidth, it's just, that's pure
17 empty argument, there no evidence supporting that.

18 JUDGE McKONE: Do you disagree that the difference between an
19 asynchronous memory and a synchronous memory is simply the addition of
20 a clock to a synchronous memory?

21 MR. LEDAHL: I would say that's certainly a critical change, but as I
22 think some of your questions got to, that's not the only thing that you would
23 likely need to address. I mean, Petitioner suggested oh, well we could have
24 looked at JEDEC as the primary reference, obviously that's not the
25 combination that was presented in the petition. What was presented was
26 take an asynchronous memory and start running a clock into it with no

1 indication of how that asynchronous memory would then become faster or
2 otherwise deal with the signaling to suddenly accept -- so, for example
3 there's no discussion of how the circuitry on the memory side, so the
4 argument was the signal, this clock signal would come from the controller.
5 We've seen nothing to suggest that somehow the memory wouldn't need to
6 be modified in some way to achieve this kind of pipelining that Mr. O'Dell
7 described. That's not in the petition, it's not in the evidence, it's just a sort
8 of naked assertion without any support. There's no showing that that's
9 actually what would happen if you made this modification, or indeed that it
10 would work. If anything, it could easily be far less efficient and achieve
11 none of the benefits. It could have high-power consumption and low-power
12 bandwidth, which no one would want to create. And there's been no
13 showing in the petition that making this combination would actually achieve
14 this bandwidth benefit.

15 And I did want to address, I think Mr. O'Dell was asked about some
16 of the other purported motivations, we certainly would suggest that none of
17 the other motivations that he mentioned are referenced in the petition. I'll
18 concede that the petition makes a reference to bandwidth as a purported
19 motivation to combine, there is no discussion in the petition that the
20 existence of JEDEC as a standard would motivate combination, and there's
21 also no discussion of reduced fabrication costs in the petition, those are
22 argued and there was a suggestion in there, but I certainly can't find them in
23 the petition.

24 JUDGE McKONE: But Petitioner has argued that your expert
25 testified as to those benefits on cross examination. Why shouldn't we --

1 MR. LEDAHL: Well I don't think that's quite correct. I think what
2 was argued was that our expert somehow talked about different benefits that
3 I think Mr. O'Dell conceded are nowhere referenced in the petition, and
4 they're benefits, to be clear, they're not purported benefits of the
5 combination. What he's talking about is these are reasons why you might
6 have a synchronous memory by itself, it has certainly functional
7 characteristics that might be useful depending on your system to have a
8 synchronous memory. That's not --

9 JUDGE McKONE: You agree that we can consider your expert's
10 testimony as to the general benefits of synchronous memory, right? You're
11 not saying that that had to be in the petition?

12 MR. LEDAHL: Well, I think if it's something that's being argued as
13 a motivation to form the combination that's being alleged by Petitioner, then
14 it did have to be in the petition. I don't think the fact that they elicited
15 testimony that A, isn't about the combination and B, isn't in the petition
16 regarding benefits in general of synchronous memory is something that can
17 then be turned into a motivation to combine, only long after the petition has
18 been submitted.

19 JUDGE McKONE: Why shouldn't we be free to use whatever is in
20 your expert's cross examination testimony that you didn't object to and
21 exclude? After all, that is trial testimony, that's not simply discovery
22 deposition testimony, that's trial testimony that if it was out of line then you
23 had an obligation to try to manage that. Now that it's in the record, why
24 shouldn't we be able to use all of it?

25 MR. LEDAHL: Well it's in the record and it can be used as evidence,
26 what it cannot be used for is to manufacture new grounds that aren't set out

1 in the petition, that's not something that you can change just by having
2 additional evidence later, whether it comes from the petition or --

3 JUDGE McKONE: What is your support for that?

4 MR. LEDAHL: Well I would say that generally speaking the statute
5 and the case as interpreting it, I apologize that I don't have cites at my
6 fingertips, that the Petitioner must set forth the grounds for their argument in
7 the petition, that that's where the Petitioner has to lay out what is the
8 combination, what is the motivation to combine and make this combination,
9 and they can't keep changing it as the proceeding goes along. That's a
10 requirement of the petition, and while evidence may be considered, it has to
11 be evidence as to whether those grounds are supported, not a basis for
12 creating new grounds. And I realize that's a somewhat complicated
13 distinction, but I'm happy to discuss it further if that would be helpful.

14 JUDGE McKONE: I think I understand your position. I'm not sure I
15 agree with it, but I understand it.

16 JUDGE TROCK: This is Judge Trock. So I'm in your sur-reply page
17 seven, and I think the only statement you make here is attorney argument
18 and it's not citing to any part of the record, it says none of these reasons
19 show that a person of ordinary skill in the art would have combined Lee and
20 JEDEC. That's your statement.

21 MR. LEDAHL: That's right, but that's Petitioner's burden to show.
22 Petitioner --

23 JUDGE TROCK: I understand that, but I think Judge McKone's
24 point is that the identification of these benefits are coming from your expert.

25 MR. LEDAHL: Well as I said, I don't think their identification of
26 benefits of the combination, which is what would matter, I think in many

1 ways the expert's identification of benefits of synchronous memory do not --
2 if anything, they suggest you wouldn't be modifying and creating this
3 Frankenstein hybrid of asynchronous and synchronous memory. Why
4 would one ever do that? There are benefits to using synchronous memory,
5 and there are benefits to using asynchronous memory, and they're distinct
6 and they have different potential uses, but the suggestion that you would sort
7 of mix and match in this way seems solely driven by hindsight in this
8 proceeding and in this petition. And I did want to address -- I'm sorry, did
9 you have a question Your Honor?

10 JUDGE TROCK: No, I was just saying I understand your position,
11 thank you, go ahead.

12 MR. LEDAHL: I also want to address the argument that we heard
13 that Lee somehow teaches or discusses or doesn't exclude synchronous
14 memory. Obviously that last one doesn't exclude is partly a teaching for a
15 motivation to combine, there's no support for a standard that as long as you
16 don't exclude something that's a motivation to combine now. In fact, every
17 embodiment of Lee is clearly talking about asynchronous memory. We
18 talked about, and I think my friend conceded, that the embodiment of Figure
19 3 is about asynchronous memory.

20 There are two other embodiments, Figure 4 and Figure 5, they both
21 also use asynchronous memory, just like Figure 3. Indeed, the discussion in
22 the specification of Lee, as both of those makes clear, that the only
23 differences really have to do with the bus organization that you have
24 between the memory and the controller and whether you have multiple buses
25 or different buses or memory data transfer and signaling and command
26 structures, but they all, in fact each paragraph that discusses those

1 embodiments actually says that the reference to memory 120, and the
2 specification refers to memory 120 prime or 120 double prime in these later
3 examples, is that in all other respects it's the same as memory 120 in the
4 original embodiment that was discussed for Figure 3.

5 So this is just -- so Figure 4, that discussion is at paragraph 36 of Lee,
6 Figure 5 is in paragraph 37, and they both make the same point, that the
7 memory is the same except for the specific things that are called out, which
8 as I said all have to do with the bus interface structure. And the fact that Lee
9 is talking about different buses I think belies the point that Petitioner was
10 arguing a few moments ago that there's really no other changes that you
11 would make between synchronous and asynchronous. Obviously there are a
12 lot of design choices that one makes, and there's really no showing that just
13 all you would do is add a clock and suddenly this Lee reference would work
14 in this magical synchronous way that would be beneficial in some
15 unspecified manner.

16 Similarly, I don't think there's much to the argument that there's a
17 claim of Lee that doesn't expressly limit itself to asynchronous memory.
18 This is in reference to Claim 5 in the Lee reference. It's still a part of the
19 Lee reference where everything in the reference is teaching about
20 asynchronous memory. The title, the figures, all the examples, every
21 embodiment, and the entire purpose of the invention as described in Lee is to
22 achieve these power saving benefits in an asynchronous memory but using
23 this different signaling technique for source synchronous interaction. And I
24 think we agree with counsel for Petitioner that source synchronous does not
25 refer to synchronous memory, that's a different thing.

1 JUDGE TROCK: Counsel, so this is Judge Trock again, but you
2 would agree with us that we don't have to look to Lee to find the rationale to
3 combine these two references, right?

4 MR. LEDAHL: You don't have to look to Lee alone, but certainly
5 you have to understand Lee and look at its teaching and whether it's
6 teaching against and teaching away from the combination. So you're right,
7 you don't, Lee is not obviously the only person that a person of skill in the
8 art might take motivation, but the only other source that's being pointed to is
9 essentially the JEDEC standard and the mere existence of synchronous
10 memories in the world. It's not at all clear how any of those constitute a
11 motivation to modify Lee in the way argued by Petitioner.

12 I'm happy to address other questions, but I think we've gotten at the
13 crux of what I think the issues are here and I don't want to take the Board's
14 time unnecessarily. But like I said, if there are questions or anything else
15 you want me to clarify I'm happy to do so.

16 JUDGE TROCK: Well hearing nothing, you've got about 10 minutes
17 left in your principle argument, but if you're done we can go back over to
18 Petitioner and see what he has to say.

19 MR. LEDAHL: I think that's fine, I don't need to belabor, we
20 discussed all the points that I wanted to cover with the Board.

21 JUDGE TROCK: Thank you. So Mr. O'Dell, you've got about three
22 minutes left for your rebuttal.

23 MR. O'DELL: All right, so I'm going to share my screen again and I
24 have it on slide 16 of the presentation, and slide 16 is showing two claims
25 from Lee, Claim 5, a system comprising a memory, and Claim 12, a system
26 comprising an asynchronous memory. Lee certainly knows the difference in

1 these terms, claims are very exact use of terminology, and Lee is clear in this
2 example that his invention of source synchronous with the turnaround strobe
3 works in generally in memory. And memory either has or doesn't have a
4 clock, it's either asynchronous or synchronous, at least in this regard and the
5 discussion of Lee those are kind of the two types of memory being
6 discussed, synchronous and asynchronous.

7 So Lee, the argument being presented by Patent Owner was Lee
8 teaches away from or it goes against its inventive concept to use
9 synchronous memory, and in fact that's not correct. So here on slide 16 is
10 just one example, on slide 15 of the presentation, it's from the detailed
11 description of Lee, and he's talking about source synchronous interface, and
12 in this example he incorporates by reference a synchronous memory device
13 system that has a source synchronous interface. And this citation to the 159
14 Patent here describes transmitting control signals using a common clock
15 protocol, so that would be a synchronous, in order to increase the bandwidth
16 of transmitting data, and that is the primary argument that we presented in
17 the petition of why one would be motivated to add a clock. It is certainly a
18 balance of design choices, adding a clock to get higher bandwidth, or not
19 having a clock which may or may not, which may reduce power
20 consumption.

21 JUDGE McKONE: I have a quick question, please. What is your
22 best evidence that the combination of Lee with JEDEC would result in
23 higher bandwidth?

24 MR. O'DELL: Well here in Lee itself, since the 159 Patent is
25 incorporated by reference into Lee, in Lee itself he recognizes that using a
26 common clock protocol provides, increases the bandwidth of transmitting

1 data. So that's one piece of evidence. The second piece of evidence was the
2 Prince textbook which was discussed in the petition and it says that the
3 synchronous interface, which is adding a clock instead of a strobe signal,
4 provides higher bandwidth, that is page five of the -- here. It is on slide 10
5 of my presentation which is showing the Prince textbook, prior art textbook
6 at page five and here, the very first sentence, new interface architectures are
7 also being used to improve the bandwidth of the RAMs, the memories. The
8 most common is the synchronous interface. And then it explains why
9 making something synchronous puts the memory system under the control
10 of the system clock and wait states are reduced, but by having it under the
11 control of the system clock. So that's the answer.

12 JUDGE TROCK: Mr. O'Dell, this is Judge Trock, so you're out of
13 time.

14 MR. O'DELL: Thank you very much for your time.

15 JUDGE TROCK: Patent Owner, anything you'd like to add?

16 MR. LEDAHL: Yes, I think two things particularly about what we
17 just heard about this incorporation by reference argument and the 150 Patent
18 that counsel was referencing. First of all, I just searched, while he was
19 talking, the petition, I can't find any reference to that 159 Patent anywhere in
20 the petition, I don't think it was every discussed, certainly I don't think it
21 was ever discussed as part of a motivation to combine. The suggestion that
22 that was in the petition I don't think it accurate. It also isn't supportive.
23 The 159 Patent that's referenced in the specification of Lee isn't Lee's
24 invention or Lee's disclosure, it's a reference to what source synchronous
25 transfer is, and that's what Lee says it's incorporating it for, not to convert
26 Lee's applications from asynchronous to synchronous memory after Lee

1 repeatedly teaches the use of asynchronous memory and the advantages for
2 the applications it discusses of using asynchronous memory.

3 And finally, I think this suggestion about Claim 5 that my friend
4 discussed is similar misplaced. As I said, there's nothing in Claim 5 that
5 makes reference to or refers in any way to a synchronous memory or to a
6 clock signal. It's an argument that there's somehow inclusion by absence,
7 that the fact that the claim doesn't talk about these things somehow means
8 that it includes them. That's not a teaching and that's certainly not support
9 for this combination that's being proposed. Again, I'm happy to answer any
10 questions, but I don't need to use all of the time available.

11 JUDGE TROCK: Okay, thank you. we appreciate your time to
12 address these issues with us, Counsel, this has been very helpful. Please stay
13 on the line if the court reporter has any questions for you with regard to
14 spelling, and with that, the case has been submitted to us and we are
15 adjourned. Thank you very much for your time.

16 (Whereupon, the above-entitled matter went off the record at 1:59
17 p.m.)

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