

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

LONGITUDE LICENSING LTD.,
Patent Owner.

IPR2023-01200
Patent 7,697,369 B2

Before RICHARD M. LEBOVITZ, DAVID C. McKONE, and
KEVIN C. TROCK, *Administrative Patent Judges*.

TROCK, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

We have authority to hear this *inter partes* review under 35 U.S.C. § 6. This Final Written Decision issues pursuant to 35 U.S.C. § 318(a) (2018) and 37 C.F.R. § 42.73 (2019). For the reasons discussed herein, we determine that Petitioner, Western Digital Technologies, Inc. (“Petitioner”) has shown by a preponderance of the evidence that claims 1, 2, 6, 7, 10, 11, 14–19, and 25–27 (the “challenged claims”) of U.S. Patent No. 7,697,369 B2 (Ex. 1001, “the ’369 patent”) are unpatentable. *See* 35 U.S.C. § 316(e) (2018); 37 C.F.R. § 42.1(d) (2019).

II. BACKGROUND

A. Procedural History

Petitioner filed a Petition (Paper 2, “Pet.” or “Petition”) requesting *inter partes* review of the challenged claims. Longitude Licensing LTD. (“Patent Owner”) (Paper 4, 1) did not file a Preliminary Response. Based on the record at that time, we issued a Decision granting *inter partes* review. Paper 6 (“Dec.” or “Institution Decision”).

After institution, Patent Owner filed a Response (Paper 16, “PO Resp.” or “Resp.”), Petitioner filed a Reply (Paper 20, “Pet. Reply” or “Reply”), and Patent Owner filed a Sur-reply (Paper 22, “PO Sur-reply” or “Sur-reply”).

On October 23, 2024, an oral hearing was held. A transcript of the hearing is made part of the record. Paper 28.

B. Related Matters

Petitioner identifies the following district court proceedings involving the ’369 patent:

1. *Longitude Licensing Limited v. ASUSTeK Computer Inc. et al.*, Case No. 8-23-cv-00033 (C.D. Cal.) (filed Jan. 9, 2023).
2. *Longitude Licensing Limited v. Lenovo Group Limited et al.*, Case No. 8-23-cv-00035 (C.D. Cal.) (filed Jan. 9, 2023).
3. *Longitude Licensing Limited v. Acer Inc. et al.*, Case No. 8-23-cv-00036 (C.D. Cal.) (filed Jan. 9, 2023).
4. *Longitude Licensing Limited v. HP Inc.*, Case No. 8-23-cv-00038 (C.D. Cal.) (filed Jan. 9, 2023).
5. *Longitude Licensing Limited v. Amazon.com, Inc.*, Case No. 8-23-cv-00039 (C.D. Cal.) (filed Jan. 9, 2023) (“Amazon Action”).
6. *Longitude Licensing Limited v. Dell Technologies Inc. et al.*, Case No. 8-22-cv-02312 (C.D. Cal.) (filed Dec. 23, 2022¹).
Pet. 69–70.

Each of the above actions (with the exception of the Amazon Action with respect to Petitioner) is stayed pending the resolution of the Amazon Action. Ex. 1011.

Patent Owner identifies the same six related matters. Paper 4, 1–2.

C. Real Parties-in-Interest

Petitioner identifies Western Digital Technologies, Inc., as the real party-in-interest. Pet. 68. Petitioner states that (1) the six cases identified above involve Petitioner’s customers as defendants, (2) Petitioner submits that Petitioner is the only real party-in-interest (“RPI”), and (3) “regardless of whether any defendant should be named as an RPI, no RPI analysis is

¹ Petitioner incorrectly identified the filing date as Dec. 23, 2023.

necessary because there are no time bar or estoppel implication for any defendant.” *Id.*

Patent Owner identifies Longitude Licensing LTD. as the real party-in-interest. Paper 4, 1.

D. The '369 Patent

The '369 patent is entitled “System with Controller and Memory.” Ex. 1001, code (54). The patent “relates to a system having a controller and a memory and, more particularly, to a data sending/receiving operation between the controller and the memory.” *Id.* at 1:6–8.

The '369 patent explains that “[i]n a conventional data sending/receiving operation between the controller and the memory, either the controller or the memory who serves as a sender generates a data strobe signal which is synchronized with a clock signal.” *Id.* at 1:9–12. The patent further explains “[i]t is an object of the ['369] invention to provide a system based on a new protocol which is different from the above-described conventional techniques.” *Id.* at 1:25–27.

Figure 1 of the '369 patent, reproduced below, is a schematic block diagram of a system according to one embodiment. *Id.* at 2:12–14.

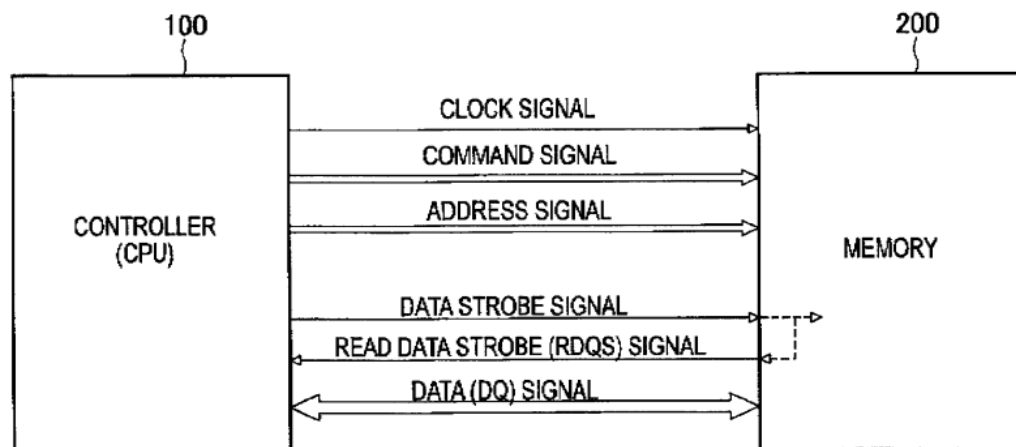


Figure 1, shown above, depicts controller 100 and memory 200. *Id.* at 3:6–11. Controller 100 outputs a clock signal, command signal, and address signal to memory 200. *Id.* Controller 100 also outputs and receives data (DQ) signal to/from memory 200. *Id.*

In a write operation, controller 100 sends out a first data strobe signal and also sends out a write data signal over the DQ signal line, as shown in Figure 1, above. *See id.* at 3:12–25. In a write operation, memory 200 receives the write data signal in synchronization with the first data strobe signal. *Id.*

In a read operation, controller 100 sends out a second data strobe signal and receives a read data signal over the DQ signal line in synchronization with a read data strobe (RDQS) signal. *Id.* The RDQS signal corresponds to the second data strobe signal. *Id.* The '369 patent explains that “memory 200 is adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal and to send out the read data signal synchronized with the read data strobe signal.” *Id.*

The '369 patent describes the following advantages:

In the system according to the first embodiment, the write/read operations to/from the memory 200 are controlled by the data strobe signal outputted from the controller 100. The write and the read operations can be carried out without the use of and independently from the clock signal. Therefore, it is not necessary for the memory 200 to produce the data strobe signal from the clock signal nor to make the read data strobe signal synchronize with the clock signal.

Id. at 3:37–44.

E. Illustrative Claim

The '369 patent has 27 claims. Claims 1, 6, 10, and 26 are the independent claims challenged. Claim 1 is illustrative of the claimed subject matter and is reproduced below, with bracketed annotations added:

1. [1.0] A system comprising:
 - [1.1] a controller adapted to send out a first data strobe signal and a write data signal in a write operation, [1.2] the write data signal being synchronized with the first data strobe signal, [1.3] the controller being adapted, in a read operation, to send out a second data strobe signal and to receive a read data signal in synchronization with a read data strobe signal, [1.4] the read data strobe signal being received by the controller in response to the second data strobe signal; and
 - [1.5] a memory adapted to receive the write data signal in synchronization with the first data strobe signal in the write operation, [1.6] the memory being adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal and to send the read data signal synchronized with the read data strobe signal.

Ex. 1001, 8:15–30.

F. Prior Art References and Other Evidence

Petitioner relies on the following references:

1. Lee, US Patent Application Publication No. 2004/0022095 A1 (February 5, 2004), (Ex. 1005, “Lee”).

2. JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79C, March 2003,² (Ex. 1007, “JEDEC”).

In addition to these references, Petitioner relies on a Declaration of R. Jacob Baker, Ph.D. Ex. 1003. Patent Owner relies on a Declaration of Bruce Jacob, Ph.D. Ex. 2003.

G. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability. Pet. 16.

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 6, 10, 14, 15, 16, 17, 18, 19, 25, 26, 27	103(a) ³	Lee
2, 7, 11	103(a)	Lee, JEDEC

III. ANALYSIS

A. Applicable Legal Standards

A claim is unpatentable as obvious under 35 U.S.C. § 103(a) “if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a) (2006). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level

² Petitioner asserts that JEDEC (Ex. 1007) was created March 31, 2003 and was publicly available as of at least June 9, 2003. Pet. 16–17. Patent Owner does not contest the date of JEDEC’s public availability.

³ Because the application from which the ’369 patent issued was filed before March 16, 2013 (Ex. 1001, code (22)), citations to 35 U.S.C. § 103 are to the pre-AIA version. Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29.

of skill in the art; and (4) so-called “secondary considerations,” including commercial success, long-felt but unsolved needs, failure of others, and unexpected results. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Neither party has presented any evidence on the fourth *Graham* factor.

B. Level of Ordinary Skill in the Art

According to Petitioner, a person of ordinary skill in the pertinent art would have had a working knowledge of the memory system art that is pertinent to the ’369 patent, including memory systems and memory controllers. A [person of ordinary skill in the art] would have had a bachelor’s degree in electrical engineering, or an equivalent, and approximately two years of professional experience relating to field of memory systems. Lack of professional experience can be remedied by additional education, and vice versa.

Pet. 15 (citing Ex. 1003 ¶¶ 18–20). Patent Owner does not challenge Petitioner’s description of someone of ordinary skill. PO Resp. 12; *see also* Ex. 2003 ¶ 21.

The parties agree on a description of a person of ordinary skill in the art, and this description appears consistent with the subject matter of the ’369 patent and the asserted prior art. We, therefore, continue to use the same description that we adopted in our Institution Decision, as it is consistent with the challenged patent and the asserted art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (the prior art itself may reflect an appropriate level of skill).

C. Claim Construction

For this *inter partes* review, the Board applies the same claim construction standard as that applied in federal courts. *See* 37 C.F.R. § 42.100(b) (2023). Under this standard, claim terms “are generally given their ordinary and customary meaning” as understood by a person of

ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc) (citations omitted). “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Extrinsic evidence is “less significant than the intrinsic record in determining ‘the legally operative meaning of claim language.’” *Phillips*, 415 F.3d at 1317.

Petitioner contends that no claim terms require express construction. Pet. 15 (citing Ex. 1003). Patent Owner agrees that no express construction of any claim term is necessary. PO Resp. 12.

We agree with the parties that no claim terms require express construction. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017); *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (only those terms that are in controversy need be construed, and only to the extent necessary to resolve the controversy). We therefore use the ordinary and customary meaning of the claim terms as would be understood by a person of ordinary skill in the art at the time of the claimed invention.

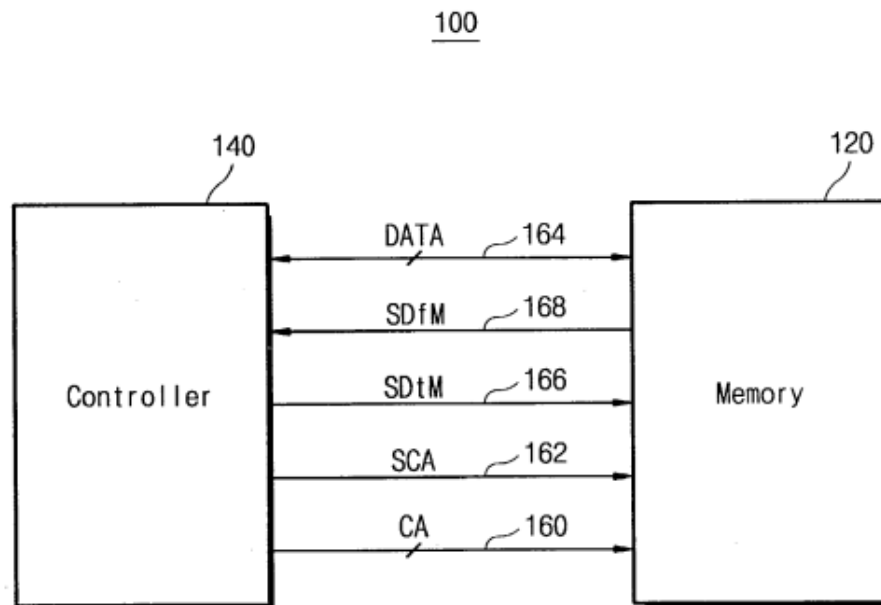
D. Prior Art References

1. Lee (Ex. 1005)

Lee is a patent application publication titled “Asynchronous Memory Using Source Synchronous Transfer and System Employing the Same.” Ex. 1005, code (54). Lee “is related to electronic devices, and, in particular,

to a system that performs data transmission between a memory and a memory controller.” *Id.* ¶ 2.

Lee’s Figure 1, reproduced below, is a block diagram of systems according to embodiments of the Lee invention. *Id.* ¶ 11.



Lee’s Figure 1, shown above, depicts memory system 100 which includes memory 120 and memory controller 140. *Id.* ¶ 17.

Lee explains that

memory controller 140 sends command/address information CA for a read/write operation to the memory 120 via a control bus 160. The memory controller 140 sends the first strobe signal SCA as a transmission reference or synchronous signal to the memory 120 via a signal line 162. That is, the command/address information CA is transferred to the memory 120 from the memory controller 140 together with the first strobe signal SCA based on the source synchronous interface.

Id. ¶ 19. Lee explains that “[a] source synchronous interface is an interface where data is sent from a transmitter to a receiver together with a clock

signal, which is used within a receive interface to latch the accompanying data.” *Id.* ¶ 18.

In a write operation, controller 140 transfers data DATA to memory 120 via data bus 164 and transfers, as a source synchronous signal, second strobe signal SDtM to memory 120 via signal line 166. *Id.* ¶ 20. Memory 120 latches the write data DATA in response to the second strobe signal SDtM. *Id.*

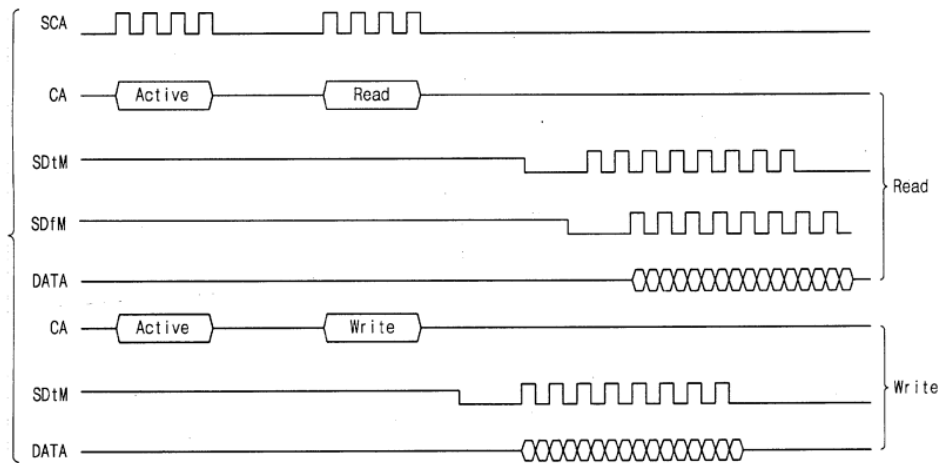
In a read operation, Lee’s system works as follows:

For a read operation, in addition to the command/address information CA, the memory controller 140 transfers to the memory 120 the second strobe signal SDtM as a transmission synchronous or reference signal at a time when it wants to receive data read out from the memory 120. The memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM. The read data that is read from the memory 120 is sent to the memory controller 140 together with the third strobe signal SDfM.

Id. ¶ 21.

Lee’s Figure 2, reproduced below, is a timing diagram of data transmission operations according to embodiments of the Lee invention.

Id. ¶ 12.



Lee's Figure 2, shown above, depicts read and write signal transmission operations between memory controller 140 and memory 120. *Id.* ¶¶ 24–26. During a write operation where data is written to memory 120, Lee explains that

first, an active command Active' (e.g., a row address) is sent to the memory controller 140 from the memory 120. The active command Active' is sent to the memory 120 by the memory controller 140 toggling the first strobe signal SCA during a predetermined time, for example, when the active command Active' is on the control bus 160 (illustrated as CA in FIG. 2). That is, the memory controller 140 loads the active command Active' on the control bus 160 and toggles the first strobe signal SCA while the command is on the control bus 160. The memory 120 latches the active command Active' in response to toggling of the first strobe signal SCA. The memory controller 140 subsequently loads the write command Write (e.g., a column address) on the control bus 160 and toggles the first strobe signal SCA while the write command Write is on the control bus 160. The memory 120 latches the write command Write in response to toggling of the first strobe signal SCA.

Id. ¶ 26.

Similarly, with respect to a read operation, Lee explains that data stored in a memory cell array (not shown) is read out via a read circuit (e.g., a sense amplifier circuit). The read data is transferred to the memory controller 140 from the memory 120 via a data bus 166, based on the control of the memory controller 140. To send data read from the memory 120 to the memory controller 140, first, the memory controller 140 transfers the second strobe signal SDtM to the memory 120. The memory 120 generates the third strobe signal SDfM in response to the received second strobe signal SDtM. The third strobe signal SDfM, as illustrated in FIG. 2, may have the same waveform as the second strobe signal SDtM delayed by a predetermined time. The memory 120 loads data on the data bus 166 (illustrated as DATA in FIG. 2) in response to the second strobe signal SDtM and outputs the third strobe signal

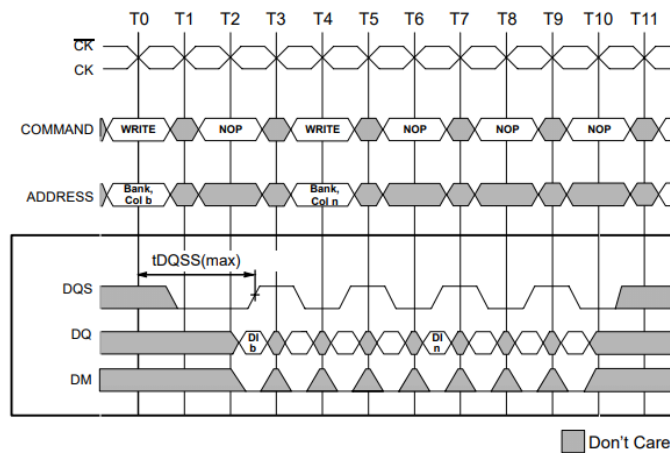
SDfM while the data is loaded on the data bus 166. The memory controller 140 latches data DATA loaded on the data bus 166 in response to the third strobe signal SDfM.

Id. ¶ 25.

2. *JEDEC (Ex. 1007)*

JEDEC is a standard of the Joint Electron Device Engineering Council entitled Double Data Rate (DDR) SDRAM Specification. Ex. 1007, 1; Ex. 1003 ¶ 104. A DDR SDRAM is a high-speed dynamic random-access memory. Ex. 1007, 7. JEDEC states that “JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Council level and subsequently reviewed and approved by the EIA [Electronic Industries Alliance] General Counsel.” *Id.* at 1–2.

JEDEC Figure 22, reproduced below, is a timing diagram for WRITE bursts. *Id.* at 37, 40.



JEDEC Figure 22, shown above, depicts clock CK and command and address signals. *Id.* at 7, 40.

E. Obviousness Based on Lee (Ground 1)

Petitioner contends that Lee would have rendered claims 1, 6, 10, 14–19, and 25–27 obvious under 35 U.S.C. § 103(a). Pet. 16. Claims 1, 6, 10,

and 26 are independent. To prove its contentions, Petitioner provides a detailed claim analysis, supported by the testimony of Dr. Baker. *See id.* at 20–57; Ex. 1003 ¶¶ 41–102.

Patent Owner does not contest Petitioner’s evidence or arguments with respect to the obviousness of claims 1, 6, 10, 14–19, and 25–27. *See* PO Resp. 1, 13–21. We consider Petitioner’s uncontested evidence and arguments with respect to the independent claims first.

1. Independent Claim 1

a) [1.0] A system comprising:

For the preamble of claim 1, Petitioner asserts that “Lee describes a system for data transmission between [a] controller and a memory.” Pet. 26–27 (citing Ex. 1005 ¶ 2). According to Petitioner, “Lee further describes ‘a memory system 100 . . . [that] includes a memory 120 and a memory controller 140.’” Pet. 27 (citing Ex. 1005 ¶ 17). “[B]ecause Lee describes a memory system that performs data transmission between a memory and a memory controller,” Petitioner asserts, “Lee renders obvious a ‘*system*’ as claimed.” Pet. 27 (citing Ex. 1003 ¶¶ 45–46).

Petitioner relies on the testimony of Dr. Baker to support its assertions, which we credit. *See* Ex. 1003 ¶¶ 45–46. Patent Owner does not contest Petitioner’s evidence and arguments. *See* PO Resp. 1, 13–21.

Based on the complete record, we find that Petitioner has established that Lee’s description of a system that performs data transmission between a memory and a memory controller meets the recited subject matter of claim 1’s preamble.

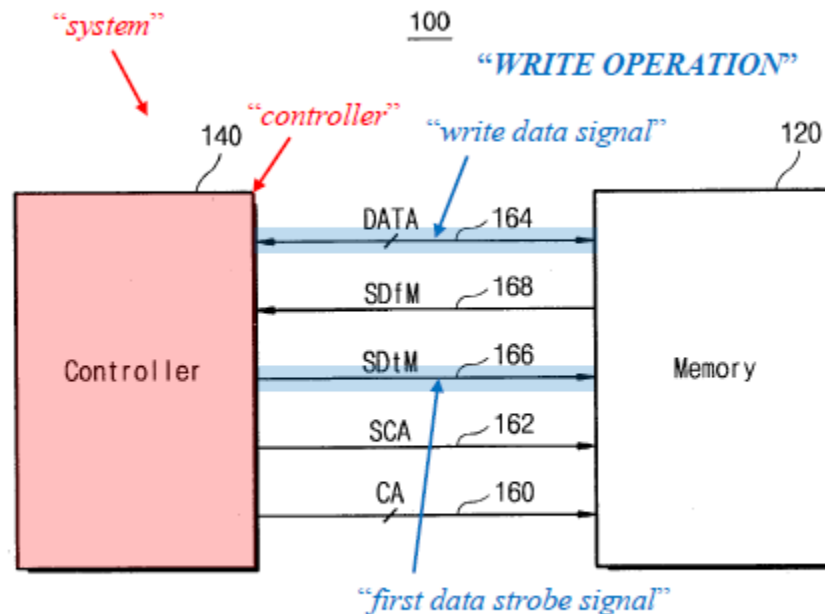
b) [1.1] a controller adapted to send out a first data strobe signal and a write data signal in a write operation,

For this limitation, Petitioner asserts that “Lee’s system includes a controller 120 (‘controller’): ‘[A] memory system 100 according to particular embodiments the present invention includes a memory 120 and a memory controller 140.’” Pet. 28 (citing Ex. 1005 ¶ 17) (alteration in original). Petitioner explains that

Lee describes a write operation in which the controller transmits strobe signal SDtM (“first data strobe signal”) over line 166 and data (“write data signal”) over line 164. Lee explains that during a write operation, “the memory controller 140 transfers data DATA to the memory 120 via a data bus 164, and transfers, as a transmission synchronous signal, the second strobe signal SDtM to the memory 120 via a signal line 166.”

Pet. 28 (citing Ex. 1005 ¶ 20).

Petitioner provides annotated Figure 1 from Lee, shown below. Pet. 28.



EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 48.

Petitioner's annotated Figure 1 from Lee, shown above, is a block diagram depicting controller 140 in communication with memory 120. Pet.

29. According to Lee, during a write operation

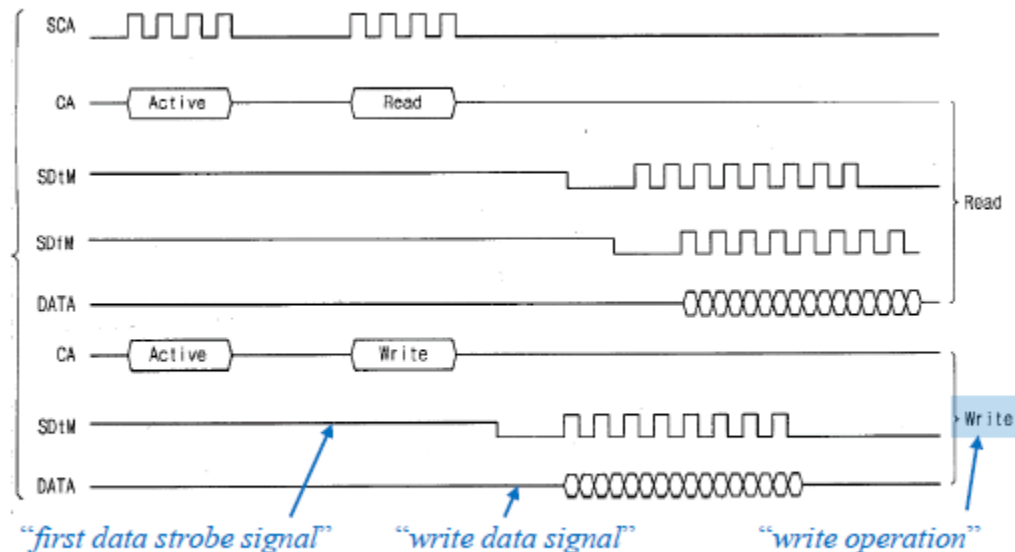
memory controller 140 transfers data DATA to the memory 120 via a data bus 164, and transfers, as a transmission synchronous signal, the second strobe signal SDtM to the memory 120 via a signal line 166. In particular, for a write operation, the write data DATA is sent to the memory 120 from the memory controller 140 together with the second strobe signal SDtM based on the source synchronous interface. The memory 120 latches the write data DATA in response to the second strobe signal SDtM.

Ex. 1005 ¶ 20. Petitioner identifies (in blue) SDtM 166 as the recited “first data strobe signal” and DATA 164 as the recited “write data signal.” Pet.

29.

Petitioner also provides annotated Figure 2 from Lee, shown below.

Pet. 30.



EX1005, Lee, Fig. 2 (annotated); EX1003, ¶ 49.

Petitioner's annotated Figure 2 from Lee, shown above, is a timing diagram of data transmission operations depicting read and write operations. Petitioner identifies (in blue) SDtM as the recited "first data strobe signal" and DATA as the recited "write data signal" for the recited "write operation." Pet. 30. According to Petitioner, in Lee "[d]uring the write operations, 'data to be written is then sent from the memory controller 140 to the memory 120. Data transmission is accomplished by toggling the second strobe signal SDtM.'" Pet. 30 (citing Ex. 1005 ¶ 27).

"Thus," Petitioner argues, "because Lee describes a controller 140 that transmits a strobe signal SDtM and a data signal over lines 166 and 164 respectively, Lee renders obvious '*a controller adapted to send out a first data strobe signal and a write data signal in a write operation*' as claimed." Pet. 30 (citing Ex. 1003 ¶¶ 47–50).

Petitioner relies on the testimony of Dr. Baker to support its assertions, which we credit. *See* Ex. 1003 ¶¶ 47–50. Patent Owner does not contest Petitioner's evidence and arguments. *See* PO Resp. 1, 13–21.

Based on the complete record, we find that Petitioner has established that Lee's description of memory controller 140 transferring data to memory 120 via data bus 164 and transferring strobe signal SDtM to memory 120 via signal line 166 during a write operation meets the recited "*controller adapted to send out a first data strobe signal and a write data signal in a write operation,*" of claim 1.

c) [1.2] *the write data signal being synchronized with the first data strobe signal,*

For this limitation, Petitioner asserts "Lee explains that the data signal is synchronous with the data strobe signal SDtM: 'For a write operation . . . the memory controller 140 transfers data DATA to the memory 120 via a

data bus 164, and transfers, *as a transmission synchronous signal*, the second strobe signal SDtM to the memory 120 via a signal line 166.” Pet. 30–31 (citing Ex. 1005 ¶ 20).

Petitioner argues that a person of ordinary skill in the art “would have further recognized that the very purpose of a strobe signal is to instruct the receiving system when to sample the transmitted data.” Pet. 31 (citing Ex. 1005 ¶ 27 (“The memory 120 latches the write data DATA in response to the second strobe signal SDtM”)). Petitioner asserts that “Lee’s asynchronous memory still uses strobe signals that are synchronized with their corresponding data signals.” *Id.* According to Petitioner, a person of ordinary skill in the art “would have thus understood that the strobe signal is synchronized with the data signal.” *Id.*

“Thus,” Petitioner argues, “because Lee describes the strobe signal as a transmission synchronous signal, Lee renders obvious ‘*the write data signal being synchronized with the first data strobe signal*’ as claimed.” Pet. 31 (citing Ex. 1003 ¶¶ 51–52).

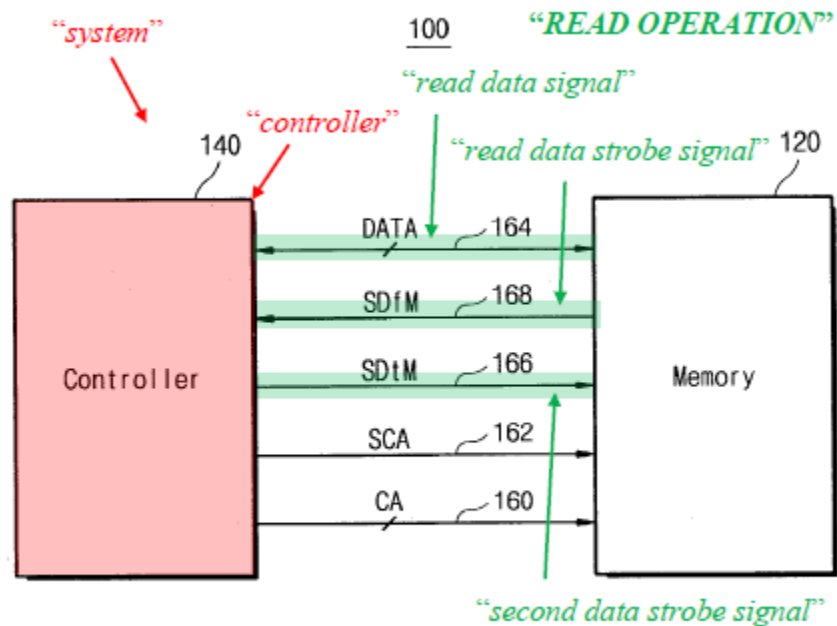
Petitioner relies on the testimony of Dr. Baker to support its assertions, which we credit. *See* Ex. 1003 ¶¶ 51–52. Patent Owner does not contest Petitioner’s evidence and arguments. *See* PO Resp. 1, 13–21.

Based on the complete record, we find that Petitioner has established that Lee’s description of a write operation where memory controller 140 transfers data to memory 120 via data bus 164, and transfers as a transmission synchronous signal, strobe signal SDtM to memory 120 via signal line 166 meets the recited “*write data signal being synchronized with the first data strobe signal*,” of claim 1.

d) [1.3] the controller being adapted, in a read operation, to send out a second data strobe signal and to receive a read data signal in synchronization with a read data strobe signal,

For this limitation, Petitioner asserts that “Lee describes a read operation in which the memory transmits strobe signal SDfM (*‘read data strobe signal’*) over line 168 and data (*‘read data signal’*) over line 164 in response to the SDtM signal (*‘second data strobe signal’*).” Pet. 31–32. According to Petitioner, “Lee explains that during a read operation, ‘the memory controller 140 transfers to the memory 120 the second strobe signal SDtM as a transmission synchronous or reference signal at a time when it wants to receive data read out from the memory 120.’” *Id.* at 32 (quoting Ex. 1005 ¶ 21). Petitioner argues that “Lee’s controller thus *‘send[s] out a second data strobe signal.’*” Pet. 32. Petitioner explains that “[t]he controller then receives data in synchronization with a read strobe signal: ‘Therefore, during the read operation the memory controller 140 receives the read data DATA from the memory 120 together with the third strobe signal SDfM at a required time,’” as Petitioner asserts that SDfM is the recited *“read data strobe signal.”* Pet. 32 (quoting Ex. 1005 ¶ 21). “Lee’s controller,” Petitioner argues, “thus *‘receive[s] a read data signal in synchronization with a read data strobe signal.’*” Pet. 32.

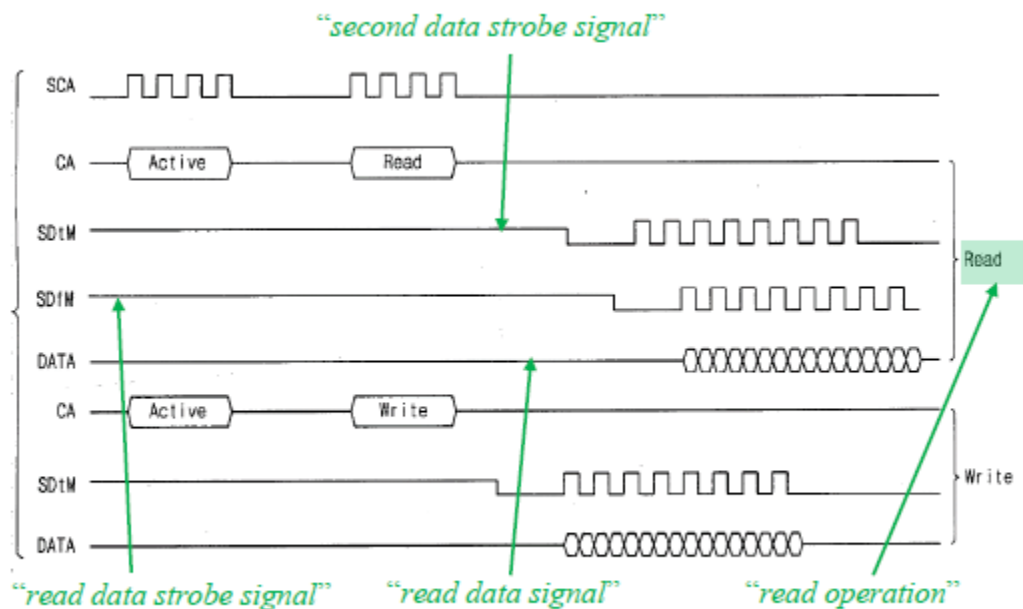
To illustrate this operation, Petitioner provides an annotated Figure 1 from Lee, shown below. Pet. 33.



EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 53.

Petitioner's annotated Figure 1 from Lee, shown above, is a block diagram depicting controller 140 in communication with memory 120 during a "read operation." Pet. 33. Petitioner identifies (in green) SDtM 166 as the recited "second data strobe signal," SDfM 168 as the recited "read data strobe signal," and DATA 164 as the recited "read data signal." *Id.*

Petitioner also provides an annotated Figure 2 from Lee, shown below. Pet. 34.

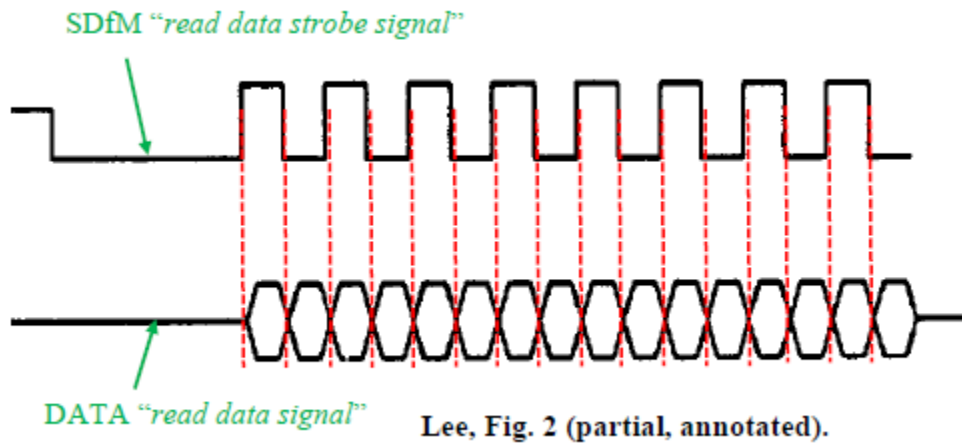


EX1005, Lee, Fig. 2 (annotated); EX1003, ¶ 54.

Petitioner’s annotated Figure 2 from Lee, shown above, is a timing diagram of data transmission operations depicting read and write operations. Petitioner identifies (in green) SDtM as the recited “second data strobe signal,” SDfM as the recited “read data strobe signal,” and DATA as the recited “read data signal” for the recited “read operation.” Pet. 34.

Petitioner points out that “Lee’s read operations are described as ‘conventional read operations.’” Pet. 34 (citing Ex. 1005 ¶ 25). According to Petitioner, “[s]uch conventional read operations include the memory generating the strobe signal SDfM (‘read data strobe signal’) in response to receipt of the strobe signal SDtM (‘second data strobe signal’).” Pet. 34. According to Petitioner, Lee explains that “[t]o send data read from the memory 120 to the memory controller 140, first, the memory controller 140 transfers the second strobe signal SDtM to the memory 120. The memory 120 generates the third strobe signal SDfM *in response* to the received second strobe signal SDtM.” Pet. 34 (quoting Ex. 1005 ¶ 25).

Dr. Baker testifies that “the SDfM signal (*‘read data strobe signal’*) is in synchronization with the read data signal.” Ex. 1003 ¶ 57. To illustrate this, Dr. Baker provides an annotated, partial view of Lee’s Figure 2, shown below. *Id.*



Dr. Baker’s annotated, partial view of Lee’s Figure 2, shown above, identifies (in green) SDfM as the recited “read data strobe signal,” and DATA as the recited “read data signal,” showing that “the rising and falling times of the strobe signal SDfM are synchronized with the switching of the data signal.” *Id.*

Based on this figure, Dr. Baker testifies that a person of ordinary skill in the art “would have understood that the SDfM signal is ‘*in synchronization with*’ the read DATA signal,” and such a person “would have understood that synchronization is done for the purpose of telling the receiving component—in this case the memory—when to sample the data.” Ex. 1003 ¶ 58 (citing Ex. 1005 ¶ 25).

“Thus,” Petitioner argues,

because Lee describes that during a read operation, the memory sends a data signal and a data strobe signal (which are synchronized) responsive to a signal from the controller, Lee

renders obvious ‘*the controller being adapted, in a read operation, to send out a second data strobe signal and to receive a read data signal in synchronization with a read data strobe signal*’ as claimed.

Pet. 36 (citing Ex. 1003 ¶¶ 53–59).

Petitioner’s arguments are supported by the testimony of Dr. Baker, which we credit. *See* Ex. 1003 ¶¶ 53–59. Patent Owner does not contest Petitioner’s evidence and arguments. *See* PO Resp. 1, 13–21.

Based on the complete record, we find that Petitioner has established that Lee’s description of a read operation where memory controller 140 transfers to memory 120 strobe signal SDtM as a transmission synchronous or reference signal at a time when it wants to receive data read out from memory 120; where memory 120 generates strobe signal SDfM in response to the received strobe signal SDtM; and memory controller 140 receives read data DATA from memory 120 together with strobe signal SDfM, meets the recited “*controller being adapted, in a read operation, to send out a second data strobe signal and to receive a read data signal in synchronization with a read data strobe signal,*” of claim 1.

e) [1.4] *the read data strobe signal being received by the controller in response to the second data strobe signal;*

For this limitation, Petitioner points out that “Lee explains that the SDfM signal is received by the controller in response to transmitting the SDtM signal: ‘The memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM.’” Pet. 37 (quoting Ex. 1005 ¶ 21); *see also* Ex. 1005 ¶ 24. “Thus,” Petitioner argues, “because Lee’s strobe signal SDfM is received in response to the strobe signal SDtM, Lee renders obvious ‘*the read data strobe signal being received by the*

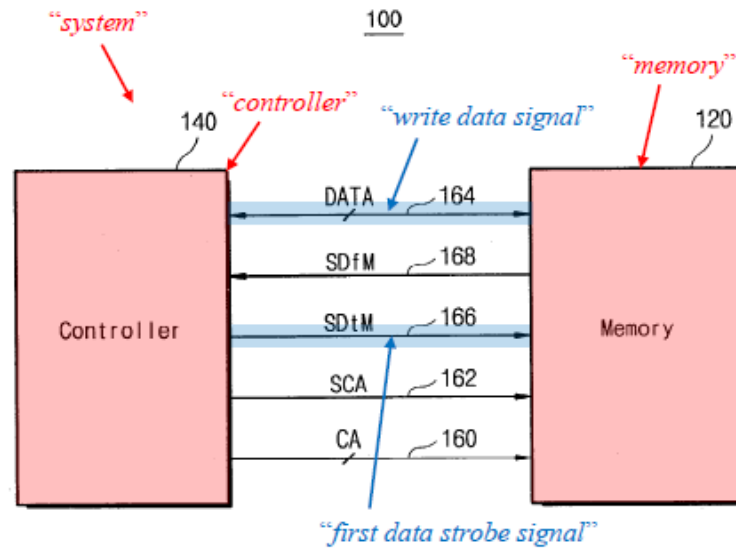
controller in response to the second data strobe signal” as claimed. Pet. 37 (citing Ex. 1003 ¶¶ 60–61).

Petitioner’s arguments are supported by Dr. Baker’s testimony, which we credit. *See* Ex. 1003 ¶¶ 60–61. Patent Owner does not contest Petitioner’s evidence and arguments. *See* PO Resp. 1, 13–21.

Based on the complete record, we find that Petitioner has established that Lee’s description of memory controller 140 transferring strobe signal SDtM to memory 120, wherein memory 120 generates strobe signal SDfM in response to received strobe signal SDtM meets the recited “*read data strobe signal being received by the controller in response to the second data strobe signal,*” of claim 1.

f) [1.5] *a memory adapted to receive the write data signal in synchronization with the first data strobe signal in the write operation,*

For this limitation, Petitioner asserts that Lee describes a “write operation in which the memory receives strobe signal SDtM (*‘first data strobe signal’*) over line 166 and data (*‘write data signal’*) over line 164.” Pet. 38. To illustrate this operation, Petitioner provides an annotated version of Lee’s Figure 1, shown below. *Id.*



EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 62.

Petitioner's annotated Figure 1 from Lee, shown above, is a block diagram depicting controller 140 in communication with memory 120. Petitioner identifies (in blue) SDtM 166 as the recited "first data strobe signal" and DATA 164 as the recited "write data signal." *Id.*

Lee explains in particular that "[f]or a write operation . . . memory controller 140 transfers data DATA to the memory 120 via a data bus 164, and transfers, as a transmission synchronous signal, the second strobe signal SDtM to the memory 120 via a signal line 166." Ex. 1005 ¶ 20.

"Thus," Petitioner argues, "because Lee describes a memory that receives the write data signal along with a strobe signal, Lee renders obvious '*a memory adapted to receive the write data signal in synchronization with the first data strobe signal in the write operation*' as claimed." Pet. 38 (citing Ex. 1003 ¶¶ 62–64).

Petitioner's arguments are supported by Dr. Baker's testimony, which we credit. *See* Ex. 1003 ¶¶ 62–64. Patent Owner does not contest Petitioner's evidence and arguments. *See* PO Resp. 1, 13–21.

Based on the complete record, we find that Petitioner has established that Lee's description of memory controller 140 transferring DATA to memory 120 via data bus 164, and also transferring, as a transmission synchronous signal, strobe signal SDtM to memory 120 via signal line 166, meets the recited "*memory adapted to receive the write data signal in synchronization with the first data strobe signal in the write operation,*" of claim 1.

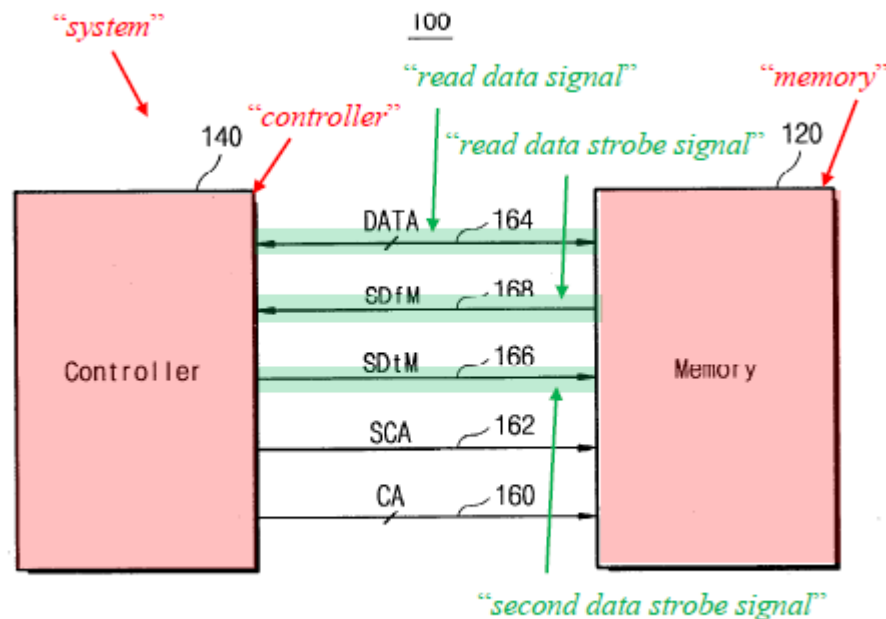
g) [1.6] *the memory being adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal and to send the read data signal synchronized with the read data strobe signal.*

For this limitation, Petitioner asserts that

Lee describes a read operation in which the memory transmits strobe signal SDfM ("*read data strobe signal*") over line 168 and data ("*read data signal*") over line 164. In Lee's read operation, "the memory controller 140 transfers to the memory 120 the second strobe signal SDtM as a transmission synchronous or reference signal at a time when it wants to receive data read out from the memory 120." EX1005, Lee, [0021]. These signals are transmitted by the memory in response to receiving the SDtM signal ("*second data strobe signal*"). "The memory 120 internally generates a third strobe signal SDfM *in response to* the second strobe signal SDtM. The read data that is read from the memory 120 is sent to the memory controller 140 together with the third strobe signal SDfM."

Pet. 39 (citing Ex. 1005 ¶ 21; *see also* Ex. 1005 ¶ 25).

To illustrate this operation, Petitioner provides an annotated version of Lee's Figure 1, shown below. Pet. 40.



EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 65.

Petitioner's annotated Figure 1 from Lee, shown above, depicts controller 140 in communication with memory 120 during a read operation. *Id.* Petitioner identifies (in green) signal SDtM 166 as the recited "second data strobe signal," signal SDfM 168 as the recited "read data strobe signal," and DATA 164 as the recited "read data signal." *Id.*

Petitioner argues that

because Lee's memory system transmits the strobe signal SDfM in response to the SDtM signal, Lee renders obvious 'the memory being adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal and to send the read data signal synchronized with the read data strobe signal' as claimed.

Pet. 40 (citing Ex. 1003 ¶¶ 65–66).

Petitioner's arguments are supported by Dr. Baker's testimony, which we credit. *See* Ex. 1003 ¶¶ 65–66. Patent Owner does not contest Petitioner's evidence and arguments. *See* PO Resp. 1, 13–21.

Based on the complete record, we find that Petitioner has established that Lee's description of memory controller 140 transferring to memory 120 strobe signal SDtM as a transmission synchronous or reference signal, wherein memory 120 generates strobe signal SDfM in response to strobe signal SDtM, and read data that is read from memory 120 is sent to memory controller 140 together with strobe signal SDfM meets the recited "*memory being adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal and to send the read data signal synchronized with the read data strobe signal,*" of claim 1.

h) Conclusion as to Independent Claim 1

We have considered Petitioner's uncontested evidence and arguments that the limitations of claim 1 are met by the teachings of Lee. Based on the complete record, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that the teachings of Lee meet the recited subject matter of independent claim 1.

2. Independent Claim 6

Petitioner contends that Lee would have rendered independent claim 6 obvious under 35 U.S.C. § 103(a). Pet. 16. Petitioner provides a claim analysis, supported by the testimony of Dr. Baker. *See* Pet. 40–43; Ex. 1003 ¶¶ 67–72. Patent Owner does not contest Petitioner's evidence and arguments with respect to claim 6. *See* PO Resp. 1, 13–21.

a) [6.0] A controller for use in a system, the system including a memory

For the preamble of claim 6, Petitioner asserts that "Lee describes a memory system 100 ('system') that includes a controller 140 ('controller') and a memory 120 ('memory')." Pet. 40–41. Petitioner quotes Lee, which states "[r]eferring to FIG. 1, a memory system 100 according to particular

embodiments the present invention includes a memory 120 and a memory controller 140.” *Id.* (quoting Ex. 1005 ¶ 17) (emphasis omitted). Petitioner argues that “because Lee describes a memory system with a controller and a memory, Lee renders obvious a ‘*controller for use in a system, the system including a memory*’ as claimed.” Pet. 41 (citing Ex. 1003 ¶¶ 67–68).

Petitioner relies on the testimony of Dr. Baker to support its arguments, which we credit. *See* Ex. 1003 ¶¶ 67–68. Patent Owner does not contest Petitioner’s evidence and arguments with respect to the preamble of claim 6. *See* PO Resp. 1, 13–21.

Based on the complete record, we find that Petitioner has established that Lee’s teachings meet the recited subject matter claim 6’s preamble.

b) [6.1] *the controller being adapted to send out a first data strobe signal and a write data signal to the memory in a write operation, the write data signal being synchronized with the first data strobe signal,*

For limitation [6.1], Petitioner relies on its evidence and arguments with respect to limitations [1.1] and [1.2]. *See* Pet. 41–42 (citing Ex. 1003 ¶ 69). Patent Owner does not contest Petitioner’s evidence and arguments with respect to limitation [6.1]. *See* PO Resp. 1, 13–21.

Based on the complete record, and for the reasons stated above with respect to limitations [1.1] and [1.2], we find that Petitioner has established that Lee’s teachings meet the recited subject matter of limitation [6.1].

c) [6.2] *the controller being adapted to send out a second data strobe signal to the memory and to receive a read data signal in synchronization with a read data strobe signal from the memory in a read operation,*

For limitation [6.2], Petitioner relies on its evidence and arguments with respect to limitation [1.3]. *See* Pet. 42 (citing Ex. 1003 ¶ 70). Patent

Owner does not contest Petitioner's evidence and arguments with respect to limitation [6.2]. *See* PO Resp. 1, 13–21.

Based on the complete record, and for the reasons stated above with respect to limitation [1.3], we find that Petitioner has established that Lee's teachings meet the recited subject matter of limitation [6.2].

d) [6.3] the read data strobe signal received by the controller corresponding to the second data strobe signal in the read operation.

For limitation [6.3], Petitioner refers to its evidence and arguments with respect to limitation [1.4] and also states that

Lee's SDfM signal is received by the controller in response to transmitting the SDtM signal: "The memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM." EX1005, Lee, [0021]. Because the SDfM signal ("read data strobe signal") is received "in response to" the SDtM signal of the read operation ("second data strobe signal"), the SDfM signal corresponds to the SDtM signal. The SDfM signal also corresponds to the SDtM signal in that it has the same form: "The third strobe signal SDfM, as illustrated in FIG. 2, may have the same waveform as the second strobe signal SDtM."

Pet. 42 (citing Ex. 1005 ¶ 25).

Petitioner's assertions are supported by the testimony of Dr. Baker, which we credit. Ex. 1003 ¶¶ 71–72. Patent Owner does not contest Petitioner's evidence and arguments with respect to limitation [6.3]. *See* PO Resp. 1, 13–21.

Based on the complete record, and for the reasons stated above with respect to limitation [1.4], we find that Petitioner has established that Lee's teachings meet the recited subject matter of limitation [6.3].

e) Conclusion as to Independent Claim 6

We have considered Petitioner’s uncontested evidence and arguments that the limitations of claim 6 are met by the teachings of Lee. Based on the complete record, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that the teachings of Lee meet the recited subject matter of independent claim 6.

3. Independent Claim 10

Petitioner contends that Lee would have rendered independent claim 10 obvious under 35 U.S.C. § 103(a). Pet. 16. Petitioner provides a claim analysis, supported by the testimony of Dr. Baker. *See id.* at 43–44; Ex. 1003 ¶¶ 73–75. Patent Owner does not contest Petitioner’s evidence and arguments with respect to claim 10. *See* PO Resp. 1, 13–21.

a) [10.0] A memory for use in a system, the system including a controller

For the preamble of claim 10, Petitioner explains that “Lee describes a memory system 100 (‘system’) that includes a controller 140 (‘controller’) and a memory 120 (‘memory’).” Pet. 43. Petitioner quotes Lee, which states “[r]eferring to FIG. 1, a memory system 100 according to particular embodiments the present invention includes a memory 120 and a memory controller 140.” *Id.* (quoting Ex. 1005 ¶ 17). “Thus,” Petitioner argues, “Lee renders obvious a ‘memory for use in a system, the system including a controller’ as claimed.” Pet. 43 (citing Ex. 1003 ¶¶ 73–74).

Petitioner relies on the testimony of Dr. Baker to support its arguments, which we credit. *See* Ex. 1003 ¶¶ 73–74. Patent Owner does not contest Petitioner’s evidence and arguments with respect to the preamble of claim 10. *See* PO Resp. 1, 13–21.

Based on the complete record, we find that Petitioner has established that Lee's teachings meet the recited subject matter of claim 10's preamble.

b) [10.1] the controller outputting a data strobe signal in a read operation, the memory being adapted to send out a read data strobe signal to the controller in response to the data strobe signal and to send out a read data signal synchronized with the read data strobe signal in a read operation.

For limitation [10.1], Petitioner relies on its evidence and arguments with respect to limitations [1.3], [1.4], and [1.6]. *See* Pet. 43–44 (citing Ex. 1003 ¶ 75). Patent Owner does not contest Petitioner's evidence and arguments with respect to limitation [10.1]. *See* PO Resp. 1, 13–21.

Based on the complete record, and for the reasons stated above with respect to limitations [1.3], [1.4], and [1.6], we find that Petitioner has established that Lee's teachings meet the recited subject matter of limitation [10.1].

c) Conclusion as to Independent Claim 10

We have considered Petitioner's uncontested evidence and arguments that the limitations of claim 10 are met by the teachings of Lee. Based on the complete record, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that the teachings of Lee meet the recited subject matter of independent claim 10.

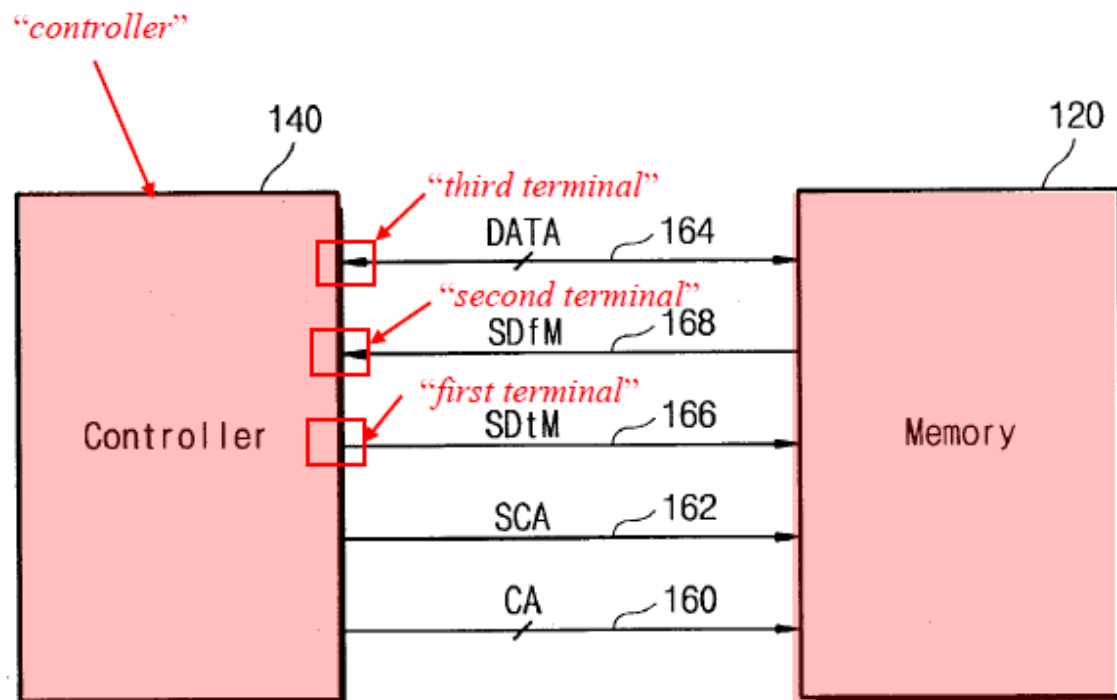
4. Independent Claim 26

Petitioner contends that Lee would have rendered independent claim 26 obvious under 35 U.S.C. § 103(a). Pet. 16. Petitioner provides a claim analysis, supported by the testimony of Dr. Baker. *See id.* at 51–57; Ex. 1003 ¶¶ 67–72. Patent Owner does not contest Petitioner's evidence and arguments with respect to claim 6. *See* PO Resp. 1, 13–21.

a) [26.0] A controller comprising a first terminal, a second terminal, and a third terminal

For the preamble of claim 26, Petitioner explains that “Lee describes a memory system 100 that includes a controller 140 (‘controller’) and a memory 120.” Pet. 51. Petitioner quotes Lee, which states “[r]eferring to FIG. 1, a memory system 100 according to particular embodiments the present invention includes a memory 120 and a memory controller 140.” *Id.* (citing Ex. 1005 ¶ 17). Petitioner notes that “Lee explains that communication between a memory and a controller uses “pins.” Pet. 51. According to Petitioner, Lee states that “[a]s is known to those of skill in the art, a memory typically provides external communications with, for example, a memory controller or chipset, via pins (e.g., data pins, address pins, control pins, power pins, and so on).” *Id.* (quoting Ex. 1005 ¶ 6).

Petitioner argues that a person of ordinary skill in the art “would have understood that the pins for the communication lines 164, 166, and 168 may be referred to as terminals as well. Such terminals are shown in [Lee’s] annotated Fig. 1 below.” Pet. 51.



Lee's Figure 1, annotated by Petitioner, depicts controller 140 on the left with memory 120 on the right connected by communication lines 164, 166, and 168. The contacts between communication lines 164, 166, and 168 with controller 140 are annotated by a red box labeled "first terminal" (166), "second terminal" (168), and "third terminal" (164).

Petitioner argues that "because Lee's controller includes pins for communicating with the memory, Lee renders obvious a '*controller comprising a first terminal, a second terminal, and a third terminal*' as claimed." Pet. 52 (citing Ex. 1003 ¶¶ 90–93).

Petitioner relies on the testimony of Dr. Baker to support its arguments, which we credit. *See* Ex. 1003 ¶¶ 90–93. Patent Owner does not contest Petitioner's evidence and arguments with respect to the preamble of claim 26. *See* PO Resp. 1, 13–21.

Based on the complete record, we find that Petitioner has established that Lee's teaching that a memory typically provides external

communication with a memory controller or chipset via pins, such as data pins, address pins, control pins, power pins, and so on, would have rendered obvious the recited subject matter of claim 26's preamble.

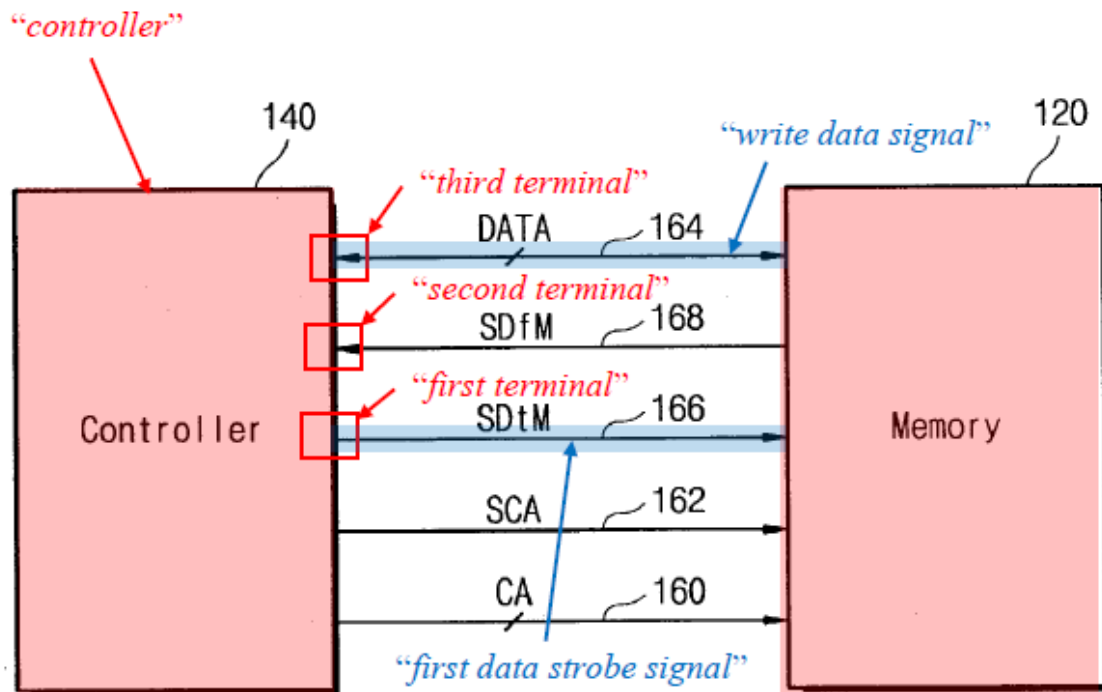
b) [26.1] *the controller being adapted to produce a first data strobe signal at the first terminal and a write data signal at the third terminal in a write operation, the write data signal being synchronized with the first data strobe signal*

For limitation [26.1], Petitioner points out that

Lee describes the write operation in which the controller transmits strobe signal SDtM (“first data strobe signal”) over line 166 (“first terminal”) and data (“write data signal”) over line 164 (“third terminal”). “For a write operation, . . . the memory controller 140 transfers data DATA to the memory 120 via a data bus 164, and transfers, as a transmission synchronous signal, the second strobe signal SDtM to the memory 120 via a signal line 166.”

Pet. 52–53 (citing Ex. 1005 ¶ 20).

Petitioner provides an annotated Figure 1 of Lee, shown below.



Petitioner's annotated Figure 1, above, depicts controller 140 on the left with memory 120 on the right, indicating DATA line 164 as "write data signal" in blue and SDtM line 166 as "first data strobe signal" in blue. Pet.

53. Petitioner notes that

Lee explains that the data signal is synchronous with the data strobe signal SDtM: "For a write operation . . . the memory controller 140 transfers data DATA to the memory 120 via a data bus 164, and transfers, **as a transmission synchronous signal**, the second strobe signal SDtM to the memory 120 via a signal line 166."

Id. (citing Ex. 1005 ¶ 20).

"Thus," Petitioner argues,

because Lee describes a controller 140 that transmits a strobe signal SDtM and a data signal over lines 166 and 164 respectively, Lee renders obvious "*the controller being adapted to produce a first data strobe signal at the first terminal and a write data signal at the third terminal in a write operation, the write data signal being synchronized with the first data strobe signal*" as claimed.

Pet. 53–54 (citing Ex. 1003 ¶¶ 94–96).

Petitioner's arguments are supported by the testimony of Dr. Baker, which we credit. Ex. 1003 ¶¶ 94–96. Patent Owner does not contest Petitioner's evidence and arguments with respect to limitation [26.1]. *See* PO Resp. 1, 13–21.

Based on the complete record, we find that Petitioner has established that Lee's teachings meet the recited subject matter of limitation [26.1].

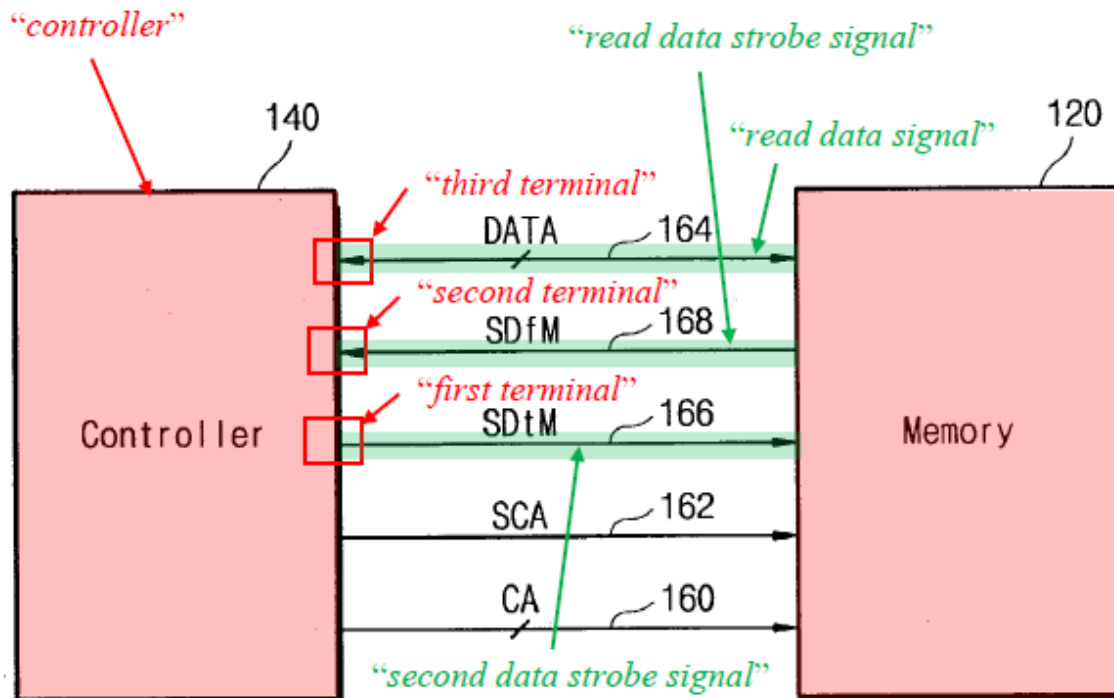
c) [26.2] the controller being adapted to produce a second data strobe signal at the first terminal and to receive a read data signal at the third terminal in synchronization with a read data strobe signal arriving at the second terminal from outside of the controller in a read operation.

For limitation [26.2], Petitioner asserts that

consistent with the discussion above at [1.3], Lee describes a read operation in which the memory (which is “*from outside the controller*”) transmits strobe signal SDfM (“*read data strobe signal*”) over line 168 (“*second terminal*”) and data (“*read data signal*”) over line 164 (“*third terminal*”) in response to the SDtM signal (“*second data strobe signal*”). “For a read operation, . . . the memory controller 140 transfers to the memory 120 the second strobe signal SDtM as a transmission synchronous or reference signal at a time when it wants to receive data read out from the memory 120.” EX1005, Lee, [0021]. In response, “the memory controller 140 receives the read data DATA from the memory 120 together with the third strobe signal SDfM at a required time.”

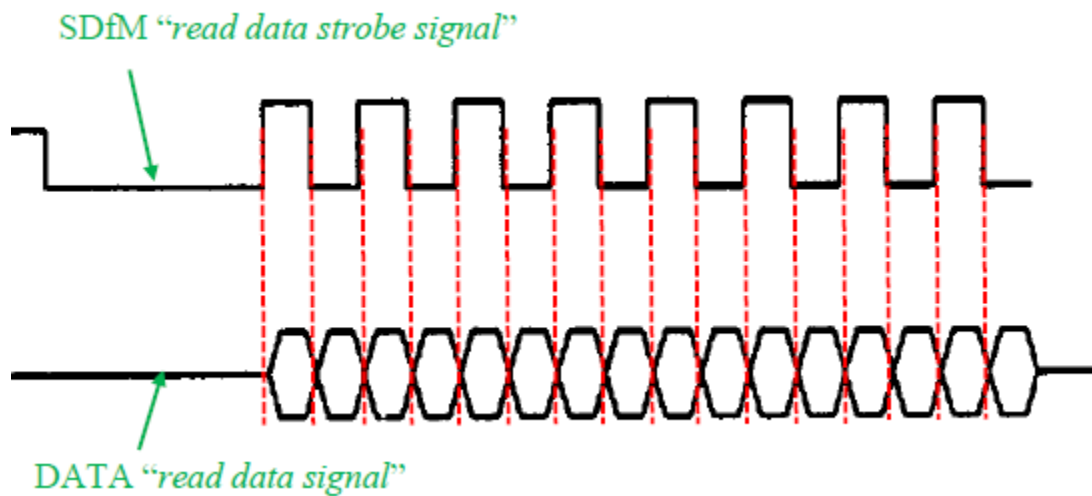
Pet. 54 (citing Ex. 1005 ¶ 21).

Petitioner provides an annotated version of Lee’s Figure 1, shown below.



Petitioner's annotated Figure 1, above, depicts controller 140 on the left with first, second, and third terminals, and memory 120 on the right. Petitioner has annotated in green signal line SDfM 168 identified as "read data strobe signal," DATA bus 164 identified as "read data signal," and signal line SDtM 166 as "second data strobe signal." Pet. 55.

Petitioner explains that "like the write operation, the SDfM signal ('read data strobe signal') is in synchronization with the read data signal. As can be seen in the annotated figure below, the rising and falling times of the strobe signal SDfM are synchronized with the switching of the data signal." *Id.* Petitioner's annotated version of Lee's Figure 2 (partial) is shown below.



The figure above is a portion of the timing diagram of Figure 2, including Petitioner’s annotations. Petitioner identifies in green the top signal as SDfM “read data strobe signal” and the bottom signal as DATA “read data signal.” Pet. 56.

“Accordingly,” Petitioner argues, a person of ordinary skill in the art “would have understood that the SDfM signal is ‘*in synchronization with*’ the read DATA signal,” and “would have understood that synchronization is done for the purpose of telling the receiving component—in this case the memory—when to sample the data: ‘The memory controller 140 latches data DATA loaded on the data bus 166 in response to the third strobe signal SDfM.’” Pet. 56 (quoting Ex. 1005 ¶ 25; citing Ex. 1003 ¶ 99).

“Thus,” Petitioner argues,

because Lee describes memory that transmits a data signal over line 164 and a strobe signal SDfM over line 168 responsive to a strobe signal SDtM over line 166, Lee renders obvious “*the controller being adapted to produce a second data strobe signal at the first terminal and to receive a read data signal at the third terminal in synchronization with a read data strobe signal arriving at the second terminal from outside of the controller in a read operation*” as claimed.

Pet. 56–57 (citing Ex. 1003 97–100).

d) Conclusion as to Independent Claim 26

We have considered Petitioner’s uncontested evidence and arguments that the limitations of claim 26 are met by the teachings of Lee. Based on the complete record, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that the teachings of Lee meet the recited subject matter of independent claim 26.

5. Dependent Claims 14–19, 25, and 27

Petitioner contends that Lee would have rendered dependent claims 14–19, 25, and 27 obvious under 35 U.S.C. § 103(a). Pet. 16. Petitioner provides a detailed claim analysis, supported by the testimony of Dr. Baker. *See* Pet. 44–51, 57; Ex. 1003 ¶¶ 76–89, 101, 102. Patent Owner does not contest Petitioner’s evidence or arguments with respect to the obviousness of these dependent claims. *See* PO Resp. 1, 13–21.

a) Dependent Claim 14

Dependent claim 14 recites: “*The system of claim 1, wherein in the read operation the memory retransmits the second data strobe signal as the read data strobe signal.*” Ex. 1001, 9:56–58.

For claim 14, Petitioner asserts that

Lee explains that “The memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM.” EX1005, Lee, [0021]. Lee also explains that “[t]he third strobe signal SDfM, as illustrated in FIG. 2, **may have the same waveform** as the second strobe signal SDtM delayed by a predetermined time.” EX1005, Lee, [0025]. Thus, by generating the third strobe signal SDfM (“*read data strobe signal*”) that has the same waveform as the received the SDtM signal (“*second data strobe signal*”), the memory system is *retransmitting* the SDtM signal as the SDfM signal. As shown

in [Lee’s Figure 2], the SDfM signal is identical to the SDtM signal in shape.

Pet. 44.

Petitioner also asserts that

[n]otably, Lee describes retransmitting the strobe signal with at least the same level of specificity as the ’369 patent, the specification of which does not provide any further explanation as to what it means to “retransmit” the second strobe signal as the read data strobe signal. What Lee explains and illustrates is thus similar to how the ’369 patent illustrates the “retransmitted” read data strobe signal.

Id. at 45–46 (citing Ex. 1001, Fig. 8; Ex. 1003 ¶ 77).

“Thus,” Petitioner argues, “because Lee describes transmitting the strobe signal SDfM with the same waveform as the received SDtM signal, Lee renders obvious ‘*wherein in the read operation the memory retransmits the second data strobe signal as the read data strobe signal*’ as claimed.”

Pet. 46 (citing Ex. 1003 ¶¶ 76–78).

Petitioner’s arguments are supported by the testimony of Dr. Baker, which we credit. Ex. 1003 ¶¶ 76–78. Patent Owner does not contest Petitioner’s evidence and arguments with respect to claim 14. *See* PO Resp. 1, 13–21.

Based on the complete record, we find that Petitioner has established that Lee’s teachings meet the recited subject matter of dependent claim 14.

b) Dependent Claim 15

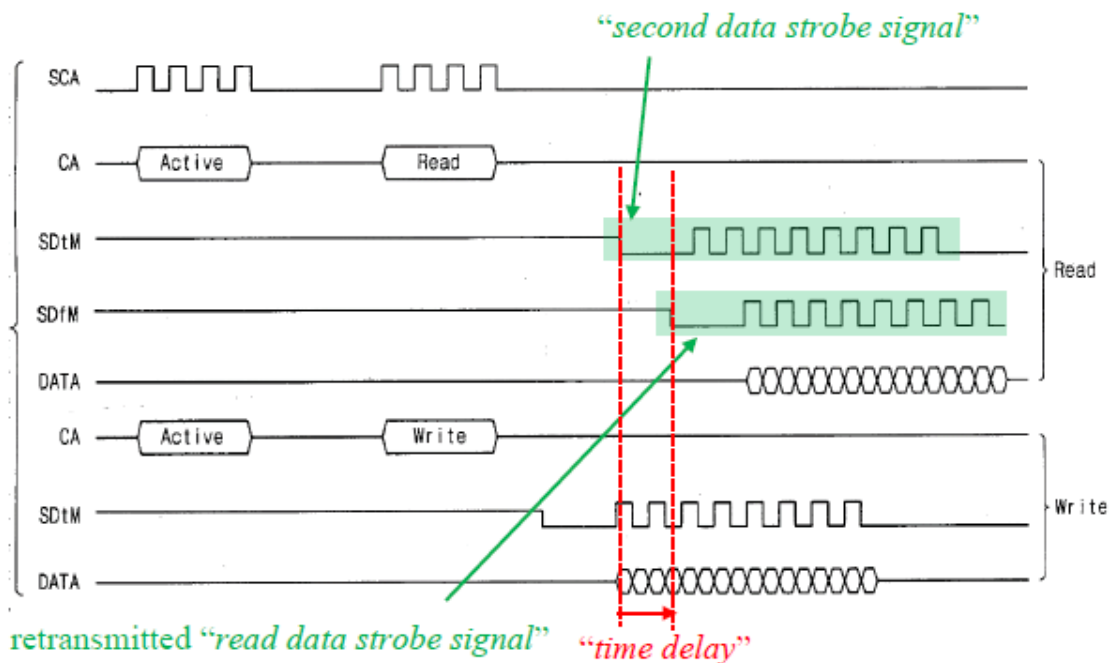
Dependent claim 15 recites: “*The system of claim 14, wherein in the read operation the memory retransmits the second data strobe signal with a time delay as the read data strobe signal.*” Ex. 1001, 9:59–61.

For claim 15, Petitioner states that

Lee explains that “[t]he memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM.” EX1005, Lee, [0021]. Lee also explains that “[t]he third strobe signal SDfM, as illustrated in FIG. 2, **may have the same waveform as the second strobe signal SDtM delayed by a predetermined time.**” EX1005, Lee, [0025]. Thus, by generating the third strobe signal SDfM (“*read data strobe signal*”) with the same waveform as the SDtM signal (“*second data strobe signal*”) with a predetermined delay, the memory system is *retransmitting* the SDtM signal as the SDfM signal with a time delay.

Pet. 46–47.

To illustrate the time delay, Petitioner provides an annotated version of Lee’s Figure 2, shown below.



Petitioner’s annotated version of Lee’s Figure 2 is a timing diagram of read and write data transmission operations with signal STdM identified as “*second data strobe signal*” in green and signal SDfM identified as “*retransmitted ‘read data strobe signal’*” in green. A “time delay” between the STdM and SDfM signals is identified in red. Pet. 47.

“Thus,” Petitioner argues,

because Lee describes transmitting the strobe signal SDfM with the same wave form as the received SDtM signal with a predetermined delay, Lee renders obvious ‘*wherein in the read operation the memory retransmits the second data strobe signal with a time delay as the read data strobe signal*’ as claimed.

Id. (citing Ex. 1003 ¶¶ 79–80).

Petitioner’s arguments are supported by the testimony of Dr. Baker, which we credit. Ex. 1003 ¶¶ 79–80. Patent Owner does not contest Petitioner’s evidence and arguments with respect to dependent claim 15. *See* PO Resp. 1, 13–21.

Based on the complete record, we find that Petitioner has established that Lee’s teachings meet the recited subject matter of dependent claim 15.

c) Dependent Claim 16

Dependent claim 16 recites: “*The controller of claim 6, wherein in the read operation the controller receives a read data signal from the memory which is a retransmission of the second data strobe signal.*” Ex. 1001, 10:1–3.

For claim 16, Petitioner directs us to its evidence and arguments it made with respect to claim 14. *See* Pet. 48 (citing Ex. 1003 ¶ 81). Petitioner’s arguments are supported by the testimony of Dr. Baker, which we credit. Ex. 1003 ¶ 81. Patent Owner does not contest Petitioner’s evidence and arguments with respect to claim 16. *See* PO Resp. 1, 13–21.

Based on the complete record, and for the reasons discussed above with respect to claim 14, we find that Petitioner has established that Lee’s teachings meet the recited subject matter of dependent claim 16.

d) Dependent Claim 17

Dependent claim 17 recites: “*The controller of claim 16, wherein in the read operation the controller receives a read data signal from the memory which is a retransmission of the second data strobe signal with a time delay.*” Ex. 1001, 10:4–7.

For claim 17, Petitioner directs us to its evidence and arguments it made with respect to claim 15. *See* Pet. 48 (citing Ex. 1003 ¶ 82). Petitioner’s arguments are supported by the testimony of Dr. Baker, which we credit. Ex. 1003 ¶ 82. Patent Owner does not contest Petitioner’s evidence and arguments with respect to claim 17. *See* PO Resp. 1, 13–21.

Based on the complete record, and for the reasons discussed above with respect to claim 15, we find that Petitioner has established that Lee’s teachings meet the recited subject matter of dependent claim 17.

e) Dependent Claim 18

Dependent claim 18 recites: “*The memory of claim 10, wherein in the read operation the read data strobe signal is a retransmission of the received data strobe signal.*” Ex. 1001, 10:8–10.

For claim 18, Petitioner directs us to its evidence and arguments it made with respect to claim 14. *See* Pet. 48 (citing Ex. 1003 ¶ 86). Petitioner’s arguments are supported by the testimony of Dr. Baker, which we credit. Ex. 1003 ¶ 83. Patent Owner does not contest Petitioner’s evidence and arguments with respect to claim 17. *See* PO Resp. 1, 13–21.

Based on the complete record, and for the reasons discussed above with respect to claim 14, we find that Petitioner has established that Lee’s teachings meet the recited subject matter of dependent claim 18.

f) Dependent Claim 19

Dependent claim 19 recites: “*The memory of claim 18, wherein in the read operation the read data strobe signal is a retransmission of the received data strobe signal with a time delay.*” Ex. 1001, 10:11–13.

For claim 19, Petitioner directs us to its evidence and arguments it made with respect to claim 15. *See* Pet. 48 (citing Ex. 1003 ¶ 84). Petitioner’s arguments are supported by the testimony of Dr. Baker, which we credit. Ex. 1003 ¶ 84. Patent Owner does not contest Petitioner’s evidence and arguments with respect to claim 19. *See* PO Resp. 1, 13–21.

Based on the complete record, and for the reasons discussed above with respect to claim 15, we find that Petitioner has established that Lee’s teachings meet the recited subject matter of dependent claim 19.

g) Dependent Claim 25

Dependent claim 25 recites:

The system according to claim 1, further comprising first and second data strobe lines each provided between the controller and the memory, the first data strobe line transferring the first data strobe signal in the write operation from the controller to the memory, the first data strobe line transferring the second data strobe signal in the read operation from the controller to the memory, and the second data strobe line transferring the read data strobe signal in the read operation from the memory to the controller.

Ex. 1001, 10:39–47.

For claim 25, Petitioner refers us to its position with respect to limitations [1.1] and [1.3] and states that “Lee’s system includes signal lines

166 and 168 (*‘first and second data strobe lines’*) between the memory and the controller.” Pet. 49.

Petitioner further explains that

signal line 166 carries the SDtM signal of the write operation (*“the first data strobe line transferring the first data strobe signal in the write operation from the controller to the memory”*): “For a write operation . . . the memory controller 140 transfers data DATA to the memory 120 via a data bus 164, and transfers, as a transmission synchronous signal, the second strobe signal SDtM to the memory 120 **via a signal line 166.**”

Id. at 49–50 (citing Ex. 1005 ¶ 20).

Petitioner then refers us to its explanation with respect to limitation [1.3], and states that “signal line 166 also carries the SDtM signal of the read operation (*‘the first data strobe line transferring the second data strobe signal in the read operation from the controller to the memory’*)”: “For a read operation . . . the memory controller 140 transfers to the memory 120 the second strobe signal SDtM.” Pet. 50 (citing Ex. 1005 ¶ 20; *see also* Ex. 1005 ¶ 21 (“SDtM to the memory 120 **via a signal line 166.**”) (emphasis added)).

Petitioner further states that

the SDfM signal is sent from the memory to the controller during the read operation (*“the second data strobe line transferring the read data strobe signal in the read operation from the memory to the controller”*): “Therefore, during the read operation the memory controller 140 receives the read data DATA from the memory 120 together with the third strobe signal SDfM at a required time.” Ex. 1005 ¶ 21. Further, the SDfM signal is sent over line 168. Ex. 1005 ¶ 33 (“the third strobe signal SDfM transferred via the signal line 168.”).

Pet. 50.

“Thus,” Petitioner argues,

because Lee’s system includes signal lines 166 and 168 between the memory controller, and the signal lines carry the strobe signals of the read and write operations, Lee renders obvious “*further comprising first and second data strobe lines each provided between the controller and the memory, the first data strobe line transferring the first data strobe signal in the write operation from the controller to the memory, the first data strobe line transferring the second data strobe signal in the read operation from the controller to the memory, and the second data strobe line transferring the read data strobe signal in the read operation from the memory to the controller*” as claimed.

Id. at 50–51 (citing Ex. 1003 ¶¶ 85–89).

Petitioner’s arguments are supported by the testimony of Dr. Baker, which we credit. Ex. 1003 ¶¶ 85–89. Patent Owner does not contest Petitioner’s evidence and arguments with respect to claim 25. *See* PO Resp. 1, 13–21.

Based on the complete record, and for the reasons discussed above with respect to claim limitations [1.1] and [1.3], we find that Petitioner has established that Lee’s teachings meet the recited subject matter of dependent claim 25.

h) Dependent Claim 27

Dependent claim 27 recites: “*The controller according to claim 26, wherein the read data strobe signal is generated outside of the controller in response to the second data strobe signal.*” Ex. 1001, 10:58–60.

For claim 27, Petitioner states that

Lee explains that the SDfM signal is generated by the memory (“*outside of the controller*”): “The **memory 120 internally generates** a third strobe signal SDfM in response to the second strobe signal SDtM.” EX1005, Lee, [0021]. Furthermore, as explained above at [1.3] and [1.4], the strobe signal SDfM

(“*read data strobe signal*”) is generated “in response to” receiving the strobe signal SDtM (“*second data strobe signal*”).
Pet. 57.

“Thus,” Petitioner argues, “because Lee’s memory generates the strobe signal SDfM in response to the strobe signal SDtM, Lee renders obvious ‘*the read data strobe signal being received by the controller in response to the second data strobe signal*’ as claimed.” *Id.* (citing Ex. 1003 ¶¶ 101–102).

Petitioner’s arguments are supported by the testimony of Dr. Baker, which we credit. Ex. 1003 ¶¶ 101–102. Patent Owner does not contest Petitioner’s evidence and arguments with respect to claim 27. *See* PO Resp. 1, 13–21.

Based on the complete record, we find that Petitioner has established that Lee’s teachings meet the recited subject matter of dependent claim 27.

i) Conclusion as to Dependent Claims 14–19, 25, and 27

We have considered Petitioner’s uncontested evidence and arguments that the limitations of dependent claims 14–19, 25, and 27 are met by the teachings of Lee. Based on the complete record, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that the teachings of Lee meet the recited subject matter of these dependent claims.

F. Obviousness Based on Lee and JEDEC (Ground 2)

Petitioner contends that dependent claims 2, 7, and 11 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Lee and JEDEC. Pet. 16. Petitioner provides a claim analysis, and relies on the testimony of Dr. Baker to support its position. *See* Pet. 63–68; Ex. 1003 ¶¶ 103–122. Petitioner also provides an explanation of a

rationale to combine the teachings of Lee and JEDEC. *See* Pet. 59–63 (citing Ex. 1003 ¶¶ 108–113).

Patent Owner disagrees, arguing that “no motivation to combine the references exist as the proposed combination would render Lee inoperable for its intended purpose of achieving low power operation.” PO Resp. 13; *see also id.* at 14–21. Patent Owner relies on the testimony of Dr. Jacob to support its position. *See* Ex. 2003 ¶¶ 101–111.

Petitioner filed a Reply disagreeing with Patent Owner’s position. *See* Pet. Reply 10–29. Patent Owner filed a Sur-reply further disagreeing with Petitioner’s evidence and arguments. *See* PO Sur-reply 2–14.

1. Dependent Claims 2, 7, and 11

Dependent claims 2, 7, and 11 depend directly from independent claims 1, 6, and 10, respectively, and are similar in that each recites a controller further adapted to send a clock signal to memory, where the data strobe signals are independent of, and separated from, the clock signal. Claims 2, 7, and 11 are set out below.

Claim 2 recites: “*The system according to claim 1, wherein the controller is further adapted to produce a clock signal and to send the clock signal to the memory, each of the first and the second data strobe signals and the read data strobe signal being independent of and separated from the clock signal.*” Ex. 1001, 8:31–35.

Claim 7 recites: “*The controller according to claim 6, wherein the controller is further adapted to produce a clock signal and to send the clock signal to the memory, each of the first and the second data strobe signals and the read data strobe signal being independent of and separated from the clock signal.*” *Id.* at 9:26–30.

Claim 11 recites: “*The memory according to claim 10, the controller being further adapted to send out a clock signal and to send the clock signal to the memory, wherein each of the data strobe signal and the read data strobe signal is independent of and separated from the clock signal.*” *Id.* at 9:45–49.

Patent Owner does not dispute that Petitioner’s proposed combination of Lee and JDEC teaches all of the recited limitations of dependent claims 2, 7, and 11. *See* PO Resp. 13–21. Instead, Patent Owner contends that Petitioner’s proposed combination of Lee and JDEC “fails to show a motivation to combine. Specifically, no motivation to combine the references exists as the proposed combination would render Lee inoperable for its intended purpose of achieving low power operation.” PO Resp. 13; *see also id.* at 14–21. Accordingly, we consider Petitioner’s rationale to combine Lee and JDEC and the parties’ arguments and evidence related thereto.

2. *Rationale to Combine Lee and JDEC*

Petitioner asserts that a person of ordinary skill in the art “would have found it obvious to implement Lee’s SCA signal in any of a variety of known and suitable ways—in either a synchronous or asynchronous manner.” Pet. 59. Petitioner explains that

Lee’s SCA signal is used to latch command/address information: “That is, the command/address information CA is transferred to the memory 120 from the memory controller 140 together with the first strobe signal SCA based on the source synchronous interface. The memory 120 latches the command/address information CA in response to the first strobe signal SCA.”

Id. (citing Ex. 1005 ¶ 19).

Petitioner asserts that “Lee further explains that the SCA signal is applied intermittently: The SCA signal ‘can be implemented using a clock signal that is toggled only during a desired period, for example, when data is on the CA bus or the DATA bus.’” Pet. 59–60 (citing Ex. 1005 ¶ 35). Petitioner explains that “[u]sing such an intermittent signal is an example of asynchronous memory.” *Id.* (citing Pet. at Sec. IV.C.; Ex. 1003 ¶ 108).

Petitioner asserts that a person of ordinary skill in the art “would have found it obvious to implement the SCA signal as a clock signal to register command/address information (i.e., synchronous memory).” Pet. 60. According to Petitioner “Lee provides evidence that it was known to use either synchronous or asynchronous memory.” *Id.* According to Lee, “the amount of current consumed by a memory system in a standby state results from the clock signal used to synchronize operations of a synchronous memory.” *Id.* (quoting Ex. 1005 ¶ 34). Petitioner explains that in Lee, “the strobe signals, such as SCA and SDtM, that are used as transmission references or synchronous signals, are used in the memory 120 only as a latch enable or latching signal.” Pet. 60 (citing Ex. 1005 ¶ 34). “This means that the memory 120 performs read and write operations in an asynchronous manner, for example, using a delay chain as a state machine.” Pet. 60 (citing Ex. 1005 ¶ 34; Ex. 1003 ¶ 109).

Petitioner asserts that a person of ordinary skill in the art “would have understood that there are design tradeoffs between using synchronous and asynchronous memories.” Pet. 60. “For example,” Petitioner explains, “asynchronous memory can provide the benefit of less power consumption, as explained by Lee.” *Id.* (citing Ex. 1005 ¶ 34). Petitioner asserts that “[s]ynchronous memory—using a clock signal for sampling information—

provides the benefit of higher bandwidth capabilities.” Pet. 60–61 (citing Ex. 1006, 5).

Petitioner points out that persons of ordinary skill in the art “used systems that had the capability to switch between synchronous and asynchronous modes.” Pet. 61 (citing Ex. 1008, title, abstract). Petitioner argues that a person of ordinary skill in the art “implementing a memory system according to Lee’s teachings would have found it obvious to use either synchronous or asynchronous memory, as either was a known option, and would choose between the two based on their specific design/power considerations.” Pet. 61. According to Petitioner, if a person of ordinary skill in the art “wanted to design the system for power conservation, they would likely choose Lee’s asynchronous option. If a [person of ordinary skill in the art] wanted to design the memory system for high bandwidth, they would likely choose the synchronous option.” *Id.* (citing Ex. 1003 ¶ 110).

Petitioner asserts that persons of ordinary skill in the art “knew how to implement memories using a clock signal and registers because industry standards defined how to do so.” Pet. 61. According to Petitioner, “[t]he JEDEC standard is an example,” as “the JEDEC standard defines the use of a continuous clock signal that is transmitted from the controller to the memory.” *Id.* (citing Ex. 1003 ¶ 110). Petitioner argues that, “the JEDEC standard does not specify the source of the clock signal, and it would be obvious and in fact common in the art for the memory controller to produce the clock signal, such as is taught by Lee with reference to the SCA signal.” Pet. 62 (citing Ex. 1005 ¶ 19; Ex. 1003 ¶ 111).

“Accordingly,” Petitioner argues, a person of ordinary skill in the art

would have found it obvious to implement Lee's SCA signal using a clock signal, consistent with the JEDEC standard. The results of using a standardized process such as the one described in the JEDEC standard would have been predictable because standardized techniques are heavily vetted: "JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Council level and subsequently reviewed and approved by the EIA General Counsel." EX1007, JEDEC, 2. For this reason, a POSITA also would have had a reasonable expectation of success. EX1003, ¶ 113. Further still, there is a general familiarity and ease-of-design in the art using synchronous devices and a continuous clock, as evidenced by the JEDEC Standard, that would motivate a POSITA to use a continuous clock for the memory device of Lee.

Pet. 62–63 (citing Ex. 1003 ¶ 112).

"Thus," Petitioner argues, "the combination of Lee and JEDEC is merely a substitute of one known element (Lee's intermittent SCA signal) with another (standardized clock signal) to obtain predictable results." Pet. 63 (citing Ex. 1003 ¶ 113).

Patent Owner disagrees. In its Response, Patent Owner argues that "no motivation to combine the references exist as the proposed combination would render Lee inoperable for its intended purpose of achieving low power operation." PO Resp. 13. Patent Owner argues that Petitioner's proposed substitution "would 'defeat[] the purpose of' the system being modified," and "that 'substitution is illogical' and cannot provide the basis for an obviousness determination." *Id.* at 14 (citing *In re Schweickert*, 676 F. App'x 988, 994 (Fed. Cir. 2017); *Plas-Pak Indus., Inc. v. Sulzer Mixpac AG*, 600 F. App'x 755, 760 (Fed. Cir. 2015)).

Patent Owner explains that

Lee teaches an asynchronous memory that, by definition, does not receive a system clock. Specifically, Lee seeks to “*avoid*” “*the need for a continuous clock*” and reduce “the current consumed by the memory 120 when not performing a read or write operation . . . over a similar memory that utilizes a continuous clock.”

PO Resp. 15 (citing Ex. 1005 ¶ 28).

“Accordingly,” Patent Owner argues

introducing the continuous clock—which Lee seeks to avoid—by using Petitioner’s proposed combination with JEDEC would render Lee inoperable for its intended purpose because it would remove the lower power operability. Ex. 2003, Jacob Decl., ¶¶ 101–110. Indeed, the specific combination of Lee and JEDEC urged by Petitioner and its expert was eschewed by Lee as frustrating its purpose of reducing power consumption.

PO Resp. 15.

According to Patent Owner,

Lee, specifically provides, however, “*the strobe signals SCA and SDtM are not used as a reference signal (e.g., a clock signal)* for a memory operation.” Ex. 1005, Lee ¶ [0034]. Dr. Baker notes that Paragraph 35 of Lee provides that “SCA . . . can be implemented using a clock signal that is toggled only during the desired period.” Ex 1003, Baker Decl., ¶115. However, such disclosure by its clear terms does not endorse the use of a “continuous clock” but one that “is toggled only during the desired period.”

PO Resp. 16.

Patent Owner argues that “Petitioner’s contention that ‘[a] POSITA would have understood that there are design tradeoffs between using synchronous and asynchronous memories’ does not show a reason to combine Lee and JEDEC.” *Id.* at 19. Patent Owner contends that “the Petition ultimately provides no coherent reason why a POSITA *would have*

been motivated to make the specific combination of Lee and JEDEC it alleges.” *Id.* at 20.

In its Reply, Petitioner argues that “[t]he alleged inventive concept of both the ’369 Patent and Lee is to modify the conventional source-synchronous operation by adding an additional strobe signal used to transfer data during read operations . . . referred to as the ‘turnaround strobe.’” Pet. Reply 5–6.⁴ Petitioner points out, and we agree, that “[s]ource-synchronous operation using a turnaround strobe is the subject matter of Ground 1 (e.g., claim 1) of the present IPR . . . and the fact that this operation is also (and previously) taught by Lee is not challenged by the Patent Owner.” *Id.* at 6.

Petitioner argues that even though the primary embodiment of Lee uses an asynchronous memory for the transfer of address and control signals, “there are multiple reasons why it would be obvious to use Lee’s source-synchronous operation with synchronous memory, many of which were spelled out in the Petition.” *Id.* According to Petitioner, “Lee is clear that asynchronous memory is an example application, or use, for its source-synchronous operation,” and a person of ordinary skill in the art “would find it obvious to use Lee’s source-synchronous operation with synchronous memories (memories using a clock signal), thereby rendering unpatentable the claims identified in Ground 2 of the Petition.” *Id.* at 7. Petitioner points out that “both the ’369 Patent and Lee incorporate by reference prior art

⁴ In its Reply, Petitioner acknowledges that “[t]he term ‘turnaround strobe’ was not used in the Petition, but was used by the Patent Owner’s expert, Dr. Jacob, during deposition and is adopted herein as a shortcut way to describe the modified source-synchronous operation of the ’369 Patent.” Pet. Reply 6 n.1 (citing Ex. 2003, 14:17–18).

patents that describe source-synchronous operation.” *Id.* at 7–8.⁵ Petitioner argues that “although Lee discusses some of the benefits of using asynchronous memory, Lee is not limited to asynchronous memory, neither does Lee teach away from using synchronous memory nor would Lee be inoperable for its intended purpose by using synchronous memory.” *Id.* at 10–11.

Petitioner contends that “[t]he Petition listed multiple reasons to combine the teaching of JEDEC, which describes a synchronous DRAM (SDRAM) that uses a clock signal, in the memory system of Lee.” Pet. Reply 11. According to Petitioner, this includes “the benefit of higher bandwidth capabilities.” *Id.* (citing Pet. 60–61; Ex. 1006, 5). “Increased bandwidth,” Petitioner argues, “as compared to reduced power, was a well-known design choice for a POSITA, as explained by Petitioner’s expert Dr. Baker.” Pet. Reply 11 (citing Ex. 1003 ¶ 110 (“If a POSITA wanted to design the system that emphasized power conservation, they could choose Lee’s asynchronous option. If a POSITA wanted to design the memory system that emphasized high bandwidth, they could choose the synchronous option.”)).

Petitioner also points out that Patent Owner’s expert, Dr. Jacob, testified at deposition that synchronous memory had certain benefits over

⁵ According to Petitioner, “The ’369 Patent incorporates by reference U.S. Pat. No. 6,789,209B1 in which ‘[d]ata signals are sent out from the sender is synchronized with the data strobe signal.’ Ex. 1001, 1:12–17. Lee incorporates by reference U.S. Pat. No. 6,336,159 titled ‘Method and Apparatus for Transferring Data in Source-Synchronous Protocol and Transferring Signals in Common Clock Protocol in Multiple Agent Processing System.’” Pet. Reply 8 n.2 (citing Ex. 1005 ¶ 18).

asynchronous memory, including predictability, simplicity of design and cost savings. Pet. Reply 16–17 (citing Ex. 1015, 22:10–23:8).⁶

Petitioner argues that “Lee does not teach away from using synchronous memory, neither does synchronous memory render Lee inoperable for its intended purpose,” as Patent Owner contends. Pet. Reply 18–20. Petitioner argues that “Lee is merely stating [the] potential benefits of using asynchronous memory in his memory system,” which “‘*may*’ be beneficial in mobile applications, or that using its source synchronous operation ‘*may*’ avoid a need for a continuous clock, or that current consumption ‘*may*’ be reduced.” *Id.* at 20 (citing Ex. 1005 ¶¶ 4, 5, 28) (emphasis by Petitioner).

Petitioner argues that “Lee is merely stating potential benefits of using asynchronous memory in his memory system,” and “Lee does not impose an intended purpose of only using asynchronous memory as asserted by Patent Owner, and does not clearly discourage using synchronous memory.” *Id.* at 20–24.

According to Petitioner, “Lee includes a listing of 25 claims, some of which show that Lee clearly contemplates covering both types of memory, asynchronous and synchronous,” including for example, independent claim 5, which, Petitioner argues, is not limited to asynchronous memory. *Id.* at 27.

⁶ We note for the record that these particular benefits were not identified or relied upon by Petitioner for its stated rationale to combine Lee and JEDC in the Petition. See Pet. 59–63. Because we rely on Petitioner’s stated rationale of higher bandwidth, we do not rely on these other benefits in making our final determination here.

Petitioner also argues that “Lee recites an embodiment using synchronous memory,” where “Lee incorporates by reference U.S. Patent No 6,336,159, which describes:

a system that transmits data using a source synchronous protocol while transmitting control signals using a common clock protocol in order to increase the bandwidth of transmitting data without a corresponding increase in the number of signals transmitted

Pet. Reply 26 (citing Ex. 1005 ¶ 18; Ex. 1014, 1:49–54).

In its Sur-reply, Patent Owner argues that “none” of the reasons identified by Petitioner “show that a POSITA *would* have combined LEE and JEDEC,” and “[a]t most they show that a POSITA could have combined the references.” PO Sur-reply 7. Patent Owner argues that Petitioner “fails to provide a reason that a POSITA would have chosen [increased bandwidth] over the low-power benefits of asynchronous memory described be Lee.” *Id.* at 8.

We disagree with Patent Owner. The test for obviousness is not whether the claimed invention is expressly suggested in any one or all of the asserted prior references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. *In re Keller*, 642 F.2d 413, 425 (CCPA 1981). A reason to combine teachings from the prior art “maybe found in explicit or implicit teachings within the references themselves, from the ordinary knowledge of those skilled in the art, or from the nature of the problem to be solved.” *WMS Gaming Inc. v. Int’l Game Tech.*, 184 F.3d 1339, 1355 (Fed. Cir. 1999) (citing *In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998)). “Under the correct [obviousness] analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining

the elements in the manner claimed.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 420 (2007).

The Supreme Court has stated that

[o]ften, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

KSR, 550 U.S. at 418. Indeed, the strongest rationale for combining references is a recognition, expressly or impliedly in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal precedent, that some advantage or expected beneficial result would have been produced by their combination. *In re Sernaker*, 702 F.2d 989, 994–995 (Fed. Cir. 1983).

Indeed, the Federal Circuit has

repeatedly held that an implicit motivation to combine exists not only when a suggestion may be gleaned from the prior art as a whole, but when the ‘improvement’ is technology-independent and the combination of references results in a product or process that is more desirable, for example because it is stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient. Because the desire to enhance commercial opportunities by improving a product or process is universal—and even common-sensical—we have held that there exists in these situations a motivation to combine prior art references even absent any hint of suggestion in the references themselves. In such situations, the proper question is whether the ordinary artisan possesses knowledge and skills rendering him capable of combining the prior art references.

Dystar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick, 464 F.3d 1356, 1368 (Fed. Cir. 2006).

Here, Petitioner expressly identifies in the Petition a specific reason to combine the Lee and JEDEC references: higher bandwidth capabilities. Pet. 60–61. Petitioner explains that “[s]ynchronous memory—using a clock signal for sampling information—provides the benefit of higher bandwidth capabilities.” Pet. 60–61. Petitioner cites to page 5 of the Prince reference (Ex. 1006) to support this assertion. *Id.* at 61. Prince is a textbook entitled “*High Performance Memories—New architecture DRAMs and SRAMs evolution and function.*” Ex. 1006, cover. Page 5 of Prince is in Section 1.2 titled “*New Memory Architectures to Improve Bandwidth.*” *Id.* at 5. Page 5 of Prince states:

New interface architectures are also being used to improve the bandwidth of the RAMs. The most common is the synchronous interface. Making a memory synchronous puts it under the control of the system clock. “Wait states”, during which the processor must wait for the output data from the RAM, can be reduced or eliminated. With a synchronous RAM the input addresses can be latched into the memory, freeing the processor to perform other tasks until the data is available after a known number of cycles. While the intrinsic speed of the RAM does not increase **by the addition of a synchronous interface, the effective speed in the system increases since the processor no longer waits for the RAM to operate.**

Id. (emphasis added).

Dr. Baker, Petitioner’s declarant, also discusses the improved bandwidth benefit of using synchronous memory in his testimony. Dr. Baker explains that, for example, “asynchronous memory can provide the benefit of less power consumption, as explained by Lee.” Ex. 1003 ¶ 110 (citing Ex. 1005 ¶ 34). Dr. Baker testifies, however, that “[s]ynchronous memory—using a continuous clock—**provides the benefit of higher bandwidth capabilities,**” citing the Prince reference as support.

Ex. 1003 ¶ 110 (emphasis added). Dr. Baker goes on to testify that persons of ordinary skill in the art

used systems that had the capability to switch between synchronous and asynchronous modes. *See generally* EX1008, Mills, title, abstract. Accordingly, a POSITA implementing a memory system according to Lee's teachings would have found it obvious to use either synchronous or asynchronous memory, as either was a suitable option depending on the characteristics considered most important. If a POSITA wanted to design the system that emphasized power conservation, they could choose Lee's asynchronous option. If a POSITA wanted to design the memory system that emphasized high bandwidth, they could choose the synchronous option. These are well-known options to a POSITA. That is, any modifications to Lee to accommodate a synchronous option, such as changing Lee's input latches to registers, are well-known and extremely common skills of a POSITA.

Id.

Dr. Baker further testifies that a person of ordinary skill in the art “knew how to implement memories using a continuous clock [synchronous memory] because industry standards defined how to do so. The JEDEC standard is an example [and] the JEDEC standard defines the use of a continuous clock signal that is transmitted from the controller to the memory.” *Id.* ¶ 111. Dr. Baker continues, testifying that a person of ordinary skill in the art “would have found it obvious to implement Lee's SCA signal using a continuous clock, consistent with the JEDEC standard. The results of using a standardized process such as the one described in the JEDEC standard would have been predictable because standardized techniques are heavily vetted” and “also would have had a reasonable expectation of success.” *Id.* ¶ 112.

Notably, at the oral hearing in this proceeding, Patent Owner’s counsel conceded that the Petition “makes a reference to bandwidth as a purported motivation to combine.” Paper 28, 19:17–19.

In its Sur-reply, Patent Owner reiterates its arguments that “Lee teaches away from synchronous memory and using synchronous memory would render Lee inoperable for its intended purpose.” PO Sur-reply 11–14. We disagree. In order to “teach away,” a reference must actually “criticize, discredit, or otherwise discourage” investigation into the claimed solution. *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004). A reference does not “teach away” if it merely expresses a general preference for an alternative invention from amongst options available to the ordinarily skilled artisan, and the reference does not discredit or discourage investigation into the invention claimed. *Id.*

A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant. The degree of teaching away will of course depend on the particular facts; in general, a reference will teach away if it suggests that the line of development flowing from the reference’s disclosure is unlikely to be productive of the result sought by the applicant. *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994).

Here, Lee does not expressly “criticize, discredit, or otherwise discourage” the combination proposed by Petitioner. Although Lee uses asynchronous memory in its embodiments, Lee does not expressly “criticize, discredit, or otherwise discourage” the use of synchronous memory as proposed by Petitioner. Indeed, Lee discusses utilizing a clock signal in some of its memory operations. For example, Lee explains that the SCA

signal “can be implemented using a clock signal that is toggled only during a desired period, for example, when data is on the CA bus or the DATA bus.” Ex. 1005 ¶ 35.

We credit Dr. Baker’s testimony that a person of ordinary skill in the art “implementing a memory system according to Lee’s teachings would have found it obvious to use either synchronous or asynchronous memory, as either was a suitable option depending on the characteristics considered most important.” Ex. 1003 ¶ 110. Dr. Baker explains that if a person of ordinary skill in the art “wanted to design the system that emphasized power conservation, they could choose Lee’s asynchronous option.” *Id.* Alternatively, Dr. Baker testifies that if a person of ordinary skill in the art “wanted to design the memory system that emphasized high bandwidth, they could choose the synchronous option.” *Id.* According to Dr. Baker, “[t]hese are well-known options” to a person of ordinary skill in the art and “any modifications to Lee to accommodate a synchronous option, such as changing Lee’s input latches to registers, are well-known and extremely common skills.” *Id.*

We also disagree with Patent Owner that Petitioner’s proposed combination of Lee and JEDEC would render Lee inoperable for its intended purpose. We credit Dr. Baker’s testimony that Lee’s source-synchronous operation may be implemented in either an asynchronous manner as Lee describes, or in a synchronous manner using a clock signal as described by JEDEC. *See id.* ¶¶ 109–113. Dr. Baker’s testimony is persuasive that a person of ordinary skill in the art “would have understood that there are design tradeoffs between using a synchronous device interface based on a

continuous clock signal, and an asynchronous device interface with a non-continuous strobe signal.” *Id.* ¶ 110.

Dr. Baker testifies, and we agree, that if a person of ordinary skill in the art “wanted to design the system that emphasized power conservation,” such as in Lee’s mobile processing embodiments, “they could choose Lee’s asynchronous option.” *Id.* If, however, a person of ordinary skill in the art “wanted to design the memory system that emphasized high bandwidth, they could choose the synchronous option.” *Id.* According to Dr. Baker, “any modifications to Lee to accommodate a synchronous option, such as changing Lee’s input latches to registers, are well-known and extremely common skills.” We also agree with Dr. Baker that “[t]he results of using a standardized process such as the one described in the JEDEC standard would have been predictable because standardized techniques are heavily vetted” and a person of ordinary skill in the art “would have had a reasonable expectation of success.” *Id.* ¶ 112.

Lee’s abstract states that it provides “[a] memory for storing data information and/or a controller for controlling read/write operations of the memory based on a source synchronous interface.” Ex. 1005, Abstr. Petitioner’s proposed combination of Lee and JEDEC provides that arrangement using a synchronous memory. *See* Ex. 1003 ¶¶ 109–113. Accordingly, contrary to Patent Owner’s arguments, Petitioner’s proposed combination of Lee and JEDEC does not render Lee inoperable for its intended purpose.

Based upon the complete record, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that a person of ordinary skill in the art would have had a reasoned basis for combining the teachings

of Lee and JEDEC in the manner proffered in the Petition and would have had a reasonable expectation of success in that endeavor.

IV. CONCLUSION⁷

For the foregoing reasons, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 1, 2, 6, 7, 10, 11, 14–19, and 25–27 of U.S. Patent 7,697,369 B2 are unpatentable on the bases set forth in the following table.

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 6, 10, 14–19, 25– 27	103(a) ⁸	Lee	1, 6, 10, 14– 19, 25–27	
2, 7, 11	103(a)	Lee, JEDEC	2, 7, 11	
Overall Outcome			1, 2, 6, 7, 10, 11, 14–19, 25–27	

⁷ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

⁸ Because the application from which the ’369 patent issued was filed before March 16, 2013 (Ex. 1001, code (22)), citations to 35 U.S.C. § 103 are to the pre-AIA version. Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29.

V. ORDER

Upon consideration of the record before us, it is

ORDERED that Petitioner has demonstrated by a preponderance of the evidence that claims 1, 2, 6, 7, 10, 11, 14–19, and 25–27 of U.S. Patent 7,697,369 B2 are unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, any party to the proceeding seeking judicial review of this Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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