

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Mianyang BOE Optoelectronics Technology Co., Ltd.; Wuhan China Star
Optoelectronics Semiconductor Display Technology Co., Ltd.; Tianma
Microelectronics Co. Ltd.; and Visionox Technology, Inc.,
Petitioner,

v.

Samsung Display Company, Ltd.,
Patent Owner.

U.S. Patent No. 9,330,593

Original Issue Date: May 3, 2016

Title: STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY
USING THE SAME

Case No. IPR2023- 01221

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 9,330,593
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42 *et seq.***

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Inter Partes Review

United States Patent No. 9,330,593

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LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 9,330,593 (the “’593 patent”)
1002	Prosecution History of U.S. Patent No. 9,330,593
1003	Declaration of Dr. Daniel Foty
1004	U.S. Patent Publication No. 2013/0285888A1 (“Chung”)
1005	U.S. Patent Publication No. 2013/0127807A1 (“Kim”)
1006	U.S. Patent Publication No. 2008/0101529A1 (“Tobita”)
1007	U.S. Patent Publication No. 2008/0062097A1 (“Jeong”)
1008	Excerpts from <i>Analog Integrated Circuit Design</i> , David A. Johns et al., John Wiley & Sons, Inc. (1997)
1009	Complainant’s Opening Claim Construction Brief, <i>In the Matter of Certain Active Matrix Organic Light-Emitting Diode Display Panels and Modules for Mobile Devices, and Components Thereof</i> , Inv. No. 337-TA-1351
1010	Excerpts from <i>Physics and Technology of Semiconductor Devices</i> , A. Grove, John Wiley & Sons (1967)
1011	Excerpts from <i>CMOS Digital Integrated Circuits: Analysis and Design</i> , (third edition), S. Kang et al., McGraw-Hill (2003)
1012	Docket from <i>Samsung Display Co., Ltd. v. BOE Technology Co., Ltd.</i> , E.D. Tex. 2-23-cv-00309
1013	U.S. Patent Publication No. 2003/0132931A1 (“Kimura”)
1014	U.S. Patent Publication No. 2005/0185752A1 (“Sasaki”)
1015	U.S. Patent Publication No. 2007/0139348A1 (“Lee”)

CHALLENGED CLAIM LISTING

Claim	Limitation No.	Limitation
1	[1-PRE]	A stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal, the stage circuit comprising:
	[1-A]	an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node;
	[1-B]	a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal; and
	[1-C]	a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node,
	[1-D]	wherein the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.
2	[2-A]	The stage circuit as claimed in claim 1, wherein the first input terminal receives an output signal of a previous stage circuit or a start signal,
	[2-B]	wherein the second input terminal receives a first clock signal, and
	[2-C]	wherein the third input terminal receives a second clock signal.
3	3	The stage circuit as claimed in claim 2, wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap.

Claim	Limitation No.	Limitation
4	4	The stage circuit as claimed in claim 3, wherein the first clock signal and the second clock signal have a period equal to two horizontal periods 2H and are supplied in different horizontal periods as low signals.
5	5	The stage circuit as claimed in claim 2, wherein the start signal is supplied to overlap the first clock signal.
6	[6-A]	The stage circuit as claimed in claim 2, wherein the first driver includes: a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and
	[6-B]	a second transistor and a third transistor serially positioned between the second node and the first power supply,
	[6-C]	wherein a gate electrode of the second transistor is coupled to the third input terminal, and
	[6-D]	wherein a gate electrode of the third transistor is coupled to the first node.
7	[7-A]	The stage circuit as claimed in claim 2, wherein the outputting unit includes: a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node:
	[7-B]	a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node;
	[7-C]	a first capacitor between the second node and the output terminal; and
	[7-D]	a second capacitor between the first node and the first power supply.

Claim	Limitation No.	Limitation
8	[8-A]	The stage circuit as claimed in claim 2, wherein the second driver includes: a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and
	[8-B]	a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.
9	[9-A]	The stage circuit as claimed in claim 2, wherein the second driver includes: a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and
	[9-B]	a seventh transistor between the first node and the second input terminal, the seventh transistor being diode connected.
14	14	The stage circuit as claimed in claim 1, wherein the transistor controls the voltage of the second node according to the on/off operation thereof.
15	[15-PRE]	An organic light emitting display, comprising:
	[15-A]	pixels positioned in regions partitioned by scan lines and data lines;
	[15-B]	a data driver for supplying data signals to the pixels through the data lines; and
	[15-C]	a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal,

Claim	Limitation No.	Limitation
	[15-D]	wherein each of the stage circuits includes: an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node,
	[15-E]	a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal, and
	[15-F]	a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node,
	[15-G]	wherein the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.
16	16	The organic light emitting display as claimed in claim 15, wherein a clock signal supplied to the third input terminal is used as the scan signal.
17	17	The organic light emitting display as claimed in claim 15, wherein the first input terminal receives a scan signal of a previous stage circuit or a start signal.
18	[18-A]	The organic light emitting display as claimed in claim 17, wherein second input terminals of odd stage circuits receive a first clock signal and third input terminals of odd stage circuits receive a second clock signal, and
	[18-B]	wherein second input terminals of even stage circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal.

Claim	Limitation No.	Limitation
19	19	The organic light emitting display as claimed in claim 18, wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap.
20	[20-A]	The organic light emitting display as claimed in claim 18, wherein the first driver includes: a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and
	[20-B]	a second transistor and a third transistor serially positioned between the second node and the first power supply,
	[20-C]	wherein a gate electrode of the second transistor is coupled to the third input terminal, and
	[20-D]	wherein a gate electrode of the third transistor is coupled to the first node.
21	[21-A]	The organic light emitting display as claimed in claim 18, wherein the outputting unit includes: a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node;
	[21-B]	a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node;
	[21-C]	a first capacitor between the second node and the output terminal; and
	[21-D]	a second capacitor between the first node and the first power supply.
22	[22-A]	The organic light emitting display as claimed in claim 18, wherein the second driver includes: a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and

Claim	Limitation No.	Limitation
	[22-B]	a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.
23	[23-A]	The organic light emitting display as claimed in claim 18, wherein the second driver includes: a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and
	[23-B]	a seventh transistor between the first node and the second input terminal, the seventh transistor being diode connected.
25	25	The organic light emitting display as claimed in claim 18, wherein the scan signal of the previous stage circuit or the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal.

I. INTRODUCTION

Pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42, Petitioner respectfully requests *inter partes* review (“IPR”) of Claims 1-9, 14-23, and 25 (“Challenged Claims”) of U.S. Patent No. 9,330,593 (the “’593 patent”).

The ’593 patent relates to stage circuits for organic light emitting diode (“OLED”) displays, which are a “[c]onventional” part of displays. Ex.1001 at 1:17-47. The ’593 patent criticizes conventional stage circuits for having too many transistors or initializing signals and purports to disclose stage circuits with “a reduced number of transistors and that output scan signals only using first and second clock signals.” *Id.* at 9:12-26.

The ’593 patent further claims an “on/off” transistor in the stage circuit, which was added during prosecution to overcome a prior-art rejection: “the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.” *See* Claims 1 and 15.

But this allegedly novel control of a transistor was itself conventional in the prior art. As this Petition shows, it was well-known to include a transistor directly controlled by the signal of a third input terminal in the first driver of a stage circuit.

Petitioner requests that the PTAB institute trial and find the Challenged Claims unpatentable for the reasons below.

II. 37 C.F.R. § 42.8(B): MANDATORY NOTICES

A. 37 C.F.R. § 42.8(b)(1): Notice of Real Parties-in-Interest

Mianyang BOE Optoelectronics Technology Co., Ltd. (“BOE”); Wuhan China Star Optoelectronics Semiconductor Display Technology Co., Ltd.; Tianma Microelectronics Co. Ltd.; and Visionox Technology, Inc. and their subsidiaries are the real parties-in-interest. No other parties exercised or could have exercised control over this Petition; no other parties funded or directed this Petition. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48759-60.

B. 37 C.F.R. § 42.8(b)(2): Notice of Related Matters

To the knowledge of Petitioner, the ’593 patent has been involved in the following matters:

Case Name	Filed
ITC Investigation No. 337-TA-1351, <i>In the Matter of Certain Active Matrix Organic Light-Emitting Diode Display Panels and Modules for Mobile Devices, and Components Thereof</i>	December 28, 2022
<i>Samsung Display Co., Ltd. v. BOE Technology Co., Ltd.</i> , E.D. Tex. 2-23-cv-00309	June 26, 2023

C. 37 C.F.R. § 42.8(b)(3) and (4): Notice of Counsel and Service Information

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Petitioner submits a Power of Attorney with this Petition. Please address all correspondence to lead counsel. Petitioner consents to service by email at the addresses listed above.

D. Fee for Inter Partes Review

The USPTO is authorized to charge the filing fee and any other fees incurred by Petitioner to the deposit account of Orrick, Herrington, & Sutcliffe LLP: 15-0665.

III. REQUIREMENTS FOR IPR

This Petition complies with all requirements under 37 C.F.R. § 42.104.

A. § 42.104(a): Grounds for Standing

The '593 patent is available for IPR. Petitioner is not barred or estopped from requesting IPR. This Petition is timely filed under 35 U.S.C. § 315(b).

B. § 42.104(b): Identification of Challenge

Under 37 C.F.R. §§ 42.104(b) and 42.22, Petitioner requests that the Board institute IPR on and cancel as unpatentable the Challenged Claims of the '593 patent.

1. § 42.104(b)(1): Challenged Claims

Petitioner challenges Claims 1-9, 14-23, and 25 of the '593 patent.

2. § 42.104(b)(2): The Prior Art and Statutory Grounds

The application for the '593 patent claims priority to foreign application KR 10-2012-0104512, filed on September 20, 2012.

While Patent Owner has not shown its claims have support for the September 20, 2012 priority date, the references relied upon herein are prior art by

that date as follows:

Patent/Publication	Filing Date	Publication / Issue Date	Prior Art	Ex.
U.S. Patent Publication No. 2013/0285888A1 (“Chung”)	August 24, 2012	October 31, 2013	102(e)	1004
U.S. Patent Publication No. 2013/0127807A1 (“Kim”)	April 18, 2012	May 23, 2013	102(e)	1005
U.S. Patent Publication No. 2008/0101529A1 (“Tobita”)	April 7, 2011	July 28, 2011	102(a), (b)	1006
U.S. Patent Publication No. 2008/0062097A1 (“Jeong”)	July 12, 2007	March 13, 2008	102(a), (b)	1007

Below are the specific statutory grounds on which the claims are challenged:

Ground Number	Ground
1	Claims 1-7, 9, 14-21, 23, and 25 are anticipated under 35 U.S.C. § 102 by Chung
2	Claims 1-5, 7-8, 14-19, 21-22, and 25 are anticipated under 35 U.S.C. § 102 by Kim
3	Claims 1-5, 14-19, and 25 are obvious under 35 U.S.C. § 103 over Tobita
4	Claims 7 and 21 are obvious under 35 U.S.C. § 103 over Tobita in view of Jeong

Apart from Jeong, none of the references on which these grounds are based

were before the Examiner during prosecution of the '593 patent.

3. Level of Ordinary Skill in the Art

A POSITA in the technology described in the '593 patent in 2012 would have had a Bachelor's degree in electrical engineering or a similar discipline, along with 2-3 years of circuit design experience. Ex.1003 ¶31.

4. § 42.104(b)(5): Evidence Supporting Challenge

The Declaration of Dr. Daniel Foty (Ex.1003) and other supporting evidence in the Exhibit List are filed herewith. Dr. Foty's background and qualifications, and the information provided to him, are discussed in Exhibit 1003.

IV. INSTITUTION SHOULD BE GRANTED

This Petition establishes a reasonable likelihood of success on the merits and all other requirements for an IPR.

A. There Are No Grounds for a § 314 Discretionary Denial

There are co-pending ITC and district court actions involving the '593 patent. The Board considers the factors set forth in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) ("*Fintiv*"), clarified by the Director, when determining institution in light of such pendency. Considered as a whole, the *Fintiv* factors weigh strongly in favor of institution. Particularly, under the Director's guidance, there are no grounds for a discretionary denial due to the co-pending ITC action. Interim Procedure for Discretionary Denials at 2-3 (June

21, 2022). And “compelling, meritorious challenges will be allowed to proceed at the PTAB even where district court litigation is proceeding in parallel.” *Id.* at 4-5. That is the case here: as explained below, the Challenged Claims of the ’593 patent are plainly unpatentable in view of the prior art.

The co-pending district court litigation is in a very early stage. Petitioner has not yet been served. *See* Ex.1012. This also weighs in favor of institution. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 8-9, 11 (PTAB June 16, 2020).

Should Patent Owner urge the Board to exercise its discretion to deny institution, Petitioner respectfully requests a reply brief.

B. Denial Under § 325(d) Would Be Inappropriate

No ground presented here was considered by the Examiner or otherwise previously considered by the Patent Office. The primary references, Chung, Kim, and Tobita, were not cited by the applicant or considered by the Examiner. *See generally* Ex.1001. Further, as explained in Section VI.B below, the prior-art references the Examiner addressed during prosecution purportedly failed to teach a transistor whose on/off operation is directly controlled by the signal of the third input terminal. In contrast, Chung, Kim, and Tobita all specifically teach this. Thus, they are substantively different from and overcome any purported deficiencies considered by the Examiner.

For these reasons, and as explained below, the Board should institute IPR.

V. TECHNOLOGY BACKGROUND

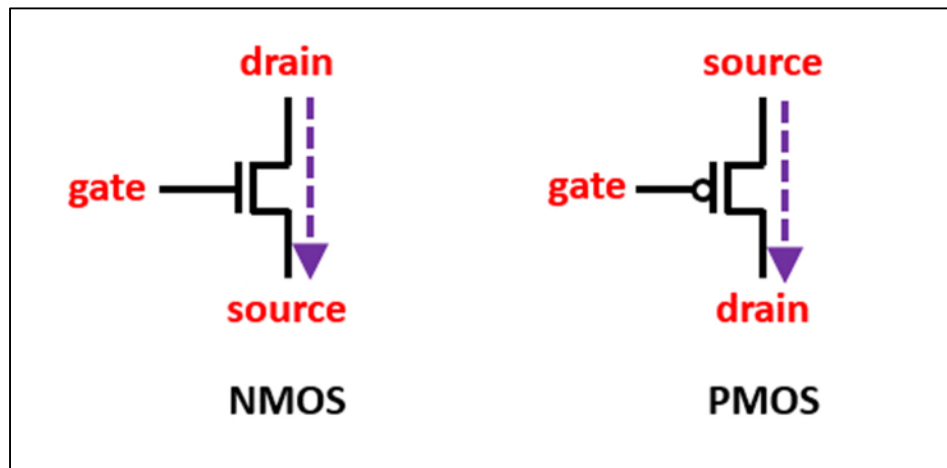
A. OLED Basics

OLED stands for organic light-emitting diode. Such diodes emit light in response to electric current. Ex.1003 ¶73. Typical OLED applications include television screens and computer monitors. OLED displays comprise a matrix of individual pixels. *Id.* ¶¶71, 73.

Pixels for OLED displays are typically arranged and activated as horizontal rows called “scan lines.” *Id.* ¶¶80-81. Control circuitry activates the lines one at a time to display an image. *Id.* ¶¶81-82.

B. Transistor Basics

Both nMOS (aka “n-channel” or “n-type” metal-oxide semiconductor) and pMOS (aka “p-channel” or “p-type”) transistors have existed for decades. Ex.1003 ¶¶35-41. Each has a gate, source, and drain terminal. *Id.* ¶¶41-51. pMOS circuit symbols are differentiated by a small circle on the gate. *Id.* ¶51. Current flows (arrow) from drain to source in nMOS transistors and source to drain in pMOS transistors. *Id.* ¶¶50-53.



For both, the gate voltage controls transistor operation (*i.e.*, turns it on/off).

Ex.1003 ¶¶42-47. The minimum gate voltage for activating a transistor is called threshold voltage. *Id.* ¶¶62-70. nMOS transistors are turned on by a high gate voltage, and pMOS transistors by a low gate voltage. Ex.1004 ¶0089; Ex.1003 ¶57.

The complementary nature and interchangeability of nMOS and pMOS switching transistors were well-known by 2012. *See, e.g.*, Ex.1004 ¶0089; Ex.1003 ¶56. The minor changes needed to substitute nMOS for pMOS was well within the knowledge and skill of a POSITA circa 2012. Ex.1003 ¶57. For example, it was well known that a pMOS circuit could be replaced with nMOS transistors, and vice versa, by reversing the logic level of input gate voltages and VDD/GND (from high to low and from low to high). Ex.1004 ¶0089; Ex.1003 ¶¶57-58. For example:

FIG.4

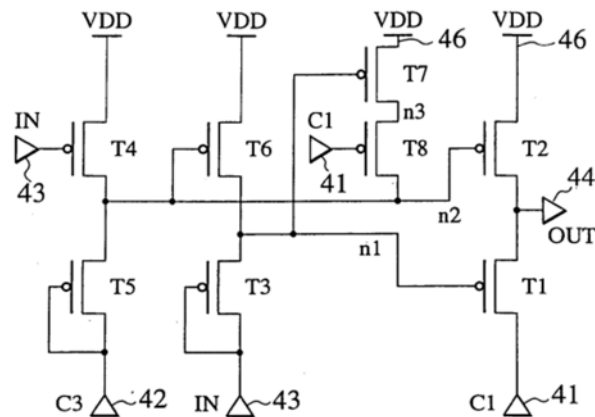
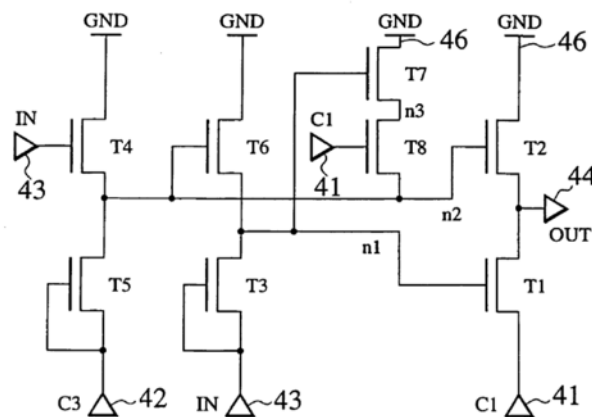


FIG.18



Ex.1014, Figs. 4, 18, ¶0084; *see also* Ex.1003 ¶¶59-60.

VI. THERE EXISTS A REASONABLE LIKELIHOOD THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE

The '593 patent relates to stage circuits used in OLED displays. Ex.1001, 1:17-18. Stage circuits, both generally and in OLED displays, were admitted prior art. *See id.* at 1:20-47.

As the '593 patent explains, it was well known that a “[c]onventional organic light emitting display includes a data driver for supplying data signals to

data lines, a scan driver for sequentially supplying scan signals to scan lines, and a pixel unit including a plurality of pixels coupled to the scan lines and the data lines.” *Id.* at 1:34-38. It was also well understood that “[t]he scan driver includes stage circuits coupled to the scan lines. The stages supply the scan signals to the scan lines coupled thereto to correspond to signals supplied thereto.” *Id.* at 1:45-47.

As the ’593 patent admits, by September 2012, the use of stage circuits in OLED displays was well established and built upon longstanding, basic circuit principles. *See* Ex.1003 ¶¶54-55, 80-82. Stage circuits were a crowded art where the concepts were well understood, predictable, and routinely combined to achieve a POSITA’s design goals. *Id.* ¶82.

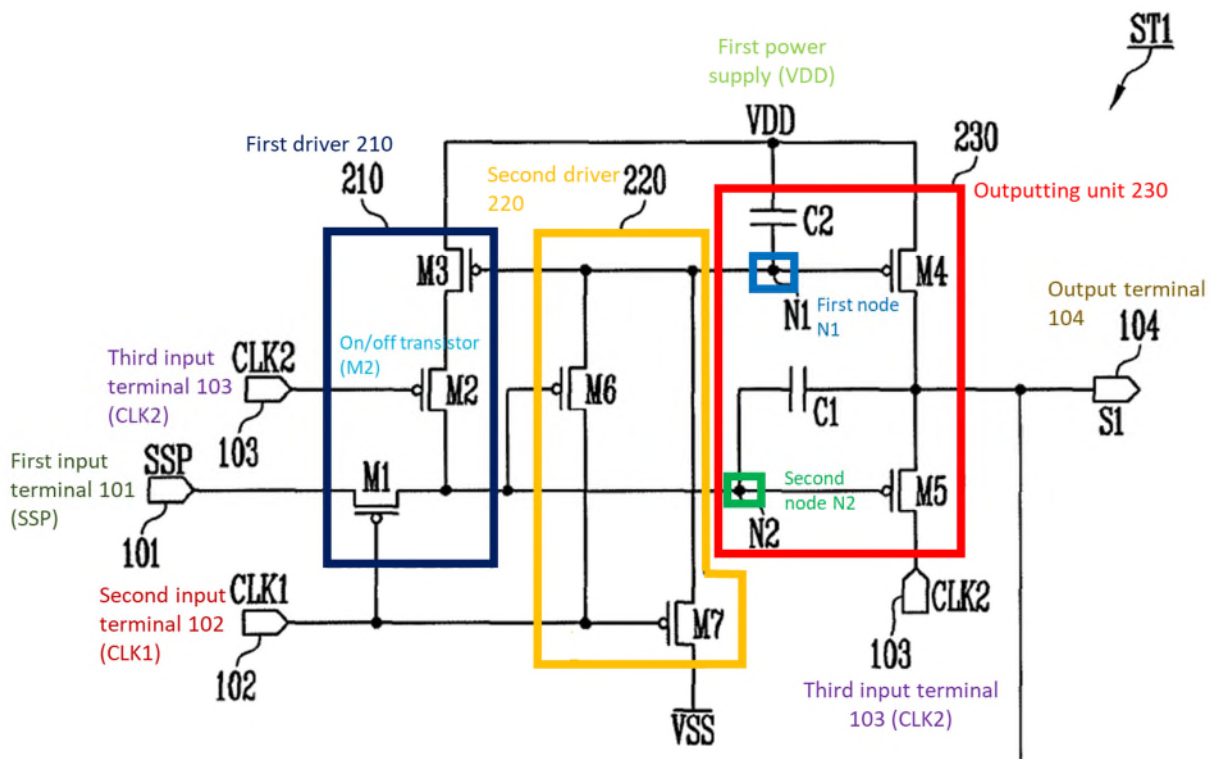
A. Problem Addressed by the ’593 Patent and the Alleged Invention

While the ’593 patent admits that stage circuits were widely used in the prior art, it identifies alleged drawbacks in certain prior-art circuits. The patent criticizes “conventional” stage circuits for requiring a large number of transistors and/or initializing signals beyond two clock signals. Ex.1001 at 9:15-18. The patent asserts that, in comparison, such excesses are unnecessary for its embodiments. *Id.* at 9:12-14; *see also* Ex.1003 ¶84.

The ’593 patent further asserts that its diminutive embodiments purportedly increase production yield and improve stability through decreased complexity.

Ex.1001, 9:18-26; Ex.1003 ¶85. Based on Patent Owner's proposed constructions and infringement theories from the ITC matter, however, nothing in the claims limits the numbers of transistors or input signals. *See, e.g.*, Ex.1003 ¶85.

Figure 3, annotated below, shows the preferred embodiment of the '593 patent. It shows the correspondance to the circuit components and signals recited in independent Claims 1 and 15.



Ex.1001, Fig. 3.¹

The preferred embodiments of the '593 patent comprise a first input terminal SSP, a second input terminal CLK1, a third input terminal CLK2, and an output

¹ All annotations in this Petition are by Petitioner.

terminal S_n , where n denotes the stage number.² The first input terminal SSP receives a start signal or the output signal from the previous stage, *e.g.*, S_{n-1} for the n -th stage. *Id.* at 5:1-7. The first and second input terminals receive two clock signals having the same period and nonoverlapping phases. *Id.* at 5:8-28. The circuits are partitioned into a first driver, a second driver, and an outputting unit. The first driver and the second driver control the voltage of the second node N2 and the first node N1, respectively. *Id.* at 5:63-67, 6:22-26. The outputting unit supplies a voltage to the output terminal S_n according to the voltage at the first node or the second node. *Id.* at 5:37-41.

“On/off transistor” M2 corresponds to the limitation: “the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.” Claims 1 and 15. It is the placement of transistor M2 in the first driver, having the “third input” coupled to its gate, where the “third input” is also applied to the outputting unit, that the patentee highlighted to overcome prior-art rejections.

The patent’s other embodiments, *see* Figures 6 and 7, are largely identical to Figure 3. The differences are relatively minor and do not relate to the circuit elements of the independent claims, or most of the Challenged Claims. *See*

² Colored texts in this Petition match the color used to annotate corresponding components in figures.

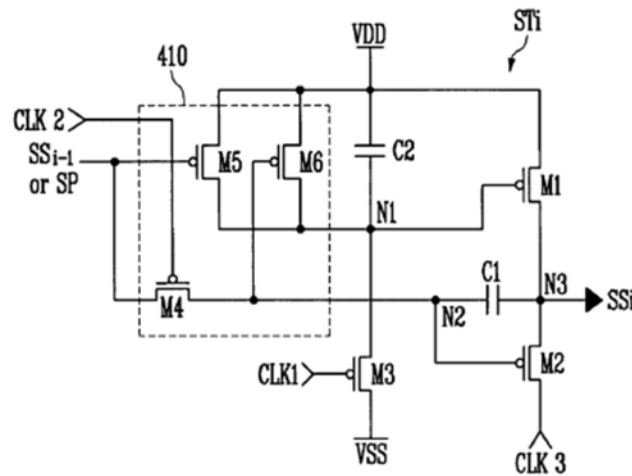
Ex.1001 at 8:28-42, 10:51-53, 12:33-35 (Challenged Claims 9 and 23 replace transistor M7 with “diode-connected” M7’, otherwise the figure uses “the same elements as those of FIG. 3”), 8:43-9:11 (the “bidirectional driver 240,” which appears only in unchallenged Claims”).

B. Prosecution History

The ’593 patent stems from foreign application KR 10-2012-0104512 and was prosecuted in the United States as Application No. 13/771,385.

In a non-final Office Action, the Examiner rejected the pending claims in view of Jeong, finding each either anticipated or obvious. Ex.1002 at 123-133 (February 9, 2015 Office Action at 2-12).

In response, the patentee amended the claims, most significantly adding to the independent claims a requirement that “the signal of the third input terminal at least controls an on/off operation of a switch.” *Id.* at 101-108 (May 5, 2015 Amendment at 2-9). The patentee argued that, as shown in Figure 4 (copied below), Jeong does not teach this limitation because the identified third input terminal (CLK3) is applied to the drain electrode, not gate electrode, of the second transistor M2. Thus, CLK3 “does **not** control an on/off operation of the second transistor M2,” *i.e.*, the claimed switch. *See id.* at 110-111 (emphasis in original). The patentee did not otherwise distinguish Jeong.



Ex.1007, Fig. 4.

The patentee argued that the switch-transistor was in the “first driver,” though that feature was not recited in the claims. *See* Ex.1002 at 111 (“claim 1 now recites that a first driver to control [sic] a voltage of a second node of an outputting unit in accordance with signals of first, second, and third input terminals, wherein **the signal of the third input terminal** at least **controls an on/off operation of a switch.**”) (emphases in original).

The Examiner then rejected the claims as obvious in view of Jeong and supplemental references. *Id.* at 81-92 (June 17, 2015 Office Action at 3-14). Following an August 13, 2015 Amendment, in view of new prior art, the Examiner proposed that the independent claims be amended to clarify the third input terminal's role in both the outputting unit and in controlling the "on/off" transistor in the first driver. *Id.* at 53 (August 21, 2015 Interview Summary).

The patentee revised accordingly:

“an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and ~~[[or]] a signal of the third input terminal to the output terminal in accordance with voltages~~ according to a voltage applied to the first node and the second node”

...

“the signal of the third input terminal directly ~~at least~~ controls an on/off operation of a transistor, the transistor included in the first driver switch.”

Id. at 31, 34-35 (September 17, 2015 Amendment at 2, 5-6); *see id.* at 40-42

(arguing the amendment put the claims in condition for allowance). A Notice of Allowance followed. *See id.* at 11-14.

C. Claim Construction

The Board construes claims under *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*) and its progeny. Under *Phillips*, claims are given their plain and ordinary meaning in light of the specification. 415 F.3d at 1315-17. The Board only construes claim terms when necessary to resolve the controversy. *See, e.g., Toyota Motor Corp. v. Cellport Sys., Inc.*, IPR2015-00633, Paper 11 at 16 (PTAB Aug. 14, 2015). Petitioner does not believe any claim construction is necessary here. Specifically, in the related ITC proceeding, Patent Owner argues that all terms should be given their plain and ordinary meaning. For purpose of this proceeding, Petitioner applies Patent Owner’s constructions and infringement

theories without agreeing to their correctness. *See also* Ex.1003 ¶¶97-98.

VII. THE PRIOR ART

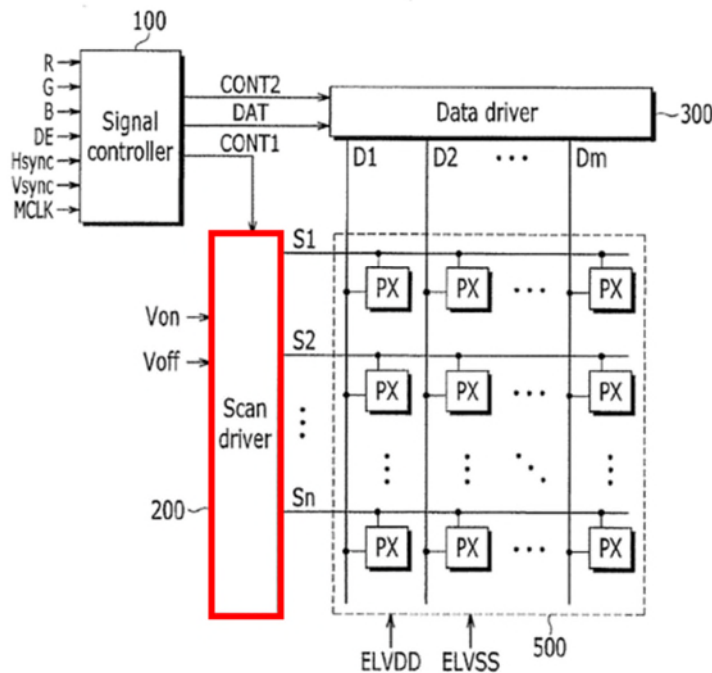
A. Chung

Chung teaches systems and methods relating to an OLED display device.

Ex.1004 ¶0063, Ex.1003 ¶¶100-102.

The display device includes a signal controller, a scan driver, a data driver, and a display unit:

FIG. 1

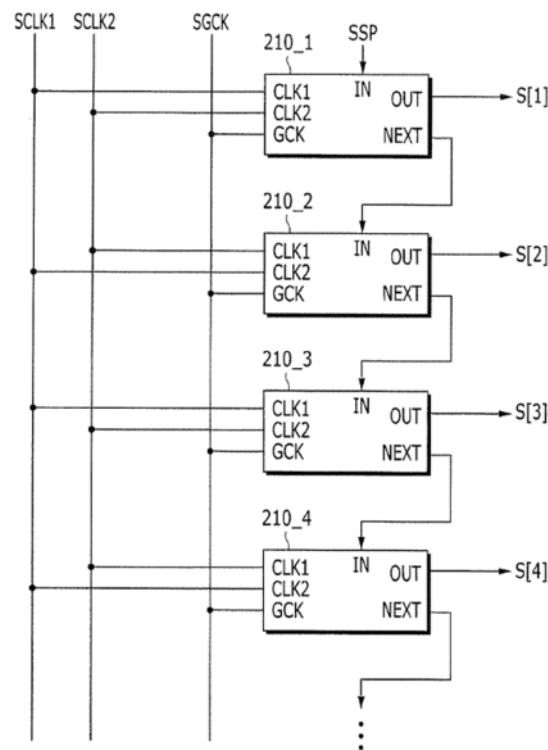


Id., Fig. 1, ¶0053.

Scan driver 200 outputs scan signals on scan lines S1-Sn that are used to

control the data signals output by data driver 300 to pixels PX in display unit 500 to control display of data. *Id.* ¶¶0056-0061. The scan driver provides a plurality of scan signals, *e.g.*, S[1] through S[4], that are output by a series of sequentially arranged scan driving blocks, *e.g.*, 210_1 through 210_4, located in the scan driver 200:

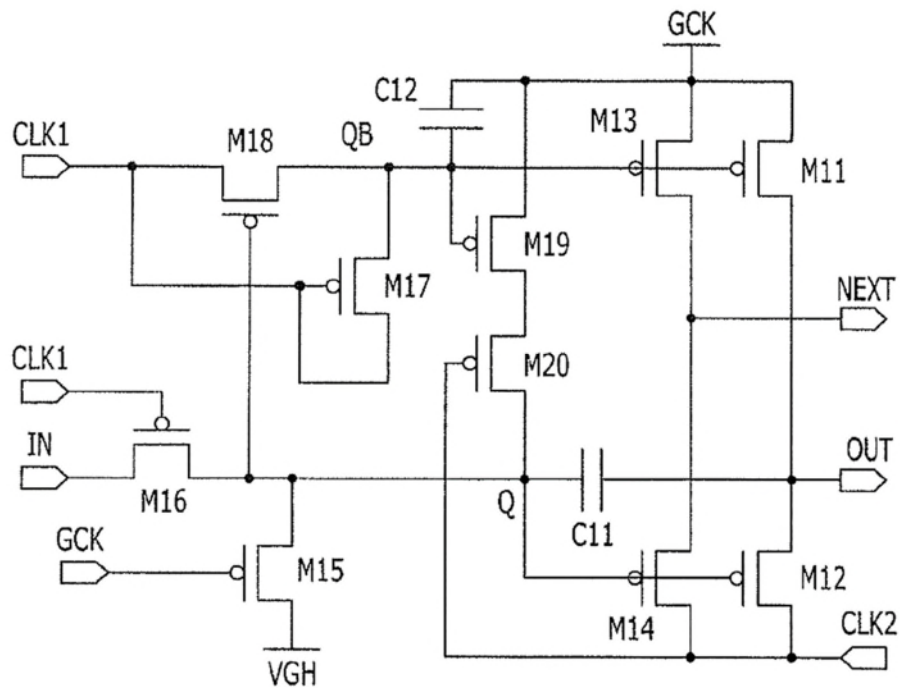
FIG. 3



Id., Fig. 3; ¶¶0067-0068.

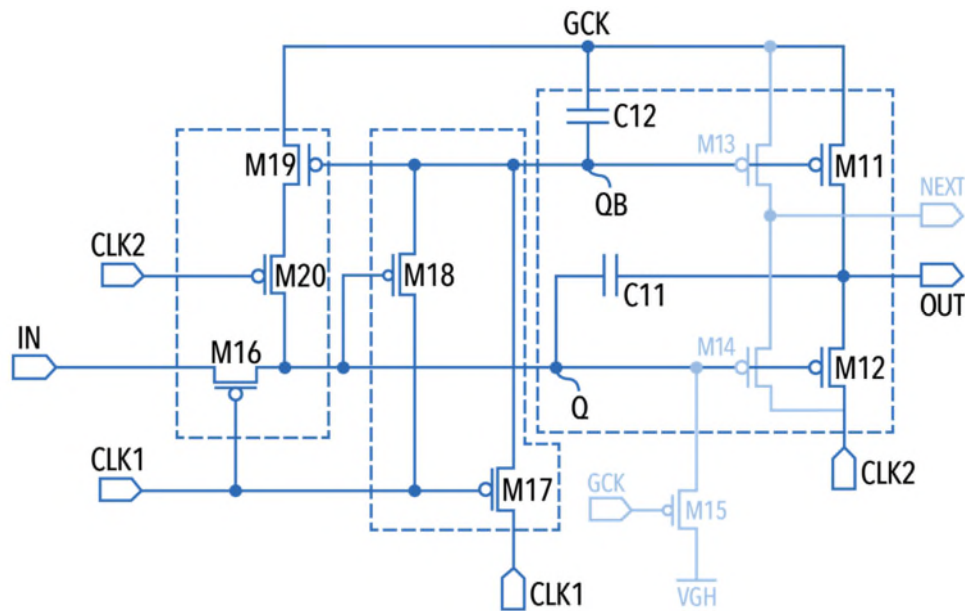
Each of these scan driving blocks is a stage circuit and includes input signals and components used to produce the output scan signals. Ex.1003 ¶204. An

exemplary embodiment of Chung's stage circuit is shown below:



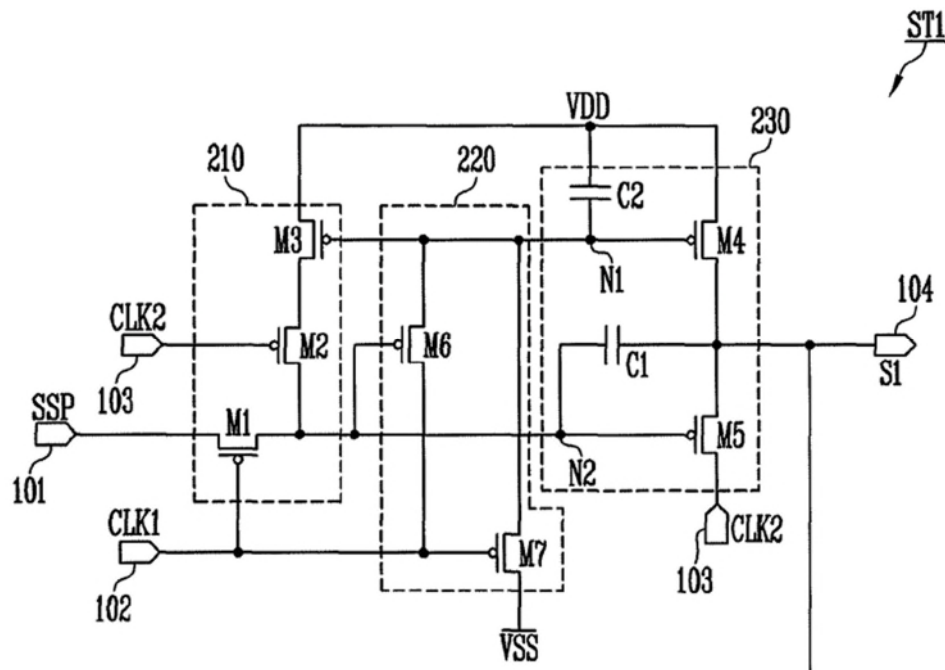
Ex.1004, Fig. 4; ¶¶0075-0089.

Rearranging the components while maintaining their connections results in the following identical circuit:



Ex.1004, Fig. 4 (components rearranged).

Comparing the Chung embodiment above with the preferred embodiment of the '593 patent below reveals that all of the same input/output signals and components are present in both.



Ex.1001, Fig. 3.

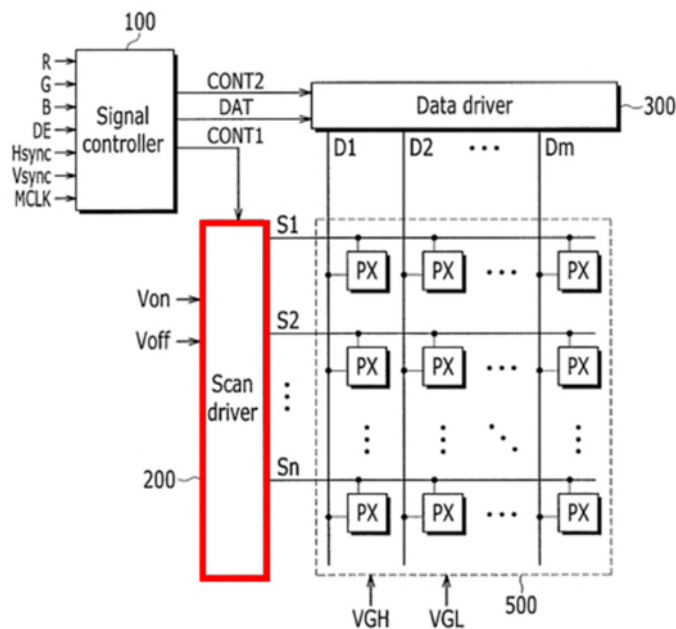
B. Kim

Kim teaches systems and methods relating to an OLED display device.

Ex.1005 ¶¶0082-0083, Ex.1003 ¶¶103-105.

The display device includes a signal controller, a scan driver, a data driver, and a display unit:

FIG. 1

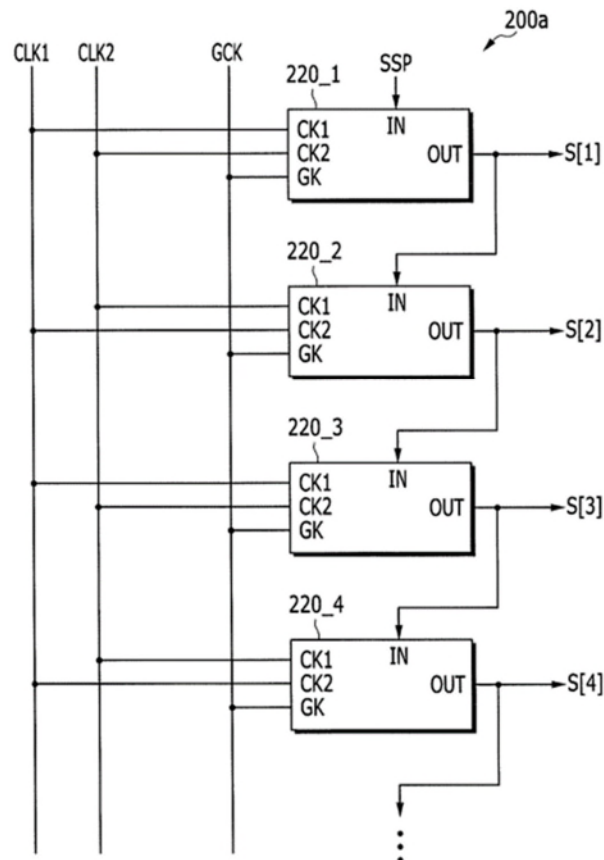


Ex.1005, Fig. 1, ¶¶0072.

Scan driver 200 outputs scan signals on scan lines S1-Sn that are used to control the data signals output by data driver 300 to pixels PX in display unit 500 to control display of data. *Id.* ¶¶0075-0078. The scan driver provides a plurality of

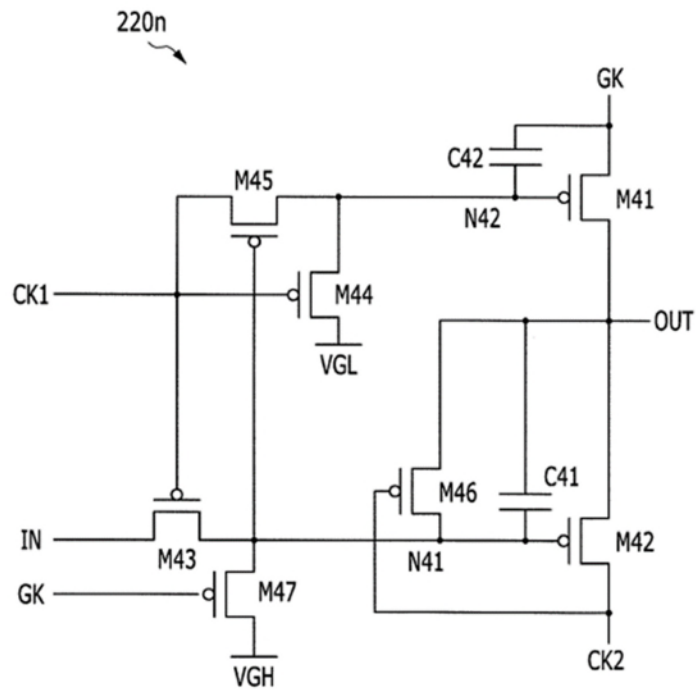
scan signals, *e.g.*, S[1] through S[4], that are output by a series of sequentially arranged scan driving blocks, *e.g.*, 220_1 through 220_4, located in the scan driver 200:

FIG. 8



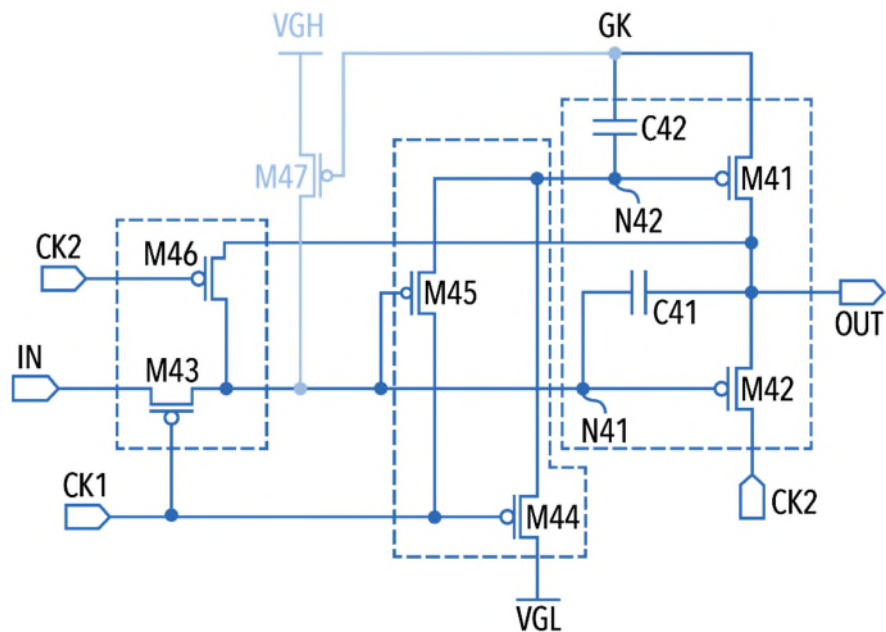
Id., Fig. 8; ¶0153.

Each of these scan driving blocks is a stage circuit and includes input signals and components used to produce the output scan signals. Ex.1003 ¶349. An exemplary embodiment of Kim's stage circuit is shown below:



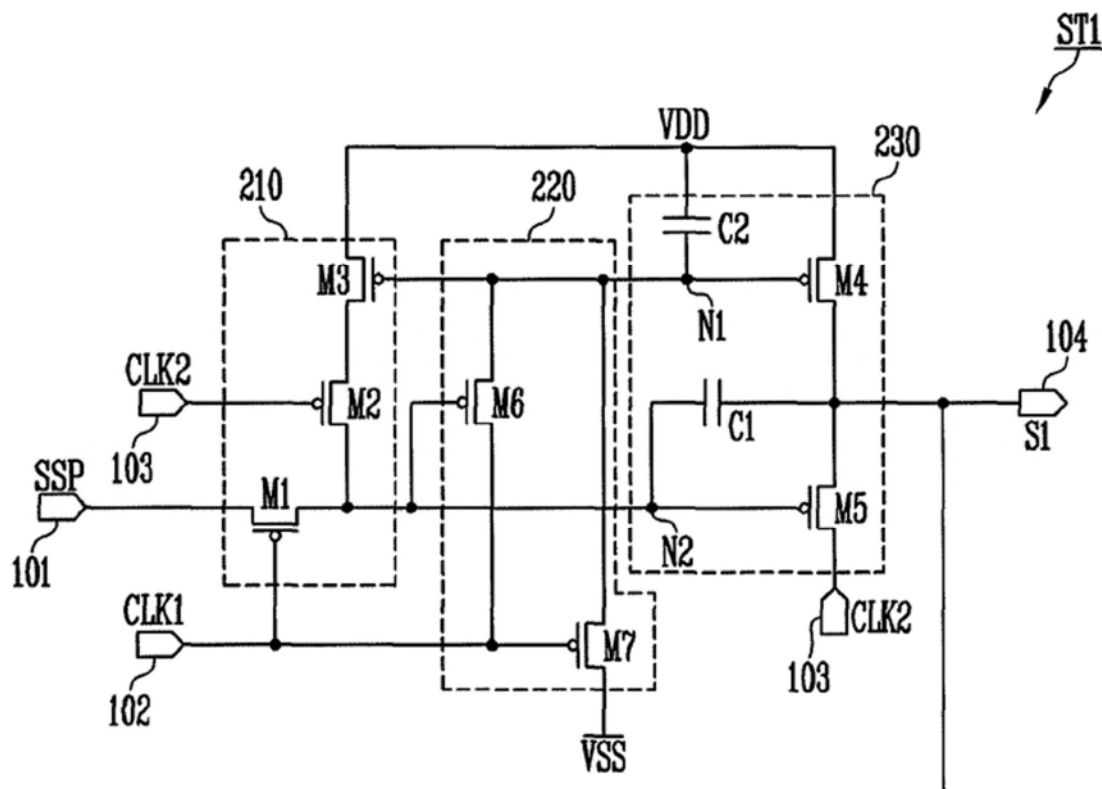
Ex.1005, Fig. 9; *id.* ¶¶0160-0169.

Rearranging the components while maintaining their connections results in the following identical circuit:



Ex.1005, Fig. 9 (components rearranged).

Comparing the Kim embodiment above with the preferred embodiment of the '593 patent below reveals that all of the same input/output signals and the same or similar components are present in both.

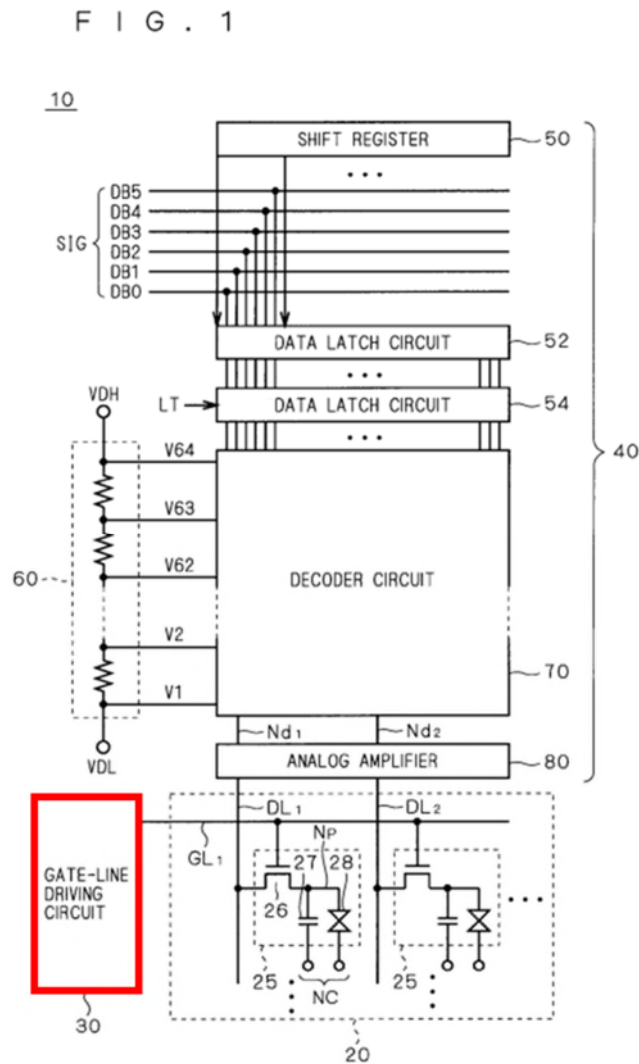


Ex.1001, Fig.3.

C. Tobita

Tobita discloses “a shift register for use as a scanning-line driving circuit for an image display apparatus.” Ex.1006 ¶0002, Ex.1003 ¶¶106-108. This circuit may be used in a liquid crystal display (“LCD”), which, like the later-developed OLED displays, comprises a matrix of pixels separated by scan and data lines.

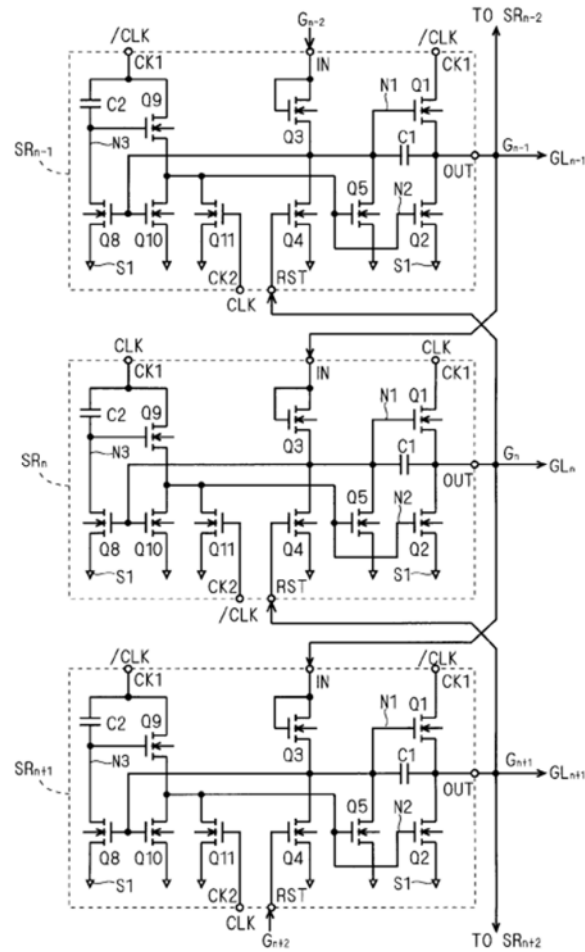
Ex.1006 ¶¶0004, 0059; Ex.1003 ¶¶74-76, 81, 107, 474. An embodiment of circuits driving such a display is shown below:



Ex.1006, Fig. 1.

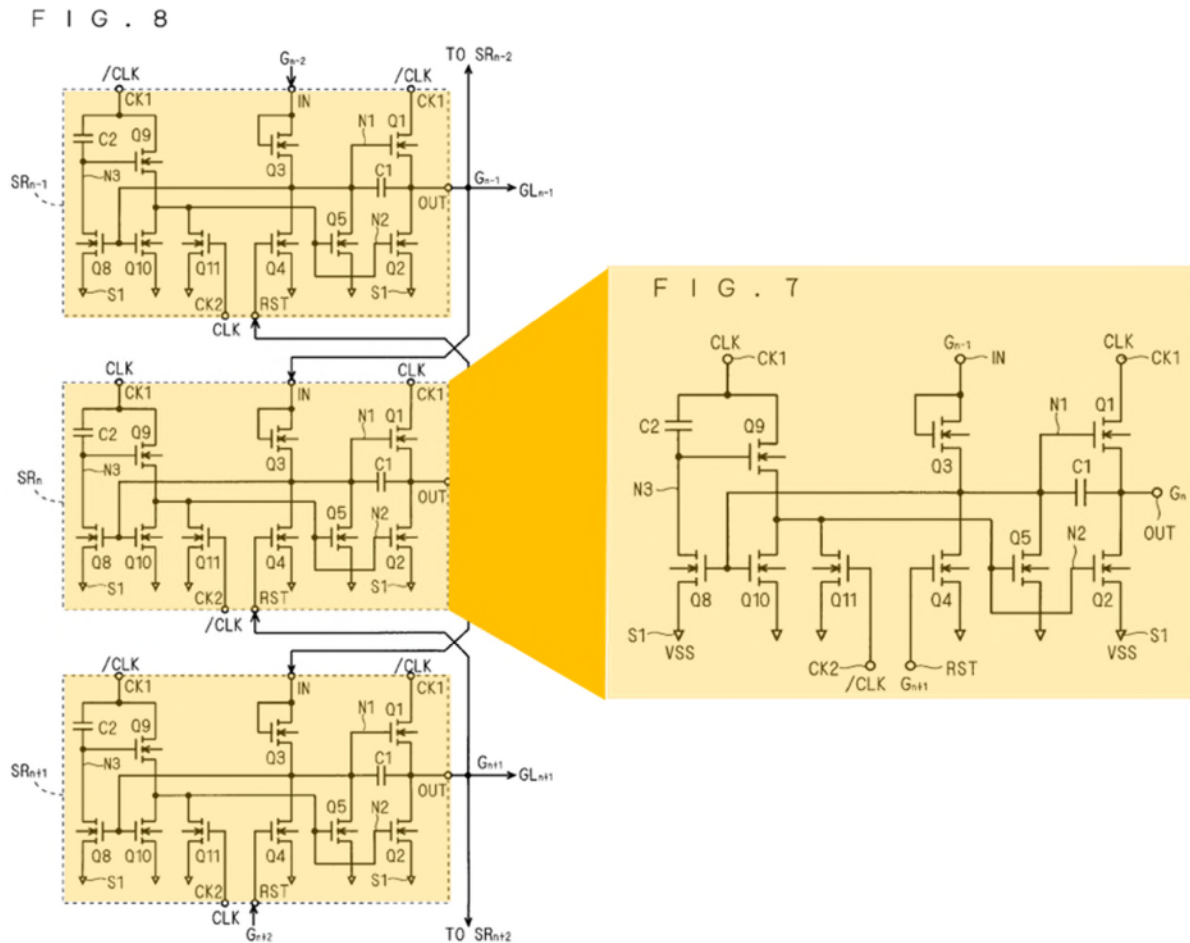
The gate-line driving circuit (or scanning-line driving circuit) 30 may comprise a cascade-connected, multistage shift register:

F I G . 8



Id., Fig. 8; see also *id.* ¶¶0027, 0117.

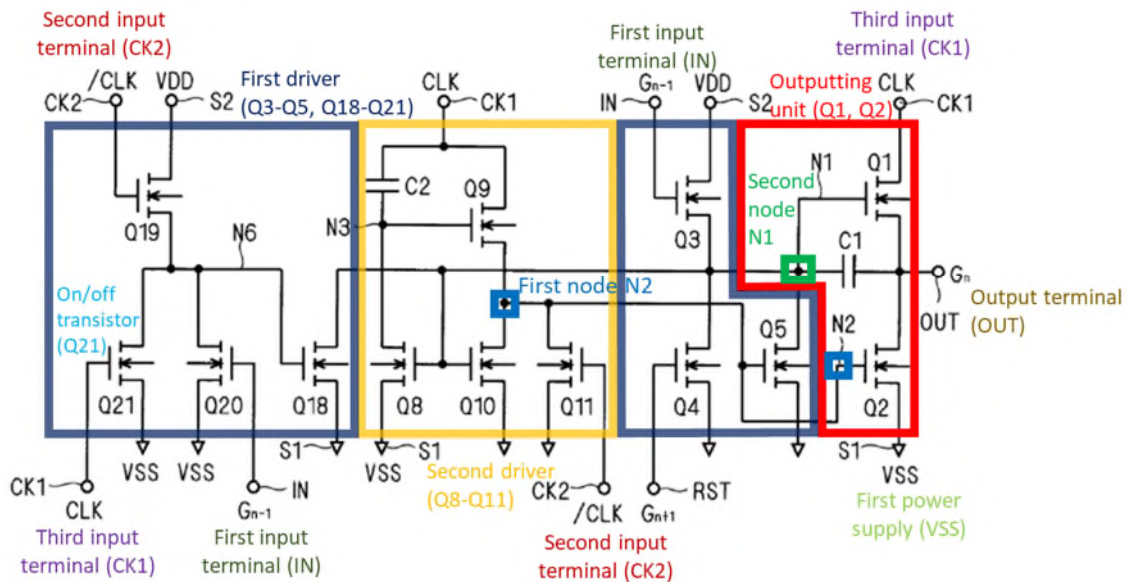
Each unit shift register SR_n in this multistage shift register can comprise the embodiment shown in Figure 7:



Id., Figs. 7-8, ¶¶0026-0027, 0117, 0167.

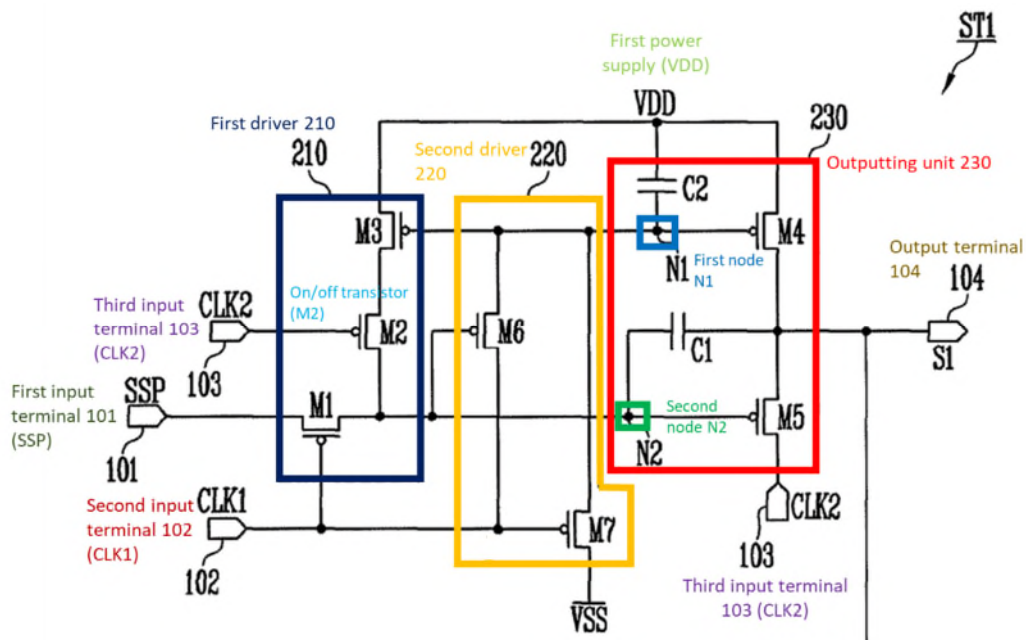
Embodiments of Figures 19 and 20 are variants of Figure 7. *Id.* ¶¶0168, 0172, 0177. In these figures, elements having similar or analogous functions are shown by the same reference designators. *Id.* The embodiments have the same functionality. Ex.1003 ¶109. The embodiment of Figure 20 is shown below:

FIG. 20



Ex.1006, Fig. 20.

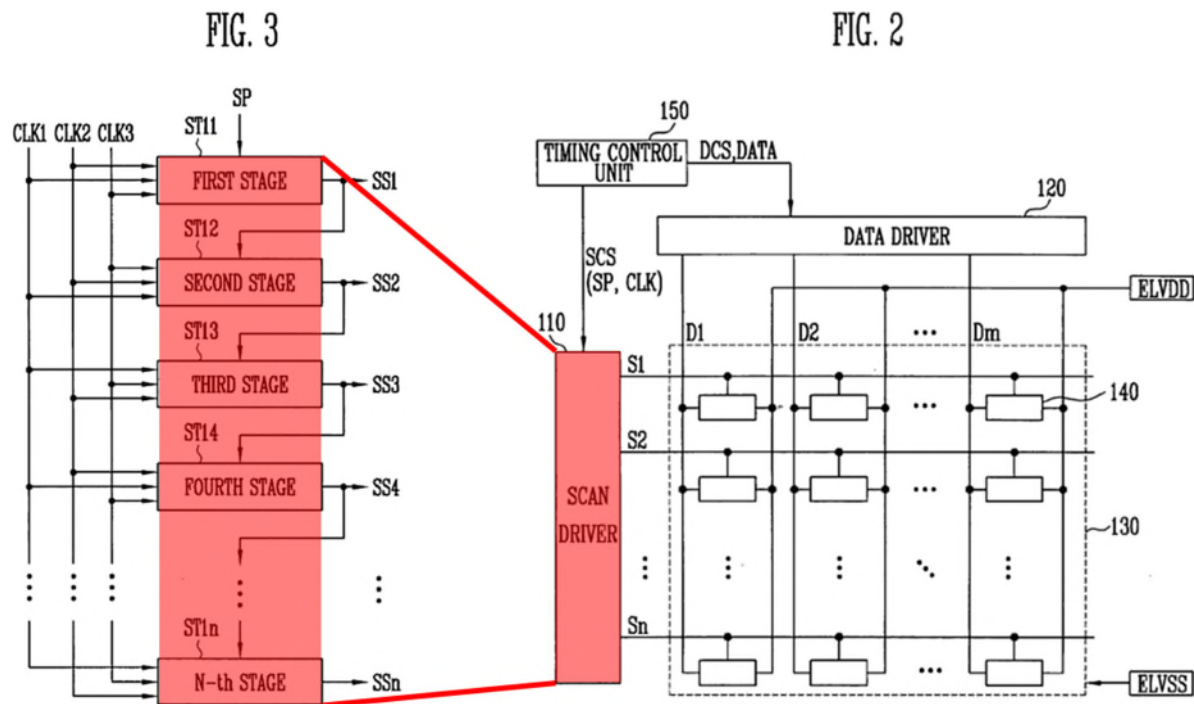
Comparing the Tobita embodiment above with the preferred embodiment of the '593 patent below reveals that all of the same input/output signals and the same or similar claimed features are present in both.



Ex.1001, Fig. 3.

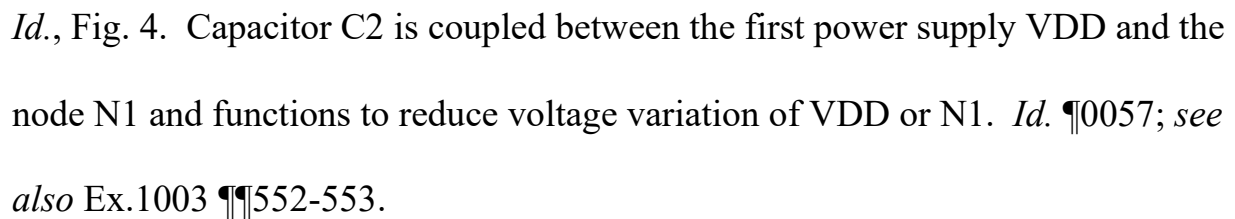
D. Jeong

Jeong discloses shift registers for a scan driver for driving pixels of an OLED display. Ex.1007 ¶0002, Ex.1003 ¶¶110-112.

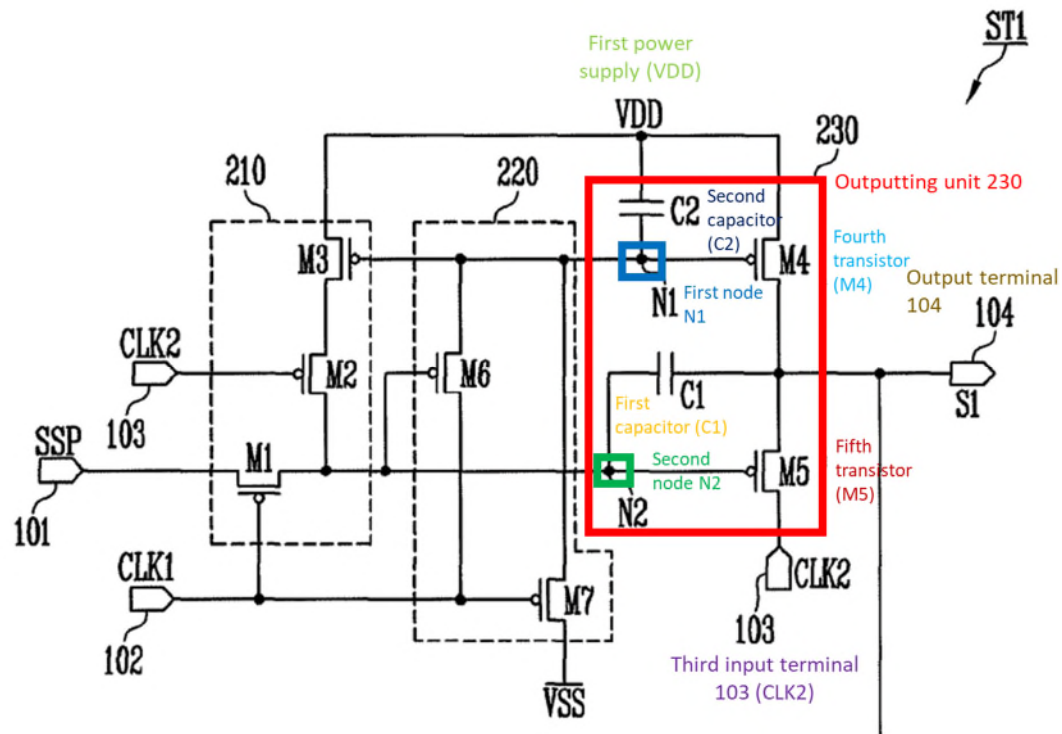


Ex.1007, Figs. 2-3.

Successive stages generate successive output signals SS1 through SSn, which are output to the respective scan lines. *Id.* ¶0041. Each stage of the scan driver comprises a shift register:



Comparing the Jeong embodiment above with the preferred embodiment of the '593 patent below reveals that all of the same input/output signals, nodes, and components of the outputting unit are present in both.



Ex.1001, Fig. 3.

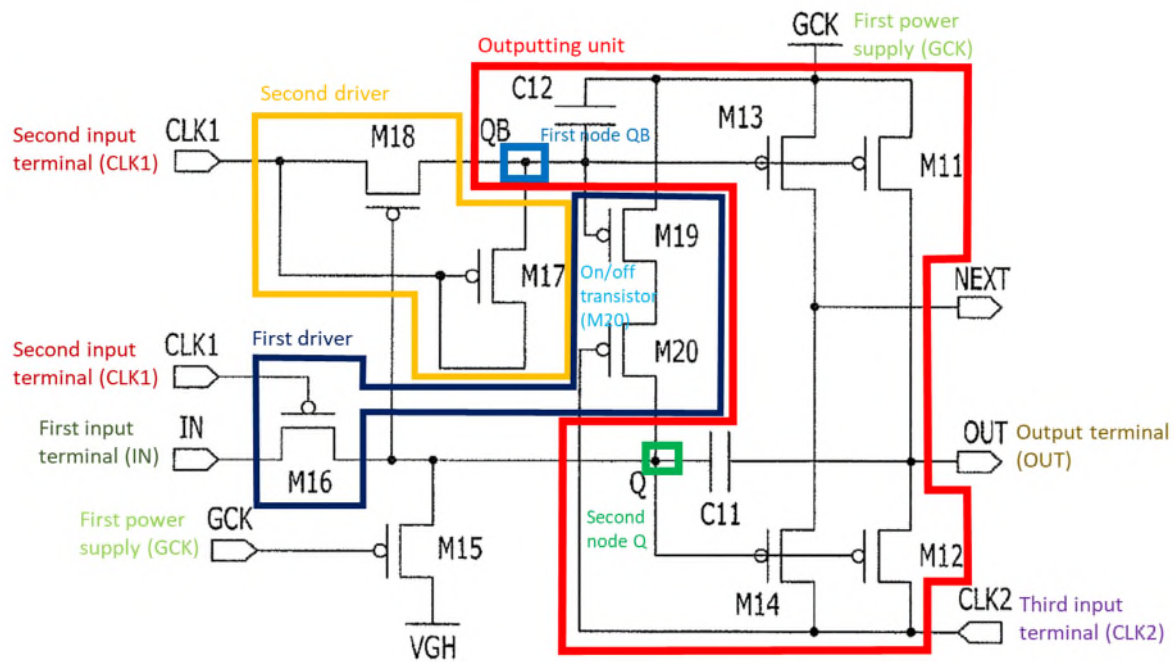
VIII. THE CHALLENGED '593 PATENT CLAIMS ARE UNPATENTABLE OVER THE PRIOR ART

A. GROUND 1: Chung Anticipates Claims 1-7, 9, 14-21, 23, and 25

1. Independent Claim 1

Chung anticipates Claim 1. Ex.1003 ¶¶118, 150.

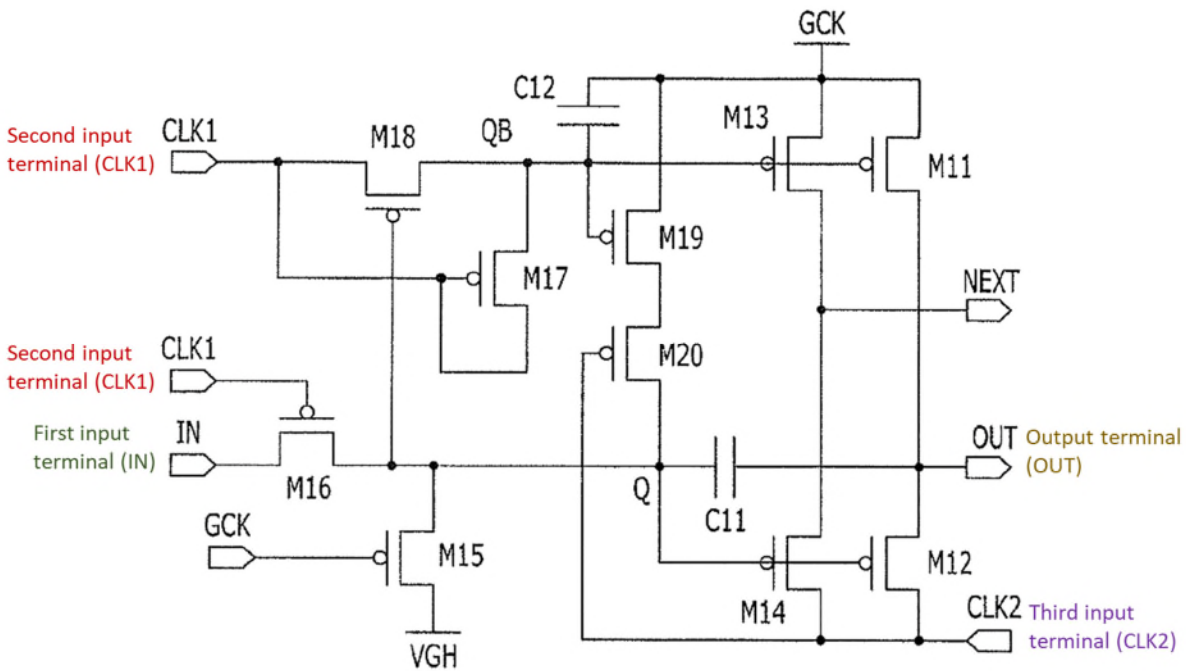
Chung depicts a stage circuit that is part of an OLED display, in which all of the signals and components recited in Claim 1 of the '593 patent are present and operate as required by the Claim, as discussed in more detail below.



Ex.1004, Fig. 4; Ex.1003 ¶117.

a) [1-PRE]

Chung discloses “[a] stage circuit having a first input terminal [IN], a second input terminal [CLK1], a third input terminal [CLK2], and an output terminal [OUT]”:

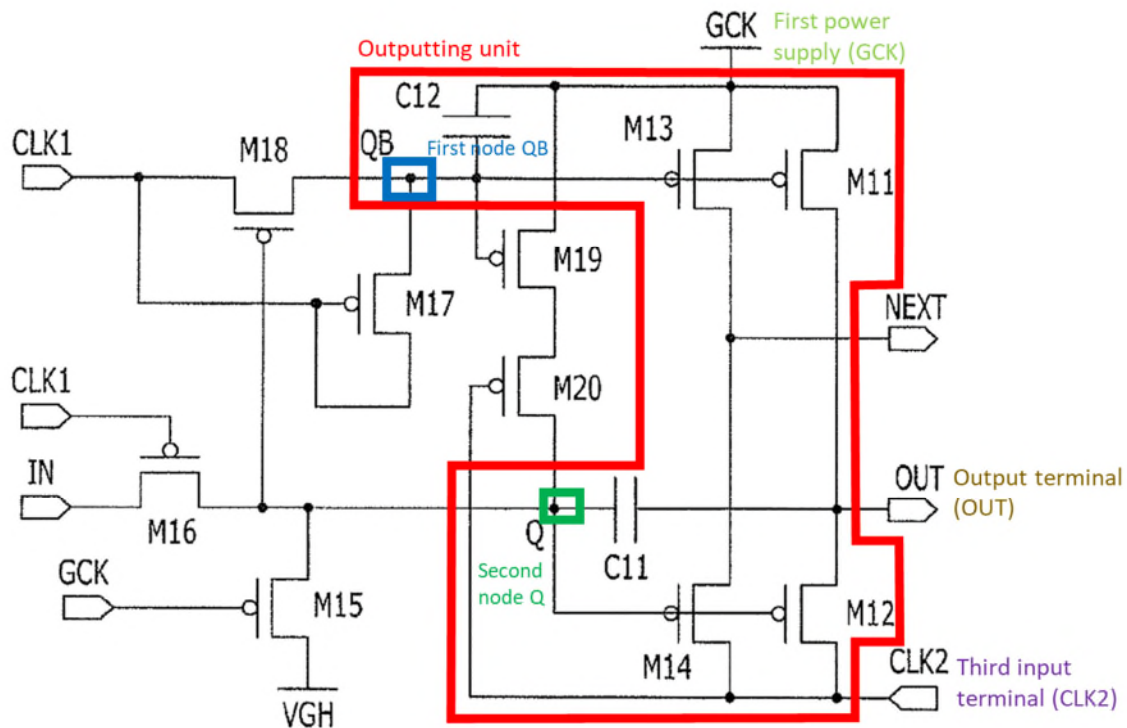


Id., Fig. 4; *see also*, e.g., *id.*, Fig. 3, ¶¶0075-0089; Ex.1003 ¶¶119-123.

b) Element [1-A]

Chung discloses “an **outputting unit** having a **first node [QB]** and a **second node [Q]**, the **outputting unit** to supply a voltage of a **first power supply [GCK]** to the **output terminal [OUT]** according to a voltage applied to the **first node [QB]** and a signal [SCLK2] of the **third input terminal [CLK2]** to the **output terminal [OUT]** according to a voltage applied to the **second node [Q]**.” Ex.1003 ¶¶124-135.

Chung’s **outputting unit** contains all of the required components:

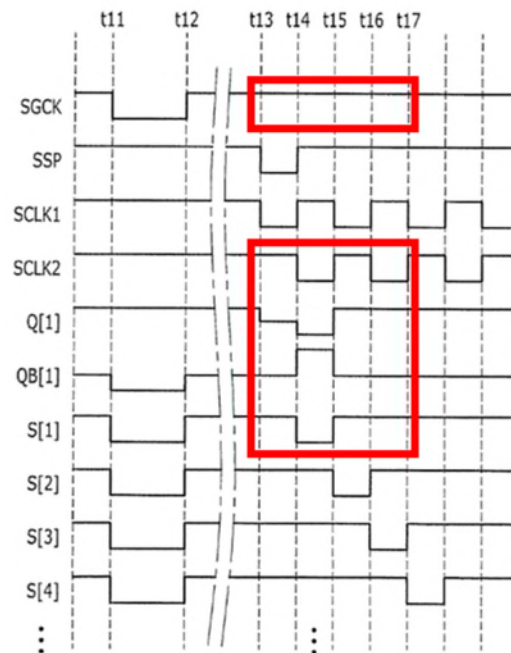


Ex.1004, Fig. 4; *see also id.* ¶¶0077-0078, 0087-0088; Ex.1003 ¶¶129-134.

Chung further describes the outputting unit functioning in a manner matching the element [1-A] requirement. For example, during the t13-to-t14 period, both first node QB and second node Q are low voltage, turning on transistors M11 and M12 and enabling the output terminal OUT to take on the logic-high state of both the first power supply GCK and the third input terminal CLK2, respectively. Ex.1004 ¶0099. During the t14-to-t15 period, first node QB is high, turning off transistor M11; second node Q is low, turning on M12 and enabling the output terminal OUT to take on the logic-low state of the third input terminal CLK2. *Id.* ¶0100. During the t15-to-t16 and t16-to-t17 periods, the

second node Q is high, turning off transistor M12; the first node QB is low, turning on transistor M11 and enabling the output terminal OUT to take on the logic-high state of the first power supply GCK. *Id.* ¶¶0101-0102.

FIG. 5

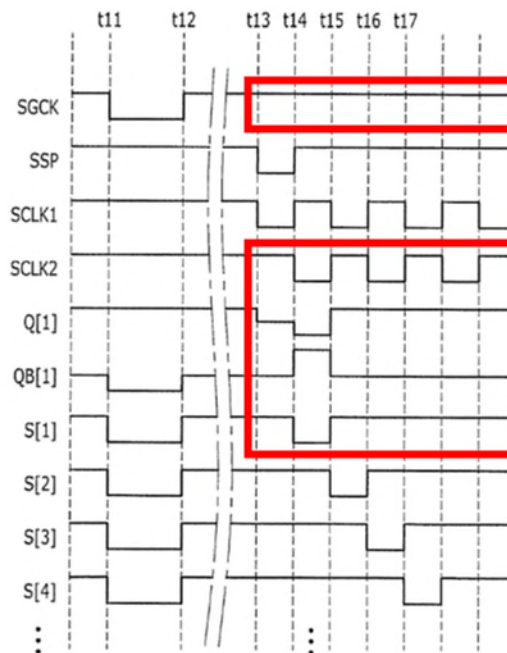


Id., Fig. 5.

In all of these scan periods, terminal GCK supplies an operational high voltage level. *Id.* ¶0097. Thus, a POSITA would understand GCK is a power supply during scan operations. Ex.1003 ¶¶125-128.

Specifically, the signal SGCK of the first power supply GCK stays high at the level of the first power supply voltage during periods of scan operation:

FIG. 5



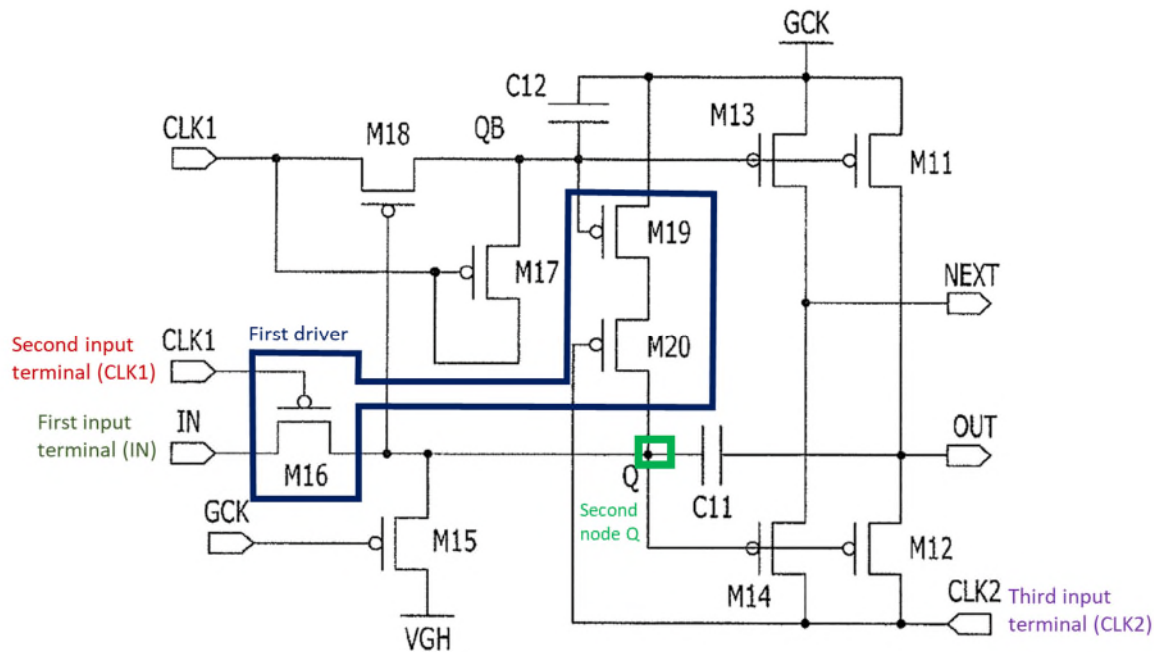
Ex.1004, Fig. 5; *see also* Ex.1003 ¶128.

SGCK only goes low during a reset-and-threshold-voltage-compensation step “during which the scan signals of the gate-on voltage are concurrently (e.g., simultaneously) output to the plurality of scan lines S1-Sn.” Ex.1004 ¶0093; *see also id.* ¶0058. The actual scan operations for which the circuit is designed utilize GCK as a constant high-voltage power. Ex.1003 ¶127.

c) Element [1-B]

Chung discloses “a first driver to control the voltage of the second node [Q] in accordance with signals of the first input terminal [IN], the second input terminal [CLK1], and the third input terminal [CLK2].” Ex.1003 ¶136.

Chung's first driver contains all of the required components:

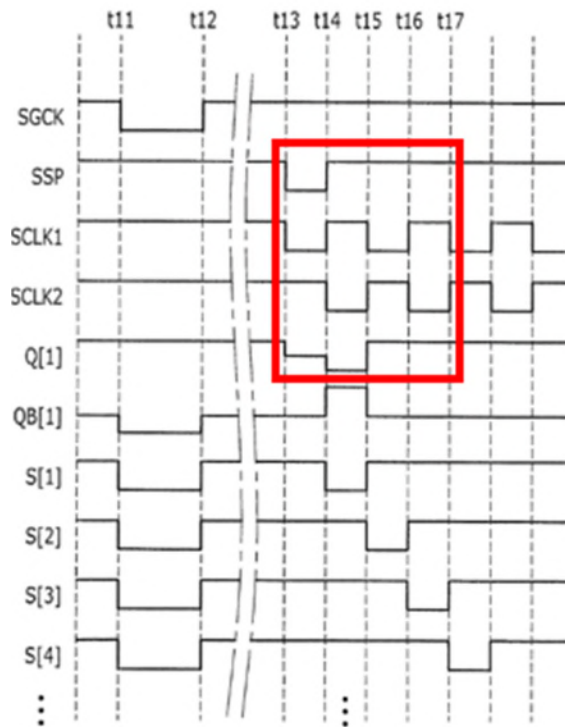


Ex.1004, Fig. 4; *see also id.* ¶¶0081-0082, 0085-0086; Ex.1003 ¶136.

Chung further describes the first driver functioning in a manner matching the element [1-B] requirement. For example, during the t13-to-t14 period, transistor M16 is turned on by the signal SCLK1 of the second input terminal CLK1. Thus, the signal SSP of the first input terminal IN is transmitted to the second node Q.

Ex.1004 ¶0099. During the t15-to-t16 period, transistor M16 is again turned on by SCLK1, thus, the signal SSP of the first input terminal IN is transmitted to the second node Q. *Id.* ¶0101. During the t16-to-t17 period, transistor M16 is turned off by SCLK1. *Id.* ¶0102. M20 is turned on by the signal SCLK2 of the third input terminal CLK2 while M19 is on, coupling the voltage of the first power

supply GCK to the second node Q, pulling Q to a logic-high state. *Id.*

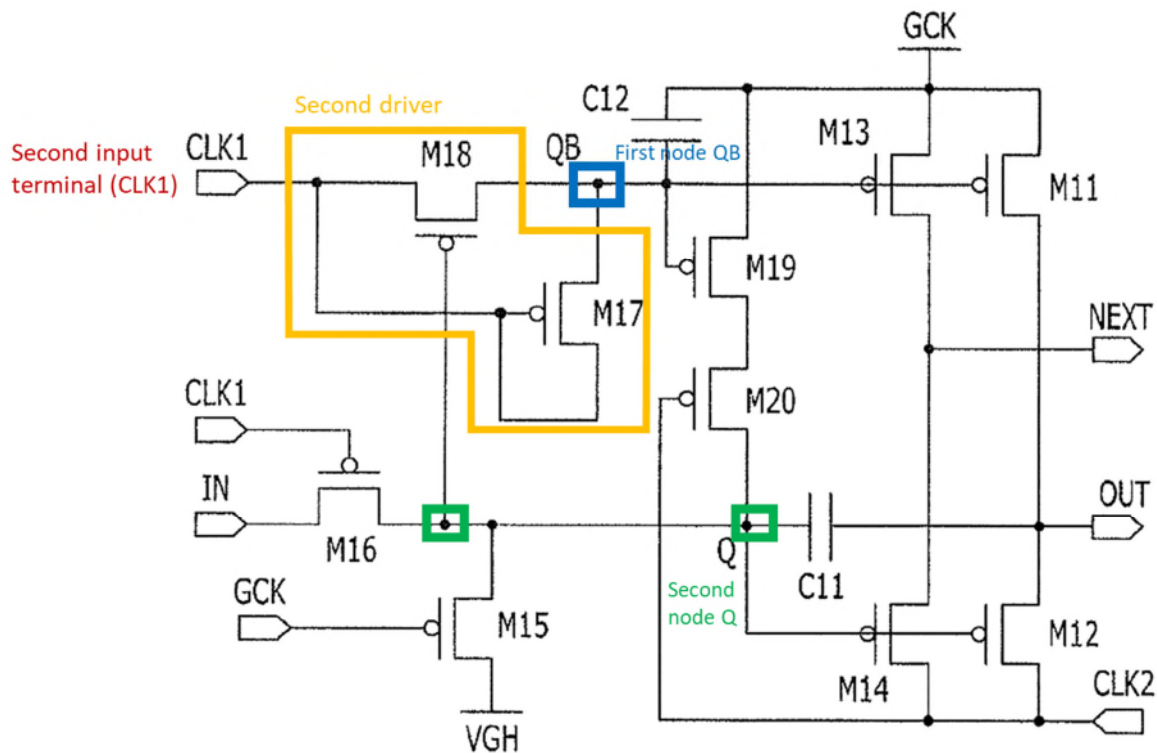


Id., Fig. 5; *see also* Ex.1003 ¶¶136-141.

d) Element [1-C]

Chung discloses “a **second driver** to control the voltage of the **first node [QB]** in accordance with the signal [SCLK1] of the **second input terminal [CLK1]** and the voltage of the **second node [Q]**.” Ex.1003 ¶142.

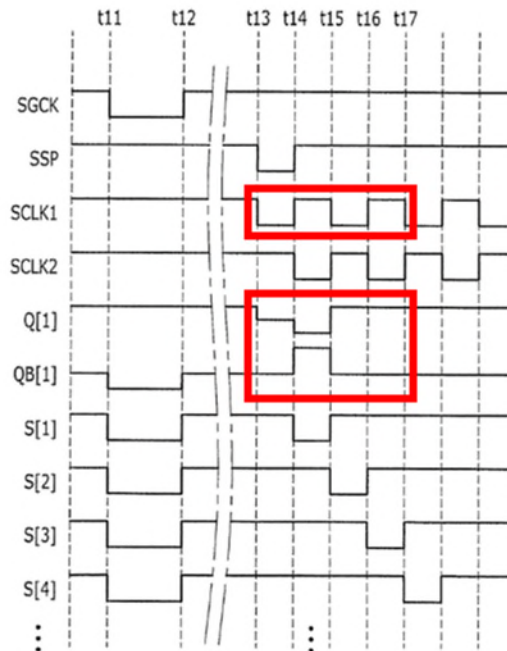
As shown in below, Chung’s **second driver** contains all of the required components:



Ex.1004, Fig. 4; *see also id.* ¶¶0083-0084; Ex.1003 ¶142.

Chung further describes the second driver functioning in a manner matching the element [1-C] requirement. For example, during the t13-to-t14 period, transistor M17 is turned on by the signal SCLK1 of the second input terminal CLK1, thus, SCLK1 is transmitted to the first node QB. Ex.1004 ¶0099. During the t14-to-t15 period, M17 is turned off by SCLK1, M18 is turned on by the low-level voltage of the second node Q, and SCLK1 is transmitted to the first node QB. *Id.* ¶0100. During the t15-to-t16 period, transistor M17 is again turned on by SCLK1. Thus, SCLK1 is transmitted to the first node QB. *Id.* ¶0101.

FIG. 5

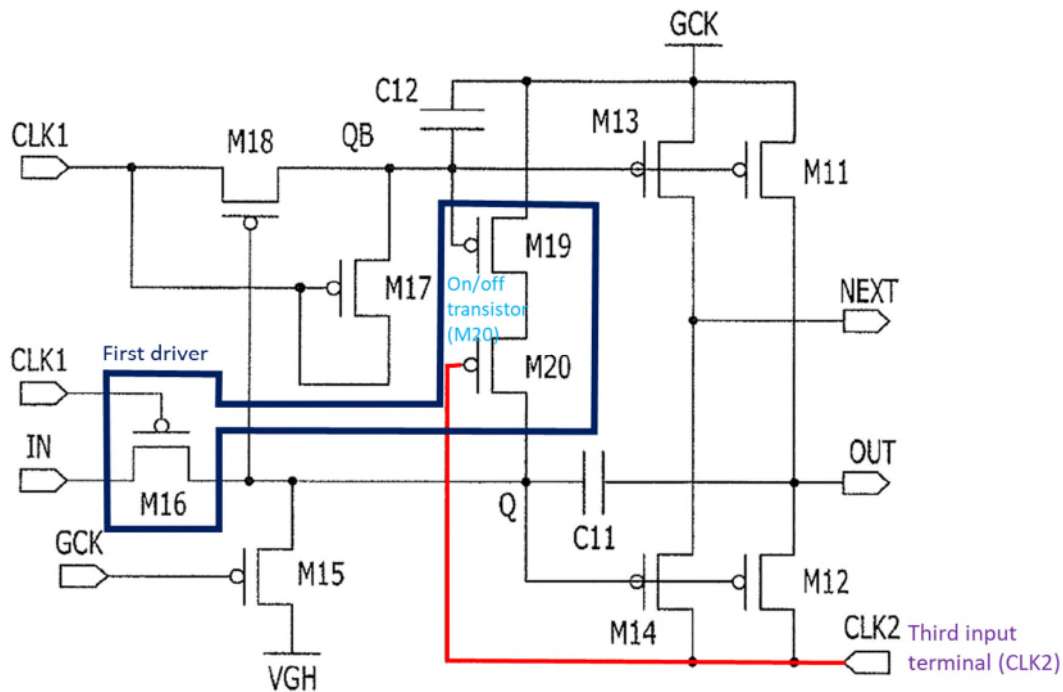


Id., Fig. 5; see also Ex.1003 ¶¶142-147

e) Element [1-D]

Chung discloses that “the signal [SCLK2] of the third input terminal [CLK2] directly controls an on/off operation of a transistor [M20], the transistor [M20] included in the first driver.” Ex.1003 ¶148.

The third input terminal CLK2 is directly coupled to the gate electrode of transistor M20, which is part of the first driver:



Ex.1004, Fig. 4; *see also id.* ¶0086.

Chung further describes the first driver functioning in a manner matching the element [1-D] requirement. Because the signal SCLK2 of the third input terminal CLK2 is coupled to the gate electrode of M20, SCLK2 directly controls the on/off operation of M20. Ex.1003 ¶148. For example, during the t16-to-t17 period, transistor M20 is turned on by SCLK2. Ex.1004 ¶0102.

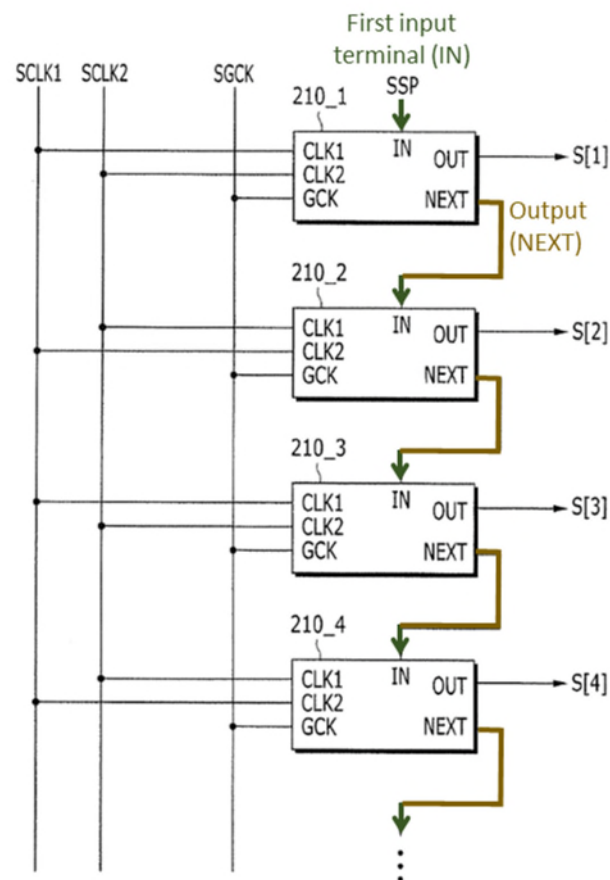
2. Claim 2

Claim 2 depends from Claim 1 and requires that “the first input terminal [IN] receives an output signal [NEXT] of a previous stage circuit or a start signal [SSP],” “the second input terminal receives a first clock signal,” and “the third input terminal receives a second clock signal.”

Chung discloses these additional limitations. Ex.1003 ¶152.

Preliminarily, Claim 2 recites “an output signal” without reciting any relationship of this signal with the output terminal of Claim 1. *Id.* ¶153. Chung’s first input terminal IN receives start signal SSP in the first stage of the stage circuit, and receives an output signal from terminal NEXT of the previous stage in subsequent stages:

FIG. 3



Ex.1004, Fig. 3; *see also id.* ¶¶0073-0074; Ex.1003 ¶154.

Additionally, the stage circuit has a second input terminal CLK1 that receives first clock signal SCLK1, and a third input terminal CLK2 that receives second clock signal SCLK2. *See* Section VIII.A.1.c; Ex.1003 ¶154.

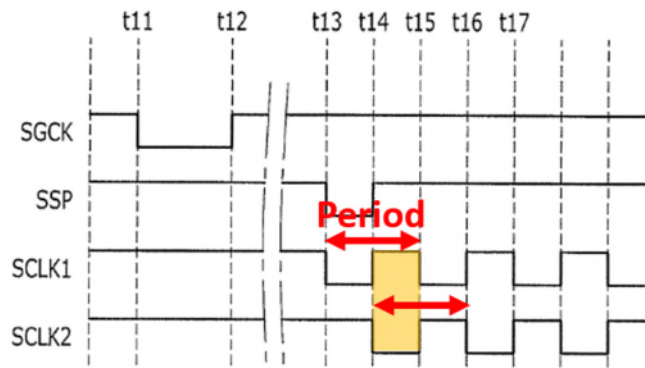
3. Claim 3

Claim 3 depends from Claim 2 and requires that “the first clock signal and the second clock signal have the same period and have phases that do not overlap.”

Chung discloses this additional limitation. Ex.1003 ¶157.

First clock signal SCLK1 and second clock signal SCLK2 have the same period and phases that do not overlap, *e.g.*, SCLK1 is high when SCLK2 is low:

FIG. 5



Ex.1004, Fig. 5 (partial); *see also id.* ¶¶0098, 0103; Ex.1003 ¶¶157-159.

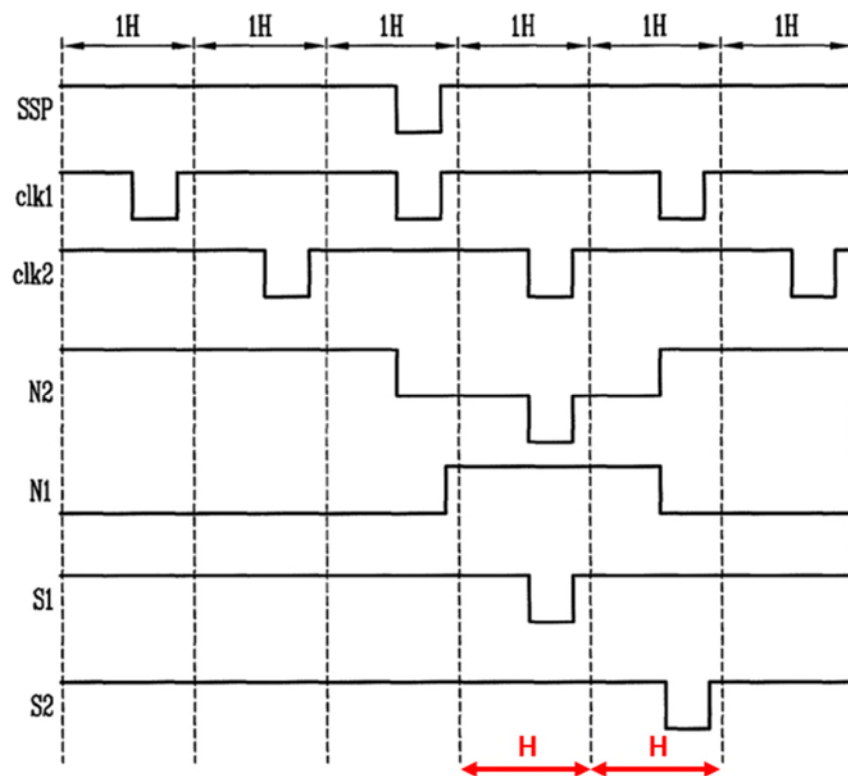
4. Claim 4

Claim 4 depends from Claim 3 and requires that “the first clock signal and the second clock signal have a period equal to two horizontal periods 2H and are

supplied in different horizontal periods as low signals.”

Chung discloses this additional limitation. Ex.1003 ¶168.

The '593 patent refers to “a period in which a scan signal is supplied to one scan line” as an exemplary horizontal period. Ex.1001 at 5:18-20. This period corresponds to the time span between outputs of successive stages, e.g., between S1 and S2:

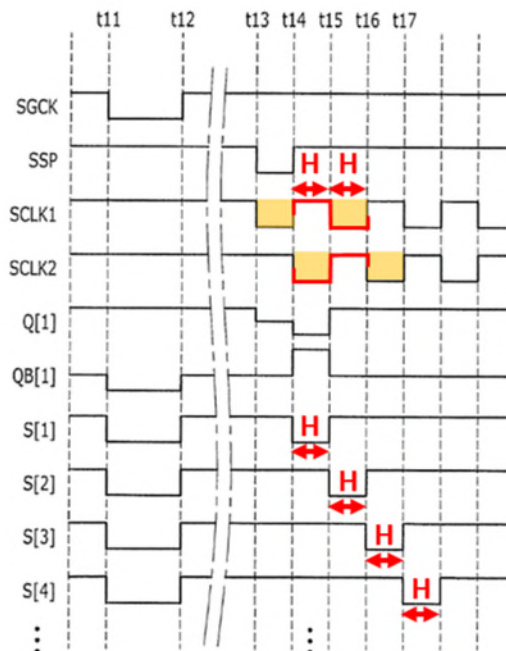


Ex.1001, Fig. 4; Ex.1003 ¶¶164-165.

Referring to a horizontal period as the period between outputs of successive stages, e.g., S[1] and S[2], both of Chung’s first and second clock signals SCLK1 and SCLK2 have a (clock) period equal to two horizontal periods 2H (e.g., t14

through t16). Further, first clock signal SCLK1 is low during the t13-to-t14 and t15-to-t16 periods, and second clock signal SCLK2 is low during the (different) t14-to-t15 and t16-to-t17 periods.

FIG. 5



Ex.1004, Fig. 5; *see also* Ex.1003 ¶¶163-167.

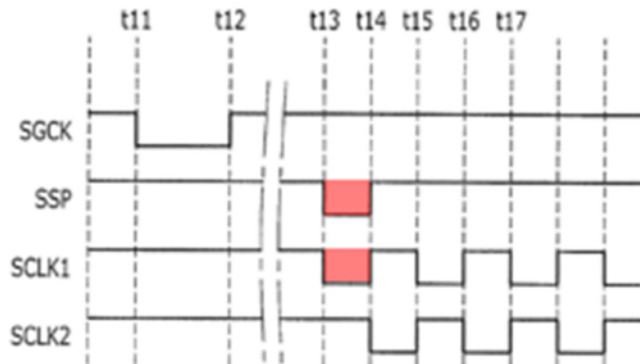
5. Claim 5

Claim 5 depends from Claim 2 and requires that “the start signal is supplied to overlap the first clock signal.”

Chung discloses this additional limitation. Ex.1003 ¶172.

The active logic-low state of start signal SSP overlaps with the active logic-low state of first clock signal SCLK1 between times t13 and t14.

FIG. 5



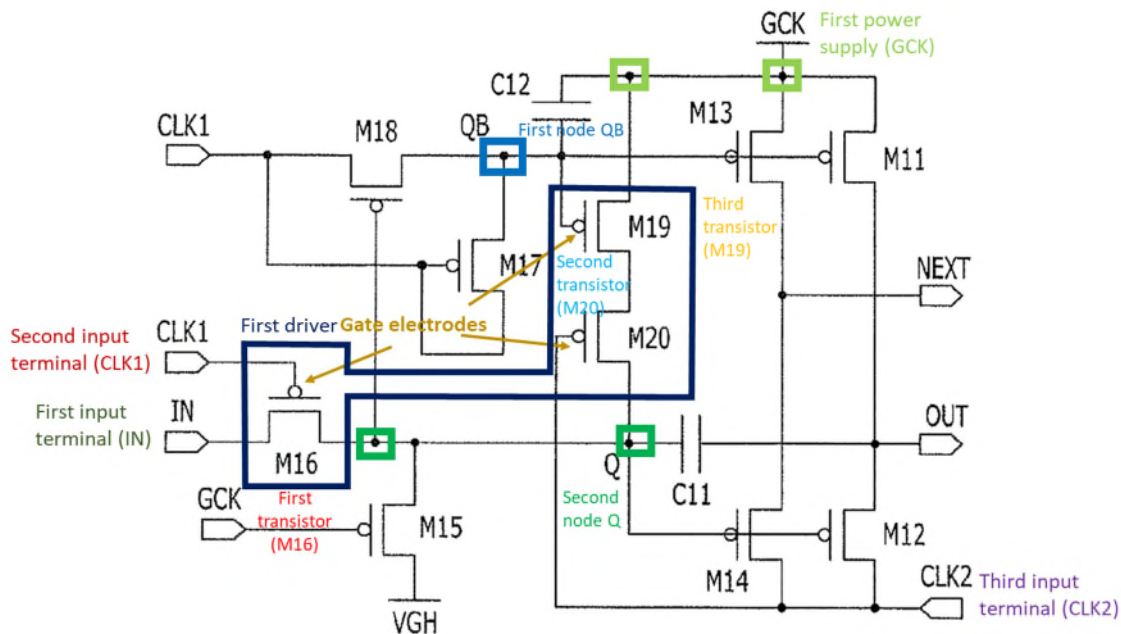
Ex.1004, Fig. 5 (partial); *see also id.* ¶0098; Ex.1003 ¶¶170-171.

6. Claim 6

Claim 6 depends from Claim 2 and requires that “the first driver includes: a first transistor [M16] between the first input terminal [IN] and the second node [Q], the first transistor [M16] having a gate electrode coupled to the second input terminal [CLK1],” “a second transistor [M20] and a third transistor [M19] serially positioned between the second node [Q] and the first power supply [GCK],” that “a gate electrode of the second transistor [M20] is coupled to the third input terminal [CLK2],” and that “a gate electrode of the third transistor [M19] is coupled to the first node [QB].”

Chung discloses these additional limitations. Ex.1003 ¶176.

Chung’s first driver contains all of the required components, arranged in the recited configuration:



Ex.1004, Fig. 4; *see also id.* ¶¶82, 85-86; Ex.1003 ¶¶174-175.

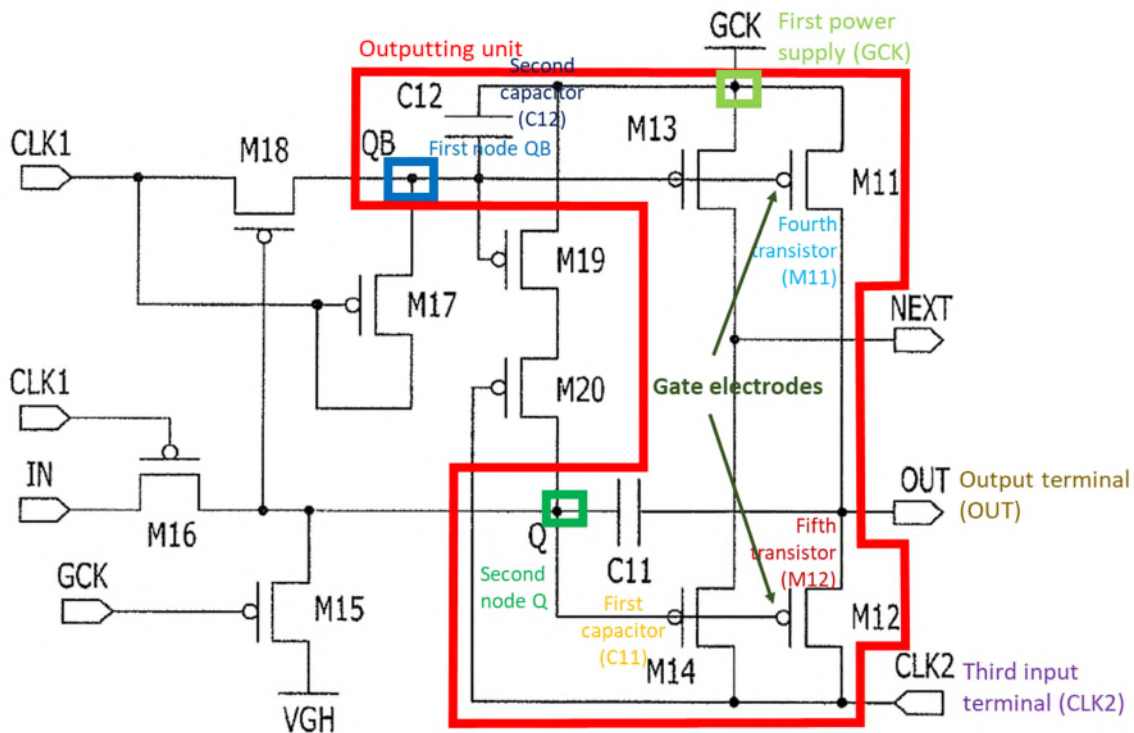
7. Claim 7

Claim 7 depends from Claim 2 and requires that “the **outputting unit** includes: a **fourth transistor [M11]** between the **first power supply [GCK]** and the **output terminal [OUT]**, the **fourth transistor [M11]** having a gate electrode coupled to the **first node [QB]**,” “a **fifth transistor [M12]** between the **output terminal [OUT]** and the **third input terminal [CLK2]**, the **fifth transistor [M12]** having a gate electrode coupled to the **second node [Q]**,” “a **first capacitor [C11]** between the **second node [Q]** and the **output terminal [OUT]**,” and “a **second capacitor [C12]** between the **first node [QB]** and the **first power supply [GCK]**.”

Chung discloses these additional limitations. Ex.1003 ¶180.

Chung’s **outputting unit** contains all of the required components, arranged in

the recited configuration:



Ex.1004, Fig. 4; *see also id.* ¶¶0077-0078, 0087-0088; Ex.1003 ¶¶178-179.

8. Claim 9

Claim 9 depends from Claim 2 and requires that “the **second driver** includes: a **sixth transistor** [M18] between the **first node** [QB] and the **second input terminal** [CLK1], the **sixth transistor** [M18] having a **gate electrode** coupled to the **second node** [Q],” and “a **seventh transistor** [M17] between the **first node** [QB] and the **second input terminal** [CLK1], the **seventh transistor** [M17] being diode connected.”

Chung discloses these additional limitations. Ex.1003 ¶184.

The diagram illustrates a 2T1M1C CMOS circuit with the following components and annotations:

- Inputs:** CLK1 (labeled "Second input terminal (CLK1)"), IN, CLK2, GCK, and VGH.
- Transistors:** M11, M12, M13, M14, M15, M16, M17, M18, M19, and M20.
- Capacitors:** C11 and C12.
- Nodes:** QB (labeled "First node QB"), Q (labeled "Second node Q"), and a node labeled "Gate electrode".
- Annotations:**
 - A yellow box highlights the "Second driver" consisting of transistors M18 and M17.
 - M18 is labeled "Sixth transistor (M18)".
 - M17 is labeled "Seventh transistor (M17)".
 - A green box highlights the node Q.
 - A blue box highlights the node QB.
- Connections:** The circuit includes various interconnections between the gates of the transistors, the nodes QB and Q, and the input/output terminals.

9. Claim 14

Chung discloses this additional limitation. Ex.1003 ¶188.

Because the second node Q is coupled to first power supply GCK through transistor M20, when M20 is turned on, the voltage of the first power supply GCK

can be transferred to the second node Q. Ex.1004 ¶¶0086, Ex.1003 ¶187. For example, during the t16-to-t17 period, transistor M20 is turned on while M19 is also on, and the logic-high voltage level of SGCK is transmitted to the second node Q1. Ex.1004 ¶0102.

10. Independent Claim 15

Chung anticipates Claim 15. Ex.1003 ¶189.

a) [15-PRE]

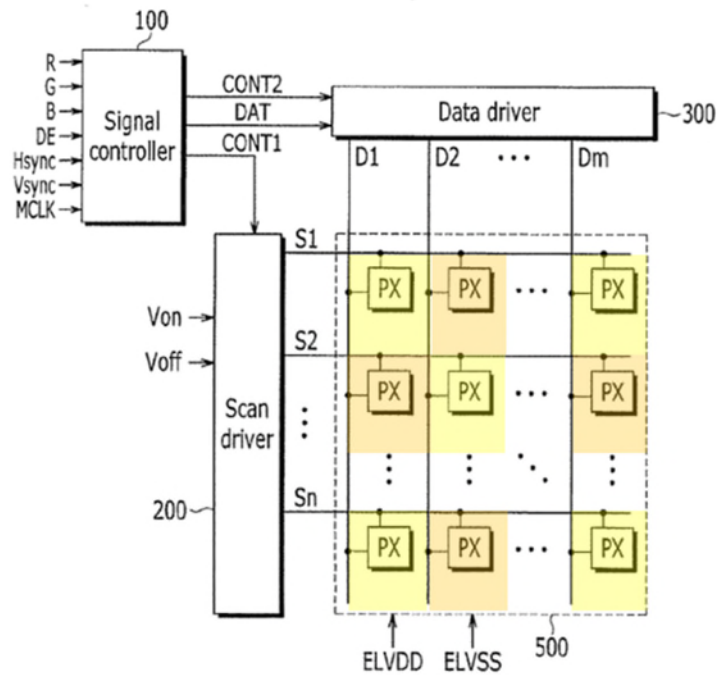
Chung discloses “[a]n organic light emitting display.” *See, e.g.*, Ex.1004, ¶0063 (“the display device according to the exemplary embodiment of the present invention is described as an organic light emitting diode display”), Fig. 2; Ex.1003 ¶¶191-192.

b) Element [15-A]

Chung discloses “pixels positioned in regions partitioned by scan lines and data lines.” Ex.1003 ¶193.

Chung depicts a plurality of pixels PX positioned in regions partitioned by scan lines S1-Sn and data lines D1-Dm, some of which are shaded for illustration:

FIG. 1



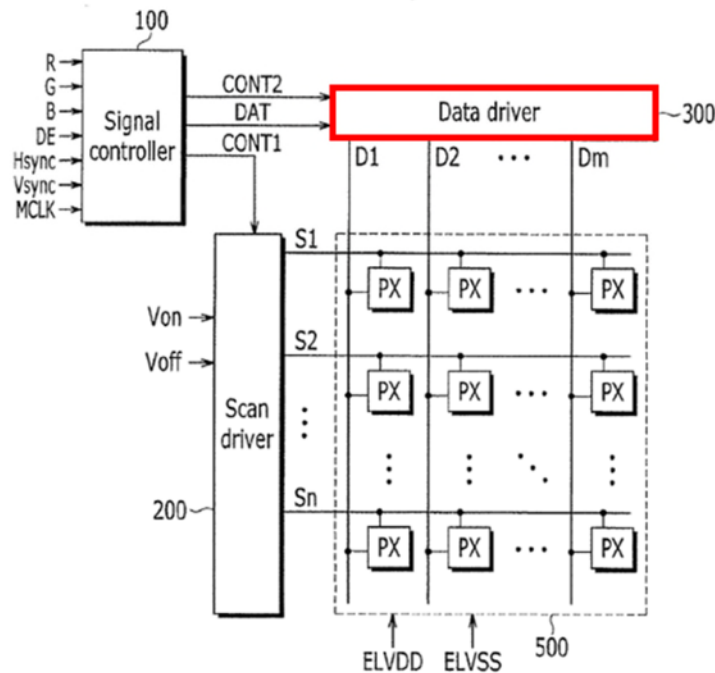
Ex.1004, Fig. 1; *see also id.* ¶¶0005, 0056; Ex.1003 ¶194.

c) Element [15-B]

Chung discloses “a data driver for supplying data signals to the pixels through the data lines.” Ex.1003 ¶196.

Chung shows data driver for supplying data signals to pixels PX through data lines D1-Dm:

FIG. 1



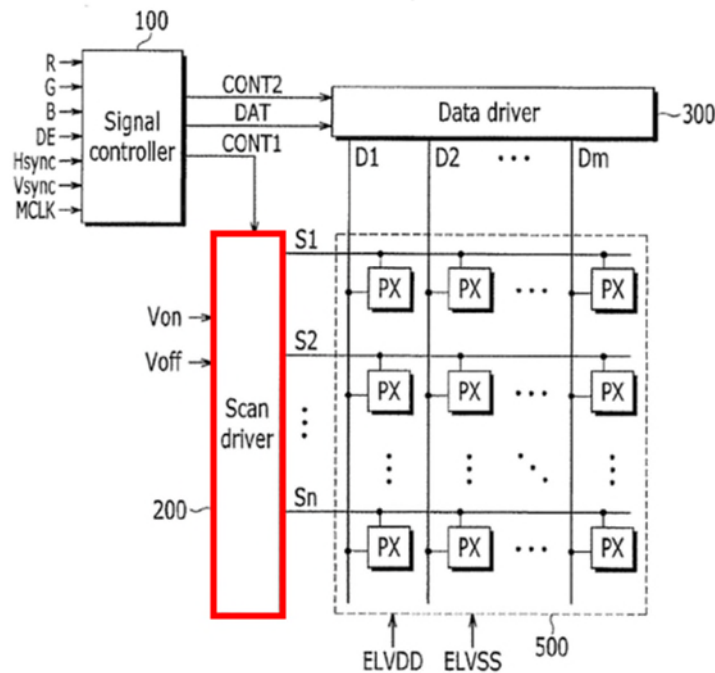
Ex.1004, Fig. 1; *see also id.* ¶¶0055, 0059; Ex.1003 ¶197.

d) Element [15-C]

Chung discloses “a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal.” Ex.1003 ¶209.

Chung depicts scan driver, which supplies scan signals to pixels PX through scan lines S1-Sn:

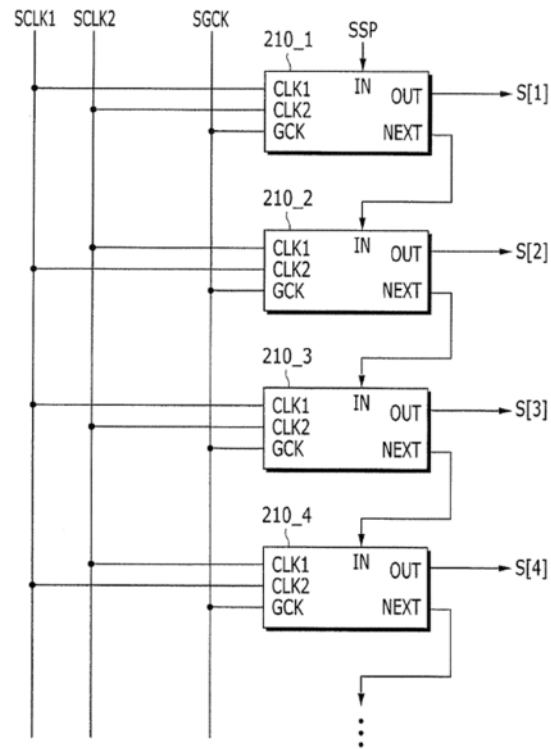
FIG. 1



Ex.1004, Fig. 1; *see also id.* ¶¶0055, 0057; Ex.1003 ¶¶200-202.

Chung also explains that its scan driver 200 includes a series of stage circuits (210_1 through 210_n), each of which generates a scan signal S[1] through S[n] that is coupled to one of scan lines S1-Sn, as depicted below:

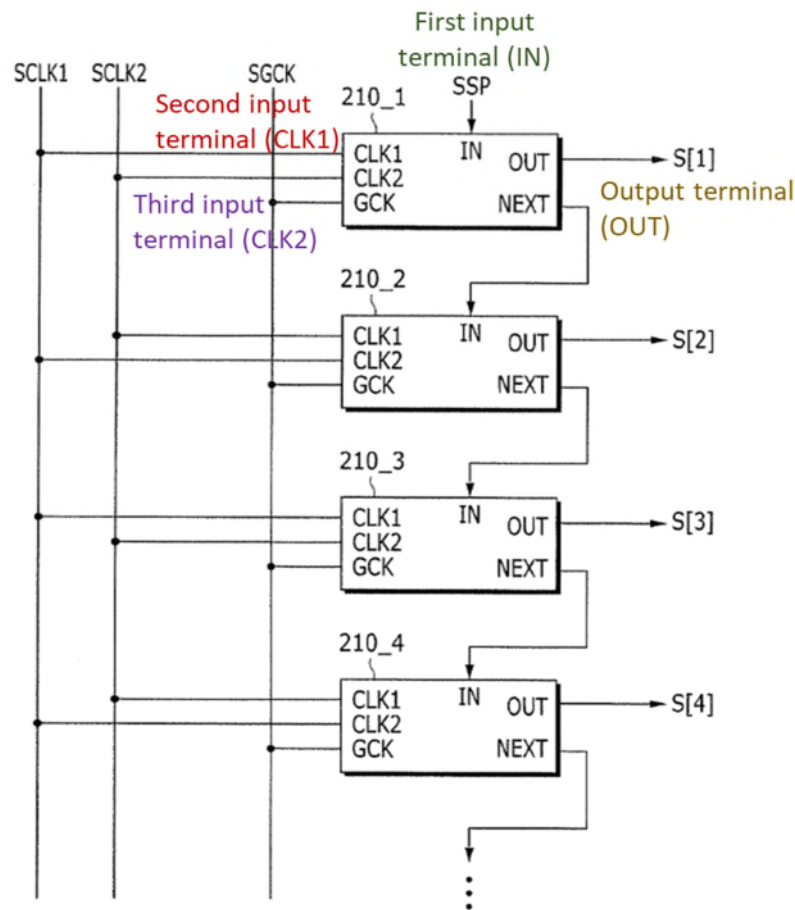
FIG. 3



Ex.1004, Fig. 3; *see also id.* ¶¶0068; Ex.1003 ¶¶203-205.

Finally, each of Chung's stage circuits has a first input terminal [IN], second input terminal [CLK1], third input terminal [CLK2], and output terminal [OUT], as discussed for, *inter alia*, Claim [1-PRE]. *See* Section VIII.A.1.a; Ex.1003 ¶¶206-208.

FIG. 3



Ex.1004, Fig. 3.

e) Elements [15-D] through [15-G]

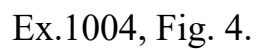
Elements [15-D] through [15-G] are the same as Elements [1-A] through [1-D]. Thus, Chung discloses these portions of Claim 15 for the same reasons discussed for Claim 1. *See supra* Section VIII.A.1; Ex.1003 ¶¶210-218.

11. Claim 16

Claim 16 depends from Claim 15 and additionally requires that “a clock

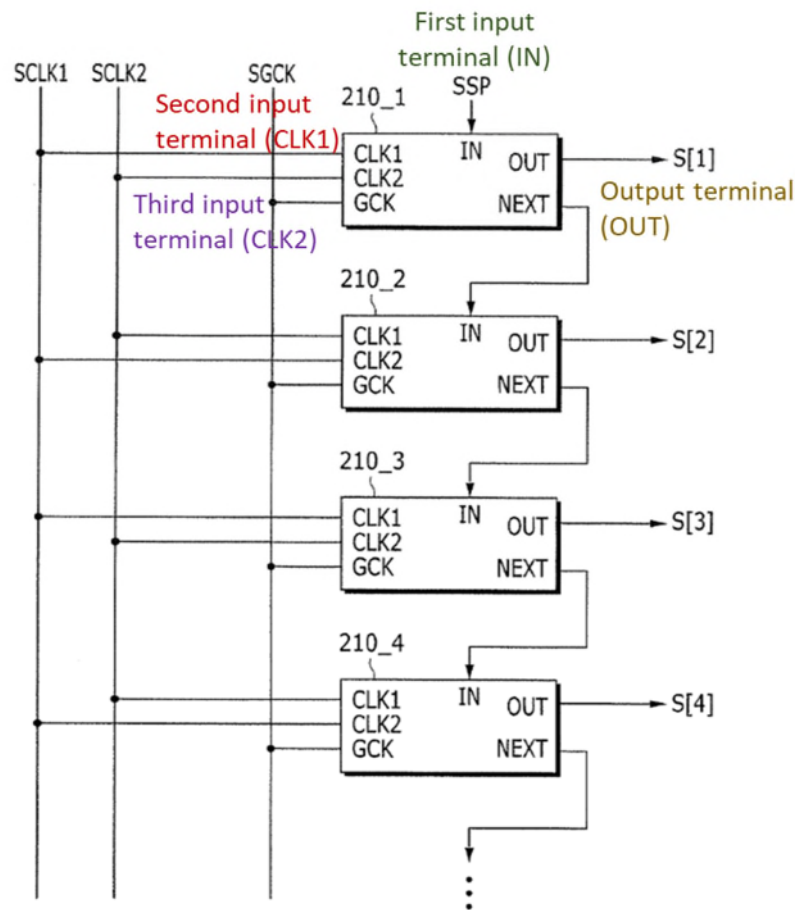
Chung discloses this additional limitation. Ex.1003 ¶221.

Ex.1003 ¶222.



Ex.1003 ¶223. The signal S[n] of the **output terminal (OUT)** is used as the scan signal:

FIG. 3



Ex.1004, Fig. 3; *see also id.* ¶0100; Ex.1003 ¶224.

12. Claim 17

The additional limitation of Claim 17 is the same as element [2-A] because a scan signal is an output signal as just explained for Claim 16. Thus, Chung discloses Claim 17 for the same reasons discussed for Claim 2. *See supra* Section VIII.A.2; Ex.1003 ¶¶226-229.

13. Claim 18

Claim 18 depends from Claim 17 and requires that the “second input terminals of odd stage circuits receive a first clock signal and third input terminals of odd stage circuits receive a second clock signal” and “second input terminals of even stage circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal.”

Chung discloses these additional limitations. Ex.1003 ¶234.

As shown in Chung Figure 3, in the odd stage circuits (*e.g.*, stage circuits 210_1 and 210_3), the second input terminals (**CLK1**) receive a first clock signal (**SCLK1**) and the third input terminals (**CLK2**) receive a second clock signal (**SCLK2**). And in the even stage circuits (*e.g.*, stage circuits 210_2 and 210_4), the second input terminals (**CLK1**) receive the second clock signal (**SCLK2**) and the third input terminals (**CLK2**) receive the first clock signal (**SCLK1**):

[illegible]

14. Claim 19

15. Claim 20

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Section VIII.A.6; Ex.1003 ¶¶239-242.

16. Claim 21

The additional limitation of Claim 21 is the same as that of Claim 7. Thus, Chung discloses Claim 21 for the same reasons discussed for Claim 7. *See supra* Section VIII.A.7; Ex.1003 ¶¶243-246.

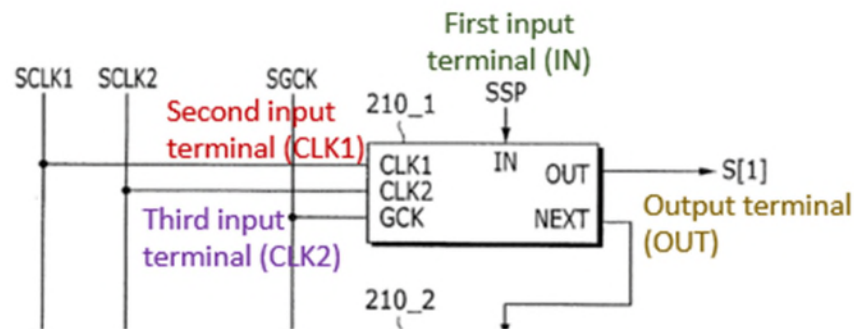
17. Claim 23

The additional limitation of Claim 23 is the same as that of Claim 9. Thus, Chung discloses Claim 23 for the same reasons discussed for Claim 9. *See supra* Section VIII.A.8; Ex.1003 ¶¶247-250.

18. Claim 25

Claim 25 depends from Claim 18 and requires that “the scan signal of the previous stage circuit or the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal.” The second alternative in this limitation is the same as the additional limitation of Claim 5 (“the start signal is supplied to overlap the first clock signal”) because Chung’s start signal SSP is supplied to the first input terminal IN, and Chung’s first clock signal SCLK1 is supplied to the second input terminal CLK1.

FIG. 3



Ex.1004, Fig. 3 (partial).

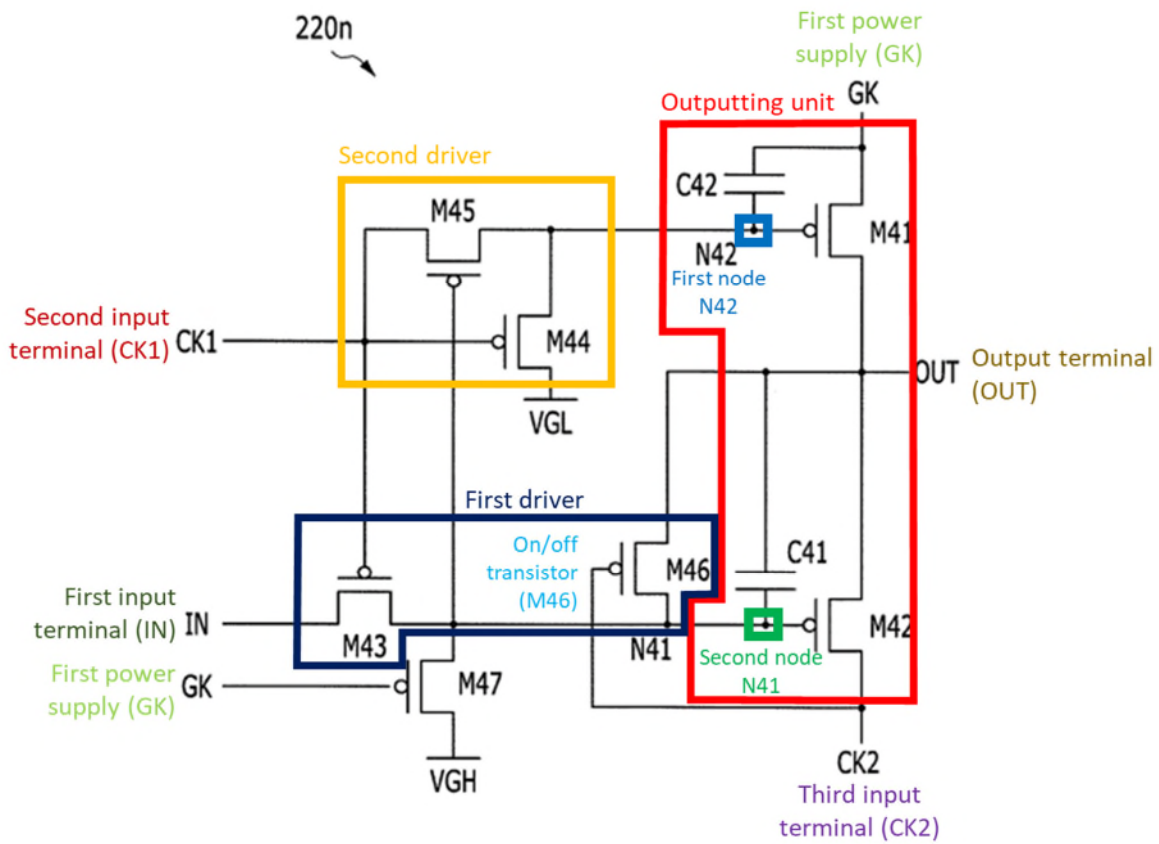
Thus, Chung discloses Claim 25 for at least the same reasons discussed for Claim 5. *See supra* Section VIII.A.5; Ex.1003 ¶¶251-256; *see also id.* ¶¶257-263 (explaining that Chung also discloses the first alternative).

B. GROUND 2: Kim Anticipates Claims 1-5, 7-8, 14-19, 21-22, and 25

1. Independent Claim 1

Kim anticipates Claim 1. Ex.1003 ¶266.

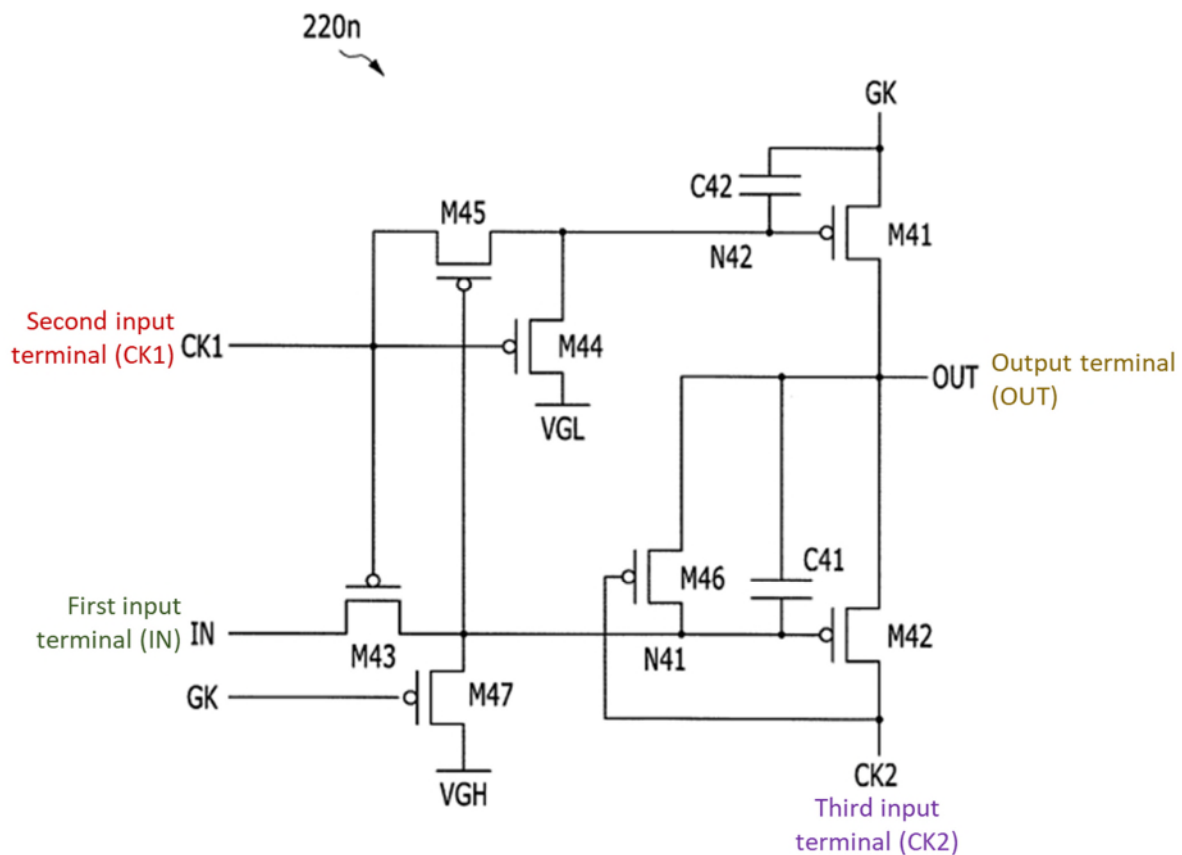
Kim depicts a stage circuit that is part of an OLED display, in which all of the signals and components recited in Claim 1 of the '593 patent are present and operate as required by the Claim, as discussed in more detail below.



Ex.1005, Fig. 9; see also Ex.1003 ¶265.

a) [1-PRE]

Kim discloses “[a] stage circuit having a first input terminal [IN], a second input terminal [CK1], a third input terminal [CK2], and an output terminal [OUT]”:

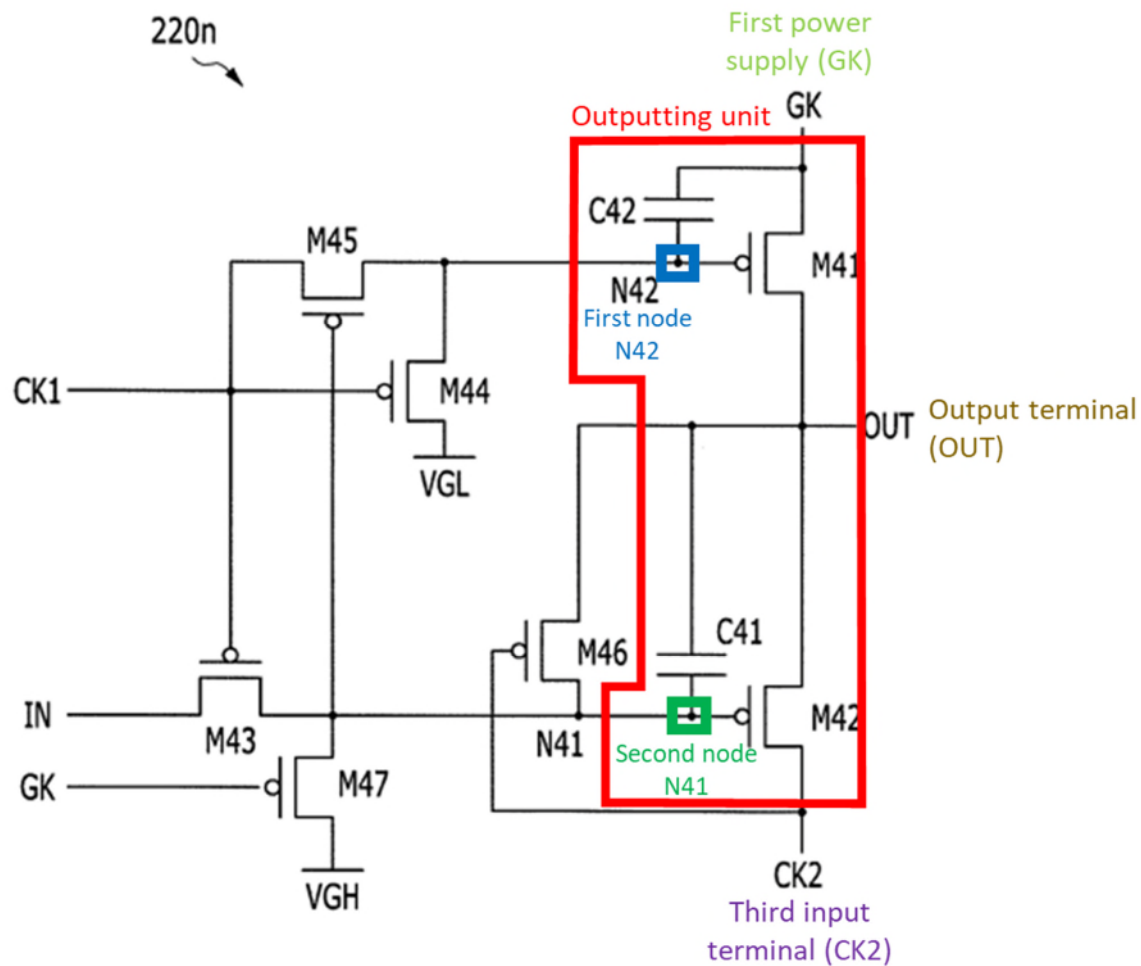


Ex.1005, Fig. 9; Ex.1003 ¶¶268-271.

b) Element [1-A]

Kim discloses “an **outputting unit** having a **first node [N42]** and a **second node [N41]**, the **outputting unit** to supply a voltage of a **first power supply [GK]** to the **output terminal [OUT]** according to a voltage applied to the **first node [N42]** and a signal [SCLK2] of the **third input terminal [CK2]** to the **output terminal [OUT]** according to a voltage applied to the **second node [N41]**.” Ex.1003 ¶283.

Kim’s **outputting unit** contains all of the required components:



Ex.1005, Fig. 9; *see also id.* ¶¶0162-0163, 0169; Ex.1003 ¶¶277-282.

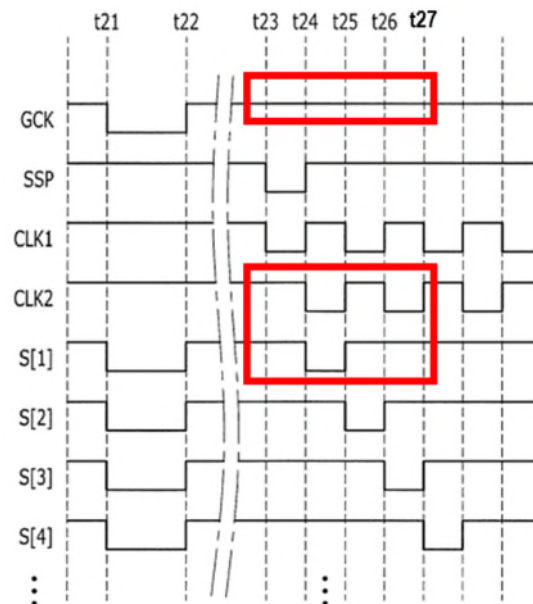
Kim further describes the outputting unit functioning in a manner matching the element [1-A] requirement. For example, during the t23-to-t24 period, both first node N42 and second node N41 are low voltage, turning on transistors M41 and M42 and enabling the output terminal OUT to take on the logic-high state of both the first power supply GK and the third input terminal CK2, respectively.

Ex.1005 ¶0178. During the t24-to-t25 period, first node N42 is high, turning off

transistor M41; second node N41 is low, turning on M42 and enabling the output terminal OUT to take on the logic-low state of the third input terminal CK2.

Ex.1005 ¶¶0179-0180. During the t25-to-t26 and t26-to-t27 periods, the second node N41 is high, turning off transistor M42; the first node N42 is low, turning on transistor M41 and enabling the output terminal OUT to take on the logic-high state of the first power supply GK. Ex.1005 ¶¶0182-0184.

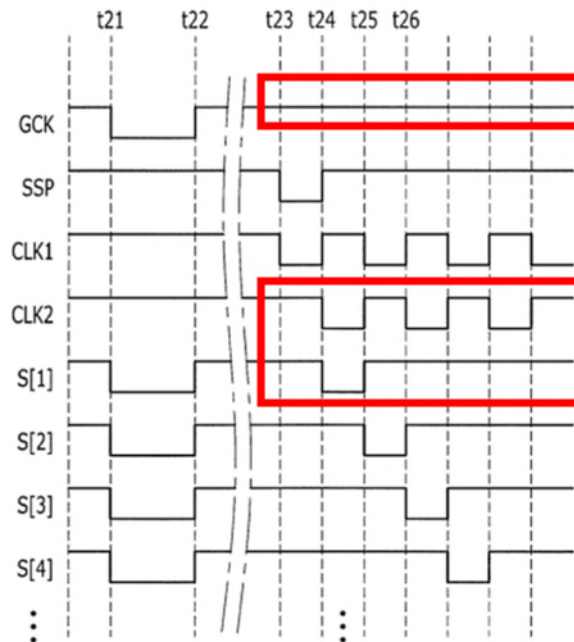
FIG. 10



Ex.1005, Fig. 10 (“t27” added).

In all of these scan periods, terminal GK supplies an operational high voltage level. *Id.* ¶0176.

FIG. 10



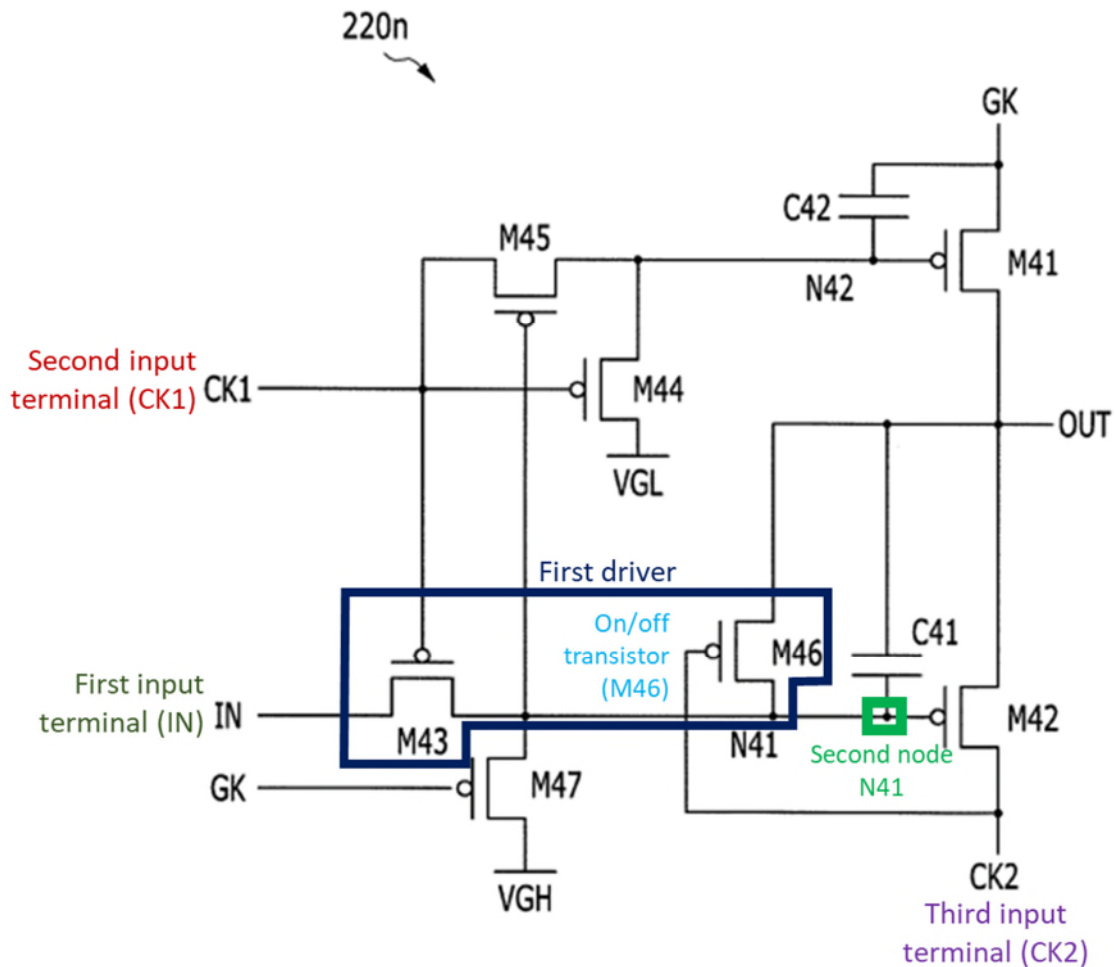
Id., Fig. 10.

Thus, for the same reason as explained for Chung, a POSITA would understand GK to functions as a power supply during scan operations. *See supra* Section VIII.A.1.b; Ex.1005 ¶¶0077, 0090, 0173-0175; Ex.1003 ¶¶273-276.

c) Element [1-B]

Kim discloses “a first driver to control the voltage of the second node [N41] in accordance with signals of the first input terminal [IN], the second input terminal [CK1], and the third input terminal [CK2].” Ex.1003 ¶284.

Kim’s first driver contains all of the required components:



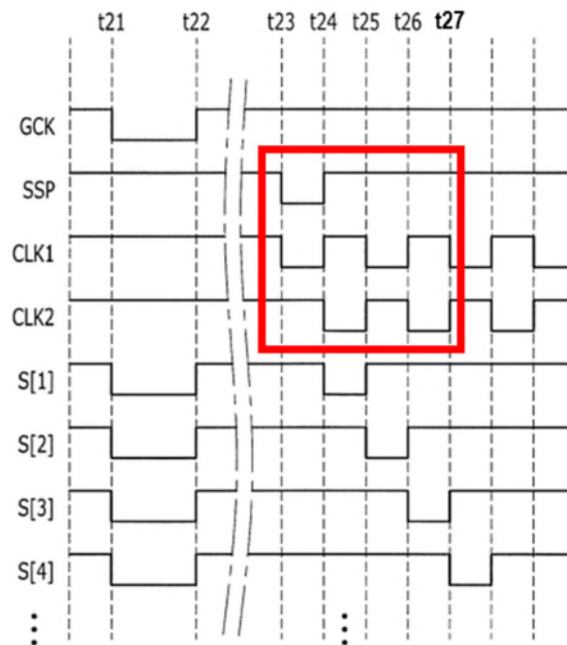
Ex.1005, Fig. 9; *see also id.* ¶¶0164, 0167-0168; Ex.1003 ¶284.

Kim further describes the first driver functioning in a manner matching the element [1-B] requirement. For example, during the t23-to-t24 period, transistor M43 is turned on by the signal CLK1 of the second input terminal CK1. Thus, the signal SSP of the first input terminal IN is transmitted to the second node N41.

Ex.1005 ¶0178. During the t25-to-t26 period, transistor M43 is again turned on by CLK1, thus, the signal SSP of the first input terminal IN is transmitted to the

second node N41. *Id.* ¶0183. During the t26-to-t27 period, transistor M43 is turned off by CLK1. *Id.* ¶0184. M46 is turned on by the signal CLK2 of the third input terminal CK2, coupling the voltage of the output terminal OUT to the second node N41, pulling N41 to a logic-high state. *Id.*

FIG. 10



Id., Fig. 10 (“t27” added); *see also* Ex.1003 ¶¶286-289.

d) Element [1-C]

Kim discloses “a **second driver** to control the voltage of the **first node [N42]** in accordance with the signal [CLK1] of the **second input terminal [CK1]** and the voltage of the **second node [N41]**.” Ex.1003 ¶296.

As shown in below, Kim’s **second driver** contains all of the required

Kim further describes the second driver functioning in a manner matching the element [1-C] requirement. For example, during the t23-to-t24 period, transistor M44 is turned on by the signal CLK1 of the second input terminal CK1, thus, the low-level signal of VGL is transmitted to the first node N42. Ex.1005 ¶0178. During the t24-to-t25 period, M44 is turned off by the signal CLK1 of the second input terminal CK1, M45 is turned on by the low-level voltage of the

second node N41, and CLK1 is transmitted to the first node N42. *Id.* ¶0179.

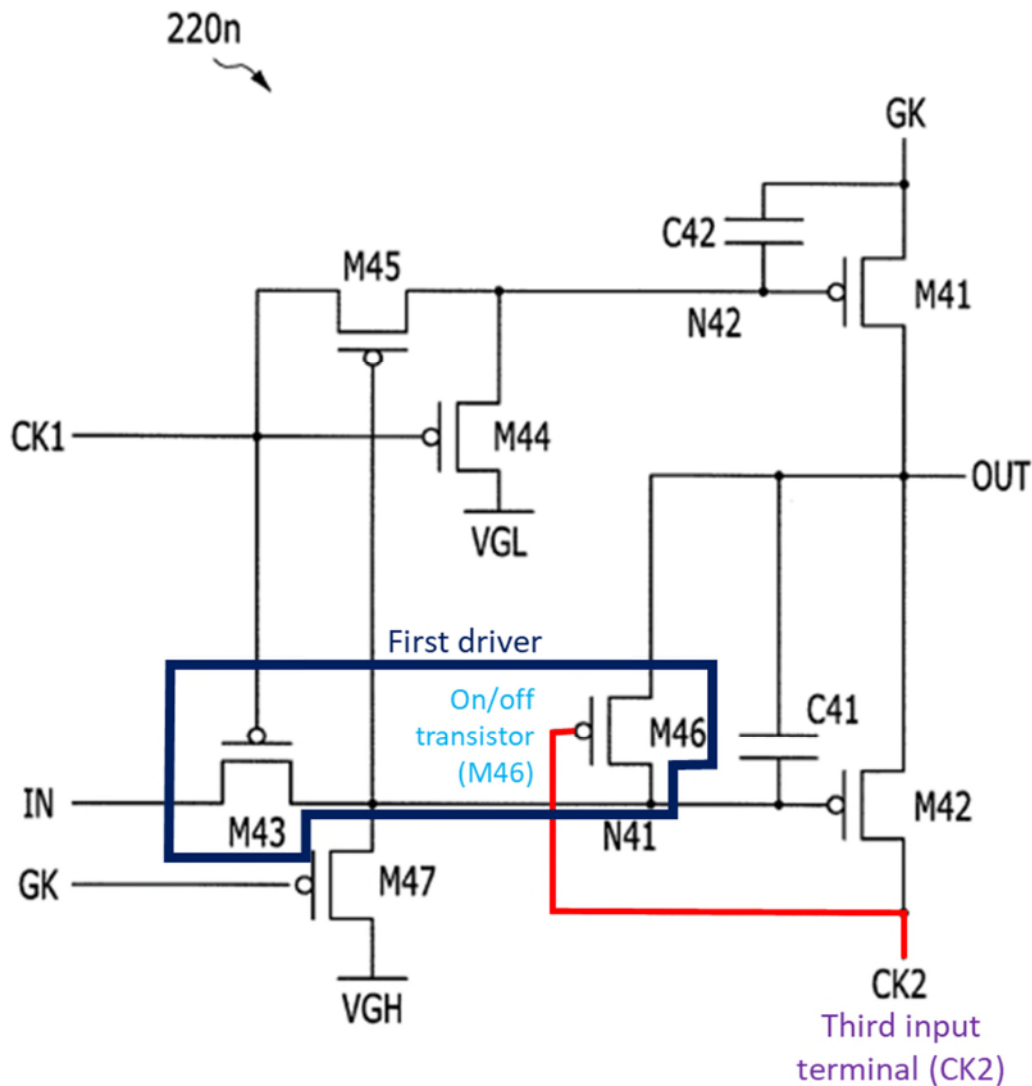
During the t25-to-t26 period, transistor M44 is again turned on by CLK1. Thus, the low-level signal of VGL is transmitted to the first node N42. *Id.* ¶0183.

Accordingly, the second driver (comprising transistors M44 and M45) controls the voltage of the first node (N42) in accordance with the signal (CLK1) of the second input terminal (CK1) and the voltage of the second node (N41). Ex.1003 ¶¶293-295.

e) Element [1-D]

Kim discloses that “the signal [CLK2] of the **third input terminal [CK2]** directly controls an on/off operation of a **transistor [M46]**, the **transistor [M46]** included in the **first driver.**” Ex.1003 ¶298.

The **third input terminal CK2** is directly coupled to the gate electrode of **transistor M46**, which is part of the **first driver**:



Ex.1005, Fig. 9; *see also id.* ¶¶0167; Ex.1003 ¶297.

Kim further describes the first driver functioning in a manner matching the element [1-D] requirement. Because the signal CLK2 of the third input terminal CK2 is coupled to the gate electrode of M46, CLK2 directly controls the on/off operation of M46. Ex.1003 ¶297. For example, during the t24-to-t25 and t26-to-t27 periods, transistor M46 is turned on by CLK2. Ex.1005 ¶¶0179, 0184.

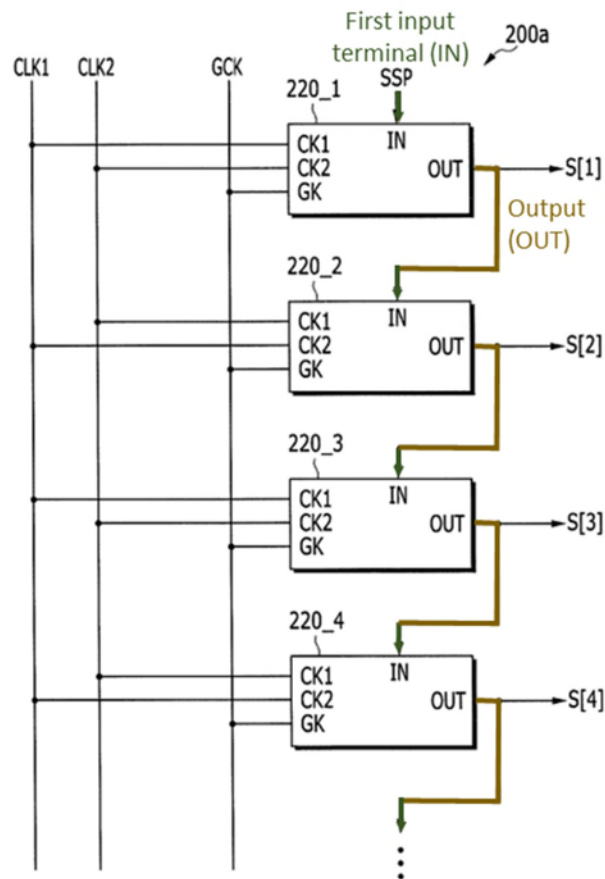
2. Claim 2

Claim 2 depends from Claim 1 and requires that “the first input terminal [IN] receives an output signal [OUT] of a previous stage circuit or a start signal [SSP],” “the second input terminal receives a first clock signal,” and “the third input terminal receives a second clock signal.”

Kim discloses these additional limitations. Ex.1003 ¶¶300-301.

Kim’s first input terminal IN receives start signal SSP in the first stage of the stage circuit, and receives an output signal from terminal OUT of the previous stage in subsequent stages:

FIG. 8



Ex.1005, Fig. 8; *see also id.* ¶¶0153-0159; Ex.1003 ¶302.

Additionally, as discussed for Claim 1, a stage circuit has a second input terminal CK1 that receives first clock signal CLK1, and a third input terminal CK2 that receives second clock signal CLK2. *See* Section VIII.B.1.c.

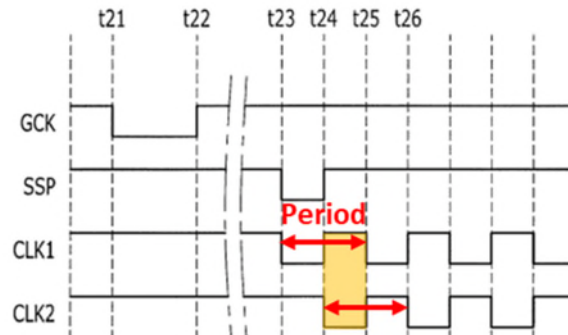
3. Claim 3

Claim 3 depends from Claim 2 and requires that “the first clock signal and the second clock signal have the same period and have phases that do not overlap.”

Kim discloses this additional limitation. Ex.1003 ¶¶304-305.

First clock signal CLK1 and second clock signal CLK2 have the same period and phases that do not overlap, *e.g.*, CLK1 is high when CLK2 is low:

FIG. 10



Ex.1005, Fig. 10 (partial); *see also id.* ¶0177; Ex.1003 ¶¶305-307.

4. Claim 4

Claim 4 depends from Claim 3 and requires that “the first clock signal and the second clock signal have a period equal to two horizontal periods 2H and are supplied in different horizontal periods as low signals.”

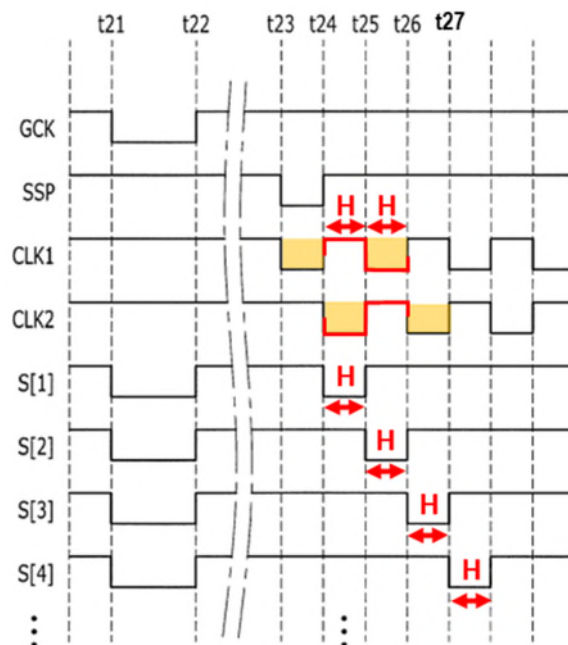
Kim discloses this additional limitation. Ex.1003 ¶316.

As explained for Chung, the '593 patent refers to “a period in which a scan signal is supplied to one scan line” as an exemplary horizontal period. Ex.1001 at 5:18-20; *see supra* Section VIII.A.4.

Referring to a horizontal period as the period between outputs of successive stages, *e.g.*, S[1] and S[2], both of Kim’s first and second clock signals CLK1 and CLK2 have a (clock) period equal to two horizontal periods 2H (*e.g.*, t24 through

t26). Further, first clock signal CLK1 is low during the t23-to-t24 and t25-to-t26 periods, and second clock signal CLK2 is low during the (different) t24-to-t25 and t26-to-t27 periods.

FIG. 10



Ex.1005, Fig. 10 (“t27” added); *see also* Ex.1003 ¶¶309-315.

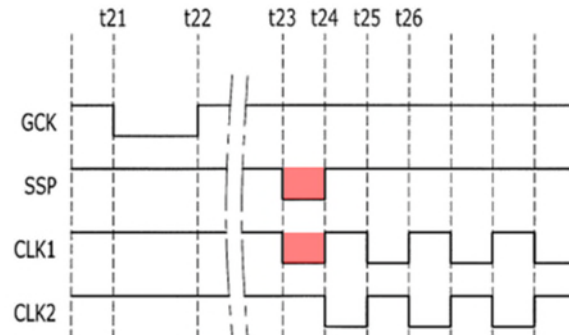
5. Claim 5

Claim 5 depends from Claim 2 and requires that “the start signal is supplied to overlap the first clock signal.”

Kim discloses this additional limitation. Ex.1003 ¶320.

The active logic-low state of start signal SSP overlaps with the active logic-low state of first clock signal CLK1 between times t23 and t24.

FIG. 10



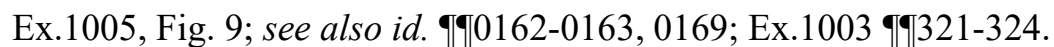
Ex.1005, Fig. 10 (partial); *see also id.* ¶¶0177-0178; Ex.1003 ¶¶317-319.

6. Claim 7

Claim 7 depends from Claim 2 and requires that “the **outputting unit** includes: a **fourth transistor [M41]** between the **first power supply [GK]** and the **output terminal [OUT]**, the **fourth transistor [M41]** having a gate electrode coupled to the **first node [N42]**,” “a **fifth transistor [M42]** between the **output terminal [OUT]** and the **third input terminal [CK2]**, the **fifth transistor [M42]** having a gate electrode coupled to the **second node [N41]**,” “a **first capacitor [C41]** between the **second node [N41]** and the **output terminal [OUT]**,” and “a **second capacitor [C42]** between the **first node [N42]** and the **first power supply [GK]**.”

Kim discloses these additional limitations. Ex.1003 ¶325.

Kim’s **outputting unit** contains all of the required components, arranged in the recited configuration:

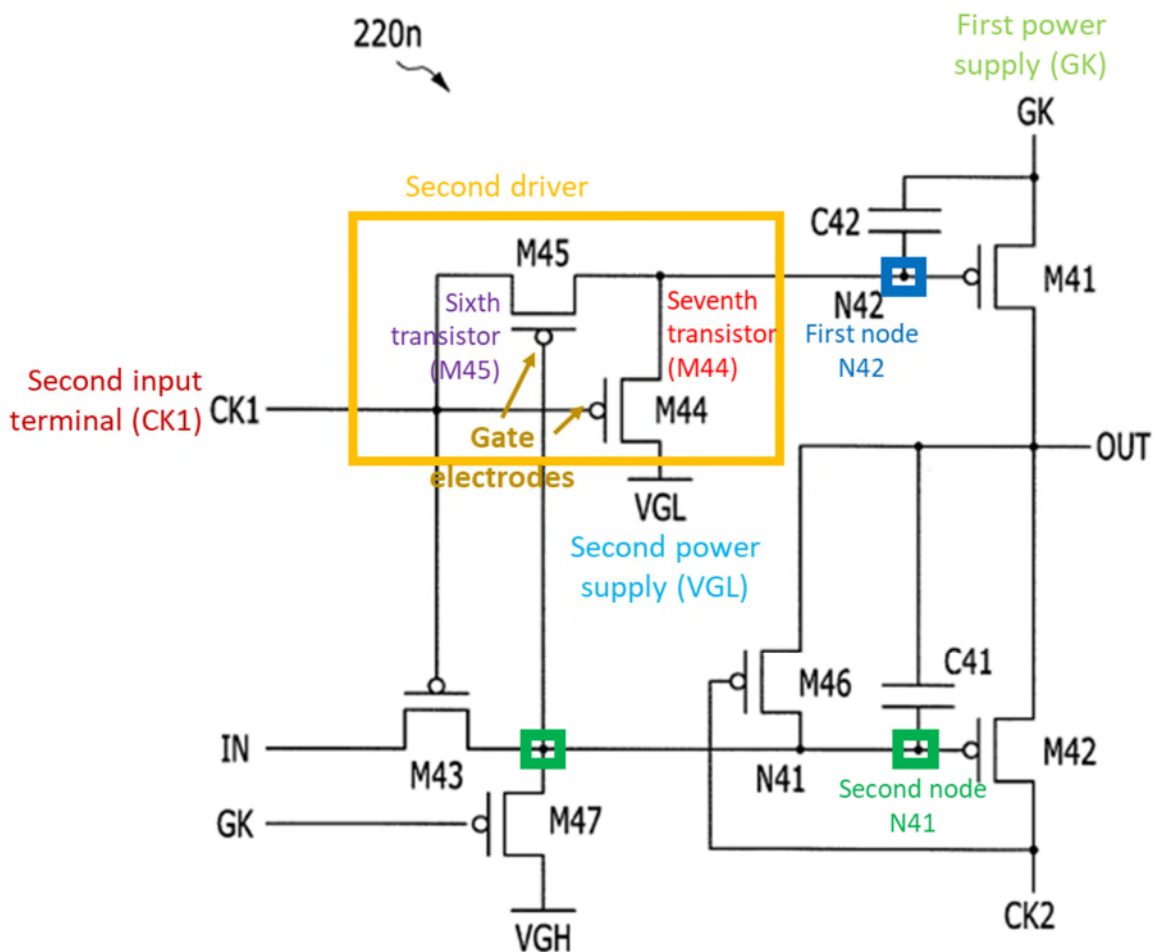


Claim 8 depends from Claim 2 and requires that “the **second driver** includes: a **sixth transistor [M45]** between the **first node [N42]** and the **second input terminal [CK1]**, the **sixth transistor [M45]** having a **gate electrode** coupled to the **second node [N41]**,” and “a **seventh transistor [M44]** between the **first node [N42]** and a **second power supply [VGL]**, the **second power supply [VGL]** having a lower

voltage than the first power supply [GK], the seventh transistor [M44] having a gate electrode coupled to the second input terminal [CK1].”

Kim discloses these additional limitations. Ex.1003 ¶329.

Kim’s second driver contains all of the required components, arranged in the recited configuration:



Ex.1005, Fig. 9; see also *id.* ¶¶0165-0166, Ex.1003 ¶¶326-328.

8. Claim 14

Claim 14 depends from Claim 1 and requires that “the transistor controls the

voltage of the second node according to the on/off operation thereof.”

Kim discloses this additional limitation. Ex.1003 ¶333.

The recited transistor reads on Kim’s transistor M46. Ex.1003 ¶331.

Specifically, because the second node N41 is coupled to the output terminal OUT through transistor M46, when M46 is turned on, the voltage of the output terminal OUT can be transferred to the second node N41. Ex.1003 ¶332. For example, during the t26-to-t27 period, transistor M46 is turned on, and the logic-high voltage level of OUT is transferred to the second node N41. Ex.1005 ¶0184.

9. Independent Claim 15

Kim anticipates Claim 15. Ex.1003 ¶334.

a) [15-PRE]

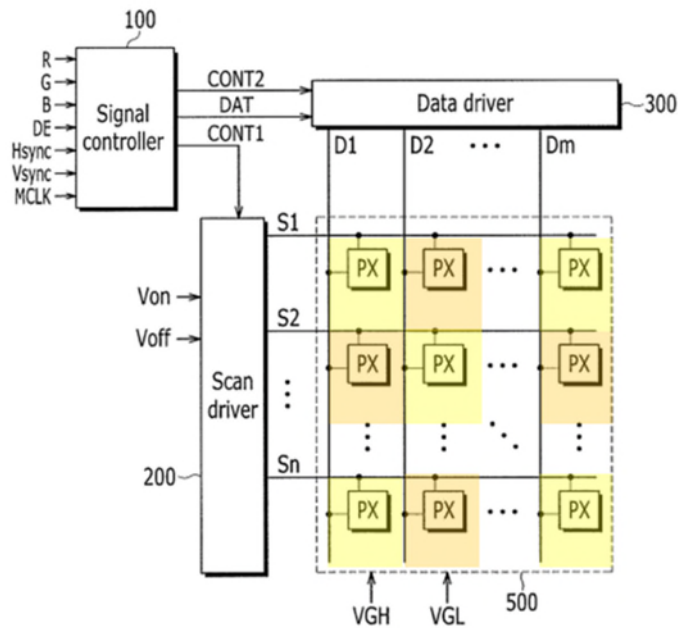
Kim discloses “[a]n organic light emitting display.” *See, e.g.*, Ex.1005, ¶¶0082-83 (“FIG. 2 illustrates an exemplary embodiment of a display device, e.g., an organic light emitting diode display using an organic light emitting diode.”), Fig. 2; Ex.1003 ¶¶336-337.

b) Element [15-A]

Kim discloses “pixels positioned in regions partitioned by scan lines and data lines.” Ex.1003 ¶338.

Kim depicts a plurality of pixels PX positioned in regions partitioned by scan lines S1-Sn and data lines D1-Dm, some of which are shaded for illustration:

FIG. 1



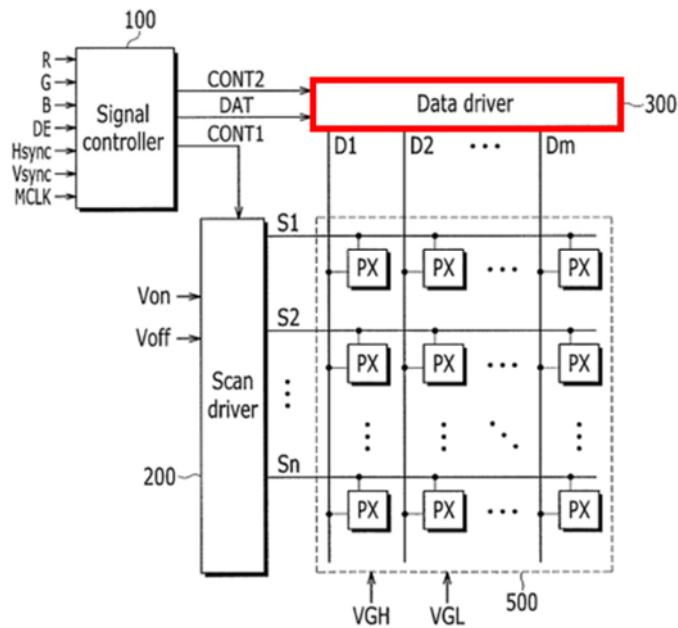
Ex.1005, Fig. 1; *see also id.* ¶¶0075-0076; Ex.1003 ¶339.

c) Element [15-B]

Kim discloses “a data driver for supplying data signals to the pixels through the data lines.” Ex.1003 ¶341.

Kim shows data driver for supplying data signals to pixels PX through data lines D1-Dm:

FIG. 1



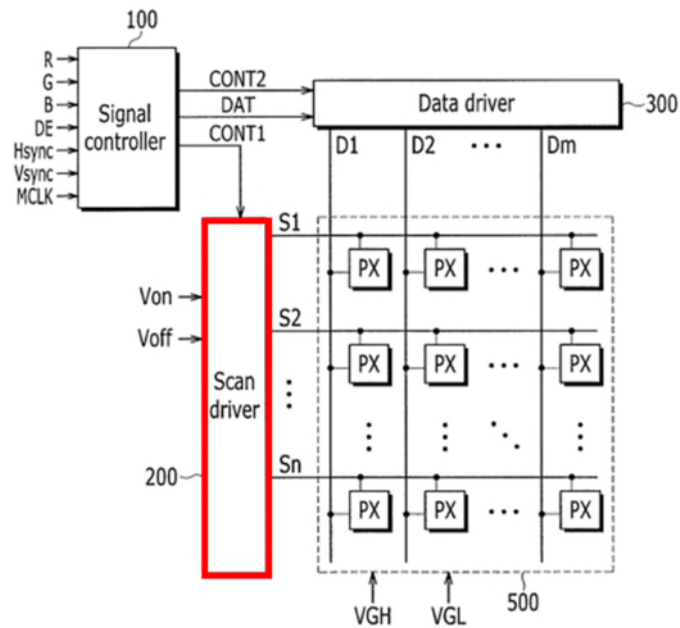
Ex.1005, Fig. 1; *see also id.* ¶¶0074-0075, 0078; Ex.1003 ¶342.

d) Element [15-C]

Kim discloses “a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal.” Ex.1003 ¶354.

Kim depicts scan driver, which supplies scan signals to pixels PX through scan lines S1-Sn:

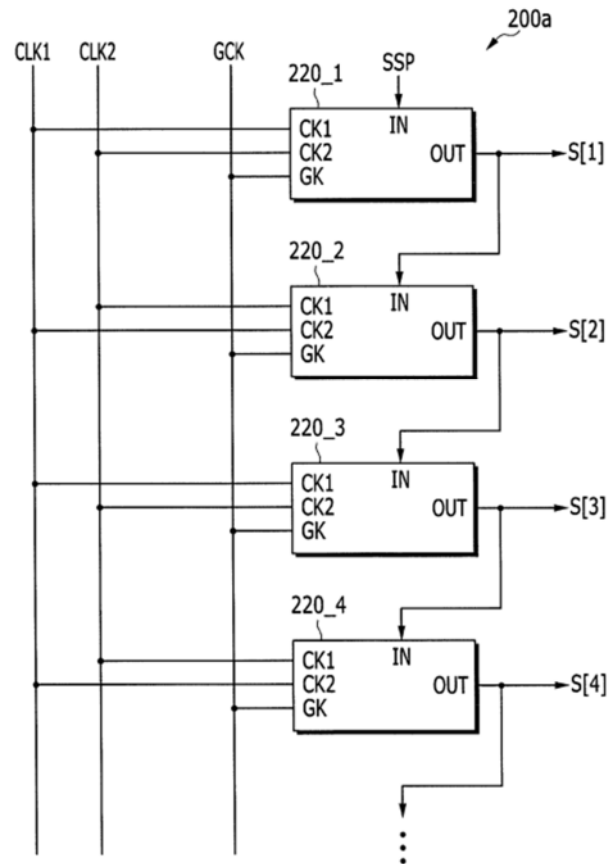
FIG. 1



Ex.1005, Fig. 1; *see also id.* ¶¶0074-0076, 0085; Ex.1003 ¶¶345-347.

Kim also explains that its scan driver 200 includes a series of scan driving blocks, *i.e.*, stage circuits (210_1 through 210_n), each of which generates a scan signal S[1], S[2], ..., S[n] that is coupled to one of scan lines S1-Sn, as depicted below:

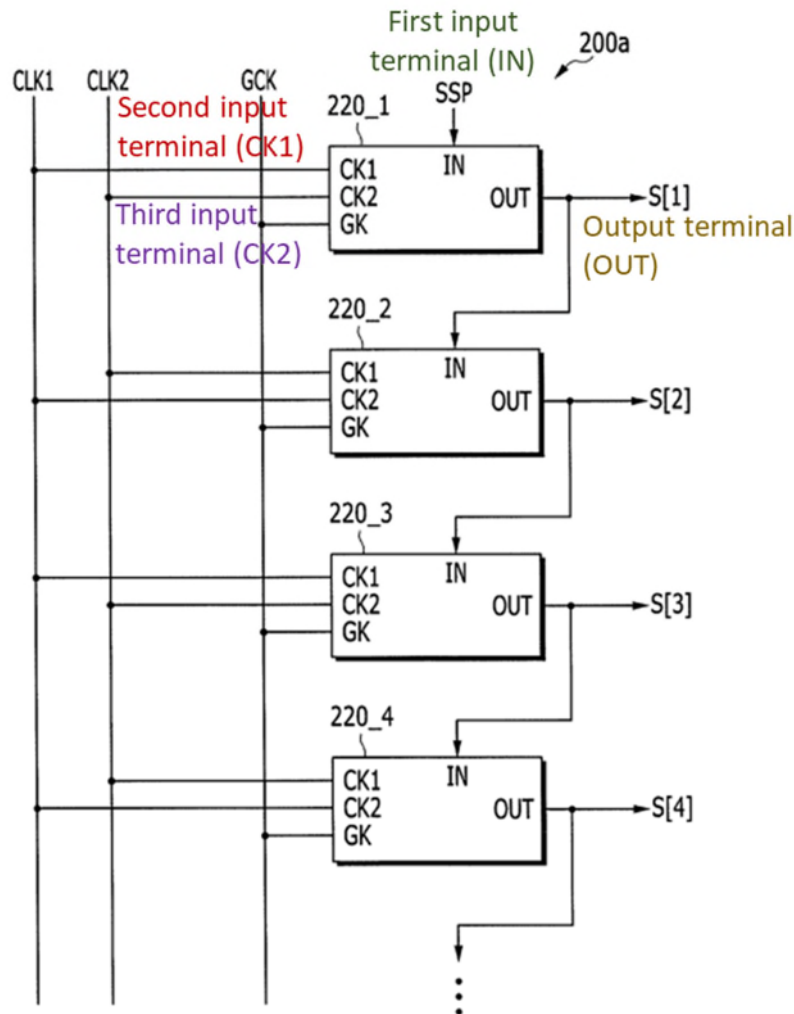
FIG. 8



Ex.1005, Fig. 8; *see also id.* ¶¶0153, 0160; Ex.1003 ¶¶348-350.

Finally, each of Kim's stage circuits has a first input terminal [IN], second input terminal [CK1], third input terminal [CK2], and output terminal [OUT], as discussed for, *inter alia*, Claim [1-PRE]. *See* Section VIII.B.1.a; Ex.1003 ¶¶351-353.

FIG. 8



Ex.1005, Fig. 8.

e) Elements [15-D] through [15-G]

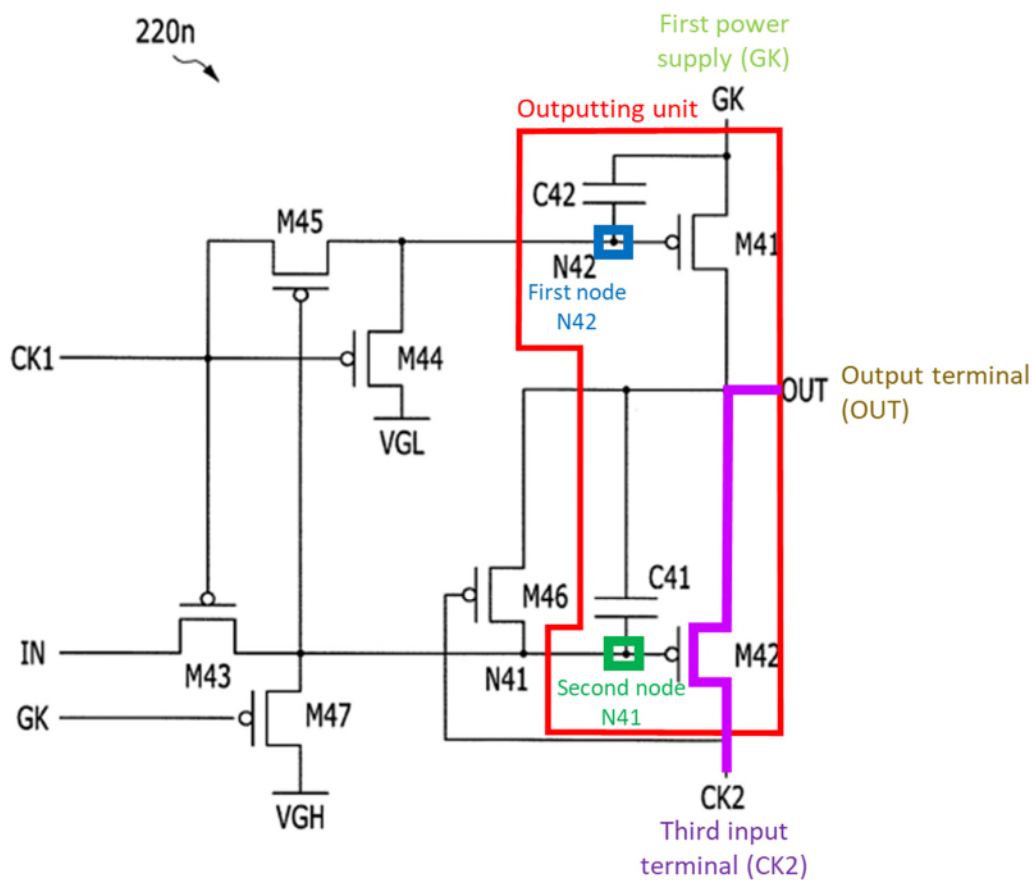
Elements [15-D] through [15-G] are the same as Elements [1-A] through [1-D] in Claim 1. Thus, Kim discloses these portions of Claim 15 for the same reasons discussed for Claim 1. *See supra* Section VIII.B.1; Ex.1003 ¶¶355-363.

10. Claim 16

Claim 16 depends from Claim 15 and additionally requires that “a clock signal supplied to the third input terminal is used as the scan signal.”

Kim discloses this additional limitation. Ex.1003 ¶366¶.

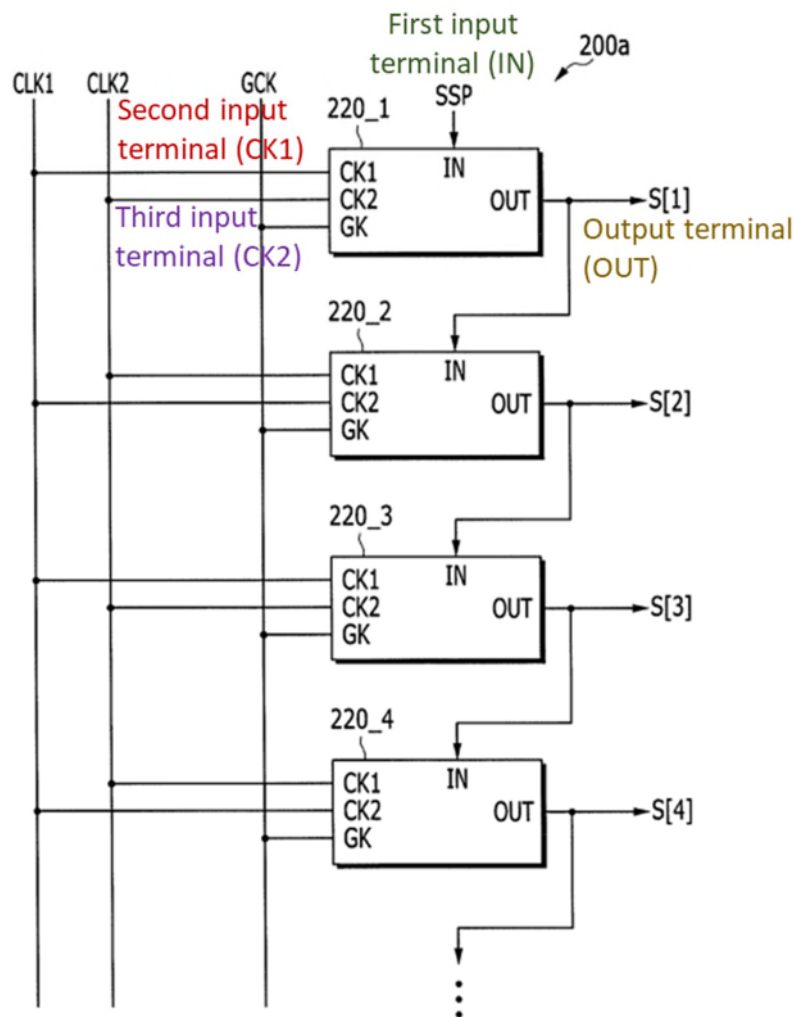
As discussed for element [1-A], Kim’s outputting unit supplies a signal of the **third input terminal (CLK2)** to the **output terminal (OUT)** according to a voltage applied to the second node (N41). *See supra* Section VIII.B.1.b; Ex.1003 ¶367.



Ex.1005, Fig. 9.

The signal CLK2 of **third input terminal CK2** is a clock signal. *Id.* ¶0155; Ex.1003 ¶368. The signal S[n] of the **output terminal (OUT)** is used as the scan signal:

FIG. 8



Ex.1005, Fig. 8; *see also id.* ¶¶0153, 0157-0159; Ex.1003 ¶369-370.

11. Claim 17

The additional limitation of Claim 17 is the same as Claim Element [2-A]

because a scan signal is an output signal as just explained for Claim 16. Thus, Kim discloses Claim 17 for the same reasons discussed for Claim 2. *See supra* Section VIII.B.2; Ex.1003 ¶¶372-375.

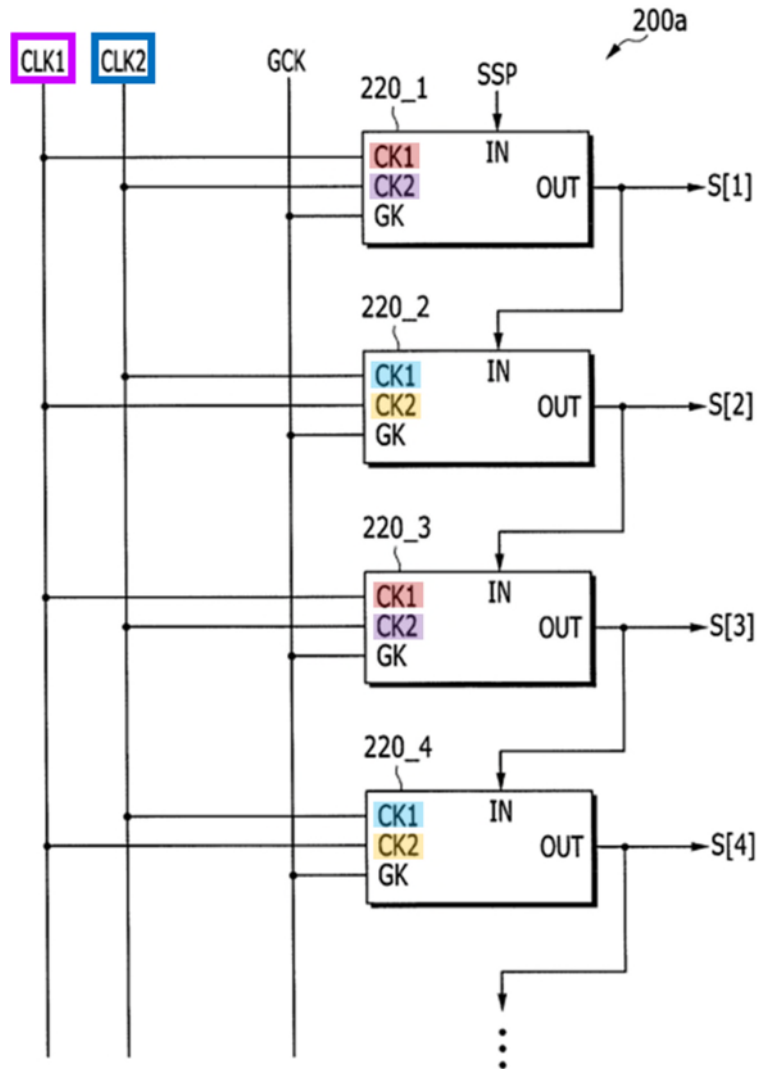
12. Claim 18

Claim 18 depends from Claim 17 and requires that the “second input terminals of odd stage circuits receive a first clock signal and third input terminals of odd stage circuits receive a second clock signal” and “second input terminals of even stage circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal.”

Kim discloses these additional limitations. Ex.1003 ¶380.

As shown in Kim Figure 8, in the odd stage circuits (*e.g.*, stage circuits 210_1 and 210_3), the second input terminals (CK1) receive a first clock signal (CLK1) and the third input terminals (CK2) receive a second clock signal (CLK2). And in the even stage circuits (*e.g.*, stage circuits 210_2 and 210_4), the second input terminals (CK1) receive the second clock signal (CLK2) and the third input terminals (CK2) receive the first clock signal (CLK1):

FIG. 8



Ex.1005, Fig. 8; *see also id.* ¶¶0155; Ex.1003 ¶¶376-379.

13. Claim 19

The additional limitation of Claim 19 is the same as that of Claim 3. Thus, Kim discloses Claim 19 for the same reasons discussed for Claim 3. *See supra* Section VIII.B.3; Ex.1003 ¶¶381-384.

14. Claim 21

The additional limitation of Claim 21 is the same as that of Claim 7. Thus, Kim discloses Claim 21 for the same reasons discussed for Claim 7. *See supra* Section VIII.B.6; Ex.1003 ¶¶385-388.

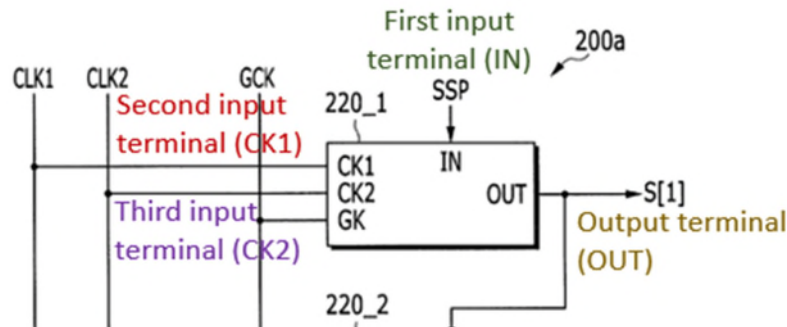
15. Claim 22

The additional limitation of Claim 22 is the same as that of Claim 8. Thus, Kim discloses Claim 22 for the same reasons discussed for Claim 8. *See supra* Section VIII.A.7; Ex.1003 ¶¶389-392.

16. Claim 25

Claim 25 depends from Claim 18 and requires that “the scan signal of the previous stage circuit or the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal.” The second alternative in this limitation is the same as the additional limitation of Claim 5 (“the start signal is supplied to overlap the first clock signal”) because Kim’s start signal SSP is supplied to the first input terminal IN, and Kim’s first clock signal CLK1 is supplied to the second input terminal CK1.

FIG. 8



Ex.1005, Fig. 8 (partial).

Thus, Kim discloses Claim 25 for at least the same reasons discussed for Claim 5. *See supra* Section VIII.B.5; Ex.1003 ¶¶393-398; *see also id.* ¶¶399-405 (explaining that Kim also discloses the first alternative).

C. GROUND 3: Tobita Renders Obvious Claims 1-5, 14-19, and 25

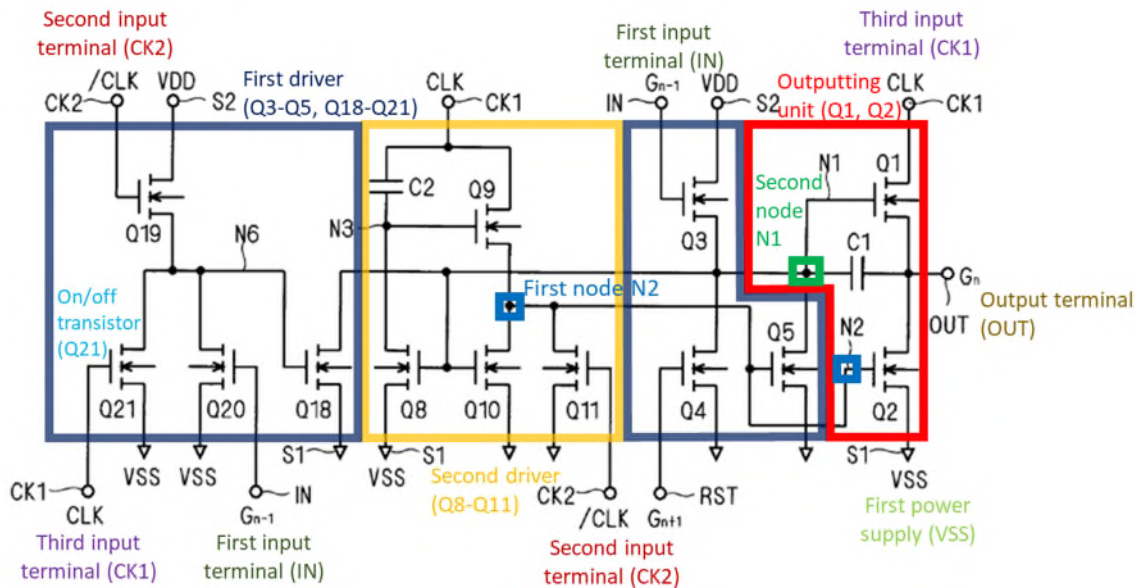
Tobita's embodiments use nMOS circuits. But, as explained in Transistor Basics, the equivalence of pMOS and nMOS circuits was well-understood. *See supra* Section V.B; Ex.1003 ¶407. Further, both the '593 patent and Tobita teaches that its embodiment may be formed using either pMOS or nMOS transistors. Ex.1001, 5:31-34; Ex.1006 ¶0108.

1. Independent Claim 1

Tobita renders obvious Claim 1. Ex.1003 ¶409.

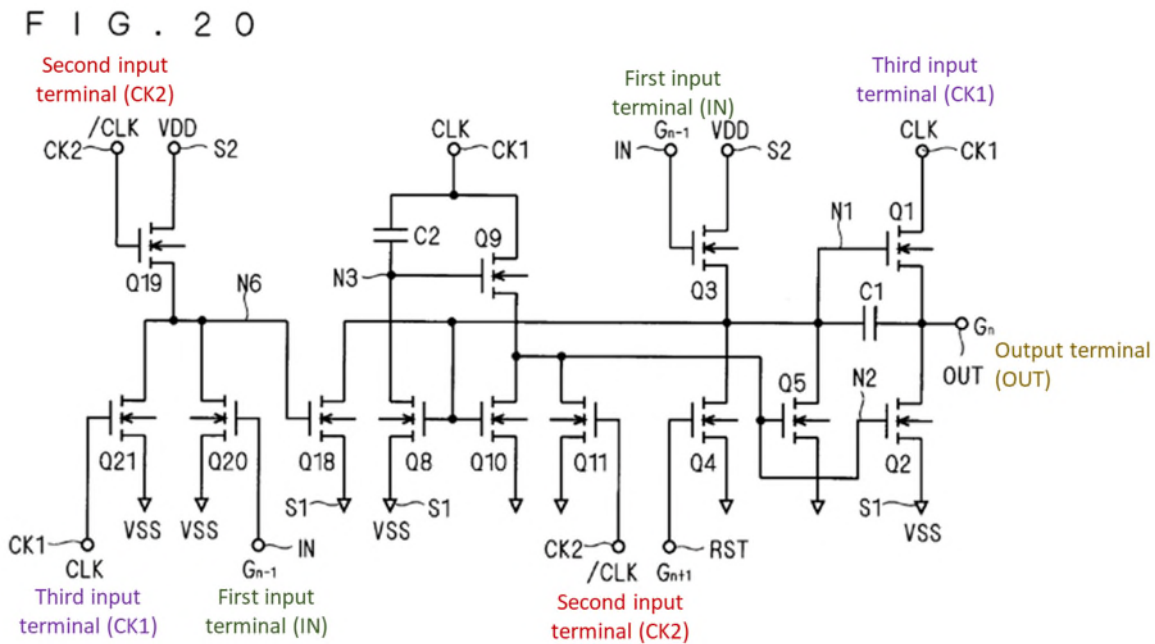
Tobita depicts a stage circuit that is part of a display, in which all of the signals and components recited in Claim 1 of the '593 patent are present and

F I G . 2 0



a) [1-PRE]

Tobita discloses “[a] stage circuit having a first input terminal [IN], a second input terminal [CK2], a third input terminal [CK1], and an output terminal [OUT].” See, e.g., Ex.1006 ¶¶0109, 0111, 0115 (describing circuit connections including an “output terminal OUT,” a “first clock terminal CK1,” an “input terminal IN,” and a “second clock terminal CK2”); *id.* ¶¶173, 178 (describing transistors Q18-Q21 and input terminals IN, CK1, and CK2):



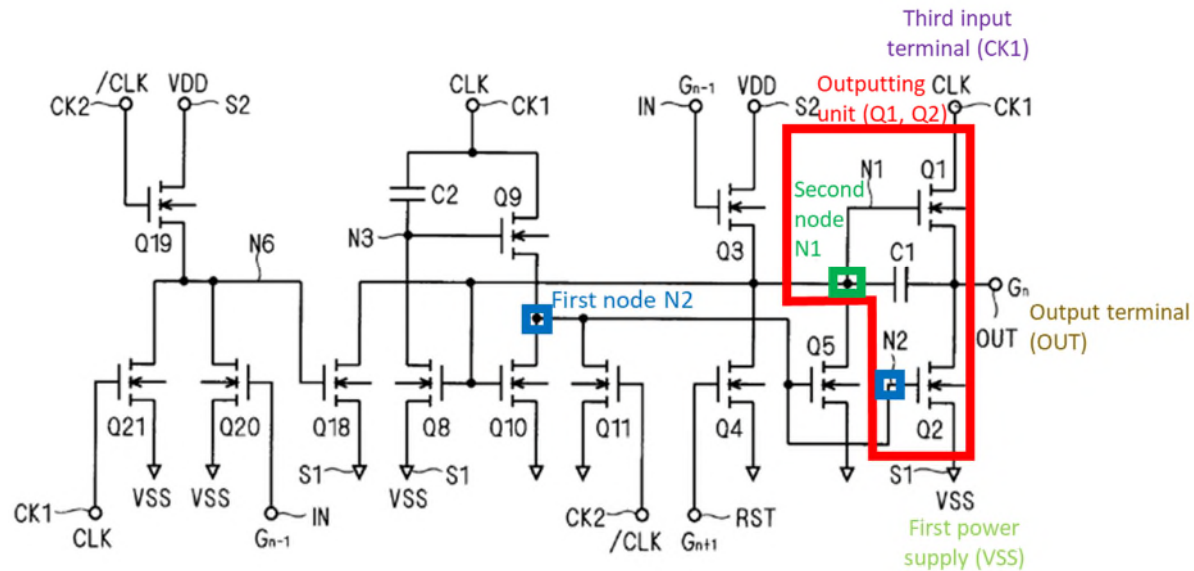
Ex.1006, Fig. 20; see also Ex.1003 ¶¶411-412.

b) Element [1-A]

Tobita discloses “an **outputting unit** having a **first node [N2]** and a **second node [N1]**, the **outputting unit** to supply a voltage of a **first power supply [VSS]** to the **output terminal [OUT]** according to a voltage applied to the **first node [N2]** and a signal of the **third input terminal [CK1]** to the **output terminal [OUT]** according to a voltage applied to the **second node [N1]**.” Ex.1003 ¶420.

Tobita’s **outputting unit** contains all the required components:

F I G . 2 0

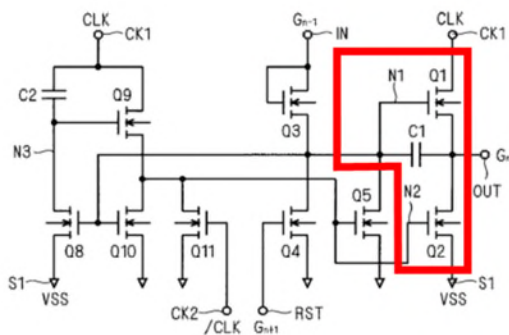


Ex.1006, Fig. 20; *see also id.* ¶0109; Ex.1003 ¶414.

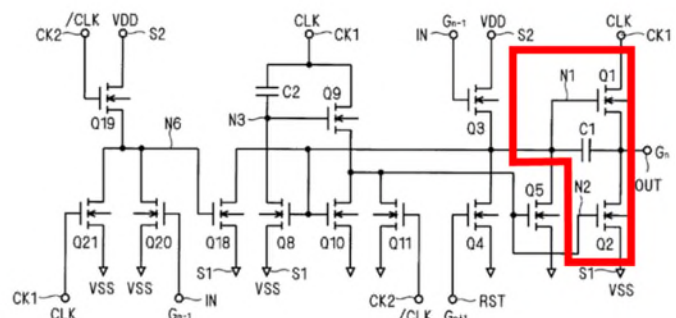
Tobita further describes the outputting unit functioning in a manner matching the element [1-A] requirement.

As discussed in Section VII.C, the embodiments of Figures 7 and 20 share common components and functionalities. Particularly, the two have identical outputting units:

F I G . 7

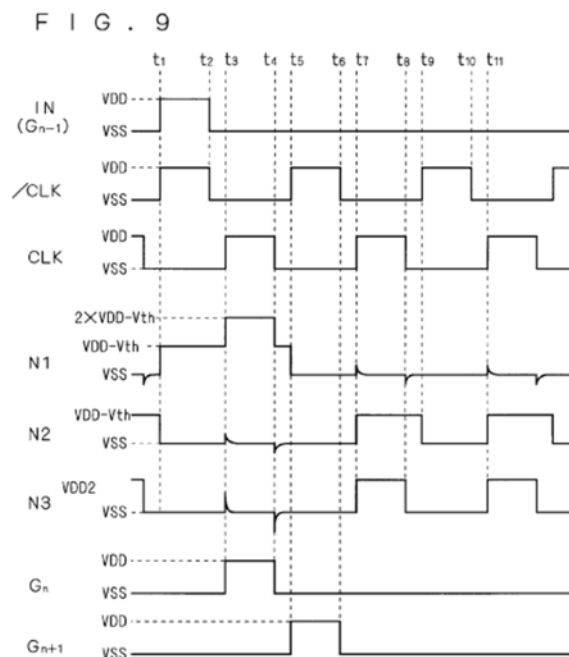


F I G . 2 0



Ex.1006, Figs. 7, 20. Thus, Tobita's disclosure regarding the embodiment of Figure 7, including the timing diagram of Figure 9, applies. *Id.* ¶¶0026-0028, 0117, 0195; Ex.1003 ¶109.

Tobita discloses that "Q1 is intended to supply the clock signal input to the first clock terminal CK1 to the output terminal OUT," and "Q2 is intended to supply the low supply voltage VSS to the output terminal OUT." Ex.1006 ¶0109. Since the gate electrodes of Q1 and Q2 are respectively connected to the second node N1 and the first node N2, the voltages of these two nodes control the coupling of CK1 and VSS to OUT, meeting the claim requirement. Ex.1003 ¶¶416-419. Tobita's description of circuit behavior confirms this.



Ex.1006, Fig. 9, ¶¶0120-0137.

For example, during the t_1 -to- t_2 and t_2 -to- t_3 periods, the first node N2 has low voltage, turning off transistor Q2. *Id.* ¶¶0120-0121. The second node N1 has high voltage, turning on transistor Q1. *Id.* Thus, signal CLK of the third input terminal CK1 is transferred to the output terminal OUT, and signal G_n is low. CLK goes high at t_3 , and thus during the t_3 -to- t_4 period, G_n becomes high. *Id.* ¶0122. CLK drops low at t_4 , and thus during the t_4 -to- t_5 period, G_n becomes low. *Id.* ¶0126. During the t_5 -to- t_6 period, both nodes N1 and N2 have low voltage, turning off Q1 and Q2. *Id.* ¶0129. G_n remains low. During the t_6 -to- t_7 period, both nodes remain low, Q1 and Q2 remain off, and G_n remains low. *Id.* ¶0130. During the t_7 -to- t_8 period, the first node N2 becomes high while the second node N1 stays low. *Id.* ¶¶0131-0133. Q1 is off and the low voltage of VSS is coupled to OUT through Q2. *Id.* ¶0132-0133. Finally, during the t_8 -to- t_9 period, the second node N1 is low, turning off Q1. *Id.* ¶0135. The first node N2 is high, coupling VSS to OUT through Q2. *Id.* ¶0134. The waveforms during t_6 -to- t_9 periods repeats until G_{n-1} of the first input terminal IN becomes high in the next frame period, and the waveforms starts again from t_1 . *Id.* ¶0137.

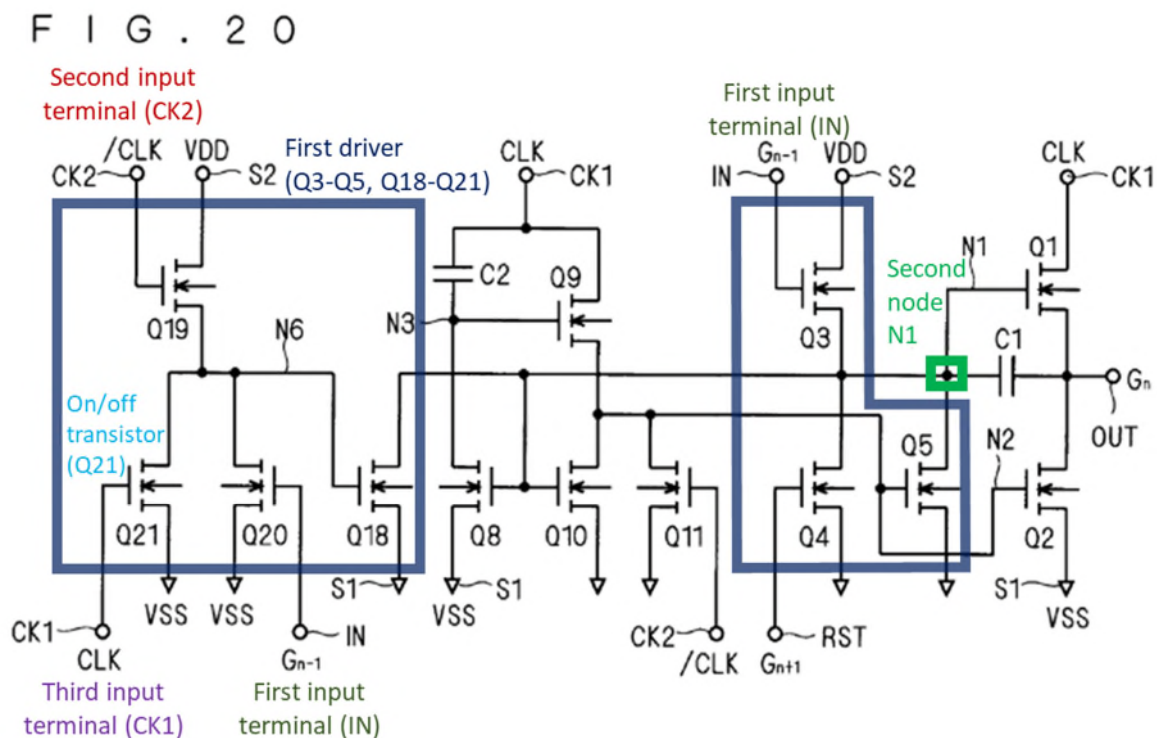
The outputting unit thus supplies a voltage of a first power supply (VSS) to the output terminal OUT according to a voltage applied to the first node N2 and a signal CLK of the third input terminal CK1 to the output terminal OUT according to a voltage applied to the second node N1, as required by element [1-A]. Ex.1003

¶¶416-419.

c) Element [1-B]

Tobita discloses “a first driver to control the voltage of the second node [N1] in accordance with signals of the first input terminal [IN], the second input terminal [CK2], and the third input terminal [CK1].” Ex.1003 ¶421.

Tobita’s first driver, which comprises the components controlling the voltage of the second node N1, contains all the required components:



Ex.1006, Fig. 20; *see also id.* ¶¶0111, 0173; Ex.1003 ¶421. Consistent with Patent Owner’s proposed constructions and infringement theories from the ITC matter, while Tobita’s embodiment of first driver uses more transistors than the preferred

embodiment first driver disclosed in the '593 patent, nothing in the element limits the number of transistors in the first driver. Ex.1003 ¶423.

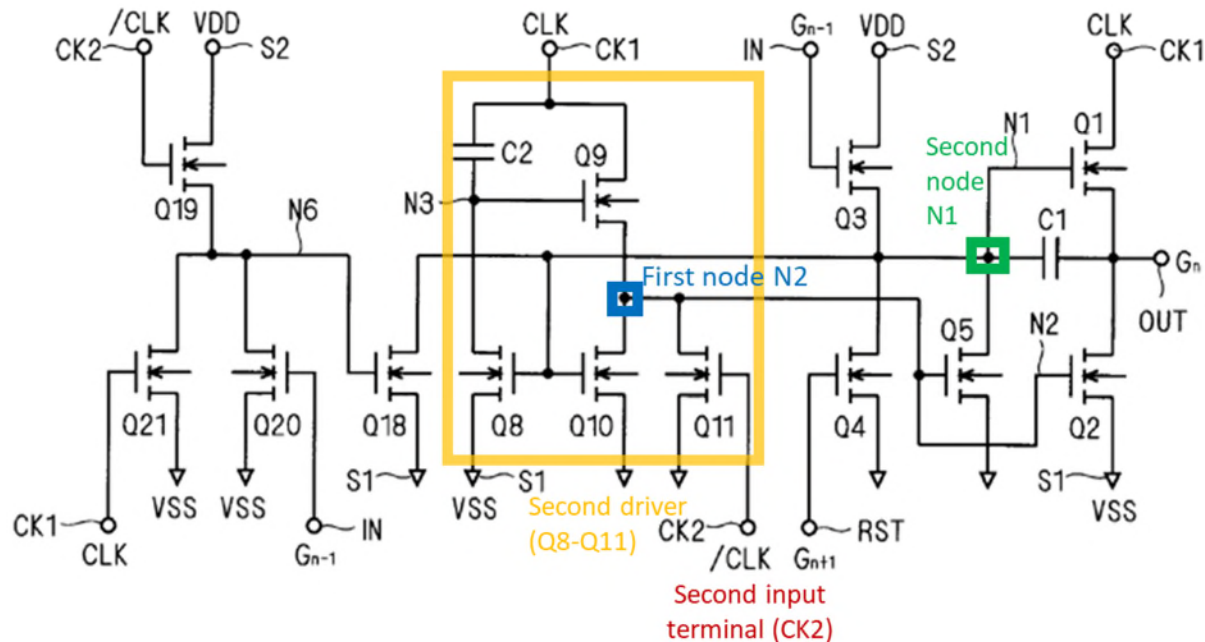
Tobita further describes the first driver functioning in a manner matching the element [1-B] requirement. Signal G_{n-1} of the first input terminal IN controls the on/off operation of transistor Q3, which in turn controls the voltage of the second node N1. *See, e.g.*, Ex.1006 ¶¶0120-0121, 0125. Transistors Q18 to Q21 controls the voltage of the second node N1, *e.g.*, bringing it to a low level. *Id.* ¶0172. Specifically, the first input terminal [IN], the second input terminal [CK2], and the third input terminal [CK1] respectively controls transistors Q20, Q19, and Q21, which transistors in turn control the voltage of node N6. *Id.* ¶¶0174-0177. Node N6 in turn controls transistor Q18, which controls the voltage of the second node [N1] in conjunction with transistors Q3 to Q5, also of the first driver. *Id.* ¶¶0175-0176. Accordingly, the first driver, comprising transistors Q3-Q5 and Q18-Q21, controls the voltage of the second node N1 in accordance with signals of the first input terminal [IN], the second input terminal [CK2], and the third input terminal [CK1], as required by the element. Ex.1003 ¶¶423-426. The other transistors connected to the second node N1, namely Q1, Q8, and Q10, are connected to N1 at their gate electrodes. Thus, N1 controls the operation of these other transistors, not vice versa. *Id.* ¶427.

d) Element [1-C]

Tobita discloses “a **second driver** to control the voltage of the **first node [N2]** in accordance with the signal of the **second input terminal [CK2]** and the voltage of the **second node [N1]**.” Ex.1003 ¶435.

Tobita’s **second driver** contains all the required components:

F I G . 2 0



Ex.1006, Fig. 20; *see also id.* ¶¶0113-0114; Ex.1003 ¶429. While the embodiment of second driver in Tobita uses more transistors than the preferred embodiment second driver disclosed in the '593 patent, consistent with Patent Owner's proposed constructions and infringement theories from the ITC matter, nothing in the element limits the number of transistors in the second driver. Ex.1003 ¶431.

Tobita further describes the second driver functioning in a manner matching

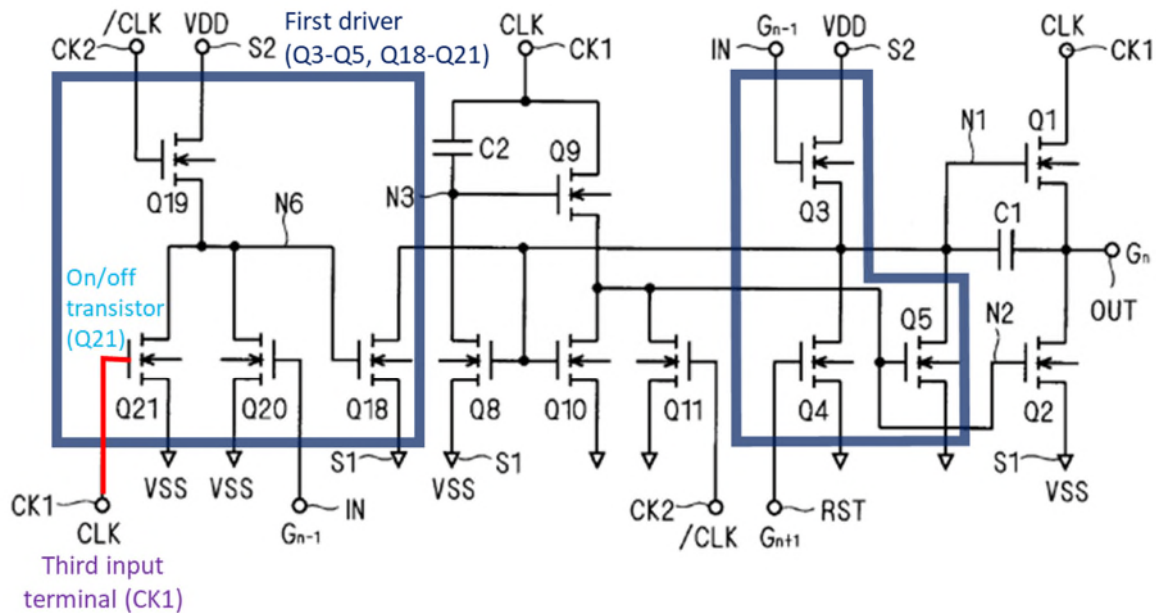
the element [1-C] requirement. As shown above, the **first node N2** is coupled to the gate electrode of transistors Q2 and Q5. Thus, **N2** controls the operation of Q2 and Q5, not vice versa. *See, e.g.*, Ex.1006 ¶¶0120, 0123-0124, 0132, 0134, 0136; Ex.1003 ¶434. On the other hand, the **first node N2** is coupled to the source or drain electrode of transistors Q9-Q11. Thus, the signals of the gate electrodes of these transistors, including /CLK of the **second input terminal** and the voltage of the **second node N1**, control the voltage of the **first node N2** by controlling on/off operation of transistors Q9-Q11. *See, e.g.*, Ex.1006 ¶¶0115, 0120-0121, 0123-0124, 0129-0132, 0134, 0136; Ex.1003 ¶¶431-433.

e) Element [1-D]

Tobita discloses that “the signal of the **third input terminal [CK1]** directly controls an on/off operation of a **transistor [Q21]**, the **transistor [Q21]** included in the **first driver**.” Ex.1003 ¶437.

The **third input terminal CK1** is directly coupled to the gate electrode of **transistor Q21**, which is part of the **first driver**:

F I G . 2 0



Ex.1006, Fig. 20; *see also id.* ¶0086; Ex.1003 ¶436.

Tobita further describes the first driver functioning in a manner matching the element [1-D] requirement. Because signal CLK of the **third input terminal CK1** is coupled to the gate electrode of **Q21**, CLK directly controls the on/off operation of **Q21**. Ex.1003 ¶436. For example, Tobita discloses that when CLK is high, Q21 is turned on. Ex.1006 ¶0177.

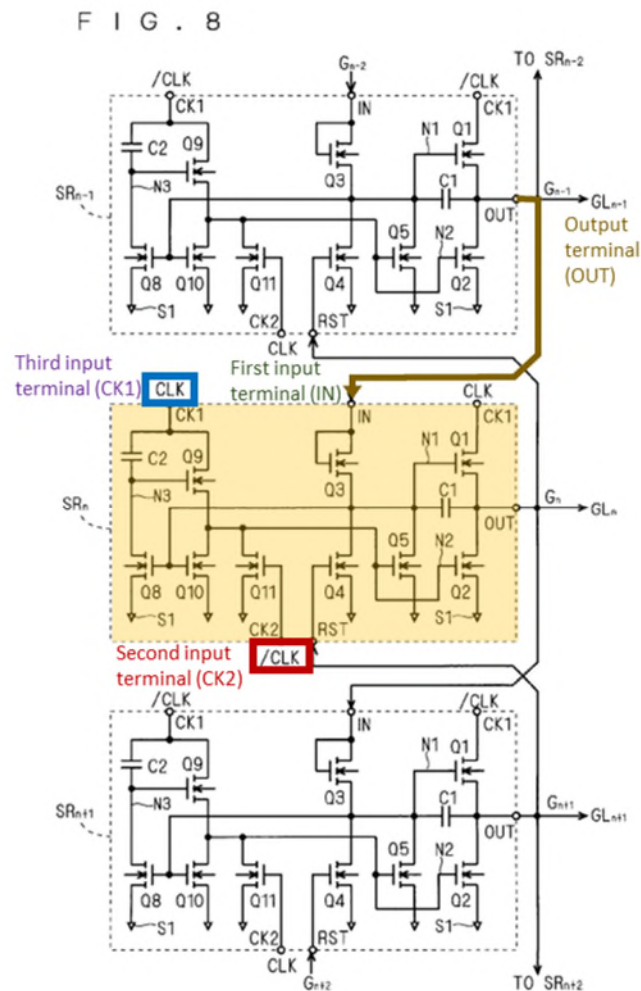
2. Claim 2

Claim 2 depends from Claim 1 and requires that “the first input terminal receives an output signal of a previous stage circuit or a start signal,” “the second input terminal receives a first clock signal,” and “the third input terminal receives a

second clock signal.”

Tobita discloses these additional limitations. Ex.1003 ¶440.

Tobita’s multistage shift register comprises stages of unit shift registers, *e.g.*, SR_{n-1} , SR_n , and SR_{n+1} :



Ex.1006, Fig. 8, ¶0117.

As shown, the first input terminal IN of SR_n receives output signal G_{n-1} of the previous stage circuit SR_{n-1} . The second input terminal CK2 of SR_n receives a

first clock signal /CLK, and the third input terminal CK1 of SR_n receives a second clock signal CLK. Both /CLK and CLK are clock signals. *Id.* ¶0118; *see also* Ex.1003 ¶¶441-445.

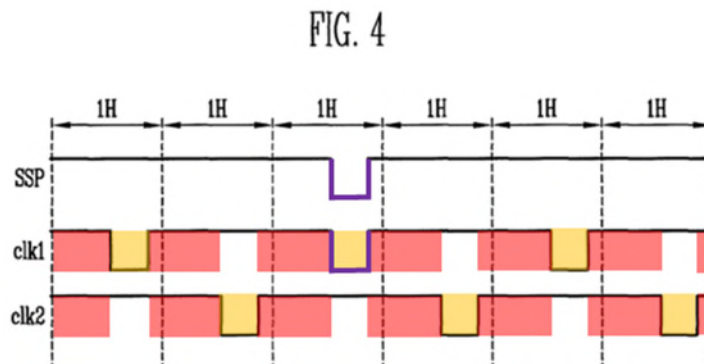
3. Claim 3

Claim 3 depends from Claim 2 and requires that “the first clock signal and the second clock signal have the same period and have phases that do not overlap.”

Tobita discloses this additional limitation. Ex.1003 ¶447.

In the context of the '593 patent, a POSITA would understand “phases that do not overlap” to refer to the active phases, during which the two clock signals activate transistors, do not overlap. Ex.1003 ¶450. It does not require the nonactive phases to also not overlap. *Id.*

This understanding is the only interpretation consistent with what the '593 patent discloses. The patent uses pMOS embodiments, which have a low active voltage. *See* Ex.1001 at 6:39-40. Accordingly, the low, active phases of the two clock signals do not overlap (shown in orange below), the fact that the high, inactive phases do coincide (red)) is not considered overlapping:



Id., Fig. 4 (partial); Ex.1003 ¶451.

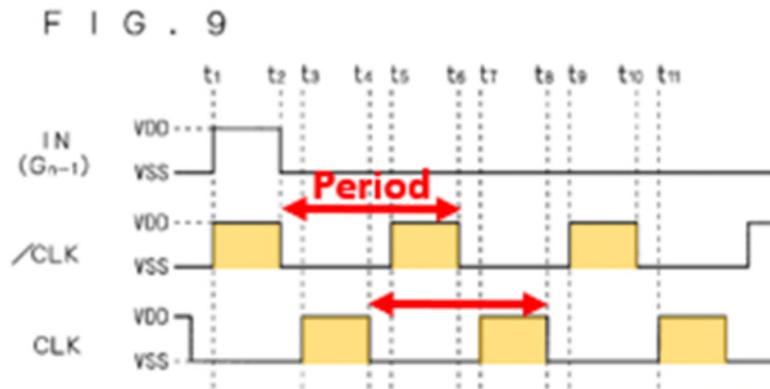
Consistent with this understanding, the '593 patent uses nonoverlapping *low* voltage as exemplary, not definitional. *See* Ex.1001 at 5:21-24 (“times when the first and second clock signals CLK1 and CLK2 are supplied, *e.g.*, the first and second clock signals CLK1 and CLK2 have a low level, do not overlap.”) (emphasis added); 5:24-28 (also using “*e.g.*” to clarify that *high*-voltage level may overlap).

This understanding is also consistent with the disclosure that “[t]he start signal may be supplied to overlap the first clock signal.” *Id.* at 2:4-5; *see also id.* at 3:51-53. Referring to the annotated Figure 4 above, the active-low SSP pulse overlaps with a low phase of the first clock signal clk1 (shown in purple).

Accordingly, for pMOS and nMOS circuits, Claim 3 requires nonoverlapping low and high clock phases, respectively. Ex.1003 ¶448.

Tobita’s circuits use nMOS transistors. *See, e.g.*, Tobita Fig. 20. Thus, the requirement of Claim 3 means high-level voltage, which turns on Tobita’s nMOS

transistors, of CLK and /CLK do not overlap. Clock signals /CLK and CLK have the same period and phases that do not overlap:



Ex.1006, Fig. 9 (partial); ¶¶0115, 0166; Ex.1003 ¶¶447, 449.

4. Claim 4

Claim 4 depends from Claim 3 and requires that “the first clock signal and the second clock signal have a period equal to two horizontal periods 2H and are supplied in different horizontal periods as low signals.”

Tobita discloses this additional limitation. Ex.1003 ¶461.

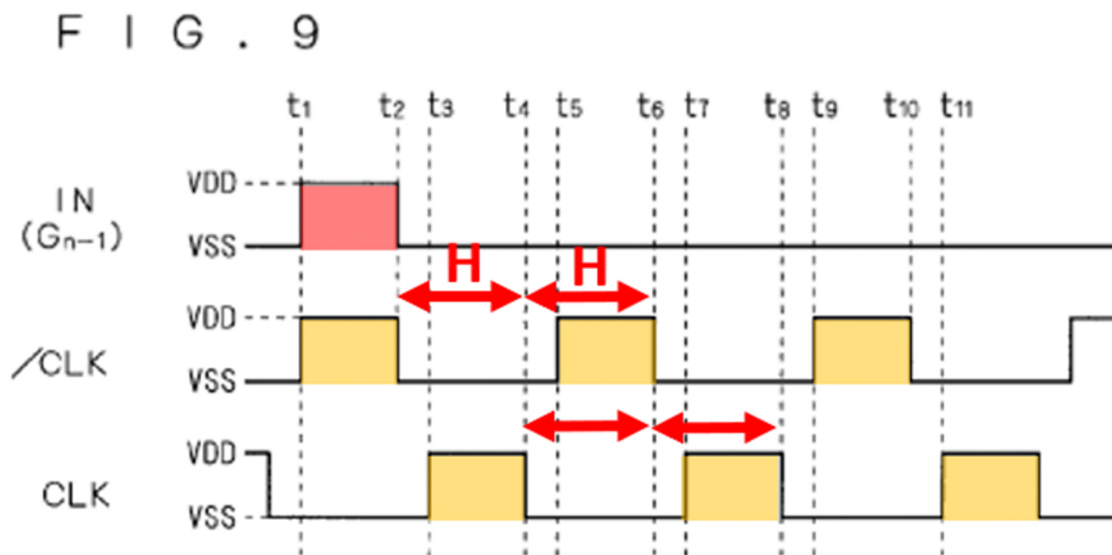
The '593 patent refers to “a period in which a scan signal is supplied to one scan line” as an exemplary horizontal period. Ex.1001 at 5:18-20. This disclosure, however, does not constitute lexicography because it is merely an example.

Constant v. Advanced Micro-Devices, Inc., 848 F.2d 1560, 1571 (Fed. Cir. 1988)

(“examples appearing in the specification will not generally be read into the claims.”). Instead, the horizontal period may be understood more broadly,

consistent with the patent disclosure. Ex.1003 ¶¶456-457.

Because the '593 patent uses pMOS transistors and Tobita's circuits use nMOS transistors, Claim 4 should be read to require the two clock signals to be supplied in different horizontal periods as *high* signals. See Ex.1006 ¶0108; Ex.1003 ¶¶458-459. The first clock signal /CLK and the second clock signal CLK have a period equal to two horizontal periods 2H (e.g., t_2 through t_6 or t_4 through t_8) and are supplied in different horizontal periods as high signals (shaded in orange).



Ex.1006, Fig. 9 (partial); see also *id.* ¶¶0115, 0166; Ex.1003 ¶460. Relatedly, the active-high polarity of the signal G_{n-1} of the first input terminal (shaded in red above) also supports construing claim 4 to require nonoverlapping high-level periods between $/CLK$ and CLK .

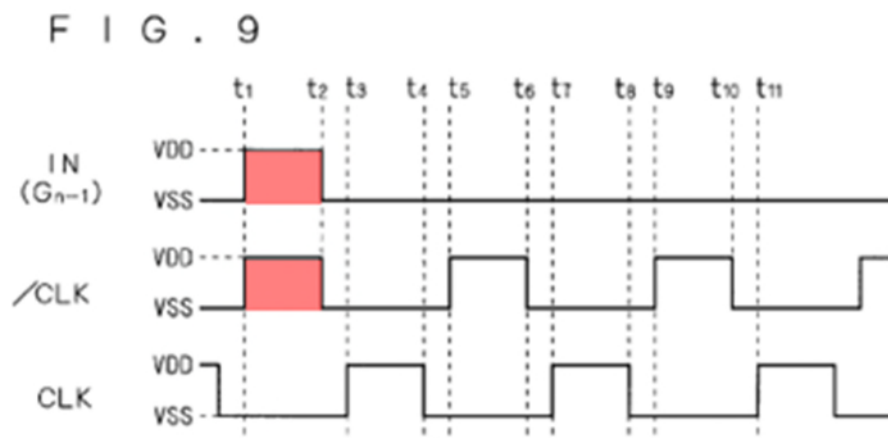
5. Claim 5

Claim 5 depends from Claim 2 and requires that “the start signal is supplied to overlap the first clock signal.”

Tobita discloses this additional limitation. Ex.1003 ¶467.

As discussed for Claim 2, the first clock signal reads on Tobita’s /CLK signal, which is input to CK2 of SR_n unit shift register. For SR_n , Tobita treats the output signal G_{n-1} from the immediately preceding stage equivalent to the start pulse SP the first stage SR_1 . Ex.1006 ¶0098. Put differently, SR_1 receives SP, not G_0 . Ex.1003 ¶¶464, 466.

G_{n-1} or equivalently the start pulse SP is supplied to overlap the first clock signal /CLK:



Ex.1006, Fig. 9 (partial); *see also id.*, Fig. 6 (same but showing SP instead of G_{n-1}); Ex.1003 ¶465.

6. Claim 14

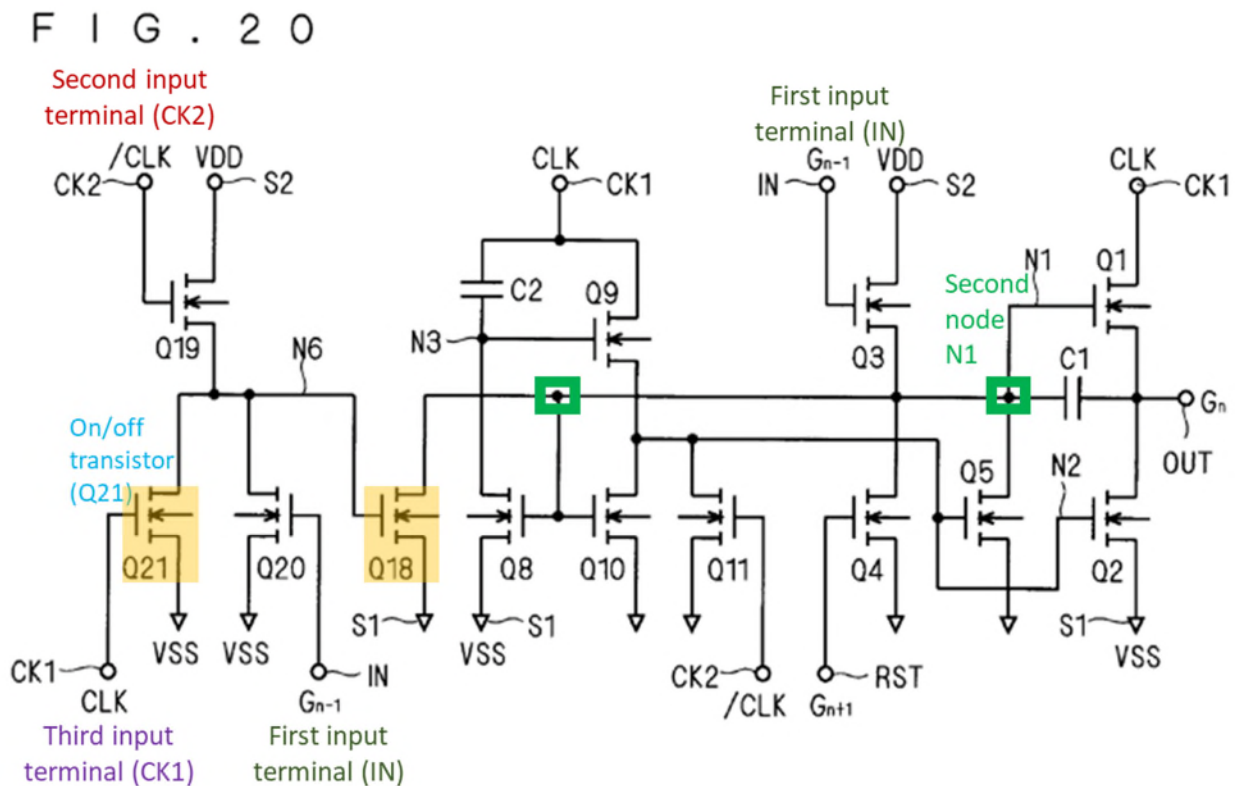
Claim 14 depends from Claim 1 and requires that “the transistor [Q21] controls the voltage of the second node [N1] according to the on/off operation thereof.”

At least under Patent Owner’s apparent interpretation of the claim, Tobita discloses this additional limitation. Ex.1003 ¶475.

In the related ITC proceeding, Patent Owner has broadly construed “control” in the phrases “a first/second driver to control the voltage of the second/first node” in Claims 1 and 15. Patent Owner argues that “control” is not limited to “directly control” and includes scenarios where “something other than the driver’s output is able to override that output” or where the driver controls the voltage of the node “in conjunction with other circuit elements.” Ex.1009 at 22-23. While Petitioner does not agree with Patent Owner’s construction, the Board can “rely[] on a patent owner’s own submissions in determining unpatentability.” *Rovalma, S.A. v. Bohler-Edelstahl GmbH & Co. KG*, 856 F.3d 1019, 1026-28 (Fed. Cir. 2017). Here, for instance, Tobita’s transistor Q21 controls the voltage of the second node N1 in conjunction with transistor Q18 under Patent Owner’s construction.

As explained for element [1-D], the transistor reads on Tobita’s transistor Q21. *See supra* Section VIII.C.1.e. The second node N1 is coupled to the drain electrode of transistor Q18, whose gate electrode is coupled to the drain electrode

of transistor Q21:



Ex.1006, Fig. 20, ¶0173; Ex.1003 ¶473.

Tobita discloses that transistor Q21, together with transistors Q18-Q20, controls the voltage of the second node N1 according to the on/off operation thereof. At a high level, “[t]he circuit formed of transistors Q18 to Q21 brings the [second] node N1 into the L level with low impedance during a period in which the [third] clock terminal CK1 is at the H level in the non-selected period of the gate line GL_n.” Ex.1006 ¶0172. Specifically, during the non-selected period of the gate line GL_n, G_{n-1} of the first input terminal [IN] is low, turning transistor Q20 off. *Id.* ¶0175. The on/off operation of Q21, which is determined by the third clock

terminal CK1, together with the on/off operation of Q19, which is determined by the second input terminal CK2, causes the voltage of node N6 to rise when CK2 is high and to fall when CK1 is high. *Id.* This in turn switches on or off transistor Q18, causing the second node N1 to remain at a low level when Q18 is on. *Id.* ¶0175. Accordingly, the transistor [Q21] controls the voltage of the second node N1 according to the on/off operation thereof at least under Patent Owner's apparent interpretation of the claim. Ex.1003 ¶¶473-475.

7. Independent Claim 15

Tobita renders obvious Claim 15. Ex.1003 ¶476.

a) [15-PRE]

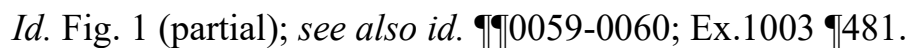
Claim 15's preamble recites "[a]n organic light emitting display." Based on Patent Owner's proposed constructions and infringement theories from the ITC matter, this preamble is not limiting because the display is not recited again in Claim 15 and is only recited in dependent claims 16-28 as "[t]he organic light emitting display as claimed in claim 15" or another claim depending from claim 15. *See Arctic Cat Inc. v. GEP Power Prod., Inc.*, 919 F.3d 1320, 1329-30 (Fed. Cir. 2019) (affirming the Board's finding that the preamble "[a] personal recreational vehicle comprising" is nonlimiting). Even if limiting, a POSITA would have found it obvious to apply Tobita's circuit, which meet elements [15-A]-[15-G] as explained below, to an OLED display as recited in the preamble.

Ex.1003 ¶479. For example, it was well known that LCD and OLED displays have pixels arranged in matrices and data drivers and scan drivers. *Id.* ¶478. It was also well known that function of the stage circuits for LCD and OLED are functionally similar and could be accomplished by similar circuits. *See, e.g.*, Ex.1015 at 14-16 (claims 1, 14).

b) Element [15-A]

Tobita discloses “pixels positioned in regions partitioned by scan lines and data lines.” Ex.1003 ¶480.

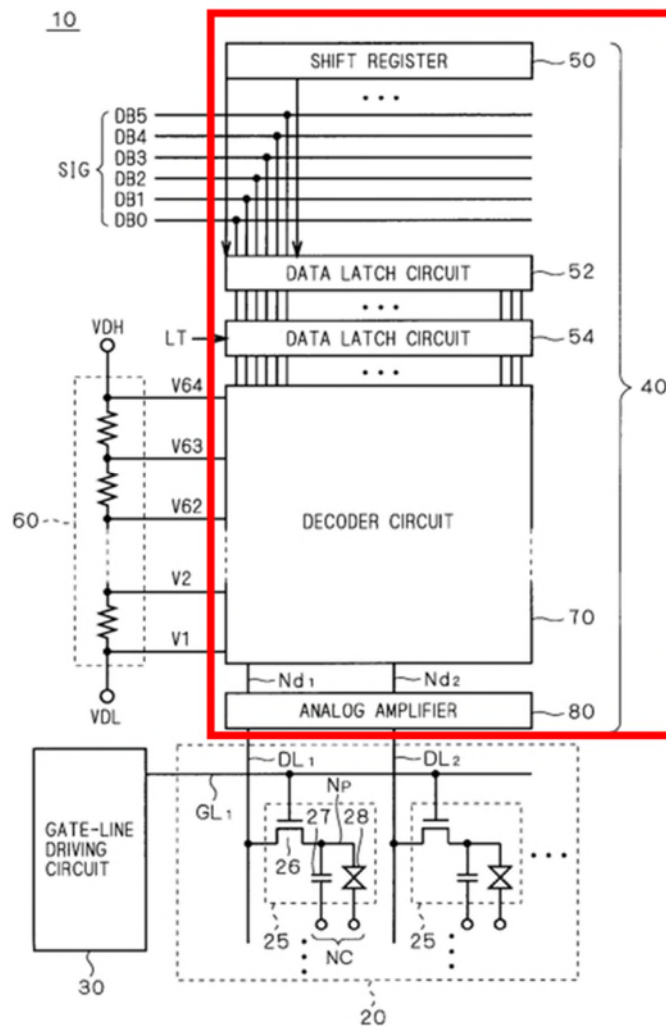
Tobita depicts a display comprising “pixels 25 arrayed in a matrix.” Ex.1006 ¶0059. Gate lines GL₁, GL₂, etc. are connected to rows of pixels and data lines DL₁, DL₂, etc. are connected to columns of pixels. *Id.* Gate lines are the same as scanning lines. *Id.* ¶0004. The scan lines and data lines partition the display into regions in which the pixels (*i.e.*, the smaller dotted boxes) are positioned:



Tobita discloses “a data driver for supplying data signals to the pixels through the data lines.” Ex.1003 ¶483.

-111-

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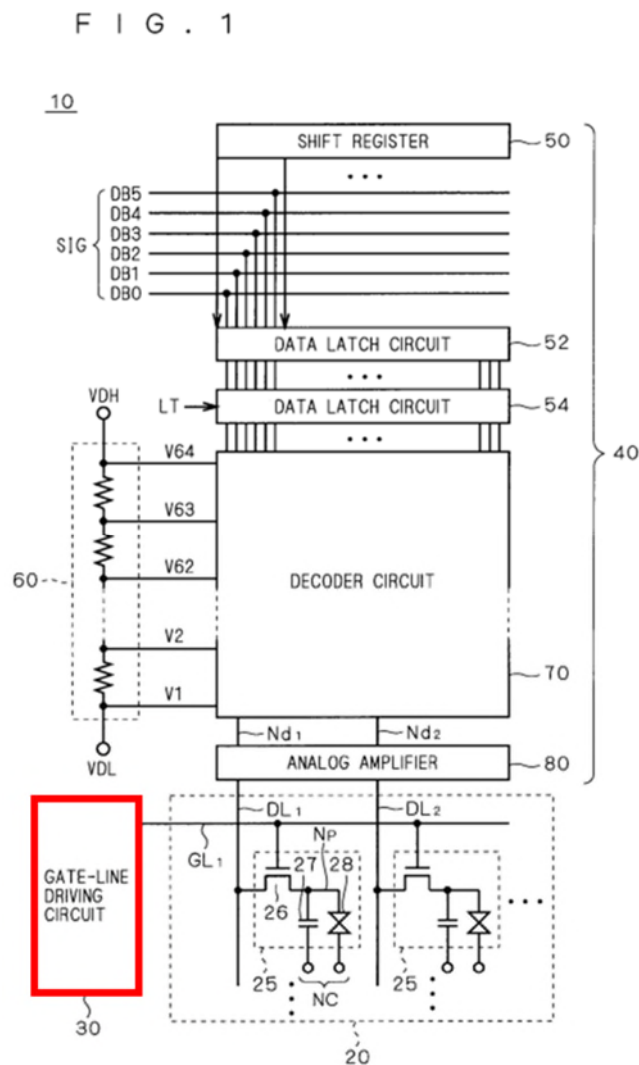
Ex.1006, Fig. 1; Ex.1003 ¶484.

d) Element [15-C]

Tobita discloses “a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input

terminal, and an output terminal.” Ex.1003 ¶497.

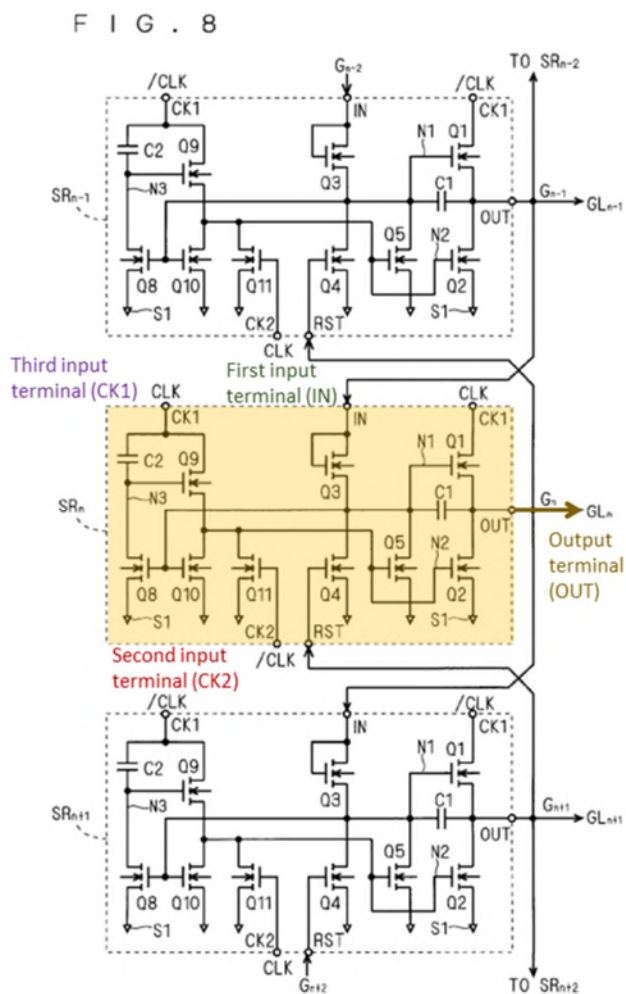
Tobita depicts a “a gate-line driving circuit (scanning-line driving circuit) 30.” Ex.1006 ¶0058. The scan line drive circuit “sequentially drives the gate lines GL_1 , GL_2 , #. . . in synchronization with the scanning cycle.” *Id.* ¶0071; *see also id.* ¶0061.



Ex.1006, Fig. 1; *see also* Ex.1003 ¶¶487-489.

The scan line drive circuit, which in an embodiment is a multistage shift register, can comprise “cascade-connected unit shift registers SR.” Ex.1006

¶0167. Each of the unit shift registers is a stage circuit generating a corresponding scan signal G_n of the scan signals and having a first input terminal IN, a second input terminal CK2, a third input terminal CK1, and an output terminal OUT as explained for Claim 1. Further, the stage circuit or unit shift register is coupled to a scan line GL:

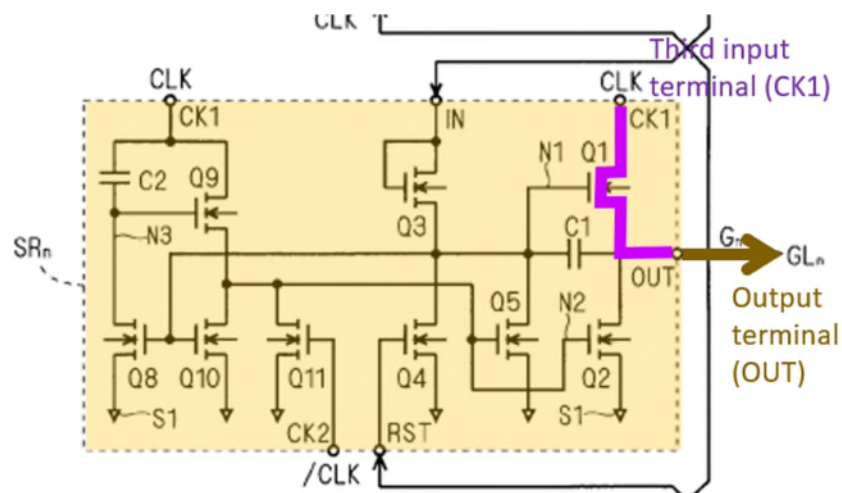


e) Elements [15-D] through [15-G]

8. Claim 16

Tobita discloses this additional limitation. Ex.1003 ¶509.

Gate lines are the same as scan lines. Ex.1006 ¶0004. The signal G_n of the output terminal OUT is output as a gate or scan signal. *See also id.* ¶¶0117, 0125. Tobita's outputting unit supplies a signal (CLK) of the third input terminal (CK1) to the output terminal (OUT) according to a voltage applied to the second node (N1). Ex.1006 ¶¶0109, 122, 126.



Id., Fig. 8 (partial); Ex.1003 ¶¶510--514.

9. Claim 17

The additional limitation of Claim 17 is the same as element [2-A] because a scan signal is an output signal as explained for Claim 16. Thus, Tobita discloses Claim 17 for the same reasons discussed for Claim 2. *See supra* Section VIII.C.2; Ex.1003 ¶¶516-519.

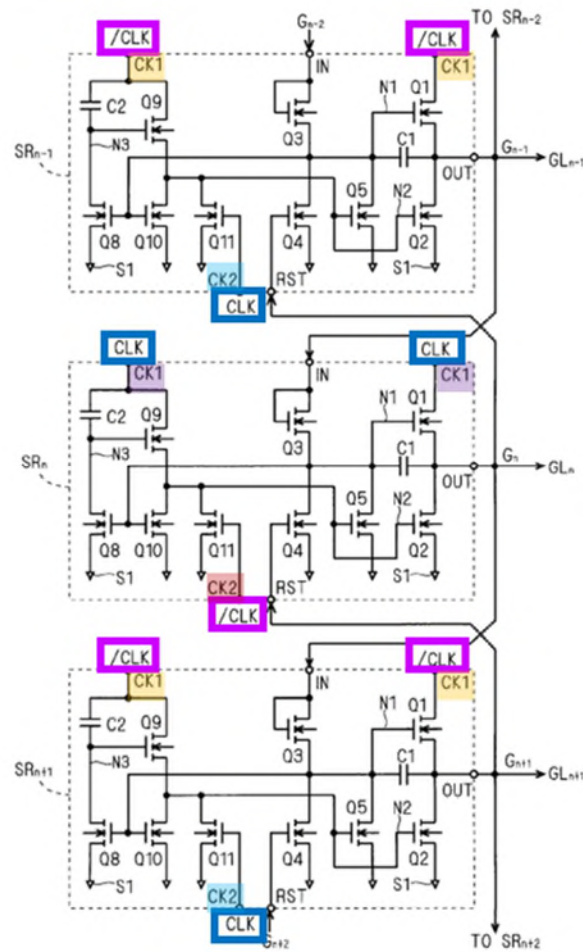
10. Claim 18

Claim 18 depends from Claim 17 and requires that the “second input terminals of odd stage circuits receive a first clock signal and third input terminals of odd stage circuits receive a second clock signal” and “second input terminals of even stage circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal.”

Tobita discloses these additional limitations. Ex.1003 ¶526.

In the odd stage circuits (*e.g.*, stage circuits SR_n), the second input terminals (CK2) receive a first clock signal (/CLK) and the third input terminals (CK1) receive a second clock signal (CLK). And in the even stage circuits (*e.g.*, stage circuits SR_{n-1} and SR_{n+1}), the second input terminals (CK2) receive the second clock signal (CLK) and the third input terminals (CK1) receive the first clock signal (/CLK):

FIG. 8



Ex.1006, Fig. 8; *see also* Ex.1003 ¶¶521-525.

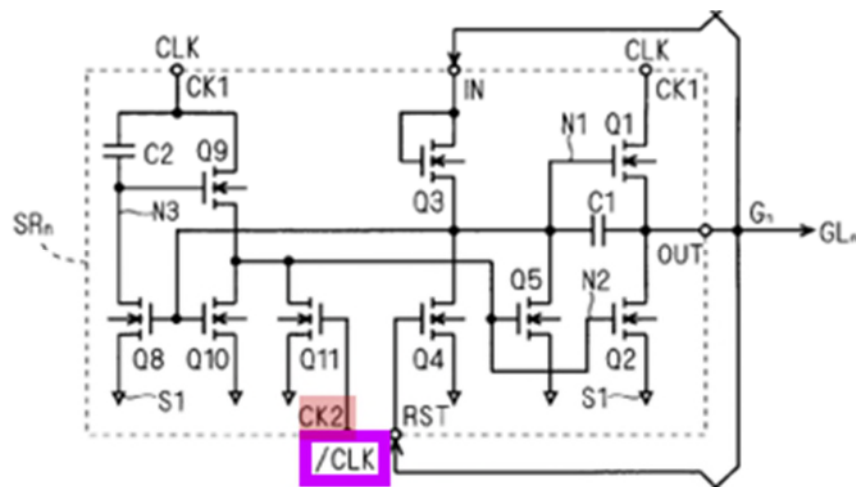
11. Claim 19

The additional limitation of Claim 19 is the same as that of Claim 3. Thus, Tobita discloses Claim 19 for the same reasons discussed for Claim 3. *See supra* Section VIII.C.3; Ex.1003 ¶¶527-530.

12. Claim 25

Claim 25 depends from Claim 18 and requires that “the scan signal of the

previous stage circuit or the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal.” The second alternative in this limitation is the same as the additional limitation of claim 5 (“the start signal is supplied to overlap the first clock signal”) because Tobita’s start signal SP is supplied to the first input terminal IN, and Tobita’s first clock signal /CLK is supplied to the second input terminal CK2 at $SR_{n=1}$:



Ex.1006, Fig. 8 (partial).

Thus, Tobita discloses Claim 25 for at least the same reasons discussed for Claim 5. *See supra* Section VIII.C.5; Ex.1003 ¶¶532-535; *see also id.* ¶¶536-541 (explaining that Tobita also discloses the first alternative).

D. GROUND 4: Tobita in View of Jeong Renders Claims 7 and 21 Obvious

1. Claim 7

Claim 7 depends from Claim 2 and requires that “the outputting unit

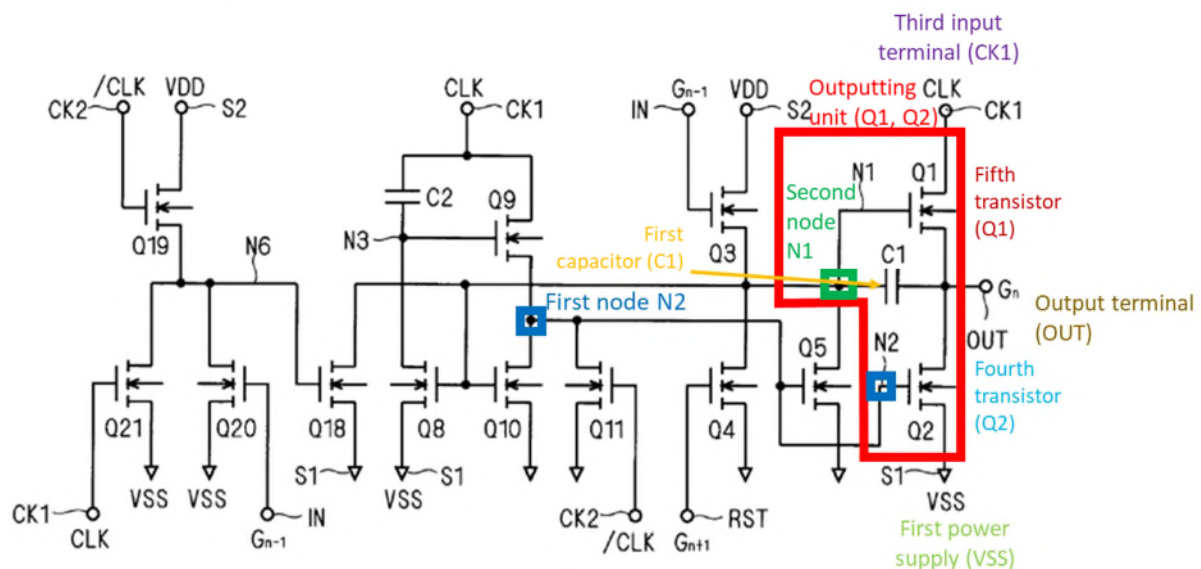
includes: a **fourth transistor [Q2]** between the **first power supply [VSS]** and the **output terminal [OUT]**, the **fourth transistor [Q2]** having a gate electrode coupled to the **first node [N2]**,” “a **fifth transistor [Q1]** between the **output terminal [OUT]** and the **third input terminal [CK1]**, the **fifth transistor [Q1]** having a gate electrode coupled to the **second node [N1]**,” “a **first capacitor [C1]** between the **second node [N1]** and the **output terminal [OUT]**,” and “a **second capacitor** between the **first node [N2]** and the **first power supply [VSS]**.”

Tobita in view of Jeong renders obvious these additional limitations.

Ex.1003 ¶559.

Tobita’s **outputting unit** contains all of the required components except the **second capacitor**, arranged in the recited configuration:

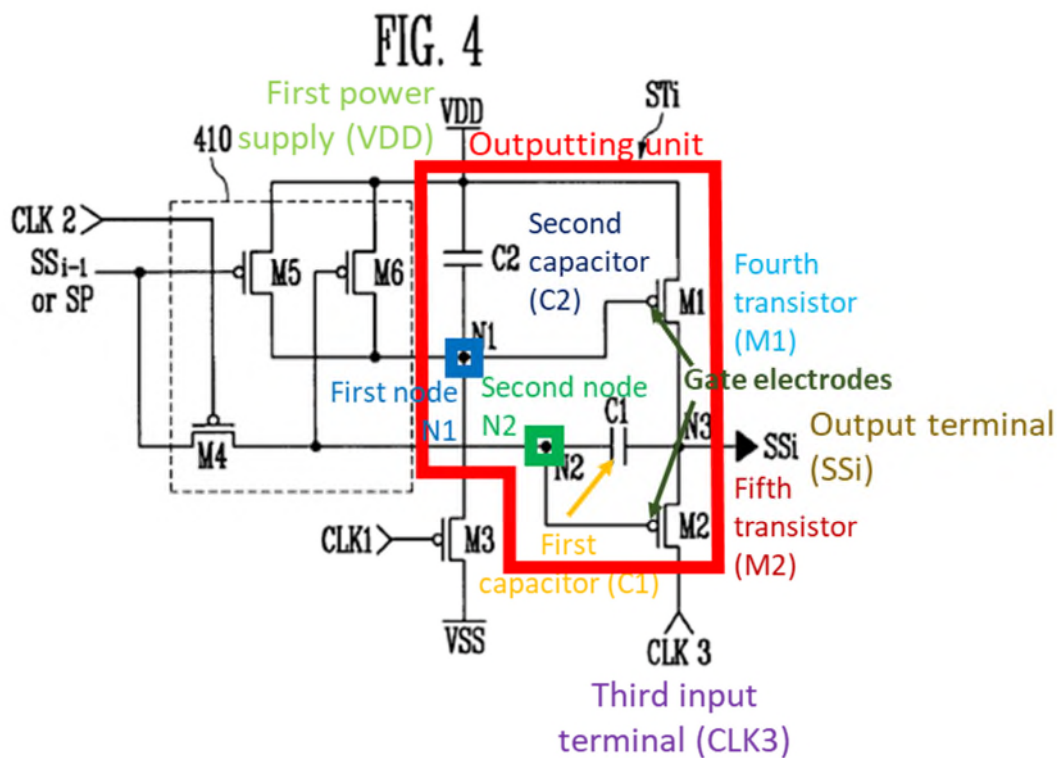
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Ex.1006, Fig. 20; see also Ex.1003 ¶549.

A POSITA would have recognized that first node N2 only has a small amount of capacitance and thus the first node may not adequately maintain a fixed voltage level in the presence of perturbations in electrical charge level or when the node is electrically isolated, *e.g.*, when Q9-Q11 are all turned off. Ex.1003 ¶550. In order to avoid this and increase the robustness of the outputting unit's operation, a POSITA would be motivated to add a capacitor to this node as taught by Jeong. *Id.* ¶¶551-554.

Jeong's **outputting unit** contains all of the components in Tobita's **outputting unit** plus the **second capacitor C2**, arranged in the recited configuration:



See also Ex.1007 ¶¶0045, 0052-0053, 0056-0057, Ex.1003 ¶557.

Specifically, Jeong discloses that its “outputting unit includes: a fourth transistor [M1] between the first power supply [VDD] and the output terminal [SSi], the fourth transistor [M1] having a gate electrode coupled to the first node [N1],” “a fifth transistor [M2] between the output terminal [SSi] and the third input terminal [CLK3], the fifth transistor [M2] having a gate electrode coupled to the second node [N2],” “a first capacitor [C1] between the second node [N2] and the output terminal [SSi],” and “a second capacitor [C2] between the first node [N1] and the first power supply [VDD].”

Jeong discloses that the second capacitor C2 “function[s] to reduce a variation of a voltage, which may be applied to the first power supply VDD or the first node N1.” Ex.1007 ¶0057; Ex.1003 ¶¶555-557. Thus, Tobita in view of Jeong renders obvious the additional requirements of Claim 7. Ex.1003 ¶558.

2. Motivation to Combine

A POSITA would have found it obvious to combine the features of Jeong with Tobita to reduce voltage variation of power supply VSS or the first node N4.

First, Tobita and Jeong both relate to shift registers in a scan driver for pixel-matrix displays. Thus, a POSITA would have been aware of both references and would have studied the advantages of the respective designs. Ex.1003 ¶544.

Further, MOS-transistor circuits, as well as such circuits for drivers of pixel-matrix display, were a known and long-explored subject for years before 2012. *Id.* Thus,

a POSITA would have had extensive knowledge about such circuits. Accordingly, it would have been common sense among POSITAs to integrate compatible circuits to achieve respective advantages. *Id.* Such combinations would have yielded predictable results based on well-known circuit-design principles. *Id.*

Specifically, a POSITA would have been motivated to combine Tobita with Jeong because both are directed to shift registers used in scan drivers. *Id.* ¶545. Both use a single type of MOS transistors and are thus compatible for combination. *Id.* Although Tobita illustrates its embodiments using nMOS transistors and Jeong uses pMOS transistors, the translation from one type to the other were well known. *Id.* Further, the similarity of the functions and designs of Tobita and Jeong would have further confirmed a POSITA's understanding that combining the teachings of the two involved straightforward modifications with predictable outcomes and a reasonable expectation of success. *Id.*

A POSITA would have further found it obvious that Tobita's outputting unit may be modified as disclosed in Jeong, because the two outputting units share essentially the same components in the same configuration. *Id.* ¶546. Further, a POSITA would have recognized that unintended voltage variation in a circuit was undesirable and would be motivated to add the second capacitor C2 between Tobita's first power supply VSS and first node N2 to reduce voltage variation of N2, as taught by Jeong. *Id.* ¶¶550-554. A POSITA would have recognized that

adding a capacitor for such a purpose was a common application of capacitors, and adding a capacitor as taught by Jeong involved nothing more than applying a well-understood technique with predictable results and a reasonable expectation of success. *Id.* ¶¶555-558.

3. Claim 21

The additional limitation of Claim 21 is the same as that of Claim 7. Thus, Tobita in view of Jeong renders obvious Claim 21 for the same reasons discussed for Claim 7. *See supra* Section VIII.D.1; Ex.1003 ¶¶560-562.

IX. SECONDARY CONSIDERATIONS

Petitioner is not aware of any secondary considerations that would overcome the strong showing of obviousness provided by the Petition. Ex.1003 ¶563.

Further, any attempt by Patent Owner to rely on alleged secondary considerations cannot overcome the showing of obviousness detailed above. *Tokai Corp. v.*

Easton Enters., Inc., 632 F.3d 1358, 1370 (Fed. Cir. 2011).

X. CONCLUSION

For the foregoing reasons, Petitioner respectfully requests the Board institute review of the '593 patent and cancel all Challenged Claims.

Inter Partes Review

United States Patent No. 9,330,593

Date: July 26, 2023

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,330,593 PURSUANT TO 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42 complies with the type volume limitation in 37 C.F.R. § 42.24(a)(1). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, a table of authorities, mandatory notices under § 42.8, certificate of service, certificate of word count, or listing of exhibits, and claim listing—contains 13,531 words.

Dated: July 26, 2023

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,330,593 PURSUANT TO 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42 and associated Exhibits 1001-1015 were caused to be served on July 26, 2023 via overnight courier upon the following counsel of record for Patent Owner:

27849 – Lee IP Law, P.C.
Attn: Eugene Lee
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Re: Samsung Display Co., Ltd; U.S. Patent No. 9,330,593

Courtesy copies were also served via email on Patent Owner's counsel of record in a related ITC investigation styled *Certain Active Matrix Organic Light-Emitting Diode Display Panels And Modules For Mobile Devices, And Components Thereof*, Inv. No. 337-TA-1351 (Violation) ITC-337-TA-1351; and in a related district court litigation styled *Samsung Display Co., Ltd. v. BOE Technology Co., Ltd.*, E.D. Tex. 2-23-cv-00309:

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Inter Partes Review

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