



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/771,385	05/03/2016	9330593	304/1043	3091

27849 7590 04/13/2016
LEE & MORSE, P.C.
3141 FAIRVIEW PARK DRIVE
SUITE 500
FALLS CHURCH, VA 22042

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 184 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Hwan-Soo JANG, Yongin-City, KOREA, REPUBLIC OF;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27849 7590 01/04/2016
LEE & MORSE, P.C.
3141 FAIRVIEW PARK DRIVE
SUITE 500
FALLS CHURCH, VA 22042

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/771,385	02/20/2013	Hwan-Soo JANG	304/1043	3091

TITLE OF INVENTION: STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	04/04/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAM, LONG D	2691	345-082000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Lee & Morse, P.C.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

SAMSUNG DISPLAY CO., LTD.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Yongin-City, Gyeonggi-Do, Republic of Korea

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

☐ A check is enclosed.

☒ Payment by credit card. Form PTO-2038 is attached.

☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 50-1645 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature

Lilia C. Lord

Date April 1, 2016

Typed or printed name

Lilia C. Lord /Lilia C. Lord/

Registration No. 58,420

Mianyang BOE Ex. 1002
Case No. IPR2023-01221

Electronic Patent Application Fee Transmittal

Application Number:	13771385			
Filing Date:	20-Feb-2013			
Title of Invention:	STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME			
First Named Inventor/Applicant Name:	Hwan-Soo JANG			
Filer:	Susan S. Morse/Sharon Bender			
Attorney Docket Number:	304/1043			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt

EFS ID:	25372350
Application Number:	13771385
International Application Number:	
Confirmation Number:	3091
Title of Invention:	STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME
First Named Inventor/Applicant Name:	Hwan-Soo JANG
Customer Number:	27849
Filer:	Susan S. Morse/Sharon Bender
Filer Authorized By:	Susan S. Morse
Attorney Docket Number:	304/1043
Receipt Date:	01-APR-2016
Filing Date:	20-FEB-2013
Time Stamp:	13:13:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$960
RAM confirmation Number	10297
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Mianyang BOE Ex. 1002
Case No. IPR2023-01221

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Issue_Fee_Transmittal_2016_04_01_As_Filed.pdf	104181 2da6f8cd539c72d925d6dfd89db785aafe3be27	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30807 de33d2b692e2b4e55c2c89915d3a3a1fed9c5329	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			134988		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

27849 7590 01/04/2016
LEE & MORSE, P.C.
3141 FAIRVIEW PARK DRIVE
SUITE 500
FALLS CHURCH, VA 22042

EXAMINER

PHAM, LONG D

ART UNIT

PAPER NUMBER

2691

DATE MAILED: 01/04/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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13/771,385

02/20/2013

Hwan-Soo JANG

304/1043

3091

TITLE OF INVENTION: STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	04/04/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

27849 7590 01/04/2016
LEE & MORSE, P.C.
3141 FAIRVIEW PARK DRIVE
SUITE 500
FALLS CHURCH, VA 22042

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

_____ (Depositor's name)
_____ (Signature)
_____ (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/771,385	02/20/2013	Hwan-Soo JANG	304/1043	3091

TITLE OF INVENTION: STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	04/04/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAM, LONG D	2691	345-082000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

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NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/771,385	02/20/2013	Hwan-Soo JANG	304/1043	3091

27849 7590 01/04/2016
LEE & MORSE, P.C.
3141 FAIRVIEW PARK DRIVE
SUITE 500
FALLS CHURCH, VA 22042

EXAMINER

PHAM, LONG D

ART UNIT	PAPER NUMBER
----------	--------------

2691

DATE MAILED: 01/04/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/771,385	Applicant(s) JANG, HWAN-SOO	
	Examiner LONG D. PHAM	Art Unit 2691	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 17 September 2015.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-28. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☒ All b) ☐ Some *c) ☐ None of the:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. ☒ Notice of References Cited (PTO-892) | 5. ☐ Examiner's Amendment/Comment |
| 2. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date ____ | 6. ☒ Examiner's Statement of Reasons for Allowance |
| 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. ☐ Other ____. |
| 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date ____. | |

/LONG D PHAM/
Primary Examiner, Art Unit 2691

Rejoin Claims

1. Please rejoin claims 9-13 and 22-26:

9-13 (Rejoined).

22-26 (Rejoined).

2. Claims 9-13 and 22-26 are previously withdrawn from consideration as a result of the election restriction, is hereby rejoined.

Because claims 9-13 and 22-26 were previously withdrawn from consideration under 37 CFR 1.142 have been rejoined, **the restriction requirement as set forth in the Office action mailed on October 21, 2014 is hereby withdrawn.** In view of the withdrawal of the restriction requirement as to the rejoined inventions, applicant(s) are advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Once the restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Jeong (U.S. Patent Pub. No. 2010/0171689) discloses a shift register and organic light emitting display device using the same.

Chung (U.S. Patent Pub. No. 2012/0013588) discloses a display, scan driving apparatus for the display, and driving method thereof.

Kim et al (U.S. Patent Pub. No. 2009/0262051) discloses an organic light emitting display device.

Lee et al (U.S. Patent Pub. No. 2013/0002630) discloses a scan driver and organic light emitting display using the same.

Reasons for Allowance

4. None of the prior art of record teaches an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node...the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.

Inquiries

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LONG D. PHAM whose telephone number is (571)270-5573. The examiner can normally be reached on Monday - Friday: 8:00a.m. - 5:00p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571)272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/LONG D PHAM/
Primary Examiner, Art Unit 2691

Notice of References Cited	Application/Control No. 13/771,385		Applicant(s)/Patent Under Reexamination JANG, HWAN-SOO	
	Examiner LONG D. PHAM		Art Unit 2691	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2009/0262051 A1	10-2009	Kim; Se-Ho	G09G3/3266	345/80
*	B	US-2010/0171689 A1	07-2010	Jeong; Seonl	G11C19/18	345/100
*	C	US-2012/0013588 A1	01-2012	Chung; Kyung-Hoon	G09G3/3266	345/211
*	D	US-2013/0002630 A1	01-2013	Lee; Hae-Yeon	G09G3/3266	345/211
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



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BIB DATA SHEET

CONFIRMATION NO. 3091

SERIAL NUMBER 13/771,385	FILING or 371(c) DATE 02/20/2013 RULE	CLASS 345	GROUP ART UNIT 2691	ATTORNEY DOCKET NO. 304/1043		
APPLICANTS INVENTORS Hwan-Soo JANG, Yongin-City, KOREA, REPUBLIC OF; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** REPUBLIC OF KOREA 10-2012-0104512 09/20/2012 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 03/11/2013						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and Acknowledged <u>/LONG PHAM/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY KOREA, REPUBLIC OF	SHEETS DRAWINGS 7	TOTAL CLAIMS 27	INDEPENDENT CLAIMS 2
ADDRESS LEE & MORSE, P.C. 3141 FAIRVIEW PARK DRIVE SUITE 500 FALLS CHURCH, VA 22042 UNITED STATES						
TITLE STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME						
FILING FEE RECEIVED 1774	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

Search Notes 	Application/Control No. 13771385	Applicant(s)/Patent Under Reexamination JANG, HWAN-SOO
	Examiner JOHN KIRKPATRICK	Art Unit 2691

CPC- SEARCHED		
Symbol	Date	Examiner
G09G3/3677, 2310/0286	1/20.2015	JCK

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner
g09g3/2003-2092,30-3291,3406-3426,36-3696 g09g2300/04-0465,0469-0495,08-0895. g09g2310/0202-024,0243-0259,0264-0297,06-068 g09g2320/02-0295,04-048,06-106 g09g2330/02-12 (Text search)	Dec. 27, 2015	LP

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
345	98-100	Dec. 27, 2015	LP

SEARCH NOTES		
Search Notes	Date	Examiner
EAST: Inventor Name Search	1/30/2015	JCK
EAST: (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB) see search history printout	1/28/2015-1/30/2015	JCK
EAST: Search updated - see search history printout.	6/10/2015-6/11/2015	JCK
EAST: Search updated - see search history printout.	8/1/2015	JCK
EAST: update text search	Dec. 27, 2015	LP

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
EAST:	Interference search	Dec. 27, 2015	LP

/LONG D PHAM/
Primary Examiner.Art Unit 2691

Issue Classification 	Application/Control No. 13771385	Applicant(s)/Patent Under Reexamination JANG, HWAN-SOO	
	Examiner LONG D PHAM	Art Unit 2691	

CPC						
Symbol					Type	Version
G09G		3		22	F	2013-01-01
H03L		7		00	I	2013-01-01
G09G		3		32	I	2013-01-01
						
						
						
						
						
						
						
						
						
						
						

CPC Combination Sets					
Symbol		Type	Set	Ranking	Version
					
					

		Total Claims Allowed: 28	
(Assistant Examiner) /LONG D PHAM/ Examiner.Art Unit 2691	(Date) 12/27/2015	O.G. Print Claim(s) 1	O.G. Print Figure 2 and 3
(Primary Examiner)	(Date)		

Issue Classification 	Application/Control No. 13771385	Applicant(s)/Patent Under Reexamination JANG, HWAN-SOO
	Examiner LONG D PHAM	Art Unit 2691

☐ Claims renumbered in the same order as presented by applicant															
☐ CPA															
☐ T.D.															
☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	18	17												
2	2	19	18												
3	3	20	19												
4	4	21	20												
5	5	22	21												
6	6	23	22												
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9	9	27	25												
10	10	28	26												
11	11	25	27												
12	12	14	28												
13	13														
15	14														
16	15														
17	16														

(Assistant Examiner)		(Date)		Total Claims Allowed:	
				28	
/LONG D PHAM/ Examiner.Art Unit 2691		12/27/2015		O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)		(Date)		1	2 and 3

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	88344	345/204-215,690-699,87-111.ccls. 377/64-81.ccls. 349/40-55.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:23
L2	197216	g09g3/2003-2092,30-3291,3406- 3426,36-3696.cpc. g09g2300/04- 0465,0469-0495,08-0895.cpc. g09g2310/0202-024,0243- 0259,0264-0297,06-068.cpc. g09g2320/02-0295,04-048,06- 106.cpc. g09g2330/02-12.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:23
L3	234261	L1 L2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:23
L4	499829	(scan\$4 gate\$2) near2 (driv\$4 circuit\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:23
L5	254416	shift\$4 near3 (register\$2 stage\$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:24
L6	128994	second near3 (clock\$2 clk)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:24
L7	2936075	output\$4 near3 (unit\$2 circuit\$3 part\$2 transistor\$2 tft\$2 switch\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:25
L8	28253	6 same 7	US-PGPUB;	OR	OFF	2015/12/27

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			18:26
L9	3757	4 and 5 and 8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:26
L10	1793	3 and 9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:26
L11	1344414	(start\$2 near2 (pulse\$2 voltage\$2 signal\$2)) ssp sp	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:26
L12	1391	10 and 11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:26
L13	205139	second near3 node\$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:26
L14	676	12 and 13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:27
L15	128994	second near3 (clock\$2 clk)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:27
L16	1344414	(start\$2 near2 (pulse\$2 voltage\$2 signal\$2)) ssp sp	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2015/12/27 18:27

			IBM_TDB			
L17	499829	(scan\$4 gate\$2) near2 (driv\$4 circuit\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:27
L18	902478	output\$4 near3 (terminal\$2 node\$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:27
L19	3962170	stage\$2 (shift\$3 near3 register\$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:27
L20	234261	L1 L2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:27
L21	2376	L15 and L16 and L17 and L18 and L19 and L20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:27
L22	196392	next near3 (stage\$2 register\$2 shift\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:27
L23	1452	L21 and L22	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:27
L24	295779	second near3 (driver\$2 driving\$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:27
L25	856	L23 and L24	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	OFF	2015/12/27 18:27

			JPO; DERWENT; IBM_TDB			
L26	385	14 not L25	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:27
L27	18	("20110227884" "20070040771" "20070242000" "20080062097" "20080130822" "20100177087" "8466905" "20110216874").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/27 18:42
S1	25	((Hwan-Soo) near2 (JANG)).INV.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/12/22 14:41
S2	15	("20110227884" "8553026" "20120327131" "20080062097" "20120062525" "20110115835").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/22 14:42
S3	11003	345/98-100.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/22 14:54
S4	1	13/771385	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/22 14:54
S5	12587	((G09G3/22 OR G09G3/32 OR H03L7/00).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/22 14:54
S6	88298	345/204-215,690-699,87-111.ccls. 377/64-81.ccls. 349/40-55.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/22 14:55
S7	197075	g09g3/2003-2092,30-3291,3406- 3426,36-3696.cpc. g09g2300/04- 0465,0469-0495,08-0895.cpc. g09g2310/0202-024,0243- 0259,0264-0297,06-068.cpc. g09g2320/02-0295,04-048,06-	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2015/12/22 14:55

		106.cpc. g09g2330/02-12.cpc.	IBM_TDB			
S8	234118	S6 S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/22 14:56
S9	23460	S3 S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/22 14:56
S10	128933	second near3 (clock\$2 clk)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/22 16:07
S11	1343999	(start\$2 near2 (pulse\$2 voltage\$2 signal\$2)) ssp sp	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/22 16:08
S12	499551	(scan\$4 gate\$2) near2 (driv\$4 circuit\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/22 16:08
S13	901822	output\$4 near3 (terminal\$2 node\$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/22 16:09
S14	3959776	stage\$2 (shift\$3 near3 register\$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/22 16:09
S15	88298	345/204-215,690-699,87-111.ccls. 377/64-81.ccls. 349/40-55.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/22 16:13
S16	197075	g09g3/2003-2092,30-3291,3406- 3426,36-3696.cpc. g09g2300/04- 0465,0469-0495,08-0895.cpc. g09g2310/0202-024,0243-	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	OFF	2015/12/22 16:13

		0259,0264-0297,06-068.cpc. g09g2320/02-0295,04-048,06- 106.cpc. g09g2330/02-12.cpc.	JPO; DERWENT; IBM_TDB			
S17	234118	S15 S16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/22 16:13
S18	2371	S10 and S11 and S12 and S13 and S14 and S17	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/22 16:13
S19	196294	next near3 (stage\$2 register\$2 shift\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/22 16:19
S20	1450	S18 and S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/22 16:19
S21	295439	second near3 (driver\$2 driving\$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/22 16:19
S22	855	S20 and S21	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/12/22 16:20

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L28	2839	"outputting unit".clm.	US-PGPUB; USPAT	OR	OFF	2015/12/27 20:29
L29	6952	"second driver".clm.	US-PGPUB; USPAT	OR	OFF	2015/12/27 20:30
L30	32067	"second node".clm.	US-PGPUB; USPAT	OR	OFF	2015/12/27 20:30
L31	2349	"third input terminal".clm.	US-PGPUB; USPAT	OR	OFF	2015/12/27 20:30
L32	1	28 and 29 and 30 and 31	US-PGPUB; USPAT	OR	OFF	2015/12/27

12/ 27/ 2015 8:46:00 PM

C:\ Users\ lpham8\ Documents\ EAST\ Workspaces\ 13771385.wsp

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Request for Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	13/771,385
Filing Date	February 20, 2013
First Named Inventor	Hwan-Soo JANG
Art Unit	2691
Examiner Name	John Kirkpatrick
Attorney Docket Number	304/1043

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

- Submission required under 37 CFR 1.114** Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

 - ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.
 - ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
 - ☐ Other _____
 - ☒ Enclosed
 - ☒ Amendment/Reply
 - ☐ Affidavit(s)/ Declaration(s)
 - ☐ Information Disclosure Statement (IDS)
 - ☐ Other _____
- Miscellaneous**

 - ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)
 - ☐ Other _____
- Fees** The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed. The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to

 - ☒ Deposit Account No. 50-1645
 - ☐ RCE fee required under 37 CFR 1.17(e)
 - ☐ Extension of time fee (37 CFR 1.136 and 1.17)
 - ☒ Other any additional fees
 - ☐ Check in the amount of \$ _____ enclosed
 - ☒ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature	<i>Lilia C. Lord</i>	Date	September 17, 2015
Name (Print/Type)	Lilia C. Lord	Registration No.	58,420

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature		Date	
Name (Print/Type)			

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 3.

May 17, 2015 BOE Ex. 1002

Case No. IPR2023-01221

Page 28 of 294

PETITION and
DEPOSIT ACCOUNT CHARGE AUTHORIZATION

This document and any concurrently filed papers are believed to be timely. Should any extension of the term be required, applicant hereby petitions the Director for such extension and requests that any applicable petition fee be charged to Deposit Account No. 50-1645.

If fee payment is enclosed, this amount is believed to be correct. However, the Director is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-1645.

Any additional fee(s) necessary to effect the proper and timely filing of the accompanying-papers may also be charged to Deposit Account No. 50-1645.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Hwan-Soo JANG

Art Unit: 2691

Serial No. 13/771,385

Examiner: John Kirkpatrick

Filed: February 20, 2013

Confirmation No. 3091

For: STAGE CIRCUIT AND ORGANIC LIGHT
EMITTING DISPLAY USING THE SAME

Attorney Docket No. 304/1043

AMENDMENT UNDER 37 C.F.R. § 1.114
-and-
REQUEST FOR CONTINUED EXAMINATION

Mail Stop: BOX RCE
Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

INTRODUCTORY COMMENTS

In response to the Office Action Made Final mailed June 17, 2015, and the Advisory Action mailed August 27, 2015, the following is respectfully submitted in connection with the above-identified application:

Amendments to the Claims are reflected in a listing of claims, which begins on page 2 of this paper.

Remarks begin on page 11 of this paper.

AMENDMENTS TO THE CLAIMS

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

Listing of Claims:

1. **(Currently Amended)** A stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal, the stage circuit comprising:

 an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and ~~[[or]]~~ a signal of the third input terminal to the output terminal ~~in accordance with voltages~~ according to a voltage applied to ~~the first node and~~ the second node;

 a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal; and

 a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, wherein

 the signal of the third input terminal directly ~~at least~~ controls an on/off operation of a transistor, the transistor included in the first driver switch.

2. **(Currently Amended)** The stage circuit as claimed in claim 1,

 wherein the first input terminal receives an output signal of a previous stage circuit or a start signal,

 wherein the second input terminal receives a first clock signal, and

 wherein the third input terminal receives a second clock signal.

3. (Original) The stage circuit as claimed in claim 2,
wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap.

4. (Original) The stage circuit as claimed in claim 3,
wherein the first clock signal and the second clock signal have a period equal to two horizontal periods $2H$ and are supplied in different horizontal periods as low signals.

5. (Original) The stage circuit as claimed in claim 2, wherein the start signal is supplied to overlap the first clock signal.

6. (Original) The stage circuit as claimed in claim 2, wherein the first driver includes:

a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and

a second transistor and a third transistor serially positioned between the second node and the first power supply,

wherein a gate electrode of the second transistor is coupled to the third input terminal,
and

wherein a gate electrode of the third transistor is coupled to the first node.

7. (Original) The stage circuit as claimed in claim 2, wherein the outputting unit includes:

a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node;

a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node;

a first capacitor between the second node and the output terminal; and

a second capacitor between the first node and the first power supply.

8. (Original) The stage circuit as claimed in claim 2, wherein the second driver includes:

a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and

a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.

9. (Withdrawn) The stage circuit as claimed in claim 2, wherein the second driver includes:

a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and

a seventh transistor between the first node and the second input terminal, the seventh transistor being diode connected.

10. (Withdrawn) The stage circuit as claimed in claim 9, wherein the seventh transistor is coupled so that a current flows from the first node to the second input terminal.

11. (Withdrawn) The stage circuit as claimed in claim 1, further comprising a bidirectional driver coupled to the first input terminal, a fifth input terminal, and the first driver.

12. (Withdrawn) The stage circuit as claimed in claim 11, wherein the bidirectional driver includes:

a tenth transistor positioned between the first input terminal and the first driver, the tenth transistor being turned on when a first control signal is supplied; and

an eleventh transistor positioned between the fifth input terminal and the first driver, the eleventh transistor being turned on when a second control signal is supplied.

13. **(Withdrawn-Currently Amended)** The stage circuit as claimed in claim 12, wherein the first input terminal receives an output signal of a previous stage circuit or a start signal, and

wherein the fifth input terminal receives an output signal of a next stage circuit or a start signal.

14. **(Currently Amended)** An organic light emitting display, comprising:
pixels positioned in regions partitioned by scan lines and data lines;
a data driver for supplying data signals to the pixels through the data lines; and
a scan driver for supplying scan signals to the pixels through the scan lines, the scan

driver including ~~stages~~ stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal,

wherein each of the ~~stages~~ stage circuits includes:

an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and ~~[[or]]~~ a signal of the third input terminal to the output terminal ~~in accordance with voltages~~ according to a voltage applied to ~~the first node and~~ the second node,

a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal, and

a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, wherein

the signal of the third input terminal directly ~~at least~~ controls an on/off operation of a transistor, the transistor included in the first driver switch.

15. (Original) The organic light emitting display as claimed in claim 14, wherein a clock signal supplied to the third input terminal is used as the scan signal.

16. **(Currently Amended)** The organic light emitting display as claimed in claim 14, wherein the first input terminal receives a scan signal of a previous stage circuit or a start signal.

17. **(Currently Amended)** The organic light emitting display as claimed in claim 16,

wherein second input terminals of odd stage circuits ~~stages~~ receive a first clock signal and third input terminals of odd stage circuits ~~stages~~ receive a second clock signal, and

wherein second input terminals of even stage circuits ~~stages~~ receive the second clock signal and third input terminals of even stage circuits ~~stages~~ receive the first clock signal.

18. (Original) The organic light emitting display as claimed in claim 17, wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap.

19. (Original) The organic light emitting display as claimed in claim 17, wherein the first driver includes:

a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and

a second transistor and a third transistor serially positioned between the second node and the first power supply,

wherein a gate electrode of the second transistor is coupled to the third input terminal, and

wherein a gate electrode of the third transistor is coupled to the first node.

20. (Original) The organic light emitting display as claimed in claim 17, wherein the outputting unit includes:

a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node;

a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node;

a first capacitor between the second node and the output terminal; and

a second capacitor between the first node and the first power supply.

21. (Original) The organic light emitting display as claimed in claim 17, wherein the second driver includes:

a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and

a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.

22. (Withdrawn) The organic light emitting display as claimed in claim 17, wherein the second driver includes:

a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and

a seventh transistor between the first node and the second input terminal, the seventh transistor being diode connected.

23. (Withdrawn) The organic light emitting display as claimed in claim 22, wherein the seventh transistor is coupled so that a current flows from the first node to the second input terminal.

24. (Withdrawn) The organic light emitting display as claimed in claim 14, further comprising a bidirectional driver coupled to the first input terminal, a fifth input terminal, and the first driver.

25. (Withdrawn) The organic light emitting display as claimed in claim 24, wherein the bidirectional driver includes:

a tenth transistor between the first input terminal and the first driver, the tenth transistor being turned on when a first control signal is supplied; and

an eleventh transistor between the fifth input terminal and the first driver, the eleventh transistor being turned on when a second control signal is supplied.

26. **(Withdrawn-Currently Amended)** The organic light emitting display as claimed in claim 25,

wherein the first input terminal receives an output signal or a start signal of a previous stage circuit, and

wherein the fifth input terminal receives an output signal or a start signal of a next stage circuit.

27. **(Currently Amended)** The organic light emitting display as claimed in claim 17, wherein the scan signal of the previous stage circuit or the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal.

28. **(Currently Amended)** The stage circuit as claimed in claim 1, wherein ~~the~~
~~signal of the third input terminal is directly coupled to a gate electrode of at least one~~
~~transistor~~ the transistor controls the voltage of the second node according to the on/off
operation thereof.

REMARKS

Prior to entry of this amendment, claims 1-28 were pending in the subject application of which claims 9-13 and 22-26 were withdrawn from consideration. Claims 1 and 14 are independent. Claims 1, 2, 13, 14, 16, 17, and 26-28 are amended. No new matter is added.

A. Introduction

In the outstanding Office Action Made Final,

1. claim 14 was objected to as requiring correction of language informalities;
2. claims 1-3, 5, 7, 8, 14-18, 20, 21, 27, and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Publication No. 2008/0062097 to Jeong et al. ("the Jeong reference") in view of U.S. Patent Publication No. 2011/0115835 to Lee ("the Lee reference");
3. claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over the Jeong reference in view of the Lee reference, and further in view of U.S. Patent Publication No. 2011/0227884 to Chung ("the Chung reference"); and
4. claims 6 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Jeong reference in view of the Lee reference, and further in view of U.S. Patent Publication No. 2012/0062525 to Kim ("the Kim reference").

B. Objection to Claim 14

In the outstanding Office Action Made Final, claim 14 was objected to as requiring correction of language informalities. Claim 14 has been amended to correct the language informalities thereof. Therefore, it is respectfully requested that this objection be withdrawn.

C. Asserted Obviousness Rejection of Claims 1-3, 5, 7, 8, 14-18, 20, 21, 27, and 28

In the outstanding Office Action Made Final, claims 1-3, 5, 7, 8, 14-18, 20, 21, 27, and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Jeong reference in view of the Lee reference. This rejection is respectfully traversed for at least the following reasons.

In the interview (which was conducted on August 21, 2015), the Examiner asserted that

U.S. Patent No. 8,553,026 (which was *newly* found) teaches the claims. Further, the Examiner suggested additional limitations to claims 1 and 14 in order to overcome the *newly* found reference (i.e., Patent No. 8,553,026).

Without conceding the assertion of the Examiner, claim 1 has been amended to include the additional limitations as suggested by the Examiner in the interview and the Advisory Action dated August 27, 2015, i.e., recite, in part, “an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node; [...] the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.” Claim 14 has been amended in a similar manner to claim 1. Therefore, it is respectfully submitted that claims 1 and 14 are allowable over the *currently* cited references and the *newly* found reference. Further, claims 2-3, 5, 7, 8, 15-18, 20, 21, 27, and 28 are allowable at least by virtue of their dependency from claim 1 or 14. Therefore, it is respectfully requested that this rejection be reconsidered and withdrawn.

D. Asserted Obviousness Rejection of Claim 4

In the outstanding Office Action Made Final, claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over the Jeong reference in view of the Lee reference, and further in view of the Chung reference. This rejection is respectfully traversed for the reasons below.

As set forth above in Section C, claims 1 and 14 are allowable over the *currently* cited references and the *newly* found reference. Further, claim 4 is allowable at least by virtue of its dependency from claim 1. Therefore, it is respectfully requested that this rejection be reconsidered and withdrawn.

E. Asserted Obviousness Rejection of Claims 6 and 19

In the outstanding Office Action Made Final, claims 6 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Jeong reference in view of the Lee reference, and further in view of the Kim reference. This rejection is respectfully traversed for the reasons below.

As set forth above in Section C, claims 1 and 14 are allowable over the *currently* cited references and the *newly* found reference. Further, claims 6 and 19 are allowable at least by virtue of their dependency from claim 1 or 14. Therefore, it is respectfully requested that this rejection be reconsidered and withdrawn.

F. Rejoinder Requested

It is respectfully submitted that claims 1 and 14 are in condition for allowance. As the withdrawn claims recite or incorporate the limitations of respective ones of allowable claims 1 and 14, it is respectfully requested that the Election of Species Requirements be withdrawn, and claims 9-13 and 22-26 be rejoined.

G. Conclusion

The above remarks demonstrate the failings of the outstanding rejections, and are sufficient to overcome them. However, while these remarks may refer to particular claim elements, they are not intended to, nor need they, comprehensively address each and every reason for the patentability of the claimed subject matter over the applied art. Accordingly, it is respectfully submitted that the claims are allowable for reasons including, but not limited to, those set forth above, and patentability of the claims does not depend solely on the particular claim elements discussed above.

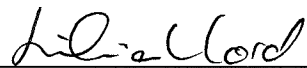
If the Examiner believes that additional discussions or information might advance the prosecution of the instant application, the Examiner is invited to contact the undersigned at the telephone number listed below to expedite resolution of any outstanding issues.

In view of the foregoing, reconsideration of this application is earnestly solicited, and an early and favorable further action upon all the claims is hereby requested.

Respectfully submitted,

LEE & MORSE, P.C.

Date: September 17, 2015



Lilia C. Lord, Registration No. 58,420
/Lilia C. Lord/

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Any additional fee(s) necessary to effect the proper and timely filing of the accompanying-papers may also be charged to Deposit Account No. 50-1645.

Electronic Patent Application Fee Transmittal

Application Number:	13771385			
Filing Date:	20-Feb-2013			
Title of Invention:	STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME			
First Named Inventor/Applicant Name:	Hwan-Soo JANG			
Filer:	Susan S. Morse/Sharon Bender			
Attorney Docket Number:	304/1043			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for Continued Examination	1801	1	1200	1200
Total in USD (\$)				1200

Electronic Acknowledgement Receipt

EFS ID:	23523272
Application Number:	13771385
International Application Number:	
Confirmation Number:	3091
Title of Invention:	STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME
First Named Inventor/Applicant Name:	Hwan-Soo JANG
Customer Number:	27849
Filer:	Susan S. Morse/Sharon Bender
Filer Authorized By:	Susan S. Morse
Attorney Docket Number:	304/1043
Receipt Date:	17-SEP-2015
Filing Date:	20-FEB-2013
Time Stamp:	14:36:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 1200
RAM confirmation Number	847
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Mianyang BOE Ex. 1002
Case No. IPR2023-01221

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		A04_2015_09_17_Amendment _RCE_As_Filed.pdf	607805 c8817f324d0586d319af682664acc899941b b2e8	yes	16
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Request for Continued Examination (RCE)		1	2	
	Amendment Submitted/Entered with Filing of CPA/RCE		3	3	
	Claims		4	12	
	Applicant Arguments/Remarks Made in an Amendment		13	16	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30666 9515ab33565c4696eb0e2c1f06d0cd04c6d 34748	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			638471		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/771,385	Filing Date 02/20/2013	☐ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO**APPLICATION AS FILED – PART I**

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	09/17/2015	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 28	Minus	** 28	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/TAMMY ACREE/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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Case No. IPR2023-01221

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/771,385	02/20/2013	Hwan-Soo JANG	304/1043	3091

27849 7590 08/27/2015
LEE & MORSE, P.C.
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FALLS CHURCH, VA 22042

EXAMINER

KIRKPATRICK, JOHN

ART UNIT	PAPER NUMBER
----------	--------------

2691

NOTIFICATION DATE	DELIVERY MODE
-------------------	---------------

08/27/2015

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

coa@lee-iplaw.com
swerbow@lee-iplaw.com

<i>Examiner-Initiated Interview Summary</i>	Application No. 13/771,385	Applicant(s) JANG, HWAN-SOO	
	Examiner JOHN KIRKPATRICK	Art Unit 2691	

All participants (applicant, applicant's representative, PTO personnel):

(1) JOHN KIRKPATRICK. (3) ____.

(2) WONSUK HWANG. (4) ____.

Date of Interview: 21 August 2015.

Type: ☒ Telephonic ☐ Video Conference
 ☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
 If Yes, brief description: ____.

Issues Discussed ☐101 ☐112 ☒102 ☐103 ☐Others
 (For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: 1.

Identification of prior art discussed: U.S. 8553026 B2.

Substance of Interview
 (For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

As a result of the additional search conducted by the Examiner, the Examiner believes that CK2 of Fig. 3 of the '026 patent discloses Applicant's amended limitation and may anticipate claim 1. The Examiner proposed amending lines 3-5 and lines 10-11 of claim 1 to recite "an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node;... the signal of the third input termina directly controls an on/off operation of a transistor included in the first dirver" in order to overcome the newly found reference.

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/JOHN KIRKPATRICK/ Examiner, Art Unit 2691	
---	--

Advisory Action Before the Filing of an Appeal Brief	Application No. 13/771,385	Applicant(s) JANG, HWAN-SOO	
	Examiner JOHN KIRKPATRICK	Art Unit 2691	AIA (First Inventor to File) Status No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 13 August 2015 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.
NO NOTICE OF APPEAL FILED

1. ☒ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance;
 (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:

a) ☐ The period for reply expires _____ months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection. The current period for reply expires _____ months from the mailing date of the prior Advisory Action or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.

Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANT'S FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because

a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);

b) ☐ They raise the issue of new matter (see NOTE below);

c) ☒ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: See continuation sheet. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): _____.

6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☒ For purposes of appeal, the proposed amendment(s): (a) ☒ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.

13. ☐ Note the attached Information *Disclosure Statement(s)*. (PTO/SB/08) Paper No(s). _____

14. ☒ Other: PTOL-2323, PTOL-413B, PTOL-892.

STATUS OF CLAIMS

15. The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____.

Claim(s) objected to: _____.

Claim(s) rejected: 1-8,14-21,27 and 28.

Claim(s) withdrawn from consideration: 9-13 and 22-26.

/JOHN KIRKPATRICK/
Examiner, Art Unit 2691

Continuation of 3: The limitations of amended independent claims 1 and 14, in particular, "the signal of the third input terminal at least controls an on/off operation of a transistor, the transistor included in the stage circuit" as recited in amended claim 1, raise new issues that require further search and/or consideration.

In response to Applicants' request for entry into AFCP 2.0, the request is acknowledged and further search and consideration has been given to Applicants' amendment as described in the attached PTO 2323 and Interview Summary.

<i>Examiner-Initiated Interview Summary</i>	Application No. 13/771,385	Applicant(s) JANG, HWAN-SOO	
	Examiner JOHN KIRKPATRICK	Art Unit 2691	

All participants (applicant, applicant's representative, PTO personnel):

(1) JOHN KIRKPATRICK. (3) ____.

(2) WONSUK HWANG. (4) ____.

Date of Interview: 21 August 2015.

Type: ☒ Telephonic ☐ Video Conference
 ☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
 If Yes, brief description: ____.

Issues Discussed ☐101 ☐112 ☒102 ☐103 ☐Others
 (For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: 1.

Identification of prior art discussed: U.S. 8553026 B2.

Substance of Interview
 (For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

As a result of the additional search conducted by the Examiner, the Examiner believes that CK2 of Fig. 3 of the '026 patent discloses Applicant's amended limitation and may anticipate claim 1. The Examiner proposed amending lines 3-5 and lines 10-11 of claim 1 to recite "an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node;... the signal of the third input termina directly controls an on/off operation of a transistor included in the first dirver" in order to overcome the newly found reference.

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/JOHN KIRKPATRICK/ Examiner, Art Unit 2691	
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Notice of References Cited	Application/Control No. 13/771,385		Applicant(s)/Patent Under Reexamination JANG, HWAN-SOO	
	Examiner JOHN KIRKPATRICK		Art Unit 2691	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-8,553,026 B2	10-2013	Park; Seong-II	G09G3/3266	345/212
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S32	1	(11/826103).APP.	USPAT; USOCR	OR	ON	2015/08/19 19:25
S33	8	("20040227718" "20050008114" "20050212746" "20060092148" "7239179").PN. OR ("7786972").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/19 19:25

EAST Search History (Interference)

<This search history is empty>

8/ 21/ 2015 4:21:25 PM
C:\ Users\ jkirkpatrick\ Documents\ EAST\ Workspaces\ 13771385.wsp

Search Notes 	Application/Control No. 13771385	Applicant(s)/Patent Under Reexamination JANG, HWAN-SOO
	Examiner JOHN KIRKPATRICK	Art Unit 2691

CPC- SEARCHED		
Symbol	Date	Examiner
G09G3/3677, 2310/0286	1/20.2015	JCK

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
EAST: Inventor Name Search	1/30/2015	JCK
EAST: (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB) see search history printout	1/28/2015-1/30/2015	JCK
EAST: Search updated - see search history printout.	6/10/2015-6/11/2015	JCK
EAST: Search updated - see search history printout.	8/1/2015	JCK

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/J.K./ Examiner.Art Unit 2691	
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Hwan-Soo JANG

Art Unit: 2691

Serial No. 13/771,385

Examiner: John Kirkpatrick

Filed: February 20, 2013

Confirmation No. 3091

For: STAGE CIRCUIT AND ORGANIC LIGHT
EMITTING DISPLAY USING THE SAME

Attorney Docket No. 304/1043

AMENDMENT UNDER 37 C.F.R. § 1.116

Mail Stop: BOX AF
Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

INTRODUCTORY COMMENTS

In response to the Office Action Made Final mailed June 17, 2015, the following is respectfully submitted in connection with the above-identified application:

Amendments to the Claims are reflected in a listing of claims, which begins on page 2 of this paper.

Remarks begin on page 11 of this paper.

AFCP 2.0 Decision

Application No.

13/771,385

Applicant(s)

JANG, HWAN-SOO

Examiner

JOHN KIRKPATRICK

Art Unit

2691

This is in response to the After Final Consideration Pilot request filed 13 August 2015.

1. **Improper Request** – The AFCP 2.0 request is improper for the following reason(s) and the after final amendment submitted with the request will be treated under pre-pilot procedure.

- ☐ An AFCP 2.0 request form PTO/SB/434 (or equivalent document) was not submitted.
- ☐ A non-broadening amendment to at least one independent claim was not submitted.
- ☐ A proper AFCP 2.0 request was submitted in response to the most recent final rejection.
- ☐ Other:

2. **Proper Request**

A. After final amendment submitted with the request will not be treated under AFCP 2.0.

The after final amendment cannot be reviewed and a search conducted within the guidelines of the pilot program.

- ☐ The after final amendment will be treated under pre-pilot procedure.

B. Updated search and/or completed additional consideration.

The examiner performed an updated search and/or completed additional consideration of the after final amendment within the time authorized for the pilot program. The result(s) of the updated search and/or completed additional consideration are:

- ☐ 1. All of the rejections in the most recent final Office action are overcome and a Notice of Allowance is issued herewith.
- ☐ 2. The after final amendment would not overcome all of the rejections in the most recent final Office action. See attached interview summary for further details.
- ☐ 3. The after final amendment was reviewed, and it raises a new issue(s). See attached interview summary for further details.
- ☒ 4. The after final amendment raises new issues, but would overcome all of the rejections in the most recent final Office action. A decision on determining allowability could not be made within the guidelines of the pilot. See attached interview summary for further details, including any newly discovered prior art.
- ☐ 5. Other:

Examiner Note: Please attach an interview summary when necessary as described above.

CERTIFICATION AND REQUEST FOR CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0		
Practitioner Docket No.: 304/1043	Application No.: 13/771,385	Filing Date: February 20, 2013
First Named Inventor: Hwan-Soo JANG	Title: STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME	
APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0 (AFCP 2.0) OF THE ACCOMPANYING RESPONSE UNDER 37 CFR 1.116. 1. The above-identified application is (i) an original utility, plant, or design nonprovisional application filed under 35 U.S.C. 111(a) [a continuing application (<i>e.g.</i>, a continuation or divisional application) is filed under 35 U.S.C. 111(a) and is eligible under (i)], or (ii) an international application that has entered the national stage in compliance with 35 U.S.C. 371(c). 2. The above-identified application contains an outstanding final rejection. 3. Submitted herewith is a response under 37 CFR 1.116 to the outstanding final rejection. The response includes an amendment to at least one independent claim, and the amendment does not broaden the scope of the independent claim in any aspect. 4. This certification and request for consideration under AFCP 2.0 is the only AFCP 2.0 certification and request filed in response to the outstanding final rejection. 5. Applicant is willing and available to participate in any interview requested by the examiner concerning the present response. 6. This certification and request is being filed electronically using the Office's electronic filing system (EFS-Web). 7. Any fees that would be necessary consistent with current practice concerning responses after final rejection under 37 CFR 1.116, <i>e.g.</i>, extension of time fees, are being concurrently filed herewith. [There is no additional fee required to request consideration under AFCP 2.0.] 8. By filing this certification and request, applicant acknowledges the following: • Reissue applications and reexamination proceedings are not eligible to participate in AFCP 2.0. • The examiner will verify that the AFCP 2.0 submission is compliant, <i>i.e.</i>, that the requirements of the program have been met (see items 1 to 7 above). For compliant submissions: ○ The examiner will review the response under 37 CFR 1.116 to determine if additional search and/or consideration (i) is necessitated by the amendment and (ii) could be completed within the time allotted under AFCP 2.0. If additional search and/or consideration is required but cannot be completed within the allotted time, the examiner will process the submission consistent with current practice concerning responses after final rejection under 37 CFR 1.116, <i>e.g.</i>, by mailing an advisory action. ○ If the examiner determines that the amendment does not necessitate additional search and/or consideration, or if the examiner determines that additional search and/or consideration is required and could be completed within the allotted time, then the examiner will consider whether the amendment places the application in condition for allowance (after completing the additional search and/or consideration, if required). If the examiner determines that the amendment does not place the application in condition for allowance, then the examiner will contact the applicant and request an interview. ▪ The interview will be conducted by the examiner, and if the examiner does not have negotiation authority, a primary examiner and/or supervisory patent examiner will also participate. ▪ If the applicant declines the interview, or if the interview cannot be scheduled within ten (10) calendar days from the date that the examiner first contacts the applicant, then the examiner will proceed consistent with current practice concerning responses after final rejection under 37 CFR 1.116.		
Signature 	Date August 13, 2015	
Name (Print/Typed) Susan S. Morse	Practitioner Registration No. 35,292	
<i>Note: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.</i>		
☒ * Total of <u>1</u> forms are submitted.		

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Hwan-Soo JANG

Art Unit: 2691

Serial No. 13/771,385

Examiner: John Kirkpatrick

Filed: February 20, 2013

Confirmation No. 3091

For: STAGE CIRCUIT AND ORGANIC LIGHT
EMITTING DISPLAY USING THE SAME

Attorney Docket No. 304/1043

AMENDMENT UNDER 37 C.F.R. § 1.116

Mail Stop: BOX AF
Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

INTRODUCTORY COMMENTS

In response to the Office Action Made Final mailed June 17, 2015, the following is respectfully submitted in connection with the above-identified application:

Amendments to the Claims are reflected in a listing of claims, which begins on page 2 of this paper.

Remarks begin on page 11 of this paper.

AMENDMENTS TO THE CLAIMS

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

Listing of Claims:

1. **(Currently Amended)** A stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal, the stage circuit comprising:

an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply or a signal of the third input terminal to the output terminal in accordance with voltages applied to the first node and the second node;

a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal; and

a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, wherein

the signal of the third input terminal at least controls an on/off operation of a **transistor,**

the transistor included in the stage circuit switch.

2. **(Currently Amended)** The stage circuit as claimed in claim 1,

wherein the first input terminal receives an output signal of a previous stage **circuit** or a start signal,

wherein the second input terminal receives a first clock signal, and

wherein the third input terminal receives a second clock signal.

3. (Original) The stage circuit as claimed in claim 2,

wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap.

4. (Original) The stage circuit as claimed in claim 3,
wherein the first clock signal and the second clock signal have a period equal to two horizontal periods $2H$ and are supplied in different horizontal periods as low signals.

5. (Original) The stage circuit as claimed in claim 2, wherein the start signal is supplied to overlap the first clock signal.

6. (Original) The stage circuit as claimed in claim 2, wherein the first driver includes:
a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and
a second transistor and a third transistor serially positioned between the second node and the first power supply,
wherein a gate electrode of the second transistor is coupled to the third input terminal,
and
wherein a gate electrode of the third transistor is coupled to the first node.

7. (Original) The stage circuit as claimed in claim 2, wherein the outputting unit includes:

a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node;

a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node;

a first capacitor between the second node and the output terminal; and

a second capacitor between the first node and the first power supply.

8. (Original) The stage circuit as claimed in claim 2, wherein the second driver includes:

a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and

a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.

9. (Withdrawn) The stage circuit as claimed in claim 2, wherein the second driver includes:

a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and

a seventh transistor between the first node and the second input terminal, the seventh transistor being diode connected.

10. (Withdrawn) The stage circuit as claimed in claim 9, wherein the seventh transistor is coupled so that a current flows from the first node to the second input terminal.

11. (Withdrawn) The stage circuit as claimed in claim 1, further comprising a bidirectional driver coupled to the first input terminal, a fifth input terminal, and the first driver.

12. (Withdrawn) The stage circuit as claimed in claim 11, wherein the bidirectional driver includes:

a tenth transistor positioned between the first input terminal and the first driver, the tenth transistor being turned on when a first control signal is supplied; and

an eleventh transistor positioned between the fifth input terminal and the first driver, the eleventh transistor being turned on when a second control signal is supplied.

13. **(Withdrawn-Currently Amended)** The stage circuit as claimed in claim 12, wherein the first input terminal receives an output signal of a previous stage circuit or a start signal, and

wherein the fifth input terminal receives an output signal of a next stage circuit or a start signal.

14. **(Currently Amended)** An organic light emitting display, comprising:
pixels positioned in regions partitioned by scan lines and data lines;
a data driver for supplying data signals to the pixels through the data lines; and
a scan driver for supplying scan signals to the pixels through the scan lines, the scan

driver including ~~stages~~ stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal,

wherein each of the ~~stages~~ stage circuits includes:

an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply or a signal of the third input terminal to the output terminal in accordance with voltages applied to the first node and the second node,

a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal, and

a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, wherein

the signal of the third input terminal at least controls an on/off operation of a transistor,
the transistor included in each of the stage circuits of the scan driver switch.

15. (Original) The organic light emitting display as claimed in claim 14, wherein a clock signal supplied to the third input terminal is used as the scan signal.

16. (Currently Amended) The organic light emitting display as claimed in claim 14, wherein the first input terminal receives a scan signal of a previous stage circuit or a start signal.

17. (Currently Amended) The organic light emitting display as claimed in claim 16, wherein second input terminals of odd stage circuits ~~stages~~ receive a first clock signal and third input terminals of odd stage circuits ~~stages~~ receive a second clock signal, and

wherein second input terminals of even stage circuits ~~stages~~ receive the second clock signal and third input terminals of even stage circuits ~~stages~~ receive the first clock signal.

18. (Original) The organic light emitting display as claimed in claim 17, wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap.

19. (Original) The organic light emitting display as claimed in claim 17, wherein the first driver includes:

a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and

a second transistor and a third transistor serially positioned between the second node and the first power supply,

wherein a gate electrode of the second transistor is coupled to the third input terminal, and

wherein a gate electrode of the third transistor is coupled to the first node.

20. (Original) The organic light emitting display as claimed in claim 17, wherein the outputting unit includes:

a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node;

a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node;

a first capacitor between the second node and the output terminal; and
a second capacitor between the first node and the first power supply.

21. (Original) The organic light emitting display as claimed in claim 17, wherein the second driver includes:

a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and

a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.

22. (Withdrawn) The organic light emitting display as claimed in claim 17, wherein the second driver includes:

a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and

a seventh transistor between the first node and the second input terminal, the seventh transistor being diode connected.

23. (Withdrawn) The organic light emitting display as claimed in claim 22, wherein the seventh transistor is coupled so that a current flows from the first node to the second input terminal.

24. (Withdrawn) The organic light emitting display as claimed in claim 14, further comprising a bidirectional driver coupled to the first input terminal, a fifth input terminal, and the first driver.

25. (Withdrawn) The organic light emitting display as claimed in claim 24, wherein the bidirectional driver includes:

a tenth transistor between the first input terminal and the first driver, the tenth transistor being turned on when a first control signal is supplied; and

an eleventh transistor between the fifth input terminal and the first driver, the eleventh transistor being turned on when a second control signal is supplied.

26. **(Withdrawn-Currently Amended)** The organic light emitting display as claimed in claim 25,

wherein the first input terminal receives an output signal or a start signal of a previous stage **circuit**, and

wherein the fifth input terminal receives an output signal or a start signal of a next stage **circuit**.

27. **(Currently Amended)** The organic light emitting display as claimed in claim 17, wherein the scan signal of the previous stage **circuit** or the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal.

28. **(Currently Amended)** The stage circuit as claimed in claim 1, wherein ~~the~~
~~signal of the third input terminal is directly coupled to a gate electrode of at least one~~
~~transistor~~ the transistor controls the voltage of the second node according to the on/off
operation thereof.

REMARKS

Prior to entry of this amendment, claims 1-28 were pending in the subject application of which claims 9-13 and 22-26 were withdrawn from consideration. Claims 1 and 14 are independent. Claims 1, 2, 13, 14, 16, 17, and 26-28 are amended. No new matter is added.

A. Introduction

In the outstanding Office Action Made Final,

1. claim 14 was objected to as requiring correction of language informalities;
2. claims 1-3, 5, 7, 8, 14-18, 20, 21, 27, and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Publication No. 2008/0062097 to Jeong et al. (“the Jeong reference”) in view of U.S. Patent Publication No. 2011/0115835 to Lee (“the Lee reference”);
3. claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over the Jeong reference in view of the Lee reference, and further in view of U.S. Patent Publication No. 2011/0227884 to Chung (“the Chung reference”); and
4. claims 6 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Jeong reference in view of the Lee reference, and further in view of U.S. Patent Publication No. 2012/0062525 to Kim (“the Kim reference”).

B. Objection to Claim 14

In the outstanding Office Action Made Final, claim 14 was objected to as requiring correction of language informalities. Claim 14 has been amended to correct the language informalities thereof. Therefore, it is respectfully requested that this objection be withdrawn.

C. Asserted Obviousness Rejection of Claims 1-3, 5, 7, 8, 14-18, 20, 21, 27, and 28

In the outstanding Office Action Made Final, claims 1-3, 5, 7, 8, 14-18, 20, 21, 27, and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Jeong reference in view of the Lee reference. This rejection is respectfully traversed for at least the following reasons.

Without conceding the correctness of the rejection, claim 14 has been amended to recite,

in part, “the signal of the third input terminal at least controls an on/off operation of a transistor, the **transistor included in each of the stage circuits of the scan driver.**” (Emphasis is added.)

Claim 1 has been amended in a similar manner to claim 14. It is respectfully submitted that the cited references fail to disclose, suggest, or render obvious the subject matter of claims 1 and 14.

Page 4 of the outstanding Office action *admits* that the Jeong reference fails to disclose a third the signal of a third input terminal to control an on/off operation of a switch, as claimed in original claim 1. However, the Office action *alleges* that the Lee reference remedies the deficiencies of the Jeong reference, because the Lee reference discloses the switching transistor M2 of the **pixel**, which is turned on by the selection signal of the selected scan line Sn, and the selection signal of the selected scan line Sn is **substantially identical** to the three clock signal CLK3 (alleged signal of the third input terminal) of the Jeong reference.

However, as noted in page 5 of the Office action, the switching transistor M2 (alleged switch/transistor) of the Lee reference is included in the **pixel**, and is **not** included in a **stage circuit of a scan driver**, which supplies a scan signal to the pixel. Thus, even if the three clock signal CLK 3 (alleged signal of the third input terminal) of the Jeong reference can be applied to the switching transistor M2 (alleged transistor) of the Lee reference, which is not conceded, the three clock signal CLK 3 of the Jeong reference *merely* controls an on/off operation of a **transistor included in a pixel, not a transistor included in a stage circuit of a scan driver.**

In contrast, claims 1 and 14 recite that a signal of a third input terminal at least controls an on/off operation of **a transistor that is included in a stage circuit (of a scan driver).**

Therefore, even assuming, *arguendo*, the cited reference could be properly combined, which is not conceded, the combination would still fail to disclose, suggest, or render obvious the subject matter of claims 1 and 14.

In addition, claim 28 has been amended to recite “the transistor controls the voltage of the second node according to the on/off operation thereof.” It is respectfully submitted that **no** portion of the cited references discloses or suggests the limitations of claim 28.

In view of the above, claims 1 and 14 are allowable over the Jeong and Lee references. Further, 2-3, 5, 7, 8, 15-18, 20, 21, 27, and 28 are allowable at least by virtue of their dependency from claim 1 or 14. Therefore, it is respectfully requested that this rejection be reconsidered and withdrawn.

D. Asserted Obviousness Rejection of Claim 4

In the outstanding Office Action Made Final, claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over the Jeong reference in view of the Lee reference, and further in view of the Chung reference. This rejection is respectfully traversed for the reasons below.

It is respectfully submitted that the Chung reference fails to remedy the deficiencies of the Jeong and Lee references set forth above in Section C. Thus, even assuming, *arguendo*, the cited reference could be properly combined, which is not conceded, the combination would still fail to disclose, suggest, or render obvious the subject matter of claim 1. Further, claim 4 is allowable at least by virtue of its dependency from claim 1. Therefore, it is respectfully requested that this rejection be reconsidered and withdrawn.

E. Asserted Obviousness Rejection of Claims 6 and 19

In the outstanding Office Action Made Final, claims 6 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Jeong reference in view of the Lee reference, and further in view of the Kim reference. This rejection is respectfully traversed for the reasons below.

It is respectfully submitted that the Kim reference fails to remedy the deficiencies of the

Jeong and Lee references set forth above in Section C. Thus, even assuming, *arguendo*, the cited reference could be properly combined, which is not conceded, the combination would still fail to disclose, suggest, or render obvious the subject matter of claims 1 and 14. Further, claims 6 and 19 are allowable at least by virtue of their dependency from claim 1 or 14. Therefore, it is respectfully requested that this rejection be reconsidered and withdrawn.

F. Rejoinder Requested

It is respectfully submitted that claims 1 and 14 are in condition for allowance. As the withdrawn claims recite or incorporate the limitations of respective ones of allowable claims 1 and 14, it is respectfully requested that the Election of Species Requirements be withdrawn, and claims 9-13 and 22-26 be rejoined.

G. Entry of Amendment Requested

Applicant respectfully submits that the pending claims are in condition for allowance, and that the instant amendments overcome the rejections set forth in the outstanding Office Action Made Final. Further, the instant amendment merely amends the claims for clarity, corrects for informalities noted by the Examiner, and requests consideration under AFCP 2.0. Accordingly, it is respectfully submitted that consideration of the instant amendment does not place an undue burden on the Examiner, and entry of the above amendment after final is respectfully requested.

H. Conclusion

The above remarks demonstrate the failings of the outstanding rejections, and are sufficient to overcome them. However, while these remarks may refer to particular claim elements, they are not intended to, nor need they, comprehensively address each and every reason for the patentability of the claimed subject matter over the applied art. Accordingly, it is respectfully submitted that the claims are allowable for reasons including, but not limited to,

those set forth above, and patentability of the claims does not depend solely on the particular claim elements discussed above.

If the Examiner believes that additional discussions or information might advance the prosecution of the instant application, the Examiner is invited to contact the undersigned at the telephone number listed below to expedite resolution of any outstanding issues.

In view of the foregoing, reconsideration of this application is earnestly solicited, and an early and favorable further action upon all the claims is hereby requested.

Respectfully submitted,

LEE & MORSE, P.C.

Date: August 13, 2015



Susan S. Morse, Registration No. 35,292
/Susan S. Morse/

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PETITION and
DEPOSIT ACCOUNT CHARGE AUTHORIZATION

This document and any concurrently filed papers are believed to be timely. Should any extension of the term be required, applicant hereby petitions the Director for such extension and requests that any applicable petition fee be charged to Deposit Account No. 50-1645.

If fee payment is enclosed, this amount is believed to be correct. However, the Director is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-1645.

Any additional fee(s) necessary to effect the proper and timely filing of the accompanying-papers may also be charged to Deposit Account No. 50-1645.

Electronic Acknowledgement Receipt

EFS ID:	23205458
Application Number:	13771385
International Application Number:	
Confirmation Number:	3091
Title of Invention:	STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME
First Named Inventor/Applicant Name:	Hwan-Soo JANG
Customer Number:	27849
Filer:	Susan S. Morse/Sharon Bender
Filer Authorized By:	Susan S. Morse
Attorney Docket Number:	304/1043
Receipt Date:	13-AUG-2015
Filing Date:	20-FEB-2013
Time Stamp:	17:24:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		A04_2015_08_13_Amendment _As_Filed.pdf	639073 4c8f36075549bf133c3c5120b2da7b53a162 2edc	yes	16

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	After Final Consideration Program Request	1	1
	Response After Final Action	2	2
	Claims	3	11
	Applicant Arguments/Remarks Made in an Amendment	12	16

Warnings:

Information:

Total Files Size (in bytes):	639073
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/771,385	Filing Date 02/20/2013	☐ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO**APPLICATION AS FILED – PART I**

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	08/13/2015	CLAIMS REMAINING AFTER AMENDMENT	Minus	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 28	Minus	** 28	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
TOTAL ADD'L FEE						0	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	Minus	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
TOTAL ADD'L FEE						

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/MARCIA GORDON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Mirnyang BOE Ex. 1002

Case No. IPR2023-01221

Page 77 of 294



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/771,385	02/20/2013	Hwan-Soo JANG	304/1043	3091

27849 7590 06/17/2015
LEE & MORSE, P.C.
3141 FAIRVIEW PARK DRIVE
SUITE 500
FALLS CHURCH, VA 22042

EXAMINER

KIRKPATRICK, JOHN

ART UNIT	PAPER NUMBER
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2691

NOTIFICATION DATE	DELIVERY MODE
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06/17/2015

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

coa@lee-iplaw.com
swerbow@lee-iplaw.com

Office Action Summary	Application No. 13/771,385	Applicant(s) JANG, HWAN-SOO	
	Examiner JOHN KIRKPATRICK	Art Unit 2691	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 5/5/2015.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-28 is/are pending in the application.
5a) Of the above claim(s) 9-13 and 22-26 is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-8, 14-21, 27, and 28 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date ____.
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date ____.
- 4) ☐ Other: ____.

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

Response to Amendment

2. Applicant's Amendment, filed May 5, 2015, has been received and entered.
3. Claims 1-28 are pending. Claims 9-13 and 22-26 remain withdrawn. Claim 28 has been added.

Claim Objections

4. Claim 14 is objected to because of the following informalities: line 5 recites "each of the stage generating a corresponding scan signal," which is grammatically incorrect. The Office suggests amending this limitation to recite --each of the stages generating a corresponding scan signal--. Appropriate correction is required.
5. Claims 15-21 and 27 each depend from claim 14 and are objected to based on the dependency of each claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-3, 5, 7, 8, 14-18, 20, 21, 27, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Jeong et al.* (U.S. Publ. 2008/0062097 A1) in view of *Lee* (U.S. Publ. 2011/0115835 A1).

As to **claim 1**, *Jeong* (Figs. 4 and 5) discloses **a stage circuit** (Fig. 4) **having a first input terminal (SSi-1 or SP), a second input terminal (CLK2), a third input terminal (CLK3), and an output terminal (SSi), the stage circuit comprising:**

an outputting unit (M1, M2, C1) having a first node (N1) and a second node (N2), the outputting unit to supply a voltage of a first power supply (VDD) or a signal of the third input terminal to the output terminal in accordance with voltages applied to the first node and the second node ([0069] discloses that when the voltage of the first node N1 drops to a low level, the first transistor M1 is turned-on to supply the voltage of the first power supply VDD to an output line of the stage ST_i; [0053] discloses that when a voltage level of the second node N2 is low, the second transistor M2 is turned-on and electrically connects an output line of the stage ST₁ to an input line of the third clock signal CLK₃);

a first driver (M4) to control the voltage of the second node (V(N2); [0048] discloses that the fourth transistor M4 is turned-on and supplies the start pulse SP or the output signal SSi-1 of a previous stage to the second node N2) **in accordance with signals of the first input terminal** (as discussed, [0048] discloses that M4 supplies the start pulse SP or the output signal SSi-1 to N2),

the second input terminal (Fig. 4 shows the level of CLK2 determines whether or not the start pulse SP or the output signal SSi-1 is supplied to N2), **and the third input terminal** (Fig. 5 shows that CLK3 is off when CLK2 causes M4 to supply SP or SSi-1 to N2; thus, voltage of N2 is controlled in accordance with CLK3); **and**

a second driver (M5, M6) to control the voltage of the first node (Figs. 4 and 5 show that M5 and M6 control the supply of VDD to N1) **in accordance with the signal of the second input terminal** (Figs. 4 and 5 show that CLK2 determines if M4 is on or off, thereby determining if SSi-1 or SP is supplied to M6 to determine if VDD is supplied to N1) **and the voltage of the second node** (Fig. 4 shows that when V(N1) is off, V(N2) is on).

Jeong does not expressly disclose “**wherein the signal of the third input terminal at least controls an on/off operation of a switch.**”

Lee (Fig. 2) discloses **wherein a scanning signal at least controls an on/off operation of a switch** ([0037] discloses that a switching transistor M2 is turned on by a selection signal applied to a selected scan line Sn).

The combination of *Jeong* and *Lee* results in the signal CLK 3 as shown in Fig. 5 of *Jeong* turning on at least the p-type transistor of the pixels 140 electrically coupled to the scan lines S1 to Sn disclosed in [0036] of *Jeong* because [0053] of *Jeong* discloses that when the second transistor M2 is turned-on, a voltage level of the output signal SSi of the stage ST1 may become substantially identical to that of the third clock signal CLK 3, and [0037] of *Lee*

discloses that a switching transistor M2 of a pixel is turned on by a selection signal applied to a selected scan line Sn. Thus, the combination of *Jeong* and *Lee* discloses “**wherein the signal of the third input terminal at least controls an on/off operation of a switch,**” as recited in claim 1.

It would have been obvious that a person of ordinary skill in the art at the time the invention was made would have known that the output of a stage of *Jeong* would have been used to turn on a switching transistor of a pixel to apply a data valued in order to cause the pixel to emit light, as disclosed in [0037] of *Lee*, because the combination is merely one of prior art elements according to known methods. In other words, *Jeong* teaches that a stage outputs a scan signal to a scan line to which pixels are coupled, and *Lee* teaches that the scan signal is used to turn on a transistor in order to apply a data voltage to the pixel. Thus, the combination of *Jeong* and *Lee* produces the predictable result of controlling a pixel to display an image using a scan signal.

As to **claim 2**, it is analyzed with regard to claim 1.

Jeong (Figs. 3, 4, and 5) discloses **wherein the first input terminal receives an output signal of a previous stage or a start signal** ([0046] discloses that the terminal SSi-1 or SP receives a start pulse SP or an output signal SSi-1 of a previous stage),

wherein the second input terminal receives a first clock signal (CLK2; Fig. 4 shows that the second input terminal receives CLK2), **and**

wherein the third input terminal receives a second clock signal

(CLK3; Fig. 4 shows that the third input terminal receives CLK3).

As to **claim 3**, it is analyzed with regard to claims 1 and 2.

Jeong (Figs. 4 and 5) discloses **wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap** (Fig. 5 shows that each of CLK2 and CLK3 have a same width and phases that do not overlap).

As to **claim 5**, it is analyzed with regard to claims 1 and 2.

Jeong (Fig. 5) discloses **wherein the start signal is supplied to overlap the first clock signal** (Fig. 5 shows that SP overlaps CLK2).

As to **claim 7**, it is analyzed with regard to claims 1 and 2.

Jeong (Figs. 4 and 5) discloses **wherein the outputting unit includes: a fourth transistor (M1) between the first power supply and the output terminal** (Fig. 4 shows that M1 is between VDD and SSi), **the fourth transistor having a gate electrode coupled to the first node** (Fig. 4 shows that the gate of M1 is coupled to N1);

a fifth transistor (M2) between the output terminal and the third input terminal (Fig. 4 shows that M2 is between SSi and CLK3), **the fifth transistor having a gate electrode coupled to the second node** (Fig. 4 shows that the gate of M2 is coupled to N2);

a first capacitor (C1) between the second node and the output terminal (Fig. 4 shows that C1 is between N2 and SSi); **and**

a second capacitor (C2) between the first node and the first power supply (Fig. 4 shows that C2 is between N1 and VDD).

As to **claim 8**, it is analyzed with regard to claims 1 and 2.

Jeong (Figs. 4 and 5) discloses **wherein the second driver includes:**

a sixth transistor (M6) between the first node and the second input terminal (Fig. 4 shows that M6 is connected between CLK2 and N1 through M4), **the sixth transistor having a gate electrode coupled to the second node** (Fig. 4 shows that the gate of M6 is connected to N2); **and**

a seventh transistor (M3) between the first node and a second power supply (Fig. 4 shows that M3 is connected between N1 and VSS), **the second power supply having a lower voltage than the first power supply** ([0054] discloses that the second power supply VSS is a low level voltage source which is less than the first power supply VDD), **the seventh transistor having a gate electrode coupled to the second input terminal** (Fig. 4 shows that the gate of M3 is coupled to CLK2 through at least C2, M1, C1, and M4).

As to **claim 14**, some of the limitations recited in this claim are similar the limitations rejected in regard to claim 1. Claim 14 differs from claim 1 in that claim 14 is directed to an organic light emitting display while claim 1 is directed to a stage circuit. Thus, the limitations of claim 14 that are similar to the limitations of claim 1 are rejected for reasons similar to those discussed in regard to claim 1.

Further, *Jeong* (Figs. 2, 3, 4, and 5) discloses **an organic light emitting display** (Fig. 2), **comprising:**

pixels (140) positioned in regions partitioned by scan lines (S1-Sn) and data lines (D1-Dm; Fig. 2 shows that the pixels 140 are separated by the scan lines and data lines);

a data driver (120) for supplying data signals to the data lines ([0034] discloses that 120 provides data signals to data lines); **and**

a scan driver (110) for supplying scan signals to the scan lines ([0041] discloses that the stages ST11 to ST1n may sequentially generate phase-delayed output signals SS1 to SSn, and may sequentially provide the generated output signals SS1 to SSn to respective scan lines), **the scan driver including stages** ([0037] discloses that Fig. 3 illustrates a block diagram of an example of a shift register included in the scan driver illustrated in Fig. 2) **coupled to the scan lines** (Fig. 3 shows that each stage is coupled to a scan line of the respective scan lines), **each of the stage generating a corresponding scan signal of the scan signals** ([0041] discloses that the stages ST11 to ST1n may sequentially generate phase-delayed output signals SS1 to SSn) **and having a first input terminal (SSi-1 or SP), a second input terminal (CLK2), a third input terminal (CLK3), and an output terminal (SSi), wherein each of the stages includes:** the features of claim 1 ([0044] discloses that Fig. 4 illustrates a detailed circuit diagram of a stage ST1).

As to **claim 15**, it is analyzed with regard to claim 14.

Jeong (Figs. 4 and 5) discloses **wherein a clock signal** (e.g. CLK3) **supplied to the third input terminal** (Fig. 4 shows that CLK3 is supplied to the terminal CLK3) **is used as the scan signal** (Fig. 5 shows that CLK3 forms SSi).

As to **claim 16**, it is analyzed with regard to claim 14.

Jeong (Figs. 3, 4, and 5) discloses **wherein the first input terminal** (SSi-1 or SP) **receives a scan signal of a previous stage** (Fig. 3 shows that the second stage receives the scan signal of the first stage) **or a start signal** (Fig. 3 shows that the first stage receives a start signal).

As to **claim 17**, it is analyzed with regard to claims 14 and 16.

Jeong (Figs. 3, 4, and 5) discloses **wherein second input terminals of odd stages receive a first clock signal** (CLK2, i.e., first clock signal, of Fig. 3; as [0045] discloses that Fig. 4 is a diagram of stage ST1, the order of terminals in Fig. 3, while not expressly shown, must be CLK2, CLK1, and CLK3; Fig. 4 shows that the terminal CLK2 receives CLK2 in the first stage; according to the pattern shown in Fig. 3 the clock assignments repeat every three stages; thus, at least another odd stage also receives CLK2 in the CLK2 terminal; therefore, odd stages receive CLK1) **and third input terminals of odd stages receive a second clock signal** (CLK3 of Fig. 3, i.e., second clock signal; Fig. 4 shows that the terminal CLK3 receives CLK3 in the first stage; according to the pattern of clocks assigned to stages as shown in Fig. 3, at least another odd stage also receives CLK3 in the CLK3 terminal; thus, the appropriate input terminals of the odd stages receive CLK2 and CLK3), **and**

wherein second input terminals of even stages receive the second clock signal (Figs. 3 and 4 shows that the second stage receives CLK3 in the CLK2 terminal; as discussed, the pattern of clocks assigned to stages discloses that another even stage is similarly configured) **and third input terminals of even stages receive the first clock signal** (Fig. 3 shows that the clock signal CLK2 is received by the terminal CLK3 in the third stage; however, the pattern of clocks assigned to stages discloses that the sixth stage receives CLK2 in the terminal CLK3 and that another even stage is similarly configured).

As to **claims 18, 20, and 21**, each claim is analyzed with regard to claims 14, 16, and 17.

Claims 18, 20, and 21 recite limitations similar to those rejected in regard to claims 3, 7, and 8, respectively. Claims 18, 20, and 21 differ from claims 3, 7, and 8 only in that these claims are directed to an organic light emitting display depending from claims 14, 16, and 17 while claims 3, 7, and 8 are directed to a stage circuit depending from claims 1 and 2. Thus, claims 18, 20, and 21 are rejected for reasons similar to those discussed in regard to claim 3, 7, and 8, respectively.

As to **claim 27**, this claim is analyzed with regard to claims 14, 16, and 17.

Jeong (Fig. 5) discloses **wherein the scan signal of the previous stage or the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal** (Fig. 5 shows that SP overlaps CLK2).

As to **claim 28**, it is analyzed with regard to claim 1.

Jeong does not expressly disclose **wherein the signal of the third input terminal is directly coupled to a gate electrode of at least one transistor**.

However, [0053] of *Jeon* discloses that “when the second transistor M2 is turned-on, a voltage level of the output signal SSi of the stage ST1 may become substantially identical to that of the third clock signal CLK3.” Specifically Fig. 4 of *Jeong* shows that the output signal SSi is CLK3. As [0037] of *Lee* discloses that a switching transistor M2 is turned on by a selection signal applied to a selected scan line Sn, the combination of *Jeong* and *Lee* discloses that CLK3 is directly coupled to the gate electrode of M2 of *Lee*. Thus, the combination of *Jeong* and *Lee* discloses “**wherein the signal of the third input terminal is directly coupled to a gate electrode of at least one transistor**,” as recited in claim 28.

It would have been obvious that a person of ordinary skill in the art at the time the invention was made would have known that the output of a stage of *Jeong* would have been used to turn on a switching transistor of a pixel to apply a data valued in order to cause the pixel to emit light, as disclosed in [0037] of *Lee* for reasons similar to those discussed in regard to claim 1.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Jeong* in view of *Lee* in further view of *Chung* (U.S. Publ. 2011/0227884 A1).

As to **claim 4**, it is analyzed with regard to claims 1, 2, and 3.

Jeong does not expressly disclose **wherein the first clock signal and the second clock signal have a period equal to two horizontal periods 2H and are supplied in different horizontal periods as low signals.**

Chung (Fig. 5) discloses **wherein the first clock signal and the second clock signal have a period equal to two horizontal periods 2H** (Fig. 5 shows that CLK2 and CLK3 have a period of 2H; [0036] discloses that 2H is equivalent to two horizontal cycles) **and are supplied in different horizontal periods as low signals** (Fig. 5 shows that CLK2 and CLK3 are low in different horizontal periods).

It would have been obvious that a person of ordinary skill in the art at the time the invention was made would have been motivated to modify the periods of the clock signals disclosed in *Jeong*, as modified by *Lee*, to be equivalent to two horizontal periods as disclosed in *Chung* because [0008] of *Chung* discloses that when the organic light emitting panel having a resolution of full high definition is driven at 120 Hz or higher, in order to prevent the generation of an abnormal scan signal due to the shortened scan time, the organic light emitting panel may be driven by increasing the pulse width of the scan signal.

9. Claims 6 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Jeong* in view of *Lee* in further view of *Kim* (U.S. Publ. 2012/0062525 A1).

As to **claim 6**, it is analyzed with regard to claims 1 and 2.

Jeong (Fig. 4) discloses **wherein the first driver includes:**

a first transistor (M4) between the first input terminal and the second node (Fig. 4 shows that M4 is between SSi-1 or SP and N2), **the first transistor having a gate electrode coupled to the second input terminal** (Fig. 4 shows that the gate of M4 is coupled to CLK2).

Jeong does not expressly disclose:

a second transistor and a third transistor serially positioned between the second node and the first power supply,

wherein a gate electrode of the second transistor is coupled to the third input terminal, and

wherein a gate electrode of the third transistor is coupled to the first node.

Kim (Fig. 3) discloses:

a second transistor (M3) and a third transistor (M4) serially positioned between the second node and the first power supply (Fig. 3 shows that M3 and M4 are positioned in series between the node N2 and the power supply VGH),

wherein a gate electrode of the third transistor is coupled to the first node (Fig. 3 shows that the gate electrode of M4 is coupled to N1).

The combination of *Jeong*, *Lee*, and *Kim* results in the transistor M1 of *Jeong*, as modified by *Lee*, being substituted with the transistors M3 and M4 of *Kim* because Fig. 3 of *Kim* shows that two transistors connected in series may be used to drive an output, such as SSi of *Jeong*, as modified by *Lee*. Thus, when

the transistor M1 of *Jeong*, as modified by *Lee*, is substituted with the transistors M3 and M4 of *Kim* to output SSi, a gate of M3 is coupled to CLK3 at least through C2 of *Jeong*, M3 and M4 of *Jeong*, as modified by *Kim*, and M2 of *Jeong*. Therefore, the combination of *Jeong*, *Lee*, and *Kim* discloses “**wherein a gate electrode of the second transistor is coupled to the third input terminal,**” as recited in claim 6.

It would have been obvious that a person of ordinary skill in the art at the time the invention was made would know that the transistor M1 of *Jeong*, as modified by *Lee*, could have been substituted with the transistors M3 and M4 of *Kim* because Fig. 3 of *Kim* suggests that the substitution would not have changed function of M1 of *Jeong*, as modified by *Lee*, because both gates of M3 and M4 of *Kim* are connected to the same input. Thus, the combination of *Jeong*, *Lee*, and *Kim* is a simple substitution of one known element for another that produces a predictable result.

As to **claim 19** this claim is analyzed with regard to claims 14, 16, and 17.

Claim 19 recites limitations similar to those rejected in regard to claim 6. Claim 19 differs from claim 6 only in that this claim is directed to an organic light emitting display depending from claims 14, 16, and 17 while claim 6 is directed to a stage circuit depending from claims 1 and 2. Thus, claim 19 is rejected for reasons similar to those discussed in regard to claim 6.

Response to Arguments

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10. Applicant's arguments with respect to amended independent claim 1 have been considered but are moot because the arguments do not apply to any of the references being used in the current rejection. Notably, the Office respectfully submits that claim 1 merely requires the third input terminal to at least control the operation of a switch and does not expressly disclose the relationship of the switch to the stage circuit. Thus, the combination of *Jeong* and *Lee* satisfies the amended limitation for reasons similar to those discussed in regard to claim 1.

11. Applicant's request for rejoinder of the withdrawn claims is acknowledged, but denied because there are presently no allowable generic claims.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN C. KIRKPATRICK whose telephone number is (571) 270-3343. The examiner can normally be reached on 9:00 am - 5:30 pm

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh D. Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JOHN C KIRKPATRICK/
Examiner, Art Unit 2691

Notice of References Cited	Application/Control No. 13/771,385	Applicant(s)/Patent Under Reexamination JANG, HWAN-SOO	
	Examiner JOHN KIRKPATRICK	Art Unit 2691	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2011/0115835 A1	05-2011	LEE, Wook	345/691
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes 	Application/Control No. 13771385	Applicant(s)/Patent Under Reexamination JANG, HWAN-SOO
	Examiner JOHN KIRKPATRICK	Art Unit 2691

CPC- SEARCHED		
Symbol	Date	Examiner
G09G3/3677, 2310/0286	1/20.2015	JCK

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
EAST: Inventor Name Search	1/30/2015	JCK
EAST: (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB) see search history printout	1/28/2015-1/30/2015	JCK
EAST: Search updated - see search history printout.	6/10/2015-6/11/2015	JCK

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/J.K./ Examiner.Art Unit 2691	
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S22	8	G09G3/3225.cpc. and @pd<"20120220" and (pixel same (writ\$4 adj1 transistor) same ((scan\$4 gate) adj1 signal))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/06/10 22:48
S23	1	G09G3/3225.cpc. and @pd<"20120220" and p-type and ((writ\$4 adj1 transistor) same ((scan\$4 gate) adj1 signal))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/06/10 23:18
S26	0	S24 and @pd<"20120220" and oled and ((writ\$4 adj1 transistor) same ((scan\$4 gate) adj1 signal))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/06/10 23:24
S25	0	S24 and @pd<"20120220" and (pixel same (writ\$4 adj1 transistor) same ((scan\$4 gate) adj1 signal))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/06/10 23:24
S24	491099	samsung.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/06/10 23:24
S28	20	S24 and @pd<"20120220" and oled and (pixel same (writ\$4) same ((scan\$4 gate) adj1 signal))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/06/10 23:25
S27	29	S24 and @pd<"20120220" and oled and ((writ\$4) same ((scan\$4 gate) adj1 signal))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/06/10 23:25
L6	70	L5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/06/11 14:43
L5	70	L4 and OLED and \$1VDD	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/06/11 14:43
L4	3543	377/64-81.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/06/11 14:43

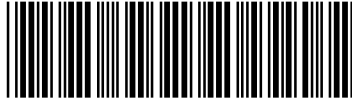
Mianyang BOE Ex. 1002
Case No. IPR2023-01221

EAST Search History (Interference)

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<i>Index of Claims</i> 	Application/Control No. 13771385	Applicant(s)/Patent Under Reexamination JANG, HWAN-SOO
	Examiner JOHN KIRKPATRICK	Art Unit 2691

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA				☐ T.D.				☐ R.1.47			
CLAIM		DATE													
Final	Original	01/30/2015	06/11/2015												
	1	✓	✓												
	2	✓	✓												
	3	✓	✓												
	4	✓	✓												
	5	✓	✓												
	6	✓	✓												
	7	✓	✓												
	8	✓	✓												
	9	N	N												
	10	N	N												
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	12	N	N												
	13	N	N												
	14	✓	✓												
	15	✓	✓												
	16	✓	✓												
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	22	N	N												
	23	N	N												
	24	N	N												
	25	N	N												
	26	N	N												
	27	✓	✓												
	28		✓												

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Hwan-Soo JANG

Art Unit: 2691

Serial No. 13/771,385

Examiner: John Kirkpatrick

Filed: February 20, 2013

Confirmation No. 3091

For: STAGE CIRCUIT AND ORGANIC LIGHT
EMITTING DISPLAY USING THE SAME

Attorney Docket No. 304/1043

AMENDMENT UNDER 37 C.F.R. § 1.111

Mail Stop: Amendment
Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

INTRODUCTORY COMMENTS

In response to the Office action mailed February 9, 2015, the following is respectfully submitted in connection with the above-identified application:

Amendments to the Claims are reflected in a listing of claims, which begins on page 2 of this paper.

Remarks begin on page 10 of this paper.

AMENDMENTS TO THE CLAIMS

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

Listing of Claims:

1. (Currently Amended) A stage circuit **having a first input terminal, a second input terminal, a third input terminal, and an output terminal, the stage circuit** comprising:
an outputting unit having a first node and a second node, the outputting unit **being configured** to supply a voltage of a first power supply or a signal of **a the** third input terminal to **an the** output terminal in accordance with voltages applied to the first node and the second node;
a first driver **configured** to control the voltage of the second node in accordance with signals of **a the** first input terminal, **a the** second input terminal, and the third input terminal; and
a second driver **configured** to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, **wherein**
the signal of the third input terminal at least controls an on/off operation of a switch.

2. (Original) The stage circuit as claimed in claim 1,
wherein the first input terminal receives an output signal of a previous stage or a start signal,
wherein the second input terminal receives a first clock signal, and
wherein the third input terminal receives a second clock signal.

3. (Original) The stage circuit as claimed in claim 2,

wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap.

4. (Original) The stage circuit as claimed in claim 3, wherein the first clock signal and the second clock signal have a period equal to two horizontal periods $2H$ and are supplied in different horizontal periods as low signals.

5. (Original) The stage circuit as claimed in claim 2, wherein the start signal is supplied to overlap the first clock signal.

6. (Original) The stage circuit as claimed in claim 2, wherein the first driver includes:

a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and

a second transistor and a third transistor serially positioned between the second node and the first power supply,

wherein a gate electrode of the second transistor is coupled to the third input terminal, and

wherein a gate electrode of the third transistor is coupled to the first node.

7. (Original) The stage circuit as claimed in claim 2, wherein the outputting unit includes:

a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node;

a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node;

a first capacitor between the second node and the output terminal; and

a second capacitor between the first node and the first power supply.

8. (Original) The stage circuit as claimed in claim 2, wherein the second driver includes:

a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and

a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.

9. (Withdrawn) The stage circuit as claimed in claim 2, wherein the second driver includes:

a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and

a seventh transistor between the first node and the second input terminal, the seventh transistor being diode connected.

10. (Withdrawn) The stage circuit as claimed in claim 9, wherein the seventh transistor is coupled so that a current flows from the first node to the second input terminal.

11. (Withdrawn) The stage circuit as claimed in claim 1, further comprising a bidirectional driver coupled to the first input terminal, a fifth input terminal, and the first driver.

12. (Withdrawn) The stage circuit as claimed in claim 11, wherein the bidirectional driver includes:

a tenth transistor positioned between the first input terminal and the first driver, the tenth transistor being turned on when a first control signal is supplied; and

an eleventh transistor positioned between the fifth input terminal and the first driver, the eleventh transistor being turned on when a second control signal is supplied.

13. (Withdrawn) The stage circuit as claimed in claim 12,
wherein the first input terminal receives an output signal of a previous stage or a start signal, and
wherein the fifth input terminal receives an output signal of a next stage or a start signal.

14. **(Currently Amended)** An organic light emitting display, comprising:
pixels positioned in regions partitioned by scan lines and data lines;
a data driver for supplying data signals to the data lines; and
a scan driver for supplying scan signals to the scan lines, the scan driver including stages coupled to the scan lines, each of the stage generating a corresponding scan signal of

the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal in order to supply scan signals to the scan lines,

wherein each of the stages includes:

an outputting unit having a first node and a second node, the outputting unit **being configured** to supply a voltage of a first power supply or a signal of **a the** third input terminal to **an the** output terminal in accordance with voltages applied to the first node and the second node,

a first driver **configured** to control the voltage of the second node in accordance with signals of **a the** first input terminal, **a the** second input terminal, and the third input terminal, and

a second driver **configured** to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, **wherein**

the signal of the third input terminal at least controls an on/off operation of a switch.

15. (Original) The organic light emitting display as claimed in claim 14, wherein a clock signal supplied to the third input terminal is used as the scan signal.

16. (Original) The organic light emitting display as claimed in claim 14, wherein the first input terminal receives a scan signal of a previous stage or a start signal.

17. (Original) The organic light emitting display as claimed in claim 16, wherein second input terminals of odd stages receive a first clock signal and third input terminals of odd stages receive a second clock signal, and

wherein second input terminals of even stages receive the second clock signal and third input terminals of even stages receive the first clock signal.

18. (Original) The organic light emitting display as claimed in claim 17, wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap.

19. (Original) The organic light emitting display as claimed in claim 17, wherein the first driver includes:

a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and

a second transistor and a third transistor serially positioned between the second node and the first power supply,

wherein a gate electrode of the second transistor is coupled to the third input terminal, and

wherein a gate electrode of the third transistor is coupled to the first node.

20. (Original) The organic light emitting display as claimed in claim 17, wherein the outputting unit includes:

a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node;

a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node;

a first capacitor between the second node and the output terminal; and
a second capacitor between the first node and the first power supply.

21. (Original) The organic light emitting display as claimed in claim 17, wherein the second driver includes:

a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and

a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.

22. (Withdrawn) The organic light emitting display as claimed in claim 17, wherein the second driver includes:

a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and

a seventh transistor between the first node and the second input terminal, the seventh transistor being diode connected.

23. (Withdrawn) The organic light emitting display as claimed in claim 22, wherein the seventh transistor is coupled so that a current flows from the first node to the second input terminal.

24. (Withdrawn) The organic light emitting display as claimed in claim 14, further comprising a bidirectional driver coupled to the first input terminal, a fifth input terminal, and the first driver.

25. (Withdrawn) The organic light emitting display as claimed in claim 24, wherein the bidirectional driver includes:

a tenth transistor between the first input terminal and the first driver, the tenth transistor being turned on when a first control signal is supplied; and

an eleventh transistor between the fifth input terminal and the first driver, the eleventh transistor being turned on when a second control signal is supplied.

26. (Withdrawn) The organic light emitting display as claimed in claim 25, wherein the first input terminal receives an output signal or a start signal of a previous stage, and

wherein the fifth input terminal receives an output signal or a start signal of a next stage.

27. (Original) The organic light emitting display as claimed in claim 17, wherein the scan signal of the previous stage or the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal.

28. (New) The stage circuit as claimed in claim 1, wherein the signal of the third input terminal is directly coupled to a gate electrode of at least one transistor.

REMARKS

Prior to entry of this amendment, claims 1-27 were pending in the subject application of which claims 9-13 and 22-26 were withdrawn from consideration. Claims 1 and 14 are independent. Claims 1 and 14 are amended. New dependent claim 28 is added. Support for this amendment may be found in, for example, FIGs. 2-3 and paragraphs [0066] and [0073] of the application as published. No new matter is added.

The Examiner's acknowledgement of the claim for foreign priority and receipt of a certified copy of the priority document is noted with appreciation.

The Examiner's acceptance of the drawings filed February 20, 2013, is noted with appreciation.

The Examiner's consideration of the Information Disclosure Statements filed February 20, 2013 and December 19, 2014, is noted with appreciation.

A. Introduction

In the outstanding Office action,

1. claims 1-3, 5, 7, 8, 14-18, 20, 21, and 27 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Publication No. 2008/0062097 to Jeong et al. ("the Jeong reference");
2. claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over the Jeong reference in view of U.S. Patent Publication No. 2011/0227884 to Chung ("the Chung reference"); and
3. claims 6 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Jeong reference in view of U.S. Patent Publication No. 2012/0062525 to Kim ("the Kim reference").

B. Asserted Anticipation Rejection of Claims 1-3, 5, 7, 8, 14-18, 20, 21, and 27

In the outstanding Office action, claims 1-3, 5, 7, 8, 14-18, 20, 21, and 27 were rejected under 35 U.S.C. § 102(b) as being anticipated by the Jeong reference. This rejection is respectfully traversed for at least the following reasons.

Claim 1 has been amended to recite, in part, “an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply or a signal of the third input terminal to the output terminal in accordance with voltages applied to the first node and the second node; a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal [...] wherein the signal of the third input terminal at least **controls an on/off operation of a switch.**” (Emphasis is added.) It respectfully submitted that the Jeong reference fails to anticipate at least a first driver to control a voltage of a second node of an outputting unit in accordance with signals of first, second, and third input terminals, wherein the signal of the third input terminal at least controls an on/off operation of a switch.

Page 3 of the outstanding Office action *alleges* that the fourth transistor M4 of the Jeong reference corresponds to the claimed first driver, because the fourth transistor M4 controls the voltage of the second node N2 in accordance with the low level output signal SSi-1 or the start pulse SP (alleged as the signal of the first input terminal of claim 1), the second low level clock signal CLK2 (alleged as the signal of the second input terminal of claim 1), and the third high level clock signal CLK3 (alleged as the signal of the third input terminal of claim 1). In particular, the Office action *alleges* that the fourth transistor M4 of the Jeong reference controls the voltage of the second node N2 according to the third high level clock signal CLK3 (alleged signal of the third input terminal), because the third high level clock signal CLK3 is off when the second low level clock signal CLK2 causes the fourth transistor M4 to supply the low level output signal SSi-1 or the start pulse SP to the second node N2.

However, FIG. 4 (shown below) and paragraph [0066] of the Jeong reference *explicitly* discloses that the third high level clock signal CLK3 (alleged signal of the third input terminal) is

The circuit diagram shows a PMOS network consisting of transistors M1 and M2 in series, connected to VDD. The NMOS network consists of transistors M3, M4, M5, and M6. Transistor M3 is connected to VSS. Transistors M4, M5, and M6 are connected in parallel. A feedback loop is formed by a capacitor C1 connected between node N2 and node N3. Node N2 is connected to the gates of M2 and M3. Node N3 is the output SSi. A second clock input CLK2 is connected to the gates of M5 and M6. A signal SSi-1 or SP is connected to the gates of M4 and M5. A capacitor C2 is connected between VDD and node N1, which is the node between M1 and M2. A signal STi is connected to the gates of M1 and M2. A signal CLK1 is connected to the gate of M3. A signal CLK3 is connected to the gates of M2 and M3. A dashed box 410 encloses transistors M4, M5, and M6.

In contrast, claim 1 now recites that a first driver to control a voltage of a second node of an outputting unit in accordance with signals of first, second, and third input terminals, wherein **the signal of the third input terminal at least controls an on/off operation of a switch**. Thus, it is respectfully submitted that the third high level clock signal CLK3 **cannot** be interpreted as a signal of a third input terminal controlling an on/off operation of a switch as recited in claim 1. Therefore, it is respectfully submitted that the Jeong reference does **not** anticipate a first driver to control a voltage of a second node of an outputting unit in accordance with signals of first, second, and third input terminals, wherein the signal of the third input terminal controls an on/off operation of a switch, as claimed in claim 1.

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Case No. IPR2023-01221
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anticipate each and every element of claim 1. Claim 14 is not anticipated by the Jeong reference because claim 14 recites subject matter similar to claim 1. Further, claims 2-3, 5, 7, 8, 15-18, 20, 21, and 27 are not anticipated by the Jeong reference at least by virtue of their dependency from claim 1 or 14. Therefore, it is respectfully requested that this rejection be reconsidered and withdrawn.

C. Asserted Obviousness Rejection of Claim 4

In the outstanding Office action, claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over the Jeong reference in view of the Chung reference. This rejection is respectfully traversed for the reasons below.

It is respectfully submitted that the Chung reference fails to remedy the deficiencies of the Jeong reference set forth above in Section B. Thus, even assuming, *arguendo*, the cited reference could be properly combined, which is not conceded, the combination would still fail to disclose, suggest, or render obvious the subject matter of claim 1. Further, claim 4 is allowable at least by virtue of its dependency from claim 1. Therefore, it is respectfully requested that this rejection be reconsidered and withdrawn.

D. Asserted Obviousness Rejection of Claims 6 and 19

In the outstanding Office action, claims 6 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Jeong reference in view of the Kim reference. This rejection is respectfully traversed for the reasons below.

It is respectfully submitted that the Kim reference fails to remedy the deficiencies of the Jeong reference set forth above in Section B. Thus, even assuming, *arguendo*, the cited reference could be properly combined, which is not conceded, the combination would still fail to disclose, suggest, or render obvious the subject matter of claims 1 and 14. Further, claims 6 and 19 are

allowable at least by virtue of their dependency from claim 1 or 14. Therefore, it is respectfully requested that this rejection be reconsidered and withdrawn.

E. Rejoinder Requested

It is respectfully submitted that claims 1 and 14 are in condition for allowance. As the withdrawn claims recite or incorporate the limitations of respective ones of allowable claims 1 and 14, it is respectfully requested that the Election of Species Requirements be withdrawn, and claims 9-13 and 22-26 be rejoined.

F. Conclusion

The above remarks demonstrate the failings of the outstanding rejections, and are sufficient to overcome them. However, while these remarks may refer to particular claim elements, they are not intended to, nor need they, comprehensively address each and every reason for the patentability of the claimed subject matter over the applied art. Accordingly, it is respectfully submitted that the claims are allowable for reasons including, but not limited to, those set forth above, and patentability of the claims does not depend solely on the particular claim elements discussed above.

The remaining documents cited in the Office action were not relied on to reject the claims. Therefore, no comments concerning these documents are considered necessary at this time.

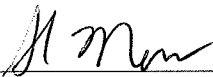
If the Examiner believes that additional discussions or information might advance the prosecution of the instant application, the Examiner is invited to contact the undersigned at the telephone number listed below to expedite resolution of any outstanding issues.

In view of the foregoing, reconsideration of this application is earnestly solicited, and an early and favorable further action upon all the claims is hereby requested.

Respectfully submitted,

LEE & MORSE, P.C.

Date: May 5, 2015



Susan S. Morse, Registration No. 35,292
/Susan S. Morse/

LEE & MORSE, P.C.
3141 FAIRVIEW PARK DRIVE, SUITE 500
FALLS CHURCH, VA 22042
703.207.0008 TEL
703.207.0003 FAX

PETITION and
DEPOSIT ACCOUNT CHARGE AUTHORIZATION

This document and any concurrently filed papers are believed to be timely. Should any extension of the term be required, applicant hereby petitions the Director for such extension and requests that any applicable petition fee be charged to Deposit Account No. 50-1645.

If fee payment is enclosed, this amount is believed to be correct. However, the Director is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-1645.

Any additional fee(s) necessary to effect the proper and timely filing of the accompanying-papers may also be charged to Deposit Account No. 50-1645.

Electronic Patent Application Fee Transmittal

Application Number:	13771385			
Filing Date:	20-Feb-2013			
Title of Invention:	STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME			
First Named Inventor/Applicant Name:	Hwan-Soo JANG			
Filer:	Susan S. Morse/Sharon Bender			
Attorney Docket Number:	304/1043			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Claims in Excess of 20	1202	1	80	80
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				80

Electronic Acknowledgement Receipt

EFS ID:	22258292
Application Number:	13771385
International Application Number:	
Confirmation Number:	3091
Title of Invention:	STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME
First Named Inventor/Applicant Name:	Hwan-Soo JANG
Customer Number:	27849
Filer:	Susan S. Morse/Sharon Bender
Filer Authorized By:	Susan S. Morse
Attorney Docket Number:	304/1043
Receipt Date:	05-MAY-2015
Filing Date:	20-FEB-2013
Time Stamp:	14:30:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$80
RAM confirmation Number	731
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Mianyang BOE Ex. 1002
Case No. IPR2023-01221

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		A02_2015_05_05_Amendment _As_Filed.pdf	630492 9619f20cb5791b6213980ae32ee9267dc764d609	yes	16
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Fee Worksheet (SB06)		1	1	
	Amendment/Req. Reconsideration-After Non-Final Reject		2	2	
	Claims		3	10	
	Applicant Arguments/Remarks Made in an Amendment		11	16	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30706 b43c13e5eb24fadfe1e62cb864be52192696e822	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			661198		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

FEE TRANSMITTAL		Complete if known	
		Application Number	13/771,385
		Filing Date	February 20, 2013
☐ Applicant asserts small entity status. See 37 CFR 1.27.		First Named Inventor	Hwan-Soo JANG
☐ Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.		Examiner Name	John Kirkpatrick
		Art Unit	2691
TOTAL AMOUNT OF PAYMENT	(\$ 80.00	Practitioner Docket No.	304/1043

METHOD OF PAYMENT (check all that apply)
☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 50-1645 Deposit Account Name: Lee & Morse, P.C.

For the above-identified deposit account, the Director is hereby authorized to (check all that apply):

☐ Charge fee(s) indicated below☐ Charge fee(s) indicated below, **except for the filing fee**
☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17
☒ Credit any overpayment of fee(s)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION**1. BASIC FILING, SEARCH, AND EXAMINATION FEES** (U = undiscounted fee; S = small entity fee; M = micro entity fee)

Application Type	FILING FEES			SEARCH FEES			EXAMINATION FEES			Fees Paid (\$)
	U (\$)	S (\$)	M (\$)	U (\$)	S (\$)	M (\$)	U (\$)	S (\$)	M (\$)	
Utility	280	140*	70	600	300	150	720	360	180	
Design	180	90	45	120	60	30	460	230	115	
Plant	180	90	45	380	190	95	580	290	145	
Reissue	280	140	70	600	300	150	2,160	1,080	540	
Provisional	260	130	65	0	0	0	0	0	0	

* The \$140 small entity status filing fee for a utility application is further reduced to \$70 for a small entity status applicant who files the application via EFS-Web.

2. EXCESS CLAIM FEES

Fee Description	Undiscounted Fee (\$)	Small Entity Fee (\$)	Micro Entity Fee (\$)
Each claim over 20 (including Reissues)	80	40	20
Each independent claim over 3 (including Reissues)	420	210	105
Multiple dependent claims	780	390	195
Total Claims			
28 - 20 or HP = 1 x	80.00		
HP = highest number of total claims paid for, if greater than 20.			
Indep. Claims			
- 3 or HP = 1 x			
HP = highest number of independent claims paid for, if greater than 3.			

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$400 (\$200 for small entity) (\$100 for micro entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

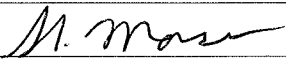
Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fees Paid (\$)
- 100 =	/ 50 =	(round up to a whole number) x	=	

4. OTHER FEE(S)

Non-English specification, \$130 fee (no small or micro entity discount)

Non-electronic filing fee under 37 CFR 1.16(t) for a utility application, \$400 fee (\$200 small or micro entity)

Other (e.g., late filing surcharge):

SUBMITTED BY			
Signature		Registration No. (Attorney/Agent) 35,292	Telephone 703.207.0008
Name (Print/Type)	Susan S. Morse		Date May 5, 2015

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 3.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/771,385	Filing Date 02/20/2013	☐ To be Mailed
---	---	----------------------------------	---------------------------------------

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO**APPLICATION AS FILED – PART I**

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	05/05/2015	CLAIMS REMAINING AFTER AMENDMENT	Minus	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 28	Minus	** 27	= 1	X \$80 =	80
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	80

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	Minus	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
						TOTAL ADD'L FEE

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/EFREM WARREN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Mirnyang BOE Ex. 1002

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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/771,385	02/20/2013	Hwan-Soo JANG	304/1043	3091

27849 7590 02/09/2015
LEE & MORSE, P.C.
3141 FAIRVIEW PARK DRIVE
SUITE 500
FALLS CHURCH, VA 22042

EXAMINER

KIRKPATRICK, JOHN

ART UNIT	PAPER NUMBER
----------	--------------

2691

NOTIFICATION DATE	DELIVERY MODE
-------------------	---------------

02/09/2015

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

coa@lee-iplaw.com
swerbow@lee-iplaw.com

Office Action Summary	Application No. 13/771,385	Applicant(s) JANG, HWAN-SOO	
	Examiner JOHN KIRKPATRICK	Art Unit 2691	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12/19/2014.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-27 is/are pending in the application.
5a) Of the above claim(s) 9-13 and 22-26 is/are withdrawn from consideration.
- 6) ☐ Claim(s) _____ is/are allowed.
- 7) ☒ Claim(s) 1-8, 14-21 and 27 is/are rejected.
- 8) ☐ Claim(s) _____ is/are objected to.
- 9) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 2/20/2013 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☒ All b) ☐ Some** c) ☐ None of the:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date _____.
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 4) ☐ Other: _____.

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

Election/Restrictions

2. Applicant's election of Species A, as shown in Fig. 2, in the reply filed on December 19, 2014 is acknowledged. Claims 9-13 and 22-26 are withdrawn and claims 1-8, 14-21, and 27 are examined on the merits. Because Applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 5, 7, 8, 14-18, 20, 21, and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by *Jeong et al.* (U.S. Publ. 2008/0062097 A1).

As to **claim 1**, *Jeong* (Figs. 4 and 5) discloses **a stage circuit** (Fig. 4),
comprising:
an outputting unit (M1, M2, C1) having a first node (N1) and a second node (N2), the outputting unit being configured to supply a voltage of a first

power supply (VDD) or a signal of a third input terminal (CLK3) to an output terminal (SSi) in accordance with voltages applied to the first node and the second node ([0069] discloses that when the voltage of the first node N1 drops to a low level, the first transistor M1 is turned-on to supply the voltage of the first power supply VDD to an output line of the stage STi; [0053] discloses that when a voltage level of the second node N2 is low, the second transistor M2 is turned-on and electrically connects an output line of the stage ST1 to an input line of the third clock signal CLK3);

a first driver (M4) configured to control the voltage of the second node (V(N2); [0048] discloses that the fourth transistor M4 is turned-on and supplies the start pulse SP or the output signal SSi-1 of a previous stage to the second node N2) **in accordance with signals of a first input terminal (SSi-1 or SP; as discussed, [0048] discloses that M4 supplies the start pulse SP or the output signal SSi-1 to N2), a second input terminal (CLK2; Fig. 4 shows the level of CLK2 determines whether or not the start pulse SP or the output signal SSi-1 is supplied to N2), and the third input terminal (CLK3; Fig. 5 shows that CLK3 is off when CLK2 causes M4 to supply SP or SSi-1 to N2; thus, voltage of N2 is controlled in accordance with CLK3); and**

a second driver (M5, M6) configured to control the voltage of the first node (Figs. 4 and 5 show that M5 and M6 control the supply of VDD to N1) **in accordance with the signal of the second input terminal** (Figs. 4 and 5 show that CLK2 determines if M4 is on or off, thereby determining if SSi-1 or SP is

supplied to M6 to determine if VDD is supplied to N1) **and the voltage of the second node** (Fig. 4 shows that when V(N1) is off, V(N2) is on).

As to **claim 2**, it is analyzed with regard to claim 1.

Jeong (Figs. 3, 4, and 5) discloses **wherein the first input terminal receives an output signal of a previous stage or a start signal** ([0046] discloses that the terminal SSi-1 or SP receives a start pulse SP or an output signal SSi-1 of a previous stage),

wherein the second input terminal receives a first clock signal (CLK2; Fig. 4 shows that the second input terminal receives CLK2), **and**

wherein the third input terminal receives a second clock signal (CLK3; Fig. 4 shows that the third input terminal receives CLK3).

As to **claim 3**, it is analyzed with regard to claims 1 and 2.

Jeong (Figs. 4 and 5) discloses **wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap** (Fig. 5 shows that each of CLK2 and CLK3 have a same width and phases that do not overlap).

As to **claim 5**, it is analyzed with regard to claims 1 and 2.

Jeong (Fig. 5) discloses **wherein the start signal is supplied to overlap the first clock signal** (Fig. 5 shows that SP overlaps CLK2).

As to **claim 7**, it is analyzed with regard to claims 1 and 2.

Jeong (Figs. 4 and 5) discloses **wherein the outputting unit includes:**

a fourth transistor (M1) between the first power supply and the output terminal (Fig. 4 shows that M1 is between VDD and SSi), **the fourth transistor having a gate electrode coupled to the first node** (Fig. 4 shows that the gate of M1 is coupled to N1);

a fifth transistor (M2) between the output terminal and the third input terminal (Fig. 4 shows that M2 is between SSi and CLK3), **the fifth transistor having a gate electrode coupled to the second node** (Fig. 4 shows that the gate of M2 is coupled to N2);

a first capacitor (C1) between the second node and the output terminal (Fig. 4 shows that C1 is between N2 and SSi); **and**

a second capacitor (C2) between the first node and the first power supply (Fig. 4 shows that C2 is between N1 and VDD).

As to **claim 8**, it is analyzed with regard to claims 1 and 2.

Jeong (Figs. 4 and 5) discloses **wherein the second driver includes:**

a sixth transistor (M6) between the first node and the second input terminal (Fig. 4 shows that M6 is connected between CLK2 and N1 through M4), **the sixth transistor having a gate electrode coupled to the second node** (Fig. 4 shows that the gate of M6 is connected to N2); **and**

a seventh transistor (M3) between the first node and a second power supply (Fig. 4 shows that M3 is connected between N1 and VSS), **the second power supply having a lower voltage than the first power supply** ([0054] discloses that the second power supply VSS is a low level voltage source which

is less than the first power supply VDD), **the seventh transistor having a gate electrode coupled to the second input terminal** (Fig. 4 shows that the gate of M3 is coupled to CLK2 through at least C2, M1, C1, and M4).

As to **claim 14**, some of the limitations recited in this claim are similar the limitations rejected in regard to claim 1. Claim 14 differs from claim 1 in that claim 14 is directed to an organic light emitting display while claim 1 is directed to a stage circuit. Thus, the limitations of claim 14 that are similar to the limitations of claim 1 are rejected for reasons similar to those discussed in regard to claim 1.

Further, *Jeong* (Figs. 2, 3, 4, and 5) discloses **an organic light emitting display** (Fig. 2), **comprising:**

pixels (140) positioned in regions partitioned by scan lines (S1-Sn) and data lines (D1-Dm; Fig. 2 shows that the pixels 140 are separated by the scan lines and data lines);

a data driver (120) for supplying data signals to the data lines ([0034] discloses that 120 provides data signals to data lines); **and**

a scan driver (110) including stages ([0037] discloses that Fig. 3 illustrates a block diagram of an example of a shift register included in the scan driver illustrated in Fig. 2) **coupled to the scan lines** ([0041] discloses that each stage is coupled to a scan line) **in order to supply scan signals (SS1-SSn) to the scan lines** ([0041] discloses that signals SS1 to SSn are output to respective scan lines), **wherein each of the stages includes:** the features of claim 1 ([0044] discloses that Fig. 4 illustrates a detailed circuit diagram of a stage ST1).

As to **claim 15**, it is analyzed with regard to claim 14.

Jeong (Figs. 4 and 5) discloses **wherein a clock signal** (e.g. CLK3) **supplied to the third input terminal** (Fig. 4 shows that CLK3 is supplied to the terminal CLK3) **is used as the scan signal** (Fig. 5 shows that CLK3 forms SSi).

As to **claim 16**, it is analyzed with regard to claim 14.

Jeong (Figs. 3, 4, and 5) discloses **wherein the first input terminal** (SSi-1 or SP) **receives a scan signal of a previous stage** (Fig. 3 shows that the second stage receives the scan signal of the first stage) **or a start signal** (Fig. 3 shows that the first stage receives a start signal).

As to **claim 17**, it is analyzed with regard to claims 14 and 16.

Jeong (Figs. 3, 4, and 5) discloses **wherein second input terminals of odd stages receive a first clock signal** (CLK2, i.e., first clock signal, of Fig. 3; as [0045] discloses that Fig. 4 is a diagram of stage ST1, the order of terminals in Fig. 3, while not expressly shown, must be CLK2, CLK1, and CLK3; Fig. 4 shows that the terminal CLK2 receives CLK2 in the first stage; according to the pattern shown in Fig. 3 the clock assignments repeat every three stages; thus, at least another odd stage also receives CLK2 in the CLK2 terminal; therefore, odd stages receive CLK1) **and third input terminals of odd stages receive a second clock signal** (CLK3 of Fig. 3, i.e., second clock signal; Fig. 4 shows that the terminal CLK3 receives CLK3 in the first stage; according to the pattern of clocks assigned to stages as shown in Fig. 3, at least another odd stage also

receives CLK3 in the CLK3 terminal; thus, the appropriate input terminals of the odd stages receive CLK2 and CLK3), **and**

wherein second input terminals of even stages receive the second clock signal (Figs. 3 and 4 shows that the second stage receives CLK3 in the CLK2 terminal; as discussed, the pattern of clocks assigned to stages discloses that another even stage is similarly configured) **and third input terminals of even stages receive the first clock signal** (Fig. 3 shows that the clock signal CLK2 is received by the terminal CLK3 in the third stage; however, the pattern of clocks assigned to stages discloses that the sixth stage receives CLK2 in the terminal CLK3 and that another even stage is similarly configured).

As to **claims 18, 20, and 21**, each claim is analyzed with regard to claims 14, 16, and 17.

Claims 18, 20, and 21 recite limitations similar to those rejected in regard to claims 3, 7, and 8, respectively. Claims 18, 20, and 21 differ from claims 3, 7, and 8 only in that these claims are directed to an organic light emitting display depending from claims 14, 16, and 17 while claims 3, 7, and 8 are directed to a stage circuit depending from claims 1 and 2. Thus, claims 18, 20, and 21 are rejected for reasons similar to those discussed in regard to claim 3, 7, and 8, respectively.

As to **claim 27**, this claim is analyzed with regard to claims 14, 16, and 17.

Jeong (Fig. 5) discloses **wherein the scan signal of the previous stage or the start signal supplied to the first input terminal overlaps the clock**

signal supplied to the second input terminal (Fig. 5 shows that SP overlaps CLK2).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Jeong* in view of *Chung* (U.S. Publ. 2011/0227884 A1).

As to **claim 4**, it is analyzed with regard to claims 1, 2, and 3.

Jeong does not expressly disclose **wherein the first clock signal and the second clock signal have a period equal to two horizontal periods 2H and are supplied in different horizontal periods as low signals.**

Chung (Fig. 5) discloses **wherein the first clock signal and the second clock signal have a period equal to two horizontal periods 2H** (Fig. 5 shows that CLK2 and CLK3 have a period of 2H; [0036] discloses that 2H is equivalent to two horizontal cycles) **and are supplied in different horizontal periods as low signals** (Fig. 5 shows that CLK2 and CLK3 are low in different horizontal periods).

It would have been obvious that a person of ordinary skill in the art at the time the invention was made would have been motivated to modify the periods of

the clock signals disclosed in *Jeong* to be equivalent to two horizontal periods as disclosed in *Chung* because [0008] of *Chung* discloses that when the organic light emitting panel having a resolution of full high definition is driven at 120 Hz or higher, in order to prevent the generation of an abnormal scan signal due to the shortened scan time, the organic light emitting panel may be driven by increasing the pulse width of the scan signal.

7. Claims 6 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Jeong* in view of *Kim* (U.S. Publ. 2012/0062525 A1).

As to **claim 6**, it is analyzed with regard to claims 1 and 2.

Jeong (Fig. 4) discloses **wherein the first driver includes:**

a first transistor (M4) between the first input terminal and the second node (Fig. 4 shows that M4 is between SSi-1 or SP and N2), **the first transistor having a gate electrode coupled to the second input terminal** (Fig. 4 shows that the gate of M4 is coupled to CLK2).

Jeong does not expressly disclose:

a second transistor and a third transistor serially positioned between the second node and the first power supply,

wherein a gate electrode of the second transistor is coupled to the third input terminal, and

wherein a gate electrode of the third transistor is coupled to the first node.

Kim (Fig. 3) discloses:

a second transistor (M3) and a third transistor (M4) serially positioned between the second node and the first power supply (Fig. 3 shows that M3 and M4 are positioned in series between the node N2 and the power supply VGH),

wherein a gate electrode of the third transistor is coupled to the first node (Fig. 3 shows that the gate electrode of M4 is coupled to N1).

The combination of *Jeong* and *Kim* results in the transistor M1 of *Jeong* being substituted with the transistors M3 and M4 of *Kim* because Fig. 3 of *Kim* shows that two transistors connected in series may be used to drive an output, such as SSi of *Jeong*. Thus, when the transistor M1 of *Jeong* is substituted with the transistors M3 and M4 of *Kim* to output SSi, a gate of M3 is coupled to CLK3 at least through C2 of *Jeong*, M3 and M4 of *Jeong*, as modified by *Kim*, and M2 of *Jeong*. Therefore, the combination of *Jeong* and *Kim* discloses “**wherein a gate electrode of the second transistor is coupled to the third input terminal,**” as recited in claim 6.

It would have been obvious that a person of ordinary skill in the art at the time the invention was made would know that the transistor M1 of *Jeong* could have been substituted with the transistors M3 and M4 of *Kim* because Fig. 3 of *Kim* suggests that the substitution would not have changed function of M1 of *Jeong* because both gates of M3 and M4 of *Kim* are connected to the same

input. Thus, the combination of *Jeong* and *Kim* is a simple substitution of one known element for another that produces a predictable result.

As to **claim 19** this claim is analyzed with regard to claims 14, 16, and 17.

Claim 19 recites limitations similar to those rejected in regard to claim 6. Claim 19 differs from claim 6 only in that this claim is directed to an organic light emitting display depending from claims 14, 16, and 17 while claim 6 is directed to a stage circuit depending from claims 1 and 2. Thus, claim 19 is rejected for reasons similar to those discussed in regard to claim 6.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN C. KIRKPATRICK whose telephone number is (571) 270-3343. The examiner can normally be reached on 9:00 am - 5:30 pm

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh D. Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2691

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JOHN C KIRKPATRICK/
Examiner, Art Unit 2691

Notice of References Cited	Application/Control No. 13/771,385	Applicant(s)/Patent Under Reexamination JANG, HWAN-SOO	
	Examiner JOHN KIRKPATRICK	Art Unit 2691	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2008/0062097 A1	03-2008	Jeong et al.	345/84
*	B	US-2012/0062525 A1	03-2012	Kim, Dong-Hwi	345/204
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	"20120327131".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/01/28 19:27
S2	2	"20110227884".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/01/28 20:13
S3	0	(12/904976).APP.	USPAT; USOCR	OR	ON	2015/01/28 20:23
S4	18	("20040217935" "20070063933" "20080055225" "20080094531" "20080219401" "20110193892" "20120050234").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/01/28 20:36
S6	119	S5 and OLED	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/01/28 21:39
S5	3438	377/64-81.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/01/28 21:39
S7	66	S5 and OLED and \$1VDD	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/01/28 21:40
S9	8	("20040227718" "20050008114" "20050212746" "20060092148" "7239179").PN. OR ("7786972").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2015/01/29 15:56
S8	1	(11/826103).APP.	USPAT; USOCR	OR	ON	2015/01/29 15:56
S10	9	"38828363".FMID.	US-PGPUB; USPAT; FPRS	OR	ON	2015/01/29 16:00
S12	175	S11 and OLED and stage and \$2VDD	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/01/29 16:41
S11	478335	samsung.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2015/01/29 16:41

			IBM_TDB			
S14	30	S11 and OLED and (stage same node) and \$2VDD and (clock clk\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/01/29 16:42
S13	41	S11 and OLED and (stage same node) and \$2VDD	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/01/29 16:42
S15	5	"20120062525"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/01/29 19:50
L14	3016	G09G2310/0286.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/01/30 23:24
L15	8012	G09G3/3677.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/01/30 23:25

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	140864	samsung.as.	US-PGPUB; USPAT; UPAD	OR	ON	2015/01/30 23:09
L2	18	JANG near2 Hwan-Soo	US-PGPUB; USPAT; UPAD	OR	ON	2015/01/30 23:10
L11	55	(I1 I2) and I10	US-PGPUB; USPAT; UPAD	OR	ON	2015/01/30 23:15
L10	461	(stage second node voltage input output terminal power driver).clm.	US-PGPUB; USPAT; UPAD	AND	ON	2015/01/30 23:15

1/ 30/ 2015 11:53:40 PM
C:\ Users\ jkirkpatrick\ Documents\ EAST\ Workspaces\ 13771385.wsp

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	13/771,385
	Filing Date	February 20, 2013
	First Named Inventor	Hwan-Soo JANG
	Art Unit	2691
(Multiple sheets used when necessary)	Examiner	John Kirkpatrick
SHEET 1 of 1; December 19, 2014	Attorney Docket No.	304/1043

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1.	US 2012/0327131 A1	12-27-2012	JANG	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code-Number-Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T ¹
	2.	KR 10-2013-0000020 A*	01-02-2013	JANG	Family member for: US 2012/0327131 A1	
* with English Abstract						

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ¹

IDENTIFICATION OF OFFICE ACTIONS AND/OR SEARCH REPORTS FROM RELATED APPLICATIONS	
A copy of each of the following document(s) is appended to the present IDS submission. Documents cited above, if any, may be identified therein. The following documents do not constitute "prior art references" but are included for informational purposes.	T ¹

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.C.K./

Examiner Signature /John Kirkpatrick/	Date Considered 01/30/2015
Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

T¹ - Place a check mark in this area when an English language Translation is attached.

Case No. IPR2023-01221

INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Multiple sheets used when necessary)</i>	Application No.	13/771,385
	Filing Date	February 20, 2013
	First Named Inventor	Hwan-Soo JANG
	Art Unit	
	Examiner	
SHEET 1 of 1; February 20, 2013	Attorney Docket No.	304/1043

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1.	2011/0227884 A1	09-22-2011	CHUNG	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code-Number-Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T ¹
	2.	KR 10-2011-0104320 A*	09-22-2011	CHUNG	Family = US 2011/0227884 A1	

* with English Abstract

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ¹

IDENTIFICATION OF OFFICE ACTIONS AND/OR SEARCH REPORTS FROM RELATED APPLICATIONS	
A copy of each of the following document(s) is appended to the present IDS submission. Documents cited above, if any, may be identified therein. The following documents do not constitute "prior art references" but are included for informational purposes.	T ¹

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Examiner Signature	/John Kirkpatrick/	Date Considered	01/30/2015
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Search Notes 	Application/Control No. 13771385	Applicant(s)/Patent Under Reexamination JANG, HWAN-SOO
	Examiner JOHN KIRKPATRICK	Art Unit 2691

CPC- SEARCHED		
Symbol	Date	Examiner
G09G3/3677, 2310/0286	1/20.2015	JCK

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
EAST: Inventor Name Search	1/30/2015	JCK
EAST: (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB) see search history printout	1/28/2015-1/30/2015	JCK

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/J.K./ Examiner.Art Unit 2691	
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<i>Index of Claims</i> 	Application/Control No. 13771385	Applicant(s)/Patent Under Reexamination JANG, HWAN-SOO
	Examiner JOHN KIRKPATRICK	Art Unit 2691

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	01/30/2015							
	1	✓							
	2	✓							
	3	✓							
	4	✓							
	5	✓							
	6	✓							
	7	✓							
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	25	N							
	26	N							
	27	✓							



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SERIAL NUMBER 13/771,385	FILING or 371(c) DATE 02/20/2013 RULE	CLASS 345	GROUP ART UNIT 2691	ATTORNEY DOCKET NO. 304/1043	
APPLICANTS INVENTORS Hwan-Soo JANG, Yongin-City, KOREA, REPUBLIC OF; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** REPUBLIC OF KOREA 10-2012-0104512 09/20/2012 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 03/11/2013					
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and /JOHN KIRKPATRICK/ Acknowledged Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY KOREA, REPUBLIC OF	SHEETS DRAWINGS 7	TOTAL CLAIMS 27	INDEPENDENT CLAIMS 2
ADDRESS LEE & MORSE, P.C. 3141 FAIRVIEW PARK DRIVE SUITE 500 FALLS CHURCH, VA 22042 UNITED STATES					
TITLE STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME					
FILING FEE RECEIVED 1694	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Hwan-Soo JANG

Art Unit: 2691

Serial No. 13/771,385

Examiner: John Kirkpatrick

Filed: February 20, 2013

Confirmation No. 3091

For: STAGE CIRCUIT AND ORGANIC LIGHT
EMITTING DISPLAY USING THE SAME

Attorney Docket No. 304/1043

RESPONSE TO ELECTION REQUIREMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA. 22313-1450

Commissioner:

In response to the Office Action dated October 21, 2014, applicants hereby elect Species A, for prosecution in the subject application. It is respectfully submitted that at least claims 1 and 14 are generic, and that claims 1-8, 14-21, and 27 read on Species A.

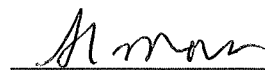
Applicants reserve the right to file a divisional application covering the subject matter of the non-elected claims.

Receipt of the initial Office Action on the merits is awaited.

Respectfully submitted,
LEE & MORSE, P.C.

December 19, 2014

Date



Susan S. Morse, Registration No. 35,292
/Susan S. Morse/

LEE & MORSE, P.C.

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FALLS CHURCH, VA 22042
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PETITION and DEPOSIT ACCOUNT CHARGE AUTHORIZATION

This document and any concurrently filed papers are believed to be timely. Should any extension of the term be required, applicant hereby petitions the Director for such extension and requests that any applicable petition fee be charged to Deposit Account No. 50-1645.

If fee payment is enclosed, this amount is believed to be correct. However, the Director is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-1645.

Any additional fee(s) necessary to effect the proper and timely filing of the accompanying-papers may also be charged to Deposit Account No. 50-1645.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Hwan-Soo JANG

Art Unit: 2691

Serial No. 13/771,385

Examiner: John Kirkpatrick

Filed: February 20, 2013

Confirmation No. 3091

For: STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE
SAME

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §1.56

Mail Stop: AMENDMENT
Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

Submitted herewith on Form PTO/SB/08 is a listing of a document(s) known to applicant in order to comply with applicant's duty of disclosure pursuant to 37 C.F.R. §1.56.

☒ A copy of each listed non-U.S. patent and/or patent publication and cited literature is being submitted to comply with the provisions of 37 C.F.R. §§1.97 & 1.98. [Box checked if applicable.]

* * *

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application. Applicant does not waive any rights to take any action that would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* prior art reference against the claims of the present application.

Where available, copies of English language patent family members of non-English patent documents have been provided. Such submission of English language patent family members is for the convenience of the Office and is not to be construed as an indication that such English language patent family members are literal translations of the non-English patents. Applicant(s) expressly reserve their right to file verified English translations of the non-English patent documents.

☒ The listed document(s) is/are being submitted in compliance with 37 C.F.R. § 1.97(b)(3): submission before the mailing date of the first action on the merits *or* 37 C.F.R. § 1.97(b)(4): submission before the mailing date of an action after the filing of a request for continued examination under § 1.114. [Box checked if applicable.]

☐ The foregoing document(s) came to applicant's attention during the prosecution of their corresponding _____ application. ☐ A copy of the _____ Notice of Allowance is also attached. [Box(es) checked if applicable.]

CERTIFICATION

☐ The undersigned hereby certifies in accordance with 37 CFR §1.97(e)(1) that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three (3) months prior to the filing of this Statement. [Box checked if applicable.]

* * *

Applicant respectfully requests that the listed document(s) be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO/SB/08 be returned in accordance with MPEP §609.

* * *

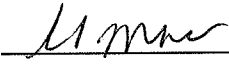
FEE PAYMENT

- ☐ The fee mandated by 37 C.F.R. §1.17(p) is believed applicable. [Box checked if applicable.]
- ☐ This fee (\$180.00) will be paid electronically by Credit Card. [Box checked if applicable.]
- ☐ This fee may be charged to Deposit Account No. 50-1645. (A duplicate copy of this paper is enclosed.) [Box checked if applicable.]

Respectfully submitted,

LEE & MORSE, P.C.

December 19, 2014
Date



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Any additional fee(s) necessary to effect the proper and timely filing of the above-paper may also be charged to Deposit Account No. 50-1645.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	13/771,385
	Filing Date	February 20, 2013
	First Named Inventor	Hwan-Soo JANG
	Art Unit	2691
(Multiple sheets used when necessary)	Examiner	John Kirkpatrick
SHEET 1 of 1; December 19, 2014	Attorney Docket No.	304/1043

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1.	US 2012/0327131 A1	12-27-2012	JANG	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code-Number-Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T ¹
	2.	KR 10-2013-0000020 A*	01-02-2013	JANG	Family member for: US 2012/0327131 A1	

* with English Abstract

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ¹

IDENTIFICATION OF OFFICE ACTIONS AND/OR SEARCH REPORTS FROM RELATED APPLICATIONS	
A copy of each of the following document(s) is appended to the present IDS submission. Documents cited above, if any, may be identified therein. The following documents do not constitute "prior art references" but are included for informational purposes.	T ¹

Examiner Signature	Date Considered
Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Case No. IPR2023-01221
Mianyang BOE Ex. 1002



US 20120327131A1

(19) **United States**

(12) **Patent Application Publication**

Jang

(10) Pub. No.: US 2012/0327131 A1

(43) Pub. Date: Dec. 27, 2012

(54) **STAGE CIRCUIT AND EMISSION DRIVER
USING THE SAME**

(52) U.S. CL. 345/690; 327/427

(76) Inventor: Hwan-Soo Jang, Yongin-city (KR)

(57) **ABSTRACT**

(21) Appl. No.: 13/403,834

(22) Filed: Feb. 23, 2012

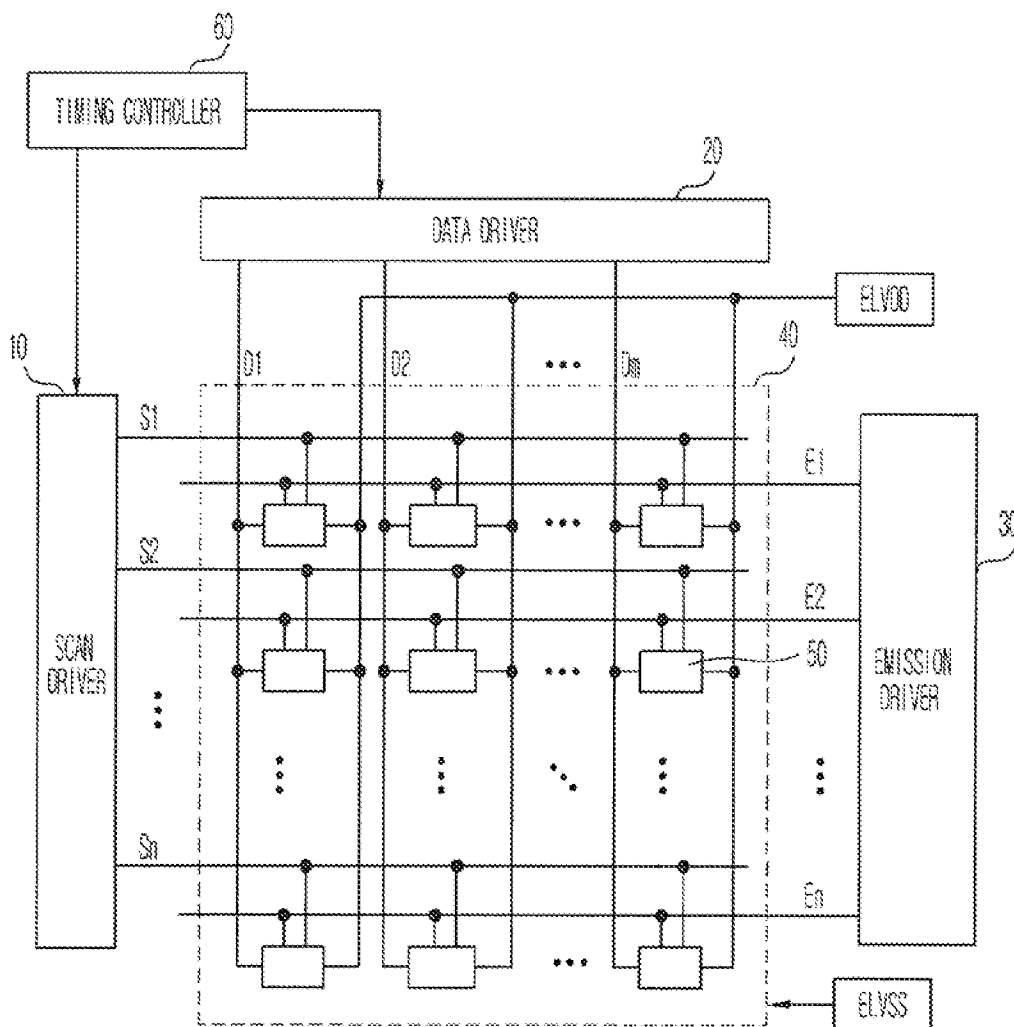
(30) **Foreign Application Priority Data**

Jun. 22, 2011 (KR) 10-2011-0050441

Publication Classification

(51) **Int. Cl.**
G09G 5/10 (2006.01)
H03K 17/687 (2006.01)

A stage circuit includes an output unit for outputting the voltage of a first or second power source to a first output terminal, corresponding to a voltage at a first or second node; a bidirectional driver for receiving sampling signals of previous and next stages; a first driver coupled to the bidirectional driver to control the voltages at the first and second nodes, corresponding to first and second clock signals; and a second driver coupled to the bidirectional driver to output a sampling signal corresponding to the first and second clock signals. The first driver includes a first transistor coupled between the first power source and the second node; a second transistor coupled between the second node and the second power source; a third transistor coupled between the bidirectional driver and the first node; and a first capacitor coupled between the second node and a second input terminal.





(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

(11) 공개번호 10-2013-0000020
(43) 공개일자 2013년01월02일

(51) 국제특허분류(Int. Cl.)

G09G 3/30 (2006.01) G09G 3/30 (2006.01)

(21) 출원번호 10-2011-0060441

(22) 출원일자 2011년06월22일

심사청구일자 없음

(71) 출원인

삼성디스플레이 주식회사

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신영무

전체 청구항 수 : 총 21 항

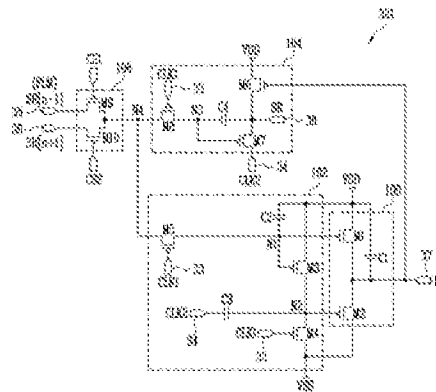
(54) 발명의 명칭 스테이지 회로 및 이를 이용한 발광 제어선 구동부

(57) 요약

본 발명은 출력의 안정성을 확보함과 동시에 발광 제어신호의 폭을 저속음계 조절할 수 있도록 한 스테이지 회로에 관한 것이다.

본 발명의 스테이지 회로는 제 1노드 및 제 2노드의 전압에 대응하여 제 1입력단자로 제 1전원 또는 제 2전원의 전압을 출력하기 위한 출력부; 이진단 스테이지 및 다중단 스테이지의 샘플링신호를 공급받는 양방향 구동부와; 상기 양방향 구동부에 접속되며, 제 1클럭신호 및 제 2클럭신호에 대응하여 상기 제 1노드 및 제 2노드의 전압을 제어하기 위한 제 1구동부와; 상기 양방향 구동부에 접속되며, 상기 제 1클럭신호 및 제 2클럭신호에 대응하여 샘플링신호를 출력하기 위한 제 2구동부를 구비하며; 상기 제 1구동부는 상기 제 1전원과 상기 제 2노드 사이에 접속되며, 게이트전극이 상기 제 1노드에 접속되는 제 3트랜지스터와; 상기 제 2노드와 상기 제 2전원 사이에 접속되며, 게이트전극이 제 1입력단자에 접속되는 제 4트랜지스터와; 상기 양방향 구동부와 상기 제 1노드 사이에 접속되며, 게이트전극이 상기 제 1입력단자에 접속되는 제 5트랜지스터와; 상기 제 2노드와 제 2입력단자 사이에 접속되는 제 3트랜지스터를 구비한다.

도 1도 - 도 3



특허청구의 범위

청구항 1

제 1노드 및 제 2노드의 전압에 대응하여 제 1출력단자로 제 1전원 또는 제 2전원의 전압을 출력하기 위한 출력부와;

이전단 스테이지 및 다음단 스테이지의 샘플링신호를 공급받는 양방향 구동부;

상기 양방향 구동부에 접속되며, 제 1클럭신호 및 제 2클럭신호에 대응하여 상기 제 1노드 및 제 2노드의 전압을 제어하기 위한 제 1구동부와;

상기 양방향 구동부에 접속되며, 상기 제 1클럭신호 및 제 2클럭신호에 대응하여 샘플링신호를 출력하기 위한 제 2구동부를 구비하며;

상기 제 1구동부는

상기 제 1전원과 상기 제 2노드 사이에 접속되며, 게이트전극이 상기 제 1노드에 접속되는 제 3트랜지스터와;

상기 제 2노드와 상기 제 2전원 사이에 접속되며, 게이트전극이 제 1입력단자에 접속되는 제 4트랜지스터와;

상기 양방향 구동부와 상기 제 1노드 사이에 접속되며, 게이트전극이 상기 제 1입력단자에 접속되는 제 5트랜지스터와;

상기 제 2노드와 제 2입력단자 사이에 접속되는 제 3커패시터를 구비하는 것을 특징으로 하는 스테이지 회로.

청구항 2

제 1항에 있어서,

상기 제 1구동부는 상기 제 1노드와 상기 제 1전원 사이에 접속되는 제 2커패시터를 더 구비하는 것을 특징으로 하는 스테이지 회로.

청구항 3

제 1항에 있어서,

상기 제 1입력단자로는 상기 제 1클럭신호가 공급되고, 상기 제 2입력단자로는 상기 제 2클럭신호가 공급되는 것을 특징으로 하는 스테이지 회로.

청구항 4

제 1항에 있어서,

상기 제 1클럭신호 및 제 2클럭신호는 서로 다른 주파수간에 공급되는 것을 특징으로 하는 스테이지 회로.

청구항 5

제 1항에 있어서,

상기 제 1전원은 상기 제 2전원 보다 높은 전압으로 설정되는 것을 특징으로 하는 스테이지 회로.

청구항 6

제 1항에 있어서,

상기 출력부는

상기 제 1전원과 상기 제 1출력단자 사이에 접속되며, 게이트전극이 상기 제 1노드에 접속되는 제 1트랜지스터와;

상기 제 1출력단자와 상기 제 2전원 사이에 접속되며, 게이트전극이 상기 제 2노드에 접속되는 제 2트랜지스터와;

상기 제 1전원과 상기 제 1출력단자 사이에 접속되는 제 1캐패시터를 구비하는 것을 특징으로 하는 스테이지 회로.

청구항 7

제 1항에 있어서,

상기 제 2구동부는

상기 제 1전원과 제 2출력단자 사이에 접속되며, 게이트전극이 상기 제 1출력단자에 접속되는 제 6트랜지스터와;

상기 제 2출력단자와 상기 제 2입력단자 사이에 접속되며, 게이트전극이 제 3노드에 접속되는 제 7트랜지스터와;

상기 제 3노드와 상기 양방향 구동부 사이에 접속되며, 게이트전극이 상기 제 1입력단자에 접속되는 제 8트랜지스터와;

상기 제 3노드와 상기 제 2출력단자 사이에 접속되는 제 4캐패시터를 구비하는 것을 특징으로 하는 스테이지 회로.

청구항 8

제 1항에 있어서,

상기 양방향 구동부는

상기 이전단 스테이지와 상기 제 1구동부 및 제 2구동부의 공통단자인 제 4노드 사이에 접속되며, 게이트전극으로 제 1제어신호를 공급받는 제 9트랜지스터와;

상기 다음단 스테이지와 상기 제 4노드 사이에 접속되며, 게이트전극으로 제 2제어신호를 공급받는 제 10트랜지스터를 구비하는 것을 특징으로 하는 스테이지 회로.

청구항 9

제 8항에 있어서,

상기 제 1제어신호 및 제 2제어신호는 서로 중첩되지 않게 공급되는 것을 특징으로 하는 스테이지 회로.

청구항 10

제 1항에 있어서,

상기 제 1노드와 상기 제 2전원 사이에 접속되며, 게이트전극으로 리셋신호를 공급받는 제 11트랜지스터를 더 구비하는 것을 특징으로 하는 스테이지 회로.

청구항 11

제 10항에 있어서,

상기 리셋신호는 전원의 입력 및 차단될 때 적어도 한번 공급되는 것을 특징으로 하는 스테이지 회로.

청구항 12

제 1항에 있어서,

상기 제 3캐패시터와 상기 제 2입력단자 사이에 접속되며, 게이트전극이 상기 제 2노드에 접속되는 제 12트랜지스터를 더 구비하는 것을 특징으로 하는 스테이지 회로.

청구항 13

제 1항에 있어서,

상기 제 3트랜지스터는 상기 제 4트랜지스터보다 낮은 저항을 갖도록 형성되는 것을 특징으로 하는 스테이지 회로.

로.

청구항 14

화소들의 발광을 제어하기 위하여 발광 제어선들로 발광 제어신호를 공급하기 위한 발광 제어선 구동부에 있어서,

상기 발광 제어선 구동부는 상기 발광 제어선들 각각과 접속되도록 상기 제 1항 내지 제 13항 중 어느 한 항에 기재된 스테이지 회로를 구비하는 것을 특징으로 하는 발광 제어선 구동부.

청구항 15

화소들의 발광을 제어하기 위하여 발광 제어선들로 발광 제어신호를 공급하기 위한 발광 제어선 구동부에 있어서,

상기 발광 제어선 구동부는 상기 발광 제어선들 각각과 접속되도록 스테이지 회로를 구비하며;

상기 스테이지 회로는

제 1노드 및 제 2노드의 전압에 대응하여 발광 제어선과 접속된 제 1출력단자로 제 1전원 또는 제 2전원의 전압을 출력하기 위한 출력부와;

이전단 스테이지 및 다음단 스테이지의 샘플링신호를 공급받는 양방향 구동부와;

상기 양방향 구동부에 접속되며, 제 1클럭신호 및 제 2클럭신호에 대응하여 상기 제 1노드 및 제 2노드의 전압을 제어하기 위한 제 1구동부와;

상기 양방향 구동부에 접속되며, 상기 제 1클럭신호 및 제 2클럭신호에 대응하여 샘플링신호를 출력하기 위한 제 2구동부를 구비하며;

상기 제 1구동부는

상기 제 1전원과 상기 제 2노드 사이에 접속되며, 게이트전극이 상기 제 1노드에 접속되는 제 3트랜지스터와;

상기 제 2노드와 상기 제 2전원 사이에 접속되며, 게이트전극이 제 1입력단자에 접속되는 제 4트랜지스터와;

상기 양방향 구동부와 상기 제 1노드 사이에 접속되며, 게이트전극이 상기 제 1입력단자에 접속되는 제 5트랜지스터와;

상기 제 2노드와 제 2입력단자 사이에 접속되는 제 3커패시터를 구비하는 것을 특징으로 하는 발광 제어선 구동부.

청구항 16

제 15항에 있어서,

$k(k$ 는 홀수 또는 짝수)번째 스테이지의 제 1입력단자로는 상기 제 1클럭신호, 제 2입력단자로는 제 2클럭신호가 공급되며;

$k+1$ 번째 스테이지의 제 1입력단자로는 상기 제 2클럭신호, 제 2입력단자로는 제 1클럭신호가 공급되는 것을 특징으로 하는 발광 제어선 구동부.

청구항 17

제 15항에 있어서,

상기 출력부는

상기 제 1전원과 상기 제 1출력단자 사이에 접속되며, 게이트전극이 상기 제 1노드에 접속되는 제 1트랜지스터와;

상기 제 1출력단자와 상기 제 2전원 사이에 접속되며, 게이트전극이 상기 제 2노드에 접속되는 제 2트랜지스터와;

상기 제 1전원과 상기 제 1출력단자 사이에 접속되는 제 1커패시터를 구비하는 것을 특징으로 하는 발광 제어선

구동부.

청구항 18

제 15항에 있어서,

상기 제 2구동부는

상기 제 1전원과 제 2출력단자 사이에 접속되며, 게이트전극이 상기 제 1출력단자에 접속되는 제 6트랜지스터와;

상기 제 2출력단자와 상기 제 2입력단자 사이에 접속되며, 게이트전극이 제 3노드에 접속되는 제 7트랜지스터와;

상기 제 3노드와 상기 양방향 구동부 사이에 접속되며, 게이트전극이 상기 제 1입력단자에 접속되는 제 8트랜지스터와;

상기 제 3노드와 상기 제 2출력단자 사이에 접속되는 제 4커패시터를 구비하는 것을 특징으로 하는 발광 제어선 구동부.

청구항 19

제 15항에 있어서,

상기 제 1노드와 상기 제 2전원 사이에 접속되며, 게이트전극으로 리셋신호를 공급받는 제 11트랜지스터를 더 구비하는 것을 특징으로 하는 발광 제어선 구동부.

청구항 20

제 19항에 있어서,

상기 리셋신호는 전원의 입력 및 차단될 때 적어도 한번 공급되는 것을 특징으로 하는 발광 제어선 구동부.

청구항 21

제 15항에 있어서,

상기 제 3커패시터와 상기 제 2입력단자 사이에 접속되며, 게이트전극이 상기 제 2노드에 접속되는 제 12트랜지스터를 더 구비하는 것을 특징으로 하는 발광 제어선 구동부.

명 세 서

기술 분야

[0001] 본 발명은 스테이지 회로 및 이를 이용한 발광 제어선 구동부에 관한 것으로, 특히 출력의 안정성을 확보함과 동시에 발광 제어신호의 폭을 자유롭게 조절할 수 있도록 한 스테이지 회로 및 이를 이용한 발광 제어선 구동부에 관한 것이다.

배경 기술

[0002] 최근 음극선관(Cathode Ray Tube)의 단점인 무게와 부피를 줄일 수 있는 각종 평판 표시장치가 많이 개발되고 있다. 평판 표시장치는 액정 표시장치(Liquid Crystal Display), 전계방출 표시장치(Field Emission Display), 플라즈마 표시패널(Plasma Display Panel) 및 유기전계발광 표시장치(Organic Light Emitting Display Device) 등이 있다.

[0003] 평판표시장치 중 유기전계발광 표시장치는 전자와 정공의 재결합에 의하여 빛을 발생시키는 유기 발광 다이오드를 이용하여 영상을 표시한다. 이러한, 유기전계발광 표시장치는 빠른 응답속도를 가짐과 동시에 낮은 소비전력으로 구동되는 장점이 있다. 일반적인 유기전계발광 표시장치는 화소마다 형성되는 트랜지스터를 이용하여 데이터신호에 대응하는 전류를 유기 발광 다이오드로 공급함으로써 유기 발광 다이오드에서 빛이 발생되게 한다.

- [0004] 이와 같은 종래의 유기전계발광 표시장치는 데이터선들로 데이터신호를 공급하기 위한 데이터 구동부, 주사선들로 주사신호를 순차적으로 공급하기 위한 주사 구동부, 발광 제어선으로 발광 제어신호를 공급하기 위한 발광 제어선 구동부 및 데이터선들, 주사선들 및 발광 제어선들과 접속되는 복수의 화소를 구비하는 화소부를 구비한다.
- [0005] 화소부에 포함된 화소들은 주사선으로 주사신호가 공급될 때 선택되어 데이터선으로부터 데이터신호를 공급받는다. 데이터신호를 공급받은 화소들은 데이터신호에 대응하는 소정 휘도의 빛을 생성하면서 소정의 영상을 표시한다. 여기서, 화소들의 발광시간은 발광 제어선으로부터 공급되는 발광 제어신호에 의하여 제어된다. 일반적으로 발광 제어신호는 하나의 주사선 또는 두개의 주사선으로 공급되는 주사신호와 중첩되도록 공급되면서 데이터신호가 공급되는 화소들을 비발광 상태로 설정한다.
- [0006] 이를 위하여, 발광 제어선 구동부는 발광 제어선들 각각과 접속되는 스테이지를 구비한다. 스테이지는 4개 이상의 출력신호를 공급받아 하이 또는 로우의 전압을 출력선으로 출력한다.
- [0007] 하지만, 종래의 발광 제어선 구동부에 포함되는 스테이지는 4개 이상의 출력신호에 의하여 구동되기 때문에 많은 수의 트랜지스터들을 포함하고, 이에 따라 제조비용을 증가함과 동시에 구동의 신뢰성 확보가 어려운 문제점이 있다. 또한, 발광 제어선 구동부를 PMOS 트랜지스터로 구성하는 경우 로우레벨의 출력이 불안정한 문제점이 있다.
- [0008] 상세히 설명하면, 발광 제어선으로 로우신호를 공급하는 경우 로우신호를 출력하는 트랜지스터의 게이트전극은 로우신호보다 낮은 전압을 유지해야 한다. 하지만, 누설전류 등에 의하여 트랜지스터의 게이트전극 전압이 상승되고, 이에 따라 로우신호의 출력이 불안정한 문제점이 있다.

발명의 내용

해결하려는 과제

- [0009] 따라서, 본 발명의 목적은 출력의 안정성을 확보함과 동시에 발광 제어신호의 폭을 자유롭게 조절할 수 있도록 한 스테이지 회로 및 이를 이용한 발광 제어선 구동부를 제공하는 것이다.

과제의 해결 수단

- [0010] 본 발명의 실시예에 의한 스테이지 회로는 제 1노드 및 제 2노드의 전압에 대응하여 제 1출력단자로 제 1전원 또는 제 2전원의 전압을 출력하기 위한 출력부; 이전단 스테이지 및 다음단 스테이지의 샘플링신호를 공급받는 양방향 구동부와; 상기 양방향 구동부에 접속되며, 제 1출력신호 및 제 2출력신호에 대응하여 상기 제 1노드 및 제 2노드의 전압을 제어하기 위한 제 1구동부와; 상기 양방향 구동부에 접속되며, 상기 제 1출력신호 및 제 2출력신호에 대응하여 샘플링신호를 출력하기 위한 제 2구동부를 구비하며; 상기 제 1구동부는 상기 제 1전원과 상기 제 2노드 사이에 접속되며, 게이트전극이 상기 제 1노드에 접속되는 제 3트랜지스터와; 상기 제 2노드와 상기 제 2전원 사이에 접속되며, 게이트전극이 제 1입력단자에 접속되는 제 4트랜지스터와; 상기 양방향 구동부와 상기 제 1노드 사이에 접속되며, 게이트전극이 상기 제 1입력단자에 접속되는 제 5트랜지스터와; 상기 제 2노드와 제 2입력단자 사이에 접속되는 제 3캐패시터를 구비한다.
- [0011] 바람직하게, 상기 제 1구동부는 상기 제 1노드와 상기 제 1전원 사이에 접속되는 제 2캐패시터를 더 구비한다. 상기 제 1입력단자로는 상기 제 1출력신호가 공급되고, 상기 제 2입력단자로는 상기 제 2출력신호가 공급된다. 상기 제 1출력신호 및 제 2출력신호는 서로 다른 수평기간에 공급된다. 상기 제 1전원은 상기 제 2전원 보다 높은 전압으로 설정된다.
- [0012] 상기 출력부는 상기 제 1전원과 상기 제 1출력단자 사이에 접속되며, 게이트전극이 상기 제 1노드에 접속되는 제 1트랜지스터와; 상기 제 1출력단자와 상기 제 2전원 사이에 접속되며, 게이트전극이 상기 제 2노드에 접속되는 제 2트랜지스터와; 상기 제 1전원과 상기 제 1출력단자 사이에 접속되는 제 1캐패시터를 구비한다.
- [0013] 상기 제 2구동부는 상기 제 1전원과 제 2출력단자 사이에 접속되며, 게이트전극이 상기 제 1출력단자에 접속되는 제 6트랜지스터와; 상기 제 2출력단자와 상기 제 2입력단자 사이에 접속되며, 게이트전극이 제 3노드에 접속되는 제 7트랜지스터와; 상기 제 3노드와 상기 양방향 구동부 사이에 접속되며, 게이트전극이 상기 제 1입력단

자에 접속되는 제 8트랜지스터와; 상기 제 3노드와 상기 제 2출력단자 사이에 접속되는 제 4캐패시터를 구비한다.

[0014] 상기 양방향 구동부는 상기 이전단 스테이지와 상기 제 1구동부 및 제 2구동부의 공통단자인 제 4노드 사이에 접속되며, 게이트전극으로 제 1제어신호를 공급받는 제 9트랜지스터와; 상기 다음단 스테이지와 상기 제 4노드 사이에 접속되며, 게이트전극으로 제 2제어신호를 공급받는 제 10트랜지스터를 구비한다. 상기 제 1제어신호 및 제 2제어신호는 서로 중첩되지 않게 공급된다.

[0015] 상기 제 1노드와 상기 제 2전원 사이에 접속되며, 게이트전극으로 리셋신호를 공급받는 제 11트랜지스터를 더 구비한다. 상기 리셋신호는 전원의 입력 및 차단될 때 적어도 한번 공급된다. 상기 제 3캐패시터와 상기 제 2 입력단자 사이에 접속되며, 게이트전극이 상기 제 2노드에 접속되는 제 12트랜지스터를 더 구비한다. 상기 제 3트랜지스터는 상기 제 4트랜지스터보다 낮은 저항을 갖도록 형성된다.

[0016] 본 발명은 회소들의 발광을 제어하기 위하여 발광 제어선들로 발광 제어신호를 공급하기 위한 발광 제어선 구동부에 있어서, 상기 발광 제어선 구동부는 상기 발광 제어선들 각각과 접속되도록 상기 제 1항 내지 제 13항 중 어느 한 항에 기재된 스테이지 회로를 구비한다.

[0017] 본 발명은 회소들의 발광을 제어하기 위하여 발광 제어선들로 발광 제어신호를 공급하기 위한 발광 제어선 구동부에 있어서; 상기 발광 제어선 구동부는 상기 발광 제어선들 각각과 접속되도록 스테이지 회로를 구비하며; 상기 스테이지 회로는 제 1노드 및 제 2노드의 전압에 대응하여 발광 제어신과 접속된 제 1출력단자로 제 1전원 또는 제 2전원의 전압을 출력하기 위한 출력부와; 이전단 스테이지 및 다음단 스테이지의 샘플링신호를 공급받는 양방향 구동부와; 상기 양방향 구동부에 접속되며, 제 1클럭신호 및 제 2클럭신호에 대응하여 상기 제 1노드 및 제 2노드의 전압을 제어하기 위한 제 1구동부와; 상기 양방향 구동부에 접속되며, 상기 제 1클럭신호 및 제 2클럭신호에 대응하여 샘플링신호를 출력하기 위한 제 2구동부를 구비하며; 상기 제 1구동부는 상기 제 1전원과 상기 제 2노드 사이에 접속되며, 게이트전극이 상기 제 1노드에 접속되는 제 3트랜지스터와; 상기 제 2노드와 상기 제 2전원 사이에 접속되며, 게이트전극이 제 1입력단자에 접속되는 제 4트랜지스터와; 상기 양방향 구동부와 상기 제 1노드 사이에 접속되며, 게이트전극이 상기 제 1입력단자에 접속되는 제 5트랜지스터와; 상기 제 2노드와 제 2입력단자 사이에 접속되는 제 3캐패시터를 구비한다.

[0018] 바람직하게, k (k 는 홀수 또는 짝수)번째 스테이지의 제 1입력단자로는 상기 제 1클럭신호, 제 2입력단자로는 제 2클럭신호가 공급되며; $k+1$ 번째 스테이지의 제 1입력단자로는 상기 제 2클럭신호, 제 2입력단자로는 제 1클럭신호가 공급된다.

발명의 효과

[0019] 본 발명의 스테이지 회로 및 이를 이용한 발광 제어선 구동부는 2개의 클럭신호에 대응하여 구동되기 때문에 회로구성이 간략화되고, 이에 따라 신뢰성을 향상시킬 수 있다. 또한, 본원 발명에서는 클럭신호가 공급될 때마다 로우신호를 출력하는 트랜지스터의 게이트전극의 전압이 하강되고, 이에 따라 로우신호를 안정적으로 출력할 수 있다.

도면의 간단한 설명

[0020] 도 1은 본 발명의 실시예에 의한 유기전계발광 표시장치를 나타내는 도면이다.

도 2는 도 1에 도시된 발광제어선 구동부의 스테이지를 개략적으로 나타내는 도면이다.

도 3은 도 2에 도시된 스테이지의 제 1실시예를 나타내는 회로도이다.

도 4는 도 3에 도시된 스테이지 회로의 구동방법을 나타내는 파형도이다.

도 5는 도 3에 도시된 스테이지 회로의 시작신호에 대응한 발광 제어신호를 나타내는 시뮬레이션 결과를 나타내는 도면이다.

도 6은 도 2에 도시된 스테이지의 제 2실시예를 나타내는 회로도이다.

도 7은 도 3에 도시된 스테이지 회로의 양방향 구동에 대응한 시뮬레이션 결과를 나타내는 도면이다.

도 8은 도 2에 도시된 스테이지의 제 3실시예를 나타내는 회로도이다.

도 9는 도 2에 도시된 스테이지의 제 4실시예를 나타내는 회로도이다.

도 10은 도 8에 도시된 스테이지 회로의 시뮬레이션 결과를 나타내는 도면이다.

발명을 실시하기 위한 구체적인 내용

- [0021] 이하, 본 발명이 속하는 기술분야에서 통상의 지식을 가진 자가 본 발명을 용이하게 실시할 수 있는 바람직한 실시 예가 첨부된 도 1 내지 도 10을 참조하여 자세히 설명하면 다음과 같다.
- [0022] 도 1은 본 발명의 실시예에 의한 유기전계발광 표시장치를 나타내는 도면이다.
- [0023] 도 1을 참조하면, 본 발명의 실시예에 의한 유기전계발광 표시장치는 주사선들(S1 내지 Sn), 데이터선들(D1 내지 Dm) 및 발광 제어선들(E1 내지 En)의 교차부에 위치되는 화소들(50)을 포함하는 화소부(40)와, 주사선들(S1 내지 Sn)을 구동하기 위한 주사 구동부(10)와, 데이터선들(D1 내지 Dm)을 구동하기 위한 데이터 구동부(20)와, 발광 제어선들(E1 내지 En)을 구동하기 위한 발광제어선 구동부(30)와, 구동부들(10, 20, 30)을 제어하기 위한 타이밍 제어부(60)를 구비한다.
- [0024] 주사 구동부(10)는 주사선들(S1 내지 Sn)로 주사신호를 순차적으로 공급한다. 주사선들(S1 내지 Sn)로 주사신호가 공급되면 화소들(50)이 수평라인 단위로 선택된다.
- [0025] 데이터 구동부(20)는 주사신호에 동기되도록 데이터선들(D1 내지 Dm)로 데이터신호를 공급한다. 데이터선들(D1 내지 Dm)로 공급된 데이터신호는 주사신호에 의하여 선택된 화소들(50)로 공급된다.
- [0026] 발광제어선 구동부(30)는 발광 제어선들(E1 내지 En)로 발광 제어신호를 순차적으로 공급한다. 여기서, 발광제어선 구동부(30)는 데이터신호에 대응하는 기간을 충전하는 기간 동안 화소들(50)이 비발광 상태로 설정되도록 발광 제어신호를 공급한다. 이를 위하여, i (i 는 자연수)번째 발광 제어선(E i)으로 공급되는 발광 제어신호는 i 번째 주사선(S i)으로 공급되는 주사신호와 중첩된다. 한편, 발광 제어신호의 폭은 화소(50)의 구조, 구현하고자 하는 휘도 등에 대응하여 자유롭게 설정될 수 있다.
- [0027] 도 2는 도 1에 도시된 발광제어선 구동부의 스테이지를 개략적으로 나타내는 도면이다.
- [0028] 도 2를 참조하면, 본 발명의 발광제어선 구동부(30)는 n 개의 발광 제어선(E1 내지 En)으로 발광 제어신호를 공급하기 위하여 n 개의 스테이지(321 내지 32n)를 구비한다. 스테이지(321 내지 32n) 각각은 발광 제어선(E1 내지 En)에 접속되며, 2개의 클럭신호(CLK1 내지 CLK2)에 의하여 구동된다.
- [0029] 스테이지(321 내지 32n) 각각은 제 1입력단자(33), 제 2입력단자(34), 제 3입력단자(35), 제 4입력단자(36) 및 제 1출력단자(37)를 구비한다.
- [0030] k (k 는 홀수 또는 짝수)번째 스테이지(32k)에 포함된 제 1입력단자(33)는 제 1클럭신호(CLK1)를 공급받고, 제 2입력단자(34)는 제 2클럭신호(CLK2)를 공급받는다. 그리고, $k+1$ 번째 스테이지(32k+1)에 포함된 제 1입력단자(33)는 제 2클럭신호(CLK2)를 공급받고, 제 2입력단자(34)는 제 1클럭신호(CLK1)를 공급받는다. 스테이지(321 내지 32n) 각각에 포함된 제 3입력단자(35)는 이전단 스테이지의 샘플링신호(또는 시작신호)를 공급받고, 제 4입력단자(36)는 다음단 스테이지의 샘플링신호(또는 시작신호)를 공급받는다. 그리고, 스테이지(321 내지 32n) 각각에 포함된 제 1출력단자(37)는 발광 제어선들(E1 내지 En 중 어느 하나)과 접속되고, 발광 제어선들(E1 내지 En 중 어느 하나)로 발광 제어신호를 출력한다.
- [0031] 이와 같은 스테이지들(321 내지 32n)은 동일한 회로로 구성되며, 시작신호(FLM)에 대응하여 폭이 변화되는 발광 제어신호를 생성한다.
- [0032] 도 3은 도 2에 도시된 스테이지의 제 1실시예를 나타내는 회로도이다. 도 3에서는 설명의 편의성을 위하여 제 1스테이지(321)를 도시하기로 한다.
- [0033] 도 3을 참조하면, 본 발명의 제 1실시예에 의한 스테이지(321)는 출력부(100), 제 1구동부(102), 제 2구동부

(104) 및 양방향 구동부(106)를 구비한다.

- [0034] 출력부(100)는 제 1노드(N1) 및 제 2노드(N2)에 인가되는 전압에 대응하여 제 1출력단자(37)로 제 1전원(VDD) 또는 제 1전원(VDD)보다 낮은 전압으로 설정되는 제 2전원(VSS)을 출력한다. 이를 위하여, 출력부(100)는 제 1트랜지스터(M1), 제 2트랜지스터(M2) 및 제 1캐패시터(C1)를 구비한다.
- [0035] 제 1트랜지스터(M1)는 제 1전원(VDD)과 제 1출력단자(37) 사이에 접속된다. 그리고, 제 1트랜지스터(M1)의 게이트전극은 제 1노드(N1)에 접속된다. 이와 같은 제 1트랜지스터(M1)는 제 1노드(N1)의 전압에 대응하여 제 1출력단자(37)로 제 1전원(VDD)의 전압을 공급한다. 제 1출력단자(37)로 공급되는 제 1전원(VDD)의 전압은 발광 제어신호로서 별광 제어신(E1)으로 공급된다.
- [0036] 제 2트랜지스터(M2)는 제 1출력단자(37)와 제 2전원(VSS) 사이에 접속된다. 그리고, 제 2트랜지스터(M2)의 게이트전극은 제 2노드(N2)에 접속된다. 이와 같은 제 2트랜지스터(M2)는 제 2노드(N2)의 전압에 대응하여 제 1출력단자(37)로 제 2전원(VSS)의 전압을 공급한다.
- [0037] 제 1캐패시터(C1)는 제 1전원(VDD)과 제 1출력단자(37) 사이에 접속된다. 이와 같은 제 1캐패시터(C1)는 제 1전원(VDD)의 전압을 기준으로 제 1출력단자(37)의 전압을 안정화한다.
- [0038] 제 1구동부(102)는 제 1클럭신호(CLK1), 제 2클럭신호(CLK2) 및 양방향 구동부(106)로부터 공급되는 전압에 대응하여 제 1노드(N1) 및 제 2노드(N2)의 전압을 제어한다. 이를 위하여, 제 1구동부(102)는 제 3트랜지스터(M3), 제 4트랜지스터(M4), 제 5트랜지스터(M5), 제 2캐패시터(C2) 및 제 3캐패시터(C3)를 구비한다.
- [0039] 제 3트랜지스터(M3)는 제 1전원(VDD)과 제 2노드(N2) 사이에 접속된다. 그리고, 제 3트랜지스터(M3)의 게이트전극은 제 1노드(N1)에 접속된다. 이와 같은 제 3트랜지스터(M3)는 제 1노드(N1)의 전압에 대응하여 제 1전원(VDD)의 전압을 제 2노드(N2)로 공급한다.
- [0040] 제 4트랜지스터(M4)는 제 2노드(N2)와 제 2전원(VSS) 사이에 접속된다. 그리고, 제 4트랜지스터(M4)의 게이트전극은 제 1입력단자(33)에 접속된다. 이와 같은 제 4트랜지스터(M4)는 제 1입력단자(33)로 공급되는 제 1클럭신호(CLK1)에 대응하여 턴-온 또는 턴-오프된다.
- [0041] 제 5트랜지스터(M5)는 양방향 구동부(106)와 제 1노드(N1) 사이에 접속된다. 그리고, 제 5트랜지스터(M5)의 게이트전극은 제 1입력단자(33)에 접속된다. 이와 같은 제 5트랜지스터(M5)는 제 1입력단자(33)로 공급되는 제 1클럭신호(CLK1)에 대응하여 턴-온 또는 턴-오프된다.
- [0042] 제 2캐패시터(C2)는 제 1노드(N1)와 제 1전원(VDD) 사이에 접속된다. 이와 같은 제 2캐패시터(C2)는 제 1노드(N1)에 인가된 전압을 저장한다.
- [0043] 제 3캐패시터(C3)는 제 2노드(N2)와 제 2입력단자(34) 사이에 접속된다. 이와 같은 제 3캐패시터(C3)는 제 2입력단자(34)로 공급되는 제 2클럭신호(CLK2)에 대응하여 제 2노드(N2)의 전압을 제어한다. 이와 같은 제 3캐패시터(C3)의 상세한 동작과정을 후술하기로 한다.
- [0044] 제 2구동부(104)는 제 1클럭신호(CLK1), 제 2클럭신호(CLK2) 및 양방향 구동부(106)로부터 공급되는 전압에 대응하여 제 2출력단자(38)로 앰플리팅신호를 출력한다. 이를 위하여, 제 2구동부(104)는 제 6트랜지스터(M6), 제 7트랜지스터(M7), 제 8트랜지스터(M8) 및 제 4캐패시터(C4)를 구비한다.
- [0045] 제 6트랜지스터(M6)는 제 1전원(VDD)과 제 2출력단자(38) 사이에 접속된다. 그리고, 제 6트랜지스터(M6)의 게이트전극은 제 1출력단자(37)에 접속된다. 이와 같은 제 6트랜지스터(M6)는 제 1출력단자(37)에 인가되는 전압에 대응하여 턴-온 또는 턴-오프된다. 실제로, 제 6트랜지스터(M6)는 제 1출력단자(37)로 발광 제어신호가 공급되는 기간 동안 턴-오프되고, 그 외의 기간 동안 턴-온된다.
- [0046] 제 7트랜지스터(M7)는 제 2출력단자(38)와 제 2입력단자(34) 사이에 접속된다. 그리고, 제 7트랜지스터(M7)의 게이트전극은 제 3노드(N3)에 접속된다. 이와 같은 제 7트랜지스터(M7)는 제 3노드(N3)로 공급되는 전압에 대응하여 턴-온 또는 턴-오프된다.
- [0047] 제 8트랜지스터(M8)는 양방향 구동부(106)와 제 3노드(N3) 사이에 접속된다. 그리고, 제 8트랜지스터(M8)의 게이트전극은 제 1입력단자(33)에 접속된다. 이와 같은 제 8트랜지스터(M8)는 제 1입력단자(33)로 공급되는 제 1클럭신호(CLK1)에 대응하여 턴-온 또는 턴-오프된다.
- [0048] 양방향 구동부(106)는 제 3입력단자(35) 및 제 4입력단자(36)와 접속된다. 이와 같은 양방향 구동부(106)는 제

1제어신호(CS1) 또는 제 2제어신호(CS2)에 대응하여 제 3입력단자(35)로 입력되는 이전단 스테이지의 샘플링신호(SRn-1, 첫번째 스테이지(321)에서는 시작신호(FLM)) 또는 다음단 스테이지의 샘플링신호(SRn+1)를 제 1구동부(102) 및 제 2구동부(104)로 공급한다.

[0049] 이를 위하여, 양방향 구동부(106)는 제 9트랜지스터(M9) 및 제 10트랜지스터(M10)를 구비한다. 제 9트랜지스터(M9)는 제 3입력단자(35)와 제 4노드(N4) 사이에 접속된다. 그리고, 제 9트랜지스터(M9)의 게이트전극은 제 1제어신호(CS1)를 공급받는다. 이와 같은 제 9트랜지스터(M9)는 제 1제어신호(CS1)가 입력될 때 턴-온되어 제 4노드(N4)와 제 3입력단자(35)를 전기적으로 접속시킨다.

[0050] 제 10트랜지스터(M10)는 제 4입력단자(36)와 제 4노드(N4) 사이에 접속된다. 그리고, 제 10트랜지스터(M10)의 게이트전극은 제 2제어신호(CS2)를 공급받는다. 이와 같은 제 10트랜지스터(M10)는 제 2제어신호(CS2)가 입력될 때 턴-온되어 제 4노드(N4)와 제 4입력단자(36)를 전기적으로 접속시킨다.

[0051] 한편, 제 1제어신호(CS1) 및 제 2제어신호(CS2)는 타이밍 제어부(60)(또는 별도의 구동부)로부터 서로 중첩되지 않도록 공급된다. 제 1제어신호(CS1)가 공급되는 경우 스테이지들(321 내지 32n)은 제 1방향(321로부터 32n으로)으로 발광 제어신호를 순차적으로 공급하고, 제 2제어신호(CS2)가 공급되는 경우 스테이지들(321 내지 32n)은 제 2방향(32n으로부터 321로)으로 발광 제어신호를 순차적으로 공급한다.

[0052] 도 4는 도 3에 도시된 스테이지의 구동방법을 나타내는 도면이다. 설명의 편의성을 위하여 도 4에서는 제 1스테이지(321)로 시작신호(FLM)가 공급되는 경우를 도시하기로 한다.

[0053] 도 4를 참조하면, 제 1클럭신호(CLK1) 및 제 2클럭신호(CLK2)는 동일한 주기를 가지며, 서로 다른 수평기간에 공급된다. 그리고, 시작신호(FLM)는 소정의 폭, 즉 제 1클럭신호(CLK1)와 적어도 한번 이상 중첩되도록 공급된다.

[0054] 동작과정을 상세히 설명하면, 먼저 제 1제어신호(CS1)에 의하여 제 9트랜지스터(M9)가 턴-온된다. 제 9트랜지스터(M9)가 턴-온된 이후에 제 3입력단자(35)로 시작신호(FLM, 로우신호)가 공급된다.

[0055] 제 3입력단자(35)로 공급된 시작신호는 제 9트랜지스터(M9)를 경유하여 제 4노드(N4)로 공급된다. 이후, 제 1입력단자(33)로 제 1클럭신호(CLK1)가 공급된다. 제 1클럭신호(CLK1)가 공급되면 제 4트랜지스터(M4), 제 5트랜지스터(M5) 및 제 8트랜지스터(M8)가 턴-온된다.

[0056] 제 5트랜지스터(M5)가 턴-온되면 제 1노드(N1)로 시작신호(FLM)가 공급된다. 제 1노드(N1)로 시작신호(FLM)가 공급되면 제 1트랜지스터(M1) 및 제 3트랜지스터(M3)가 턴-온된다. 제 1트랜지스터(M1)가 턴-온되면 제 1출력단자(37)로 제 1전원(VDD)의 전압, 즉 발광 제어신호가 공급된다. 이때, 제 1노드(N1)의 전압은 제 2커패시터(C2)에 충전된다.

[0057] 제 3트랜지스터(M3)가 턴-온되면 제 2노드(N2)와 제 1전원(VDD)이 전기적으로 접속된다. 그리고, 제 1클럭신호(CLK1)에 의하여 제 4트랜지스터(M4)가 턴-온되면 제 2노드(N2)와 제 2전원(VSS)이 전기적으로 접속된다. 이 경우, 제 1전원(VDD), 제 3트랜지스터(M3), 제 4트랜지스터(M4) 및 제 2전원(VSS)이 전기적으로 접속된다.

[0058] 여기서, 제 3트랜지스터(M3) 및 제 4트랜지스터(M4)가 동일한 저항값으로 설정된다고 가정하면 제 2노드(N2)에는 대략 제 1전원(VDD)의 절반에 대응하는 전압이 인가되고, 이에 따라 제 2트랜지스터(M2)는 턴-오프 상태로 설정된다. 추가적으로, 본원 발명에서는 제 3트랜지스터(M3)가 제 4트랜지스터(M4)보다 낮은 저항(예를 들면, 채널비 조정, 다수 트랜지스터 병렬연결 등)을 갖도록 형성될 수 있다. 이 경우, 제 2노드(N2)에 인가되는 전압이 상승되어 제 2트랜지스터(M2)가 보다 안정적으로 턴-오프될 수 있다.

[0059] 제 8트랜지스터(M8)가 턴-온되면 제 3노드(N3)로 시작신호(FLM)가 공급된다. 제 3노드(N3)로 시작신호(FLM)가 공급되면 제 7트랜지스터(M7)가 턴-온된다. 제 7트랜지스터(M7)가 턴-온되면 제 2입력단자(34)와 제 2출력단자(38)가 전기적으로 접속된다. 이때, 제 2출력단자(38)로 제 2클럭신호(CLK2)가 공급되지 않기 때문에 제 2출력단자(38)로는 하이전압이 공급된다. 그리고, 제 7트랜지스터(M7)가 턴-온될 때 제 4커패시터(C4)에는 제 7트랜지스터(M7)의 턴-온에 대응하는 전압이 충전된다.

[0060] 이후, 제 1클럭신호(CLK1)의 공급이 중단되어 제 4트랜지스터(M4), 제 5트랜지스터(M5) 및 제 8트랜지스터(M8)가 턴-오프된다. 이때, 제 2커패시터(C2)에 충전된 전압에 대응하여 제 1트랜지스터(M1) 및 제 3트랜지스터(M3)가 턴-온 상태를 유지한다. 제 1트랜지스터(M1)가 턴-온되면 제 1출력단자(37)로 제 1전원(VDD)의 전압이

공급된다. 제 3트랜지스터(M3)가 턴-온되면 제 2노드(N2)로 제 1전원(VDD)의 전압이 공급되어 제 2트랜지스터(M2)가 턴-오프 상태로 설정된다. 그리고, 제 8트랜지스터(M8)가 턴-오프되더라도 제 4캐패시터(C4)에 충전된 전압에 대응하여 제 7트랜지스터(M7)는 턴-온 상태를 유지한다.

- [0061] 이후, 제 2입력단자(34)로 제 2클럭신호(CLK2)(즉, 로우신호)가 공급된다. 제 2입력단자(34)로 제 2클럭신호(CLK2)가 공급되면 제 7트랜지스터(M7)를 경유하여 제 2출력단자(38)로 제 2클럭신호(CLK2)가 공급된다. 제 2출력단자(38)로 공급된 제 2클럭신호(CLK2)는 샘플링신호(SR)로서 다음단 및 이전단 스테이지로 공급된다.
- [0062] 그리고, 제 2입력단자(34)로 공급된 제 2클럭신호(CLK2)는 제 3캐패시터(C3)의 제 1단자로 공급된다. 이때, 제 2노드(N2)는 제 1전원(VDD)과 전기적으로 접속되기 때문에 제 2노드(N2)의 전압은 제 2클럭신호(CLK2)와 무관하게 제 1전원(VDD)의 전압을 유지한다.
- [0063] 이후, 시작신호(FLM)의 공급이 중단됨과 아울러 제 1입력단자(33)로 제 1클럭신호(CLK1)가 공급된다. 제 1클럭신호(CLK1)가 공급되면 제 4트랜지스터(M4), 제 5트랜지스터(M5) 및 제 8트랜지스터(M8)가 턴-온된다.
- [0064] 제 5트랜지스터(M5)가 턴-온되면 제 1노드(N1)로 하이전압이 공급된다. 제 1노드(N1)로 하이전압이 공급되면 제 1트랜지스터(M1) 및 제 3트랜지스터(M3)가 턴-오프된다.
- [0065] 제 4트랜지스터(M4)가 턴-온되면 제 2노드(N2)로 제 2전원(VSS)이 공급된다. 제 2노드(N2)로 제 2전원(VSS)이 공급되면 제 2트랜지스터(M2)가 턴-온된다. 제 2트랜지스터(M2)가 턴-온되면 제 1출력단자(37)로 제 2전원(VSS)의 전압이 공급된다. 제 1출력단자(37)로 제 2전원(VSS)의 전압이 공급되면 제 6트랜지스터(M6)가 턴-온된다. 제 6트랜지스터(M6)가 턴-온되면 제 2출력단자(38)로 제 1전원(VDD)의 전압이 공급된다.
- [0066] 제 8트랜지스터(M8)가 턴-온되면 제 3노드(N3)로 하이전압이 공급된다. 제 3노드(N3)로 하이전압이 공급되면 제 7트랜지스터(M7)가 턴-오프된다. 이때, 제 4캐패시터(C4)는 제 7트랜지스터(M7)의 턴-오프에 대응하는 전압을 충전한다.
- [0067] 제 1클럭신호(CLK1)가 공급된 이후 다음 수평기간에 제 2클럭신호(CLK2)가 공급된다. 이때, 제 7트랜지스터(M7)가 턴-오프 상태로 설정되기 때문에 제 2클럭신호(CLK2)는 제 2출력단자(38)로 공급되지 않는다. 추가적으로, 제 2입력단자(34)로 공급된 제 2클럭신호(CLK2)는 제 3캐패시터(C3)의 커패시턴스에 의하여 제 2노드(N2)로 전달된다.
- [0068] 그러면, 제 2노드(N2)의 전압은 제 2전원(VSS)보다 낮은 전압으로 하강된다. 이 경우, 제 1출력단자(37)로는 보다 낮은 전압(VSS)이 공급될 수 있다. 상세히 설명하면, 제 2노드(N2)로 제 2전원(VSS)이 공급되는 경우 제 2트랜지스터(M2)의 게이트전압과 제 2전극의 전압이 동일하게 설정된다. 이 경우, 제 1출력단자(37)의 전압은 제 2전원(VSS)의 전압에서 제 2트랜지스터(M2)의 문턱전압을 합한 전압으로 설정된다.
- [0069] 한편, 제 3캐패시터(C3)의 커패시턴스에 의하여 제 2노드(N2)의 전압이 제 2전원(VSS)보다 낮은 전압으로 하강되는 경우 제 1출력단자(37)로 제 2전원(VSS)의 전압이 출력되고, 이에 따라 출력의 안정성을 확보할 수 있다. 그리고, 제 2노드(N2)의 전압은 제 2클럭신호(CLK2)가 공급될 때 마다 하강되기 때문에 제 2노드(N2)의 전압은 안정적으로 로우전압으로 유지되고, 이에 따라 제 1출력단자(37)로 제 2전원(VSS)의 전압을 안정적으로 출력할 수 있다.
- [0070] 한편, 샘플링신호(SR)는 제 2클럭신호(CLK2)와 동기되도록 다음단 스테이지 또는 이전단 스테이지로 공급된다. (다음단 및 이전단 스테이지는 제 1입력단자로 제 2클럭신호(CLK2)가 공급된다.) 이 경우, 다음단 스테이지는 샘플링신호를 이용하여 안정적으로 발광 제어신호를 출력한다.
- [0071] 추가적으로 도 4에는 시작신호(FLM)에 대응하여 하나의 샘플링신호가 생성되는 것으로 도시되었지만 본원 발명이 이에 한정되지는 않는다. 예를 들어, 시작신호(FLM)가 2개의 제 1클럭신호(CLK1)와 중첩되는 경우 2개의 샘플링신호가 다음단 및 이전단 스테이지로 공급된다. 즉, 본원 발명에서는 시작신호(FLM)의 폭을 제어함으로써 발광 제어신호의 폭을 자유롭게 조절할 수 있다.
- [0072] 도 5는 도 3에 도시된 스테이지 회로의 시뮬레이션 결과를 나타내는 도면이다.
- [0073] 도 5를 참조하면, 제 1클럭신호(CLK1) 및 제 2클럭신호(CLK2)를 교번적으로 공급하면서 시작신호(FLM)의 폭을 다양하게 설정하는 경우 제 1출력단자(37)(즉 발광 제어신(E1))로 공급되는 발광 제어신호는 시작신호(FLM)의 폭에 대응하여 변화된다. 즉, 본원 발명의 스테이지 회로는 시작신호(FLM)의 폭에 대응하여 발광 제어신호의

폭이 안정적으로 변화된다.

- [0074] 도 6은 도 2에 도시된 스테이지의 제 2실시예를 나타내는 회로도이다. 도 6을 설명할 때 도 3과 동일한 구성에 대해서는 동일한 도면부호를 할당함과 아울러 상세한 설명은 생략하기로 한다.
- [0075] 도 6을 참조하면, 본 발명의 제 2실시예에 의한 스테이지(321)는 제 1노드(N1)와 제 2전원(VSS) 사이에 접속되는 제 11트랜지스터(M11)를 더 구비한다. 제 11트랜지스터(M11)의 게이트전극은 제 5입력단자(39)에 접속된다. 제 5입력단자(39)는 타이밍 제어부(60)로부터 리셋신호(Reset)를 공급받는다.
- [0076] 동작과정을 설명하면, 전원의 온 및/또는 오프시에 타이밍 제어부(60)는 제 5입력단자(39)로 리셋신호(Reset)를 공급한다. 제 5입력단자(39)로 리셋신호(Reset)가 공급되면 제 11트랜지스터(M11)가 턴-온된다. 제 11트랜지스터(M11)가 턴-온되면 제 1노드(N1)로 제 2전원(VSS)의 전압이 공급된다.
- [0077] 제 1노드(N1)로 제 2전원(VSS)이 공급되면 제 1트랜지스터(M1) 및 제 3트랜지스터(M3)가 턴-온된다. 제 1트랜지스터(M1)가 턴-온되면 제 1출력단자(37)로 제 1전원(VDD)의 전압이 출력된다. 제 3트랜지스터(M3)가 턴-온되면 제 2노드(N2)로 제 1전원(VDD)이 공급된다. 제 2노드(N2)로 제 1전원(VDD)이 공급되면 제 2트랜지스터(M2)가 턴-오프되고, 이에 따라 제 1출력단자(37)로 제 1전원(VDD)의 전압을 안정적으로 공급할 수 있다.
- [0078] 상술한 바와 같이 제 11트랜지스터(M11)는 전원의 온 및/또는 오프시에 턴-온된다. 그러면, 전원의 온 및/또는 오프시에 파소들(50)이 강제적으로 오프상태로 설정되고, 이에 따라 과전류가 흐르는 것을 방지할 수 있다.
- [0079] 도 7은 도 3에 도시된 스테이지 회로의 양방향 구동을 나타내는 도면이다.
- [0080] 도 7을 참조하면, 발광 제어선들(E1 내지 E4)은 제 1방향 및 제 2방향으로 발광 제어신호를 순차적으로 공급한다. 즉, 본원 발명에서는 스테이지들(321 내지 32n)을 이용하여 안정적으로 제 1방향 및 제 2방향으로 발광 제어신호를 공급할 수 있고, 이에 따라 다양한 구동방법에 적용 가능한 장점이 있다.
- [0081] 도 8은 도 2에 도시된 스테이지의 제 3실시예를 나타내는 회로도이다. 도 8을 설명할 때 도 3과 동일한 구성에 대해서는 동일한 도면부호를 할당함과 아울러 상세한 설명은 생략하기로 한다.
- [0082] 도 8을 참조하면, 본 발명의 제 3실시예에 의한 스테이지(321)는 제 3캐패시터(C3)와 제 2입력단자(34) 사이에 접속되는 제 12트랜지스터(M12)를 더 구비한다. 제 12트랜지스터(M12)의 게이트전극은 제 2노드(N2)에 접속된다. 이와 같은 제 12트랜지스터(M12)는 제 2노드(N2)에 로우전압(예를 들면, 제 2전원(VSS), 샘플링신호 또는 시작신호)이 공급될 때 턴-온되고, 하이전압(예를 들면, 제 1전원(VDD))이 공급될 때 턴-오프된다.
- [0083] 즉, 제 12트랜지스터(M12)는 제 2노드(N2)로 하이전압이 공급될 때 턴-오프되어 제 2클럭신호(CLK2)에 대응하여 제 2노드(N2)의 전압이 변화되는 것을 방지한다. 그리고, 제 12트랜지스터(M12)는 제 2노드(N2)로 로우전압이 공급될 때 턴-온되어 제 2클럭신호(CLK2)에 대응하여 제 2노드(N2)의 전압이 낮아지도록 한다. 그 외의 동작은 도 3과 동일하므로 상세한 설명은 생략하기로 한다.
- [0084] 한편, 본원 발명에서 도 6에 도시된 제 11트랜지스터(M11)는 도 9와 같이 도 8에 도시된 스테이지 회로에 추가로 포함될 수 있다. 이 경우, 전원의 온 및/또는 오프시에 제 11트랜지스터(M11)를 턴-온 상태로 설정하여 패셀에 과전류가 흐르는 것을 방지할 수 있다.
- [0085] 도 10은 도 8에 도시된 스테이지 회로의 시뮬레이션 결과를 나타내는 도면이다.
- [0086] 도 10을 참조하면, 제 1클럭신호(CLK1) 및 제 2클럭신호(CLK2)를 교번적으로 공급하면서 시작신호(FLM)의 폭을 다양하게 설정하는 경우 제 1출력단자(37)(즉 발광 제어선(E1))로 공급되는 발광 제어신호는 시작신호(FLM)의 폭에 대응하여 변화된다. 즉, 본원 발명의 스테이지 회로는 시작신호(FLM)의 폭에 대응하여 발광 제어신호의 폭이 안정적으로 변화된다.
- [0087] 본 발명의 기술 사상을 상기 바람직한 실시예에 따라 구체적으로 기술하였으나, 상기한 실시예는 그 설명을 위한 것이며 그 제한을 위한 것이 아님을 주의하여야 한다. 또한, 본 발명의 기술 분야의 통상의 지식을 가진 자

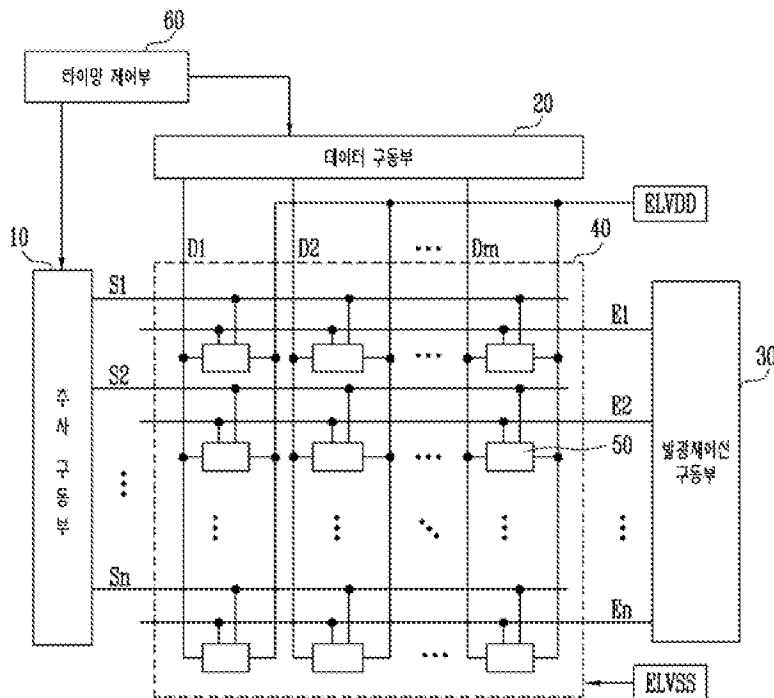
라면 본 발명의 기술 사상의 범위 내에서 다양한 변형예가 가능함을 이해할 수 있을 것이다.

부호의 설명

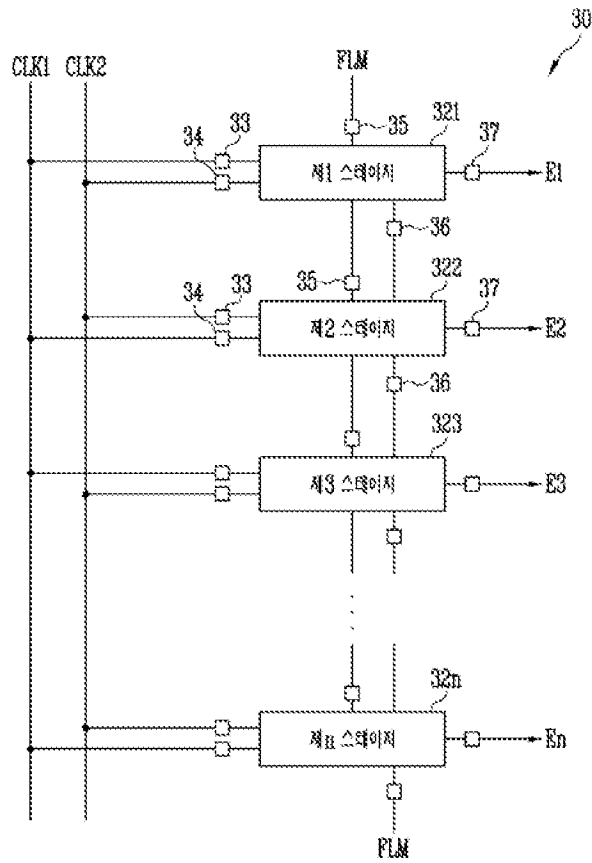
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	30 : 발광 제어신 구동부	33,34,35,36 : 입력단자
	37,38 : 출력단자	40 : 화소부
	50 : 화소	60 : 타이밍 제어부
	100 : 출력부	102,104 : 구동부
	106 : 양방향 구동부	321,322,323,326 : 스테이지

도면

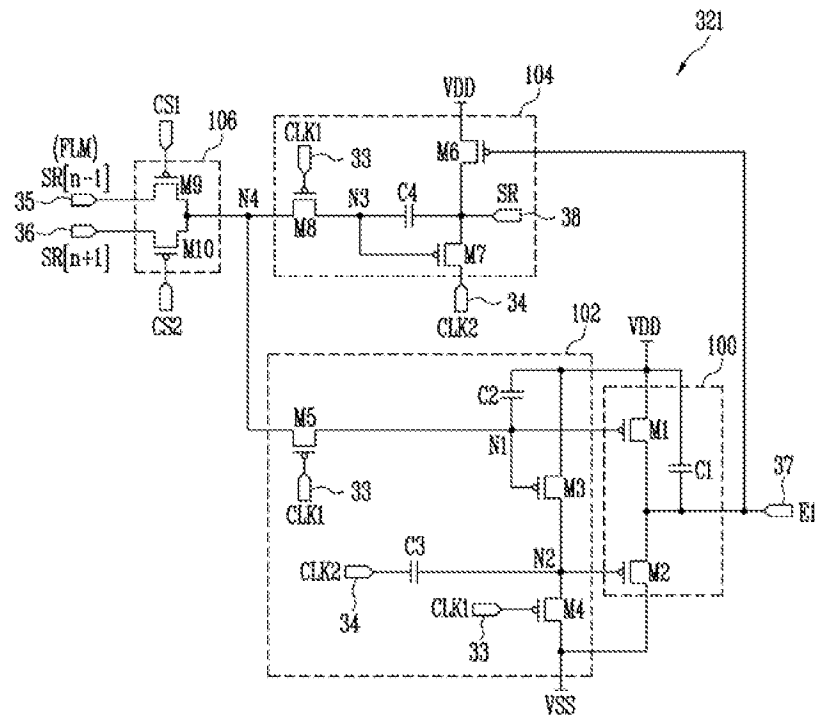
도면1



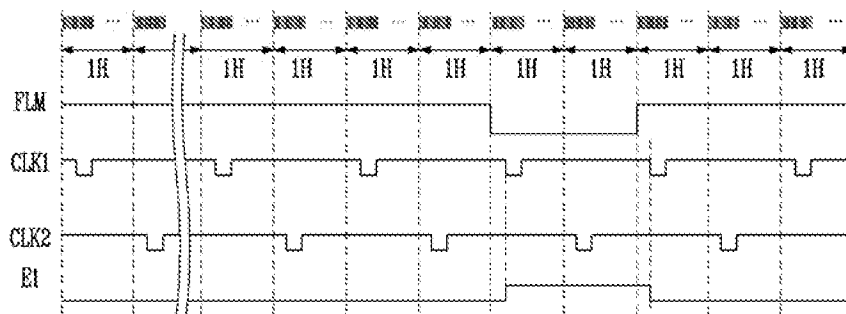
도면2



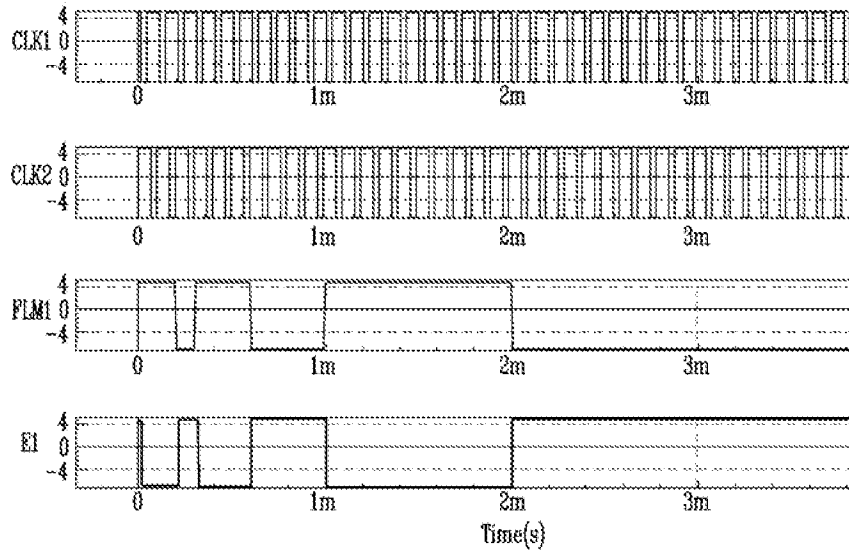
559



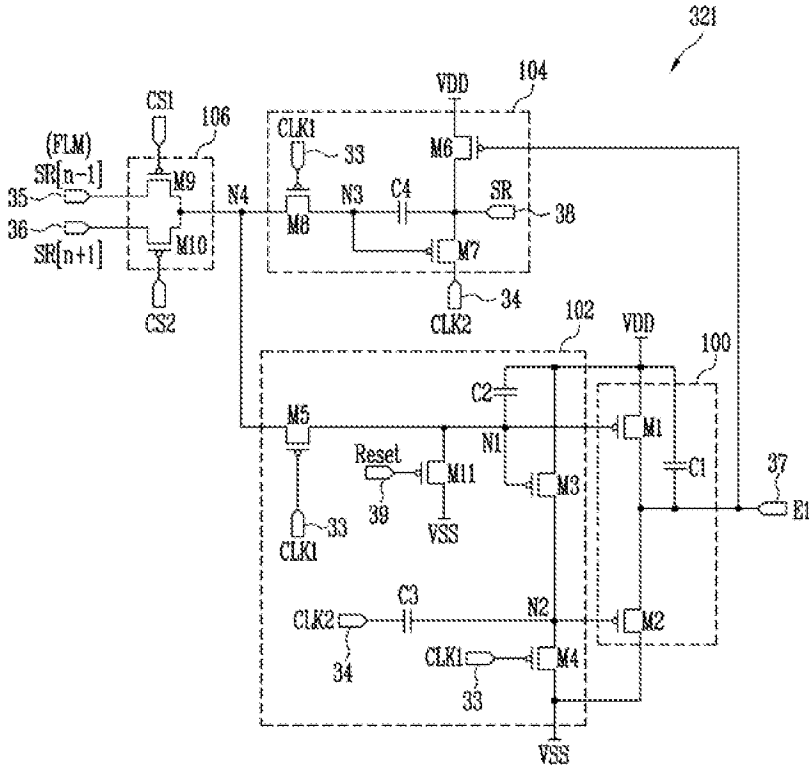
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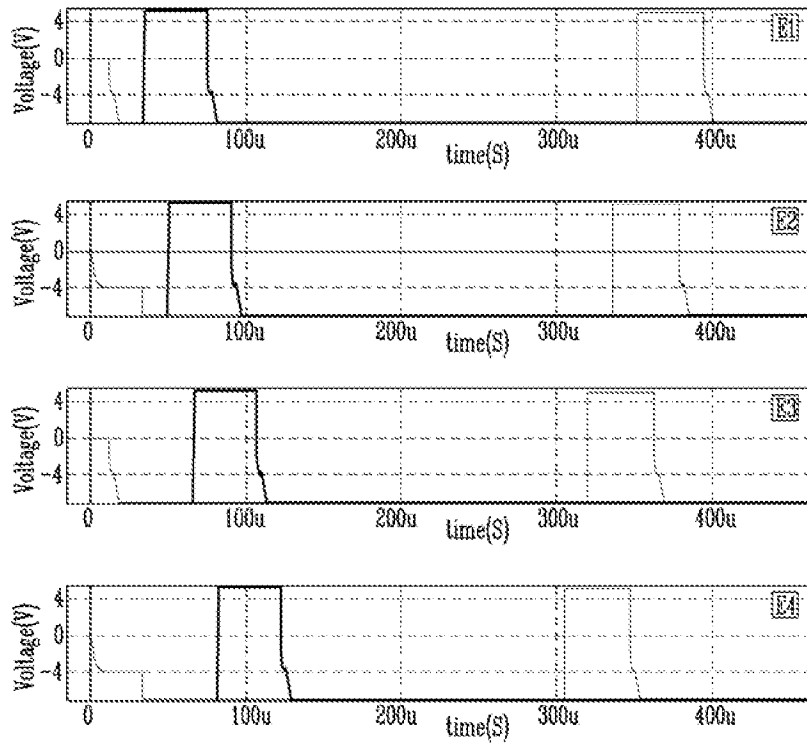
도면5



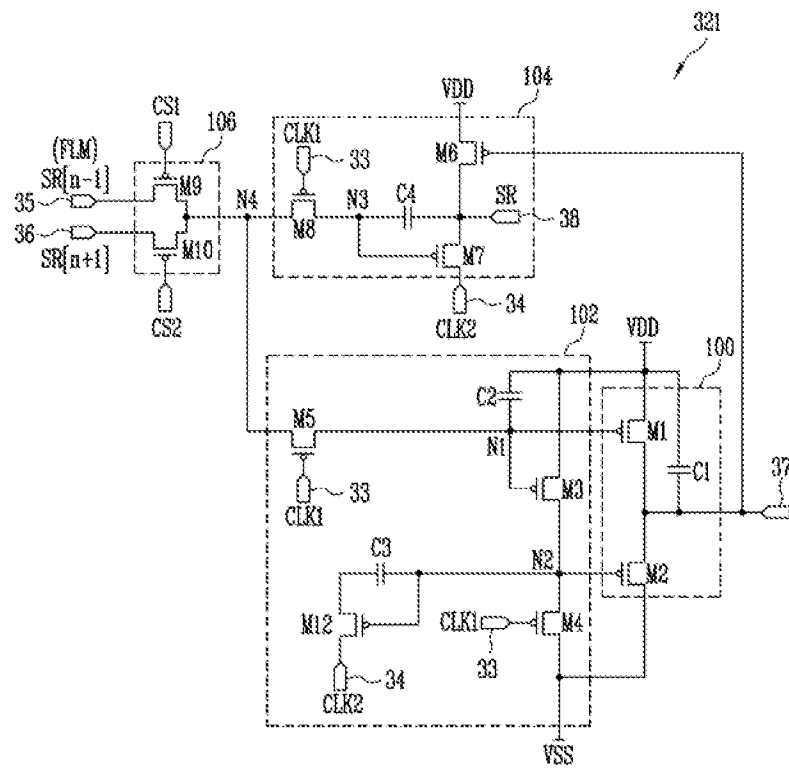
도면6



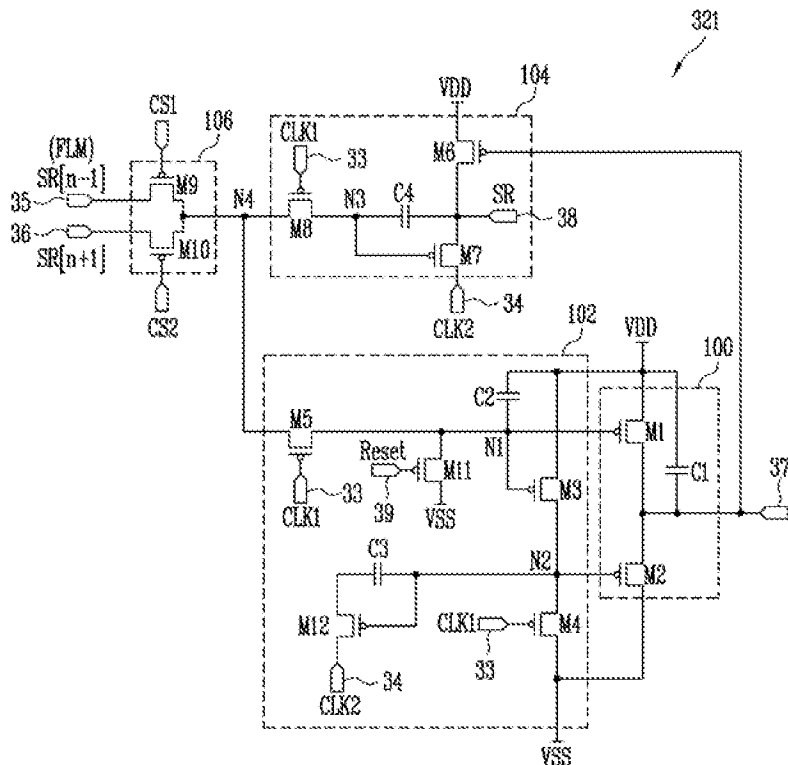
도면7



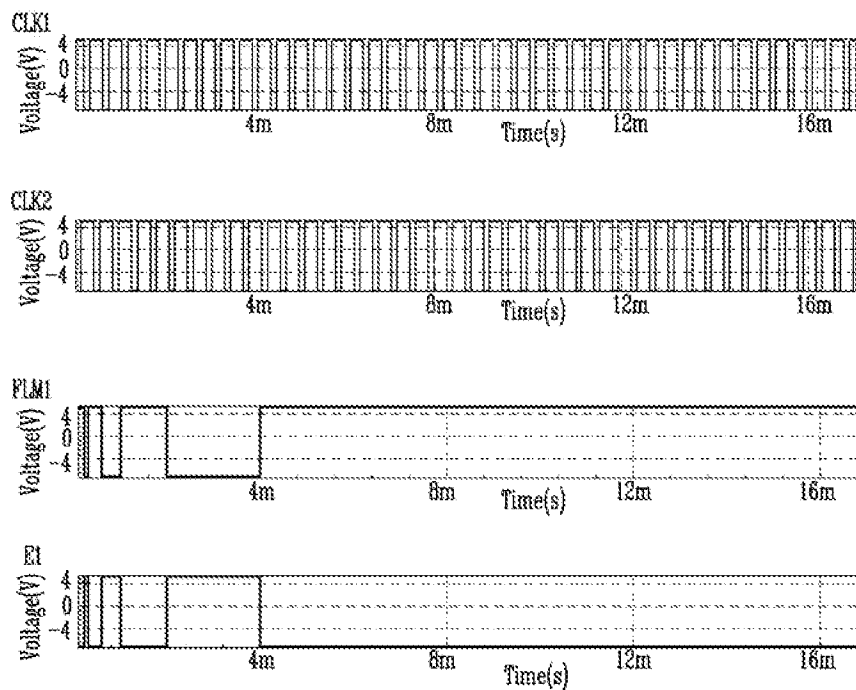
도면8



500



580



Electronic Acknowledgement Receipt

EFS ID:	21020464
Application Number:	13771385
International Application Number:	
Confirmation Number:	3091
Title of Invention:	STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME
First Named Inventor/Applicant Name:	Hwan-Soo JANG
Customer Number:	27849
Filer:	Susan S. Morse/Jana Robbins
Filer Authorized By:	Susan S. Morse
Attorney Docket Number:	304/1043
Receipt Date:	19-DEC-2014
Filing Date:	20-FEB-2013
Time Stamp:	15:26:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		A01_2014_12_19_IDS_ELEC_R esponse_as_filed.pdf	223441 db6496d54341c14fbc11753ca3ce1c67fbc636b	yes	5

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Response to Election / Restriction Filed		1	1	
	Transmittal Letter		2	4	
	Information Disclosure Statement (IDS) Form (SB08)		5	5	
Warnings:					
Information:					
2	Foreign Reference	KR1020130000020A.pdf	5507862	no	19
			1047c23df21cbce23da8db10e6a2ce60cdfa b999		
Warnings:					
Information:					
Total Files Size (in bytes):			5731303		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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13/771,385

02/20/2013

Hwan-Soo JANG

304/1043

3091

27849 7590 10/21/2014
LEE & MORSE, P.C.
3141 FAIRVIEW PARK DRIVE
SUITE 500
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EXAMINER

KIRKPATRICK, JOHN

ART UNIT

PAPER NUMBER

2691

NOTIFICATION DATE

DELIVERY MODE

10/21/2014

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

coa@lee-iplaw.com
swerbow@lee-iplaw.com

Office Action Summary	Application No. 13/771,385	Applicant(s) JANG, HWAN-SOO	
	Examiner JOHN KIRKPATRICK	Art Unit 2691	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 2/20/2013.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-26 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☐ Claim(s) ____ is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☒ Claim(s) 1-26 are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☐ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date ____. | 4) ☐ Other: ____. |

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

Election/Restrictions

2. This application contains claims directed to the following patentably distinct species:

A. Species of Fig. 3 showing a seventh transistor M7 positioned between the first node N1 and a second power supply VSS.

B. Species of Fig. 6 showing a seventh transistor M7' diode-connected between the first node N1 and the second input terminal 102.

C. Species of Fig. 7 showing a bidirectional driver 240.

3. The species are independent or distinct because (1) the species as claimed are either not capable of use together or can have a materially different design, mode of operation, function, or effect; and (2) the species do not overlap in scope, i.e., are mutually exclusive. In addition, these species are not obvious variants of each other based on the current record.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species, or a single grouping of patentably indistinct species, for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable.

Currently, claims 1 and 14 are generic.

There is a search and/or examination burden for the patentably distinct species as set forth above because at least the following reason(s) apply: a different field of search (e.g., different search queries) is required.

4. **Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species or a grouping of patentably indistinct species to be examined** even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected species or grouping of patentably indistinct species**, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

The election may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the election of species requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected species or grouping of patentably indistinct species.

Should applicant traverse on the ground that the species, or groupings of patentably indistinct species from which election is required, are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing them

to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other species.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN C. KIRKPATRICK whose telephone number is (571) 270-3343. The examiner can normally be reached on 9:00 am - 5:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh D. Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic

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Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JOHN C. KIRKPATRICK/
Patent Examiner, Art Unit 2691



별첨 사본은 아래 출원의 원본과 동일함을 증명함.

This is to certify that the following application annexed hereto
is a true copy from the records of the Korean Intellectual
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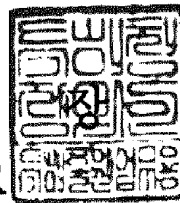
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출 원 인 : 삼성디스플레이 주식회사
Applicant(s) Samsung Display Co., Ltd.

2014년 04월 23일

특 허 청
COMMISSIONER



제출 일자 : 2012-09-20

【서지사항】

【서류명】 특허출원서
【출원구분】 특허출원
【출원인】
【명칭】 삼성디스플레이 주식회사
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【포괄위임등록번호】 2012-058000-4
【발명의 국문명칭】 스테이지 회로 및 이를 이용한 유기전계발광 표시장치
【발명의 영문명칭】 Stage Circuit and Organic Light Emitting Display Device
Using the same
【발명자】
【성명】 장환수
【성명의 영문표기】 HWANSOO JANG
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【취지】 위와 같이 특허청장에게 제출합니다.

대리인 신영무 (서명 또는 인)

【수수료】

【출원료】 0 면 38,000 원

제출 일자 : 2012-09-20

【가산출원료】	36	면	0	원
【우선권주장료】	0	건	0	원
【심사청구료】	0	항	0	원
【합계】	38,000			원

【명세서】

【발명의 명칭】

스테이지 회로 및 이를 이용한 유기전계발광 표시장치{Stage Circuit and Organic Light Emitting Display Device Using the same}

【기술분야】

<1> 본 발명의 실시예는 스테이지 회로 및 이를 이용한 유기전계발광 표시장치에 관한 것으로, 특히 안정성을 향상시킬 수 있도록 한 스테이지 회로 및 이를 이용한 유기전계발광 표시장치에 관한 것이다.

【배경기술】

<2> 최근 음극선관(Cathode Ray Tube)의 단점인 무게와 부피를 줄일 수 있는 각종 평판 표시장치들이 개발되고 있다. 평판 표시장치로는 액정 표시장치(Liquid Crystal Display), 전계방출 표시장치(Field Emission Display), 플라즈마 표시패널(Plasma Display Panel) 및 유기전계발광 표시장치(Organic Light Emitting Display Device) 등이 있다.

<3> 평판표시장치 중 유기전계발광 표시장치는 전자와 정공의 재결합에 의하여 빛을 발생하는 유기 발광 다이오드를 이용하여 영상을 표시한다. 이러한, 유기전계발광 표시장치는 빠른 응답속도를 가짐과 동시에 낮은 소비전력으로 구동되는 장점이 있다. 일반적인 유기전계발광 표시장치는 화소마다 형성되는 트랜지스터를

이용하여 데이터신호에 대응하는 전류를 유기 발광 다이오드로 공급함으로써 유기 발광 다이오드에서 빛이 발생되게 한다.

<4> 이와 같은 종래의 유기전계발광 표시장치는 데이터선들로 데이터신호를 공급하기 위한 데이터 구동부, 주사선들로 주사신호를 순차적으로 공급하기 위한 주사 구동부, 주사선들 및 데이터선들에 접속되는 복수의 화소를 포함하는 화소부를 구비한다.

<5> 화소부에 포함된 화소들은 주사선으로 주사신호가 공급될 때 선택되어 데이터선으로부터 데이터신호를 공급받는다. 데이터신호를 공급받은 화소들은 데이터신호에 대응하는 소정 휘도의 빛을 생성하면서 영상을 표시한다.

<6> 한편, 주사 구동부는 주사선들과 각각 접속되는 스테이지 회로를 구비한다. 스테이지는 자신에게 공급되는 신호에 대응하여 자신과 접속된 주사선으로 주사신호를 공급한다. 여기서, 종래의 스테이지 회로는 주사신호를 공급하기 위하여 다수의 트랜지스터들(예를 들면, 10개 이상) 및 커패시터가 포함되고, 이에 따라 안정성이 저하되는 문제점이 있다. 다시 말하여, 스테이지에 다수의 트랜지스터들이 포함되는 경우 공정 수율이 저하되며, 이에 따라 구동의 안정성이 저하되는 문제점이 발생한다.

【발명의 내용】

【해결하려는 과제】

<7> 따라서, 본 발명의 실시예의 목적은 안정성을 향상시킬 수 있도록 한 스테이지 회로 및 이를 이용한 유기전계발광 표시장치를 제공하는 것이다.

【과제의 해결 수단】

<8> 본 발명의 실시예에 의한 스테이지 회로는 제 1노드 및 제 2노드에 인가된 전압에 대응하여 출력단자로 제 1전원 또는 제 3입력단자의 전압을 공급하기 위한 출력부와; 제 1입력단자, 제 2입력단자 및 상기 제 3입력단자의 신호에 대응하여 상기 제 2노드의 전압을 제어하기 위한 제 1구동부와; 상기 제 2입력단자 및 제 2노드의 전압에 대응하여 상기 제 1노드의 전압을 제어하기 위한 제 2구동부를 구비한다.

<9> 바람직하게, 상기 제 1입력단자는 이전단 스테이지의 출력신호 또는 시작신호, 상기 제 2입력단자는 제 1클럭신호, 상기 제 3입력단자는 제 2클럭신호를 공급받는다. 상기 제 1클럭신호 및 제 2클럭신호는 동일한 주기를 가지며 위상이 서로 중첩되지 않는다. 상기 제 1클럭신호 및 제 2클럭신호는 2 수평기간(2H)의 주기를 가지며, 로우신호가 서로 다른 수평기간에 공급된다. 상기 시작신호는 상기 제 1클럭신호와 중첩되게 공급된다.

<10> 상기 제 1구동부는 상기 제 1입력단자와 상기 제 2노드 사이에 위치되며, 게이트전극이 상기 제 2입력단자에 접속되는 제 1트랜지스터와; 상기 제 2노드와 상

기 제 1전원 사이에 직렬로 위치되는 제 2트랜지스터 및 제 3트랜지스터를 구비하며; 상기 제 2트랜지스터의 게이트전극은 상기 제 3입력단자에 접속되고, 상기 제 3트랜지스터의 게이트전극은 상기 제 1노드에 접속된다.

<11> 상기 출력부는 상기 제 1전원과 상기 출력단자 사이에 위치되며, 게이트전극이 상기 제 1노드에 접속되는 제 4트랜지스터와; 상기 출력단자와 상기 제 3입력단자 사이에 접속되며, 게이트전극이 상기 제 2노드에 접속되는 제 5트랜지스터와; 상기 제 2노드와 상기 출력단자 사이에 접속되는 제 1커패시터와; 상기 제 1노드와 상기 제 1전원 사이에 접속되는 제 2커패시터를 구비한다.

<12> 상기 제 2구동부는 상기 제 1노드와 상기 제 2입력단자 사이에 위치되며, 게이트전극이 상기 제 2노드에 접속되는 제 6트랜지스터와; 상기 제 1노드와 상기 제 1전원보다 낮은 전압으로 설정되는 제 2전원 사이에 위치되며, 게이트전극이 상기 제 2입력단자에 접속되는 제 7트랜지스터를 구비한다.

<13> 상기 제 2구동부는 상기 제 1노드와 상기 제 2입력단자 사이에 위치되며, 게이트전극이 상기 제 2노드에 접속되는 제 6트랜지스터와; 상기 제 1노드와 상기 제 2입력단자 사이에 다이오드 형태로 접속되는 제 7트랜지스터를 구비한다. 상기 제 7트랜지스터는 상기 제 1노드로부터 상기 제 2입력단자로 전류가 흐를 수 있도록 접속된다. 상기 제 1입력단자 및 제 5입력단자와 상기 제 1구동부 사이에 접속되는 양방향 구동부를 더 구비한다.

<14> 상기 양방향 구동부는 상기 제 1입력단자와 상기 제 1구동부 사이에 위치되며, 제 1제어신호가 공급될 때 턴-온되는 제 10트랜지스터와; 상기 제 5입력단자와

상기 제 1구동부 사이에 위치되며, 제 2제어신호가 공급도리 때 턴-온되는 제 11트랜지스터를 구비한다. 상기 제 1입력단자는 이전단 스테이지의 출력신호 또는 시작신호를 공급받고, 상기 제 5입력단자는 다음단 스테이지의 출력신호 또는 시작신호를 공급받는다.

<15> 본 발명의 실시예에 의한 유기전계발광 표시장치는 주사선들 및 데이터선들에 의하여 구획된 영역에 위치되는 화소들과; 상기 데이터선들로 데이터신호를 공급하기 위한 데이터 구동부와; 상기 주사선들로 주사신호를 공급하기 위하여 상기 주사선들과 각각 접속되는 스테이지를 포함하는 주사 구동부를 구비하며; 상기 스테이지들 각각은 제 1노드 및 제 2노드에 인가된 전압에 대응하여 출력단자로 제 1전원 또는 제 3입력단자의 전압을 공급하기 위한 출력부와; 제 1입력단자, 제 2입력단자 및 상기 제 3입력단자의 신호에 대응하여 상기 제 2노드의 전압을 제어하기 위한 제 1구동부와; 상기 제 2입력단자 및 제 2노드의 전압에 대응하여 상기 제 1노드의 전압을 제어하기 위한 제 2구동부를 구비한다.

<16> 바람직하게, 상기 제 3입력단자로 공급되는 클럭신호가 상기 주사신호로 이용된다. 상기 제 1입력단자는 이전단 스테이지의 주사신호 또는 시작신호를 공급받는다. 홀수번째 스테이지의 제 2입력단자는 제 1클럭신호, 제 3입력단자는 제 2클럭신호를 공급받고, 짝수번째 스테이지의 제 2입력단자는 제 2클럭신호, 제 3입력단자는 제 1클럭신호를 공급받는다. 상기 제 1클럭신호 및 제 2클럭신호는 동일한 주기를 가지며 위상이 서로 중첩되지 않는다.

<17> 상기 제 1구동부는 상기 제 1입력단자와 상기 제 2노드 사이에 위치되며, 제

이트전극이 상기 제 2입력단자에 접속되는 제 1트랜지스터와; 상기 제 2노드와 상기 제 1전원 사이에 직렬로 위치되는 제 2트랜지스터 및 제 3트랜지스터를 구비하며; 상기 제 2트랜지스터의 게이트전극은 상기 제 3입력단자에 접속되고, 상기 제 3트랜지스터의 게이트전극은 상기 제 1노드에 접속된다.

<18> 상기 출력부는 상기 제 1전원과 상기 출력단자 사이에 위치되며, 게이트전극이 상기 제 1노드에 접속되는 제 4트랜지스터와; 상기 출력단자와 상기 제 3입력단자 사이에 접속되며, 게이트전극이 상기 제 2노드에 접속되는 제 5트랜지스터와; 상기 제 2노드와 상기 출력단자 사이에 접속되는 제 1커패시터와; 상기 제 1노드와 상기 제 1전원 사이에 접속되는 제 2커패시터를 구비한다.

<19> 상기 제 2구동부는 상기 제 1노드와 상기 제 2입력단자 사이에 위치되며, 게이트전극이 상기 제 2노드에 접속되는 제 6트랜지스터와; 상기 제 1노드와 상기 제 1전원보다 낮은 전압으로 설정되는 제 2전원 사이에 위치되며, 게이트전극이 상기 제 2입력단자에 접속되는 제 7트랜지스터를 구비한다.

<20> 상기 제 2구동부는 상기 제 1노드와 상기 제 2입력단자 사이에 위치되며, 게이트전극이 상기 제 2노드에 접속되는 제 6트랜지스터와; 상기 제 1노드와 상기 제 2입력단자 사이에 다이오드 형태로 접속되는 제 7트랜지스터를 구비한다. 상기 제 7트랜지스터는 상기 제 1노드로부터 상기 제 2입력단자로 전류가 흐를 수 있도록 접속된다. 상기 제 1입력단자 및 제 5입력단자와 상기 제 1구동부 사이에 접속되는 양방향 구동부를 더 구비한다.

<21> 상기 양방향 구동부는 상기 제 1입력단자와 상기 제 1구동부 사이에 위치되

며, 제 1제어신호가 공급될 때 턴-온되는 제 10트랜지스터와; 상기 제 5입력단자와 상기 제 1구동부 사이에 위치되며, 제 2제어신호가 공급도리 때 턴-온되는 제 11트랜지스터를 구비한다. 상기 제 1입력단자는 이전단 스테이지의 출력신호 또는 시작신호를 공급받고, 상기 제 5입력단자는 다음단 스테이지의 출력신호 또는 시작신호를 공급받는다. 상기 제 1입력단자로 공급되는 이전단 스테이지의 주사신호 또는 시작신호는 상기 제 2입력단자로 공급되는 클럭신호와 중첩된다.

【발명의 효과】

<22> 본 발명의 스테이지 회로 및 이를 이용한 유기전계발광 표시장치에 의하면 비교적 간단한 회로로 스테이지를 구현할 수 있고, 이에 따라 안정성을 향상시킬 수 있는 장점이 있다. 또한, 본원 발명의 스테이지 회로는 2개의 클럭신호만을 이용하여 주사신호를 생성하고, 이에 따라 주사신호의 폭을 넓게 설정할 수 있는 장점이 있다.

【도면의 간단한 설명】

<23> 도 1은 본 발명의 실시예에 의한 유기전계발광 표시장치를 나타내는 도면이다.

도 2는 도 1에 도시된 주사 구동부의 실시예를 나타내는 도면이다.

도 3은 도 2에 도시된 스테이지의 실시예를 나타내는 회로도이다.

도 4는 도 3에 도시된 스테이지 회로의 구동방법을 나타내는 파형도이다.

도 5는 도 3의 스테이지 회로의 시뮬레이션 결과를 나타내는 파형도이다.

도 6은 본 발명의 다른 실시예에 의한 스테이지를 나타내는 회로도이다.

도 7은 본 발명의 또 다른 실시예에 의한 스테이지 회로를 나타내는 회로도이다.

【발명을 실시하기 위한 구체적인 내용】

<24> 이하, 본 발명이 속하는 기술분야에서 통상의 지식을 가진 자가 본 발명을 용이하게 실시할 수 있는 바람직한 실시 예가 첨부된 도 1 내지 도 7을 참조하여 자세히 설명하면 다음과 같다.

<25> 도 1은 본 발명의 실시예에 의한 유기전계발광 표시장치를 나타내는 도면이다.

<26> 도 1을 참조하면, 본 발명의 실시예에 의한 유기전계발광 표시장치는 주사선들(S1 내지 Sn) 및 데이터선들(D1 내지 Dm)의 교차부에 위치되는 화소들(30)을 포함하는 화소부(40)와, 주사선들(S1 내지 Sn)을 구동하기 위한 주사 구동부(10)와, 데이터선들(D1 내지 Dm)을 구동하기 위한 데이터 구동부(20)와, 주사 구동부(10) 및 데이터 구동부(20)를 제어하기 위한 타이밍 제어부(50)를 구비한다.

<27> 주사 구동부(10)는 주사선들(S1 내지 Sn)로 주사신호를 공급한다. 일례로, 주사 구동부(10)는 주사선들(S1 내지 Sn)로 주사신호를 순차적으로 공급할 수

있다. 이 경우, 화소들(30)이 수평라인 단위로 선택된다. 이를 위하여, 주사 구동부(10)는 주사선들(S1 내지 S_n) 각각과 접속되는 스테이지 회로(미도시)를 구비한다.

<28> 데이터 구동부(20)는 주사신호에 동기되도록 데이터선들(D1 내지 D_m)로 데이터신호를 공급한다. 그러면, 주사신호에 의하여 선택된 화소들(30)로 데이터신호에 대응하는 전압이 충전된다.

<29> 타이밍 제어부(50)는 주사 구동부(10) 및 데이터 구동부(20)를 제어한다. 또한, 타이밍 제어부(50)는 외부로부터의 데이터(미도시)를 데이터 구동부(20)로 전달한다.

<30> 화소들(30)은 주사신호가 공급될 때 선택되어 데이터신호에 대응하는 전압을 충전하고, 충전된 전압에 대응하는 전류를 유기 발광 다이오드(미도시)로 공급하면서 소정 휘도의 빛을 생성한다.

<31> 도 2는 도 1에 도시된 주사 구동부의 실시예를 나타내는 도면이다. 도 2에서는 설명의 편의성을 위하여 4개의 스테이지를 도시하기로 한다.

<32> 도 2를 참조하면, 본 발명의 실시예에 의한 주사 구동부(10)는 복수의 스테이지(ST1 내지 ST4)를 구비한다. 스테이지(ST1 내지 ST4) 각각은 주사선들(S1 내지 S4) 중 어느 하나와 접속되며 클럭신호(CLK1, CLK2)에 대응하여 구동된다. 이와 같은 스테이지(ST1 내지 ST4)들은 동일한 회로로 구성된다.

- <33> 스테이지(ST1 내지 ST4) 각각은 제 1입력단자(101) 내지 제 3입력단자(103), 출력단자(104)를 구비한다.
- <34> 스테이지(ST1 내지 ST4) 각각의 제 1입력단자(101)는 이전단 스테이지의 출력신호(즉, 주사신호) 또는 시작신호(SSP)를 공급받는다. 일례로, 첫 번째 스테이지(ST1)의 제 1입력단자(101)는 시작신호(SSP)를 공급받고, 나머지 스테이지들(ST2 내지 ST4)의 제 1입력단자(101)는 이전단 스테이지의 출력신호를 공급받는다.
- <35> i (i 는 홀수 또는 짝수)번째 스테이지(ST i)의 제 2입력단자(102)는 제 1클럭신호(CLK1), 제 3입력단자(103)는 제 2클럭신호(CLK2)를 공급받는다. $i+1$ 번째 스테이지(ST i)의 제 2입력단자(102)는 제 2클럭신호(CLK2), 제 3입력단자(103)는 제 1클럭신호(CLK1)를 공급받는다.
- <36> 제 1클럭신호(CLK1) 및 제 2클럭신호(CLK2)는 동일한 주기를 가지며 위상이 서로 중첩되지 않는다. 일례로, 하나의 주사선으로 주사신호가 공급되는 기간을 1수평기간(1H) 이라고 할 때, 클럭신호(CLK1, CLK2) 각각은 2H의 주기를 가지며 서로 다른 수평기간에 공급된다.
- <37> 도 3은 도 2에 도시된 스테이지의 실시예를 나타내는 회로도이다. 도 3에서는 설명의 편의성을 위하여 제 1스테이지(ST1) 및 제 2스테이지(ST2)를 도시하기로 한다. 그리고, 도 3에서는 트랜지스터들이 PMOS로 형성되는 것으로 도시되었지만, 본원 발명이 이에 한정되지는 않는다. 일례로, 트랜지스터들은 NMOS로 형성될 수

있다.

<38> 도 3을 참조하면, 본 발명의 제 1실시예에 의한 스테이지(ST1)는 제 1구동부(210), 제 2구동부(220) 및 출력부(230)를 구비한다.

<39> 출력부(230)는 제 1노드(N1) 및 제 2노드(N2)에 인가되는 전압에 대응하여 출력단자(104)로 공급되는 전압을 제어한다. 이를 위하여, 출력부(230)는 제 4트랜지스터(M4), 제 5트랜지스터(M5), 제 1커패시터(C1) 및 제 2커패시터(C2)를 구비한다.

<40> 제 4트랜지스터(M4)는 제 1전원(VDD)과 출력단자(104) 사이에 위치되며, 게이트전극이 제 1노드(N1)에 접속된다. 이와 같은 제 4트랜지스터(M4)는 제 1노드(N1)에 인가되는 전압에 대응하여 제 1전원(VDD)과 출력단자(104)의 접속을 제어한다. 여기서, 제 1전원(VDD)은 게이트 오프 전압, 예를 들면 하이레벨의 전압으로 설정된다.

<41> 제 5트랜지스터(M5)는 출력단자(104)와 제 3입력단자(103) 사이에 위치되며, 게이트전극이 제 2노드(N2)에 접속된다. 이와 같은 제 5트랜지스터(M5)는 제 2노드(N2)에 인가되는 전압에 대응하여 출력단자(104)와 제 3입력단자(103)의 접속을 제어한다.

<42> 제 1커패시터(C1)는 제 2노드(N2)와 출력단자(104) 사이에 접속된다. 이와 같은 제 1커패시터(C1)는 제 5트랜지스터(M5)의 턴-온 및 턴-오프에 대응하는 전압을 충전한다.

- <43> 제 2커패시터(C2)는 제 1노드(N1)와 제 1전원(VDD) 사이에 접속된다. 이와 같은 제 2커패시터(C2)는 제 1노드(N1)에 인가되는 전압을 충전한다.
- <44> 제 1구동부(210)는 제 1입력단자(101) 내지 제 3입력단자(103)로 공급되는 신호들에 대응하여 제 2노드(N2)의 전압을 제어한다. 이를 위하여, 제 1구동부(210)는 제 1트랜지스터(M1) 내지 제 3트랜지스터(M3)를 구비한다.
- <45> 제 1트랜지스터(M1)는 제 1입력단자(101)와 제 2노드(N2) 사이에 위치되며, 게이트전극이 제 2입력단자(102)에 접속된다. 이와 같은 제 1트랜지스터(M1)는 제 2입력단자(102)로 공급되는 전압에 대응하여 제 1입력단자(101)와 제 2노드(N2)의 접속을 제어한다.
- <46> 제 2트랜지스터(M2) 및 제 3트랜지스터(M3)는 제 2노드(N2)와 제 1전원(VDD) 사이에 직렬로 접속된다. 실제로, 제 2트랜지스터(M2)는 제 3트랜지스터(M3)와 제 2노드(N2) 사이에 위치되며, 게이트전극이 제 3입력단자(103)에 접속된다. 이와 같은 제 2트랜지스터(M2)는 제 3입력단자(103)로 공급되는 전압에 대응하여 제 3트랜지스터(M3)와 제 2노드(N2)의 접속을 제어한다.
- <47> 제 3트랜지스터(M3)는 제 2트랜지스터(M2)와 제 1전원(VDD) 사이에 위치되며, 게이트전극이 제 1노드(N1)에 접속된다. 이와 같은 제 3트랜지스터(M3)는 제 1노드(N1)의 전압에 대응하여 제 2트랜지스터(M2)와 제 1전원(VDD)의 접속을 제어한다.
- <48> 제 2구동부(220)는 제 2입력단자(102) 및 제 2노드(N2)의 전압에 대응하여

제 1노드(N1)의 전압을 제어한다. 이를 위하여, 제 2구동부(220)는 제 6트랜지스터(M6) 및 제 7트랜지스터(M7)를 구비한다.

<49> 제 6트랜지스터(M6)는 제 1노드(N1)와 제 2입력단자(102) 사이에 위치되며, 게이트전극이 제 2노드(N2)에 접속된다. 이와 같은 제 6트랜지스터(M6)는 제 2노드(N2)의 전압에 대응하여 제 1노드(N1)와 제 2입력단자(102)의 접속을 제어한다.

<50> 제 7트랜지스터(M7)는 제 1노드(N1)와 제 2전원(VSS) 사이에 위치되며, 게이트전극이 제 2입력단자(102)에 접속된다. 이와 같은 제 7트랜지스터(M7)는 제 2입력단자(102)의 전압에 대응하여 제 1노드(N1)와 제 2전원(VSS)의 접속을 제어한다. 여기서, 제 2전원(VSS)은 게이트 온 전압, 예를 들면 로우레벨의 전압으로 설정된다.

<51> 도 4는 도 3에 도시된 스테이지 회로의 구동방법을 나타내는 파형도이다. 도 4에서는 설명의 편의성을 위하여 제 1스테이지(ST1)를 이용하여 동작과정을 설명하기로 한다.

<52> 도 4를 참조하면, 제 1클럭신호(CLK1) 및 제 2클럭신호(CLK2)는 2수평기간(2H)의 주기를 가지며, 서로 다른 수평기간에 공급된다. 그리고, 제 2입력단자(102)로 공급되는 클럭신호(CLK1 또는 CLK2)와 동기되도록 시작신호(SSP)가 공급된다.

<53> 동작과정을 상세히 설명하면, 먼저 제 1클럭신호(CLK1)와 동기되도록 시작신

호(SSP)가 공급된다.

<54> 제 1클럭신호(CLK1)가 공급되면 제 1트랜지스터(M1) 및 제 7트랜지스터(M7)가 턴-온된다. 제 1트랜지스터(M1)가 턴-온되면 제 1입력단자(101)와 제 2노드(N2)가 전기적으로 접속된다. 이 경우, 제 1입력단자(101)로 공급되는 시작신호(SSP)에 의하여 제 2노드(N2)가 로우전압으로 설정된다. 제 2노드(N2)가 로우전압으로 설정되면 제 5트랜지스터(M5) 및 제 6트랜지스터(M6)가 턴-온된다.

<55> 제 5트랜지스터(M5)가 턴-온되면 제 3입력단자(103)와 출력단자(104)가 전기적으로 접속된다. 여기서, 제 3입력단자(103)는 하이전압으로 설정(즉, 제 2클럭신호(CLK2)가 공급되지 않음)되고, 이에 따라 출력단자(104)로도 하이전압이 출력된다. 제 6트랜지스터(M6)가 턴-온되면 제 2입력단자(102)와 제 1노드(N1)가 전기적으로 접속된다. 그러면, 제 2입력단자(102)로 공급되는 제 1클럭신호(CLK1)의 전압, 즉 로우전압이 제 1노드(N1)로 공급된다. 추가적으로, 제 1클럭신호(CLK1)에 대응하여 제 7트랜지스터(M7)가 턴-온되어 제 1노드(N1)로는 제 2전원(VSS)의 전압이 공급된다. 여기서, 제 2전원(VSS)의 전압은 제 1클럭신호(CLK1)와 동일(또는 유사)한 전압으로 설정되고, 이에 따라 제 1노드(N1)는 안정적으로 로우전압을 유지한다.

<56> 제 1노드(N1)로 로우전압이 공급되면 제 4트랜지스터(M4) 및 제 3트랜지스터(M3)가 턴-온된다. 제 3트랜지스터(M3)가 턴-온되면 제 1전원(VDD)과 제 2트랜지스터(M2)가 전기적으로 접속된다. 여기서, 제 2트랜지스터(M2)가 턴-오프 상태로 설정되기 때문에 제 3트랜지스터(M3)가 턴-온되더라도 제 2노드(N2)는 안정적으로

로우전압을 유지한다. 제 4트랜지스터(M4)가 턴-온되면 출력단자(104)로 제 1전원(VDD)의 전압이 공급된다. 여기서, 제 1전원(VDD)의 전압은 제 3입력단자(103)로 공급되는 하이전압과 동일한 전압으로 설정되고, 이에 따라 출력단자(104)는 안정적으로 하이전압을 유지한다.

<57> 이후, 시작신호(SSP) 및 제 1클럭신호(CLK1)의 공급이 중단된다. 제 1클럭신호(CLK1)의 공급이 중단되면 제 1트랜지스터(M1) 및 제 7트랜지스터(M7)가 턴-오프된다. 이때, 제 1커패시터(C1)에 저장된 전압에 대응하여 제 5트랜지스터(M5) 및 제 6트랜지스터(M6)는 턴-온 상태를 유지한다.

<58> 제 5트랜지스터(M5)가 턴-온 상태를 유지하는 경우 출력단자(104)와 제 3입력단자(103)는 전기적 접속을 유지한다. 따라서, 출력단자(104)는 제 3입력단자(103)로부터 하이전압을 공급받는다.

<59> 한편, 제 6트랜지스터(M6)가 턴-온 상태를 유지하기 때문에 제 1노드(N1)와 제 2입력단자(102)는 전기적으로 접속된다. 여기서, 제 2입력단자(102)의 전압은 제 1클럭신호(CLK1)의 공급중단에 대응하여 하이전압으로 설정되고, 이에 따라 제 1노드(N1)도 하이전압으로 설정된다. 제 1노드(N1)로 하이전압이 공급되면 제 4트랜지스터(M4)가 턴-오프된다.

<60> 이후, 제 3입력단자(103)로 제 2클럭신호(CLK2)가 공급된다. 이때, 제 5트랜지스터(M5)가 턴-온 상태로 설정되기 때문에 제 3입력단자(103)로 공급된 제 2클럭신호(CLK2)는 출력단자(104)로 공급된다. 이 경우, 출력단자(104)는 제 2클럭신호(CLK2)를 주사신호로서 주사선(S1)으로 출력한다.

<61> 주사선(S1)으로 주사신호가 출력된 후 제 1클럭신호(CLK1)가 공급된다. 제 1클럭신호(CLK1)가 공급되면 제 1트랜지스터(M1) 및 제 7트랜지스터(M7)가 턴-온된다. 제 1트랜지스터(M1)가 턴-온되면 제 1입력단자(101)와 제 2노드(N2)가 전기적으로 접속된다. 이때, 제 1입력단자(101)로는 시작신호(SSP)가 공급되지 않고, 이에 따라 하이전압으로 설정된다. 따라서, 제 1트랜지스터(M1)가 턴-온되면 제 2노드(N2)로 하이전압이 공급되고, 이에 따라 제 5트랜지스터(M5) 및 제 6트랜지스터(M6)가 턴-오프된다.

<62> 제 7트랜지스터(M7)가 턴-온되면 제 2전원(VSS)이 제 1노드(N1)로 공급되고, 이에 따라 제 3트랜지스터(M3) 및 제 4트랜지스터(M4)가 턴-온된다. 제 4트랜지스터(M4)가 턴-온되면 출력단자(104)로 제 1전원(VDD)의 전압이 공급된다. 이후, 제 4트랜지스터(M4) 및 제 3트랜지스터(M3)는 제 2커패시터(C2)에 충전된 전압에 대응하여 턴-온 상태를 유지하고, 이에 따라 출력단자(104)는 제 1전원(VDD)의 전압을 안정적으로 공급받는다.

<63> 추가적으로 제 2클럭신호(CLK2)가 공급될 때 제 2트랜지스터(M2)가 턴-온된다. 이때, 제 3트랜지스터(M3)가 턴-온 상태로 설정되기 때문에 제 2노드(N2)로 제 1전원(VDD)의 전압이 공급된다. 이 경우, 제 5트랜지스터(M5) 및 제 6트랜지스터(M6)는 안정적으로 턴-오프 상태를 유지한다.

<64> 한편, 제 2스테이지(ST2)는 제 2클럭신호(CLK2)와 동기되도록 제 1스테이지(ST1)의 출력신호(즉, 주사신호)를 공급받는다. 이 경우, 제 2스테이지(ST2)는 제 1클럭신호(CLK1)와 동기되도록 제 2주사선(S2)으로 주사신호를 출력한다. 실제로,

본원 발명의 스테이지들(ST)은 상술한 과정을 반복하면서 주사선들로 주사신호를 순차적으로 출력한다.

<65> 도 5는 도 3의 스테이지 회로의 시뮬레이션 결과를 나타내는 파형도이다.

<66> 도 5를 참조하면, 본 발명의 실시예에 의한 스테이지 회로를 이용한 주사 구동부는 주사선들로 주사신호를 순차적으로 공급한다. 또한, 본원 발명의 스테이지 회로는 제 1클럭신호(CLK1) 및 제 2클럭신호(CLK2) 만을 이용하여 주사선으로 주사신호를 출력한다. 즉, 본원 발명의 스테이지 회로는 별도의 초기화신호를 공급받지 않고, 이에 따라 주사신호의 폭을 넓게 설정(예를 들면, 1H기간)할 수 있는 장점이 있다.

<67> 도 6은 본 발명의 다른 실시예에 의한 스테이지를 나타내는 회로도이다. 도 6에서 도 3과 동일한 구성에 대해서는 동일한 도면부호를 할당함과 아울러 상세한 설명은 생략하기로 한다.

<68> 도 6을 참조하면, 본 발명의 다른 실시예에 의한 스테이지에서 제 7트랜지스터(M7')는 제 1노드(N1)와 제 2입력단자(102) 사이에 다이오드 형태로 접속된다. 다시 말하여, 제 7트랜지스터(M7')는 제 1노드(N1)로부터 제 2입력단자(102)로 전류가 흐를 수 있도록 다이오드 형태로 접속된다. 이 경우, 제 2입력단자(102)로 로우전압이 공급되는 경우 제 1노드(N1)의 전압이 로우전압까지 하강된다. 이 외

의 동작과정은 도 3에 도시된 본 발명의 실시예에 의한 스테이지와 동일하므로 생략하기로 한다.

<69> 도 7은 본 발명의 또 다른 실시예에 의한 스테이지 회로를 나타내는 회로도이다. 도 7에서 도 3과 동일한 구성에 대해서는 동일한 도면부호를 할당함과 아울러 상세한 설명은 생략하기로 한다.

<70> 도 7을 참조하면, 본 발명의 또 다른 실시예에 의한 스테이지 회로는 양방향 구동부(240)를 더 구비한다. 양방향 구동부(240)는 주사신호가 제 1방향(제 1주사선(S1))으로부터 제 n주사선(Sn)) 또는 제 2방향(제 n주사선(Sn))으로부터 제 1주사선(S1))으로 공급될 수 있도록 제어한다. 이를 위하여, 양방향 구동부(240)는 제 10트랜지스터(M10) 및 제 11트랜지스터(M11)를 구비한다.

<71> 제 10트랜지스터(M10)는 제 1입력단자(101)와 제 1구동부(210) 사이에 접속된다. 이와 같은 제 10트랜지스터(M10)는 제 1제어신호(CS1)가 공급될 때 턴-온된다. 여기서, 제 1입력단자(101)는 이전단 스테이지의 주사신호(또는 시작신호)를 공급받는다.

<72> 제 11트랜지스터(M11)는 제 5입력단자(105)와 제 1구동부(210) 사이에 접속된다. 이와 같은 제 11트랜지스터(M11)는 제 2제어신호(CS2)가 공급될 때 턴-온된다. 여기서, 제 5입력단자(105)는 다음단 스테이지의 주사신호(또는 시작신호)를 공급받는다.

<73> 동작과정을 설명하면, 제 1제어신호(CS1)가 공급되는 경우 제 10트랜지스터(M10)가 턴-온된다. 제 10트랜지스터(M10)가 턴-온되면 스테이지들 각각은 이전단 스테이지의 주사신호에 대응하여 구동되고, 이에 따라 제 1방향으로 주사신호가 순차적으로 출력된다.

<74> 그리고, 제 2제어신호(CS2)가 공급되는 경우 제 11트랜지스터(M11)가 턴-온된다. 제 11트랜지스터(M11)가 턴-온되면 스테이지들 각각은 다음단 스테이지의 주사신호에 대응하여 구동되고, 이에 따라 제 2방향으로 주사신호가 출력된다. 그 외의 구동과정은 도 3에 도시된 본원 발명의 실시예에 의한 스테이지와 동일하므로 상세한 설명은 생략하기로 한다.

<75> 본 발명의 기술 사상은 상기 바람직한 실시예에 따라 구체적으로 기술되었으나, 상기한 실시예는 그 설명을 위한 것이며 그 제한을 위한 것이 아님을 주의하여야 한다. 또한, 본 발명의 기술 분야의 통상의 지식을 가진 자라면 본 발명의 기술 사상의 범위 내에서 다양한 변형예가 가능함을 이해할 수 있을 것이다.

【부호의 설명】

<76>	10 : 주사 구동부	20 : 데이터 구동부
	30 : 화소	40 : 화소부
	50 : 타이밍 제어부	101,102,103 : 입력단자
	104 : 출력단자	210,220 : 구동부

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230 : 출력부

240 : 양방향 구동부

【특허 청구범위】

【청구항 1】

제 1노드 및 제 2노드에 인가된 전압에 대응하여 출력단자로 제 1전원 또는 제 3입력단자의 전압을 공급하기 위한 출력부와;

제 1입력단자, 제 2입력단자 및 상기 제 3입력단자의 신호에 대응하여 상기 제 2노드의 전압을 제어하기 위한 제 1구동부와;

상기 제 2입력단자 및 제 2노드의 전압에 대응하여 상기 제 1노드의 전압을 제어하기 위한 제 2구동부를 구비하는 것을 특징으로 하는 스테이지 회로.

【청구항 2】

제 1항에 있어서,

상기 제 1입력단자는 이전단 스테이지의 출력신호 또는 시작신호, 상기 제 2입력단자는 제 1클럭신호, 상기 제 3입력단자는 제 2클럭신호를 공급받는 것을 특징으로 하는 스테이지 회로.

【청구항 3】

제 2항에 있어서,

상기 제 1클럭신호 및 제 2클럭신호는 동일한 주기를 가지며 위상이 서로 중첩되지 않는 것을 특징으로 하는 스테이지 회로.

【청구항 4】

제 3항에 있어서,

상기 제 1클럭신호 및 제 2클럭신호는 2 수평기간(2H)의 주기를 가지며, 로우신호가 서로 다른 수평기간에 공급되는 것을 특징으로 하는 스테이지 회로.

【청구항 5】

제 2항에 있어서,

상기 시작신호는 상기 제 1클럭신호와 중첩되게 공급되는 것을 특징으로 하는 스테이지 회로.

【청구항 6】

제 2항에 있어서,

상기 제 1구동부는

상기 제 1입력단자와 상기 제 2노드 사이에 위치되며, 게이트전극이 상기 제 2입력단자에 접속되는 제 1트랜지스터와;

상기 제 2노드와 상기 제 1전원 사이에 직렬로 위치되는 제 2트랜지스터 및 제 3트랜지스터를 구비하며;

상기 제 2트랜지스터의 게이트전극은 상기 제 3입력단자에 접속되고, 상기 제 3트랜지스터의 게이트전극은 상기 제 1노드에 접속되는 것을 특징으로 하는 스테이지 회로.

【청구항 7】

제 2항에 있어서,

상기 출력부는

상기 제 1전원과 상기 출력단자 사이에 위치되며, 게이트전극이 상기 제 1노드에 접속되는 제 4트랜지스터와;

상기 출력단자와 상기 제 3입력단자 사이에 접속되며, 게이트전극이 상기 제 2노드에 접속되는 제 5트랜지스터와;

상기 제 2노드와 상기 출력단자 사이에 접속되는 제 1커패시터와;

상기 제 1노드와 상기 제 1전원 사이에 접속되는 제 2커패시터를 구비하는 것을 특징으로 하는 스테이지 회로.

【청구항 8】

제 2항에 있어서,

상기 제 2구동부는

상기 제 1노드와 상기 제 2입력단자 사이에 위치되며, 게이트전극이 상기 제 2노드에 접속되는 제 6트랜지스터와;

상기 제 1노드와 상기 제 1전원보다 낮은 전압으로 설정되는 제 2전원 사이에 위치되며, 게이트전극이 상기 제 2입력단자에 접속되는 제 7트랜지스터를 구비하는 것을 특징으로 하는 스테이지 회로.

【청구항 9】

제 2항에 있어서,

상기 제 2구동부는

상기 제 1노드와 상기 제 2입력단자 사이에 위치되며, 게이트전극이 상기 제

2노드에 접속되는 제 6트랜지스터와;

상기 제 1노드와 상기 제 2입력단자 사이에 다이오드 형태로 접속되는 제 7 트랜지스터를 구비하는 것을 특징으로 하는 스테이지 회로.

【청구항 10】

제 9항에 있어서,

상기 제 7트랜지스터는 상기 제 1노드로부터 상기 제 2입력단자로 전류가 흐를 수 있도록 접속되는 것을 특징으로 하는 스테이지 회로.

【청구항 11】

제 1항에 있어서,

상기 제 1입력단자 및 제 5입력단자와 상기 제 1구동부 사이에 접속되는 양방향 구동부를 더 구비하는 것을 특징으로 하는 스테이지 회로.

【청구항 12】

제 11항에 있어서,

상기 양방향 구동부는

상기 제 1입력단자와 상기 제 1구동부 사이에 위치되며, 제 1제어신호가 공급될 때 턴-온되는 제 10트랜지스터와;

상기 제 5입력단자와 상기 제 1구동부 사이에 위치되며, 제 2제어신호가 공급도리 때 턴-온되는 제 11트랜지스터를 구비하는 것을 특징으로 하는 스테이지 회로.

【청구항 13】

제 12항에 있어서,

상기 제 1입력단자는 이전단 스테이지의 출력신호 또는 시작신호를 공급받고,

상기 제 5입력단자는 다음단 스테이지의 출력신호 또는 시작신호를 공급받는 것을 특징으로 하는 스테이지 회로.

【청구항 14】

주사선들 및 데이터선들에 의하여 구획된 영역에 위치되는 화소들과;

상기 데이터선들로 데이터신호를 공급하기 위한 데이터 구동부와;

상기 주사선들로 주사신호를 공급하기 위하여 상기 주사선들과 각각 접속되는 스테이지를 포함하는 주사 구동부를 구비하며;

상기 스테이지들 각각은

제 1노드 및 제 2노드에 인가된 전압에 대응하여 출력단자로 제 1전원 또는 제 3입력단자의 전압을 공급하기 위한 출력부와;

제 1입력단자, 제 2입력단자 및 상기 제 3입력단자의 신호에 대응하여 상기 제 2노드의 전압을 제어하기 위한 제 1구동부와;

상기 제 2입력단자 및 제 2노드의 전압에 대응하여 상기 제 1노드의 전압을 제어하기 위한 제 2구동부를 구비하는 것을 특징으로 하는 유기전계발광 표시장치.

【청구항 15】

제 14항에 있어서,

상기 제 3입력단자로 공급되는 클럭신호가 상기 주사신호로 이용되는 것을
특징으로 하는 유기전계발광 표시장치.

【청구항 16】

제 14항에 있어서,

상기 제 1입력단자는 이전단 스테이지의 주사신호 또는 시작신호를 공급받는
것을 특징으로 하는 유기전계발광 표시장치.

【청구항 17】

제 16항에 있어서,

홀수번째 스테이지의 제 2입력단자는 제 1클럭신호, 제 3입력단자는 제 2클
럭신호를 공급받고,

짝수번째 스테이지의 제 2입력단자는 제 2클럭신호, 제 3입력단자는 제 1클
럭신호를 공급받는 것을 특징으로 하는 유기전계발광 표시장치.

【청구항 18】

제 17항에 있어서,

상기 제 1클럭신호 및 제 2클럭신호는 동일한 주기를 가지며 위상이 서로 중
첩되지 않는 것을 특징으로 하는 유기전계발광 표시장치.

【청구항 19】

제 17항에 있어서,

상기 제 1구동부는

상기 제 1입력단자와 상기 제 2노드 사이에 위치되며, 게이트전극이 상기 제 2입력단자에 접속되는 제 1트랜지스터와;

상기 제 2노드와 상기 제 1전원 사이에 직렬로 위치되는 제 2트랜지스터 및 제 3트랜지스터를 구비하며;

상기 제 2트랜지스터의 게이트전극은 상기 제 3입력단자에 접속되고, 상기 제 3트랜지스터의 게이트전극은 상기 제 1노드에 접속되는 것을 특징으로 하는 유기전계발광 표시장치.

【청구항 20】

제 17항에 있어서,

상기 출력부는

상기 제 1전원과 상기 출력단자 사이에 위치되며, 게이트전극이 상기 제 1노드에 접속되는 제 4트랜지스터와;

상기 출력단자와 상기 제 3입력단자 사이에 접속되며, 게이트전극이 상기 제 2노드에 접속되는 제 5트랜지스터와;

상기 제 2노드와 상기 출력단자 사이에 접속되는 제 1커패시터와;

상기 제 1노드와 상기 제 1전원 사이에 접속되는 제 2커패시터를 구비하는

것을 특징으로 하는 유기전계발광 표시장치.

【청구항 21】

제 17항에 있어서,

상기 제 2구동부는

상기 제 1노드와 상기 제 2입력단자 사이에 위치되며, 게이트전극이 상기 제 2노드에 접속되는 제 6트랜지스터와;

상기 제 1노드와 상기 제 1전원보다 낮은 전압으로 설정되는 제 2전원 사이에 위치되며, 게이트전극이 상기 제 2입력단자에 접속되는 제 7트랜지스터를 구비하는 것을 특징으로 하는 유기전계발광 표시장치.

【청구항 22】

제 17항에 있어서,

상기 제 2구동부는

상기 제 1노드와 상기 제 2입력단자 사이에 위치되며, 게이트전극이 상기 제 2노드에 접속되는 제 6트랜지스터와;

상기 제 1노드와 상기 제 2입력단자 사이에 다이오드 형태로 접속되는 제 7트랜지스터를 구비하는 것을 특징으로 하는 유기전계발광 표시장치.

【청구항 23】

제 22항에 있어서,

상기 제 7트랜지스터는 상기 제 1노드로부터 상기 제 2입력단자로 전류가 흐

를 수 있도록 접속되는 것을 특징으로 하는 유기전계발광 표시장치.

【청구항 24】

제 14항에 있어서,

상기 제 1입력단자 및 제 5입력단자와 상기 제 1구동부 사이에 접속되는 양방향 구동부를 더 구비하는 것을 특징으로 하는 유기전계발광 표시장치.

【청구항 25】

제 24항에 있어서,

상기 양방향 구동부는

상기 제 1입력단자와 상기 제 1구동부 사이에 위치되며, 제 1제어신호가 공급될 때 턴-온되는 제 10트랜지스터와;

상기 제 5입력단자와 상기 제 1구동부 사이에 위치되며, 제 2제어신호가 공급도리 때 턴-온되는 제 11트랜지스터를 구비하는 것을 특징으로 하는 유기전계발광 표시장치

【청구항 26】

제 25항에 있어서,

상기 제 1입력단자는 이전단 스테이지의 출력신호 또는 시작신호를 공급받고,

상기 제 5입력단자는 다음단 스테이지의 출력신호 또는 시작신호를 공급받는 것을 특징으로 하는 유기전계발광 표시장치.

【청구항 27】

제 17항에 있어서,

상기 제 1입력단자로 공급되는 이전단 스테이지의 주사신호 또는 시작신호는
상기 제 2입력단자로 공급되는 클럭신호와 중첩되는 것을 특징으로 하는 유기전계
발광 표시장치.

【요약서】

【요약】

본 발명은 안정성을 향상시킬 수 있도록 한 스테이지 회로에 관한 것이다.

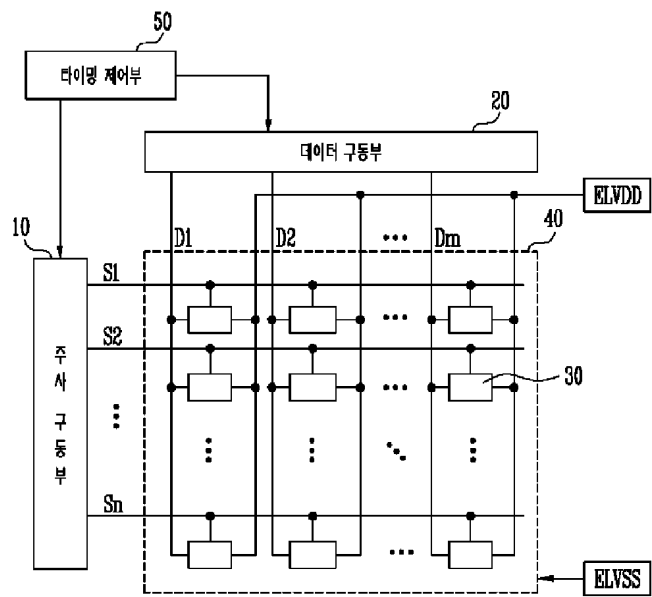
본 발명의 스테이지 회로는 제 1노드 및 제 2노드에 인가된 전압에 대응하여 출력단자로 제 1전원 또는 제 3입력단자의 전압을 공급하기 위한 출력부와; 제 1입력단자, 제 2입력단자 및 상기 제 3입력단자의 신호에 대응하여 상기 제 2노드의 전압을 제어하기 위한 제 1구동부와; 상기 제 2입력단자 및 제 2노드의 전압에 대응하여 상기 제 1노드의 전압을 제어하기 위한 제 2구동부를 구비한다.

【대표도】

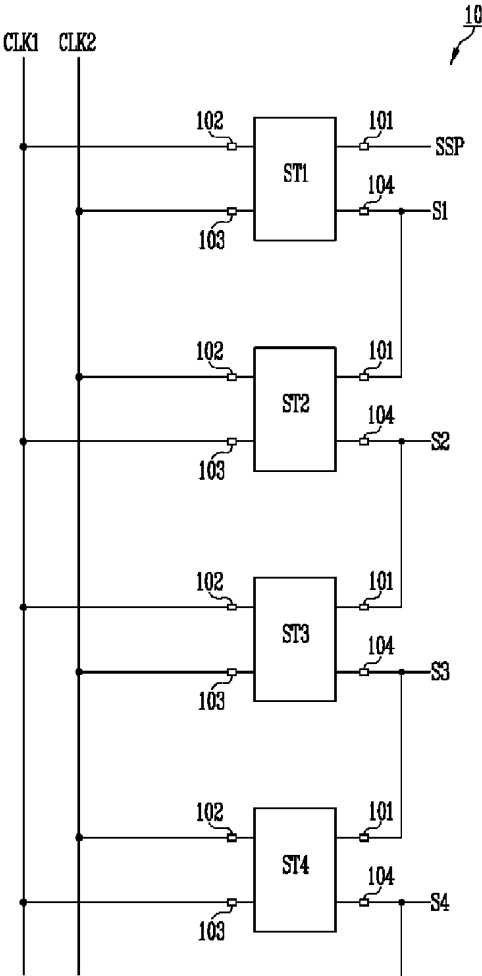
도 3

【도면】

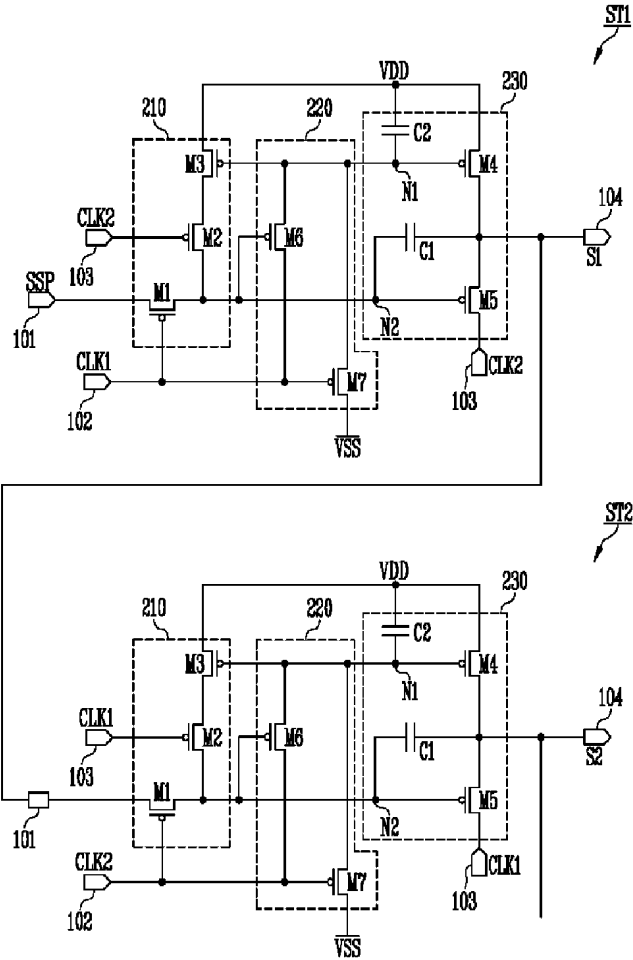
【도 1】



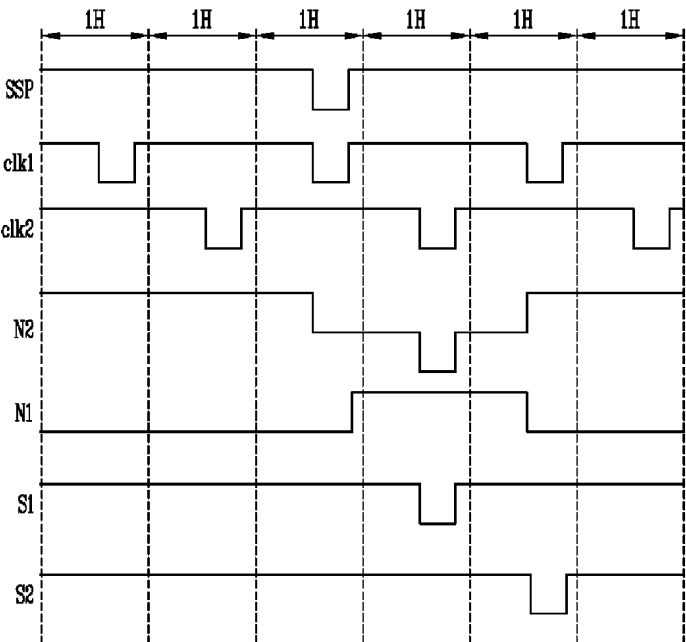
【도 2】



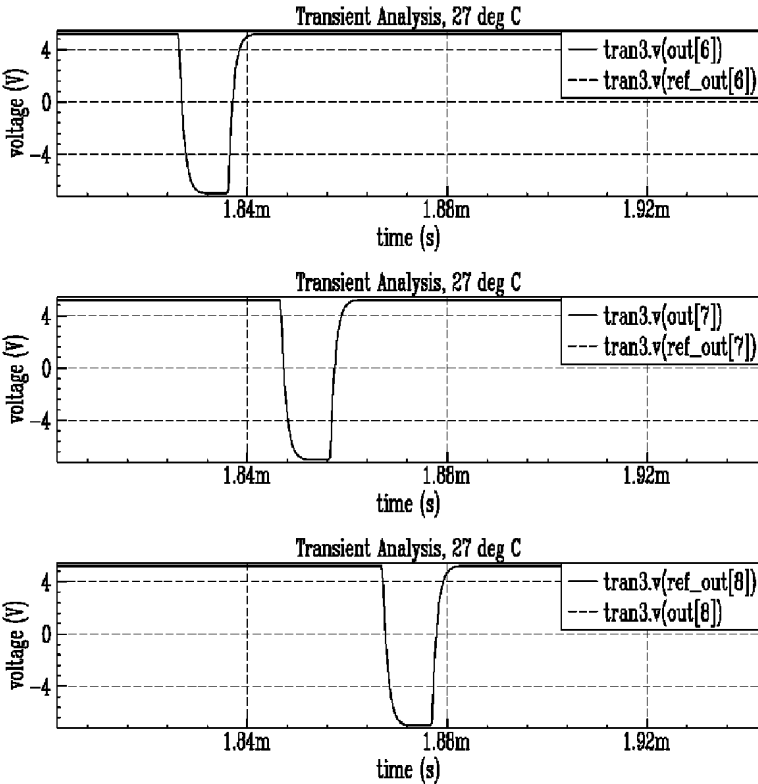
【도 3】



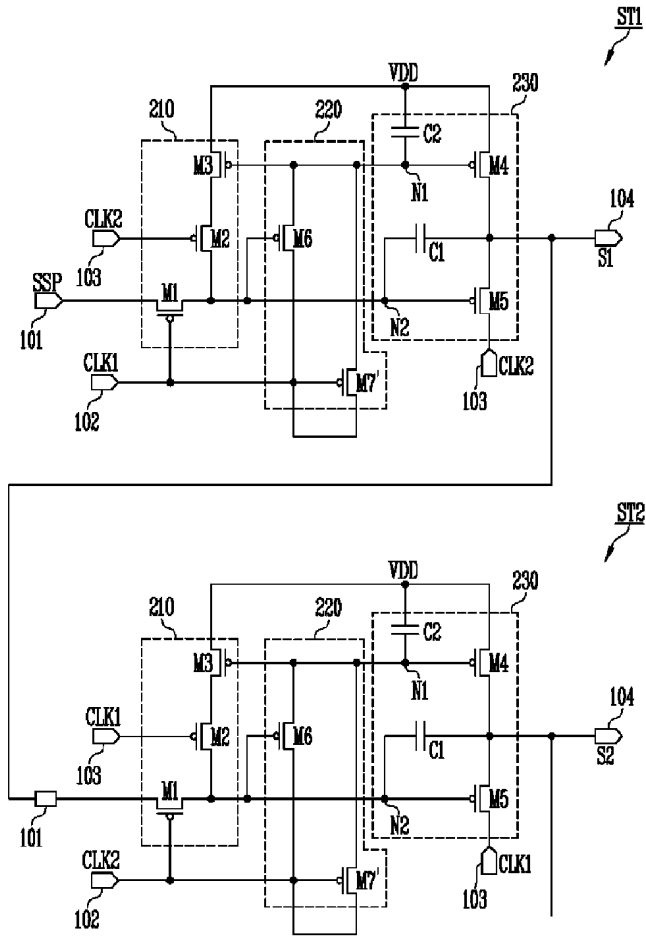
【도 4】



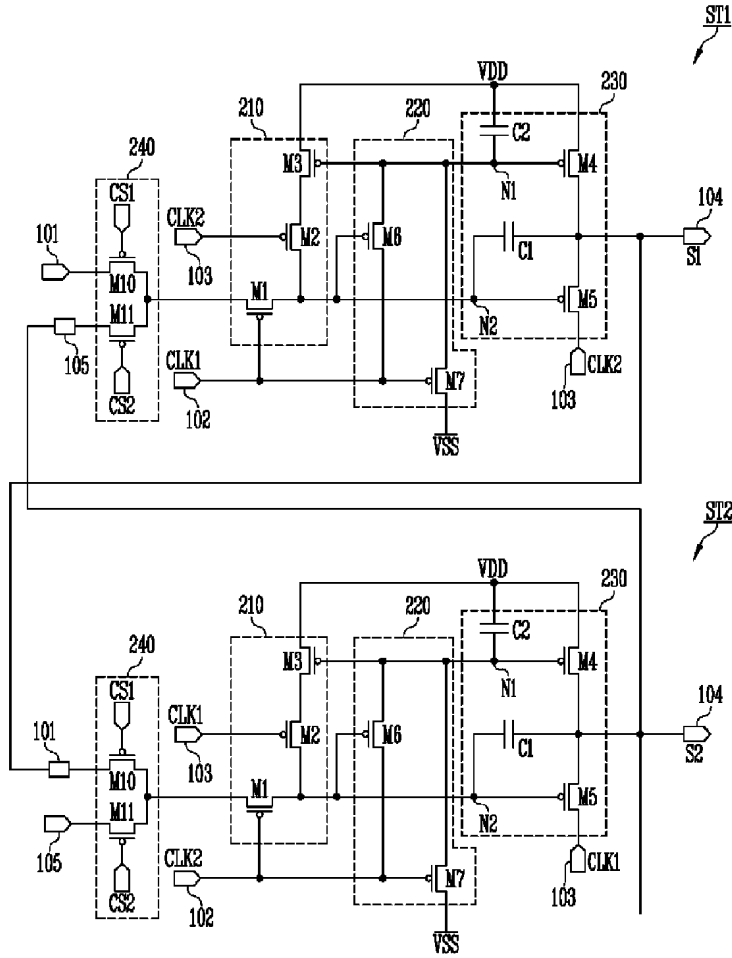
【도 5】



【도 6】



【도 7】





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Title: STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/771,385			
APPLICATION AS FILED - PART I									
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)		
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	390		
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	620		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250		
TOTAL CLAIMS (37 CFR 1.16(j))	27	minus 20 = * 7				x 62 =	434		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *				x 250 =	0.00		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00		
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00		
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1694		
APPLICATION AS AMENDED - PART II									
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =		
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =		
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
			TOTAL ADD'L FEE			TOTAL ADD'L FEE			
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =		
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =		
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
			TOTAL ADD'L FEE			TOTAL ADD'L FEE			
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
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CONFIRMATION NO. 3091

27849

LEE & MORSE, P.C.
3141 FAIRVIEW PARK DRIVE
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FALLS CHURCH, VA 22042

FILING RECEIPT



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Date Mailed: 03/15/2013

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Inventor(s)

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Power of Attorney: The patent practitioners associated with Customer Number 27849

Domestic Applications for which benefit is claimed - None.

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REPUBLIC OF KOREA 10-2012-0104512 09/20/2012

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Projected Publication Date: 03/20/2014

Non-Publication Request: No

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Title

STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME

Preliminary Class

370

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Customer Number
27849

TO: Commissioner for Patents
Mail Stop Patent Application
P.O. Box 1450
Alexandria, VA 22313-1450

Attorney Docket No. 304/1043

UTILITY PATENT APPLICATION TRANSMITTAL
(new nonprovisional application under 37 CFR 1.53(b))

Transmitted herewith for filing is the patent application of:

INVENTOR(S): HWAN-SOO JANG

**TITLE: STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY
USING THE SAME**

CORRESPONDENCE ADDRESS:

LEE & MORSE, P.C.

CUSTOMER NUMBER 27849

Telephone: (703) 207-0008
Fax Number: (703)-207-0003

In connection with this application, the following are enclosed:

APPLICATION ELEMENTS:

☒ Specification, Claims and Abstract - 30 TOTAL PAGES

(preferred arrangement:)

- Descriptive Title of the Invention
- Cross Reference to Related Applications
- Statement Regard Fed sponsored R&D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

☒ Drawings - 7 Total Sheets (depicting Figures 1-7)

- ☒ Declaration and Power of Attorney - 1 Total Sheets
- ☒ Newly executed (original or copy)
- ☐ Copy from a prior application (37 CFR 1.63(d))
(relates to continuation/divisional boxes completed) - NOTE: Box below
- ☐ Deletion of Inventor(s): Signed statement attached deleting inventor(s) named in prior application; see 37 CFR 1.63(d)(2) and 1.33(b)
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- ☐ Microfiche Computer Program (Appendix)
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- ☒ Application Data Sheet (ADS)
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Basic Fee				\$ 390.00
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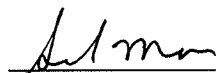
☒ The Commissioner is hereby authorized to charge any additional fees (or credit any overpayment) associated with the filing of this application to Deposit Account No. 50-1645.

Respectfully submitted,

LEE & MORSE, P.C.

February 20, 2013

Date



Susan S. Morse, Registration No. 35,292

**STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE
SAME**

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application claims priority under 35 U.S.C. § 119 to Korean Patent Application No. 10-2012-0104512, filed on September 20, 2012, in the Korean Intellectual Property Office, and entitled: “Stage Circuit and Organic Light Emitting Display Using the Same,” which is incorporated by reference herein in its entirety.

BACKGROUND

1. Field

[0002] Embodiments relate to a stage circuit and an organic light emitting display using the same.

2. Description of the Related Art

[0003] Recently, various flat panel displays (FPD) capable of reducing weight and volume that are disadvantages of cathode ray tubes (CRT) have been developed. The FPDs include liquid crystal displays (LCD), field emission displays (FED), plasma display panels (PDP), and organic light emitting displays.

[0004] Among the FPDs, the organic light emitting displays display images using organic light emitting diodes (OLED) that generate light by re-combination of electrons and holes. Organic light emitting displays have high response speeds and low power consumption. A typical organic light emitting display supplies currents corresponding to data signals to OLEDs using transistors formed in pixels so that the OLEDs may emit light.

[0005] Conventional organic light emitting display includes a data driver for supplying data signals to data lines, a scan driver for sequentially supplying scan signals to scan lines, and a pixel unit including a plurality of pixels coupled to the scan lines and the data lines.

[0006] The pixels included in the pixel unit are selected when the scan signals are supplied to the scan lines to receive the data signals from the data lines. The pixels that receive the data signals generate light components with predetermined brightness components corresponding to the data signals to display an image.

[0007] The scan driver includes stage circuits coupled to the scan lines. The stages supply the scan signals to the scan lines coupled thereto to correspond to signals supplied thereto.

SUMMARY

[0008] One or more embodiments are directed to providing a stage circuit, including an outputting unit having a first node and a second node, the outputting unit being configured to supply a voltage of a first power supply or a voltage of a third input terminal to an output terminal in accordance with voltages applied to the first node and the second node, a first driver configured to control the voltage of the second node in accordance with signals of a first input terminal, a second input terminal, and the third input terminal, and a second driver configured to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node.

[0009] The first input terminal may receive an output signal of a previous stage or a start signal. The second input terminal may receive a first clock signal. The third input terminal may receive a second clock signal. The first clock signal and the second clock signal have the same period and have phases that do not overlap. The first clock signal and the second clock signal may have a period of two horizontal periods $2H$ and may be supplied in different horizontal periods as low signals. The start signal may be supplied to overlap the first clock signal.

[0010] The first driver may include a first transistor positioned between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal, and a second transistor and a third transistor serially positioned between the second node and the first power supply. The gate electrode of the second transistor may be coupled to the third input terminal and the gate electrode of the third transistor may be coupled to the first node.

[0011] The outputting unit may include a fourth transistor positioned the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node, a fifth transistor coupled between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node, a first capacitor coupled between the second node and the output terminal, and a second capacitor coupled between the first node and the first power supply.

[0012] The second driver may include a sixth transistor positioned between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node, and a seventh transistor positioned between the first node and a

second power supply, having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.

[0013] The second driver may include a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node, and a seventh transistor coupled between the first node and the second input terminal, the seventh transistor being diode connected. The seventh transistor is coupled so that a current may flow from the first node to the second input terminal.

[0014] The stage circuit may further include a bidirectional driver coupled to the first input terminal, a fifth input terminal, and the first driver.

[0015] The bidirectional driver may include a tenth transistor between the first input terminal and the first driver, the tenth transistor being turned on when a first control signal is supplied, and an eleventh transistor between the fifth input terminal and the first driver, the eleventh transistor being turned on when a second control signal is supplied. The first input terminal may receive an output signal of a previous stage or a start signal and the fifth input terminal may receive an output signal of a next stage or a start signal.

[0016] One or more embodiments are directed to an organic light emitting display, including pixels positioned in regions partitioned by scan lines and data lines, a data driver for supplying data signals to the data lines, and a scan driver including stages coupled to the scan lines in order to supply scan signals to the scan lines. Each of the stages may include an outputting unit having a first node and a second node, the outputting unit being configured to supply a voltage of a first power supply or a voltage

of a third input terminal to an output terminal in accordance with voltages applied to the first node and the second node, a first driver configured to control the voltage of the second node in accordance with signals of a first input terminal, a second input terminal, and the third input terminal, and a second driver configured to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node.

[0017] A clock signal supplied to the third input terminal may be used as the scan signal. The first input terminal may receives a start signal or a scan signal of a previous stage. The second input terminals of odd stages may receive a first clock signal and the third input terminals of odd stages receive a second clock signal. The second input terminals of even stages may receive the second clock signal and the third input terminals of even stages receive the first clock signal. The first clock signal and the second clock signal may have the same period and may have phases that do not overlap.

[0018] The first driver may include a first transistor positioned between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal, and a second transistor and a third transistor serially positioned between the second node and the first power supply. The gate electrode of the second transistor may be coupled to the third input terminal and the gate electrode of the third transistor may be coupled to the first node.

[0019] The outputting unit may include a fourth transistor positioned the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node, a fifth transistor coupled between the output terminal and the third input

terminal, the fifth transistor having a gate electrode coupled to the second node, a first capacitor coupled between the second node and the output terminal, and a second capacitor coupled between the first node and the first power supply.

[0020] The second driver may include a sixth transistor positioned between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node, and a seventh transistor positioned between the first node and a second power supply, having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.

[0021] The second driver may include a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node, and a seventh transistor coupled between the first node and the second input terminal, the seventh transistor being diode connected. The seventh transistor is coupled so that a current may flow from the first node to the second input terminal.

[0022] The stage circuit may further include a bidirectional driver coupled to the first input terminal, a fifth input terminal, and the first driver.

[0023] The bidirectional driver may include a tenth transistor between the first input terminal and the first driver, the tenth transistor being turned on when a first control signal is supplied, and an eleventh transistor between the fifth input terminal and the first driver, the eleventh transistor being turned on when a second control signal is supplied. The first input terminal may receive an output signal of a previous stage or a start signal and the fifth input terminal may receive an output signal of a next stage or a start signal.

[0024] The start signal or the scan signal of the previous stage supplied to the first input terminal may overlap the clock signal supplied to the second input terminal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] Features will become apparent to those of ordinary skill in the art by describing in detail exemplary embodiments with reference to the attached drawings in which:

[0026] FIG. 1 illustrates a view of an organic light emitting display according to an embodiment;

[0027] FIG. 2 illustrates a view of an embodiment of the scan driver illustrated in FIG. 1;

[0028] FIG. 3 illustrates a circuit diagram of a first embodiment of the stages illustrated in FIG. 2;

[0029] FIG. 4 illustrates a waveform diagram of a method of driving the stage circuits illustrated in FIG. 3;

[0030] FIG. 5 illustrates a waveform diagram of simulation results of the stage circuits of FIG. 3;

[0031] FIG. 6 illustrates a circuit diagram of stages according to a second embodiment; and

[0032] FIG. 7 illustrates a circuit diagram of stage circuits according to a third embodiment.

DETAILED DESCRIPTION

[0033] Example embodiments will now be described more fully hereinafter with reference to the accompanying drawings; however, they may be embodied in different

forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey exemplary implementations to those skilled in the art. Like reference numerals refer to like elements throughout.

It will also be understood that when an element is referred to as being “between”, “connected to”, or “coupled to” another element, it can be directly between, connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being “directly between,” “directly connected to”, or “directly coupled to” another element, there are no intervening elements present.

Hereinafter, a stage circuit and an organic light emitting display using the same will be described in detail as follows with reference to FIGs. 1 to 7 in which exemplary embodiments by which those who skilled in the art may easily perform the present inventive concept are included.

[0034] FIG. 1 illustrates a view of an organic light emitting display according to an embodiment. Referring to FIG. 1, the organic light emitting display according to the embodiment includes a pixel unit 40 having pixels 30 positioned at the intersections of scan lines S1 to Sn and data lines D1 to Dm, a scan driver 10 for driving the scan lines S1 to Sn, a data driver 20 for driving the data lines D1 to Dm, and a timing controller 50 for controlling the scan driver 10 and the data driver 20.

[0035] The scan driver 10 supplies scan signals to the scan lines S1 to Sn. For example, the scan driver 10 may sequentially supply the scan signals to the scan lines S1 to Sn. In this case, the pixels 30 are selected in units of horizontal lines. For this purpose, the

scan driver 10 includes a stage circuit (shown in FIG. 2) coupled to the scan lines S1 to Sn.

[0036] The data driver 20 supplies data signals to the data lines D1 to Dm in synchronization with the scan signals. Then, voltages corresponding to the data signals are charged in the pixels 30 selected by the scan signals.

[0037] The timing controller 50 controls the scan driver 10 and the data driver 20. In addition, the timing controller 50 transmits data (not shown) from the outside to the data driver 20.

[0038] The pixels 30 are selected when the scan signals are supplied to charge the voltages corresponding to the data signals and supply currents corresponding to the charged voltages to organic light emitting diodes (not shown) to generate light components with predetermined brightness components.

[0039] FIG. 2 illustrates a view of an embodiment of the scan driver illustrated in FIG. 1. In FIG. 2, for convenience, four stages will be illustrated.

[0040] Referring to FIG. 2, the scan driver 10 includes a plurality of stages ST1 to ST4. The stages ST1 to ST4 are coupled to the scan lines S1 to S4, respectively, and are driven in accordance with clock signals CLK1 and CLK2. The stages ST1 to ST4 may have the same circuit layout. Each of the stages ST1 to ST4 includes a first input terminal 101 to a third input terminal 103 and an output terminal 104.

[0041] The first input terminal 101 of each of the stages ST1 to ST4 receives the output signal, i.e., the scan signal, of a previous stage or a start signal SSP. For example, the first input terminal 101 of the first stage ST1 receives the start signal SSP and the first

input terminals 101 of the remaining stages ST2 to ST4 receive the output signal of the previous stage.

[0042] The second input terminal 102 of an i th (i is odd or even) stage ST i receives the first clock signal CLK1 and the third input terminal 103 of the i th stage ST i receives the second clock signal CLK2. The second input terminal 102 of an $(i+1)$ th stage ST i receives the second clock signal CLK2 and the third input terminal 103 of the $(i+1)$ th stage ST i receives the first clock signal CLK1.

[0043] The first clock signal CLK1 and the second clock signal CLK2 have the same period and have phases that do not overlap. For example, when a period in which a scan signal is supplied to one scan line is referred to as a 1 horizontal period 1H, the clock signals CLK1 and CLK2 have periods of 2H and are supplied in different horizontal periods. In particular, times when the first and second clock signals CLK1 and CLK2 are supplied, e.g., the first and second clock signals CLK1 and CLK2 have a low level, do not overlap, although times when the first and second clock signals CLK1 and CLK2 are not supplied may overlap, e.g., both the first and second clock signals CLK1 and CLK2 may have a high level at the same time.

[0044] FIG. 3 illustrates a circuit diagram of a first embodiment of the stages illustrated in FIG. 2. In FIG. 3, for convenience, the first stage ST1 and the second stage ST2 will be illustrated. In FIG. 3, transistors are PMOS transistors. However, embodiments are not limited to the above. For example, the transistors may be NMOS transistors. Referring to FIG. 3, the stage ST1 according to the first embodiment includes a first driver 210, a second driver 220, and an outputting unit 230.

[0045] The outputting unit 230 controls a voltage supplied to the output terminal 104 in accordance with voltages applied to a first node N1 and a second node N2. For this purpose, the outputting unit 230 includes a fourth transistor M4, a fifth transistor M5, a first capacitor C1, and a second capacitor C2.

[0046] The fourth transistor M4 is positioned between a first power supply VDD and the output terminal 104. A gate electrode of the fourth transistor M4 is coupled to the first node N1. The fourth transistor M4 controls coupling between the first power supply VDD and the output terminal 104 in accordance with the voltage applied to the first node N1. Here, the first power supply VDD is set as a gate off voltage, for example, a high level voltage.

[0047] The fifth transistor M5 is positioned between the output terminal 104 and the third input terminal 103. A gate electrode of the fifth transistor M5 is coupled to the second node N2. The fifth transistor M5 controls coupling between the output terminal 104 and the third input terminal 103 in accordance with the voltage applied to the second node N2.

[0048] The first capacitor C1 is coupled between the second node N2 and the output terminal 104. The first capacitor C1 charges the voltage corresponding to turn on and off of the fifth transistor M5.

[0049] The second capacitor C2 is coupled between the first node N1 and the first power supply VDD. The second capacitor C2 charges the voltage applied to the first node N1.

[0050] The first driver 210 controls the voltage of the second node N2 in accordance with signals supplied to the first input terminal 101 to the third input terminal 103. For this purpose, the first driver 210 includes a first transistor M1, a second transistor M2, and a third transistor M3.

[0051] The first transistor M1 is positioned between the first input terminal 101 and the second node N2. A gate electrode of the first transistor M1 is coupled to the second input terminal 102. The first transistor M1 controls coupling between the first input terminal 101 and the second node N2 in accordance with the voltage supplied to the second input terminal 102.

[0052] The second transistor M2 and the third transistor M3 are serially coupled between the second node N2 and the first power supply VDD. In particular, the second transistor M2 is positioned between the third transistor M3 and the second node N2. A gate electrode of the second transistor M2 is coupled to the third input terminal 103. The second transistor M2 controls coupling between the third transistor M3 and the second node N2 in accordance with the voltage supplied to the third input terminal 103.

[0053] The third transistor M3 is positioned between the second transistor M2 and the first power supply VDD. A gate electrode of the third transistor M3 is coupled to the first node N1. The third transistor M3 controls coupling between the second transistor M2 and the first power supply VDD in accordance with the voltage of the first node N1.

[0054] The second driver 220 controls the voltage of the first node N1 in accordance with signals supplied to the second input terminal 102 and the second node N2. For this

purpose, the second driver 220 includes a sixth transistor M6 and a seventh transistor M7.

[0055] The sixth transistor M6 is positioned between the first node N1 and the second input terminal 102. A gate electrode of the sixth transistor M6 is coupled to the second node N2. The sixth transistor M6 controls coupling between the first node n1 and the second input terminal 102 in accordance with the voltage of the second node N2.

[0056] The seventh transistor M7 is positioned between the first node N1 and a second power supply VSS. A gate electrode of the seventh transistor M7 is coupled to the second input terminal 102. The seventh transistor M7 controls coupling between the first node N1 and the second power supply VSS in accordance with the voltage of the second input terminal 102. Here, the second power supply VSS is set as a gate on voltage, e.g., a low level voltage.

[0057] FIG. 4 illustrates a waveform diagram of a method of driving the stage circuits illustrated in FIG. 3. In FIG. 4, for convenience, operation processes will be described using the first stage ST1.

[0058] Referring to FIG. 4, the first clock signal CLK1 and the second clock signal CLK2 have two horizontal periods and are supplied in different horizontal periods. The start signal SSP (or the output signal of the previous stage) is supplied in synchronization with the clock signal CLK1 or CLK2 supplied to the second input terminal 102.

[0059] In detail, during a third horizontal period, the start signal SSP is supplied in synchronization with the first clock signal CLK1. When the first clock signal CLK1 is

supplied, the first transistor M1 and the seventh transistor M7 are turned on. When the first transistor M1 is turned on, the first input terminal 101 and the second node N2 are electrically coupled to each other. In this case, the second node N2 is set to be at a low voltage by the start signal SSP supplied to the first input terminal 101. When the second node N2 is set to be at the low voltage, the fifth transistor M5 and the sixth transistor M6 are turned on.

[0060] When the fifth transistor M5 is turned on, the third input terminal 103 and the output terminal 104 are electrically coupled to each other. Here, the third input terminal 103 is set to be at a high voltage, i.e., the second clock signal CLK2, so that the high voltage is output to the output terminal 104. When the sixth transistor M6 is turned on, the second input terminal 102 and the first node N1 are electrically coupled to each other. Then, the voltage of the first clock signal CLK1 supplied to the second input terminal 102, that is, a low voltage is supplied to the first node N1. Additionally, since the seventh transistor M7 is turned on, the voltage of the second power supply VSS is supplied to the first node N1. Here, the voltage of the second power supply VSS is set as the same voltage as (or a similar voltage to) the first clock signal CLK1 so that the first node N1 stably maintains the low voltage.

[0061] When the low voltage is supplied to the first node N1, the fourth transistor M4 and the third transistor M3 are turned on. When the third transistor M3 is turned on, the first power supply VDD and the second transistor M2 are electrically coupled to each other. Here, since the second transistor M2 is set to be in a turn off state, although the third transistor M3 is turned on, the second node N2 stably maintains the low voltage.

When the fourth transistor M4 is turned on, the voltage of the first power supply VDD is supplied to the output terminal 104. Here, the voltage of the first power supply VDD is set as the same voltage as the high voltage supplied to the third input terminal 103 so that the output terminal 104 stably maintains the high voltage.

[0062] Then, supply of the start signal SSP and the first clock signal CLK1 is stopped. When the supply of the first clock signal CLK1 is stopped, the first transistor M1 and the seventh transistor M7 are turned off. At this time, the fifth transistor M5 and the sixth transistor M6 maintain a turn on state in accordance with the voltage stored in the first capacitor C1.

[0063] When the fifth transistor M5 maintains the turn on state, the output terminal 104 and the third input terminal 103 maintain electric coupling. Therefore, the output terminal 104 receives the high voltage from the third input terminal 103.

[0064] On the other hand, since the sixth transistor M6 maintains the turn on state, the first node N1 and the second input terminal 102 are electrically coupled to each other. Here, the voltage of the second input terminal 102 is set as a high voltage as the supply of the first clock signal CLK1 is stopped so that the first node N1 is set to be at the high voltage. When the high voltage is supplied to the first node N1, the fourth transistor M4 is turned off.

[0065] Then, in the fourth horizontal period, the second clock signal CLK2 is supplied to the third input terminal 103. At this time, since the fifth transistor M5 is set to be in the turn on state, the second clock signal CLK2 supplied to the third input terminal 103

is supplied to the output terminal 104. In this case, the output terminal 104 outputs the second clock signal CLK2 as a scan signal to the scan line S1.

[0066] After the scan signal is output to the scan line S1, the first clock signal CLK1 is supplied in the fifth horizontal period. When the first clock signal CLK1 is supplied, the first transistor M1 and the seventh transistor M7 are turned on. When the fifth transistor M1 is turned on, the first input terminal 101 and the second node N2 are electrically coupled to each other. At this time, the start signal SSP is not supplied to the first input terminal 101 so that the first input terminal 101 is set to be at the high voltage. Therefore, when the first transistor M1 is turned on, the high voltage is supplied to the second node N2 so that the fifth transistor M5 and the sixth transistor M6 are turned off.

[0067] When the seventh transistor M7 is turned on, the second power supply VSS is supplied to the first node N1 so that the third transistor M3 and the fourth transistor M4 are turned on. When the fourth transistor M4 is turned on, the voltage of the first power supply VDD is supplied to the output terminal 104. Then, the fourth transistor M4 and the third transistor M3 maintain a turn on state in accordance with the voltage charged in the second capacitor C2 so that the output terminal 104 stably receives the voltage of the first power supply VDD.

[0068] In addition, when the second clock signal CLK2 is supplied, the second transistor M2 is turned on. At this time, since the third transistor M3 is set to be in the turn on state, the voltage of the first power supply VDD is supplied to the second node

N2. In this case, the fifth transistor M5 and the sixth transistor M6 stably maintain a turn off state.

[0069] The second stage ST2 receives the output signal (that is, the scan signal) of the first stage ST1 in synchronization with the second clock signal CLK2. In this case, the second stage ST2 outputs the scan signal to the second scan line S2 in synchronization with the first clock signal CLK1 during the fifth horizontal period. In practice, the stages ST repeat the above-described processes to sequentially output the scan signals to the scan lines.

[0070] FIG. 5 illustrates a waveform diagram of simulation results of the stage circuits of FIG. 3. Referring to FIG. 5, the scan driver using the stage circuits according to the first embodiment sequentially supplies the scan signals to the scan lines. In addition, the stage circuits according to the first embodiment output the scan signals to the scan lines using only the first clock signal CLK1 and the second clock signal CLK2. That is, the stage circuits according to the present invention do not receive additional initializing signals so that the width of the scan signals may be set to be large (for example, 1H).

[0071] FIG. 6 illustrates a circuit diagram of stages according to a second embodiment. In FIG. 6, the same elements as those of FIG. 3 will be denoted by the same reference numerals and detailed description thereof will not be repeated.

[0072] Referring to FIG. 6, in the stage according to the second embodiment, a second driver 220a includes a seventh transistor M7' diode-connected between the first node N1 and the second input terminal 102. That is, the seventh transistor M7' is diode-connected so that a current may flow from the first node N1 to the second input terminal

102. In this case, when a low voltage is supplied to the second input terminal 102, the voltage of the first node N1 is reduced to the low voltage. Since the other operation processes are the same as the operation processes of the stage according to the first embodiment, the operation processes will not be repeated.

[0073] FIG. 7 illustrates a circuit diagram of stage circuits according to a third embodiment. In FIG. 7, the same elements as those of FIG. 3 are denoted by the same reference numerals and detailed description thereof will not be repeated.

[0074] Referring to FIG. 7, the stage circuit according to the third embodiment further includes a bidirectional driver 240. The bidirectional driver 240 performs control so that the scan signal may be supplied in a first direction (from the first scan line S1 to the nth scan line Sn) or in a second direction (from the nth scan line Sn to the first scan line S1). For this purpose, the bidirectional driver 240 includes a 10th transistor M10 and an 11th transistor M11.

[0075] The 10th transistor M10 is coupled between the first input terminal 101 and the first driver 210. The 10th transistor M10 is turned on when a first control signal CS1 is supplied. Here, the first input terminal 101 receives the scan signal of a previous stage (or the start signal).

[0076] The 11th transistor M11 is coupled between a fifth input terminal 105 and the first driver 210. The 11th transistor M11 is turned on when a second control signal CS2 is supplied. Here, the fifth input terminal 105 receives the scan signal of a next stage (or the start signal).

[0077] In describing operation processes, when the first control signal CS1 is supplied, the 10th transistor M10 is turned on. When the 10th transistor M10 is turned on, the stages are driven in accordance with the scan signal of the previous stage so that the scan signals are sequentially output in the first direction.

[0078] When the second control signal CS2 is supplied, the 11th transistor M11 is turned on. When the 11th transistor M11 is turned on, the stages are driven in accordance with the scan signals of the next stage so that the scan signals are output in the second direction. Since the other driving processes are the same as the driving processes of the stage according to the first embodiment, detailed description thereof will not be repeated.

[0079] By way of summation and review, embodiments provide stages having a reduced number of transistors and that output scan signals only using first and second clock signals. In contrast, conventional stage circuits includes a plurality of transistors, e.g., at least ten transistors, to supply the scan signals and/or require use of initializing signal in addition to the first and second clock signals. When a number of transistors in a stage increases, process yield deteriorates, so that stability of driving is deteriorated. When more initializing signals are required, there is less time for supplying scan signals, thereby reducing stability. When a number of transistors is increased and/or more initializing signals are required, complexity increases. Therefore, stages according to embodiments, and an organic light emitting display using the same, improve stability and reduce complexity.

[0080] Example embodiments have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. In some instances, as would be apparent to one of ordinary skill in the art as of the filing of the present application, features, characteristics, and/or elements described in connection with a particular embodiment may be used singly or in combination with features, characteristics, and/or elements described in connection with other embodiments unless otherwise specifically indicated. Accordingly, it will be understood by those of skill in the art that various changes in form and details may be made without departing from the spirit and scope of the present invention as set forth in the following claims.

WHAT IS CLAIMED IS:

1. A stage circuit, comprising:

an outputting unit having a first node and a second node, the outputting unit being configured to supply a voltage of a first power supply or a signal of a third input terminal to an output terminal in accordance with voltages applied to the first node and the second node;

a first driver configured to control the voltage of the second node in accordance with signals of a first input terminal, a second input terminal, and the third input terminal; and

a second driver configured to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node.

2. The stage circuit as claimed in claim 1,

wherein the first input terminal receives an output signal of a previous stage or a start signal,

wherein the second input terminal receives a first clock signal, and

wherein the third input terminal receives a second clock signal.

3. The stage circuit as claimed in claim 2,

wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap.

4. The stage circuit as claimed in claim 3,
wherein the first clock signal and the second clock signal have a period equal to two horizontal periods 2H and are supplied in different horizontal periods as low signals.
5. The stage circuit as claimed in claim 2, wherein the start signal is supplied to overlap the first clock signal.
6. The stage circuit as claimed in claim 2, wherein the first driver includes:
a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and
a second transistor and a third transistor serially positioned between the second node and the first power supply,
wherein a gate electrode of the second transistor is coupled to the third input terminal, and
wherein a gate electrode of the third transistor is coupled to the first node.
7. The stage circuit as claimed in claim 2, wherein the outputting unit includes:
a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node;

a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node;

a first capacitor between the second node and the output terminal; and

a second capacitor between the first node and the first power supply.

8. The stage circuit as claimed in claim 2, wherein the second driver includes:

a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and

a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.

9. The stage circuit as claimed in claim 2, wherein the second driver includes:

a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and

a seventh transistor between the first node and the second input terminal, the seventh transistor being diode connected.

10. The stage circuit as claimed in claim 9, wherein the seventh transistor is coupled so that a current flows from the first node to the second input terminal.

11. The stage circuit as claimed in claim 1, further comprising a bidirectional driver coupled to the first input terminal, a fifth input terminal, and the first driver.

12. The stage circuit as claimed in claim 11, wherein the bidirectional driver includes:

a tenth transistor positioned between the first input terminal and the first driver, the tenth transistor being turned on when a first control signal is supplied; and

an eleventh transistor positioned between the fifth input terminal and the first driver, the eleventh transistor being turned on when a second control signal is supplied.

13. The stage circuit as claimed in claim 12, wherein the first input terminal receives an output signal of a previous stage or a start signal, and

wherein the fifth input terminal receives an output signal of a next stage or a start signal.

14. An organic light emitting display, comprising:
pixels positioned in regions partitioned by scan lines and data lines;
a data driver for supplying data signals to the data lines; and

a scan driver including stages coupled to the scan lines in order to supply scan signals to the scan lines,

wherein each of the stages includes:

an outputting unit having a first node and a second node, the outputting unit being configured to supply a voltage of a first power supply or a signal of a third input terminal to an output terminal in accordance with voltages applied to the first node and the second node,

a first driver configured to control the voltage of the second node in accordance with signals of a first input terminal, a second input terminal, and the third input terminal, and

a second driver configured to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node.

15. The organic light emitting display as claimed in claim 14, wherein a clock signal supplied to the third input terminal is used as the scan signal.

16. The organic light emitting display as claimed in claim 14, wherein the first input terminal receives a scan signal of a previous stage or a start signal.

17. The organic light emitting display as claimed in claim 16,
wherein second input terminals of odd stages receive a first clock signal and third input terminals of odd stages receive a second clock signal, and

wherein second input terminals of even stages receive the second clock signal and third input terminals of even stages receive the first clock signal.

18. The organic light emitting display as claimed in claim 17, wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap.

19. The organic light emitting display as claimed in claim 17, wherein the first driver includes:

a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and

a second transistor and a third transistor serially positioned between the second node and the first power supply,

wherein a gate electrode of the second transistor is coupled to the third input terminal, and

wherein a gate electrode of the third transistor is coupled to the first node.

20. The organic light emitting display as claimed in claim 17, wherein the outputting unit includes:

a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node;

a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node;
a first capacitor between the second node and the output terminal; and
a second capacitor between the first node and the first power supply.

21. The organic light emitting display as claimed in claim 17, wherein the second driver includes:

a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and

a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.

22. The organic light emitting display as claimed in claim 17, wherein the second driver includes:

a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and

a seventh transistor between the first node and the second input terminal, the seventh transistor being diode connected.

23. The organic light emitting display as claimed in claim 22, wherein the seventh transistor is coupled so that a current flows from the first node to the second input terminal.

24. The organic light emitting display as claimed in claim 14, further comprising a bidirectional driver coupled to the first input terminal, a fifth input terminal, and the first driver.

25. The organic light emitting display as claimed in claim 24, wherein the bidirectional driver includes:

a tenth transistor between the first input terminal and the first driver, the tenth transistor being turned on when a first control signal is supplied; and

an eleventh transistor between the fifth input terminal and the first driver, the eleventh transistor being turned on when a second control signal is supplied.

26. The organic light emitting display as claimed in claim 25, wherein the first input terminal receives an output signal or a start signal of a previous stage, and

wherein the fifth input terminal receives an output signal or a start signal of a next stage.

27. The organic light emitting display as claimed in claim 17, wherein the scan signal of the previous stage or the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal.

ABSTRACT OF THE DISCLOSURE

A stage circuit includes an outputting unit having a first node and a second node, the output unit configured to supply a voltage of a first power supply or a voltage of a third input terminal to an output terminal in accordance with voltages applied to the first node and the second node, a first driver configured to control the voltage of the second node in accordance with signals of a first input terminal, a second input terminal, and the third input terminal, and a second driver configured to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node.

FIG. 1

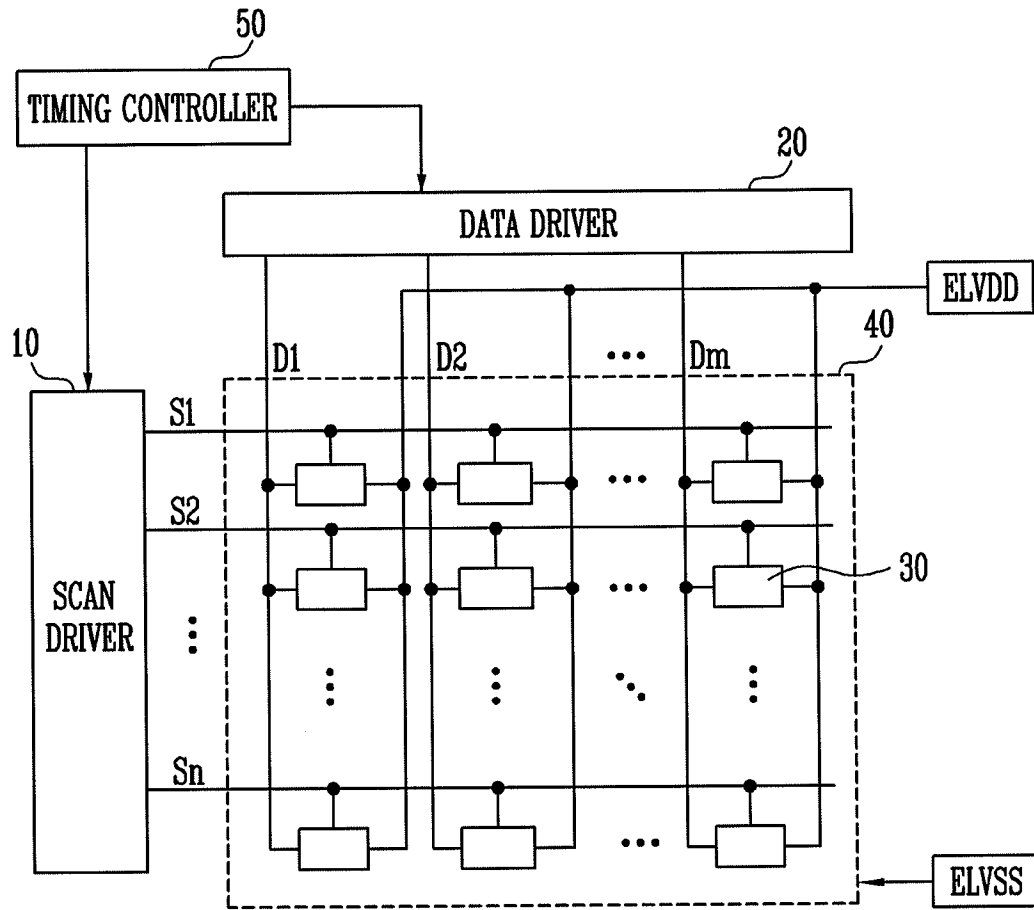


FIG. 2

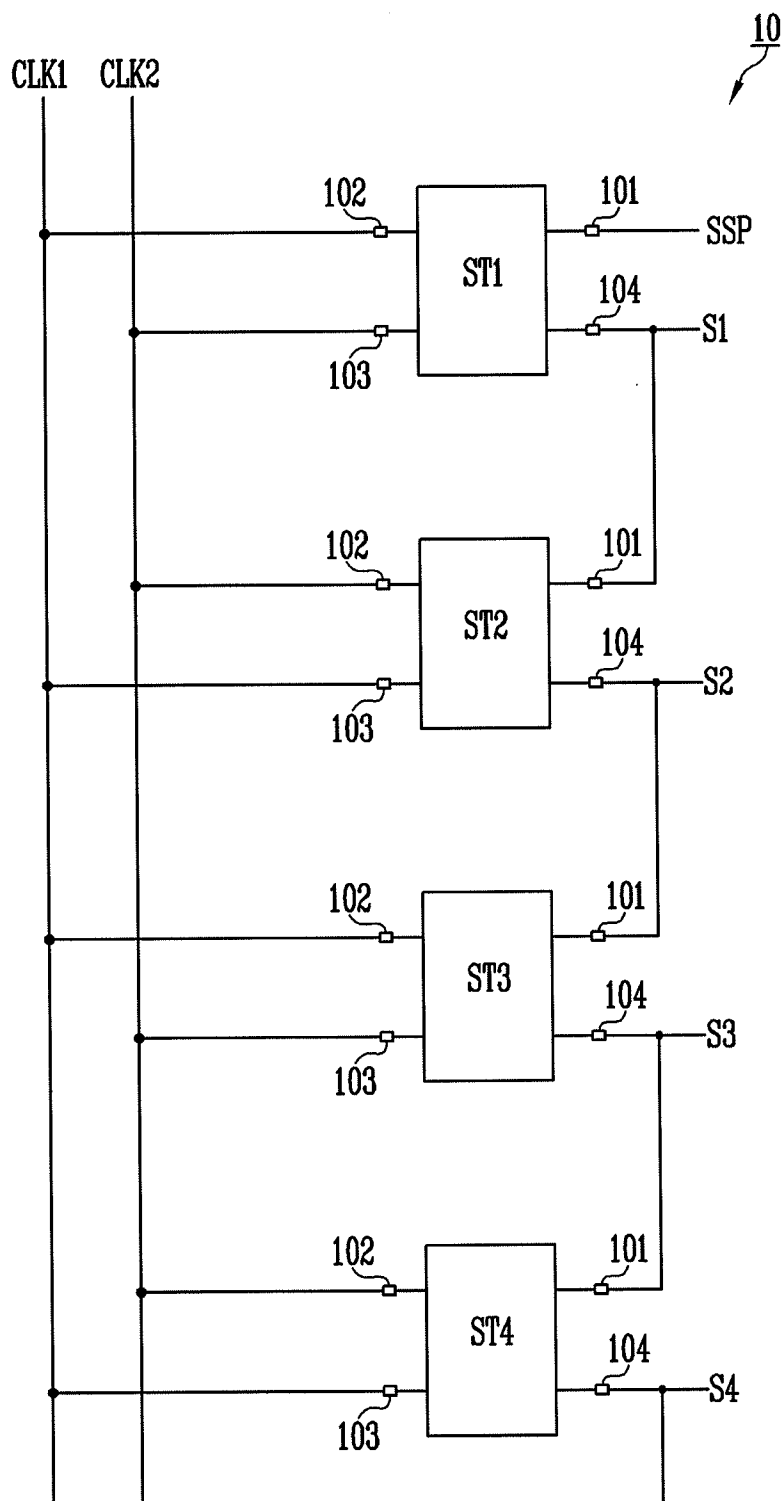


FIG. 3

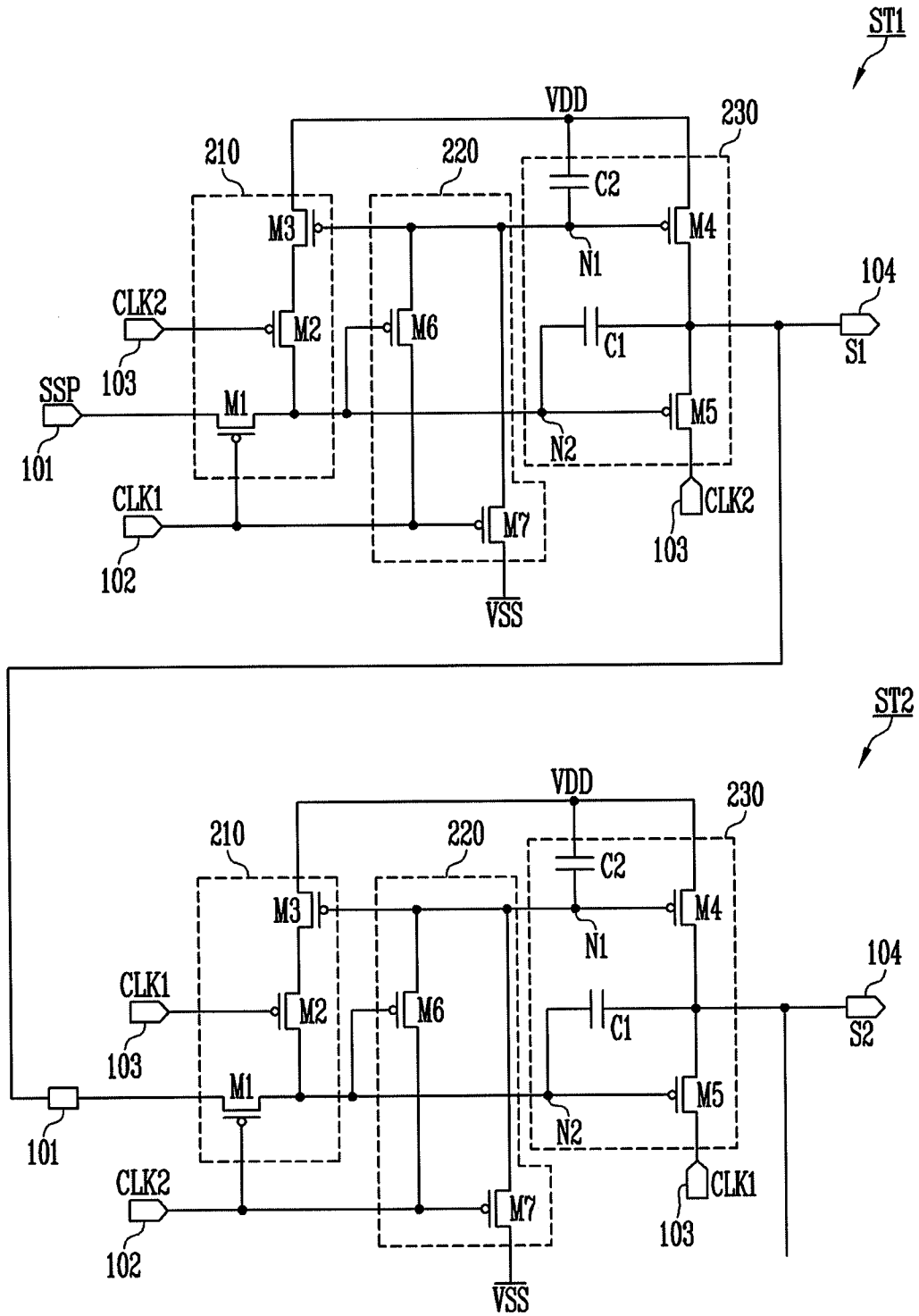


FIG. 4

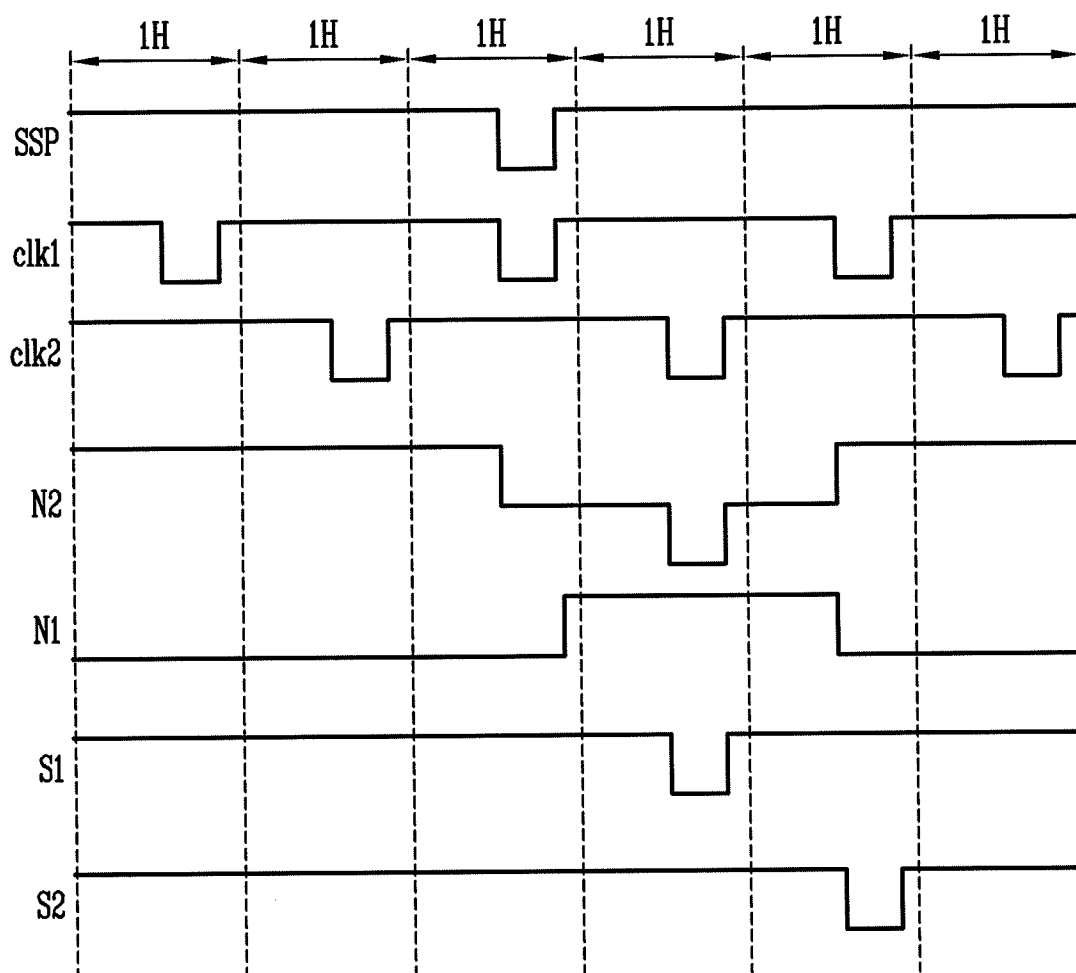


FIG. 5

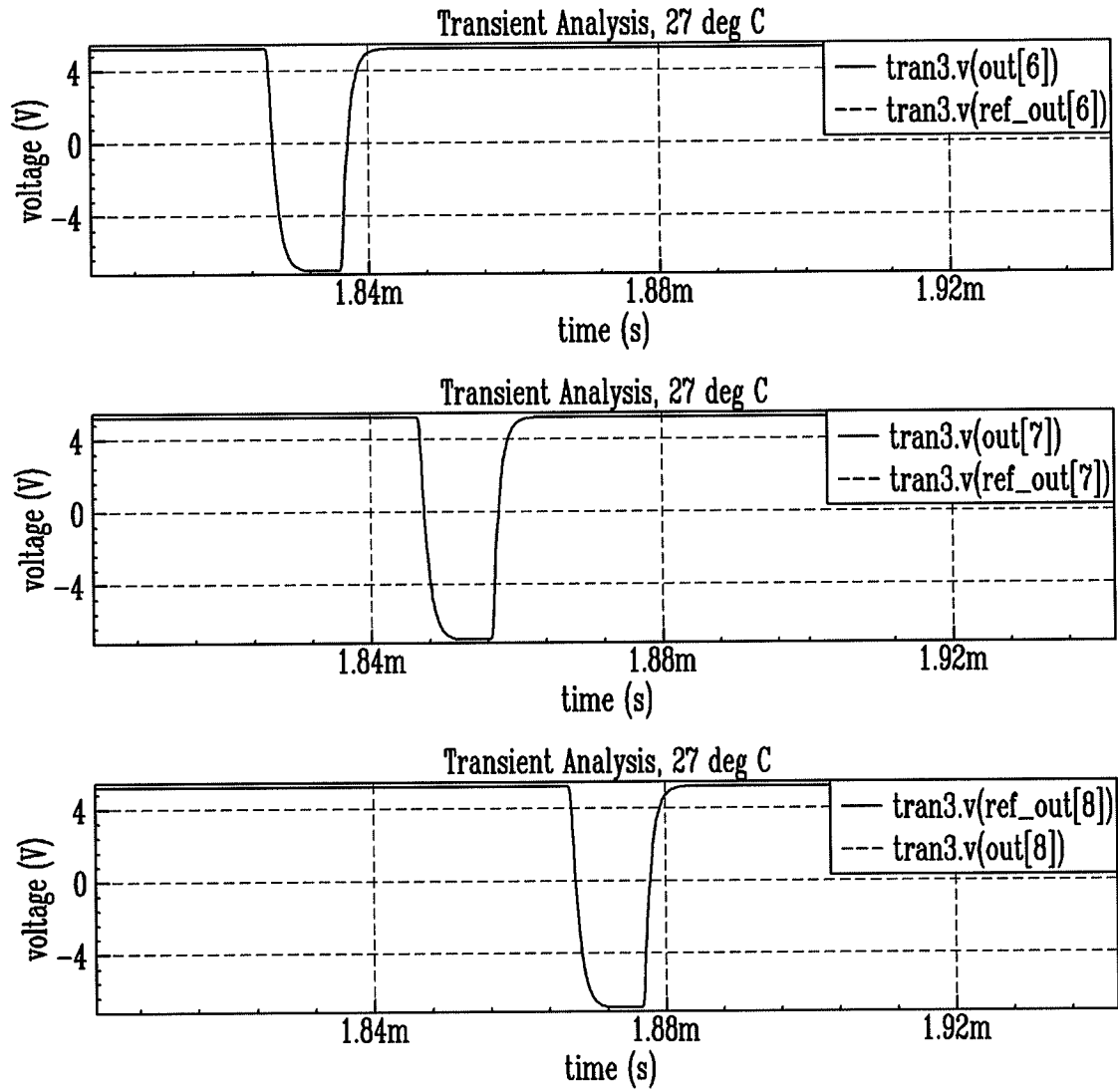


FIG. 6

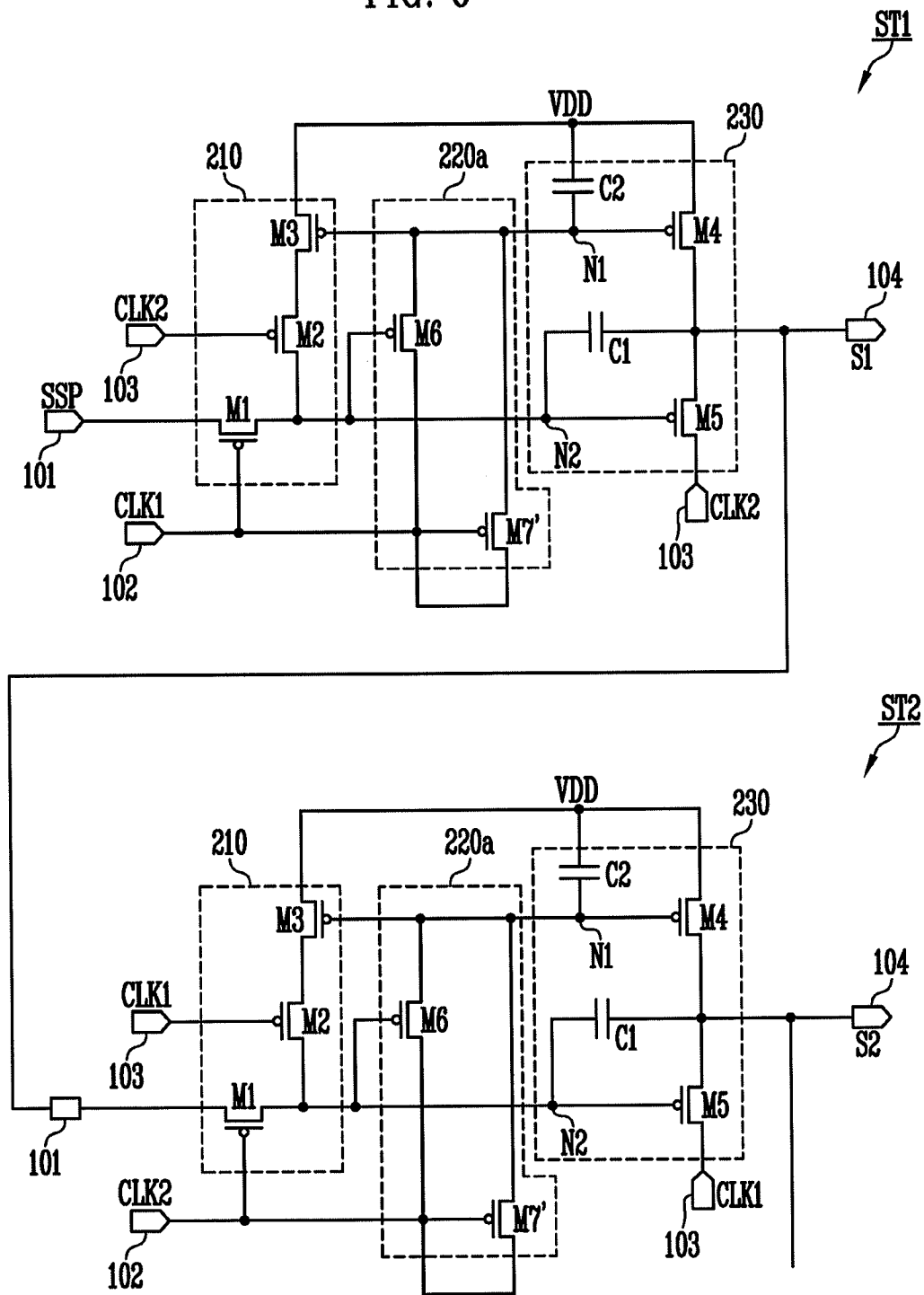
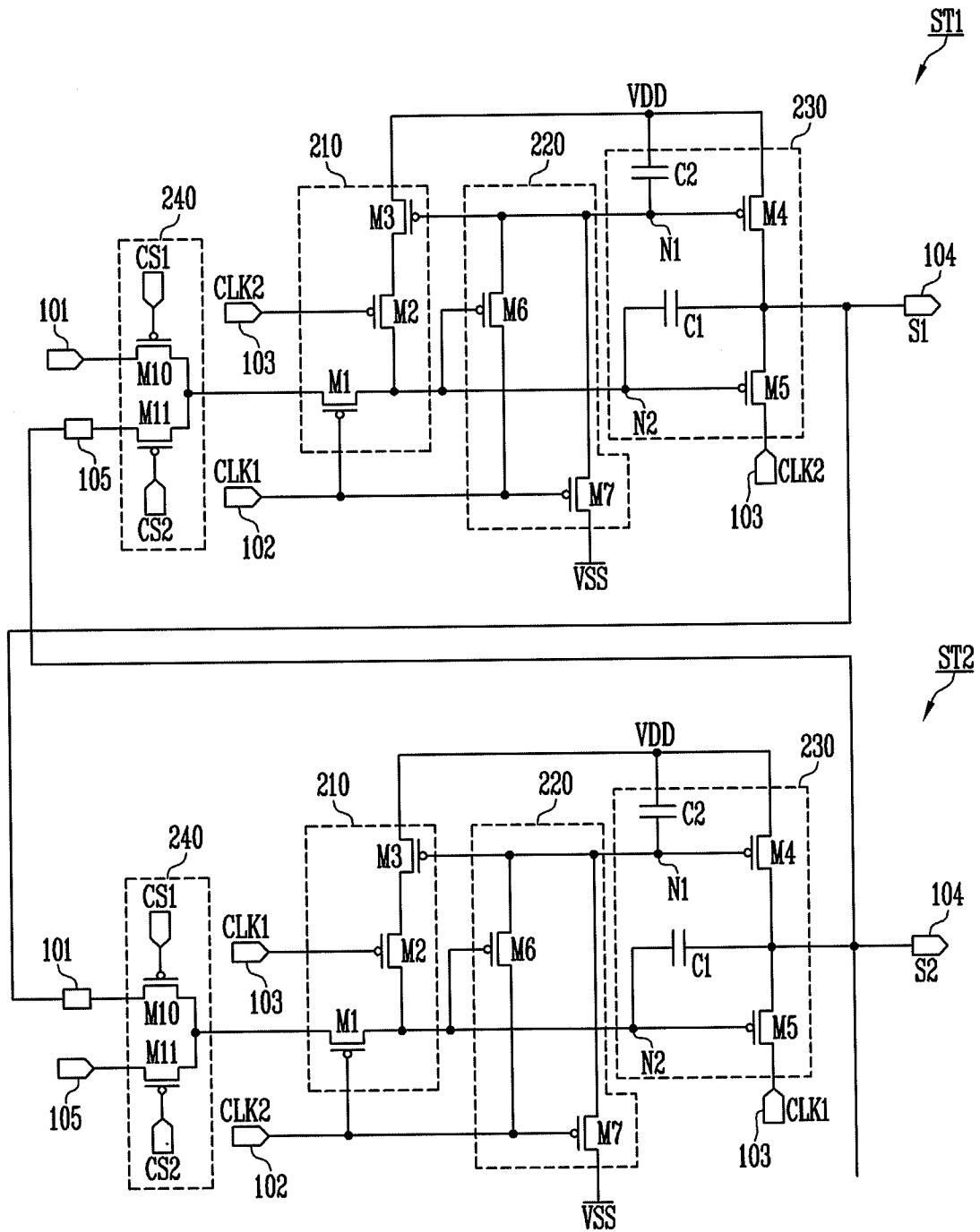


FIG. 7



**DECLARATION (37 C.F.R. § 1.63) AND POWER OF ATTORNEY
FOR APPLICATION USING AN APPLICATION DATA SHEET (37 C.F.R. § 1.76)**

Title of Invention:	STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME
------------------------	---

As the below named inventor(s), I/we hereby declare that:

This declaration is directed to the application attached hereto, unless the following box is checked:

☐ United States application or PCT international application number _____
filed on _____
☐ As amended on _____ (if applicable);

The above-identified application was made or authorized to be made by me/us.

I/we believe that I/we am/are the original inventor/original joint inventors of the subject matter which is claimed and for which patent is sought.

I/we hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than (5) years, or both.

I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referenced above.

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56.

POWER OF ATTORNEY: I/we hereby appoint as my attorneys, with full powers of substitution and revocation, to prosecute this application and transact all business in the Patent and Trademark Office practitioners associated with CUSTOMER NUMBER 27849.

CORRESPONDENCE ADDRESS: Direct all correspondence to the address associated with CUSTOMER NUMBER 27849: LEE & MORSE, P.C., 3141 FAIRVIEW PARK DRIVE, SUITE 500, FALLS CHURCH, VIRGINIA 22042. Address all telephone communications to Eugene M. Lee at (703) 207-0008.

Legal Name of First or Sole Inventor Hwan-Soo JANG	Date (mm/dd/yyyy) February 8, 2013
Signature: Hwan-Soo JANG	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No. 304/1043

In re the Application of:

Hwan-Soo JANG

Serial No.

Filed: February 20, 2013

For: STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE
SAME

CLAIM FOR CONVENTION PRIORITY
and REQUEST TO RETRIEVE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA. 22313-1450

Commissioner:

The benefit of the filing date of the following prior foreign application filed in the following foreign country is hereby requested, and the right of priority provided in 35 U.S.C. § 119 is hereby claimed.

Korean Application No. 10-2012-0104512 filed September 20, 2012

The USPTO is requested to retrieve an electronic copy of each of the above documents from the KIPO (participating foreign intellectual property office).

Respectfully submitted,

LEE & MORSE, P.C.

February 20, 2013
Date


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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Hwan-Soo JANG

Serial No.

Filed: February 20, 2013

For: STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING
THE SAME

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §1.56

Mail Stop: AMENDMENT
Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

Submitted herewith on Form PTO/SB/08 is a listing of a document(s) known to applicant in order to comply with applicant's duty of disclosure pursuant to 37 C.F.R. §1.56.

☒ A copy of each listed non-U.S. patent and/or patent publication and cited literature is being submitted to comply with the provisions of 37 C.F.R. §§1.97 & 1.98. [Box checked if applicable.]

* * *

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application. Applicant does not waive any rights to take any action that would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* prior art reference against the claims of the present application.

- ☒ The listed document(s) is/are being submitted in compliance with 37 C.F.R. 1.97(b)(3): submission before the mailing date of the first action on the merits. [Box checked if applicable.]
- ☐ The foregoing document(s) came to applicant's attention during the prosecution of their corresponding _____ application. ☐ A copy of the _____ Search Report is also attached. [Box(es) checked if applicable.]

CERTIFICATION

- ☐ The undersigned hereby certifies in accordance with 37 CFR §1.97(e)(1) that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three (3) months prior to the filing of this Statement. [Box checked if applicable.]

* * *

Applicant respectfully requests that the listed document(s) be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO/SB/08 be returned in accordance with MPEP §609.

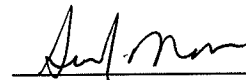
* * *

FEE PAYMENT

- ☐ The fee mandated by 37 C.F.R. §1.17(p) is believed applicable. [Box checked if applicable.]
- ☐ Attached is Form PTO-2038 in payment of this fee (\$180.00). [Box checked if applicable.]
- ☐ This fee may be charged to Deposit Account No. 50-1645. (A duplicate copy of this paper is enclosed.) [Box checked if applicable.]

Respectfully submitted,

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DEPOSIT ACCOUNT CHARGE AUTHORIZATION

If fee payment is enclosed, this amount is believed to be correct. However, the Director is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-1645.

Any additional fee(s) necessary to effect the proper and timely filing of the above-paper may also be charged to Deposit Account No. 50-1645.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	
	Filing Date	February 20, 2013
	First Named Inventor	Hwan-Soo JANG
	Art Unit	
(Multiple sheets used when necessary)	Examiner	
SHEET 1 of 1; February 20, 2013	Attorney Docket No.	304/1043

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1.	2011/0227884 A1	09-22-2011	CHUNG	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code-Number-Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T ¹
	2.	KR 10-2011-0104320 A*	09-22-2011	CHUNG	Family = US 2011/0227884 A1	

* with English Abstract

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ¹

IDENTIFICATION OF OFFICE ACTIONS AND/OR SEARCH REPORTS FROM RELATED APPLICATIONS	
A copy of each of the following document(s) is appended to the present IDS submission. Documents cited above, if any, may be identified therein. The following documents do not constitute "prior art references" but are included for informational purposes.	T ¹

Examiner Signature	Date Considered
Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

T¹ - Place a check mark in this area when an English language Translation is attached. Case No. IPR2023-01221



US 20110227884A1

(19) **United States**

(12) **Patent Application Publication**
Chung

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(43) **Pub. Date: Sep. 22, 2011**

(54) **SCAN DRIVER AND ORGANIC LIGHT
EMITTING DISPLAY USING THE SCAN
DRIVER**

Publication Classification

(51) **Int. Cl.**
G09G 5/00 (2006.01)

(52) **U.S. Cl.** 345/204

(57) **ABSTRACT**

(76) **Inventor:** **Kyung-Hoon Chung**, Yongin-City
(KR)

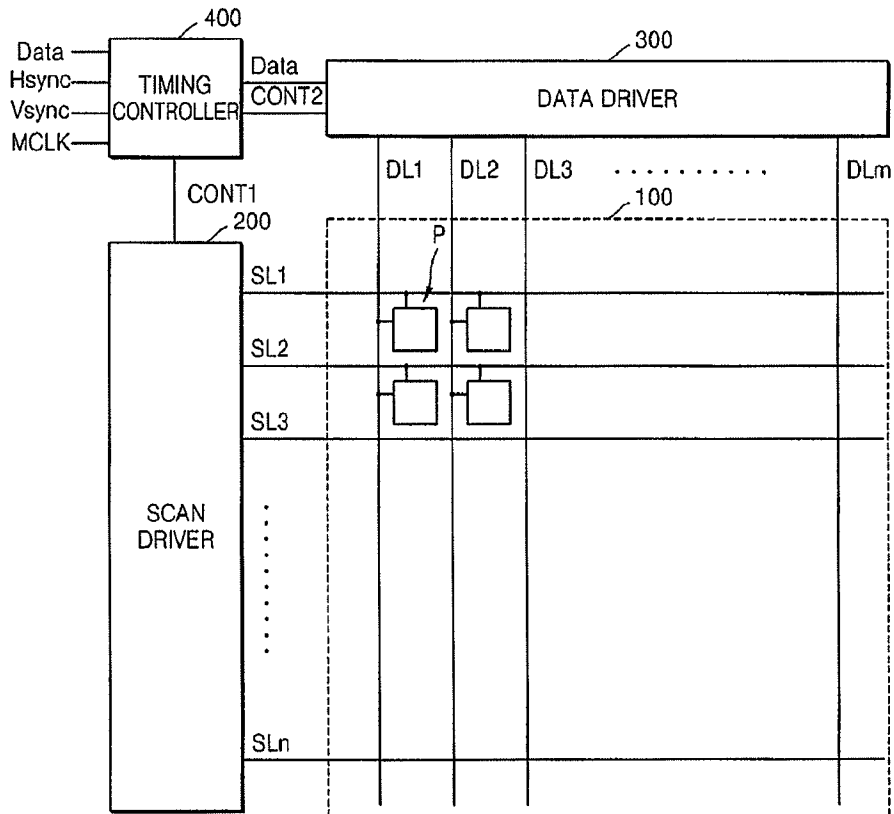
(21) **Appl. No.:** **12/904,976**

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(30) **Foreign Application Priority Data**

Mar. 16, 2010 (KR) 10-2010-0023401

A scan driver is coupled to a plurality of scan lines and includes a plurality of stages. Each of the stages is configured to sequentially receives clock signals that are phase delayed by two horizontal cycles or more from three of a plurality of clock lines, and output a scan signal having a pulse width of two horizontal cycles or more to a corresponding scan line. The scan signals are overlapped with each other by one horizontal cycle or more.





(19) 대한민국특허청(KR)
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(11) 공개번호 10-2011-0104320
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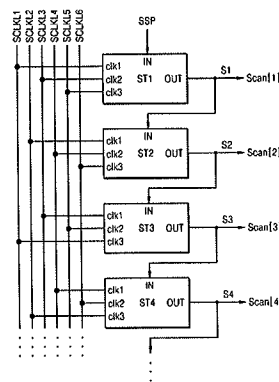
(54) 스캔 드라이버 및 이를 이용한 유기 발광 표시 장치

(57) 요약

스캔 드라이버 및 이를 이용한 유기 발광 표시 장치를 개시한다.

본 발명은 스캔 신호의 펄스 폭을 2수평주기 이상으로 증가시켜 유기발광패널을 구동함으로써 고품질의 영상을 제공할 수 있다.

대표도 - 도2



특허청구의 범위

청구항 1

다수의 스캔 라인과 연결되고, 다수의 클럭라인 중 3개의 클럭라인으로부터 2수평주기 이상 위상 지연된 클럭 신호들을 순차적으로 입력받아 해당 스캔 라인에 2수평주기 이상의 펄스 폭을 갖는 스캔 신호를 출력하는 다수의 스테이지들을 포함하며, 상기 스캔 신호들이 서로 1수평주기 이상 오버랩되는 것을 특징으로 하는 스캔 드라이버.

청구항 2

제1항에 있어서,

상기 다수의 클럭라인은 6상 클럭라인이고, 각 스테이지는 상기 6상 클럭라인 중 3개의 클럭라인으로부터 2수평주기 만큼씩 위상 지연된 3개의 클럭신호들을 순차적으로 입력받아 해당 스캔 라인에 2수평주기의 펄스 폭을 갖는 스캔 신호를 출력하고, 상기 스캔 신호들이 1수평주기 만큼씩 서로 오버랩되는 것을 특징으로 하는 스캔 드라이버.

청구항 3

제1항에 있어서,

상기 다수의 클럭라인은 9상 클럭라인이고, 각 스테이지는 상기 9상 클럭라인 중 3개의 클럭라인으로부터 3수평주기 만큼씩 위상 지연된 3개의 클럭신호들을 순차적으로 입력받아 해당 스캔 라인에 3수평주기의 펄스 폭을 갖는 스캔 신호를 출력하고, 상기 스캔 신호들이 2수평주기 만큼씩 서로 오버랩되는 것을 특징으로 하는 스캔 드라이버.

청구항 4

제1항에 있어서,

상기 다수의 클럭라인은 1수평주기 만큼씩 위상 지연된 클럭신호를 순차적으로 공급하는 것을 특징으로 하는 스캔 드라이버.

청구항 5

제1항에 있어서, 각 스테이지는

전단 스테이지의 스캔 신호 또는 최초 시작신호가 인가되는 입력단자에 게이트 전극이 연결되고 제1전원에 제1전극이 연결되고 제2노드에 제2전극이 연결된 제6스위칭소자;

제2클럭단자에 게이트 전극이 연결되고 상기 입력단자에 제1전극이 연결되고 제1노드에 제2전극이 연결된 제5스위칭소자;

제1클럭단자에 게이트 전극이 연결되고 상기 제2노드에 제1전극이 연결되고 제2전원에 제2전극이 연결된 제4스위칭소자;

상기 제2노드에 게이트 전극이 연결되고 상기 제1전원에 제1전극이 연결되고 상기 제1노드에 제2전극이 연결된 제3스위칭소자;

상기 제1노드에 게이트 전극이 연결되고 출력단자에 제1전극이 연결되고 제3클럭단자에 제2전극이 연결된 제2스위칭소자; 및

상기 제2노드에 게이트 전극이 연결되고 상기 제1전원에 제1전극이 연결되고 상기 출력단자에 제2전극이 연결된 제1스위칭소자;를 포함하는 것을 특징으로 하는 스캔 드라이버.

청구항 6

제5항에 있어서,

상기 전단 스테이지의 스캔 신호 또는 최초 시작 신호는 2수평주기 이상의 펄스 폭을 갖는 것을 특징으로 하는 스캔 드라이버.

청구항 7

제5항에 있어서,

상기 제1노드와 상기 출력단자 사이에 연결된 제1용량성소자와 상기 제1전원과 상기 제2노드 사이에 연결된 제2용량성소자;를 더 포함하는 것을 특징으로 하는 스캔 드라이버.

청구항 8

제5항에 있어서,

상기 제1스위칭소자 내지 상기 제6스위칭소자는 PMOS 트랜지스터인 것을 특징으로 하는 스캔 드라이버.

청구항 9

다수의 데이터 라인 및 다수의 스캔 라인이 서로 교차하여 정의된 다수의 화소를 구비하는 유기발광패널;

상기 다수의 데이터 라인과 연결되고, 상기 데이터 라인에 데이터 신호를 인가하는 데이터 드라이버; 및

상기 다수의 스캔 라인과 연결되고, 다수의 클럭라인 중 3개의 클럭라인으로부터 2수평주기 이상 위상 지연된 클럭신호들을 순차적으로 입력받아 상기 스캔 라인에 2수평주기 이상의 펄스 폭을 갖는 스캔 신호를 순차적으로 공급하며, 인접하는 스캔 신호들이 서로 1수평주기 이상 오버랩되는 스캔 드라이버;를 포함하는 것을 특징으로 하는 유기 발광 표시 장치.

청구항 10

제9항에 있어서,

상기 다수의 클럭라인은 6상 클럭라인이고, 각 스테이지는 상기 6상 클럭라인 중 3개의 클럭라인으로부터 2수평주기 만큼씩 위상 지연된 3개의 클럭신호들을 순차적으로 입력받아 해당 스캔 라인에 2수평주기의 펄스 폭을 갖는 스캔 신호를 출력하고, 상기 스캔 신호들이 1수평주기 만큼씩 서로 오버랩되는 것을 특징으로 하는 유기 발광 표시 장치.

청구항 11

제9항에 있어서,

상기 다수의 클럭라인은 9상 클럭라인이고, 각 스테이지는 상기 9상 클럭라인 중 3개의 클럭라인으로부터 3수평주기 만큼씩 위상 지연된 3개의 클럭신호들을 순차적으로 입력받아 해당 스캔 라인에 3수평주기의 펄스 폭을 갖는 스캔 신호를 출력하고, 상기 스캔 신호들이 2수평주기 만큼씩 서로 오버랩되는 것을 특징으로 하는 유기 발광 표시 장치.

청구항 12

제9항에 있어서,

상기 다수의 클럭라인은 1수평주기 만큼씩 위상 지연된 클럭신호를 순차적으로 공급하는 것을 특징으로 하는 유기 발광 표시 장치.

청구항 13

제9항에 있어서, 상기 스캔 드라이버는 상기 스캔 신호를 순차적으로 출력하는 다수의 스테이지를 포함하며, 각 스테이지는

전단 스테이지의 스캔 신호 또는 최초 시작신호가 인가되는 입력단자에 게이트 전극이 연결되고 제1전원에 제1전극이 연결되고 제2노드에 제2전극이 연결된 제6스위칭소자;

제2클럭단자에 게이트 전극이 연결되고 상기 입력단자에 제1전극이 연결되고 제1노드에 제2전극이 연결된 제5스위칭소자;

제1클럭단자에 게이트 전극이 연결되고 상기 제2노드에 제1전극이 연결되고 상기 제2전원에 제2전극이 연결된 제4스위칭소자;

상기 제2노드에 게이트 전극이 연결되고 상기 제1전원에 제1전극이 연결되고 상기 제1노드에 제2전극이 연결된 제3스위칭소자;

상기 제1노드에 게이트 전극이 연결되고 출력단자에 제1전극이 연결되고 제3클럭단자에 제2전극이 연결된 제2스위칭소자; 및

상기 제2노드에 게이트 전극이 연결되고 상기 제1전원에 제1전극이 연결되고 상기 출력단자에 제2전극이 연결된 제1스위칭소자;를 포함하는 것을 특징으로 하는 유기 발광 표시 장치.

청구항 14

제13항에 있어서,

상기 전단 스테이지의 스캔 신호 또는 최초 시작 신호는 2수평주기 이상의 펄스 폭을 갖는 것을 특징으로 하는 유기 발광 표시 장치.

청구항 15

제13항에 있어서,

상기 제1노드와 상기 출력단자 사이에 연결된 제1용량성소자와 상기 제1전원과 상기 제2노드 사이에 연결된 제2용량성소자;를 더 포함하는 것을 특징으로 하는 유기 발광 표시 장치.

명세서

기술 분야

[0001] 본 발명은 스캔 드라이버 및 이를 이용한 유기 발광 표시 장치에 관한 것으로서, 더욱 상세하게는, 비정상 스캔 신호 발생을 방지할 수 있는 스캔 드라이버 및 이를 이용한 유기 발광 표시 장치에 관한 것이다.

배경 기술

[0002] 유기 발광 표시 장치는 퍼스널 컴퓨터, 휴대전화기, PDA 등의 휴대 정보단말기 등의 표시장치나 각종 정보기기의 표시장치로서 사용되고 있다. 또한, 음극선관에 비교하여 무게와 부피가 작은 각종 발광 표시장치들이 개발되고 있으며, 특히 발광효율, 휘도 및 시야각이 뛰어나며 응답속도가 빠른 유기 발광 표시 장치가 주목받고 있다.

[0003] 종래의 유기 발광 표시 장치는 스캔 라인 및 스캔 라인과 교차하는 데이터 라인 사이에 전기적으로 연결된 화소들을 포함하는 유기발광패널, 스캔 라인을 구동하기 위한 스캔 드라이버 및 데이터 라인을 구동하기 위한 데이터 드라이버를 구비한다. 스캔 드라이버는 스캔 신호를 스캔 라인을 통해 유기발광패널로 순차적으로 공급하고 데이터 드라이버는 데이터 신호를 데이터 라인을 통해 유기발광패널로 순차적으로 공급한다. 유기발광패널은 데이터 라인과 스캔 라인에 전기적으로 연결되어 데이터 신호와 스캔 신호를 인가받아 발광하게 된다.

[0004] 대형 유기발광패널은 FHD(Full High-Definition) 이상의 해상도를 가지며, 120Hz 이상의 구동 주파수를 갖는다. 이때, 스캔 라인의 부하(load)가 커져 신호의 RC 딜레이(delay)가 증가하며, 수평 라인(Horizontal line) 수가 많고 주파수가 빨라서 1H(수평주기)의 스캔 타임(scan time)이 짧다는 문제가 있다. 이 경우 비정상적인 스캔 신호가 출력되어 화소에 정상적인 데이터 신호가 입력되지 못한다. 또한, 보상 화소 회로에서는 스캔 타임이 짧아지면, 보상 시간도 짧아져 정상적인 보상 동작이 이루어지지 않아 불균일한 화면의 원인이 된다.

[0005] 따라서, FHD 120Hz 이상의 유기발광패널을 구동시 짧은 스캔 타임에 의한 비정상 스캔 신호 발생을 방지하기 위해, 스캔 신호의 펄스 폭을 증가시켜 구동할 필요가 있다.

발명의 내용

해결하려는 과제

[0006] 본 발명은 비정상 스캔 신호 발생을 방지하고 균일한 화면을 제공할 수 있는 스캔 드라이버 및 이를 이용하는

유기 발광 표시 장치를 제공하기 위한 것이다.

과제의 해결 수단

- [0007] 본 발명의 바람직한 일 실시예에 따른 스캔 드라이버는, 다수의 스캔 라인과 연결되고, 다수의 클럭라인 중 3개의 클럭라인으로부터 2수평주기 이상 위상 지연된 클럭신호들을 순차적으로 입력받아 해당 스캔 라인에 2수평주기 이상의 펄스 폭을 갖는 스캔 신호를 출력하는 다수의 스테이지들을 포함하며, 상기 스캔 신호들이 서로 1수평주기 이상 오버랩되는 것을 특징으로 한다.
- [0008] 보다 바람직하게, 상기 다수의 클럭라인은 6상 클럭라인이고, 각 스테이지는 상기 6상 클럭라인 중 3개의 클럭라인으로부터 2수평주기 만큼씩 위상 지연된 3개의 클럭신호들을 순차적으로 입력받아 해당 스캔 라인에 2수평주기의 펄스 폭을 갖는 스캔 신호를 출력하고, 상기 스캔 신호들이 1수평주기 만큼씩 서로 오버랩될 수 있다.
- [0009] 보다 바람직하게, 상기 다수의 클럭라인은 9상 클럭라인이고, 각 스테이지는 상기 9상 클럭라인 중 3개의 클럭라인으로부터 3수평주기 만큼씩 위상 지연된 3개의 클럭신호들을 순차적으로 입력받아 해당 스캔 라인에 3수평주기의 펄스 폭을 갖는 스캔 신호를 출력하고, 상기 스캔 신호들이 2수평주기 만큼씩 서로 오버랩될 수 있다.
- [0010] 보다 바람직하게, 상기 다수의 클럭라인은 1수평주기 만큼씩 위상 지연된 클럭신호를 순차적으로 공급할 수 있다.
- [0011] 보다 바람직하게, 각 스테이지는, 전단 스테이지의 스캔 신호 또는 최초 시작신호가 인가되는 입력단자에 게이트 전극이 연결되고 제1전원에 제1전극이 연결되고 제2노드에 제2전극이 연결된 제6스위칭소자; 제2클럭단자에 게이트 전극이 연결되고 상기 입력단자에 제1전극이 연결되고 제1노드에 제2전극이 연결된 제5스위칭소자; 제1클럭단자에 게이트 전극이 연결되고 상기 제2노드에 제1전극이 연결되고 상기 제2전원에 제2전극이 연결된 제4스위칭소자; 상기 제2노드에 게이트 전극이 연결되고 상기 제1전원에 제1전극이 연결되고 상기 제1노드에 제2전극이 연결된 제3스위칭소자; 상기 제1노드에 게이트 전극이 연결되고 출력단자에 제1전극이 연결되고 제3클럭단자에 제2전극이 연결된 제2스위칭소자; 및 상기 제2노드에 게이트 전극이 연결되고 상기 제1전원에 제1전극이 연결되고 상기 출력단자에 제2전극이 연결된 제1스위칭소자;를 포함할 수 있다.
- [0012] 보다 바람직하게, 상기 전단 스테이지의 스캔 신호 또는 최초 시작 신호는 2수평주기 이상의 펄스 폭을 가질 수 있다.
- [0013] 보다 바람직하게, 상기 스테이지는, 상기 제1노드와 상기 출력단자 사이에 연결된 제1용량성소자와 상기 제1전원과 상기 제2노드 사이에 연결된 제2용량성소자;를 더 포함할 수 있다.
- [0014] 본 발명의 바람직한 일 실시예에 따른 유기 발광 표시 장치는, 다수의 데이터 라인 및 다수의 스캔 라인이 서로 교차하여 정의된 다수의 화소를 구비하는 유기발광패널; 상기 다수의 데이터 라인과 연결되고, 상기 데이터 라인에 데이터 신호를 인가하는 데이터 드라이버; 및 상기 다수의 스캔 라인과 연결되고, 다수의 클럭라인 중 3개의 클럭라인으로부터 2수평주기 이상 위상 지연된 클럭신호들을 순차적으로 입력받아 상기 스캔 라인에 2수평주기 이상의 펄스 폭을 갖는 스캔 신호를 순차적으로 공급하며, 인접하는 스캔 신호들이 서로 1수평주기 이상 오버랩되는 스캔 드라이버;를 포함할 수 있다.

발명의 효과

- [0015] 본 발명은 스캔 신호의 펄스 폭을 2수평주기(2H) 이상으로 증가시켜 구동할 수 있는 스캔 드라이버를 구비하여, FHD 120Hz 이상으로 유기발광표시패널을 구동할 때 짧은 스캔 타임에 의한 비정상 스캔 신호 발생을 방지하고 균일한 화면을 제공할 수 있다.

도면의 간단한 설명

- [0016] 도 1은 본 발명의 일 실시예에 따른 유기 발광 표시 장치의 구조를 개략적으로 도시한 회로도이다.
- 도 2는 본 발명의 일 실시예에 따른 스캔 드라이버의 개략적인 블록도이다.
- 도 3은 도 2의 스캔 드라이버의 동작을 나타내는 타이밍도이다.
- 도 4는 도 2에 도시된 스캔 드라이버에서 임의의 스테이지(Si)에 대한 구체적인 회로도이다.
- 도 5는 도 4의 임의의 스테이지의 동작을 나타내는 타이밍도이다.

도 6은 본 발명의 다른 실시예에 따른 스캔 드라이버의 개략적인 블록도이다.

도 7은 도 6의 스캔 드라이버의 동작을 나타내는 타이밍도이다.

발명을 실시하기 위한 구체적인 내용

- [0017] 이하 본 발명의 바람직한 실시예가 첨부된 도면들을 참조하여 설명될 것이다. 도면상의 동일한 부호는 동일한 요소를 지칭한다. 하기에서 본 발명을 설명함에 있어, 관련된 공지 기능 또는 구성에 대한 구체적인 설명이 본 발명의 요지를 불필요하게 흐릴 수 있다고 판단되는 경우에는 그 상세한 설명을 생략할 것이다.
- [0018] 도 1은 본 발명의 일 실시예에 따른 유기 발광 표시 장치의 구조를 개략적으로 도시한 회로도이다.
- [0019] 도 1을 참조하면, 본 발명의 유기 발광 표시 장치는 유기발광패널(100), 스캔 드라이버(200), 데이터 드라이버(300) 및 타이밍 컨트롤러(400)를 포함한다.
- [0020] 유기발광패널(100)은 다수의 스캔 라인(S1-Sn), 다수의 데이터 라인(D1-Dm) 및 다수의 화소(P)를 포함한다. 다수의 스캔 라인(S1-Sn)은 일정하게 이격되어 행으로 배열되며 각각 스캔 신호를 전달하고, 다수의 데이터 라인(D1-Dm)은 일정하게 이격되어 열로 배열되며 각각 데이터 신호를 전달한다. 다수의 스캔 라인(S1-Sn)과 다수의 데이터 라인(D1-Dm)은 매트릭스 형태로 배열되며, 이때 그 교차부에는 하나의 화소(P)가 형성된다. 이때, 화소(P)가 전류 기입형 화소인 경우에 데이터 신호는 전류이고, 전압 기입형 화소인 경우에 데이터 신호는 전압이다.
- [0021] 한편, 색 표시를 구현하기 위해서는 각 화소가 원색 중 하나의 색상을 고유하게 표시하거나 각 화소가 시간에 따라 번갈아 원색을 표시하게 하여, 이들 원색의 공간적 또는 시간적 합으로 원하는 색상이 인식되도록 한다. 원색의 예로는 적색(R), 녹색(G) 및 청색(B)을 들 수 있다. 이때, 시간적 합으로 색상을 표시하는 경우에는 한 화소에서 시간적으로 R, G 및 B 색상이 번갈아 표시되어서 한 색상이 구현된다. 그리고 공간적 합으로 색상을 표시하는 경우에는 R 화소, G 화소 및 B 화소의 세 화소에 의해 한 색상이 구현되므로, 각 화소를 부화소라 부르고 세 개의 부화소를 하나의 화소라 부르기도 한다. 또한, 공간적 합으로 색상을 표시하는 경우에는 R 화소, G 화소 및 B 화소가 행 방향 또는 열 방향으로 번갈아 가면서 배열될 수 있으며, 또는 세 화소가 삼각형의 세 꼭지점에 해당하는 위치에 배열될 수도 있다.
- [0022] 스캔 드라이버(200)는 유기발광패널(100)의 스캔 라인(S1-Sn)에 연결되어 게이트 온 전압과 게이트 오프 전압의 조합으로 이루어진 스캔 신호를 스캔 라인(S1-Sn)에 인가한다. 이때, 스캔 드라이버(200)는 다수의 스캔 라인(S1-Sn)에 각각 인가되는 다수의 선택 신호가 차례로 게이트 온 전압을 가지도록 스캔 신호를 인가할 수 있다. 그리고 스캔 신호가 게이트 온 전압을 가지는 경우에, 해당 스캔 라인에 연결되는 스위칭 트랜지스터가 턴-온된다.
- [0023] 상기 스캔 드라이버(200)는 쉬프트 레지스터 역할을 하는 다수의 스테이지들을 포함한다. 각 스테이지는 다수의 클럭라인 중 3개의 클럭라인으로부터 2수평주기 이상 위상 지연된 클럭신호를 입력받아 해당 스캔 라인에 2수평주기 이상의 펄스 폭을 갖는 스캔 신호를 출력한다. 인접하는 스캔 신호들은 서로 1수평주기 이상 오버랩될 수 있다. 다수의 클럭라인은 1수평주기 만큼씩 위상 지연된 클럭신호를 순차적으로 공급한다.
- [0024] 데이터 드라이버(300)는 유기발광패널(100)의 데이터 라인(D1-Dm)에 연결되어 계조를 나타내는 데이터 신호를 데이터 라인(D1-Dm)에 인가한다. 이러한 데이터 드라이버(300)는 타이밍 컨트롤러(400)로부터 입력되는 계조를 가지는 입력 영상 데이터(Data)를 전압 또는 전류 형태의 데이터 신호로 변환한다.
- [0025] 타이밍 컨트롤러(400)는 외부의 그래픽 제어기(도시하지 않음)로부터 입력 영상 데이터(Data) 및 이의 표시를 제어하는 입력 제어 신호를 제공받는다. 입력 제어 신호에는 예를 들어 수평 동기 신호(Hsync), 수직 동기 신호(Vsync) 및 메인 클럭(MCLK)이 있다. 타이밍 컨트롤러(400)는 입력 영상 데이터(Data)를 데이터 드라이버(300)로 전달하고, 스캔 제어 신호(CONT1) 및 데이터 제어 신호(CONT2)를 생성하여 각각 스캔 드라이버(200) 및 데이터 드라이버(300)로 전달한다. 스캔 제어 신호(CONT1)는 스캔 시작을 지시하는 스캔 시작 신호(SSP)와 다수의 클럭 신호(SCLK)를 포함하며, 데이터 제어 신호(CONT2)는 한 행의 화소(110)에 대한 입력 영상 데이터의 전달을 지시하는 수평 동기 시작 신호(STH)와 클럭 신호를 포함한다.
- [0026] 한편, 타이밍 컨트롤러(400)는 한 행에 해당하는 입력 영상 데이터를 데이터 드라이버(300)로 전달하는 경우에, 입력 영상 데이터(Data)를 세 개의 채널을 통해서 색상 별로 전달할 수도 있으며, 입력 영상 데이터(Data)를 하나의 채널을 통하여 차례로 전달할 수도 있다.

- [0027] 도 2는 본 발명의 일 실시예에 따른 스캔 드라이버의 개략적인 블록도이다. 도 3은 도 2의 스캔 드라이버의 동작을 나타내는 타이밍도이다.
- [0028] 도 2 및 도 3을 참조하면, 본 발명의 스캔 드라이버는 스캔 시작 신호(SSP) 라인과 6상 클럭라인(SCLK1 내지 SCLK6) 중 3개의 클럭라인에 각각 접속된 n개의 스테이지(ST1 내지 STn)를 포함한다. 6상 클럭라인(SCLK1 내지 SCLK6)의 클럭 신호(SCLK1 내지 SCLK6)는 1수평주기(1H) 만큼씩 위상 지연된 형태로 공급되고, 스캔 시작 신호(SSP)와 클럭 신호(SCLK1 내지 SCLK6)는 모두 2수평주기(2H) 동안 인가되어 2H의 펄스 폭을 갖는다. 도 2 및 도 3에서는 편의상 제1 내지 제4스테이지(ST1 내지 ST4)와 이들의 타이밍도만을 도시하였다.
- [0029] 각 스테이지의 출력단(OUT)으로 출력되는 스캔 신호들(S1 내지 Sn)은 해당 스캔 라인(Scan[1] 내지 Scan[n])으로 공급되고, 동시에 후단 스테이지의 시작 신호로서 후단 스테이지의 입력단(IN)에 공급된다. 각 스테이지의 입력단(IN)은 제1스테이지(ST1)에서는 스캔 시작 신호(SSP)가 입력되고, 제2 내지 제n스테이지들(ST2 내지 STn)에는 전단 스테이지의 출력신호, 즉 스캔 신호(S1 내지 Sn-1)가 입력된다.
- [0030] 제1스테이지(ST1)는 제1클럭단자(c1k1)가 제1클럭라인(SCLK1)에 전기적으로 연결되고, 제2클럭단자(c1k2)가 제3클럭라인(SCLK3)에 전기적으로 연결되고, 제3클럭단자(c1k3)가 제5클럭라인(SCLK5)에 전기적으로 연결된다. 그리고 입력단(IN)으로 초기 스캔 시작 신호(SSP)를 입력받아 출력단(OUT)의 제1스캔라인(Scan[1])으로 2H의 펄스 폭을 갖는 제1스캔 신호(S1)를 출력한다.
- [0031] 제2스테이지(ST2)는 제1클럭단자(c1k1)가 제2클럭라인(SCLK2)에 전기적으로 연결되고, 제2클럭단자(c1k2)가 제4클럭라인(SCLK4)에 전기적으로 연결되고, 제3클럭단자(c1k3)가 제6클럭라인(SCLK6)에 전기적으로 연결된다. 그리고 입력단(IN)으로 제1스캔 신호(S1)를 입력받아 출력단(OUT)의 제2스캔라인(Scan[2])으로 2H의 펄스 폭을 갖는 제2스캔 신호(S2)를 출력한다.
- [0032] 제3스테이지(ST3)는 제1클럭단자(c1k1)가 제3클럭라인(SCLK3)에 전기적으로 연결되고, 제2클럭단자(c1k2)가 제5클럭라인(SCLK5)에 전기적으로 연결되고, 제3클럭단자(c1k3)가 제1클럭라인(SCLK1)에 전기적으로 연결된다. 그리고 입력단(IN)이 제2스캔 신호(S2)를 입력받아 출력단(OUT)의 제3스캔라인(Scan[3])으로 2H의 펄스 폭을 갖는 제3스캔 신호(S3)를 출력한다.
- [0033] 유사하게, 제4스테이지(ST4) 내지 제n스테이지(STn)는 제1 내지 제6 클럭라인(SCLK1 내지 SCLK6)의 클럭 신호(SCLK1 내지 SCLK6) 중 2H 만큼씩 위상 지연된 3개의 클럭 신호를 이용하여, 입력단(IN)으로 인가되는 전단 스캔 신호(S3 내지 Sn-1)를 입력받아 출력단(OUT)의 스캔라인(Scan[3] 내지 Scan[n])으로 2H의 펄스 폭을 갖는 스캔 신호(S3 내지 Sn)를 출력한다.
- [0034] 본 발명의 스캔 드라이버는 제1 내지 제6 클럭 신호(SCLK1 내지 SCLK6)가 사용되므로 6개의 스테이지마다 클럭 신호가 반복된다.
- [0035] 스캔라인(Scan[1] 내지 Scan[n])으로 공급되는 스캔 신호들은 스캔 펄스 듀레이션 타임인 스캔 타임(scan time)이 2H이고, 인접하는 스테이지들로부터 출력되는 스캔 신호들은 1H 만큼 오버랩된다. 제1구간(t2) 내지 제3구간(t3)에서의 스캔 신호 생성 과정은 이후 상세히 설명하겠다.
- [0036] 도 4는 도 2에 도시된 스캔 드라이버에서 임의의 스테이지(Si)에 대한 구체적인 회로도이다. 이하에서는 제1스테이지(S1)를 중심으로 설명하며, 구성 및 동작은 나머지 스테이지에 동일하게 적용할 수 있다.
- [0037] 도 4를 참조하면, 제1스테이지(S1)는 제1스위칭소자(T1), 제2스위칭소자(T2), 제3스위칭소자(T3), 제4스위칭소자(T4), 제5스위칭소자(T5), 제6스위칭소자(T6), 제1용량성소자(C1), 및 제2용량성소자(C2)를 포함한다. 제1전원전압(SVDD)은 외부 제1전원으로부터 공급되는 하이레벨 신호이고, 제2전원전압(SVSS)은 외부 제2전원으로부터 공급되는 로우레벨 신호이다.
- [0038] 제6스위칭소자(T6)는 게이트 전극이 입력단자(IN)에 전기적으로 연결되고, 제1전극(드레인 전극 또는 소스 전극)이 제1전원에 전기적으로 연결되고, 제2전극(소스 전극 또는 드레인 전극)이 제2노드(QB)에 전기적으로 연결된다. 제6스위칭소자(T6)는 게이트 전극에 로우레벨 신호가 인가되면 턴 온되어 제2노드(QB)를 제1전원전압(SVDD)으로 충전한다.
- [0039] 제5스위칭소자(T5)는 제1전극이 입력단자(IN)에 전기적으로 연결되고, 제2전극이 제1노드(Q)에 전기적으로 연결되고, 게이트 전극이 제2클럭단자(c1k2)에 전기적으로 연결된다. 제5스위칭소자(T5)는 게이트 전극에 로우레벨 신호가 인가되면 턴 온되어 제1노드(Q)에 입력단자(IN)의 전압을 공급한다.

- [0040] 제4스위칭소자(T4)는 제1전극이 제2노드(QB)에 전기적으로 연결되고, 제2전극이 제2전원에 전기적으로 연결되고, 게이트 전극이 제1클럭단자(c1k1)에 전기적으로 연결된다. 제4스위칭소자(T4)는 게이트 전극에 로우레벨 신호가 인가되면 턴 온되어 제2노드(QB)를 제2전원전압(SVSS)으로 충전한다.
- [0041] 제3스위칭소자(T3)는 제1전극이 제1전원에 전기적으로 연결되고, 제2전극이 제1노드(Q)에 전기적으로 연결되고, 게이트 전극이 제2노드(QB)에 전기적으로 연결된다. 제3스위칭소자(T3)는 게이트 전극에 로우레벨 신호가 인가되면 턴 온되어 제1노드(Q)를 제1전원전압(SVDD)으로 충전한다.
- [0042] 제2스위칭소자(T2)는 게이트 전극이 제1노드(Q)와 전기적으로 연결되고, 제1전극이 출력단자(OUT)에 전기적으로 연결되고, 제2전극이 제3클럭단자(c1k3)에 전기적으로 연결된다. 제2스위칭소자(T2)는 게이트 전극에 로우레벨 신호가 인가되면 턴 온되어 제3클럭단자(c1k3)로부터 입력되는 클럭신호의 전압을 출력단자(OUT)로 공급한다.
- [0043] 제1스위칭소자(T1)는 게이트 전극이 제2노드(QB)에 전기적으로 연결되고, 제1전극이 제1전원에 전기적으로 연결되고, 제2전극이 출력단자(OUT)에 전기적으로 연결된다. 제1스위칭소자(T1)는 게이트 전극에 로우레벨 신호가 인가되면 턴 온되어 제1전원전압(SVDD)을 출력단자(OUT)로 공급한다.
- [0044] 제1용량성소자(C1)는 제1전극이 제1노드(Q)에 전기적으로 연결되고 제2전극이 출력단자(OUT)에 전기적으로 연결된다. 제1용량성소자(C1)는 제1노드(Q)와 출력단자(OUT)가 접속된 노드, 즉 제1스위칭소자(T1)의 제2전극과 제2스위칭소자(T2)의 제1전극이 전기적으로 연결된 노드 간의 전압 차가 저장된다.
- [0045] 제2용량성소자(C2)는 제1전극이 제1전원에 전기적으로 연결되고 제2전극이 제2노드(QB)에 전기적으로 연결되어, 양 전극 간의 전압 차가 저장된다.
- [0046] 제1노드(Q)에는 제5스위칭소자(T5)의 제2전극, 제3스위칭소자(T3)의 제2전극, 제2스위칭소자(T2)의 게이트 전극이 접속된다. 제2노드(QB)에는 제6스위칭소자(T6)의 제2전극, 제4스위칭소자(T4)의 제1전극, 제3스위칭소자(T3)의 게이트 전극, 제1스위칭소자(T1)의 게이트 전극이 접속된다.
- [0047] 본 발명의 일 실시예에서 스위칭소자들(T1 내지 T6)은 모두 PMOS 트랜지스터로 구현되는 예를 설명하였으나, NMOS 트랜지스터로 구현하고 신호를 반전시킴으로써 본 발명의 구동 방법을 적용할 수 있음은 물론이다.
- [0048] 도 5는 도 4의 임의의 스테이지(STi)의 동작을 나타내는 타이밍도이다.
- [0049] 도 4 및 도 5를 참조하면, 입력단자(IN)로 입력되는 시작 신호, 제1 내지 제3클럭단자(c1k1 내지 c1k3)의 클럭 신호, 및 출력단자(OUT)에서 출력되는 스캔 신호는 2H의 펄스 폭을 가진다. 제1 내지 제3 클럭단자(c1k1 내지 c1k3)로 입력되는 클럭신호는 2H 만큼 위상 지연되어 입력된다. 스캔 신호는 시작 신호로부터 2H 만큼 쉬프트되어 출력된다.
- [0050] 제1구간(t1)에서는 전단 스테이지의 스캔 신호 또는 최초 시작 신호(SSP)가 입력단자(IN)를 통해 제6스위칭소자(T6)의 게이트 전극으로 인가되고, 동시에 제5스위칭소자(T5)의 제1전극으로 인가된다. 또한, 제2클럭단자(c1k2)를 통해 로우레벨의 클럭신호가 제5스위칭소자(T5)에 인가된다. 이때, 제1 및 제3클럭단자(c1k1, c1k3)에는 하이레벨의 클럭신호가 각각 인가된다.
- [0051] 이 경우, 로우레벨의 시작신호(SSP)에 의해 제6스위칭소자(T6)가 턴-온되어 제2노드(QB)가 하이레벨의 제1전원전압(SVDD)으로 충전된다. 그리고 제2클럭단자(c1k2)에 인가되는 로우레벨의 클럭신호에 의해 제5스위칭소자(T5)가 턴-온되고 제1노드(Q)가 로우레벨의 제2전원전압(SVSS)과 문턱전압($|V_{th}|$)의 합($SVSS+|V_{th}|$)으로 선충전(pre-charge)되고, 제2스위칭소자(T2)가 턴-온된다.
- [0052] 상기 제2노드(QB)가 하이레벨의 제1전원전압(SVDD)으로 충전됨에 따라, 제1스위칭소자(T1) 및 제3스위칭소자(T3)가 턴-오프된다.
- [0053] 따라서, 제2스위칭소자(T2)의 제2전극으로 제3클럭단자(c1k3)를 통해 하이레벨의 클럭신호가 인가되어 제2스위칭소자(T2)의 제1전극과 연결된 출력 단자(OUT)에 하이레벨의 스캔 신호가 출력된다.
- [0054] 즉, 상기 제1구간(t1)에서 스캔 라인을 통해 출력되는 스캔 신호는 하이레벨을 갖는다. 또한 상기 제1노드(Q) 및 출력단자(OUT) 사이에 접속된 제1용량성소자(C1)는 상기 제1구간(t1) 동안 제1노드(Q) 및 출력단자(OUT) 사이의 전위차에 의해 전압이 충전된다.
- [0055] 제2구간(t2)에서는 전단 스테이지의 스캔 신호 또는 최초 시작 신호(SSP)와 제2클럭단자(c1k2)의 클럭신호가 하이레벨로 반전되고, 제3클럭단자(c1k3)의 클럭신호가 로우레벨로 반전된다. 제1클럭단자(c1k1)의 클럭신호는 하

이레벨을 유지한다.

- [0056] 이 경우, 하이레벨의 시작 신호(SSP)와 제1 및 제2클럭단자(c1k1, c1k2)의 클럭신호에 의해 제2스위칭소자(T2)를 제외한 다른 스위칭소자는 모두 턴-오프된다.
- [0057] 상기 제2스위칭소자(T2)를 통해 출력단자(OUT) 노드의 전압이 제2전원전압(SVSS)을 향해 떨어지기 시작하고, 상기 제1용량성소자(C1)에 의해 충전된 전압이 방전됨에 따라 부트스트래핑(bootstrapping) 현상이 발생하여 제1노드(Q)의 전압이 제2전원전압(SVSS)보다 훨씬 낮은 전압으로 떨어짐으로써 제2스위칭소자(T2)를 완전히 턴-온시킨다.
- [0058] 따라서, 제2스위칭소자(T2)의 제2전극으로 제3클럭단자(c1k3)를 통해 로우레벨의 클럭신호가 인가되고, 제2스위칭소자(T2)의 제1전극과 연결된 출력 단자(OUT)에 로우레벨의 스캔 신호가 출력된다.
- [0059] 즉, 상기 제2구간(t2)에서 스캔 라인을 통해 출력되는 신호는 로우레벨을 갖는다.
- [0060] 제3구간(t3)에서는 제3클럭단자(c1k3)의 클럭신호가 하이레벨로 반전되고, 제1클럭단자(c1k1)의 클럭신호가 로우레벨로 반전되고, 시작 신호(SSP)와 제2클럭단자(c1k2)의 클럭신호는 하이레벨을 유지한다.
- [0061] 이 경우, 제1클럭단자(c1k1)의 로우레벨의 클럭신호에 의해 제4스위칭소자(T4)가 턴-온되어 제2노드(QB)가 로우레벨의 제2전원전압(SVSS)으로 충전된다. 상기 제2노드(QB)가 로우레벨의 제2전원전압(SVSS)으로 충전됨에 따라, 제1스위칭소자(T1)와 제3스위칭소자(T3)가 턴-온된다. 따라서, 제1스위칭소자(T1)의 제1전극으로 입력되는 하이레벨의 제1전원전압(SVDD)이 제1스위칭소자(T1)의 제2전극과 연결된 출력단자(OUT)에 하이레벨의 스캔 신호로서 출력된다. 이때, 제3스위칭소자(T3)가 턴-온됨에 따라 제1노드(Q)는 하이레벨의 제1전원전압(SVDD)으로 충전되고, 이에 따라, 제2스위칭소자(T2)가 턴-오프된다.
- [0062] 즉, 상기 제3구간(t3)에서 스캔 라인을 통해 출력되는 스캔 신호는 하이레벨을 갖는다.
- [0063] 여기서, 제2용량성소자(C2)는 제1전원전압(SVDD)과 제2노드(QB) 사이에 접속되어, 제1전원전압(SVDD)과 제2노드(QB)에 걸리는 전압의 변동을 줄이는 역할을 수행한다.
- [0064] 이하, 도 3 내지 도 5를 함께 참조하여, 제2구간(t2)에서, 인접하는 스테이지들 간의 쉬프트 레지스터 동작을, 제1스테이지(ST1)와 제2스테이지(ST2)로부터 제1스캔라인(Scan[1])과 제2스캔라인(Scan[2])에 각각 출력되는 스캔 신호(S1, S2)를 예를 들어 설명하겠다.
- [0065] 제1스테이지(ST1)에는 제1클럭단자(c1k1)에 제1클럭신호(SCLK1), 제2클럭단자(c1k2)에 제3클럭신호(SCLK3), 제3클럭단자(c1k3)에 제5클럭신호(SCLK5)가 각각 입력된다. 그리고, 제2스테이지(ST2)에는 제1클럭단자(c1k1)에 제2클럭신호(SCLK2), 제2클럭단자(c1k2)에 제4클럭신호(SCLK4), 제3클럭단자(c1k3)에 제6클럭신호(SCLK6)가 각각 입력된다.
- [0066] 제2구간(t2)에서, 제1스테이지(ST1)에서는 최초 시작 신호(SSP)와 제3클럭신호(SCLK3)가 하이레벨로 반전되고, 제5클럭신호(SCLK5)가 로우레벨로 반전된다. 제1클럭신호(SCLK1)는 하이레벨을 유지한다. 이 경우, 하이레벨의 시작 신호(SSP)와 제1 및 제3클럭신호(SCLK1, SCLK3)에 의해 제2스위칭소자(T2)를 제외한 다른 스위칭소자는 모두 턴-오프된다. 상기 제2스위칭소자(T2)의 경우, 상기 제1용량성소자(C1)에 의한 부트스트래핑(bootstrapping) 현상으로 제1노드(Q)의 전압이 제2전원전압보다 훨씬 낮은 전압으로 떨어짐으로써 제2스위칭소자(T2)를 완전히 턴-온시킨다. 따라서, 제2스위칭소자(T2)의 제2전극으로 제3클럭단자(c1k3)를 통해 로우레벨의 제5클럭신호(SCLK5)가 인가되고, 제2스위칭소자(T2)의 제1전극과 연결된 출력 단자(OUT)에 로우레벨의 스캔 신호가 출력된다.
- [0067] 제2구간(t2)의 전반 1H 동안, 제2스테이지(ST2)에는 로우레벨의 제4클럭신호(SCLK4)가 인가되어 제5스위칭소자(T5)가 턴-온되어 제1노드(Q)가 로우레벨의 제2전원전압으로 선충전(pre-charge)된다. 이에 따라, 제2스위칭소자(T2)가 턴-온되고, 제2스위칭소자(T2)를 통해 하이레벨의 제6클럭신호(SCLK6)가 인가되어 출력단자(OUT)에 하이레벨의 스캔 신호가 출력된다. 다음으로, 제2구간(t2)의 후반 1H 동안, 상기 제2스테이지(ST2)에는 제1용량성소자(C1)에 의한 부트스트래핑(bootstrapping) 현상으로 제1노드(Q)의 전압이 제2전원전압보다 훨씬 낮은 전압으로 떨어짐으로써 제2스위칭소자(T2)를 턴-온시킨다. 이에 따라, 제2스위칭소자(T2)를 통해 로우레벨의 제6클럭신호(SCLK6)가 인가되어 출력 단자(OUT)에 로우레벨의 스캔 신호가 출력된다.
- [0068] 따라서 제1스테이지(ST1)와 제2스테이지(ST2) 간에 연속적인 쉬프트 레지스터(shift register) 동작이 이루어지며, 이는 타 스테이지들 간에도 동일하게 적용될 수 있다.

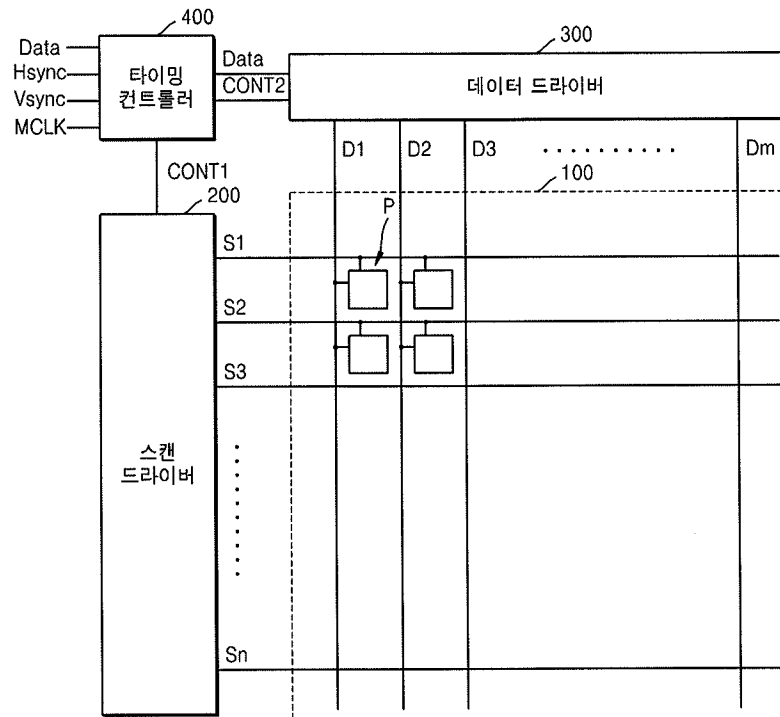
- [0069] 도 6은 본 발명의 다른 실시예에 따른 스캔 드라이버의 개략적인 블록도이다. 도 7은 도 6의 스캔 드라이버의 동작을 나타내는 타이밍도이다.
- [0070] 도 6 및 도 7을 참조하면, 본 발명의 스캔 드라이버는 스캔 시작 신호(SSP) 라인과 9상 클럭라인(SCLK1 내지 SCLK9) 중 3개의 클럭라인에 각각 접속된 n개의 스테이지(ST1 내지 STn)를 포함한다. 9상 클럭라인(SCLK1 내지 SCLK9)의 클럭 신호(SCLK1 내지 SCLK9)는 1수평주기(1H) 만큼씩 위상 지연된 형태로 공급되고, 스캔 시작 신호(SSP)와 클럭 신호(SCLK1 내지 SCLK9)는 모두 3수평주기(3H) 동안 인가되어 3H의 펄스 폭을 갖는다. 도 6 및 도 7에서는 편의상 제1 내지 제4스테이지(ST1 내지 ST4)와 이들의 타이밍도만을 도시하였다.
- [0071] 각 스테이지의 출력단(OUT)으로 출력되는 스캔 신호들(S1 내지 Sn)은 각각 해당 스캔 라인(Scan[1] 내지 Scan[n])으로 공급되고, 동시에 후단 스테이지의 시작 신호로서 후단 스테이지의 입력단(IN)에 공급된다. 각 스테이지의 입력단(IN)은 제1스테이지(ST1)에서는 스캔 시작 신호(SSP)가 입력되고, 제2 내지 제n스테이지들(ST2 내지 STn)에는 전단 스테이지의 출력신호, 즉 스캔 신호(S1 내지 Sn-1)가 입력된다.
- [0072] 제1스테이지(ST1)는 제1클럭단자(c1k1)가 제1클럭라인(SCLK1)에 전기적으로 연결되고, 제2클럭단자(c1k2)가 제4클럭라인(SCLK4)에 전기적으로 연결되고, 제3클럭단자(c1k3)가 제7클럭라인(SCLK7)에 전기적으로 연결된다. 그리고 입력단(IN)으로 초기 스캔 시작 신호(SSP)를 입력받아 출력단(OUT)의 제1스캔라인(Scan[1])으로 3H의 펄스 폭을 갖는 제1스캔 신호(S1)를 출력한다.
- [0073] 제2스테이지(ST2)는 제1클럭단자(c1k1)가 제2클럭라인(SCLK2)에 전기적으로 연결되고, 제2클럭단자(c1k2)가 제5클럭라인(SCLK5)에 전기적으로 연결되고, 제3클럭단자(c1k3)가 제8클럭라인(SCLK8)에 전기적으로 연결된다. 그리고 입력단(IN)으로 제1스캔 신호(S1)를 입력받아 출력단(OUT)의 제2스캔라인(Scan[2])으로 3H의 펄스 폭을 갖는 제2스캔 신호(S2)를 출력한다.
- [0074] 제3스테이지(ST3)는 제1클럭단자(c1k1)가 제3클럭라인(SCLK3)에 전기적으로 연결되고, 제2클럭단자(c1k2)가 제6클럭라인(SCLK6)에 전기적으로 연결되고, 제3클럭단자(c1k3)가 제9클럭라인(SCLK9)에 전기적으로 연결된다. 그리고 입력단(IN)이 제2스캔 신호(S2)를 입력받아 출력단(OUT)의 제3스캔라인(Scan[3])으로 3H의 펄스 폭을 갖는 제3스캔 신호(S3)를 출력한다.
- [0075] 유사하게 제4스테이지(ST4) 내지 제n스테이지(STn)는 제1 내지 제9클럭라인(SCLK1 내지 SCLK9)의 클럭 신호(SCLK1 내지 SCLK9) 중 3H 만큼씩 위상 지연된 3개의 클럭 신호를 이용하여, 입력단(IN)으로 인가되는 전단 스캔 신호(S3 내지 Sn-1)를 입력받아 출력단(OUT)의 스캔라인(Scan[3] 내지 Scan[n])으로 3H의 펄스 폭을 갖는 스캔 신호(S3 내지 Sn)를 출력한다.
- [0076] 본 발명의 스캔 드라이버는 제1 내지 제9 클럭 신호(SCLK1 내지 SCLK9)가 사용되므로 9개의 스테이지마다 클럭 신호가 반복된다.
- [0077] 스캔라인(Scan[1] 내지 Scan[n])으로 공급되는 스캔 신호들은 스캔 펄스 듀레이션 타임인 스캔 타임(scan time)이 3H이고, 인접하는 스테이지들로부터 출력되는 스캔 신호들은 2H 만큼 오버랩된다.
- [0078] 상기 제2 실시예에서 각 스테이지의 구동 회로는 제1 실시예의 도 4의 구동 회로를 동일하게 적용할 수 있으며, 그에 따라 각 스테이지의 동작 타이밍도가 각 신호의 펄스 폭이 3H인 것을 제외하고 도 5와 동일하고, 구동 방법 또한 동일하므로 상세한 설명은 생략하겠다.
- [0079] 본 발명은 각 스테이지로 인가되는 클럭 신호의 펄스 폭과 위상 지연 시간을 조절하여 스캔 신호의 펄스 폭을 2H 이상이 되도록 하고 인접하는 스테이지의 스캔 신호 간에는 1H, 2H의 오버랩 구간을 가지도록 한다. 따라서 FHD 120Hz 이상의 유기발광패널 구동시 짧은 스캔 타임에 의한 비정상 스캔 신호 발생을 방지하고 균일한 화면을 제공할 수 있다.
- [0080] 본 발명은 도면에 도시된 실시예를 참고로 설명되었으나 이는 예시적인 것에 불과하며, 당해 기술 분야에서 통상의 지식을 가진 자라면 이로부터 다양한 변형 및 균등한 다른 실시예가 가능하다는 점을 이해할 것이다. 따라서, 본 발명의 진정한 기술적 보호 범위는 첨부된 특허청구범위의 기술적 사상에 의하여 정해져야 할 것이다.

부호의 설명

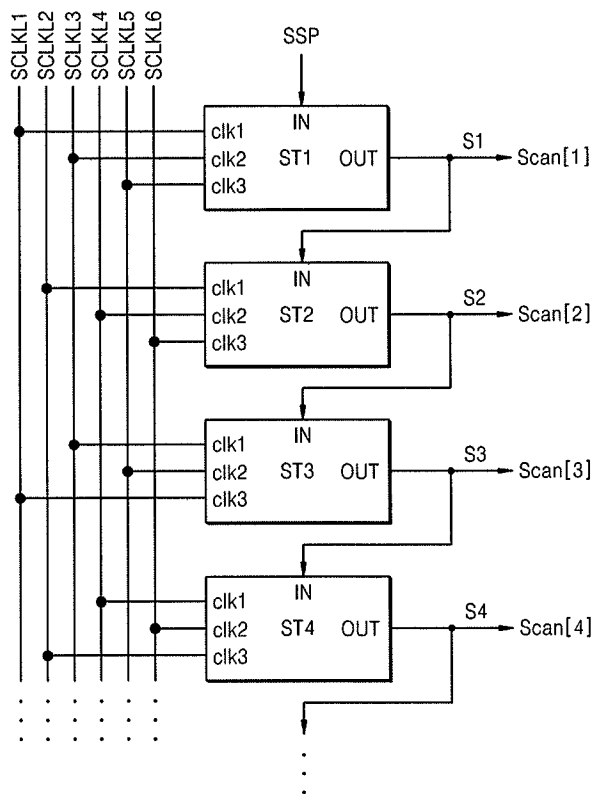
- [0081] 100: 패널, 200: 스캔 드라이버
300: 데이터 드라이버, 400: 타이밍 컨트롤러

도면

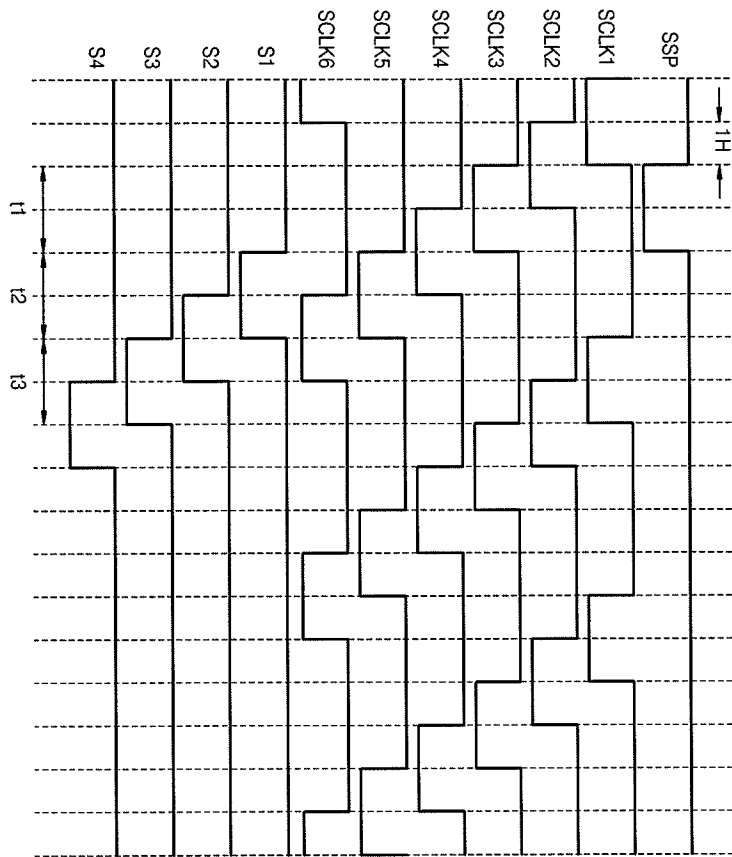
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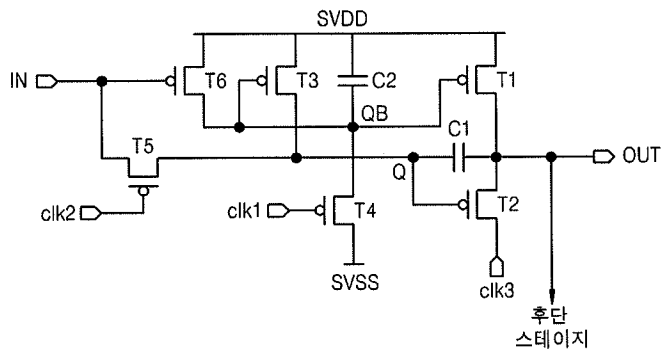
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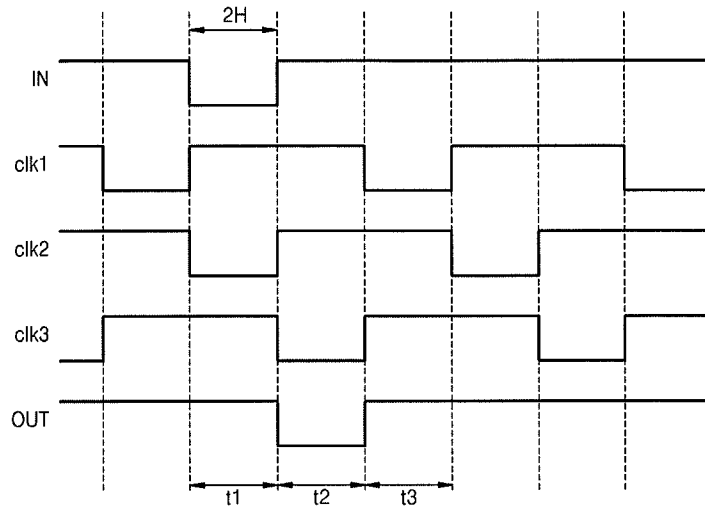
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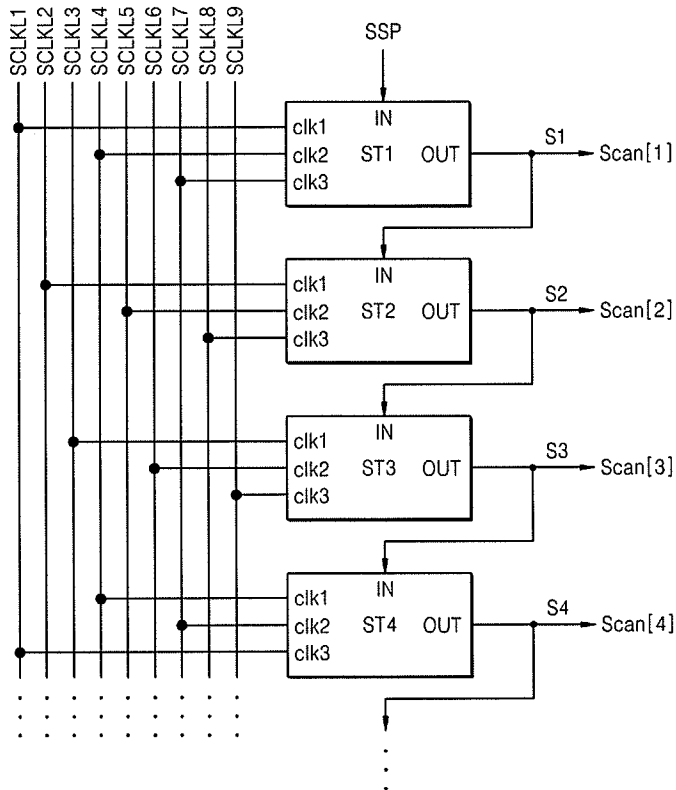
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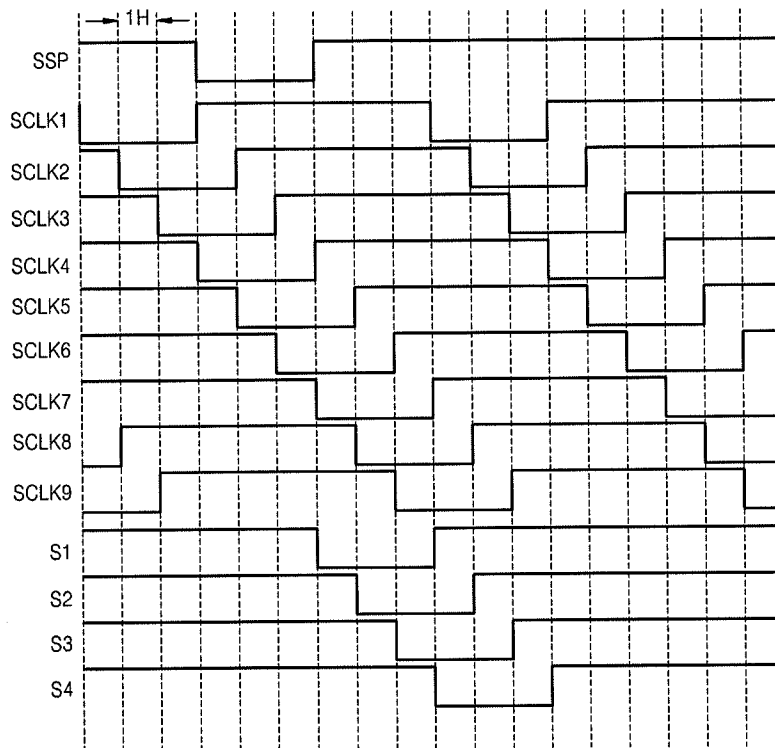
도면5



도면6



도면7



Electronic Patent Application Fee Transmittal

Application Number:				
Filing Date:				
Title of Invention:	STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME			
First Named Inventor/Applicant Name:	Hwan-Soo JANG			
Filer:	Susan S. Morse/Sharon Bender			
Attorney Docket Number:	304/1043			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	390	390
Utility Search Fee	1111	1	620	620
Utility Examination Fee	1311	1	250	250
Pages:				
Claims:				
Claims in excess of 20	1202	7	62	434
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1694

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EFS ID:	15000716
Application Number:	13771385
International Application Number:	
Confirmation Number:	3091
Title of Invention:	STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME
First Named Inventor/Applicant Name:	Hwan-Soo JANG
Customer Number:	27849
Filer:	Susan S. Morse/Sharon Bender
Filer Authorized By:	Susan S. Morse
Attorney Docket Number:	304/1043
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Authorized User	MORSE, SUSAN S.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Mianyang BOE Ex. 1002

Case No. IPR2023-01221

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File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	ADS_SDC_updated_2012_10_11.pdf	997725	no	6
			3534905451e65f36d7dd9c1041cce5bdc1c51038		
Warnings:					
Information:					
2		App_As_Filed_2013_02_20.pdf	2278654	yes	62
			74c48ee19fc713c11a368b1c7ff7351503025daf		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal of New Application		1	3	
	Specification		4	23	
	Claims		24	32	
	Abstract		33	33	
	Drawings-only black and white line drawings		34	40	
	Oath or Declaration filed		41	41	
	Request for USPTO to retrieve priority docs		42	42	
	Transmittal Letter		43	45	
	Information Disclosure Statement (IDS) Form (SB08)		46	46	
	Foreign Reference		47	62	
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	36819	no	2
			ae5c4b5022c6c860625c6796c47c335d17233e52		
Warnings:					
Information:					
Total Files Size (in bytes):			3313198		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	304/1043
		Application Number	
Title of Invention	STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--

Inventor Information:

Inventor 1 Remove				
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Hwan-Soo		JANG	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Yongin-City, Gyeonggi-Do	Country of Residence	KR	
Mailing Address of Inventor:				
Address 1		c/o Samsung Display Co., Ltd.		
Address 2		95, Samsung 2 Ro, Giheung-Gu		
City	Yongin-City, Gyeonggi-Do	State/Province		
Postal Code		Country	KR	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add				

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence information of this application.			
Customer Number	27849		
Email Address	eoal@lee-iplaw.com	Add Email	Remove Email

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	304/1043
		Application Number	
Title of Invention	STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME		

Application Information:

Title of the Invention	STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME		
Attorney Docket Number	304/1043	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)		Suggested Figure for Publication (if any)	

Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐	Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	27849		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.			
Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

Mianyang BOE Ex. 1002

Case No. IPR2023-01221

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	304/1043
		Application Number	
Title of Invention	STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME		
This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).			
			Remove
Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Priority Claimed
10-2012-0104512	KR	2012-09-20	☒ Yes ☐ No
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Authorization to Permit Access:

☐	Authorization to Permit Access to the Instant Application by the Participating Offices
If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application. In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application. In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	304/1043
	Application Number	
Title of Invention	STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME	

Applicant 1	
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.	
Remove	
☐ Assignee	☐ Legal Representative under 35 U.S.C. 117
☐ Person to whom the inventor is obligated to assign.	☐ Person who shows sufficient proprietary interest
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:	
Name of the Deceased or Legally Incapacitated Inventor :	
If the Assignee is an Organization check here. ☐	

Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information:				
Address 1				
Address 2				
City		State/Province		
Country i		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Applicant Data may be generated within this form by selecting the Add button. Add				

Signature:					Remove
NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications					
Signature	/Susan S. Morse/			Date (YYYY-MM-DD)	2013-02-20
First Name	Susan S.	Last Name	Morse	Registration Number	35292
Additional Signature may be generated within this form by selecting the Add button. Add					

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	304/1043
		Application Number	
Title of Invention	STAGE CIRCUIT AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.