IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MIANYANG BOE OPTOELECTRONICS TECHNOLOGY CO., LTD.; WUHAN CHINA STAR OPTOELECTRONICS SEMICONDUCTOR DISPLAY TECHNOLOGY CO., LTD.; TIANMA MICROELECTRONICS CO. LTD.; AND VISIONOX TECHNOLOGY, INC.
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

U.S. Patent No. 9,330,593

Inter Partes Review No. IPR2023-01221

DECLARATION OF DR. DANIEL FOTY

TABLE OF CONTENTS

I. INTRODUCTION 6
II. QUALIFICATIONS 7
III. COMPENSATION 7
IV. MATERIALS CONSIDERED 7
V. UNDERSTANDING OF THE LAW 9
A. Legal Standards 9
1. Claim Construction 9
2. Burden of Proof 10
3. Anticipation 10
4. Obviousness 11
B. Priority Date 14
C. Level of Skill in the Art 14
VI. SUMMARY OF OPINIONS 16
VII. TECHNOLOGY BACKGROUND 16
A. Fundamental Concepts of Transistor-Based Circuit Design 16
1. Field-Effect Transistors (FETs) 17
2. nMOS/pMOS Interchangeability 29
3. The Diode-Connected Configuration of a Field-Effect Transistor 34
4. The Transistor Threshold Voltage 35
B. Pixel-Based Displays 38
1. Pixel Technologies 39
2. Pixels and Pixel Arrays 40
3. Scan Lines and Control Signals in a Display 41
VIII. THE CHALLENGED PATENT 43
A. General Overview 43

B. File History 44

C. Claim Construction 46

IX. OVERVIEW OF THE PRIOR ART REFERENCES 47

A. Chung 47

B. Kim 48

C. Tobita 49

D. Jeong 50

X. MOTIVATION TO COMBINE CERTAIN PRIOR ART REFERENCES 51

XI. CLAIM TERMS 51

XII. UNPATENTABILITY ANALYSIS ..... 52~~51~~

A. Ground 1: Chung Anticipates Claims 1-7, 9, 14-21, 23, and 25 52

1. Independent Claim 1 52
2. Dependent Claim 2 71
3. Dependent Claim 3 73
4. Dependent Claim 4 75
5. Dependent Claim 5 79
6. Dependent Claim 6 80
7. Dependent Claim 7 81
8. Dependent Claim 9 83
9. Dependent Claim 14 84
10. Independent Claim 15 87
11. Dependent Claim 16 100
12. Dependent Claim 17 103
13. Dependent Claim 18 103
14. Dependent Claim 19 105
15. Dependent Claim 20 106

16. Dependent Claim 21 107
17. Dependent Claim 23 107
18. Dependent Claim 25 108

B. Ground 2: Kim Anticipates Claims 1-5, 7-8, 14-19, 21-22, and 25 115

1. Independent Claim 1 116
2. Dependent Claim 2 135
3. Dependent Claim 3 137
4. Dependent Claim 4 139
5. Dependent Claim 5 143
6. Dependent Claim 7 144
7. Dependent Claim 8 145
8. Dependent Claim 14 147
9. Independent Claim 15 149
10. Dependent Claim 16 160
11. Dependent Claim 17 163
12. Dependent Claim 18 164
13. Dependent Claim 19 166
14. Dependent Claim 21 167
15. Dependent Claim 22 167
16. Dependent Claim 25 168

C. Ground 3: Tobita Renders Obvious Claims 1-5, 14-19, and 25 175

1. Independent Claim 1 176
2. Dependent Claim 2 191
3. Dependent Claim 3 194
4. Dependent Claim 4 196
5. Dependent Claim 5 199
6. Dependent Claim 14 202

7. Independent Claim 15 205
8. Dependent Claim 16 215
9. Dependent Claim 17 219
10. Dependent Claim 18 219
11. Dependent Claim 19 222
12. Dependent Claim 25 223

D. Ground 4: Tobita in View of Jeong and the Knowledge of a POSITA Renders Claims 7 and 21 Obvious 227
1. Generalized Motivation to Combine 227
2. Dependent Claim 7 229
3. Dependent Claim 21 235

XIII. SECONDARY CONSIDERATIONS 235
XIV. CONCLUSION 235

I. INTRODUCTION

1. I have been retained by counsel for Mianyang BOE Optoelectronics Technology Group Co., Ltd. et al. ("BOE" or "Petitioner") in the above-captioned matter as an independent consultant to offer opinions regarding the patentability of the claims in U.S. Patent No. 9,330,593 ("the '593 patent" or "the challenged patent").

2. In the preparation of this Declaration, I have confined my analysis to the materials and opinions that were available at the time of the preparation of this Declaration – supplemented with my own knowledge and experience in the field. Should new materials, analyses, or opinions be introduced subsequent to the filing of this Declaration, I reserve the right to provide supplementary Declarations to the extent necessary to address any such newly introduced items.

3. If requested, I am prepared to explain (in a deposition or at a trial before the Patent Trial and Appeal Board (the "Board")) the technology disclosed in the challenged patent – including the state of the art in the relevant timeframe. Similarly, I am prepared to explain the technology disclosed in the prior art references cited herein. This may include, among other things, background information on driver circuits and OLED displays.

II. QUALIFICATIONS

4. My qualifications to testify as an expert in electronics technology are set forth in my *curriculum vitae* attached as Appendix A – which includes a listing of cases in which I have provided expert testimony. I have more than thirty years of experience as an engineer, scientist, and consultant in the electronics industry, including in the areas of integrated circuit (IC) design, layout, structure, and operation, in the design and analysis of transistor-based digital and analog circuits, in RF technology for wireless communications, in technology development, and in technical and business development.

5. My curriculum vitae contains further details regarding my experience, education, publications, and other qualifications that allow me to render expert opinions in connection with this proceeding.

III. COMPENSATION

6. I am being compensated for my work in this matter at an hourly rate of $425 for consulting services. My compensation does not depend on the content of my opinions or the outcome of this proceeding.

IV. MATERIALS CONSIDERED

7. In preparing this declaration, I reviewed and considered the following materials, along with any other materials referenced in the body of my declaration:

Mianyang BOE Ex. 1003
Case No. IPR2023-01221
Page 7 of 273

Exhibit	Description
EX1001	U.S. Pat. 9,330,593 ("Jang")
EX1002	Prosecution History of U.S. Patent No. 9,330,593
EX1003	Unused
EX1004	U.S. Patent Publication No. 2013/0285888A1 ("Chung")
EX1005	U.S. Patent Publication No. 2013/0127807A1 ("Kim")
EX1006	U.S. Patent Publication No. 2008/0101529A1 ("Tobita")
EX1007	U.S. Patent Publication No. 2008/0062097A1 ("Jeong")
EX1008	Excerpts from *Analog Integrated Circuit Design*, David A. Johns et al., John Wiley & Sons, Inc., 1997.
EX1009	Complainant's Opening Claim Construction Brief, *In the Matter of Certain Active Matrix Organic Light-Emitting Diode Display Panels and Modules for Mobile Devices, and Components Thereof*, Inv. No. 337-TA-1351
EX1010	Excerpts from *Physics and Technology of Semiconductor Devices*, A. Grove, John Wiley & Sons, 1967.
EX1011	Excerpts from *CMOS Digital Integrated Circuits: Analysis and Design*, (third edition), S. Kang et al., McGraw-Hill, 2003.
EX1012	Unused
EX1013	U.S. Patent Publication No. 2003/0132931A1 ("Kimura")
EX1014	U.S. Patent Publication No. 2005/0185752A1 ("Sasaki")
EX1015	U.S. Patent Publication No. 2007/0139348A1 ("Lee")

8. I may use these documents and information, or other information obtained during the course of this proceeding, as well as representative charts,

graphs, schematics and diagrams, animations, and models based on those documents and information, to support and to explain my testimony.

9. My opinions are based in part on a review and analysis of the above-mentioned documents and materials. I have also drawn on my education, experience, and knowledge of basic engineering and circuit design principles in forming my opinions.

V. UNDERSTANDING OF THE LAW

A. Legal Standards

10. I am not an attorney, but I have been informed of several legal principles, which I have employed in forming my opinions in this declaration. I have been informed that each patent claim is considered separately for purposes of patentability and that a dependent claim that depends from another claim includes all of the limitations of the claim it depends from.

1. Claim Construction

11. I have been informed that the claims of the challenged patent in this proceeding are to be construed using the same claim construction standard applied in district court. I have been informed the claim construction analysis begins with the ordinary meaning of a claim term, and there is a presumption that the term carries its plain and ordinary meaning to persons of ordinary skill in the art as of the effective filing date of the patent. I have also been informed that the most important

sources for determining the meaning of a claim term are the claims, the specification, and the prosecution history of the patent at issue, which collectively is called "intrinsic evidence." I have been further informed that the meaning of a claim term may also be guided by "extrinsic evidence," such as contemporaneous dictionaries and treatises, as well as the testimony of technically skilled witnesses such as myself.

2. Burden of Proof

12. I have been informed that the petitioner in an *inter partes* review bears the burden of establishing unpatentability by "a preponderance of the evidence." I have been further informed and understand that, to prove an assertion by "a preponderance of the evidence," the party with the burden of proof must demonstrate that it is more likely than not that the assertion is true.

3. Anticipation

13. I have been informed that a patent claim is unpatentable if it is "anticipated" by prior art. I have been informed that a reference anticipates a claim if the reference discloses each limitation of the claim at issue, either expressly or inherently. I have been informed that a prior art reference may anticipate a claim without disclosing a feature of the claimed invention if that missing characteristic is necessarily present, or inherent, in the single anticipating reference as would have been understood by one of ordinary skill in the art.

14. I have been informed that material not explicitly contained in a single prior art document may still be considered for purposes of anticipation if that material is incorporated by reference into the document.

4. Obviousness

15. I have been informed that a patent claim is unpatentable if it would have been obvious to a person of ordinary skill in the art ("POSITA") at the time of the claimed invention. I have been further informed that a claimed invention is not patentable if differences between it and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. I have been informed that factors relevant to the determination of obviousness include the scope and content of the prior art, the level of ordinary skill in the art at the time of the invention, differences between the claimed invention and the prior art, and "secondary considerations" or objective indicia of non-obviousness.

16. I have been informed that a single reference alone can render a patent claim obvious, if any differences between the reference and the claim would have been known or obvious to a POSITA at the time of the invention. That is, if the POSITA could have adapted the reference to meet the claims of the patent by applying known concepts to achieve expected results, then the patent claims are rendered obvious by that reference.

17. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yielding predictable results. I have been further informed and understand that when a patent claim simply arranges old elements with each performing the same function it had been known to perform, and yields no more than one of ordinary skill would expect from such an arrangement, the combination is obvious.

18. I have been informed that a patent claim composed of several limitations is not obvious merely because each limitation was independently known in the prior art. Hindsight reasoning is not an appropriate basis for combining references to form an obviousness combination. I have been further informed that it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine multiple prior art references, or multiple teachings of the same prior art reference.

19. I have been informed that various "secondary considerations" (sometimes referred to as objective indicia of non-obviousness) may support a determination of non-obviousness and that such secondary considerations must be considered as part of an obviousness analysis. I have been informed that even strong evidence of secondary considerations may not be sufficient to rebut a strong showing of obviousness. I have been informed that the patentee bears the burden of showing the existence and effect of secondary considerations of non-obviousness, after which

the burden of coming forward with rebuttal evidence shifts to the party arguing obviousness. I have been informed that the following secondary considerations may indicate non-obviousness:

20. Copying: evidence that others, including the accused infringer, copied the patented invention.

21. Long-standing problem or need: evidence of a persistent problem or need in the art that was resolved by the patented invention.

22. Prior failure: evidence that others have tried and failed to solve the problem or failed to provide the need resolved by the claimed invention.

23. Commercial acquiescence of competitors: the willingness of industry to license the patent at issue.

24. Skepticism: evidence that those of ordinary skill in the art were skeptical as to the merits of the invention.

25. Praise: evidence of praise directed to an invention by others in the field.

26. Unexpected results: evidence that those of ordinary skill in the art were surprised by the capabilities of the claimed invention.

27. I have also been informed that the near-simultaneous invention by others can be evidence that a claimed invention is obvious. I have further been informed that the patentee bears the burden of showing a "nexus" between the claimed invention and the evidence proffered on secondary considerations (*e.g.*,

proof of commercial success of a product that practices the claimed invention is not enough; there must be evidence that the commercial success resulted, at least in part, from the claimed invention).

B. Priority Date

28. I have been informed that a U.S. patent may claim "priority" to the filing date of one or more earlier filed applications. I have been informed that the priority date, also called the "effective filing date," is the earliest filing date to which a claim is entitled – and that such date is relevant for determining what qualifies as prior art. I understand that a claim must have written description support in the application(s) to which it claims priority to be entitled to an earlier effective filing date. I have been informed that the priority date determination is done on a claim-by-claim basis, and that claims in the same patent may have different priority dates. I have not seen any particular evidence that supports Patent Owner's assertion that the '593 patent has a September 20, 2012 priority date; however, the references I relied upon in preparing this declaration are prior art with respect to that date.

C. Level of Skill in the Art

29. I have been informed that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons one of ordinary skill in the art may have for combining references.

30. I have been informed that factors that may be considered in determining the level of ordinary skill include: (1) the type of problems encountered in the art; (2) prior art solutions to those problems; (3) rapidity with which innovations are made; (4) sophistication of the technology; and (5) education level of active workers in the relevant field. I have been further informed that a POSITA is also a person of ordinary creativity.

31. The challenged patent pertains generally to the field of OLED displays, and more particularly to the circuitry used to drive and control the pixels that comprise the light-generating elements of the display. A person of ordinary skill in the art in the technology field of the '593 patent at the time of the alleged invention would have had a Bachelor's degree in electrical engineering or a similar discipline, along with 2-3 years of circuit design experience. A Master's or Ph.D. degree in a relevant field may substitute for some work experience and vice versa. I was at the time of the alleged invention at least a POSITA in the art relevant to the challenged patent. Further, based on my experience, I understand and know of the capabilities of a POSITA in 2012 – and I am familiar with how a POSITA would have understood and used the terminology found in the challenged patent at the time of its filing, and with the state of the art at that time.

VI. SUMMARY OF OPINIONS

32. I have been asked to compare various prior art references to Claims 1-9, 14-23, and 25 of the ’593 patent (the “Challenged Claims”). In my opinion, the Challenged Claims are all unpatentable as anticipated or obvious – based on these prior art references, combined with the knowledge of a POSITA.

33. My substantive analysis in Section XII provides examples of why these prior art references render the Challenged Claims unpatentable. I reserve the right to cite and rely on additional portions of these references in any future declarations or depositions.

VII. TECHNOLOGY BACKGROUND

34. Before considering the ‘593 patent in detail, some background on the technology of the ‘593 patent should be considered. This involves both the basic notions of transistor-based circuits, and of light-emitting elements (and their use in display screens).

A. Fundamental Concepts of Transistor-Based Circuit Design

35. Ever since the invention of the first transistor in 1947, transistors have been used as fundamental building blocks for the design of electronic circuits. Although a variety of transistor types have appeared over the years, by 2003 the transistor space was overwhelmingly dominated by a type of transistor that is known as the “field-effect transistor” (for reasons that will be described below). The

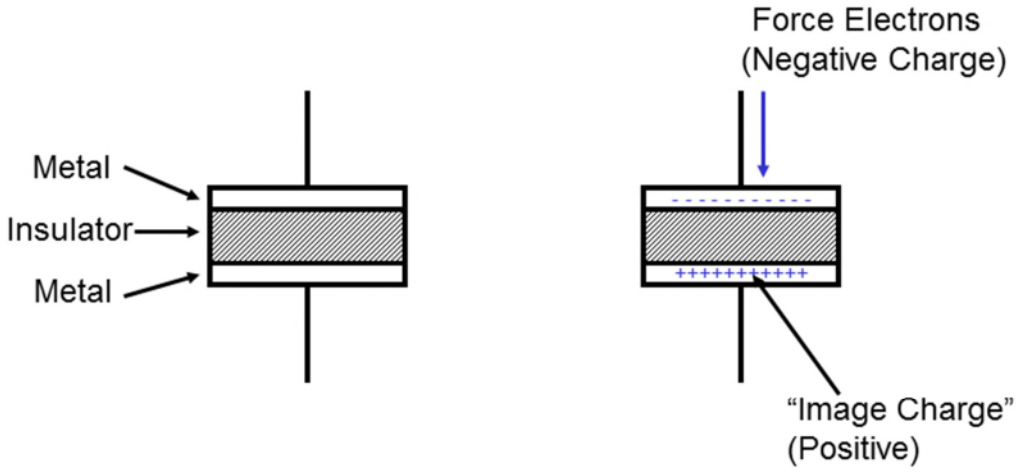
circuitry disclosed in the '593 patent is based on the use of field-effect transistors as the fundamental building blocks – with that particular type being known as a "thin-film transistor" (TFT); the TFT can be readily understood, due to its strong similarity to the better-known (and extremely ubiquitous) silicon-based metal-oxide-semiconductor field-effect transistor (MOSFET).[1]

36. Thus, before considering the '593 patent (and similar prior art), it is helpful to provide a brief overview of the basics of field-effect transistors and their usage in circuitry.

1. Field-Effect Transistors (FETs)

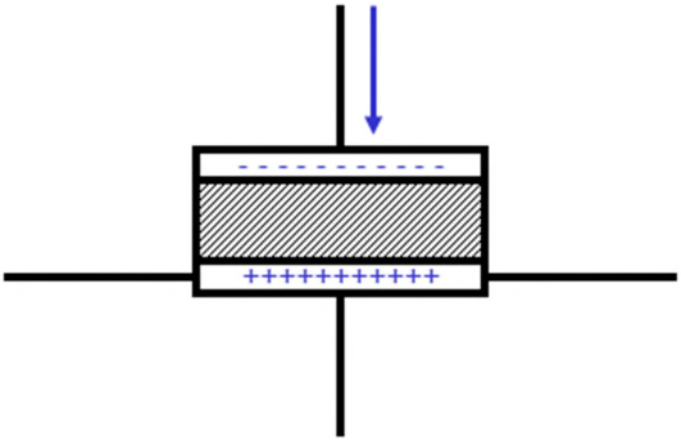
37. The field-effect transistor (FET) is actually based on a charge control mechanism that has long been known in the art – which is the simple charge control inherent in a basic capacitor.

[1] It is the silicon MOSFET that has been the specific transistor type that has made "Moore's Law" possible.



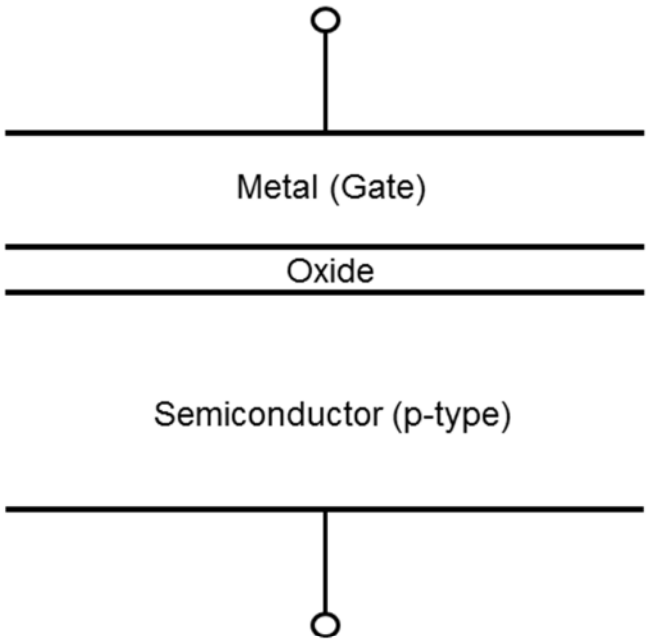
When a negative charge (electrons) is forced onto one plate of the capacitor, basic electromagnetic theory requires that a corresponding "image charge" (i.e., an equal-but-opposite charge) appear on the other plate of the capacitor. In the same way, if a positive charge is forced onto one plate of the capacitor, an equal-but-opposite negative charge appears on the other plate of the capacitor. A capacitor will store charge and maintain a voltage until discharged.

38. A field-effect transistor is based on using this ability (to create or remove a charge layer on the other plate of a capacitor as a charge-control mechanism) – combined with the addition of lateral contacts that allow current to flow when the image charge is present and to *not* flow when the image charge is absent.



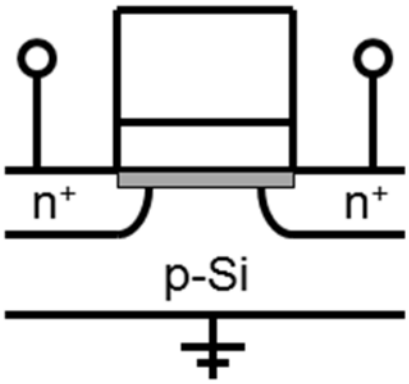
This, of course, indicates the possibility of using this type of structure as an on/off switch (with no moving parts).

39. In 1955, it was discovered (accidentally) that an insulating silicon dioxide layer can easily be grown on top of a silicon semiconductor substrate; by depositing a metal layer (such as aluminum) on top of the oxide, a simple capacitor is formed.



40. The silicon semiconductor layer is described as "p-type" – as it has (intentionally) been infused with a concentration of atoms of a species (usually boron) that contribute free positive (hence "p-type") charge to the silicon; these introduced impurity atoms are called "dopants," and the process of infusing them into silicon (or another semiconductor material) is known as "doping." When a positive charge is applied to the metal contact layer (i.e., the upper plate of the capacitor), a negative image charge forms at the surface of the silicon (as in a simple capacitor) – and is trapped there by the silicon dioxide insulator layer.

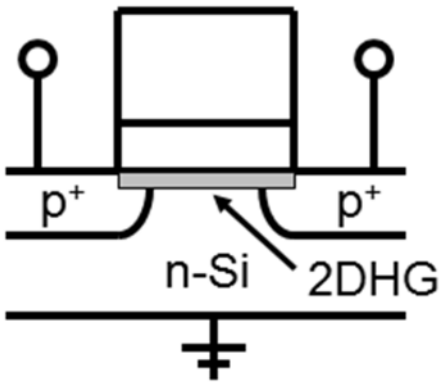
41. It was also long-known in the art that if other particular types of atoms (such as phosphorous and arsenic) are used as dopants, these atoms will cause negative-polarity free-charge to appear in the silicon – and it will be known as "n-type." If a very large amount of phosphorus or arsenic is infused into silicon that is already p-type, the n-type atoms will simply overwhelm (by sheer numbers) the p-type atoms – and the silicon so-infused will become selectively n-type. By infusing a small pocket of n-type atoms (in such a high concentration that the silicon becomes so strongly n-type that is often called "n+"), it is possible to create the sought-after two lateral contacts.



This structure provides the capacitor-with-lateral-contacts discussed earlier – so that the gate voltage controls the presence (shown in the figure) or absence of charge in the capacitor structure; meanwhile, the n^+ pockets provide the lateral contacts – so that current can flow (or not flow) based upon the presence of (or absence of) the induced charge layer; when the charge layer is present, applying a voltage difference between the lateral contacts will cause current to flow in the device. This type of transistor is known as an "nMOS transistor."

42. Also, while the MOS transistor clearly can be used as a simple on/off switch, it should be noted (for future reference herein) that the MOS transistor is a voltage-controlled current source – as the voltage on the gate controls whether or not (and to what degree) current flows between the lateral terminals.

43. Returning to the basic MOSFET structure, it is possible to reverse the polarities of the dopant atoms – so that the silicon substrate is n-type and the contact pockets are p^+.



Here, a negative voltage on the gate terminal will cause a positive charge layer to appear in the silicon, and current will flow when a voltage is applied between the two lateral terminals. This type of transistor is known as a "pMOS transistor."

44. It has long been known in the art that these two types of transistors (nMOS and pMOS) are not only structurally mirror images of each other – they are also electrical mirror images of each other. Writing in 1967, Andy Grove[2] (at pp. 329 – 330) described this situation for the two types of transistor:

> The preceding discussion so far was for an *n*-channel device of the type where we have to apply a positive voltage to the gate in order to bring about the onset of channel conduction. By complete analogy, the discussion could have been applied to a *p*-channel where a negative gate voltage would have been required to bring about channel conduction. Because with zero gate voltage applied neither of these devices conducts, such devices are called *normally "off"* MOS transistors. (Emphasis in the original.)

[2] EX1010, A. Grove, *Physics and Technology of Semiconductor Devices*, John Wiley & Sons, 1967.

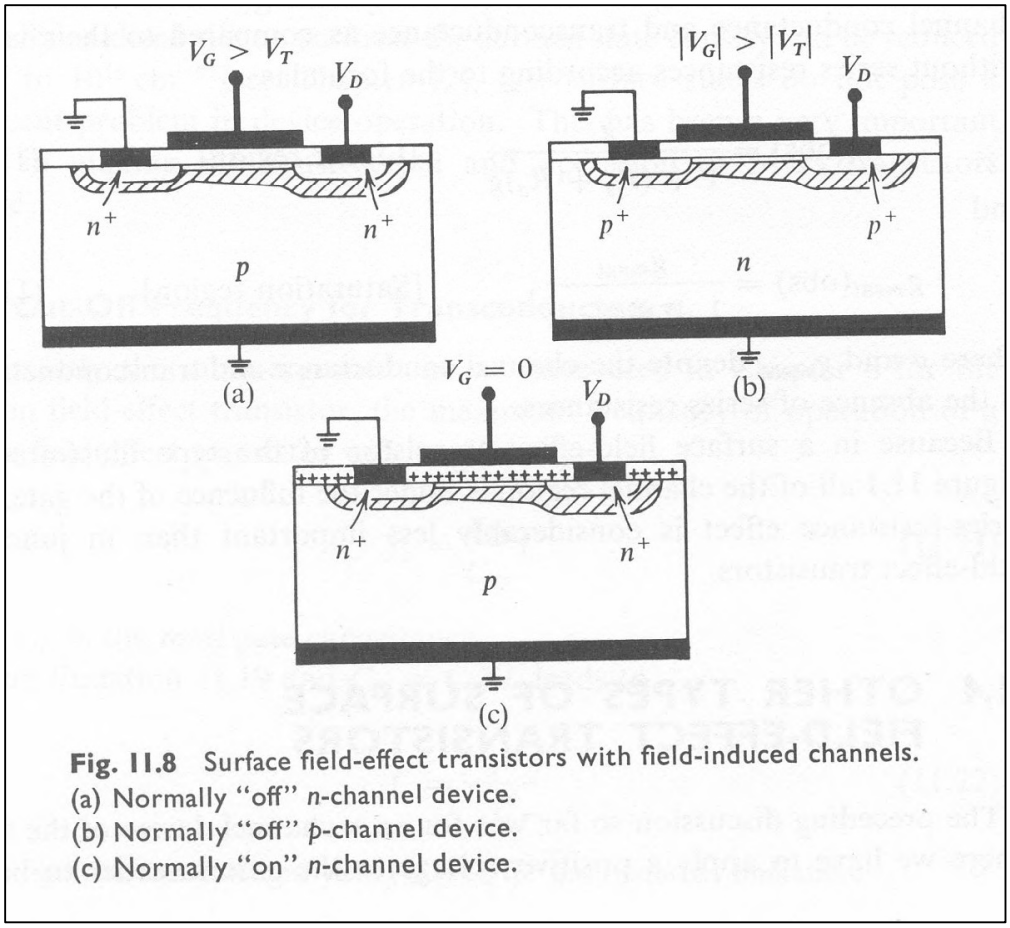


Fig. 11.8 Surface field-effect transistors with field-induced channels.
(a) Normally "off" *n*-channel device.
(b) Normally "off" *p*-channel device.
(c) Normally "on" *n*-channel device.

The MOS transistor was new at the time, and so this was the physics-based state of the art at the time.

45. However, it was soon realized that nMOS transistors and pMOS transistors could be made to be "complementary" (a word-usage that will be explained momentarily) by changing the substrate bias that is applied to the pMOS transistor. As a more-recent textbook[3] on digital design states (at p. 71) the situation,

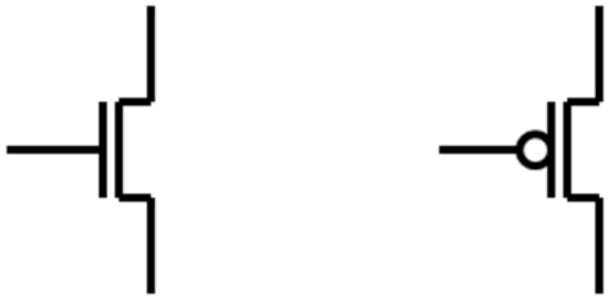
[3] EX1011, S. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design* (third edition), McGraw-Hill, 2003.

"Notice that in order to be biased properly, the n-well region must also have a VDD contact." As is well-known in the art, the n-well provides the substrate contact (via which the substrate bias is applied) for a pMOS transistor in a typical silicon fabrication process.

46. However, as they are fabricated in (as the name indicates) a thin film (rather than in a silicon substrate), thin-film transistors are unable to have a substrate contact (of the type shown above, in the figure from Grove 1967); only a gate contact and the two lateral contacts (for the current flow) are available.

47. Thus, thin-film transistors will not be able to use the type of complementarity that is fundamental to silicon-based transistor technology (such as the ubiquitous complementary MOS (CMOS) technology that dominates the semiconductor landscape today). Instead, nMOS thin-film transistors and pMOS thin-film transistors must be operated as per the discussion in Grove 1967 that was quoted above – that in order to induce conduction in an nMOS transistor a positive voltage must be applied to the gate, while in a pMOS transistor a negative voltage must be applied to the gate. In this way, nMOS and pMOS transistors are able to provide simple on/off switches – which turn on or off under mirror-opposite control voltages.

48. Further, the "complementary" situation also led, in the art, to the following simple circuit symbols for nMOS (left) and pMOS (right) transistor types.



An analog CMOS textbook[4] (from 1997) also shows commonly-used nMOS and pMOS transistor symbols. *See* EX1008 at 18 (especially Figure 1.7(a) and Figure 1.8(c)). The pMOS symbol in particular is notable for its inclusion of a small circle on the gate contact; this symbol is used in electronic circuitry (and digital-logic circuitry) to indicate "NOT" – which is a way of denoting a pMOS transistor as behaving in the opposite (i.e., "NOT") way as an nMOS transistor behaves.

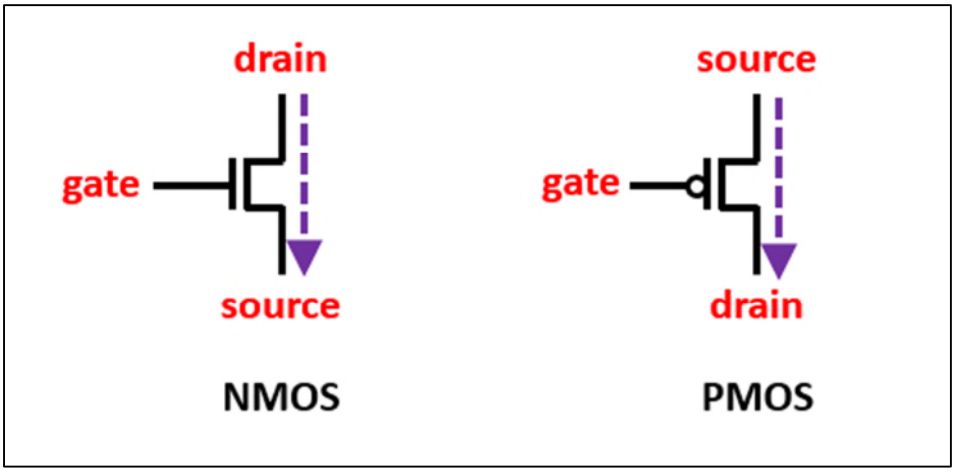
49. Even though a pMOS thin-film transistor is not able be rendered "complementary" (as it lacks a substrate contact), the use of the pMOS symbol depicted above is still commonly used in the art to represent a pMOS TFT.

50. Further, although the MOS transistor is inherently a symmetric device, some way of separately identifying the two lateral terminals is required. For historical reasons, the side that provides the entry point for carrier flow came to be known as the "source," while the side that provides the exit point for the carrier flow

[4] EX1008, D. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, 1997.

came to be known as the "drain." However, defining the "direction" of the current flow is slightly problematic – as "current" is defined in the art (and has been for centuries) as the direction in which what would be positive charge flows; thus, for example, if there is a flow of negatively-charged electrons moving in some direction, the defined direction of the current flow is the *opposite* of the direction in which the electrons are actually moving.

51. This situation can be depicted graphically:



This methodology allows the "source" and the "drain" to be defined via the direction of the current flow (which is determined by the relative voltages on the lateral terminals) in any particular transistor (of either type). This is explained succinctly in Chapter 1 of Johns & Martin 1997:

> It should be noted that there is no physical difference between the drain and the source. *The source terminal of an n-channel transistor is defined as whichever of the two terminals has a lower voltage.* For a p-channel transistor, the source would be the terminal with the higher voltage. When a transistor is turned on, current flows from the

> drain to the source in an n-channel transistor and from the source to the drain in a p-channel transistor. In both cases, the true carriers travel from the source to the drain, but the current directions are different because n-channel carriers (electrons) are negative, whereas p-channel carriers (holes) are positive.

EX1008 at 16-17 (emphasis in original).

52. In most circuit applications, the flow of current through any transistor during circuit operation is one-way – that is, current flows through any particular transistor in only one of the two possible ways[5]; this allows the current flow to define what are the "source" and the "drain" of any transistor based on this operational characteristic. However, the MOS transistor is inherently a symmetric device – where the current can be induced to flow in either direction by the application of different voltage differences between the two lateral terminals; a prominent example of this situation is the single transistor which controls the charge-storage node of a DRAM memory cell – where different lateral voltages (i.e., positive or negative) are used to put charge into the storage node and to take charge out of the storage node. In theory, the "source" and the "drain" would be swapped back-and-forth during these different circuit operations – even though there is (obviously) no material change in the transistor itself. Further, when a circuit "netlist" is created (usually

[5] This is the case for the circuitry disclosed in the '593 patent, and for the prior art considered in this Declaration.

for purposes of describing the circuit to a circuit simulation CAD tool, such as a SPICE circuit simulator), the four terminals of a MOS transistor (the drain, the gate, the source, and the substrate) must be explicitly specified – and will not be changed "on the fly" based on the voltages applied to a particular transistor; however, in this type of situation, if the sign of the voltage between the drain and source is reversed, the circuit simulator will simply cope with this – since, as mentioned above, the MOS transistor is inherently symmetric (and can be "operated" in either direction).

53. Fortunately (as mentioned above) this complex issue need not be of concern here – since (as also mentioned above) the circuitry described in the '593 patent (and in the prior art to be discussed later in this Declaration) operates such that current will only flow through any MOS transistor in one direction only. Thus, the scheme discussed above (and depicted in the figure above) of defining the "source" and the "drain" in terms of the current flow in the type of device in question (nMOS or pMOS) is workable here; thus, the working definition of "source" and "drain" will be used in this Declaration.

54. Finally, with respect to field-effect transistors in general and the '593 patent in particular, as was noted above the field-effect transistors in the '593 patent are of type known as a thin-film transistor (TFT). A TFT is sufficiently similar to a MOSFET (or, basically, any other type of field-effect transistor) to allow the basic understandings and descriptions (both qualitative and quantitative) associated with

the ubiquitous MOSFET (as detailed above) to be applied to the TFT. The patentee was aware of this basic relationship (as would be a POSITA) – and used it (as will be detailed later) to describe the TFTs that appear in the '593 patent.

55. TFTs are very advantageous in display applications – as they can be fabricated directly on the glass that is used in the display; however, TFTs (as just noted) are still field-effect transistors – and operate in the same way as do silicon-based field-effect transistors (as described above).

2. nMOS/pMOS Interchangeability

56. As detailed above, the nMOS transistor and the pMOS transistor are essentially mirror images of each other. Furthermore, as was detailed earlier, a field-effect transistor, in its simplest usage, provides an electronic on/off switch with no moving parts – and this statement applies to both nMOS and pMOS transistors. This has long been well-known in the art – as can be seen in Kang and Leblebici 2003 (EX1011 at 198):

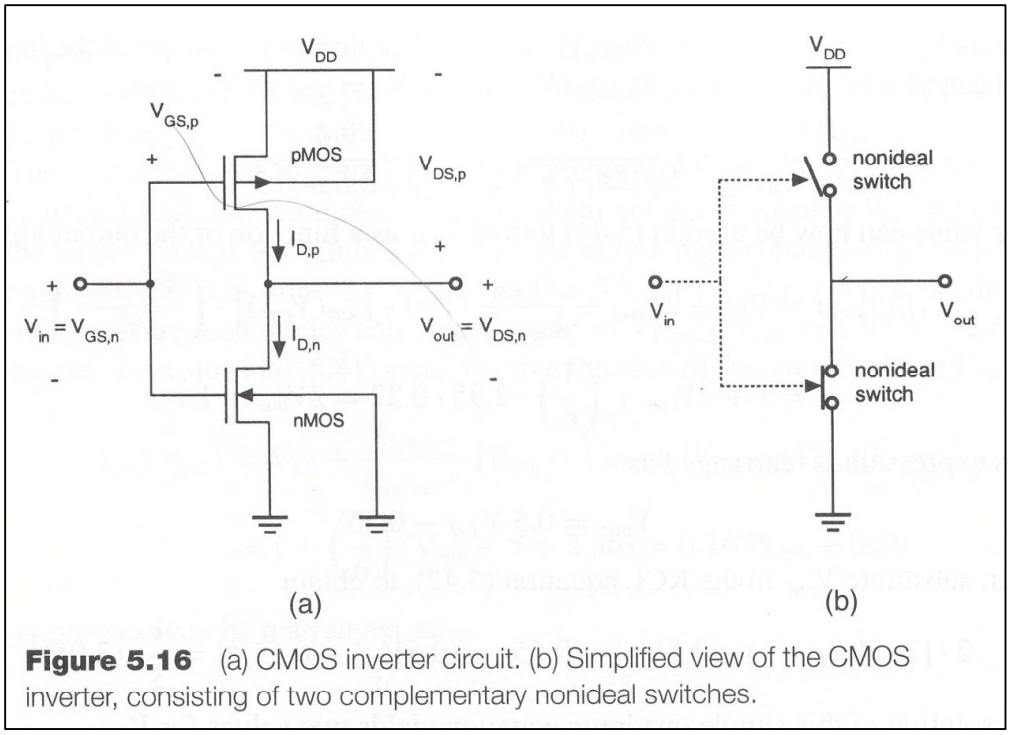


Figure 5.16 (a) CMOS inverter circuit. (b) Simplified view of the CMOS inverter, consisting of two complementary nonideal switches.

57. If the design need is for a transistor to be used as a simple on/off switch, then either an nMOS transistor or a pMOS transistor can be chosen – since, as shown in the figure from Kang and Leblebici 2003 above, each can function as a simple on-off switch. As the primary operational difference between nMOS and pMOS (when a simple switch is desired) is that the on/off characteristics are the opposite of each other – and the on-off signals to be applied must be altered (i.e., reversed as it were) to account for this. In particular, as described in Section VII.A.1, nMOS devices turn on in response to a "high" voltage on the gate terminal and turn off when a "low" voltage is applied. This is known in the art as "active-high" signaling. pMOS transistors are just the opposite – they turn on when a "low" voltage is applied to the gate terminal and turn off in response to a "high" voltage on the gate. This is known

in the art as "active-low" signaling. Changing the polarity of a switching transistor (from nMOS to pMOS or vice versa) would require changing the polarity of the gate signal to achieve the same functionality, but doing so was easy and well-known to a POSITA by the effective filing date of the '593 patent. For example, U.S. Patent Publication No. 2003/0132931 ("Kimura") teaches replacing nMOS transistors with pMOS transistors when the transistors function as simple on/off switches. *See*, *e.g.*, EX1013, [0438] ("Note that a structure is used [in Figs. 3B-3D] in which the TFTs 304 and 306 are n-channel TFTs.…**However, the TFTs 304 and 306 function as simple switching devices, and therefore any polarity may be used.**" (Emphasis added)); *id*., [0396] (same for Figs. 1B-2); *id.*, [0445] (same for Figs. 4B-4D); *id*., [0649] ("All other TFTs are only used as switching devices for performing only on and off control, and therefore may be of any polarity."); *id*., [0362] (showing an all-pMOS driver circuit in Fig. 22). Note that it was well known at the time to a POSITA that "any polarity" refers to the use of either nMOS or pMOS transistors (and see also Figure 5.16 from Kang and Leblebici, above).

58. Further, beyond just generally teaching the interchangeability of nMOS and pMOS switching transistors, Kimura actually provides further details about using pMOS transistors. For instance, Kimura discusses the replacement of the first or fourth transistor in Figure 33 with a pMOS device – and even provides an example circuit in Figure 34A, where the fourth transistor is a pMOS device. *See* EX1013,

[0659] ("[T]he polarity of one of the TFTs [first or fourth transistors] may be made opposite to the polarity of the other TFT…."). It was well-known to a POSITA at the time that "opposite polarity" refers to the two different transistor types – nMOS and pMOS (and again, see also Figure 5.16 from Kang and Leblebici, above).

59. As a further example, U.S. Patent Publication No. 2005/0185752 ("Sasaki") presents two equivalent embodiments, in which the pMOS transistors of one embodiment (as depicted in Figure 4) are replaced by nMOS transistors in another embodiment (as depicted in Figure 18):

FIG.4

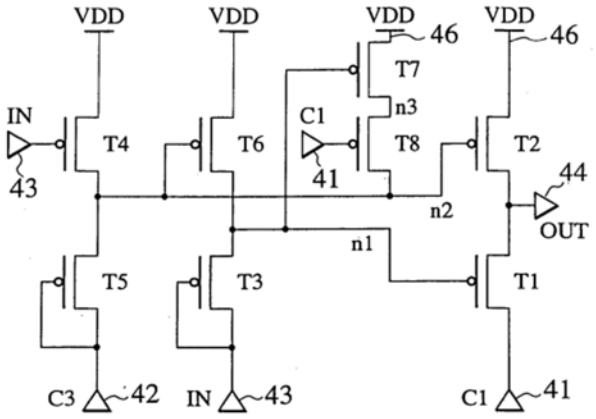
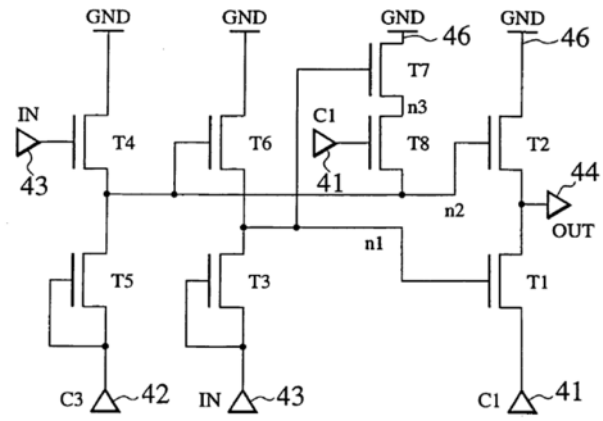


FIG.18



EX1014, Figs. 4, 18. As Sasaki explains,

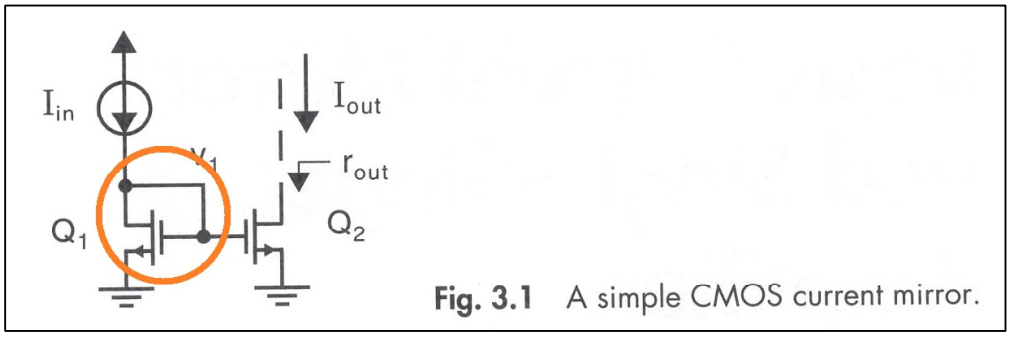
> Heretofore, description has been made throughout the first to the eighth embodiments regarding a case where the shift register is composed only of the p-MOS transistors for shifting the phase of the input signal IN having a concave waveform. Alternatively, it is also possible to arrange a shift resister composed only of n-MOS transistors for shifting a phase of an input Signal IN having a convex waveform. As shown in FIG. 18, all the transistors in the shift register of a ninth embodiment are n-MOS transistors. This shift register has a constitution where all the transistors shown in FIG. 4 are replaced by n-MOS transistors, and the voltage electrode 46 is connected to the ground potential GND. As a matter of course, without limitation to the shift register of FIG. 4, n-MOS transistors may replace the p-MOS transistors of the shift register in any of the other embodiments.

EX1014 [0084]. Note that, in contrast to Kimura, Sasaki's architecture requires a wholesale usage of transistors of all one polarity or the other (i.e., all-nMOS or all-pMOS), and the change from the VDD connections at the top (pMOS implementation) to GND connections at the top (nMOS implementation); however, the basic notion of the simple ability to exchange nMOS switching transistors for pMOS switching transistors is clearly shown.

60. These two examples confirm, as stated above, that it was well known in the art at the time of the '593 patent that, when used as simple switches, nMOS transistors and pMOS transistors are interchangeable.

3. The Diode-Connected Configuration of a Field-Effect Transistor

61. To connect a transistor "in the form of a diode" is something that is well-known in the art – and refers to a configuration of a field-effect transistor in which the gate of the transistor is directly connected to either the source or the drain of that same transistor. For example, Johns and Martins 1997 illustrates this well-known configuration being used in a current mirror:[6]



EX1008 at 125-126; annotation added. Referring to this figure, this text states (on p. 125): "Note that Q1 is diode-connected (i.e., its drain and gate are connected)…." As can be seen, in this configuration, the gate and the drain are directly connected together – so that the voltages on these two transistor terminals will always be the same in this configuration. As the gate/drain voltage is increased above the threshold voltage, the output current increases in a form that strongly resembles the current-voltage characteristic of a forward-biased diode – and hence the name of this

[8] The diode-connected portion of the current mirror is circled in orange.

structure, even though the transistor is not actually functioning explicitly as a diode does.

4. The Transistor Threshold Voltage

62. In Section VII.A.1, the basic notions of field-effect transistors were presented. In particular, for the simplified case of the use of such transistors as simple on/off switches, the operational considerations for the transistors involved are also rather simple.

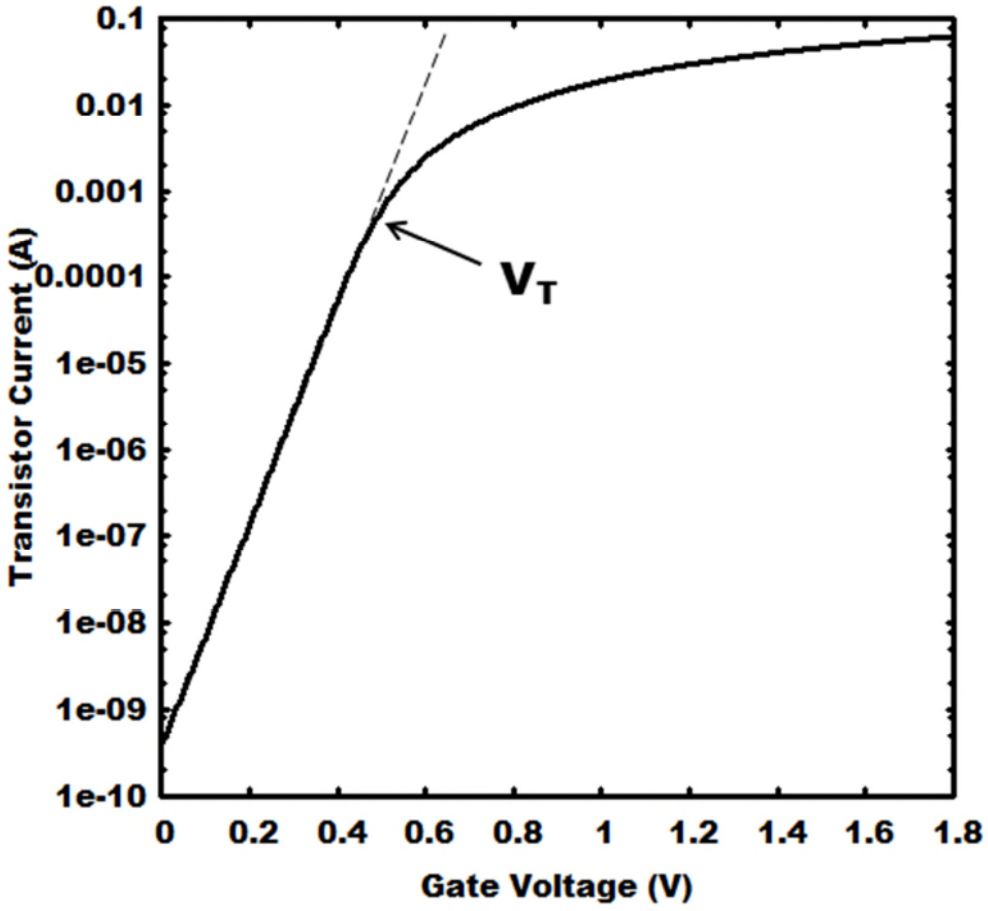
63. However, one issue that was glossed over is how the "off" state and the "on" state are differentiated from each other – other than that these two operational states actually exist. The only other consideration (to be discussed below) is to make sure that the "on" state is really on, and (more challenging) that the "off" state is really off.

64. In Section VII.A.1, it was described how a field-effect transistor is turned on or off by changing the gate voltage from either high-to-low or low-to-high). That the "change" must occur at *some* particular (and identifiable) gate voltage value (for a particular transistor); that particular voltage value has long been known in the art as the "threshold voltage." *See*, *e.g.*, EX1008 at 20.

65. In an ideal transistor, for a gate voltage below the threshold voltage, the transistor would simply be completely off (i.e., absolutely *no* current flowing through it), while for a gate voltage above the threshold voltage, the transistor would

be in a completely-on state (i.e., for any gate voltage above the threshold voltage, the current is constant at the "on" current level). In fact, in this situation, the actual value of the threshold voltage would essentially not matter – as long as it was somewhere between the low voltage level and the high voltage level (of the on/off logic voltage levels).

66. However, the field-effect transistor is not so simple a structure – and the threshold voltage behavior is much more complex. This is readily illustrated by an exemplary depiction of the device current (in logarithmic scale) versus the applied gate voltage.



In this figure, the threshold voltage can be defined via the point where the straight line at low gate voltage changes (as the gate voltage increases) to the more-slowly increasing curve.

67. This curve shows that the MOS transistor does not, in detail, operate explicitly as a simple on/off switch; rather, the behavior of the current as a function of the gate voltage shows what was stated earlier – that in detail, the MOS transistor (like all field-effect transistors) is a voltage-controlled current source. In addition, this curve highlights the two critical issues that revolve around the "threshold voltage" *not* being able to exist as a simple dividing point between (as described above) all-off and all-on.

68. First, it can be easily seen that for gate voltages above the threshold voltage, the current is not a constant with gate voltage – but, rather, increases noticeably for higher gate voltages. As circuit switching speed is (among other things) a direct function of the current, it is desirable (in the on state) to have as much current as possible flowing through the transistor – which indicates that the threshold voltage should be as low as possible.

69. Second, though, it can also be seen that the characteristic behavior of a field-effect transistor is not ideal – in that the transistor current does not go to zero just below the threshold voltage, but rather decreases (exponentially) as the gate voltage decreases below the threshold voltage. As a result, the threshold voltage has

to be chosen (during manufacturing-process design) to be somewhat higher than the desired near-zero gate-voltage value – so that the off-state current that flows through the transistor will not be too large.

70. In sum, the value of the threshold voltage should be as low as possible – but not lower; otherwise, even though the transistor will be to some degree "off," there will be too much current flowing in the "off" state – which is something that can have serious-and-unpleasant consequences in most circuit applications.

B. Pixel-Based Displays

71. As the title of the '593 patent indicates, the '593 patent involves displays. As the '593 patent makes clear (such as in Figure 1), these displays are comprised of pixels – wherein a "pixel" (short for picture element) is a single dot in the display, and a very large number of such pixels are constructed together, so that the pixels can, collectively, produce an image on the display.

72. There are two notably aspects of such displays that are material to the disclosures of the '593 patent. One is the particular technology that is used for the fabrication and operation of the pixels themselves, and the other is the organization and control of the set of pixels in a display (so that an image can be created on the display); these two issues will be considered in turn, with the second issue being divided into two separate sections.

1. Pixel Technologies

73. As its title indicates (via "organic light emitting display"), the '593 patent involves the use of organic light-emitting diodes (OLEDs). OLEDs are able to be used in pixels (to create an image on a display), since they will emit light – and will do so under the control of electronic circuitry. OLEDs function in basically the same manner as do conventional LEDs – but they have come into wide use in displays, for a variety of reasons. Among the noted advantages[7] of OLEDs (particularly when used in displays) are the lighter materials involved (which are plastic), flexibility (again, because OLEDs use plastic material), greater brightness, lower power consumption, and ease of manufacturing (as they can be produced in sheet form rather than as individual LEDs).

74. However, other types of pixel technologies were well known in the art (and had been for some time). One prominent example is liquid crystal display (LCD) technology. As the name implies, an LCD pixel involves a liquid crystal – with the key aspect that the liquid crystal configuration can be changed using an applied electric field; the applied field is able to change the configuration of the liquid crystal from one of two possible forms to the other, with the configuration remaining in place even after the electric field is removed. The state of the liquid

[7] https://electronics.howstuffworks.com/oled5.htm.

crystal can thus be induced by applying an electric field – so that the liquid crystal (working in tandem with polarizers) either passes or blocks the passage of light. By placing a liquid crystal in front of backlight, the light can be allowed to pass, or it can be blocked; by using a large number of such liquid crystals as pixels, an image can be created on a display by controlling each pixel as an individual unit (in essentially the same general way as is done with LED/OLED-based pixels in displays based on LEDs/OLEDs).

75. Like OLED technology, LCD technology allows for the easy creation, along with the pixel-base technology, of thin-film transistors (TFTs) in the same manufacturing process. Thus, again like OLEDs, the control circuitry for LCDs can be created *in-situ* with the pixels – so that the control circuitry need not be separate.

76. LCD TFTs provide the same advantages as those discussed above with respect to OLEDs. LCD displays are often preferable in situations where either cost or power consumption (or both) is of high importance.

2. Pixels and Pixel Arrays

77. A pixel is the basic unit of a light-based display screen – with that display consisting of row and columns of pixels – with a higher pixel density leading to a higher resolution in the display. This row/column structure of a display is well-known in the art by the use of the number of rows and columns that a display has – such as 1280 x 720, 1920 x 1080, and so forth. Note that these numbers provide the

Mianyang BOE Ex. 1003
Case No. IPR2023-01221
Page 40 of 273

total number of pixels in a display – irrespective of the physical size of the display. In general, it is the areal density of pixels in a display that defines the quality of the image that can be produced by a display. Each pixel includes driving circuitry that provides current to the diode; further, each pixel typically includes a "driving transistor" to provide current for the light emitting diode, and various "switching transistors" that act as on/off switches to control the operation of the pixel.

78. Further, as the numbers above indicate (and as mentioned in association with them), in a display, the pixels are arranged into rows and columns – and these row and columns of the display are activated sequentially to produce images on a display screen.

79. In addition to pixel density, the quality of a display image is also a function of the brightness of the pixels – with brighter pixels generally leading to better image quality.

3. Scan Lines and Control Signals in a Display

80. As noted above, in a display based on pixels, the pixels are typically arranged in a row-and-column fashion. In operation, the individual pixels are generally not all "fired" simultaneously – that is, as individual pixels must change (i.e., turn on or off) when the image to be displayed changes, the individual pixels typically do not all change together at the same time.

81. Rather, a technique that has been used since the invention of screens that create dynamic images using some form of light (that is, going back to the earliest days of cathode-ray tubes (CRTs), such as those used in the first televisions) has been adopted. In this technique, the rows (sometimes called "lines") of the display are treated as the basic units for changing pixel output as the display image changes – with all the pixels of a single row being changed as needed, and then the same process being applied to the next row, etc. In the context of an OLED display or LCD (liquid crystal display), a "scan signal" or "scan line signal" generally refers to the aforementioned control signal that is used for programming a line/row of pixels. This process continues until the entire display has been refreshed – via this sequential refreshing of each row; further, once the entire display has been refreshed in sequence, the next overall refresh sequence can begin.[8] As long as the speed of the refresh rate is faster than the ability of the human eye to detect it, the viewer will perceive the entire image changing fluidly upon the screen.[9]

---

[8] There have long been variations on this basic theme – such as, for example, refreshing every other row in one refresh pass, then refreshing the previously-unrefreshed row in the next refresh path; however, the basic approach of refreshing the display by sequentially (in one form or another) refreshing rows of pixels remains essentially the same.

[9] If the refresh rate is "too slow," the human eye will perceive a noticeable (and unpleasant) flicker in the display.

82. As can be inferred from this discussion, a significant amount of behind-the-scenes control circuitry has long been required to manage this rather intricate sort of screen-refresh operation. But this was a well-explored and well-understood technical field – wherein various basic circuit concepts were routinely mixed and matched as needed to achieve a POSITA's design goals. It was this sort of control circuitry that is the main topic of the '593 patent.

VIII. THE CHALLENGED PATENT

83. U.S. Patent No. 9,330,593 ("the '593 patent" or "the challenged patent") is entitled "Stage Circuit and Organic Light Emitting Display Using the Same." The listed inventor is H. Jang. The '593 patent claims priority to a Korean application (No. 10-2012-0104512), which was filed on September 20, 2012.

A. General Overview

84. As the title indicates, the '593 patent discloses circuitry that is used to control the OLED light emitters that are used in displays; the patentee claims that the disclosed circuitry is simpler and requires fewer transistors. As the '593 patent asserts, its embodiments "provide stages having a reduced number of transistors and that output scan signals only using first and second clock signals. In contrast, conventional stage circuits includes [sic] a plurality of transistors, e.g., at least ten transistors, to supply the scan signals and/or require use of initializing signal in addition to the first and second clock signals." ('593 patent at 9:12-18.)

85. The ’593 patent goes on to explain what it considers to be the benefits of having a reduced number of transistors and initializing signals: “When a number of transistors in a stage increases, process yield deteriorates, so that stability of driving is deteriorated. When more initializing signals are required, there is less time for supplying scan signals, therey [sic] reducing stability. When a number of transistors is increased and/or more initializing signals are required, complexity increases. Therefore, stages according to embodiments, and an organic light emitting display using the same, improve stability and reduce complexity.” (*Id.* at 9:18-26.) The ’593 patent thus asserts that the components’ arrangements in the circuits in its specification are the purported inventive concept, and are necessary to achieve these recited benefits. Consistent with Patent Owner’s proposed constructions and infringement theories from the related ITC Investigation, however, the claims of the ’593 patent impose no requirements on the number of transistors or initializing signals.

B. File History

86. The application which led eventually to the issuance of the ‘593 patent was filed with the USPTO on February 20, 2013, and claims priority to a Korean application (No. 10-2012-0104512), which was filed on September 20, 2012. This application was published on March 20, 2014 as US2014/0078029.

87. On October 21, 2014, the applicant received a non-final rejection from the USPTO, on the grounds that the application contained "independent or distinct" species – and the applicant was required (by law) "to elect a single disclosed species, or a single grouping of patentably indistinct species."

88. On December 19, 2014, the applicant replied that were identifying a particular species, and as support provided a Korean patent application (KR 10-2013-0000020).

89. On February 9, 2015, the applicant received a non-final rejection from the USPTO. Claims 1-3, 5, 7, 8, 14-18, 20, 21, and 27 were rejected as being anticipated by Jeong (US2008/0062097), Claim 4 was rejected as being unpatentable based on Jeong in view of Chung (US2011/0227884), and Claims 6 and 19 were rejected as being unpatentable based on Jeong in view of Kim (US2012/0062525).

90. On May 5, 2015, the applicant provided a reply, in which Claims 1 and 14 were amended, Claims 9 - 13 and Claims 22 - 26 were withdrawn, and a new claim (Claim 28) was added.

91. On June 17, 2015, the applicant received a final rejection from the USPTO. Claims 1-3, 5, 7, 8, 14-18, 20, 21, 27 and 28 were rejected as being unpatentable based on Jeong in view of Lee (2011/0115835), Claim 4 was rejected as being unpatentable based on Jeong in view of Lee in further view of Chung, and

Claims 6 and 19 were rejected as being unpatentable based on Jeong in view of Lee in further view of Kim.

92. On August 13, 2015, the applicant provided a reply, in which Claims 1, 2, 13, 14, 16, 17, and 26 - 28 were amended.

93. Following an interview on August 21, 2015 (in which U.S. Patent 8,553,026 was discussed), on August 27, 2015 the Examiner provided a reply in which he stated that he "believes that CK2 of Fig. 3 of the '026 patent discloses Applicant's amended limitation and may anticipate claim 1."

94. On September 17, 2015, the applicant provided a reply, in which Claims 1, 2, 13, 14, 16, 17, and 26 - 28 were amended. The applicant argued that the amended claims including "the signal of the third input terminal directly ~~at least~~ controls an on/off operation of a transistor, the transistor included in the first driver ~~switch~~" were allowable over the Examiner's references.

95. On January 4, 2016, the Applicant received a notice of allowability. The reason of allowance cited the last amendment in reasons for allowance and withdrew the earlier restriction requirement. U.S Patent No. 9,330,593 issued on May 3, 2016.

C. Claim Construction

96. It is my understanding that the Board only construes particular claim terms of the patent at issue when necessary. Otherwise, all claim terms should be

given their plain-and-ordinary meaning, as that meaning would have been understood by a person of ordinary skill in the art at the time of the alleged invention, taking into consideration the language of the claims, the specification, and the prosecution history.

97. In this proceeding, consistent with Patent Owner's proposed constructions and infringement theories in the related ITC Investigation, I have applied plain-and-ordinary meaning to all claim terms – though I do not necessarily agree with Patent Owner that all claim terms should be construed based on their plain-and-ordinary meaning.

98. Should the Board construe a term differently, I reserve the right to supplement my analysis and conclusions – particularly if the construction of any term changes the substance of my analysis and/or conclusions.

IX. OVERVIEW OF THE PRIOR ART REFERENCES

99. In the unpatentability analysis which follows in Section XII, four grounds of unpatentability are provided – based on four prior art references. A brief overview of each of these references will be provided here.

A. Chung

100. The Chung reference ("Chung") is U.S. Patent Application Publication No. 2013/0285888, entitled "Scan Driving Device and Driving Method Thereof."

The filing date is listed as August 24, 2012; this filing date makes Chung prior art to the '593 patent.

101. The technological field of Chung is (as depicted in Figure 1) circuitry which controls and drives the pixels of a display. Chung mentions as an example OLED displays (*see, e.g.*, EX1003 [0063]). It was well understood in the art at the time that one of a variety of technologies (LCD, LED, OLED, and others) could constitute the particular technology used in a particular display – with the same driving circuitry able to be used across this variety of display technologies.

102. As per the title, Chung's particular focus is on the scan driving circuitry – that is, the circuitry that controls and drives the rows of pixels in a display. Several embodiments of field-effect-transistor-based circuitry that perform this function are disclosed in Chung.

B. Kim

103. The Kim reference ("Kim") is U.S. Patent Application Publication No. 2013/0127807, entitled "Scan Driver and Driving Method Thereof." The filing date is listed as April 18, 2012; this filing date makes Kim prior art to the '593 patent.

104. The technological field of Kim is (as depicted in Figure 1) circuitry which controls and drives the pixels of a display. Kim mentions as an example OLED displays (*see, e.g.*, EX1004 [0082]). It was well understood in the art at the time that one of a variety of technologies (LCD, LED, OLED, and others) could

constitute the particular technology used in a particular display – with the same driving circuitry able to be used across this variety of display technologies.

105. As per the title, Kim's particular focus is on the scan driving circuitry – that is, the circuitry that controls and drives the rows of pixels in a display. Several embodiments of field-effect-transistor-based circuitry that perform this function are disclosed in Kim.

C. Tobita

106. The Tobita reference ("Tobita") is U.S. Patent Application Publication No. 2008/0101529, entitled "Shift Register and Image Display Apparatus Containing the Same." The filing date is listed as July 31, 2007; this filing date makes Tobita prior art to the '593 patent.

107. The technological field of Tobita is (as depicted in Figure 1) circuitry which controls and drives the pixels of a display; although Tobita mentions LCD displays (*see, e.g.*, EX1006 [0004]), it was well understood in the art at the time that one of a variety of technologies (LCD, LED, OLED, and others) could constitute the particular technology used in a particular display – with the same driving circuitry able to be used across this variety of display technologies.

108. As per the title, Tobita's particular focus is shift register circuity, which provides the scan driving circuitry (which Tobita refers to as both the "gate-line driving circuit" and the "scanning-line driving circuit"), which controls and drives

the rows of pixels in a display. Several embodiments of field-effect-transistor-based circuitry that perform this function are disclosed in Tobita.

109. Tobita discloses embodiments with portions that are identical, and uses the same reference designators to indicate components having the same or analogous functions. (*See, e.g.*, *id.* [0168], [0172], [0177].) In particular, the embodiment of Figure 7 constitutes part of the embodiments of Figures 19 and 20. (*See id.* Figs. 7, 19, 20, [0168], [0172], [0177]). The identical or analogous portions of the embodiment have the same functionality, and Tobita's disclosure with respect to one embodiment applies to the other embodiments as well.

D. Jeong

110. The Jeong reference ("Jeong") is U.S. Patent Application Publication No. 2008/0062097, entitled "Shift Register and Organic Light Emitting Display Using the Same." The filing date is listed as July 12, 2007; this filing date makes Jeong prior art to the '593 patent.

111. The technological field of Jeong is (as depicted in Figure 2) circuitry which controls and drives the pixels of a display; although Jeong specifically mentions organic light emitting diodes (OLEDs) in the title, the circuitry disclosed by Jeong is not restricted to displays using OLEDs as the light-emitting device in a display.

112. As per the title, Jeong's particular focus is on the scan driving circuitry – that is, the circuitry that controls and drives the rows of pixels in a display. An embodiment of field-effect-transistor-based circuitry that performs this function are disclosed in Jeong.

X. MOTIVATION TO COMBINE CERTAIN PRIOR ART REFERENCES

113. As will be explained below (in Section XII), all of the claims of the '593 patent may be found in the referenced prior art – either explicitly, or in forms that require only modest (and obvious) modification. In one particular instance, a POSITA would be motivated to combine two prior art references – and would be able to do so without undue experimentation and a high expectation of success; that combination will be considered in the discussion of Ground 4, in Section XII.D.

XI. CLAIM TERMS

114. As explained in Section VIII.C, consistent with SDC's proposed constructions and infringement theories from the related ITC Investigation, I have given the terms in the challenged claims their plain and ordinary meanings, as would have been understood by a person of ordinary skill in the art at the time of the alleged invention, taking into consideration the language of the claims, the specification, and the prosecution history of the '593 patent. I have applied these understandings of the claim terms in my analysis and in forming my opinions where appropriate in this Declaration.

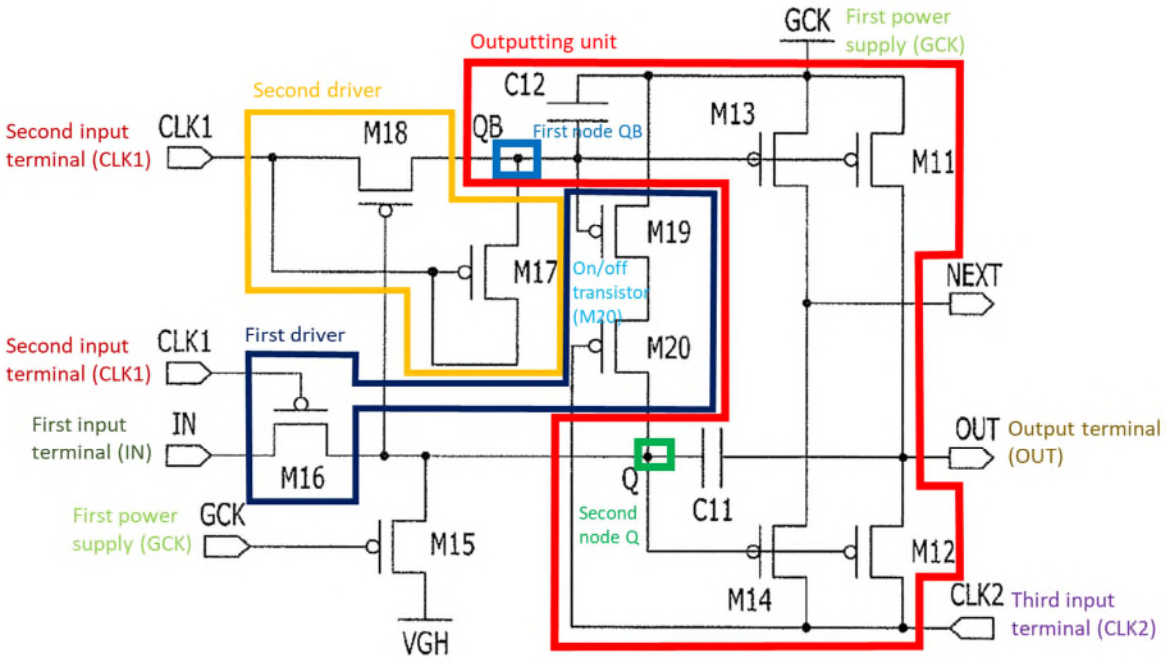
XII. UNPATENTABILITY ANALYSIS

115. As briefly mentioned above, from the analysis which follows, it is my conclusion and opinion that the challenged claims of the '593 patent are unpatentable – based on disclosures in the prior art. This analysis will encompass four separate grounds of unpatentability.

A. Ground 1: Chung Anticipates Claims 1-7, 9, 14-21, 23, and 25

116. As will be discussed below, it is my conclusion and opinion that Claims 1-7, 9, 14-21, 23, and 25 of the '593 patent are anticipated by Chung.

117. Before beginning a discussion of the analysis, it will be helpful to first provide an annotated version of Figure 4 of Chung – with the annotations indicating the identification of the specific structures recited in the claims of the '593 patent, as mapped to Chung.



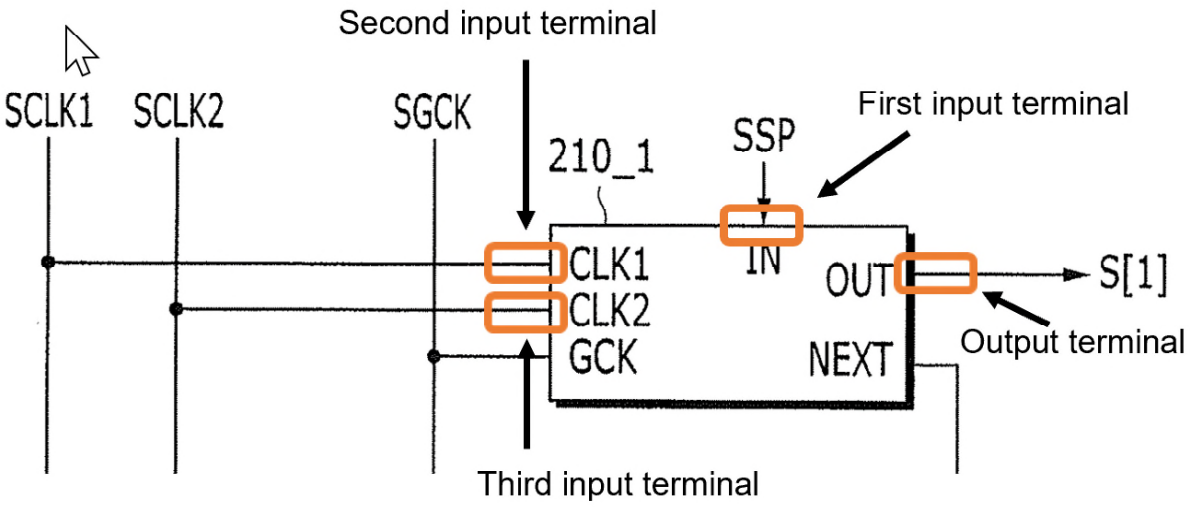
1. Independent Claim 1

118. It is my conclusion and opinion that Claim 1 of the '593 patent is anticipated by Chung.

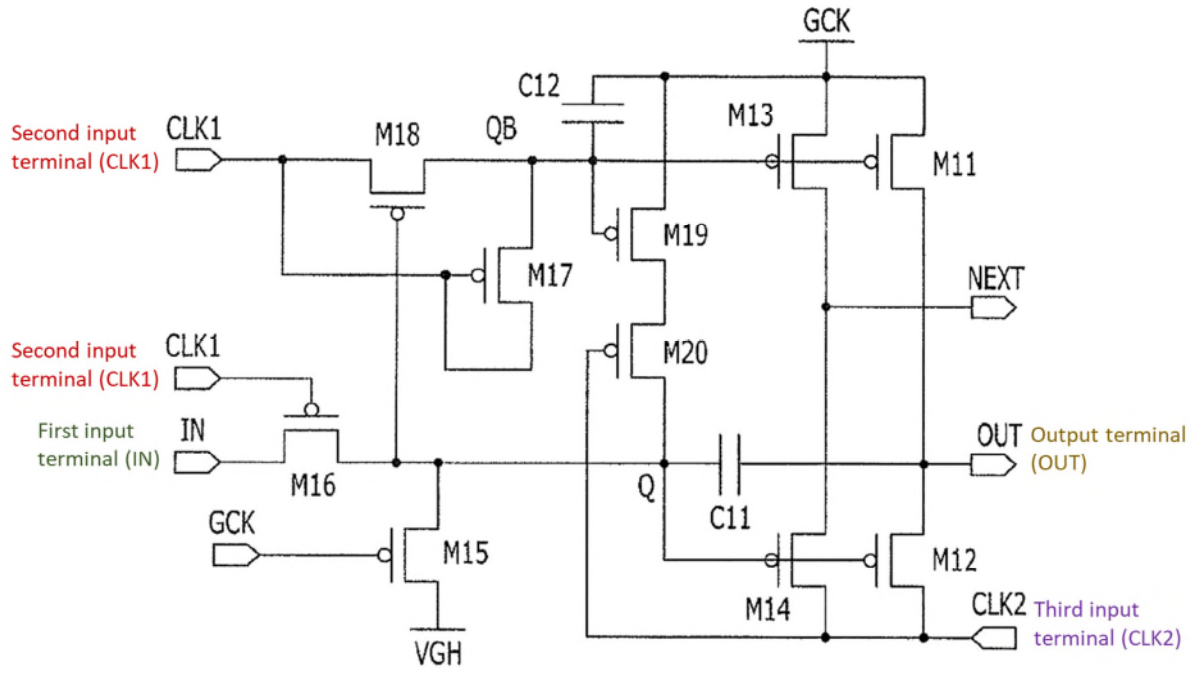
a. *[1-pre]: "A stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal, the stage circuit comprising:"*

119. As an initial matter, I will be offering no opinion regarding whether or not the preamble of Claim 1 is limiting. I have been instructed by counsel for Petitioner to offer an opinion as to whether or not the prior art discloses the preamble, regardless of whether or not the preamble is limiting.

120. Chung discloses the preamble of Claim 1 of the '593 patent; this can be seen readily via annotated versions of Figure 3 and Figure 4 of Chung:



(Excerpted from Figure 3 of Chung; annotations added.)



(Annotations added.)

121. The excerpt above from Figure 3 of Chung is the "black box" version of the more-detailed circuit depiction of Figure 4 of Chung; the annotations identify the same terms in both figures.

122. As can be seen in both annotated figures, Chung discloses a first input terminal, a second input terminal, a third input terminal, and an output terminal – all of which are part of a stage circuit.

123. Thus, Chung discloses the preamble of Claim 1 of the '593 patent.

b. [1-a]: "an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node:"

124. Claim element [1-a] is rather long – and thus the analysis will be simpler to explain if this claim element is broken up into sub-elements.

125. As a preliminary matter, note that this claim element requires "a voltage of a first power supply."

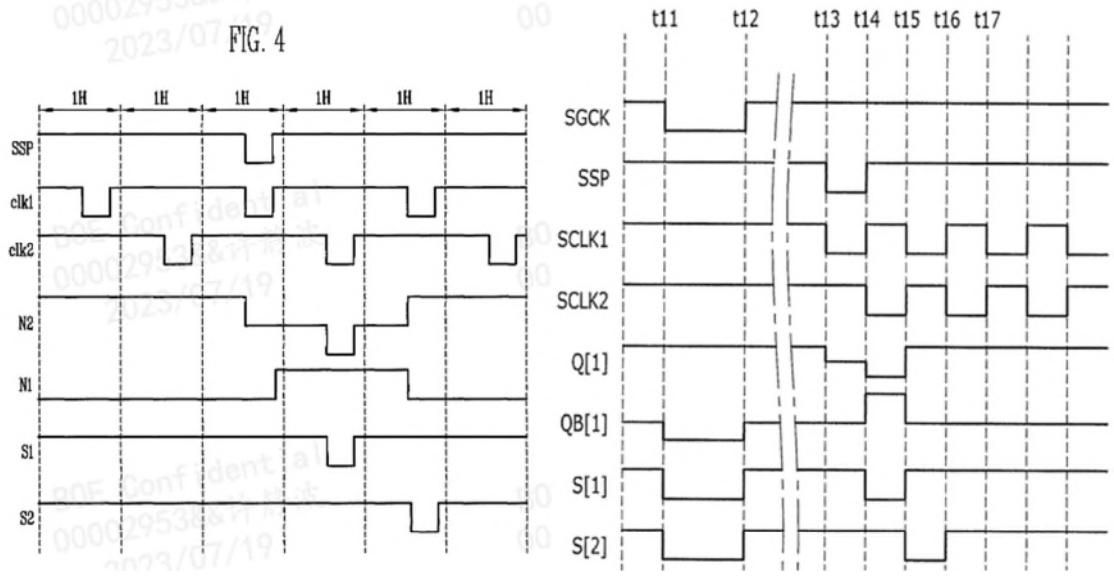
126. The actual scan operations for which Chung's circuitry has been designed begin at time t13, which Chung describes as:

> A period after t13 is a period of the scan step (c) during which the scan signals of the gate-on voltage are sequentially output to the plurality of scan lines S1-Sn. **During the period after t13, the output control signal SGCK is applied as a logic high-level voltage.** (Chung at [0097]; emphasis added.)

As this excerpt states clearly, beginning at time t13 the output control signal SGCK (which is applied to the output control signal input terminals of the stage circuits) is set to a logic high-level voltage – and remains constant at that logic high-level voltage during the scan operations.

127. Thus, during those circuit operations, the voltage at the stage circuit input terminal GCK is maintained at the logic high-level voltage (VGH) – and thus, during those circuit operations, GCK provides a power supply voltage. Therefore, it is acceptable, during the aforementioned scan operations, to refer to the voltage at the input terminal GCK as being the first power supply voltage – since a constant DC voltage will be applied there, and will not change.

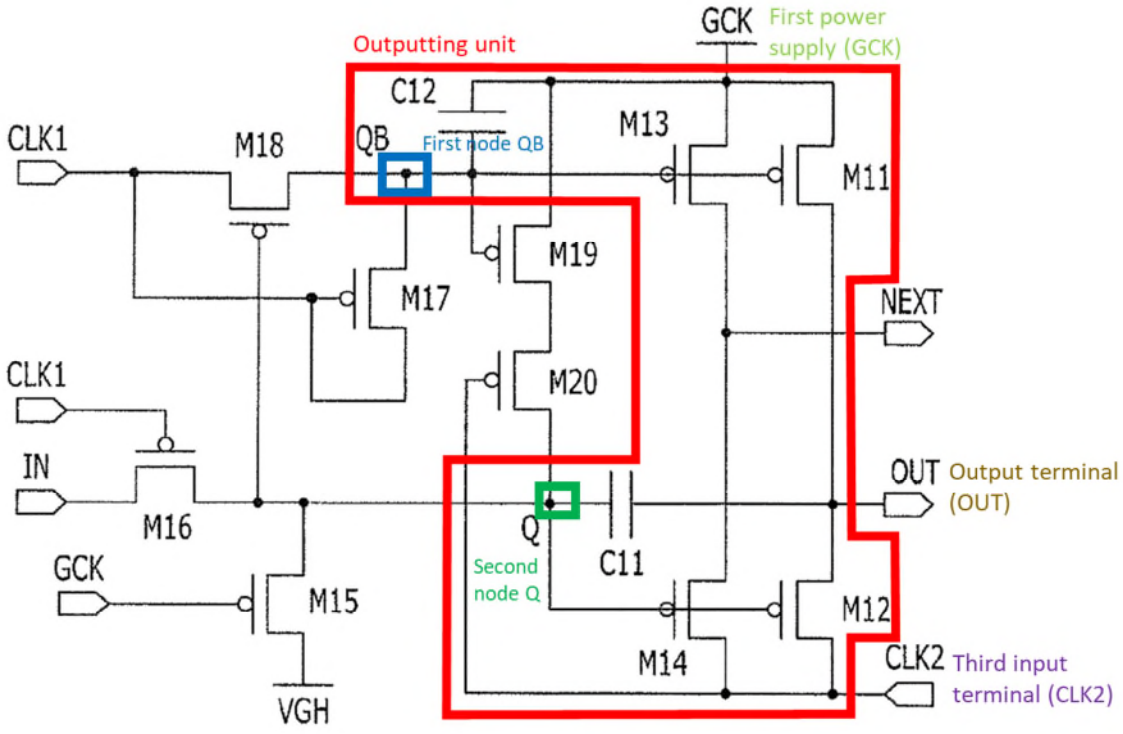
128. Further, the duration of the actual scan operations is the only time period that the ’593 patent addresses. This is revealed through the timing diagram in Figure 4 of the ’593 patent and its associated descriptions. Although Figure 4 shows two horizontal periods before the period in which the start signal SSP becomes active, the associated description detailing the timing diagram begins “during a third horizontal period [in which] the start signal SSP is supplied.” (’593 patent at 6:41-53.) This third horizontal period and subsequent periods parallel the periods at t13 and later in Figure 5 of Chung, i.e., the duration of the actual scan operations:



’593 patent, Fig. 4, Chung, Fig. 5.

i. [1-a-1]: “an outputting unit having a first node and a second node,”

129. Chung discloses this claim sub-element; this is evident via an annotated version of Figure 4 of Chung:

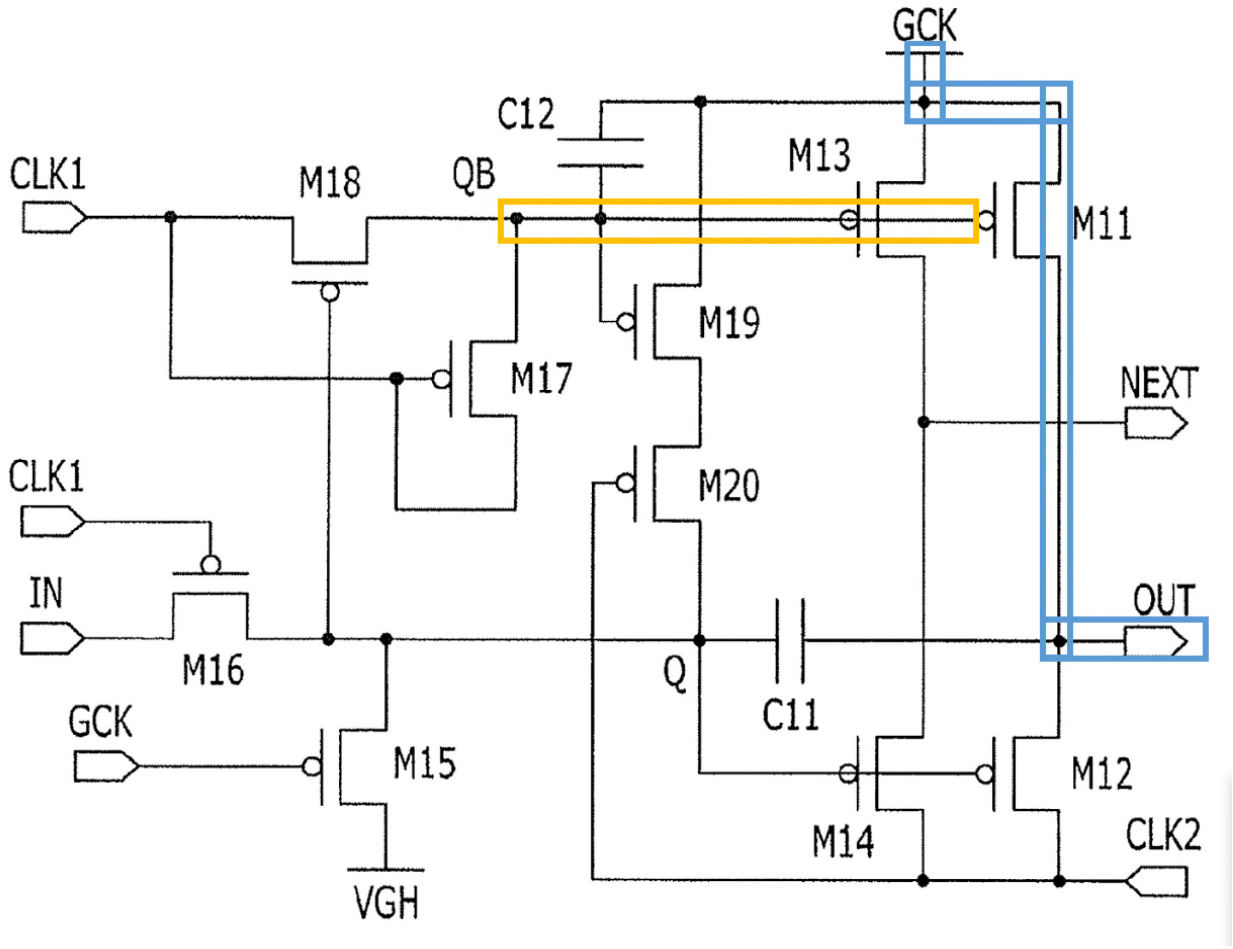


(Annotations added.) The node labeled "QB" is the first node, and the node labeled "Q" is the second node – while the "outputting unit" is a shown via the annotation box-bounding in red.

130. Thus, Chung discloses this claim sub-element of this claim element of Claim 1 of the '593 patent.

ii. [1-a-2]: "the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node"

131. Chung discloses this claim sub-element; this is evident via an annotated version of Figure 4 of Chung:

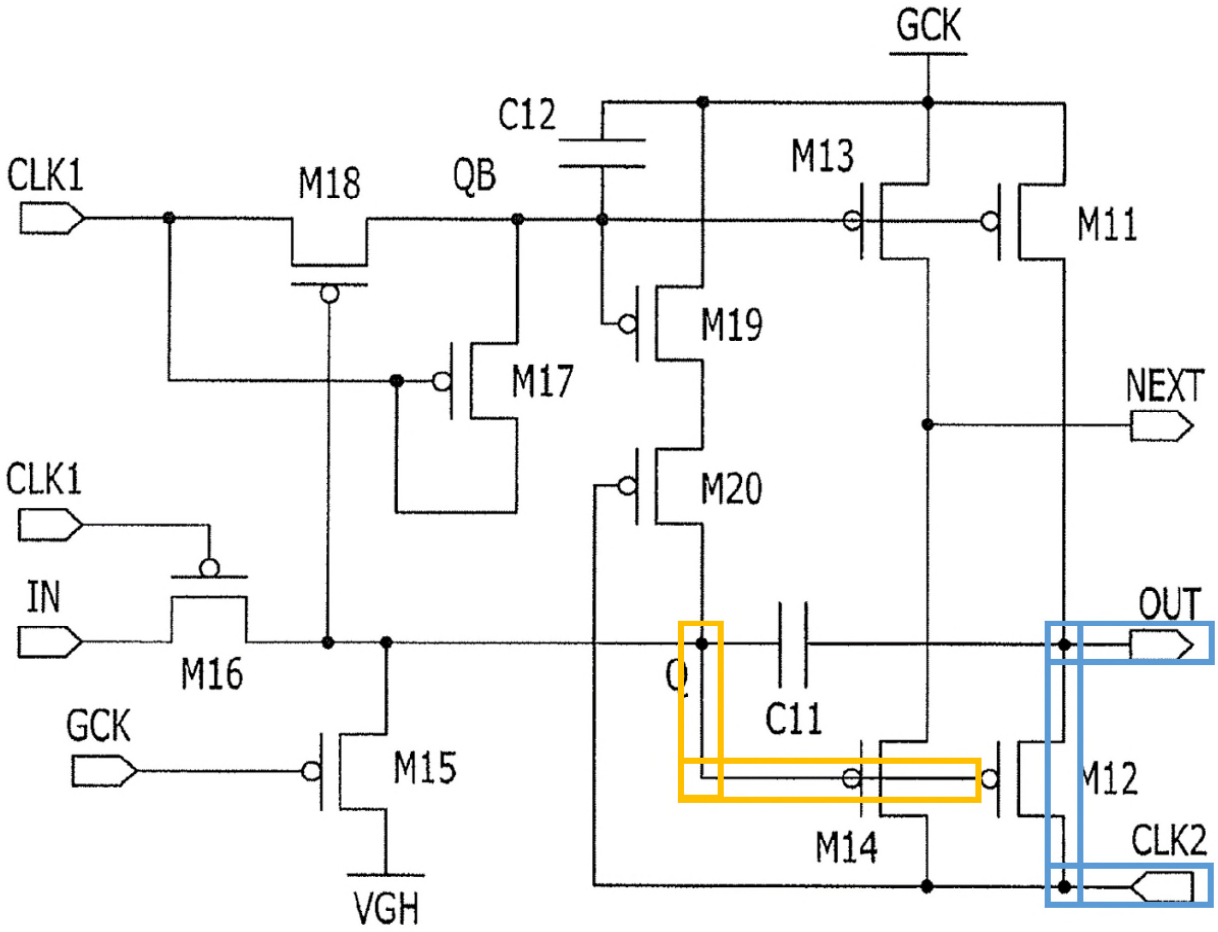


(Annotations added.) As the annotations show, when an appropriate (i.e., turn-on) voltage is applied at the first node (the node labeled "QB"), transistor M11 will turn on; this will connect the first power supply voltage at GCK to the node of the output terminal ("OUT") – and thus the voltage of the first power supply connection (GCK) is supplied to the output terminal ("OUT"). (On the other hand, when a turn-on voltage is not applied at the first node ("QB"), transistor M11 will not turn on – and the voltage of the first power supply connection (GCK) is not supplied to the output terminal.)

132. Thus, Chung discloses this claim sub-element of this claim element of Claim 1 of the '593 patent.

iii. [1-a-3]: "and a signal of the third input terminal to the output terminal according to a voltage applied to the second node:"

133. Chung discloses this claim sub-element; this is evident via an annotated version of Figure 4 of Chung:



As the annotations show, when an appropriate (i.e., turn-on) voltage is applied at the second node (the node labeled "Q"), transistor M12 will turn on; this will connect

the signal of the third input terminal ("CLK2") to the node of the output terminal ("OUT") – and thus the signal of the third input terminal (CLK2) is supplied to the output terminal ("OUT"). (On the other hand, when a turn-on voltage is not applied at the second node ("Q"), transistor M12 will not turn on – and thus the signal of the third input terminal (CLK2) in not supplied to the output terminal ("OUT").)

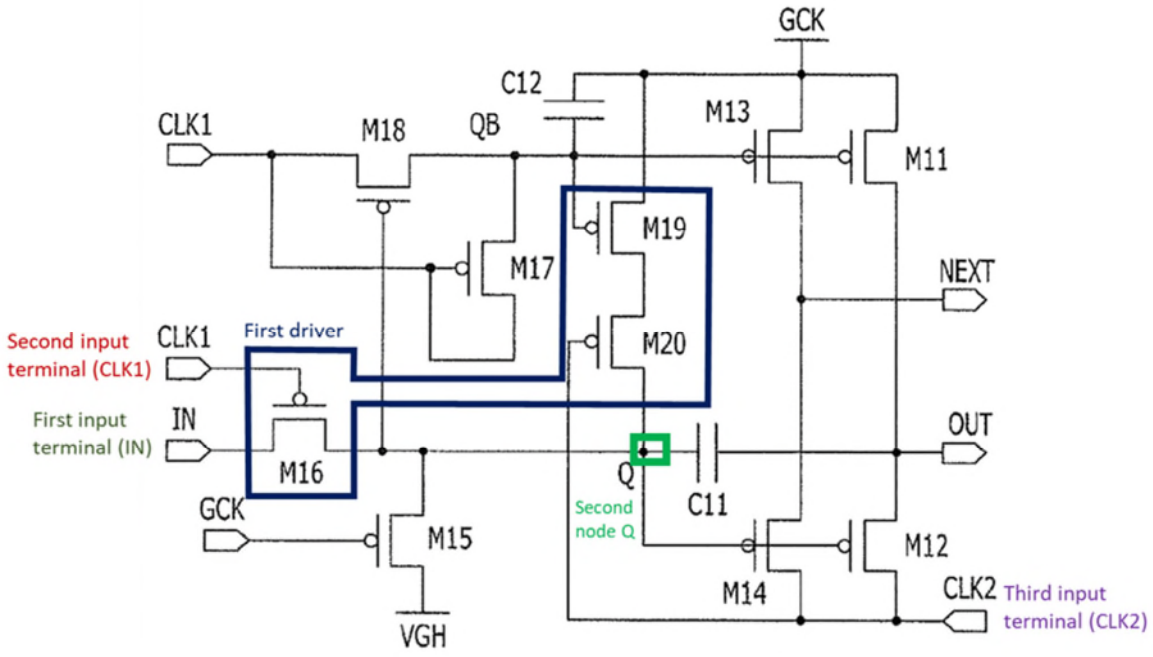
134. Thus, Chung discloses this claim sub-element of this claim element of Claim 1 of the '593 patent.

iv. Claim Element [1-a] Summary

135. As just demonstrated, Chung discloses claim sub-elements [1-a-1], [1-a-2], and [1-a-3] of the '593 patent; thus, Chung discloses claim element [1-a] of Claim 1 of the '593 patent.

c. *[1-b]: "a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal; and"*

136. Chung discloses this claim element of the '593 patent; this is evident via an annotated version of Figure 4 of Chung:

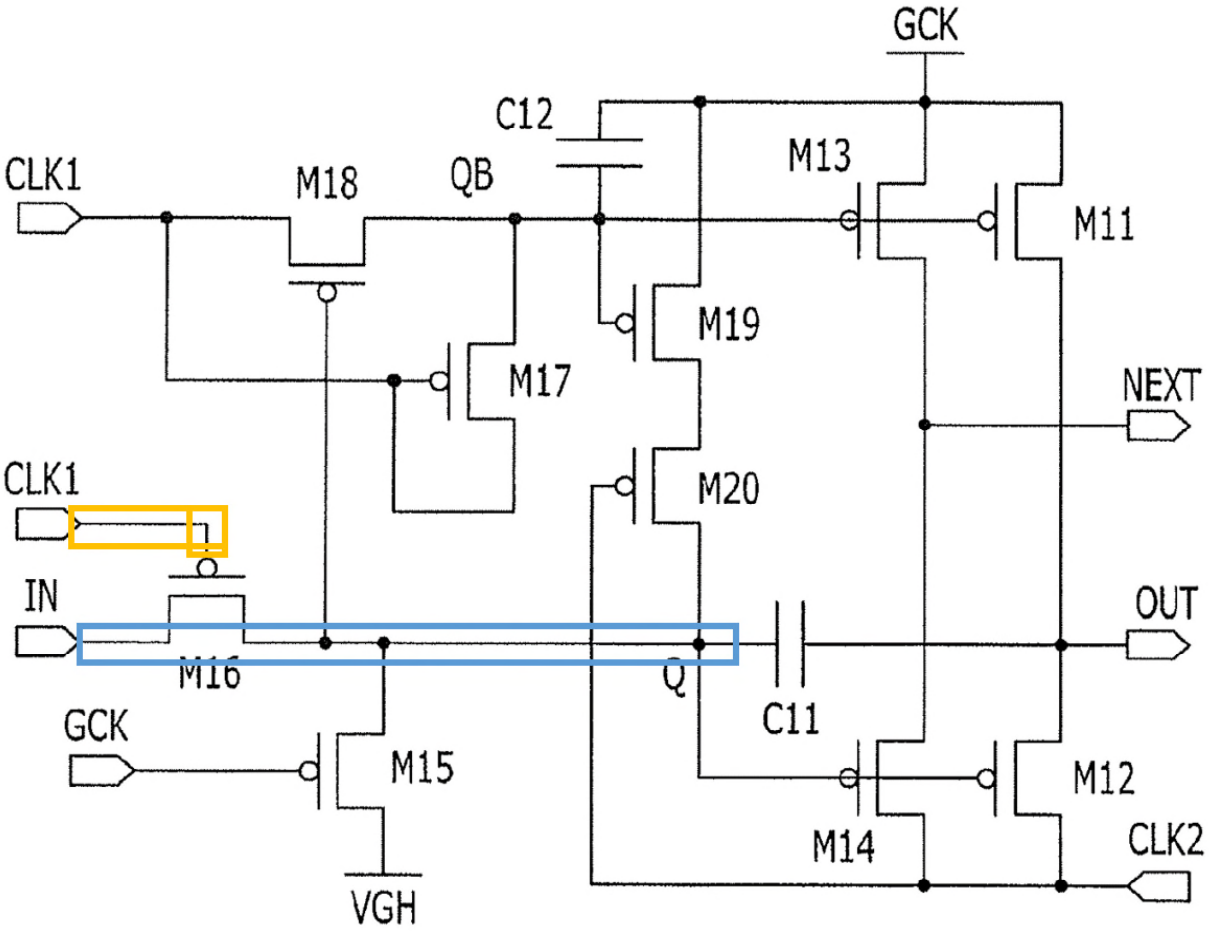


(Annotations added.)

137. In the Chung figure above, the "first driver" is identified using navy blue box-bounding.

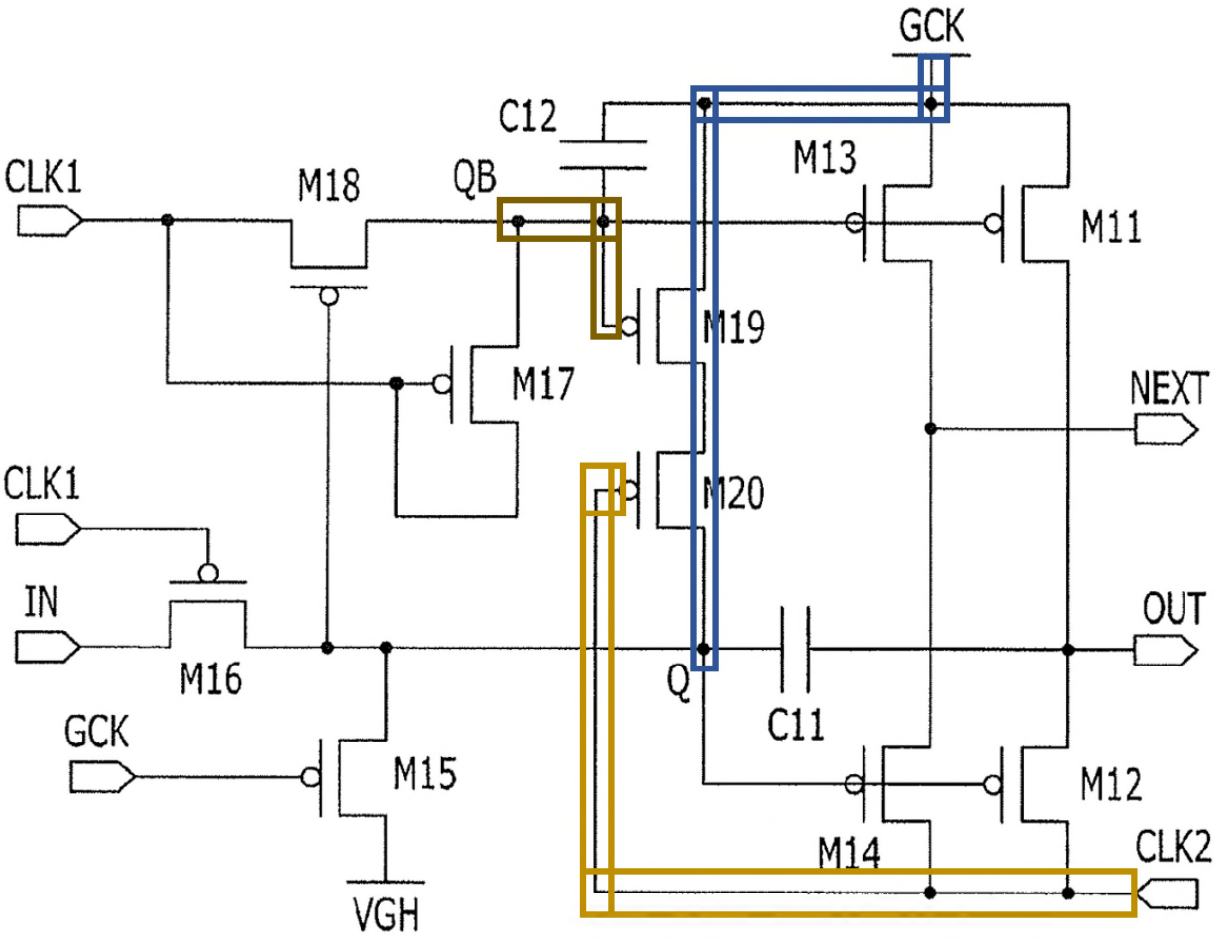
138. The voltage on the second node ("Q") is controlled in accordance with the signals of the first input terminal, the second input terminal, and the third input terminal – as shown by the annotations to the following versions of Figure 4 of Chung. As these annotations show, this functionality is implemented in two separate ways.

139. The first way is implemented as described here.



(Annotations added.) The first way occurs when the second input signal (at CLK1) is pulled to a voltage that causes transistor M16 to turn on; when this is done, the content of the input signal at the first input terminal (IN) is supplied to the second node (Q). (On the other hand, when transistor M16 is not turned on, the content of the input signal at the first input terminal (IN) is not supplied to the second node (Q).)

140. The second way will now be described.



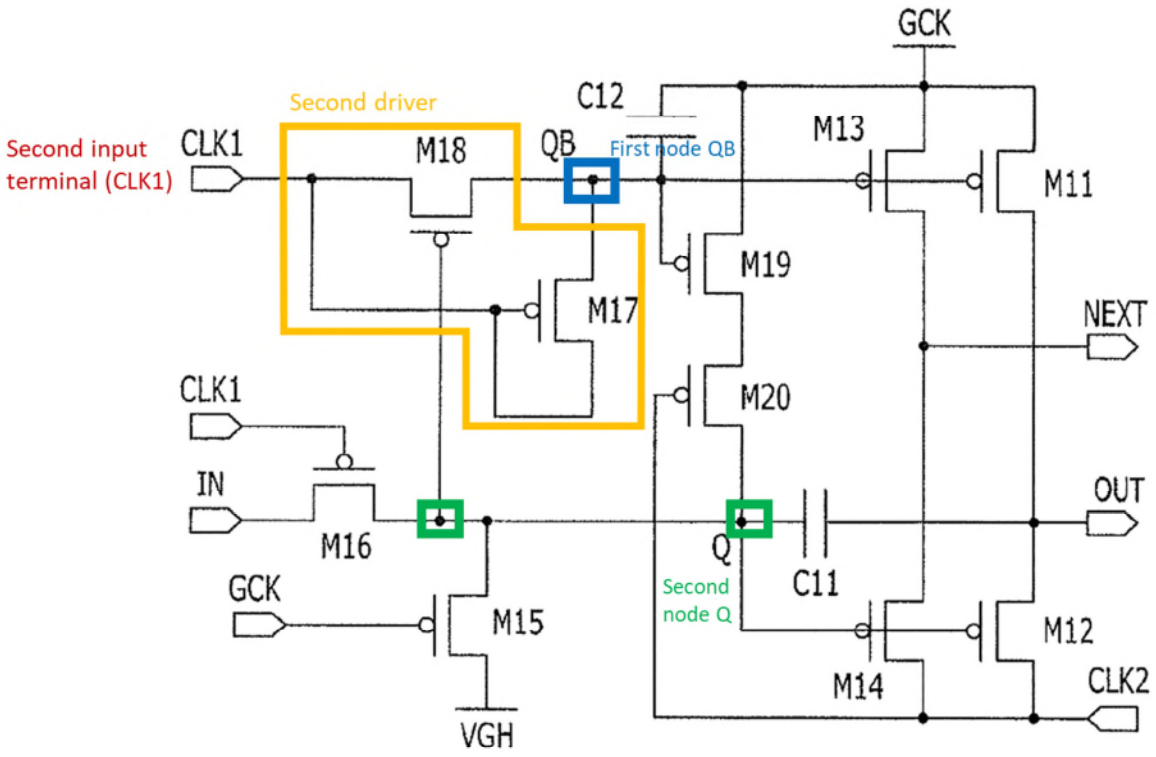
The second way occurs when the third input signal (CLK2) is pulled to a voltage that causes transistor M20 to turn on; when this is done, the specific outcome at the second node (Q) will depend on the state of transistor M19 – the gate of which is controlled by the voltage on the first node (QB).[10] (On the other hand, when transistor M20 is not turned on, this functionality will not occur.)

[10] Transistor M15 is always turned off during actual scan periods - as during these periods, the first power supply GCK is always high. Thus, transistor M15 has no effect on the scan operation.

141. Thus, Chung discloses this claim element of Claim 1 of the '593 patent.

d. [1-c]: "a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, wherein"

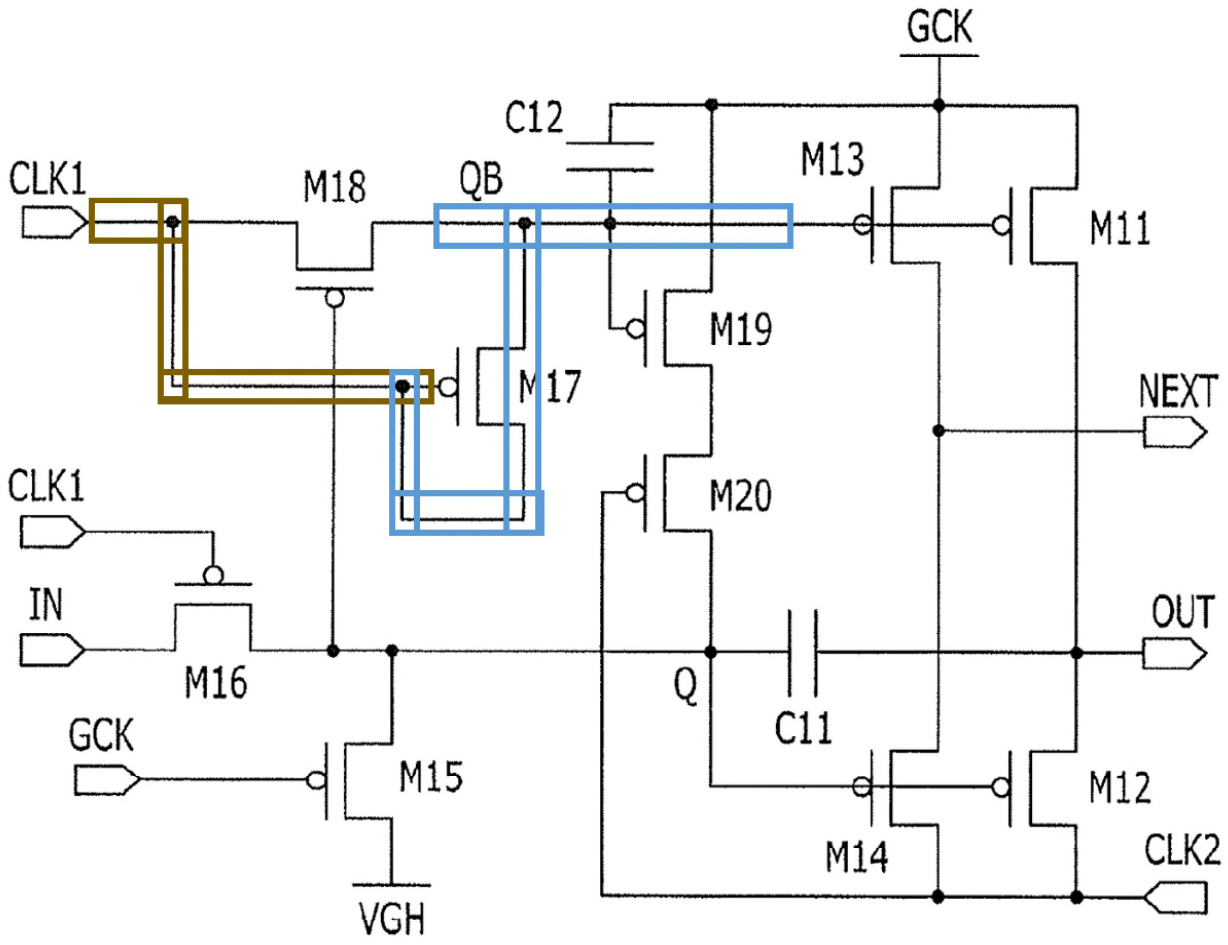
142. Chung discloses this claim element of the '593 patent; this is evident via an annotated version of Figure 4 of Chung:



(Annotations added.)

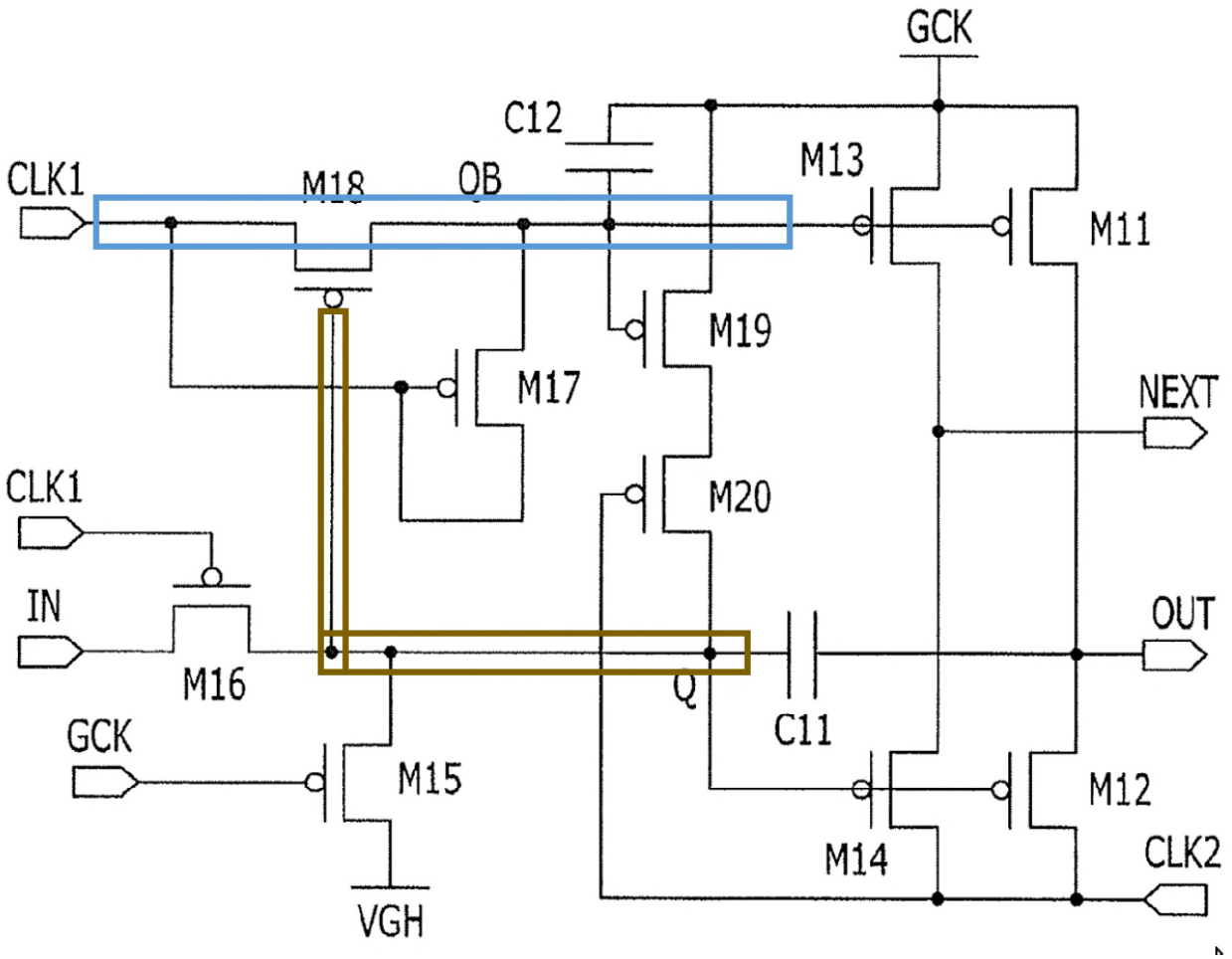
143. In the Chung figure above, the "second driver" is identified using orange box-bounding.

144. The voltage on the first node ("QB") is controlled in accordance with the signal of the second input terminal and the voltage of the second node ("Q") – as shown by the following annotated versions of Figure 4 of Chung.



145. First, when the signal on the second input terminal (CLK1) is pulled low, this will turn on transistor M17; as this transistor is connected in the diode-connected configuration (which was described in Section VII.A.3), the signal on the second input terminal will be transferred to the first node (QB) – which will thus take on the signal's low voltage value. (When the signal on the second input terminal

(CLK1) is pulled high, transistor M17 is turned off – and this functionality is not available).

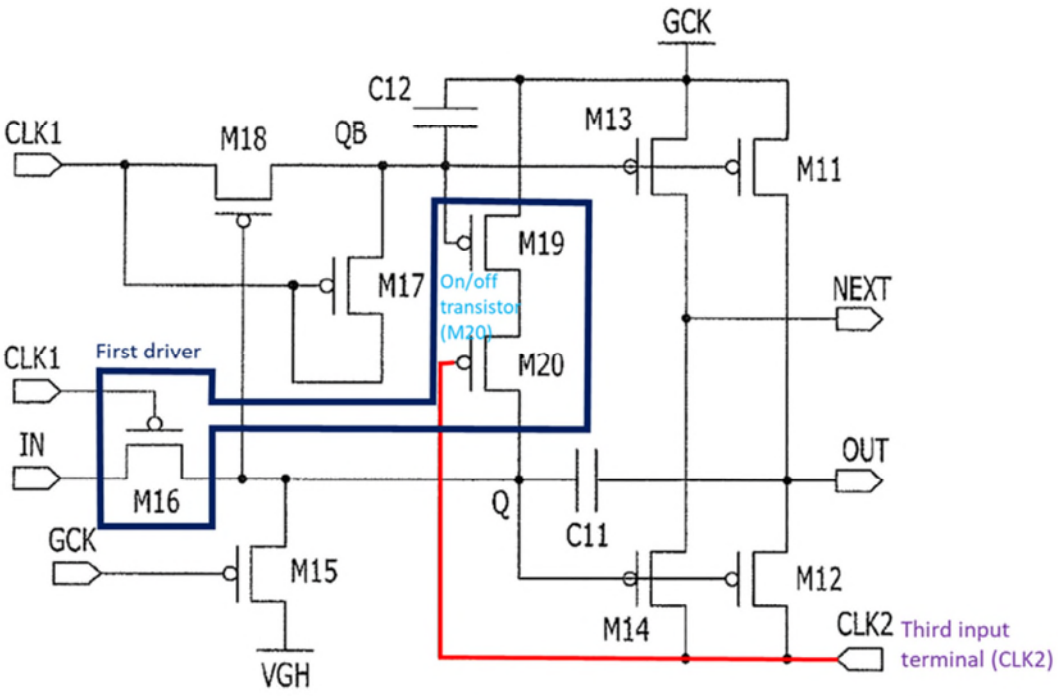


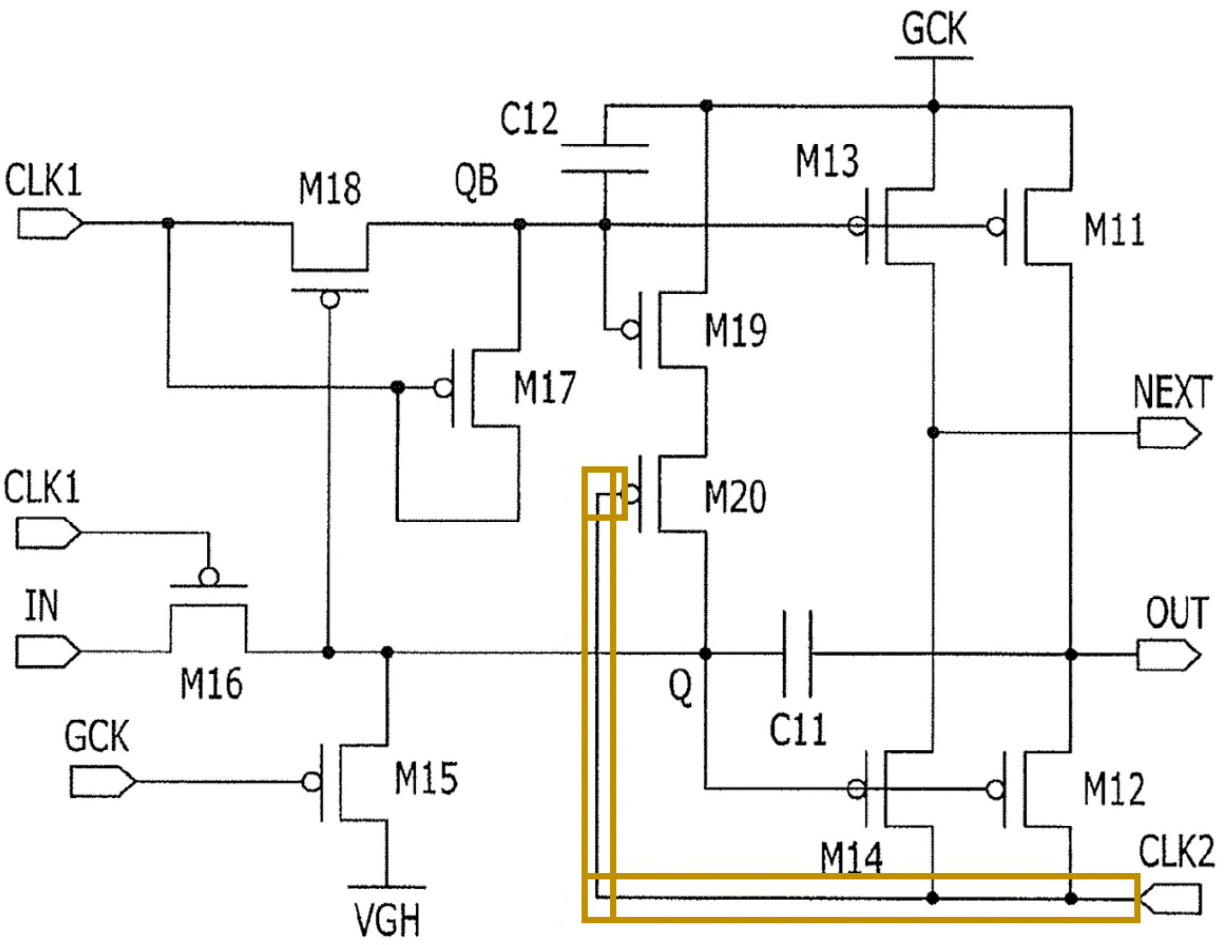
146. Second, when the second node (Q) has a low voltage value, the transistor M18 will be turned on; this will transfer the signal on the second input terminal (CLK1) to the first node (QB). (When the second node (Q) has a high voltage value, transistor M18 will be turned off – and this functionality will not be available).

147. Thus, Chung discloses this claim element of Claim 1 of the '593 patent.

e. [1-d]: "the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver."

148. Chung discloses this claim element of the '593 patent; this is evident via two annotated versions of Figure 4 of Chung:





(Annotations added.) As the annotations show, the third input signal ("CLK2") is (among other things) connected directly to the gate of transistor M20, which is part of the first driver; thus, the third input signal directly controls the on/off operation of a transistor that is included in the first driver.

149. Thus, Chung discloses this claim element of Claim 1 of the '593 patent.

f. Claim 1 Summary

150. As just shown, Chung discloses each element of Claim 1 of the '593 patent; thus, Chung anticipates Claim 1 of the '593 patent.

2. Dependent Claim 2

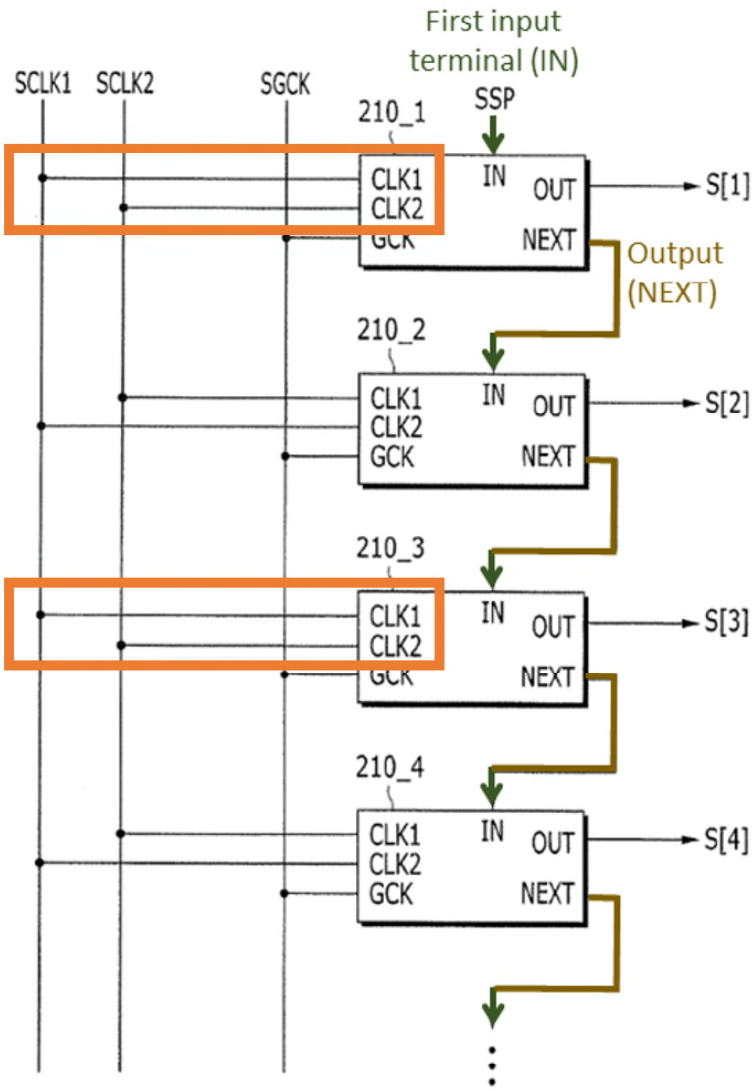
151. As an initial matter, Claim 2 depends from Claim 1; as was shown above, Claim 1 of the '593 patent is disclosed by Chung.

152. Claim 2 further requires that "wherein the first input terminal receives an output signal of a previous stage circuit or a start signal, wherein the second input terminal receives a first clock signal, and wherein the third input terminal receives a second clock signal." Chung discloses this claim of the '593 patent.

153. Preliminarily, I note that Claim 2 recites "an output signal" without reciting any relationship of this signal to the "output terminal" of Claim 1.

154. It was shown above (in Section XII.A.1.a) that the first input terminal can receive a start signal (SSP), the second input terminal receives a first clock signal, and the third input terminal receives a second clock signal. Claim 2 adds that the first input terminal can also receive an output signal of a previous stage circuit; this is disclosed in Chung – as an annotated version of Figure 3 from Chung makes clear.

FIG. 3



(Annotations added.) As can be seen from examination of this annotated figure, the first stage circuit block (210_1) receives a start signal (SSP) at its first input terminal, while subsequent stage circuit blocks (210_2, 210_3, 210_4…) receive an output signal of a previous stage circuit block at the first input terminal. The output signal comes from the terminal NEXT. Note in particular that the third stage circuit block

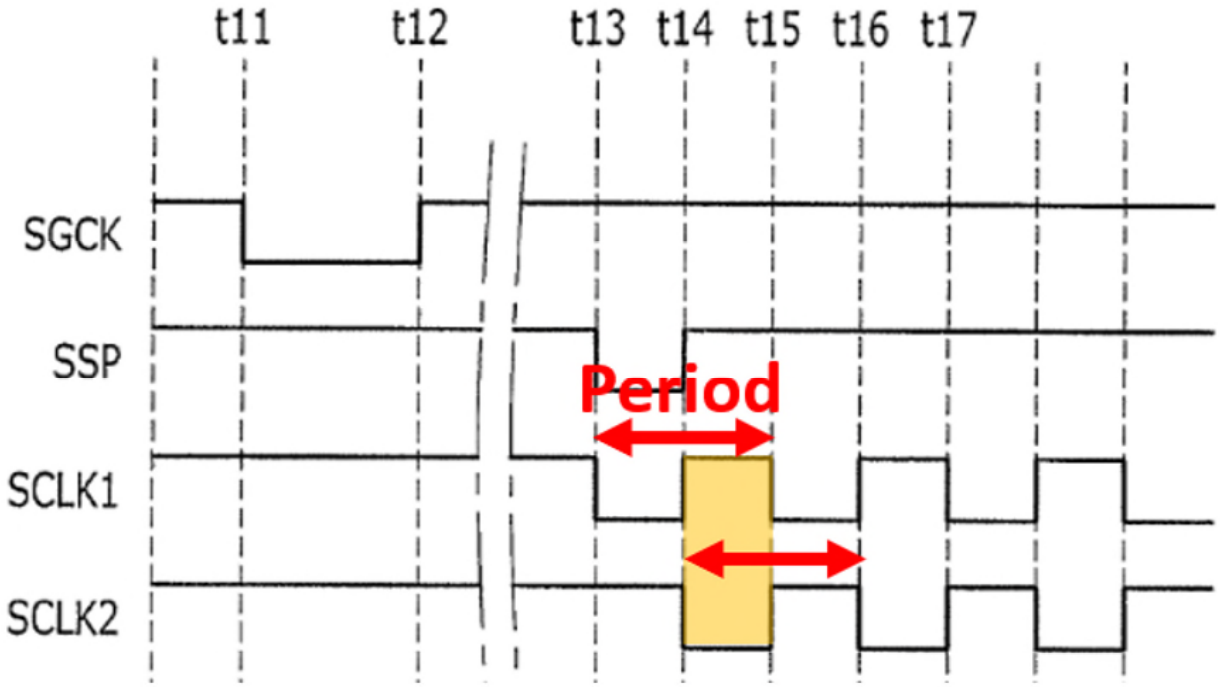
(210_3), like the first stage circuit block (210_1), is configured so that the second input terminal (CLK1) receives a first clock signal (SCLK1) and the third input terminal (CLK2) receives a second clock signal (SCLK2).

155. Thus, Chung anticipates Claim 2 of the '593 patent.

3. Dependent Claim 3

156. As an initial matter, Claim 3 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the '593 patent are disclosed by Chung.

157. Claim 3 further requires that "wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap." Chung discloses this claim of the '593 patent – as is evident from examination of an annotated version of Figure 5 from Chung.



(Annotations added.) It is well-known in the art that the "period" of a recurring waveform is defined as the amount of time that passes before the waveform repeats itself; the annotations added to Figure 5 of Chung identify the period of the first clock signal (SCLK1) and the period of the second clock signal (SLCK2). As is evident from inspection of this figure, the period of the first clock signal (SCLK1) and the second clock signal (SCLK2) are the same.

158. Claim 3 also requires that the two clock signal waveforms "have phases that do not overlap." At a minimum, it is well-known in the art that the term "phase" (with regard to a recurring waveform) is used to describe specifically when (in time) the waveform reaches some identified point along its single-period form; this is of particular importance when referring to how a particular recurring waveform might

be shifted in time ("changing the phase"), or (more commonly and more importantly) when two otherwise-identical recurring waveforms are offset from each other (in time). When two otherwise-identical recurring waveforms are offset from each other (in time), it is said that the two waveforms are "out of phase" (to contrast from *not* being offset in time, where they would be "in phase") – and the specific amount of the offset difference between the two waveforms is known as the "phase difference." As examination of Figure 5 of Chung clearly shows that the first clock signal (SCLK1) and the second clock signal (SCLK2) are out of phase with each other – and thus, their phases do not overlap.

159. Further, note that these two signals are digital waveforms – that is, they are square waves that have only one of two signal states – high or low. With digital waveforms, the term "phases that do not overlap" is known in the art as meaning that the two waveforms will not both be in their turn-on state, e.g., logic low and high for pMOS and nMOS circuits, respectively, at the same time.

160. Thus, Chung anticipates Claim 3 of the '593 patent.

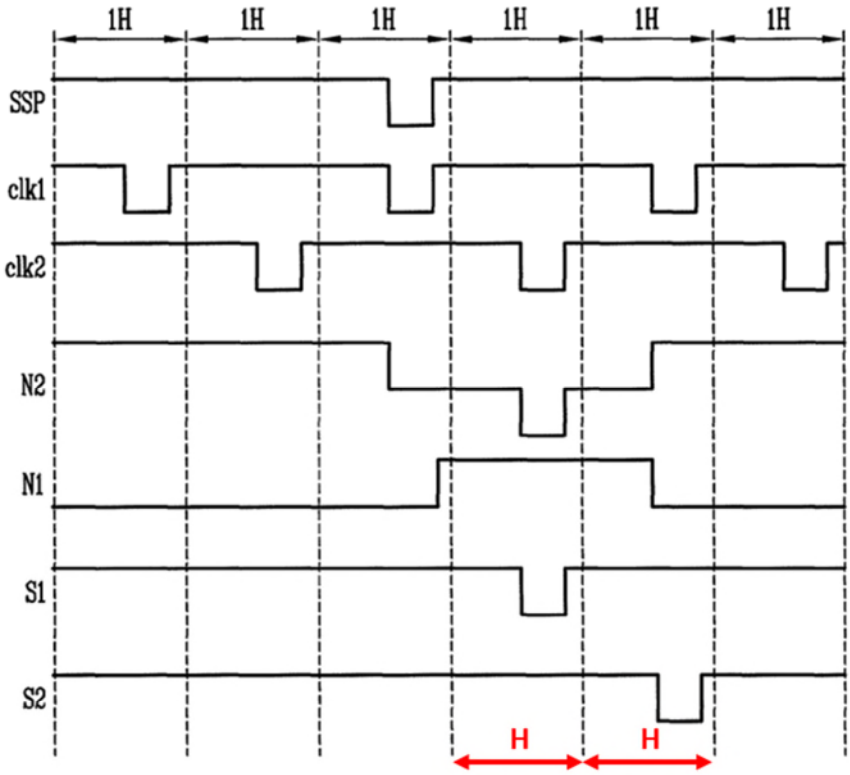
4. Dependent Claim 4

161. As an initial matter, Claim 4 depends from Claim 3, which depends from Claim 2, which depends from Claim 1; as was shown above, Claim 1, Claim 2, and Claim 3 of the '593 patent are disclosed by Chung.

162. Claim 4 further requires "wherein the first clock signal and the second clock signal have a period equal to two horizontal periods 2H and are supplied in different horizontal periods as low signals." The language in this claim may be somewhat confusing – as the word "period" appears three times but the word clearly carries two different meanings depending on the usage.

163. The first instance of "period" is described via "the first clock signal and the second clock signal have a period"; this "period" is of the form described above with respect to Claim 3, in which "period" refers to the amount it takes for a recurring waveform to repeat itself.

164. The second instance of "period" occurs twice later in the claim, and refers (in both usages) to "horizontal periods"; this "period" refers to a particular amount of time (as in "a period of time"), and not to the repetition of a recurring waveform. More specifically, the '593 patent refers to "a period in which a scan signal is supplied to one scan line" as an exemplary horizontal period. ('593 patent, 5:18-20.) This period corresponds to the time span between outputs of successive stages, e.g., between S1 and S2, as shown in an annotated version of '593 patent Figure 4:

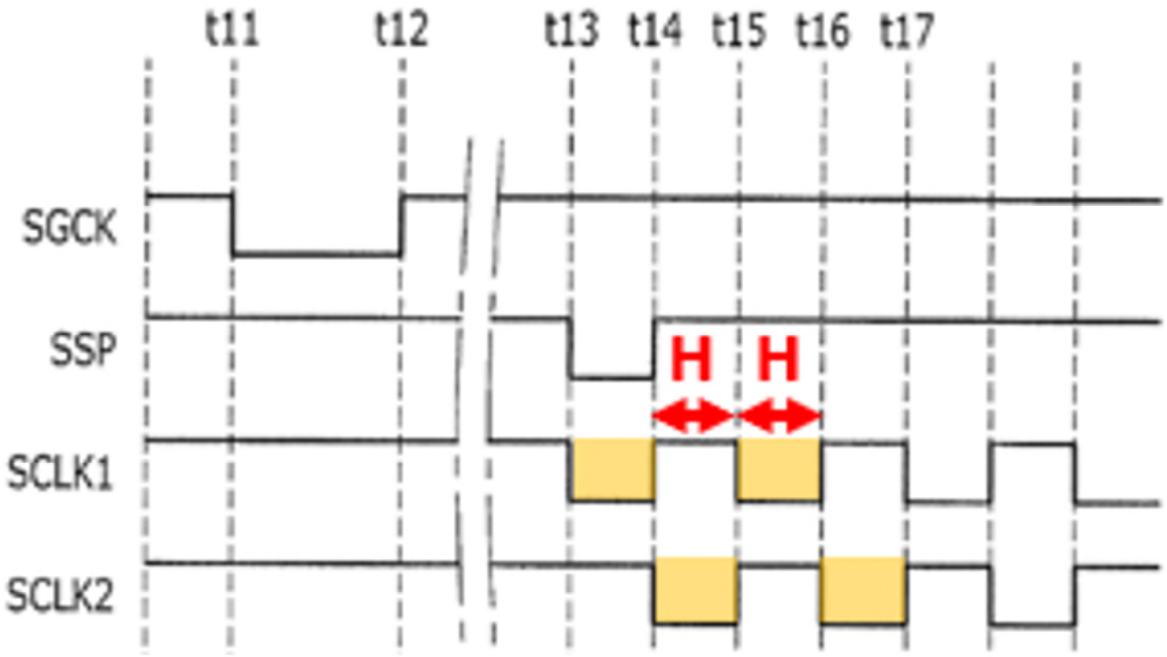


165. Thus, the claim basically states that the amount of time of the period of the recurring waveforms (the first clock signal and the second clock signal) is twice as long as two sub-periods ("H") that, in sum, are the length (in time) of the time it takes for the recurring waveform to repeat itself. Further, the claim states that these sub-periods sum to "2H" – which means that each sub-period has a duration of H, so that the duration of the two sub-periods is the same.

166. The final stipulation of Claim 4 is that the first clock signal and the second clock signal are "supplied in different horizontal periods as low signals." As the '593 patent uses pMOS transistors in its circuitry, low signals will be the turn-on voltage level for the transistors used in the circuitry in the '593 patent. So, essentially, this requirement is the same as the one discussed above with respect to

Claim 3 and "phases that do not overlap." As Chung also uses pMOS transistors in its circuitry, the same condition (low signals are transistor turn-on signals) is disclosed in Chung.

167. That Chung discloses this claim element of the '593 patent can readily be seen via an annotated version of Figure 5 of Chung.



The first clock signal (SCLK1) and the second clock signal (SCLK2) have two sub-periods of equal duration H – so that the total period of the recurring waveforms of SCLK1 and SCLK2) is 2H. Further, the first clock signal (SCLK1) is high when the second clock signal (SCLK2) is low, and vice versa. Thus, the first clock signal and the second clock signal are supplied in different horizontal periods as low signals.

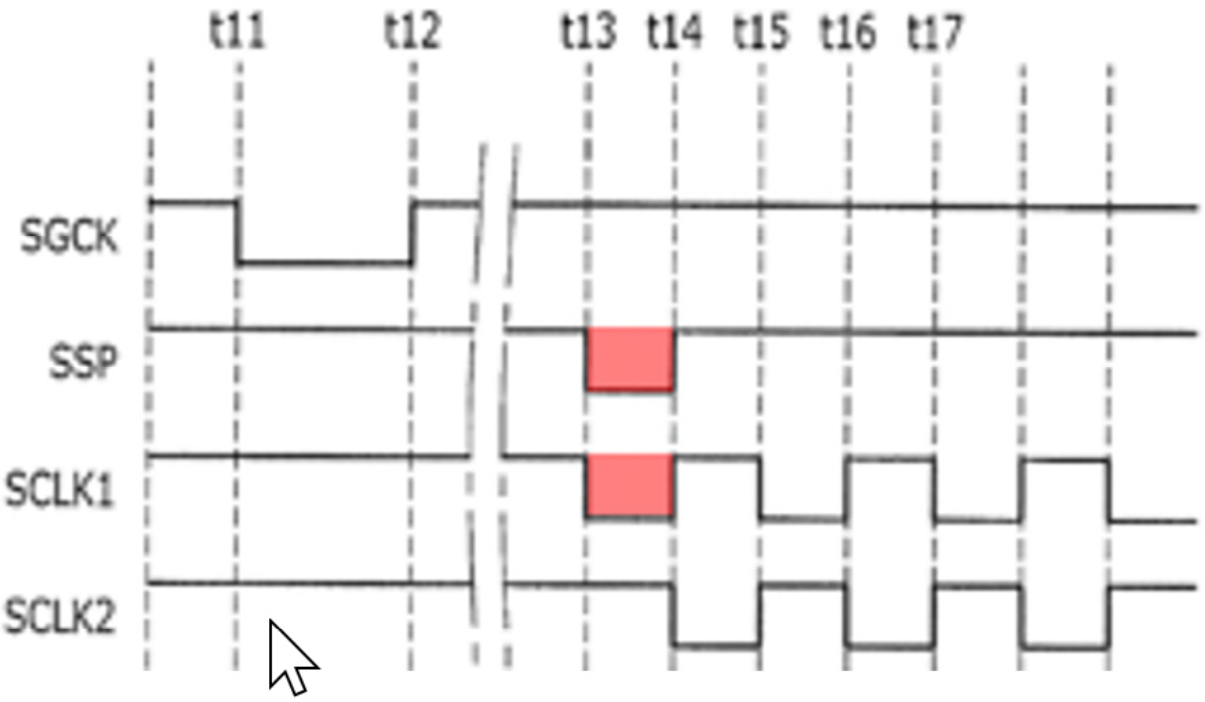
168. Thus, Chung anticipates this claim of the '593 patent.

5. Dependent Claim 5

169. As an initial matter, Claim 5 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the '593 patent are disclosed by Chung.

170. Claim 5 further requires that "the start signal is supplied to overlap the first clock signal."

171. This can be readily seen via an annotated version of Figure 5 of Chung.



As can be seen, the start signal (SSP) goes low (its "active" level) at the same time and for the same duration that the first clock signal (SCLK1) goes low (also its

"active" level) as part of its recurring square wave behavior. Thus, the start signal (SSP) overlaps the first clock signal (SCLK1).[11]

172. Thus, Chung anticipates this claim of the '593 patent.

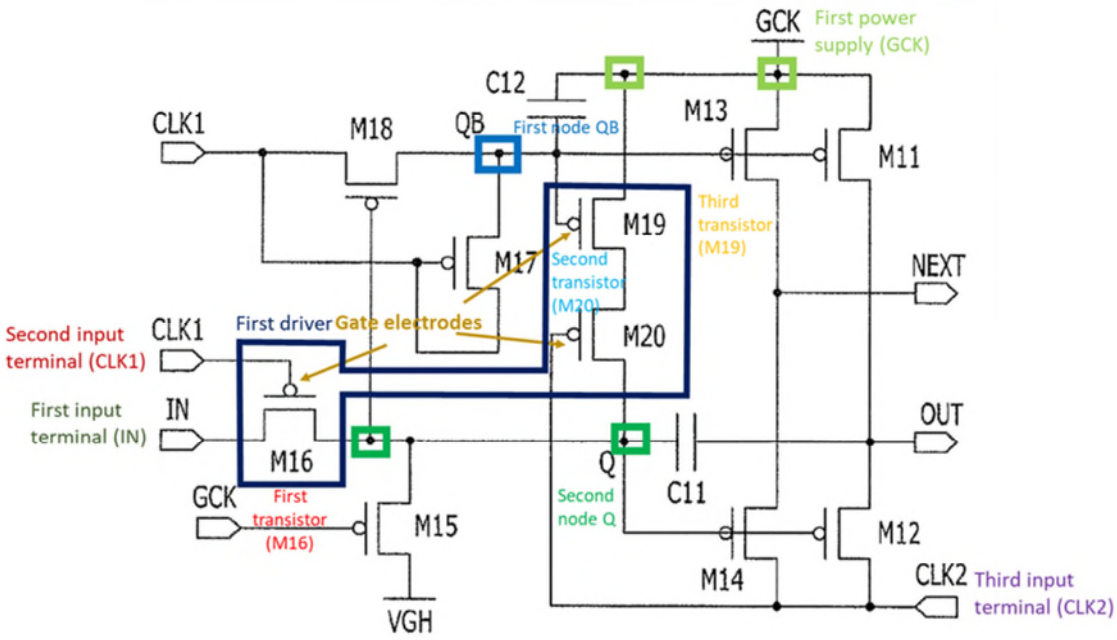
6. Dependent Claim 6

173. As an initial matter, Claim 6 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the '593 patent are disclosed by Chung.

174. Claim 6 further requires that "the first driver includes: a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and a second transistor and a third transistor serially positioned between the second node and the first power supply, wherein a gate electrode of the second transistor is coupled to the third input terminal, and wherein a gate electrode of the third transistor is coupled to the first node." This is a verbal form of a topological description of circuitry – which describes the components of the described circuitry, the terminals of those components, and the way that the various terminals of the various components are connected together.

[11] This is a sufficient but not necessary way for two digital waveforms to "overlap."

175. How this topological description reads on Chung is best-described via an annotated version of Figure 4 of Chung.



(Annotations added.) As the annotations show, the description of the circuit topology in the claim is found, element for element, in Chung.

176. Thus, Chung anticipates this claim of the '593 patent.

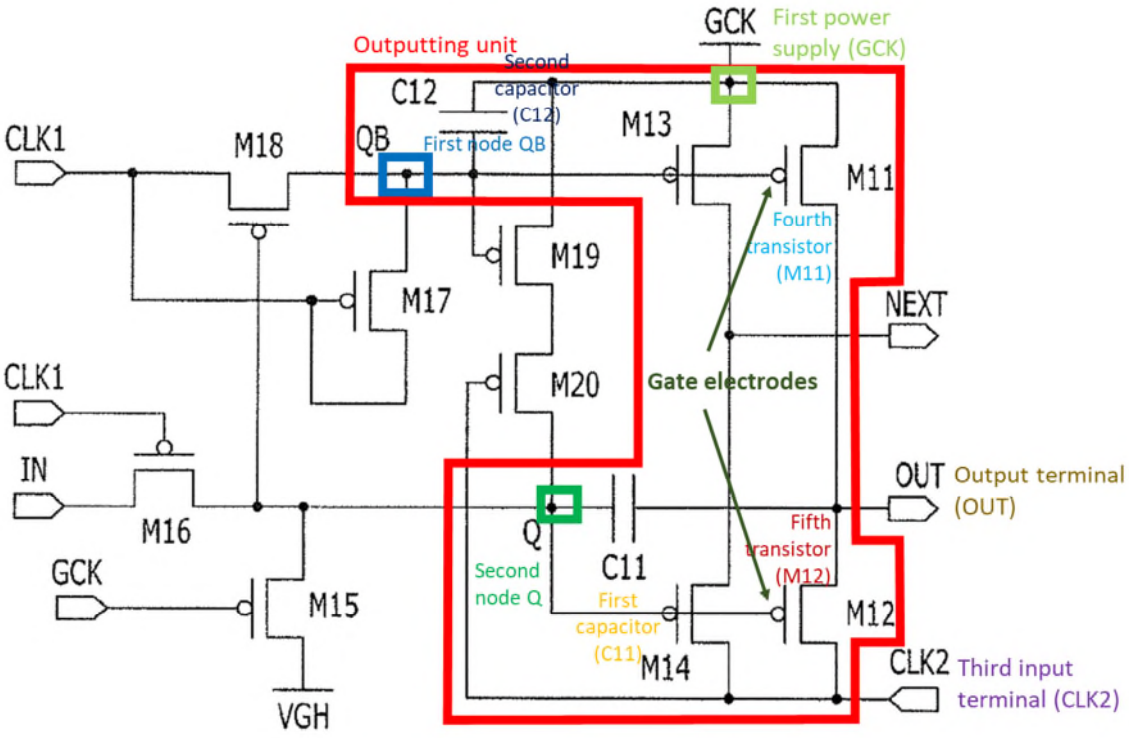
7. Dependent Claim 7

177. As an initial matter, Claim 7 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the '593 patent are disclosed by Chung.

178. Claim 7 further requires that "the outputting unit includes: a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node: a fifth transistor between

the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node, a first capacitor between the second node and the output terminal; and a second capacitor between the first node and the first power supply."

179. As in Claim 6, this is a verbal form of a topological description of circuitry – and as in Claim 6, how this topological description reads on Chung is best described via an annotated version of Figure 4 of Chung.



(Annotations added.) As the annotations show, the description of the circuit topology in the claim is found, element for element, in Chung.

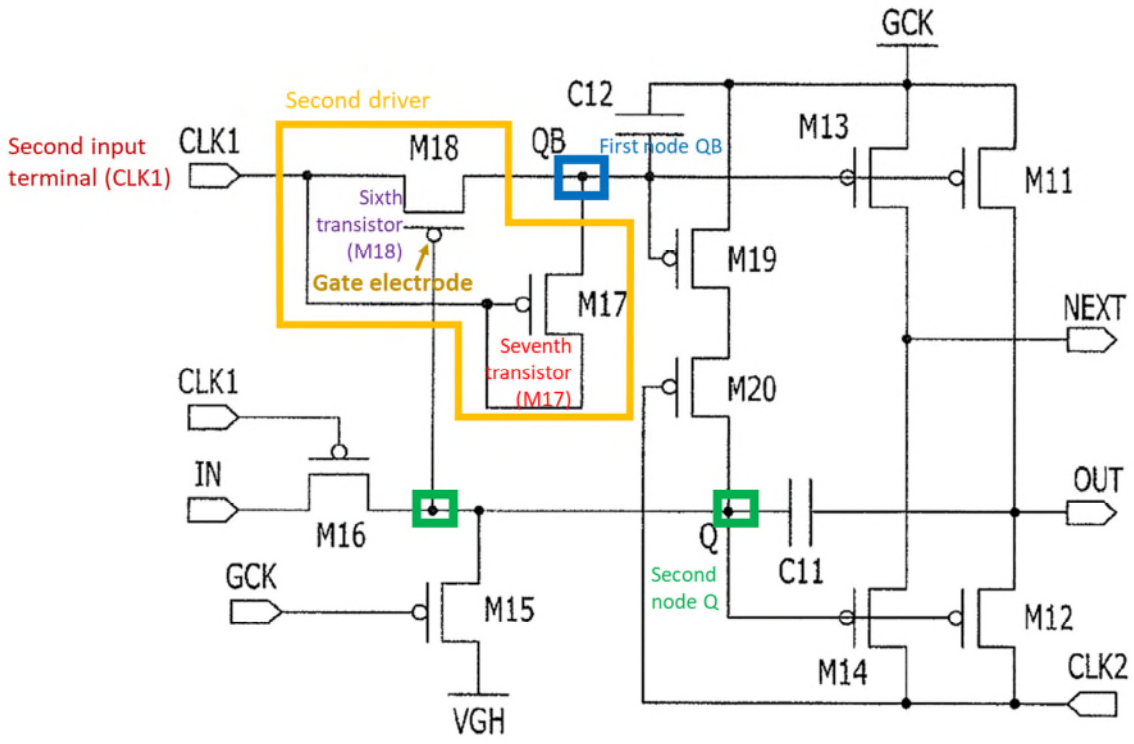
180. Thus, Chung anticipates this claim of the '593 patent.

8. Dependent Claim 9

181. As an initial matter, Claim 9 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the '593 patent are disclosed by Chung.

182. Claim 9 further requires that "the second driver includes: a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and a seventh transistor between the first node and the second input terminal, the seventh transistor being diode connected."

183. Once again, this is a verbal form of a topological description of circuitry – and once again, how this topological description reads on Chung is best-described via an annotated version of Figure 4 of Chung.



(Annotations added.) As the annotations show, the description of the circuit topology in the claim is found, element for element, in Chung.

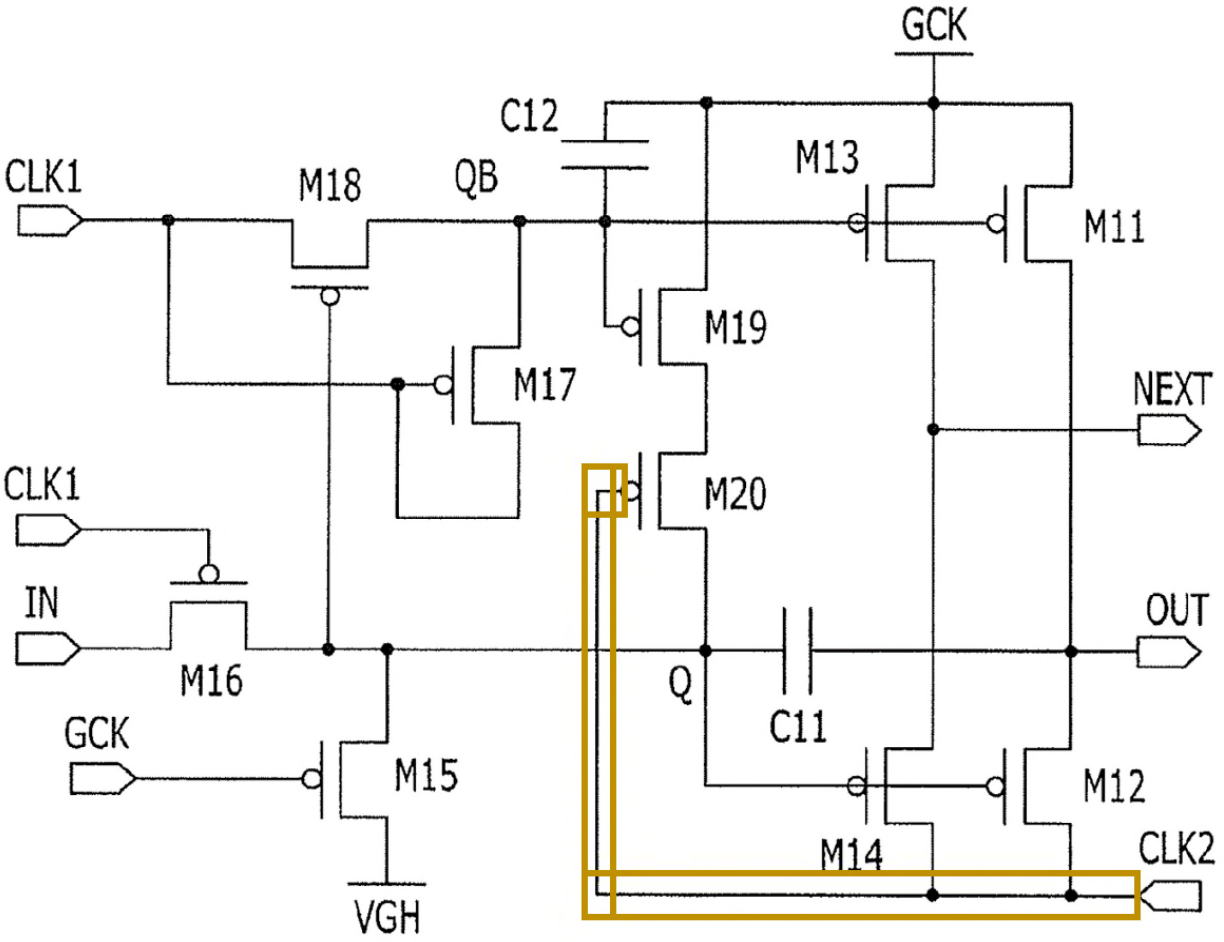
184. Thus, Chung anticipates this claim of the '593 patent.

9. Dependent Claim 14

185. As an initial matter, Claim 14 depends from Claim 1; as was shown above, Claim 1 of the '593 patent is disclosed by Chung.

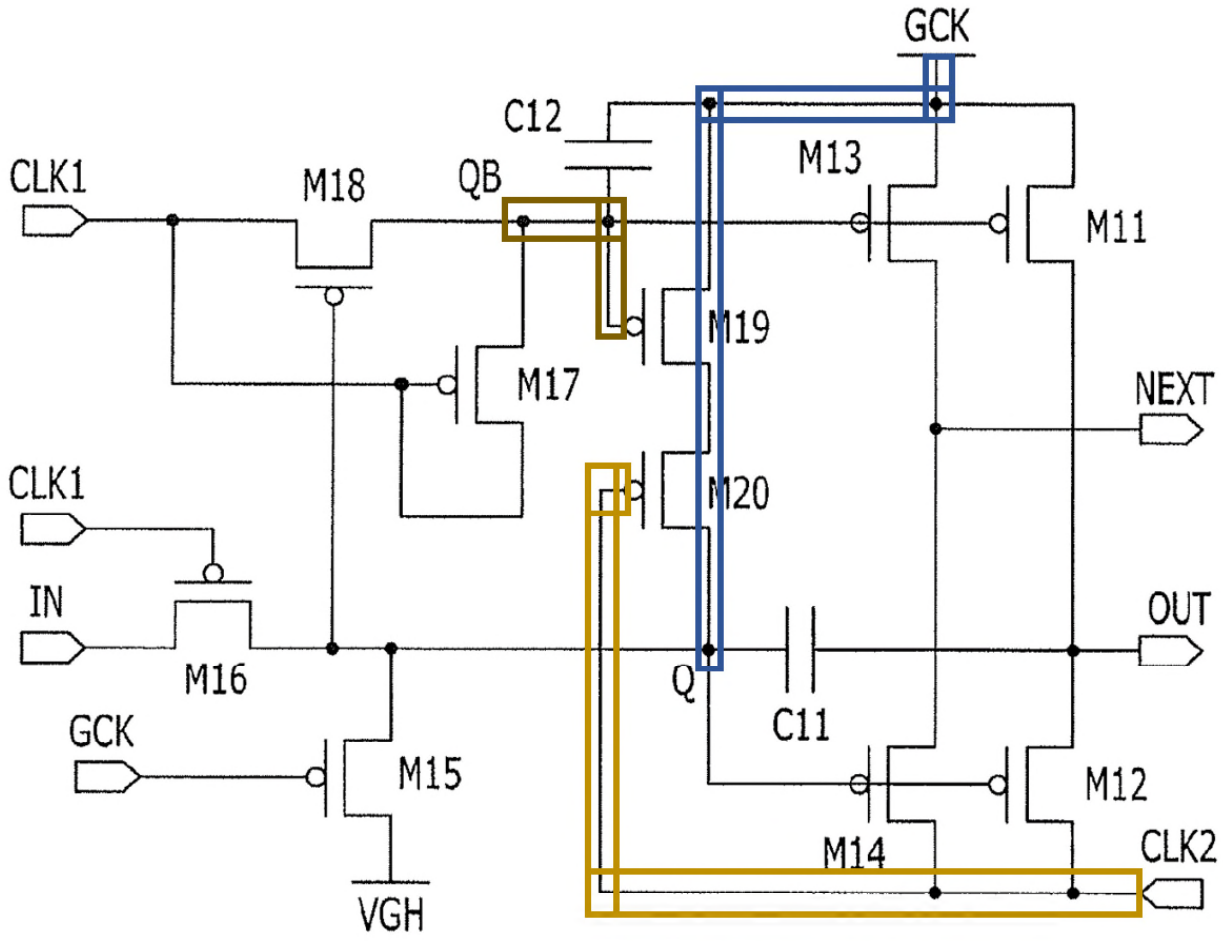
186. Claim 14 further requires that "the transistor controls the voltage of the second node according to the on/off operation thereof." Claim 14 does not provide details regarding which transistor is "the" transistor being described here; however, Claim 1 makes reference to only one transistor – in claim element [1-d] (which was described in Section XII.A.1.e), where this transistor was identified in the claim

element via "the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver." In Section XII.A.1.e, that transistor was specifically identified as transistor M20, via an annotated version of Figure 4 of Chung – which is reprised here.



(Annotations added.) As the annotations show, the third input signal ("CLK2") is (among other things) connected directly to the gate of transistor M20, which is part of the first driver; thus, the third input signal directly controls the on/off operation of a transistor (specifically, transistor M20) that is included in the first driver.

187. In comparison to claim element [1-d], this claim further requires that the on/off operation of this transistor serves to control the voltage of the second node (i.e., "Q"); that this is the case is readily seen via the examination of an annotated version of Figure 4 of Chung that was presented in the discussion of claim element [1-b], in Section XII.A.1.c.



(Annotations added.) As depicted in this annotated version of Figure 4 of Chung, when the voltage on the first node ("QB") turns on transistor M19, the only thing between the first power supply ("GCK") and the second node ("Q") is the transistor

M20. Thus, when transistor M20 is turned on, current will flow from the first power supply (GCK) to the second node ("Q"), charging up the second node ("Q") and controlling its voltage. (In contrast, when transistor M20 is turned off, this access from the first power supply (GCK) to the second node ("Q") is blocked by transistor M20 – and the voltage on the second node ("Q") will be (and *must* be) unaffected by any influences that would be coming into that node via the path that runs through transistor M20.)

188. Thus, Chung anticipates this claim of the '593 patent.

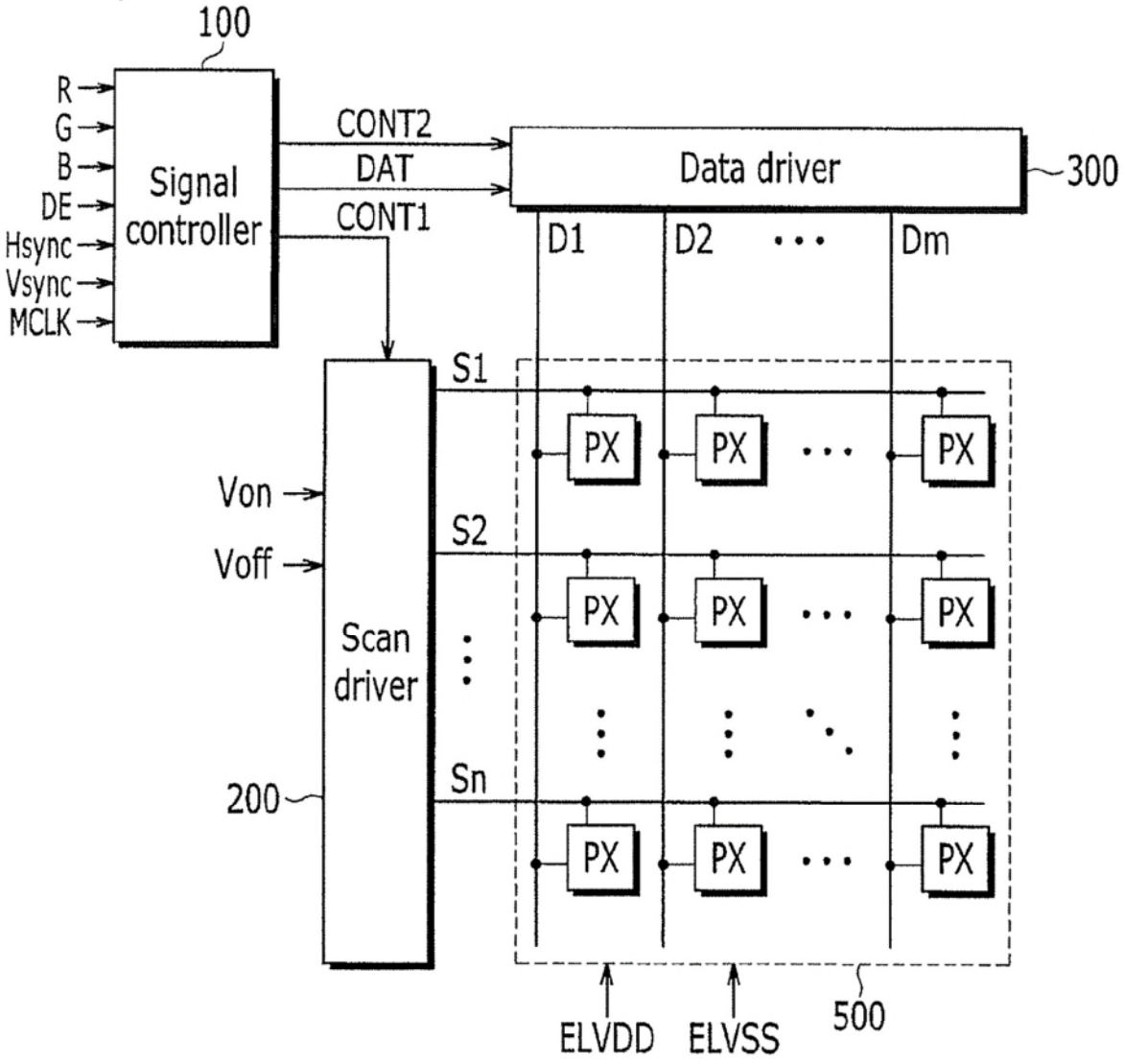
10. Independent Claim 15

189. It is my conclusion and opinion that Claim 15 of the '593 patent is anticipated by Chung.

a. [15-pre]: "An organic light emitting display, comprising:"

190. As an initial matter, I will be offering no opinion regarding whether or not the preamble of Claim 15 is limiting. I have been instructed by counsel for Petitioner to offer an opinion as to whether or not the prior art discloses the preamble, regardless of whether or not the preamble is limiting.

191. Chung discloses the preamble of Claim 15 of the '593 patent. First, Chung discloses in Figure 1 (a figure that will be discussed in more detail below) a diagram of an apparatus that is a display.



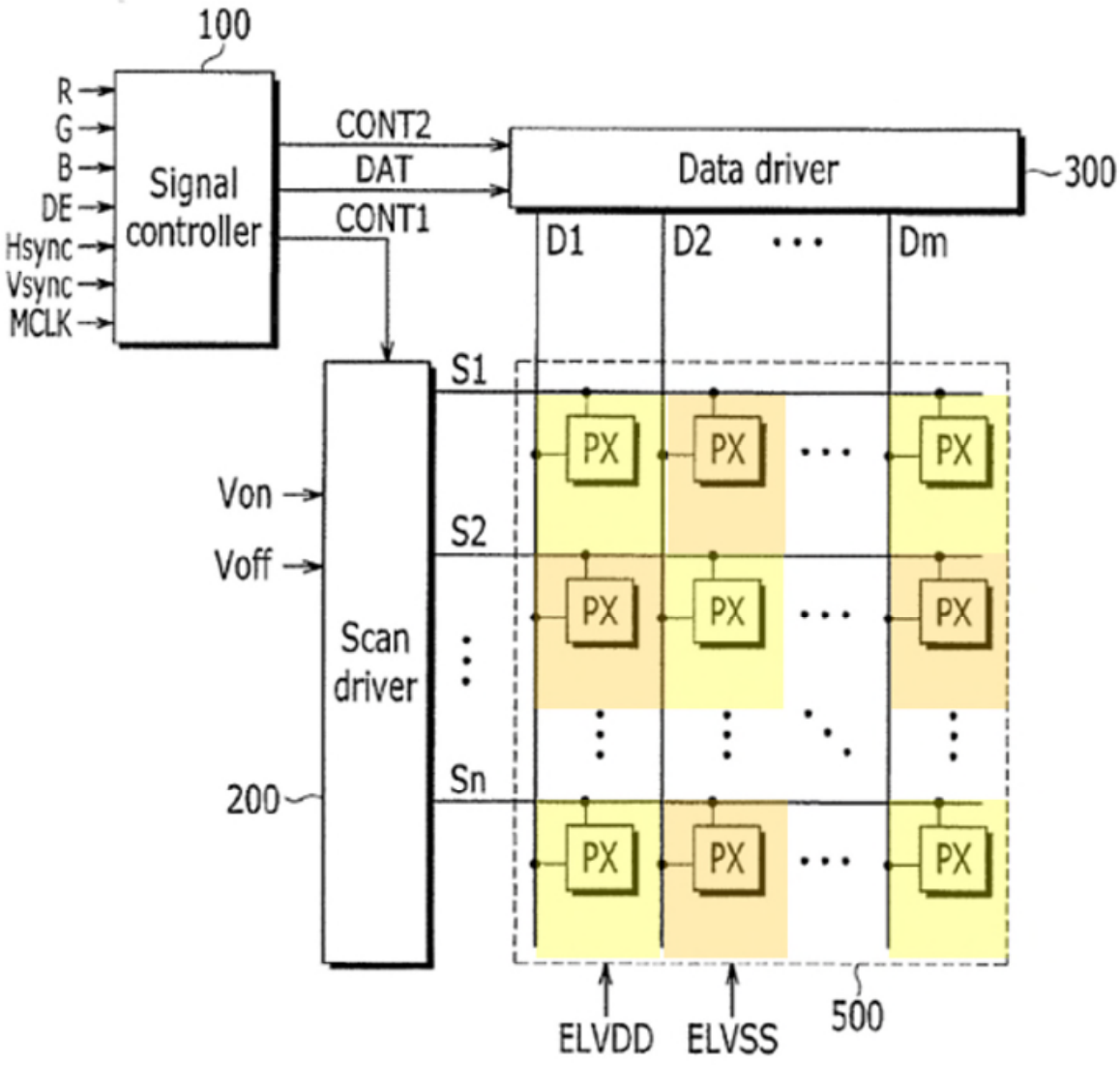
Given that Chung refers multiple times (at [0054], [0056], [0057], and [0061]) to the "PX" elements as being pixels, a POSITA would have understood that Figure 1 of Chung is describing a display. Further, Chung describes the exemplary embodiment at [0063] as: "the display device according to the exemplary embodiment of the present invention is described as an organic light emitting diode display using an organic light emitting diode."

192. Thus, Chung discloses the preamble of Claim 15 of the '593 patent.

b. [15-a]: "pixels positioned in regions partitioned by scan lines and data lines;"

193. Chung discloses this claim element of Claim 15 of the '593 patent.

194. This can readily be seen via an annotated version of Figure 1 of Chung.



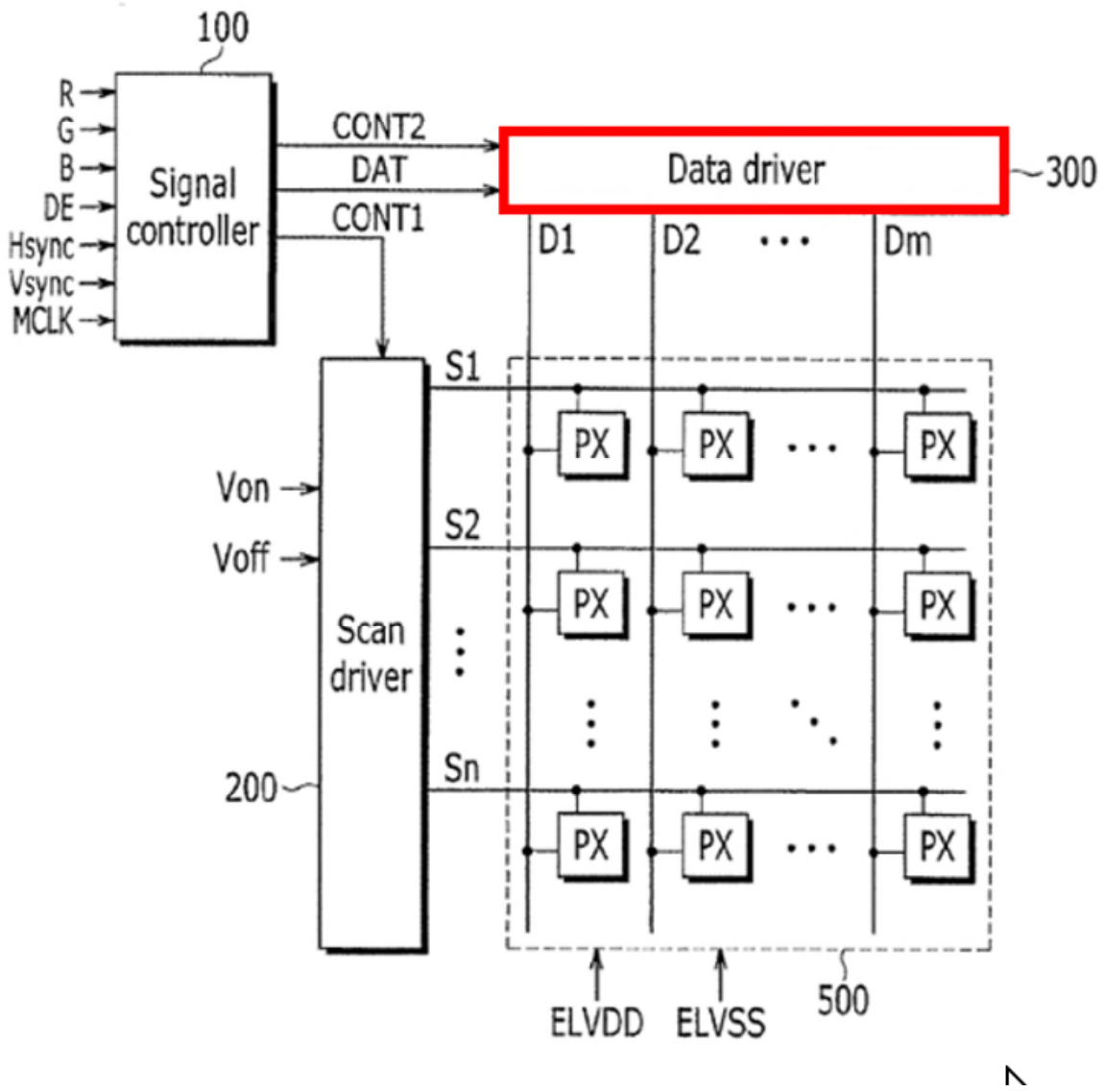
(Annotations added.) As noted above, Chung identifies the "PX" elements as pixels. Further, Chung notes the general presence of scan lines and data lines at [0005] ("A display area of a display device includes a plurality of pixels that are coupled to a plurality of scan lines and a plurality of data lines and arranged substantially in a matrix format."), and more specifically at e.g. [0056], where the related details in Figure 1 of Chung are explained ("The display unit 500 includes a plurality of scan lines S1-Sn, a plurality of data lines D1-Dm, and a plurality of pixels PX coupled to the plurality of signal lines S1-Sn and D1-Dm and arranged approximately in a matrix format.").

195. Thus, Chung discloses this claim element of Claim 15 of the '593 patent.

c. [15-b]: "a data driver for supplying data signals to the pixels through the data lines; and"

196. Chung discloses this claim element of Claim 15 of the '593 patent.

197. This can be readily seen by further examination of Figure 1 of Chung.



(Annotations added.) The presence of a data driver is explicitly depicted as such in Figure 1 of Chung; further, the data driver is described explicitly (by name) at, e.g., [0055] and [0059] of Chung. As noted above, the lines labeled D1, D2 … Dm are described in Chung as being data lines (at, e.g., [0056]), which provide data signals to the pixels (PXs).

198. Thus, Chung discloses this claim element of Claim 15 of the '593 patent.

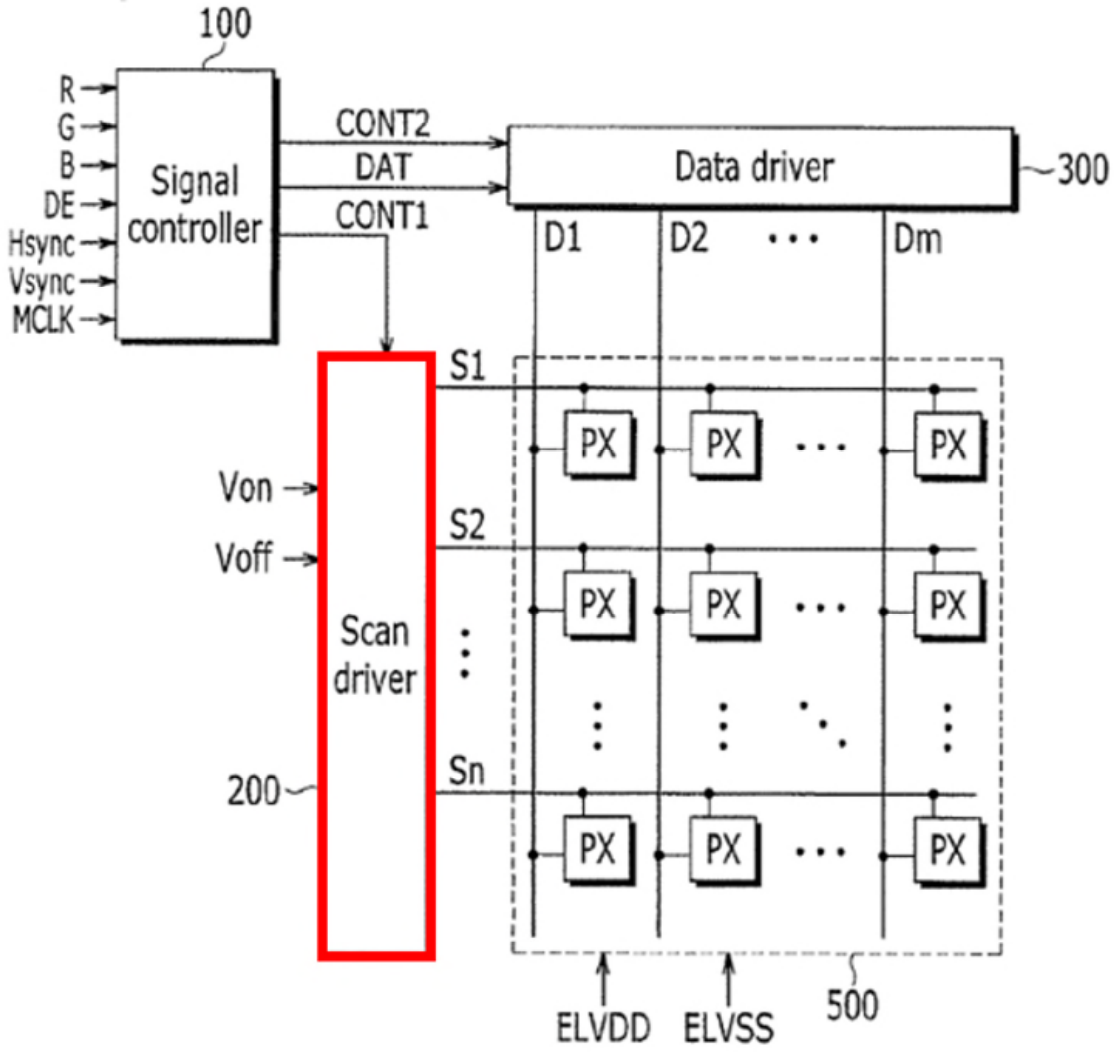
d. [15-c]: "a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal,"

199. Claim element [15-c] is rather long – and thus the analysis will be simpler to explain if this claim element is broken up into sub-elements.

i. [15-c-1]: "a scan driver for supplying scan signals to the pixels through the scan lines"

200. Chung discloses this claim sub-element of claim element [15-c] of Claim 15 of the '593 patent.

201. This can be readily seen by further examination of Figure 1 of Chung.



(Annotations added.) The presence a scan driver is explicitly depicted as such in Figure 1 of Chung; further, the scan driver is described explicitly (by name) at, e.g., [0055] and [0057] of Chung.[12] At [0055] and [0057], Chung identifies the lines

[12] At [0055] and [0057], Chung names the Scan Driver 200 (in this annotated version of Figure 1 of Chung shown above) as "the scan driving apparatus"; this is the same thing as the "scan driver."

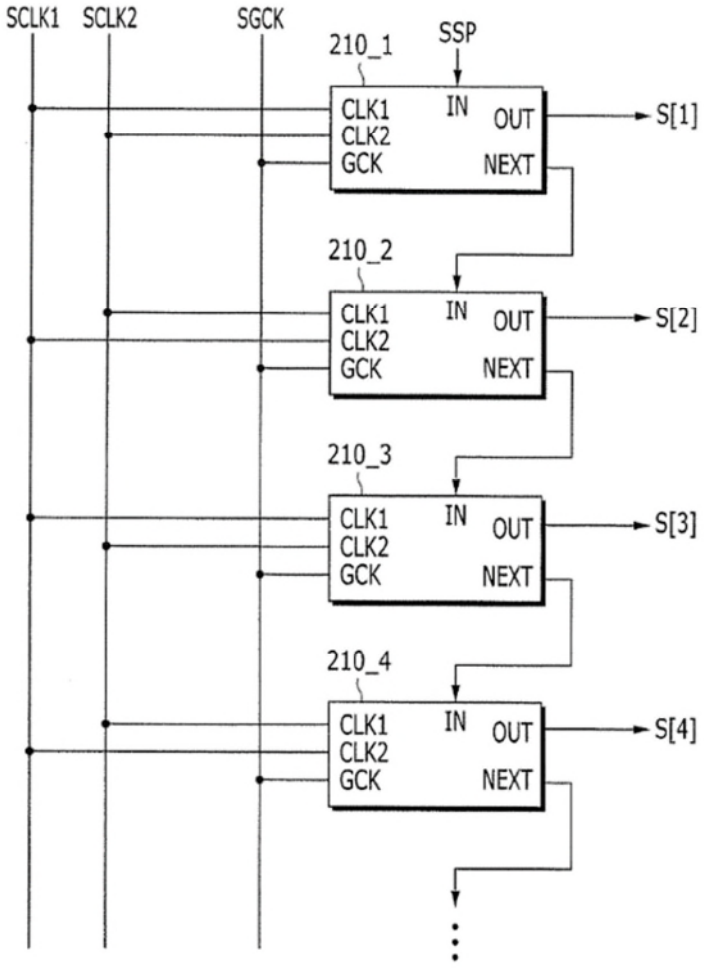
labeled S1, S2 … Sn as being scan lines (at, e.g., [0056]), which provide scan signals to the pixels (PXs).

202. Thus, Chung discloses this claim sub-element of claim element [15-c] of Claim 15 of the '593 patent.

ii. [15-c-2]: "the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals"

203. Chung discloses this claim sub-element of claim element [15-c] of Claim 15 of the '593 patent.

204. Chung describes the inner details of the scan driver in Figure 3.



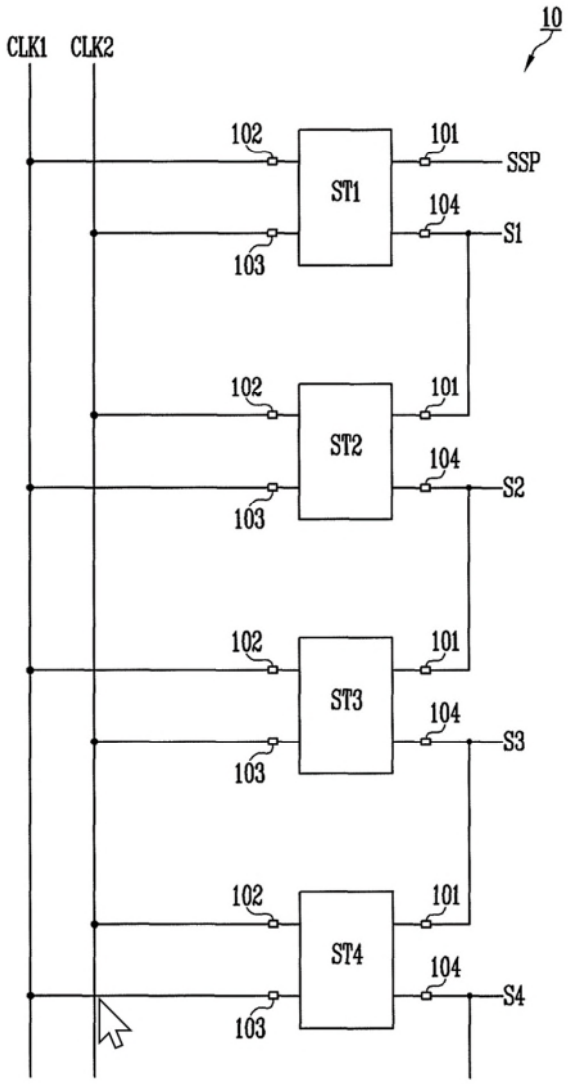
The functional details of this circuitry are explained in Chung at [0068]:

> Referring to FIG. 3, the scan driver includes a plurality of sequentially arranged scan driving blocks 210_1, 210_2, 210_3, 210_4, etc. Each of the scan driving blocks 210_1, 210_2, 210_3, 210_4, etc. receives an input signal and generates scan signals S[1], S[2], S[3], S[4], etc. respectively coupled to the plurality of scan lines S1 to Sn.

The "scan driving blocks" of Chung are the "stage circuits" of the '593 patent; the "stage circuits" of the '593 patent are so-called because they are arranged in a

cascade, where the output of one stage is supplied as input to the next stage – as is depicted in Figure 2 of the '593 patent:

FIG. 2



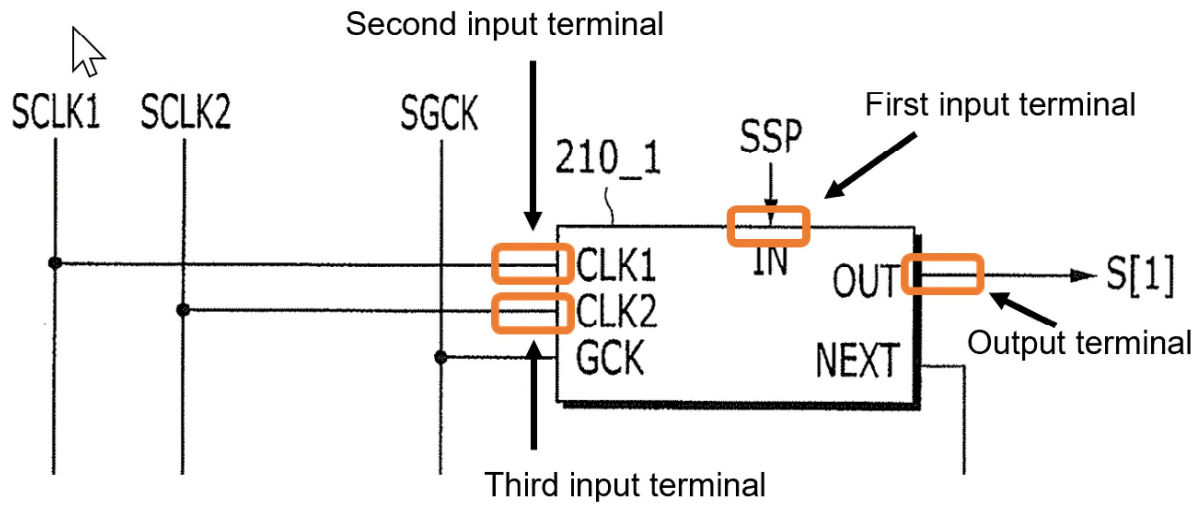
The output signal of each stage circuit is supplied as an input to the next stage – and the stage circuits are thus arranged in a cascade of such stage circuits. This is what is described in Chung – and the strong similarity between Figure 3 of Chung and Figure 2 of the '593 patent confirms this.

205. Thus, Chung discloses this claim sub-element of claim element [15-c] of Claim 15 of the '593 patent.

iii. [15-c-3]: "and having a first input terminal, a second input terminal, a third input terminal, and an output terminal,"

206. This claim sub-element of claim element [15-c] of Claim 15 of the '593 patent is disclosed by Chung.

207. The claim sub-element is essentially identical to the preamble of Claim 1 of the '593 patent – which was already discussed in detail earlier (at Section XII.A.1.a) – where it was shown that these details are disclosed by Chung. An annotated figure (Figure 3 from Chung) from Section XII.A.1.a can be repeated here to reinforce the point.



(Annotations added.)

208. Thus, Chung discloses this claim sub-element of claim element [15-c] of Claim 15 of the '593 patent.

iv. Claim Element [15-c] Summary

209. As just demonstrated, Chung discloses claim sub-elements [15-c-1], [15-c-2], and [15-c-3] of the '593 patent; thus, Chung discloses claim element [15-c] of Claim 15 of the '593 patent.

e. Preface to claim elements [15-d] – [15-g]

210. Between claim element [15-c] and claim element [15-d], Claim 15 includes the phrase "wherein each of the stage circuits includes:". It is taken here that this is intended to mean that "includes" is stated with regard to the sequential list claim elements which follow for the remainder of Claim 15 – that is, claim elements [15-d], [15-e], [15-f], and [15-g]. Each of these claim elements will be considered in turn.

f. [15-d]: "an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node,"

211. This claim element is identical to claim element [1-a] of Claim 1 of the '593 patent – which was discussed earlier (in Section XII.A.1.b).

212. Thus, Chung discloses this claim element of Claim 15 of the '593 patent.

g. [15-e]: "a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal, and"

213. This claim element is identical to claim element [1-b] of Claim 1 of the '593 patent – which was discussed earlier (in Section XII.A.1.c).

214. Thus, Chung discloses this claim element of Claim 15 of the '593 patent.

h. [15-f]: "a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, wherein"

215. This claim element is identical to claim element [1-c] of Claim 1 of the '593 patent – which was discussed earlier (in Section XII.A.1.d).

216. Thus, Chung discloses this claim element of Claim 15 of the '593 patent.

i. [15-g]: "the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver."

217. This claim element is identical to claim element [1-d] of Claim 1 of the '593 patent – which was discussed earlier (in Section XII.A.1.e).

218. Thus, Chung discloses this claim element of Claim 15 of the '593 patent.

j. Claim 15 Summary

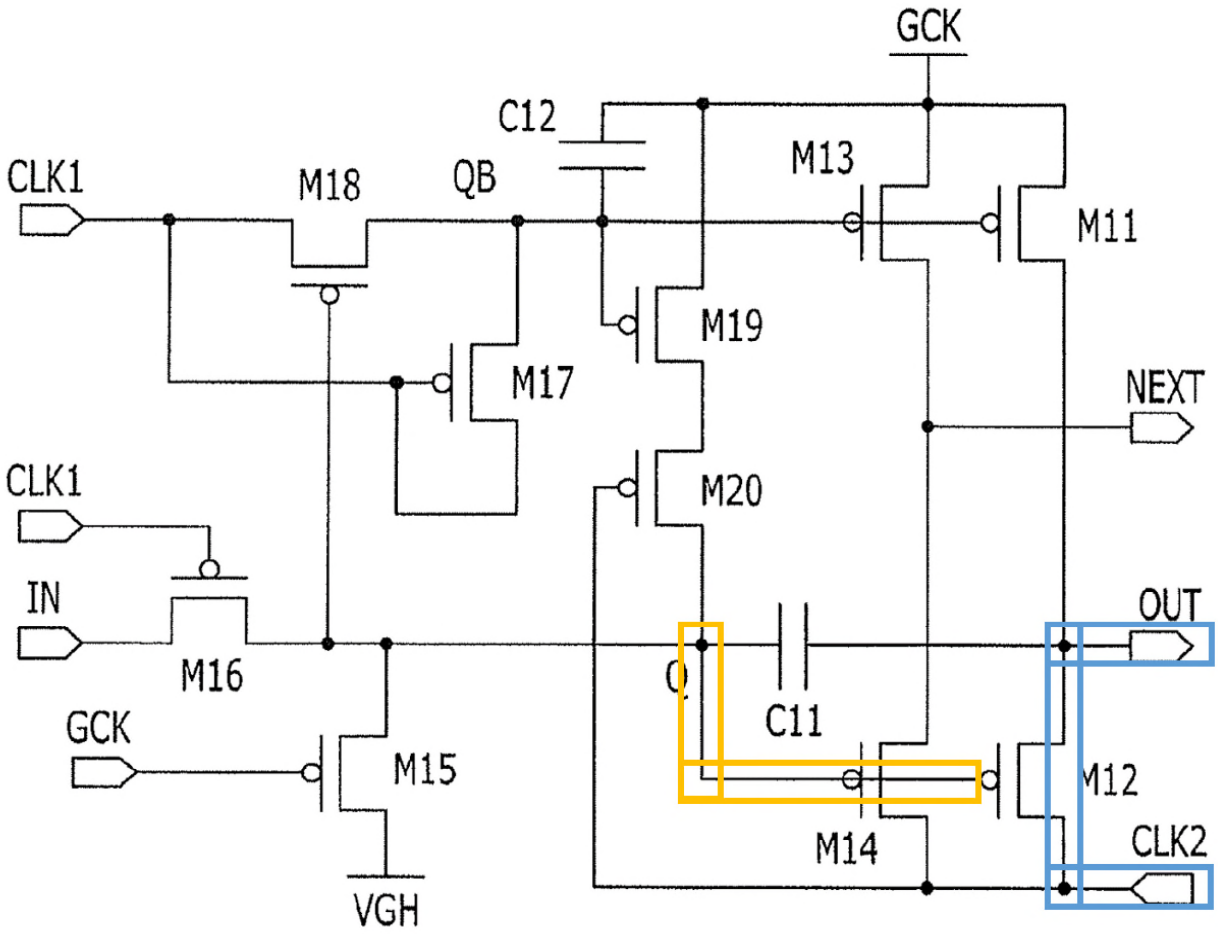
219. As just shown, Chung discloses each element of Claim 15 of the '593 patent; thus, Chung anticipates Claim 15 of the '593 patent.

11. Dependent Claim 16

220. As an initial matter, Claim 16 depends from Claim 15; as was shown above, Claim 15 of the '593 patent is disclosed by Chung.

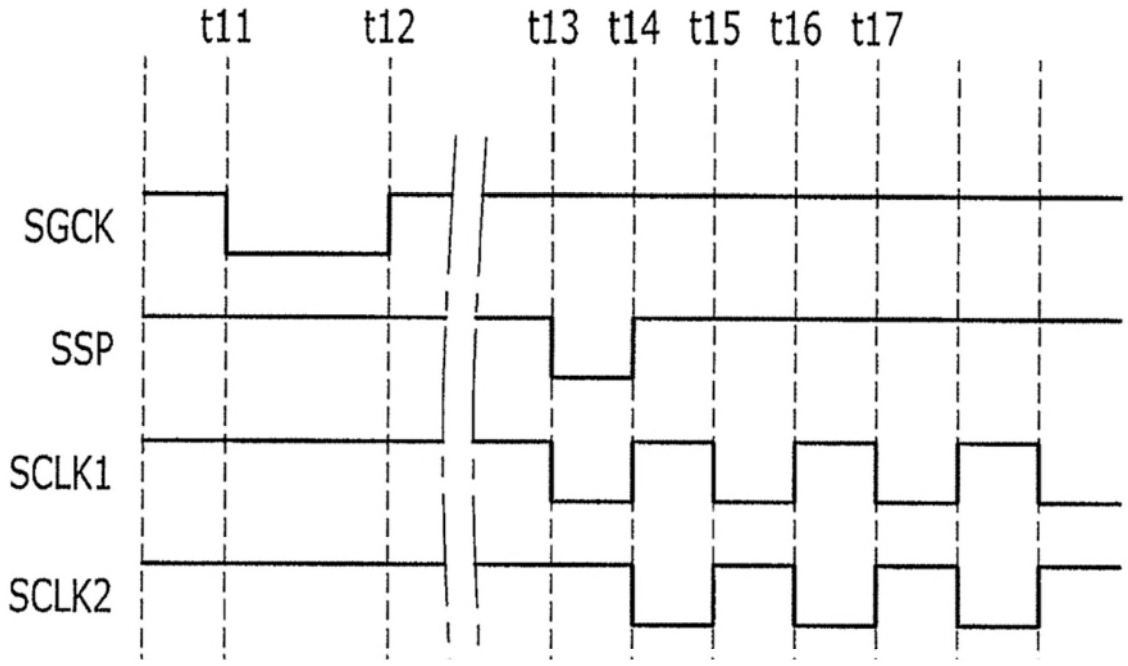
221. Claim 16 further requires "a clock signal supplied to the third input terminal is used as the scan signal." Chung discloses this claim of the '593 patent.

222. The first part of this claim element ("a clock signal supplied to the third input terminal") was already discussed earlier (in Section XII.A.1.b.iii) – with respect to claim sub-element [1-a-3] of claim element [1-a] of Claim 1 of the '593 patent. An annotated version of Figure 4 of Chung was provided there for purposes of explanation – and for clarity, that figure will be repeated here.



As detailed in Section XII.A.1.b.iii, when an appropriate (i.e., turn-on) voltage is applied at the second node (the node labeled "Q"), transistor M12 will turn on; this will connect the signal of the third input terminal ("CLK2") to the node of the output terminal ("OUT") – and thus the signal of the third input terminal (CLK2) is supplied to the output terminal ("OUT").

223. As also discussed earlier, the third input terminal (CLK2) receives a clock signal – in particular, the clock signal SCLK2, which is depicted in Figure 5 of Chung.



As the name itself indicates, the signal SCLK is clearly a clock signal.

224. Finally, with respect to this clock signal being used as "the scan signal," it was shown above (see the annotated version of Figure 4 of Chung above) that when transistor M12 is turned on, the input signal that is being applied to the third input terminal CLK2 (which, in this case is the clock signal SCLK2) is supplied to the output terminal OUT. As explained in Chung (at [0100]), "the logic low-level second clock signal SCLK2 is output as the scan signal S[1] through the first output terminal OUT." Therefore, the "clock signal applied to the third input terminal is used as the scan signal."

225. Thus, Chung anticipates this claim of the '593 patent.

12. Dependent Claim 17

226. As an initial matter, Claim 17 depends from Claim 15; as was shown above, Claim 15 of the '593 patent is disclosed by Chung.

227. Claim 17 further requires that "the first input terminal receives a scan signal of a previous stage circuit or a start signal."

228. This claim is identical to an element of Claim 2 of the '593 patent – which was discussed earlier (in Section XII.A.2).

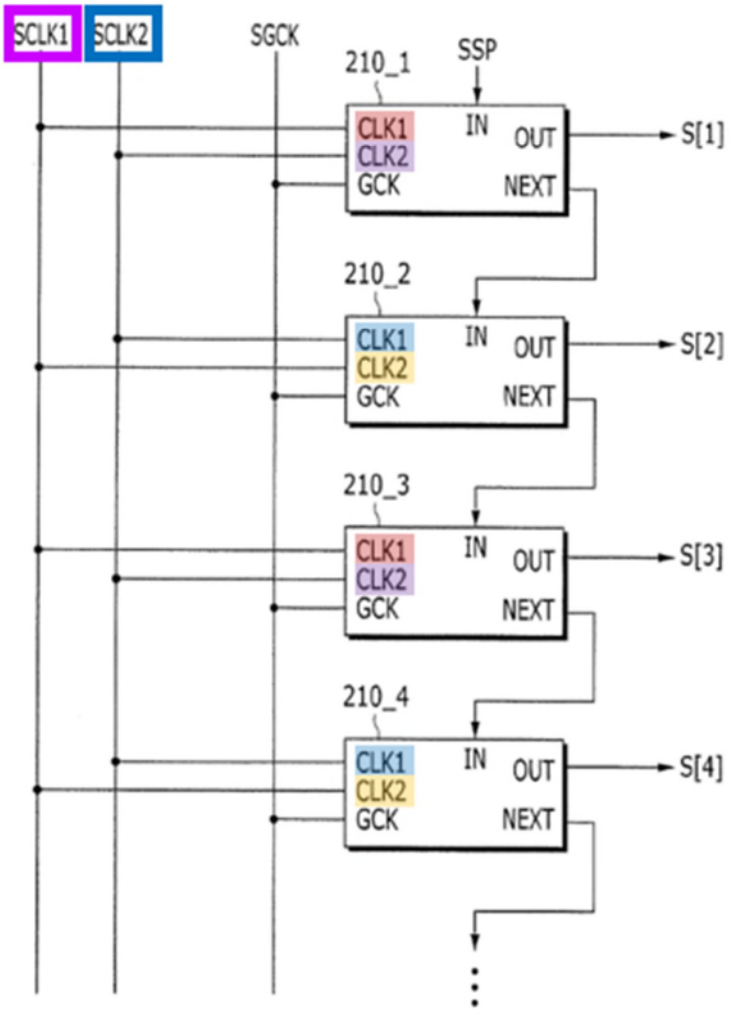
229. Thus, Chung anticipates this claim of the '593 patent.

13. Dependent Claim 18

230. As an initial matter, Claim 18 depends from Claim 17, and Claim 17 depends from Claim 15; as was shown above, Claim 15 and Claim 17 of the '593 patent are disclosed by Chung.

231. Claim 18 further requires "wherein second input terminals of odd stage circuits receive a first clock signal and third input terminals of odd stage circuits receive a second clock signal, and wherein second input terminals of even stage circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal." In other words, the first clock signal and the second clock signal alternate between the second input terminal and the third terminal along the sequence of stage circuits.

232. This is readily demonstrated via an annotated version of Figure 3 of Chung.



(Annotations added.) To simplify the explanation of what is going on, the first clock signal (SCLK1) is annotated in magenta, and its destinations are highlighted in maroon for odd-numbered stage circuits (210_1, 210_3, …) and orange for even-numbered stage circuits (210_2, 210_4, …). The second clock signal (SCLK2) is annotated in blue, and its destinations are highlighted in purple for odd-numbered

stage circuits (210_1, 210_3, …) and light blue for even-numbered stage circuits (210_2, 210_4, …). As can be seen by inspection, the first clock signal (SCLK1) goes to the second input terminal (CLK1) of the odd-numbered stage circuits (210_1, 210_3, …) and to the third input terminal (CLK2) of the even numbered stage circuits (210_2, 210_4, …), while the second clock signal (SCLK2) goes to the third input terminal (CLK2) of the odd-numbered stage circuits and to the second input terminal (CLK1) of the even-numbered stage circuits.

233. What is going on is also explained in Chung at [0070]:

> A first clock signal input terminal CLK1 of each of odd-numbered scan driving blocks 210_1, 210_3, etc., of the plurality of scan driving blocks 210_1, 210_2, 210_3, 210_4, etc., is applied with a first clock signal SCLK1, and a second clock signal input terminal CLK2 thereof is applied with a second clock signal SCLK2. In addition, a first clock signal input terminal CLK1 of each of even-numbered scan driving blocks of the plurality of scan driving blocks 210_1, 210_2, 210_3, 210_4, etc., is applied with the second clock signal SCLK2, and a second clock signal input terminal CLK2 thereof is applied with the first clock signal SCLK1.

234. Thus, Chung anticipates this claim of the ‘593 patent.

14. Dependent Claim 19

235. As an initial matter, Claim 19 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the ‘593 patent are disclosed by Chung.

236. Claim 19 further requires that "the first clock signal and the second clock signal have the same period and have phases that do not overlap."

237. This claim is identical to Claim 3 of the '593 patent – which was discussed earlier (in Section XII.A.3).

238. Thus, Chung anticipates this claim of the '593 patent.

15. Dependent Claim 20

239. As an initial matter, Claim 20 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the '593 patent are disclosed by Chung.

240. Claim 20 further requires "wherein the first driver includes: a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and a second transistor and a third transistor serially positioned between the second node and the first power supply, wherein a gate electrode of the second transistor is coupled to the third input terminal, and wherein a gate electrode of the third transistor is coupled to the first node."

241. This claim is identical to Claim 6 of the '593 patent – which was discussed earlier (in Section XII.A.6).

242. Thus, Chung anticipates this claim of the '593 patent.

16. Dependent Claim 21

243. As an initial matter, Claim 21 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the '593 patent are disclosed by Chung.

244. Claim 21 further requires "wherein the outputting unit includes: a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node: a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node: a first capacitor between the second node and the output terminal; and a second capacitor between the first node and the first power supply."

245. This claim is identical to Claim 7 of the '593 patent – which was discussed earlier (in Section XII.A.7).

246. Thus, Chung anticipates this claim of the '593 patent.

17. Dependent Claim 23

247. As an initial matter, Claim 23 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the '593 patent are disclosed by Chung.

248. Claim 23 further requires "wherein the second driver includes: a sixth transistor between the first node and the second input terminal, the sixth transistor

having a gate electrode coupled to the second node; and a seventh transistor between the first node and the second input terminal, the seventh transistor being diode connected."

249. This claim is identical to Claim 9 of the '593 patent – which was discussed earlier (in Section XII.A.8).

250. Thus, Chung anticipates this claim of the '593 patent.

18. Dependent Claim 25

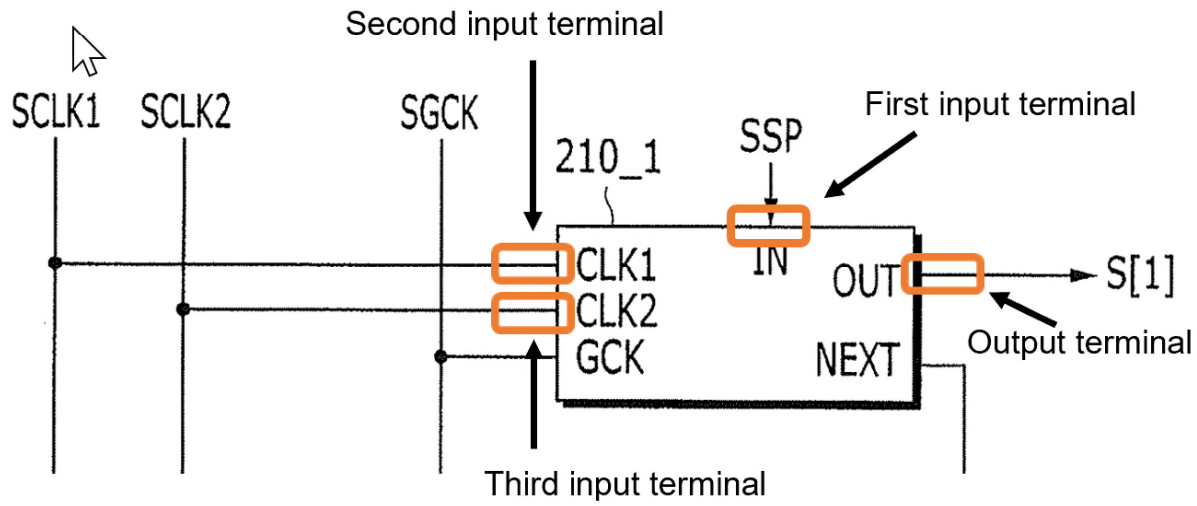
251. As an initial matter, Claim 25 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the '593 patent are disclosed by Chung.

252. Claim 25 further requires that "the scan signal of the previous stage circuit ***or*** the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal." (Emphasis added.) As per the emphasis added to the word "or" in the claim, Claim 25 of the '593 patent offers two alternatives regarding the provision of a signal to the first input terminal (such that it overlaps the clock signal supplied to the second input terminal).

253. The second alternative specifies that it is the start signal that is applied to the first input terminal (and with the condition that follows – that the signal thus supplied overlaps the clock signal supplied to the second input terminal) – and is thus identical to Claim 5 of the '593 patent (which was discussed earlier, in Section

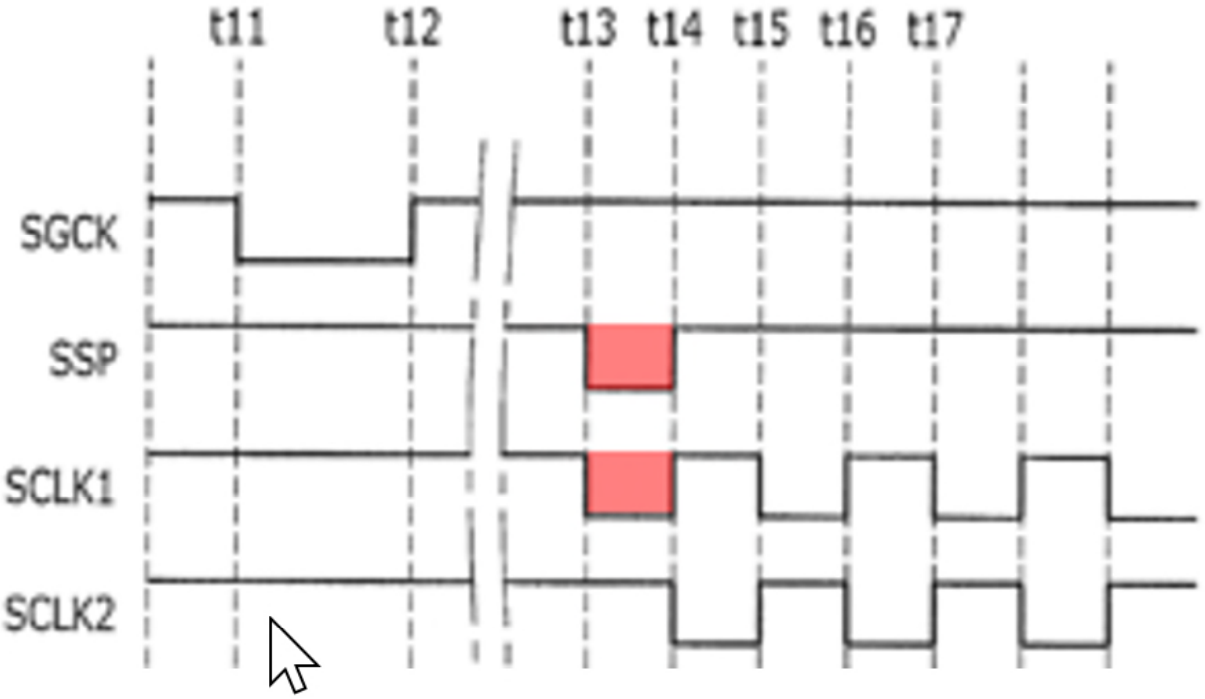
XII.A.5), which requires that "the start signal is supplied to overlap the first clock signal."

254. Further, Claim 5 depends from Claim 2, which depends from Claim 1 – and it is in Claim 1 (more specifically, in the preamble of Claim 1 – which was discussed in Section XII.A.1.a) that the inputs and outputs of the first stage circuit are explained; thus, a figure from Section XII.A.1.a is simply repeated here.



(Annotations added.) As can once again be seen by examination of this annotated excerpt from Figure 3 of Chung, the start signal (SSP) is supplied to the first input terminal (IN), while the first clock signal (SCLK1) is supplied to the second input terminal (CLK1).

255. The timing diagram for these waveforms is found in Figure 5 of Chung – and thus, an annotated version of this diagram, which was presented earlier in the discussion of Claim 5 (in Section XII.A.5) is reprised here.



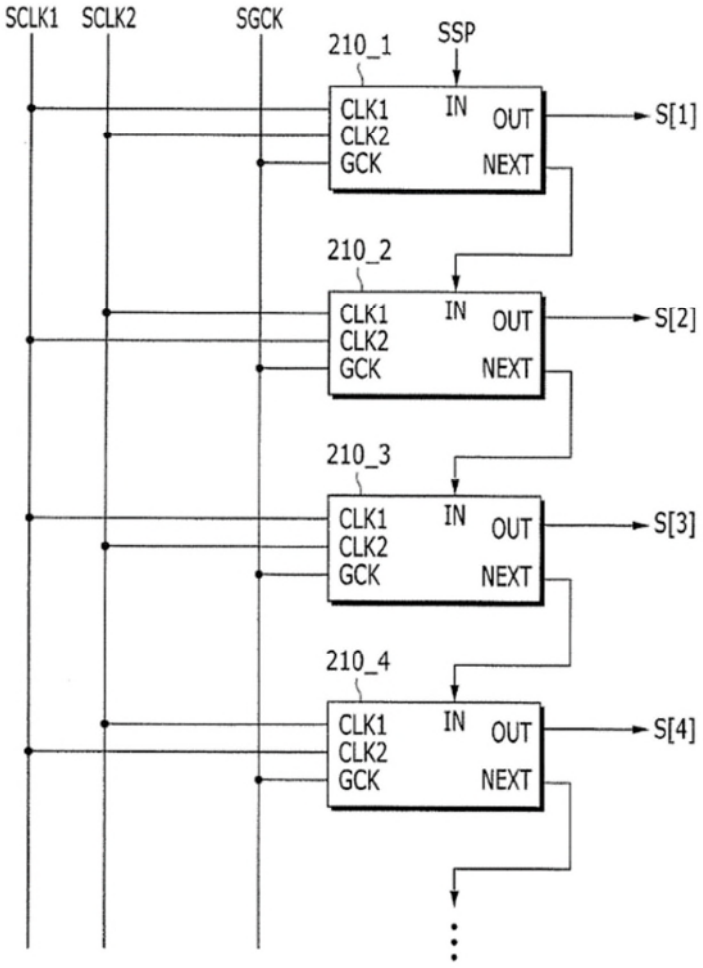
As can be seen, the start signal (SSP) goes low (its "active" level) at the same time and for the same duration that the first clock signal (SCLK1) goes low (also its "active" level) as part of its recurring square wave behavior. Thus, the start signal (SSP) overlaps the first clock signal (SCLK1).

256. Thus, Chung anticipates this claim of the '593 patent.

257. For completeness, it is worth noting that the first alternative on offer in Claim 25 specifies that it is the scan signal of the previous stage circuit that is applied to the first input terminal (and with the condition that follows – that the signal thus

supplied overlaps the clock signal supplied to the second input terminal). As detailed earlier (in the discussion of claim sub-element [15-c-2] in Section XII.10.d.ii), after the first stage circuit (which receives a start signal as the input signal at the first input terminal), the first input terminal of subsequent stage circuits receives the signal that is output from the output terminal of the preceding stage circuit. Meanwhile, for odd-numbered stages, the second input terminal (CLK1) receives the first clock signal (SCLK1) – while for even-numbered stages, the second input terminal (CLK1) receives the second clock signal (SCLK2).

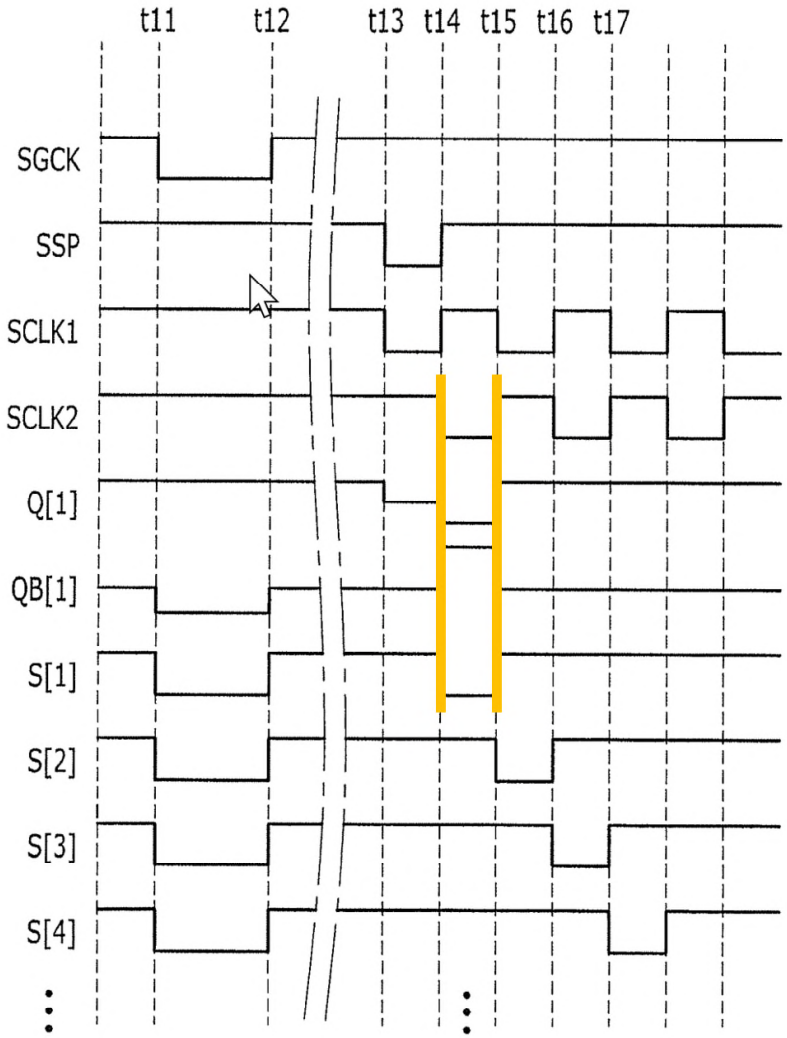
258. This is all readily summarized in Figure 3 of Chung – which was presented in Section XII.10.d.ii (without annotations), and which is reprised here.



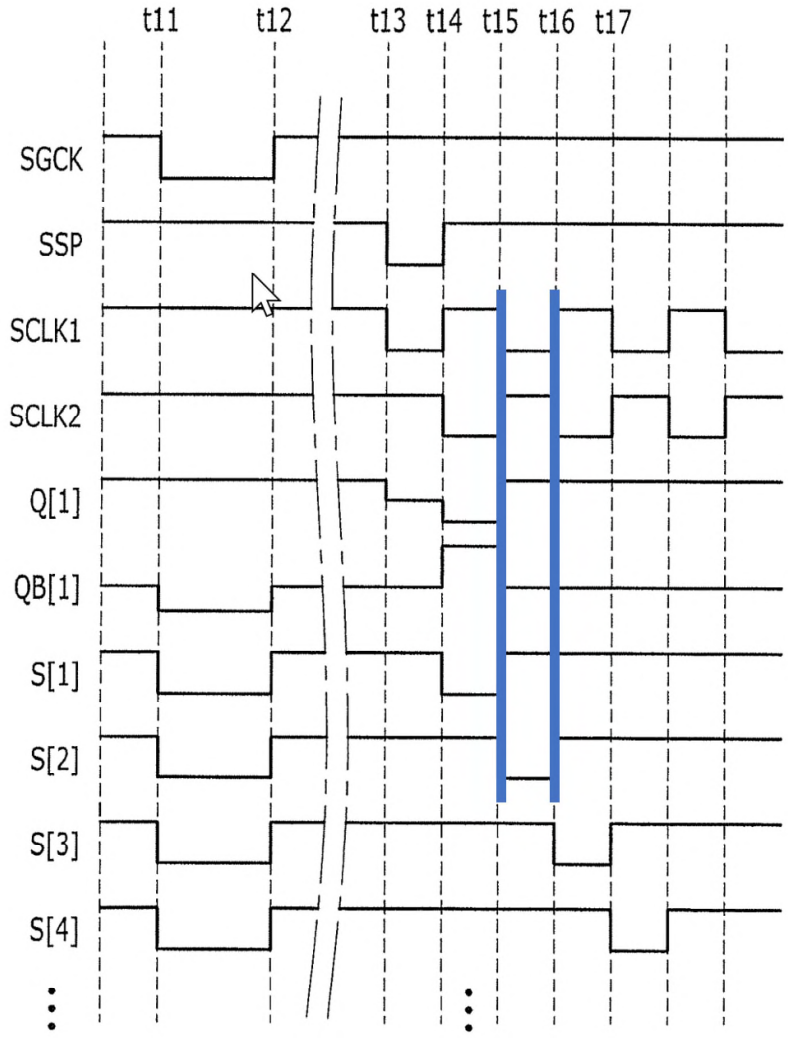
259. Consider the second stage circuit (210_2); this stage circuit will receive the output from the first stage circuit (S[1]) at its input terminal (IN), and receive the second clock signal (SCLK2) at its second input terminal (CLK1). Now consider the third stage circuit (210_3); this stage circuit will receive the output from the second stage circuit (S[2]) at its input terminal (IN), and receive the first clock signal (SCLK1) at its second input terminal (CLK1). This pattern can readily be repeated to provide the same details for all subsequent stage circuits.

260. In order to meet the first alternative of Claim 25 (as discussed just above), for even-numbered stage circuits the signal received at the input terminal (IN) must overlap with the second clock signal (SCLK2), while for odd-numbered stage circuits the signal received at the input terminal (IN) must overlap with the first clock signal (SCLK1).

261. Examination of Figure 5 of Chung shows that this is indeed the case – as two annotated versions of this figure make clear.



(Annotations added.) The annotations here are for the second stage circuit – which receives the output signal from the first stage circuit (S[1]) at its input terminal (IN) and the second clock signal (SCLK2) at its second input terminal (CLK1). As can be seen, S[1] overlaps SCLK2 – meeting the requirement specified in the first alternative of Claim 25 of the '593 patent.



(Annotations added.) The annotations here are for the third stage circuit – which receives the output signal from the second stage circuit (S[2]) at its input terminal

(IN) and the first clock signal (SCLK1) at its second input terminal (CLK1). As can be seen, S[2] overlaps SCLK1 – meeting the requirement specified in the first alternative of Claim 25 of the '593 patent.

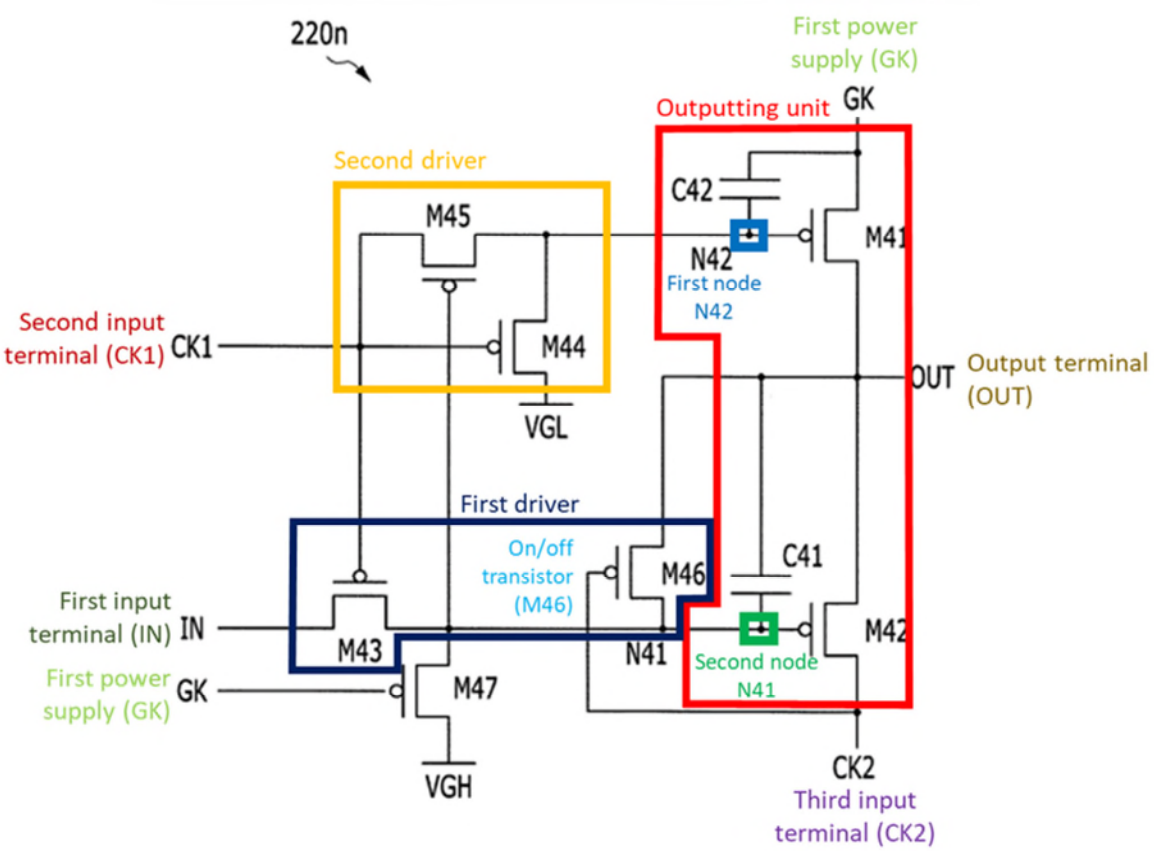
262. It is also evident from both annotated versions of Figure 5 of Chung presented here that this analysis could be repeated for the fourth stage circuit, the fifth stage circuit, … and for all further even-numbered and odd-numbered stage circuits – and that the same results would be found for each stage circuit.

263. Thus, Chung anticipates this claim of the '593 patent for these additional (and separate) reasons.

B. Ground 2: Kim Anticipates Claims 1-5, 7-8, 14-19, 21-22, and 25

264. As will be discussed below, it is my conclusion and opinion that Claims 1-5, 7-8, 14-19, 12-22, and 25 of the '593 patent are anticipated by Kim.

265. Before beginning a discussion of the analysis, it will be helpful to first provide an annotated version of Figure 9 of Kim – with the annotations indicating the identification of the specific structures recited in the claims of the '593 patent, as mapped to Kim.



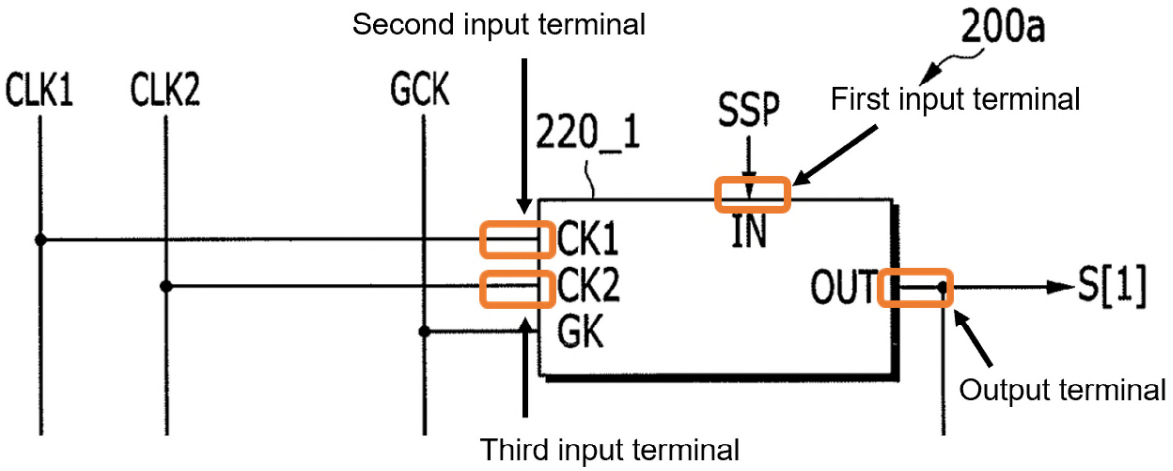
1. Independent Claim 1

266. It is my conclusion and opinion that Claim 1 of the '593 patent is anticipated by Kim.

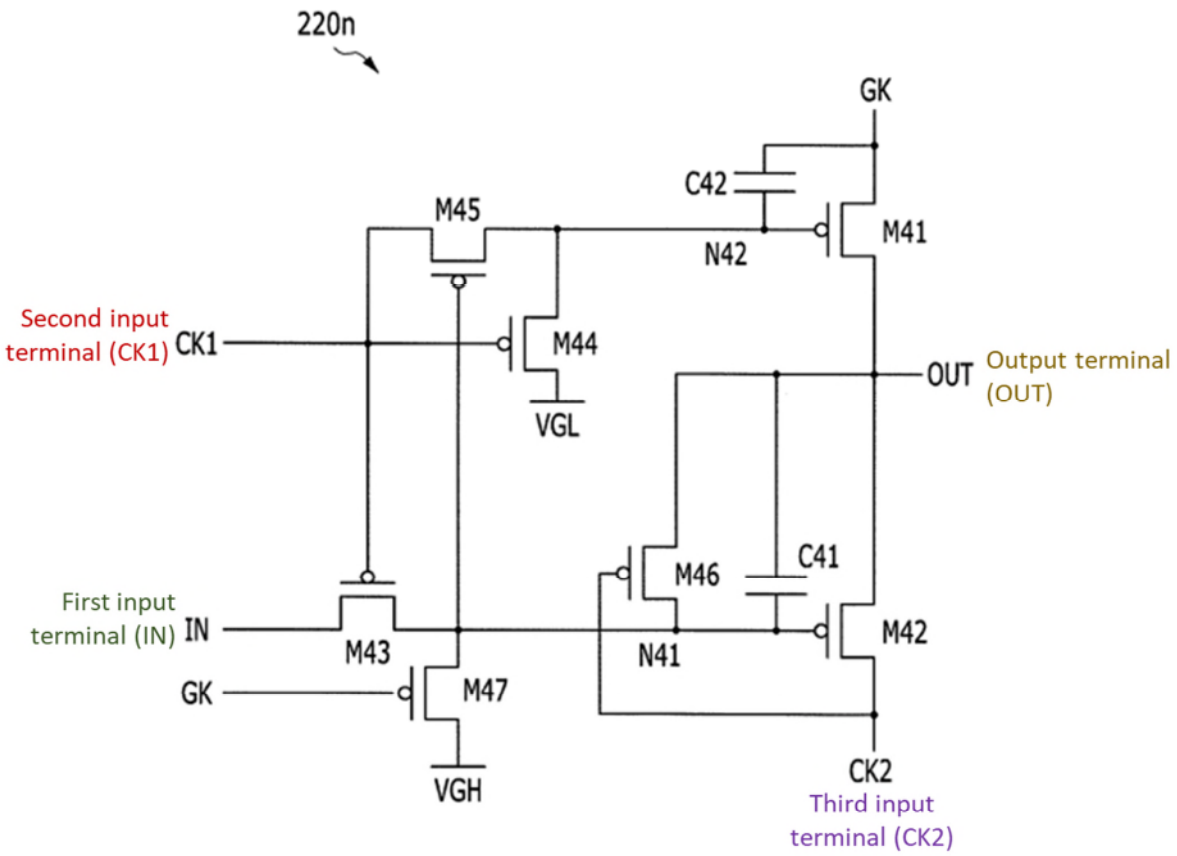
a. [1-pre]: "A stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal, the stage circuit comprising:"

267. As an initial matter, I will be offering no opinion regarding whether or not the preamble of Claim 1 is limiting. I have been instructed by counsel for Petitioner to offer an opinion as to whether or not the prior art discloses the preamble, regardless of whether or not the preamble is limiting.

268. Kim discloses the preamble of Claim 1 of the '593 patent; this can be seen readily via annotated versions of Figure 8 and Figure 9 of Kim:



(Excerpted from Figure 8 of Kim; annotations added.)



(Annotations added.)

269. The excerpt above from Figure 8 of Kim is the "black box" version of the more-detailed circuit depiction of Figure 9 of Kim; the annotations identify the same terms in both figures.

270. As can be seen in both annotated figures, Kim discloses a first input terminal, a second input terminal, a third input terminal, and an output terminal – all of which are part of a stage circuit.

271. Thus, Kim discloses the preamble of Claim 1 of the '593 patent.

b. [1-a]: "an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power

> ***supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node:"***

272. Claim element [1-a] is rather long – and thus the analysis will be simpler to explain if this claim element is broken up into sub-elements.

273. As a preliminary matter, note that this claim element requires "a voltage of a first power supply."

274. The actual scan operations for which Kim's circuitry has been designed begin at time t23, which Kim describes as:

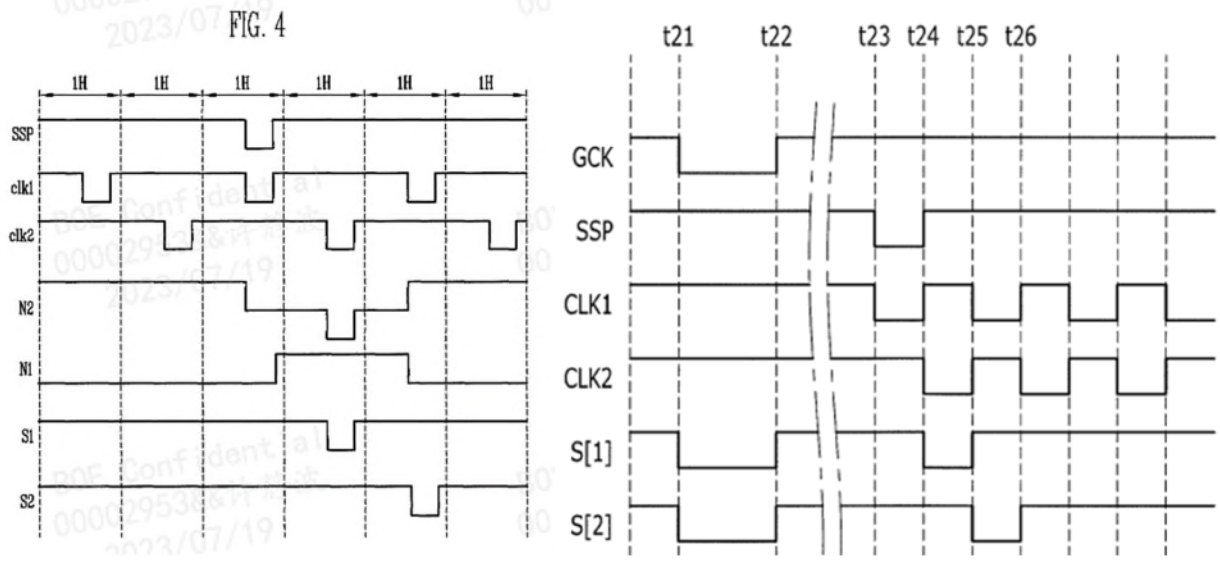
> A period after t23 is a period of the scanning (c) during which the scan signals of the gate-on voltage are sequentially output to the plurality of scan lines S1 to Sn. **In the period after t23, the output control signal GCK is applied as the logic high level voltage**. (Kim at [0176]; emphasis added.)

As this excerpt states clearly, beginning at time t23 the output control signal GCK (which is applied to the output control signal input terminals of the stage circuits) is set to a logic high-level voltage – and remains constant at that logic high-level voltage during the scan operations.

275. Thus, during those circuit operations, the voltage at the stage circuit input terminal GK is maintained at the logic high-level voltage (VGH) – and thus, during those circuit operations, GK provides a power supply voltage. Therefore, it is acceptable, during the aforementioned scan operations, to refer to the voltage at

the input terminal GK as being the first power supply voltage – since a constant DC voltage will be applied there, and will not change.

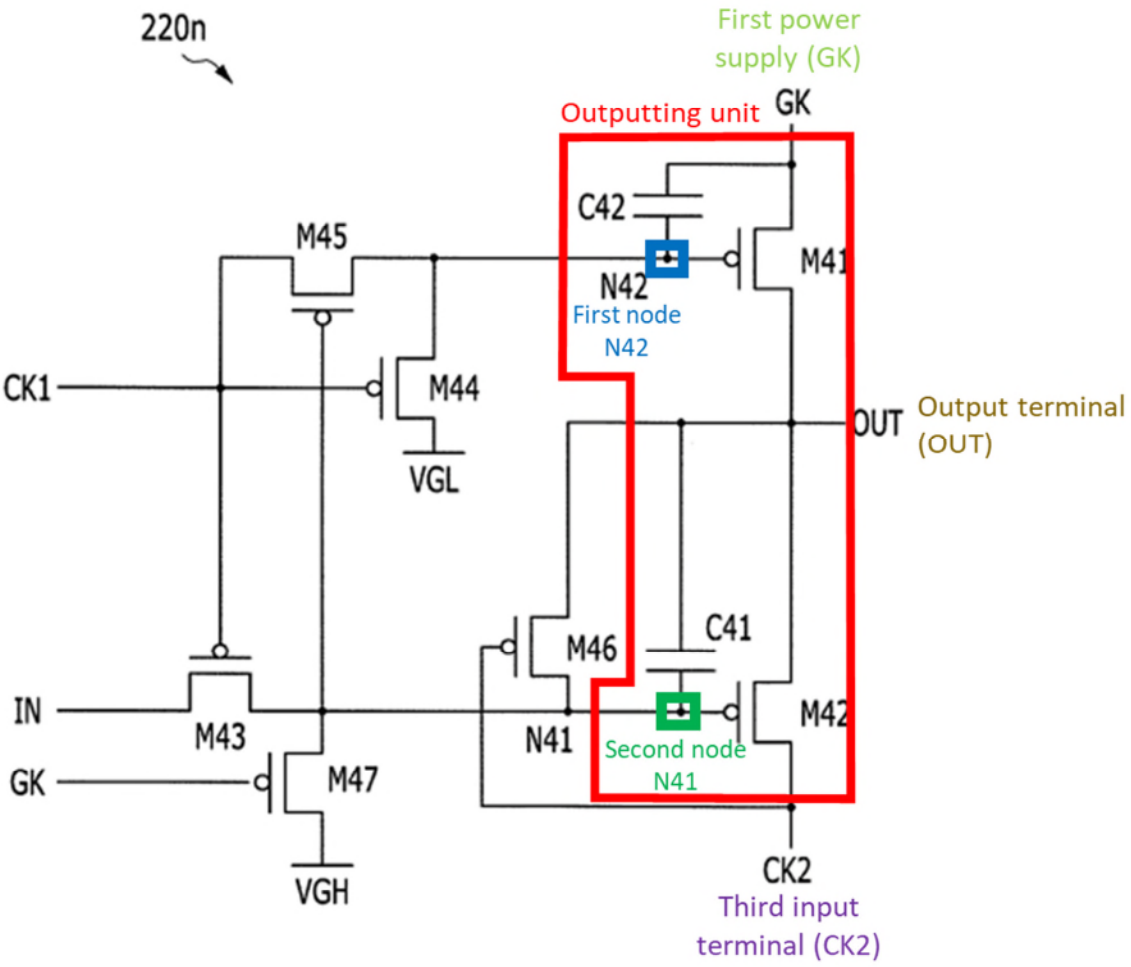
276. Further, the duration of the actual scan operations is the only time period that the ’593 patent addresses. This is revealed through the timing diagram in Figure 4 of the ’593 patent and its associated descriptions. Although Figure 4 shows two horizontal periods before the period in which the start signal SSP becomes active, the associated description detailing the timing diagram begins “during a third horizontal period [in which] the start signal SSP is supplied.” (’593 patent at 6:41-53.) This third horizontal period and subsequent periods parallel the periods at t23 and later in Figure 10 of Kim, i.e., the duration of the actual scan operations:



’593 patent, Fig. 4, Kim, Fig. 10.

i. [1-a-1]: "an outputting unit having a first node and a second node,"

277. Kim discloses this claim sub-element; this is evident via an annotated version of Figure 9 of Kim:



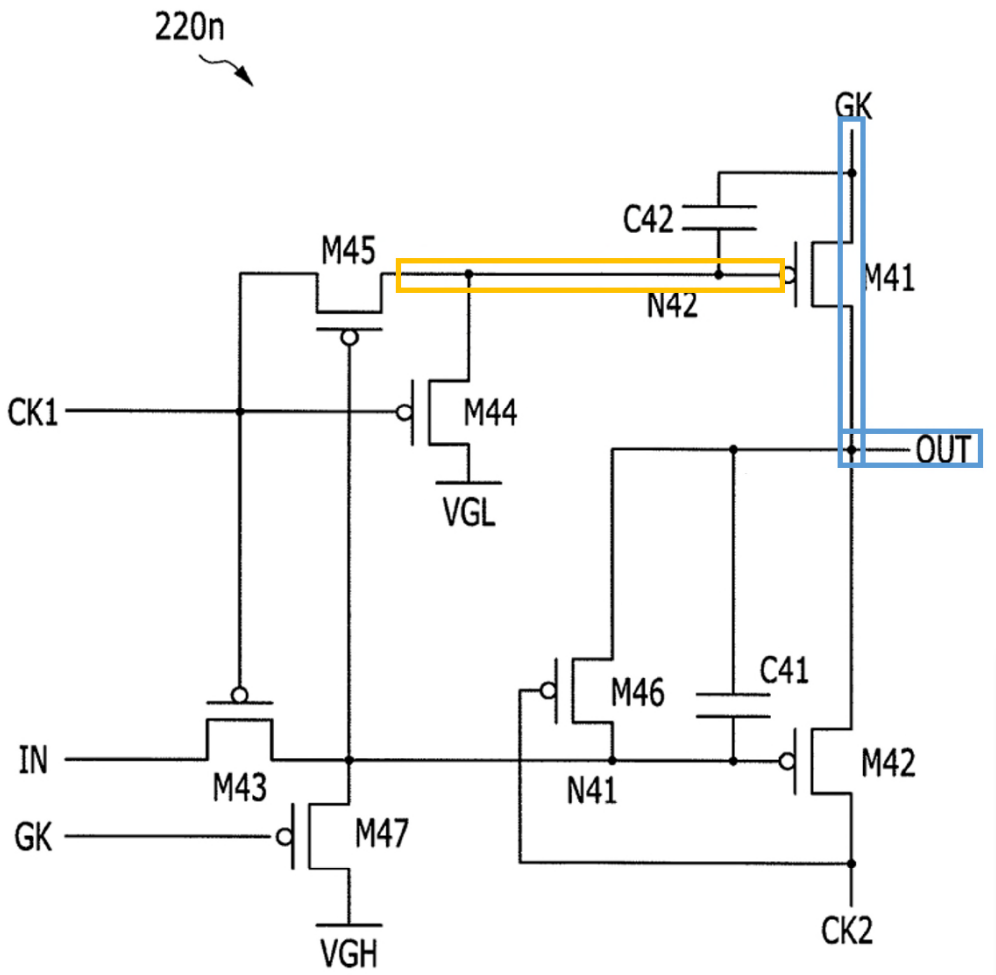
(Annotations added.) The node labeled "N42" is the first node, and the node labeled "N41" is the second node – while the "outputting unit" is a shown via the annotation box-bounding in red.

278. Thus, Kim discloses this claim sub-element of this claim element of Claim 1 of the '593 patent.

ii. [1-a-2]: "the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node"

279. Kim discloses this claim sub-element; this is evident via an annotated version of Figure 9 of Kim:

FIG. 9



(Annotations added.) As the annotations show, when an appropriate (i.e., turn-on) voltage is applied at the first node (the node labeled "N42"), transistor M41 will turn

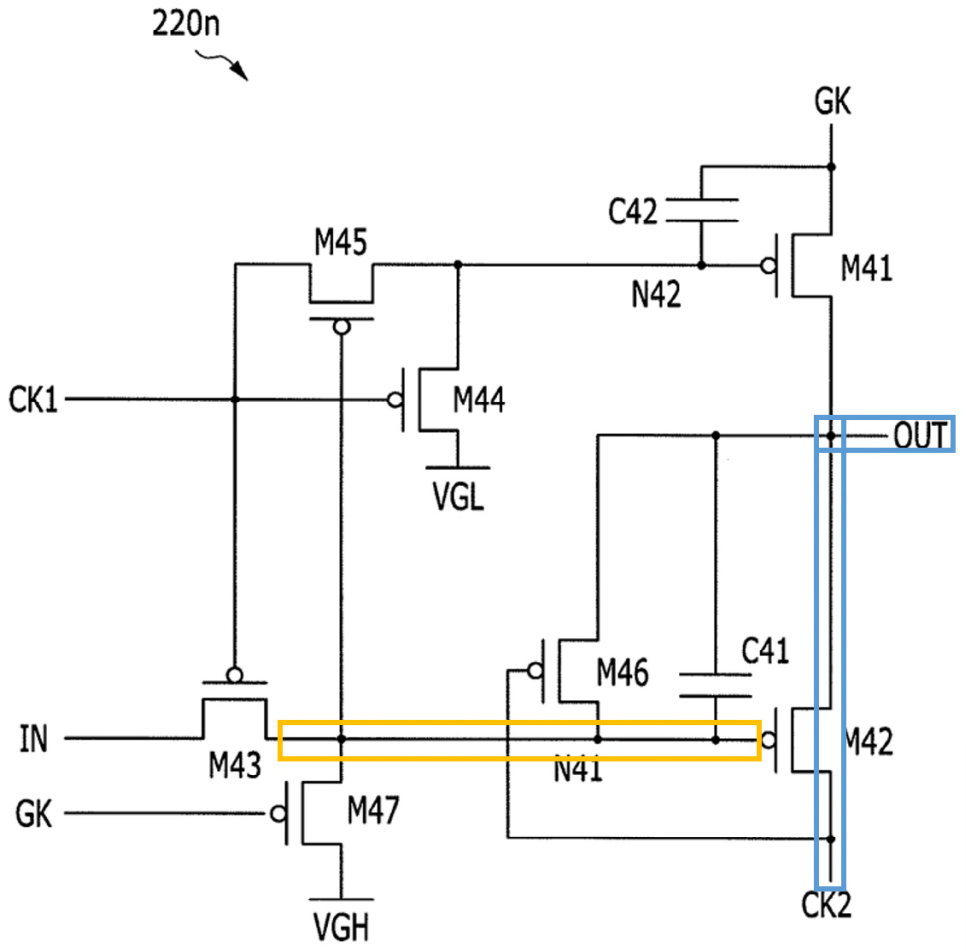
on; this will connect the first power supply voltage at GK to the node of the output terminal ("OUT") – and thus the voltage of the first power supply connection (GK) is supplied to the output terminal ("OUT"). (On the other hand, when a turn-on voltage is not applied at the first node ("N42"), transistor M41 will not turn on – and the voltage of the first power supply connection (GK) is not supplied to the output terminal.)

280. Thus, Kim discloses this claim sub-element of this claim element of Claim 1 of the '593 patent.

iii. [1-a-3]: "and a signal of the third input terminal to the output terminal according to a voltage applied to the second node:"

281. Kim discloses this claim sub-element; this is evident via an annotated version of Figure 9 of Kim:

FIG. 9



As the annotations show, when an appropriate (i.e., turn-on) voltage is applied at the second node (the node labeled "N41"), transistor M42 will turn on; this will connect the signal of the third input terminal ("CK2") to the node of the output terminal ("OUT") – and thus the signal of the third input terminal (CK2) is supplied to the output terminal ("OUT"). (On the other hand, when a turn-on voltage is not applied at the second node ("N41"), transistor M42 will not turn on – and thus the signal of the third input terminal (CK2) in not supplied to the output terminal ("OUT").)

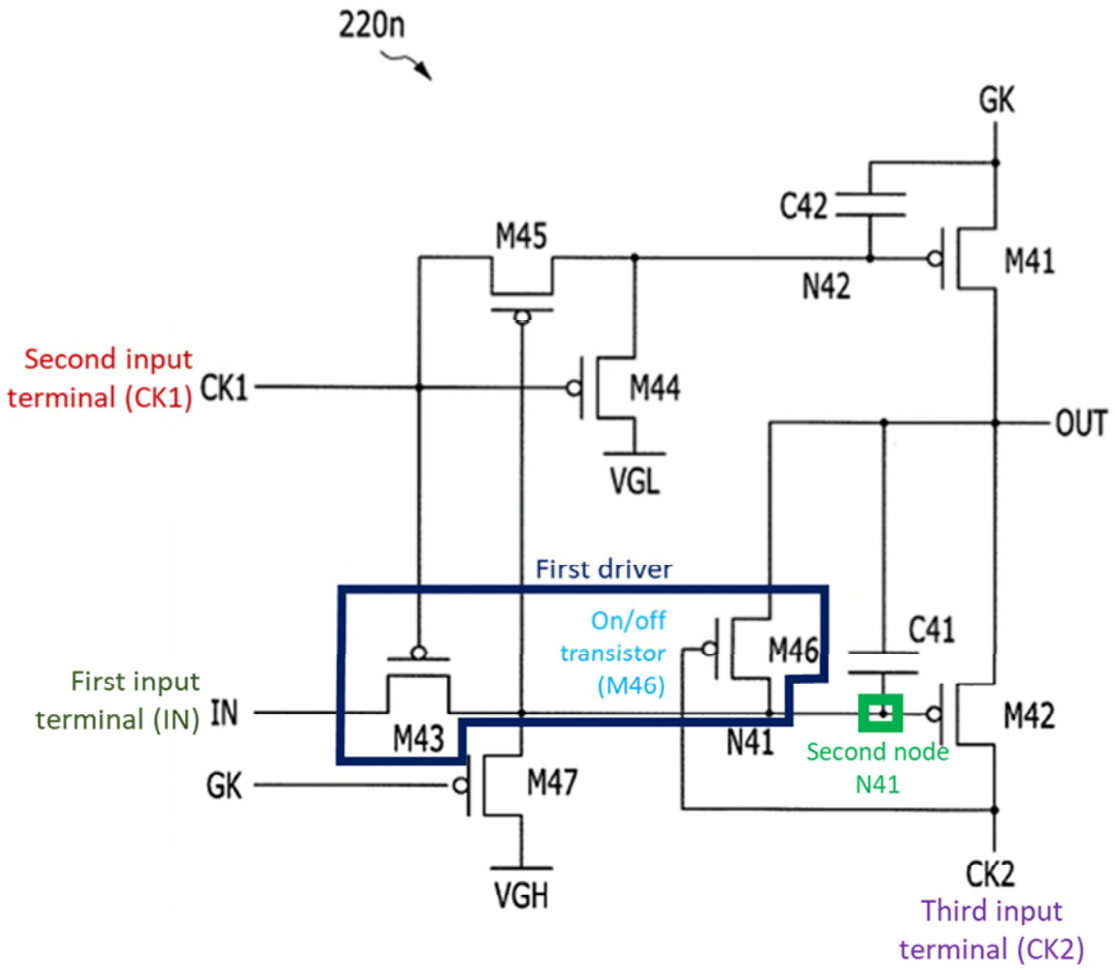
282. Thus, Kim discloses this claim sub-element of this claim element of Claim 1 of the ‘593 patent.

iv. Claim Element [1-a] Summary

283. As just demonstrated, Kim discloses claim sub-elements [1-a-1], [1-a-2], and [1-a-3] of the ‘593 patent; thus, Kim discloses claim element [1-a] of Claim 1 of the ‘593 patent.

c. [1-b]: “a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal; and”

284. Kim discloses this claim element of the ‘593 patent; this is evident via an annotated version of Figure 9 of Kim:



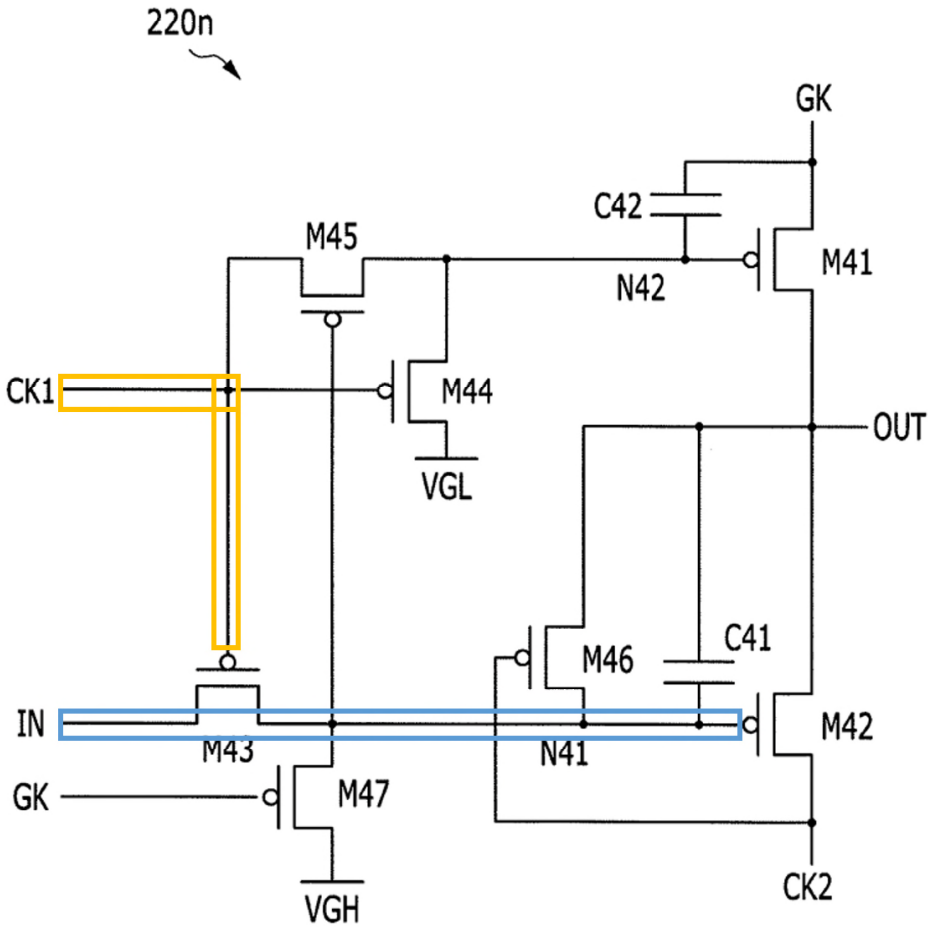
(Annotations added.)

285. In the Kim figure above, the "first driver" is identified using navy blue box-bounding.

286. The voltage on the second node ("N41") is controlled in accordance with the signals of the first input terminal, the second input terminal, and the third input terminal – as shown by the annotations added to the following versions of Figure 9 of Kim. As these annotations show, this functionality is implemented in two separate ways.

287. The first way is implemented as described here.

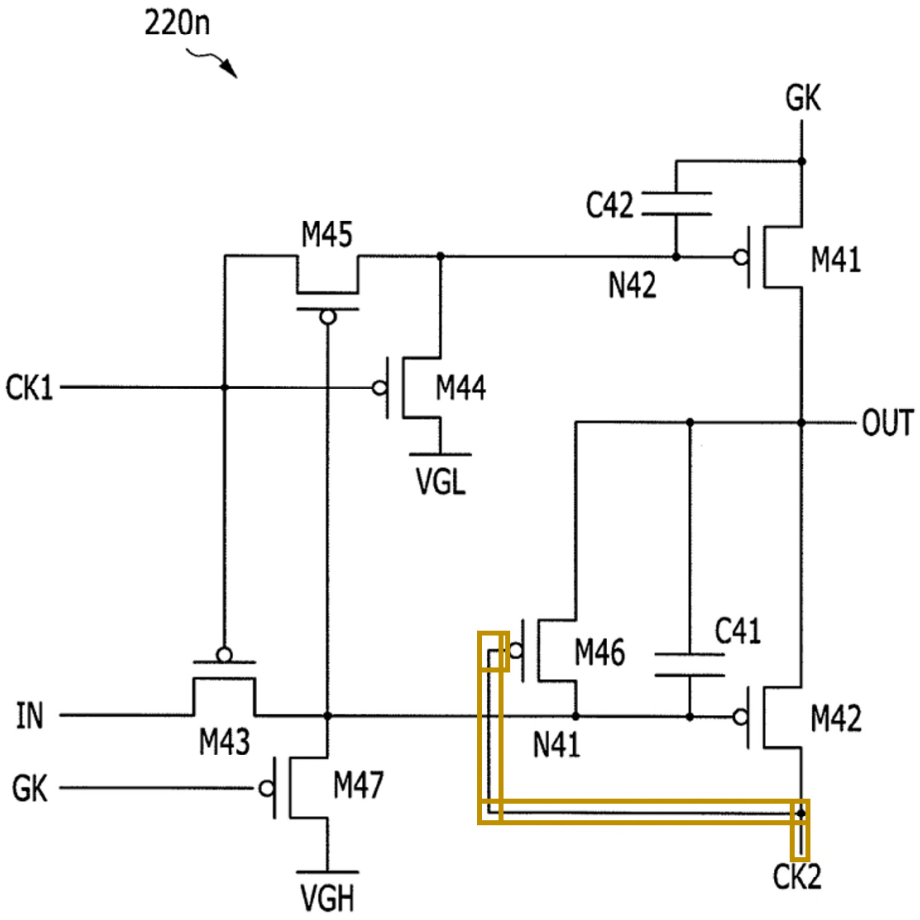
FIG. 9



(Annotations added.) The first way occurs when the second input signal (at CK1) is pulled to a voltage that causes transistor M43 to turn on; when this is done, the content of the input signal at the first input terminal (IN) is supplied to the second node (N41). (On the other hand, when transistor M43 is not turned on, the content of the input signal at the first input terminal (IN) is not supplied to the second node (N41).)

288. The second way will now be described.

FIG. 9



(Annotations added.) As the annotations show, the third input signal (at CK2) is connected directly to the gate of transistor M46, which is part of the first driver.

289. What happens at transistor M46 is described by Kim:

> The sixth transistor M46 is turned on by the second clock signal CLK2 at the logic low level and the logic high level voltage of the output terminal OUT is transferred to the [second] node N41. (Kim at [0184].)

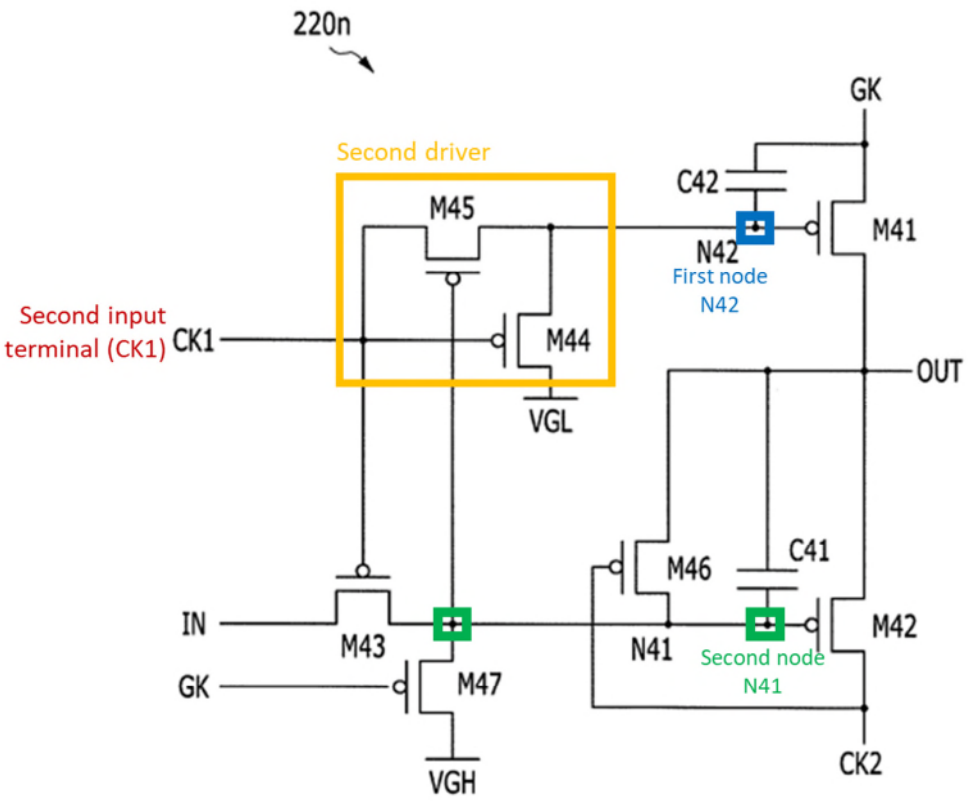
(On the other hand, when transistor M46 is not turned on, the content of the third input signal (at CK2) is not supplied to the second node (N41).) Therefore, the voltage of the second node is controlled in accordance with the signal of the third input terminal.[13]

290. Thus, Kim discloses this claim element of Claim 1 of the '593 patent.

d. [1-c]: "a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, wherein"

291. Kim discloses this claim element of the '593 patent; this is evident via an annotated version of Figure 9 of Kim:

[13] Transistor M47 is always turned off during actual scan periods during which the first power supply GK is always high. Thus, transistor M47 has no effect on the scan operation.

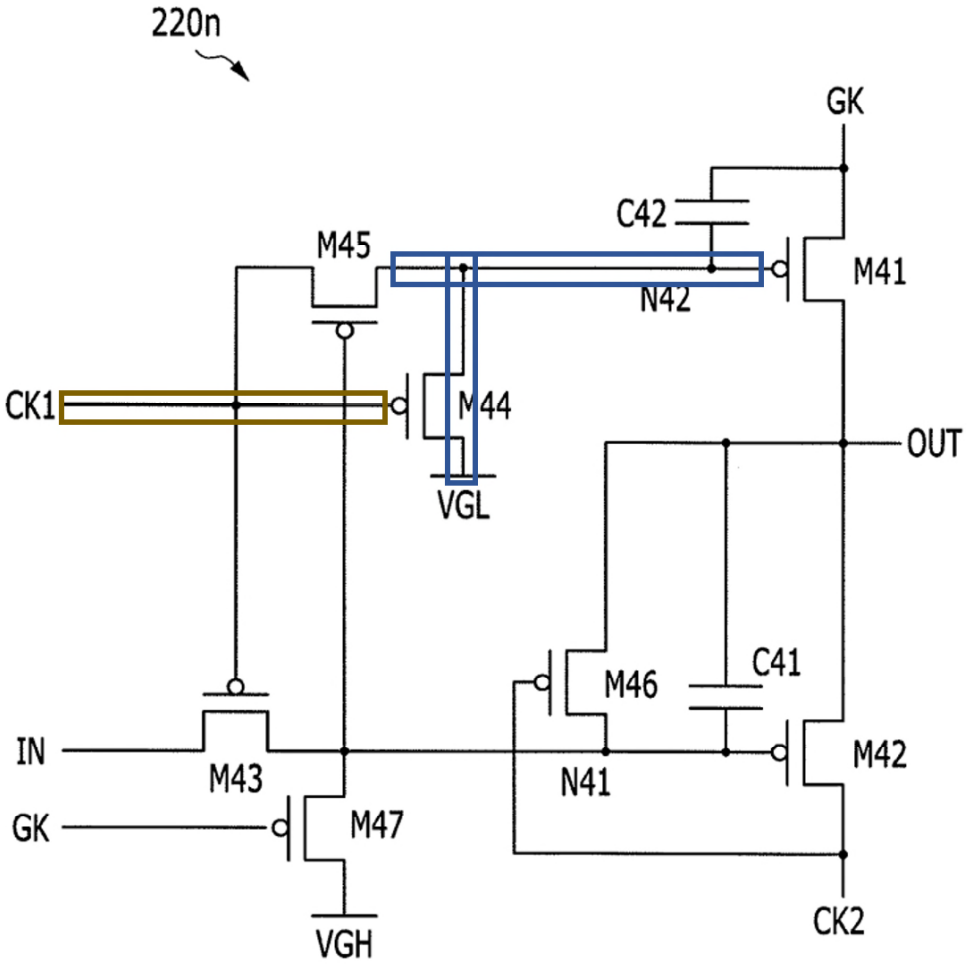


(Annotations added.)

292. In the Kim figure above, the "second driver" is identified using orange box-bounding.

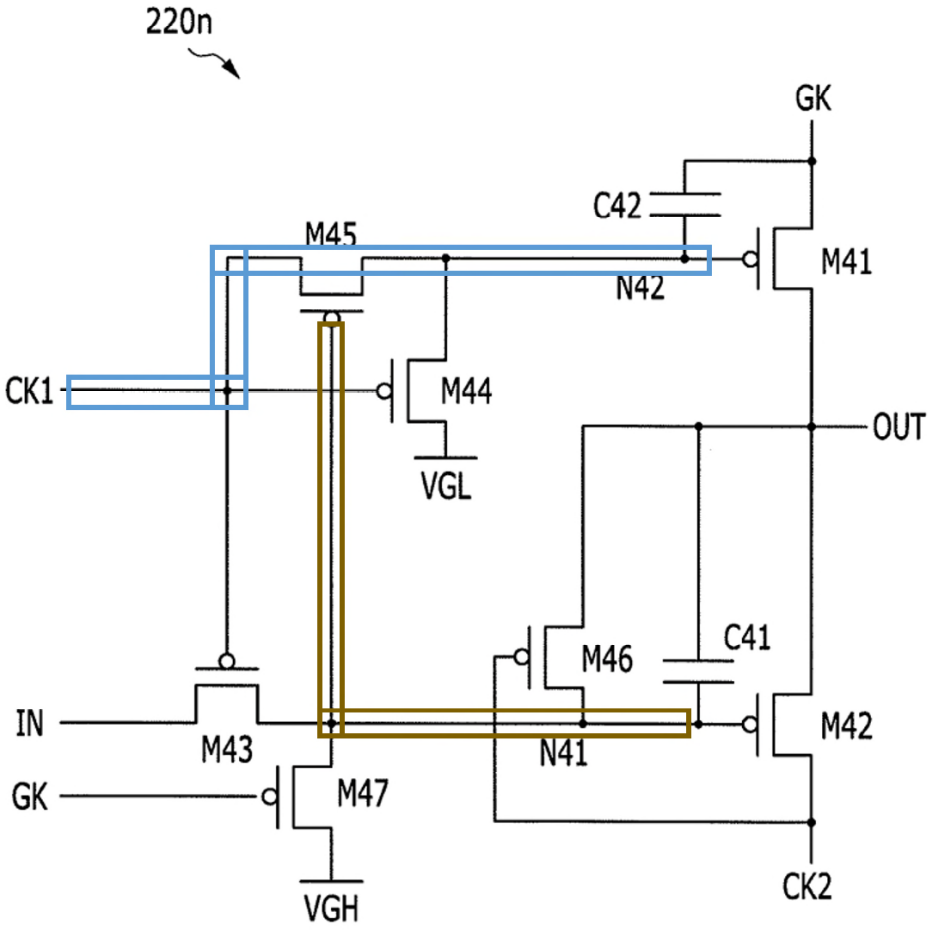
293. The voltage on the first node ("N42") is controlled in accordance with the signal of the second input terminal and the voltage of the second node ("N41") – as shown by the following annotated versions of Figure 9 of Kim.

FIG. 9



294. First, when the signal on the second input terminal (CK1) is pulled low, this will turn on transistor M44; as this transistor is connected directly to the low-logic voltage level (VGL), this will pull the first node (N42) to this low voltage. (When the signal on the second input terminal (CK1) is pulled high, transistor M44 is turned off – and this functionality is not available).

FIG. 9

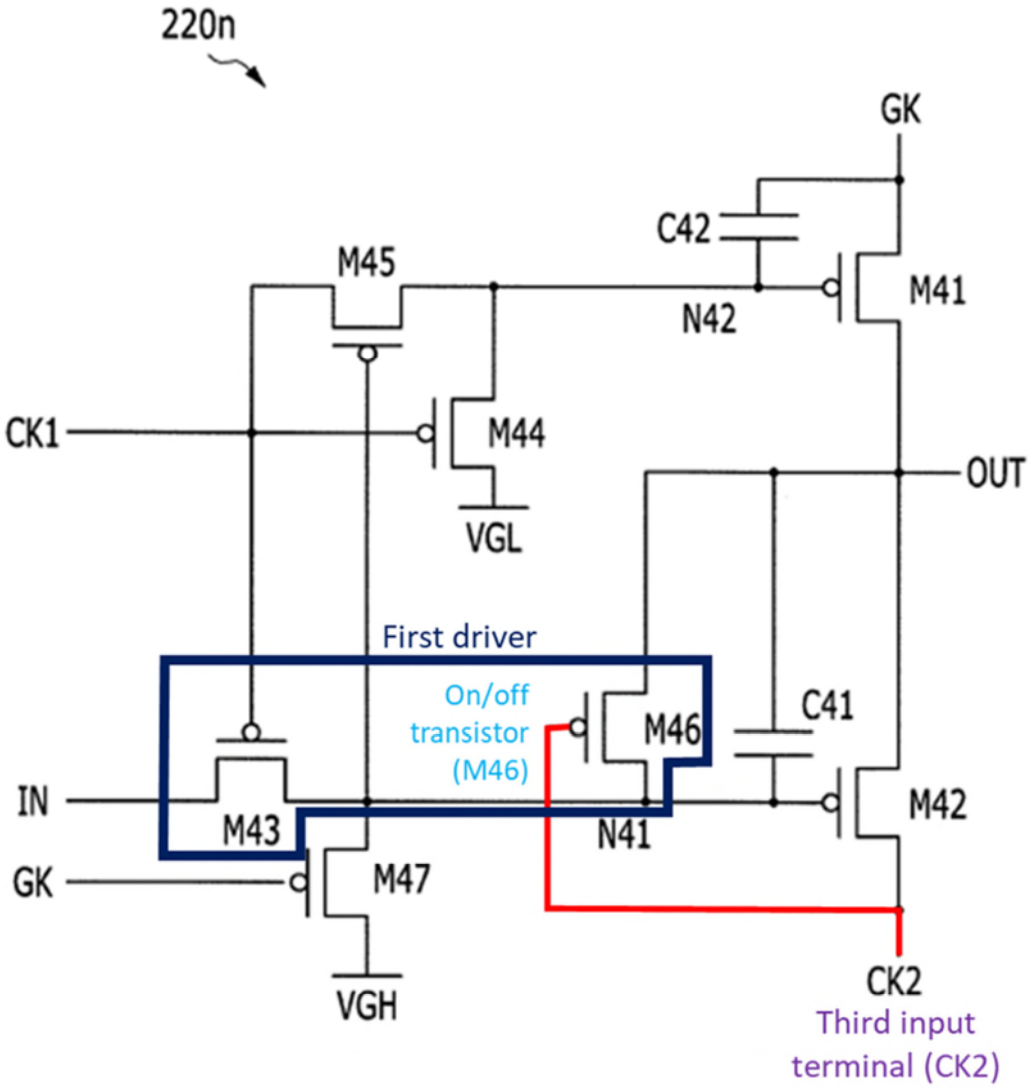


295. Second, when the second node (N41) has a low voltage value, the transistor M45 will be turned on; this will transfer the signal on the second input terminal (CK1) to the first node (N42). (When the second node (N41) has a high voltage value, transistor M45 will be turned off – and this functionality will not be available).

296. Thus, Kim discloses this claim element of Claim 1 of the '593 patent.

e. [1-d]: "the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver."

297. Kim discloses this claim element of the '593 patent; this is evident via annotated versions of Figure 9 of Kim:



(Annotations added.) As the annotations show, the third input signal ("CK2") is (among other things) connected directly to the gate of transistor M46, which is part

of the first driver; thus, the third input signal directly controls the on/off operation of a transistor that is included in the first driver.

298. Thus, Kim discloses this claim element of Claim 1 of the '593 patent.

f. Claim 1 Summary

299. As just shown, Kim discloses each element of Claim 1 of the '593 patent; thus, Kim anticipates Claim 1 of the '593 patent.

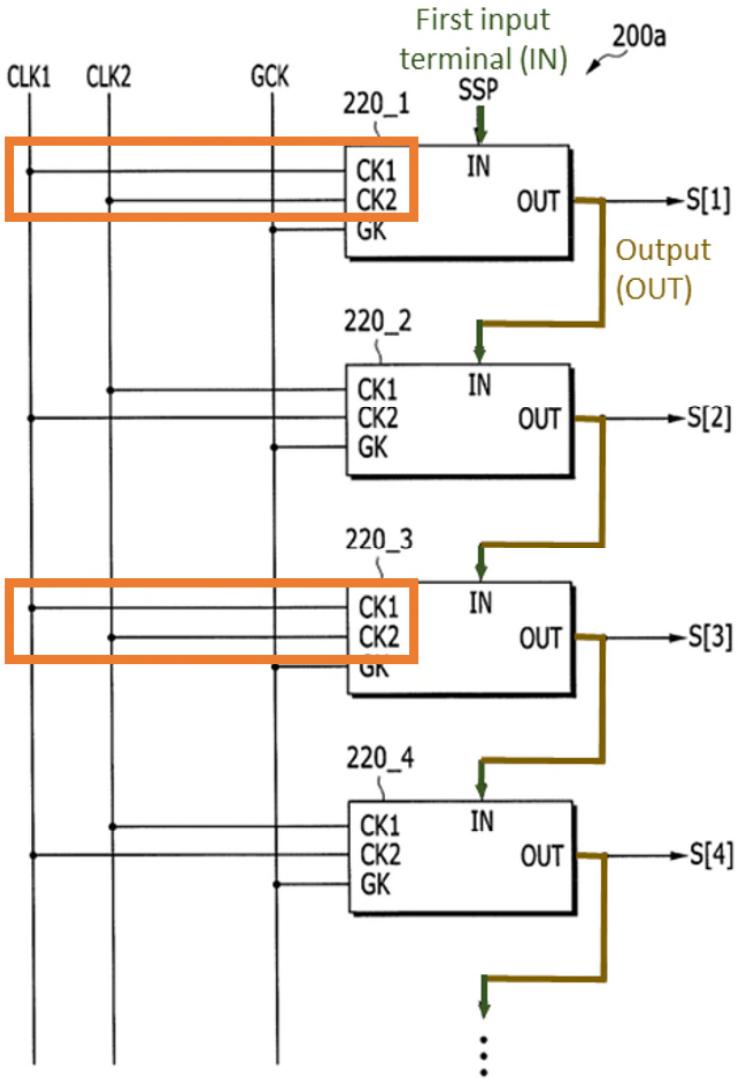
2. Dependent Claim 2

300. As an initial matter, Claim 2 depends from Claim 1; as was shown above, Claim 1 of the '593 patent is disclosed by Kim.

301. Claim 2 further requires that "wherein the first input terminal receives an output signal of a previous stage circuit or a start signal, wherein the second input terminal receives a first clock signal, and wherein the third input terminal receives a second clock signal." Kim discloses this claim of the '593 patent.

302. It was shown above (in Section XII.B.1.a) that the first input terminal can receive a start signal, the second input terminal receives a first clock signal, and the third input terminal receives a second clock signal. Claim 2 adds that the first input terminal can also receive an output signal of a previous stage circuit; this is disclosed in Kim – as an annotated version of Figure 8 from Kim makes clear.

FIG. 8



(Annotations added.) As can be seen from examination of this annotated figure, the first stage circuit block (220_1) receives a start signal (SSP) at its first input terminal, while subsequent stage circuit blocks (220_2, 220_3, 220_4…) receive an output signal of a previous stage circuit block at the first input terminal. Note in particular that the third stage circuit block (220_3), like the first stage circuit block (220_1), is

configured so that the second input terminal receives a first clock signal and the third input terminal receives a second clock signal.

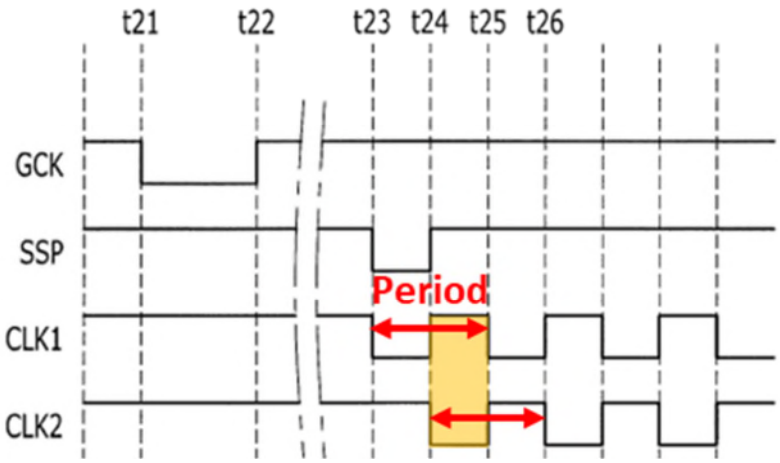
303. Thus, Kim anticipates Claim 2 of the '593 patent.

3. Dependent Claim 3

304. As an initial matter, Claim 3 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the '593 patent are disclosed by Kim.

305. Claim 3 further requires that "wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap." Kim discloses this claim of the '593 patent – as is evident from examination of an annotated version of Figure 10 from Kim.

FIG. 10



(Annotations added.) It is well-known in the art that the "period" of a recurring waveform is defined as the amount of time that passes before the waveform repeats itself; the annotations added to Figure 10 of Kim identify the period of the first clock signal (CLK1) and the period of the second clock signal (CLK2). As is evident from inspection of this figure, the period of the first clock signal (CLK1) and the second clock signal (CLK2) are the same.

306. Claim 3 also requires that the two clock signal waveforms "have phases that do not overlap." At a minimum, it is well-known in the art that the term "phase" (with regard to a recurring waveform) is used to describe specifically when (in time) the waveform reaches some identified point along its single-period form; this is of particular importance when referring to how a particular recurring waveform might be shifted in time ("changing the phase"), or (more commonly and more importantly) when two otherwise-identical recurring waveforms are offset from each other (in time). When two otherwise-identical recurring waveforms are offset from each other (in time), it is said that the two waveforms are "out of phase" (to contrast from *not* being offset in time, where they would be "in phase") – and the specific amount of the offset difference between the two waveforms is known as the "phase difference." As examination of Figure 10 of Kim clearly shows that the first clock signal (CLK1) and the second clock signal (CLK2) are out of phase with each other – and thus, their phases do not overlap.

307. Further, note that these two signals are digital waveforms – that is, they are square waves that have only one of two signal states – high or low. With digital waveforms, the term "phases that do not overlap" is known in the art as meaning that the two waveforms will not both be in their turn-on state, e.g., logic low for pMOS-based circuits and logic high for nMOS-based circuits, respectively, at the same time.

308. Thus, Kim anticipates Claim 3 of the '593 patent.

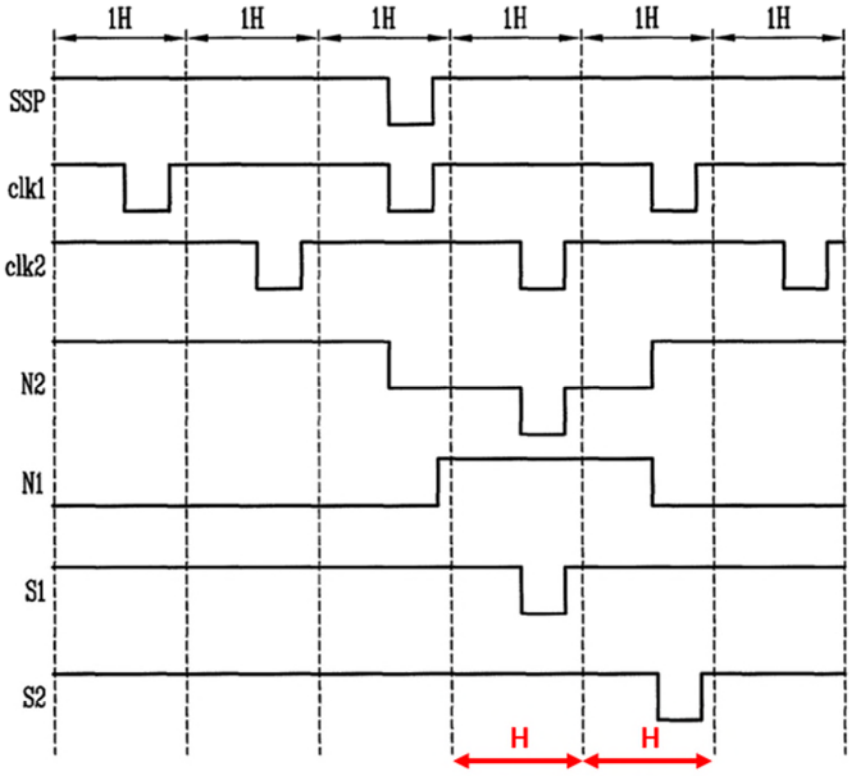
4. Dependent Claim 4

309. As an initial matter, Claim 4 depends from Claim 3, which depends from Claim 2, which depends from Claim 1; as was shown above, Claim 1, Claim 2, and Claim 3 of the '593 patent are disclosed by Kim.

310. Claim 4 further requires "wherein the first clock signal and the second clock signal have a period equal to two horizontal periods 2H and are supplied in different horizontal periods as low signals." The language in this claim may be somewhat confusing – as the word "period" appears three times but the word clearly carries two different meanings depending on the usage.

311. The first instance of "period" is described via "the first clock signal and the second clock signal have a period"; this "period" is of the form described above with respect to Claim 3, in which "period" refers to the amount it takes for a recurring waveform to repeat itself.

312. The second instance of "period" occurs twice later in the claim, and refers (in both usages) to "horizontal periods"; this "period" refers to a particular amount of time (as in "a period of time"), and not to the repetition of a recurring waveform. More specifically, the '593 patent refers to "a period in which a scan signal is supplied to one scan line" as an exemplary horizontal period. ('593 patent, 5:18-20.) This period corresponds to the time span between outputs of successive stages, e.g., between S1 and S2, as shown in the annotated version of '593 patent Figure 4:



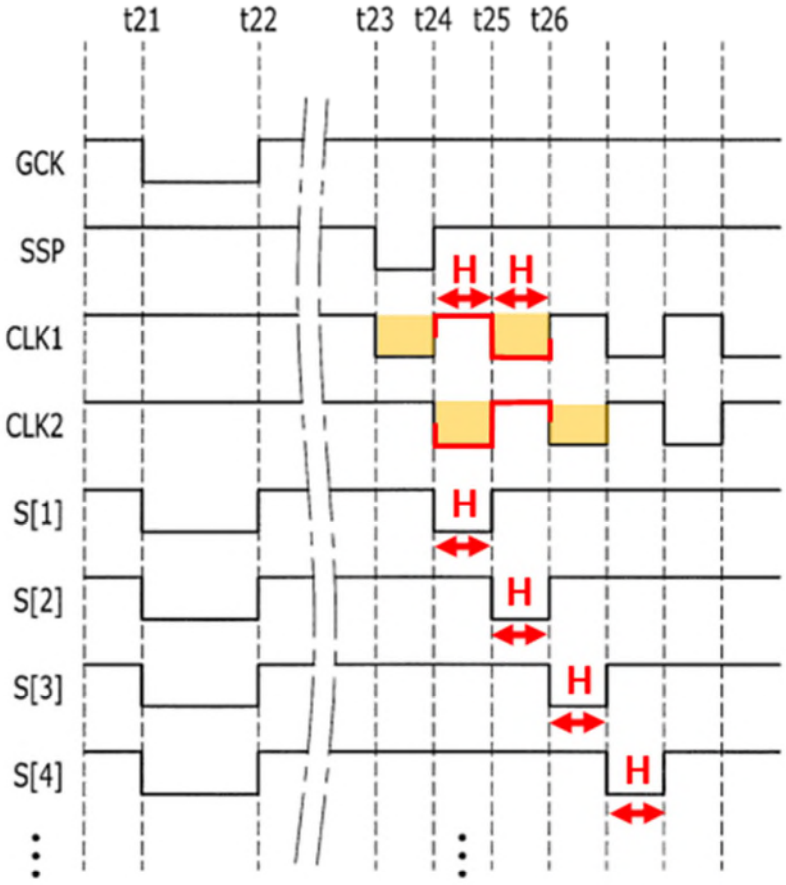
313. Thus, the claim basically states that the amount of time of the period of the recurring waveforms (the first clock signal and the second clock signal) is twice as long as two sub-periods ("H") that, in sum, are the length (in time) of the time it

takes for the recurring waveform to repeat itself. Further, the claim states that these sub-periods sum to "2H" – which means that each sub-period has a duration of H, so that the duration of the two sub-periods is the same.

314. The final stipulation of Claim 4 is that the first clock signal and the second clock signal are "supplied in different horizontal periods as low signals." As the '593 patent uses pMOS transistors in its circuitry, low signals will be the turn-on voltage level for the transistors used in the circuitry in the '593 patent. So, essentially, this requirement is the same as the one discussed above with respect to Claim 3 and "phases that do not overlap." As Kim also uses pMOS transistors in its circuitry, the same condition (low signals are transistor turn-on signals) is disclosed in Kim.

315. That Kim discloses this claim element of the '593 patent can readily be seen via an annotated version of Figure 10 of Kim.

FIG. 10



The first clock signal (CLK1) and the second clock signal (CLK2) have two sub-periods of equal duration H – so that the total period of the recurring waveforms of CLK1 and CLK2) is 2H. Further, the first clock signal (CLK1) is high when the second clock signal (CLK2) is low, and vice versa. Thus, the first clock signal and the second clock signal are supplied in different horizontal periods as low signals.

316. Thus, Kim anticipates this claim of the '593 patent.

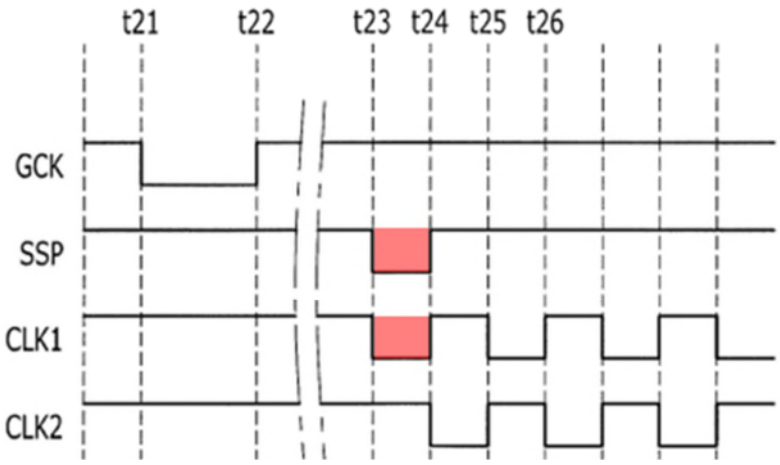
5. Dependent Claim 5

317. As an initial matter, Claim 5 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the '593 patent are disclosed by Kim.

318. Claim 5 further requires that "the start signal is supplied to overlap the first clock signal."

319. This can be readily seen via an annotated version of Figure 10 of Kim.

FIG. 10



As can be seen, the start signal (SSP) goes low (its "active" level) at the same time and for the same duration that the first clock signal (CLK1) goes low (also its "active" level) as part of its recurring square wave behavior. Thus, the start signal (SSP) overlaps the first clock signal (CLK1).

320. Thus, Kim anticipates this claim of the '593 patent.

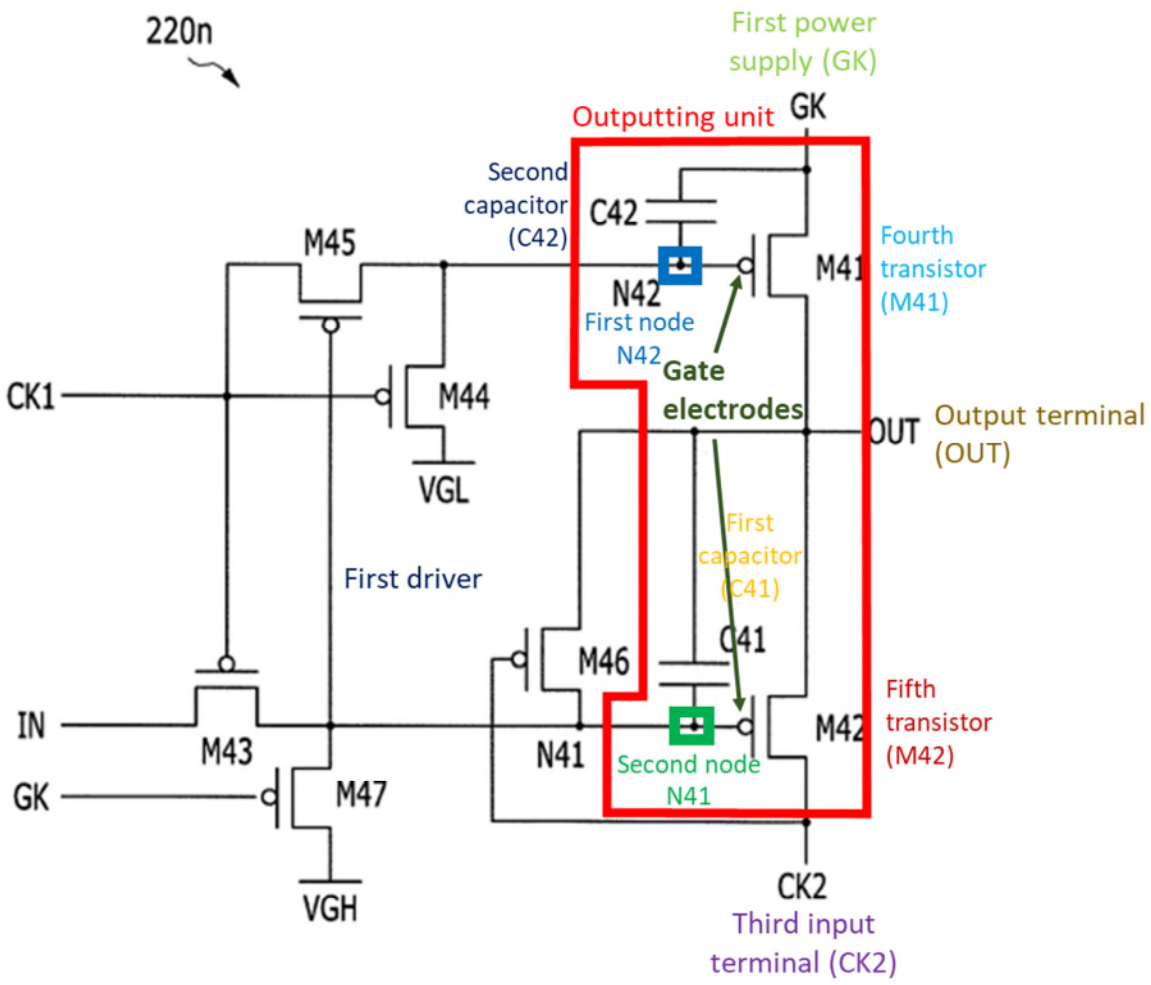
6. Dependent Claim 7

321. As an initial matter, Claim 7 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the '593 patent are disclosed by Kim.

322. Claim 7 further requires that "the outputting unit includes: a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node: a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node, a first capacitor between the second node and the output terminal; and a second capacitor between the first node and the first power supply."

323. This is a verbal form of a topological description of circuitry – which describes the components of the described circuitry, the terminals of those components, and the way that the various terminals of the various components are connected together.

324. How this topological description reads on Kim is best described via an annotated version of Figure 9 of Kim.



(Annotations added.) As the annotations show, the description of the circuit topology in the claim is found, element for element, in Kim.

325. Thus, Kim anticipates this claim of the '593 patent.

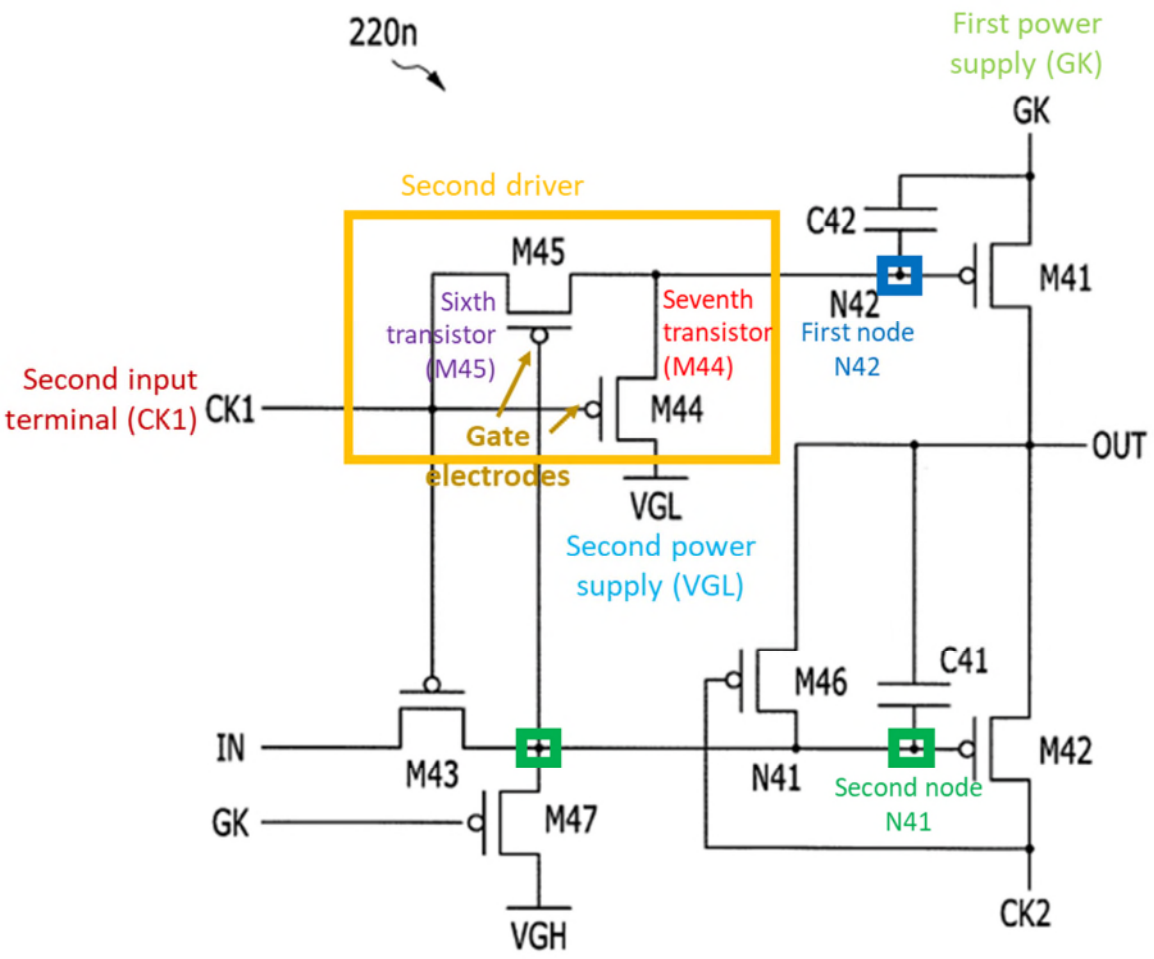
7. Dependent Claim 8

326. As an initial matter, Claim 8 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the '593 patent are disclosed by Kim.

327. Claim 8 further requires that "the second driver includes: a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal."

328. Once again, this is a verbal form of a topological description of circuitry – and once again, how this topological description reads on Kim is best described via an annotated version of Figure 9 of Kim.

Mianyang BOE Ex. 1003
Case No. IPR2023-01221
Page 143 of 273



(Annotations added.) As the annotations show, the description of the circuit topology in the claim is found, element for element, in Kim.

329. Thus, Kim anticipates this claim of the '593 patent.

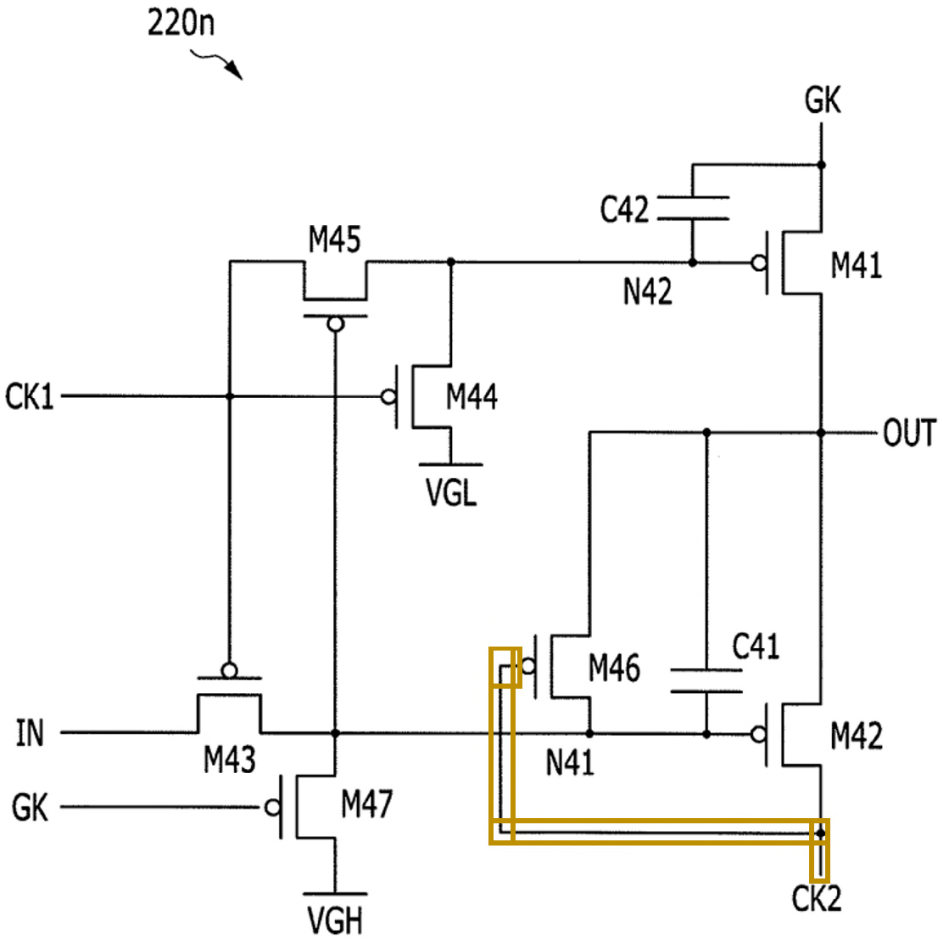
8. Dependent Claim 14

330. As an initial matter, Claim 14 depends from Claim 1; as was shown above, Claim 1 of the '593 patent is disclosed by Kim.

331. Claim 14 further requires that "the transistor controls the voltage of the second node according to the on/off operation thereof." Claim 14 does not provide

details regarding which transistor is "the" transistor being described here; however, Claim 1 makes reference to only one transistor – in claim element [1-d] (which was described in Section XII.B.1.e), where this transistor was identified in the claim element via "the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver." In Section XII.B.1.e, that transistor was specifically identified as transistor M46, via an annotated version of Figure 9 of Kim – which is reprised here.

FIG. 9



(Annotations added.) As the annotations show, the third input signal (at CK2) is (among other things) connected directly to the gate of transistor M46, which is part of the first driver; thus, the third input signal directly controls the on/off operation of a transistor (specifically, transistor M46) that is included in the first driver.

332. What happens at transistor M46 is described by Kim:

> The sixth transistor M46 is turned on by the second clock signal CLK2 at the logic low level and the logic high level voltage of the output terminal OUT is transferred to the [second] node N41. (Kim at [0184].)

Therefore, the transistor M46 controls the voltage of the second node.

333. Thus, Kim anticipates this claim of the '593 patent.

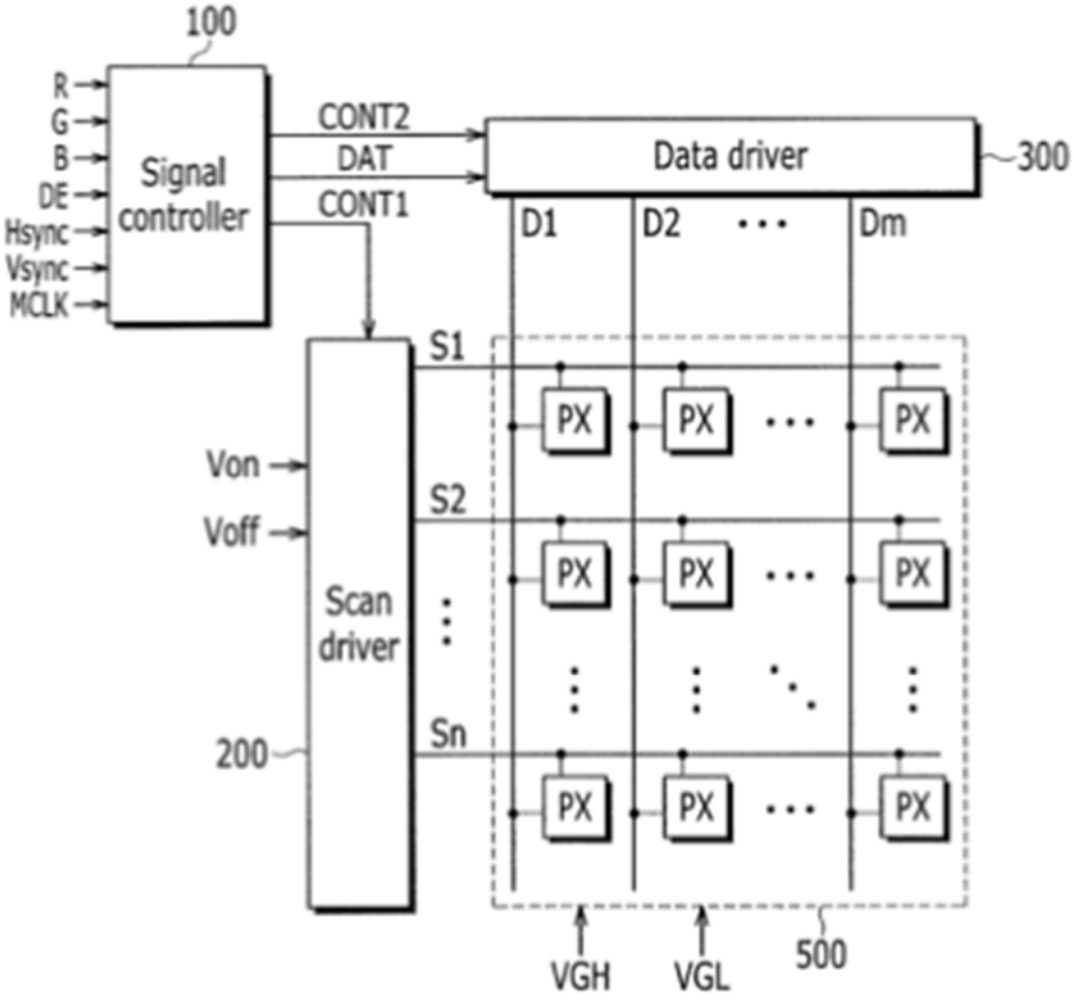
9. Independent Claim 15

334. It is my conclusion and opinion that Claim 15 of the '593 patent is anticipated by Kim.

a. [15-pre]: "An organic light emitting display, comprising:"

335. As an initial matter, I will be offering no opinion regarding whether or not the preamble of Claim 15 is limiting. I have been instructed by counsel for Petitioner to offer an opinion as to whether or not the prior art discloses the preamble, regardless of whether or not the preamble is limiting.

336. Kim discloses the preamble of Claim 15 of the '593 patent. First, Kim discloses in Figure 1 (a figure that will be discussed in more detail below) a diagram of an apparatus that is a display.



Given that Kim refers multiple times (at [0073], [0075], [0076], and [0080]) to the "PX" elements as being pixels, a POSITA would have understood that Figure 1 of Kim is describing a display. Further, Kim describes the exemplary embodiment at [0082] as: "an exemplary embodiment of a display device, e.g., an organic light emitting diode display using an organic light emitting diode."

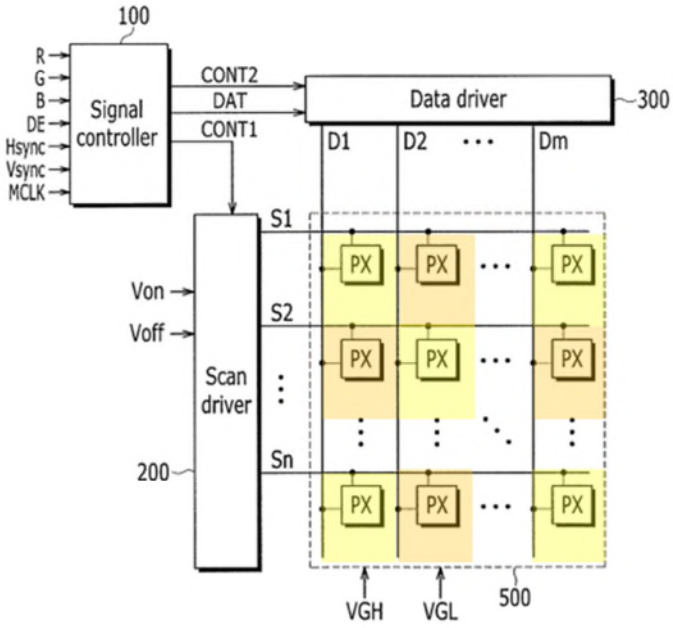
337. Thus, Kim discloses the preamble of Claim 15 of the '593 patent.

b. [15-a]: "pixels positioned in regions partitioned by scan lines and data lines;"

338. Kim discloses this claim element of Claim 15 of the '593 patent.

339. This can readily be seen via an annotated version of Figure 1 of Kim.

FIG. 1



(Annotations added.) As noted above, Kim identifies the "PX" elements as pixels. Further, Kim notes the general presence of scan lines and data lines at [0005] ("In a panel display, scan signals having a gate-on voltage are sequentially applied to a plurality of scan lines and data signals corresponding to the scan signals and having a gate-on voltage are applied to a plurality of data lines, in order to display a video."), and more specifically at e.g. [0075], where the related details in Figure 1 of Kim are explained ("The display unit 500 includes a plurality of pixels PX which are

connected to a plurality of scan lines S1-Sn, a plurality of data lines D1-Dm. The plurality of signal lines S1-Sn and the plurality of data lines D1-Dm may be arranged in a substantially matrix form.").

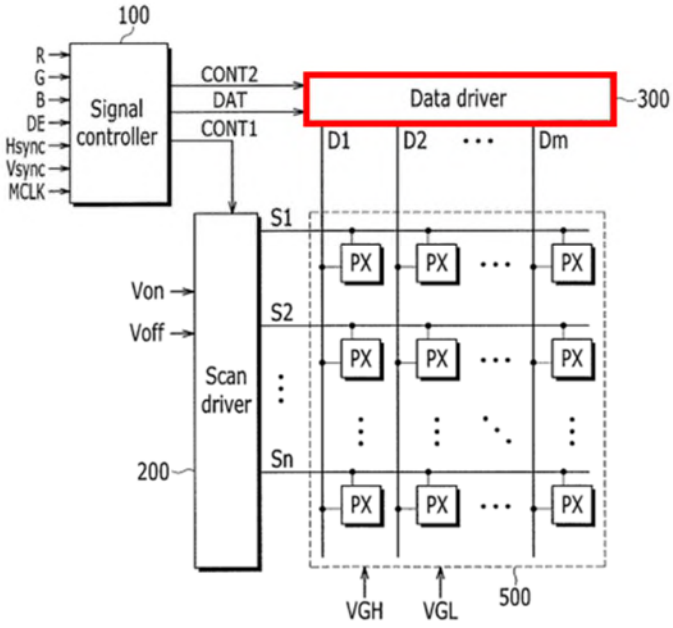
340. Thus, Kim discloses this claim element of Claim 15 of the '593 patent.

c. [15-b]: "a data driver for supplying data signals to the pixels through the data lines; and"

341. Kim discloses this claim element of Claim 15 of the '593 patent.

342. This can be readily seen by further examination of Figure 1 of Kim.

FIG. 1



(Annotations added.) The presence of a data driver is explicitly depicted as such in Figure 1 of Kim; further, the data driver is described explicitly (by name) at, e.g., [0074], [0075], and [0078] of Kim. As noted above, the lines labeled D1, D2 … Dm

are described in Kim as being data lines (at, e.g., [0075]), which provide data signals to the pixels (PXs).

343. Thus, Kim discloses this claim element of Claim 15 of the '593 patent.

d. [15-c]: "a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal,"

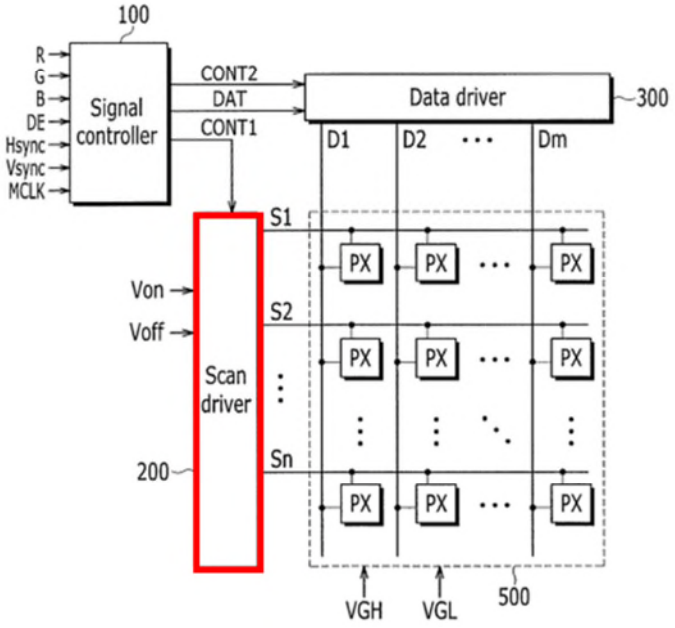
344. Claim element [15-c] is rather long – and thus the analysis will be simpler to explain if this claim element is broken up into sub-elements.

i. [15-c-1]: "a scan driver for supplying scan signals to the pixels through the scan lines"

345. Kim discloses this claim sub-element of claim element [15-c] of Claim 15 of the '593 patent.

346. This can be readily seen by further examination of Figure 1 of Kim.

FIG. 1



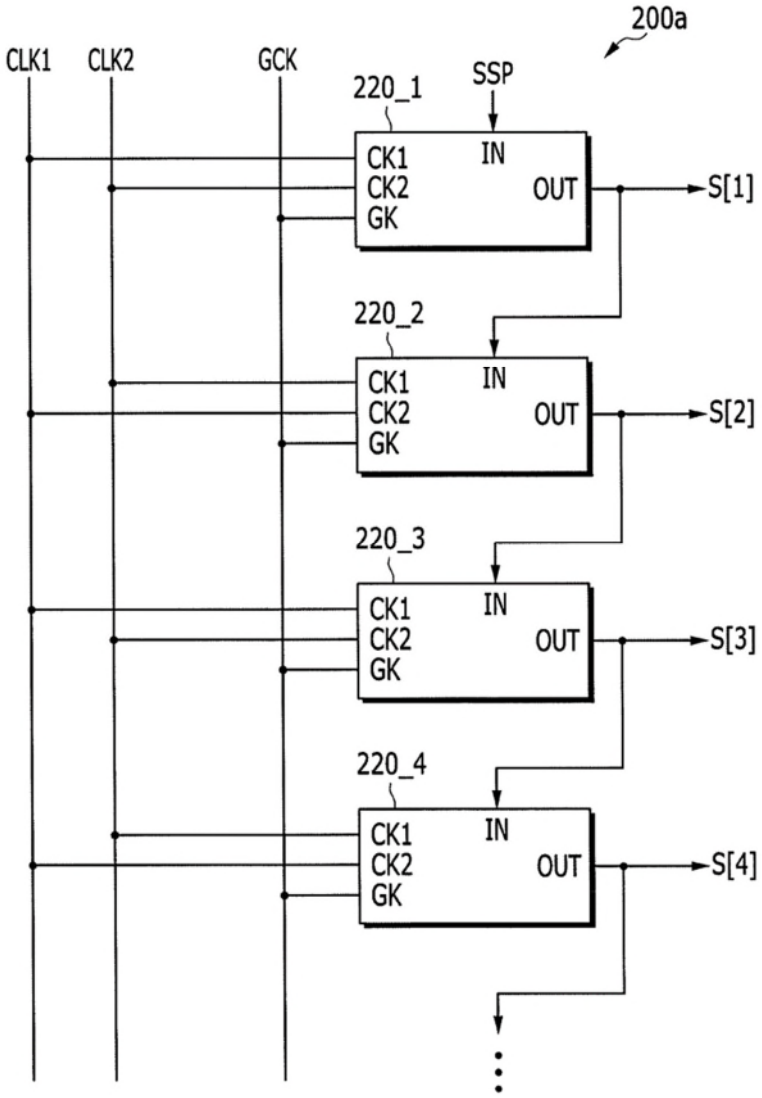
(Annotations added.) The presence a scan driver is explicitly depicted as such in Figure 1 of Kim; further, the scan driver is described explicitly (by name) at, e.g., [0074] and [0076] of Kim. At [0075] and [0076], Kim identifies the lines labeled S1, S2 … Sn as being scan lines (at, e.g., [0075]), which provide scan signals to the pixels (PXs).

347. Thus, Kim discloses this claim sub-element of claim element [15-c] of Claim 15 of the '593 patent.

ii. [15-c-2]: "the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals"

348. Kim discloses this claim sub-element of claim element [15-c] of Claim 15 of the '593 patent.

349. Kim describes the inner details of the scan driver in Figure 8.



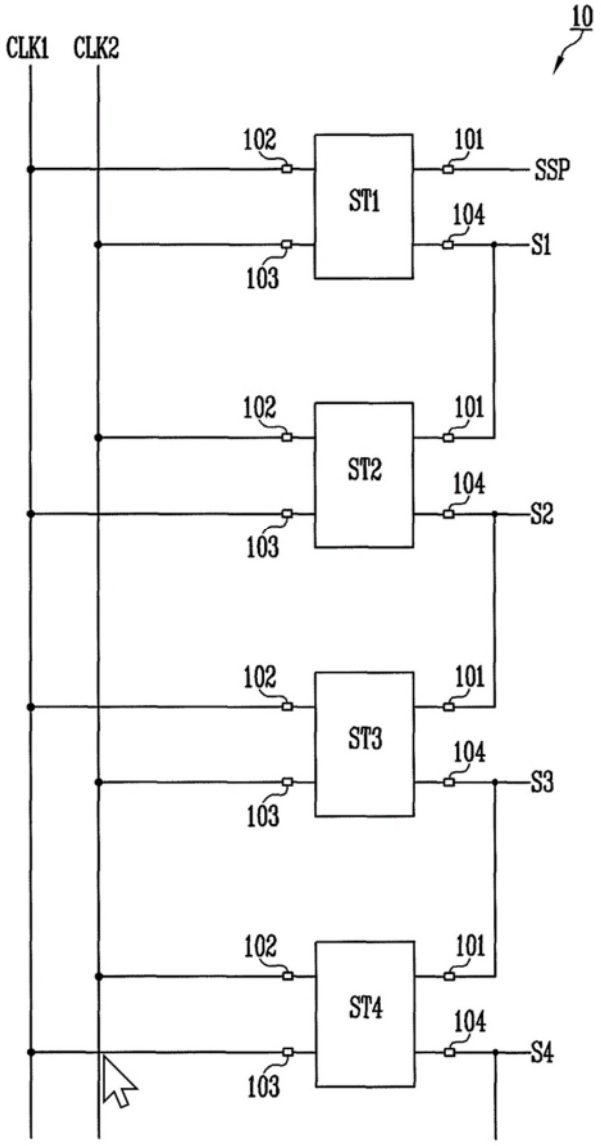
The functional details of this circuitry are explained in Kim at [0153]:

> Referring to FIG. 8, the scan driver 200a includes a plurality of scan driving blocks 220_1, 220_2, 220_3,220_4, ... that arranged sequentially. The scan driving blocks 220_1, 220_2, 220_3, 220_4, ... generate scan signals S[1], S[2], S[3], S[4], ... transferred to a

plurality of scan lines S1 to Sn by receiving input signals, respectively.

The “scan driving blocks” of Kim are the “stage circuits” of the ‘593 patent; the “stage circuits” of the ‘593 patent are so-called because they are arranged in a cascade, where the output of one stage is supplied as input to the next stage – as is depicted in Figure 2 of the ‘593 patent:

FIG. 2



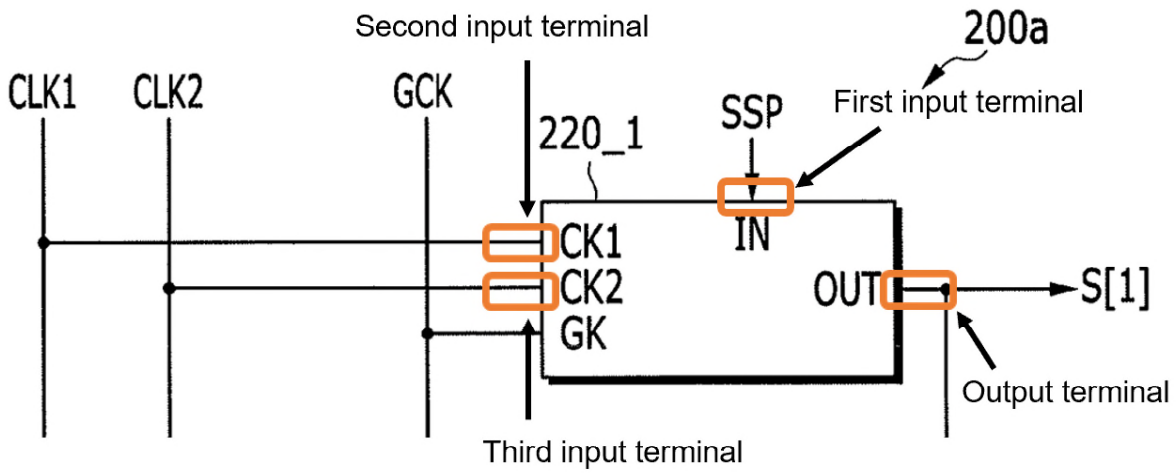
The output signal of each stage circuit is supplied as an input to the next stage – and the stage circuits are thus arranged in a cascade of such stage circuits. This is what is described in Kim – and the strong similarity between Figure 8 of Kim and Figure 2 of the '593 patent confirms this.

350. Thus, Kim discloses this claim sub-element of claim element [15-c] of Claim 15 of the '593 patent.

iii. [15-c-3]: "and having a first input terminal, a second input terminal, a third input terminal, and an output terminal,"

351. This claim sub-element of claim element [15-c] of Claim 15 of the '593 patent is disclosed by Kim.

352. The claim sub-element is essentially identical to the preamble of Claim 1 of the '593 patent – which was already discussed in detail earlier (at Section XII.B.1.a) – where it was shown that these details are disclosed by Kim. An annotated figure (Figure 8 from Kim) from Section XII.B.1.a can be repeated here to reinforce the point.



(Annotations added.)

353. Thus, Kim discloses this claim sub-element of claim element [15-c] of Claim 15 of the '593 patent.

iv. Claim Element [15-c] Summary

354. As just demonstrated, Kim discloses claim sub-elements [15-c-1], [15-c-2], and [15-c-3] of the '593 patent; thus, Kim discloses claim element [15-c] of Claim 15 of the '593 patent.

e. Preface to claim elements [15-d] – [15-g]

355. Between claim element [15-c] and claim element [15-d], Claim 15 includes the phrase "wherein each of the stage circuits includes:". It is taken here that this is intended to mean that "includes" is stated with regard to the sequential list of claim elements which follow for the remainder of Claim 15 – that is, claim

elements [15-d], [15-e], [15-f], and [15-g]. Each of these claim elements will be considered in turn.

f. [15-d]: "an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node,"

356. This claim element is identical to claim element [1-a] of Claim 1 of the '593 patent – which was discussed earlier (in Section XII.B.1.b).

357. Thus, Kim discloses this claim element of Claim 15 of the '593 patent.

g. [15-e]: "a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal, and"

358. This claim element is identical to claim element [1-b] of Claim 1 of the '593 patent – which was discussed earlier (in Section XII.B.1.c).

359. Thus, Kim discloses this claim element of Claim 15 of the '593 patent.

h. [15-f]: "a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, wherein"

360. This claim element is identical to claim element [1-c] of Claim 1 of the '593 patent – which was discussed earlier (in Section XII.B.1.d).

361. Thus, Kim discloses this claim element of Claim 15 of the '593 patent.

i. [15-g]: "the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver."

362. This claim element is identical to claim element [1-d] of Claim 1 of the '593 patent – which was discussed earlier (in Section XII.B.1.e).

363. Thus, Kim discloses this claim element of Claim 15 of the '593 patent.

j. Claim 15 Summary

364. As just shown, Kim discloses each element of Claim 15 of the '593 patent; thus, Kim anticipates Claim 15 of the '593 patent.

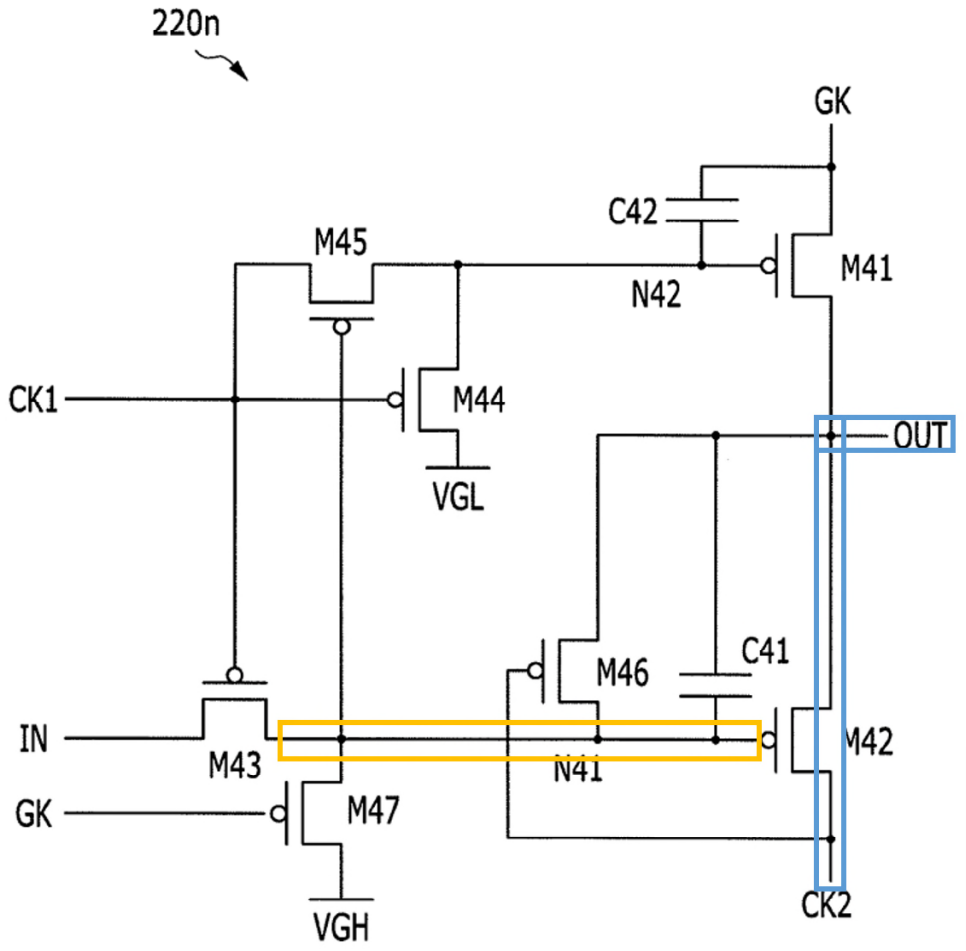
10. Dependent Claim 16

365. As an initial matter, Claim 16 depends from Claim 15; as was shown above, Claim 15 of the '593 patent is disclosed by Kim.

366. Claim 16 further requires "a clock signal supplied to the third input terminal is used as the scan signal." Kim discloses this claim of the '593 patent.

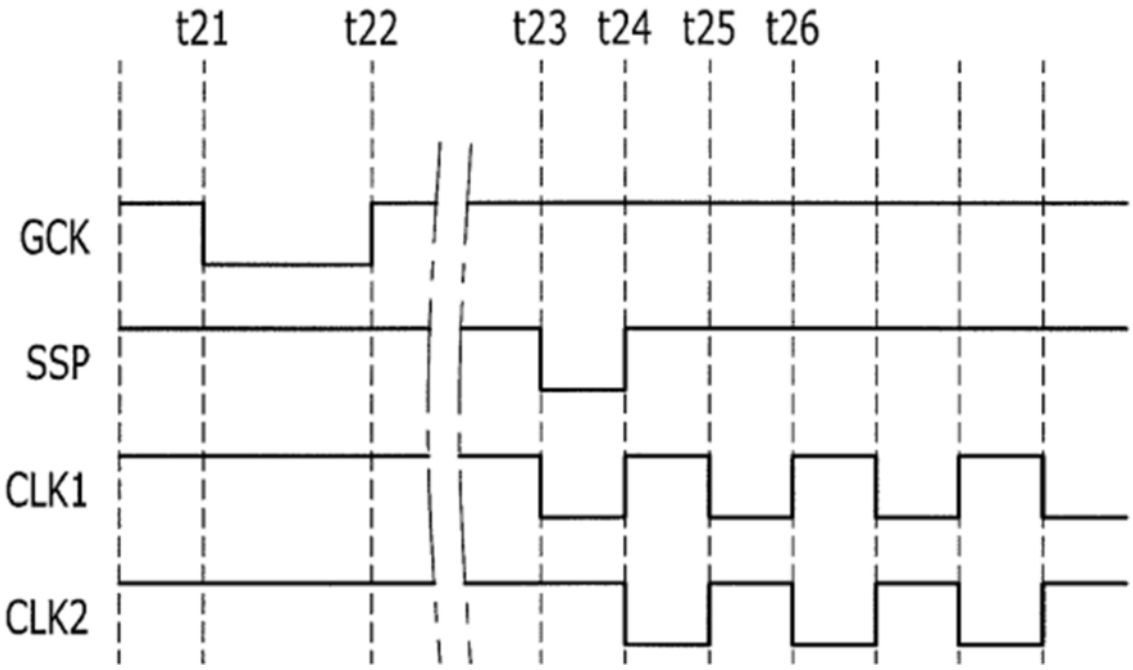
367. The first part of this claim element ("a clock signal supplied to the third input terminal") was already discussed earlier (in Section XII.B.1.b.iii) – with respect to claim sub-element [1-a-3] of claim element [1-a] of Claim 1 of the '593 patent. An annotated version of Figure 9 of Kim was provided there for purposes of explanation – and for clarity, that figure will be repeated here.

FIG. 9



As detailed in Section XII.B.1.b.iii, when an appropriate (i.e., turn-on) voltage is applied at the second node (the node labeled "N41"), transistor M42 will turn on; this will connect the signal of the third input terminal ("CK2") to the node of the output terminal ("OUT") – and thus the signal of the third input terminal (CK2) is supplied to the output terminal ("OUT").

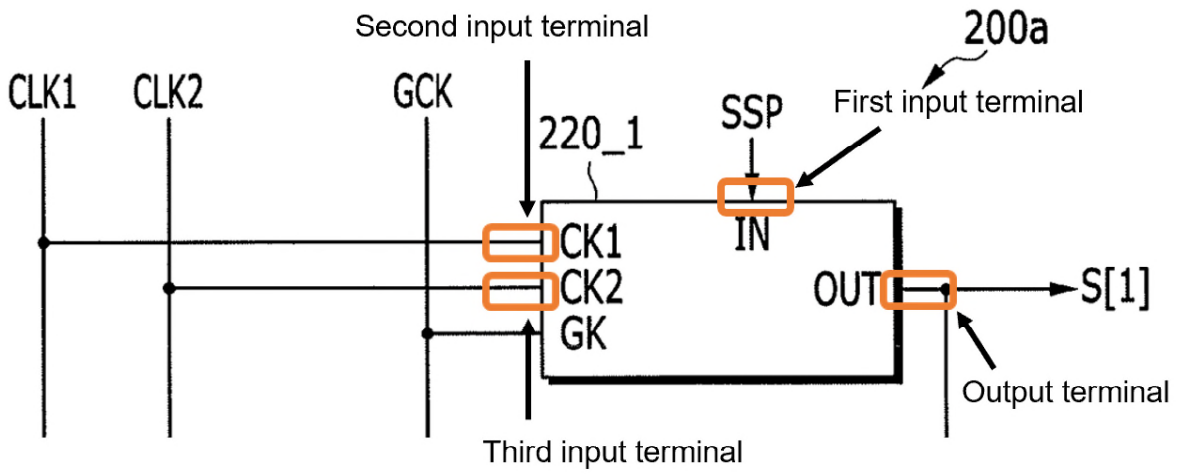
368. As also discussed earlier, the third input terminal (CK2) receives a clock signal – in particular, the clock signal CLK2, which is depicted in Figure 10 of Kim.



As the name itself indicates, the signal CLK2 is clearly a clock signal.

369. Finally, with respect to this clock signal being used as "the scan signal," it was shown above (see the annotated version of Figure 9 of Kim above) that when transistor M42 is turned on, the input signal that is being applied to the third input terminal CK2 (which, in this case is the clock signal CLK2) is supplied to the output terminal OUT.

370. Figure 8 of Kim shows that the output at the terminal OUT is used as a scan signal.



(Annotations added.) Therefore, the "clock signal applied to the third input terminal is used as the scan signal."

371. Thus, Kim anticipates this claim of the '593 patent.

11. Dependent Claim 17

372. As an initial matter, Claim 17 depends from Claim 15; as was shown above, Claim 15 of the '593 patent is disclosed by Kim.

373. Claim 17 further requires that "the first input terminal receives a scan signal of a previous stage circuit or a start signal."

374. This claim is identical to an element of Claim 2 of the '593 patent – which was discussed earlier (in Section XII.B.2).

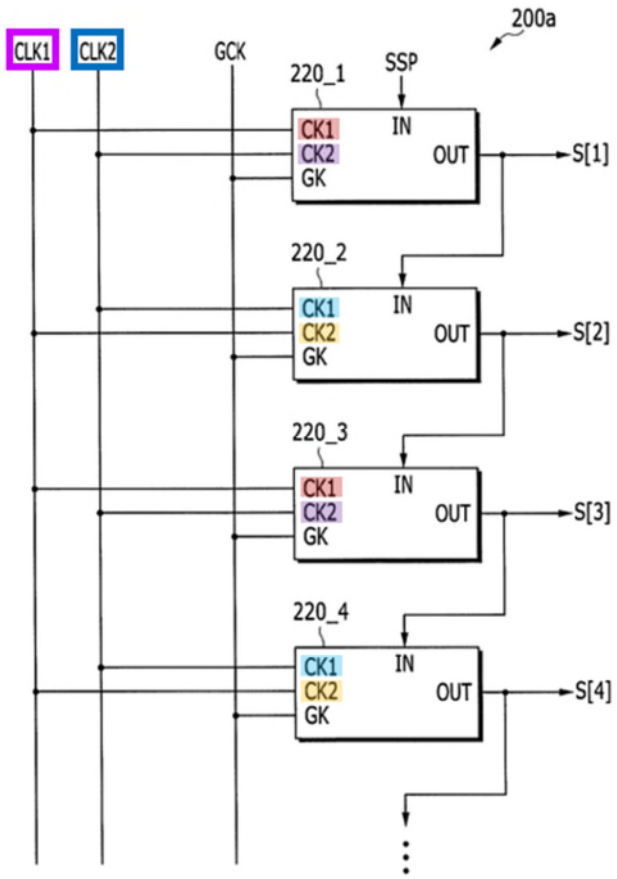
375. Thus, Kim anticipates this claim of the '593 patent.

12. Dependent Claim 18

376. As an initial matter, Claim 18 depends from Claim 17, and Claim 17 depends from Claim 15; as was shown above, Claim 15 and Claim 17 of the '593 patent are disclosed by Kim.

377. Claim 18 further requires "wherein second input terminals of odd stage circuits receive a first clock signal and third input terminals of odd stage circuits receive a second clock signal, and wherein second input terminals of even stage circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal." In other words, the first clock signal and the second clock signal alternate between the second input terminal and the third terminal along the sequence of stage circuits.

378. This is readily demonstrated via an annotated version of Figure 8 of Kim.



(Annotations added.) To simplify the explanation of what is going on, the first clock signal (CLK1) is annotated in magenta, and its destinations are annotated in maroon for odd-numbered stage circuits (220_1, 220_3, …) and orange for even-numbered stage circuits (220_2, 220_4, …). The second clock signal (CLK2) is annotated in blue, and its destinations are annotated in purple for odd-numbered stage circuits (220_1, 220_3, …) and light blue for even-numbered stage circuits (220_2, 220_4, …). As can be seen by inspection, the first clock signal (CLK1) goes to the second input terminal (CK1) of the odd-numbered stage circuits (220_1, 220_3, …) and to the third input terminal (CK2) of the even numbered stage circuits (220_2, 220_4,

…), while the second clock signal (CLK2) goes to the third input terminal (CK2) of the odd-numbered stage circuits and to the second input terminal (CK1) of the even-numbered stage circuits.

379. What is going on is also explained in Kim at [0155]:

> The first clock signal CLK1 is input into the first clock signal input terminals CK1 of odd numbered scan driving blocks 220_1, 220_3. . . . among the plurality of scan driving blocks 220_1, 220_2, 220_3, 220_4, . . . and the second clock signal CLK2 is input into the second clock signal input terminals CK2. In addition, the second clock signal CLK2 is input into the first clock signal input terminals CK1 of even numbered scan driving blocks 220_2, 220_4, ... among the plurality of scan driving blocks 220_1, 220_2. 220_3,220_4, ... and the first clock signal CLK1 is input into the second clock signal input terminals CK2.

380. Thus, Kim anticipates this claim of the '593 patent.

13. Dependent Claim 19

381. As an initial matter, Claim 19 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the '593 patent are disclosed by Kim.

382. Claim 19 further requires that "the first clock signal and the second clock signal have the same period and have phases that do not overlap."

383. This claim is identical to Claim 3 of the '593 patent – which was discussed earlier (in Section XII.B.3).

384. Thus, Kim anticipates this claim of the '593 patent.

14. Dependent Claim 21

385. As an initial matter, Claim 21 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the '593 patent are disclosed by Kim.

386. Claim 21 further requires "wherein the outputting unit includes: a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node: a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node: a first capacitor between the second node and the output terminal; and a second capacitor between the first node and the first power supply."

387. This claim is identical to Claim 7 of the '593 patent – which was discussed earlier (in Section XII.B.6).

388. Thus, Kim anticipates this claim of the '593 patent.

15. Dependent Claim 22

389. As an initial matter, Claim 22 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the '593 patent are disclosed by Kim.

390. Claim 22 further requires "wherein the second driver includes: a sixth transistor between the first node and the second input terminal, the sixth transistor

having a gate electrode coupled to the second node; and a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal."

391. This claim is identical to Claim 8 of the '593 patent – which was discussed earlier (in Section XII.B.7).

392. Thus, Kim anticipates this claim of the '593 patent.

16. Dependent Claim 25

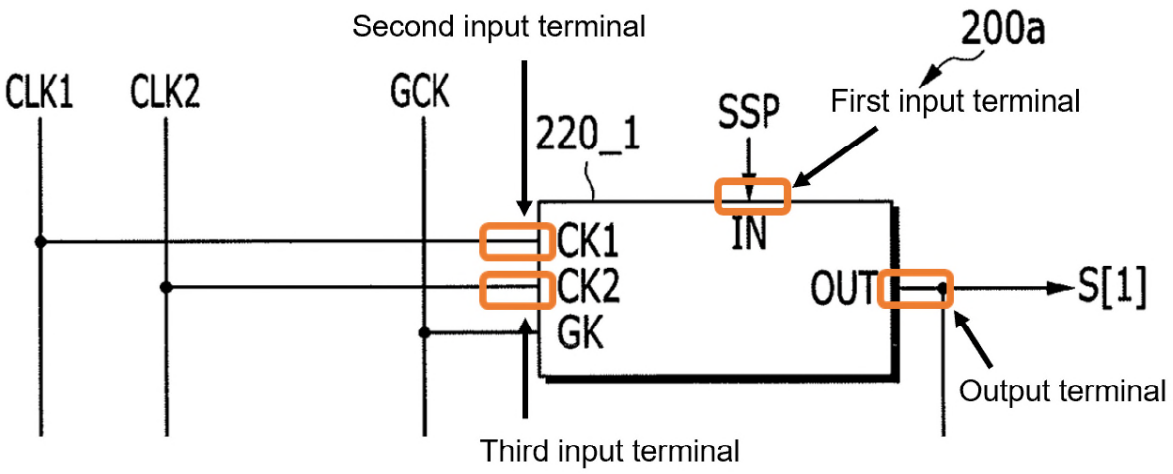
393. As an initial matter, Claim 25 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the '593 patent are disclosed by Kim.

394. Claim 25 further requires that "the scan signal of the previous stage circuit ***or*** the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal." (Emphasis added.) As per the emphasis added to the word "or" in the claim, Claim 25 of the '593 patent offers two alternatives regarding the provision of a signal to the first input terminal (such that it overlaps the clock signal supplied to the second input terminal).

395. The second alternative specifies that it is the start signal that is applied to the first input terminal (and with the condition that follows – that the signal thus supplied overlaps the clock signal supplied to the second input terminal) – and is

thus identical to Claim 5 of the '593 patent (which was discussed earlier, in Section XII.A.5), which requires that "the start signal is supplied to overlap the first clock signal."

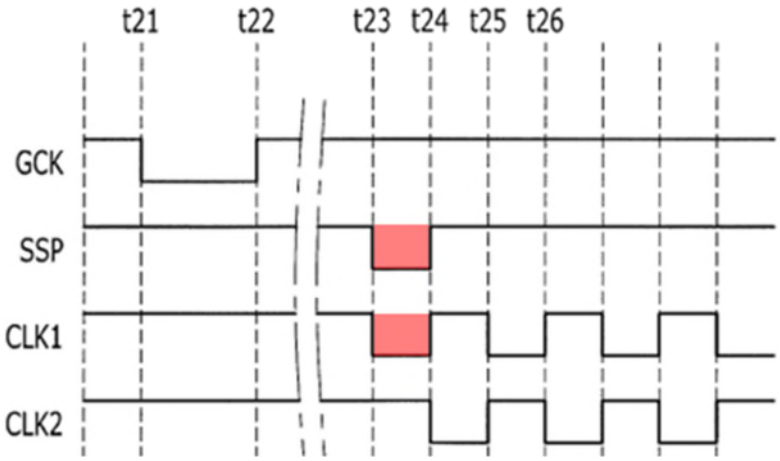
396. Further, Claim 5 depends from Claim 2, which depends from Claim 1 – and it is in Claim 1 (more specifically, in the preamble of Claim 1 – which was discussed in Section XII.B.1.a) that the inputs and outputs of the first stage circuit are explained; thus, a figure from Section XII.B.1.a is simply repeated here.



(Annotations added.) As can once again be seen by examination of this annotated excerpt from Figure 8 of Kim, the start signal (SSP) is supplied to the first input terminal (IN), while the first clock signal (CLK1) is supplied to the second input terminal (CK1).

397. The timing diagram for these waveforms is found in Figure 10 of Kim – and thus, an annotated version of this diagram, which was presented earlier in the discussion of Claim 5 (in Section XII.A.5) is reprised here.

FIG. 10



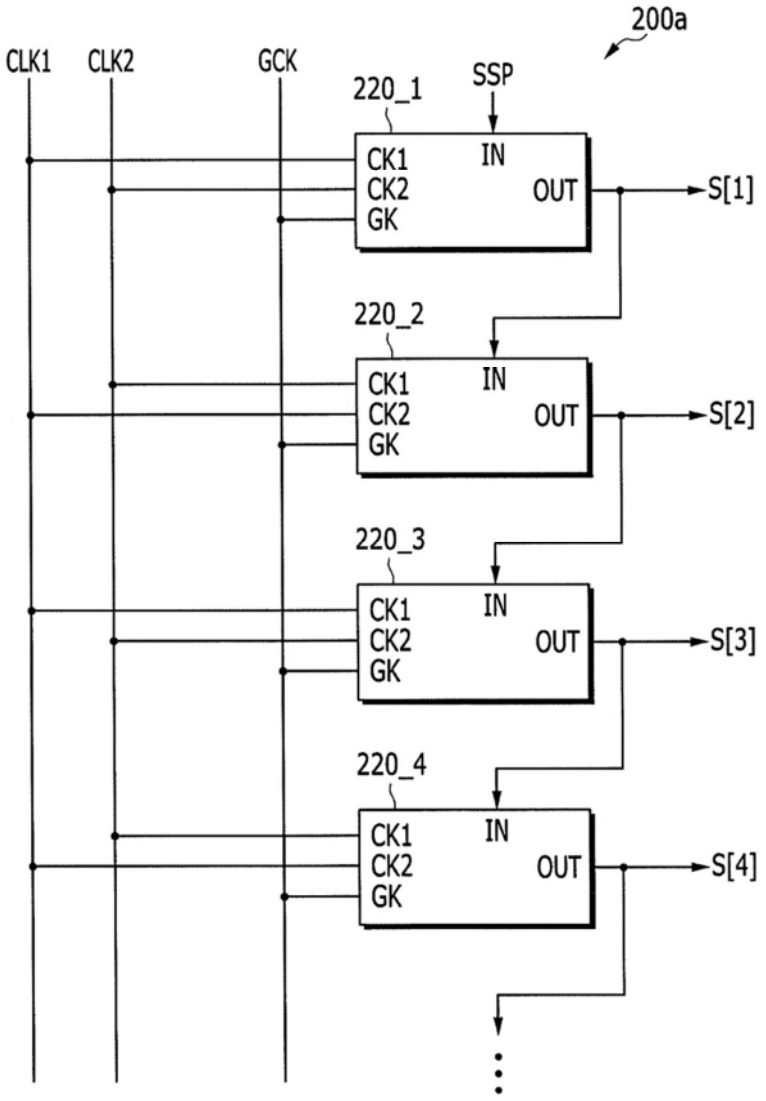
As can be seen, the start signal (SSP) goes low (its "active" level) at the same time and for the same duration that the first clock signal (CLK1) goes low (also its "active" level) as part of its recurring square wave behavior. Thus, the start signal (SSP) overlaps the first clock signal (CLK1).

398. Thus, Kim anticipates this claim of the '593 patent.

399. For completeness, it is worth noting that the first alternative on offer in Claim 25 specifies that it is the scan signal of the previous stage circuit that is applied to the first input terminal (and with the condition that follows – that the signal thus supplied overlaps the clock signal supplied to the second input terminal). As detailed

earlier (in the discussion of claim sub-element [15-c-2] in Section XII.B.9.d.ii), after the first stage circuit (which receives a start signal as the input signal at the first input terminal), the first input terminal of subsequent stage circuits receives the signal that is output from the output terminal of the preceding stage circuit. Meanwhile, for odd-numbered stages, the second input terminal (CK1) receives the first clock signal (CLK1) – while for even-numbered stages, the second input terminal (CK1) receives the second clock signal (CLK2).

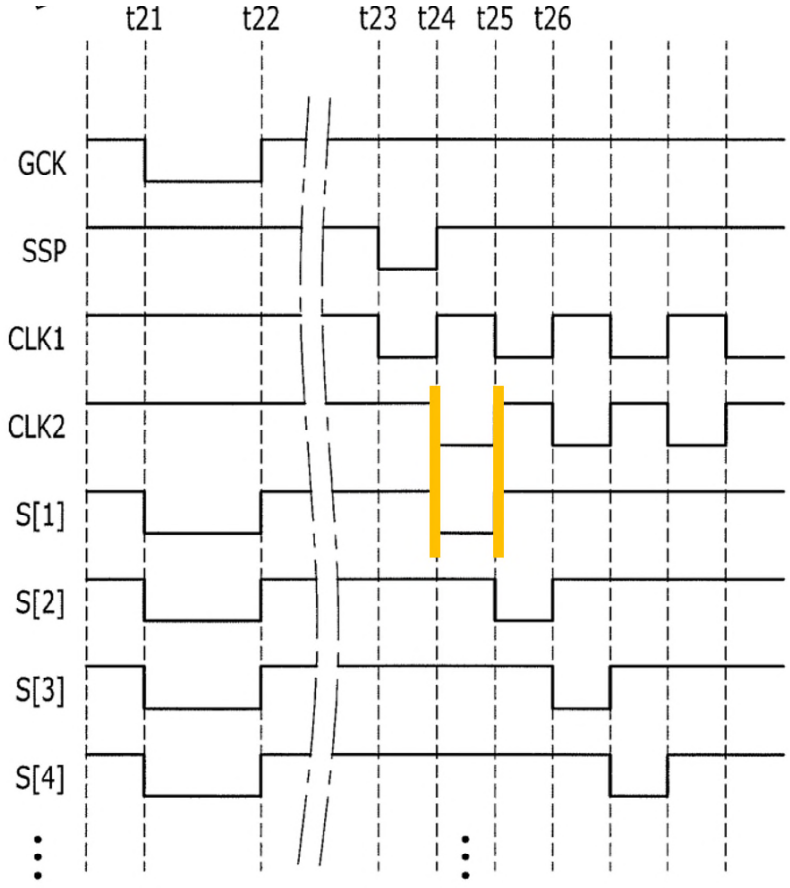
400. This is all readily summarized in Figure 8 of Kim – which was presented in Section XII.B.9.d.ii (without annotations), and which is reprised here.



401. Consider the second stage circuit (220_2); this stage circuit will receive the output from the first stage circuit (S[1]) at its input terminal (IN), and receive the second clock signal (CLK2) at its second input terminal (CK1). Now consider the third stage circuit (220_3); this stage circuit will receive the output from the second stage circuit (S[2]) at its input terminal (IN), and receive the first clock signal (CLK1) at its second input terminal (CK1). This pattern can readily be repeated to provide the same details for all subsequent stage circuits.

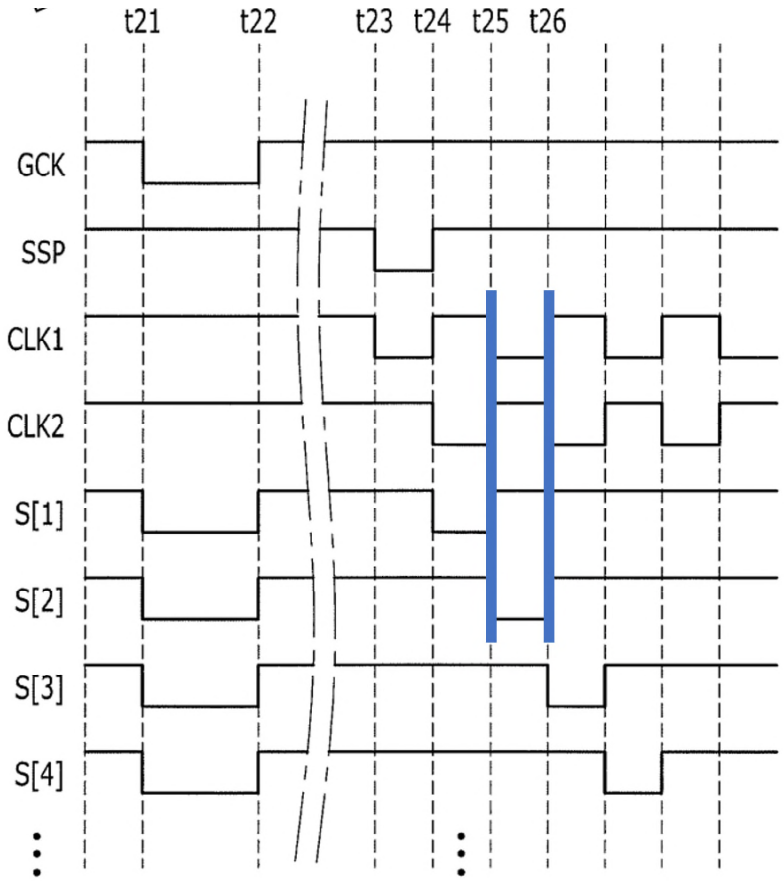
402. In order to meet the first alternative of Claim 25 (as discussed just above), for even-numbered stage circuits the signal received at the input terminal (IN) must overlap with the second clock signal (CLK2), while for odd-numbered stage circuits the signal received at the input terminal (IN) must overlap with the first clock signal (CLK1).

403. Examination of Figure 5 of Chung shows that this is indeed the case – as two annotated versions of this figure make clear.



(Annotations added.) The annotations here are for the second stage circuit – which receives the output signal from the first stage circuit (S[1]) at its input terminal (IN)

and the second clock signal (CLK2) at its second input terminal (CK1). As can be seen, S[1] overlaps CLK2 – meeting the requirement specified in the first alternative of Claim 25 of the '593 patent.



(Annotations added.) The annotations here are for the third stage circuit – which receives the output signal from the second stage circuit (S[2]) at its input terminal (IN) and the first clock signal (CLK1) at its second input terminal (CK1). As can be seen, S[2] overlaps CLK1 – meeting the requirement specified in the first alternative of Claim 25 of the '593 patent.

404. It is also evident from both annotated versions of Figure 10 of Kim presented here that this analysis could be repeated for the fourth stage circuit, the fifth stage circuit, … and for all further even-numbered and odd-numbered stage circuits – and that the same results would be found for each stage circuit.

405. Thus, Kim anticipates this claim of the '593 patent for these additional (and separate) reasons.

C. Ground 3: Tobita Renders Obvious Claims 1-5, 14-19, and 25

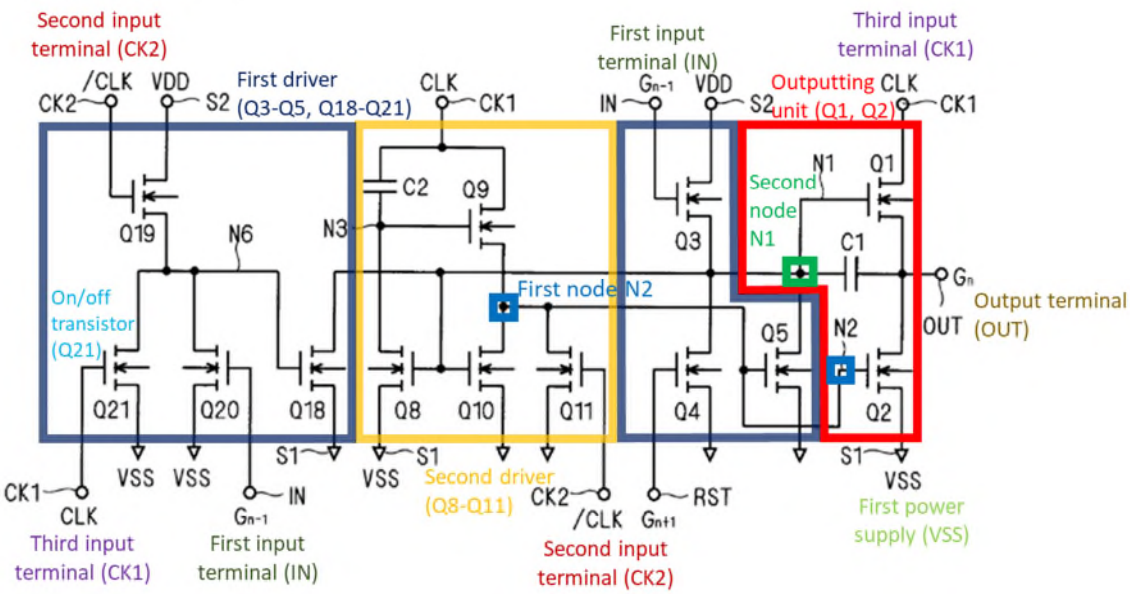
406. As will be discussed below, it is my conclusion and opinion that Claims 1-5, 14-19, and 25 of the '593 patent are rendered obvious by Tobita.

407. As an initial matter, the circuitry disclosed in the embodiments of Tobita uses nMOS transistors, while the circuitry disclosed in the embodiments of the '593 patent uses pMOS transistors. As was explained in detail in Section VII.A.2, when transistors are used as simple switches, either nMOS transistors or pMOS transistors can be used – and further, when simple switches are to be used, one type of transistor can be swapped for the other; the minor consequent modifications required were detailed in Section VII.A.2. It was also shown in Section VII.A.2 that this was all well-known in the art at the time of the '593 patent – and thus would have known to a POSITA at that time.

408. Before beginning a discussion of the analysis, it will be helpful to first provide an annotated version of Figure 20 of Tobita – with the annotations indicating

the identification of the specific structures recited in the claims of the '593 patent, as mapped to Tobita.

F I G . 2 0



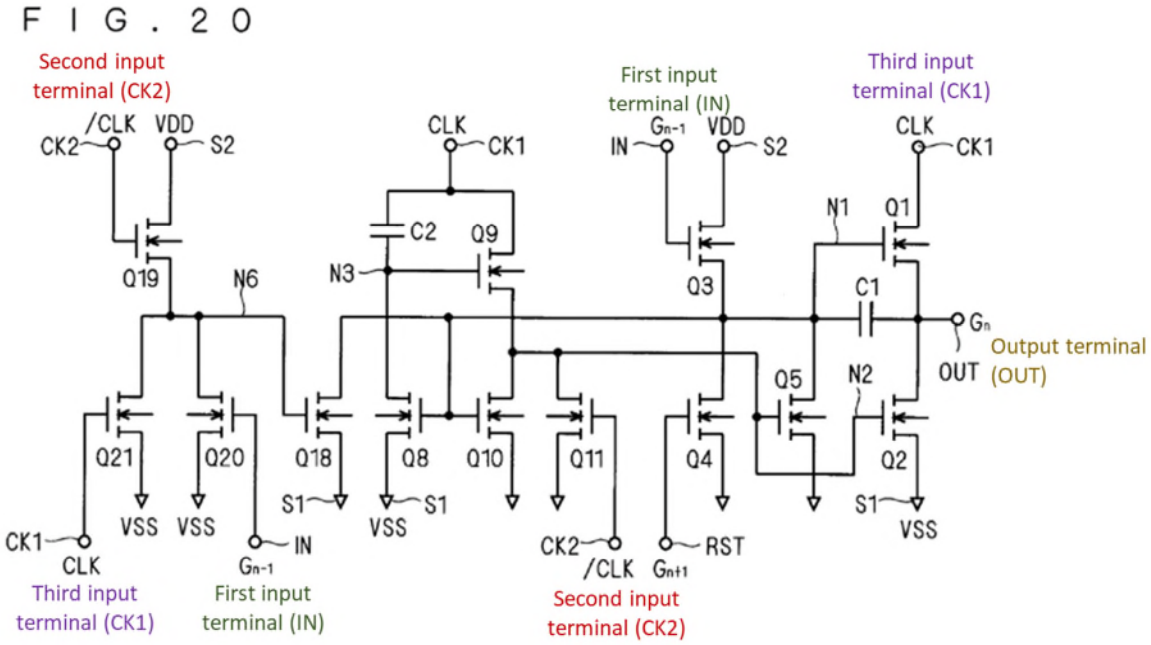
1. Independent Claim 1

409. It is my conclusion and opinion that Claim 1 of the '593 patent is rendered obvious by Tobita.

a. [1-pre]: "A stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal, the stage circuit comprising:"

410. As an initial matter, I will be offering no opinion regarding whether or not the preamble of Claim 1 is limiting. I have been instructed by counsel for Petitioner to offer an opinion as to whether or not the prior art discloses or renders obvious the preamble, regardless of whether or not the preamble is limiting.

411. Tobita discloses the preamble of Claim 1 of the '593 patent; this can be seen readily via annotated versions of Figure 20 of Tobita:



(Annotations added.)

As can be seen in this annotated figure, Tobita discloses a first input terminal, a second input terminal, a third input terminal, and an output terminal – all of which are part of a stage circuit.

412. Thus, Tobita discloses the preamble of Claim 1 of the '593 patent.

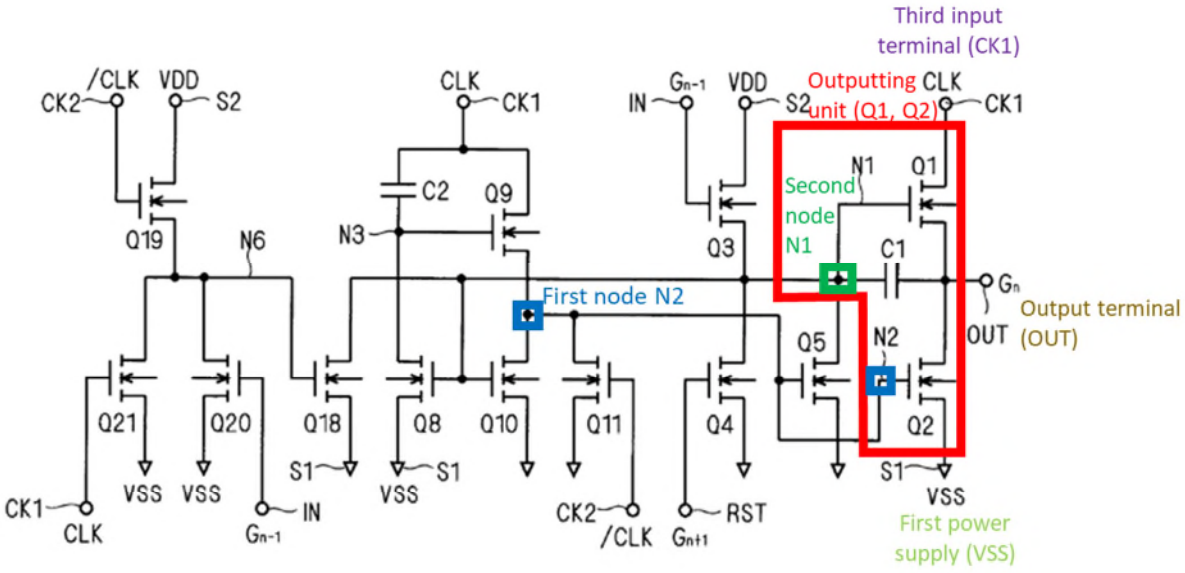
b. [1-a]: "an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node:"

413. Claim element [1-a] is rather long – and thus the analysis will be simpler to explain if this claim element is broken up into sub-elements.

i. [1-a-1]: "an outputting unit having a first node and a second node,"

414. Tobita discloses this claim sub-element; this is evident via an annotated version of Figure 20 of Tobita:

FIG. 20

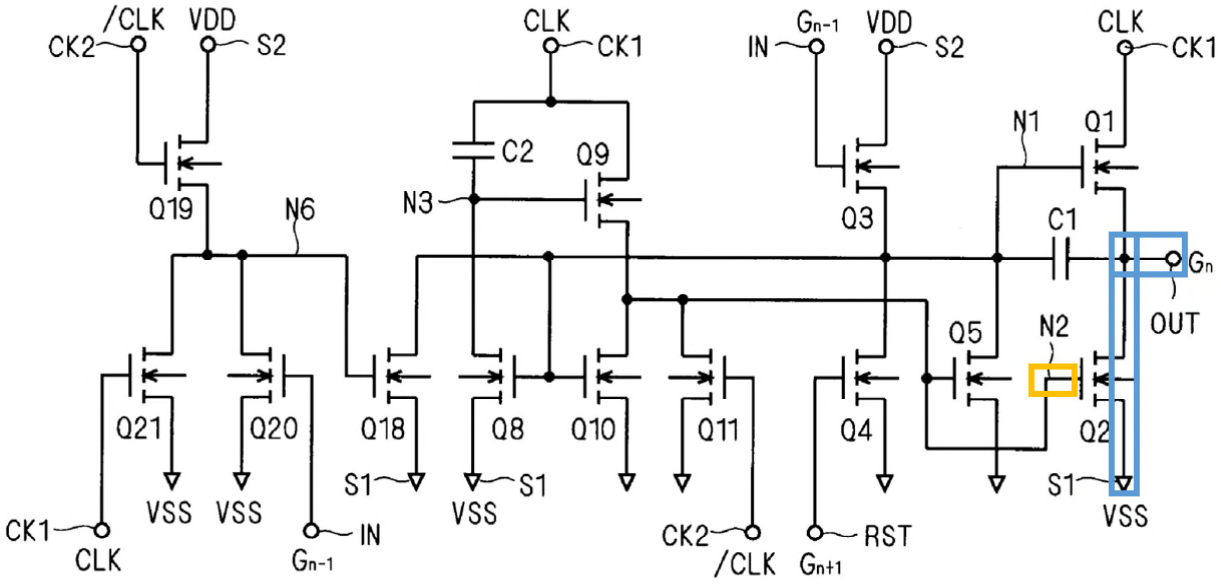


(Annotations added.) The node labeled "N2" is the first node, and the node labeled "N1" is the second node – while the "outputting unit" is a shown via the annotation box-bounding in red.

415. Thus, Tobita discloses this claim sub-element of this claim element of Claim 1 of the '593 patent.

ii. [1-a-2]: "the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node"

416. Tobita discloses this claim sub-element; this is evident via an annotated version of Figure 20 of Tobita:



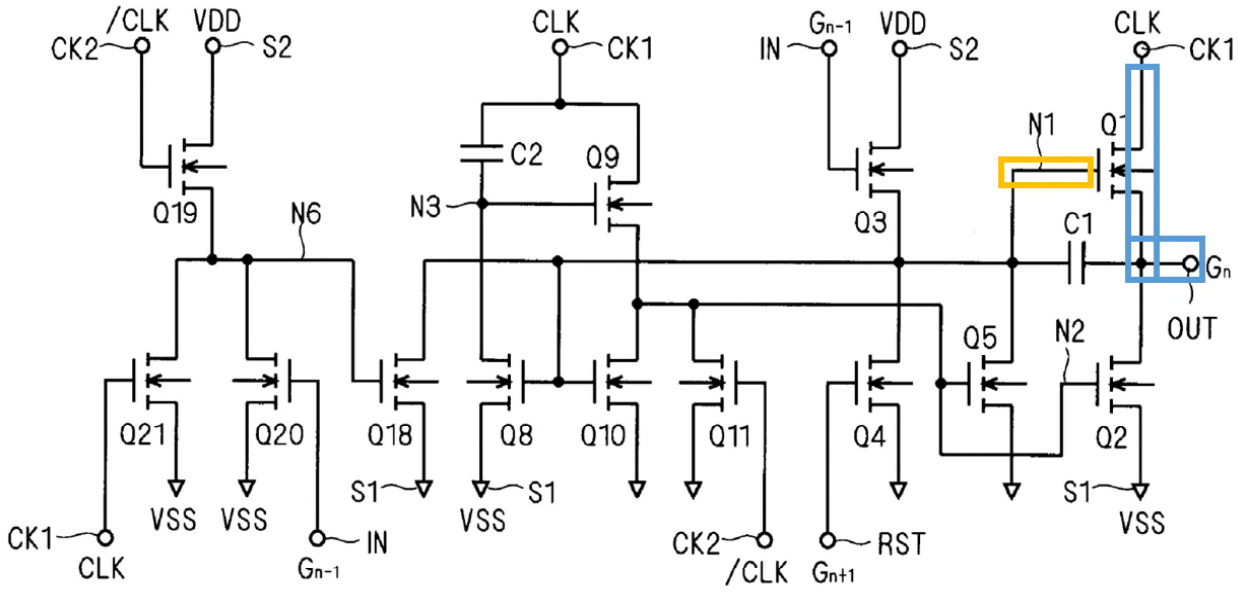
(Annotations added.) As the annotations show, when an appropriate (i.e., turn-on) voltage is applied at the first node (the node labeled "N2"), transistor Q2 will turn on; this will connect the first power supply voltage (VSS) to the node of the output terminal ("OUT") – and thus the voltage of the first power supply connection (VSS) is supplied to the output terminal ("OUT"). (On the other hand, when a turn-on voltage is not applied at the first node ("N2"), transistor Q2 will not turn on – and the voltage of the first power supply connection (VSS) is not supplied to the output terminal.)

417. Thus, Tobita discloses this claim sub-element of this claim element of Claim 1 of the '593 patent.

iii. [1-a-3]: "and a signal of the third input terminal to the output terminal according to a voltage applied to the second node:"

418. Tobita discloses this claim sub-element; this is evident via an annotated version of Figure 20 of Tobita:

FIG. 20



(Annotations added.) As the annotations show, when an appropriate (i.e., turn-on) voltage is applied at the second node (the node labeled "N1"), transistor Q1 will turn on; this will connect the signal of the third input terminal ("CK1") to the node of the output terminal ("OUT") – and thus the signal of the third input terminal ("CK1") is

supplied to the output terminal ("OUT"). (On the other hand, when a turn-on voltage is not applied at the second node ("N1"), transistor Q1 will not turn on – and thus the signal of the third input terminal (CK1) is not supplied to the output terminal ("OUT").)

419. Thus, Tobita discloses this claim sub-element of this claim element of Claim 1 of the '593 patent.

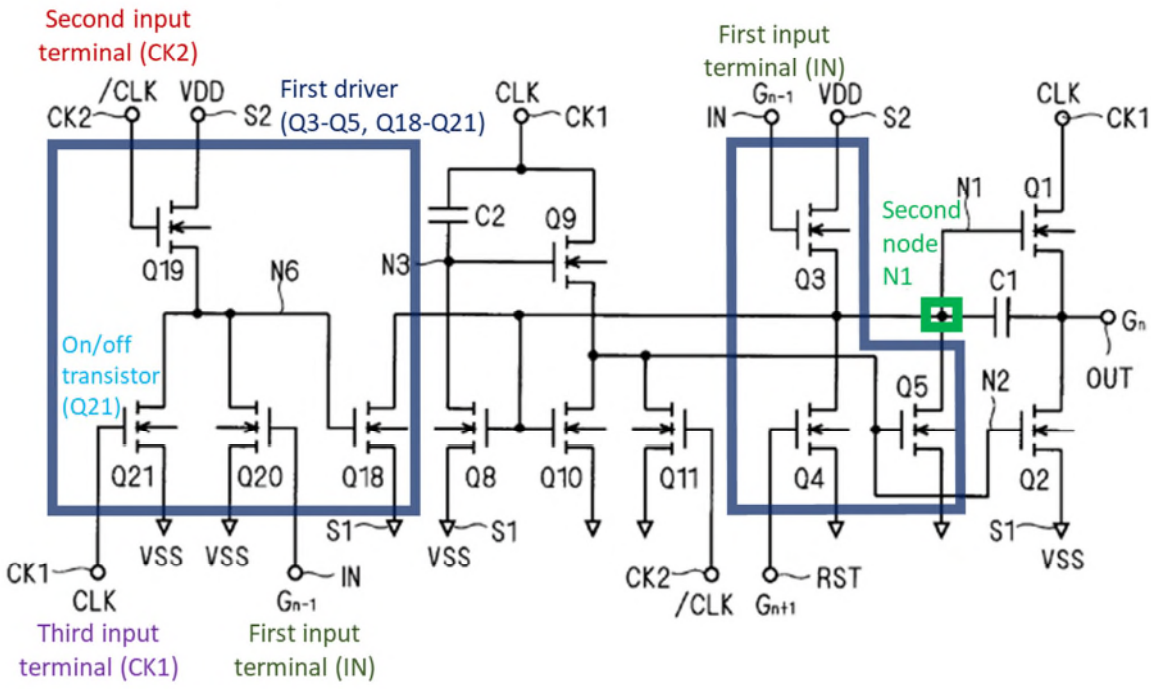
iv. Claim Element [1-a] Summary

420. As just demonstrated, Tobita discloses claim sub-elements [1-a-1], [1-a-2], and [1-a-3] of the '593 patent; thus, Tobita discloses claim element [1-a] of Claim 1 of the '593 patent.

c. [1-b]: "a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal; and"

421. Tobita discloses this claim element of the '593 patent; this is evident via an annotated version of Figure 20 of Tobita:

FIG. 20



(Annotations added.)

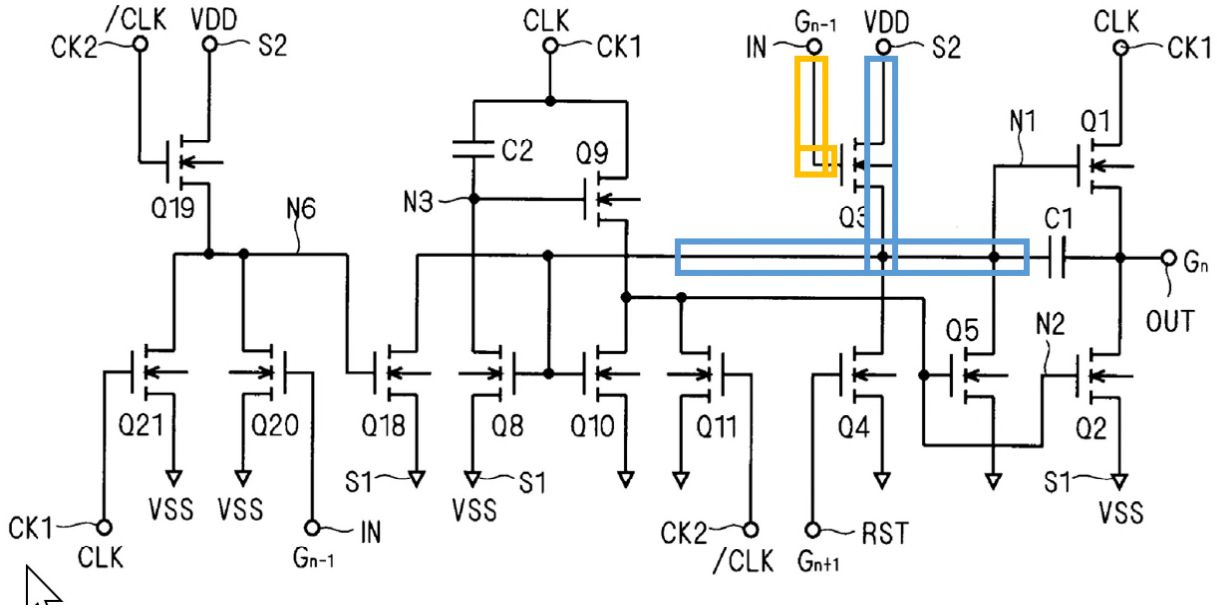
422. In the Tobita figure above, the "first driver" is identified using navy blue box-bounding.

423. While Tobita's embodiment of first driver has more transistors than the preferred embodiment first driver disclosed in the '593 patent, consistent with Patent Owner's proposed constructions and infringement theories from the related ITC Investigation, there is nothing in the claim element limiting the number of transistors in the first driver. Further, the voltage on the second node ("N1") is controlled in accordance with the signals of the first input terminal, the second input terminal, and the third input terminal – as will be shown by the annotations to the following

versions of Figure 20 of Tobita. As these annotations show, this functionality is implemented in three separate ways – one for each of the three input terminals.

424. The first way, using the first input terminal, is implemented as described here.

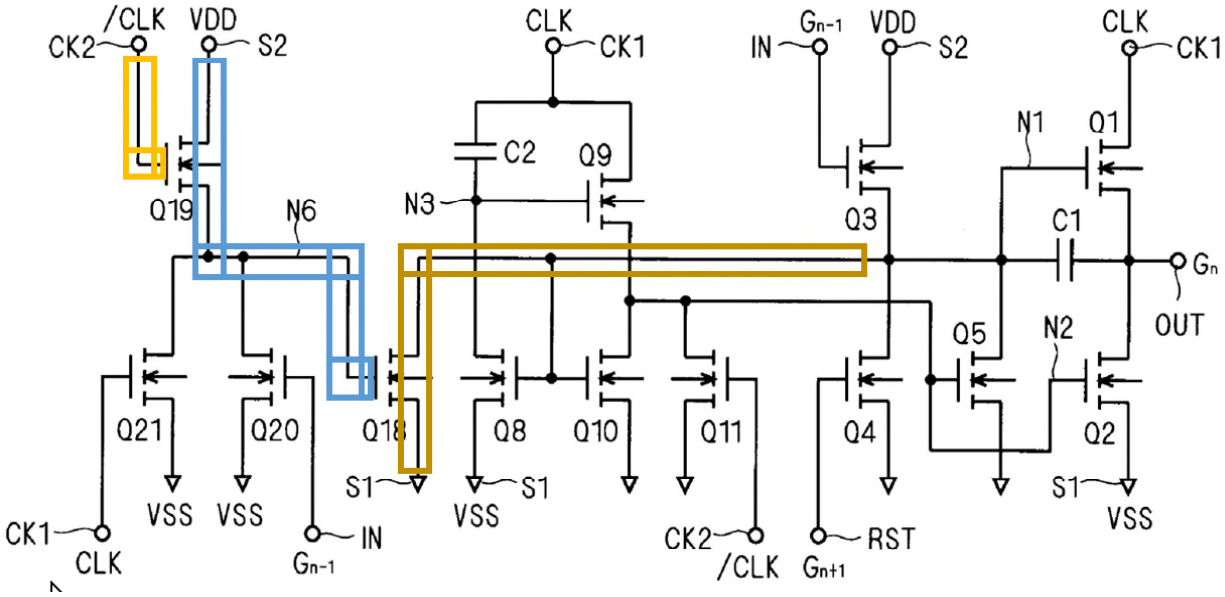
F I G . 2 0



(Annotations added.) The first way occurs when the first input signal (G_{n-1}) at the first input terminal (IN) is pulled to a voltage that causes transistor Q3 to turn on; when this is done, the second node (N1) is pulled to the high voltage level VDD. (On the other hand, when transistor Q3 is not turned on, the high voltage VDD is not supplied to the second node (N1).)

425. The second way will now be described.

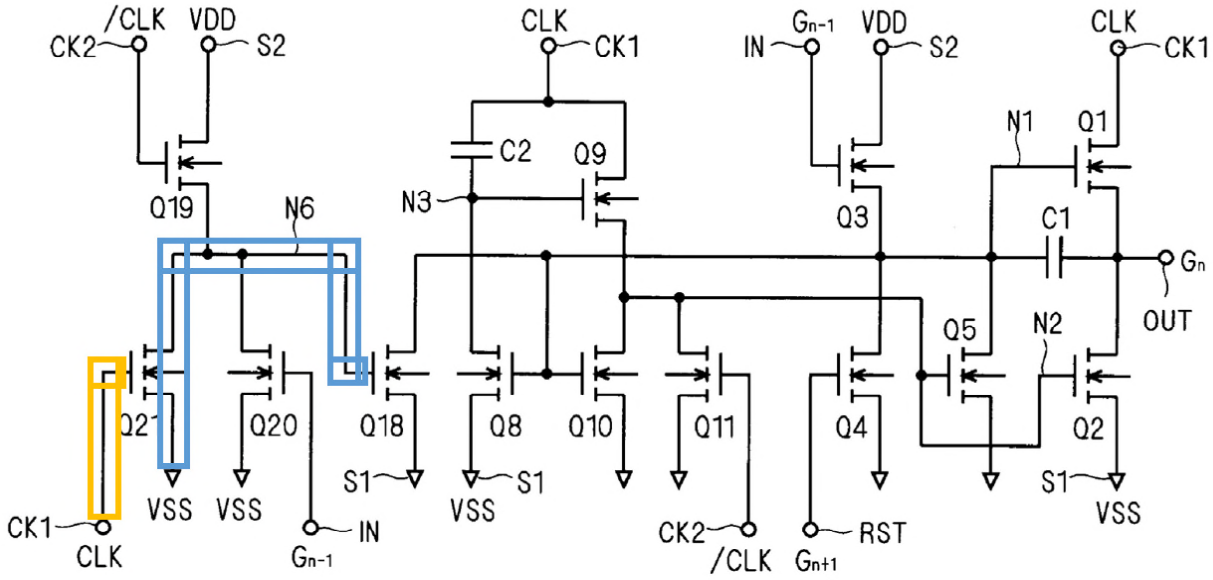
F I G . 2 0



The second way occurs when the input signal (/CLK) at the second input terminal (CK2) is pulled to a voltage that causes transistor Q19 to turn on; this will pull the node labeled "N6" to the high (i.e., VDD) voltage level. This will cause transistor Q18 to turn on; when this is done, the second node (N1) is pulled to the low voltage level VSS. (On the other hand, when transistor Q19 is not turned on, the transistor Q18 will not turn on, and the low voltage VSS is not supplied to the second node (N1).)

426. The third way will now be described.

FIG. 20



The third way occurs when the input signal (CLK) at the third input terminal (CK1) is pulled to a voltage that causes transistor Q2 to turn on. This causes the low voltage level VSS to be passed through transistor Q2 to the node labeled "N6," and thus to be passed to the gate of transistor Q18 – which causes transistor Q18 to be turned off.

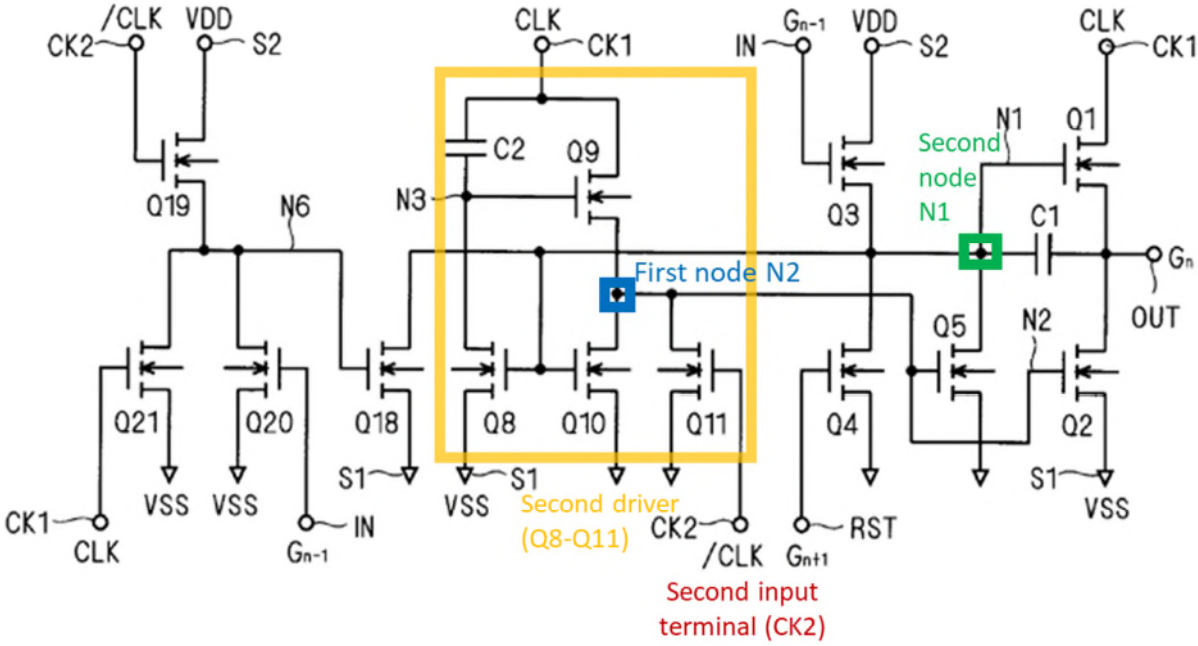
427. Relatedly, note that the second node N1 is coupled to the gate electrodes of transistors Q1, Q8, and Q10. Thus, the second node N1 controls the operation of these transistors, not the other way around.

428. Thus, Tobita discloses this claim element of Claim 1 of the '593 patent.

d. [1-c]: "a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, wherein"

429. Tobita discloses this claim element of the '593 patent; this is evident via an annotated version of Figure 20 of Tobita:

F I G . 2 0



(Annotations added.)

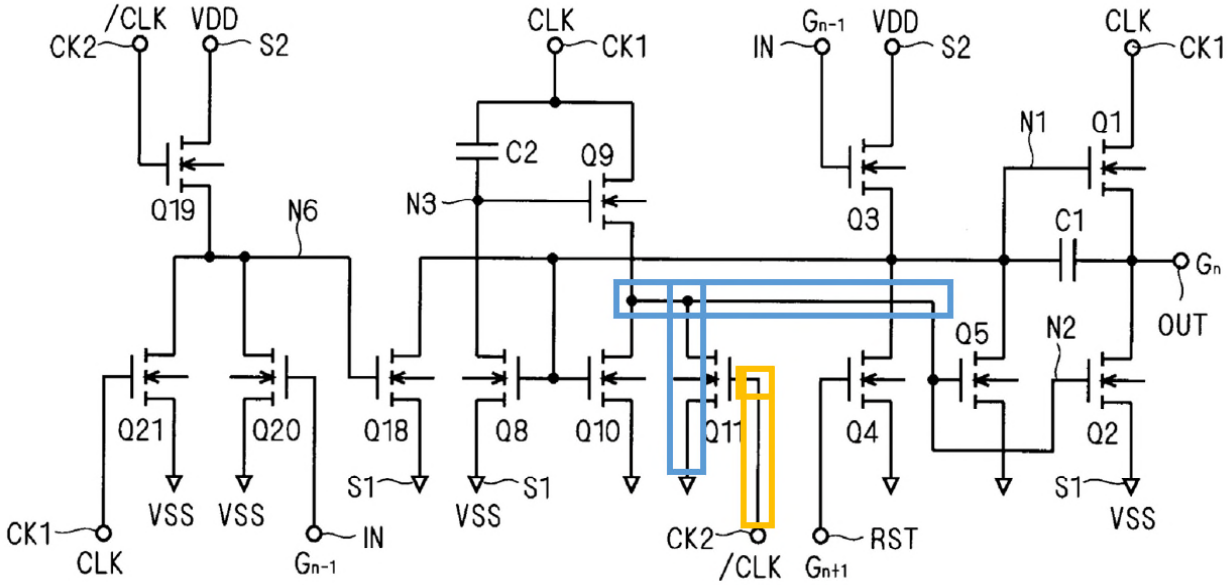
430. In the Tobita figure above, the "second driver" is identified using yellow box-bounding.

431. While Tobita's embodiment of second driver has more transistors than the preferred embodiment first driver disclosed in the '593 patent, consistent with Patent Owner's proposed constructions and infringement theories from the related

ITC Investigation, there is nothing in the claim element limiting the number of transistors in the second driver. Further, the voltage on the first node ("N2") is controlled in accordance with the signal of the second input terminal, and the voltage of the second node – as will be shown by the annotations to the following versions of Figure 20 of Tobita. As these annotations show, this functionality is implemented in two separate ways.

432. The first way, using the second input terminal, is implemented as described here.

FIG. 20

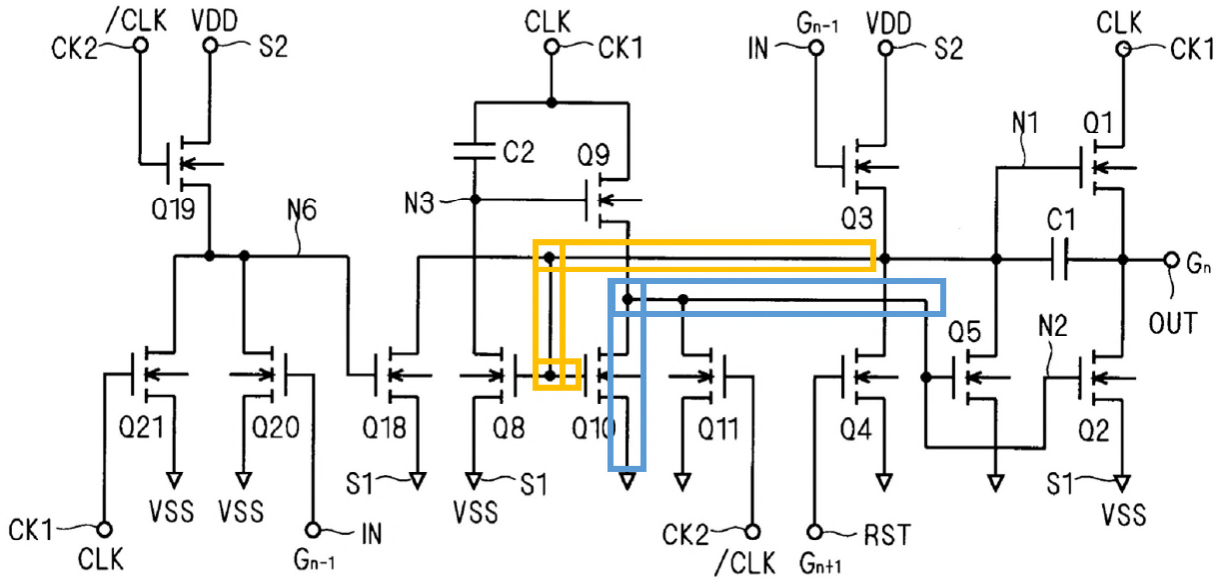


When a voltage is applied to the second input terminal (CK2) that turns on the transistor Q11, Q11 connects the first node (N2) to the low voltage rail (VSS) – which pulls the voltage on the first node (N2) to the low rail voltage (VSS). (When

transistor Q11 is not turned on, this functionality is not available). Thus the voltage on the first node is controlled in accordance with the signal of the second input terminal.

433. The second way, using the voltage on the second node (N1), is implemented as described here.

FIG. 20



When the voltage on the second node (N1) is such that it will turn on transistor Q10, the first node (N2) will be connected to the low voltage rail (VSS) through the transistor Q10 – which will serve to pull the voltage on the first node (N2) to the low voltage rail voltage (VSS). (When the voltage on the second node (N1) is such that it will not turn on transistor Q10, then this functionality is not available). Thus, the

voltage on the first node is controlled in accordance with the voltage of the second node.

434. Relatedly, note that the first node N2 is coupled to the gate electrodes of transistors Q2 and Q5. Thus, the first node N2 controls the operation of these transistors, not the other way around.

435. Therefore, Tobita discloses this claim element of Claim 1 of the '593 patent.

e. [1-d]: "the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver."

436. Tobita discloses this claim element of the '593 patent; this is evident via annotated versions of Figure 20 of Tobita:

F I G . 2 0

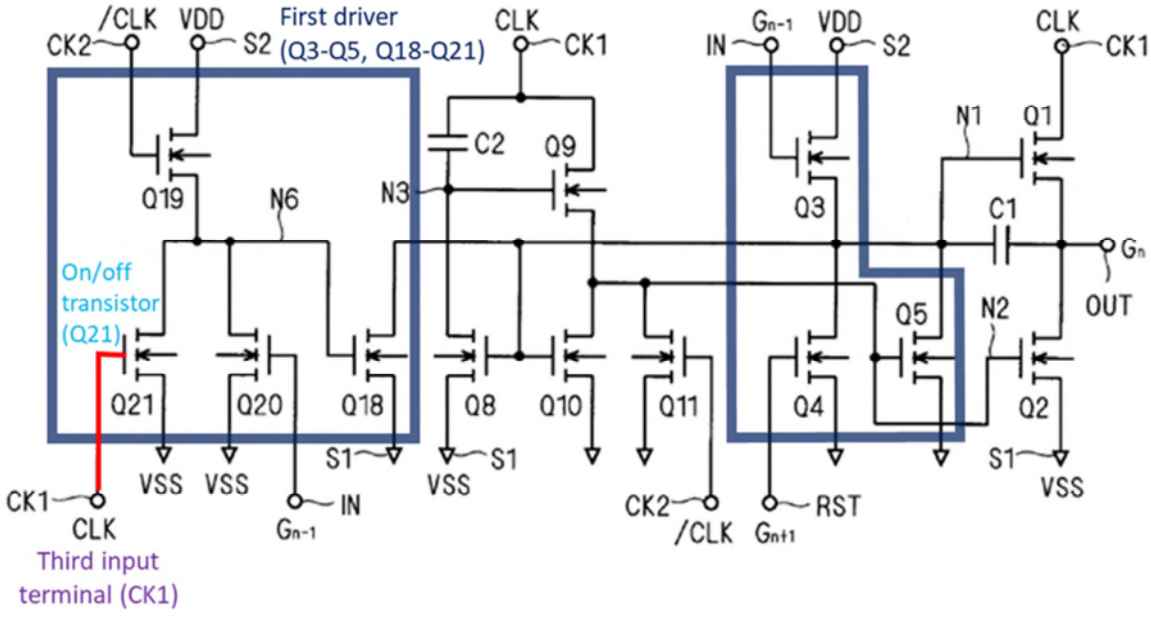
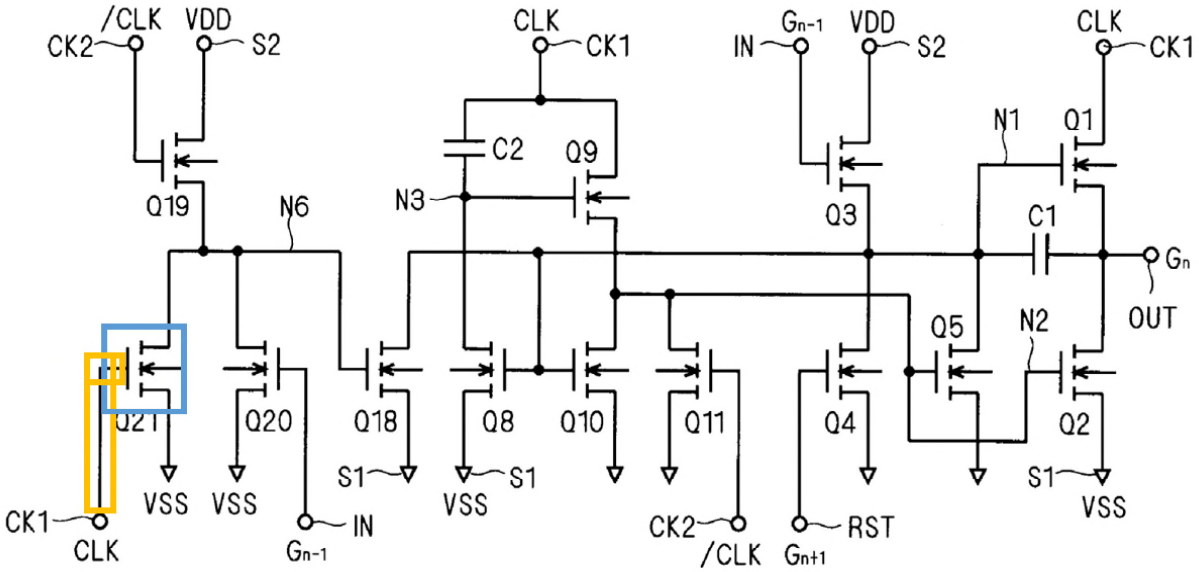


FIG. 20



When a signal (such as CLK) is applied to the third input terminal (CK1), it directly controls the on/off operation of transistor Q21 – which is part of the first driver.

437. Thus, Tobita discloses this claim element of Claim 1 of the '593 patent.

f. Claim 1 Summary

438. As just shown, Tobita discloses each element of Claim 1 of the '593 patent; thus, Tobita renders obvious Claim 1 of the '593 patent.

2. Dependent Claim 2

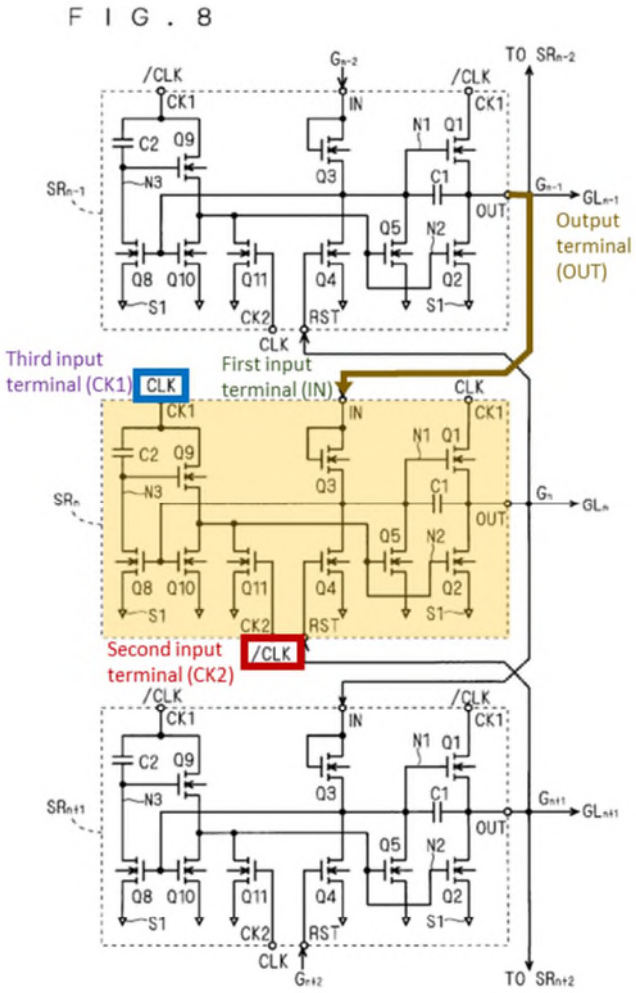
439. As an initial matter, Claim 2 depends from Claim 1; as was shown above, Claim 1 of the '593 patent is disclosed by Tobita.

440. Claim 2 further requires that "wherein the first input terminal receives an output signal of a previous stage circuit or a start signal, wherein the second input

terminal receives a first clock signal, and wherein the third input terminal receives a second clock signal." Tobita discloses this claim of the '593 patent.

441. To begin, note that the first part of the claim language just cited includes "wherein the first input terminal receives an output signal of a previous stage circuit ***or*** a start signal" (emphasis added). Because of the use of "or," the presence of this claim element term can be shown to be present in Tobita if the first input terminal receives either "an output signal of a previous stage circuit" or "a start signal"; it will be shown next that Tobita discloses the first of these two options.

442. This item and the remainder of Claim 2 can be shown to be disclosed by Tobita via the examination of an annotated version of Figure 8 of Tobita.



(Annotations added.) As can be seen from examination of this annotated figure, the middle stage circuit block (SR_n) receives an output signal of a previous stage circuit block at the first input terminal (IN). Also, the second input terminal (CK2) receives a first clock signal (/CLK), and the third input terminal (CK1) receives a second clock signal (CLK); Tobita specifically identifies /CLK and CLK as being clock signals (e.g., "… clock signals CLK and /CLK …" (Tobita at [0095]). Note in particular that the third stage circuit block (SR_3), like the first stage circuit block

(SR_1), is configured so that the second input terminal receives a first clock signal and the third input terminal receives a second clock signal. (*Id.*)

443. Thus, Tobita renders obvious Claim 2 of the '593 patent.

444. For completeness, it can be noted that the other part of the "or" situation discussed at the beginning of this discussion of Claim 2 ("wherein the first input terminal receives an output signal of a previous stage circuit ***or*** a start signal") is also present in Tobita. Figure 8 of Tobita depicts a cascade of shift registers – in which (as just detailed) the first input terminal of a particular stage circuit receives an output signal of the previous stage circuit; however, Figure 8 does not include the initial stage circuit that is present as the first stage circuit in the cascade. However, Tobita notes that in this instance, the first stage circuit would receive a start signal:

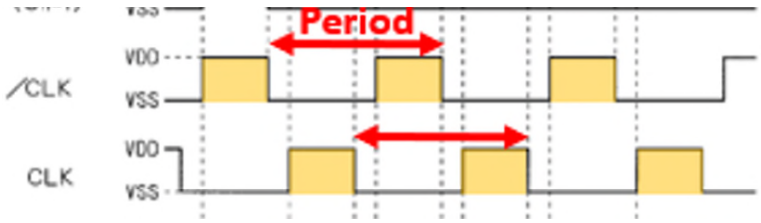
> … when the output signal G_{n-1} from the immediately preceding stage (or the start pulse SP in the first stage)… (Tobita at [0086]).
>
> Specifically, each of the unit shift registers SR has its input terminal IN connected to the output terminal OUT of a unit shift register SR of the immediately preceding stage, except that the input terminal IN of the unit shift register SR_1 of the first stage receives a start pulse SP as an input signal. (Tobita at [0094].)
>
> Starting from that mode, the output signal G_{n-1} from the immediately preceding stage (start pulse SP in the case of the first stage), when raised to the H level, is input to the input terminal IN of the unit shift register SR… (Tobita at [0098].)

445. Thus, Tobita renders obvious Claim 2 of the '593 patent.

3. Dependent Claim 3

446. As an initial matter, Claim 3 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the '593 patent are disclosed by Tobita.

447. Claim 3 further requires that "wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap." Tobita discloses this claim of the '593 patent – as is evident from examination of an annotated version of Figure 9 from Tobita.



448. Note that, as described earlier, the circuitry disclosed in Tobita uses nMOS transistors – and thus, digital waveforms will be conveying turn-on signals when they are given a high voltage level (i.e., VDD) rather than a low voltage level (i.e., VSS). As was detailed in Section VII.A.2, when used as simple on/off switches, nMOS transistors can be exchanged for pMOS transistors – as long as waveforms (such as those depicted above in the annotated version of Figure 9 from Tobita) are inverted in form (that is, what was high for nMOS becomes low for pMOS, and what was low for nMOS becomes high for pMOS). Under such a change

in transistor type and a change in the waveforms, the circuit structure and the circuit operation will remain the same.

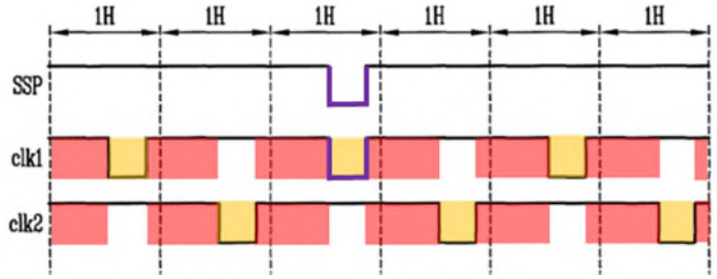
449. Further, it can also be seen from the annotated figure above that the first clock signal (/CLK) and the second clock signal (CLK) have the same period.[14]

450. Further, note that these two signals are digital waveforms – that is, they are square waves that have only one of two signal states – high or low. With digital waveforms, the term "phases that do not overlap" is known in the art as meaning that the two waveforms will not both be in their turn-on state, e.g., logic low for pMOS-based circuits and logic high for nMOS-based circuits, respectively, at the same time. The term does not mean the waveforms will not both be in their turn-off states at the same time.

451. The '593 patent disclosure is consistent with this understanding of a POSITA. As shown in the annotated, partial Figure 4 of the '593 patent, the turn-on low state of clock signals clk1 and clk2 (annotated in orange) do not overlap. But the turn-off high state of these clock signals overlaps in periods annotated in red:

[14] The term "period" was defined in the discussion of Claim 3 with respect to Ground 1 (at Section XII.A.3).

FIG. 4



452. Thus, Tobita renders obvious Claim 3 of the '593 patent.

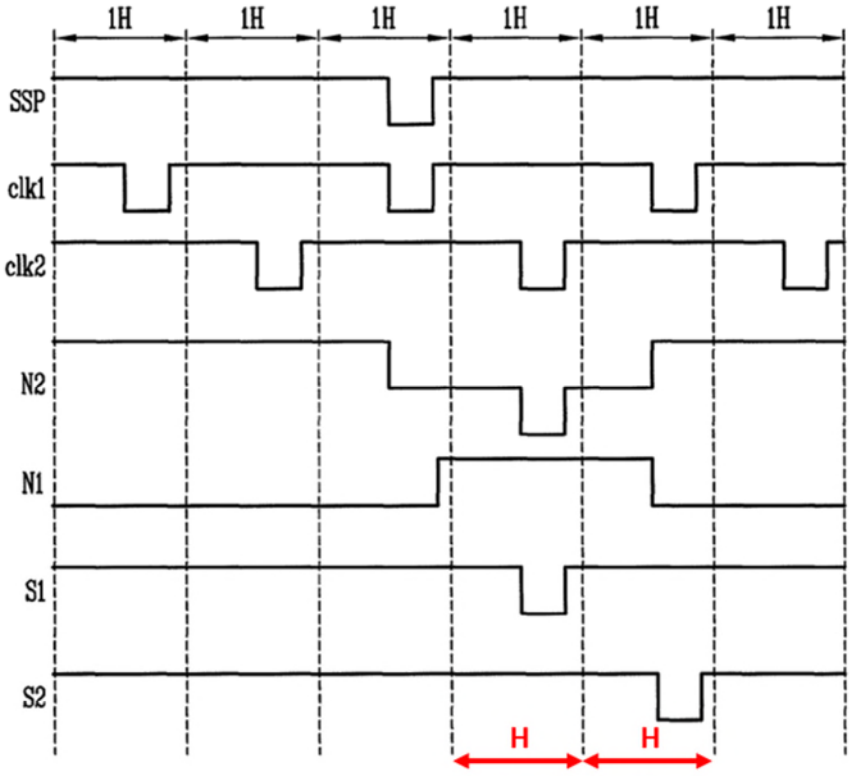
4. Dependent Claim 4

453. As an initial matter, Claim 4 depends from Claim 3, which depends from Claim 2, which depends from Claim 1; as was shown above, Claim 1, Claim 2, and Claim 3 of the '593 patent are disclosed by Tobita.

454. Claim 4 further requires "wherein the first clock signal and the second clock signal have a period equal to two horizontal periods 2H and are supplied in different horizontal periods as low signals." The language in this claim may be somewhat confusing – as the word "period" appears three times but the word clearly carries two different meanings depending on the usage.

455. The first instance of "period" is described via "the first clock signal and the second clock signal have a period"; this "period" is of the form described above with respect to Claim 3, in which "period" refers to the amount it takes for a recurring waveform to repeat itself.

456. The second instance of "period" occurs twice later in the claim, and refers (in both usages) to "horizontal periods"; this "period" refers to a particular amount of time (as in "a period of time"), and not to the repetition of a recurring waveform. More specifically, the '593 patent refers to "a period in which a scan signal is supplied to one scan line" as an exemplary horizontal period. ('593 patent, 5:18-20.) This period corresponds to the time span between outputs of successive stages, e.g., between S1 and S2, as shown in the annotated version of '593 patent Figure 4:



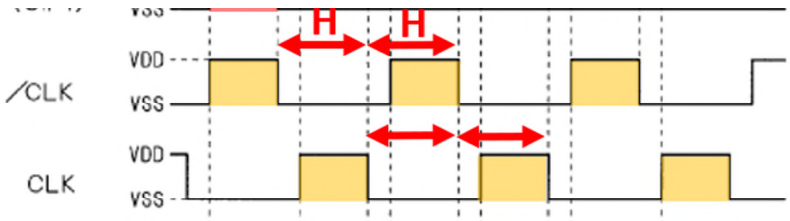
457. Thus, the claim basically states that the amount of time of the period of the recurring waveforms (the first clock signal and the second clock signal) is twice as long as two sub-periods ("H") that, in sum, are the length (in time) of the time it

takes for the recurring waveform to repeat itself. Further, the claim states that these sub-periods sum to "2H" – which means that each sub-period has a duration of H, so that the duration of the two sub-periods is the same.

458. The final stipulation of Claim 4 is that the first clock signal and the second clock signal are "supplied in different horizontal periods as low signals." However, as discussed with respect to Claim 4 in Ground 1, the '593 patent and the reference used in Ground 1 (Chung) both employ pMOS transistors in their disclosed circuitry – and thus, "low signals" specifically mean "turn-on signals."

459. The circuitry disclosed in Tobita uses nMOS transistors rather than pMOS transistors. As was explained in Section VII.A.2, when switching transistors are used, nMOS transistors and pMOS transistors are interchangeable – requiring only minor consequent modifications. Thus, "supplied in different horizontal periods as low signals" that applies directly to the '593 patent (and to Chung and Kim) applies to Tobita in the opposite way – as "supplied in different horizontal periods as *high* signals."

460. That this claim is met by Tobita is made readily evident via examination of an annotated version of Figure 9 of Tobita:



First, it can readily be seen that the CLK and /CLK signals are arranged such that they are supplied in different horizontal periods as high signals. Second, as the annotations show, the period of these two waveforms (CLK and /CLK) is 2H (as discussed above with respect to this Claim), and each waveform is easily divided into two equal sub-periods that each have a time-duration of H.

461. Thus, Tobita renders obvious this claim of the '593 patent.

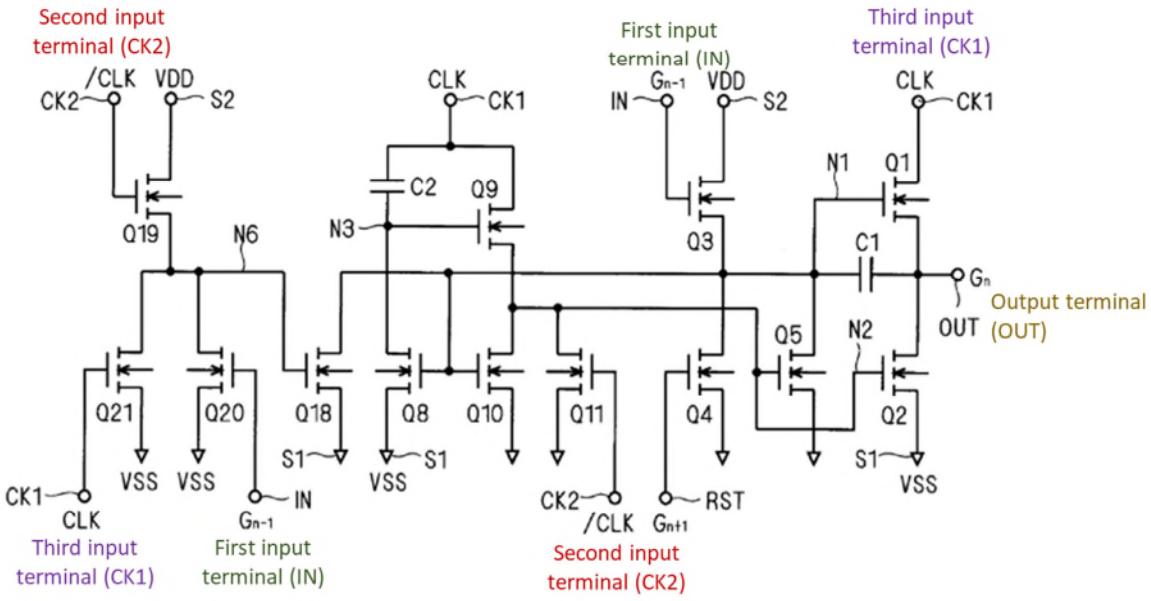
5. Dependent Claim 5

462. As an initial matter, Claim 5 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the '593 patent are disclosed by Tobita.

463. Claim 5 further requires that "the start signal is supplied to overlap the first clock signal."

464. As described earlier (in the discussion of Claim 2 (Section XII.C.2)), in Tobita, the "first clock signal" is the clock signal labeled "/CLK." Further, as was explained in Section XII.C.1.a, the signal that is applied to the input terminal of the stage circuit block is labeled in Figure 20 of Tobita as "G_{n-1}":

FIG. 20



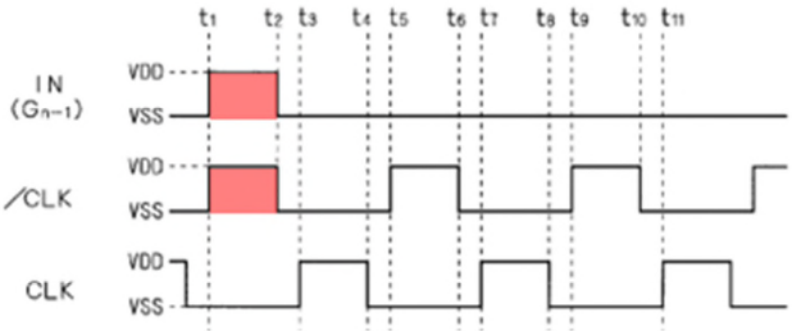
Earlier, in the discussion of Claim 2 (Section XII.C.2), it was shown that Tobita specifically associates a start signal with the first input terminal (IN) of the stage circuit:

> … when the output signal G_{n-1} from the immediately preceding stage (or the start pulse SP in the first stage)… (Tobita at [0086]).
>
> Specifically, each of the unit shift registers SR has its input terminal IN connected to the output terminal OUT of a unit shift register SR of the immediately preceding stage, except that the input terminal IN of the unit shift register SR_1 of the first stage receives a start pulse SP as an input signal. (Tobita at [0094].)
>
> Starting from that mode, the output signal G_{n-1} from the immediately preceding stage (start pulse SP in the case of the first stage), when raised to the H level, is input to the input terminal IN of the unit shift register SR_n … (Tobita at [0098].)

Thus, Tobita treats the output signal G_{n-1} from an immediately preceding stage as being equivalent to the start pulse SP that is received by the first stage (SR_1).

465. The waveforms G_{n-1} and /CLK are both presented in Figure 9 of Tobita.

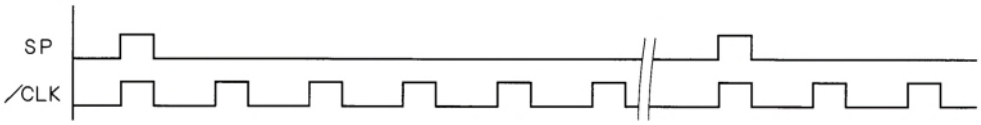
FIG. 9



As can be seen, the signal G_{n-1} goes high (the G_{n-1} "active" level) at the same time and for the same duration that the first clock signal (/CLK) goes high (the /CLK "active" level).

466. Figure 6 of Tobita shows the same sorts of waveforms – except that the start signal (SP) is explicitly included in Figure 6.

FIG. 6



As can be seen, the signal SP goes high (its "active" level) at the same time and for the same duration that the first clock signal (/CLK) goes high (also its "active" level) as part of its recurring square wave behavior.

467. Thus, the start signal (SP) overlaps the first clock signal (/CLK).

468. As noted earlier, Tobita uses nMOS transistors for its switching transistors, rather than the pMOS transistor used in the '593 patent (and in Chung, the reference which undergirds Ground 1). As described at the outset of Section XII.C and with reference back to Section VII.A.2, when used as switching transistors, nMOS transistors and pMOS transistors are interchangeable – with the only minor consequent modifications. Thus, if the transistors in Tobita were changed from nMOS to pMOS, the only change to the signals G_{n-1}, SP, and /CLK would be that they would be changed from active high (for nMOS) to active low (for pMOS); however, as both would be changed in the same way, they would still overlap in the same way – and thus the start signal would still overlap the first clock signal.

469. Thus, Tobita renders obvious this claim of the '593 patent.

6. Dependent Claim 14

470. As an initial matter, Claim 14 depends from Claim 1; as was shown above, Claim 1 of the '593 patent is disclosed by Tobita.

471. Claim 14 further requires that "the transistor controls the voltage of the second node according to the on/off operation thereof." Claim 14 does not provide details regarding which transistor is "the" transistor being described here; however, Claim 1 makes reference to only one transistor– in claim element [1-d] (which was described in Section XII.C.1.e), where this transistor was identified in the claim

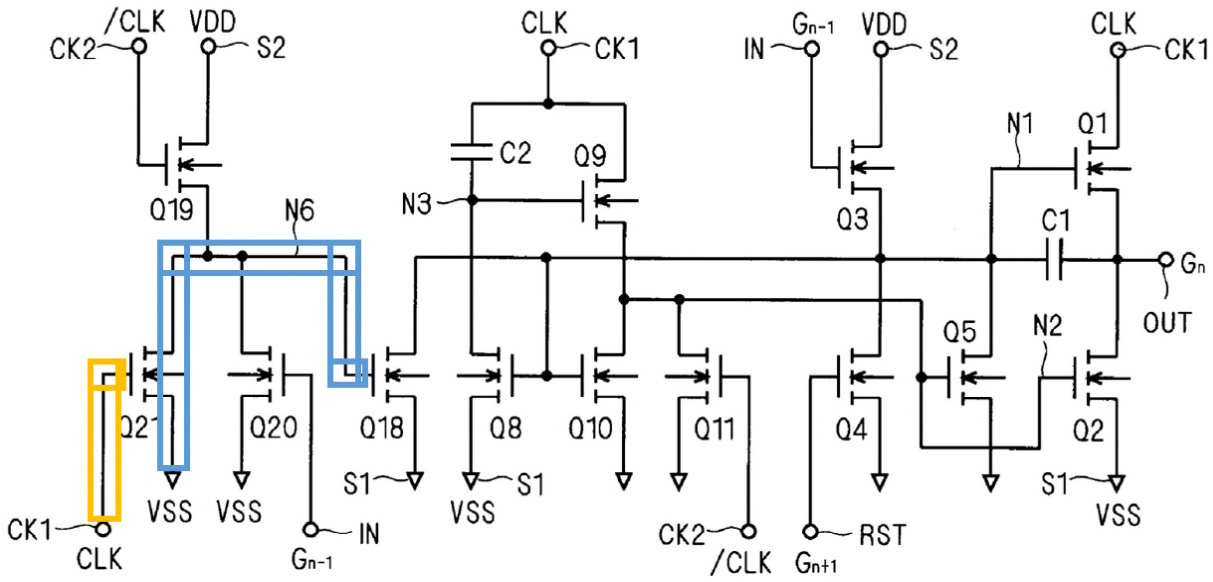
element via "the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver." In Section XII.C.1.e, that transistor was specifically identified as transistor Q21. As was described there, the third input signal ("CK1") is (among other things) connected directly to the gate of transistor Q21, which is part of the first driver; thus, the third input signal directly controls the on/off operation of a transistor (specifically, transistor Q21) that is included in the first driver.

472. In comparison to claim element [1-d], this claim further requires that the on/off operation of this transistor serves to control the voltage of the second node (i.e., "N1"). I understand that in the related ITC proceeding, Patent Owner broadly construed "control" in the phrases "a first/second driver to control the voltage of the second/first node" in Claims 1 and 15. Patent Owner argues that "control" is not limited to "directly control" and includes scenarios where "something other than the driver's output is able to override that output" or where the driver controls the voltage of the node "in conjunction with other circuit elements." EX1009 at 22-23. While I do not agree with that interpretation, I apply it here.

473. That Tobita discloses the additional claim element is readily seen via the examination of an annotated version of Figure 20 of Tobita that was presented in the discussion of claim element [1-b], in Section XII.C.1.c.

Mianyang BOE Ex. 1003
Case No. IPR2023-01221
Page 200 of 273

FIG. 20



As depicted in this annotated version of Figure 20 of Tobita (and as also detailed in Section XII.C.1.c), when the CLK signal applied to the third input terminal (CK1) is pulled high and turns on transistor Q21, the node labeled "N6" is pulled low (to the voltage VSS); this turns off transistor Q18, which serves to prevent the second node (N1) from being pulled low (to the voltage VSS) through Q18. When the CLK signal applied to the third input terminal (CK1) is pulled low and turns off transistor Q21, this functionality is not available.

474. Thus, transistor Q21 controls the voltage of the second node according to the on/off operation of transistor Q21, as just described.

475. Therefore, Tobita renders obvious this claim of the '593 patent at least under Patent Owner's apparent interpretation of the claim.

7. Independent Claim 15

476. It is my conclusion and opinion that Claim 15 of the '593 patent is rendered obvious by Tobita.

a. [15-pre]: "An organic light emitting display, comprising:"

477. As an initial matter, I will be offering no opinion regarding whether or not the preamble of Claim 15 is limiting. I have been instructed by counsel for Petitioner to offer an opinion as to whether or not the prior art discloses or renders obvious the preamble, regardless of whether or not the preamble is limiting.

478. The circuitry disclosed in Tobita is stated as being applied for use with liquid crystal displays (LCDs). As was described in Section VII.B.3, stage circuitry of the type disclosed in the '593 patent can be employed with more than one type of display technology; the same can be said of Tobita. Indeed, the circuity disclosed by the '593 patent performs the function of providing sequences of signals to drive the rows of a display. As discussed above, this structure of having rows of pixels in a display that are sequentially driven is well known, and it is common to most display technologies. For example, U.S. Patent Publication No. 2007/0139348A1 ("Lee") claims an invention comprising stage circuits that can provide scan signals to either LCD or OLED panels. EX1015 at 14-16 (claims 1, 14). Thus, a POSITA would have found it obvious that Tobita's embodiment providing sequential sequencing signals for LCDs could be employed to perform the similar sort of sequential

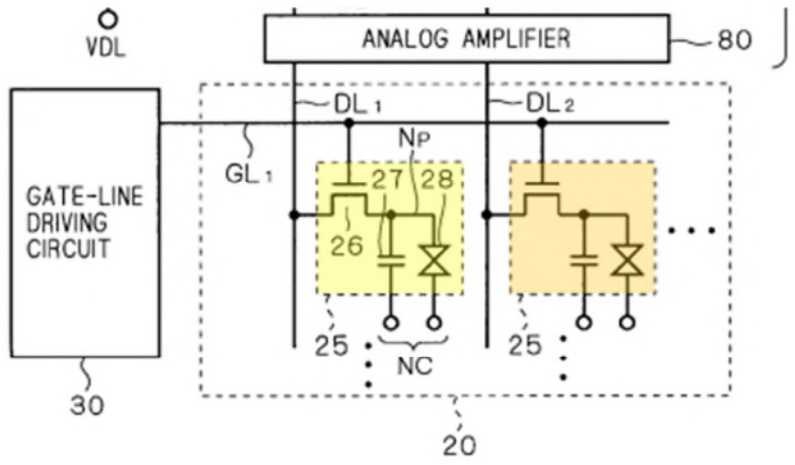
signaling required by an OLED display. This is evident from the similar functionality of the Tobita circuitry as compared to the '593 circuitry.

479. Thus, even if the preamble of Claim 15 is limiting, Tobita renders obvious the preamble of Claim 15 of the '593 patent.

b. [15-a]: "pixels positioned in regions partitioned by scan lines and data lines;"

480. Tobita discloses this claim element of Claim 15 of the '593 patent.

481. This can readily be seen via an annotated excerpt from Figure 1 of Tobita.



(Annotations added.) The details of the structures depicted in this figure are provided by Tobita in the specification.

> The liquid crystal array part 20 includes a plurality of pixels 25 arrayed in a matrix. The columns of pixels (hereinafter also referred to as "pixel lines") are respectively provided with gate lines GL_1, GL_2, #. . . (hereinafter also generically referred to as a "gate line GL), and the rows of pixels (hereinafter also referred to as "pixel rows") are respectively provided with data lines

> DL_1, DL_2, #. . . (hereinafter generically referred to as a "data line DL"). FIG. 1 representatively shows pixels 25 of the first and second rows in the first column and corresponding gate line GL_1 and data lines DL_1 and DL_2.
>
> Each pixel 25 has a pixel switching device 26 disposed between a corresponding data line DL and a pixel node Np, and a capacitor 27 and a liquid crystal display device 28 connected in parallel between the pixel node Np and a common electrode node NC.
>
> (Tobita at [0059] – [0060].)

Note that the "gate lines" of Tobita are the same as the "scan lines" of the '593 patent – as Tobita explicitly states (at, e.g., [0004] ("A gate line (scanning line) is provided for each row of pixels") and at [0058] ("… a gate-line driving circuit (scanning-line driving circuit)…").

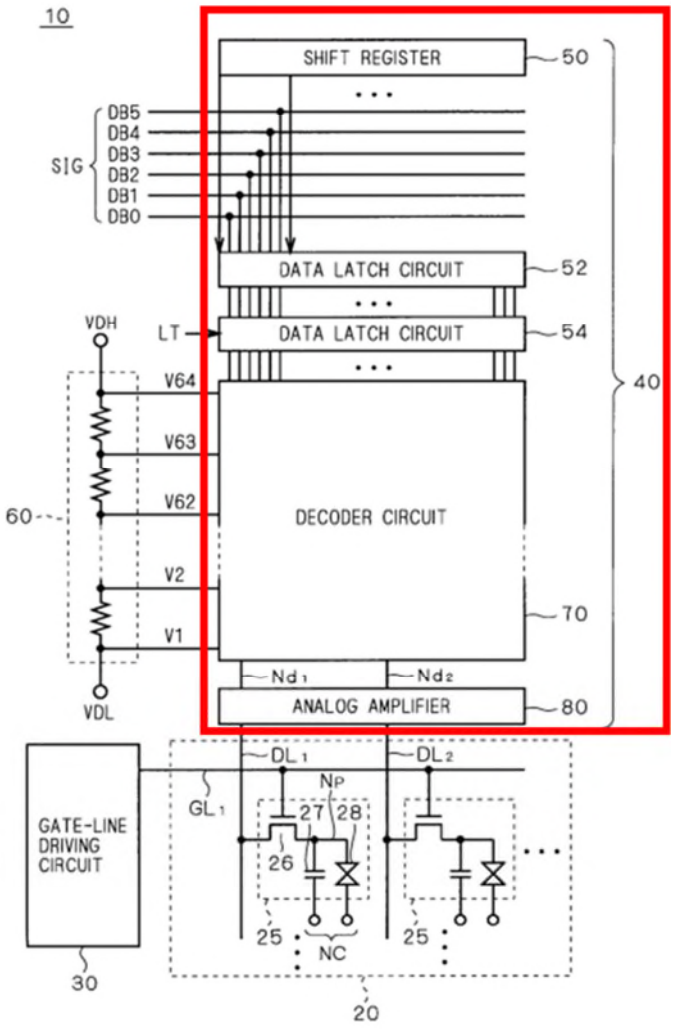
482. Thus, Tobita discloses this claim element of Claim 15 of the '593 patent.

c. [15-b]: "a data driver for supplying data signals to the pixels through the data lines; and"

483. Tobita discloses this claim element of Claim 15 of the '593 patent.

484. This can be readily seen by a more-extensive examination of Figure 1 of Tobita.

F I G . 1



(Annotations added.) The data lines and pixel structures depicted in Figure 1 of Tobita were already explained just above, in the discussion of claim element [15-a] – where, among other things, the lines DL_1, DL_2, … were identified as being data lines. The annotated structure (40) is identified in Tobita as being a "source driver" (e.g., at [0058]). This structure is clearly supplying data signals to the pixels through the data lines; thus, the "source driver" of Tobita is the same thing as the "data driver" of the '593 patent.

485. Therefore, Tobita discloses this claim element of Claim 15 of the '593 patent.

d. [15-c]: "a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal,"

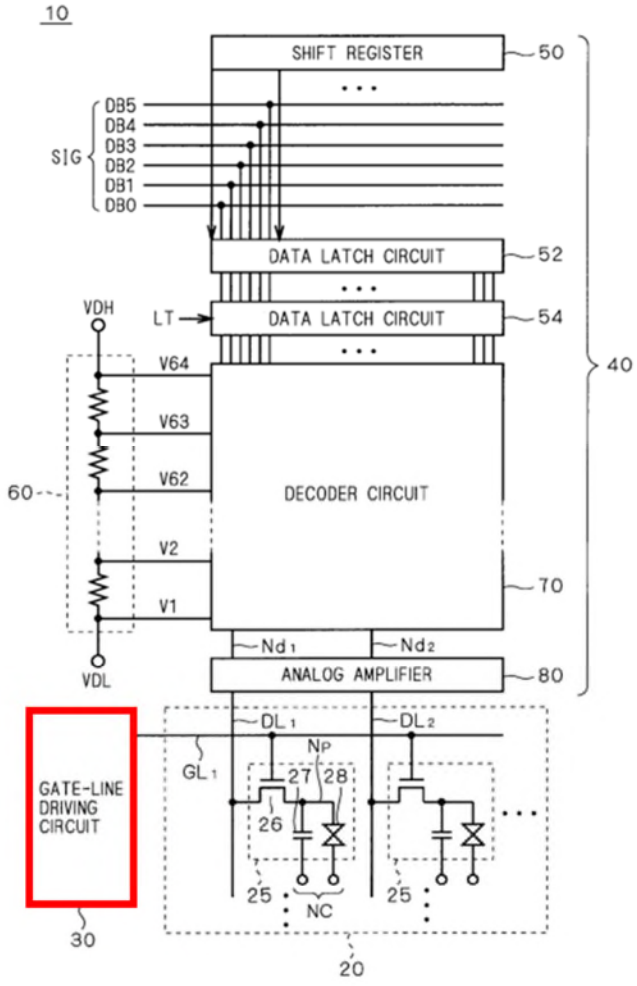
486. Claim element [15-c] is rather long – and thus the analysis will be simpler to explain if this claim element is broken up into sub-elements.

i. [15-c-1]: "a scan driver for supplying scan signals to the pixels through the scan lines"

487. Tobita discloses this claim sub-element of claim element [15-c] of Claim 15 of the '593 patent.

488. This can readily be seen by examination of Figure 1 of Tobita.

F I G . 1



(Annotations added.) As was explained above, Tobita notes (at, e.g., [0004] and [0058]) that the "gate lines" and the "scan lines" are the same thing under two different names. Therefore, the "gate line driving circuit" is the same thing as a "scan line drive circuit" – i.e., it is a scan driver. Further, as was also discussed earlier (in the discussion of claim element [15-a]), the gate/scan driver supplies scan signals to the pixels through the scan lines – as can once again be seen in the annotated figure above.

489. Thus, Tobita discloses this claim sub-element of claim [15-c] of Claim 15 of the '593 patent.

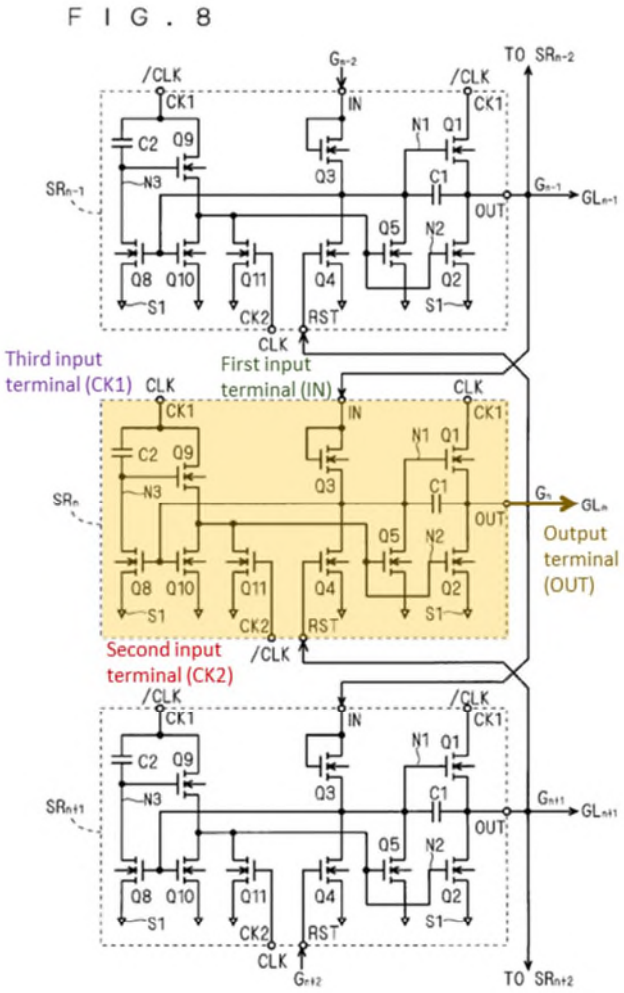
ii. [15-c-2]: "the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals"

490. Tobita discloses this claim sub-element of claim element [15-c] of Claim 15 of the '593 patent.

491. Just above, in the discussion of claim sub-element [15-c-1], it was explained how Tobita describes a "gate line driving circuit" (30) that drives the gate lines that drive the pixels (as a row of pixels) of the display – and how the "gate lines" of Tobita are thus the same thing as the "scan lines" of the '593 patent. Further, Tobita describes the gate line driving circuit (i.e., the scan driver) as follows:

> The gate-line driving circuit 30 includes a plurality of unit shift registers SR1, SR2, SR3, SR4, # ... connected in cascade (Tobita at [0074]; ellipsis in the original.)

492. Tobita describes the inner details of the scan driver in Figure 8.



(Annotations added; the annotation labels were explained earlier, in the discussion of Claim 2.) As can be seen by inspection of Figure 8 of Tobita, the scan driver includes stage circuits (shift registers) that are coupled to the scan lines (which, as detailed above, Tobita calls "the gate lines"). Further, that each of the stage circuits generates a corresponding scan signal of the scan signals was described earlier – in the discussion associated with Claim 1, where the output characteristics of the shift register circuitry were detailed.

493. Thus, Tobita discloses this claim sub-element of claim element [15-c] of Claim 15 of the ‘593 patent.

iii. [15-c-3]: “and having a first input terminal, a second input terminal, a third input terminal, and an output terminal,”

494. This claim sub-element of claim element [15-c] of Claim 15 of the ‘593 patent is disclosed by Tobita.

495. The claim sub-element is essentially identical to the preamble of Claim 1 of the ‘593 patent – which was already discussed in detail earlier (at Section XII.C.1.a) – where it was shown that these details are disclosed by Tobita.

496. Thus, Tobita discloses this claim sub-element of claim element [15-c] of Claim 15 of the ‘593 patent.

iv. Claim Element [15-c] Summary

497. As just demonstrated, Tobita discloses claim sub-elements [15-c-1], [15-c-2], and [15-c-3] of the ‘593 patent; thus, Tobita discloses claim element [15-c] of Claim 15 of the ‘593 patent.

e. Preface to claim elements [15-d] – [15-g]

498. Between claim element [15-c] and claim element [15-d], Claim 15 includes the phrase “wherein each of the stage circuits includes:”. It is taken here that this is intended to mean that “includes” is stated with regard to the sequential

list claim elements which follow for the remainder of Claim 15 – that is, claim elements [15-d], [15-e], [15-f], and [15-g]. Each of these claim elements will be considered in turn.

f. [15-d]: "an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node,"

499. This claim element is identical to claim element [1-a] of Claim 1 of the '593 patent – which was discussed earlier (in Section XII.C.1.b).

500. Thus, Tobita discloses this claim element of Claim 15 of the '593 patent.

g. [15-e]: "a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal, and"

501. This claim element is identical to claim element [1-b] of Claim 1 of the '593 patent – which was discussed earlier (in Section XII.C.1.c).

502. Thus, Tobita discloses this claim element of Claim 15 of the '593 patent.

h. [15-f]: "a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, wherein"

503. This claim element is identical to claim element [1-c] of Claim 1 of the '593 patent – which was discussed earlier (in Section XII.C.1.d).

504. Thus, Tobita discloses this claim element of Claim 15 of the '593 patent.

i. [15-g]: "the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver."

505. This claim element is identical to claim element [1-d] of Claim 1 of the '593 patent – which was discussed earlier (in Section XII.C.1.e).

506. Thus, Tobita discloses this claim element of Claim 15 of the '593 patent.

j. Claim 15 Summary

507. As just shown, Tobita discloses each element of Claim 15 of the '593 patent; thus, Tobita renders obvious Claim 15 of the '593 patent.

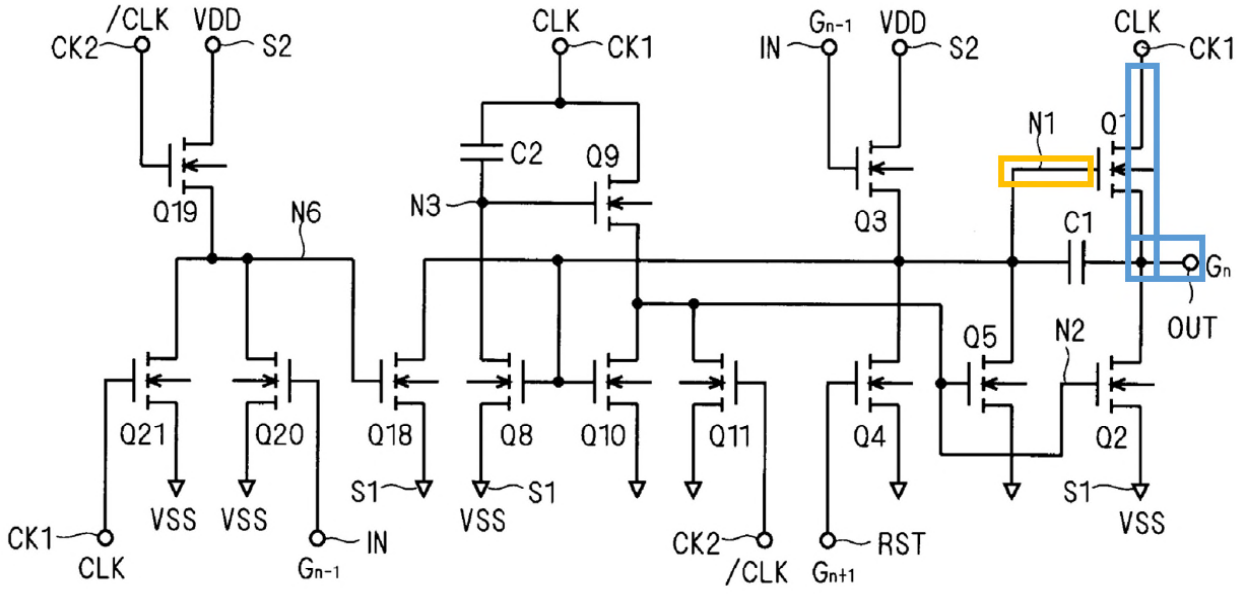
8. Dependent Claim 16

508. As an initial matter, Claim 16 depends from Claim 15; as was shown above, Claim 15 of the '593 patent is disclosed by Tobita.

509. Claim 16 further requires "a clock signal supplied to the third input terminal is used as the scan signal." Tobita discloses this claim of the '593 patent.

510. The first part of this claim element ("a clock signal supplied to the third input terminal") was already discussed earlier (in Section XII.C.1.b.iii) – with respect to claim sub-element [1-a-3] of claim element [1-a] of Claim 1 of the '593 patent. An annotated version of Figure 20 of Tobita was provided there for purposes of explanation – and for clarity, that figure will be repeated here.

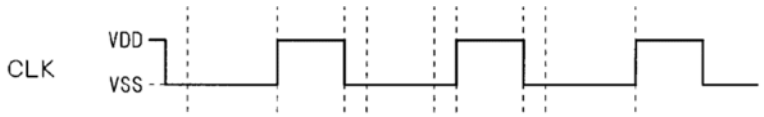
F I G . 2 0



(Annotations added.) As detailed in Section XII.C.1.b.iii, when an appropriate (i.e., turn-on) voltage is applied at the second node (the node labeled "N1"), transistor Q1 will turn on; this will connect the signal of the third input terminal ("CK1") to the node of the output terminal ("OUT") – and thus the signal of the third input terminal ("CK1") is supplied to the output terminal ("OUT"). (On the other hand, when a turn-on voltage is not applied at the second node ("N1"), transistor Q1 will not turn

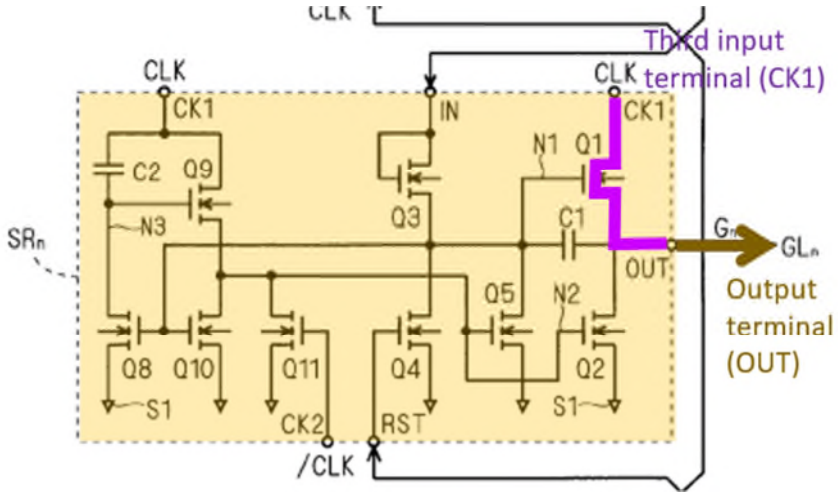
on – and thus the signal of the third input terminal (CK1) is not supplied to the output terminal ("OUT").)

511. As also discussed earlier, the third input terminal (CK1) receives a clock signal – in particular, the clock signal CLK, which is depicted in Figure 9 of Tobita.



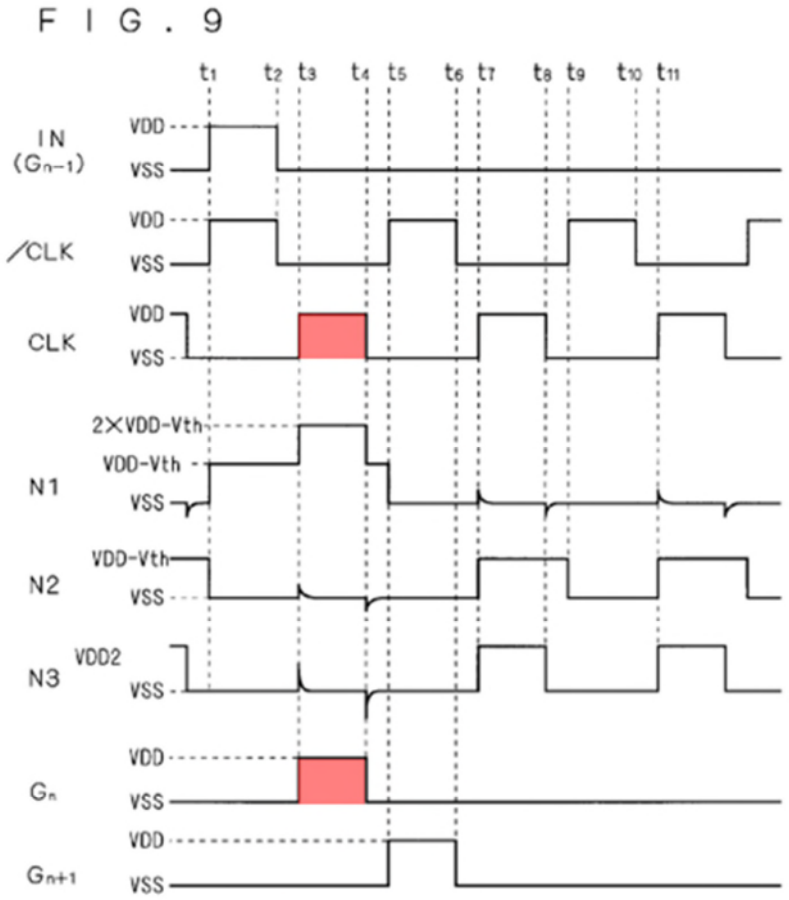
As the name itself implies, the signal CLK is clearly a clock signal – and, as detailed in the discussion of Claim 2, Tobita identifies (e.g., at [0095]) CLK as a clock signal.

512. Finally, with respect to this clock signal being used as "the scan signal," it was shown above (see the annotated version of Figure 20 of Tobita above) that when transistor Q1 is turned on, the input signal that is being applied to the third input terminal CK1 (which, in this case is the clock signal CLK) is supplied to the output terminal OUT. What that signal (at OUT) is being used for is made clear via a partial, annotated version of Figure 8 of Tobita:



As can be seen, the output of the first stage circuit block (SR_n) is being fed to GL_n; as described earlier (in Section XII.C.7.d), the "gate lines" of Tobita are the same thing as the "scan lines" of the '593 patent. (Note also that each stage circuit block (SR_{n-1}, SR_n, SR_{n+1}, …) feeds the output of its OUT terminal to a gate/scan line of its own.)

513. Further, Figure 9 of Tobita shows what use is being made of the clock signal CLK (which is being provided to the output terminal).



As the annotations show, during the period $t_3 – t_4$, the clock signal supplied to the third input terminal (i.e., CLK) is used as the scan signal (i.e., G_n).

514. Therefore, the clock signal that is supplied to the third input terminal is passed to the output terminal (OUT), where it is then used as a scan signal.

515. Thus, Tobita renders obvious this claim of the ‘593 patent.

9. Dependent Claim 17

516. As an initial matter, Claim 17 depends from Claim 15; as was shown above, Claim 15 of the ‘593 patent is disclosed by Tobita.

517. Claim 17 further requires that "the first input terminal receives a scan signal of a previous stage circuit or a start signal."

518. This claim is identical to an element of Claim 2 of the '593 patent – which was discussed earlier (in Section XII.C.2).

519. Thus, Tobita renders obvious this claim of the '593 patent.

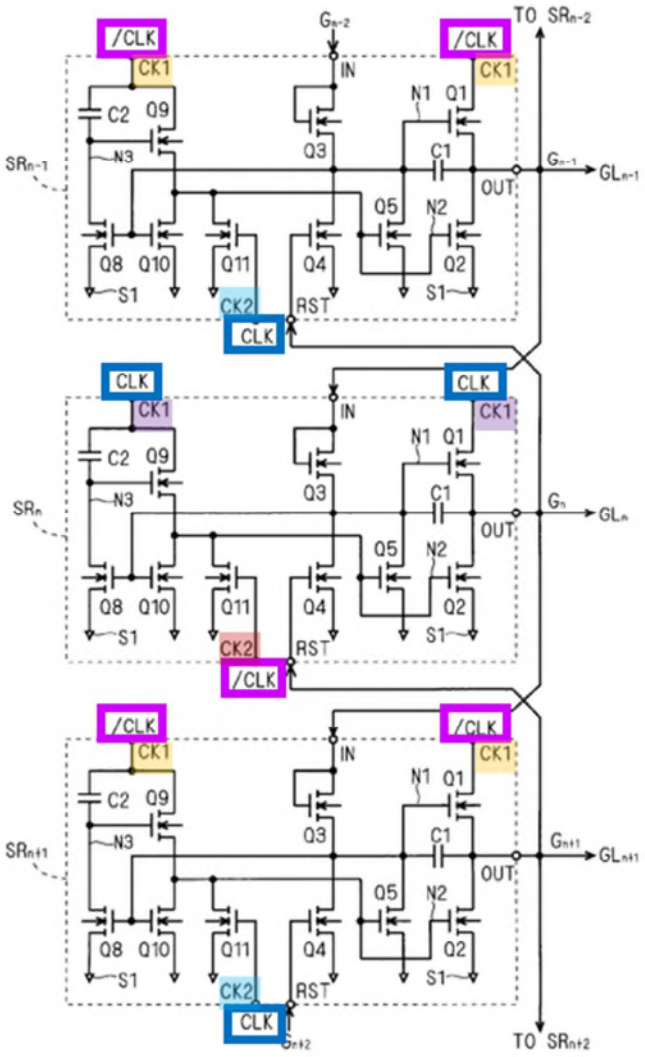
10. Dependent Claim 18

520. As an initial matter, Claim 18 depends from Claim 17, and Claim 17 depends from Claim 15; as was shown above, Claim 15 and Claim 17 of the '593 patent are disclosed by Tobita.

521. Claim 18 further requires "wherein second input terminals of odd stage circuits receive a first clock signal and third input terminals of odd stage circuits receive a second clock signal, and wherein second input terminals of even stage circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal." In other words, the first clock signal and the second clock signal alternate between the second input terminal and the third terminal along the sequence of stage circuits.

522. This is readily demonstrated via an annotated version of Figure 8 of Tobita.

FIG. 8



(Annotations added.) To simplify the explanation of what is going on, the first clock signal (/CLK) is annotated in magenta, and its destinations are highlighted in maroon for odd-numbered stage circuits (G_n, …) and orange for even-numbered stage circuits (G_{n-1}, G_{n+1}, …). The second clock signal (CLK) is annotated in blue, and its destinations are highlighted in purple for odd-numbered stage circuits (G_n, …) and light blue for even-numbered stage circuits (G_{n-1}, G_{n+1}, …). As can be seen by

inspection, the first clock signal (/CLK) goes to the second input terminal (CK2) of the stage circuit SR_n, and to the third input terminal (CK1) of the stage circuits SR_{n-1} and SR_{n+1}; meanwhile the second clock signal (CLK) goes to the third input terminal (CK1) of the stage circuit SR_n, and to the second input terminal (CK2) of the of the stage circuits SR_{n-1} and SR_{n+1}.

523. Tobita, at [0027], describes the stage circuits of Figure 8 as being "connected in a cascade." As was noted earlier, Tobita further describes the meaning of cascade as "The gate-line driving circuit 30 includes a plurality of unit shift registers SR_1, SR_2, SR_3, SR_4, # . . . connected in cascade" (ellipsis in the original); this is also shown in Figure 2 of Tobita (and described at [0073] and [0092] of Tobita), and in Figure 5 of Tobita (and described at [0094] of Tobita).

524. Referring back to Figure 8 (and the annotated version of Figure 8 presented just above), these further explanations of the "cascade" described by Tobita show that the depiction of Figure 8 is an excerpt from a larger cascade of such stage circuits. Further, it is readily understood that if the excerpt were to be (e.g.) expanded from three stage circuits to five stage circuits, so as to include the next stage at the top of the stack in Figure 8 (which would be SR_{n-2}) and the next stage at the bottom of the stack in Figure 8 (which would be SR_{n+2}), the stage circuits SR_{n-2} and SR_{n+2} would be configured exactly as is stage circuit SR_n – with, in

particular, the same locations of the inputs of the first clock signal (/CLK) and the second clock signal (CLK) as in stage circuit SR_n.

525. Therefore, the stage circuits SR_{n-1} and SR_{n+1} (and beyond, in the "cascade") provide the "even stage circuits," while the stage circuits SR_{n-2}, SR_n, and SR_{n+2} (and beyond, in the "cascade") provide the "odd stage circuits." And thus, the second input terminals of odd stage circuits receive a first clock signal and third input terminals of odd stage circuits receive a second clock signal, and the second input terminals of even stage circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal.

526. Thus, Tobita renders obvious this claim of the '593 patent.

11. Dependent Claim 19

527. As an initial matter, Claim 19 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the '593 patent are disclosed by Tobita.

528. Claim 19 further requires that "the first clock signal and the second clock signal have the same period and have phases that do not overlap."

529. This claim is identical to Claim 3 of the '593 patent – which was discussed earlier (in Section XII.C.3).

530. Thus, Tobita renders obvious this claim of the '593 patent.

12. Dependent Claim 25

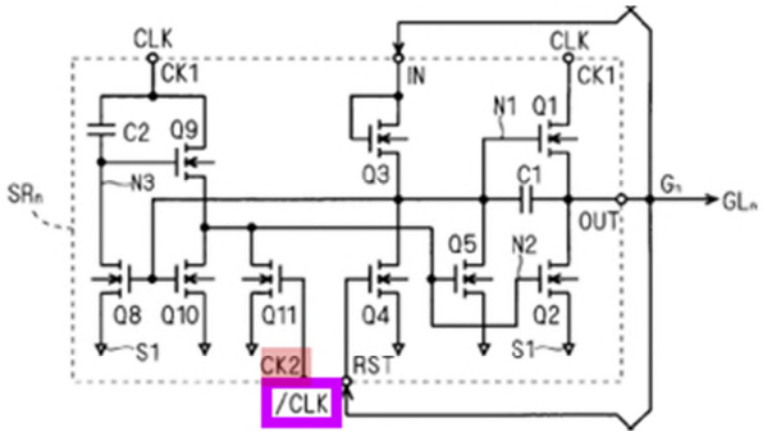
531. As an initial matter, Claim 25 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the '593 patent are disclosed by Tobita.

532. Claim 25 further requires that "the scan signal of the previous stage circuit ***or*** the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal." (Emphasis added.) As per the emphasis added to the word "or" in the claim, Claim 25 of the '593 patent offers two alternatives regarding the provision of a signal to the first input terminal (such that it overlaps the clock signal supplied to the second input terminal).

533. The second alternative specifies that "the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal." As the start signal is always applied to the first input terminal, this form of Claim 25 is thus essentially identical to Claim 5 of the '593 patent (which was discussed earlier, in Section XII.C.5), which requires that "the start signal is supplied to overlap the first clock signal."

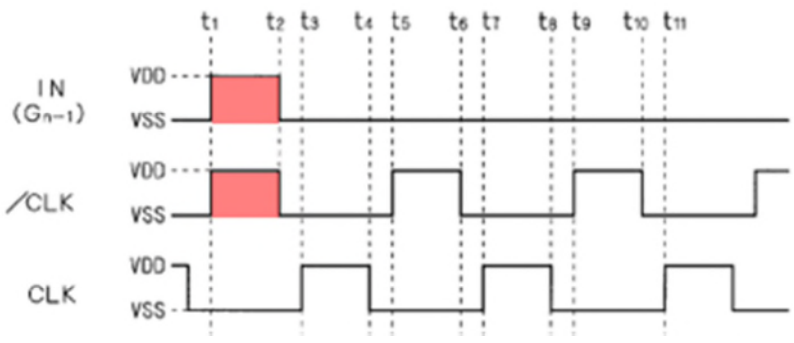
534. On this particular detail of "essentially identical," Claim 5 reads "the start signal is supplied to overlap the first clock signal," while Claim 25 reads "the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal." First, as mentioned above, as the start signal is always

supplied to the first input terminal, this addition to Claim 25 actually adds nothing of substance. Second, the phrase "the clock signal supplied to the second input terminal" will be met in Tobita whenever the first clock signal (i.e., /CLK) is the clock signal that is supplied to the second input terminal – which, as per the discussion associated with Claim 18, is always the case for the "odd-numbered" stage circuits. For example, providing a detail from the annotated version of Figure 8 that was presented as part of the discussion above regarding Claim 18,



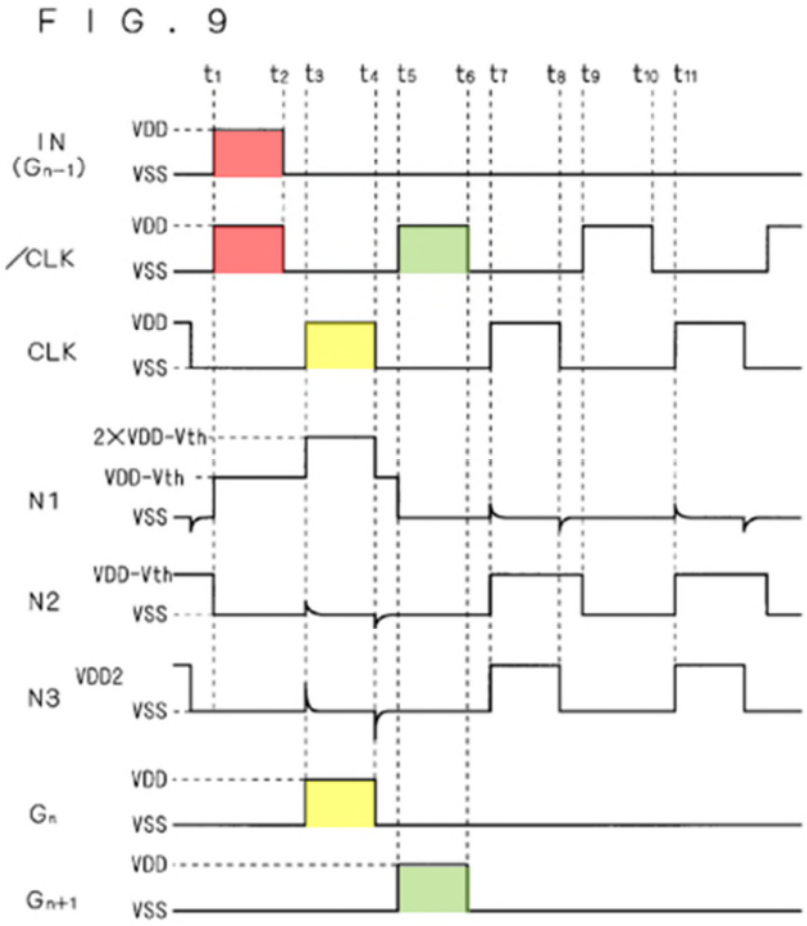
As described above, the first clock signal (i.e., /CLK) is supplied to the second input terminal – and as this annotated version of Figure 9 shows, the start signal (supplied, as always, to the first input terminal) overlaps this clock signal:

FIG. 9



535. On this basis, Tobita renders obvious this claim of the '593 patent.

536. Alternatively, the first alternative specifies that "the scan signal of the previous stage circuit … overlaps the clock signal supplied to the second input terminal." This can be observed in Tobita Figure 9:



537. Recall that the odd stage circuit SR_n, as shown in Tobita Figures 7 and 20, receives the scan signal of the previous stage circuit G_{n-1} at its first input terminal (IN) and the first clock signal /CLK at its second input terminal (CK2). Their overlap is shown above with red annotation.

538. Recall further that, as shown above with respect to Claim 18, the input clock signals that are input to Tobita's stage circuits alternate between odd and even stages. Thus, even stage SR_{n+1} receives the clock signal CLK at its second input terminal (CK2) and receives the scan signal of the previous stage circuit G_n at its first input terminal (IN). Their overlap is shown above with yellow annotation.

539. The next odd stage SR_{n+2} receives the clock signal /CLK at its second input terminal (CK2) and receives the scan signal of the previous stage circuit G_{n+1} at its first input terminal (IN). Their overlap is shown above with green annotation.

540. This pattern would repeat for successive stages of the circuit. For each stage, the output of the previous stage (G_{n-1} for SR_n, G_n for SR_{n+1}, etc.) aligns with the clock signal supplied to the second input terminal – which will be /CLK for odd-numbered stages (e.g., SR_n), and CLK for even-numbered stages (e.g., SR_{n+1}).

541. Therefore, on this separate, second basis, Tobita discloses this claim of the '593 patent.

D. Ground 4: Tobita in View of Jeong and the Knowledge of a POSITA Renders Claims 7 and 21 Obvious

542. As will be discussed below, it is my conclusion and opinion that Claims 7 and 21 of the '593 patent are rendered obvious by Tobita in combination with Jeong and the knowledge of a POSITA.

1. Generalized Motivation to Combine

543. Before going into the details of Ground 4, some of the generalized aspects of the motivation to combine Jeong with Tobita should be considered.

544. As an initial matter, Tobita and Jeong both involve shift register circuitry that forms the basis of a scan driver used in the operation of pixel-matrix displays. Thus, a POSITA would have been aware of both of these references, and would have studied the advantages of these two respective designs. Further, field-effect transistors, circuits based on them, and the use of such circuits for the drivers in a pixel-matrix display, were well known in the art – and had been well known for years prior to 2012. Therefore, a POSITA at the time of the alleged inventions of the '593 patent would have had extensive knowledge about such circuits and their usage. Accordingly, it would have been sensible for a POSITA to integrate compatible circuits, so as to garner respective advantages of two or more references. Further, because the circuit design and circuit operation principles were already well known in the art, such combinations would have yielded predictable results.[15]

545. Further, a POSITA would have been motivated to combine Tobita with Jeong because, as noted above, both involve the use of shift registers to provide scan

[15] As per some of the references cited in Section VII.A, this knowledge predates the '593 patent by an extensive period of time – with one of the references cited going back to 1967.

drivers for use in pixel-based displays. Both Tobita and Jeong use field-effect transistors, and in each reference the circuits disclosed use only one species (either nMOS or pMOS) of field-effect transistor. As per the discussion in Section VII.A.2, while Tobita's disclosed circuitry uses nMOS transistors and Jeong's disclosed circuity uses PMOS transistors, the ability to change switching transistors from nMOS to pMOS (or vice versa), along with the operational changes necessary for this change, were well known in the art at the time of the '593 patent. Further, the similarity of the functions and designs of Tobita and Jeong would have further confirmed to a POSITA that combining the teachings of these two references would involve straightforward modifications (as discussed just above) – with both predictable outcomes and a reasonable expectation of success.

546. Finally, a POSITA would have observed that Tobita's outputting unit and Jeong's outputting unit share what are essentially the same components in the same configuration – and thus Jeong is close enough to Tobita to make the combination of details from Jeong into Tobita a reasonable prospect.

2. Dependent Claim 7

547. As an initial matter, Claim 7 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above (in Section XII.C), Claim 1 and Claim 2 of the '593 patent are rendered obvious by Tobita.

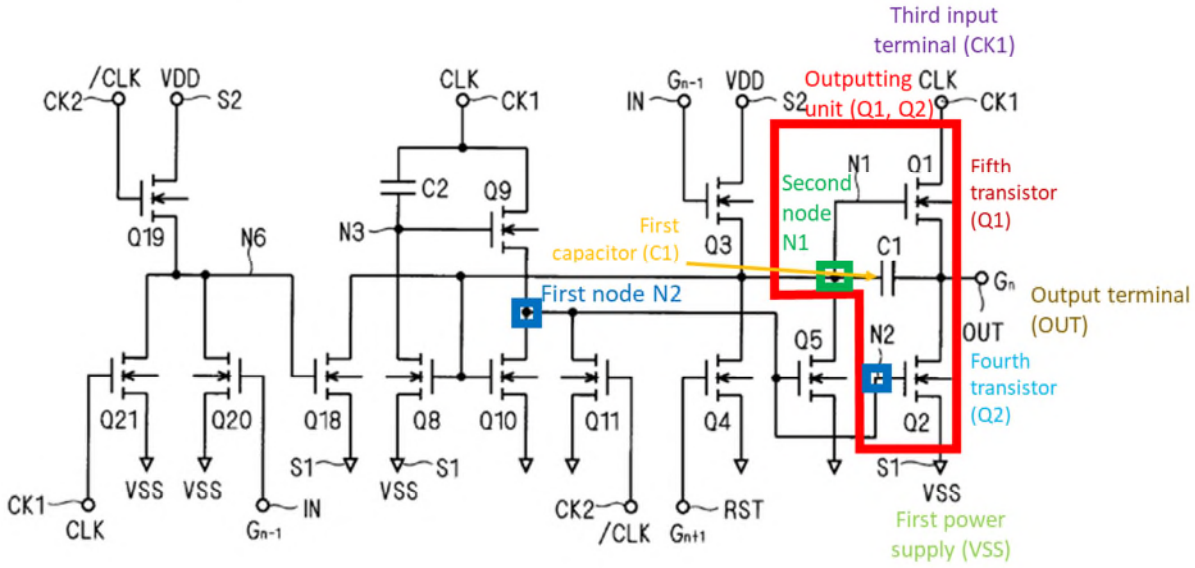
548. Claim 7 further requires:

> wherein the outputting unit includes:
>
> a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node;
>
> a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node;
>
> a first capacitor between the second node and the output terminal; and
>
> a second capacitor between the first node and the first power supply.

As will be shown here, Tobita combined with Jeong and the knowledge of a POSITA renders obvious this claim of the '593 patent.

549. Simple inspection of the circuitry of Figure 20 of Tobita shows that this circuitry contains all of the elements recited in Claim 7, arranged in the configuration that is recited in Claim 7 – with the exception of the second capacitor, which is not present in the circuitry of Figure 20 of Tobita.

F I G . 2 0



A POSITA examining this circuitry would reach several conclusions – since these conclusions are well-known in the art.

550. First, a POSITA would recognize that the first node (N2) that will be electrically isolated whenever the three transistors which provide electrical access to this node (Q9, Q10, and Q11) are all turned off. Second, a POSITA would also understand that the amount of charge stored at the node would determine the isolated voltage at that node using the simple and well-known equation

$$Q = CV,$$

where Q is the charge on the node, V is the resulting voltage at the node, and C is the capacitance at the node. For example, if the first capacitor (C1) were not there, then the capacitance would be supplied only by the wiring to which the node is connected; however, as wiring holds very little charge, it has very little capacitance

– and thus, the resulting voltage value will be based upon a very small amount of charge.

551. This can be problematic, since perturbations in the amount of charge (due to, for example, electromagnetic interference (EMI)) may cause sizeable changes in the voltage on the node – which, given that output voltage is being used to control the voltage terminal, is undesirable. Therefore, a POSITA would be motivated to seek methods of making the circuitry of Tobita more robust against a problem of this sort.

552. In addition, the "isolation" of this node is being provided by turning off all the transistors that provide electrical connection(s) to that node when any one of them is turned on – and, as described above, examination of Figure 20 of Tobita indicates that that there are three such transistors (Q9, Q10, Q11) that provide electrical connections to the first node (N2), and the first node (N2) is isolated when all of these transistors are turned off. However, as described in Section VII.A.4, a transistor does not turn off perfectly – and some off-state leakage current will be present. If the voltage at the isolated first node (N2) is defined by a very small amount of charge, then that charge will leak away very quickly via the imperfect off-state of the transistors – and the voltage will change quickly with time, and may even quickly reach the low (VSS) voltage as its inevitable endpoint.

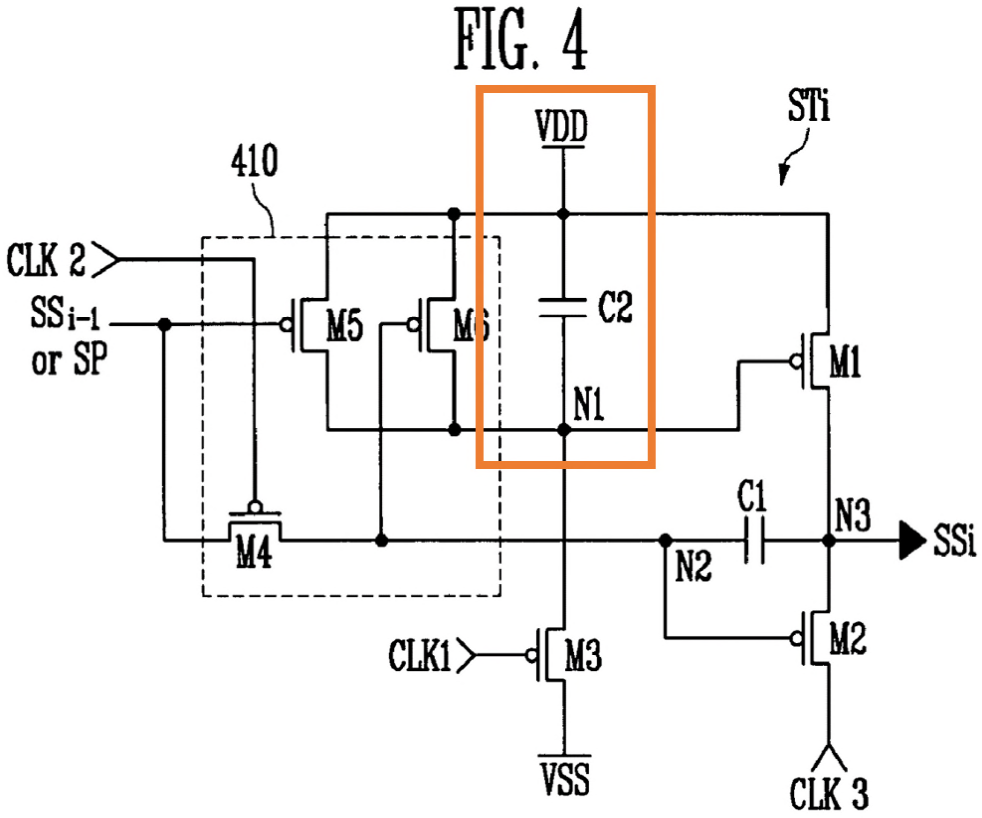
553. As a POSITA would thus know, the voltage at this node would be made more robust (i.e., it would be able to hold the isolated voltage value more stably against upsets like EMI, and would take a long time to drain the charge away through the imperfect off-state transistors and thus would retain the isolated voltage much longer) if the capacitance at the node could be increased. This is actually quite easily done – by adding a capacitor to the isolated node, so that the amount of charge used to create the voltage at the node is much larger; as can readily been seen from the equation presented above, for the same voltage, a larger capacitance would hold a proportionately larger charge.

554. Thus, a POSITA looking at the circuitry of Tobita would realize that these vulnerabilities exist. Further, even though Tobita states that the capacitor C1 is included for the purpose of "bootstrapping" the second node (N1), a capacitor at this location in the circuitry can also make the charge on the second node (N1) more robust when that node is charged up and is then electrically isolated from the rest of the circuitry.

555. Thus, it would be a relatively straightforward decision to conclude that the first node (N2) in Tobita should have a capacitor included and connected to it – for the reasons just cited above.

556. One simple method for adding a capacitor to accomplish this would be to connect that capacitor between the first node (N2) (the required connection) and a DC power supply voltage (the optional-location-choice connection).

557. A simple example of this insertion is provided by Jeong, at Figure 4:



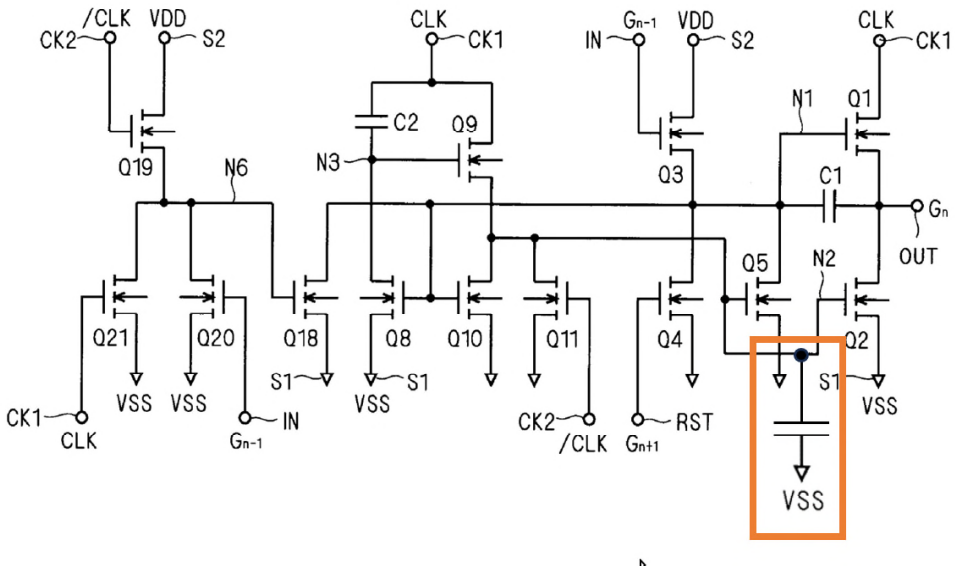
(Annotation added.) As can be seen by inspection, when the transistors M5 and M6 are turned off, the node N1 is electrically isolated – and will retain the charge (and thus the corresponding voltage) that is present there. For the reasons detailed above (i.e., increasing the robustness of the voltage that is present at the node N1), the capacitor C2 is added. As Jeong explains,

> The second capacitor C2 may be coupled between the first power supply VDD and the first node N1. The second capacitor C2 may *function to reduce a variation of a voltage*, which may be applied to the first power supply VDD or the first node N1. (Jeong at [0057]; emphasis added.)

This is a description of the enhanced robustness of the voltage present at the node N1, consistent with what was discussed above.

558. As an example, this capacitor could be added to the circuitry of Figure 20 of Tobita in the following manner:

FIG. 20



(Highlighted added capacitor and annotations added.) This capacitor is connected between the first node and the first power supply.

559. Thus, Tobita in view of Jeong and the knowledge of a POSITA renders obvious this claim of the '593 patent.

3. Dependent Claim 21

560. As an initial matter, Claim 21 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above (in Section XII.C), Claim 15, Claim 17, and Claim 18 of the '593 patent are disclosed by Tobita.

561. This claim is identical to Claim 7 of the '593 patent – which was discussed just above (in Section XII.D.1).

562. Thus, Tobita in view of Jeong and the knowledge of a POSITA renders obvious this claim of the '593 patent.

XIII. SECONDARY CONSIDERATIONS

563. I am not aware of any secondary considerations of non-obviousness that are relevant to the challenged claims. If I later become aware of arguments of any secondary consideration, I may assess those arguments when they arise, in order to form opinions regarding their correctness; I reserve the right to file supplemental declarations should such circumstances occur. In any event, it is my opinion that, even if Patent Owner proffers evidence of secondary considerations of non-obviousness, such evidence cannot overcome the showing of obviousness through the prior art references analyzed in this Declaration.

XIV. CONCLUSION

564. As per the analysis presented above, it is my conclusion and opinion that Claims 1-9, 14-23, and 25 of the '593 patent are unpatentable. It is thus my

Mianyang BOE Ex. 1003
Case No. IPR2023-01221
Page 233 of 273

further conclusion and opinion that IPR proceedings regarding the '593 patent should be instituted, and that the challenged claims should be cancelled as unpatentable.

565. I am aware that this declaration will be filed as evidence in an IPR proceeding before the PTAB. I am aware that making willfully false statements in my declaration are punishable by fine or imprisonment, or both (under 18 U.S.C. § 1001), and that such actions may compromise the validity of the IPR Petition. All statements herein made by me of my own knowledge are true, and all statements made on information and belief are believed to be true.

566. I declare under penalty of perjury that the foregoing is true and correct. Executed this 26th day of July, 2023 in Fletcher, Vermont.



Daniel Foty, Ph.D.

APPENDIX A

DANIEL FOTY, Ph.D.

SUMMARY

Dr. Foty has more than 30 years of engineering and management experience in the mainstream of the technology industry. During this time, he has worked in semiconductor physics, device design, process integration, modeling/simulation (process, device, and circuit), circuit design/analysis, and wireless communications. After seven years at the microelectronics unit of IBM, he founded his own consulting firm, Gilgamesh Associates, LLC, which works in very demanding areas of technology design and development such as analog, mixed-signal, RF, signal processing, wireless communications, and ultra-low-power design.

Dr. Foty is also an advisor to the Tallinn University of Technology (Estonia) and the University of Pretoria (South Africa). He is also the author of *MOSFET Modeling with SPICE: Principles and Practice*, the more-recent *Moore's Law: The Untold* Story, and several other books. He has also authored well over 100 journal articles and conference presentations, and is a frequent plenary (keynote) speaker at major international conferences throughout the world. He is also a licensed pilot and aircraft owner, possesses both an instrument rating and a seaplane rating, and is a registered "angel pilot" with Patient Airlift Services.

Expertise

- Analog/Mixed-Signal/RF CMOS
- CMOS Integrated Circuit Design
- IC Modeling/Simulation
- CMOS Technology and Process Integration
- Semiconductor Manufacturing/Fabrication
- Nanotechnology
- Design Automation (EDA) Software
- Semiconductor Memory (DRAM, SRAM, Flash)
- Semiconductor Physics
- RF/Radio Technology, Wireless Networks, and Wireless Communications
- Power Management
- Digital Communications, Signal Integrity, and Electromagnetic Interference
- Cryogenic Electronics

PROFESSIONAL EXPERIENCE

1994 to Present **Gilgamesh Associates, LLC**
President

- Analysis of analog/mixed-signal/RF CMOS circuits
- New technologies in high-speed wireless data communications
- Specialized process-design-kits (PDKs) for circuit design/simulation
- Foundry interfacing for fabless IC design companies
- Professional education via short courses and lectures
- Litigation support in various aspects of the integrated circuit industry

1988 to 1994 **IBM Microelectronics Division**
Scientist/Engineer

- Process integration, device design, semiconductor/IC physics
- Process and device simulation; circuit simulation
- Process and device integration for memory and logic technologies
- Process-design-kits (PDKs) for circuit simulation
- Spearheaded initial IBM foray into OEM foundry market; responsible for all "external customer" PDKs and support/interfacing; business grew from nothing to $66M in revenue in first year.

EDUCATION

Ph.D., Materials Science, University of Vermont, 2001
MS, Electrical Engineering, University of Illinois, 1985
BS, Physics and Chemistry, Bates College, 1983

LITIGATION RELATED EXPERIENCE

Dr. Foty has served as a testifying expert, and provided declarations, expert reports, trial testimony, and arbitration-hearing testimony for cases that have touched on the complete spectrum of semiconductor/electronics engineering issues, electronic design automation software, wireless technology, contract interpretations and business processes, and prior art searches in both patents and the public-domain literature. He has also served as a consulting expert. Dr. Foty has been deposed some thirty times, and has testified at trial six times. Below are matters in which he has written expert reports and given testimony either at deposition, trial, or before an arbitration panel.

Type of Matter:	*Inter Partes* review involving power conversion technology in solar power systems
Law Firm:	Sheridan Ross LLP, Denver, Colorado
Case Name:	SolarEdge Technologies, Ltd. v. Koolbridge Solar, Inc.
Represented:	Patent holder
Case Number:	IPR2022-00007, -00010, -00013
Filing Date:	10/11/2021, 10/11/2021, 10/8/2021
Court:	Patent Trial and Appeal Board
Disposition:	Prepared three declarations supporting the patent holder; deposed; ongoing.
Date:	June 2022 – present.

Type of Matter:	Patent infringement involving wireless communications technology
Law Firm:	Folio Law Group, LLP, Seattle, Washington
Case Name:	Dali Wireless v. Corning
Represented:	Patent holder
Case Number:	6:20-cv-00827-ADA
Filing Date:	10/22/2020
Court:	US District Court District of the Western District of Texas
Disposition:	Prepared an expert report, deposed; ongoing.
Date:	November 2021 – present.

Type of Matter:	Patent infringement involving integrated circuit layout for lithographic control
Law Firm:	Jones Day LLP, Chicago, Illinois
Case Name:	NXP Semiconductors v. Impinj
Represented:	Plaintiff
Case Number:	2:20-cv-01503-RSM-SKV337-TA-1272
Filing Date:	10/7/2020
Court:	US District Court of the Western District of Washington,
Disposition:	Ongoing.
Date:	November 2021 – present.

Type of Matter:	Patent infringement involving integrated circuit technology
Law Firm:	Jones Day LLP, Washington DC (ITC matter)
Case Name:	MediaTek v. NXP Semiconductors
Represented:	Respondent
Case Number:	337-TA-1272
Filing Date:	6/21/2021
Court:	International Trade Commission
Disposition:	Ongoing.
Date:	April 2021 – present.

Type of Matter:	Patent infringement involving portable vehicle battery jump starters
Law Firm:	Fox Rothschild LLP, Philadelphia, Pennsylvania (ITC matter)
Case Name:	The Noco Company v. Deltran Global
Represented:	Respondent
Case Number:	337-TA-1256
Filing Date:	1/19/2021
Court:	International Trade Commission
Disposition:	Prepared an expert report; deposed; plaintiff withdrew complaint against Deltran.
Date:	June 2021 – November 2021.

Type of Matter:	Patent infringement involving integrated circuit technology and signal integrity
Law Firm:	Jones Day LLP, Chicago, Illinois
Case Name:	WSOU v. Xilinx
Represented:	Respondent
Case Number:	1:20-cv-01228-CFC; 1:20-cv-01229-CFC
Filing Date:	09/16/2020
Court:	US District Court District of Delaware
Disposition:	Ongoing.
Date:	April 2021 – present.

Type of Matter:	Patent infringement involving wireless communications technology
Law Firm:	Folio Law Group, LLP, Seattle, Washington
Case Name:	Dali Wireless v. JMA
Represented:	Patent holder
Case Number:	1:19-cv-02367-RGA
Filing Date:	12/30/2019
Court:	US District Court District of Delaware
Disposition:	Settled.
Date:	March 2021 – November 2021.

Type of Matter:	Patent infringement involving wireless communications technology
Law Firm:	Folio Law Group, LLP, Seattle, Washington

Case Name:	Dali Wireless v. Commscope
Represented:	Patent holder
Case Number:	1:19-cv-00952
Filing Date:	5/22/2019
Court:	US District Court District of Delaware
Disposition:	Prepared an expert report; deposed; ongoing.
Date:	March 2021 – present.
Type of Matter:	Patent infringement involving integrated circuit technology (ITC matter)
Law Firm:	Troutman Pepper LLP, Boston, Massachusetts
Case Name:	Tela v. Intel
Represented:	Patent holder
Case Number:	337-TA-1246
Filing Date:	12/18/2020
Court:	International Trade Commission
Disposition:	Settled; this includes all prior disputes between the parties
Date:	March 2021 – April 2021.
Type of Matter:	Patent infringement involving wireless battery charging and discharging
Law Firm:	Feinberg Day Kramer Alberti Limtonkovich & Belloli LLP
Case Name:	Garrity Power Services v. Samsung
Represented:	Patent holder
Case Number:	2:20-cv-00269-JRG
Filing Date:	08/17/2020
Court:	US District Court Eastern District of Texas
Disposition:	Case dismissed by the Court
Date:	October 2020 – March 2022.
Type of Matter:	*Inter Partes* review involving wireless battery charging and discharging
Law Firm:	Spencer Fane LLP, Plano, Texas
Case Name:	Samsung v. Garrity Power Services
Represented:	Patent holder
Case Number:	IPR2021-00389
Filing Date:	12/31/2020
Court:	Patent Trial and Appeal Board
Disposition:	Prepared a declaration; PTAB denied institution.
Date:	October 2020 – July 2021.
Type of Matter:	Patent infringement involving MOS transistor design and MOS transistor manufacturing processes
Law Firm:	Fish & Richardson LLP, Boston, Massachusetts
Case Name:	Innovative Foundry Technologies v. SMIC, Broadcom, Cypress Semiconductor, and Dish Network
Represented:	Respondents

Case Number:	6:19-cv-00719-ADA
Filing Date:	12/20/2019
Court:	US District Court Western District of Texas
Disposition:	Settled
Date:	June 2020 – April 2021.
Type of Matter:	Patent infringement involving digital communications integrated circuit technology
Law Firm:	Morrison & Foerster LLP, Los Angeles, California
Case Name:	Analog Devices v. Xilinx
Represented:	Respondent
Case Number:	1:19-cv-02225-RGA
Filing Date:	12/05/2019
Court:	US District Court District of Delaware
Disposition:	Ongoing.
Date:	April 2020 – present.
Type of Matter:	Patent infringement involving integrated circuit technology
Law Firm:	Pepper Hamilton LLP, Boston, Massachusetts
Case Name:	Intel v. Tela
Represented:	Respondent
Case Number:	3:18-cv-02848-WHO
Filing Date:	05/15/2018
Court:	US District Court Northern District of California
Disposition:	Prepared two expert reports; deposed; matter settled.
Date:	March 2019 – April 2021.
Type of Matter:	Patent infringement involving integrated circuit technology (ITC matter)
Law Firm:	Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C., Boston, Massachusetts
Case Name:	Globalfoundries v. TSMC
Represented:	Patent holder
Case Number:	337-TA-1177
Filing Date:	08/26/2019
Court:	International Trade Commission
Disposition:	Settled.
Date:	August 2019 – October 2019.
Type of Matter:	*Inter Partes* review involving wireless/RF technology
Law Firm:	Jones, Day LLP, Cleveland, Ohio
Case Name:	Intel v. Qualcomm
Represented:	Patent holder
Case Number:	IPR2019-00128, IPR2019-00129, IPR2019-00047, IPR2019-00048, IPR2019-00049
Filing Date:	11/8/2018
Court:	Patent Trial and Appeal Board

Disposition:	Prepared five declarations supporting patent owner responses; deposed; PTAB upheld all challenged claims of the patent as valid.
Date:	June 2019 – July 2020.
Type of Matter:	Patent infringement involving integrated circuit technology
Law Firm:	Pepper Hamilton LLP, Boston, Massachusetts
Case Name:	Tela v. Intel
Represented:	Patent holder
Case Number:	337-TA-1148
Filing Date:	12/19/2018
Court:	International Trade Commission
Disposition:	Prepared two declarations supporting claim construction; prepared an expert report; deposed; testified at the hearing/trial in December 2019.
Date:	March 2019 – December 2019.
Type of Matter:	Patent infringement involving RF/wireless technology
Law Firm:	Quinn Emanuel Urquhart & Sullivan LLP, New York, New York
Case Name:	Qualcomm v. Apple
Represented:	Patent holder
Case Number:	3:17-cv-02402-CAB-MDD
Filing Date:	12/29/2017
Court:	US District Court Southern District of California
Disposition:	Settled.
Date:	January 2018 – December 2018.
Type of Matter:	Patent infringement involving RF/wireless technology
Law Firm:	Quinn Emanuel Urquhart & Sullivan LLP, New York, New York
Case Name:	Qualcomm v. Apple
Represented:	Patent holder
Case Number:	337-TA-1093
Filing Date:	7/7/2017
Court:	International Trade Commission
Disposition:	Prepared two expert reports regarding RF-IC/wireless technology; deposed; testified at the hearing/trial in September 2018.
Date:	January 2018 – September 2018.
Type of Matter:	Patent infringement involving integrated circuit technology and printed-circuit board technology
Law Firm:	Dovel and Luner, LLP, Santa Monica, California
Case Name:	X2Y v. Intel
Represented:	Patent holder
Case Number:	3:18-cv-01394-HZ
Filing Date:	07/25/2018
Court:	US District Court District of Oregon
Disposition:	Prepared a declaration supporting claim construction; deposed; case settled.

Date:	June 2017 – December 2019.
Type of Matter:	Patent infringement involving integrated circuit technology
Law Firm:	Jones, Day LLP, San Francisco, California, and Slater Matsil LLP, Dallas, Texas
Case Name:	IPBridge v. Xilinx
Represented:	Respondent
Case Number:	3:17-cv-06376-JD
Filing Date:	11/01/2017
Court:	US District Court Northern District of California
Disposition:	Settled.
Date:	February 2017 – February 2019.
Type of Matter:	Patent infringement involving analog circuits
Law Firm:	Covington & Burling LLP, San Diego, California
Case Name:	Tessera v. Broadcom
Represented:	Patent holder
Case Number:	1:16-cv-00380-LPS-CJB
Filing Date:	05/23/2016
Court:	US District Court District of Delaware
Disposition:	Settled.
Date:	December 2016 – December 2017.
Type of Matter:	Patent infringement involving integrated circuit design methods and integrated circuit design-automation software
Law Firm:	Jones, Day LLP, Cleveland, Ohio
Case Name:	Synopsys v. ATopTech
Represented:	Patent holder
Disposition:	Prepared an expert report; deposed; matter was suspended when ATopTech filed for Chapter 11 bankruptcy.
Date:	June 2016 – March 2017.
Type of Matter:	Patent infringement involving integrated circuit process/manufacturing technology for wireless communications
Law Firm:	McKool Smith, LLP, Dallas, Texas
Case Name:	Ericsson v. TCL
Represented:	Plaintiff
Disposition:	Prepared an expert report regarding the costs and timelines associated with the development of integrated circuits for wireless communications, and the related difficulties encountered; trial was stayed when an IPR proceeding began, matter has since ended.
Date:	November 2015 – March 2016.
Type of Matter:	*Inter Partes* review involving integrated circuit design methods and integrated circuit design-automation software
Law Firm:	Jones, Day LLP, Cleveland, Ohio
Case Name:	ATopTech v. Synopsys

Represented:	Patent holder
Disposition:	Prepared two declarations; deposed.
Date:	November 2014 – January 2016.
Type of Matter:	*Inter Partes* review involving a semiconductor flash memory technology patent
Law Firm:	Aka Chan LLP, Santa Clara, California
Case Name:	Silicon Motion Technology Corp. v. Phison Electronics Corp.
Represented:	Petitioner
Disposition:	Prepared a declaration; deposed; hearing before the PTAB in September 2014, PTAB ruled completely in Petitioners' favor
Date:	May 2014 – September 2014.
Type of Matter:	Patent infringement involving integrated circuit design
Law Firm:	Bragalone, Conroy, PC, Dallas, Texas
Case Name:	HSM v. Elpida Memory et al. (was HSM v. Fujitsu et al.)
Represented:	Plaintiff
Disposition:	Prepared numerous declarations and two expert reports; deposed; all respondents eventually settled.
Date:	February 2012 – February 2016.
Type of Matter:	Patent infringement involving integrated circuit process/manufacturing technology (ITC matter)
Law Firm:	McKool Smith, LLP, Dallas, Texas
Case Name:	Samsung v. Ericsson
Represented:	Defendant
Disposition:	Was assigned one patent in a larger matter, having done much original engineering work on the technology in question; produced extensive background prior art (having created much of it), demonstrated that the accused technology clearly did not practice the teachings of the patent, and clearly showed that the aforementioned prior art would call the patent's validity seriously into question; plaintiff dropped that patent from the action.
Date:	January 2013 – May 2013.
Type of Matter:	Patent infringement involving integrated circuit design, with a focus on RF-ICs for wireless communications
Law Firm:	Antonelli, Harrington, & Thompson, LLP, Houston, Texas
Case Name:	Semiconductor Ideas to the Market, BV v. Texas Instruments et al.
Represented:	Plaintiff
Disposition:	Prepared a declaration for pre-hearing; major defendant (Qualcomm) settled following this expert's examination of their Confidential Business Information (CBI) in June, 2012; other defendants settled shortly thereafter.
Date:	May 2012 – August 2012.
Type of Matter:	Bond forfeiture proceeding (ITC matter)

Law Firm:	Adduci, Mastriani, & Schaumberg, LLP, Washington, D.C.
Case Name:	Tessera v. Freescale
Represented:	Plaintiff
Disposition:	Following unfavorable ITC ruling, respondent argued that posted bond (pending final disposition) should be returned to them; prepared a declaration for hearing; ITC ruled against respondent, who then agreed to cease litigation and forfeit the bond.
Date:	April 2012 – October 2012.
Type of Matter:	Theft of trade secrets involving integrated circuit design, manufacturing, and characterization technology
Law Firm:	Shore, Chan, Bragalone, and DePumpo, LLP, Dallas, Texas
Case Name:	Xicor v. SST
Represented:	Plaintiff
Disposition:	Prepared a declaration for hearing regarding plaintiff's identification of its trade secrets; following favorable ruling on this, defendant agreed to settle on terms favorable to the plaintiff
Date:	February 2012 – September 2012.
Type of Matter:	Patent infringement in integrated circuit substrates (ITC matter)
Law Firm:	Alston + Bird, LLP, Atlanta, Georgia
Case Name:	X2Y v. Intel
Represented:	Plaintiff
Disposition:	Consulted on technology involved
Date:	August 2011 – August 2012.
Type of Matter:	Theft of trade secrets involving design of power management integrated circuits (ITC enforcement proceeding)
Law Firm:	Alston + Bird, LLP, Menlo Park, California
Case Name:	Richtek v. uPI, and Sapphire Technology
Represented:	Plaintiff
Disposition:	Prepared an expert report and a supplemental expert report; deposed; testified at hearing/trial; subsidiary respondent Sapphire settled and exited the case shortly before trial.
Date:	June 2011 – March 2012; follow-on district/superior court cases temporarily stayed, but pending.
Type of Matter:	Patent infringement in switching power supplies
Law Firm:	McDermott, Will & Emery, LLP, Miami, Florida
Case Name:	Power Integrations, Inc. v. Fairchild Semiconductor International, Inc.
Representing:	Defendant
Disposition:	Presented the tutorial at the Markman hearing in San Jose, California (Northern District of California) in March; matter ongoing, but no longer involved.
Date:	December 2010 – March 2011.

Type of Matter:	Patent infringement in the power management methodologies of portable/mobile device (ITC matter)
Law Firm:	Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, Washington, D.C.
Case Name:	HTC v. Apple
Represented:	Plaintiff
Disposition:	Deposed in March; testified at trial/hearing (ITC) in May; outcome pending.
Date:	November 2010 – May 2011.

Type of Matter:	Theft of trade secrets involving design of power management integrated circuits (ITC matter)
Law Firm:	Alston + Bird, LLP, Menlo Park, California
Case Name:	Richtek v. uPI, AMD, Sapphire Technology, Diamond Multimedia, and XFX Technology
Represented:	Plaintiff
Disposition:	Prepared an expert report and a supplemental expert report; deposed twice (three days total); subsidiary respondents settled and exited the case during May 2010 – July 2010; main respondent uPI agreed on 21 July 2010 to a Consent Order that included a ten-year ban on importation of the accused products to avoid an ITC hearing.
Date:	January 2010 – July 2010; ITC enforcement proceeding opened against uPI and Sapphire, June 2011 – March 2012 (see above); follow-on district/superior court cases temporarily stayed, but pending.

Type of Matter:	Patent infringement and theft of trade secrets involving integrated circuit manufacturing
Law Firm:	Keker and Van Nest, LLP, San Francisco, California
Case Name:	TSMC v. SMIC
Represented:	Plaintiff
Disposition:	Deposed; testified at trial September 2009; jury returned guilty verdict on all 18 counts; parties settled during damages phase of trial.
Date:	July 2007 – September 2009.

Type of Matter:	Theft of Trade Secrets
Law Firm:	Baker & McKenzie, LLP, San Diego, California
Case Name:	Neology Inc. v. B. Roesner et al.
Represented:	Plaintiff
Disposition:	Reviewed materials produced during discovery and found considerable facially-labeled trade secret material in the possession of the defendant. Case Settled
Date:	April 2007 – May 2007

Type of Matter:	Theft of Trade Secrets
Law Firm:	Weil, Gotshal, and Manges, LLP, New York, New York
Case Name:	Synopsys v. Nassda
Represented:	Defendant
Disposition:	Wrote an expert report on behalf of defendant but was not deposed. Case Settled
Date:	September 2003 - August 2004

Type of Matter:	Theft of Trade Secrets
Law Firm:	Howrey, Simon, Arnold & White, LLP, Menlo Park, California
Case Name:	Silvaco, Inc. v. Circuit Semantics, Inc.
Represented:	Defendant
Disposition:	Wrote an expert report on behalf of defendant and was deposed. Case Settled
Date:	February 2003 - September 2003

Type of Matter:	Contract dispute, Copyright Infringement, and Theft of Trade Secret matter involving integrated circuit design tools
Law Firm:	Russo & Hale, LLP, Palo Alto, California
Case Name:	Virtual Silicon Technology, Inc. v. Library Technologies, Inc.,
Represented:	Plaintiff
Disposition:	On behalf of plaintiff, wrote an expert report, was deposed and testified at arbitration hearing. Decision of binding arbitration released in November 2003; all findings-of-fact in favor of the plaintiff.
Date:	December 2002 - November 2003

PUBLICATIONS

Books

1. D. Foty, "Moore's Law: The Untold Story," August 2017.

2. D. Foty, "The Rise and Fall of Classical Athens: A Short History," January 2018.

3. D. Foty, "Thomas Seebeck: His Life and Science," September 2018.

4. D. Foty, "Essential Digital, Analog, and Semiconductor Electronics Technology," Chapter 19 in *Concise Higher Electrical Engineering* (ed. by E. Chikuni, M. Khan, and O. Okoro), Juta Academic, 2008.

5. D. Foty, *MOSFET Modeling with SPICE: Principles and Practice*, Prentice-Hall (now Pearson Education), 1997 (now in its third printing; Vietnamese-language edition published in 2006).

6. Proceedings of the Symposium on Low Temperature Electronics and High Temperature Superconductors (ed. by S. Raider, C. Claeys, D. Foty, T. Kawai, and R. Kirschman) (published in October 1993).

7. Proceedings of the Symposium on Low Temperature Electronic Device Operation (ed. by D. Foty) (published in December 1991).

Guest Journal Editor

1. Guest editor, special issue on Low Voltage/Low Power Design, Analog Integrated Circuits and Signal Processing, December 1999.

Refereed Journal Publications

1. D. Foty, "Nanoscale Electron Devices: Difficulties, Granularities, and Applications" (Invited Paper), Romanian Journal of Information Sciences and Technology, (published by the Romanian Academy of Sciences), January 2009, vol. 12(3), pp. 317 – 338.

2. D. Foty, "An Evaluation of Deep-Submicron CMOS Design Optimized for Operation at 77K" (Invited Paper), Analog Integrated Circuits and Signal Processing vol. 49, pp. 97 – 105 (2006).

3. D. Foty and K. Runge, "What's Ahead in High-Speed Wireless Data Communications? The Future Will Be Better Tomorrow – And Different Than What We've Been Expecting" (Invited Paper), the African Journal of Information and Communications Technology (online publication).

4. S. Terry, J. Rochelle, D. Binkley, B. Blaylock, D. Foty, and M. Bucher, "Comparison of a BSIM3V3 and EKV MOST Model for a 0.5µm Process and Implications for Analog Circuit Design," IEEE Transactions on Nuclear Science vol. NS-50, pp. 915 - 920 (2003).

5. D. Binkley, C. Hopper, S. Tucker, B. Moss, J. Rochelle, and D. Foty, "A CAD Methodology for Optimizing Transistor Current and Sizing in Analog CMOS Design," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems vol. CAD-22, pp. 225 – 237 (2003).

6. D. Foty, "Perspectives on Analytical Modeling of Small Geometry MOSFETs in SPICE for Low Voltage/Low Power CMOS Circuit Design" (Invited Paper), Analog Integrated Circuits and Signal Processing vol. 21, pp. 229 – 252 (1999).

7. D. Foty, "Taking a Deep Look at Analog CMOS," IEEE Circuits and Devices, March 1999, pp. 23 – 28.

8. D. Foty, "MOSFET Modeling for Circuit Simulation: Where Do We Go From Here?," IEEE Circuits and Devices, July 1998, pp. 26 – 31.

9. G. Gildenblat and D. Foty, "Low Temperature Models of Metal-Oxide-Semiconductor Field-Effect Transistors" (Invited Paper), The International Journal of High Speed Electronics and Systems vol. 6, pp. 317 - 373 (1995).

10. D. Foty and E. Nowak, "MOSFET Technology for Low Voltage/Low Power Applications" (Invited Paper), IEEE Micro, June 1994, pp. 68 - 77.

11. D. Foty, P. Wyns, and K. Oughstun, "On the Propagation of Short Optical Pulses in a Linear Dispersive Medium," IEEE Journal of Quantum Electronics vol. 28, pp. 1619 - 1622 (1992).

12. E. Farrell, P. Appino, D. Foty, and T. Linton, "Visual Interpretation of Multi-Dimensional Computations and Transistor Design," IBM Journal of Research and Development vol. 35, pp. 26 - 44 (1991).

13. D. Foty, "Impurity Ionization in MOSFETs at Very Low Temperatures," Cryogenics vol. 30, pp. 1056 - 1063 (1990).

14. D. Cole, E. Buturla, S. Furkay, K. Varahramyan, J. Slinkman, J. Mandelman, D. Foty, O. Bula, A. Strong, J. Park, T. Linton, J. Johnson, M. Fischetti, S. Laux, P. Cottrell, H. Lustig, F. Pileggi, and D. Katcoff, "The Use of Simulation in Semiconductor Technology Development" (Invited Paper), Solid State Electronics vol. 33, pp. 591 - 623 (1990).

15. K. Oughstun, P. Wyns, and D. Foty, "Numerical Determination of the Signal Velocity in Linear Dispersive Pulse Propagation," Journal of the Optical Society of America A vol. 6, pp. 1430 - 1440 (1989).

16. P. Wyns, D. Foty, and K. Oughstun, "Numerical Analysis of the Precursor Fields in Dispersive Pulse Propagation," Journal of the Optical Society of America A vol. 6, pp. 1421 - 1429 (1989).

17. D. Foty, "Thermal Effects in p-Channel MOSFETs at Low Temperatures," IEEE Transactions on Electron Devices vol. 36, pp. 1542 - 1544 (1989).

18. D. Foty and S. Titcomb, "Thermal Effects in n-Channel Enhancement MOSFETs Operated at Cryogenic Temperatures," IEEE Transactions on Electron Devices vol. 34, pp. 107 - 114 (1987).

Refereed Conference Proceedings

1. D. Foty, "Amplification, Feedback, and Sub-Biasing: Applying Analog Techniques to High-Speed, Low-Power Digital CMOS Circuits," *Invited Conference Plenary Lecture,* Proceedings of the 13th International Symposium on Signals, Circuits, and Systems, pp. 123 - 128 (published July 2017).

2. D. Foty, "The Future of 'Moore's Law' – Does It Have One?" *Invited Conference Plenary Lecture,* Proceedings of the 11th International Symposium on Signals, Circuits, and Systems, pp. 1 - 8 (published July 2013).

3. D. Foty, "The Future of 'Moore's Law' – Does It Have One?" *Invited Conference Plenary Lecture*, Proceedings of the 13th Baltic Electronics Conference, pp. 21 – 26 (published October 2012).

4. D. Foty, B. Smith, S. Sinha, and M. Schröter, "Expanding Wireless Bandwidth in a Power-Efficient Way: Developing a Viable mm-Wave Radio Technology," *Invited Conference Plenary Lecture*, Proceedings of the 10th IEEE East-West Design and Test Symposium, pp. 264 - 269 (published September 2012).

5. D. Foty, B. Smith, S. Sinha, and M. Schröter, "The Wireless Bandwidth Crisis and the Need for Power-Efficient Bandwidth," (Invited Paper), Proceedings of the 10th International Symposium on Signals, Circuits, and Systems, pp. 275 - 279 (published July 2011).

6. D. Foty, "Breaking the Entropy Addiction: Understanding Power Consumption and Overcoming It," *Invited Conference Plenary Lecture*, Proceedings of Africon2009, Proceedings on DVD (published September 2009).

7. B.C. Mabuza, S. Sinha and D. Foty, "On-chip Impedance Tuning for mm-wave Applications,"• Proceedings of the South African Conference on Semiconductor and Superconductor Technology, pp. 49 – 53 (published April 2009).

8. D. Foty, S. Sinha, M. Weststrate, C. Coetzee, A. Uys, and E. Sibanda, "mm-Wave Radio Communications Systems: The Quest Continues," *Invited Conference Plenary Lecture*, Proceedings of the International Radio Electronics Forum, pp. 14 – 17 (published October 2008).

9. D. Foty, "Prospects for Nanoscale Electron Devices: Some Little-Recognized Problems," *Invited Conference Plenary Lecture*, Proceedings of the 31st Conference on Semiconductor Physics, pp. 3 – 13 (published October 2008).

10. D. Foty, "Nanoscale Electron Devices: The Untold Technology Story," *Invited Conference Plenary Lecture*, Proceedings of the 11th Baltic Electronics Conference, pp. 59 - 69 (published October 2008).

11. D. Foty**,** "Next-Generation Wireless Networks: A New World, From Bottom to Top," *Invited Conference Keynote Lecture*, Proceedings of Africon2007, Proceedings on DVD (published September 2007).

12. D. Foty, "Next-Generation Wireless Networks: New Building Blocks and New Network Topologies," *Invited Conference Plenary Lecture*, Proceedings of the International Conference on Dependable Systems, Services, and Technologies, pp. 220 - 228 (published April 2007).

13. D. Foty, "Factors in High-Speed Wireless Data Networking – New Ideas and a New Perspective," Invited Conference Plenary Lecture, Proceedings of the East-West Design and Test Workshop, pp. 29 - 38 (published September 2006).

14. D. Foty, "New Directions in Technology for High-Speed Wireless Data Communications," Invited Conference Plenary Lecture, Proceedings of the 13th International Conference on the Mixed Design of Integrated Circuits and Systems, pp. 19 – 27 (published June 2006).

15. D. Foty and G. Gildenblat, "Fundamental Aspects of CMOS Technology: Basics, Implications, and a Roadmap to the Future" (Invited Paper), Proceedings of the International Workshop on System-on-Chip pp. xxx - xxx (published July 2005). (Paper was submitted on time but was inadvertently not included in the Proceedings volume – available upon request.)

16. D. Foty and G. Gildenblat, "Scaling Theory and 'Punctuated Equilibrium' in CMOS Technology," Invited Conference Plenary Lecture, Proceedings of the 7th International Symposium on Signals, Circuits, and Systems, pp. 1 - 8 (published July 2005).

17. D. Foty, "An Evaluation of Deep-Submicron CMOS Design Optimized for Operation at 77K" (Special Session Paper), Proceedings of the 12th International Conference on the Mixed Design of Integrated Circuits and Systems, pp. 939 - 945 (published June 2005).

18. D. Foty, "An Evaluation of Deep-Submicron CMOS Design Optimized for Operation at 77K" (Special Session Paper), Proceedings of the International Symposium on Industrial Electronics, pp. 1139 - 1144 (published June 2005).

19. D. Foty and K. Runge, ""What's Ahead in High-Speed Wireless Data Communications? The Future Will Be Better Tomorrow – And Different Than What We've Been Expecting," Invited Conference Plenary Lecture, Proceedings of the 12th International Conference on Telecommunications, (conference proceedings pages not numbered), (published May 2005).

20. D. Foty and G. Gildenblat, "Fundamental Aspects of CMOS Technology: Basics, Implications, and a Roadmap to the Future," Invited Conference Plenary Lecture, Proceedings of the 8th International Conference CADSM, pp. 21 – 28 (published February 2005).

21. D. Foty, "Perspectives on Scaling Theory and CMOS Technology – Past, Present, and Future" (Invited Paper), Proceedings of the 11th International Conference on Electronics, Circuits, and Systems, pp. 631 – 637 (published December 2004).

22. G. Gildenblat, C. McAndrew, H. Wang, W. Wu, D. Foty, L. Lemaitre and P. Bendix, "Advanced Compact Models: Gateway to Modern CMOS Design" (Invited Paper), Proceedings of the 11th International Conference on Electronics, Circuits, and Systems, pp. 638 – 641 (published December 2004).

23. P. Bendix, D. Foty, and D. Pachura, "Practical Aspects of MOS Transistor Model 'Accuracy' in Modern CMOS Technology" (Invited Paper), Proceedings of the 11th International Conference on Electronics, Circuits, and Systems, pp. 642 - 645 (published December 2004).

24. D. Foty and G. Gildenblat, "CMOS Scaling Theory – Why Our 'Theory of Everything' Still Works, and What That Means For The Future" (Invited Paper), Proceedings of the 12th International Symposium on Electron Devices for Microwave and Optoelectronic Applications, pp. 27 – 38 (published November 2004).

25. D. Foty, "Perspectives on Scaling Theory and CMOS Technology – Punctuated Equilibrium and Evolutionary Biology," Invited Conference Plenary Lecture, Proceedings of the 9th Baltic Electronics Conference, pp. 17- 24 (published October 2004).

26. D. Foty, "Re-Interpreting the MOS Transistor for the 21st Century: Generalized Methods and Their Extension to Nanotechnology," Invited Conference Plenary

Lecture, Nordic VLSI Design Conference (NorChip), pp. 8 - 15 (published November 2003).

27. D. Foty, "Re-Generalizing the MOS Transistor, for Improved Analog Design and Extension to Nanotechnology: New Rules for a New Century," Invited Conference Plenary Lecture, Proceedings of the 4th Electronic Circuits and Systems Conference, pp. 86 - 95 (published September 2003).

28. D. Foty, "Re-Thinking and Re-Generalizing the MOS Transistor: Understanding, CMOS Design, and Extension to Nanotechnology," Invited Conference Plenary Lecture, Proceedings of the 16th European Conference on Circuit Theory and Design, pp. I-16 – I-21 (published September 2003).

29. D. Foty, "Modernizing the Framework for Deep Submicron Design – For CMOS and Beyond," Invited Conference Plenary Lecture, Proceedings of the 10th International Conference on the Mixed Design of Integrated Circuits and Systems, pp. 19 - 24 (published June 2003).

30. S. Terry, J. Rochelle, D. Binkley, B. Blaylock, D. Foty, and M. Bucher, "Comparison of a BSIM3V3 and EKV MOST Model for a 0.5µm Process and Implications for Analog Circuit Design," Proceedings of the IEEE Nuclear Science Symposium, (conference proceedings pages not numbered), (published November 2002).

31. D. Foty, M. Bucher, and D. Binkley, "Re-Interpreting the MOS Transistor Via the Inversion Coefficient and the Continuum of gms/Id," Proceedings of the 9th International Conference on Electronics, Circuits, and Systems, pp. 1179 - 1182 (published September 2002).

32. M. Bucher, D. Kazazis, F. Krummenacher, D. Binkley, D. Foty, and Y. Papananos, "Analysis of Transconductances at All Levels of Inversion in Deep Submicron CMOS," Proceedings of the 9th International Conference on Electronics, Circuits, and Systems, pp. 1183 -1186 (published September 2002).

33. D. Foty, D. Binkley, and M. Bucher, "gm/Id-Based MOSFET Modeling and Modern Analog Design" (Invited Paper), Proceedings of the 9th International Conference on the Mixed Design of Integrated Circuits and Systems, pp. 55 - 58 (published June 2002).

34. D. Foty, D. Binkley, and M. Bucher, "Starting Over: gm/Id-Based MOSFET Modeling as a Basis for Modernized Analog Design Methodologies" (Invited Paper), Proceedings of the International Conference on the Modeling and Simulation of Microsystems, pp. 682 - 685 (published in April 2002).

35. D. Foty, D. Binkley, and M. Bucher, "Measurements and Modeling of MOSFET Inversion Level Over a Wide Range as a Basis for Analog Design," Proceedings of the 15th European Conference on Circuit Theory and Design, pp. I-85 – I-88 (published in August 2001).

36. D. Foty, "MOSFET Modeling for Circuit Simulation: Requiem or Recovery?," Proceedings of the 15th European Conference on Circuit Theory and Design, pp. I-81 – I-84 (published in August 2001).

37. D. Binkley, M. Bucher, and D. Foty, "Design-Oriented Characterization of CMOS Over the Continuum of Inversion Level and Channel Length," Proceedings of the 7th International Conference on Electronics, Circuits, and Systems, pp. 161 – 164 (published in December 2000).

38. D. Foty and E. Nowak, "Performance, Reliability, and Supply Voltage Reduction, with the Addition of Temperature as a Design Variable" (Invited Paper), Proceedings of the 1993 European Solid State Device Research Conference, pp. 943 - 948.

39. D. Foty and E. Nowak, "Performance/Reliability Trade-Off and Optimized nMOSFET Design for 77K CMOS Logic," Proceedings of the Symposium on Low Temperature Electronics and High Temperature Superconductors (ed. by S. Raider), pp. 89 - 95 (published in October 1993).

40. D. Foty, "The Design of Deep Submicron FETs for Low Temperature Operation" (Invited Paper), Proceedings of the Symposium on Low Temperature Electronics and High Temperature Superconductors (ed. by S. Raider), pp. 63 - 77 (published in October 1993).

41. D. Foty, H. Hanafi, P. Agnello, and H. Ho, "Mixed Schottky/p-n Junction Behavior in Diodes Produced by Outdiffusion from Polycrystalline Cobalt Disilicide," Technical Digest of the 1992 International Electron Devices Meeting, pp. 841 - 845.

42. D. Foty, "Low Temperature Electronics and Future Electron Devices" (Invited Paper), Proceedings of the Symposium on Low Temperature Electronic Device Operation (ed. by D. Foty), pp. 13 - 24 (published in December 1991).

43. D. Foty and S. Titcomb, "Freeze-Out and Field Dependent Ionization in MOSFETs at Very Low Temperatures," Proceedings of the Symposium on Low Temperature Electronics and High Temperature Superconductors (ed. by S. Raider), pp. 151 - 160 (published in March 1988).

Articles in Industry Trade Publications

1. D. Foty, "It's Time to Write Off the Past – Vermont Needs an Economic Future," Ethan Allen Institute Newsletter, November 2002. (This article was also published in the Springfield (Vt.) Reporter, the Brandon (Vt.) Bugle, the Brattleboro (Vt.) Reformer, and The Vermont Times.)

2. D. Foty and P. Bendix, "An Executive Guide to MOS Transistor Modeling," Fabless Forum, March 2002.

3. D. Foty, "Radio-Frequency Technology: Easier Said Than Done?," Fabless Forum, September 1999.

4. D. Foty, "A Traveler's Tales – An Essay on Globalization and the Culture of the 'New Economy'," Vermont Business Magazine, September 1998.

5. D. Foty, "MOSFET Modeling for Circuit Simulation: Where Do We Go From Here?," Fabless Forum, March 1998.

Conference Presentations

1. D. Foty, "Amplification, Feedback, and Sub-Biasing: Applying Analog Techniques to High-Speed, Low-Power Digital CMOS Circuits at Dimensions Below 100nm," (Invited Conference Plenary Lecture), presented at the 16th Baltic Electronics Conference, Tallinn, Estonia, 8 October 2018.

2. D. Foty, "Developing Critical Infrastructure – Data-Centric, Next-Generation Communications Networks," (Invited Conference Plenary Lecture), presented at the 2nd Regional African Conference of the International Telecommunications Society, Lusaka, Zambia, 16 March 2018.

3. D. Foty, "Amplification, Feedback, and Sub-Biasing: Applying Analog Techniques to High-Speed, Low Power Digital CMOS Circuits," (Invited Conference Plenary Lecture), presented at the 13th International Symposium on Signals, Circuits, and Systems, Iaşi, Romania, 13 July 2017.

4. D. Foty, "Developing Data-Centric, Next-Generation Communications Networks That Actually Work – and Work Well," (Invited Conference Plenary Lecture), presented at the EAI International Conference for Research, Innovation and Development for Africa, Victoria Falls, Zimbabwe, 21 June 2017.

5. D. Foty, "Amplification, Feedback, and Sub-Biasing: Applying Analog Techniques to High-Speed, Low Power Digital CMOS Circuits," (Invited Conference Plenary Lecture), presented at the 15th Baltic Electronics Conference, Tallinn, Estonia, 3 October 2016.

6. D. Foty, "The Future of 'Moore's Law' – Does It Have One?" (Invited Conference Plenary Lecture), presented at the 12th International Conference on Synthesis, Modeling, Analysis, and Simulation Methods and Applications to Circuit Design, Istanbul, Turkey, 7 September 2015.

7. D. Foty, "Patents, Trade Secrets, Intellectual Property, and Such: What Engineers Need to Know," (Invited Conference Plenary Lecture), presented at the 12th International Symposium on Signals, Circuits, and Systems, Iaşi, Romania, 10 July 2015.

8. D. Foty, "Patents, Trade Secrets, Intellectual Property, and Such: What Engineers Need to Know," (Invited Conference Plenary Lecture), presented at the 14th Baltic Electronics Conference, Laulasmaa, Estonia, 8 October 2014.

9. D. Foty, "The Future of 'Moore's Law' – Does It Have One?" (Invited Conference Plenary Lecture), presented at the 11th International Symposium on Signals, Circuits, and Systems, Iaşi, Romania, 11 July 2013.

10. D. Foty, "The Future of 'Moore's Law' – Does It Have One?" (Invited Conference Plenary Lecture), presented at the 13th Baltic Electronics Conference, Laulasmaa, Estonia, 5 October 2012.

11. D. Foty, B. Smith, S. Sinha, and M. Schröter, "Expanding Wireless Bandwidth in a Power-Efficient Way: Developing a Viable mm-Wave Radio Technology," (Invited Conference Plenary Lecture), presented at the 10th IEEE East-West Design and Test Symposium, Kharkov, Ukraine, 15 September 2012.

12. D. Foty, B. Smith, S. Sinha, and M. Schröter, "Addressing the Problem of Wireless Bandwidth and Power-Efficiency: Prospects for mm-Wave Radio Technology," presented at MASFOR2012, Istanbul, Turkey, 22 June 2012.

13. D. Foty, B. Smith, S. Sinha, and M. Schröter, "Addressing the Emerging Wireless Bandwidth Crisis and the Need for Power-Efficient Bandwidth: Prospects for mm-Wave Radio Technology," (Invited Conference Keynote Lecture), presented at Africon2011, Livingstone, Zambia, 13 September 2011.

14. D. Foty, B. Smith, S. Sinha, and M. Schröter, "The Wireless Bandwidth Crisis and the Need for Power-Efficient Bandwidth," (Invited Paper), presented at the 10th International Symposium on Signals, Circuits, and Systems, Iaşi, Romania, 1 July 2011.

15. D. Foty, "Thomas Johann Seebeck – Two Centuries Later, An Appreciation," (Invited Conference Plenary Lecture – the Thomas Johann Seebeck Memorial Lecture), presented at the 12th Baltic Electronics Conference, Tallinn, Estonia, 4 October 2010.

16. D. Foty, B. Smith, S. Sinha, and M. Schröter, "Next-Generation Wireless Communications Networks - From Chips to Architecture," (Invited Conference Plenary Lecture), presented at the International Association of Science and Technology for Development (IASTED) International Conference on Modeling and Simulation, Gaborone, Botswana, 7 September 2010.

17. D. Foty, "Breaking the Entropy Addiction: Understanding Power Consumption and Overcoming It," (Invited Conference Plenary Lecture), presented at Africon2009, Nairobi, Kenya, 25 September 2009.

18. D. Foty, S. Sinha, M. Weststrate, C. Coetzee, A. Uys, and E. Sibanda, "mm-Wave Radio Communications Systems: The Quest Continues" (Invited Conference Plenary Lecture), presented at the International Radio Electronics Forum, Kharkov, Ukraine, 23 October 2008.

19. D. Foty, "Prospects for Nanoscale Electron Devices: Some Little-Recognized Problems" (Invited Conference Plenary Lecture), presented at the 31st Conference on Semiconductor Physics, Sinaia, Romania, 13 October 2008.

20. D. Foty, "Nanoscale Electron Devices: The Untold Technology Story" (Invited Conference Plenary Lecture), presented at the 11th Baltic Electronics Conference, Laulasmaa, Estonia, 8 October 2008.

21. D. Foty, "Electron Devices in Nanoelectronic Circuits and Systems: Problems and Prospects," *Invited Presentation*, presented at the IEEE Electron Devices Society / Solid State Circuits Society Mini-Colloquium "Nanoelectronic Devices: Present and Perspective," Sinaia, Romania, 14 October 2007.

22. D. Foty, "Next-Generation Wireless Networks: A New World, From Bottom to Top," Invited Conference Keynote Lecture, presented at Africon2007, Windhoek, Namibia, 26 September 2007.

23. D. Foty, "The 'MOS Miracle' – A Behind-the-Scenes Look," Conference tutorial presented at the 8th International Symposium on Signals, Circuits, and Systems, Iaşi, Romania, 11 July 2007.

24. D. Foty, "Next-Generation Wireless Networks: New Building Blocks and New Network Topologies," Invited Conference Keynote Lecture, presented at the International Conference on Dependable Systems, Services, and Technologies, Kirovohrad, Ukraine, 27 April 2007.

25. D. Foty, "Factors in High-Speed Wireless Data Networking – New Ideas and a New Perspective" (Invited Conference Plenary Lecture), presented at the East-West Design and Test Workshop, Sochi, Russia, 18 September 2006.

26. D. Foty, "New Directions in Technology for High-Speed Wireless Data Communications" (Invited Conference Plenary Lecture), presented at the 13th International Conference on the Mixed Design of Integrated Circuits and Systems, Gdynia, Poland, 24 June 2006.

27. D. Foty and G. Gildenblat, "Fundamental Aspects of CMOS Technology: Basics, Implications, and a Roadmap to the Future" (Invited Paper), presented at the International Workshop on System-on-Chip, Banff, Alberta, Canada, 22 July 2005.

28. D. Foty and G. Gildenblat, "Scaling Theory and 'Punctuated Equilibrium' in CMOS Technology" (Invited Conference Plenary Lecture), presented at the 7th International Symposium on Signals, Circuits, and Systems, Iaşi, Romania, 14 July 2005.

29. D. Foty, "An Evaluation of Deep-Submicron CMOS Design Optimized for Operation at 77K" (Special Session Paper), presented at the 12th International Conference on the Mixed Design of Integrated Circuits and Systems, Krakow, Poland, 23 June 2005.

30. D. Foty, "An Evaluation of Deep-Submicron CMOS Design Optimized for Operation at 77K" (Special Session Paper), presented at the International Symposium on Industrial Electronics, Dubrovnik, Croatia, 20 June 2005.

31. D. Foty and K. Runge, "What's Ahead in High-Speed Wireless Data Communications? The Future Will Be Better Tomorrow – And Different Than What We've Been Expecting" (Invited Conference Plenary Lecture), presented at the 12th International Conference on Telecommunications, Cape Town, South Africa, 4 May 2005.

32. D. Foty and G. Gildenblat, "Fundamental Aspects of CMOS Technology: Basics, Implications, and a Roadmap to the Future" (Invited Conference Plenary Lecture), presented at the 8th International Conference CADSM, Polyana, Ukraine, 23 February 2005.

33. D. Foty, "Perspectives on Scaling Theory and CMOS Technology – Past, Present, and Future" (Invited Paper), presented at the 11th International Conference on Electronics, Circuits, and Systems, Tel Aviv, Israel, 15 December 2004.

34. G. Gildenblat, C. McAndrew, H. Wang, W. Wu, D. Foty, L. Lemaitre and P. Bendix, "Advanced Compact Models: Gateway to Modern CMOS Design" (Invited Paper), presented at the 11th International Conference on Electronics, Circuits, and Systems, Tel Aviv, Israel, 15 December 2004.

35. P. Bendix, D. Foty, and D. Pachura, "Practical Aspects of MOS Transistor Model 'Accuracy' in Modern CMOS Technology" (Invited Paper), presented at the 11th International Conference on Electronics, Circuits, and Systems, Tel Aviv, Israel, 15 December 2004.

36. D. Foty and G. Gildenblat, "CMOS Scaling Theory – Why Our 'Theory of Everything' Still Works, and What That Means For The Future" (Invited Paper), presented at the 12th International Symposium on Electron Devices for Microwave and Optoelectronic Applications, Berg-en-Dal, Kruger National Park, South Africa, 8 November 2004.

37. D. Foty, "Perspectives on Scaling Theory and CMOS Technology – Punctuated Equilibrium and Evolutionary Biology" (Invited Conference Plenary Lecture), presented at the 9th Baltic Electronics Conference, Tallinn, Estonia, 4 October 2004.

38. D. Foty, "Re-Interpreting the MOS Transistor for the 21st Century: Generalized Methods and Their Extension to Nanotechnology," (Invited Conference Plenary Lecture), presented at the Nordic VLSI Design Conference (NorChip), Riga, Latvia, 10 November 2003.

39. D. Foty, "Pondering the MOS Transistor in the 21st Century" (Conference Tutorial), presented at the Nordic VLSI Design Conference (NorChip), Riga, Latvia, 9 November 2003.

40. D. Foty, "Re-Generalizing the MOS Transistor, for Improved Analog Design and Extension to Nanotechnology: New Rules for a New Century" (Invited Conference Plenary Lecture), presented at the 4th Electronic Circuits and Systems Conference, Bratislava, Slovakia, 12 September 2003.

41. D. Foty, "Re-Thinking and Re-Generalizing the MOS Transistor: Understanding, CMOS Design, and Extension to Nanotechnology" (Invited Conference Plenary Lecture), presented at the 16th European Conference on Circuit Theory and Design, Krakow, Poland, 2 September 2003.

42. D. Foty, "Modernizing the Framework for Deep Submicron Design – For CMOS and Beyond" (Invited Conference Plenary Lecture), presented at the 10th International Conference on the Mixed Design of Integrated Circuits and Systems, Lodz, Poland, 27 June 2003.

43. D. Foty, M. Bucher, and D. Binkley, "Re-Interpreting the MOS Transistor Via the Inversion Coefficient and the Continuum of gms/Id," presented at the 9th International Conference on Electronics, Circuits, and Systems, Dubrovnik, Croatia, 18 September 2002.

44. D. Foty, and M. Bucher, "New Techniques for Modern Analog Design: CMOS Design Methodologies and the EKV MOSFET Model" (Conference Tutorial), presented at the 9th International Conference on Electronics, Circuits, and Systems, Dubrovnik, Croatia, 15 September 2002.

45. D. Foty, D. Binkley, and M. Bucher, "gm/Id-Based MOSFET Modeling and Modern Analog Design" (Invited Paper), presented at the 9th International Conference on the Mixed Design of Integrated Circuits and Systems, Wrocław, Poland, 20 June 2002.

46. D. Foty and D. Binkley, "MOS Modeling as a Basis for Design Methodologies: New Techniques for Modern Analog Design" (Conference Tutorial), presented at the International Symposium on Circuits and Systems, Scottsdale, Arizona, 26 May 2002.

47. D. Foty, "MOS Modeling, Design Quality, and Modern Analog Design" (Conference Tutorial), presented at the Workshop on Compact Modeling, International Conference on the Modeling and Simulation of Microsystems, San Juan, Puerto Rico, 25 April 2002.

48. D. Foty, D. Binkley, and M. Bucher, "Starting Over: gm/Id-Based MOSFET Modeling as a Basis for Modernized Analog Design Methodologies" (Invited Paper),

presented at the Workshop on Compact Modeling, International Conference on the Modeling and Simulation of Microsystems, San Juan, Puerto Rico, 23 April 2002.

49. D. Foty, "MOS Modeling, Design Quality, and Modern Analog Design" (Conference Tutorial), presented at the International Symposium on Quality Electronic Design, San Jose, California, 18 March 2002.

50. D. Foty, D. Binkley, and M. Bucher, "Measurements and Modeling of MOSFET Inversion Level Over a Wide Range as a Basis for Analog Design," presented at the 15th European Conference on Circuit Theory and Design, Espoo, Finland, 29 August 2001.

51. D. Foty, "MOSFET Modeling for Circuit Simulation: Requiem or Recovery?," presented at the 15th European Conference on Circuit Theory and Design, Espoo, Finland, 29 August 2001.

52. D. Foty and D. Binkley, "MOS Modeling as a Basis for Design Methodologies: New Techniques for Next-Generation Analog Circuit Design" (Conference Tutorial), presented at the 15th European Conference on Circuit Theory and Design, Espoo, Finland, 28 August 2001.

53. D. Foty and D. Binkley, "Re-Connecting MOS Modeling and Circuit Design: New Methods for Design Quality" (Conference Tutorial), presented at the International Symposium on Quality Electronic Design, San Jose, California, 26 March 2001.

54. D. Foty and D. Binkley, "MOS Modeling and Circuit Design: Re-Establishing a Lost Connection" (Conference Tutorial), presented at the Design Automation Conference, Los Angeles, California, 7 June 2000.

55. D. Foty, "A Circuit Designer's Guide to MOS Modeling" (Conference Tutorial), presented at the International Symposium on Circuits and Systems, Geneva, Switzerland, 28 May 2000.

56. D. Foty, "MOS Models as a Factor in the Quality of Electronic Design" (Conference Tutorial), presented at the International Symposium on Quality Electronic Design, San Jose, California, 20 March 2000.

57. D. Foty, "MOS Modeling – A Crucial Circuit Design Activity," presented at Silicon RF-IC: Modeling and Design," Lausanne, Switzerland, 25 February 2000.

58. D. Foty, "An Overview of AC Simulation Aspects of MOS Modeling," presented at the RF MOS Modeling Workshop, Munich, Germany, 16 February 1999.

59. D. Foty, "AC Simulation Aspects of MOS Modeling," presented at Northcon, Seattle, Washington, 22 October 1998.

60. D. Foty, "Effective MOSFET Modeling for SPICE Circuit Simulation" (Conference Tutorial), presented at Northcon, Seattle, Washington, 22 October 1998.

61. D. Foty, "What Every Circuit Designer Needs to Know About MOS Modeling for SPICE Circuit Simulation" (One-Day Short Course), presented at the Electronic Design Automation and Test Conference, Asia, Hsinchu, Taiwan, 15 October 1998.

62. D. Foty, "MOS Modeling of Small Geometry Structures for Circuit Simulation" (Conference Tutorial), presented at the Custom Integrated Circuits Conference, Santa Clara, California, 11 May 1998.

63. D. Foty, "MOS Modeling for Deep Submicron CMOS Circuit Simulation" (Conference Tutorial), presented at the Southeastern Workshop on Mixed-Signal VLSI, Knoxville, Tennessee, 1 April 1998.

64. D. Foty, "MOS Modeling Issues in the Emerging Analog and Low Power Era" (Conference Tutorial), presented at the Electronic Design Automation and Test Conference, Asia, Hsinchu, Taiwan, 28 August 1997.

65. D. Foty, "MOS Modeling Issues in the Emerging Analog and Low Power Era" (Conference Tutorial), presented at the Electronic Design Automation and Test Conference, Asia, Shanghai, China, 22 August 1997.

66. D. Foty, "Aspects of MOS Modeling for Analog/Mixed-Signal Design," presented at the CMP Analog/Mixed-Signal Design Conference, San Jose, California, 22 July 1997.

67. D. Foty, "MOS Modeling and SPICE: Are You an Educated Model Consumer?" (Conference Tutorial), presented at the Custom Integrated Circuits Conference, Santa Clara, California, 5 May 1997.

68. D. Foty, "The SPICE FET Models: Pitfalls and Prospects" (Conference Tutorial), presented at the Design Automation Conference, Las Vegas, Nevada, 5 June 1996.

69. D. Foty and E. Nowak, "Performance, Reliability, and Supply Voltage Reduction, with the Addition of Temperature as a Design Variable" (Invited Paper), presented at the Symposium on Low Voltage-Low Power Integrated Circuits, 1993 European Solid State Device Research Conference, Grenoble, France, 16 September 1993.

70. D. Foty and E. Nowak, "Performance/Reliability Trade-Off and Optimized nMOSFET Design for 77K CMOS Logic," presented at the Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 20 May 1993.

71. D. Foty, "The Design of Deep Submicron FETs for Low Temperature Operation" (Invited Paper), presented at the Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 20 May 1993.

72. D. Foty, H. Hanafi, P. Agnello, and H. Ho, "Mixed Schottky/p-n Junction Behavior in Diodes Produced by Outdiffusion from Polycrystalline Cobalt Disilicide," presented at the 1992 International Electron Devices Meeting, San Francisco, California, 16 December 1992.

73. D. Foty, "Low Temperature Electronics and Future Electron Devices (Invited Paper), presented at the Symposium on Low Temperature Electronic Device Operation, Washington, DC, 7 May 1991.

74. D. Foty, "Impurity Ionization in MOSFETs at Very Low Temperatures," presented at the First International Conference on Low Temperature Electronics, Berkeley, California, 24 April 1990.

75. D. Foty and T. Furukawa, "Behavior of an NMOS Trench Isolated Corner Parasitic Device at Low Temperature," presented at the Symposium on Low Temperature Electronics, Materials, and Processing, Hollywood, Florida, 17 October 1989.

76. D. Foty and S. Titcomb, "Freeze-Out and Field Dependent Ionization in MOSFETs at Very Low Temperatures," presented at the Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 20 October 1987.

Co-Authored Conference Presentations

1. S. Sinha and D. Foty, "SiGe Technology for mm-Wave Applications," (Invited Conference Plenary Lecture), presented at the 13th Baltic Electronics Conference, Tallinn, Estonia, 3 October 2012.

2. B.C. Mabuza, S. Sinha and D. Foty, "On-chip Impedance Tuning for mm-Wave Applications," presented at the South African Conference on Semiconductor and Superconductor Technology, Stellenbosch, South Africa 8 April 2009.

3. S. Terry, J. Rochelle, D. Binkley, B. Blaylock, D. Foty, and M. Bucher, "Comparison of a BSIM3V3 and EKV MOST Model for a 0.5µm Process and Implications for Analog Circuit Design," presented at the IEEE Nuclear Science Symposium, Norfolk, Virginia, 15 November 2002.

4. M. Bucher, D. Kazazis, F. Krummenacher, D. Binkley, D. Foty, and Y. Papananos, "Analysis of Transconductances at All Levels of Inversion in Deep Submicron CMOS," presented at the 9th International Conference on Electronics, Circuits, and Systems, Dubrovnik, Croatia, 18 September 2002.

5. D. Binkley, M. Bucher, and D. Foty, "Design-Oriented Characterization of CMOS Over the Continuum of Inversion Level and Channel Length," presented at the 7th

International Conference on Electronics, Circuits, and Systems, Kaslik, Lebanon, 18 December 2000.

6. G. Gildenblat, M. Bradford, and D. Foty, "A New MOS C-V Simulator for Low Temperature Applications," presented at the Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 20 May 1993.

Conference Panel Participation

1. Member of Panel Discussion, 2nd Regional African Conference of the International Telecommunications Society, Lusaka, Zambia, 15 March 2018.

2. Member of Panel Discussion, 12th International Conference on Synthesis, Modeling, Analysis, and Simulation Methods and Applications to Circuit Design, Istanbul, Turkey, 7 September 2015.

3. Member of Panel Discussion, Future Wireless Telecommunications, "Telecosm," Lake George, New York, 16 October 2007.

4. Moderator of Panel Discussion, International Workshop on System-on-Chip, Banff, Alberta, Canada, 22 July 2005.

5. Member of Panel Discussion, Custom Integrated Circuits Conference, San Jose, California, 23 September 2003.

6. Co-moderator of Panel Discussion, Fabless Semiconductor Association Modeling Workshop, Santa Clara, California, 9 September 2002.

7. Member of Panel Discussion, Workshop on Compact Modeling, International Conference on the Modeling and Simulation of Microsystems, San Juan, Puerto Rico, 23 April 2002.

8. Member of Panel Discussion, "Vermont's High-Tech Future – Does it Have One?," Room 11, the Statehouse, Montpelier, Vermont, 26 April 2001.

9. Member of Panel Discussion, Fabless Semiconductor Association Quarterly Meeting, San Jose, California, 5 September 1999.

10. Member of Panel Discussion, Fabless Semiconductor Association Modeling Workshop, San Jose California, 24 May 1999.

11. Member of Panel Discussion, Symposium on Low Voltage-Low Power Integrated Circuits at the 1993 European Solid State Device Research Conference, Grenoble, France, 16 September 1993.

12. Member of Panel Discussion, Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 19 May 1993.

Invited Seminars/Lectures

1. "Digital Semiconductor Electronics: Why It Happened, And Where It's Going," short course hosted by the University of Pretoria, Pretoria, South Africa, 15 August 2011.

2. "The Untold Story of 'Moore's Law': *Why* It Happened," short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Iaşi, Romania, 4 – 5 July 2011.

3. "Some Background Thoughts On mm-Wave Radio Technology," seminar presented at the University of Pretoria, Pretoria, South Africa, 17 August 2010.

4. "Digital Semiconductor-Based Electronics: Why It Became A Juggernaut," short course hosted by the University of Pretoria, Pretoria, South Africa, 16 August 2010.

5. "Some Thoughts On mm-Wave Radio Technology," short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Oradea, Romania, 13 July 2010.

6. "Silicon-Based Semiconductor Electronics – How It Came To Dominate," short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Oradea, Romania, 12 July 2010.

7. "The Powerful Entropy Challenge: Dealing With Power Consumption," presented at the IEEE South Africa Section Meeting, Pretoria, South Africa, 18 August 2009.

8. "Digital CMOS Electronics: The Background Story," short course hosted by the University of Pretoria, Pretoria, South Africa, 17 August 2009.

9. "An Overview of mm-Wave Radio Technology," short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Iaşi, Romania, 13 July 2009.

10. "Modern Electronics: How We Got Here," short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Iaşi, Romania, 13 July 2009.

11. "Prospects for mm-Wave Radio Technology: An Overview," short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Oradea, Romania, 22 July 2008.

12. "Into the NanoSmall: The Unexpected Challenges," short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Oradea, Romania, 22 July 2008.

13. “A Concise History of Modern Electron Devices,” short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Oradea, Romania, 22 July 2008.

14. "Issues In mm-Wave Radio Systems: Prospects and Challenges," short course hosted by the University of Pretoria, Pretoria, South Africa, 8 May 2008.

15. "Prospects for mm-Wave Radio Technology: An Executive Summary for Decision-Makers," presented at the IEEE Region 8 meeting, University of Pretoria, Pretoria, South Africa, 8 May 2008.

16. “The MOS Transistor, On a Tourist Visa,” short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Iaşi, Romania, 16 July 2007.

17. “Semiconductor Electronics: Some Fundamental Background,” short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Iaşi, Romania, 16 July 2007.

18. “The MOS Transistor and CMOS Technology: Past, Present, and Future,” short course hosted by Tallinn University of Technology, Tallinn, Estonia, 13 – 14 November 2006.

19. “New Directions in Technology for High-Speed Wireless Data Communications,” seminar presented at the Universitatea Politehnica Bucureşti, Bucharest, Romania, 28 July 2006.

20. “The MOS Transistor and CMOS Technology: History as a Guide to the Future,” short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Braşov, Romania, 25 July 2006.

21. “The Underpinnings of the MOS Transistor and CMOS Technology in the 21st Century - Scaling Theory and New Methods in Analog/RF Design,” short course hosted by l'École Polytechnique de Montréal, Montréal, Québec, Canada; sponsored by ReSMiQ and the local IEEE Solid State Circuits Society chapter, 27 October 2005.

22. “The Underpinnings of the MOS Transistor and CMOS Technology in the 21st Century – Scaling Theory and New Methods in Analog/RF Design,” short course hosted by the Department of Electrical, Electronic, and Computer Engineering, University of Pretoria, Pretoria, South Africa, and sponsored by the IEEE South Africa Section, 9 – 10 May 2005.

23. “What’s Ahead in High-Speed Wireless Data Communications? The Future Will Be Better Tomorrow – And Different Than What We’ve Been Expecting,” seminar presented at the Department of Electrical Engineering, University of Cape Town, Cape Town, South Africa, 7 May 2005.

24. "Low Temperature CMOS: A Bad Idea Whose Time Has (Finally) Come?", seminar presented at the Department of Computer-Aided Design, L'viv Polytechnic National University, L'viv, Ukraine, 28 February 2005.

25. "The Underpinnings of the MOS Transistor and CMOS Technology in the 21st Century – Scaling Theory and New Methods in Analog/RF Design," Full-day "Eurotraining" course, held at the Danish Technical University, Lyngby, Denmark, 27 October 2004.

26. "The Underpinnings of the MOS Transistor and CMOS Technology in the 21st Century – Scaling Theory and New Methods in Analog/RF Design," Full-day "Eurotraining" course, held at the Politechnico di Torino, Turin, Italy, 25 October 2004.

27. "CMOS Scaling and Low Temperature CMOS: A Bad Idea Whose Time Has Come?", seminar presented at the Department of Electrical and Computer Engineering, Oakland University, Auburn Hills, Michigan, 25 March 2004.

28. "Modernizing the Interpretation of the MOS Transistor for the 21st Century: Generalized Methods and Their Extension to Nanotechnology," presented at the IEEE Southeast Michigan Spring Section Meeting, Auburn Hills, Michigan, 24 March 2004.

29. "Re-Interpreting the MOS Transistor for the 21st Century: Generalized Methods and Their Extension to Nanotechnology," seminar presented at Tallinn Technical University, Tallinn, Estonia, 13 November 2003.

30. "Re-Interpreting the MOS Transistor for the 21st Century: Generalized Methods and Their Extension to Nanotechnology," seminar presented at Helsinki University of Technology, Espoo, Finland, 7 November 2003.

31. "A Practical Examination of MOS Transistor Model 'Accuracy' in Modern CMOS Technology," presented at the MOS Arbeitskreis Meeting, Crolles, France, 5 May 2003.

32. "Building a New Framework for Deep Submicron Analog/RF CMOS Design – and Beyond," invited seminar presented at the Department of Electrical Engineering, Columbia University, New York, New York, 25 April 2003.

33. "A New Framework for Deep Submicron Analog/RF CMOS Design – and Beyond," seminar presented at the Department of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, Georgia, 20 March 2003.

34. "Starting Over: Modernizing the Framework for Deep Submicron Analog CMOS Design," seminar presented at the Nokia Research Center, Helsinki, Finland, 29 November 2002.

35. "Modernizing the Framework for Deep Submicron Analog CMOS Design," Distinguished Guest Lecturer, IEEE Baltic Region Meeting (sponsored by Tallinn Technical University), Sagadi, Estonia, 19 – 20 August 2002.

36. "Modernizing the Framework for Deep Submicron Analog CMOS Design," seminar presented at Helsinki University of Technology, Espoo, Finland, 16 August 2002.

37. "gm/Id-Based MOSFET Modeling and Modern Analog Design," presented at the MOS Arbeitskreis Meeting, Ünterpremstatten, Austria, 19 November 2001.

38. "MOS Modeling and Analog Circuit Design," lecture as part of "Practical Aspects of Analog Design," professional short course sponsored by Mead Microelectronics, San Francisco, California, 13 November 2001.

39. "MOS Modeling and Analog Circuit Design," lecture as part of "Transistor-Level Analog IC Design," professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 10 October 2001.

40. "Please Stop Imitating Us!' – An Engineer Looks at the (Unstable) State of the Humanities," presented at a meeting of the National Association of Scholars, Burlington,Vermont, 14 July 2001.

41. "Introduction to the Fabless Semiconductor Association (FSA) and the Modeling Committee Activities," presented at the MOS Arbeitskreis Meeting, Munich, Germany, 5 March 2001.

42. "The EKV MOSFET Model: A MOS Model of, by, and for Analog Designers," presented at Broadcom Corp., Irvine, California, 30 November 2000.

43. "Modeling and Simulation for Mixed-Signal IC Design," lecture as part of "Transistor-Level Analog IC Design," professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 27 September 2000.

44. "MOS Models as a Factor in the Quality of Electronic Design," presented at the Rockwell Scientific Center, Thousand Oaks, California, 17 March 2000.

45. "MOS Models as a Factor in the Quality of Electronic Design," presented at Micron Technology, Inc., Boise Idaho, 4 March 2000.

46. "Modeling and Simulation for Mixed-Signal IC Design," lecture as part of "Practical Aspects of Analog and Mixed-Signal ICs," professional short course sponsored by Mead Microelectronics, Monterey, California, 3 February 2000.

47. "Modeling and Simulation for Mixed-Signal IC Design," lecture as part of "Transistor-Level Analog IC Design," professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 30 September 1999.

48. "AC Simulation Aspects of MOS Modeling," presented at the Fabless Semiconductor Association Modeling Workshop, San Jose, California, 25 May 1999.

49. D. Foty, M. Bucher, and C. Enz, "The EKV MOSFET Model – A MOS Model for the Analog Designer," presented at the Fabless Semiconductor Association Modeling Workshop, San Jose, California, 25 May 1999.

50. Several lectures on MOS device physics, modeling, and analog design, presented at Mentor Graphics, Heliopolis, Cairo, Egypt, 5 – 8 May 1999.

51. "A Brief History of MOS Modeling (or, How We Got In This Mess In the First Place)," presented at Philips Research Laboratories, Eindhoven, The Netherlands, 24 March 1999.

52. "An Overview of MOS Modeling for SPICE Circuit Simulation," presented at Mitel Corporation, Bromont, Québec, Canada, 2 February 1999.

53. "Modeling and Simulation for Mixed-Signal IC Design," lecture as part of "Practical Aspects of Analog and Mixed-Signal ICs," professional short course sponsored by Mead Microelectronics, Monterey, California, 12 December 1998.

54. "MOS Modeling Challenges for Deep Submicron CMOS," lecture presented as part of "Deep Submicron CMOS Design," professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 12 October 1998.

55. "Modeling the Temperature-Dependent Characteristics of MOSFETs for Circuit Simulation," presented at the Electronic Parts Selection and Management Workshop, Center for the Analysis of Life-Cycle Engineering, University of Maryland, College Park, Maryland, 17 June 1998.

56. "A Primer on Trench Isolation Technology (or, Why Do Process Engineers Hate Circuit Designers?)," presented at the Fabless Semiconductor Association Modeling Subcommittee Meeting, Opti, Inc., Milpitas, California, 12 May 1998.

57. C. Enz, M. Bucher, and D. Foty, "The EKV MOSFET Model for Analog and Mixed-Mode Circuit Design," satellite broadcast class, National Technological University (hosted by North Carolina State University, Raleigh, North Carolina), 30 April 1998.

58. "MOS Modeling Challenges for Deep Submicron CMOS Circuit Simulation," presented at Digital Equipment Corporation, Hudson, Massachusetts, 13 April 1998.

59. "Challenges for 0.25μm CMOS Circuit Design: Scaling, MOS Modeling, and Complexity," presented at CERN, Geneva, Switzerland, 6 February 1998.

60. "MOS Modeling Challenges for Deep Submicron CMOS," lecture presented as part of "Deep Submicron CMOS Design," professional short course sponsored by Mead Microelectronics, Monterey, California, 11 December 1997.

61. C. Enz, M. Bucher, and D. Foty, "The EKV MOSFET Model for Analog and Mixed-Mode Circuit Design," one-day short course sponsored by the Fabless Semiconductor Association, San Jose, California, 8 November 1997.

62. "MOS Modeling Issues in the Emerging Analog and Low Power Era," presented Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, 27 August 1997.

63. "Current Problems in MOSFET Modeling for Analog Circuit Simulation," presented at Level One Communications, Inc., Sacramento, California, 9 August 1997.

64. Guest lecturer, Centre National pour les Récherches Scientifique (CNRS) Summer Lecture Series, La Londe des Maures, France, 23 – 28 June 1997.

65. "MOSFET Modeling and Analog Circuit Design," presented at the Centre National pour les Récherches Scientifique (CNRS) Summer Lecture Series, La Londe des Maures, France, 27 June 1997.

66. "Benchmarking and Pre-Screening SPICE FET Models for Circuit Simulation Usage," presented at the Fabless Semiconductor Association Modeling Subcommittee Meeting, Adaptec, Inc., Milpitas, California, 6 May 1997.

67. "Benchmarking and Pre-Screening SPICE FET Models for Circuit Simulation Usage," presented at Cirrus Logic, Inc., Fremont, California, 6 May 1997.

68. "MOSFET Modeling and SPICE: Are You an Educated Model Consumer?," presented at Cirrus Logic, Inc., Fremont, California, 6 May 1997.

69. "MOS Modeling and SPICE: Are You an Educated Model Consumer?," satellite broadcast class, National Technological University (hosted by North Carolina State University, Raleigh, North Carolina), 21 April 1997.

70. "An Overview of the SPICE FET Modeling Infrastructure" lecture presented as part of "Modeling and Simulation of MOS Analog ICs," professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 18 February 1997.

71. "An Overview of the SPICE FET Modeling Infrastructure" lecture presented as part of "Modeling and Simulation of MOS Analog ICs," professional short course sponsored by Mead Microelectronics, Monterey, California, 12 December 1996.

72. "Analytical MOSFET Modeling and SPICE - Past, Present, and Future", seminar presented at the Department of Electrical Engineering, Ohio State University, Columbus, Ohio, 9 May 1995.

73. "Constraints on CMOS Technology for Low Voltage/Low Power Applications", seminar presented at the Department of Electrical Engineering, Ohio State University, Columbus, Ohio, 8 May 1995.

74. "Submicron FET Design: Physical Considerations and Technological Choices", seminar presented at the Electrical Engineering Department, University of Hawaii, Honolulu, Hawaii, 24 May 1993.

75. "Aspects of the Design of Deep Submicron FETs for CMOS Operation at 300K and 77K", seminar presented at the Department of Electrical Engineering, Pennsylvania State University, University Park, Pennsylvania, 10 November 1992.

PROFESSIONAL AFFILIATIONS & AWARDS

Honorary Member of the Applied Radio Electronics Science Academy of Ukraine

Senior Member, The Institute of Electrical and Electronic Engineers (IEEE); and of the Electron Devices, Lasers and Electro-Optics, Circuits and Systems, and Communications Societies of the IEEE.

Reviewer/evaluator of funding proposals, Natural Science and Engineering Research Council of Canada, 1991 - present.

Reviewer/evaluator of funding proposals, California MICRO program, 2001 - present.

Reviewer/evaluator of funding proposals, National Research Foundation of South Africa, 2007- present.

Industrial and Academic Mentoring

Member of the Advisory Board, Department of Electrical, Electronic & Computer Engineering, University of Pretoria, South Africa, 2012 – present.

Advisor to the Tshwane University of Technology, Pretoria, South Africa, 2007 - present.

Advisor to the University of Pretoria, Pretoria, South Africa, 2005 – present.

Advisor to the Tallinn University of Technology, Tallinn, Estonia, 2004 – present.

Industrial Mentor for "Development and Applications of a New MOS C-V Simulator for the 2 - 300K Temperature Range" (Professor Gennady Gildenblat, Principal Investigator, Department of Electrical Engineering, Pennsylvania State University, University Park, Pennsylvania), funded by the IBM Shared University Research Contract program, calendar year 1992.

Committees/Conferences

1. Member of the Organizing Committee, and Chair of the Track on Electromagnetics and Antennas, Africon 2011, Victoria Falls, Zambia, September 2011.

2. Member of the Organizing Committee, and Chair of the Track on Electron Devices and Circuits, Africon 2009, Nairobi, Kenya, September 2009.

3. Session Chair, 31st International Conference on Semiconductor Physics, Sinaia, Romania, 14 October 2008.

4. Session Chair, Africon 2007, Windhoek, Namibia, 27 September 2007.

5. Session Chair, 13th International Conference on the Mixed Design of Integrated Circuits and Systems, Gdynia, Poland, 24 June 2006.

6. Session Chair, International Workshop on System-on-Chip, Banff, Alberta, Canada, 22 July 2005.

7. Session Chair, 7th International Symposium on Signals, Circuits, and Systems, 4Iaşi, Romania, 15 July 2005.

8. Member of the Scientific Committee, European Conference on Circuit Theory and Design (ECCTD), 2005.

9. Special Session Organizer, 12th International Conference on the Mixed Design of Integrated Circuits and Systems, Krakow, Poland, 22 - 25 June 2005.

10. Special Session Organizer, International Symposium on Industrial Electronics, Dubrovnik, Croatia, 20 – 23 June 2005.

11. Session Chair, 12th International Conference on Telecommunications, Cape Town, South Africa, 4 – 6 May 2005.

12. Session Chair, 11th International Conference on Electronics, Circuits, and Systems, Tel Aviv, Israel, 13 - 15 December 2004.

13. Session Chair, the 12th International Symposium on Electron Devices for Microwave and Optoelectronic Applications, Berg-en-Dal, Kruger National Park, South Africa, 8 - 9 November 2004.

14. Member of the International Program Committee, International Conference on Mixed Design of Integrated Circuits and Systems, 2004 – present.

15. Member of the Technical Program Committee, International Symposium on Signals, Circuits, and Systems, 2004 – present.

16. Special Session Organizer, 11th International Conference on Electronics, Circuits, and Systems, Tel Aviv, Israel, 13 – 15 December 2004.

17. Session Chair, 4th Electronic Circuits and Systems Conference, Bratislava, Slovakia, 11 – 12 September 2003.

18. Member of the Scientific Committee, European Conference on Circuit Theory and Design (ECCTD), 2003.

19. Session Chair, 9th International Conference on Electronics, Circuits, and Systems, Dubrovnik, Croatia, 16 - 18 September 2002.

20. Member, Analog Signal Processing Technical Committee, IEEE Circuits and Systems Society, 2002 – present.

21. Member, Program Committee, Analog Circuits and Signal Processing, International Symposium on Circuits and Systems (ISCAS), 2002 – present.

22. Session Chair, International Symposium on Quality Electronic Design, San Jose, California (ISQED), 18 – 20 March 2002.

23. Chairman, Modeling Subcommittee, Fabless Semiconductor Association, 2001 – 2003.

24. Chairman, Fabless Semiconductor Association Modeling Workshop, 2001 – present.

25. Member of Technical Program Committee, European Conference on Circuit Theory and Design (ECCTD), 2001.

26. Member, IEEE Advisory Committee, 2001 – present.

27. Member of the Organizing Committee, International Symposium on Quality Electronic Design (ISQED), 2000 – 2002.

28. Member of the Modeling Committee, International Symposium on Quality Electronic Design (ISQED), 2000 – 2002.

29. Chairman of the Modeling Committee, International Symposium on Quality Electronic Design (ISQED), 2001.

30. Session Chair, International Symposium on Quality Electronic Design, San Jose, California (ISQED), 26 – 28 March 2001.

31. Lead Organizer, Fabless Semiconductor Association Workshop, 2000 – present.

32. Member of the MOS Arbeitskreis, 2000 – present.

33. Co-Chairman, Modeling Subcommittee, Fabless Semiconductor Association, 1999 – 2000.

34. Member of the Executive Committee, Modeling Subcommittee, Fabless Semiconductor Association, 1998 – present.

35. Member, Modeling Subcommittee, Fabless Semiconductor Association, 1996 – present.

36. Organizer, Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 16 - 21 May 1993.

37. Organizer, Symposium on the Physics and Fabrication of Semiconductor Nanostructures, Washington DC, 5 - 10 May 1991.

38. Lead Organizer, Symposium on Low Temperature Electronic Device Operation, Washington DC, 5 - 10 May 1991.

39. Co-Chaired the Symposium on Low Temperature Electronics, Materials, and Processing, Hollywood, Florida, 17 October 1989.