

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,

Petitioner

v.

LONGITUDE LICENSING LTD.

Patent Owner

IPR2023-01230

U.S. Patent No. 9,207,701

DECLARATION OF DR. HAVEY J. STIEGLER

UNDER 37 C.F.R. § 1.68

IN SUPPORT OF PETITION FOR INTER PARTES REVIEW

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I, Dr. Harvey J. Stiegler, do hereby declare as follows:

I. INTRODUCTION

1. I have been retained by counsel for Western Digital Technologies, Inc. (“Western Digital” or “Petitioner”) as a technical expert in connection with the proceeding identified above. I submit this declaration in support of Western Digital’s Petition for Inter Partes Review of U.S. Patent No. 9,207,701 (“the ’701 patent”). I am being compensated at my usual and customary rate for the time I spend in connection with this Request. My compensation is not affected by the outcome of this Request.

2. I have been asked to provide my opinions regarding claims 1-18 (each a “Challenged Claim” and collectively the “Challenged Claims”) of the ’701 patent. Specifically, I have been asked to provide my opinions regarding the claims’ obviousness to a person having ordinary skill in the art (“POSITA”) as of the claims’ priority date. My opinions regarding these topics are set forth below.

3. In preparing this Declaration, I have reviewed:

- 1) EX1001, the ’701 patent;
- 2) EX1002, prosecution file history of the ’701 patent;
- 3) EX1005, US 7,427,888 to Zhang et al. (“Zhang”);
- 4) EX1006, US 5,767,735 to Javanifard et al. (“Javanifard”);

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- 5) EX1007, prosecution history of Zhang (App. 10/888667) (“667 app”);
- 6) EX1008, Charge Pump Circuit Design, Pan et al., 1st Edition, 2006 (“Pan”);
- 7) EX1009, prosecution file history of parent of ’701 patent (App. 12/052422) (“’422 app”);
- 8) EX1010, prosecution file history of parent of ’701 patent (App. 13/912845) (“’845 app”);
- 9) EX1014, U.S. Patent No. 7,579,902 to Frulio et al. (“Frulio”);
- 10) EX1015, U.S. Patent No. 7,477,093 to Al-Shamma et al. (“Al-Shamma”);
- 11) EX1016, U.S. Patent No. 7,046,076 to Daga et al. (“Daga”);
- 12) EX1017, U.S. Patent No. 6,157,242 to Fukui (“Fukui”);
- 13) EX1018, U.S. Patent No. 7,505,350 to Lee et al. (“Lee”);
- 14) EX1019, U.S. Patent No. 6,954,386 to Narui et al. (“Narui”);
- 15) EX1020, “Charge Pump Circuits with Low Area and High Power Efficiency for Memory Applications,” Kang et al.,

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16) EX1021, U.S. Patent No. 6,034,539 to Hwang

(“Hwang”)

17) EX1022, U.S. App. Pub. No. 2003/0067063A1 to Muff

et al. (“Muff”)

18) EX1023, U.S. Patent No. 6,346,738 to Kim et al.

(“Kim”)

19) any other document cited below.

4. I have been informed by counsel to Western Digital that the earliest claimed priority date for the '701 patent is March 27, 2007, although any given claim of the '701 Patent may or may not be entitled to the earliest claimed date.

5. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of art, and have considered the viewpoint of a Person of Ordinary Skill in the Art (POSITA), as of March 27, 2007.

I have also considered:

- a) the documents listed above,
- b) any additional documents and references cited in the analysis below,

- c) the relevant legal standards, including the standard for obviousness, and
- d) my knowledge and experience based upon my work in this area as described below.

II. BACKGROUND AND QUALIFICATIONS

6. My qualifications are set forth in my curriculum vitae, a copy of which is attached as Exhibit 1004. I have over 25 years of industry experience in the semiconductor industry serving in IC design, design management, and technology development. I have summarized in this section my educational background, career history, and other qualifications relevant to this matter. As set forth in my curriculum vitae:

7. From November, 2011 – present, I have been a Visiting Researcher at the University of Texas at Dallas, and from April, 2009 – November, 2011, I was employed by the University of Texas at Dallas as a Research Scientist. In my role as a Research Scientist and a Visiting Researcher, I have contributed to the development of devices and circuits utilizing organic and inorganic semiconductors for flexible electronics and the development of bio-molecular sensor devices for medical applications, sensor device SPICE models, sensor support circuits, and low-temperature fabrication of neuromorphic circuits and associated SPICE modeling.

8. From February, 2012 – April, 2014, I was employed by Business Control Systems (BCS), and I provided design, design support, and consulting services.

9. From 1979 – 1983 and 1985 – 2009, I was employed by Texas Instruments Incorporated. I held various Design Engineering and Management roles related to memory devices during my tenure at Texas Instruments Incorporated as described in further detail below. Much of my time was spent in design, which not only included the initial circuit design and layout, but modifications based on various timing, leakage, and voltage conditions identified during simulation.

10. From 2005 – 2009, I was a Senior Member of the Technical Staff in the Analog Technology Development Group. In this role, I contributed to the development of memory technologies, including non-volatile memory (Flash Memory, Electrically Erasable Programmable Read-Only Memory (EEPROM), One-Time-Programmable Memory (OTP) and static random-access memory (RAM), for Analog and Mixed Signal Technologies.

11. From 2004 – 2005, I was a Senior Member of the Technical Staff in the Radio-Frequency Identification (RFID) Business Ultra-High Frequency (UHF) Engineering Group. In this role, I contributed to defining the roadmap for RFID next-generation Non-Volatile Memory (NVM) and the Switched Capacitor (SC) technology roadmap for RFID. I contributed to enabling and staffing the IC design

team, and setting up the right design tools, defined technology and simulation methodology to enhance RFID, and participated in debug and analysis of prototype devices as needed.

12. From 2000 – 2004, I was a Manager of Static Random-Access Memory (SRAM) Test Engineering. In this role, I was responsible for managing a group of test engineers that provide embedded SRAM test programs, redundancy analysis, and laser/eFuse repair for Sun SPARC microprocessors.

13. From 1996 – 2000, I was a Senior Design Engineer for Mixed Signal Products and System Interface Team. In this role, I contributed to the circuit design and supervision of layout for various circuit components of multiple mixed-signal and logic products, for example a low-power sigma-delta A/D converter and a custom cable modem chip. I conducted evaluations of statistical modeling and circuit design tools, contributed to evaluation of potential product opportunities utilizing Merged DRAM and Logic technology, conducted architecture studies and cost analysis of product opportunities. I supported analysis and debug of system-related product issues.

14. From 1989 – 1995, I was a Senior Design Engineer and subsequently a Project Design Manager for flash memories. My responsibilities included contributing to and managing the design of the flash memory products.

15. From 1985 - 1989, I was a Senior DRAM Design Engineer. In this role, I was one of the principal contributors to architectural analysis and circuit design of the initial version of the 16Mbit DRAM. I was also responsible for portions of the productization of the 1Mbit DRAM and 4Mbit DRAM generations.

16. From 1979 - 1983, I was a Design Engineer contributing to the design of 16K thru 128K EPROMS and 64K and 1Mbit DRAM generations.

17. In 1989, I obtained a PhD in Electrical and Computer Engineering from Rice University.

18. In 1985, I obtained a M.S. in Electrical and Computer Engineering from Rice University.

19. In 1973, I obtained a B.S.E.E., with honors, from Texas Tech University.

20. In view of the above and my curriculum vitae in Exhibit 1004, I received a doctorate in Electrical and Computer Engineering and years of work experience on technologies including circuit design prior to the priority date of the '701 patent. Thus, as of the earliest claimed priority date of the '701 patent (i.e., March 27, 2007), I was at least a person of ordinary skill in the art of the '701 patent, and I had direct personal knowledge of the technologies involved in the '701 patent.

III. UNDERSTANDING OF PATENT LAW

21. I am not an attorney. For the purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law was provided to me by Requester's attorneys.

22. I understand that prior art to the '701 patent includes patents and printed publications in the relevant art that predate the priority date of the '701 patent. For purposes of this Declaration, and for the reasons set forth in more detail below, I have applied the date of March 27, 2007, the filing date of Japanese Patent Application No. 2007-081754, as the priority date.

23. I have been asked to provide my opinions regarding whether the Challenged Claims of the '701 patent would have been anticipated or obvious to a POSITA at the time of the alleged invention in light of the prior art.

24. I have been informed by counsel that a patent claim is unpatentable as anticipated if each element of that claim is present either explicitly or inherently in a single prior art reference. I have also been informed that, to be an inherent disclosure, the prior art reference must necessarily disclose the limitation.

25. I understand that a claim is also unpatentable if it would have been obvious. Obviousness of a claim requires that the claim would have been obvious from the perspective of a POSITA at the time the alleged invention was made. I

understand that a claim could have been obvious from a single prior art reference or from a combination of two or more prior art references.

26. I understand that an obviousness analysis requires an understanding of the scope and content of the prior art, any differences between the alleged invention and the prior art, and the level of ordinary skill in evaluating the pertinent art.

27. I further understand that a claim would have been obvious if it unites old elements with no change to their respective functions, or alters prior art by mere substitution of one element for another known in the field and that combination yields predictable results. Also, I understand that obviousness does not require physical combination/bodily incorporation, but rather consideration of what the combined teachings would have suggested to POSITAs at the time of the alleged invention. I understand that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.

28. While it may be helpful to identify a reason for this combination, I understand that there is no rigid requirement of finding an express teaching, suggestion, or motivation to combine within the references. When a product is available, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a POSITA can implement a predictable variation, obviousness likely bars its patentability. For the same reason, if a

technique has been used to improve one device and a POSITA would recognize that it would improve similar devices in the same way, using the technique would have been obvious. I understand that a claim would have been obvious if common sense directs one to combine multiple prior art references or add missing features to reproduce the alleged invention recited in the claims.

29. I further understand that certain factors may support or rebut the obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the patented invention, skepticism of those having ordinary skill in the art at the time of invention, unexpected results of the invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field. I understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

30. I am not aware of any allegations by the named inventor of the '701 patent or any assignee of the '701 patent that any secondary considerations tend to rebut the obviousness of any Challenged Claim of the '701 patent.

31. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

32. The analysis in this declaration is in accordance with the above-stated legal principles.

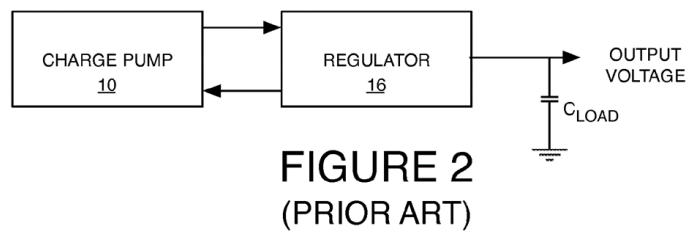
IV. TECHNICAL BACKGROUND

A. Charge Pump System

33. Charge pumps are switched-capacitor circuits commonly employed to obtain an output voltage higher than that of the power supply. EX1008, Pan, 43 (“Charge pumps are circuits that generate a voltage level higher than the chip supply voltage from which they operate.”); EX1014, Frulio, 1:11-14 (“Charge pumps are switched-capacitor circuits employed to obtain either an output voltage higher than that of the power supply (V) or a negative voltage in an electronic system.”).

34. Charge pumps are widely used in the integrated circuit industry to supply voltages in many applications such as power ICs, filters, memories, etc. Flash memory devices are among these applications since high voltage levels are needed to perform flash memory operations such as program and erase. Moreover, due to the trend of increasingly lower voltage supply requirements, a voltage level higher than the voltage supply may also be needed for flash memory read operation. EX1014, Frulio, 1:11-22.

35. It was also well known in the art that it would often be necessary to regulate the output voltage of the charge pump. As shown in FIG. 2 of Frulio below, a regulator circuit 16 may be used to ensure that the output voltage does not exceed a maximum value and does not drop below a minimum value. Various regulation techniques (e.g., pulse-skip regulation, linear regulation) were well known in the art. EX1014, Frulio, 1:40-47.



EX1014, Frulio, FIG. 2

1. Single-Stage and Multi-Stage Charge Pumps

36. It was well-known that a charge pump may include one or more stages. EX1016, Daga, FIGS. 2A-2B (describing a single-stage charge pump), 4 (describing an N-stage charge pump using cascading basic stages of FIG. 2B). Connecting more stages in series can provide a higher voltage boost compared to using a smaller number of stages in series. Each stage in the charge pump contributes to increasing the voltage level, and the total voltage boost is the cumulative effect of all the stages. By connecting multiple stages in series, the voltage boost may be multiplied. In a simplified example, if each stage provides a voltage multiplication factor of 2

(doubling the voltage), and there are 3 stages connected in series, the total voltage boost = $V_{out} - V_{in} = (2^3 - 1) * V_{in} = 7 * V_{in}$.

37. As shown in FIG. 1 of Frulio below, a conventional multi-stage charge pump circuit is illustrated.

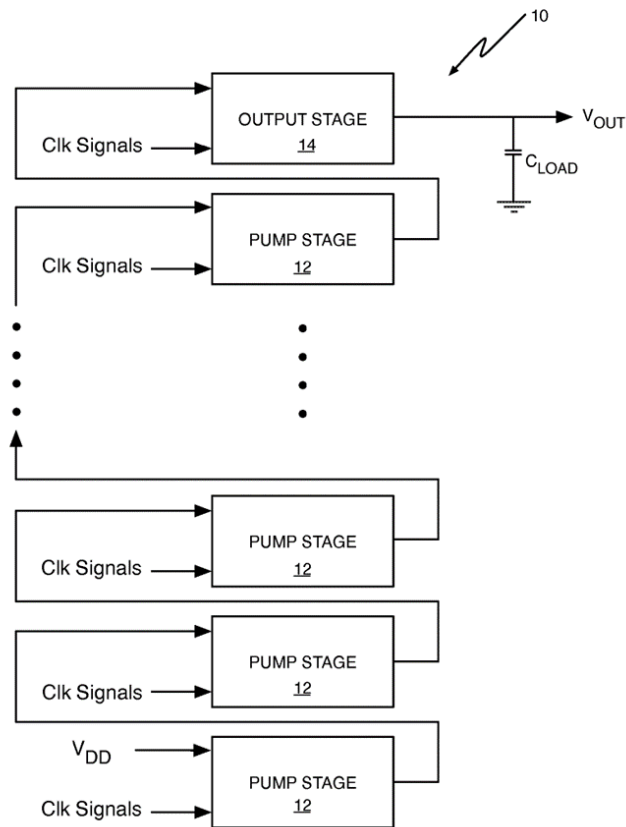


FIGURE 1
 (PRIOR ART)

EX1014, Frulio, FIG. 1

38. Referring to FIG. 1 of Frulio, a conventional charge pump circuits 10 comprise a series of pumping stages 12, the number of which depends on the voltage gain required, and usually an output stage 14. As will be appreciated by persons of ordinary skill in the art, each pumping stage includes one or more capacitors for accumulating charges, and is controlled by one or more clock signals. Voltage multiplication is obtained by properly charging and switching the pumping stage capacitors. Different ways to obtain voltage multiplication are possible by changing the topology of the pump stage, switching order, etc.

2. Pump Stage

39. Various different pump stage designs to be used either in a single-stage charge pump or a multi-stage charge pump were well-known. EX1014, Frulio, 1:23-34. As shown in FIG. 3-2 of Pan, an example simple voltage doubler for implementing a pump stage to generate an output voltage level higher than the supply voltage is illustrated.

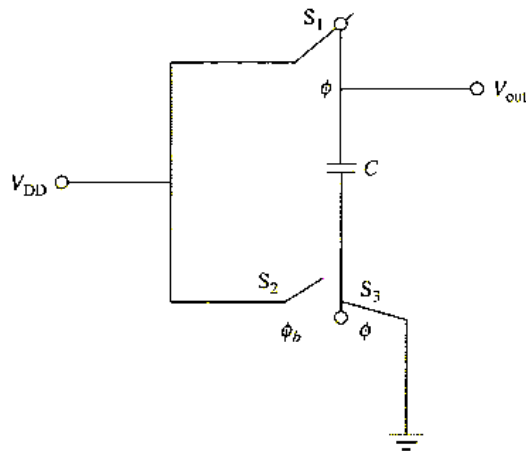


Figure 3-2 Simple voltage doubler:

EX1008, Pan, FIG. 3-2

40. By charging the pump stage capacitor C driven by a clock, a pump stage provides an output voltage level higher than the supply voltage. For example, in the simple voltage doubler of FIG. 3-2 of Pan, during clock phase ϕ , switches S1 and S3 are closed, and the capacitor is charged to the supply voltage V_{DD} . EX1008, Pan, 43. Next, in the second clock phase ϕ_b , switches S1 and S3 are opened and switch S2 is closed, and the bottom plate of the capacitor assumes a potential of V_{DD} , while the capacitor C maintains its charge of $Q = C \cdot V_{DD}$ from the previous phase. This means that $Q = C \cdot (V_{out} - V_{DD}) = C \cdot V_{DD}$, i.e., $V_{out} = 2 \cdot V_{DD}$. EX1008, Pan, 43-44. In other words, to maintain this V_{DD} across itself, the capacitor C forces V_{out} to be $2 \cdot V_{DD}$, thereby providing an output voltage level ($V_{out} = 2 \cdot V_{DD}$) higher than the supply voltage V_{DD} .

41. Various designs of pump stages other than the voltage doublers were also well known. For example, as shown in FIG. 1 of Al-Shamma below, a charge pump stage includes capacitors 160 and 162 for charge storage to raise the output voltage, coupled to a pair of cross-coupled charge transfer switch devices. EX1015, Al-Shamma, FIG. 1, 4:61-64 (“Such a charge pump stage 150 is frequently incorporated as one of a plurality of series-coupled charge pump stages within a charge pump circuit.”); 4:65-5:59 (describing the operation of the charge pump stage of FIG. 1); *see also* EX1016, Daga, FIGS. 2A-2B (describing a single-stage charge pump), FIG. 4 (illustrating an N-stage charge pump using cascading basic stages of FIG. 2B).

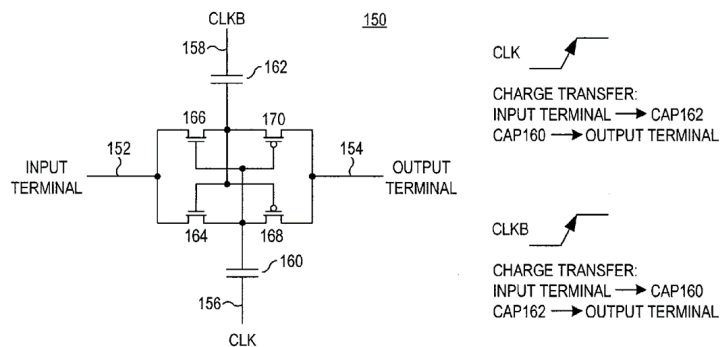


FIG. 1
(PRIOR ART)

EX1015, Al-Shamma, FIG. 1

V. OVERVIEW OF THE '701 PATENT

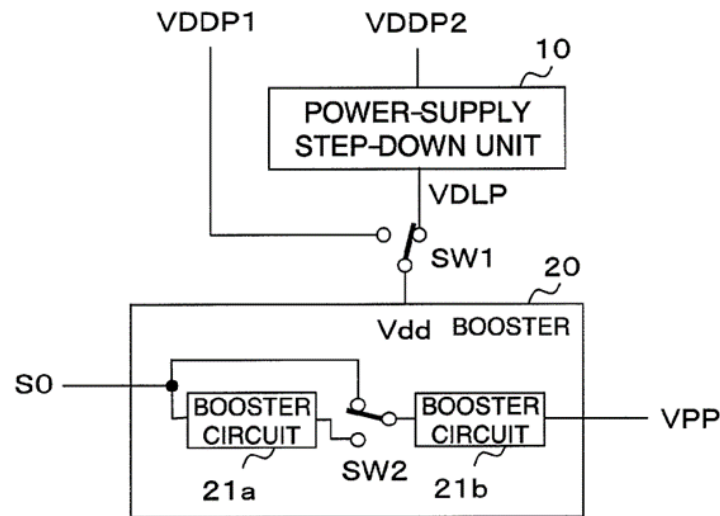
A. Summary

42. In conventional semiconductor storage devices, such as flash or EEPROM, there will be one or more power supply voltages (each called “VDD” or “VCC”). For example, a first power supply voltage (VDD1) of 5V can be used for one section of the device, and a second power supply voltage (VDD2) of 3.3V can be used in another section of the device. In addition, these semiconductor storage devices may periodically require additional, often higher, internally-generated supply voltages, such as 7V, to perform operations such as a memory erase. These internal supply voltages, also called pump voltages or “VPP,” are produced by a booster circuit, also called a charge pump circuit. Continuing with the examples above, it was well known that boosting a first power supply voltage VDD1 of 3.3V to a VPP of 7V is different from boosting a second power supply voltage VDD2 of 5V to 7V.

43. Referring to FIG. 1 of '701 patent below, '701 patent describes that a supply voltage generating circuit includes a switch element SW1 for switching between power supply voltages provided to the booster 20. EX1001, '701 patent 4:49-54. “The switch element SW1 switches between application of the voltage of an external power supply VDDP1 to power supply Vdd of the booster 20 directly or as power supply VDL P following stepping down of the voltage of an external power

supply VDDP2 by the power-supply step-down unit 10.” EX1001, ’701 patent, 4:49-59.

FIG.1



EX1001, ’701 patent FIG. 1

44. The booster 20 includes a second switch SW2 for “switching between the booster circuits 21a and 21b.” EX1001, ’701 patent, 4:60-64. “[S]witch element SW2 changes over the number of booster stages in the booster 20 to one stage, namely the booster circuit 21b, or to two stages, namely the booster circuits 21a and 21b,” based on the selection of switch SW1. EX1001, ’701 patent, 5:1-4.

45. Independent claim 1 of the ’701 patent is representative:

A method for generating a supply voltage, comprising:

selecting one of a first input node supplied with a first power supply voltage and a second input node supplied with a second power supply voltage that is higher than the first power supply voltage;

coupling a selected one of the first and second input nodes to booster circuitry comprising a plurality of booster stages to provide an output voltage, wherein selection of the first input node corresponds to a first number of booster stages and selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number; and

changing the booster circuitry from the first number of booster stages corresponding to selection of the first input node to the second number of booster stages when the second input node is selected.

46. As discussed in detail below, the device and method presented in the '701 patent, namely, changing the number of booster stages of a booster circuitry according to selection of the input power supply voltage, was well known to persons of ordinary skill in the art before the priority date of the '701 patent.

B. Priority Date of the '701 Patent

47. I understand that the '701 patent was filed as App. No. 14/480,768 (“’768 application”) (EX1002) on September 9, 2014, which is a continuation of App. No. 13/912,845 filed Jun. 7, 2013, which is a continuation of App. No. 12/052,422 filed Mar. 20, 2008, which claims the benefit of the priority of Japanese Patent Application No. 2007-081754, filed on Mar. 27, 2007. I understand that the earliest alleged priority date of the '701 patent is March 27, 2007, and all the prior art cited in the grounds predates March 27, 2007.

C. Prosecution History and Reasons for Allowance

1. Prosecution History of '422 App (Parent of '701 Patent)

48. During the prosecution of the '422 app, the pending claims were rejected under sections 102 and 103 over Kimura (US20070210774). EX1009, '422 app, 309-312. Specifically, Examiner rejected claim 2 under 103 over Kimura, where claim 2 recited that “the capacitor element is constituted by a MOS transistor having a gate oxide film, and the gate oxide film is a thickness less than a thickness of a gate oxide film of a MOS transistor included in a load circuit having the output of said booster as its power supply.” EX1009, '422 app, 311, 288. Examiner explained that “it would be obvious at the time the invention was made, to a person having ordinary skill in the art to use **optimize the general capacitor in such a way wherein the gate oxide film is a thickness less than a thickness of a gate oxide film of a MOS transistor in the load.**” EX1009, '422 app, 311, 288. Applicant did not directly dispute Examiner’s rejection of claim 2. EX1009, '422 app, 271-273, 298.

49. After cancellation of claims (including claim 2) and substantial amendments in response to multiple Office Actions and Final Office Actions, Notice of Allowance issued. EX1009, '422 app, 8-14. The allowed claims do not include limitations related to a thickness of a gate oxide film of a MOS transistor.

2. Prosecution History of '845 App (Parent of '701 Patent)

50. During the prosecution of the '845 app, Examiner indicated that claim 9 recited allowable subject matter, where claim 9 recited “the capacitor of the first boosting circuit is coupled to the voltage output node and the capacitor of the second boosting circuit is disconnected from each of the voltage output node and the capacitor of the first boosting circuit.” EX1010, '845 app, 76.

51. Notice of Allowance issued after Applicant incorporated features of dependent claim 9 to the independent claim. EX1010, '845 app, 8-16, 39.

3. Prosecution History of '701 Patent

52. In Office Actions dated October 7, 2014 and January 9, 2015, Examiner rejected claims 1-10 as anticipated over Imanaka (US 2009/0160367) and Williams (US 2009/0039947) respectively. '768 app, 126-133, 144-151.

53. In Response of July 9, 2015, Applicant amended claim 1, cancelled claims 2-10, and added new claim 11-27. '768 app, 101-105. Applicant further argued that Williams, which was filed Aug. 8, 2007, does not qualify as prior art because “a proper foreign priority claim to JP Application No. 2007-081754, and has been accorded the foreign priority date of March 27, 2007.” *Id.*

54. After Applicant amended the claims, Notice of Allowance issued on August 3, 2015, and the examiner's statement of reasons for allowance stated that the prior art of record failed to suggest or disclose “wherein the booster circuitry

configured to have a first number of booster stages when the first input node is selected to be changed to a second number of booster stages when the second input node is selected, the second number being less than the first number.” EX1002, ’768 app, 28.

VI. LEVEL OF ORDINARY SKILL IN THE PERTINENT ART

55. I understand that the level of ordinary skill may be reflected by the prior art of record, and that a POSITA to which the claimed subject matter pertains would have the capability of understanding the scientific and engineering principles applicable to the pertinent art. I understand that one of ordinary skill in the art has ordinary creativity, and is not a robot.

56. I understand there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including (1) the levels of education and experience of persons working in the field at the time of the invention; (2) the sophistication of the technology; (3) the types of problems encountered in the field; and (4) the prior art solutions to those problems. There is likely a wide range of educational backgrounds in the technology fields pertinent to the ’701 patent.

57. I am very familiar with the knowledge and capabilities that a person of ordinary skill in the art of circuit design would have possessed on March 27, 2007. Specifically, my experience in the industry and with engineers practicing in the industry during the relevant timeframe allowed me to become personally familiar

with the knowledge and capabilities of a person of ordinary skill in the area of circuit design. Unless otherwise stated, my testimony below refers to the knowledge of one of ordinary skill in the art in the field of circuit design at the time of the priority date of the '701 patent.

58. In my opinion, a person having ordinary skill in the art of the '701 patent at the time of its filing would have been a person having: (1) at least an undergraduate degree in electrical or computer engineering or a closely related scientific field, or similar advanced post-graduate education in this area; and (2) 2-3 years of professional experience relating to circuit design. Furthermore, a person with less formal education but more experience, or more formal education but less experience, could have also met the relevant standard for POSITA. Such a person of ordinary skill in the art would have been capable of understanding the '701 patent and the prior art references discussed herein. This level of skill in the art would apply at the assumed earliest priority date of the '701 patent (i.e., March 27, 2007).

59. Based on my education, training, and professional experience in the field of the claimed invention, I am familiar with the level and abilities of a person of ordinary skill in the art at the time of the claimed invention. Additionally, I met at least these minimum qualifications to be a POSITA at least as of March 27, 2007. Further, although my qualifications may exceed those of the hypothetical person having ordinary skill in the art defined above, my analysis and opinions regarding

the '701 patent have been rendered from the perspective of a person having ordinary skill in the art at the time of the invention.

VII. CLAIM CONSTRUCTION

60. It is my understanding that in order to properly evaluate the '701 patent, the terms of the claims must first be interpreted. It is my understanding that for the purposes of this inter partes review, the claim terms are given their ordinary and accustomed meaning as would be understood by one of ordinary skill in the art, unless the inventor has set forth a special meaning for a term. In order to construe the claims, I have reviewed the entirety of the '701 patent along with the prosecution history of the '701 patent.

61. Based on my review of the '701 patent, it is my opinion that a specific construction is not necessary for any claim term. No express construction is necessary for this proceeding to show the unpatentability of the claims.

VIII. GROUNDS

62. The discussion below provides a detailed analysis of how the prior art references disclose, teach, or suggest the elements of the Challenged Claims of the '701 patent.

63. As part of my analysis, I have considered the scope and content of the prior art and any potential differences between the claimed subject matter and the prior art. I conducted my analysis as of the priority date of the '701 patent of March

27, 2007. I have also considered the level of ordinary skill in the pertinent art as of that date.

64. I describe in detail below the scope and content of the prior art, as well as any differences between the claimed subject matter and the prior art, on an element-by-element basis for each Challenged Claim. This analysis supports my finding that the elements of the Challenged Claim are disclosed in the prior art, or that the differences between the Challenged Claim and the prior art discussed herein are such that the subject matter as a whole would have been anticipated or obvious at the time of the filing of the '701 patent to a POSITA to which the subject matter pertains.

65. As described in detail below, the claimed subject matter of the Challenged Claims would have been unpatentable in view of the teachings of the identified prior art references as well as the knowledge of a POSITA.

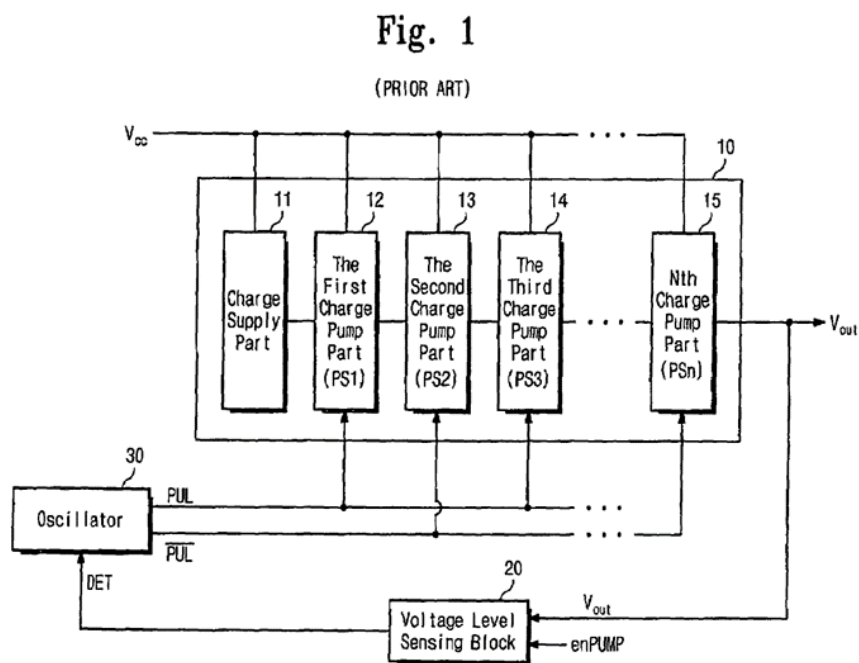
66. I will now describe, in the grounds below, on an element-by-element basis how the prior art discloses or teaches all elements of Challenged Claims. Unless otherwise noted, all *italic*, and **bold italic** emphases in any quoted material have been added.

A. Prior Art

1. Summary of Zhang

67. Like the '701 patent, Zhang is in the field of using a charge pump circuit to provide a supply output voltage. Specifically, it describes a “Charge Pump Circuit Operating Responsive to a Mode,” and describes “a charge pump circuit that operates responsive to a test or general operation mode.” EX1005, Zhang, Title, Abstract.

68. Specifically, as shown in FIG. 1 below, Zhang describes that a conventional charge pump circuit includes “a voltage sensing block 20, an oscillator 30, and a charge pump block 10.” EX1005, Zhang, 1:15-18. “The charge pump block 10 comprises a charge supply part 11 and a plurality of charge pump parts 12-15. The charge supply part 11 receives an external voltage VCC, and provides supply charges to a first charge pump part PSI. The charge pump parts PS1, PS2, PS3, ..., PSn are serially connected. The charge pump parts 12-15 generate an output voltage Vout by pumping charges supplied from the charge supply part 11.” EX1005, Zhang, 1:33-39.



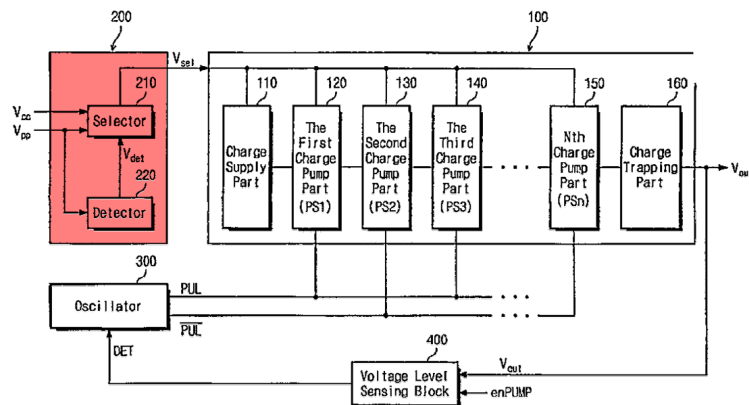
EX1005, Zhang, FIG. 1

69. Zhang provides that the conventional charge pump circuit as shown in FIG. 1 “pre-charges the output voltage V_{out} corresponding to the external voltage VCC at each node of the charge supply part 11 and the charge pump parts 12-15. Accordingly, the time to precharge increases in the output voltage V_{out} . This additional time is undesired, particularly where testing integrated chips that require high voltages quickly.” EX1005, Zhang, 1:63-2:2.

70. To address this issue, Zhang describes an invention, as shown in annotated FIG. 4 below, that operates “both in a test and in a general operation mode,” and provides “a selecting circuit block [200 that] generates a selected voltage that is one of a high voltage and a supply voltage to the at least one charge pump

part, the high voltage having a level higher than the supply voltage.” EX1005, Zhang, 2:9-19.

Fig. 4



EX1005, Zhang, FIG. 4, annotated

71. Referring to FIG. 4, Zhang describes that “the charge pump circuit ... comprises a selecting circuit block 200.” EX1005, Zhang, 3:19-20. “The selecting circuit 200 includes a selector 210” selecting from VCC and VPP, where “power supply voltage VCC refers to the power voltage operating in general operation mode,” and “[t]he voltage VPP refers to a high voltage provided externally during a test operation mode. The high voltage VPP may be applied externally in the test operation mode as well as during the general operation mode.” EX1005, Zhang, 3:21-27.

72. As such, by using a selecting circuit block 200 to supply a selected voltage from VCC and VPP to the charge pump block 100, “the charge pump circuit

can obtain a wanted output voltage V_{out} within a short time by further including selective means capable of applying high voltage rather than the power voltage V_{CC} .” EX1005, Zhang, 5:12-15.

2. Summary of Javanifard

73. Like the '701 patent, Javanifard is in the field of using charge pump circuits to provide a power supply voltage. EX1006, Javanifard, Title, 1:6-11. Specifically, it relates to “providing a charge pump having a variable number as opposed to a fixed number of stages **according to charge pump power supply input levels and desired charge pump output levels.**” EX1006, Javanifard, 1:8-11. Javanifard’s variable stage charge pump provides great design flexibility, which can both “accommodate different output levels for a given charge pump power supply input level,” and “accommodate a given output level for different charge pump power supply input levels.” EX1006, Javanifard, 2:22-24.

a. Embodiment 1

74. Specifically, as shown in FIG. 1 below, Javanifard’s variable stage charge pump achieves these objects by providing different configurations, where **“the number of stages and the coupling of the charge pump stages** to each other may be varied.” EX1006, Javanifard, 3:19-21. The variable stage charge pump may be identified as an “X/Y” stage pump, where “X” refers to the number of rungs that may be coupled in series, and “Y” indicates the number of stages for each fixed stage

charge pump. FIG. 1 of Embodiment 1 illustrates a “2/2” stage pump, including two rungs, each rung including a two-stage charge pump.

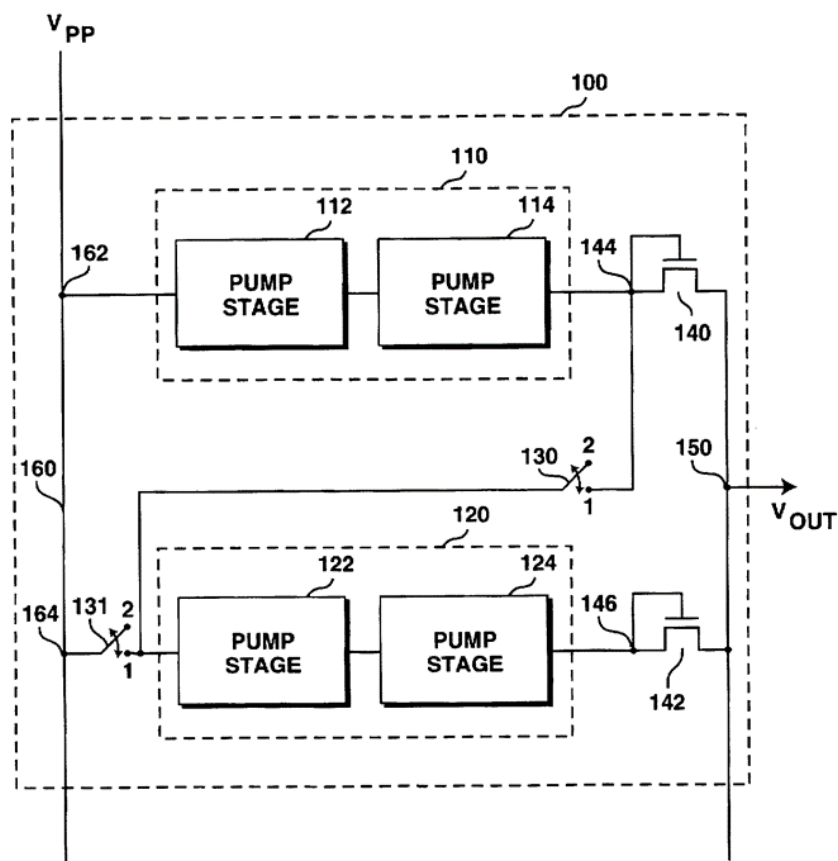


Figure 1

EX1006, Javanifard, FIG. 1

75. As shown in Table 1 of Javanifard below, there are three applicable configurations (corresponding to the first, second, and third rows of Table 1) out of four configurations, “[b]y choosing a different one of the four position combinations [of switches 130 and 131], the number of stages and the couple of the charge pump

stages to each other can be varied.” EX1006, Javanifard, 3:19-21. The fourth configuration (the fourth row) is included for completeness but is not to be used. EX1006, Javanifard, 3:65-4:5. “The control for the switches would be a function of the available power supply voltage, VPP, and the desired variable stage charge pump output voltage.” EX1006, Javanifard, 5:65-67. The control for the switches may additionally be a function of power save mode or current requirement, e.g., using a single charge pump 110 for power save mode (e.g., row 1 of Table 1), and using parallel-coupled charge pumps 110 and 120 for twice the amount of current (e.g., row 2 of Table 1). EX1006, Javanifard, 3:39-42, 3:50-53.

TABLE 1			
Switch 130	Switch 131	Charge Pump 110	Charge Pump 120
OFF	OFF	ON	OFF
OFF	ON	ON	parallel-coupled to charge pump 110
ON	OFF	ON	series-coupled to charge pump 110
ON	ON	N/A	N/A

EX1006, Javanifard, Table 1

76. Corresponding to row 1 of Table 1, Javanifard explains that “if both switches are off, charge pump 110 will be the only charge pump providing voltage to node 150. Thus, because charge pump 110 is a two stage charge pump, this configuration of switches 130 and 131 will effectively result in a two stage charge

pump,” and this configuration “might be used in a power saving mode.” EX1006, Javanifard, 3:35-40. Corresponding to row 2 of Table 1, Javanifard explains that “[i]f switch 130 is off and switch 131 is on,” “110 and 120 are parallel-coupled, charge pump 110 will be able to provide approximately twice the amount of current as was the case when only charge pump 110 was operating.” EX1006, Javanifard, 3:42-52.

77. Corresponding to third 3 row of Table 1, Javanifard explains that “[i]f switch 130 is on and switch 131 is off, charge pump 120 will be coupled so that charge pumps 110 and 120 are series-coupled. In other words, the input voltage for charge pump 120 will be provided from the output of charge pump 110. Because both 110 and 120 are two stage charge pumps, this means that charge pump 100 will effectively be a four stage charge pump with all four stages serially coupled.” EX1006, Javanifard, 3:54-60. “In this configuration, charge pump 100 will provide approximately twice the output voltage at node 150 as the previous two cases.” EX1006, Javanifard, 3:60-63.

78. In addition to the embodiment of FIG. 1 and Table 1 (referred to as **Embodiment 1**), Javanifard describes additional embodiments.

b. Embodiment 2

79. Embodiment 2 is described with reference to FIG. 2 (reproduced below) and Tables 2 and 3, and describes a multi-power-source charge pump system that

selects from multiple power sources (e.g., VCC and VPP), and provides the selected power supply source to a variable stage charge pump. EX1006, Javanifard, 6:61-64.

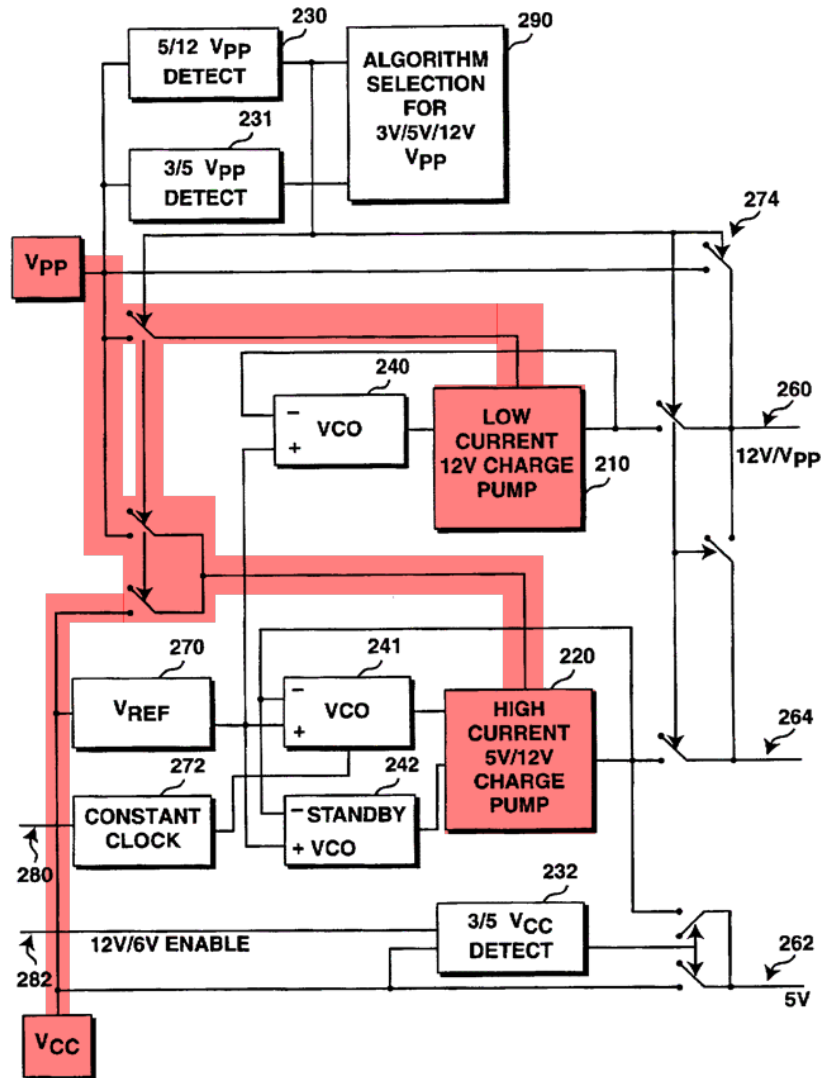


Figure 2

EX1006, Javanifard, FIG. 2, annotated

80. As shown in annotated FIG. 2 above, FIG. 2 “illustrates the power supply circuitry for a flash memory including variable stage charge pumps for accommodating a 5 volt, 9 volt, and 12 volt voltage level from either a 3.3 volt or 5 volt power supply,” using variable stage charge pumps 210 and 220. EX1006, Javanifard, 6:61-64. Two different power supplies, VCC and VPP, to two input nodes respectively. Switches are used to select from the different power supplies VCC and VPP, and the selected input node is coupled to the variable stage charge pumps 210 and 220, which are configured based on the input power supply voltage (VCC or VPP) to provide required output voltage levels (e.g., at the output nodes 262 or 264). EX1006, Javanifard, 6:44-52 (describing that “power for the flash memory device is provided **by two sources**. These sources include a VCC line and a VPP line. The VCC line is the primary power source for the flash device. The supplemental voltage provided by supply line, VPP, is typically needed only when writing or erasing the memory because of the higher voltages needed during those operations. In one embodiment, VCC is approximately 5 volts. VPP, however, might be 3.3, 5, or 12 volts.”).

81. A POSITA would have understood that FIG. 2 is an example of Embodiment 2, and that Embodiment 2 is not limited by FIG. 2.

c. Embodiment 3

82. Embodiment 3 is described with reference to FIG. 3 illustrating “a variable stage charge pump coupled to a flash memory array.” EX1006, Javanifard, 2:37-38. Similar to the variable stage charge pump of Embodiment 1, Javanifard describes that a variable stage charge pump “might be constructed with n rungs of charge pumps, each charge pump having y stages.” EX1006, Javanifard, 4:49-51. FIG. 3 of Embodiment 3 illustrates a “12/2” stage pump, including twelve rungs, each rung including a two-stage charge pump.

3. Summary of Kang

83. Like the '701 patent, Kang is in the field of using a charge pump circuit to provide a supply output voltage. Specifically, Kang is titled “Charge Pump Circuits with Low Area and High Power Efficiency for Memory Applications,” and describes charge pump circuits that use “the thin-oxide MOSFETs as the pumping capacitors” (also referred to as thin-oxide capacitors) to “reduce the area of charge pumps greatly while keeping their driving capability.” EX1020, Kang, Title, Abstract. Kang was published in Journal of Semiconductor Technology And Science (JSTS), Vol.6, No.4, December, 2006. As shown in JSTS website (<http://jsts.org/jsts/>), JSTS is an open access journal with accessible both in print version (ISSN:1598-1657) and online (ISSN:2233-4866). A POSITA interested in

improving charge pump designs would have looked to Kang for development in the integrated circuit technology including charge pump designs.

84. Referring to FIGS. 1(a) and 1(b) of Kang below, Kang illustrates a conventional charge pump using capacitors made with thick-oxide transistors (FIG. 1(a)) and proposes a low-area pump circuit where “C1, C2, and C3 as shown in Fig. 1(b) can be made with the **thin-oxide transistors**.” EX1020, Kang, 258.

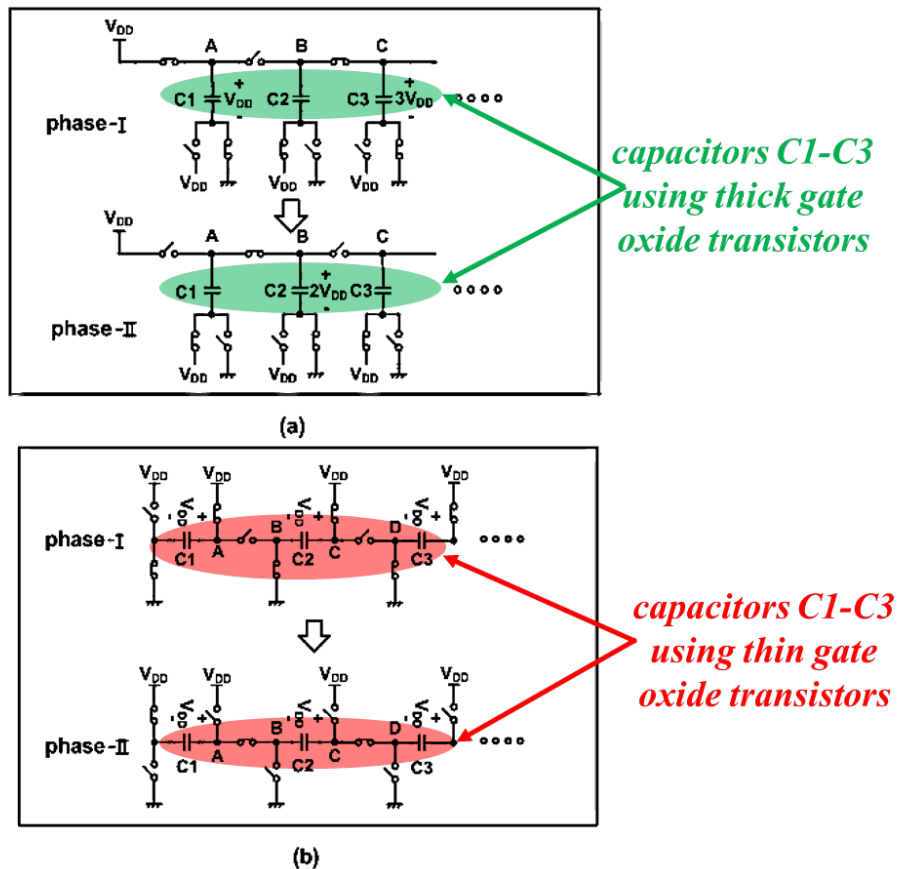


Fig. 1. (a) A conceptual diagram of the conventional charge pump (b) A conceptual diagram of new charge pump.

EX1020, Kang, FIG. 1, annotated

85. Kang provides that by using capacitors formed using thin oxide transistors, in the charge pump of FIG. 1(b), “the layout area of C1, C2, and C3 becomes **smaller** compared with that of thick oxide transistors,” thereby “reducing the total pump area.” EX1020, Kang, 258. Kang also provides additional charge pump designs (e.g., 3-stage pumps of FIGS. 2(c) and 2(d)) where in each pump stage, the pumping capacitor is a thin-oxide capacitor.

4. Analogous Art

86. Zhang, Javanifard, and Kang are analogous art to the '701 patent because each is at least (1) in the same field of endeavor (charge pump system); or (2) reasonably pertinent to a problem with which the inventor of the '701 patent was involved (e.g., supporting multiple power supply sources and reducing chip area). *Compare* EX1001, Title (“Supply Voltage Generating Circuit”), Abstract (“A supply voltage generating circuit that enables a reduction in chip area includes: a booster for outputting a boosted voltage upon generating the boosted voltage by charge pumping of a capacitor element”); EX1005, Zhang, 1:10-13 (“The present invention relates to...charge pump circuits operating responsive to a mode that enables selection of a power voltage or an external high voltage.”); EX1006, Javanifard, 1:8-11 (“this invention relates to providing a charge pump having a variable number as opposed to a fixed number of stages according to charge pump power supply input levels and desired charge pump output levels.”); EX1020, Kang,

Title (“Charge Pump Circuits with Low Area and High Power Efficiency for Memory Applications”), Abstract (describing charge pump designs to “reduce the area of charge pumps greatly while keeping their driving capability.”).

B. Ground 1: Claims 1-18 are Rendered Obvious under § 103 over Zhang in view of Javanifard

87. In my opinion, Zhang in view of Javanifard renders claims 1-18 of the '701 patent obvious.

88. It is noted that while the analysis below mainly focuses on the example of FIG. 1 and Table 1 of Javanifard providing a “X=2/Y=2 stage pump,” in the combination of Zhang and Javanifard, it would have been obvious to a POSITA to use various suitable X, Y, and pump stage designs based on the design needs (e.g., to provide a required output voltage according to the different power supply input levels).

89. Further, the analysis below relies on pump stages (e.g., pump stages 112, 114, 122, and 124 of Javanifard) to disclose the claimed “*booster stages*,” as would have been understood by a POSITA. *See, e.g.*, EX1017, Fukui, 2:13-45 (referring to stages in a charge pump as “boosting stage” and “pump stage” interchangeably). To the extent that Patent Owner asserts that each claimed “*booster stage*” requires a charge pump circuit, Javanifard’s charge pump circuits (e.g.,

charge pump circuits 110 and 120) disclose such asserted “*booster stages*” and the associated configuration changes (e.g., by using switch 130) for the same reasons.

1. Reasons to Combine Zhang and Javanifard

90. A POSITA would have been motivated to apply Javanifard’s teaching of a variable stage charge pump in Zhang’s multi-power-source charge pump system to produce the obvious, beneficial, and predictable results of a variable stage charge pump system, which can both “accommodate different output levels for a given charge pump power supply input level,” “accommodate a given output level for different charge pump power supply input levels,” and provide flexibility for design needs (e.g., power saving mode, and current requirements), area reduction, and performance improvement, as taught by Javanifard.

91. **First**, as discussed at VIII.A.4, like the ’701 patent, Zhang and Javanifard are analogous prior art to the ’701 patent, are in the same field of endeavor pertaining to generating a supply voltage using charge pump systems. *See, e.g.*, EX1001, ’701 patent Title, 1:14-20 (Field of the Invention) (“This invention relates to a supply voltage generating circuit and, more particularly, to a supply voltage generating circuit for generating a boosted voltage within a semiconductor storage device.”); EX1005, Zhang, 1:10-13 (“The present invention relates to high-voltage generators and, more specifically, to charge pump circuits operating responsive to a mode that enables selection of a power voltage or an

external high voltage.”); EX1006, Javanifard, 1:8-11 (“This invention relates to the field of charge pumps. More particularly, this invention relates to providing a charge pump having a variable number as opposed to a fixed number of stages **according to charge pump power supply input levels and desired charge pump output levels.**”). In fact, another patent in the Javanifard family, US 5,781,473 (“Javanifard 473”), was listed on the face of Zhang and cited by examiner as anticipating claims of Zhang. EX1007, ’667 app, 213.

92. **Second**, Javanifard explicitly provides motivations to apply its teaching of the variable stage charge pump to replace the fixed stage charge pump in Zhang’s charge pump system. Javanifard addresses various disadvantages (e.g., area usage, performance including pump efficiency, lack of flexibility) of using the fixed stage charge pump, including, e.g., “us[ing] a number of charge pump circuits each having a fixed number of stages ...each charge pump circuit requires a dedicated space in the integrated circuit,” “the fixed stage method typically sacrifices performance at one power supply voltage to accommodate another power supply voltage.” EX1006, Javanifard, 1:67-2:2. Javanifard achieves area reduction by using a single variable stage charge pump circuit to provide different output levels, and improves performance (e.g., pump efficiency) by configuring the number of pump stages based on the power supply voltage and the desired output voltage level. Javanifard’s variable stage charge pump can both “accommodate

different output levels for a given charge pump power supply input level,”

“accommodate a given output level for different charge pump power supply input levels,” and provide flexibility for various design needs (e.g., configurations based on power saving mode, and/or current requirements). EX1006, Javanifard, 2:18-24, 3:39-31, 3:50-53.

93. A POSITA facing the need to improve its charge pump system would have looked to Javanifard and been motivated to apply Javanifard’s teachings of the variable stage charge pump in the multi-power-source charge pump system of Zhang using fixed stage charge pump, because Javanifard’s teachings provide the obvious, beneficial, and predictable results of a power supply generation circuit that can both “accommodate different output levels for a given charge pump power supply input level,” “accommodate a given output level for different charge pump power supply input levels,” with improved flexibility for design needs (e.g., power saving mode, and current requirements), area reduction, and performance improvement, as taught by Javanifard.

94. Furthermore, while Zhang describes “a charge pump circuit that operates responsive to a test or general operation mode,” Zhang’s teachings including its selector circuit are not limited for only “a test or general operation mode.” *See*, EX1005, Zhang, 5:23-51 (claiming a charge pump circuit including a selector circuit without any operation mode requirement). As such, a POSIA would

have been motivated to apply Javanifard's teachings in Zhang to provide a multi-power-source charge pump to support a device having multiple operation modes, including a device having "a test or general operation mode" and devices having other operation modes (e.g., a memory device having different read, write, programming modes). *See, e.g.*, EX1006, Javanifard, FIG. 2 (illustrating variable stage charge pumps used for a multi-power-source memory device with different modes).

95. **Finally**, applying Javanifard's teachings in embodiments of Zhang would have been no more than the combination of known elements according to known methods (e.g., incorporating a charge pump circuit design in a multi-power-source charge pump system according to the known IC design) obvious to a POSITA. For example, techniques for configuring the variable stage charge pump (e.g., using control circuitry to generate signals to control the switches in the variable stage charge pump based on selected power supply and desired output voltage) were well-known. Techniques for designing (e.g., using IC design and simulation tools) and making an IC including various components like charge pumps were well-known.

96. As such, the combination of Javanifard's variable stage charge pump with the multi-power-source charge pump system of Zhang is nothing more than the

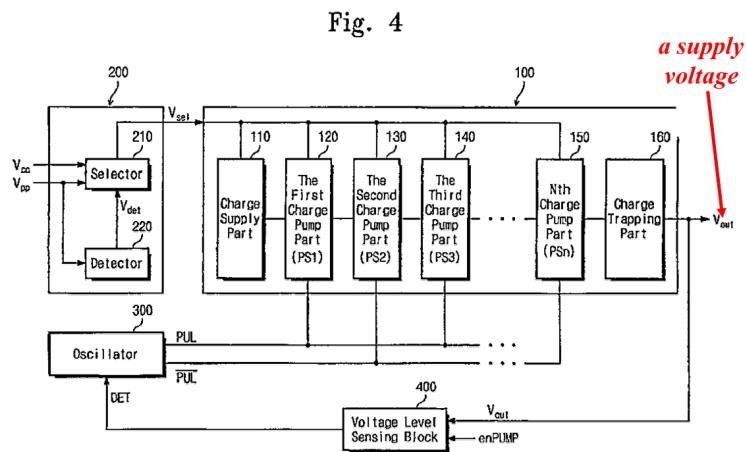
combination of known elements applying known methods, and would have been obvious to a POSITA.

2. Claim 1 would have been obvious over Zhang in view of Javanifard

[1.0] 1. A method for generating a supply voltage, comprising:

97. To the extent that the preamble is limiting, Zhang in view of Javanifard renders it obvious.

98. As shown in annotated FIG. 4 below, Zhang describes generating, using a charge pump circuit, an output voltage V_{out} (a supply voltage). Specifically, the charge pump circuit includes “a charge pump block 100, a selecting circuit block 200, an oscillator 300, and a voltage level sensing block 400,” and generates an output voltage V_{out} . EX1005, Zhang, 2:55-3:2; *see also* EX1005, Zhang, FIG. 8.



EX1005, Zhang, FIG. 2, annotated

99. Similarly, Javanifard describes a variable stage charge pump providing a supply voltage in integrated circuits, e.g., to “provide the proper voltages for the

memory circuitry,” which can both accommodate “a given output level for different charge pump power supply input levels” and “different output levels for a given charge pump power supply input level.” EX1006, Javanifard, FIGS. 1, 2, 3, 2:18-24; 6:56-59.

100. In the combination of Zhang and Javanifard, Javanifard’s teaching of a variable stage charge pump is applied in Zhang’s charge pump system, such that the charge pump system generates a supply voltage, while the charge pump system has the flexibility to both accommodate “a given output level for different charge pump power supply input levels” and “different output levels for a given charge pump power supply input level.” EX1006, Javanifard, 2:18-24.

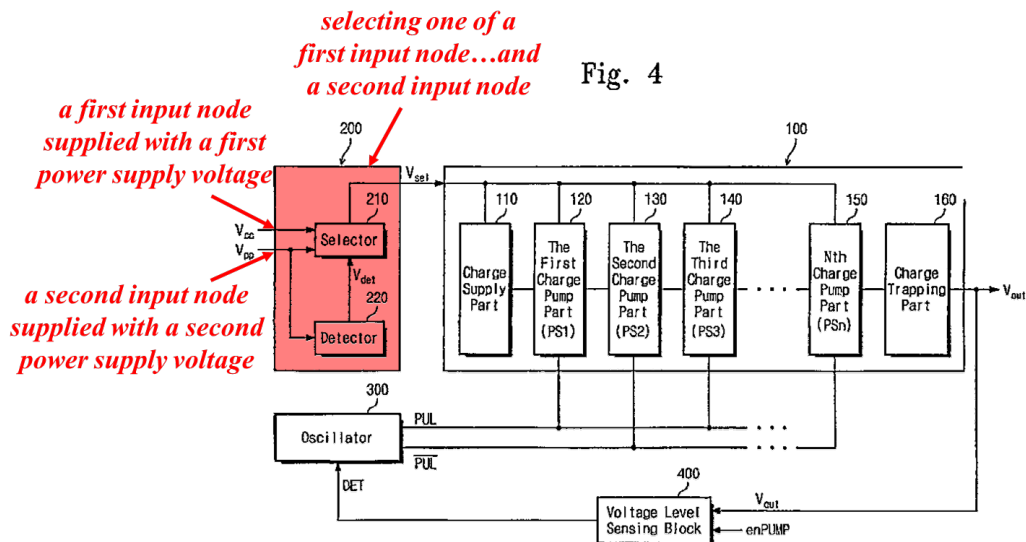
101. Accordingly, Zhang in view of Javanifard renders obvious “[a] *method for generating a supply voltage*” as claimed.

[1.1] selecting one of a first input node supplied with a first power supply voltage and a second input node supplied with a second power supply voltage that is higher than the first power supply voltage;

102. Zhang discloses or at least renders obvious selecting one of a first input node supplied with a first power supply voltage and a second input node supplied with a second power supply voltage that is higher than the first power supply voltage.

103. Specifically, as shown in annotated FIG. 4 of Zhang below, Zhang describes a selecting circuit block 200 that selects one of a first node supplied with VCC (a first power supply voltage) and a second node supplied with VPP (a second

power supply voltage), where “the high voltage VPP is **higher than** the power voltage VCC.” EX1005, Zhang, 3:34-36; *see also* EX1005, Zhang, FIG. 8, 5:5-7 (illustrating that VPP (8V) is higher than VCC (1.8V)).



EX1005, Zhang, FIG. 4, annotated

104. Referring to FIG. 4, Zhang describes that the “charge supply part 110 provides a charge corresponding to **voltage Vsel provided, in turn, by the selecting circuit block 200.**” EX1005, Zhang, 2:62-64. Zhang provides that the “selecting circuit block 200 includes a selector 210 and a detector 220. In the specification power supply voltage VCC refers to the power voltage operating in general operation mode. The voltage VPP refers to a high voltage provided externally during a test operation mode. The high voltage VPP may be applied externally in the test operation mode as well as during the general operation mode.” EX1005, Zhang, 3:21-27.

105. Zhang describes that the “selector 210 selects between the power voltage VCC and the high voltage VPP. The detector 220 detects the level of the high voltage VPP to generate detection signal VDET. The detector 220 enables the detection signal VDET when the high voltage VPP is higher than the power voltage VCC. The selector 210 switches between the power voltage VCC to the high voltage VPP responsive to the detection signal VDET. Put differently, the signal VSEL is VCC in the general operation mode and VPP in the test operation mode allowing for a high Voltage within a short time.” EX1005, Zhang, 3:29-40; *see also* EX1005, Zhang, FIGS. 6 and 7 (providing example selector 210 and detector 220 of FIG. 4).

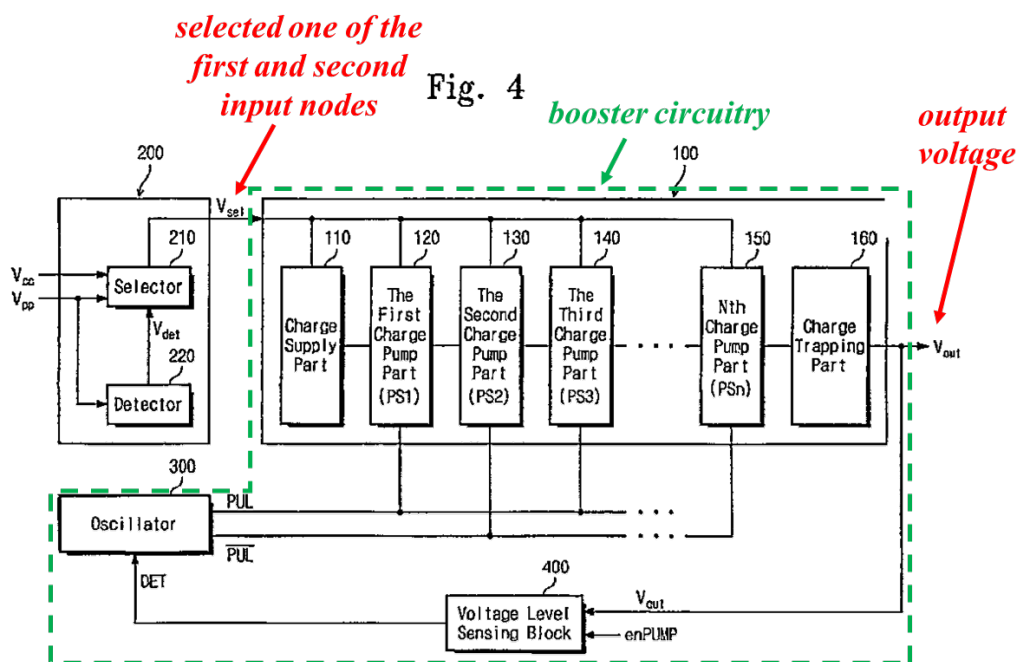
106. Accordingly, Zhang discloses or renders obvious “*selecting one of a first input node supplied with a first power supply voltage and a second input node supplied with a second power supply voltage that is higher than the first power supply voltage*” as claimed.

[1.2.1] coupling a selected one of the first and second input nodes to booster circuitry comprising a plurality of booster stages to provide an output voltage,

107. Zhang in view of Javanifard renders obvious coupling a selected one of the first and second input nodes to booster circuitry comprising a plurality of booster stages to provide an output voltage.

108. **First**, as shown in annotated FIG. 4 below, Zhang describes coupling Vsel (a selected one of the first and second input nodes) to a booster circuitry

(including charge pump block 100) to provide V_{out} (an output voltage), which is a boosted voltage (e.g., 10V) that is higher than V_{sel} (e.g., one of $V_{CC} = 1.8V$ and $V_{PP} = 8V$). The charge pump block 100 of the booster circuitry includes a plurality of booster stages (First Charge Pump Part PS1, Second Charge Pump Part PS2, ... Nth Charge Pump Part PSn).



EX1005, Zhang, FIG. 4, annotated

109. **Second**, Javanifard describes coupling an input node with a power supply voltage to a booster circuitry comprising a plurality of booster stages to provide an output voltage.

110. For example, referring to annotated FIG. 1 of Javanifard below, Javanifard describes that “[a] power supply voltage, V_{PP} , provides the supply

voltage to common input bus 160,” which is coupled to a variable stage charge pump 100 (booster circuitry) providing an output voltage V_{OUT} . EX1006, Javanifard, 2:52-53. The variable stage charge pump 100 (booster circuitry) includes a plurality of pump stages 112, 114, 122, 124 (booster stages). It was well-known in the art that pump stages are also referred to as booster stages or boosting stages. *See, e.g.*, EX1017, Fukui, 2:13-45 (referring to stages in a charge pump as “boosting stage” and “pump stage” interchangeably).

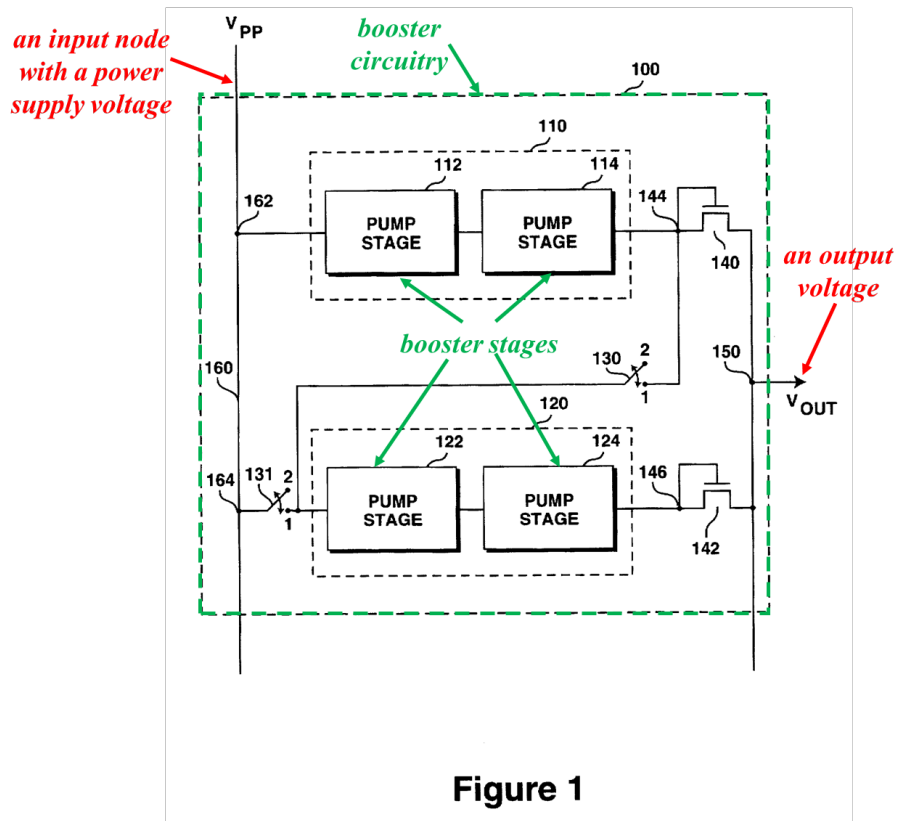
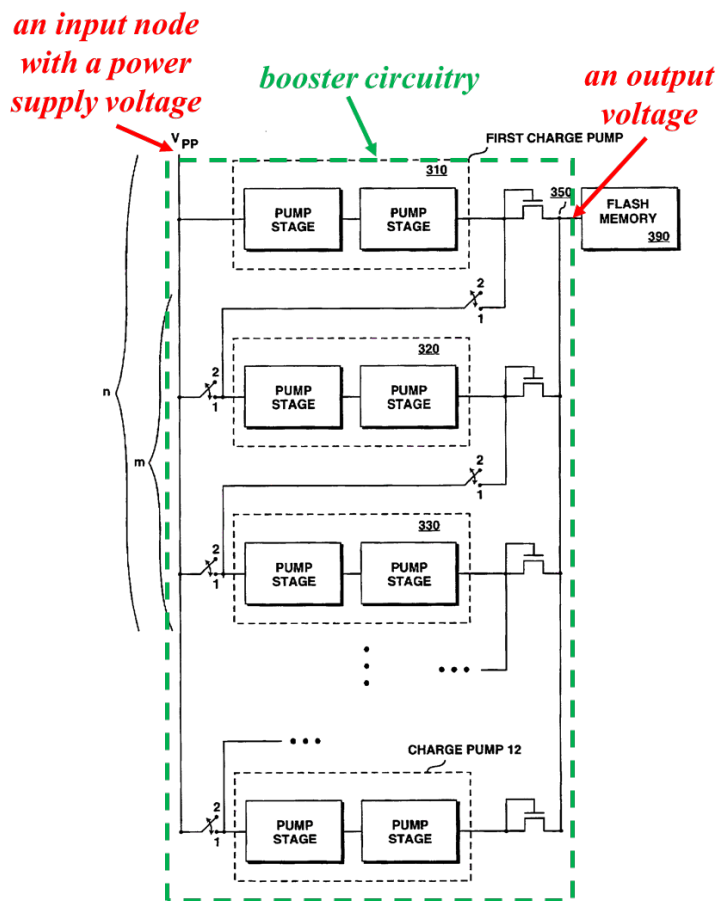


Figure 1
EX1006, Javanifard, FIG. 1, annotated

111. Similarly, as shown in FIG. 3 of Javanifard below, Javanifard describes coupling an input node with a power supply voltage to a booster circuitry comprising

a plurality of booster stages to provide an output voltage, where the variable stage charge pump of the booster circuitry includes 12 rungs and is coupled to a flash memory array 390, “[e]ach rung includes a charge pump having 2 stages.” EX1006, Javanifard, 5:3-6.

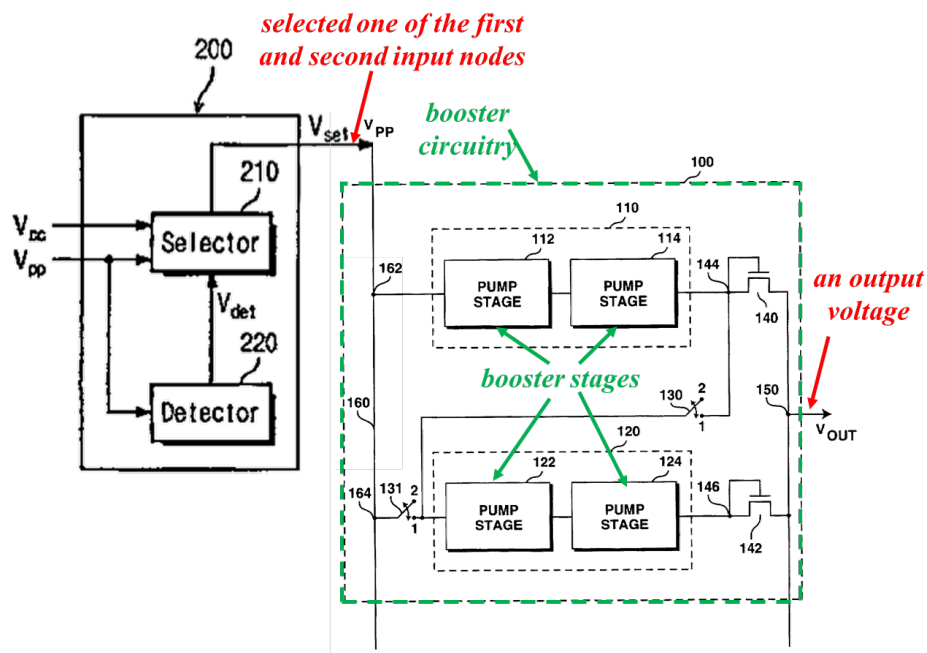


EX1006, Javanifard, FIG. 3, annotated

112. **Third**, a POSITA would have been motivated to apply Javanifard’s teachings of a variable stage charge pump in Zhang’s system, for the benefit of providing a charge pump that can both “accommodate different output levels for a

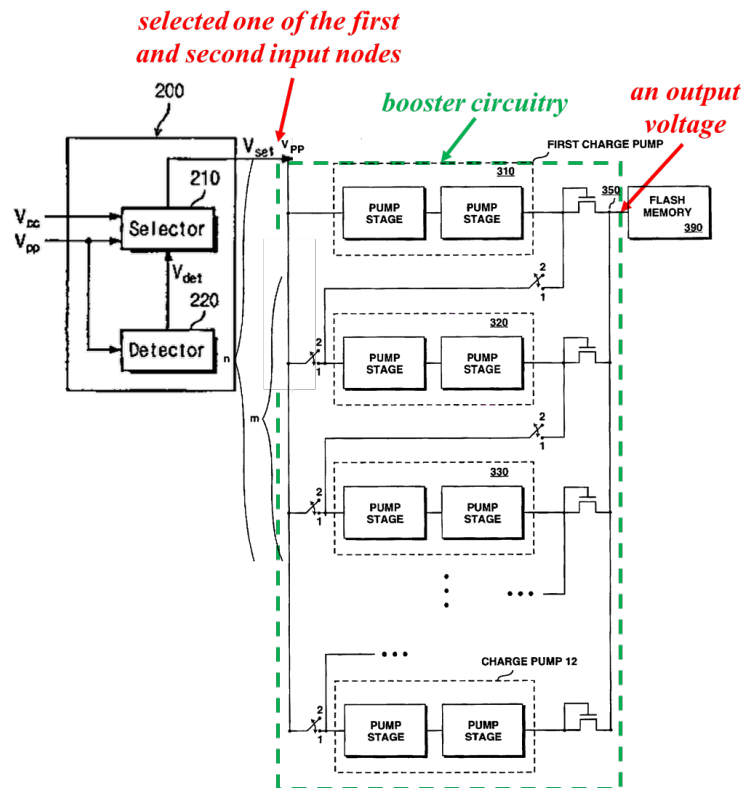
given charge pump power supply input level,” (EX1006, Javanifard, 2:18-20) and “accommodate a given output level for different charge pump power supply input levels.” EX1006, Javanifard, 2:21-24.

113. An example (Example A) of the combination of Zhang and Javanifard is illustrated below, which is a composite figure of selecting circuit block 200 of FIG. 4 of Zhang and variable stage charge pump 100 of FIG. 1 of Javanifard.



Example A of Combination of Zhang and Javanifard

114. Another example (Example B) of the combination of Zhang and Javanifard is illustrated below, which is a composite figure of selecting circuit block 200 of FIG. 4 of Zhang and variable stage charge pump of FIG. 3 of Javanifard.



Example B of Combination of Zhang and Javanifard

115. As shown in Examples A and B, in the combination of Zhang and Javanifard, a selected one of the first and second input nodes (the selected input node of the corresponding supply voltage VCC or VPP) of Zhang is coupled to a variable stage charge pump comprising a plurality of booster stages as taught by Javanifard, to provide an output voltage, to achieve the benefits of a power supply circuit that can both “accommodate different output levels for a given charge pump power supply input level,” (EX1006, Javanifard, 2:18-20) and “accommodate a given output level for different charge pump power supply input levels.” EX1006, Javanifard, 2:21-24.

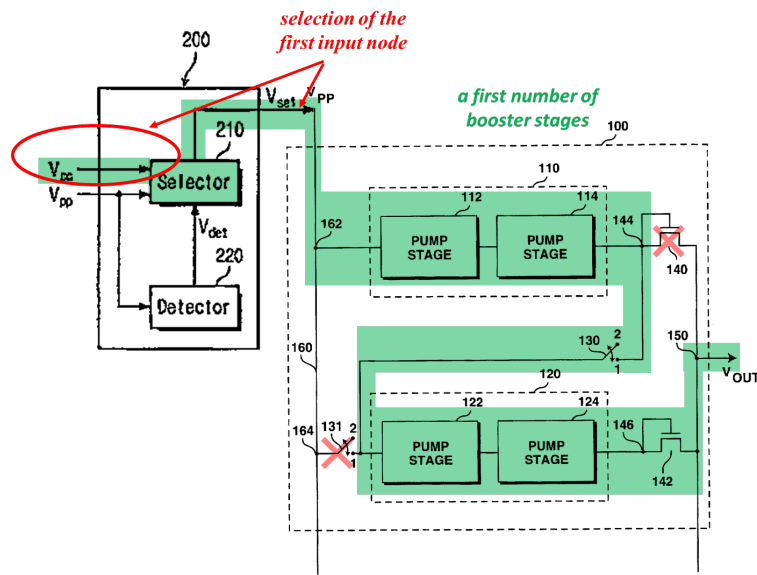
116. Accordingly, Zhang in view of Javanifard renders obvious “*coupling a selected one of the first and second input nodes to booster circuitry comprising a plurality of booster stages to provide an output voltage*” as claimed.

[1.2.2] wherein selection of the first input node corresponds to a first number of booster stages and

117. Zhang in view of Javanifard renders obvious that selection of the first input node corresponds to a first number of booster stages.

118. **First**, as discussed at [1.2.1], it would have been obvious to combine Zhang’s teaching of a selecting circuit block and Javanifard’s teaching of a variable stage charge pump, such that a selected one of the first node and second input node is coupled to a booster circuitry comprising a plurality of booster stages to provide an output voltage.

119. **Second**, as shown in the annotated figure for Example A of Zhang combined with Javanifard below, it would have been obvious that in the combination of Zhang and Javanifard, selection of the first input node (with a lower input power supply voltage level) corresponds to a first number (a higher number e.g., 4) of booster stages, e.g., for generating the same output voltage as the selection of the second input node with a higher input power voltage level.



Example A of Zhang Combined with Javanifard

(Selection of the First Input Node with Lower Supply Voltage)

120. Javanifard describes providing a variable stage charge pump to “accommodate a **given** output level for **different** charge pump power supply input levels.” EX1006, Javanifard, 2:22-24; *see also* EX1005, Zhang, FIG. 8 (providing the same output voltage level for different power supply input levels). Specifically, to “accommodate a **given** output level” (EX1006, Javanifard, 2:22-24) for the first input node with a lower power supply voltage, a POSITA would have configured the variable stage charge pump of FIG. 1 of Javanifard according to row 3 of Table 1 below, because row 3 of Table 1 provides a first (higher) number of serially connected booster stages to provide a higher voltage boost (e.g., by serially connecting charge pumps 110 and 120), compared to row 1 of Table 1 (by providing

only charge pump 110 in operation and thereby having a lower number of serially connected booster stages). Connecting more stages in series provide a higher voltage boost compared to using a smaller number of stages in series, as each stage in the charge pump contributes to increasing the voltage level, and the total voltage boost is the cumulative effect of all the stages.

TABLE 1

Switch 130	Switch 131	Charge Pump 110	Charge Pump 120	
OFF	OFF	ON	OFF	<i>a second number of booster stages, the second number being less than first number</i>
OFF	ON	ON	parallel-coupled to charge pump 110	
ON	OFF	ON	series-coupled to charge pump 110	<i>a first number of booster stages</i>
ON	ON	N/A	N/A	

EX1006, Javanifard, Table 1, annotated

121. Corresponding to row 3 of Table 1, Javanifard explains that “[i]f switch 130 is on and switch 131 is off, charge pump 120 will be coupled so that charge pumps 110 and 120 are series-coupled. In other words, the input voltage for charge pump 120 will be provided from the output of charge pump 110. Because both 110 and 120 are two stage charge pumps, this means that charge pump 100 will **effectively be a four stage charge pump with all four stages serially coupled.**” EX1006, Javanifard, 3:54-60; compare with row 1 of Table 1 (“this configuration of switches 130 and 131 will effectively result **in a two stage charge pump,**” and this

configuration “might be used in a power saving mode” compared with row 2 of Table 1). EX1006, Javanifard, 3:35-40.

122. Javanifard describes that “[i]n this configuration [of row 3 of Table 1], charge pump 100 will provide approximately twice the output voltage at node 150 as the previous two cases [including row 1 of Table 1].” EX1006, Javanifard, 3:60-63. A POSITA would have understood that this statement of “approximately twice the output voltage at node 150” applies when the input voltage levels are the same, and in a design to accommodate “a **given output level for different** charge pump power supply input levels,” the configuration of row 3 with more serially-connected stages provides more voltage boost for a lower power supply input level.

123. Similar analysis applies to Example B of the combination of Zhang and Javanifard. While the example of FIG. 1 and Table 1 of Javanifard provides a “X=2/Y=2 stage pump,” in the combination of Zhang and Javanifard, it would have been obvious to a POSITA to use various suitable X, Y, and pump stage designs to provide the required output voltage according to the different power supply input levels.

124. Accordingly, Zhang in view of Javanifard renders obvious “*wherein selection of the first input node corresponds to a first number of booster stages*” as claimed.

[1.2.3] selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number; and

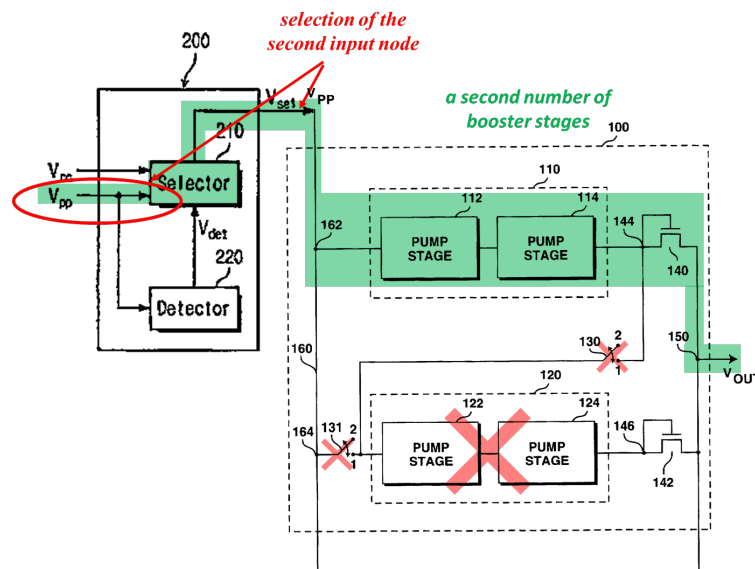
125. Zhang in view of Javanifard renders obvious that selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number.

126. **First**, as discussed at [1.2.1] and [1.2.2], it would have been obvious that in the combination of Zhang and Javanifard, selection of the first input node (with a lower input power supply voltage level) corresponds to a first number (a higher number, e.g., 4) of booster stages, e.g., for generating the same output voltage as the selection of the second input node with a higher input power voltage level.

127. **Second**, for the similar reasons as discussed at [1.2.2], as shown in the annotated figure for Example A of Zhang combined with Javanifard below, it would have been obvious that in the combination of Zhang and Javanifard, selection of the second input node (with a higher input power supply voltage level) corresponds to a second number (a lower number, e.g., 2) of booster stages, e.g., for generating the same output voltage as the selection of the first input node with a lower input power voltage level.

128. Javanifard describes providing a variable stage charge pump to “accommodate a **given** output level for **different** charge pump power supply input levels.” EX1006, Javanifard, 2:22-24; *see also* EX1005, Zhang, FIG. 8 (providing

the same output voltage level for different power supply input levels). Specifically, to “accommodate a **given output level**” (EX1006, Javanifard, 2:22-24) for the second input node with a higher power supply voltage, a POSITA would have configured the variable stage charge pump of FIG. 1 of Javanifard according to row 1 of Table 1 below, because row 1 of Table 1 provides a second (lower) number of serially connected booster stages to provide a lower voltage boost (by providing only charge pump 110 in operation and thereby having a lower number of serially connected booster stages). Connecting less stages in series provide a lower voltage boost compared to using a higher number of stages in series, as each stage in the charge pump contributes to increasing the voltage level, and the total voltage boost is the cumulative effect of all the stages.



Example A of Zhang Combined with Javanifard

(Selection of Second Input Node with Higher Supply Voltage)

TABLE 1

Switch 130	Switch 131	Charge Pump 110	Charge Pump 120	
OFF	OFF	ON	OFF	<i>a second number of booster stages, the second number being less than first number</i>
OFF	ON	ON	parallel-coupled to charge pump 110	
ON	OFF	ON	series-coupled to charge pump 110	<i>a first number of booster stages</i>
ON	ON	N/A	N/A	

EX1006, Javanifard, Table 1, annotated

129. Additionally, while configurations of rows 1 and 2 of Table 1 may provide substantially the same voltage boost, a POSITA would have used row 1 based on a design need for power saving mode. EX1006, Javanifard, 3:39-42 (“This configuration [of row 1] might be used in a power saving mode if charge pump 100 is otherwise providing sufficient current and voltage output levels.”).

130. Similar analysis applies to Example B of the combination of Zhang and Javanifard. While the example of FIG. 1 and Table 1 of Javanifard provides a “X=2/Y=2 stage pump,” in the combination of Zhang and Javanifard, it would have been obvious to a POSITA to use various suitable X, Y, and pump stage designs to provide the required output voltage according to the different power supply input levels.

131. Accordingly, Zhang in view of Javanifard renders obvious “*selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number*” as claimed.

[1.3] changing the booster circuitry from the first number of booster stages corresponding to selection of the first input node to the second number of booster stages when the second input node is selected.

132. Zhang in view of Javanifard renders obvious changing the booster circuitry from the first number of booster stages corresponding to selection of the first input node to the second number of booster stages when the second input node is selected.

133. **First**, as discussed at Ground 1: [1.2.2] and [1.2.3], in the combination of Zhang and Javanifard, selection of the first input node corresponds to a first number of booster stages, and selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number, e.g., to provide the same output voltage for different power supply voltage levels.

134. **Second**, Javanifard describes changing the booster circuitry from a higher number (e.g., 4) of booster stages corresponding to a lower power supply voltage to a lower number (e.g., 2) of booster stages when the power supply voltage is higher. EX1006, Javanifard, 1:8-11 (“providing a charge pump having a variable number as opposed to a fixed number of stages **according to charge pump power**”

supply input levels and desired charge pump output levels”); EX1006, Javanifard, 5:65-66 (“The control for the switches would be a function of the available power supply voltage, VPP, and the desired variable stage charge pump output voltage.”). Specifically, as shown in Table 1 below, the number of the booster stages of the booster circuitry is changed (e.g., reduced from 4 to 2) by changing switch 130 from on (row 3) to off (row 1) to provide the same output voltage level, when the charge pump power supply input level increases.

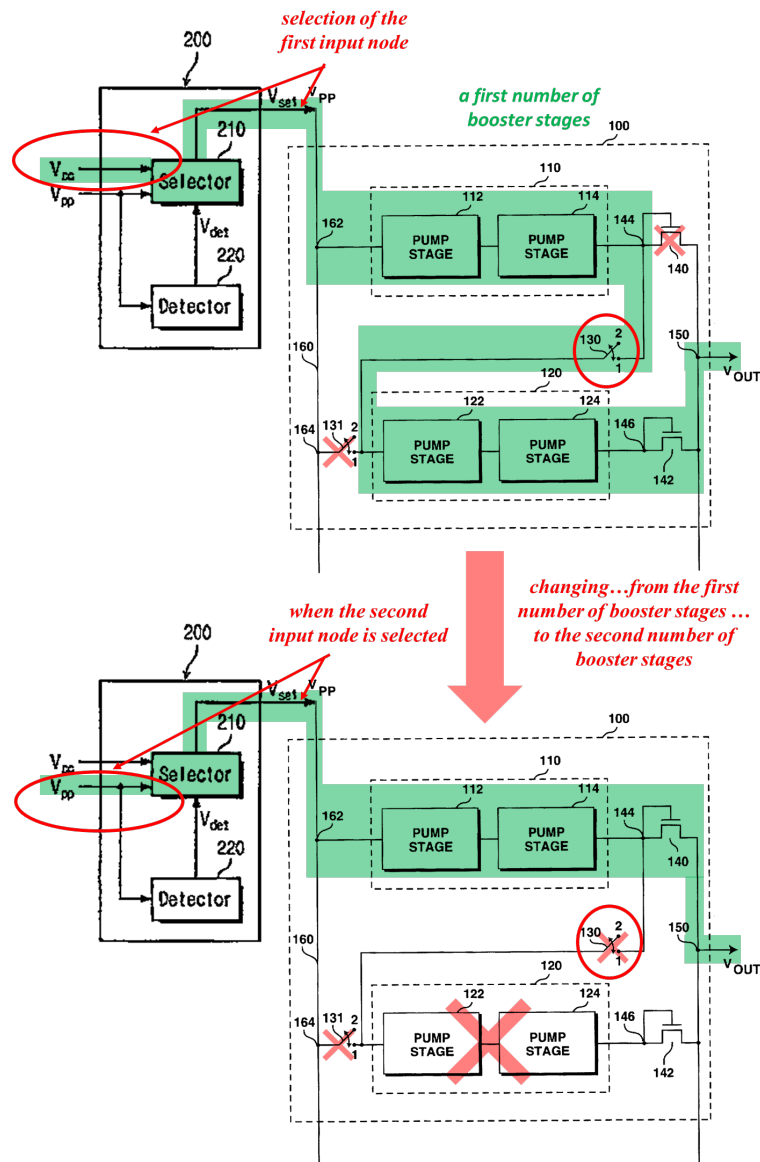
TABLE 1			
Switch 130	Switch 131	Charge Pump 110	Charge Pump 120
OFF	OFF	ON	OFF
OFF	ON	ON	parallel-coupled to charge pump 110
ON	OFF	ON	series-coupled to charge pump 110
ON	ON	N/A	N/A

a second number of booster stages, the second number being less than first number

a first number of booster stages

EX1006, Javanifard, Table 1, annotated

135. As shown in the figure of Example A of Zhang combined with Javanifard below, in the combination of Zhang and Javanifard, when the selection of the input node is changed to the higher power supply voltage, the booster circuitry is changed from the first number of booster stages (e.g., 4) to the second number of booster stages (e.g., 2), by turning off switch 130.



Example A of Zhang Combined with Javanifard
(Changing Booster Circuitry with Switch 130)

136. Similar analysis applies to Example B of the combination of Zhang and Javanifard. While the example of FIG. 1 and Table 1 of Javanifard provides a “X=2/Y=2 stage pump,” in the combination of Zhang and Javanifard, it would have

been obvious to a POSITA to use various suitable X, Y, and pump stage designs to provide the required output voltage according to the different power supply input levels.

137. Accordingly, Zhang in view of Javanifard renders obvious “*changing the booster circuitry from the first number of booster stages corresponding to selection of the first input node to the second number of booster stages when the second input node is selected*” as claimed.

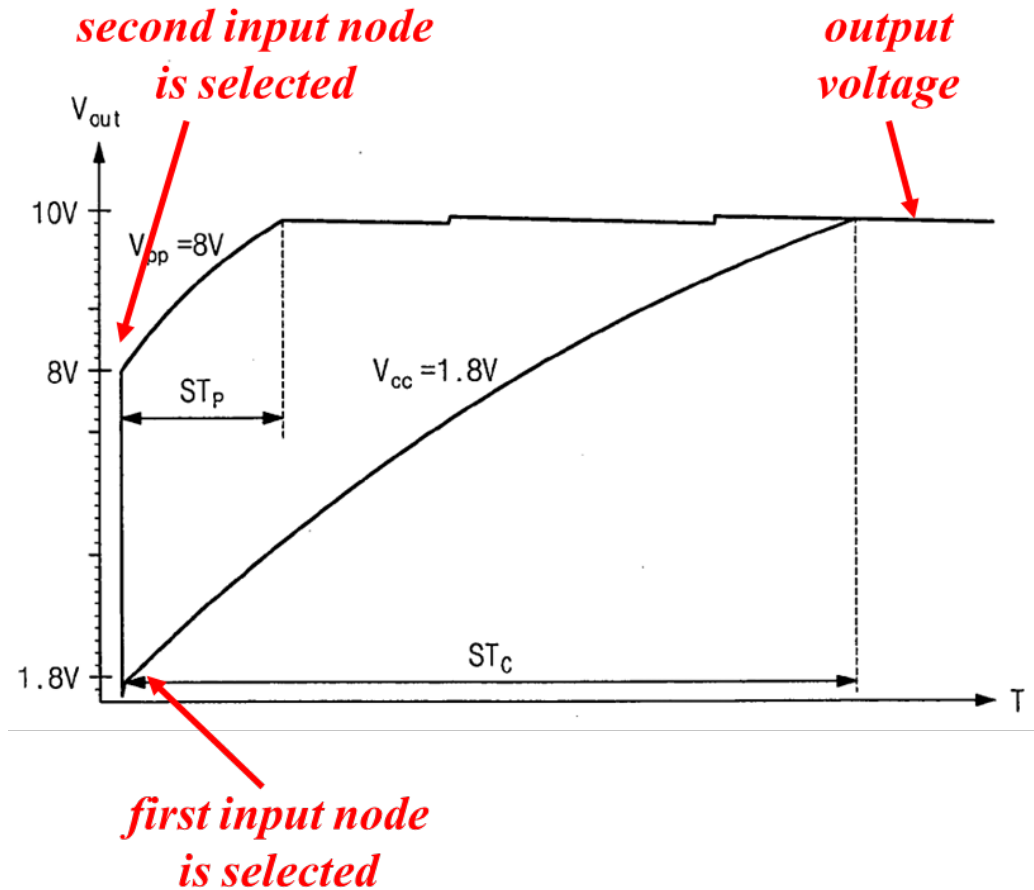
3. Claim 2 would have been obvious over Zhang and Javanifard

[2.0] 2. The method as claimed in claim 1, wherein the output voltage is the same when the first input node is selected and when the second input node is selected.

138. Zhang in view of Javanifard renders obvious that the output voltage is the same when the first input node is selected and when the second input node is selected.

139. **First**, as shown in FIG. 8 below, Zhang describes that the output voltage (e.g., $V_{out} = 10V$) is the same when the first input node (e.g., $V_{CC} = 1.8V$) is selected and when the second input node (e.g., $V_{PP} = 8V$) is selected.

Fig. 8



EX1005, Zhang, FIG. 8, annotated

140. **Second**, similarly, Javanifard teaches this element. Javanifard describes using its variable charge pump to “accommodate a **given output level for different charge pump power supply input levels.**” EX1006, Javanifard, 2:21-24; EX1006, Javanifard, 1:8-11 (“providing a charge pump having a variable number as opposed to a fixed number of stages **according to** charge pump power supply input levels and desired charge pump output levels”); EX1006, Javanifard, 5:61-65 (“the

designer can provide a control to the switches that will switch stages in and out, or change the coupling of the stages to ensure the appropriate output voltage from the variable stage charge pump regardless of the input voltage.”).

141. As such, in the combination of Zhang and Javanifard, a given output level is provided for different charge pump power supply input levels, e.g., by changing the configuration of the variable stage charge pump based on the required output level and the different charge pump power supply levels. Specifically, the output voltage is the same when the first input node is selected (e.g., with a lower input power supply voltage corresponding to a higher number of pump stages) and when the second input node is selected (e.g., with a higher input power supply voltage corresponding to a lower number of power stages).

142. Accordingly, Zhang in view of Javanifard renders obvious that “*the output voltage is the same when the first input node is selected and when the second input node is selected*” as claimed.

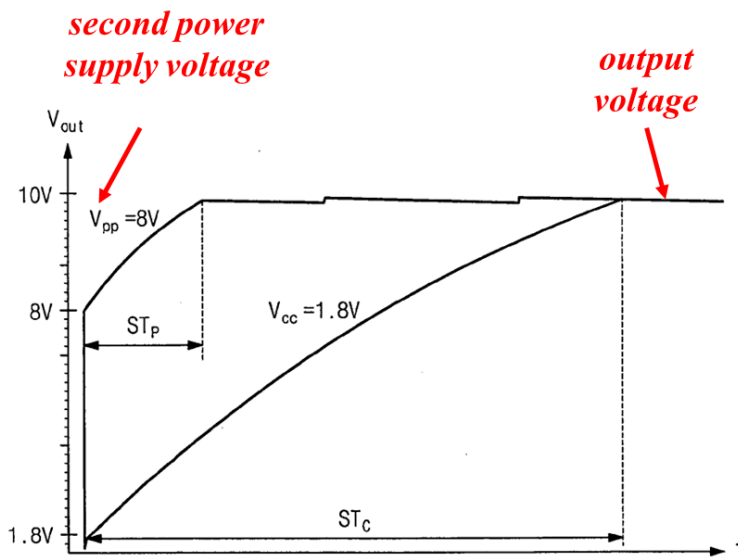
4. Claim 3 would have been obvious over Zhang and Javanifard.

[3.0] 3. The method as claimed in claim 1, wherein the output voltage is higher than the second power supply voltage.

143. Zhang in view of Javanifard renders obvious that the output voltage is higher than the second power supply voltage.

144. Each of Zhang and Javanifard teaches this element, because each describes that the output voltage is greater than each of its voltage power supplies, including both the first and second power supply voltages. *See, e.g.*, EX1005, Zhang, annotated FIG. 8 below (illustrating that the charge pump circuit generates an output voltage (e.g., $V_{out} = 10V$) that is higher than the second power supply voltage V_{PP} (e.g., $V_{PP} = 8V$); *see also* EX1008, Pan, 43 (“Charge pumps are circuits that generate a voltage level higher than the chip supply voltage from which they operate.”)).

Fig. 8



EX1005, Zhang, FIG. 8, annotated

145. Similarly, Javanifard teaches this element. Specifically, Javanifard describes that the output voltage is greater than each of its voltage power supplies, including both the first and second power supply voltages. EX1006, Javanifard,

1:20-30 (“Many operations, however, require voltages greater than that provided by **the lower voltage power supplies**. ... Charge pump technology permits the generation of voltages having a magnitude **greater than** that of the power supply.”).

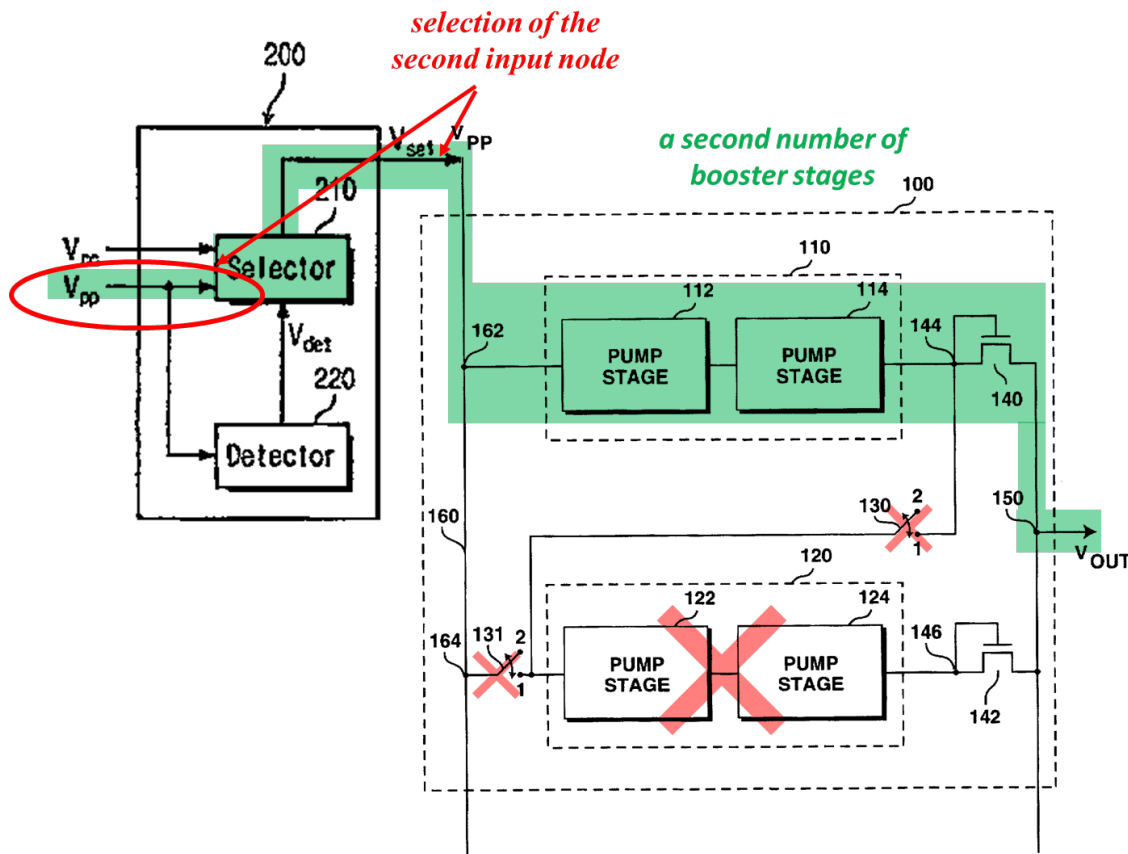
146. Accordingly, in the combination of Zhang and Javanifard, the charge pump system provides an output voltage higher than the input power supply voltage, including both the second power supply voltage and the first power supply voltage, which renders obvious “*wherein the output voltage is higher than the second power supply voltage*” as claimed.

5. Claim 4 would have been obvious over Zhang and Javanifard.

[4.0] 4. The method as claimed in claim 1, wherein the second number of booster stages is one.

147. Zhang in view of Javanifard renders obvious that the second number of booster stages is one.

148. **First**, as discussed above at Ground 1: [1.2.2] and [1.2.3] and as shown in the figure of Example A below, in the combination of Zhang and Javanifard, selection of the second input node supplied with the higher power supply voltage corresponds to selection of a second/lower number of booster stages.



Example A of Zhang Combined with Javanifard

(Selection of Second Input Node with Higher Supply Voltage)

149. **Second**, Javanifard describes that the variable stage charge pump may be configured as an “X/Y stage pump,” where “the ‘X’ refers to the number of rungs (and therefore the maximum number of fixed stage charge pumps) that may be coupled in series. The ‘Y’ indicates the number of stages for each fixed stage charge pump.”). EX1006, Javanifard, 2:59-64.

150. It would have been obvious to a POSITA to implement Y (the number of stages for each fixed stage charge pump) with any suitable numbers including one

(1) based on the design needs. Various suitable pump stage designs (e.g., voltage doubler or other designs of pump stages) to be used to implement the pump stage in a single-stage charge pump system were well-known. *See, e.g.*, EX1008, Pan, FIG. 3-2, 43-44 (describing voltage doubler circuits as a charge pump stage); EX1015, Al-Shamma, FIGS. 1, 2, 4:61-5:59 (describing a charge pump stage design utilizing a pair of cross-coupled charge transfer switch devices); EX1016, Daga, FIGS. 2A-2B (describing a single-stage charge pump), 4 (describing an N-stage charge pump using cascading basic stages of FIG. 2B). As such, in combination of Zhang and Javanifard, it would have been obvious to implement the fixed stage charge pump 110 with a single pump stage. In such implementation, when the second input node with the higher power supply voltage is selected, the selected charge pump 110 has one (1) booster stage.

151. Accordingly, Zhang in view of Javanifard renders obvious that “*the second number of booster stages is one*” as claimed.

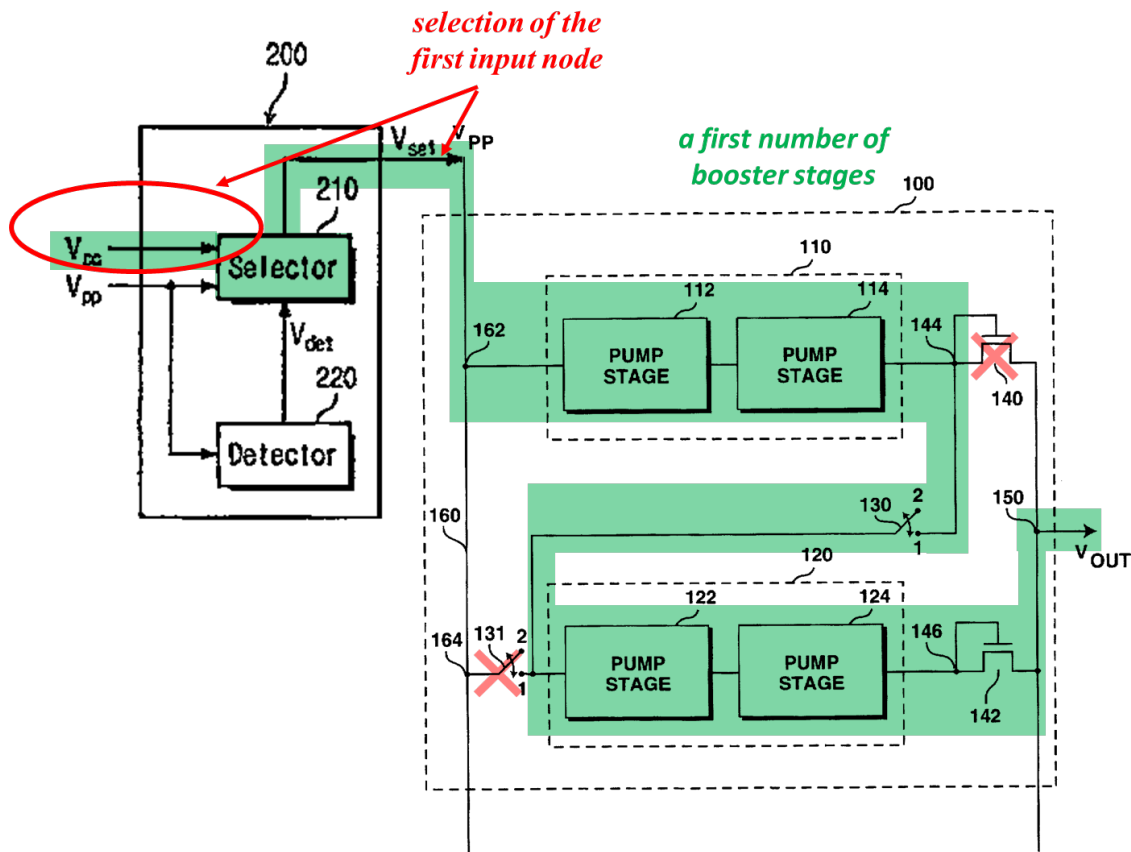
6. Claim 5 would have been obvious over Zhang and Javanifard.

[5.0] 5. The method as claimed in claim 4, wherein the first number of booster stages is two.

152. Zhang in view of Javanifard renders obvious this element.

153. **First**, as discussed at Ground 1: [1.2.2], [1.2.3], and as shown in the figure of Example A below, in the combination of Zhang and Javanifard, selection

of the first input node supplied with the lower power supply voltage corresponds to selection of a first/higher number of booster stages, which is the combined booster stages of charge pumps 110 and 120.



Example A of Zhang Combined with Javanifard

(Selection of First Input Node with Lower Power Supply Voltage)

154. **Second**, as discussed above at Ground 1:[4.0], it would have been obvious that in the combination of Zhang and Javanifard, the “X/Y stage pump” variable stage charge pump is implemented such that Y (the number of stages for each fixed stage charge pump) is one (1) based on the design needs, and as such,

each of the fixed stage charge pump (e.g., charge pumps 110 and 120) is implemented with a single pump stage. *See, e.g.*, EX1008, Pan, FIG. 3-2, 43-44; EX1015, Al-Shamma, FIGS. 1, 2, 4:61-5:59; EX1016, Daga, FIGS. 2A-2B (describing a single-stage charge pump), 4 (describing an N-stage charge pump using cascading basic stages of FIG. 2B).

155. As such, in combination of Zhang and Javanifard, it would have been obvious to implement each of the fixed stage charge pumps 110 and 120 with a single pump stage. In such implementation, when the first input node with the lower power supply voltage is selected, the booster circuitry 100 (where charge pumps 110 and 120 are connected serially) has two booster stages, one booster stage from each of the charge pumps 110 and 120.

156. Accordingly, Zhang in view of Javanifard renders obvious “*wherein the first number of booster stages is two*” as claimed.

7. Claim 6 would have been obvious over Zhang and Javanifard.

[6.0] 6. The method as claimed in claim 1, wherein the booster circuitry is changed between the first number of booster stages and the second number of booster stages with a switch.

157. Zhang in view of Javanifard renders obvious this element.

158. Javanifard teaches this element. As discussed at Ground 1:[1.3] and the annotated figures below, Javanifard teaches that the booster circuitry is changed

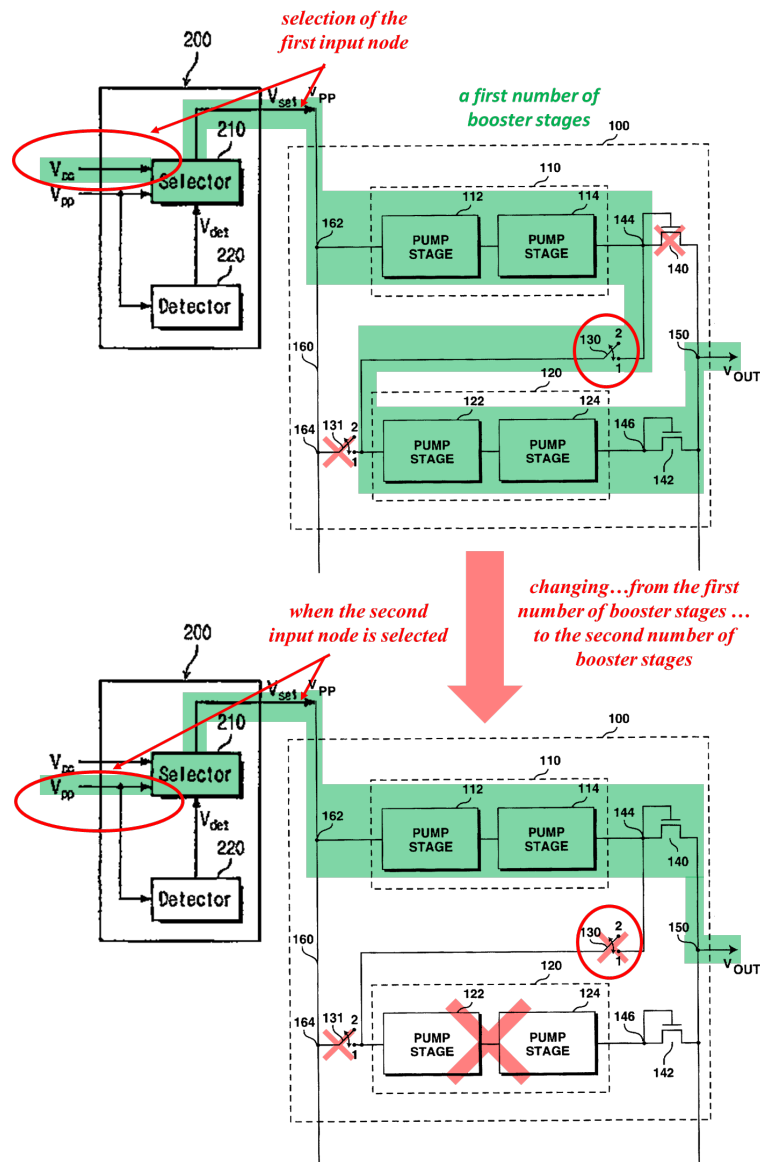
between the first/higher number of booster stages (e.g., 4) and the second/lower number (e.g., 2) of booster stages, using a switch 130.

booster circuitry is changed...with a switch

TABLE 1

Switch 130	Switch 131	Charge Pump 110	Charge Pump 120	
OFF	OFF	ON	OFF	<i>a second number of booster stages, the second number being less than first number</i>
OFF	ON	ON	parallel-coupled to charge pump 110	
ON	OFF	ON	series-coupled to charge pump 110	<i>a first number of booster stages</i>
ON	ON	N/A	N/A	

EX1006, Javanifard, Table 1, annotated



Example A of Combination of Zhang and Javanifard

(Changing Booster Circuitry with Switch 130)

159. Accordingly, as shown in Example A of the combination of Zhang in view of Javanifard, the booster circuitry 100 is changed between different number of stages using switch 130, which renders obvious this element. Zhang in view of

Javanifard renders obvious “*wherein the booster circuitry is changed between the first number of booster stages and the second number of booster stages with a switch*” as claimed.

8. Claim 7 would have been obvious over Zhang and Javanifard.

[7.0] 7. The method as claimed in claim 1, wherein the booster circuitry is changed with a selected one of a metal option, a bonding option, and a fuse option.

160. Zhang in view of Javanifard renders obvious that the booster circuitry is changed with a selected one of a metal option, a bonding option, and a fuse option.

161. Javanifard teaches the element. As discussed at Ground 1:[6.0], Javanifard teaches that the booster circuitry is changed between different configurations (corresponding to different number of booster stages), e.g., by using a switch (e.g., switch 130). EX1006, Javanifard, 5:61-65.

162. Since Javanifard describes changing its booster circuitry between different configurations, a POSITA would know of three techniques to do so: using a bonding option, a metal option, or a fuse option. EX1023, Kim, 1:15-18 (“IC products of a semiconductor use **an option operating method in order to change an operational mode** of a device, product or system. This conventional method is divided into **a bonding option, a metal option or a fuse option.**”); EX1018, Lee, 1:64-65 (“Conventional techniques for option transaction include **bonding option, metal option, and fuse option.**”). These known techniques for allowing a

device maker to make changes, or options, for a device are fundamental to a POSITA, are used in the same known way, and are thus obvious. In so doing, this allows the device maker to make a one-time change during the manufacture or assembly of the device to provide products of different specifications, all from the same die design. For example, based on the needs of an end user, the device maker may use one of a bonding option, a metal option or a fuse option to configure devices of the same die design to provide (1) products that support both VCC and VPP supply lines, with the booster circuitry re-configurable using a control circuit, (2) products that support only the VCC supply line, with the booster circuitry configured based on VCC supply line; or (3) products that support only the VPP supply line, with the booster circuitry configured based on the VPP supply line. Thus, a POSITA would be well aware, as part of his/her basic knowledge of providing an “option” for the device to be modified as needed, using any of the three claimed techniques. *See also* EX1001, '701 patent, 3:17-19 (simply describing the general use of such well-known fundamental techniques that “in the supply voltage generating circuit of the present invention, the switch circuit group is controlled by any of a metal option, fuse option and bonding option.”).

163. A POSITA would have been motivated to, in the multi-power-source charge pump design, include the option operating design to change the booster circuitry, because it provides a manufacturer the flexibility to provide products with

different specifications by configuring dies with the same multi-power-source charge pump design (e.g., during fabrication, packaging, or post-packaging process). A POSITA would have selected one of these well-known fundamental bonding, metal, and fuse options based on the design needs (e.g., functionality, flexibility, cost considerations, process stage for configuration). *See, e.g.*, EX1021, Hwang, 1:27-31 (“The provision of bonding option architecture in ICs has the benefits of increasing the testability, lowering the costs, expanding the functionality, and adding extra values for the IC products.”); EX1022, Muff, [0014] (describing using metal options to form simple switches); EX1023, Kim, 1:15-59 (describing advantages and disadvantages of the fuse option, including the laser cutting fuse option and the electrical cutting fuse option).

164. As such, in the combination of Zhang and Javanifard, a POSITA would have selected one of a bonding option, a metal option, or a fuse option to control the switch (e.g., switch 130) to change the booster circuitry configuration, based on the design needs.

165. Accordingly, Zhang in view of Javanifard renders obvious that “*the booster circuitry is changed with a selected one of a metal option, a bonding option, and a fuse option*” as claimed.

9. Claim 8 would have been obvious over Zhang and Javanifard.

[8.0] 8. The method as claimed in claim 1, wherein the output voltage is a power supply voltage VPP.

166. Zhang in view of Javanifard renders obvious that the output voltage is a power supply voltage VPP.

167. Javanifard teaches this element. Javanifard describes that the output voltage is provided as a power supply voltage to a local circuit, including for example, “various voltage levels required by a flash memory array” for each mode of operation including reading, erasing, programming, and therefore teaches that the output voltage is a power supply voltage VPP. EX1006, Javanifard, 6:5-17.

168. For example, as shown in FIG. 3 of Javanifard below, the output voltage at output node 350 of the variable charge pump is provided as a power supply to a flash memory array 390. *See also* EX1006, Javanifard, 5:56-59 (“Designing the variable stage charge pump with an appropriate number of stages **permits a charge pump circuit that can provide the proper voltages for the memory circuitry** irrespective of the available power supply voltage.”), 6:5-17 (“a variable stage charge pump might be used to provide the **various voltage levels required by a flash memory array**. A flash memory array is made of up memory cells including floating gate field effect transistor devices. These transistors can be programmed by changing the charge stored on a floating gate, and the condition (programmed or

erased) may be detected by interrogating the cells. Different voltage requirements are needed by the flash memory cells for the different operation modes. A variable stage charge pump (or pumps) might provide the appropriate supply voltages for each mode of operation of the flash memory array. These modes include reading, programming, and erasing.”), 8:35-38 (“high current charge pump 220 is needed to provide 5 volts **for the wordlines** (i.e., gates of the flash memory cells) on line 262”).

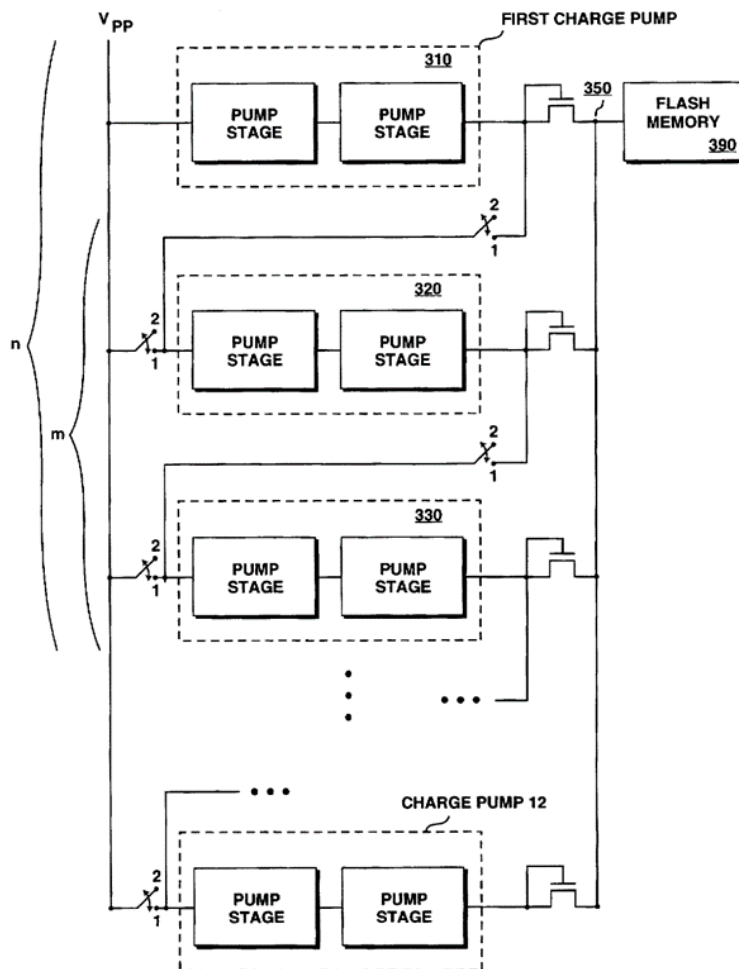


Figure 3

EX1006, Javanifard, FIG. 3

169. It was well-known in the art that the term “VPP” (also referred to as “V_{PP}”) is generally used to refer to power supply voltages to circuits, including for example, a power supply voltage to a charge pump circuit or a power supply voltage to a memory device. For example, in Javanifard, in FIGS. 1 and 3, VPP is used to refer to a power supply voltage provided to common input bus 160, and in FIG. 2, VPP is used to refer to a supplemental voltage provided to a flash memory device where “VPP, is typically needed only when writing or erasing the memory because of the higher voltages needed during those operations.” EX1006, Javanifard, 6: 44-50 (“In one embodiment, power for the flash memory device is provided by two sources. These sources include a VCC line and a VPP line. The VCC line is the primary power source for the flash device. The supplemental voltage provided by supply line, VPP, is typically needed only when writing or erasing the memory because of the higher voltages needed during those operations. In one embodiment, VCC is approximately 5 volts. VPP, however, might be 3.3, 5, or 12 volts.”); EX1006, Javanifard, FIG. 1, 2:52-53 (“A power supply voltage, VPP, provides the supply voltage to common input bus 160.”); 5:66-67 (“The control for the switches would be a function of the available power supply voltage, VPP, and the desired variable stage charge pump output voltage.”); EX1005, Zhang, 3:24-25 (“The voltage VPP refers to a high voltage provided externally during a test operation

mode.”). This general usage of “VPP” referring to a power supply voltage is consistent with the ’701 patent, which describes “**suppl[ying] the boosted voltage** to a local circuit,..., **as power supply VPP**,” and “an example of [local circuit] is a circuit for driving a word line.” EX1001, ’701 patent 4:64-67 (“The booster 20 ... **supplies the boosted voltage to a local circuit**, an example of which is a circuit for driving a word line, **as power supply VPP**.”).

170. To the extent that Patent Owner attempts to assert that the claimed “*power supply voltage VPP*” requires a voltage for driving a word line, such arguments should be rejected, because the ’701 patent only provides the circuit for driving a word line as an example use of VPP. Regardless, Javanifard teaches this element, because Javanifard’s variable stage charge pump provides various power supply voltage levels required by a flash memory device, including the power supply for driving a word line. EX1006, Javanifard, 6:5-17 (“A variable stage charge pump (or pumps) might provide the appropriate supply voltages for each mode of operation of the flash memory array. These modes include reading, programming, and erasing.”), 8:35-38 (“high current charge pump 220 is needed to provide 5 volts **for the wordlines** (i.e., gates of the flash memory cells) on line 262”).

171. Accordingly, Zhang in view of Javanifard renders obvious that “*the output voltage is a power supply voltage VPP*” as claimed.

10.Claim 9 would have been obvious over Zhang in view of Javanifard.

[9.0] 9. The method as claimed in claim 1, wherein the booster circuitry comprises capacitors formed using thin gate oxide transistors.

172. Zhang in view of Javanifard renders obvious this element.

173. **First**, Javanifard teaches this element. Javanifard teaches a variable stage charge pump, and it was well-known that pump stages in the variable stage charge pump include pumping capacitors for storing charges and thereby generating an output voltage higher than the input voltage. *See*, e.g., IV.A.2 (citing EX1014, Frulio, 1:23-34; EX1008, Pan, FIG. 3-2, 43-44; EX1015, Al-Shamma, FIG. 1, 4:61-64; 4:65-5:59; EX1016, Daga, FIGS. 2A-2B, FIG. 4); *see also* EX1005, Zhang, FIG. 5 (illustrating that charge pump parts 120, 130, 140, 150 (pump stages connected in series) include capacitors C120, C130, C140, and C150 respectively); EX1005, Zhang, 3:61-64 (“Each charge pump part 120, 130, 140 and 150 comprises one PMOS transistor, e.g., transistor P120, one capacitor, e.g., capacitor C120, and one high-voltage NMOS transistor, e.g., transistor N120.”).

174. A POSITA would have found it obvious to implement pumping capacitors in the variable stage charge pump of Javanifard in any of a variety of known and suitable ways—using either a thick gate oxide transistor or a thin gate oxide transistor in capacitor configuration (also referred to as a MOS capacitor), and would have been motivated to optimize the booster circuitry/variable stage charge

pump of Javanifard by optimizing the pump capacitor by using a thin gate oxide transistor for the benefit of reduced area. *See, e.g.*, EX1020, Kang, Abstract (“Using the thin-oxide capacitors can reduce the area of charge pumps greatly while keeping their driving capability.”), 258 (“Hence the pumping capacitors are C1, C2, and C3 as shown in Fig. 1(b) can be made with the thin-oxide transistors. By doing so, the layout area of C1, C2, and C3 becomes smaller compared with that of thick-oxide transistors. Because the area of the pumping capacitors takes the largest part of the total pump area, it is very helpful to make the area of the pumping capacitors small for reducing the total pump area.”); EX1019, Narui, 9:51-64 (In a boosted potential generation circuit, “MOS transistor of a thin gate insulating film and low withstand pressure can be used as the capacitor MOS transistor. The capacitor MOS transistor having the thin gate insulating film can realize a large capacitance by a small area, and it is effective for reducing a chip size. For example, use of a MOS transistor having a gate insulating film of a thickness 3.5 nm as the capacitor MOS transistor enables reduction of an area required by the boosted potential generation circuit by about 30% compared with the case of using the MOS transistor constituting the memory cell or the MOS transistor having a gate insulating film of a thickness 6.0 nm used for the transfer MOS transistor as the capacitor MOS transistor.”).

175. The prosecution history of the '701 patent further supports that it would have been obvious to use a thin-oxide capacitor in the booster circuitry. EX1009,

'422 app, 288, 311 (during the prosecution of the parent of the '701 patent, Examiner similarly rejected a claim limitation related to a thickness of the gate oxide film of a capacitor as obvious, explaining that “[w]here the general conditions of the claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. Therefore it would be obvious at the time the invention was made, to a person having ordinary skill in the art to use **optimize the general capacitor** in such a way wherein the gate oxide film is a thickness less than a thickness of a gate oxide film of a MOS transistor in the load.” Applicant did not directly dispute Examiner’s rejection. EX1009, '422 app, 271-273, 298.

176. As such, in the combination of Zhang and Javanifard, a POSITA would have been motivated to implement the pump capacitors in the booster circuitry using thin gate oxide transistors for the benefit of area reduction.

177. Accordingly, Zhang in view of Javanifard renders obvious that “*the booster circuitry comprises capacitors formed using thin gate oxide transistors*” as claimed.

11.Claim 10 would have been obvious over Zhang and Javanifard.

[10.0] 10. A semiconductor device comprising:

178. To the extent that the preamble is limiting, Zhang discloses or renders obvious the preamble.

179. Specifically, Zhang describes a charge pump system implemented on integrated chips, as such, teaches a semiconductor device because an integrated chip includes semiconductor devices on a semiconductor wafer. EX1005, Zhang, 1:63-2:3 (“The conventional charge pump circuit pre-charges the output voltage V_{out} corresponding to the external voltage V_{CC} ... This additional time is undesirable, particularly when testing **integrated chips** that require high voltages quickly.”). Zhang teaches that the charge pump system is a semiconductor device including various circuits (e.g., selector 210) implemented using PMOS and NMOS transistors, which are semiconductor devices using semiconductor materials (e.g., p-type or n-type semiconductors). *See, e.g.*, EX1005, Zhang, 4, 35-40 (“Referring to FIG. 6, the selector 210 uses a level shifter to control the high voltage V_{PP} . The selector 210 comprises **high-voltage NMOS transistors N211 to N218, high-voltage PMOS transistors P211 to P218 and P210 I where $i=1$ to 4**, and two serially connected inverters.”).

180. Accordingly, Zhang discloses or renders obvious “*a semiconductor device*” as claimed.

[10.1] a first input node supplied with a first power supply voltage;

181. Zhang in view of Javanifard renders obvious this element for the reasons discussed at Ground 1:[1.1].

[10.2] a second input node supplied with a second power supply voltage higher than the first power supply voltage;

182. Zhang in view of Javanifard renders obvious this element for the reasons discussed at Ground 1:[1.1].

[10.3] booster circuitry comprising a plurality of booster stages to provide an output voltage; and

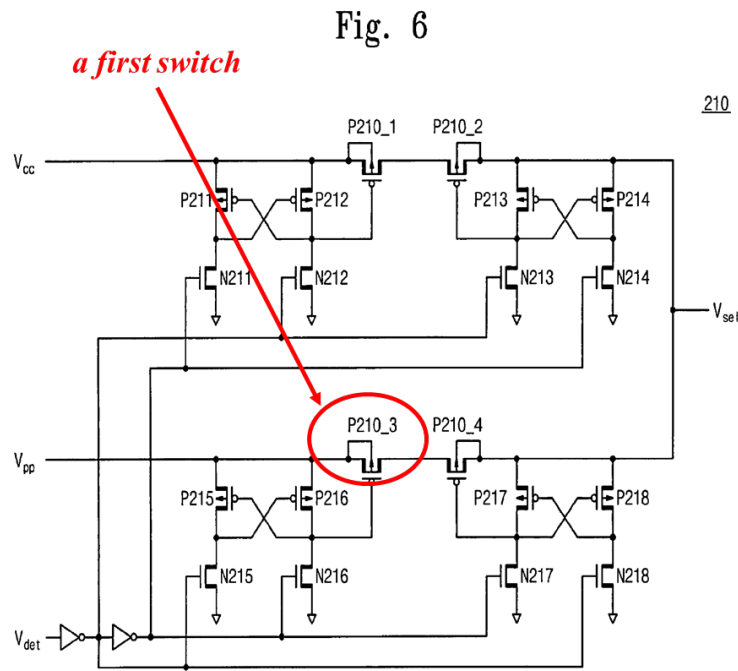
183. Zhang in view of Javanifard renders obvious this element for the reasons discussed at Ground 1:[1.2.1].

[10.4] a first switch configured to couple a selected one of the first input node and the second input node to the booster circuitry,

184. Zhang in view of Javanifard renders obvious this element.

185. **First**, as discussed at Ground 1:[1.2.1]-[1.2.3], in the combination of Zhang and Javanifard, a selected one of the first and second input nodes (e.g., as taught by the selecting circuit block 200 of Zhang) is coupled to booster circuitry (e.g., a variable stage charge pump as taught by Javanifard) comprising a plurality of booster stages to provide an output voltage.

186. **Second**, referring to annotated FIG. 6 of Zhang below, Zhang describes that in selector 210 of the selecting circuit block 200 of the charge pump system, a first switch (P201_1, P210_2, P210_3, P210_4, and/or a combination thereof) is configured to couple a selected one of the first input node and the second input node to the booster circuitry.



EX1005, Zhang, FIG. 6, annotated

187. Specifically, Zhang describes that FIG. 6 is an example of the selector 210 of the selecting circuit block 200 of FIG. 4, and selector 210 uses one or more switches (using PMOS transistors) to select one of V_{CC} and V_{PP} as its output voltage V_{SEL} . EX1005, Zhang, 4:35-51. “The selector 210 comprises high-voltage NMOS transistors N211 to N218, high-voltage PMOS transistors P211 to P218 and P210_I where $i=1$ to 4, and two serially connected inverters. The level shifter selects between the power voltage V_{CC} and the high voltage V_{PP} . For instance, the high-voltage NMOS transistors N216 and N217 turn on in the test operation mode where the detection signal V_{DET} is enabled. The **high-voltage PMOS transistors P210_3 and P210_4 turn on. As a result, V_{SEL} is equal to V_{PP}** . However, since

the high-voltage NMOS transistors N212 and N213 are turned off, the **high-voltage PMOS transistors P210_1 and P210_2 are also turned off**. Accordingly, VSEL is not equal to VCC. To the contrary, VSEL is equal to VCC in general operation mode where the detection signal VDET is disabled.”

188. PMOS transistors are MOSFETs, and Zhang’s use of PMOS transistors to implement switches was consistent with the well-known knowledge in the art. *See, e.g.*, EX1006, Javanifard, 3:13-15 (“switches 130 and 131 are implemented from metal oxide semiconductor field effect transistors (MOSFETs)”).

189. As such, in the combination of Zhang and Javanifard, the selecting circuit block (e.g., as taught by FIGS. 4 and 6 of Zhang) includes a switch configured to couple Vsel to a variable stage charge pump (e.g., as taught by Javanifard). Accordingly, Zhang in view of Javanifard renders obvious “*a first switch configured to couple a selected one of the first input node and the second input node to the booster circuitry*” as claimed.

[10.5] wherein the booster circuitry configured to have a first number of booster stages when the first input node is selected and to be changed to a second number of booster stages when the second input node is selected, the second number being less than the first number.

190. Zhang in view of Javanifard renders obvious this element for the reasons discussed at Ground 1:[1.2.2], [1.2.3], and [1.3].

191. Specifically, Zhang in view of Javanifard renders obvious “*the booster circuitry configured to have a first number of booster stages when the first input node is selected*” for the reasons discussed at Ground 1:[1.2.2], and renders obvious “*to be changed to a second number of booster stages when the second input node is selected, the second number being less than the first number*” for the reasons discussed at Ground 1:[1.2.3] and [1.3].

12.Claim 11 would have been obvious over Zhang and Javanifard.

[11.0] 11. The semiconductor device as claimed in claim 10, wherein the output voltage is the same when the first input node is selected and when the second input node is selected.

192. Zhang in view of Javanifard renders obvious this element for the reasons discussed at Ground 1:[2.0].

13.Claim 12 would have been obvious over Zhang and Javanifard.

[12.0] 12. The semiconductor device as claimed in claim 10, wherein the output voltage is higher than the second power supply voltage.

193. Zhang in view of Javanifard renders obvious this element for the reasons discussed at Ground 1:[3.0].

14.Claim 13 would have been obvious over Zhang and Javanifard.

[13.0] 13. The semiconductor device as claimed in claim 10, wherein the second number of booster stages is one.

194. Zhang in view of Javanifard renders obvious this element for the reasons discussed at Ground 1:[4.0].

15.Claim 14 would have been obvious over Zhang and Javanifard.

[14.0] 14. The semiconductor device as claimed in claim 13, wherein the first number of booster stages is two.

195. Zhang in view of Javanifard renders obvious this element for the reasons discussed at Ground 1:[5.0].

16.Claim 15 would have been obvious over Zhang and Javanifard.

[15.0] 15. The semiconductor device as claimed in claim 10, wherein the booster circuitry is changed from the first number of booster stages and the second number of booster stages with a second switch.

196. Zhang in view of Javanifard renders obvious this element.

197. **First**, as discussed at Ground 1:[10.4], in the combination of Zhang and Javanifard, a first switch in a selecting block circuit is configured to couple a selected one of the first input node and the second input node to the booster circuitry.

198. **Second**, as discussed at Ground 1:[6.0], in the combination of Zhang and Javanifard, a switch (e.g., switch 130) in the variable stage charge pump, which is different from the first switch, is used to change the booster circuitry from the first number of booster stages to the second number of booster stages. The switch (e.g., switch 130) in the variable stage charge pump teaches “*a second switch*” as claimed.

199. Accordingly, Zhang in view of Javanifard renders obvious that “*the booster circuitry is changed from the first number of booster stages and the second number of booster stages with a second switch*” as claimed.

17.Claim 16 would have been obvious over Zhang and Javanifard.

[16.0] 16. The semiconductor device as claimed in claim 10, wherein the booster circuitry is changed with a selected one of a metal option, a bonding option, and a fuse option.

200. Zhang in view of Javanifard renders obvious this element for the reasons discussed at Ground 1:[7.0].

18.Claim 17 would have been obvious over Zhang and Javanifard.

[17.0] 17. The semiconductor device as claimed in claim 10, wherein the output voltage is a power supply voltage VPP.

201. Zhang in view of Javanifard renders obvious this element for the reasons discussed at Ground 1:[8.0].

19.Claim 18 would have been obvious over Zhang and Javanifard.

[18.0] 18. The semiconductor device as claimed in claim 10, wherein the booster circuitry comprises capacitors formed using thin gate oxide transistors.

202. Zhang in view of Javanifard renders obvious this element for the reasons discussed at Ground 1:[9.0].

C. Ground 2: Claims 1-18 are Rendered Obvious under § 103 over Javanifard.

1. Reasons to Combine Embodiments of Javanifard.

203. As discussed above at VIII.A.2, Javanifard describes various embodiments of variable stage charge pumps.

204. Each of Embodiment 1 (described with example of FIG. 1 and Table 1) and Embodiment 3 (described with example of FIG. 3) describes a variable stage

charge pump having a variable number (as opposed to a fixed number) of stages according to charge pump power supply input levels and desired charge pump output levels. The variable stage charge pump may be identified as an “X/Y” stage pump, where “X” refers to the number of rungs that may be coupled in series, and “Y” indicates the number of stages for each fixed stage charge pump. FIG. 1 of Embodiment 1 illustrates a “2/2” stage pump, including two rungs, each rung including a two-stage charge pump. FIG. 3 of Embodiment 3 illustrates a “12/2” stage pump, including twelve rungs, each rung including a two-stage charge pump.

205. Embodiment 2 (described with example of FIG. 2 below and Tables 2 and 3) describes selecting from multiple power sources (e.g., VCC and VPP), and providing the selected power supply source to the variable stage charge pumps (e.g., variable stage charge pumps 210 and 220). EX1006, Javanifard, 6:61-64. Each of the variable stage charge pumps is configured based on the input power supply voltage (e.g., VCC or VPP) to provide required output voltage levels.

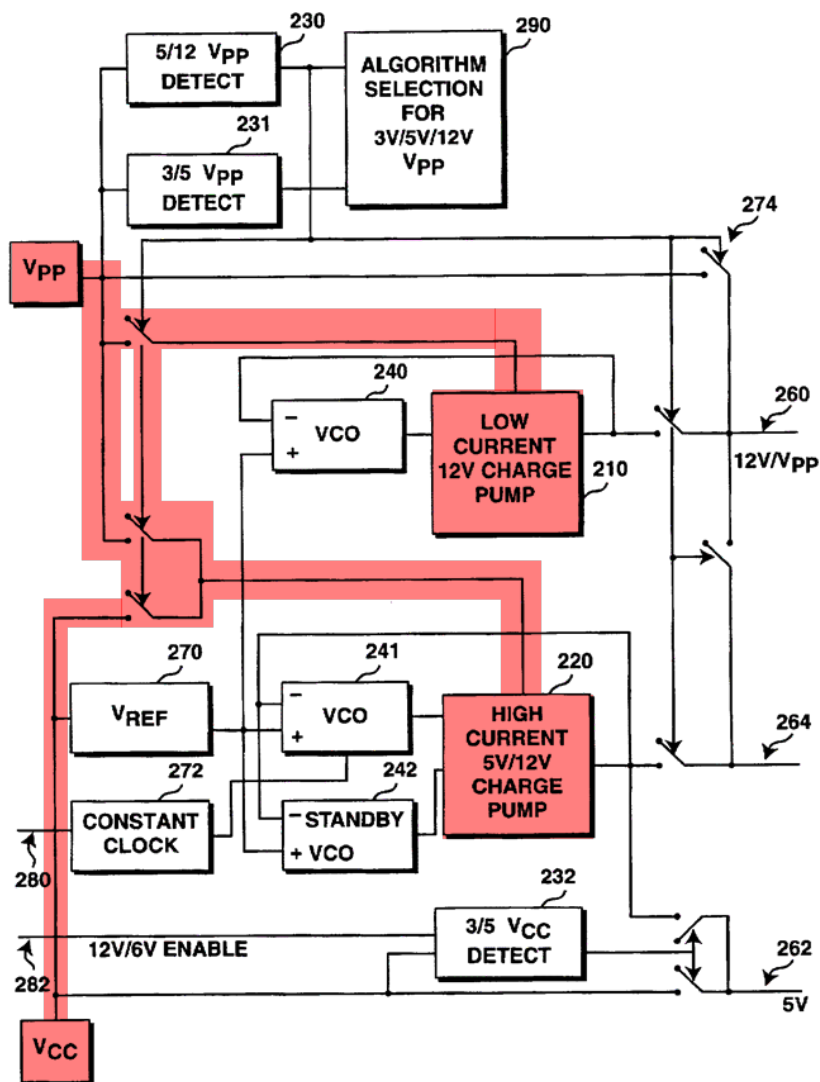


Figure 2

EX1006, Javanifard, FIG. 2, annotated

206. A POSITA would have been motivated to apply Embodiment 2's teachings of a multi-power-source charge pump system that selects from multiple power sources to the variable stage charge pump as taught in Embodiments 1 or 3,

by selecting and supplying the selected power supply source (as taught in Embodiment 2) to the input of the variable stage charge pump, to produce the obvious, beneficial, and predictable results of a multi-power-source variable stage charge pump system that supports multiple power sources, e.g., supporting a device provided by multiple power sources. *See, e.g.*, EX1006, Javanifard, 6:45-46 (describing that “[i]n one embodiment, power for the flash memory device is provided by two sources” including a primary power source VCC line and a supplemental power supply line, VPP) ; *see also* EX1005, Zhang, Abstract, FIG. 4 (describing “a charge pump circuit that operates responsive to a test or general operation mode,” where the operation mode corresponds to a selected voltage from two power sources VCC and VPP).

207. Javanifard explicitly provides motivations to apply its teaching of selection from multiple power sources of Embodiment 2 to the variable stage charge pump of Embodiments 1 or 3, by providing the selected power supply to the variable stage charge pump. For example, one of Javanifard’s objects is to “provide a charge pump that can accommodate a given output level for **different charge pump power supply input levels.**” EX1006, Javanifard, 2:21-23. It was well-known that often different charge pump power supply input levels are provided by different power supply source lines. *See, e.g.*, EX1006, Javanifard, 6:45-46 and EX1005, Zhang, Abstract, FIG. 4. As such, it would have been obvious to apply Embodiment 2’s

teaching of selection from multiple power sources to the variable stage charge pump, to achieve Javanifard's object to "accommodate a given output level for different charge pump power supply input levels." EX1006, Javanifard, 2:21-23.

208. Applying Javanifard's teaching of selection from multiple power sources of Embodiment 2 to the variable stage charge pump of Embodiments 1 or 3 would have been no more than the combination of known elements according to known methods (e.g., incorporating a power source selection design in a variable stage charge pump according to well-known IC design techniques) obvious to a POSITA, which does no more than yield predictable results. Techniques (e.g., voltage detectors and selectors) to select and provide a selected power supply voltage to a charge pump were well-known. *See e.g.* EX1006, Javanifard, FIG. 2 (detectors 230 and 231 and selector 290 used to select and provide the selected power supply voltage to variable stage charge pumps 210 and 220); EX1005, Zhang, FIG. 4 (selecting circuit block 200 used to select and supply the selected power supply voltage to the charge pump block 100).

209. As detailed below, the combination of Javanifard's embodiments renders claims 1-18 of the '701 patent obvious.

2. Claim 1 would have been obvious over Javanifard.

[1.0] 1. A method for generating a supply voltage, comprising:

210. To the extent that the preamble is limiting, Javanifard discloses it or renders it obvious.

211. Specifically, as shown in FIG. 1 of Javanifard below, Javanifard describes a variable stage charge pump generating a supply voltage in integrated circuits for various devices, e.g., to “**provide the proper voltages** for the memory circuitry,” which can both accommodate “**a given output level** for different charge pump power supply input levels” and “**different output levels** for a given charge pump power supply input level.” EX1006, Javanifard, FIG. 1, 5:18-24; 6:56-59; *see also* EX1006, Javanifard, FIGS. 2, 3 (each illustrating that a supply voltage is generated for a memory device).

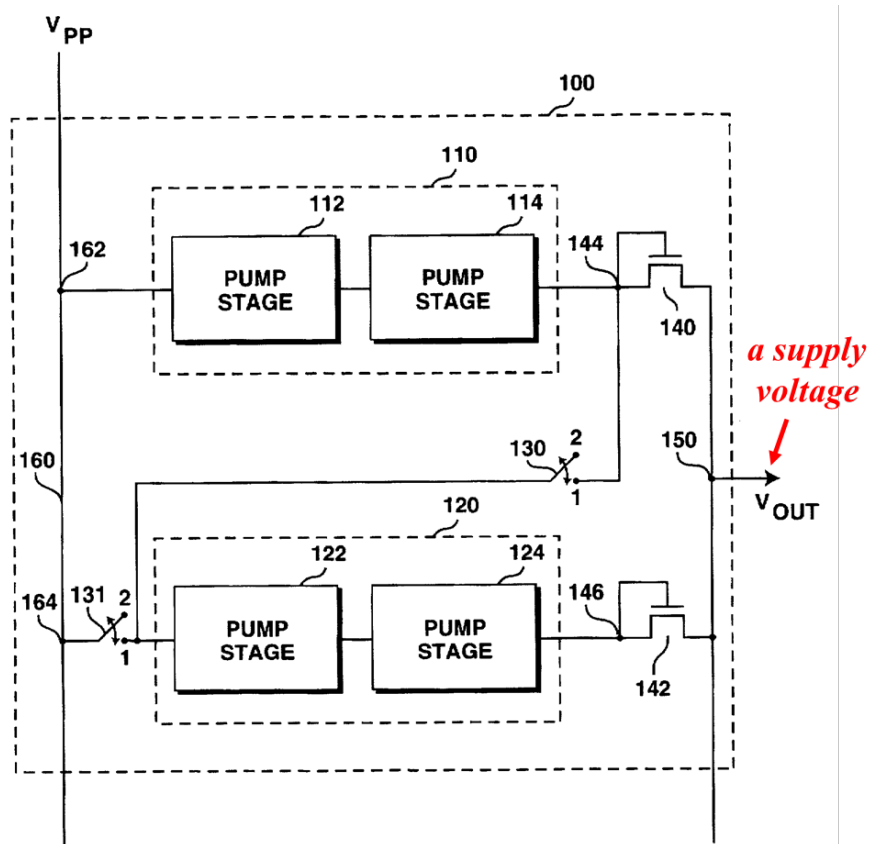


Figure 1

EX1006, Javanifard, FIG. 1, annotated

212. Accordingly, Javanifard discloses or renders obvious “[a] method for generating a supply voltage” as claimed.

[1.1] selecting one of a first input node supplied with a first power supply voltage and a second input node supplied with a second power supply voltage that is higher than the first power supply voltage;

213. Javanifard discloses or at least renders obvious this element.

214. **First**, as discussed at Ground 1:[1.1], Javanifard describes coupling an input node with a power supply voltage to a booster circuitry comprising a plurality of booster stages to provide an output voltage, as shown in annotated FIG. 1 (Embodiment 1) and FIG. 3 (Embodiment 3) of Javanifard and below.

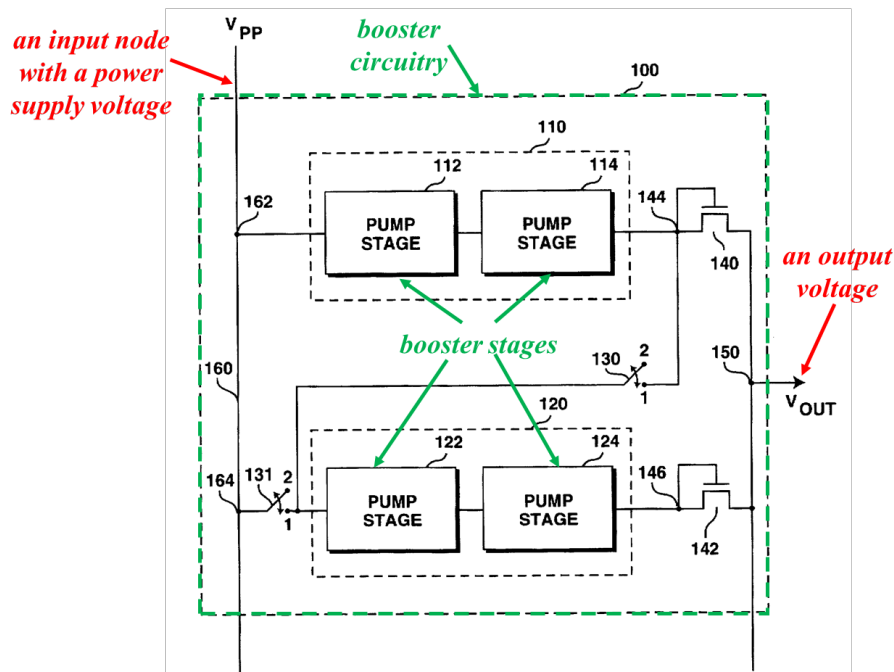


Figure 1

EX1006, Javanifard, FIG. 1, annotated

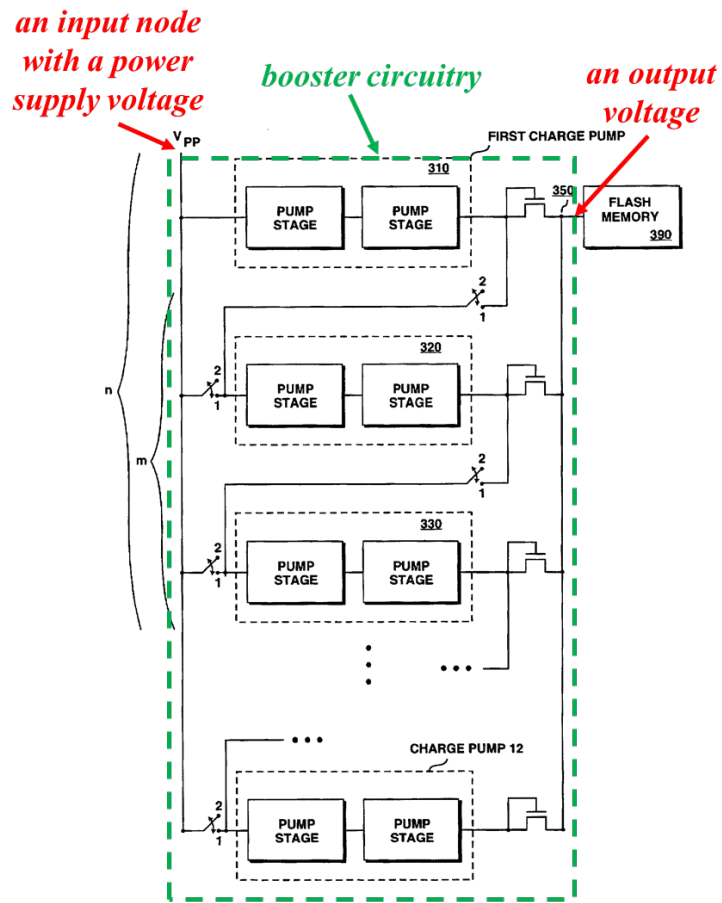


Figure 3

EX1006, Javanifard, FIG. 3, annotated

215. **Second**, as shown in FIG. 2 below, Javanifard describes an input power supply selector (including one or more switches) for selecting from a first input node supplied with a first power supply voltage (e.g., VCC) and a second input node supplied with a second power supply voltage (e.g., VPP), where VPP (e.g., VPP = 5 volts) is higher than VCC (e.g., VCC = 3.3 volts). EX1006, Javanifard, 6:61-64 (“FIG. 2 illustrates the power supply circuitry for a flash memory including variable stage charge pumps for accommodating a 5 volt, 9 volt, and 12 volt voltage level

from **either a 3.3 volt or 5 volt power supply.**”); 7:15 (providing an example where “VCC = 3.3 volts”); 8:24-29 (providing an example where “VPP has a nominal value of 5 volts”). The switches for the selection are controlled by control signals provided by a selection circuit (e.g., selection circuit 290 with voltage detect circuits 230 and 231).

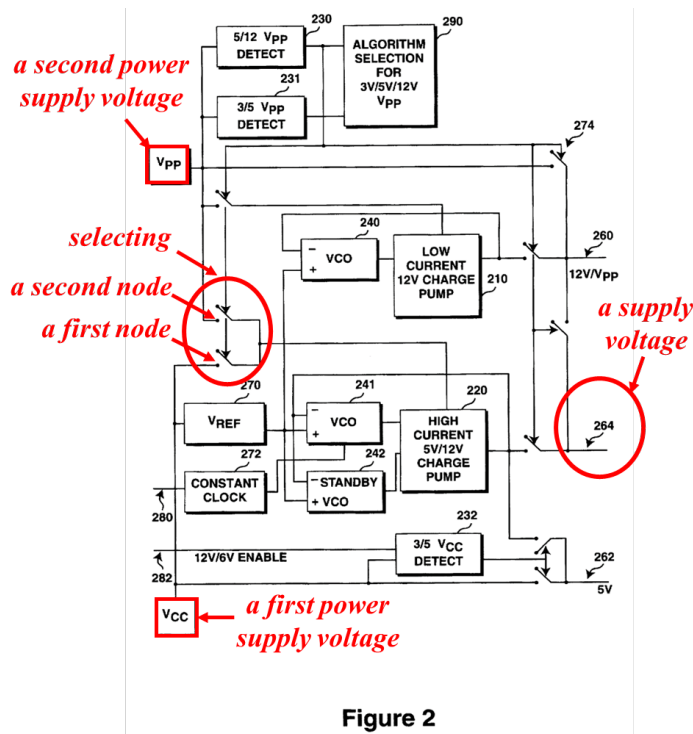


Figure 2

EX1006, Javanifard, FIG. 2, annotated

216. **Third**, as shown in the figures of Examples C and D of combinations of embodiments of Javanifard below, a POSITA would have been motivated to apply Javanifard teachings of an input power supply selector for selecting from input nodes supplied with different power supply voltages (as taught in Embodiment 2) in Javanifard’s variable stage charge pump system (e.g., as taught by variable stage

charge pump 100 of Embodiment 1 or the variable stage charge pump with n-charge pumps as taught in Embodiment 3). Such combinations have the benefit of providing a charge pump that can “**accommodate a given output level for different charge pump power supply input levels**”, e.g., for a device supplied with multiple power sources using two source lines (e.g., a primary power source and a supplemental power source). EX1006, Javanifard, 6:45-46 (describing that a flash memory device is provided by two sources including a primary power source VCC line and a supplemental power supply line, VPP); EX1005, Zhang, Abstract (describing “a charge pump circuit that operates responsive to a test or general operation mode,” where the operation mode corresponds to a selected voltage from two power sources VCC and VPP), FIG. 4; *see also* Ground 2: Reasons to Combine Embodiments of Javanifard.

217. As shown in the figures of Examples C and D below, in the combinations, one of a first input node supplied with a first (lower) power supply voltage and a second input node supplied with a second (higher) power supply voltage is selected, and provided to a booster circuitry. The figures below are simplified for illustration purposes, and it would have been obvious to a POSITA to implement additional well-known circuits (e.g., voltage detection circuit, voltage selection circuit providing control signals to selection switches, clock signals for driving the charge pumps) according to the design needs. Further, it would have

been obvious to a POSITA that various voltages for VCC (e.g., 3.3 volts or other voltages) and VPP (e.g., 5 volts or other voltages greater than VCC) would be used based on design needs.

218. Example C (Embodiments 1 and 2 of Javanifard combined) is illustrated below, which is a composite figure of FIGS. 1 and 2 of Javanifard.

*selecting one of a first input
node...and a second input node*

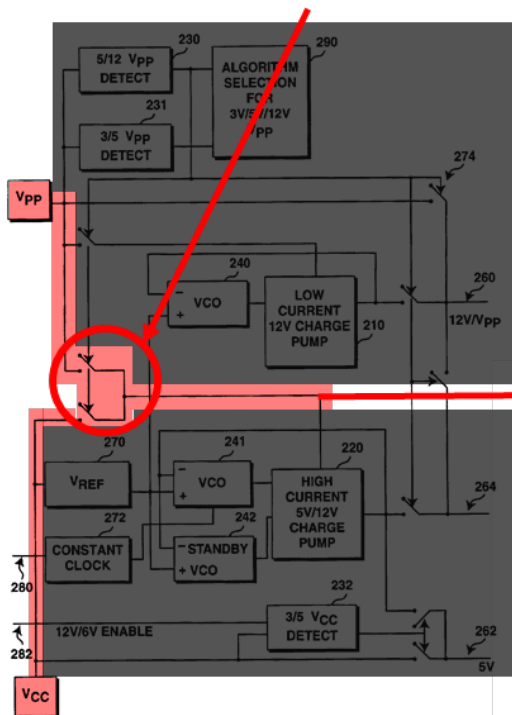


Figure 2

*booster
circuitry*

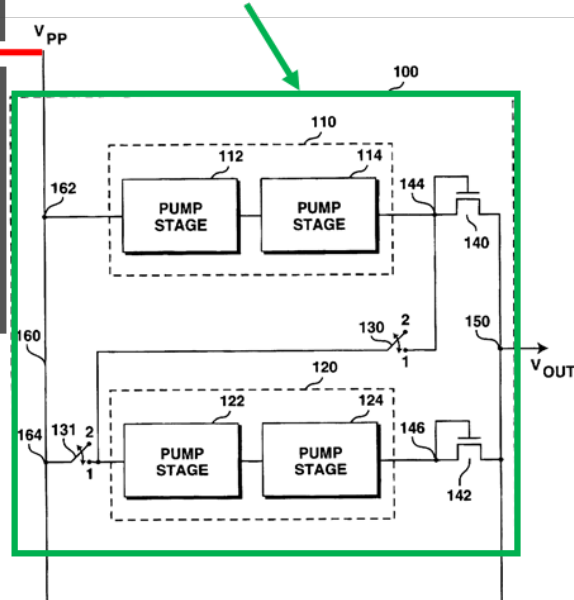


Figure 1

Example C (Embodiments 1 and 2 of Javanifard Combined)

219. Example D (Embodiments 2 and 3 of Javanifard combined) is illustrated below, which is a composite figure of FIGS. 2 and 3 of Javanifard.

*selecting one of a first input
node...and a second input node*

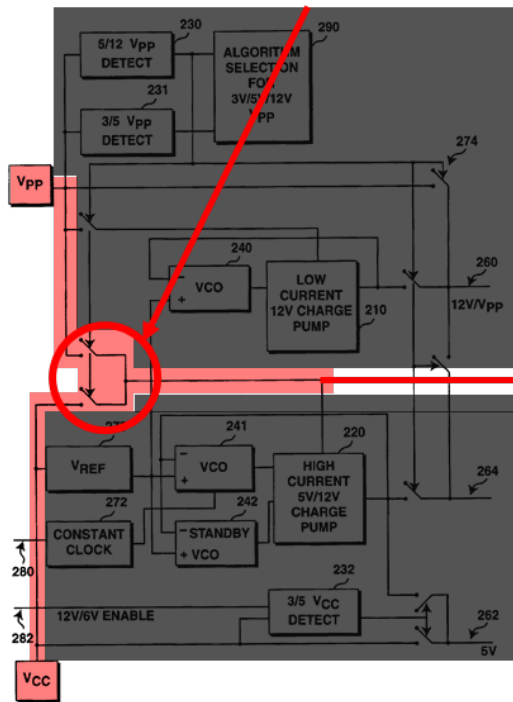


Figure 2

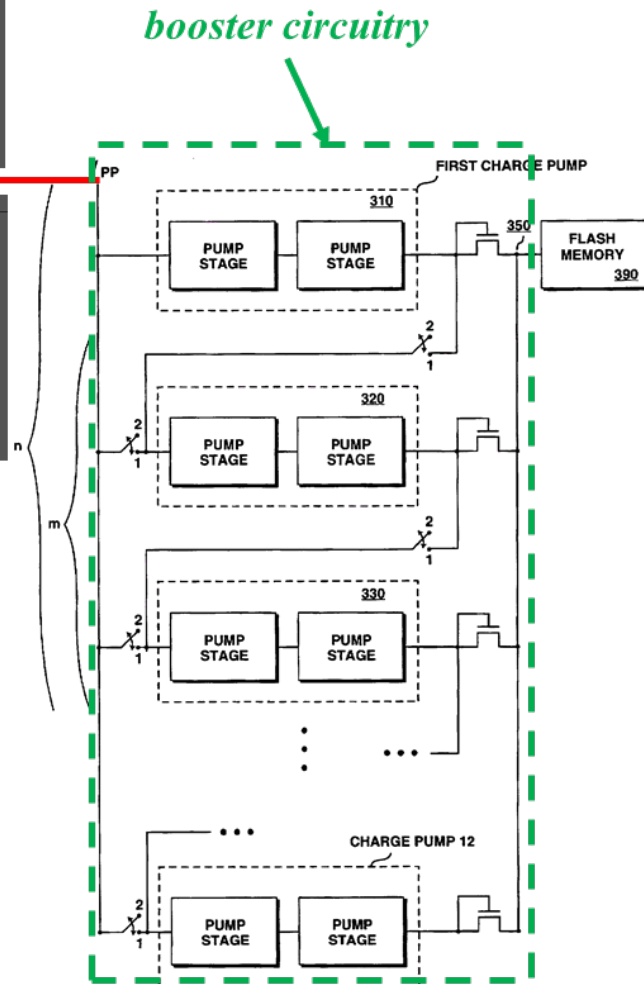


Figure 3

Example D (Embodiments 2 and 3 of Javanifard Combined)

220. Accordingly, Javanifard discloses or renders obvious “*selecting one of a first input node supplied with a first power supply voltage and a second input node supplied with a second power supply voltage that is higher than the first power supply voltage*” as claimed.

[1.2.1] coupling a selected one of the first and second input nodes to booster circuitry comprising a plurality of booster stages to provide an output voltage,

221. Javanifard discloses or at least renders obvious this element.

222. **First**, as discussed at Ground 2:[1.1], the combinations of embodiments of Javanifard teach that a selected one of the first and second input nodes is coupled to a variable stage charge pump (booster circuitry).

223. **Second**, as discussed at Ground 1:[1.2.1], as shown in FIGS. 1 and 3 of Javanifard, Javanifard describes that its variable stage charge pump (booster circuitry) comprises a plurality of booster stages to provide an output voltage.

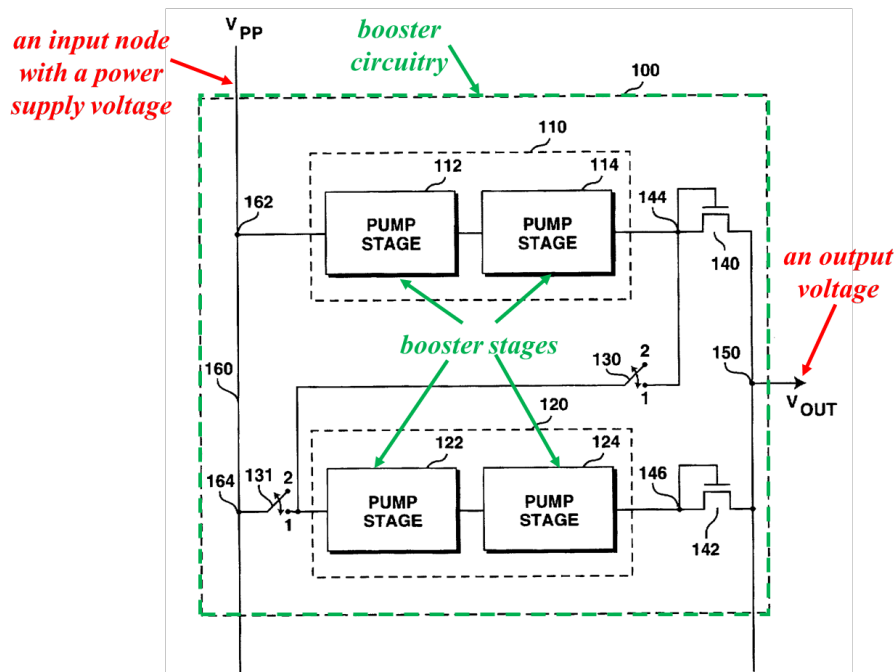


Figure 1

EX1006, Javanifard, FIG. 1, annotated

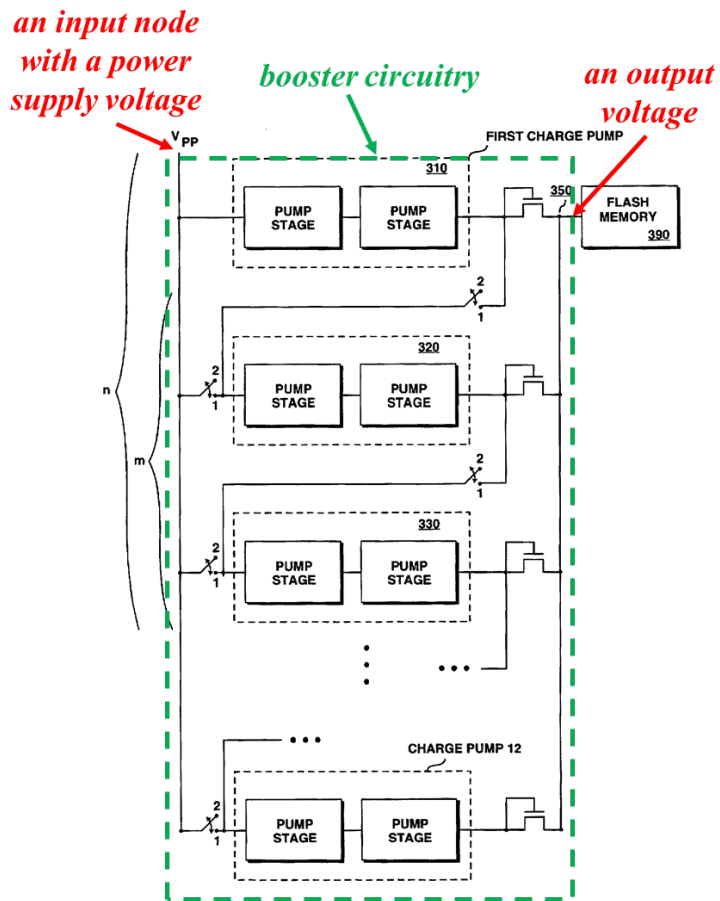


Figure 3

EX1006, Javanifard, FIG. 3, annotated

224. As such, in the combinations of embodiments of Javanifard, a selected one of the first and second input nodes is coupled to a variable stage charge pump (booster circuitry) comprising a plurality of booster stages to provide V_{out} .

225. Accordingly, Javanifard renders obvious “coupling a selected one of the first and second input nodes to booster circuitry comprising a plurality of booster stages to provide an output voltage” as claimed.

[1.2.2] wherein selection of the first input node corresponds to a first number of booster stages and

226. Javanifard renders obvious this element.

227. As discussed above at Ground 1:[1.2.2], Javanifard describes providing a variable stage charge pump to “accommodate a **given output level for different** charge pump power supply input levels.” EX1006, Javanifard, 2:22-24. For example, a POSITA would have configured the variable stage charge pump of FIG. 1 of Javanifard according to row 3 of Table 1 for a lower charge pump power supply input level, such that selection of the first input node corresponds to a first number (a higher number, e.g., 4) of booster stages.

228. As such, in Example C, to “accommodate a **given output level”** (EX1006, Javanifard, 2:22-24) for the first input node with a lower power supply voltage VCC, a POSITA would have configured the variable stage charge pump of FIG. 1 of Javanifard according to row 3 of Table 1 below, because row 3 of Table 1 provides a first number (a higher number, e.g., 4) of serially connected booster stages to provide a higher voltage boost (e.g., by serially connecting charge pumps 110 and 120), compared to row 1 of Table 1 (by providing only charge pump 110 in operation and thereby having a lower number of serially connected booster stages). Connecting more stages in series provide a higher voltage boost compared to using a smaller number of stages in series, as each stage in the charge pump contributes to

increasing the voltage level, and the total voltage boost is the cumulative effect of all the stages.

TABLE 1

Switch 130	Switch 131	Charge Pump 110	Charge Pump 120	
OFF	OFF	ON	OFF	<i>a second number of booster stages, the second number being less than first number</i>
OFF	ON	ON	parallel-coupled to charge pump 110	
ON	OFF	ON	series-coupled to charge pump 110	<i>a first number of booster stages</i>
ON	ON	N/A	N/A	

EX1006, Javanifard, Table 1, annotated

229. Corresponding to row 3 of Table 1, Javanifard explains that “[i]f switch 130 is on and switch 131 is off, charge pump 120 will be coupled so that charge pumps 110 and 120 are series-coupled. In other words, the input voltage for charge pump 120 will be provided from the output of charge pump 110. Because both 110 and 120 are two stage charge pumps, this means that charge pump 100 will **effectively be a four stage charge pump with all four stages serially coupled.**” EX1006, Javanifard, 3:54-60; compare with row 1 of Table 1 (“this configuration of switches 130 and 131 will effectively result in **a two stage charge pump,**” and this configuration “might be used in a power saving mode” compared with row 2 of Table 1). EX1006, Javanifard, 3:35-40.

230. Javanifard describes that “[i]n this configuration [of row 3 of Table 1], charge pump 100 will provide approximately twice the output voltage at node 150 as the previous two cases [including row 1 of Table 1].” EX1006, Javanifard, 3:60-63. A POSITA would have understood that this statement of “approximately twice the output voltage at node 150” applies when the input voltage levels are the same, and in a design to accommodate “a given output level for different charge pump power supply input levels,” the configuration of row 3 with more serially-connected stages provides more voltage boost for a lower power supply input level.

231. Similar analysis applies to Example D. It would have been obvious to a POSITA to use various suitable X and Y in the “X/Y stage pump,” pump stage designs, and configurations to provide the required output voltage according to the different power supply input levels.

232. Accordingly, Javanifard renders obvious “*wherein selection of the first input node corresponds to a first number of booster stages*” as claimed.

[1.2.3] selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number; and

233. Javanifard discloses or at least renders obvious this element.

234. **First**, as discussed at Ground 2:[1.2.1] and [1.2.2], in the combination of embodiments of Javanifard, selection of the first input node (with a lower input

power supply voltage level) corresponds to a first number (a higher number, e.g., 4) of booster stages.

235. **Second**, for similar reasons as discussed at Ground 2:[1.2.2], in the combination of embodiments of Javanifard, selection of the second input node (with a higher input power supply voltage level) corresponds to a second number (a lower number, e.g., 2) of booster stages, e.g., for generating the same output voltage as the selection of the first input node with a lower input power voltage level (corresponding to a higher number of booster stages).

236. Javanifard describes providing a variable stage charge pump to “accommodate a **given output level** for **different** charge pump power supply input levels.” EX1006, Javanifard, 2:22-24. Specifically, to “accommodate a **given output level**” (EX1006, Javanifard, 2:22-24) for the second input node with a higher power supply voltage, a POSITA would have configured the variable stage charge pump of FIG. 1 of Javanifard according to row 1 of Table 1 below, because row 1 of Table 1 provides a second (lower, e.g., 2) number of serially connected booster stages to provide a lower voltage boost (by providing only charge pump 110 in operation and thereby having a lower number of serially connected booster stages). Connecting less stages in series provide a lower voltage boost compared to using a higher number of stages in series, as each stage in the charge pump contributes to

increasing the voltage level, and the total voltage boost is the cumulative effect of all the stages.

TABLE 1

Switch 130	Switch 131	Charge Pump 110	Charge Pump 120	
OFF	OFF	ON	OFF	<i>a second number of booster stages, the second number being less than first number</i>
OFF	ON	ON	parallel-coupled to charge pump 110	
ON	OFF	ON	series-coupled to charge pump 110	<i>a first number of booster stages</i>
ON	ON	N/A	N/A	

EX1006, Javanifard, Table 1, annotated

237. Additionally, while configurations of rows 1 and 2 of Table 1 may provide substantially the same voltage boost, a POSITA would have used row 1 based on a design need for power saving mode, because it provides a lower current than row 2. EX1006, Javanifard, 3:39-42 (“This configuration [of row 1] might be used in a power saving mode if charge pump 100 is otherwise providing sufficient current and voltage output levels.”).

238. Similar analysis applies to Example D of the combination of Embodiments 2 and 3 of Javanifard. While the example of FIG. 1 and Table 1 of Javanifard provides a “X=2/Y=2 stage pump,” it would have been obvious to a POSITA to use various suitable X, Y, and pump stage designs to provide the required

output voltage according to the different power supply input levels, where a lower input voltage corresponds to a selection of a higher number of booster stages.

239. Accordingly, Javanifard discloses or renders obvious “*selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number*” as claimed.

[1.3] changing the booster circuitry from the first number of booster stages corresponding to selection of the first input node to the second number of booster stages when the second input node is selected.

240. Javanifard discloses or at least renders obvious this element.

241. **First**, as discussed at Ground 2: [1.2.2] and [1.2.3], in the combination of embodiments of Javanifard, selection of the first input node corresponds to a first number of booster stages, and selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number, e.g., to provide the same output voltage for different power supply voltage levels.

242. **Second**, as discussed at Ground 1:[1.3], Javanifard describes changing the booster circuitry from a higher number (e.g., 4) of booster stages corresponding to a lower power supply voltage to a lower number (e.g., 2) of booster stages when the power supply voltage is higher. EX1006, Javanifard, 1:8-11 (“providing a charge pump having a variable number as opposed to a fixed number of stages according to charge pump power supply input levels and desired charge pump

output levels”); EX1006, Javanifard, 5:65-66 (“The control for the switches would be a function of the available power supply voltage, VPP, and the desired variable stage charge pump output voltage.”). Specifically, as shown in Table 1 below, the number of the booster stages of the booster circuitry is changed (e.g., reduced from 4 to 2) by changing switch 130 from on (row 3) to off (row 1) to provide the same output voltage level, when the charge pump power supply input level increases.

TABLE 1

Switch 130	Switch 131	Charge Pump 110	Charge Pump 120	
OFF	OFF	ON	OFF	<i>a second number of booster stages, the second number being less than first number</i>
OFF	ON	ON	parallel-coupled to charge pump 110	
ON	OFF	ON	series-coupled to charge pump 110	<i>a first number of booster stages</i>
ON	ON	N/A	N/A	



EX1006, Javanifard, Table 1, annotated

243. Similar to the discussion at Ground 1:[1.3], in the combination of embodiments of Javanifard, when the selection of the input node is changed to the higher power supply voltage, the booster circuitry is changed from the first number of booster stages (e.g., 4) to the second number of booster stages (e.g., 2), by turning off switch 130.

244. Similar analysis applies to Example D of the combination of Embodiments 2 and 3 of Javanifard. While the example of FIG. 1 and Table 1 of

Javanifard provides a “X=2/Y=2 stage pump,” it would have been obvious to a POSITA to use various suitable X, Y, and pump stage designs to provide the required output voltage according to the different power supply input levels, where a lower input voltage corresponds to a selection of a higher number of booster stages.

245. Accordingly, Javanifard discloses or renders obvious “*changing the booster circuitry from the first number of booster stages corresponding to selection of the first input node to the second number of booster stages when the second input node is selected*” as claimed.

3. Claim 2 would have been obvious over Javanifard.

[2.0] 2. The method as claimed in claim 1, wherein the output voltage is the same when the first input node is selected and when the second input node is selected.

246. Javanifard renders obvious this element for reasons discussed at Ground 1:[2.0].

247. Specifically, as discussed at [1.2.2] and [1.2.3], Javanifard describes providing a variable stage charge pump to “accommodate a **given output level for different** charge pump power supply input levels.” EX1006, Javanifard, 2:22-24. As such, in the combinations of embodiments of Javanifard, a POSITA would have used the variable stage charge pump to provide the same output voltage for different charge pump power supply input levels, which are provided when the first input

node is selected and when the second input node is selected. *See also* Ground 1:
Claim 2.

248. Accordingly, Javanifard renders obvious “*wherein the output voltage is the same when the first input node is selected and when the second input node is selected*” as claimed.

4. Claim 3 would have been obvious over Javanifard.

[3.0] 3. The method as claimed in claim 1, wherein the output voltage is higher than the second power supply voltage.

249. Javanifard discloses or at least renders obvious this element for reasons discussed at Ground 1:[3.0].

250. Specifically, a charge pump circuit was used to generate an output voltage higher than an input power supply voltage, as well-known in the art and as explicitly described in Javanifard. *See, e.g.*, EX1008, Pan, 43 (“Charge pumps are circuits that generate a voltage level higher than the chip supply voltage from which they operate.”); EX1006, Javanifard, 1:20-30 (“Many operations, however, require voltages **greater than** that provided by the lower voltage power supplies. For example, flash electrically-erasable programmable read only memory (flash EEPROM) requires approximately 12 volts for erase and programming operations. **Charge pump technology permits the generation of voltages having a magnitude greater than that of the power supply.** Through the use of charge

pump circuitry 12 volts can be generated from 3.3 volts by using one or more charge pump stages.”).

251. As such, in the combinations of embodiments of Javanifard, the variable stage charge pump provides an output voltage higher than either one of the input power supply voltages, including the second power supply voltage.

252. Accordingly, Javanifard discloses or renders obvious “*wherein the output voltage is higher than the second power supply voltage*” as claimed.

5. Claim 4 would have been obvious over Javanifard.

[4.0] 4. The method as claimed in claim 1, wherein the second number of booster stages is one.

253. Javanifard discloses or at least renders obvious this element for the reasons discussed at Ground 1:[4.0].

254. As discussed at [1.2.2] and [1.2.3], in Example C with the variable stage charge pump of FIG. 1, the second number of booster stage is two. It would have been obvious to a POSITA to implement Y (the number of stages for each of fixed stage charge pumps 110 and 120) with any suitable numbers including one (1) based on the design needs. *See, e.g.*, EX1008, Pan, FIG. 3-2, 43-44; EX1015, Al-Shamma, FIGS. 1, 2, 4:61-5:59; EX1016, Daga, FIGS. 2A-2B, 4. As such, it would have been obvious to modify Example C and implement the fixed stage charge pump 110 of FIG. 1 with a single pump stage. In such implementation, when the second input

node with the higher power supply voltage is selected, the selected charge pump 110 has one (1) booster stage.

255. Accordingly, Zhang in view of Javanifard renders obvious that “*the second number of booster stages is one*” as claimed.

6. Claim 5 would have been obvious over Javanifard.

[5.0] 5. The method as claimed in claim 4, wherein the first number of booster stages is two.

256. Javanifard discloses or at least renders obvious this element for the reasons discussed at Ground 1:[5.0].

257. As discussed at Ground 2: [1.2.2] and [1.2.3], in Example C with the variable stage charge pump of FIG. 1, the first number of booster stage is 4, and as discussed at Ground 2:[4.0], it would have been obvious to modify Example C and implement the fixed stage charge pump 110 of FIG. 1 with a single pump stage. In such implementation, when the first input node with the lower power supply voltage is selected, the selected charge pump 110 has two (2) booster stages.

7. Claim 6 would have been obvious over Javanifard.

[6.0] 6. The method as claimed in claim 1, wherein the booster circuitry is changed between the first number of booster stages and the second number of booster stages with a switch.

258. Javanifard discloses or at least renders obvious this element for the reasons discussed at Ground 1:[6.0].

8. Claim 7 would have been obvious over Javanifard.

[7.0] 7. The method as claimed in claim 1, wherein the booster circuitry is changed with a selected one of a metal option, a bonding option, and a fuse option.

259. Javanifard discloses or at least renders obvious this element for the reasons discussed at Ground 1:[7.0].

9. Claim 8 would have been obvious over Javanifard.

[8.0] 8. The method as claimed in claim 1, wherein the output voltage is a power supply voltage VPP.

260. Javanifard discloses or at least renders obvious this element for the reasons discussed at Ground 1:[8.0].

10.Claim 9 would have been obvious over Javanifard.

[9.0] 9. The method as claimed in claim 1, wherein the booster circuitry comprises capacitors formed using thin gate oxide transistors.

261. Javanifard renders obvious this element for the reasons discussed at Ground 1:[9.0].

262. **First**, as discussed at Ground 1:[9.0], it was well-known that the pump stages in the booster circuitry include pumping capacitors for storing charges and thereby generating an output voltage higher than the input voltage. *See*, e.g., IV.A.2 (citing EX1014, Frulio, 1:23-34; EX1008, Pan, FIG. 3-2, 43-44; EX1015, Al-Shamma, FIG. 1, 4:61-64; 4:65-5:59; EX1016, Daga, FIGS. 2A-2B, FIG. 4); *see also* EX1005, Zhang, FIG. 5, 3:61-64. A POSITA would have found it obvious to

implement pumping capacitors in any of a variety of known and suitable ways—using either a thick gate oxide transistor or a thin gate oxide transistor in capacitor configuration (also referred to as a MOS capacitor), and would have been motivated to optimize the booster circuitry design by optimizing the pump capacitor by using a thin gate oxide transistor for the benefit of reduced area. *See, e.g.*, EX1020, Kang, Abstract, 258; EX1019, Narui, 9:51-64; EX1009, '422 app, 288, 311; EX1009, '422 app, 271-273, 298.

263. As such, in the combination of embodiments of Javanifard, a POSITA would have been motivated to implement the pump capacitors in the booster circuitry using thin gate oxide transistors for the benefit of area reduction.

264. Accordingly, Javanifard renders obvious that “*the booster circuitry comprises capacitors formed using thin gate oxide transistors*” as claimed.

11.Claim 10 would have been obvious over Javanifard.

[10.0] 10. A semiconductor device comprising:

265. To the extent that the preamble is limiting, Javanifard discloses or at least renders obvious the preamble.

266. Specifically, Javanifard teaches a semiconductor device, because it describes charge pump systems implemented in “integrated circuits,” and integrated circuit is a set of electronic circuits integrated on a semiconductor chip. EX1006, Javanifard, 1:15-19. Further, Javanifard teaches that the charge pump system is a

semiconductor device including semiconductor components (e.g., switches 130 and 131) implemented from metal oxide semiconductor field effect transistors (MOSFETs), which are semiconductor devices using semiconductor materials. EX1006, Javanifard, 3:13-15.

267. Accordingly, Javanifard discloses or renders obvious “*a semiconductor device*” as claimed.

[10.1] a first input node supplied with a first power supply voltage;

268. Javanifard discloses or at least renders obvious this element for the reasons discussed at Ground 2:[1.1].

[10.2] a second input node supplied with a second power supply voltage higher than the first power supply voltage;

269. Javanifard discloses or at least renders obvious this element for the reasons discussed at Ground 2:[1.1].

[10.3] booster circuitry comprising a plurality of booster stages to provide an output voltage; and

270. Javanifard discloses or at least renders obvious this element for the reasons discussed at Ground 2:[1.2.1].

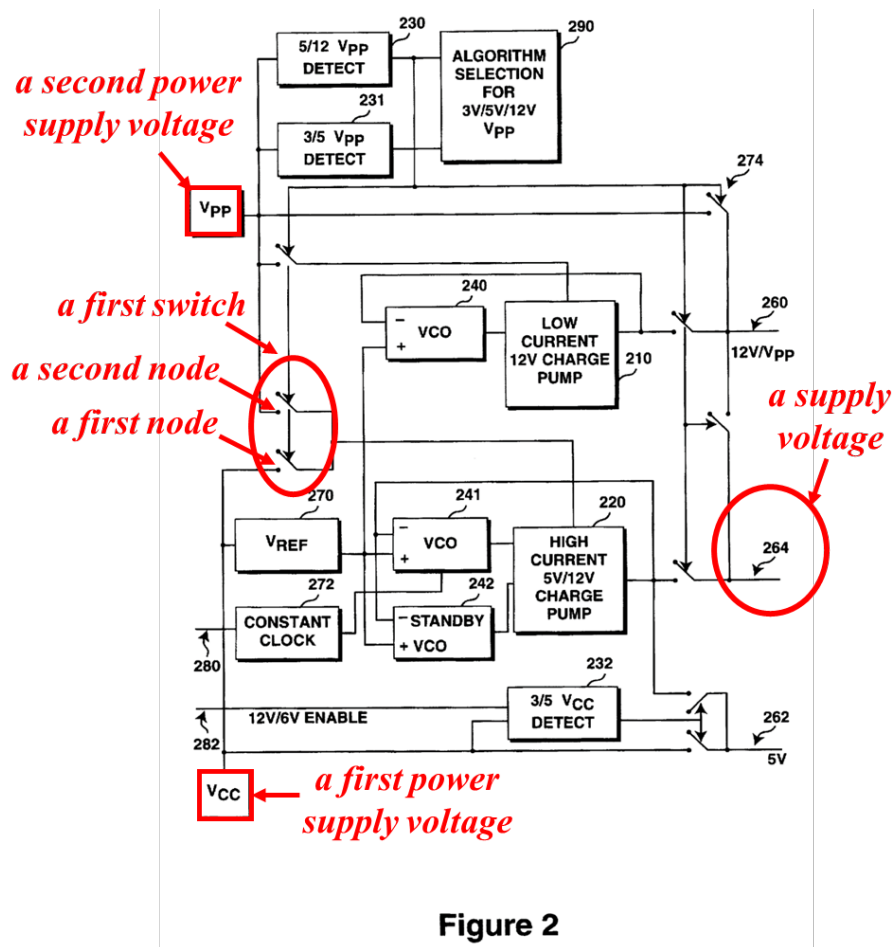
[10.4] a first switch configured to couple a selected one of the first input node and the second input node to the booster circuitry,

271. Javanifard discloses or at least renders obvious this element.

272. **First**, as discussed above at Ground 2:[1.1] and [1.2.1] above Javanifard describes an input power supply selector (including one or more

switches) for selecting from a first input node supplied with a first power supply voltage (e.g., VCC) and a second input node supplied with a second power supply voltage (e.g., VPP), and coupling the selected input node to the booster circuitry.

273. **Second**, as shown in annotated FIG. 2 of Javanifard below, Javanifard's input power supply selector includes one or more switches for selecting the input node. In FIG. 2 of Javanifard, two switches are illustrated for such selection, and either one of these switches teach the first switch as claimed. Furthermore, to the extent that Patent Owner argues that "only" one switch is used for such selection (which the claim does not require), it would have been obvious to a POSITA to implement the selection function as shown in FIG. 2 of Javanifard using either two switches (as illustrated in FIG. 2) or using a single switch (e.g., a three-way switch).



EX1006, Javanifard, FIG. 2, annotated

274. As such, in the combination (e.g., Examples C and D) of embodiments of Javanifard, a switch is used to couple a selected input node to the booster circuitry.

275. Accordingly, Javanifard discloses or renders obvious “*a first switch configured to couple a selected one of the first input node and the second input node to the booster circuitry*” as claimed.

[10.5] wherein the booster circuitry configured to have a first number of booster stages when the first input node is selected and to be changed to a second number of booster stages when the second input node is selected, the second number being less than the first number

276. Javanifard discloses or at least renders obvious this element for the reasons discussed at Ground 2:[1.2.2], [1.2.3] and [1.3]. Specifically, Javanifard teaches “*the booster circuitry configured to have a first number of booster stages when the first input node is selected*” for the reasons discussed at Ground 2:[1.2.2], and teaches that the booster circuitry is configured “*to be changed to a second number of booster stages when the second input node is selected, the second number being less than the first number*” for the reasons discussed at Ground 2:[1.2.2] and [1.3].

12.Claim 11 would have been obvious over Javanifard.

[11.0] 11. The semiconductor device as claimed in claim 10, wherein the output voltage is the same when the first input node is selected and when the second input node is selected.

277. Javanifard discloses or at least renders obvious this element for the reasons discussed at Ground 2:[2.0].

13.Claim 12 would have been obvious over Javanifard.

[12.0] 12. The semiconductor device as claimed in claim 10, wherein the output voltage is higher than the second power supply voltage.

278. Javanifard discloses or at least renders obvious this element for the reasons discussed at Ground 2:[3.0].

14.Claim 13 would have been obvious over Javanifard.

[13.0] 13. The semiconductor device as claimed in claim 10, wherein the second number of booster stages is one.

279. Javanifard discloses or at least renders obvious this element for the reasons discussed at Ground 2:[4.0].

15.Claim 14 would have been obvious over Javanifard.

[14.0] 14. The semiconductor device as claimed in claim 13, wherein the first number of booster stages is two.

280. Javanifard discloses or at least renders obvious this element for the reasons discussed at Ground 2:[5.0].

16.Claim 15 would have been obvious over Javanifard.

[15.0] 15. The semiconductor device as claimed in claim 10, wherein the booster circuitry is changed from the first number of booster stages and the second number of booster stages with a second switch.

281. Javanifard renders obvious this element.

282. **First**, as discussed at Ground 2:[10.4], in the combination of Javanifard embodiments, a first switch in a selector circuit is configured to couple a selected one of the first input node and the second input node to the booster circuitry.

283. **Second**, as discussed at Ground 2:[1.3] and [6.0], Javanifard teaches using a second switch (e.g., switch 130) in the variable stage charge pump, which is different from the first switch in the selector, is used to change the booster circuitry from the first number of booster stages to the second number of booster stages. The

switch (e.g., switch 130) in the variable stage charge pump teaches “*a second switch*” as claimed.

284. Accordingly, Javanifard renders obvious that “*the booster circuitry is changed from the first number of booster stages and the second number of booster stages with a second switch*” as claimed.

17.Claim 16 would have been obvious over Javanifard.

[16.0] 16. The semiconductor device as claimed in claim 10, wherein the booster circuitry is changed with a selected one of a metal option, a bonding option, and a fuse option.

285. Javanifard discloses or at least renders obvious this element for the reasons discussed at Ground 2:[7.0].

18.Claim 17 would have been obvious over Javanifard.

[17.0] 17. The semiconductor device as claimed in claim 10, wherein the output voltage is a power supply voltage VPP.

286. Javanifard discloses or at least renders obvious this element for the reasons discussed at Ground 2:[8.0].

19.Claim 18 would have been obvious over Javanifard.

[18.0] 18. The semiconductor device as claimed in claim 10, wherein the booster circuitry comprises capacitors formed using thin gate oxide transistors.

287. Javanifard discloses or at least renders obvious this element for the reasons discussed at Ground 2:[9.0].

D. Grounds 3 and 4: Combination of Zhang, Javanifard, and Kang (Ground 3) and Combination of Javanifard and Kang Render Obvious Claims 9 and 18 (Ground 4).

288. The analysis for Grounds 3 and 4 rely on the analysis and evidence as provided for Ground 1 (Zhang and Javanifard) and Ground 2 (Javanifard), respectively, except for where additional analysis (applying for both Grounds 3 and 4) is provided below.

1. Reasons to Combine Javanifard and Kang

289. As discussed at Grounds 1 and 2 above, the combination of Zhang and Javanifard and the combination of Javanifard embodiments similarly teach a multi-power-source charge pump system using a variable stage charge pump as taught in Javanifard.

290. A POSITA would have been motivated to apply Kang's teaching of using thin-oxide MOSFETs as the pumping capacitors in the variable stage charge pump, to produce the obvious, beneficial, and predictable results of a charge pump system with "low area and high power efficiency," as taught by Kang.

291. **First**, like the '701 patent, Kang is analogous prior art to the '701 patent, and is in the same field of endeavor pertaining to generating a supply voltage using charge pump systems. *See, e.g.*, EX1001, '701 patent Title, 1:14-20; EX1020, Kang, Title ("Charge Pump Circuits with Low Area and High Power Efficiency for Memory Applications"), Abstract (describing charge pump circuits that use "the

thin-oxide MOSFETs as the pumping capacitors” to “reduce the area of charge pumps greatly while keeping their driving capability.”).

292. **Second**, Kang explicitly provides motivations to apply its teaching of using the thin-oxide MOSFETs as the pumping capacitors in a charge pump system, to achieve “charge pump circuits with low area and high power efficiency.” EX1020, Kang, 262. Specifically, Kang describes that by using thin-oxide transistors to form the pumping capacitors, “the layout area of [pumping capacitors] becomes smaller compared with that of thick-oxide transistor,” and “[b]ecause the area of the pumping capacitors takes the largest part of the total pump area, it is very helpful to make the area of the pumping capacitors small for reducing the total pump area.” EX1020, Kang, 258; *see also* EX1019, Narui, 9:51-64 (explaining that in a boosted potential generation circuit, using a capacitor MOS transistor with thin gate insulating film “is effective for reducing a chip size.”).

293. A POSITA designing a charge pump system including a variable stage charge pump as taught by Javanifard would have been motivated to apply Kang’s teachings of a pump stage design using the thin-oxide MOSFETs as the pumping capacitors for the obvious, beneficial, and predictable results of an improved charge pump system by “reduc[ing] the area of charge pumps greatly while keeping their driving capability,” as taught by Kang. EX1020, Kang, Abstract.

294. Applying Kang's teachings in the variable stage charge pump of Javanifard would have been no more than the combination of known elements according to known methods (implementing the generic pump stages of a variable stage charge pump using a pump stage design using thin oxide pumping capacitors according to known IC design methods) obvious to a POSITA. While examples of Kang (e.g., FIG. 1(b), FIG. 2(c) and 2(d)) illustrate 3-stage charge pumps, it would have been obvious to a POSITA to apply Kang's teaching of using thin-oxide capacitors in each pump stage of the charge pump, regardless of the charge pump's number of stages. Techniques for designing (e.g., using IC design and simulation tools) and making an IC including various components like charge pumps and pump stages were well-known.

2. Claim 9 would have been obvious over Zhang in view of Javanifard in view of Kang, and would have been obvious over Javanifard in view of Kang.

[9.0] 9. The method as claimed in claim 1, wherein the booster circuitry comprises capacitors formed using thin gate oxide transistors.

295. Javanifard in view of Kang renders obvious this element.

296. **First**, as discussed in Grounds 1 and 2:[9.0], it would have been obvious to use pumping capacitors formed using thin gate oxide transistors in the variable stage charge pump for the benefit of area reduction..

297. **Second**, Kang explicitly describes pump stage designs where capacitors are formed using thin gate oxide transistors. EX1020, Kang, Abstract (“Using the thin-oxide capacitors [to form the pumping capacitors] can reduce the area of charge pumps greatly while keeping their driving capability.”; EX1020, Kang, FIG. 1(b), 258 (illustrating an example low-area pump circuit where “pumping capacitors...can be made with the thin oxide transistors”); FIG. 2(c) and 2(d) (illustrating charge pump designs where pumping capacitors are made with the thin-oxide transistors), 260-262 (providing simulation results verifying the power efficiency and area efficiency of the pump circuit designs using thin-oxide capacitors).

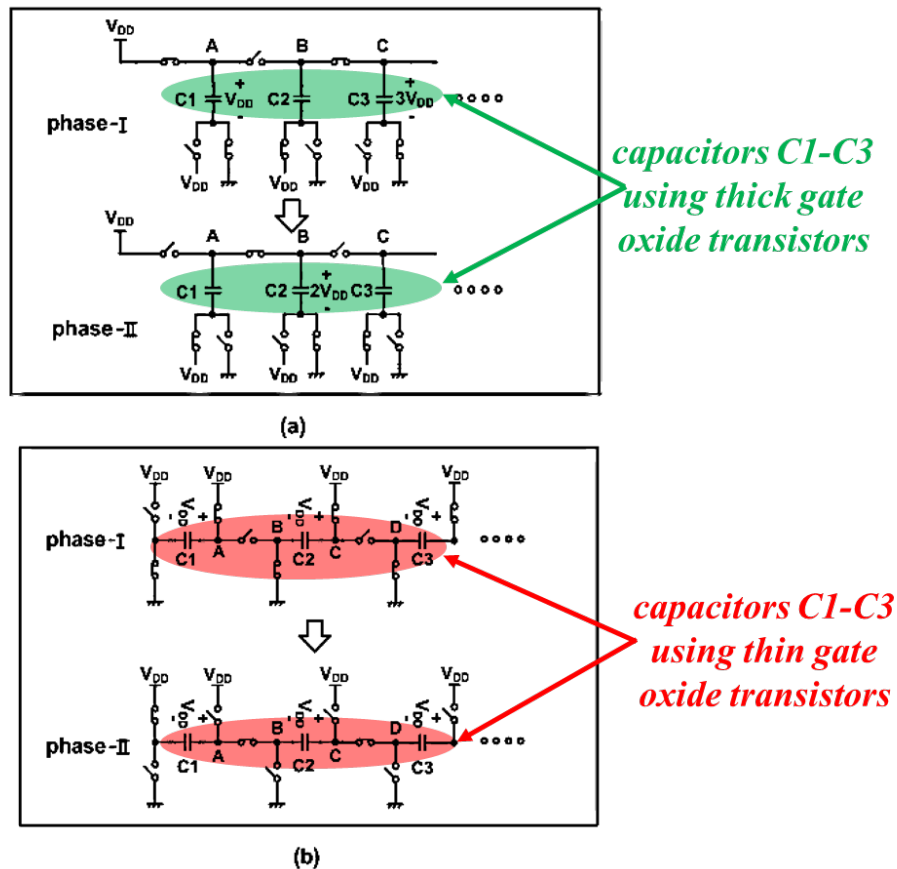


Fig. 1. (a) A conceptual diagram of the conventional charge pump (b) A conceptual diagram of new charge pump.

EX1020, Kang, FIG. 1, annotated

298. A POSITA would have been motivated to apply Kang's teaching of a pump stage design using thin-oxide MOSFETs as the pumping capacitors in Javanifard's variable stage charge pump to produce the obvious, beneficial, and predictable results of a charge pump system with "low area and high power efficiency," as taught by Kang. *See also* Grounds 3 and 4: Reasons to combine Javanifard and Kang.

299. Accordingly, Javanifard in view of Kang renders obvious that “*the booster circuitry comprises capacitors formed using thin gate oxide transistors*” as claimed.

3. Claim 18 would have been obvious over Zhang in view of Javanifard and Kang and would have been obvious over Javanifard and Kang.

[18.0] 18. The semiconductor device as claimed in claim 10, wherein the booster circuitry comprises capacitors formed using thin gate oxide transistors.

300. Javanifard in view of Kang renders obvious this element for the reasons discussed at Grounds 3 and 4:[9.0].

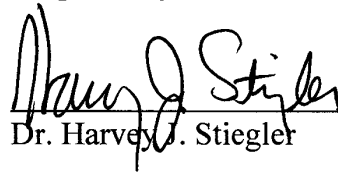
Declaration of Dr. Harvey J. Stiegler Under 37 C.F.R. § 1.68
In Support of *Inter Partes* Review of U.S. Patent No. 9,207,701

IX. CONCLUSION

301. I hereby declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct, and that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements are punishable by fine or imprisonment or both. *See* 18 U.S.C. § 1001.

Date: 7/20/23

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Harvey J. Stiegler", is written over a horizontal line.

Dr. Harvey J. Stiegler