

Harvey J. Stiegler

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Education:

PhD Electrical and Computer Engineering, Rice University, 1989.
MS Electrical and Computer Engineering, Rice University, 1985.
BS Electrical Engineering (with honors), Texas Tech University, 1973.

Employment and Professional Experience:

08/11 – present: Technical Consultant
04/09 – present: The University of Texas at Dallas
05/79 – 03/09: Texas Instruments Incorporated
08/73 – 03/79: U.S. Air Force

Experience (Summary):

- Twenty-five years MOS circuit design experience emphasizing transistor-level circuit design of MOS circuits (analog, digital, mixed-signal, system interface), integrated circuit architecture, memory-related circuits and architectures (EPROM, Flash Memory, DRAM, and SRAM), memory interfaces and interface circuits, SPICE simulation, layout, parasitic extraction, full-chip simulation including power bus and interconnect parasitics, DRC, LVS, chip architectures, and design methodology.
- Extensive experience interacting with process development and process integration teams including:
 - Knowledge of EPROM, Flash, DRAM, and SRAM memory technologies and storage cell structures.
 - Knowledge of analog and digital CMOS process technologies, device structures, design rules, and design/process interaction.
 - Knowledge of semiconductor devices and device physics from the design perspective.
 - Experience in use of TCAD simulators (SUPREM3, TSUPREM4, Medici) and statistical design tools.
- Patent committee member (MOS Memory Division, 8 years) responsible for evaluating submitted disclosures for significant value based on novelty and enforceability, reading and understanding claims, analyzing if products infringe claims, researching potential prior art, evaluating issued patents for patent incentive awards based on internal and external use.
- Five years design management experience leading design teams from 5 to 22 people.
- Three-plus years experience managing a product engineering team specializing in test, redundancy repair, debug, and yield analysis of embedded cache SRAMs for SPARC microprocessors.

Assignment Details (Technical Consultant):

08/11 – Present: Technical Consultant

- Integrated circuit design consulting.
- Patent and intellectual property consultant.

Assignment Details (University of Texas at Dallas):

04/09 – Present: Adjunct Professor (2007-2009), Research Scientist (04/09 – 12/11),
Visiting Researcher (12/11 – present), Dept. of Materials Science and Engineering

- Research in analog circuits and floating gate devices.
- Development of devices and circuits utilizing organic and inorganic semiconductors for flexible electronics.
- Development of bio-molecular sensor devices for medical applications, sensor device SPICE models, and sensor support circuits.
- Research into low-temperature fabrication of neuromorphic circuits and associated SPICE modeling.

Assignment Details (Texas Instruments):

12/05 – 03/09: Senior Member, Technical Staff, Analog Technology Development Group

- Senior design engineer and technical contributor for a team responsible for developing memory technologies, including non-volatile memory (Flash Memory, EEPROM, OTP) and static RAMs, for Analog and Mixed Signal Technologies.

11/04 – 12/05: Senior Member, Technical Staff, RFID Business UHF Engineering Group

- Responsible for working with Technology Development to define the roadmap for RFID next-generation Non-Volatile Memory (NVM). Work with Technology Development and External Manufacturing to define SC technology roadmap for RFID. Enable and staff IC design team for RFID UHF Engineering Group and put design tools in place. Define technology and simulation methodology to enhance RFID. Participate in debug and analysis of prototype devices as needed.

12/00 – 11/04: Manager, SRAM Test Engineering, SPARC Products Group

- Responsible for managing a group of test engineers that provide embedded SRAM test programs, redundancy analysis, and laser/eFuse repair for all new Sun SPARC microprocessors. Supported test, design debug, failure analysis, and yield improvement of microprocessor cache SRAMs.

2/99 - 12/00: SMTS and Design Engineer, Mixed Signal Products

- Senior design engineer responsible for circuit design and supervision of layout for various circuit components for mixed-signal integrated circuits.

1/96 – 1/99: SMTS and Senior Design Engineer

- Conducted evaluations of statistical modeling and circuit design tools. Initiated the first effort within TI to pursue statistical SPICE model generation and circuit simulation. This effort was subsequently transferred to the SPICE model labs and the MSLP statistical design group.
- Responsible for evaluation of potential product opportunities utilizing Merged DRAM and Logic technology. Conducted architecture studies and cost analysis of product opportunities.
- Senior design engineering member of System Interface Team supporting analysis and debug of system-related product issues.
- Responsible for resolving all customer-related design issues with the PTEC Custom Flash Lifetime Buy after the sale of the MOS Memory Division to Micron.

1990 - 1995: Project Design Manager, Flash Memory

- Managed the design of the 28F010, 28F210, and 28F512 flash memories. These 1Mbit and 512Kbit devices were the first TI high-volume production flash memory products.
- Tasks included working with Process Development and Technology groups to develop process requirements and a production-worthy Flash technology and solve technology issues such as over-erase and program/erase endurance.
- Managed the design of the PTEC custom flash memory product for Ford. Supervised a large design team which completed a very complex design on schedule to customer requirement. The PTEC project achieved first-pass design success and on time delivery of samples which met Ford's critical milestones when the second-source competitor failed, resulting in TI being awarded 100% of the business.
- Principal developer of procedural design methodology for Commodity Flash Memory products and subsequent derivatives.

1989 - 1990: Senior Design Engineer, Flash Memory

- Senior technical contributor to the design of development vehicles for 5V-only Flash Memory technology.

6/85 - 1989: Senior DRAM Design Engineer

- Principal contributor to architectural analysis and circuit design of the initial version of the 16Mbit DRAM.
- Key contributor in working with Process Development / Process Integration engineers to define the storage cell, design rules, and process requirements.
- Responsible for multiple design debug and productization tasks on the 1Mbit DRAM generation and support of 4Mbit DRAM productization. Performed full-chip SPICE simulation, including simulation of power bus structure and interconnect parasitics for major global signals, and chip-level LVS.

9/83 - 5/85: On Educational Leave of Absence at Rice University.

5/79 - 8/83: Design Engineer

- Design engineer on 16K thru 128K EPROMS.
- Responsible for all circuit design, SPICE simulation, layout, and LVS of complete designs, as well as some test and laboratory debug of prototypes.
- Contributing design engineer on 64K and 1Mbit DRAM generations.

U. S. Patents:

- 9,787,263, Patel, Ujas N., Marshall, Andrew, Stiegler, Harvey J. and Jarreau, Keith M. "Mismatch Correction in Differential Amplifiers Using Analog Floating Gate Transistors."
- 9,042,173, Stiegler, Harvey J. and Dang, Luan, "Efficient Memory Sense Architecture."
- 8,908,412, Stiegler, Harvey J. and Mitchell, Allan T., "Array Architecture for Reduced Voltage, Low Power, Single Poly EEPROM."
- 8,174,884, Mitchell, Allan T. and Stiegler, Harvey J., "Low Power, Single Poly EEPROM Cell with Voltage Divider."
- 5,786,702, Stiegler, Harvey J. and Krzentz, Steven V., "Method for detecting defects in integrated-circuit arrays."
- 5,773,997, Stiegler, Harvey J., "Reference circuit for sense amplifier."
- 5,528,543, Stiegler, Harvey J., "Sense amplifier circuitry."
- 5,313,432, Lin, Sung-Wei, Schreck, John F., Truong, Phat. C., McElroy, David J., Stiegler, Harvey J., Ashmore, Jr., Benjamin H., Gill, Manzur, "Segmented, multiple-decoder memory array and method for programming a memory array."
- 4,692,638, Stiegler, Harvey J., "CMOS/NMOS decoder and high-level driver circuit."

Honors and Awards:

Senior Member, Technical Staff, Texas Instruments, elected 1993

Member, Group Technical Staff, Texas Instruments, elected 1990

NSF Graduate Student Fellowship

Professional Memberships and Technical Activities:

- Life Senior Member, IEEE, IEEE Solid State Circuits Society, IEEE Electron Devices Society, and IEEE Computer Society
- Member, American Physical Society
- Member, American Association for the Advancement of Science
- Member, Tau Beta Pi, Engineering Honorary
- Member, Eta Kappa Nu, Electrical Engineering Honorary

Additional Past Technical Activities:

- Industry mentor to the IRAM (Intelligent RAM) project, University of California Berkeley.
- Member, Corporate Patent Committee, Texas Instruments
- Member, MOS Memory Division Patent Committee, Texas Instruments
- IDEA Program Representative, Texas Instruments
- Member, Design Methodology QIT, MOS Memory Division, Texas Instruments
- Member, SPICE Model Council, Texas Instruments

Additional Interests and Activities:

- Member of the Board of Directors, Vice President, and President, **Voices of Change** – New Music Ensemble of Dallas, 2009-2015
- Member of the Board of Directors, **Dallas Symphony Orchestra Guild**, 2012-2014.
- Member of the Board of Directors and President, **Open Classical**, 2014-present.

Publications and Presentations:

Jin Woong Kwak, Andrew Marshall, and Harvey Stiegler, “28nm STT-MRAM Array and Sense Amplifier”, 2019 8th International Conference on Modern Circuits and Systems Technologies (MOCAS), Thessaloniki, Greece, May 13-15, 2019.

Ujas Patel, Sai Govinda Rao Nimmalapudi, Harvey Stiegler, Andrew Marshall, and Keith Jarreau, “Enhancing Circuit Operation using Analog Floating Gates”, IEEE International Conference on Quality Electronic Design (ISQED), Santa Clara, March 13-14, 2018.

D. Mao, I. Mejia, A. L. Salas-Villasenor, H. J. Stiegler, B. E. Gnade, and M. A. Quevedo-Lopez, “Low Temperature Processed Two-Transistor- Two-Capacitor-Based Ferroelectric Random Access Memory”, *IEEE Transactions on Electron Devices*, DOI: 10.1109/TED.2014.2347053, 2014.

A. Subramaniam, K. D. Cantley, H. J. Stiegler, R. A. Chapman, and E. M. Vogel, “Low-Temperature Fabrication of Spiking Soma Circuits Using Nanocrystalline-Silicon TFTs”, *IEEE Transactions on Neural Networks and Learning Systems*, DOI: 10.1109/TNNLS.2013.2256926, 2013.

K. D. Cantley, A. Subramaniam, H. J. Stiegler, R. A. Chapman, and E. M. Vogel, “Neural Learning Circuits Utilizing Nano-Crystalline Silicon Transistors and Memristors,” *IEEE Transactions on Neural Networks and Learning Systems*, DOI: 10.1109/TNNLS.2012.2184801, 2012.

A. Subramaniam, K. D. Cantley, H. J. Stiegler, R. A. Chapman, and E. M. Vogel, “Submicron Ambipolar Nanocrystalline Silicon Thin-Film Transistors and Inverters,” *IEEE Transactions on Electron Devices*, DOI: 10.1109/TED.2011.2176737, 2012.

P. G. Fernandes, R. A. Chapman, O. Seitz, H. J. Stiegler, H.-C. Wen, Y. J. Chabal, and E. M. Vogel, “Effect of Back-Gate Biasing on Floating Electrolytes in Silicon-on-Insulator-Based Nanoribbon Sensors”, *IEEE Electron Device Letters*, DOI: 10.1109/LED.2011.2179115, 2012.

K. D. Cantley, P. G. Fernandes, Mingyue Zhao, H. J. Stiegler, R. A. Chapman and Eric M. Vogel, “Noise effects in field-effect transistor biological sensor detection circuits”, *2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, DOI: 10.1109/MWSCAS.2012.6292034, 2012.

B. Shrestha, R. Pieper, W. Wondmagegn, Duo Mao, I. Mejia, H. Stiegler, B. E. Gnade, and M. Quevedo-Lopez, “A practical model to analytically characterize the polarization hysteresis of ferroelectric capacitors”, *2012 44th Southeastern Symposium on System Theory (SSST)*, DOI: 10.1109/SSST.2012.6195142, 2012.

A. Subramaniam, K. D. Cantley, R. A. Chapman, H. J. Stiegler, and E. M. Vogel, “Submicron Ambipolar Nanocrystalline-silicon TFTs with High- κ Gate Dielectrics,” *International Semiconductor Device Research Symposium (ISDRS)*, College Park, MD, 2011.

P. G. Fernandes, H. J. Stiegler, M. Zhao, K. D. Cantley, B. Obradovic, R. A. Chapman, H.-C. Wen, G. Mahmud, and E. M. Vogel, “SPICE Macromodel of Silicon-on-Insulator-Field-Effect-Transistor-Based Biological Sensors,” *Sensors and Actuators B*, DOI: 10.1016/j.snb.2011.10.002, 2011.

Israel Mejia, Ana L. Salas-Villasenor, Adrian Avendano-Bolivar, Julius Horvath, Harvey Stiegler, Bruce E. Gnade, and Manuel A. Quevedo-Lopez, “Low-Temperature Hybrid CMOS Circuits Based on Chalcogenides and Organic TFTs”, *IEEE Electron Device Letters*, 10.1109/LED.2011.2157801

D. Mao, I. Mejia, H. Stiegler, B. E. Gnade, M. A. Quevedo-Lopez, “Fatigue characteristics of poly(vinylidene fluoride-trifluoroethylene) copolymer ferroelectric thin film capacitors for flexible electronics memory applications”, *Organic Electronics*, Org. Electron. (2011), doi:10.1016/j.orgel.2011.04.011

Oliver Seitz, Poornika G. Fernandes, Gazi A. Mahmud, Huang-Chun Wen, Harvey J. Stiegler, Richard A. Chapman, Eric M. Vogel, and Yves J. Chabal, “One-Step Selective Chemistry for Silicon-on-Insulator Sensor Geometries”, *Langmuir*, dx.doi.org/10.1021/la200471b | Langmuir 2011, 27, 7337–7340.

K. D. Cantley, A. Subramaniam, H. J. Stiegler, R. A. Chapman, and E. M. Vogel, "Spike Timing-Dependent Synaptic Plasticity Using Memristors and Nano-Crystalline Silicon TFT Memories," 11th International Conference on Nanotechnology (IEEE Nano), 2011.

K. D. Cantley, A. Subramaniam, H. J. Stiegler, R. A. Chapman, and E. M. Vogel, "Hebbian Learning in Spiking Neural Networks with Non-crystalline Silicon TFTs and Memristive Synapses," IEEE Transactions on Nanotechnology, DOI 10.1109/TNANO.2011.2105887, 2011.

W. T. Wondmagegn, N.T. Satyala, R.J. Pieper, M.A. Quevedo-Lopez, S. Gowrisanker, H.N. Alshareef, H.J. Stiegler, B.E. Gnade, "Impact of Semiconductor/Metal Interfaces on Contact Resistance and Operating Speed of Organic Thin Film Transistors", Journal of Computational Electronics, 10(1-2), pp. 144-153, June 2011.

Richard A. Chapman, Poornika G. Fernandes, Oliver Seitz, Harvey J. Stiegler, Huang-Chun Wen, Yves J. Chabal, and Eric M. Vogel, "Comparison of Methods to Bias Fully Depleted SOI-Based MOSFET Nanoribbon pH Sensors," IEEE Trans. Electron Devices, vol. ED-58, no. 6, pp. 1752-1760, June. 2011.

W. T. Wondmagegn, N. T. Satyala, I. Mejia-Silva, D. Mao, S. Gowrisanker, H. N. Alshareef, H. J. Stiegler, M. A. Quevedo-Lopez, R. J. Pieper, B. E. Gnade, "Experimental and modeling study of the capacitance-voltage characteristics of metal-insulator-semiconductor capacitor based on pentacene/parylene", Thin Solid Films, 519(13), pp. 4313-4318 29 April 2011.

O. Seitz, P. G. Fernandes, R. Tian, H.-C. Wen, H. J. Stiegler, R. A. Chapman, E. M. Vogel, Y. J. Chabal, "Control and stability of self-assembled monolayers under biosensing conditions", Journal of Materials Chemistry, 21(12), pp. 4384-4392, (28 March 2011), 10.1039/C1JM10132C.

W. T. Wondmagegn, N. T. Satyala, H. J. Stiegler, M. A. Quevedo-Lopez, E. W. Forsythe, R. J. Pieper, B. E. Gnade, "Simulation based performance comparison of transistors designed using standard photolithographic and coarse printing design specifications", Thin Solid Films, 519(6), pp. 1943-1949, 3 January 2011.

P. G. Fernandes, R. A. Chapman, H. J. Stiegler, H.-C. Wen, B. Obradovic, and E. M. Vogel, "Models for Nanoscale Silicon Chemical and Biological Sensors," TxACEAnalog Symposium, Dallas, TX, Nov. 15, 2010

P. G. Fernandes, O. Seitz, R. A. Chapman, H. J. Stiegler, H.-C. Wen, Y. J. Chabal, and E. M. Vogel, "Ultra-low detection using ultra-thin SOI-based nanoribbon sensors," MRS Fall 2010, Boston, MA

P. G. Fernandes, R. A. Chapman, O. Seitz, H. J. Stiegler, H.-C. Wen, Y. J. Chabal, and E. M. Vogel, "Impact of Back-Gate Biasing on Ultra-thin Silicon-On-Insulator-Based Nanoribbon Sensors," IEEE International SOI Conference, October 2010, 10.1109/SOI.2010.5641066

D. Mao, I. Mejia, H. Stiegler, B. E. Gnade, M.A. Quevedo-Lopez; "Polarization Behavior of Poly(vinylidene fluoride-trifluoroethylene) Copolymer ferroelectric thin film capacitors for Non-Volatile Memory Application in Flexible Electronics", Journal of Applied Physics, 108(9), 1 November 2010, 10.1063/1.3500428.

K. D. Cantley, A. Subramaniam, R. R. Pratiwadi, H. C. Floresca, J. Wang, H. J. Stiegler, R. A. Chapman, M. J. Kim, and E. M. Vogel, "Hydrogenated Amorphous Silicon Nanowire Transistors with Schottky Barrier Source/Drain Junctions," Applied Physics Letters, vol. 97, no. 14, 2010.

K. D. Cantley, A. Subramaniam, H. J. Stiegler, R. A. Chapman, and E. M. Vogel, "SPICE Simulation of Nanoscale Non-Crystalline Silicon TFTs in Spiking Neuron Circuits," Int. Midwest Symp. Circuits and Systems (MWSCAS), Seattle, WA, August 2010.

P. G. Fernandes, O. Seitz, R. A. Chapman, H. J. Stiegler, H. -C. Wen, Y. J. Chabal, and E. M. Vogel, "Effect of mobile ions on ultra-thin SOI-based sensors," Applied Physics Letters **97**, 034103 (2010) ***Selected for the August 2, 2010 issue of Virtual Journal of Nanoscale Science & Technology**

D. Mao, M. A. Quevedo-Lopez, H. Stiegler, B. E. Gnade, H. N. Alshareef; "Optimization of poly(vinylidene fluoride-

trifluoroethylene) films as non-volatile memory for flexible electronics”, *Organic Electronics*, 11, 925-932 (2010).

D. Mao, I. Mejia, H. Stiegler, B. E. Gnade and M.A. Quevedo-Lopez; “Polarization behavior of poly(vinylidene fluoride-trifluoroethylene) copolymer ferroelectric thin film capacitors for non-volatile memory application in flexible electronics.” *Organic Microelectronics & Optoelectronics Workshop VI*, San Francisco, July 2010.

A. Avendano, M. R. Perez, H. J. Stiegler, B. E. Gnade, M. A. Quevedo-Lopez “Characterization of semiconductor/hybrid gate dielectric interfaces for improved reliability organic thin film transistors” *Flextech 2010*, Phoenix, Feb 2010.

Duo Mao, M. A. Quevedo-Lopez, Harvey J. Stiegler, Husam N. Alshareef, Bruce E. Gnade; “Low Voltage Flexible Ferroelectric Non-Volatile Memory based on Poly(vinylidene fluoride-trifluoroethylene)”, *FlexTech 2010*, Phoenix, Feb 2010.

P. G. Fernandes, O. Seitz, R. A. Chapman, H. J. Stiegler, H.-C. Wen, Y. J. Chabal, and E. M. Vogel, “Effects of Fluid Media on Ultra-Thin SOI Based pH Sensors,” *IEEE International Semiconductor Device Research Symposium*, 2009. 10.1109/ISDRS.2009.5378055

Duo Mao, M. A. Quevedo-Lopez, Harvey J. Stiegler, Husam N. Alshareef, Bruce E. Gnade; “Impact of Thickness and Thermal Treatment on the Materials and Electrical Properties of Poly(vinylidene fluoride-trifluoroethylene) Films for Non-Volatile Memory”, *MRS Fall 2009*, Boston.

Kurtis D. Cantley, Harvey J. Stiegler, Richard A. Chapman, and Eric M. Vogel, “Fabrication and SPICE Modeling of Hydrogenated Amorphous Silicon Nanowire Transistors for Artificial Neural Systems,” SRC/NRI SWAN Site Review, Austin, TX, September 2009. (Poster)

Kurtis D. Cantley, Harvey J. Stiegler, Richard A. Chapman, and Eric M. Vogel, “Fabrication and SPICE Modeling of Hydrogenated Amorphous Silicon Nanowire Transistors for Artificial Neural Systems,” *The Fifth International Nanotechnology Conference (INC5)*, Los Angeles, CA, May 2009. (Poster)

S. Gowrisanker, Y. Ai, H. Jia, M. A. Quevedo-Lopez, H. N. Alshareef, I. Trachtenberg, H. Stiegler, H. Edwards, R. Barnett, and B. E. Gnade, “Organic Thin-film Transistors with Low Threshold Voltage Variation on Low Temperature Substrates” *Electrochemical and Solid-State Letters*, 12(3) H50-H53 (2009).

Yuming Ai, Srinivas Gowrisanker, Huiping Jia, Isaac Trachtenberg, Eric Vogel, Robert M. Wallace, Bruce E. Gnade, Raymond Barnett, Harvey Stiegler, and Hal Edwards, “14 MHz Organic Diodes Fabricated Using Photolithographic Processes,” *Applied Physics Letters* **90**, 262105 (2007).

Harvey Stiegler, Ray Barnett, Hal Edwards, Yuming Ai, Huiping Jia, Srinivas Gowrisanker, and Bruce Gnade, “Organic Electronics for RFID and Other Applications,” Given at *Semiconductor Process Users’ Group*, University of Texas at Dallas, December 2006.

Harvey Stiegler, Ray Barnett, Hal Edwards, Yuming Ai, Huiping Jia, Srinivas Gowrisanker, and Bruce Gnade, “Organic Electronics for RFID and Other Applications,” *MSTD Technology Conference*, Texas Instruments, Dallas, Texas, October 2006.

John R. Brews, (rev. Harvey J. Stiegler), “The Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET),” in *The Electrical Engineering Handbook, Third Edition, Electronics, Power Electronics, Optoelectronics, Microwaves, Electromagnetics, and Radar*, ed. Richard C. Dorf (Boca Raton: CRC Press, 2006), pp. 3-39 – 3-52.

M. McConnell, B. Ashmore, R. Bussey, M. Gill, S.-W. Lin, D. McElroy, J. F. Schreck, P. Shah, H. Stiegler, P. Truong, A. L. Esquivel, J. Paterson, B. Riemenschneider, “An experimental 4 Mb flash EEPROM with sector erase,” *IEEE J. Solid-State Circuits*, vol. 26, no. 4, pp. 484-491, April 1991.

B. Riemenschneider, A. L. Esquivel, J. Paterson, M. Gill, S. Lin, J. Schreck, D. McElroy, P. Truong, R. Bussey, B. Ashmore, M. McConnell, H. Stiegler, P. Shah, “A process technology for a 5-volt only 4Mb flash EEPROM with an 8.6 UM2 cell,” *Symp. on VLSI Technology Digest of Technical Papers*, June 1990.

H. Stiegler, B. Ashmore, R. Bussey, M. Gill, S. Lin, M. McConnell, D. McElroy, J. Schreck, P. Shah, P. Truong, A. L. Esquivel, J. Paterson, B. Riemenschneider, "A 4Mb 5 V-only flash EEPROM with sector erase," Symp. on VLSI Circuits Digest of Technical Papers, June 1990.

W. F. Richardson, D. N. Anderson, B. W. Shen, E. J. Solowiej, I. C. Chen, C. W. Teng, H. P. McAdams, W. B. Holland, D. J. Redwine, H. J. Stiegler, T. H. Herndon, C. Price, T. Nasu, and W. K. Loh, "A Composed Trench Transistor (CTT) Cell for 16/64 MB dRAMS," Proc. Symp. VLSI Technology, Kyoto, Japan, May 1989.

Harvey J. Stiegler, "Electrical and Thermal Modeling of Electrostatic Discharge Protection Structures for Submicron VLSI." Ph.D. thesis, Rice University, 1989.

C. Duvvury, R. N. Rountree, H. J. Stiegler, T. Polgreen, and D. Corum, "ESD Phenomena in Graded Junction Devices," Proc. Int. Rel. Phys. Symp., Phoenix, Arizona, Apr. 1989.

R. N. Rountree, C. Duvvury, T. Maki, and H. Stiegler, "A Process-Tolerant Input Protection Circuit for Advanced CMOS Processes," Proc. EOS/ESD Symp., Anaheim, California, Sep. 1989.

Charvaka Duvvury, Donald J. Redwine, and Harvey J. Stiegler, "Leakage Current Degradation in N-MOSFET's Due to Hot-Electron Stress," IEEE Electron Device Letters, vol. 9, no. 11, pp. 579-581, Nov. 1988.

G. B. Shinn, F. Steigerwald, H. Stiegler, R. Sauerbrey, F. K. Tittel, and W. L. Wilson, Jr., "Excimer Laser Photoablation of Silicon," J. Vac. Sci. Technol. B., vol. 4, no. 6, pp. 1273-1277, Nov/Dec 1986.

H. Stiegler, W. L. Wilson, Jr., F. K. Tittel, N. Nishida, and W. L. Nighan, "Novel Approaches for the Development of High Energy Broadband Blue-Green Excimer Lasers", Proc. Int. Conf. on Lasers '85, Dec. 1985.

G. Marowsky, N. Nishida, H. Stiegler, F. K. Tittel, W. L. Wilson, Jr., Y. Zhu, and William L. Nighan, "Efficient Narrow Spectral Output in the Blue-Green Region from an Injection-Controlled Electron-Beam Excited XeF (C→A) Laser," Appl. Phys. Lett., vol. 47, no. 7, pp. 657-660, 1 October 1985.

Harvey J. Stiegler, "An Electron-Beam Controlled Discharge Laser on the C→A Transition of Xenon Fluoride," M.S. thesis, Rice University, 1985.

Daniel C. Guterman, Jeffrey Klaas, Gregory Armstrong, Joseph H. Neal, David J. McElroy, Paul Reed, William F. Richardson, Harvey Stiegler, and Isham H. Rimawi, "X-Series Approach to High Density 128K and High Speed 32K EPROMs," ISSCC Digest of Technical Papers, 1980.