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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/888,667	09/23/2008	7427888	4591-380	4240

20575 7590 09/03/2008

MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 69 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Pyung-Moon Zhang, Gyeonggi-do, KOREA, REPUBLIC OF;
Seung-Keun Lee, Gyeonggi-do, KOREA, REPUBLIC OF;

IR103 (Rev. 11/05)

Electronic Patent Application Fee Transmittal

Application Number:	10888667
Filing Date:	08-Jul-2004
Title of Invention:	CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE
First Named Inventor/Applicant Name:	Pyung-Moon Zhang
Filer:	Hosoon Lee/Stormi Davis
Attorney Docket Number:	4591-380

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1440	1440
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1740**

Electronic Acknowledgement Receipt

EFS ID:	3784895
Application Number:	10888667
International Application Number:	
Confirmation Number:	4240
Title of Invention:	CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE
First Named Inventor/Applicant Name:	Pyung-Moon Zhang
Customer Number:	20575
Filer:	Hosoon Lee/Stormi Davis
Filer Authorized By:	Hosoon Lee
Attorney Docket Number:	4591-380
Receipt Date:	14-AUG-2008
Filing Date:	08-JUL-2004
Time Stamp:	18:56:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		85B.pdf	217585 9327bd46b4a47db2b360352c18a3aacd4be30e9d	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Post Allowance Communication - Incoming	1	1
	Issue Fee Payment (PTO-85B)	2	2

Warnings:					
Information:					
2	Fee Worksheet (PTO-06)	fee-info.pdf	8292 eab9d8457f26d0f37bc0706916bb51c3870f9469	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	225877		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION
Docket No.: 4591-380
Client Ref. No.: ID13095-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Pyung-Moon ZHANG et al.		
Serial No.:	10/888,667	Examiner:	Hiltunen, Thomas J.
Filed:	July 8, 2004	Group Art Unit:	2816
Confirmation No.:	4240		
For:	CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE		
Date:	August 14, 2008		

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPLICANT'S COMMENTS ON EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

The Examiner's statement of reasons for allowance includes language which does not appear in the claims and should not be interpreted as imparting any limitations not recited therein.

Claims 3-5, 23-28 and 30-32 recite features which are neither shown nor suggested by the cited references, and are therefore, independently allowable.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Joseph S. Makuch
Reg. No. 39,286

MARGER JOHNSON & McCOLLOM, P.C.
210 SW Morrison Street, Suite 400
Portland, OR 97204
503-222-3613

PART B - FEE(S) TRANSMITTAL

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PTO/SB/17 (10-07)
Approved for use through 08/31/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

AUG 14 2008

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

20575 7590 05/16/2008

MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

08/15/2008 SSANDAR1 00000009 131703 10888667

01 FC:1501 1440.00 DA
02 FC:1504 300.00 DA

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/888,667	07/08/2004	Pyung-Moon Zhang	4591-380	4240

TITLE OF INVENTION: CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE

The PTO did not receive the following listed item(s) credit card form

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1440	$300	$0	$1740	08/18/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
HILTUNEN, THOMAS J	2816	327-536000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 MARGER JOHNSON &
2 McCOLLOM, P.C.
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Samsung Electronics Co., Ltd.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Suwon-si, Gyeonggi-do, Republic of Korea

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☒ Payment ~~by credit card. Form PTO-2038 is attached.~~ made electronically.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 13-1703 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date August 14, 2008

Typed or printed name Joseph S. Makuch Registration No. 39,286

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

20575 7590 05/16/2008

MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

EXAMINER	
HILTUNEN, THOMAS J	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/16/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/888,667	07/08/2004	Pyung-Moon Zhang	4591-380	4240

TITLE OF INVENTION: CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1440	$300	$0	$1740	08/18/2008

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/888,667	07/08/2004	Pyung-Moon Zhang	4591-380	4240

TITLE OF INVENTION: CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1440	$300	$0	$1740	08/18/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
HILTUNEN, THOMAS J	2816	327-536000

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2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

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❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/888,667	07/08/2004	Pyung-Moon Zhang	4591-380	4240

20575 7590 05/16/2008

MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

EXAMINER	
HILTUNEN, THOMAS J	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/16/2008

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 69 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 69 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Notice of Allowability	Application No.	Applicant(s)	
	10/888,667	ZHANG ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed 30 April 2008*.

2. ☒ The allowed claim(s) is/are *1,3-5,19 and 23-32*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Reasons For Allowance

With respect to claims 1, 3-5 and 19 and 23-28, there is no cited art that discloses the specific charge pump composed of a plurality of charge pump parts, a selector and a detector connected and composed as recited, wherein the detector further comprises a fist and second high voltage NMOS transistor coupled to the supply voltage and the high voltage, respectively, and the first node of the detector as recited in claims 1 and 19.

With respect to claims 29-32, there is no cited art that discloses the specific charge pump composed of a plurality of charge pump parts, a selector and a detector connected and composed as recited, wherein the selector further comprises a "first inverter", "first and second high voltage NMOS transistors", a "second inverter" and "third and fourth high voltage NMOS transistors" connected as recited in claim 29.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on M-F 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571)272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TH /N. Drew Richards/
May 13, 2008 Supervisory Patent Examiner, Art Unit 2816

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10888667	ZHANG ET AL.
	Examiner	Art Unit
	Thomas J Hiltunen	2816

ORIGINAL		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
327	536	G	0	5	F	1 / 10 (2006.01.01)					

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
363	60				

/Thomas J Hiltunen/ (Assistant Examiner)	05/13/08 (Date)		Total Claims Allowed: 15	
/N. Drew Richards/ (Primary Examiner)		5/14/08 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 4,7

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4	"5912564".pn. "5272393".pn. "5828620".pn. "5483486".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/05/13 09:23
L3	111	327/536,537,143,60,63,82.ccls. and @pd>="20080123"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/05/13 09:34
L4	21	363/59-60,63.ccls. and @pd>="20080123"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/05/13 09:38
L5	9	4 not 3	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/05/13 09:38
L6	80	365/189.09.ccls. and @pd>="20080123"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/05/13 09:38
L7	79	6 not (4 3)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/05/13 09:39
L8	4676993	(mux multiplexer multiplexor select$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/05/13 09:41
L9	1677466	(output voltage supply vpp vbb level) with (sens$4 detect$4 monitor$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/05/13 09:42
L10	118010	(charge voltage current) near2 (pump $4 doubl$4 multipl$4 multiplication)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/05/13 09:42
L11	4472	8 same 9 same 10	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/05/13 09:43
L12	98031	(pll dlll delay adj lock$4 adj loop phase adj lock$4 adj loop)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/05/13 09:44
L14	3361	11 not 12	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/05/13 09:44
L15	821	14 and inverter	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/05/13 09:47

L21	2380	14 not 15	US-PGPUB; USPAT; USOCR	OR	ON	2008/05/13 10:39
L22	99	21 and (precharge pre adj charge pre $1charge)	US-PGPUB; USPAT; USOCR	OR	ON	2008/05/13 10:39
L23	2281	21 not 22	US-PGPUB; USPAT; USOCR	OR	ON	2008/05/13 10:41
L24	26	23 and 9 with (nmos n adj mos n adj fet nfet nmosfet n adj mosfet)	US-PGPUB; USPAT; USOCR	OR	ON	2008/05/13 10:42
L25	2255	23 not 24	US-PGPUB; USPAT; USOCR	OR	ON	2008/05/13 10:43
L26	17	25 and 9 same (nmos n adj mos n adj fet nfet nmosfet n adj mosfet)	US-PGPUB; USPAT; USOCR	OR	ON	2008/05/13 10:43
L27	2238	25 not 26	US-PGPUB; USPAT; USOCR	OR	ON	2008/05/13 10:44
L28	1401	8 with 9 and 27	US-PGPUB; USPAT; USOCR	OR	ON	2008/05/13 10:45
L29	986	(8 and 9 and 10).clm.	US-PGPUB	OR	ON	2008/05/13 11:16
L33	530499	(zhang lee).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/13 11:36
L35	2688	33 and 10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/13 11:36
L36	1932	35 and (sens$4 detect$4 monitor$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/05/13 11:37
L37	1480	36 and 8	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/05/13 11:37
L39	1422	37 not 29	US-PGPUB; USPAT; USOCR	OR	ON	2008/05/13 11:40

5/13/2008 1:23:21 PM
C:\Documents and Settings\thiltunen\My Documents\EAST\Workspaces\10888667.5.wsp

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BIB DATA SHEET

CONFIRMATION NO. 4240

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/888,667	07/08/2004 RULE	327	2816	4591-380

APPLICANTS

Pyung-Moon Zhang, Gyeonggi-do, KOREA, REPUBLIC OF;
Seung-Keun Lee, Gyeonggi-do, KOREA, REPUBLIC OF;

**** CONTINUING DATA **************************

**** FOREIGN APPLICATIONS **************************

REPUBLIC OF KOREA 2003-46799 07/10/2003

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

08/30/2004

Foreign Priority claimed	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☑ Yes ☐ No	☐	KOREA, REPUBLIC OF	7	18	3
35 USC 119(a-d) conditions met ☑ Yes ☐ No					
Verified and Acknowledged /THOMAS J HILTUNEN/ Examiner's Signature	Initials				

ADDRESS

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210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204
UNITED STATES

TITLE

Charge pump circuit operating responsive to a mode

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
1370	No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10888667	ZHANG ET AL.
	Examiner	Art Unit
	Thomas J Hiltunen	2816

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	01/25/2008	05/13/2008							
1	1	✓	=							
	2	O	-							
2	3	O	=							
3	4	O	=							
4	5	O	=							
	6	-	-							
	7	-	-							
	8	-	-							
	9	-	-							
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	16	-	-							
	17	-	-							
	18	✓	-							
6	19	✓	=							
	20	✓	-							
	21	✓	-							
	22	O	-							
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9	25	O	=							
10	26	O	=							
11	27	O	=							
5	28	✓	=							
12	29	O	=							
13	30	O	=							
14	31	O	=							
15	32	O	=							

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2816

PATENT APPLICATION
Docket No.: 4591-380
Client Ref. No.: ID13095-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Pyung-Moon ZHANG et al.		
Serial No.:	10/888,667	Examiner:	Hiltunen, Thomas J.
Filed:	July 8, 2004	Group Art Unit:	2816
Confirmation No.:	4240		
For:	CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE		

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

OK TO ENTER: /T.H./
05/13/2008

SUPPLEMENTAL AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR 1.116

Responsive to the Final Office Action, Paper No. 20080125, dated January 31, 2008, and the Advisory Action, Paper No. 20080410, dated April 11, 2008, please amend the application as follows.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 7 of this paper.

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/888,667	ZHANG ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

SEARCHED			
Class	Subclass	Date	Examiner
327	536,537 143,82,60, 63	11/9/2005	TH
363	60	11/9/2005	TH
Updated	above	4/6/2006	TH
Updated	above	9/27/2006	TH
363	63	9/28/2006	TH
Updated	above	3/1/2007	TH
363	59	3/1/2007	TH
365	189.09	3/1/2007	TH
Updated	above	1/23/2008	TH
Updated	above	5/13/2008	TH

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
See attached EAST text search		5/13/2008	TH

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
See attached EAST text search	11/14/2005	TH
See attached EAST text search	4/10/2006	TH
See attached EAST text search	9/28/2006	TH
See attached EAST text search	3/7/2007	TH
See attached EAST text search	1/25/2008	TH
See attached EAST text search	5/13/2008	TH

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2816

PATENT APPLICATION
Docket No.: 4591-380
Client Ref. No.: ID13095-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Pyung-Moon ZHANG et al.		
Serial No.:	10/888,667	Examiner:	Hiltunen, Thomas J.
Filed:	July 8, 2004	Group Art Unit:	2816
Confirmation No.:	4240		
For:	CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE		

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR 1.116

Responsive to the Final Office Action, Paper No. 20080125, dated January 31, 2008, and the Advisory Action, Paper No. 20080410, dated April 11, 2008, please amend the application as follows.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 7 of this paper.

IN THE CLAIMS

1. (Currently amended) A charge pump circuit comprising:

a charge pump block including a plurality of charge pump parts, each charge pump part including at least one pre-charge device;

a selector circuit coupled to the at least one pre-charge device of each of the charge pump parts, the selector circuit being structured to receive a supply voltage and a high voltage; and

a detector circuit comprising a first node, a second node, a high voltage inverter, and a low voltage inverter, the high voltage inverter being coupled to the low voltage inverter, the first node being coupled to the supply voltage and the high voltage, the second node being coupled to an input of the high voltage inverter, the second node having a voltage high enough to invert an output of the high voltage inverter responsive to the high voltage being higher than the supply voltage, the low voltage inverter being configured to provide a detect signal to the selector circuit responsive to the inverted output of the high voltage inverter[[.]],

wherein the detector circuit further comprises a first high voltage NMOS transistor coupled between the supply voltage and the first node and a second high voltage NMOS transistor coupled between the high voltage and the first node, the first node having a voltage of one of (a) a difference between the supply voltage and a threshold voltage of the first high voltage NMOS transistor and (b) a difference between the high voltage and a threshold voltage of the second high voltage NMOS transistor.

2. (Cancelled)

3. (Currently amended) The charge pump circuit of claim[[2]] 1, wherein the detector circuit further comprises a high voltage PMOS transistor coupled between the first node and the second node, the high voltage PMOS transistor having substantially an off state responsive to the first node having the voltage corresponding to the difference between the supply voltage and the threshold voltage of the first high voltage NMOS transistor, the detect signal indicating a general mode of operation responsive to the PMOS transistor having the off state.

4. (Currently amended) The charge pump circuit of claim[[2]] 1, wherein the second node has a high enough voltage to invert the output of the high voltage inverter responsive to the first node having the voltage corresponding to the difference between the high voltage and the threshold voltage of the second high voltage NMOS transistor, the detect signal indicating a test mode of operation responsive to the high enough voltage.

5. (Previously presented) The charge pump circuit of claim 1,

wherein the charge pump block is configured to generate an output voltage on an output terminal, the output terminal being coupled to the at least one pre-charge device of each of the plurality of charge pump parts; and

wherein the selector circuit further comprises:

a first inverter configured to receive the detect signal, an output terminal of the first inverter being coupled to a first node, the first node being coupled to gate terminals of first and second high voltage NMOS transistors;

a second inverter, an input terminal of the second inverter being coupled to the first node, an output terminal of the second inverter being coupled to a second node, the second node being coupled to gate terminals of third and fourth high voltage NMOS transistors;

at least one high voltage PMOS transistor coupled to the supply voltage, the at least one high voltage PMOS transistor having a gate terminal coupled to drain terminals of the first and third high voltage NMOS transistors;

at least another high voltage PMOS transistor coupled to the high voltage, the at least another high voltage PMOS transistor having a gate terminal coupled to drain terminals of the second and fourth high voltage NMOS transistors; and

an output terminal coupled to the high voltage PMOS transistors, wherein the detect signal controls a state of the first, second, third, and fourth high voltage NMOS transistors, and the high voltage NMOS transistors control a state of the high voltage PMOS transistors, the output terminal configured to transmit one of the supply voltage and the high voltage responsive to the state of the high voltage PMOS transistors.

6-18. (Cancelled)

19. (Currently amended) A charge pump circuit comprising:

a charge pump block including a plurality of charge pump parts, each charge pump part including at least one pre-charge device;[[and]]

a selector circuit coupled to the at least one pre-charge device of each of the charge pump parts, the selector circuit being structured to receive a supply voltage and a high voltage; and

a detector circuit comprising a first node, a second node, a high voltage inverter, and a low voltage inverter, the high voltage inverter being coupled to the low voltage inverter, the first node being coupled to the supply voltage and the high voltage, the second node being coupled to an input of the high voltage inverter,

wherein the second node has a voltage high enough to invert an output of the high voltage inverter responsive to the high voltage being higher than the supply voltage, the low voltage inverter being configured to provide a detect signal to the selector circuit responsive to the inverted output of the high voltage inverter, and

wherein the detector circuit further comprises a first high voltage NMOS transistor coupled between the supply voltage and the first node and a second high voltage NMOS transistor coupled between the high voltage and the first node.

20-22. (Cancelled)

23. (Currently amended) The charge pump circuit of claim[[22]] 19, wherein the first node has a voltage of one of (a) a difference between the supply voltage and a threshold voltage of the first high voltage NMOS transistor and (b) a difference between the high voltage and a threshold voltage of the second high voltage NMOS transistor.

24. (Previously presented) The charge pump circuit of claim 23, wherein the detector circuit further comprises a high voltage PMOS transistor coupled between the first node and the second node, the high voltage PMOS transistor having substantially an off state responsive to the first node having the voltage corresponding to the difference between the supply voltage and the threshold voltage of the first high voltage NMOS transistor.

25. (Previously presented) The charge pump circuit of claim 24, wherein the detect signal indicates a general mode of operation responsive to the PMOS transistor having the off state.

26. (Previously presented) The charge pump circuit of claim 23 wherein the second node has a high enough voltage to invert the output of the high voltage inverter responsive to the first node having the voltage corresponding to the difference between the high voltage and the threshold voltage of the second high voltage NMOS transistor.

27. (Previously presented) The charge pump circuit of claim 26, wherein the detect signal indicates a test mode of operation responsive to the high enough voltage.

28. (Previously presented) The charge pump circuit of claim 1, wherein the charge pump block is configured to generate an output voltage on an output terminal, the output terminal being coupled to the at least one pre-charge device of each of the plurality of charge pump parts.

29. (Currently amended) [[The]]A charge pump circuit ~~of claim 1, wherein the selector circuit further comprises~~, comprising:

a charge pump block including a plurality of charge pump parts, each charge pump part including at least one pre-charge device;

a selector circuit coupled to the at least one pre-charge device of each of the charge pump parts, the selector circuit being structured to receive a supply voltage and a high voltage; and

a detector circuit comprising a first node, a second node, a high voltage inverter, and a low voltage inverter, the high voltage inverter being coupled to the low voltage inverter, the first node being coupled to the supply voltage and the high voltage, the second node being coupled to an input of the high voltage inverter, the second node having a voltage high enough to invert an output of the high voltage inverter responsive to the high voltage being higher than the supply voltage, the low voltage inverter being configured to provide a detect signal to the selector circuit responsive to the inverted output of the high voltage inverter, wherein the selector circuit further comprises:

a first inverter configured to receive the detect signal, an output terminal of the first inverter being coupled to a first node, the first node being coupled to gate terminals of first and second high voltage NMOS transistors; and

a second inverter, an input terminal of the second inverter being coupled to the first node, an output terminal of the second inverter being coupled to a second node, the second node being coupled to gate terminals of third and fourth high voltage NMOS transistors.

30. (Previously presented) The charge pump circuit of claim 29, wherein the selector circuit further comprises:

at least one high voltage PMOS transistor coupled to the supply voltage, the at least one high voltage PMOS transistor having a gate terminal coupled to drain terminals of the first and third high voltage NMOS transistors.

31. (Previously presented) The charge pump circuit of claim 29, wherein the selector circuit further comprises:

at least another high voltage PMOS transistor coupled to the high voltage, the at least another high voltage PMOS transistor having a gate terminal coupled to drain terminals of the second and fourth high voltage NMOS transistors.

32. (Previously presented) The charge pump circuit of claim 31, wherein the selector circuit further comprises:

an output terminal coupled to the high voltage PMOS transistors,

wherein the detect signal controls a state of the first, second, third, and fourth high voltage NMOS transistors,

wherein the high voltage NMOS transistors control a state of the high voltage PMOS transistors, and

wherein the output terminal is configured to transmit one of the supply voltage and the high voltage responsive to the state of the high voltage PMOS transistors.

REMARKS

Claims 1-5 and 18-32 are pending in the application.

Claims 1, 18-21 and 28 are rejected.

Claims 2-5, 22-27 and 29-32 are objected to.

Claim 19 stands rejected under 35 U.S.C. 102(b).

Claims 1 and 28 stand rejected under 35 U.S.C. 103(a).

Claim 18 stands rejected under 35 U.S.C. 103(a).

Claims 20 and 21 stand rejected under 35 U.S.C. 103(a).

Claims 1, 3, 4, 19, 23 and 29 have been amended.

Claims 2, 18 and 20-22 have been cancelled.

No new matter has been added.

The Applicant requests reconsideration and allowance of claims 1, 3-5, 19 and 23-32 in light of the following amendments and remarks.

Allowable Subject Matter

Claims 2-5, 22-27 and 29-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Applicant thanks Examiner Hiltunen for acknowledging the patentable subject matter of these claims.

In accordance with the Examiner's indication of allowability with reference to claims 2-5, 22-27, and 29-32, the Applicant has amended the independent claims to include the limitations of at least one of the allowable claims including all of the limitations of the base claim and any intervening claims. Therefore, in all respects, this case is now in condition for allowance.

Specifically, claim 1 has been amended to include the limitations of allowable claim 2, including all of the limitations of the base claim. In this instance, there are no intervening claims. In other words, claim 1 is in essence claim 2 rewritten in independent form including all of the limitations of the base claim. Claim 2 has correspondingly been cancelled. Claims 3 and 4 have been amended to depend from claim 1. As such, claim 1 is in proper form for allowance, as are dependent claims 3-5 and 28.

Claim 18 has been cancelled.

Claim 19 has been amended to include all of the limitations of allowable claim 22, including all of the limitations of intervening claims 20 and 21, and including all of the limitations of the base claim 19. Claims 20-22 have correspondingly been cancelled. Claim 23 has been amended to depend from claim 19. Thus, claim 19 is now in proper form for allowance, as are dependent claims 23-27.

Claim 29, which was also indicated to be allowable, has been rewritten in independent form including all of the limitations of the base claim and any intervening claims. Specifically, claim 29 now includes all of the limitations of base claim 1. Thus, claim 29 is in proper form for allowance, as are dependent claims 30-32.

Claim Rejections

Claims 1 and 28 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kai et al. (U.S. Patent No. 5,912,564), hereinafter "Kai" in view of Suwa (Japanese Publication No. 2001-35193), hereinafter "Suwa."

Claim 18 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Horiguchi et al. (U.S. Patent No. 5,272,393), hereinafter "Horiguchi" in view of Foss et al. (U.S. Patent No. 5,828,620), hereinafter "Foss."

Claims 20 and 21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kai et al. (U.S. Patent No. 5,912,564) in view of Suwa (Japanese Publication No. 2001-35193).

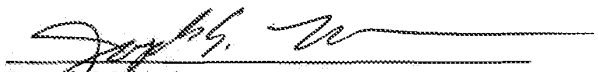
Claim 19 is rejected under 35 U.S.C. 102(b) as being anticipated by Kai et al. (U.S. Patent No. 5,912,564).

While the Applicant respectfully traverses the rejections, the Applicant has nonetheless amended the claims in accordance with the Examiner's indication of allowable subject matter, such that the independent claims now include limitations of the allowable claims including all of the limitations of the base claim and any intervening claims. In view of these amendments, this case should now be in condition for allowance.

For the foregoing reasons, reconsideration and allowance of claims 1, 3-5, 19 and 23-32 of the application as amended is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



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210 SW Morrison Street, Suite 400
Portland, OR 97204
503-222-3613
Customer No. 20575

Electronic Acknowledgement Receipt

EFS ID:	3236613
Application Number:	10888667
International Application Number:	
Confirmation Number:	4240
Title of Invention:	Charge pump circuit operating responsive to a mode
First Named Inventor/Applicant Name:	Pyung-Moon Zhang
Customer Number:	20575
Filer:	Hosoon Lee/Stormi Davis
Filer Authorized By:	Hosoon Lee
Attorney Docket Number:	4591-380
Receipt Date:	30-APR-2008
Filing Date:	08-JUL-2004
Time Stamp:	19:01:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		4591-380h.pdf	704712 c70f7740a5e3f3872316e6464821b3d8947af164	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Supplemental Response or Supplemental Amendment	2	2
	Claims	3	7
	Applicant Arguments/Remarks Made in an Amendment	8	10
Warnings:			
Information:			
	Total Files Size (in bytes):	704712	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

MISCELLANEOUS LETTER

REGARDING PAYMENT OF FEES AND EXTENSION OF TIME

	Claims Remaining After Amendment	Highest Number Previously Paid For	Present Extra Claims
Total Claims	15	20-20	0
Independent Claims	3	5-3	0

☒ Applicant petitions the Commissioner to extend the time for response (if applicable).

☒ Payment of fees is made via electronic filing system authorizing credit card payments for the extra claims and/or Petition.

☒ Applicant is paying with a Visa card; however, Applicant requests that any deficiency or overpayment be charged or credited to deposit account number 13-1703.

Respectfully submitted,

Customer No. 20575

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Date: April 30, 2008

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PTO/SB/06 (07-06)
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
10/888,667	07/08/2004	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
AMENDMENT	04/30/2008	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 15	Minus	** 20	= 0	X $ =		OR	X $50=	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***5	= 0	X $ =		OR	X $210=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/JULIET MCMILLAN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2816

PATENT APPLICATION
Docket No.: 4591-380
Client Ref. No.: ID13095-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Pyung-Moon ZHANG et al.		
Serial No.:	10/888,667	Examiner:	Hiltunen, Thomas J.
Filed:	July 8, 2004	Group Art Unit:	2816
Confirmation No.:	4240		
For:	CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE		

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DO NOT ENTER: /T.H./
04/10/2008

AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR 1.116

Responsive to the Final Office Action, Paper No. 20080125, dated January 31, 2008, please amend the application as follows.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 8 of this paper.

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/888,667	07/08/2004	Pyung-Moon Zhang	4591-380	4240

20575 7590 04/11/2008

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EXAMINER	
HILTUNEN, THOMAS J	
ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
04/11/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/888,667	**Applicant(s)** ZHANG ET AL.	
	Examiner Thomas J. Hiltunen	**Art Unit** 2816	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 31 March 2008 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☒ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: *claims 2 and 22 were previously indicated allowable if the claims were rewritten in independent form including all of the limiations of the base claims. However, claims 1,18, 19, 29, and 30 currently do not contain all of the previous limitions of claims 2 and 22. Therefore, the above amendment requires further search and consideration and does not simplify matters for appeal* . (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: *2-5,22-27 and 29-32*.
   Claim(s) rejected: *1,18-21 and 28*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/N. Drew Richards/
Supervisory Patent Examiner, Art Unit 2816

U.S. Patent and Trademark Office

EX1007 / Page 37 of 375
Western Digital Technologies, Inc.

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2816

PATENT APPLICATION
Docket No.: 4591-380
Client Ref. No.: ID13095-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR 1.116

Responsive to the Final Office Action, Paper No. 20080125, dated January 31, 2008, please amend the application as follows.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 8 of this paper.

IN THE CLAIMS

1. (Currently amended) A charge pump circuit comprising:

a charge pump block including a plurality of charge pump parts, each charge pump part including at least one pre-charge device;

a selector circuit coupled to the at least one pre-charge device of each of the charge pump parts, the selector circuit being structured to receive a supply voltage and a high voltage; and

a detector circuit comprising a first node, a second node, a high voltage inverter, and a low voltage inverter, the high voltage inverter being coupled to the low voltage inverter, the first node being coupled to the supply voltage and the high voltage, the second node being coupled to an input of the high voltage inverter, the second node having a voltage high enough to invert an output of the high voltage inverter responsive to the high voltage being higher than the supply voltage, the low voltage inverter being configured to provide a detect signal to the selector circuit responsive to the inverted output of the high voltage inverter[[.]],

wherein the detector circuit further comprises a first high voltage NMOS transistor coupled between the supply voltage and the first node and a second high voltage NMOS transistor coupled between the high voltage and the first node.

2. (Currently amended) The charge pump circuit of claim 1, wherein ~~the detector circuit further comprises a first high voltage NMOS transistor coupled between the supply voltage and the first node and a second high voltage NMOS transistor coupled between the high voltage and the first node,~~ the first node ~~having~~ has a voltage of one of (a) a difference between the supply voltage and a threshold voltage of the first high voltage NMOS transistor and (b) a difference between the high voltage and a threshold voltage of the second high voltage NMOS transistor.

3. (Previously presented) The charge pump circuit of claim 2, wherein the detector circuit further comprises a high voltage PMOS transistor coupled between the first node and the second node, the high voltage PMOS transistor having substantially an off state responsive to the first node having the voltage corresponding to the difference between the supply voltage and the threshold voltage of the first high voltage NMOS transistor, the detect signal indicating a general mode of operation responsive to the PMOS transistor having the off state.

4. (Previously presented) The charge pump circuit of claim 2, wherein the second node has a high enough voltage to invert the output of the high voltage inverter responsive to the first node having the voltage corresponding to the difference between the high voltage and the threshold voltage of the second high voltage NMOS transistor, the detect signal indicating a test mode of operation responsive to the high enough voltage.

5. (Previously presented) The charge pump circuit of claim 1,

wherein the charge pump block is configured to generate an output voltage on an output terminal, the output terminal being coupled to the at least one pre-charge device of each of the plurality of charge pump parts; and

wherein the selector circuit further comprises:

a first inverter configured to receive the detect signal, an output terminal of the first inverter being coupled to a first node, the first node being coupled to gate terminals of first and second high voltage NMOS transistors;

a second inverter, an input terminal of the second inverter being coupled to the first node, an output terminal of the second inverter being coupled to a second node, the second node being coupled to gate terminals of third and fourth high voltage NMOS transistors;

at least one high voltage PMOS transistor coupled to the supply voltage, the at least one high voltage PMOS transistor having a gate terminal coupled to drain terminals of the first and third high voltage NMOS transistors;

at least another high voltage PMOS transistor coupled to the high voltage, the at least another high voltage PMOS transistor having a gate terminal coupled to drain terminals of the second and fourth high voltage NMOS transistors; and

an output terminal coupled to the high voltage PMOS transistors, wherein the detect signal controls a state of the first, second, third, and fourth high voltage NMOS transistors, and the high voltage NMOS transistors control a state of the high voltage PMOS transistors, the output terminal configured to transmit one of the supply voltage and the high voltage responsive to the state of the high voltage PMOS transistors.

6-17. (Cancelled)

18. (Currently amended) A charge pump circuit comprising:

a charge pump block including at least one charge pump part;

a voltage level sensing block to sense a level of an output voltage and generate a level sensing signal responsive thereto;

an oscillator to generate a pulse signal responsive to the level sensing signal;

a detector to generate a detection signal responsive to a high voltage and a power voltage, the detector comprising:

a first high voltage NMOS transistor coupled between the power voltage and a node; and

a second high voltage NMOS transistor coupled between the high voltage and the node, the node having a voltage of one of (a) a difference between the power voltage and a threshold voltage of the first high voltage NMOS transistor and (b) a difference between the high voltage and a threshold voltage of the second high voltage NMOS transistor; and

a selector to provide one of the high voltage and [[a]]the power voltage responsive to the detection signal to the charge pump block[[;]].

~~where the detector compares the high voltage to the power voltage; and~~

~~where the output of the detector is high responsive to the high voltage being higher than the power voltage.~~

19. (Currently amended) A charge pump circuit comprising:

a charge pump block including a plurality of charge pump parts, each charge pump part including at least one pre-charge device;[[and]]

a selector circuit coupled to the at least one pre-charge device of each of the charge pump parts, the selector circuit being structured to receive a supply voltage and a high voltage[[.]]; and

a detector circuit comprising: a first node, a second node, a high voltage inverter, a low voltage inverter, and a high voltage NMOS transistor, the high voltage NMOS transistor being coupled between the supply voltage and the first node, the high voltage inverter being coupled to the low voltage inverter, the first node being coupled to the supply voltage and the high voltage, and the second node being coupled to an input of the high voltage inverter.

20. (Cancelled)

21. (Currently amended) The charge pump circuit of claim[[20]] 19, wherein the second node has a voltage high enough to invert an output of the high voltage inverter responsive to the high voltage being higher than the supply voltage, the low voltage inverter being configured to provide a detect signal to the selector circuit responsive to the inverted output of the high voltage inverter.

22. (Currently amended) The charge pump circuit of claim 21, wherein the detector circuit further comprises ~~a first high voltage NMOS transistor coupled between the supply voltage and the first node and~~ a second high voltage NMOS transistor coupled between the high voltage and the first node.

23. (Previously presented) The charge pump circuit of claim 22, wherein the first node has a voltage of one of (a) a difference between the supply voltage and a threshold voltage of the first high voltage NMOS transistor and (b) a difference between the high voltage and a threshold voltage of the second high voltage NMOS transistor.

24. (Previously presented) The charge pump circuit of claim 23, wherein the detector circuit further comprises a high voltage PMOS transistor coupled between the first node and the second node, the high voltage PMOS transistor having substantially an off state responsive to the first node having the voltage corresponding to the difference between the supply voltage and the threshold voltage of the first high voltage NMOS transistor.

25. (Previously presented) The charge pump circuit of claim 24, wherein the detect signal indicates a general mode of operation responsive to the PMOS transistor having the off state.

26. (Previously presented) The charge pump circuit of claim 23 wherein the second node has a high enough voltage to invert the output of the high voltage inverter responsive to the first node having the voltage corresponding to the difference between the high voltage and the threshold voltage of the second high voltage NMOS transistor.

27. (Previously presented) The charge pump circuit of claim 26, wherein the detect signal indicates a test mode of operation responsive to the high enough voltage.

28. (Previously presented) The charge pump circuit of claim 1, wherein the charge pump block is configured to generate an output voltage on an output terminal, the output terminal being coupled to the at least one pre-charge device of each of the plurality of charge pump parts.

29. (Currently amended) [[The]]A charge pump circuit ~~of claim 1, wherein the selector circuit further comprises~~ comprising:

a charge pump block including a plurality of charge pump parts, each charge pump part including at least one pre-charge device; and

a selector circuit coupled to the at least one pre-charge device of each of the charge pump parts, the selector circuit being structured to receive a supply voltage and a high voltage, wherein the selector circuit comprises:

an [[first]]inverter configured to receive the detect signal, an output terminal of the [[first]]inverter being coupled to a [[first]]node, the [[first]]node being coupled to gate terminals of first and second high voltage NMOS transistors[[; and]].

~~a second inverter, an input terminal of the second inverter being coupled to the first node, an output terminal of the second inverter being coupled to a second node, the second node being coupled to gate terminals of third and fourth high voltage NMOS transistors.~~

30. (Currently amended) The charge pump circuit of claim 29, wherein the inverter comprises a first inverter, the node comprises a first node, and the selector circuit further comprises:

a second inverter, an input terminal of the second inverter being coupled to the first node, an output terminal of the second inverter being coupled to a second node, the second node being coupled to gate terminals of third and fourth high voltage NMOS transistors; and

at least one high voltage PMOS transistor coupled to the supply voltage, the at least one high voltage PMOS transistor having a gate terminal coupled to drain terminals of the first and third high voltage NMOS transistors.

31. (Previously presented) The charge pump circuit of claim 29, wherein the selector circuit further comprises:

at least another high voltage PMOS transistor coupled to the high voltage, the at least another high voltage PMOS transistor having a gate terminal coupled to drain terminals of the second and fourth high voltage NMOS transistors.

32. (Previously presented) The charge pump circuit of claim 31, wherein the selector circuit further comprises:

an output terminal coupled to the high voltage PMOS transistors,

wherein the detect signal controls a state of the first, second, third, and fourth high voltage NMOS transistors,

wherein the high voltage NMOS transistors control a state of the high voltage PMOS transistors, and

wherein the output terminal is configured to transmit one of the supply voltage and the high voltage responsive to the state of the high voltage PMOS transistors.

REMARKS

Claims 1-5 and 18-32 are pending in the application.

Claims 1, 18-21 and 28 are rejected.

Claims 2-5, 21-27 and 29-32 are objected to.

Claim 19 stands rejected under 35 U.S.C. 102(b).

Claims 1 and 28 stand rejected under 35 U.S.C. 103(a).

Claim 18 stands rejected under 35 U.S.C. 103(a).

Claims 20 and 21 stand rejected under 35 U.S.C. 103(a).

Claims 1-2, 18-19, 21-22 and 29-30 have been amended.

Claim 20 has been cancelled.

No new matter has been added.

The Applicant requests reconsideration and allowance of claims 1-5, 18-19 and 21-32 in light of the following amendments and remarks.

Claim Rejections – 35 U.S.C. § 103

Claims 1 and 28 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kai et al. (U.S. Patent No. 5,912,564), hereinafter "Kai" in view of Suwa (Japanese Publication No. 2001-35193), hereinafter "Suwa." The Applicant traverses the rejection.

Claim 1 has been amended to set forth "a charge pump block including a plurality of charge pump parts, each charge pump part including at least one pre-charge device; a selector circuit coupled to the at least one pre-charge device of each of the charge pump parts, the selector circuit being structured to receive a supply voltage and a high voltage; and a detector circuit comprising a first node, a second node, a high voltage inverter, and a low voltage inverter, the high voltage inverter being coupled to the low voltage inverter, the first node being coupled to the supply voltage and the high voltage, the second node being coupled to an input of the high voltage inverter, the second node having a voltage high enough to invert an output of the high voltage inverter responsive to the high voltage being higher than the supply voltage, the low voltage inverter being configured to provide a detect signal to the selector circuit responsive to the inverted output of the high voltage inverter, wherein the detector circuit further comprises a first high voltage NMOS transistor coupled between the supply voltage and the first node and a second high voltage NMOS transistor coupled between the high voltage and the first node."

Specifically, elements of claim 2 including the high voltage NMOS transistors and their respective arrangement, which were indicated to be allowable by the Examiner, are now included in claim 1. The corresponding elements have been deleted from claim 2. Based at least on the Examiner's indication that no cited art discloses the specific detector circuit having first and second high voltage NMOS transistors coupled between the supply voltage and the high voltage, respectively, the Applicant submits that claim 1 is now patentable under 35 U.S.C. 103(a) over Kai and Suwa, as are dependent claims 2-5 and 28.

Claim 18 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Horiguchi et al. (U.S. Patent No. 5,272,393), hereinafter "Horiguchi" in view of Foss et al. (U.S. Patent No. 5,828,620), hereinafter "Foss." The Applicant traverses the rejection.

Claim 18 has been amended to set forth "a charge pump block including at least one charge pump part; a voltage level sensing block to sense a level of an output voltage and generate a level sensing signal responsive thereto; an oscillator to generate a pulse signal responsive to the level sensing signal; a detector to generate a detection signal responsive to a high voltage and a power voltage, the detector comprising: a first high voltage NMOS transistor coupled between the power voltage and a node; and a second high voltage NMOS transistor coupled between the high voltage and the node, the node having a voltage of one of (a) a difference between the power voltage and a threshold voltage of the first high voltage NMOS transistor and (b) a difference between the high voltage and a threshold voltage of the second high voltage NMOS transistor; and a selector to provide one of the high voltage and the power voltage responsive to the detection signal to the charge pump block." Additionally, the two "where" clauses at the end of claim 18 have been deleted.

Although claim 18 stands rejected under 35 U.S.C. 103(a) over Horiguchi in view of Foss, the Applicant amends claim 18 to include elements of the detector indicated to be allowable by the Examiner, namely the first and second high voltage NMOS transistors coupled between the power voltage and the high voltage, respectively, and the node generally corresponding to the first node of claim 2. For at least this reason, claim 18 is now patentable under 35 U.S.C. 103(a) over Horiguchi, even when viewed in combination with Foss.

Claims 20 and 21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kai et al. (U.S. Patent No. 5,912,564) in view of Suwa (Japanese Publication No. 2001-35193). The

Applicant traverses the rejection. Claim 20 has been cancelled and claim 21 now depends from amended claim 19, as explained below.

Claim Rejections – 35 U.S.C. § 102

Claim 19 is rejected under 35 U.S.C. 102(b) as being anticipated by Kai et al. (U.S. Patent No. 5,912,564). The Applicant traverses the rejection.

Claim 19 has been amended to set forth "a charge pump block including a plurality of charge pump parts, each charge pump part including at least one pre-charge device; a selector circuit coupled to the at least one pre-charge device of each of the charge pump parts, the selector circuit being structured to receive a supply voltage and a high voltage; and a detector circuit comprising: a first node, a second node, a high voltage inverter, a low voltage inverter, and a high voltage NMOS transistor, the high voltage NMOS transistor being coupled between the supply voltage and the first node, the high voltage inverter being coupled to the low voltage inverter, the first node being coupled to the supply voltage and the high voltage, and the second node being coupled to an input of the high voltage inverter."

Specifically, claim 19 now includes the limitations of claim 20. Claim 20 has correspondingly been cancelled. Claim 19 also sets forth "a high voltage NMOS transistor, the high voltage NMOS transistor being coupled between the supply voltage and the first node," which is an element from claim 22 indicated to be allowable. The Examiner noted that claim 22 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. While amended claim 19 does not include all of the limitations of claim 22, the Applicant submits that the included limitation of "a high voltage NMOS transistor, the high voltage NMOS transistor being coupled between the supply voltage and the first node" is not taught in the prior art, and with the other limitations of claim 19, places claim 19 in proper form for allowance.

Claim 21 has been amended to depend from claim 20. Based at least on their dependency from claim 19, and for their own merits, claims 21-27 are likewise in proper form for allowance.

Allowable Subject Matter

Claims 2-5, 22-27 and 29-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of

the base claim and any intervening claims. The Applicant thanks Examiner Hiltunen for acknowledging the patentable subject matter of these claims.

Regarding claims 29-32, the Applicant amends claim 29 to be an independent claim including limitations from claim 1. Claim 29 now sets forth "a charge pump circuit, comprising: a charge pump block including a plurality of charge pump parts, each charge pump part including at least one pre-charge device; and a selector circuit coupled to the at least one pre-charge device of each of the charge pump parts, the selector circuit being structured to receive a supply voltage and a high voltage, wherein the selector circuit comprises: an inverter configured to receive the detect signal, an output terminal of the inverter being coupled to a node, the node being coupled to gate terminals of first and second high voltage NMOS transistors." The element including the second inverter has been deleted from claim 29 and inserted into dependent claim 30.

In the Office Action, the Examiner noted that no cited art discloses the specific selector circuit as recited in claim 29. The Applicant notes that while amended claim 29 does not include all of the limitations of the base and intervening claims, the Applicant respectfully submits that "an inverter configured to receive the detect signal, an output terminal of the inverter being coupled to a node, the node being coupled to gate terminals of first and second high voltage NMOS transistors" includes allowable subject matter not taught by the prior art. Therefore, claim 29 is now in proper form for allowance, as are dependent claims 30-32.

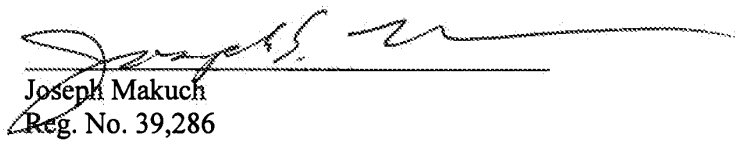
Regarding claims 22-27, as previously explained above, amended claim 19 now includes some limitations from allowable claim 22. Claim 22 remains with some limitations. The Applicant submits that amended claim 19 is in proper form for allowance, as are dependent claims 21-27.

Regarding claims 2-5, as previously explained above, amended claim 1 now includes some limitations from allowable claim 2. Claim 2 remains with some limitations. The Applicant submits that amended claim 1 is in proper form for allowance, as are dependent claims 2-5 and 28.

For the foregoing reasons, reconsideration and allowance of claims 1-5, 18-19 and 21-32 of the application as amended is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



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503-222-3613
Customer No. 20575

Electronic Acknowledgement Receipt

EFS ID:	3082369
Application Number:	10888667
International Application Number:	
Confirmation Number:	4240
Title of Invention:	Charge pump circuit operating responsive to a mode
First Named Inventor/Applicant Name:	Pyung-Moon Zhang
Customer Number:	20575
Filer:	Hosoon Lee/Stormi Davis
Filer Authorized By:	Hosoon Lee
Attorney Docket Number:	4591-380
Receipt Date:	31-MAR-2008
Filing Date:	08-JUL-2004
Time Stamp:	19:37:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		4591-380g.pdf	955440 6b59ca3f31b17c963e30bcfd6c4771be7f2f7bd1	yes	13

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Amendment After Final	2	2
	Claims	3	8
	Applicant Arguments/Remarks Made in an Amendment	9	13
Warnings:			
Information:			
	Total Files Size (in bytes):	955440	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

MISCELLANEOUS LETTER

REGARDING PAYMENT OF FEES AND EXTENSION OF TIME

	Claims Remaining After Amendment	Highest Number Previously Paid For	Present Extra Claims
Total Claims	19	20-20	0
Independent Claims	4	5-3	0

☒ Applicant petitions the Commissioner to extend the time for response (if applicable).

☒ Payment of fees is made via electronic filing system authorizing credit card payments for the extra claims and/or Petition.

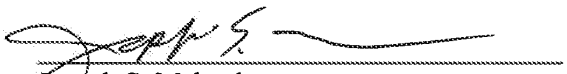
☒ Applicant is paying with a Visa card; however, Applicant requests that any deficiency or overpayment be charged or credited to deposit account number 13-1703.

Respectfully submitted,

Customer No. 20575

MARGER JOHNSON & McCOLLOM, P.C.

Date: March 31, 2008



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PTO/SB/06 (07-06)
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
10/888,667	07/08/2004	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
	03/30/2008	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	* 19	Minus	** 20	= 0	X $ =		OR	X $50=	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***5	= 0	X $ =		OR	X $210=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)					
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/GLORIA PORTER/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/888,667	07/08/2004	Pyung-Moon Zhang	4591-380	4240

20575 7590 01/31/2008

MARGER JOHNSON & MCCOLLOM, P.C.
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EXAMINER	
HILTUNEN, THOMAS J	
ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
01/31/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/888,667	ZHANG ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 18-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,18-21 and 28* is/are rejected.

7)☐ Claim(s) *2-5,21-27 and 29-32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's amendment filed 06 November 07 has been received and entered in the case. The claims and arguments filed 06 November 2007 are considered below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 19 is rejected under 35 U.S.C. 102(b) as being anticipated by Kai et al. (USPN 5,912,564)

With respect to claim 19, Kai et al. discloses in Figs. 9-11, a charge pump circuit (circuit of Fig. 9) comprising:

a charge pump block (110, 12, 16, 18, 20) including a plurality of charge pump parts (16 with 10, and 20 with N2), each charge pump part including at least one pre-charge device (16 and 20 are precharge devices that precharge the voltage at N1 and N2 to the voltage of Vout minus the threshold drop of 16 and 20, see Fig. 11); and

a selector circuit (64) coupled to the at least one pre-charge device of each of the charge pump parts (Vout of 64 is coupled to both 16 and 20), the selector circuit being structured to receive a supply voltage (VDD) and a high voltage (BOOSTB).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kai et al. (USPN 5,912,564) in view of Suwa (JP0 2001035193).

With respect to claim 1, Kai et al. discloses in Figs. 9-11, a charge pump circuit (circuit of Fig. 9) comprising:

a charge pump block (110, 12, 16, 18, 20) including and a plurality of charge pump parts (16 with 10, and 20 with N2), each charge pump part including at least one pre-charge (16 and 20 are precharge devices that precharge the voltage at N1 and N2 to the voltage of Vout minus the threshold drop of 16 and 20, see Fig. 11) device:

a selector circuit (64) coupled to the at least one pre-charge device of each of the charge pump parts (Vout of 64 is coupled to both 16 and 20), the selector circuit being structured to receive a supply voltage (VDD) and a high voltage (BOOSTB); and

Kai et al. fails to discloses, “a detector circuit comprising a first node, a second node, a high voltage inverter, and a low voltage inverter, the high voltage inverter being coupled to the low voltage inverter, the first node being coupled to the supply voltage and the high voltage, the second node being coupled to an input of the high voltage inverter, the second node having a voltage high enough to invert an output of the high

voltage inverter responsive to the high voltage being higher than the supply voltage, the low voltage inverter being configured to provide a detect signal to the selector circuit responsive to the inverted output of the high voltage inverter." Note Kai et al. discloses the selector circuit 64 being responsive to a generic "burn in mode signal" MODE B (see Col. 11 lines 49-51) Kai et al. fails to disclose the specifics of the circuit that generates a "burn in mode signal".

Suwa discloses in Fig. 9 a specific burn in test signal generator (see, machine translation provided with reference), wherein the burn in signal generator comprises:

a detector circuit (circuit of Fig. 9) comprising a first node (node coupled to the source of 138), a second node (node coupled to the drain of 138), a high voltage inverter (504, which is a high voltage inverter, since it receives the high voltage output of the second node), and a low voltage inverter (506, which is a low voltage inverter since it receives the lower voltage output from 504, i.e., voltage based on Vcc), the high voltage inverter being coupled to the low voltage inverter (504 is coupled to 506), the first node being coupled to the supply voltage (the first node is coupled to Vcc through charge pump 502) and the high voltage (the high voltage Vpp is directly connected to the first node), the second node being coupled to an input of the high voltage inverter (the second node is coupled to the input of 504), the second node has a voltage high enough to invert an output of the high voltage inverter (clearly the voltage at the drain of 138 and source of 140 is high enough to invert the output of 504) responsive to the high voltage being higher than the supply voltage (Vpp must be higher than Vcc to invert the voltage at the output 504, since Vpp is a pump voltage that is larger than Vcc and the

threshold of the detector is set to detect Vpp), the low voltage inverter being configured to provide a detect signal to the selector circuit responsive to the inverted output of the high voltage inverter (506 outputs a signal to 508, which controls the detect burn in signal TOUT, i.e., MODEB as modified above, which controls the selector 4 of 64 of Kia et al.). Suwa's circuit of Fig. 9 generates a specific burn in mode signal and has the ability to check whether a test condition setup at the time of performing a burn-in examination has been made correctly (see paragraph [0015] of the provided machine translation).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the specific burin in mode signal generation circuit of Suwa to produce the generic burn in mode signal MODEB of Kai et al. for the purpose having a specific burin mode signal generating circuit that is capable of checking whether a test condition setup at the time of performing a burn-in examination has been made correctly.

With respect to claim 28, the above combination discloses, the charge pump circuit of claim 1, wherein the charge pump block is configured to generate an output voltage on an output terminal (BOOSTA), the output terminal being coupled to the at least one pre-charge device of each of the plurality of charge pump parts (when 18 is controlled to be in a conductive state BOOSTA is coupled to node N2, which is coupled to the precharge device 20. Thus, BOOSTA is coupled to 20 via the source to drain connection of transistor 18).

Claims 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiguchi et al. (USPN 5,272,393) in view of Foss et al. (USPN 5,828,620).

With respect to claims 18, Horiguchi et al. discloses, "a charge pump circuit comprising (202 of Fig. 10):

a charge pump block to including at least one charge pump part (charge pump block of 202, which contains at least one charge pump part since 202 itself is a charge pump);

a detector to generate (4) a detection signal responsive to a high voltage (output 4 which is responsive to the high voltage V2); and

a selector (3) to provide one of the high voltage (V2) and a power voltage (V1) responsive to the detection signal to the charge pump (3 outputs one of V2 and V1 to 202 based on the output of 4)

where the detector is configured to compare the supply voltage with the high voltage (4 compares V1 and V2);

where the detector output is high responsive to a level of the high voltage being higher than a level of the supply voltage (4 outputs a high when V2 is higher than V1);

Horiguchi et al. fails to disclose, in Fig. 10, "a voltage level sensing block to sense a level of an output voltage and generate a level sensing signal responsive thereto; an oscillator to generate a pulse signal responsive to the level sensing signal." Note Horiguchi et al. merely discloses a generic word line driver (202). However, Foss et al. discloses, in Figs. 3 and 6, a specific world line driver (circuit of Fig. 6) that includes a charge pump (39) responsive "to a voltage level sensing block (35-38) to

sense a level of an output voltage (Vpp) and generate a level sensing signal (INHIBIT) responsive thereto; an oscillator (44) to generate pulse signal responsive to the level sensing signal (44 generates complementary pulse signals Φ1 and Φ2 and Φ1 bar and Φ2 bar, see Fig. 3, responsive to the INHIBIT signal)." Foss et al.'s word line driving circuit provides a highly regulated word line voltage signal that prevents both an over-voltage and an under-voltage condition of the word line diving signal, thus increasing the reliability of the circuit controlled by the boosted word line signal.

It would have been obvious to replace the generic word line driving circuit 202 of Fig. 10 of Horiguchi et al. with the specific word line driving circuit of Fig. 6 of Foss et al. for the purpose of increasing the reliability of the circuit of Fig. 10 of Horiguchi et al.

Claims 20 and 21 rejected under 35 U.S.C. 103(a) as being unpatentable over Kai et al. (USPN 5,912,564) in view of Suwa (JP0 2001035193).

With respect to claim 20, Kai et al. discloses, the charge pump circuit of claim 19. Kai et al. fails to disclose, "a detector circuit comprising a first node, a second node, a high voltage inverter, and a low voltage inverter, the high voltage inverter being coupled to the low voltage inverter, the first node being coupled to the supply voltage and the high voltage, the second node being coupled to an input of the high voltage inverter." Note Kai et al. discloses the selector circuit 64 being responsive to a generic "burn in mode signal" MODE B (see Col. 11 lines 49-51) Kai et al. fails to disclose the specifics of the circuit that generates a "burn in mode signal".

Suwa discloses in Fig. 9 a specific burn in test signal generator (see, machine translated abstract), wherein the burn in signal generator comprises:

a detector circuit (circuit of Fig. 9) comprising a first node (node coupled to the source of 138), a second node (node coupled to the drain of 138), a high voltage inverter (504, which is a high voltage inverter, since it receives the high voltage output of the second node), and a low voltage inverter (506, which is a low voltage inverter since it receives the lower voltage output from 504, i.e., voltage based on Vcc), the high voltage inverter being coupled to the low voltage inverter (504 is coupled to 506), the first node being coupled to the supply voltage (the first node is coupled to Vcc through charge pump 502) and the high voltage (the high voltage Vpp is directly connected to the first node), the second node being coupled to an input of the high voltage inverter (the second node is coupled to the input of 504). Suwa's circuit of Fig. 9 generates a specific burn in mode signal and has the ability to check whether a test condition setup at the time of performing a burn-in examination has been made correctly (see paragraph [0015] of the provided machine translation).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the specific burin in mode signal generation circuit of Suwa to produce the generic burn in mode signal MODEB of Kai et al. for the purpose having a specific burin mode signal generating circuit that is capable of verifying temperature and generating the required burn in mode signal and Kai et al.

With respect to claim 21, the above modification discloses, "the charge pump circuit of claim 20, wherein the second node has a voltage high enough to invert an

output of the high voltage inverter (clearly the voltage at the drain of 138 and source of 140 is high enough to invert the output of 504) responsive to the high voltage being higher than the supply voltage (Vpp must be higher than Vcc to invert the voltage at the output 504, since Vpp is a pump voltage that is larger than Vcc), the low voltage inverter being configured to provide a detect signal to the selector circuit responsive to the inverted output of the high voltage inverter (506 outputs a signal to 508, which controls the detect burn in signal TOUT, i.e., MODEB as modified above, which controls the selector 4 of 64 of Kia et al.).

Response to Arguments

Applicant's arguments filed 06 November 2007 have been fully considered but they are not persuasive.

The argument that it would not be obvious to replace Horiguchi's generic "word line driver" circuit 202 with the specific “word line driver” circuit of Foss, since Foss' word line driver “prevents an over-voltage condition” and providing “an over-voltage condition” is essential to Horiguchi’s word line driver circuit operation is not persuasive. Applicant argues that Foss' circuit would prevent "a voltage higher than the one applied in ordinary operation" from being impressed on a supply terminal before delivery of semiconductor devices so as to exclude therefrom those devices which become imperfect after the voltage is applied. However, it can be seen that Foss' line driver circuit allows for the application of a voltage much higher than a normal operation voltage. For instance, a supply voltage such as VDD is used by a semiconductor

device during normal operation. Foss' circuit allows for the boosting of the output voltage to two times VDD (i.e., 2VDD, see Col. 2 lines 14-16). Therefore, Foss' circuit is capable of supplying a voltage that is higher than the one applied in ordinary operation. Examiner agrees with applicant that it Horiguchi intends to use a boosted voltage to "age" circuits to exclude imperfect devices (i.e., weak) from the semiconductor circuit. However, that does not mean that Horiguchi intends to destroy all of the devices of the semiconductor circuit, which may happen if too large of a boosted voltage is supplied to the semiconductor devices. For instance, if a word line voltage became too high for normal devices (i.e., non-imperfect devices) to withstand then they will also be destroyed thereby destroying Horiguchi's semiconductor device. Therefore, one of ordinary skill in the art would be motivated to prevent an overvoltage condition (i.e., a voltage condition where normal devices would be destroyed) within Horiguchi's circuit.

Allowable Subject Matter

Claims 2-5, 22-27 and 29-32 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claims 2-4, and 22-27, there is no cited art that discloses the specific detector circuit having fist and second high voltage NMOS transistor coupled between the supply voltage and the high voltage, respectively, and the first node as recited in claims 2, and 21.

With respect to claims 5, 29-32, there is no cited art that discloses the specific selector circuit as recited in claims 5 and 29.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on M-F 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571)272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TH
January 25, 2008

/N. Drew Richards/

Supervisory Patent Examiner, Art Unit 2816

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	Examiner Thomas J. Hiltunen	Art Unit 2816	Page 1 of 1

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(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号
特開2001－35193
（P2001－35193A）
(43)公開日　平成13年２月９日(2001.2.9)

(51)Int.Cl.[7]	識別記号	ＦＩ		テーマコード（参考）
Ｇ１１Ｃ　29/00	６７１	Ｇ１１Ｃ　29/00	６７１Ｆ	２Ｇ０３２
Ｇ０１Ｒ　31/28		Ｇ０６Ｆ　11/24	３１０	５Ｂ０１８
Ｇ０６Ｆ　11/24	３１０		12/16 ３３０Ａ	５Ｂ０２４
12/16	３３０	Ｇ０１Ｒ　31/28	Ｂ	５Ｂ０４８
Ｇ１１Ｃ　11/401		Ｇ１１Ｃ　11/34	３７１Ａ	５Ｌ１０６

審査請求　未請求　請求項の数12　ＯＬ　（全 11 頁）

(21)出願番号　特願平11－202882

(22)出願日　平成11年７月16日(1999.7.16)

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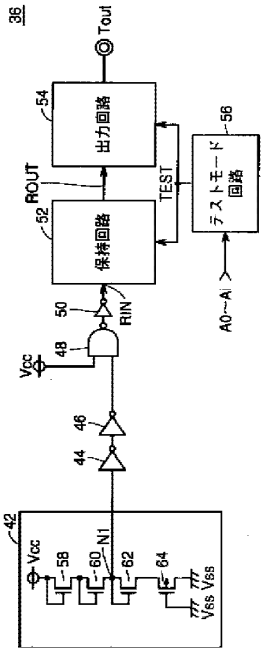
Ｆターム(参考)　2G032 AB02 AE08 AE10 AK11
5B018 GA03 HA31 NA02 PA03 QA13
5B024 AA15 BA29 CA15 EA01
5B048 AA19 CC06 FF01 FF03
5L106 DD21 DD36 FF01 GG00

(54)【発明の名称】　半導体記憶装置

(57)【要約】
【課題】　バーンイン試験等が適切な条件でなされたか否かを半導体記憶装置ごとに調べることが可能な半導体記憶装置を提供する。
【解決手段】　バーンイン試験時における試験電圧が所定の電圧を超えたことを検出する高電圧検出回路４２と、検出結果を保持する保持回路５２と、保持回路５２の保持内容を外部に出力する出力回路５４とを備える。観測する試験電圧を内部電源電圧にすれば、内部で発生される内部電源電圧が適切な値になっているかを知ることができる。好ましくは、複数の異なる電圧を検知する高電圧検出回路と、対応する検出結果を保持する保持回路とを備えることにより、電圧範囲も特定することができる。さらに、高温検出回路を内蔵すれば温度条件についても確認可能である。



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【特許請求の範囲】
【請求項１】　テスト時におけるテスト条件を検出する検出回路と、
前記検出回路の出力を受けて保持する保持回路と、
前記保持回路の出力を読出す出力回路とを備える半導体記憶装置。
【請求項２】　前記検出回路は、
テスト電圧が第１の電圧を超えたことを検出する第１の電圧検出回路を含む、請求項１に記載の半導体記憶装置。
【請求項３】　前記検出回路は、
前記テスト電圧が前記第１の電圧より高い第２の電圧を超えたことを検出する第２の電圧検出回路をさらに含む、請求項２に記載の半導体記憶装置。
【請求項４】　外部から与えられる電源電圧を受けて内部電源電圧を発生する電圧発生回路と、
前記内部電源電圧によって動作するメモリアレイとをさらに備え、
前記テスト電圧は、前記内部電源電圧である、請求項２に記載の半導体記憶装置。
【請求項５】　前記検出回路は、
テスト時の温度を検出する温度検出回路を含む、請求項１に記載の半導体記憶装置。
【請求項６】　前記保持回路は、
第１の時刻において活性化され前記検出回路の出力を保持する第１のデータ保持回路と、
前記第１の時刻より後の第２の時刻において活性化され前記検出回路の出力を保持する第２のデータ保持回路とを含む、請求項１に記載の半導体記憶装置。
【請求項７】　前記保持回路は、
前記検出回路の出力を受けて保持する揮発性データ保持回路を含む、請求項１に記載の半導体記憶装置。
【請求項８】　前記揮発性データ保持回路は、
前記検出回路の出力を受けて保持するラッチ回路を含む、請求項７に記載の半導体記憶装置。
【請求項９】　前記保持回路は、
前記検出回路の出力を受けて保持する不揮発性データ保持回路を含む、請求項１に記載の半導体記憶装置。
【請求項１０】　前記不揮発性データ保持回路は、
電気信号に応じて一端と他端の間の導通状態を変化させる電気ヒューズを含む、請求項９に記載の半導体記憶装置。
【請求項１１】　前記電気ヒューズは、所定電圧より大きな電圧が両端に印加されると導通状態となる、アンチヒューズである、請求項１０に記載の半導体記憶装置。
【請求項１２】　前記テストは、バーンイン試験である、請求項１に記載の半導体記憶装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】この発明は、半導体記憶装置

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に関し、より特定的には、信頼性評価のための試験に関連する回路を有する半導体記憶装置に関する。
【０００２】
【従来の技術】近年では、半導体装置の高集積化によりＭＯＳトランジスタの微細化が進み、それに伴いＭＯＳトランジスタのゲート酸化膜の厚さも年々減少する方向にある。このため、ゲート酸化膜の耐圧が下がり、ゲート電圧を高く設定すると、ＭＯＳトランジスタの信頼性に影響を及ぼす可能性がある。
【０００３】たとえば、半導体記憶装置が使用されるシステムにおいては、システム自体の電源電圧より半導体記憶装置の内部動作に必要な電圧のほうが低い場合がある。このような場合は、システム自体の電源電圧から半導体記憶装置の電源電圧を供給するため、半導体記憶装置の内部で電圧を降下させて半導体記憶装置の動作に必要な内部電源電圧を発生する場合が多い。
【０００４】このようにして内部電源電圧を発生する回路を電圧降下回路と呼ぶ。このような電圧降下回路を用いることによって、半導体記憶装置の消費電力は大きく低減し、半導体記憶装置内部の内部電源電圧を安定化させることができる。
【０００５】次に信頼性評価のための試験について説明する。一般に、半導体装置に故障が発生する期間は、３つの期間に大別される。この期間は時間の経過順に初期故障期間、偶発故障期間、摩耗故障期間である。
【０００６】初期故障期間は、半導体装置の作成時の欠陥が故障として現れたもので、使用開始直後に発生する初期故障が発生する期間である。この初期故障の割合は時間とともに急速に減少する。
【０００７】その後は、低い故障率が一定期間長く続く偶発故障期間となる。やがて、半導体装置は耐用年数に近づき、急激に故障率が増大する摩耗故障期間になる。
【０００８】半導体装置は、偶発故障期間内で使用することが望ましい。したがって、半導体装置の信頼性を高めるには、初期故障が発生する半導体装置を予め除去する必要がある。このために、半導体装置に一定時間の加速動作エージングを行ない、不良品を除去するスクリーニングが行なわれる。スクリーニングを短期間で効果的に行なうためには、初期故障率が時間に対して急速に減少し、早く偶発故障期間に入るような試験をすることが望ましい。
【０００９】現在、このスクリーニング手法の一つとして一般に高温動作試験（バーンイン試験）を行なっている。バーンイン試験は、実デバイスを用いて誘電体膜を直接評価できる手法であり、アルミ配線のマイグレーションを初め、あらゆる不良要因を高電界のストレスを印加することにより顕在化させる試験である。
【００１０】このバーンイン試験は、特に、高温中で半導体装置を動作させて加速性を高めると効果的となる。
【００１１】

【発明が解決しようとする課題】従来の半導体記憶装置では、半導体記憶装置内部にテスト条件を検出できる機能がないので、適切な条件でバーンイン試験が行なわれたかどうかがわからないという問題点があった。

【００１２】たとえば、バーンイン試験の前後では半導体記憶装置の外観は変わることがない。したがって、試験前後の製品の区別には十分な注意が必要である。このような場合に、半導体記憶装置にバーンイン試験が行なわれたことを半導体記憶装置ごとに内部で保持しておき、出荷時のテストにおいて電気的に読取ることができれば便利である。

【００１３】また、バーンイン試験装置によって、半導体記憶装置に対して条件設定、たとえば温度条件や電圧条件の設定が適切にされていたかをバーンイン試験の後に知ることができれば便利である。

【００１４】さらに、バーンイン試験時においては、外部から与える電源電圧を所定の高電圧にするが、このときに、半導体記憶装置が内蔵する電圧降下回路によって発生される内部電源電圧が変化しないのでは、加速試験を実施したことにならない。したがって、通常は電圧降下回路は、バーンイン試験時には通常時の内部電源電圧よりもさらに高い内部電源電圧を発生するように動作が切換わる。この電圧降下回路の動作切換が正常に行なわれたか否かを検出して保持できればさらにバーンイン試験の信頼度が上がる。

【００１５】この発明の目的は、バーンイン試験等を実行する際の試験条件設定が正しくなされたか否かを半導体記憶装置ごとに確認することが可能な半導体記憶装置を提供することである。

【００１６】

【課題を解決するための手段】請求項１に記載の半導体記憶装置は、テスト時におけるテスト条件を検出する検出回路と、検出回路の出力を受けて保持する保持回路と、保持回路の出力を読出す出力回路とを備える。

【００１７】請求項２に記載の半導体記憶装置は、請求項１に記載の半導体記憶装置の構成に加えて、検出回路は、テスト電圧が第１の電圧を超えたことを検出する第１の電圧検出回路を含む。

【００１８】請求項３に記載の半導体記憶装置は、請求項２に記載の半導体記憶装置の構成に加えて、検出回路は、テスト電圧が第１の電圧より高い第２の電圧を超えたことを検出する第２の電圧検出回路をさらに含む。

【００１９】請求項４に記載の半導体記憶装置は、請求項２に記載の半導体記憶装置の構成に加えて、外部から与えられる電源電圧を受けて内部電源電圧を発生する電圧発生回路と、内部電源電圧によって動作するメモリアレイとをさらに備え、テスト電圧は、内部電源電圧である。

【００２０】請求項５に記載の半導体記憶装置は、請求項１に記載の半導体記憶装置の構成に加えて、検出回路は、テスト時の温度を検出する温度検出回路を含む。

【００２１】請求項６に記載の半導体記憶装置は、請求項１に記載の半導体記憶装置の構成に加えて、保持回路は、第１の時刻において活性化され検出回路の出力を保持する第１のデータ保持回路と、第１の時刻より後の第２の時刻において活性化され検出回路の出力を保持する第２のデータ保持回路とを含む。

【００２２】請求項７に記載の半導体記憶装置は、請求項１に記載の半導体記憶装置の構成に加えて、保持回路は、検出回路の出力を受けて保持する揮発性データ保持回路を含む。

【００２３】請求項８に記載の半導体記憶装置は、請求項７に記載の半導体記憶装置の構成に加えて、揮発性データ保持回路は、検出回路の出力を受けて保持するラッチ回路を含む。

【００２４】請求項９に記載の半導体記憶装置は、請求項１に記載の半導体記憶装置の構成に加えて、保持回路は、検出回路の出力を受けて保持する不揮発性データ保持回路を含む。

【００２５】請求項１０に記載の半導体記憶装置は、請求項９に記載の半導体記憶装置の構成に加えて、不揮発性データ保持回路は、電気信号に応じて一端と他端の間の導通状態を変化させる電気ヒューズを含む。

【００２６】請求項１１に記載の半導体記憶装置は、請求項１０に記載の半導体記憶装置の構成において、電気ヒューズは、所定電圧より大きな電圧が両端に印加されると導通状態となる、アンチヒューズである。

【００２７】請求項１２に記載の半導体記憶装置は、請求項１に記載の半導体記憶装置の構成において、テストは、バーンイン試験である。

【００２８】

【発明の実施の形態】以下において、本発明の実施の形態について図面を参照して詳しく説明する。なお、図中同一符号は同一または相当部分を示す。

【００２９】［実施の形態１］図１は、本発明の実施の形態１の半導体記憶装置１の構成を示す概略ブロック図である。

【００３０】図１を参照して、半導体記憶装置１は、制御信号ｅｘｔ．／ＲＡＳ、ｅｘｔ．／ＣＡＳ、ｅｘｔ．／ＷＥをそれぞれ受ける制御信号入力端子２～６と、アドレス入力端子群８と、データ信号を入力する入力端子Ｄｉｎと、データ信号を出力する出力端子Ｄｏｕｔと、接地電位Ｖｓｓが与えられる接地端子１２と、電源電位Ｅｘｔ．Ｖｃｃが与えられる電源端子１０とを備える。

【００３１】半導体記憶装置１は、さらに、クロック発生回路２２と、行および列アドレスバッファ２４と、行デコーダ２６と、列デコーダ２８と、センスアンプ＋入出力制御回路３０と、メモリセルアレイ３２と、ゲート回路１８と、データ入力バッファ２０およびデータ出力バッファ３４とを備える。

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【００３２】クロック発生回路２２は、制御信号入力端子２、４を介して外部から与えられる外部行アドレスストローブ信号ｅｘｔ．／ＲＡＳと外部列アドレスストローブ信号ｅｘｔ．／ＣＡＳとに基づいた所定の動作モードに相当する制御クロックを発生し、半導体記憶装置全体の動作を制御する。

【００３３】行および列アドレスバッファ２４は、外部から与えられるアドレス信号Ａ０～Ａｉ（ｉは自然数）に基づいて生成したアドレス信号を行デコーダ２６および列デコーダ２８に与える。

【００３４】行デコーダ２６と列デコーダ２８とによって指定されたメモリセルアレイ３２中のメモリセルは、センスアンプ＋入出力制御回路３０とデータ入力バッファ２０またはデータ出力バッファ２２とを介して入出力端子Ｄｉｎまたは出力端子Ｄｏｕｔを通じて外部とデータをやり取りする。

【００３５】半導体記憶装置１は、さらに、アドレス信号Ａ０～Ａｉの設定に応じたテストモードにおいてテスト条件を検出して検出結果を保持する条件検出回路３６と、条件検出回路３６の保持結果を出力するための端子Ｔｏｕｔと、外部電源電圧Ｅｘｔ．Ｖｃｃおよび接地電位Ｖｓｓを受けて内部電源電位Ｖｃｃを出力する電圧降下回路３８とを含む。

【００３６】図１に示した半導体記憶装置１は、代表的な一例であり、たとえば同期型半導体記憶装置（ＳＤＲＡＭ）にも本発明は適用可能である。

【００３７】図２は、図１に示した条件検出回路３６の構成を示すブロック図である。図２を参照して、条件検出回路３６は、内部電源電位Ｖｃｃが所定の高電位に設定されたか否かを検出する高電圧検出回路４２と、高電圧検出回路４２の出力を受ける直列に接続された２つのインバータ４４、４６と、一方の入力がＨレベルに固定され、他方の入力にインバータ４６の出力を受けるＮＡＮＤ回路４８と、ＮＡＮＤ回路４８の出力を受けて反転し、信号ＲＩＮを出力するインバータ５０とを含む。

【００３８】条件検出回路３６は、さらに、アドレス信号Ａ０～Ａｉの設定に応じてテストモードを検出し、テスト信号ＴＥＳＴを出力するテストモード回路５６と、テストモード信号ＴＥＳＴが活性化されたときに信号ＲＩＮの活性化に応じてテスト条件に対応する情報を保持する保持回路５２と、保持回路５２の保持する情報に応じた信号ＲＯＵＴをテスト信号ＴＥＳＴの活性化時に端子Ｔｏｕｔに出力する出力回路５４を含む。

【００３９】テストモード回路５６は、たとえば、アドレス信号Ａ０～Ａｉの与えられる端子のうち所定の端子に電源電位より高い電位が与えられたときにテストモードであることを検出し、その時の他の端子の設定状態により、どのテストが行なわれているかを検知し対応する制御をするためにテスト信号を出力する。

【００４０】高電圧検出回路４２は、ゲートとドレインがともに内部電源電位Ｖｃｃに結合されるＮチャネルＭＯＳトランジスタ５８と、ゲートとドレインがともにＮチャネルＭＯＳトランジスタ５８のソースに接続されソースがノードＮ１に接続されるＮチャネルＭＯＳトランジスタ６０と、ゲートとドレインがノードＮ１に接続されるＮチャネルＭＯＳトランジスタ６２と、ゲートとドレインがともに接地電位Ｖｓｓに接続されソースがＮチャネルＭＯＳトランジスタ６２のソースに接続されるＰチャネルＭＯＳトランジスタ６４とを含む。

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【００４１】ノードＮ１の電位は、ＮチャネルＭＯＳトランジスタ５８、６０のしきい値電圧分だけ内部電源電位Ｖｃｃより低い電圧となる。通常使用時においては、電源電圧が低いので、高電圧検出回路の出力であるノードＮ１の電位はＬレベルとなる。

【００４２】バーンイン試験時には、初期故障不良品をスクリーニングするため、予め設定された高電圧が外部から与えられ、そして内部電源電位Ｖｃｃも通常よりも高い電圧となる。このときに、高電圧検出回路４２の出力はインバータ４４の入力しきい値電圧を超え、保持回路５２に対する書込を行なう信号ＲＩＮがＨレベルとなる。

【００４３】図３は、図２における保持回路５２の構成を示す回路図である。図３を参照して、保持回路５２は、信号ＲＩＮを受けて反転し／Ｓを出力するインバータ６２と、テスト信号ＴＥＳＴを受けるインバータ６６と、インバータ６６の出力とテスト信号ＴＥＳＴを受けて信号／Ｒを出力するＮＡＮＤ回路６８と、信号／ＳがＬレベルのときにセットされ信号／ＲがＬレベルのときにリセットされるラッチ回路６４とを含む。

【００４４】ラッチ回路６４は、信号／Ｓを一方の入力に受け保持回路５２の出力である信号ＲＯＵＴを出力するＮＡＮＤ回路７０と、信号／Ｒおよび信号ＲＯＵＴを受けるＮＡＮＤ回路７２とを含む。ＮＡＮＤ回路７０の他方の入力にはＮＡＮＤ回路７２の出力が接続される。ラッチ回路６４は、テスト信号ＴＥＳＴの立上がり時にインバータ６６およびＮＡＮＤ回路６８によって発生されるパルス信号によってリセットされ、保持回路入力である信号ＲＩＮがＨレベルに活性化されたときにデータがセットされる。ラッチ回路６４にデータがセットされると、信号ＲＯＵＴはＨレベルとなり、半導体装置が適切な電圧でバーンイン試験されたことがわかる。

【００４５】図３に示した保持回路の構成は、バーンイン試験直後に電源電圧を保持したままで判定を行なう場合に使用可能な揮発性回路の例であったが、不揮発性の記憶素子を用いれば電源を断状態とした後の出荷検査においても判定が可能となる。

【００４６】図４は、保持回路５２の他の例である保持回路５２ａの構成を示す回路図である。

【００４７】図４を参照して、保持回路５２ａは、第１の入力に信号ＲＩＮを受け、第２の入力にテスト信号Ｔ

ＥＳＴを受ける３入力のＡＮＤ回路７４と、ＡＮＤ回路７４の出力がＨレベルのときにイネーブル信号ＥＮを間欠的に活性化させるパルス発生回路７５と、イネーブル信号ＥＮの活性化に応じて高電圧ＢＶを出力する高電圧発生回路７６と、イネーブル信号ＥＮの活性化時に高電圧ＢＶを受けてデータ保持を行なう不揮発性データ保持回路７８と、不揮発性データ保持回路７８の出力を受ける直列に接続されたインバータ８０、８２と、インバータ８２の出力を受けて反転し、信号ＲＯＵＴを出力するインバータ８４とを含む。インバータ８２の出力は、ＡＮＤ回路７４の第３の入力にも与えられる。

【００４８】不揮発性データ保持回路７８は、イネーブル信号ＥＮがＨレベルのときに高電圧ＢＶをノードＮ２に伝達するＮチャネルＭＯＳトランジスタ８６と、内部電源電位Ｖｃｃが与えられる電源ノードとノードＮ２との間に接続される抵抗８８と、接地電位Ｖｓｓが与えられる接地ノードとノードＮ２との間に接続されるアンチヒューズ９０とを含む。ノードＮ２からは不揮発性データ保持回路７８の出力信号が出力される。

【００４９】情報を記憶するため、特定のフューズに対しレーザ光線や電気信号を印加し、電気的性質を変えることをブローという。アンチフューズは電気フューズの一種であるが、ブローすることで電極間が導通する性質を持つ。

【００５０】アンチフューズ９０は、特開平７－３７９８４号公報に示されるように、ブロー前に高抵抗を有し、適当な電圧を印加すると低抵抗へとその導通状態を変化させる要素である。アンチフューズは、キャパシタ型の構造を有しており、たとえば、アルミニウムのような２個の導電層の間に二酸化ケイ素のような薄い絶縁層を挟んだものである。そのままではキャパシタすなわちオープン回路であるが、高電圧を印加してブローすると絶縁層に導電性のパスが発生し、数ｋΩ程度の抵抗値を持つ抵抗素子となる。

【００５１】なお、不揮発性データ保持回路７８に代えて、フラッシュメモリ等に用いられているフローティングゲートを有するトランジスタを用いた構成としてもデータを不揮発性的に保持することが可能である。もちろん、保持回路５２ａに代えて、フラッシュメモリそのものを用いてもかまわない。

【００５２】以上のように不揮発性のデータ保持回路で保持回路を構成すれば、バーンイン試験後に一旦電源を断状態にした後の出荷検査においてもバーンイン試験が正常に行なわれたか否かの判定が可能である。さらに、出荷後において、故障が発生した場合でも、バーンイン試験が正常に行なわれていたか否かの解析に使用することもできる。

【００５３】［実施の形態２］実施の形態２では、図１における条件検出回路３６に代えて条件検出回路１００を備える。

【００５４】図５は、条件検出回路１００の構成を示すブロック図である。図５を参照して、条件検出回路１００は、高電圧検出回路１０２と、高電圧検出回路１０２の出力を受ける直列に接続されるインバータ１０４、１０６と、一方の入力がＨレベルに固定され他方の入力にインバータ１０６の出力を受けるＮＡＮＤ回路１０８と、ＮＡＮＤ回路１０８の出力を受けて反転するインバータ１１０と、アドレス信号Ａ０～Ａｉの設定に応じてテスト信号ＴＥＳＴを活性化させるテストモード回路１１６と、テスト信号ＴＥＳＴの活性化時にインバータ１１０の出力に応じた値を内部に保持する保持回路１１２と、テスト信号ＴＥＳＴの活性化時に保持回路１１２の出力を受けて端子Ｔｏｕｔ１から出力する出力回路１１４とを含む。

【００５５】条件検出回路１００は、さらに、高電圧検出回路４２と、高電圧検出回路４２の出力を受ける直列に接続されたインバータ１２４、１２６と、一方の入力がＨレベルに固定され他方の入力にインバータ１２６の出力を受けるＮＡＮＤ回路１２８と、ＮＡＮＤ回路１２８の出力を受けて反転するインバータ１３０と、テスト信号ＴＥＳＴの活性化時にインバータ１３０の出力に応じた値を内部に保持する保持回路１３２と、テスト信号ＴＥＳＴの活性化時に保持回路１３２の保持する情報に応じた信号を受けて端子Ｔｏｕｔ２に出力する出力回路１３４とを含む。

【００５６】高電圧検出回路４２は、図２における高電圧検出回路４２と同様な構成を有するため説明は繰返さない。

【００５７】高電圧検出回路１０２は、内部電源電位Ｖｃｃにドレインおよびゲートが結合されソースがノードＮ３に接続されるＮチャネルＭＯＳトランジスタ１３８と、ノードＮ３にゲートおよびドレインが接続されるＮチャネルＭＯＳトランジスタ１４０と、ＮチャネルＭＯＳトランジスタ１４０のソースにゲートおよびドレインが接続されるＮチャネルＭＯＳトランジスタ１４２と、ゲートおよびドレインが接地電位Ｖｓｓに結合されソースがＮチャネルＭＯＳトランジスタ１４２のソースと接続されるＰチャネルＭＯＳトランジスタ１４４とを含む。ノードＮ３からは高電圧検出回路１０２の出力信号が出力される。

【００５８】高電圧検出回路４２は内部電源電位ＶｃｃからＮチャネルＭＯＳトランジスタ５８、６０のしきい値電圧分だけ低い電圧がノードＮ１から出力されるが、高電圧検出回路１０２においては、内部電源電位ＶｃｃからＮチャネルＭＯＳトランジスタ１３８のしきい値電圧分だけ低い電位がノードＮ３から出力される。

【００５９】このように、２つの高電圧検出回路において、異なる電圧を検出させることができる。この構成においては、バーンイン試験において内部電源電位Ｖｃｃとして内部メモリセルに印加された電圧範囲の特定が可

能となる。

【００６０】すなわち、実施の形態１においては、ある電源電圧以上の値が与えられたことは検出できるが、図５で示した構成にすれば、ある電源電位以上でかつある電源電位未満の電圧が与えられていたことを検出することが可能である。

【００６１】［実施の形態３］実施の形態３においては、図１における条件検出回路３６に代えて条件検出回路２００を備える。

【００６２】図６は、条件検出回路２００の構成を示すブロック図である。図６を参照して、条件検出回路２００は、高温検出回路２０２と、高温検出回路２０２の出力を受けて反転するインバータ２０４と、一方の入力がＨレベルに固定され、他方の入力にインバータ２０４の出力を受けるＮＡＮＤ回路２０６と、ＮＡＮＤ回路２０６の出力を受けて反転するインバータ２０８と、アドレス信号Ａ０～Ａｉの設定に応じてテスト信号ＴＥＳＴを活性化するテストモード回路２１４と、テスト信号ＴＥＳＴが活性化時にインバータ２０８の出力に応じた情報を保持する保持回路２１０と、テストモード信号ＴＥＳＴが活性化時に保持回路２１０が保持する情報を受けて端子Ｔｏｕｔに出力する出力回路２１２とを含む。

【００６３】高温検出回路２０２は、検出部２１９と、検出部２１９の出力電位に応じてインバータ２０４に信号を出力する出力部２２９とを含む。

【００６４】検出部２１９は、内部電源電位Ｖｃｃにソースが結合されゲートとドレインが接続されたＰチャネルＭＯＳトランジスタ２２０と、ＰチャネルＭＯＳトランジスタ２２０のドレインと接地ノードとの間に接続されるＮチャネルＭＯＳトランジスタ２２２と、ソースが接地ノードと接続されゲートおよびドレインがＮチャネルＭＯＳトランジスタ２２２のゲートに接続されるＮチャネルＭＯＳトランジスタ２２８と、ドレインがＮチャネルＭＯＳトランジスタ２２８のドレインと接続されゲートがＰチャネルＭＯＳトランジスタ２２０のドレインに接続されるＰチャネルＭＯＳトランジスタ２２６と、内部電源電位Ｖｃｃが与えられる電源ノードとＰチャネルＭＯＳトランジスタ２２６のドレインとの間に接続される抵抗２２４とを含む。

【００６５】出力部２２９は、ＮチャネルＭＯＳトランジスタ２２８のドレインにゲートが接続されソースが接地電位Ｖｓｓに結合されるＮチャネルＭＯＳトランジスタ２３２と、内部電源電位Ｖｃｃが与えられる電源ノードとＮチャネルＭＯＳトランジスタ２３２のドレインとの間に接続される抵抗２３０とを含む。ＮチャネルＭＯＳトランジスタ２３２のドレインの電位は高温検出回路２０２の出力電位となる。

【００６６】検出部２１９が含む抵抗２２４に流れる電流は、絶対温度に比例するように調整されている。すなわち、抵抗２２４の抵抗値を適切に選択することで、ＰチャネルＭＯＳトランジスタ２２０、２２６はサブスレッショルド電流領域で動作するようにできる。

【００６７】サブスレッショルド電流領域においては、ＭＯＳトランジスタのドレイン電流Ｉｄｓの対数を取った値すなわちｌｏｇ（Ｉｄｓ）とゲート－ソース間電圧Ｖｇｓとの間の関係は一定の傾きを有する直線となる。

【００６８】この傾きはサブスレッショルド係数Ｓとよばれ温度と近似的に次式のような関係が有る。ｋはボルツマン係数、Ｔは絶対温度である。

【００６９】Ｓ∝ｋＴ…（１）

ＮチャネルＭＯＳトランジスタ２２２、２２８によって構成されるカレントミラー回路によって、ＰチャネルＭＯＳトランジスタ２２０とＰチャネルＭＯＳトランジスタ２２６には等しい電流Ｉｄｓが流れる。

【００７０】ここで、ＰチャネルＭＯＳトランジスタ２２０とＰチャネルＭＯＳトランジスタ２２６とのトランジスタサイズ（Ｗ／Ｌ）の比を１：１０にする。ＰチャネルＭＯＳトランジスタ２２０とＰチャネルＭＯＳトランジスタ２２６のゲート－ソース間電圧をそれぞれＶｇｓ１、Ｖｇｓ２とすると、次式が成り立つ。

【００７１】Ｖｇｓ１－Ｖｇｓ２＝Ｓ…（２）

また抵抗２２４の抵抗値をＲとすると、Ｒの両端にかかる電位差はＶｇｓ１－Ｖｇｓ２なので、次式が成り立つ。

【００７２】

Ｉｄｓ＝（Ｖｇｓ１－Ｖｇｓ２）／Ｒ…（３）

したがって、（１）～（３）式より、次式が導き出される。

【００７３】Ｉｄｓ＝Ｓ／Ｒ∝ｋＴ…（４）

すなわち、半導体記憶装置が高温になると、抵抗２２４を流れる電流値は増加する。ＮチャネルＭＯＳトランジスタ２２８に流れる電流とＮチャネルＭＯＳトランジスタ２３２に流れる電流とはトランジスタサイズが等しければ等しくなる。したがって、ＮチャネルＭＯＳトランジスタ２３２に流れる電流値は、半導体記憶装置の温度が高温になるとやはり増加する。抵抗２３０の抵抗値は温度依存性が小さいので流れる電流が増大すれば出力部２２９の出力する電位は低くなる。

【００７４】抵抗２３０を抵抗２２４より大きな抵抗値にすると温度変化に対するより大きな振幅を得ることができる。

【００７５】したがって、高温になれば、インバータ２０４の出力はＨレベルとなり、応じてインバータ２０８の出力もＨレベルとなり保持回路２１０には半導体記憶装置が高温になったことが保持される。

【００７６】保持回路２１０は、図３に示した保持回路５２や図４に示した保持回路５２ａと同様な構成を有するものを用いることができる。

【００７７】以上説明したように、実施の形態３においては、半導体記憶装置がバーンイン試験時において適切

な温度で実施されたか否かを確認することが可能となる。

【００７８】また図５と同様に検出温度が異なる複数の高温検出回路を用いれば、温度範囲の特定が可能となる。

【００７９】［実施の形態４］実施の形態４では図１に示した条件検出回路３６に代えて、条件検出回路３００を備える。

【００８０】図７は、条件検出回路３００の構成を示すブロック図である。図７を参照して、条件検出回路３００は、高電圧検出回路４２と、高電圧検出回路４２の出力を受ける直列に接続されたインバータ３０４、３０６と、高温検出回路２０２と、高温検出回路２０２の出力を受けて反転するインバータ３１０と、インバータ３０６の出力とインバータ３１０の出力を受けるＮＡＮＤ回路３１２と、ＮＡＮＤ回路３１２の出力を受けて反転するインバータ３１４とを含む。

【００８１】条件設定回路３００は、さらに、アドレス信号Ａ０～Ａｉの設定に応じてテストモードを検出してテストモード信号ＴＥＳＴを出力するテストモード回路３２０と、テストモード信号ＴＥＳＴの活性化に応じてインバータ３１４の出力に応じた値を情報として保持する保持回路３１６と、テストモード信号ＴＥＳＴの活性化に応じて保持回路３１６の保持する情報に対応する信号を受けて端子Ｔｏｕｔに出力する出力回路３１８とを含む。

【００８２】高電圧検出回路４２は図２において示した高電圧検出回路４２と同様の構成を有するため説明は繰返さない。高温検出回路２０２は図６に示した高温検出回路２０２と同様の構成を有するため説明は繰返さない。

【００８３】保持回路３１６は、図３に示した保持回路５２や図４に示した保持回路５２ａと同様な構成を有するものを用いることができる。

【００８４】以上のような構成にすることによって、設定どおりの高温高電圧が印加されたか否かを確認することが可能となる。

【００８５】［実施の形態５］実施の形態５では、図１に示した条件検出回路３６に代えて条件検出回路４００を備える。

【００８６】図８は、条件検出回路４００の構成を示すブロック図である。図８を参照して、条件検出回路４００は、高電圧検出回路４２と、高電圧検出回路４２の出力を受ける直列に接続されたインバータ４０２、４０４と、高温検出回路２０２と、高温検出回路２０２の出力を受けて反転するインバータ４０６と、アドレス信号Ａ０～Ａｉの状態に応じてテストモードを検出し、テスト信号ＴＥＳＴ、φ１、φ２を出力するテストモード回路４２０と、インバータ４０４の出力とインバータ４０６の出力とテスト信号φ１とを受ける３入力のＮＡＮＤ回路４０８と、ＮＡＮＤ回路４０８の出力を受けて反転するインバータ４１０とテスト信号ＴＥＳＴの活性化時にインバータ４１０の出力に応じた情報を保持する保持回路４１６と、テストモード信号ＴＥＳＴの活性化時に保持回路４１６の保持する情報に応じた信号を受けて端子Ｔｏｕｔ１に出力する出力回路４１８とを含む。

【００８７】条件検出回路４００は、さらに、インバータ４０４の出力とインバータ４０６の出力とテスト信号φ２を受ける３入力のＮＡＮＤ回路４１２と、ＮＡＮＤ回路４１２の出力を受けて反転するインバータ４１４と、テストモード信号ＴＥＳＴの活性化時にインバータ４１４の出力に応じた値を情報として保持する保持回路４２２と、テストモード信号ＴＥＳＴの活性化時に保持回路４２２が保持する情報に対応する信号を受けて端子Ｔｏｕｔ２に出力する出力回路４２４とを含む。

【００８８】保持回路４１６，４２２は、図３に示した保持回路５２や図４に示した保持回路５２ａと同様な構成を有するものを用いることができる。

【００８９】テストモード回路４２０はテスト時における異なる時間においてテスト信号φ、φ２を活性化する。たとえば、バーンイン試験開始直後にテスト信号φ１をＨレベルに活性化しバーンイン試験開始時の条件を保持回路４１６に保持する。バーンイン試験終了直前には、テスト信号φ２をＨレベルに活性化し、条件検出結果を保持回路４２２に書込む。

【００９０】このようにすれば、保持回路４１６、４２２の保持するデータがともに所定の条件を満たしていることを確認することで、バーンイン試験期間中適切な試験電圧および試験温度であったことが確認できる。さらに保持回路を増やし、試験中の異なる時間におけるデータを定期的にサンプリングすることも可能である。

【００９１】［実施の形態６］実施の形態６では、図１における条件検出回路３６に代えて条件検出回路５００を備える。

【００９２】図９は、条件検出回路５００の構成を示すブロック図である。図９を参照して、条件検出回路５００は、高電圧検出回路１０２と、高電圧検出回路１０２の出力を受ける直列に接続されたインバータ５０４、５０６と、一方の入力がＨレベルに固定され、他方の入力にインバータ５０６の出力を受けるＮＡＮＤ回路５０８と、ＮＡＮＤ回路５０８の入力を受けて反転するインバータ５１０と、アドレス信号Ａ０～Ａｉの状態に応じてテストモード信号ＴＥＳＴを活性化するテストモード回路５１６と、テストモード信号ＴＥＳＴが活性化しているときにインバータ５１０の出力に応じた情報を保持する保持回路５１２と、テストモード信号ＴＥＳＴが活性化時に保持回路５１２の保持する情報に応じた信号を端子Ｔｏｕｔに出力する出力回路５１４とを含む。

【００９３】高電圧検出回路１０２には、内部電源電位Ｖｃｃを昇圧電源発生回路５０２によって昇圧した昇圧

電位Ｖｐｐが与えられている。昇圧電位Ｖｐｐは、メモリセルアレイのワード線の活性化電位等として用いられる。高電圧検出回路１０２は、図５における高電圧検出回路１０２と同様の構成を有するため説明は繰返さない。

【００９４】昇圧電源回路５０２は、内部電源電位より高い昇圧電位Ｖｐｐを発生するもので、バーンイン試験時においては、内部電源電位Ｖｃｃが高く設定されるので、通常時よりさらに高い電圧が発生されている。この場合において異常に高い電圧になると内部の回路が破壊されるおそれがあるため、昇圧電位Ｖｐｐがバーンイン試験時に設計された値になっているかどうか確認することが重要である。このような構成とすることによって昇圧電位Ｖｐｐのチェックをすることも可能となる。

【００９５】今回開示された実施の形態はすべての点で例示であって制限的なものではないと考えられるべきである。本発明の範囲は上記した説明ではなくて特許請求の範囲によって示され、特許請求の範囲と均等の意味および範囲内でのすべての変更が含まれることが意図される。

【００９６】

【発明の効果】請求項１に記載の半導体記憶装置は、半導体記憶装置が適切な条件で試験されたか否かを半導体記憶装置ごとに確認することができる。

【００９７】請求項２に記載の半導体記憶装置は、請求項１に記載の半導体記憶装置が奏する効果に加えて、半導体記憶装置が適切な電圧以上で試験されたか否かを半導体記憶装置ごとに確認することができる。

【００９８】請求項３に記載の半導体記憶装置は、請求項２に記載の半導体記憶装置が奏する効果に加えて、半導体記憶装置が適切な電圧範囲で試験されたか否かを半導体記憶装置ごとに確認することができる。

【００９９】請求項４に記載の半導体記憶装置は、請求項２に記載の半導体記憶装置が奏する効果に加えて、半導体記憶装置内部で発生する電源電圧が適切な電圧以上で試験されたか否かを半導体記憶装置ごとに確認することができる。

【０１００】請求項５に記載の半導体記憶装置は、請求項１に記載の半導体記憶装置が奏する効果に加えて、半導体記憶装置が適切な温度以上で試験されたか否かを半導体記憶装置ごとに確認することができる。

【０１０１】請求項６に記載の半導体記憶装置は、請求項１に記載の半導体記憶装置が奏する効果に加えて、半導体記憶装置が適切な条件で試験されたか否かを試験中の複数の時刻において半導体記憶装置ごとに確認することができる。

【０１０２】請求項７、８に記載の半導体記憶装置は、請求項１に記載の半導体記憶装置が奏する効果に加えて、半導体記憶装置が適切な条件で試験されたか否かを試験直後の通電状態において、半導体記憶装置ごとに確認することができる。

【０１０３】請求項９～１１に記載の半導体記憶装置は、請求項１に記載の半導体記憶装置が奏する効果に加えて、半導体記憶装置が適切な条件で試験されたか否かを試験後に一旦電源断状態となった後でも、半導体記憶装置ごとに確認することができる。

【０１０４】請求項１２に記載の半導体記憶装置は、バーンイン試験において半導体記憶装置が適切な条件で試験されたか否かを半導体記憶装置ごとに確認することができる。

【図面の簡単な説明】

【図１】　本発明の実施の形態１の半導体記憶装置１の構成を示す概略ブロック図である。

【図２】　図１に示した条件検出回路３６の構成を示すブロック図である。

【図３】　図２における保持回路５２の構成を示す回路図である。

【図４】　保持回路５２の他の例である保持回路５２ａの構成を示す回路図である。

【図５】　条件検出回路１００の構成を示すブロック図である。

【図６】　条件検出回路２００の構成を示すブロック図である。

【図７】　条件検出回路３００の構成を示すブロック図である。

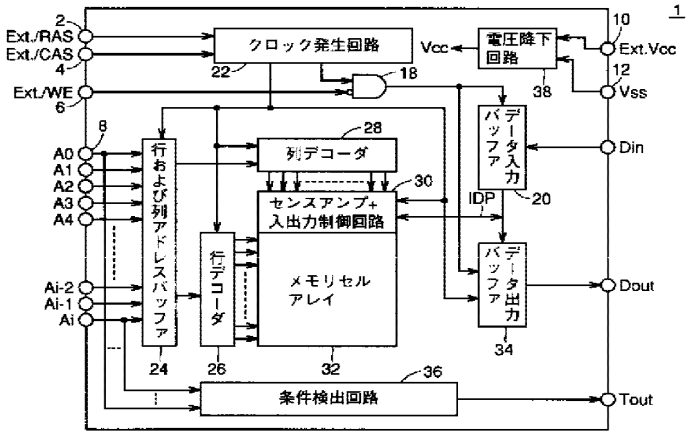
【図８】　条件検出回路４００の構成を示すブロック図である。

【図９】　条件検出回路５００の構成を示すブロック図である。

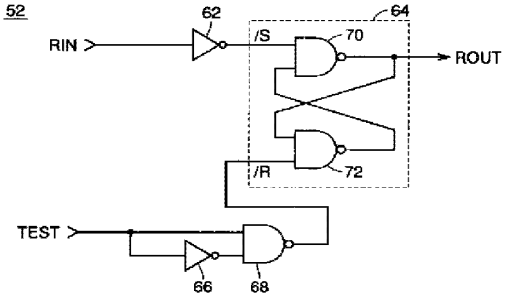
【符号の説明】

１　半導体装置、３６　条件検出回路、３８　電圧降下回路、４２，１０２高電圧検出回路、５２，１１２，１３２，２１０，３１６，４１６，４２２　保持回路、５４，１１４，１３４，２１２，３１８，４１８，４２４　出力回路、５６，１１６，２１４，３２０，４２０　テストモード回路、６４　ラッチ、７５　パルス発生回路、７６　高電圧発生回路、７８　不揮発性データ保持回路、２０２　高温検出回路。

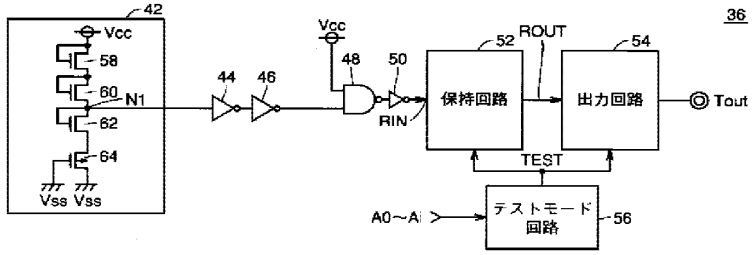
【図１】


Ext./RAS
Ext./CAS
Ext./WE
A0
A1
A2
A3
A4
Ai-2
Ai-1
Ai
クロック発生回路
電圧降下回路
Vcc
Ext.Vcc
Vss
Din
Dout
Tout
行および列アドレスバッファ
行デコーダ
列デコーダ
センスアンプ+入出力制御回路
メモリセルアレイ
データ入力バッファ
データ出力バッファ
IDP
条件検出回路

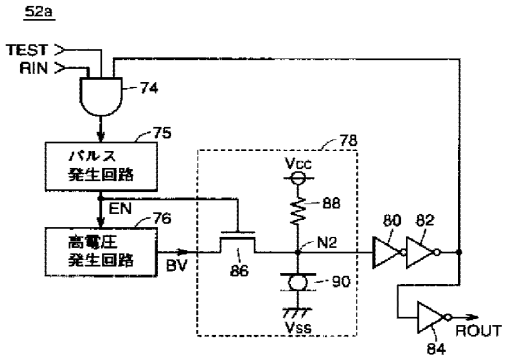
【図３】


RIN
/S
/R
ROUT
TEST

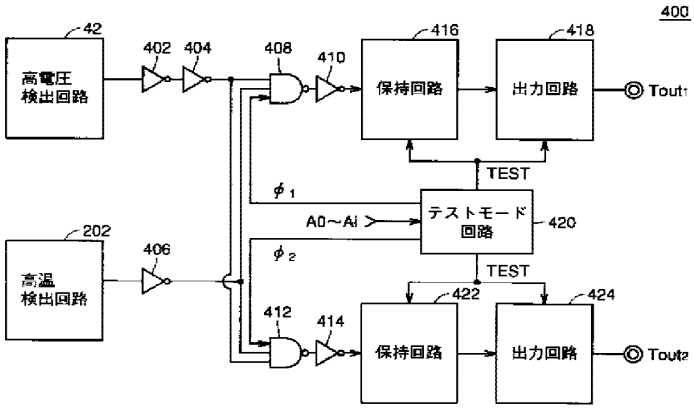
【図２】


Vcc
N1
Vss
RIN
保持回路
出力回路
Tout
TEST
A0～Ai
テストモード回路

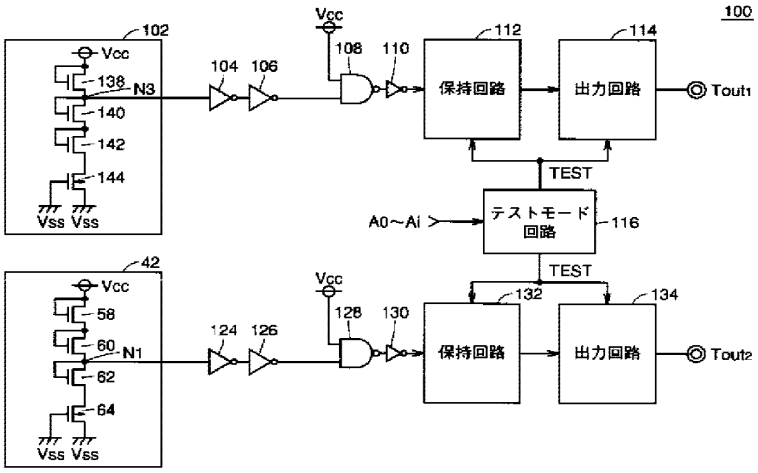
【図４】


TEST
RIN
パルス発生回路
高電圧発生回路
EN
BV
Vcc
N2
Vss
ROUT

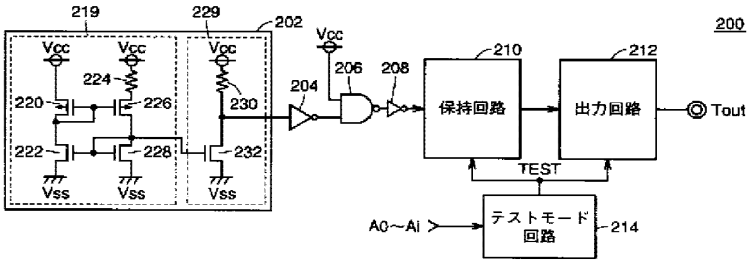
【図８】


高電圧検出回路
高温検出回路
保持回路
出力回路
Tout1
Tout2
TEST
テストモード回路
A0～Ai

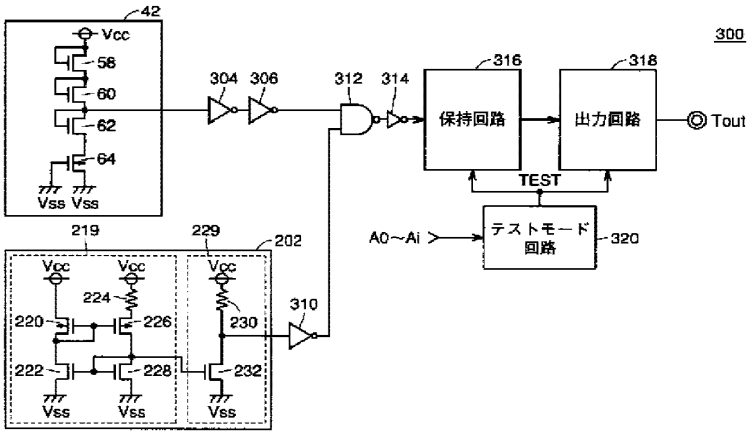
【図５】


100
102
Vcc
138
N3
140
142
144
Vss Vss
104 106
Vcc
108 110
112
保持回路
114
出力回路
Tout1
TEST
A0～Ai
テストモード回路
116
42
Vcc
58
60
N1
62
64
Vss Vss
124 126
Vcc
128 130
132
保持回路
134
出力回路
Tout2

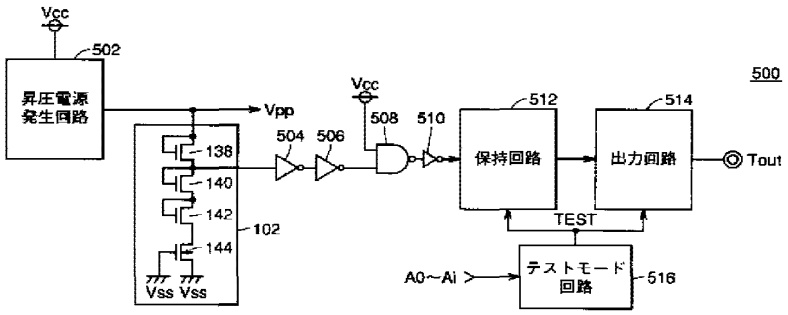
【図６】


200
219
229
202
Vcc
224
220
226
230
222
228
232
Vss
204
Vcc
206 208
210
保持回路
212
出力回路
Tout
TEST
A0～Ai
テストモード回路
214

【図７】


300
42
Vcc
58
60
62
64
Vss Vss
304 306
312 314
316
保持回路
318
出力回路
Tout
TEST
A0～Ai
テストモード回路
320
219
229
202
Vcc
224
220
226
230
222
228
232
Vss
310

【図９】


Vcc
502
昇圧電源
発生回路
Vpp
138
140
142
144
102
Vss Vss
504
506
Vcc
508
510
512
保持回路
514
出力回路
500
Tout
TEST
A0～Ai
テストモード
回路
516

PAT-NO: JP02001035193A
DOCUMENT-IDENTIFIER: JP 2001035193 A
TITLE: SEMICONDUCTOR MEMORY
PUBN-DATE: February 9, 2001

INVENTOR-INFORMATION:

NAME	COUNTRY
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NAME	COUNTRY
MITSUBISHI ELECTRIC CORP	N/A

APPL-NO: JP11202882
APPL-DATE: July 16, 1999

INT-CL (IPC): G11C029/00 , G01R031/28 , G06F011/24 , G06F012/16 , G11C011/401

ABSTRACT:

PROBLEM TO BE SOLVED: To provide a semiconductor memory which can examine whether a burn-in test and the like are performed by appropriate conditions or not for each semiconductor memory.

SOLUTION: This device is provided with a high voltage detecting circuit 42 detecting that test

voltage at the time of burn-in test exceeds the prescribed voltage, a holding circuit 52 holding a detected result, and an output circuit 54 outputting holding contents of the holding circuit 52 to the outside. It can be understood whether internal power source voltage internally generated is made appropriate value or not by making observing test voltage as internal power source voltage. Preferably, a range of voltage can be specified by providing a high voltage detecting circuit detecting plural different voltage and a holding circuit holding corresponding detected result. Further, also temperature conditions can be verified by incorporating a high temperature detecting circuit.

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Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/888,667	ZHANG ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

SEARCHED			
Class	Subclass	Date	Examiner
327	536,537 143,82,60, 63	11/9/2005	TH
363	60	11/9/2005	TH
Updated	above	4/6/2006	TH
Updated	above	9/27/2006	TH
363	63	9/28/2006	TH
Updated	above	3/1/2007	TH
363	59	3/1/2007	TH
365	189.09	3/1/2007	TH
Updated	above	1/23/2008	TH

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
See attached EAST text search	11/14/2005	TH
See attached EAST text search	4/10/2006	TH
See attached EAST text search	9/28/2006	TH
See attached EAST text search	3/7/2007	TH
See attached EAST text search	1/25/2008	TH

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10888667	ZHANG ET AL.
	Examiner	Art Unit
	Thomas J Hiltunen	2816

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	01/25/2008								
	1	✓								
	2	O								
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	26	O								
	27	O								
	28	✓								
	29	O								
	30	O								
	31	O								
	32	O								

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	8253	(burnin burn adj in burn$1in) with (detect$4 mode test $4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/01/25 08:52
L2	60	1 same (charge adj pump$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/01/25 08:52
L8	642	(burnin burn adj in burn$1in) with (detect$4 mode test $4).ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/01/25 09:07
L9	13	8 and charge adj pump	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/01/25 09:07
L11	18	8 and high adj voltage with detect $4	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/01/25 09:08
L12	189	1 and high adj voltage with detect $4	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/01/25 09:16
L21	5729	(detect$4 compar $4) with (vpp (high boost$4 pump$4) near2 voltage) with (supply near2 voltage vdd vcc)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/01/25 10:27
L22	24	1 same 21	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/01/25 10:28
S13	509893	switch$4 near2 circuit mux multiplexer multiplexor select $4 near2 circuit	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/23 12:43

S14	857470	(boost$4 pump$4 high$4 big$4 large) near2 (supply power source voltage) vpp vcc2 2vcc "2" adj vcc vdd2 2vdd "2" adj vdd	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/23 12:45
S15	1372816	(power supply voltage source) near2 (supply power source voltage) vcc vdd	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/23 12:46
S16	7149	S13 with S14 with S15	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/23 12:47
S17	112723	(charge voltage current) near3 (multipl$4 multiplication pump $4)	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/23 12:48
S18	724	S16 same S17	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/23 12:48
S26	2142	S16 and S17	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/23 15:37
S27	674203	(output voltage source supply) with detect$4	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/23 15:37
S28	1170	S26 and S27	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/23 15:38
S29	844	S28 not S18	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/23 15:38
S30	2	(vpp with vbb) with (generat$4 pump $4) same bootstrap $4	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/23 15:39
S31	13	(vpp) with (generat $4 pump$4) and (vbb) with (generat $4 pump$4) and bootstrap$4	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/23 15:41
S42	15294	inverter with S27	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/23 16:48

S43	2337	S42 and S17	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/23 16:49
S44	2141	S43 not (S18 S29)	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/23 16:49
S45	1130	S44 and S13	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/23 16:49
S46	224	S45 and (pre adj charg$4 precharg $4 pre$1charg$4)	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/23 16:50
S47	927	S45 not (pll dll)	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/23 16:51
S48	752	S47 not S46	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/23 16:51
S55	20	(burn adj in burn $1in burnin) with detect$4 and inverter same vpp same (vcc vdd)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/01/24 11:40
S67	53266	(increas$4 fast$4 speed$4 quick$4 great$4 high$4) with (ramp adj up rampup ramp$1up (boost$4 charg$4 pump$4) near2 (rate time))	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/24 13:42
S68	112858	(charge voltage current) near3 (multipl$4 multiplication pump $4)	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/24 13:43
S69	510315	switch$4 near2 circuit mux multiplexer multiplexor select $4 near2 circuit	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/24 13:43
S70	1463	S67 same S68	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/24 13:43
S71	574	S70 and S69	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/24 13:45

S83	20	(burnin burn adj in burn$1in) with (detect$4) same S68	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/24 15:58
S92	5	(burnin burn adj in burn$1in) with (detect$4).ti.	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/24 16:26
S94	9	(burnin burn adj in burn$1in) with test $4 with mode.ti.	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/24 16:29
S95	805	(burnin burn adj in burn$1in).ti.	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/24 16:30
S99	17	S95 and high adj voltage with inverter	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/24 16:56
S100	52	S95 and high with voltage with detect $4	US-PGPUB; USPAT; USOCR	OR	ON	2008/01/24 16:58

1/25/2008 11:04:30 AM
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[JP,2001-035193,A]

Japanese (PDF)

File Wrapper Information

FULL CONTENTS CLAIM + DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS DESCRIPTION OF DRAWINGS DRAWINGS

[Translation done.]

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This English translation is produced by machine translation and may contain errors.The JPO, the INPIT, and and those who drafted this document in the original language are not responsible for the result of the translation.

Notes:
1. Untranslatable words are replaced with asterisks (****).
2. Texts in the figures are not translated and shown as it is.

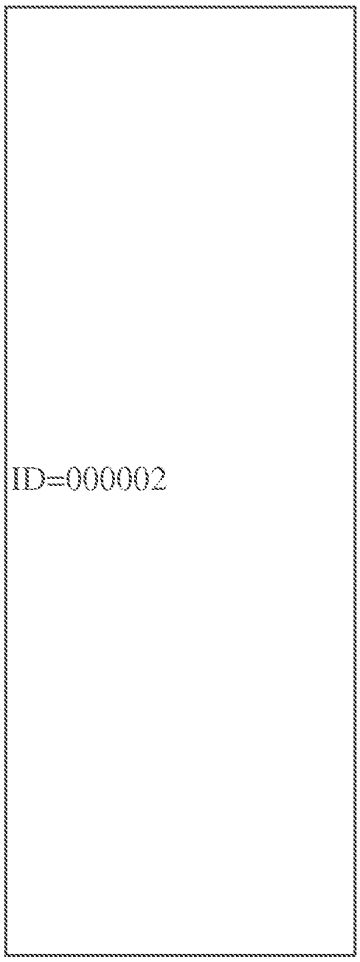
Translated: 23:50:49 JST 01/28/2008
Dictionary: Last updated 01/18/2008 / Priority:

CLAIMS

[Claim(s)]
[Claim 1] A semiconductor memory device equipped with the detector circuit which detects the test conditions at the time of a test, the holding circuit held in response to the output of said detector circuit, and the output circuit which reads the output of said holding circuit.
[Claim 2] Said detector circuit is the semiconductor memory device according to claim 1 including the 1st voltage detector circuit which detects that test voltage exceeded the 1st voltage.
[Claim 3] Said detector circuit is a semiconductor memory device according to claim 2 which includes further the 2nd

Drawing selection

Representative drawi



[Translation done.]

voltage detector circuit which detects that said test voltage exceeded the 2nd voltage higher than said 1st voltage.
[Claim 4] It is the semiconductor memory device according to claim 2 said whose test voltage it has further the voltage generating circuit which generates internal electrical power source voltage in response to the power supply voltage given from the outside, and the memory array which operates with said internal electrical power source voltage, and is said internal electrical power source voltage.
[Claim 5] Said detector circuit is the semiconductor memory device according to claim 1 including the temperature detector circuit which detects the temperature at the time of a test.
[Claim 6] Said holding circuit is the semiconductor memory device according to claim 1 including the 1st data-hold circuit which is activated in the 1st time and holds the output of said detector circuit, and the 2nd data-hold circuit which is activated in the 2nd time after said 1st time, and holds the output of said detector circuit.
[Claim 7] Said holding circuit is the semiconductor memory device according to claim 1 including the volatile data-hold circuit held in response to the output of said detector circuit.
[Claim 8] Said volatile data-hold circuit is the semiconductor memory device according to claim 7 including the latch circuitry held in response to the output of said detector circuit.
[Claim 9] Said holding circuit is the semiconductor memory device according to claim 1 including the fixity data-hold circuit held in response to the output of said detector circuit.
[Claim 10] Said fixity data-hold circuit is the semiconductor memory device according to claim 9 containing the electric fuse to which the switch-on between one end and the other end is changed according to an electric signal.
[Claim 11] Said electric fuse is a semiconductor memory device according to claim 10 which will be in switch-on if bigger voltage than predetermined voltage is impressed to both ends and which is an antifuse.
[Claim 12] Said test is a semiconductor memory device according to claim 1 which is a burn-in examination.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]

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[Field of the Invention] More specifically, this invention relates to the semiconductor memory device which has a circuit relevant to the examination for reliability assessment about a semiconductor memory device.

[0002]

[Description of the Prior Art] In recent years, the miniaturization of a MOS transistor progresses by high integration of a semiconductor device, and the thickness of the gate oxide of a MOS transistor also tends to decrease in connection with it every year. For this reason, if pressure-proofing of gate oxide falls and gate voltage is set up highly, the reliability of a MOS transistor may be affected.

[0003] For example, in the system by which a semiconductor memory device is used, the voltage required for internal operation of a semiconductor memory device may be lower than the power supply voltage of the system itself. In such a case, in order to supply the power supply voltage of a semiconductor memory device from the power supply voltage of the system itself, voltage is dropped inside a semiconductor memory device and internal electrical power source voltage required for operation of a semiconductor memory device is generated in many cases.

[0004] Thus, the circuit which generates internal electrical power source voltage is called a voltage drop circuit. By using such a voltage drop circuit, the power consumption of a semiconductor memory device can be reduced greatly, and can stabilize the internal electrical power source voltage inside a semiconductor memory device.

[0005] Next, the examination for reliability assessment is explained. Generally the period when failure occurs in a semiconductor device is divided roughly into three periods. This period is an early failure period, a chance failure period, and a wear failure period in order of progress of time.

[0006] The defect at the time of creation of a semiconductor device is what appeared as failure, and an early failure period is a period when the early failure generated immediately after the beginning of using occurs. The rate of this early failure decreases quickly with time.

[0007] It becomes the chance failure period which a low failure rate is long during a fixed period after that, and continues. Soon, a semiconductor device approaches a life and becomes the wear failure period when a failure rate

increases rapidly.
[0008] As for a semiconductor device, it is desirable to use it within a chance failure period. Therefore, in order to raise the reliability of a semiconductor device, it is necessary to remove beforehand the semiconductor device which early failure generates. For this reason, acceleration operation aging of a definite period of time is performed to a semiconductor device, and screening which removes inferior goods is performed. In order to screen effectively for a short period of time, it is desirable to do an examination which the rate of early failure decreases quickly to time, and enters early at a chance failure period.
[0009] Generally the high temperature operation test (burn-in examination) is done as one of the screening techniques of these now. A burn-in examination is the technique of the ability to carry out the direct valuation of the dielectric film using a real device, and is an examination actualized by impressing the migration of aluminum wiring and impressing the stress of high **** for all poor factors in the beginning.
[0010] If especially this burn-in examination operates a semiconductor device in high temperature and acceleration nature is raised, it will become effective.
[0011]
[Problem to be solved by the invention] In the conventional semiconductor memory device, since there was no function in which test conditions are detectable inside a semiconductor memory device, there was a problem that there was no telling whether the burn-in examination was done on relevant conditions.
[0012] For example, the appearance of a semiconductor memory device does not change before and after a burn-in examination. Therefore, sufficient cautions are required for distinction of the product before and behind an examination. In such a case, it is convenient, if it holds inside that the burn-in examination was done on the semiconductor memory device for every semiconductor memory device and can read electrically in the test at the time of shipment.
[0013] Moreover, it is convenient if it can be known after a burn-in examination whether a condition setup, for example, a setup of temperature conditions or voltage conditions, was made suitable to the semiconductor memory device by burn-in test equipment.

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[0014] Furthermore, if the internal electrical power source voltage generated by the voltage drop circuit which a semiconductor memory device contains at this time does not change, it does not mean carrying out an accelerated test, although power supply voltage given from the outside at the time of a burn-in examination is made into the predetermined high voltage. Therefore, operation usually switches so that a voltage drop circuit may generate internal electrical power source voltage usually still higher than the internal electrical power source voltage at the time at the time of a burn-in examination. If it can be detected and held whether the change of this voltage drop circuit of operation was performed normally, the reliability of a burn-in examination will go up further.
[0015] The purpose of this invention is to offer the semiconductor memory device which can check whether a test condition setup at the time of performing a burn-in examination etc. has been made correctly for every semiconductor memory device.
[0016]
[Means for solving problem] A semiconductor memory device according to claim 1 is equipped with the detector circuit which detects the test conditions at the time of a test, the holding circuit held in response to the output of a detector circuit, and the output circuit which reads the output of a holding circuit.
[0017] In addition to the composition of a semiconductor memory device according to claim 1, a semiconductor memory device according to claim 2 includes the 1st voltage detector circuit where a detector circuit detects that test voltage exceeded the 1st voltage.
[0018] As for a semiconductor memory device according to claim 3, in addition to the composition of a semiconductor memory device according to claim 2, a detector circuit includes further the 2nd voltage detector circuit which detects that test voltage exceeded the 2nd voltage higher than the 1st voltage.
[0019] In addition to the composition of a semiconductor memory device according to claim 2, a semiconductor memory device according to claim 4 is further equipped with the voltage generating circuit which generates internal electrical power source voltage in response to the power supply voltage given from the outside, and the memory

array which operates with internal electrical power source voltage, and test voltage is internal electrical power source voltage.
[0020] In addition to the composition of a semiconductor memory device according to claim 1, a semiconductor memory device according to claim 5 includes the temperature detector circuit where a detector circuit detects the temperature at the time of a test.
[0021] A semiconductor memory device according to claim 6 in the composition of a semiconductor memory device according to claim 1 [in addition, a holding circuit] The 1st data-hold circuit which is activated in the 1st time and holds the output of a detector circuit, and the 2nd data-hold circuit which is activated in the 2nd time after the 1st time, and holds the output of a detector circuit are included.
[0022] In addition to the composition of a semiconductor memory device according to claim 1, a semiconductor memory device according to claim 7 includes the volatile data-hold circuit which holds a holding circuit in response to the output of a detector circuit.
[0023] In addition to the composition of a semiconductor memory device according to claim 7, a semiconductor memory device according to claim 8 includes the latch circuitry which holds a volatile data-hold circuit in response to the output of a detector circuit.
[0024] In addition to the composition of a semiconductor memory device according to claim 1, a semiconductor memory device according to claim 9 includes the fixity data-hold circuit which holds a holding circuit in response to the output of a detector circuit.
[0025] In addition to the composition of a semiconductor memory device according to claim 9, in a fixity data-hold circuit, a semiconductor memory device according to claim 10 contains the electric fuse to which the switch-on between one end and the other end is changed according to an electric signal.
[0026] A semiconductor memory device according to claim 11 is an antifuse from which it will be in switch-on if voltage with an electric bigger fuse than predetermined voltage is impressed to both ends in the composition of a semiconductor memory device according to claim 10.
[0027] In the composition of a semiconductor memory device according to claim 1, the test of a semiconductor

memory device according to claim 12 is a burn-in examination.
[0028]
[Mode for carrying out the invention] The form of operation of this invention is explained in detail with reference to Drawings below. In addition, a same-among figure mark shows the same or a considerable portion.
[0029] [Form 1 of operation] Drawing 1 is the outline block diagram showing the composition of the semiconductor memory device 1 of the form 1 of operation of this invention.
[0030] The control signal input terminals 2-6 with which the semiconductor memory device 1 receives control signal ext./RAS, ext./CAS, and ext./WE with reference to drawing 1 , respectively, It has the address input terminal group 8, the input terminal Din which inputs a data signal, the output terminal Dout which outputs a data signal and the grounding terminal 12 with which the grounding potential Vss is given, and the power supply terminal 10 with which power supply potential Ext.Vcc is given.
[0031] Further the semiconductor memory device 1 The clock generation circuit 22, and a line and the sequence address buffer 24, It has the line decoder 26, the sequence decoder 28, the sense amplifier + input-and-output control circuit 30, the memory cell array 32, the gate circuit 18, and the data input buffer 20 and the data output buffer 34.
[0032] The clock generation circuit 22 generates the control clock equivalent to the predetermined mode of operation based on external line address strobe ext./RAS and external sequence address strobe ext./CAS which are given from the outside through the control signal input terminals 2 and 4. Operation of the whole semiconductor memory device is controlled.
[0033] A line and the sequence address buffer 24 give the address signal generated based on the address signals A0-Ai (i is a natural number) given from the outside to the line decoder 26 and the sequence decoder 28.
[0034] [the memory cell in the memory cell array 32 specified by the line decoder 26 and the sequence decoder 28] The exterior and data are exchanged through the input-and-output terminal Din or the output terminal Dout through the sense amplifier + input-and-output control circuit 30, the data input buffer 20, or the data output buffer 22.

[0035] The condition detector circuit 36 which the semiconductor memory device 1 detects test conditions further in the test mode according to a setup of the address signals A0-Ai, and holds a detection result, The voltage drop circuit 38 which outputs the internal electrical power source potential Vcc in response to Terminal Tout, external power-supply-voltage Ext.Vcc, and the grounding potential Vss for outputting the maintenance result of the condition detector circuit 36 is included.
[0036] The semiconductor memory device 1 shown in drawing 1 is a typical example, for example, can apply this invention also to a synchronous semiconductor memory device (SDRAM).
[0037] Drawing 2 is the block diagram showing the composition of the condition detector circuit 36 shown in drawing 1 . The high-voltage detector circuit 42 which detects whether the condition detector circuit 36 was set as high potential predetermined in the internal electrical power source potential Vcc with reference to drawing 2 , Two inverters 44 and 46 which undergo the output of the high-voltage detector circuit 42 and which were connected in series, It is fixed to H level, and one input is reversed in response to the output of NAND circuit 48 which receives the output of an inverter 46 in the input of another side, and NAND circuit 48, and contains the inverter 50 which outputs Signal RIN.
[0038] The test mode circuit 56 which the condition detector circuit 36 detects a test mode further according to a setup of the address signals A0-Ai, and outputs the test signal TEST, The holding circuit 52 which holds the information corresponding to test conditions according to activation of Signal RIN when the test mode signal TEST is activated, and the output circuit 54 which outputs the signal ROUT according to the information which the holding circuit 52 holds to Terminal Tout at the time of activation of the test signal TEST are included.
[0039] Detect that the test mode circuit 56 is a test mode when potential higher than power supply potential is given to a predetermined terminal for example, among the terminals with which the address signals A0-Ai are given, and [with the setting state of other terminals at that time] A test signal is outputted in order to carry out control which detects and corresponds [which test is done and].

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[0040] N channel MOS transistor 58 by which a gate and a drain are combined with the internal electrical power source potential Vcc in both the high-voltage detector circuits 42, N channel MOS transistor 60 by which both a gate and a drain are connected to the source of N channel MOS transistor 58, and a source is connected to a node N1, A gate and a drain contain N channel MOS transistor 62 connected to a node N1, and P channel MOS transistor 64 by which both a gate and a drain are connected to the grounding potential Vss, and a source is connected to the source of N channel MOS transistor 62.

[0041] The potential of a node N1 serves as voltage by threshold voltage of N channel MOS transistors 58 and 60 lower than the internal electrical power source potential Vcc. Usually, since power supply voltage is low at the time of use, the potential of the node N1 which is the output of a high-voltage detector circuit serves as L level.

[0042] In order to screen early failure inferior goods at the time of a burn-in examination, the high voltage set up beforehand is given from the outside, and the internal electrical power source potential Vcc also serves as voltage higher than usual. At this time, the output of the high-voltage detector circuit 42 exceeds the input threshold voltage of an inverter 44, and the signal RIN which performs the writing to the holding circuit 52 serves as H level.

[0043] Drawing 3 is the circuit diagram showing the composition of the holding circuit 52 in drawing 2 . The inverter 62 which reverses the holding circuit 52 in response to Signal RIN, and outputs /S with reference to drawing 3 , The inverter 66 which receives the test signal TEST, the output of an inverter 66 and NAND circuit 68 which outputs a signal/R in response to the test signal TEST, and the latch circuitry 64 which is set when a signal/S is L levels, and is reset when a signal/R is L levels are included.

[0044] The latch circuitry 64 contains NAND circuit 70 which receives a signal/S in one input, and outputs the signal ROUT which is the output of the holding circuit 52, and NAND circuit 72 which receives a signal /R, and Signal ROUT. The output of NAND circuit 72 is connected to the input of another side of NAND circuit 70. The latch circuitry 64 is reset by the pulse signal generated by the inverter 66 and NAND circuit 68 at the time of the standup

of the test signal TEST, and data is set when the signal RIN which is a holding circuit input is activated by H level. When data is set to the latch circuitry 64, it turns out that Signal ROUT was set to H level and the burn-in examination of the semiconductor device was done on suitable voltage.

[0045] The composition of the holding circuit shown in drawing 3 was the example of the usable volatile circuit, when judging holding power supply voltage immediately after a burn-in examination, but if it uses the storage cell of fixity, the judgment of it will be attained also in the delivery inspection after making a power supply into a disconnection state.

[0046] Drawing 4 is the circuit diagram showing the composition of the holding circuit 52a which are other examples of the holding circuit 52.

[0047] AND circuit 74 of 3 inputs which the holding circuit 52a receives Signal RIN in the 1st input, and receives the test signal TEST in the 2nd input with reference to drawing 4 , The pulse generating circuit 75 which activates the enabling signal EN intermittently when the output of AND circuit 74 is H level, The high-voltage generating circuit 76 which outputs the high voltage BV according to activation of the enabling signal EN, The fixity data-hold circuit 78 which performs data-hold in response to the high voltage BV at the time of activation of the enabling signal EN, The inverters 80 and 82 which undergo the output of the fixity data-hold circuit 78 and which were connected in series, and the inverter 84 which is reversed in response to the output of an inverter 82, and outputs Signal ROUT are included. The output of an inverter 82 is also given to the 3rd input of AND circuit 74.

[0048] N channel MOS transistor 86 which the fixity data-hold circuit 78 delivers the high voltage BV to a node N2 when the enabling signal EN is H level, The resistance 88 connected between the power supply node and node N2 to which the internal electrical power source potential Vcc is given, and the antifuse 90 connected between the grounding node and node N2 to which the grounding potential Vss is given are included. From a node N2, the output signal of the fixity data-hold circuit 78 is outputted.

[0049] In order to memorize information, laser beams and an electric signal are impressed to specific FUYUZU, and it

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is called blow to change electric character. Although anti FUYUZU is a kind of electric FUYUZU, it has the character in which inter-electrode flows by blowing.

[0050] As shown in JP,H7-37984,A, when anti FUYUZU 90 has high resistance and suitable voltage is impressed before a blow, it is an element to which the switch-on is changed to low resistance. Anti FUYUZU has capacitor type structure, for example, sandwiches a thin insulating layer like 2 silicon oxides between two electric conduction layers like aluminum. If it remains as it is, it is a capacitor, i. e., an open circuit, but if the high voltage is impressed and blown, a conductive path will be generated in an insulating layer, and it becomes a resistive element with the resistance which is about several kohms.

[0051] In addition, it is possible to replace with the fixity data-hold circuit 78, and to hold data in fixity also as composition using the transistor which has the floating gate used for the flash memory etc. Of course, it may replace with the holding circuit 52a, and the flash memory itself may be used.

[0052] If a holding circuit is constituted from a data-hold circuit of fixity as mentioned above, the judgment of whether also in the delivery inspection once making a power supply into a disconnection state after a burn-in examination, the burn-in examination was done normally is possible. Furthermore, even when failure occurs after shipment, it can also be used for the analysis of whether the burn-in examination was done normally.

[0053] [Form 2 of operation] With the form 2 of operation, it replaces with the condition detector circuit 36 in drawing 1 , and has the condition detector circuit 100.

[0054] Drawing 5 is the block diagram showing the composition of the condition detector circuit 100. With reference to drawing 5 , the condition detector circuit 100 The high-voltage detector circuit 102, The inverters 104 and 106 which undergo the output of the high-voltage detector circuit 102 and which are connected in series, NAND circuit 108 which one input is fixed to H level and receives the output of an inverter 106 in the input of another side, The inverter 110 reversed in response to the output of NAND circuit 108, and the test mode circuit 116 which activates the test signal TEST according to a setup of the address signals A0-Ai, The holding circuit 112 which holds the value

according to the output of the inverter 110 inside at the time of activation of the test signal TEST, and the output circuit 114 outputted from terminal Tout1 in response to the output of the holding circuit 112 at the time of activation of the test signal TEST are included.

[0055] The inverters 124 and 126 with which the condition detector circuit 100 undergoes the output of the high-voltage detector circuit 42 and the high-voltage detector circuit 42 further and which were connected in series, NAND circuit 128 which one input is fixed to H level and receives the output of an inverter 126 in the input of another side, The inverter 130 reversed in response to the output of NAND circuit 128, and the holding circuit 132 which holds the value according to the output of the inverter 130 inside at the time of activation of the test signal TEST, The output circuit 134 outputted to terminal Tout2 in response to the signal according to the information which the holding circuit 132 holds at the time of activation of the test signal TEST is included.

[0056] Since it has the same composition as the high-voltage detector circuit 42 in drawing 2 , the high-voltage detector circuit 42 does not repeat explanation.

[0057] N channel MOS transistor 138 by which a drain and a gate are combined with the internal electrical power source potential Vcc in the high-voltage detector circuit 102, and a source is connected to a node N3, N channel MOS transistor 140 by which a gate and a drain are connected to a node N3, N channel MOS transistor 142 by which a gate and a drain are connected to the source of N channel MOS transistor 140, P channel MOS transistor 144 by which a gate and a drain are combined with the grounding potential Vss, and a source is connected with the source of N channel MOS transistor 142 is included. From a node N3, the output signal of the high-voltage detector circuit 102 is outputted.

[0058] [the high-voltage detector circuit 42] although the voltage of N channel MOS transistors 58 and 60 low by threshold voltage is outputted by the node N1 from the internal electrical power source potential Vcc In the high-voltage detector circuit 102, the potential of N channel MOS transistor 138 low by threshold voltage is outputted from a node N3 from the internal electrical power source potential Vcc.

[0059] Thus, different voltage can be made to detect in two

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high-voltage detector circuits. In this composition, specification of the voltage range impressed to the internal memory cell as internal electrical power source potential Vcc in the burn-in examination is attained.

[0060] That is, in the form 1 of operation, although it is detectable that the value more than a certain power supply voltage was given, if it has composition shown by drawing 5 , it is more than a certain power supply potential, and it is possible to detect that the voltage of under a certain power supply potential was given.

[0061] [Form 3 of operation] In the form 3 of operation, it replaces with the condition detector circuit 36 in drawing 1 , and has the condition detector circuit 200.

[0062] Drawing 6 is the block diagram showing the composition of the condition detector circuit 200. The inverter 204 which reverses the condition detector circuit 200 with reference to drawing 6 in response to the output of the high temperature detector circuit 202 and the high temperature detector circuit 202, NAND circuit 206 which one input is fixed to H level and receives the output of an inverter 204 in the input of another side, The inverter 208 reversed in response to the output of NAND circuit 206, and the test mode circuit 214 which activates the test signal TEST according to a setup of the address signals A0-Ai, The test signal TEST includes the holding circuit 210 which holds the information according to the output of the inverter 208 at the time of activation, and the output circuit 212 which the test mode signal TEST outputs to Terminal Tout in response to the information which the holding circuit 210 holds at the time of activation.

[0063] The high temperature detector circuit 202 contains a primary detecting element 219 and the output part 229 which outputs a signal to an inverter 204 according to the output potential of a primary detecting element 219.

[0064] P channel MOS transistor 220 to which, as for the primary detecting element 219, the source was combined with the internal electrical power source potential Vcc, and the gate and the drain were connected, N channel MOS transistor 222 connected between the drain of P channel MOS transistor 220, and a grounding node, N channel MOS transistor 228 to which a source is connected with a grounding node and a gate and a drain are connected at the gate of N channel MOS transistor 222, P channel MOS

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transistor 226 by which a drain is connected with the drain of N channel MOS transistor 228, and a gate is connected to the drain of P channel MOS transistor 220, The resistance 224 connected between the power supply node to which the internal electrical power source potential Vcc is given, and the drain of P channel MOS transistor 226 is included.
[0065] N channel MOS transistor 232 by which, as for the output part 229, a gate is connected to the drain of N channel MOS transistor 228, and a source is combined with the grounding potential Vss, The resistance 230 connected between the power supply node to which the internal electrical power source potential Vcc is given, and the drain of N channel MOS transistor 232 is included. The potential of the drain of N channel MOS transistor 232 turns into output potential of the high temperature detector circuit 202.
[0066] The current which flows into the resistance 224 which a primary detecting element 219 includes is adjusted so that it may be proportional to the absolute temperature. That is, P channel MOS transistors 220 and 226 can operate in a subSURESSHORUDO current field by choosing the resistance of resistance 224 appropriately.
[0067] In a subSURESSHORUDO current field, the relation between the values, i.e., log (Ids) and the voltage Vgs between gate sources, which took the logarithm of the drain current Ids of a MOS transistor serves as a straight line which has fixed inclination.
[0068] This inclination is called the subSURESSHORUDO coefficient S, and has a relation like the following formula in approximation to temperature. k is the Boltzmann coefficient and T is the absolute temperature.
[0069] S**kT -- (1)
Equal current Ids flows into P channel MOS transistor 220 and P channel MOS transistor 226 by the current Miller circuit constituted by N channel MOS transistors 222 and 228.
[0070] Here, the ratio of the transistor size (W/L) of P channel MOS transistor 220 and P channel MOS transistor 226 is set to 1:10. The following formula will be realized if voltage between gate sources of P channel MOS transistor 220 and P channel MOS transistor 226 is set to Vgs1 and Vgs2, respectively.
[0071] Vgs1-Vgs2=S -- (2)
Moreover, since the potential difference concerning the both

ends of R is Vgs1-Vgs2 when the resistance of resistance 224 is set to R, the following formula is realized.
[0072]
Ids=(Vgs1-Vgs2)/R -- (3)
Therefore, the following formula is drawn from (1) - (3) type.
[0073] Ids=S/R**kT -- (4)
That is, if a semiconductor memory device becomes high temperature, the current value which flows through resistance 224 will increase. It will become equal if transistor size is equal to the current which flows into N channel MOS transistor 228, and the current which flows into N channel MOS transistor 232. Therefore, the current value which flows into N channel MOS transistor 232 will increase too, if the temperature of a semiconductor memory device becomes high temperature. The potential to which the output part 229 will output the resistance of resistance 230 if the current which flows since temperature dependence is small increases becomes low.
[0074] If resistance 230 is made into bigger resistance than resistance 224, big amplitude can be obtained [rather than] to a temperature change.
[0075] Therefore, if it becomes high temperature, it will be held that the output of the inverter 204 was set to H level, responded, the output of the inverter 208 was also set to H level, and the semiconductor memory device became high temperature in the holding circuit 210.
[0076] What has the same composition as the holding circuit 52 shown in drawing 3 or the holding circuit 52a shown in drawing 4 can be used for the holding circuit 210.
[0077] As explained above, in the form 3 of operation, it becomes possible to check whether the semiconductor memory device has been carried out at a suitable temperature at the time of a burn-in examination.
[0078] Moreover, if several high temperature detector circuits where detection temperature differs like drawing 5 are used, specification of the temperature range will be attained.
[0079] [Form 4 of operation] With the form 4 of operation, it replaces with the condition detector circuit 36 shown in drawing 1 , and has the condition detector circuit 300.
[0080] Drawing 7 is the block diagram showing the composition of the condition detector circuit 300. The

inverters 304 and 306 with which the condition detector circuit 300 undergoes the output of the high-voltage detector circuit 42 and the high-voltage detector circuit 42 with reference to drawing 7 and which were connected in series, The high temperature detector circuit 202, the inverter 310 reversed in response to the output of the high temperature detector circuit 202, NAND circuit 312 which undergoes the output of an inverter 306 and the output of an inverter 310, and the inverter 314 reversed in response to the output of NAND circuit 312 are included.

[0081] The test mode circuit 320 which the condition setting circuit 300 detects a test mode further according to a setup of the address signals A0-Ai, and outputs the test mode signal TEST, The holding circuit 316 which holds the value according to the output of the inverter 314 as information according to activation of the test mode signal TEST, and the output circuit 318 outputted to Terminal Tout in response to the signal corresponding to the information which the holding circuit 316 holds according to activation of the test mode signal TEST are included.

[0082] Since it has the same composition as the high-voltage detector circuit 42 shown in drawing 2 , the high-voltage detector circuit 42 does not repeat explanation. Since it has the same composition as the high temperature detector circuit 202 shown in drawing 6 , the high temperature detector circuit 202 does not repeat explanation.

[0083] What has the same composition as the holding circuit 52 shown in drawing 3 or the holding circuit 52a shown in drawing 4 can be used for the holding circuit 316.

[0084] By having the above composition, it becomes possible to check whether the high temperature high voltage as a setting has been impressed.

[0085] [Form 5 of operation] With the form 5 of operation, it replaces with the condition detector circuit 36 shown in drawing 1 , and has the condition detector circuit 400.

[0086] Drawing 8 is the block diagram showing the composition of the condition detector circuit 400. The inverters 402 and 404 with which the condition detector circuit 400 undergoes the output of the high-voltage detector circuit 42 and the high-voltage detector circuit 42 with reference to drawing 8 and which were connected in series, The high temperature detector circuit 202 and the inverter 406 reversed in response to the output of the high

temperature detector circuit 202, The test mode circuit 420 which detects a test mode according to the state of the address signals A0-Ai, and outputs the test signal TEST, phi 1, and phi 2, NAND circuit 408 of 3 inputs which receives the output of an inverter 404, the output of an inverter 406, and the test signal phi 1, The inverter 410 reversed in response to the output of NAND circuit 408, and the holding circuit 416 which holds the information according to the output of the inverter 410 at the time of activation of the test signal TEST, The output circuit 418 outputted to terminal Tout1 in response to the signal according to the information which the holding circuit 416 holds at the time of activation of the test mode signal TEST is included.

[0087] NAND circuit 412 of 3 inputs from which the condition detector circuit 400 receives the output of an inverter 404, the output of an inverter 406, and the test signals phi 2 further, The inverter 414 reversed in response to the output of NAND circuit 412, and the holding circuit 422 which holds the value according to the output of the inverter 414 as information at the time of activation of the test mode signal TEST, The output circuit 424 outputted to terminal Tout2 in response to the signal corresponding to the information which the holding circuit 422 holds at the time of activation of the test mode signal TEST is included.

[0088] What has the same composition as the holding circuit 52 shown in drawing 3 or the holding circuit 52a shown in drawing 4 can be used for the holding circuit 416,422.

[0089] The test mode circuit 420 activates the test signal phi and phi 2 in the time at the time of a test to differ. For example, the test signal phi 1 is activated on H level immediately after a burn-in test start, and the conditions at the time of a burn-in test start are held to the holding circuit 416. The test signal phi 2 is activated on H level just before the end of burn-in test, and a condition detection result is written in the holding circuit 422.

[0090] If it does in this way, it can check that they have been suitable test voltage and test temperature during burn-in exam time by checking that both the data that the holding circuits 416 and 422 hold fulfills predetermined conditions. Furthermore, it is also possible to sample periodically the data in time to increase a holding circuit and differ under examination.

[0091] [Form 6 of operation] With the form 6 of operation,

it replaces with the condition detector circuit 36 in drawing 1 , and has the condition detector circuit 500.

[0092] Drawing 9 is the block diagram showing the composition of the condition detector circuit 500. With reference to drawing 9 , the condition detector circuit 500 The high-voltage detector circuit 102, The inverters 504 and 506 which undergo the output of the high-voltage detector circuit 102 and which were connected in series, NAND circuit 508 which one input is fixed to H level and receives the output of an inverter 506 in the input of another side, The inverter 510 reversed in response to the input of NAND circuit 508, and the test mode circuit 516 which activates the test mode signal TEST according to the state of the address signals A0-Ai, The holding circuit 512 which holds the information according to the output of the inverter 510 while the test mode signal TEST is being activated, and the output circuit 514 where the test mode signal TEST outputs the signal according to the information which the holding circuit 512 holds at the time of activation to Terminal Tout are included.

[0093] The ** pressure potential Vpp which carried out ** pressure of the internal electrical power source potential Vcc by the ** pressure power supply generating circuit 502 is given to the high-voltage detector circuit 102. The **** potential Vpp is used as activation potential of the word line of a memory cell array etc. Since it has the same composition as the high-voltage detector circuit 102 in drawing 5 , the high-voltage detector circuit 102 does not repeat explanation.

[0094] Since the **** power supply circuit 502 generates the ** pressure potential Vpp higher than internal electrical power source potential and the internal electrical power source potential Vcc is highly set up at the time of a burn-in examination, voltage usually still higher than the time is generated. In this case, since there is a possibility that an internal circuit may be destroyed when it becomes unusually high voltage, it is important to check whether the ** pressure potential Vpp is the value designed at the time of a burn-in examination. It becomes possible [also checking ** pressure potential Vpp] by having such composition.

[0095] It should be thought that the form of the operation indicated this time is [no] illustration at points, and restrictive. The range of this invention is shown by the

above-mentioned not explanation but Claims, and it is meant that Claims, an equal meaning, and all the change in within the limits are included.

[0096]

[Effect of the Invention] The semiconductor memory device according to claim 1 can check whether the semiconductor memory device has been examined on relevant conditions for every semiconductor memory device.

[0097] In addition to the effect that a semiconductor memory device according to claim 1 does so, the semiconductor memory device according to claim 2 can check whether examined above voltage with a suitable semiconductor memory device for every semiconductor memory device.

[0098] In addition to the effect that a semiconductor memory device according to claim 2 does so, the semiconductor memory device according to claim 3 can check whether the semiconductor memory device has been examined in the suitable voltage range for every semiconductor memory device.

[0099] It can be checked for every semiconductor memory device whether, in addition to the effect that a semiconductor memory device according to claim 2 does so, the semiconductor memory device according to claim 4 has been examined above voltage with suitable power supply voltage generated inside a semiconductor memory device.

[0100] In addition to the effect that a semiconductor memory device according to claim 1 does so, the semiconductor memory device according to claim 5 can check whether examined above temperature with a suitable semiconductor memory device for every semiconductor memory device.

[0101] The semiconductor memory device according to claim 6 can check whether, in addition to the effect that a semiconductor memory device according to claim 1 does so, the semiconductor memory device has been examined on relevant conditions for every semiconductor memory device in two or more time under examination.

[0102] Claim 7 and the semiconductor memory device given in 8 can check whether, in addition to the effect that a semiconductor memory device according to claim 1 does so, the semiconductor memory device has been examined on relevant conditions for every semiconductor memory device

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in the energization state immediately after an examination.
[0103] A semiconductor memory device according to claim 9 to 11 can be checked for every semiconductor memory device, also once in addition to the effect that a semiconductor memory device according to claim 1 does so a semiconductor memory device will be in a power off state after examining whether it was examined on relevant conditions.
[0104] The semiconductor memory device according to claim 12 can check whether, in a burn-in examination, the semiconductor memory device has been examined on relevant conditions for every semiconductor memory device.

[Translation done.]

Report Mistranslation | Japanese (whole document in PDF)

PATENT APPLICATION
Docket No.: 4591-380
Client Ref. No.: ID13095-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Pyung-Moon ZHANG, et al.		
Serial No.:	10/888,667	Examiner:	Hiltunen, Thomas J.
Filed:	July 8, 2004	Group Art Unit:	2816
Confirmation No.:	4240		
For:	CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Responsive to the Office Action, Paper No. 20070802, dated August 7, 2007, please amend the application as follows.

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 4 of this paper.

Remarks/Arguments begin on page 10 of this paper.

IN THE SPECIFICATION

Please replace the paragraph beginning at page 1, line 24 with the following:

As shown in FIG. 3, the oscillator 30 comprises one NOR gate G1 and four invertors INV1, INV2, INV3 and INV4. And the oscillator 30 responds to the level sensing signal DET to generate the complimentary pulse signals PUL, /PUL.

Please replace the paragraph beginning at page 4, line 4 with the following:

The oscillator 300 generates complementary pulse signals PUL and /PUL responsive to the level sensing signal DET. If the level sensing signal [[DE)]]DET is enabled, all charge pump parts 120, 130, 140 and 150 increase the output voltage Vout. If the level sensing signal DET is disabled, the charge pump parts 120, 130, 140 and 150 do not operate.

Please replace the paragraph beginning at page 4, line 27 with the following:

The charge supply part 110 comprises high-voltage PMOS transistor P110 available simultaneously in general and test operation modes. The high-voltage PMOS transistor P110 is connected between node 1 and node 2. Source and bulk terminals of the high-voltage PMOS transistor P110 are connected to the node 1. A drain terminal is connected to the node 2. A gate is connected to a ground GND terminal. The charge supply part 110 is available for a charge supply device and supplies charges to a first charge pump part 120 located in next part. For example, if VSEL is [[VPP]]VCC in the general operation mode, charges corresponding to the power voltage VCC are pre-charged at node 2. In addition, if VSEL is VPP in test operation mode, charges corresponding to the high voltage [[VCC]]VPP are pre-charged at node 2.

Please replace the paragraph beginning at page 5, line 29 with the following:

FIG. 6 is a circuit diagram of the selector 210 shown in FIG. 4. Referring to FIG. 6, the selector 210 uses a level shifter to control the high voltage VPP. The selector 210 comprises high-voltage NMOS transistors N211 to N218, high-voltage PMOS transistors P211 to P218 and P210_I where i =1 to 4, and two serially connected inverters. The level shifter selects between the power voltage VCC and the high voltage VPP. For instance, the high-voltage NMOS transistors N216 and N217 turn on in the test operation mode where the detection signal VDET is ~~enables~~ enabled. The high-voltage PMOS transistors P210_3 and P210_4 turn on. As a result,

VSEL is equal to VPP. However, since the high-voltage NMOS transistors N212 and N213 are turned off, the high-voltage PMOS transistors P210_1 and P210_2 are also turned off. Accordingly, VSEL is not equal to VCC. To the contrary, VSEL is equal to VCC in general operation mode where the detection signal VDET is disabled.

Please replace the paragraph beginning at page 6, line 17 with the following:

FIG. 8 is a graph of the output voltage Vout depending on whether the charge pump circuit uses the power voltage VCC or external high voltage VPP. Settling time is a time required for the pumping operation to obtain a wanted output voltage Vout. Referring to FIG. 8, if the selected voltage VSEL is under the condition that the power voltage VCC is equal to 1.8V, and the external voltage VPP is equal to 8V, it is known that four times settling times (STp) is required to obtain an output voltage Vout of 10V. That is, when external high voltage VPP is supplied with the power voltage VCC, a wanted output voltage Vout can be obtained within ~~more short~~ a shorter time.

IN THE CLAIMS

1. (Currently amended) A charge pump circuit comprising:

a charge pump block including ~~at least one charge pump part; and~~ a plurality of charge pump parts, each charge pump part including at least one pre-charge device;

~~a voltage supply circuit to supply one of a supply voltage or a high voltage to the at least one charge pump part responsive to a detect signal, where the high voltage is higher than the supply voltage;~~

~~where the voltage supply circuit includes a detector circuit to generate the detect signal responsive to a comparison of the supply voltage and the high voltage; and~~

~~where the detect signal is high responsive to the high voltage being higher than the supply voltage~~

a selector circuit coupled to the at least one pre-charge device of each of the charge pump parts, the selector circuit being structured to receive a supply voltage and a high voltage; and

a detector circuit comprising a first node, a second node, a high voltage inverter, and a low voltage inverter, the high voltage inverter being coupled to the low voltage inverter, the first node being coupled to the supply voltage and the high voltage, the second node being coupled to an input of the high voltage inverter, the second node having a voltage high enough to invert an output of the high voltage inverter responsive to the high voltage being higher than the supply voltage, the low voltage inverter being configured to provide a detect signal to the selector circuit responsive to the inverted output of the high voltage inverter.

2. (Currently amended) The charge pump circuit of claim 1, ~~where the voltage supply circuit is configured to supply the supply voltage in a general mode~~ wherein the detector circuit further comprises a first high voltage NMOS transistor coupled between the supply voltage and the first node and a second high voltage NMOS transistor coupled between the high voltage and the first node, the first node having a voltage of one of (a) a difference between the supply voltage and a threshold voltage of the first high voltage NMOS transistor and (b) a difference between the high voltage and a threshold voltage of the second high voltage NMOS transistor.

3. (Currently amended) The charge pump circuit of claim[[1]] 2, ~~where the voltage supply circuit is configured to supply the high voltage in a test mode~~ wherein the detector circuit further comprises a high voltage PMOS transistor coupled between the first node and the second node, the high voltage PMOS transistor having substantially an off state responsive to the first node having the voltage corresponding to the difference between the supply voltage and the threshold voltage of the first high voltage NMOS transistor, the detect signal indicating a general mode of operation responsive to the PMOS transistor having the off state.

4. (Currently amended) The charge pump circuit of claim[[1]] 2, ~~where the voltage supply circuit includes:~~ wherein the second node has a high enough voltage to invert the output of the high voltage inverter responsive to the first node having the voltage corresponding to the difference between the high voltage and the threshold voltage of the second high voltage NMOS transistor, the detect signal indicating a test mode of operation responsive to the high enough voltage.

~~a selector circuit to supply the one of the supply voltage or the high voltage responsive to the detect signal.~~

5. (Currently amended) The charge pump circuit of claim 1,

~~where~~ wherein the charge pump block is configured to generate an output voltage on an output terminal, the output terminal being coupled to the at least one pre-charge device of each of the plurality of charge pump parts; and

wherein the selector circuit further comprises:

a first inverter configured to receive the detect signal, an output terminal of the first inverter being coupled to a first node, the first node being coupled to gate terminals of first and second high voltage NMOS transistors;

a second inverter, an input terminal of the second inverter being coupled to the first node, an output terminal of the second inverter being coupled to a second node, the second node being coupled to gate terminals of third and fourth high voltage NMOS transistors;

at least one high voltage PMOS transistor coupled to the supply voltage, the at least one high voltage PMOS transistor having a gate terminal coupled to drain terminals of the first and third high voltage NMOS transistors;

at least another high voltage PMOS transistor coupled to the high voltage, the at least another high voltage PMOS transistor having a gate terminal coupled to drain terminals of the second and fourth high voltage NMOS transistors; and

an output terminal coupled to the high voltage PMOS transistors, wherein the detect signal controls a state of the first, second, third, and fourth high voltage NMOS transistors, and the high voltage NMOS transistors control a state of the high voltage PMOS transistors, the output terminal configured to transmit one of the supply voltage and the high voltage responsive to the state of the high voltage PMOS transistors.

~~where the voltage supply circuit comprises:~~

~~a voltage level sensing block to generate a level sensing signal responsive to a pump enable signal and the output voltage; and~~

~~an oscillator to generate complementary pulse signals responsive to the level sensing signal.~~

6-17. (Canceled)

18. (Previously presented) A charge pump circuit comprising:

a charge pump block including at least one charge pump part;

a voltage level sensing block to sense a level of an output voltage and generate a level sensing signal responsive thereto;

an oscillator to generate a pulse signal responsive to the level sensing signal;

a detector to generate a detection signal responsive to a high voltage; and

a selector to provide one of the high voltage and a power voltage responsive to the detection signal to the charge pump block;

where the detector compares the high voltage to the power voltage; and

where the output of the detector is high responsive to the high voltage being higher than the power voltage.

19. (New) A charge pump circuit comprising:

a charge pump block including a plurality of charge pump parts, each charge pump part including at least one pre-charge device; and

a selector circuit coupled to the at least one pre-charge device of each of the charge pump parts, the selector circuit being structured to receive a supply voltage and a high voltage.

20. (New) The charge pump circuit of claim 19, further comprising:

a detector circuit comprising a first node, a second node, a high voltage inverter, and a low voltage inverter, the high voltage inverter being coupled to the low voltage inverter, the first node being coupled to the supply voltage and the high voltage, the second node being coupled to an input of the high voltage inverter.

21. (New) The charge pump circuit of claim 20, wherein the second node has a voltage high enough to invert an output of the high voltage inverter responsive to the high voltage being higher than the supply voltage, the low voltage inverter being configured to provide a detect signal to the selector circuit responsive to the inverted output of the high voltage inverter.

22. (New) The charge pump circuit of claim 21, wherein the detector circuit further comprises a first high voltage NMOS transistor coupled between the supply voltage and the first node and a second high voltage NMOS transistor coupled between the high voltage and the first node.

23. (New) The charge pump circuit of claim 22, wherein the first node has a voltage of one of (a) a difference between the supply voltage and a threshold voltage of the first high voltage NMOS transistor and (b) a difference between the high voltage and a threshold voltage of the second high voltage NMOS transistor.

24. (New) The charge pump circuit of claim 23, wherein the detector circuit further comprises a high voltage PMOS transistor coupled between the first node and the second node, the high voltage PMOS transistor having substantially an off state responsive to the first node having the voltage corresponding to the difference between the supply voltage and the threshold voltage of the first high voltage NMOS transistor.

25. (New) The charge pump circuit of claim 24, wherein the detect signal indicates a general mode of operation responsive to the PMOS transistor having the off state.

26. (New) The charge pump circuit of claim 23 wherein the second node has a high enough voltage to invert the output of the high voltage inverter responsive to the first node having the voltage corresponding to the difference between the high voltage and the threshold voltage of the second high voltage NMOS transistor.

27. (New) The charge pump circuit of claim 26, wherein the detect signal indicates a test mode of operation responsive to the high enough voltage.

28. (New) The charge pump circuit of claim 1, wherein the charge pump block is configured to generate an output voltage on an output terminal, the output terminal being coupled to the at least one pre-charge device of each of the plurality of charge pump parts.

29. (New) The charge pump circuit of claim 1, wherein the selector circuit further comprises:

a first inverter configured to receive the detect signal, an output terminal of the first inverter being coupled to a first node, the first node being coupled to gate terminals of first and second high voltage NMOS transistors; and

a second inverter, an input terminal of the second inverter being coupled to the first node, an output terminal of the second inverter being coupled to a second node, the second node being coupled to gate terminals of third and fourth high voltage NMOS transistors.

30. (New) The charge pump circuit of claim 29, wherein the selector circuit further comprises:

at least one high voltage PMOS transistor coupled to the supply voltage, the at least one high voltage PMOS transistor having a gate terminal coupled to drain terminals of the first and third high voltage NMOS transistors.

31. (New) The charge pump circuit of claim 29, wherein the selector circuit further comprises:

at least another high voltage PMOS transistor coupled to the high voltage, the at least another high voltage PMOS transistor having a gate terminal coupled to drain terminals of the second and fourth high voltage NMOS transistors.

32. (New) The charge pump circuit of claim 31, wherein the selector circuit further comprises:

an output terminal coupled to the high voltage PMOS transistors,

wherein the detect signal controls a state of the first, second, third, and fourth high voltage NMOS transistors,

wherein the high voltage NMOS transistors control a state of the high voltage PMOS transistors, and

wherein the output terminal is configured to transmit one of the supply voltage and the high voltage responsive to the state of the high voltage PMOS transistors.

REMARKS

Claims 1-5 and 7-18 are pending in the application.

Claims 1-5 and 7-18 are rejected.

Claims 1-5 and 7-12 stand rejected under 35 U.S.C. 112.

Claims 1-4 stand rejected under 35 U.S.C. 102(b).

Claims 1, 5 and 7-18 stand rejected under 35 U.S.C. 103(a).

Claims 1-5 are amended.

Claims 6-17 are canceled.

Claims 19-32 are added.

No new matter is added. The Applicant respectfully requests reconsideration in light of the following amendment and remarks.

Specification

The specification has been amended to correct various typographical errors, as indicated above.

Claim Rejections – §112

Claims 1-5 and 7-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner states that with respect to claims 1, 7 and 12, the recitation of "where the high voltage is higher than the supply voltage" is misdescriptive because the high voltage is not always higher than the supply voltage. The Applicant agrees with the Examiner and has removed the indicated language by amending claim 1 and canceling claims 7 and 12. Therefore, the Applicant requests that the rejection be withdrawn.

Claim Rejections – §102 and §103

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated Horiguchi, et al. (U.S. Patent No. 5,272,393).

Claims 1, 5 and 7-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horiguchi, et al. (U.S. Patent No. 5,272,393) in view of Foss, et al. (U.S. Patent No. 5,828,620).

The Applicant respectfully traverses the rejections.

The Examiner suggests that it would have been obvious to replace the word line driving circuit of Horiguchi with the word line driving circuit of Foss because "Foss, et al.'s word line driving circuit provides a highly regulated word line voltage signal that prevents both an over-voltage and an under-voltage condition of the word line driving signal, thus increasing the reliability of the circuit controlled by the boosted word line signal." Office Action, bottom of page 5, top of page 6.

MPEP 2143.01(V) states "[i]f the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)." Here, the Examiner has suggested that it would have been obvious to replace the word line driving circuit of Horiguchi with the word line driving circuit of Foss because Foss' prevents an over-voltage condition of the word line driving signal. However, providing an over-voltage condition of the word line driving signal is an essential element of Horiguchi, that is, "a voltage higher than the one applied in ordinary operation is impressed on a supply terminal before delivery of semiconductor devices so as to exclude therefrom those devices which become imperfect after the voltage is applied." Horiguchi, column 2, lines 20-24.

Replacing the word line driver of Horiguchi with a word line driver that prevents an over-voltage condition from occurring would render Horiguchi's word line driver unsatisfactory for its intended purpose (i.e., impressing a higher voltage on semiconductor devices to exclude imperfect devices prior to shipment). Furthermore, the Applicant notes that the present disclosure does not concern impressing a higher voltage on semiconductor devices to exclude devices. Rather, the present disclosure involves shortening a time for achieving a desired output voltage. One of the problems of the prior art involves settling times—that is, the time required for the pumping operation to obtain a wanted output voltage Vout. The desired output voltage Vout can be acquired four times as quickly using the charge pump circuit as set forth in the present disclosure. See Disclosure, page 6, lines 17-24 and figure 8. Thus, not only do the disclosures of Horiguchi and Foss fail to teach the charge pump circuit of the present disclosure, the combination of Horiguchi with Foss would render Horiguchi's circuit inoperable.

Notwithstanding the defective combination of Horiguchi and Foss, the Applicant amends the following claims to progress with the prosecution of the present application.

Claim 1 has been amended to set forth a charge pump circuit comprising "a charge pump block including a plurality of charge pump parts, each charge pump part including at least one pre-charge device; a selector circuit coupled to the at least one pre-charge device of each of the charge pump parts, the selector circuit being structured to receive a supply voltage and a high voltage; and a detector circuit comprising a first node, a second node, a high voltage inverter, and a low voltage inverter, the high voltage inverter being coupled to the low voltage inverter, the first node being coupled to the supply voltage and the high voltage, the second node being coupled to an input of the high voltage inverter, the second node having a voltage high enough to invert an output of the high voltage inverter responsive to the high voltage being higher than the supply voltage, the low voltage inverter being configured to provide a detect signal to the selector circuit responsive to the inverted output of the high voltage inverter."

The amendment to claim 1 is supported by at least page 3, lines 20-32, page 5, lines 29-34, page 6, lines 1-16, and figures 4, 6 and 7. The Applicant submits that the prior art fails to teach each limitation as set forth in claim 1. Therefore, claim 1 is in proper form for allowance.

Claim 2 has been amended to set forth the charge pump circuit of claim 1, "wherein the detector circuit further comprises a first high voltage NMOS transistor coupled between the supply voltage and the first node and a second high voltage NMOS transistor coupled between the high voltage and the first node, the first node having a voltage of one of (a) a difference between the supply voltage and a threshold voltage of the first high voltage NMOS transistor and (b) a difference between the high voltage and a threshold voltage of the second high voltage NMOS transistor." This amendment is supported by at least page 6, lines 6-16, and figure 7. The prior art fails to teach each of these limitations. Thus, claim 2 is allowable.

Claim 3 has been amended to set forth the charge pump of claim 2, "wherein the detector circuit further comprises a high voltage PMOS transistor coupled between the first node and the second node, the high voltage PMOS transistor having substantially an off state responsive to the first node having the voltage corresponding to the difference between the supply voltage and the threshold voltage of the first high voltage NMOS transistor, the detect signal indicating a general mode of operation responsive to the PMOS transistor having the off state." This amendment is supported by at least page 6, lines 6-16, and figure 7. The prior art fails to teach each of these limitations; therefore, claim 3 is likewise allowable.

Claim 4 has been amended to set forth the charge pump of claim 2, "wherein the second node has a high enough voltage to invert the output of the high voltage inverter responsive to the first node having the voltage corresponding to the difference between the high voltage and the threshold voltage of the second high voltage NMOS transistor, the detect signal indicating a test mode of operation responsive to the high enough voltage." This amendment is supported by at least page 6, lines 6-16, and figure 7. Claim 4 is not taught by the prior art and is therefore allowable.

Claim 5 has been amended to set forth the charge pump circuit of claim 1, "wherein the charge pump block is configured to generate an output voltage on an output terminal, the output terminal being coupled to the at least one pre-charge device of each of the plurality of charge pump parts; and wherein the selector circuit further comprises: a first inverter configured to receive the detect signal, an output terminal of the first inverter being coupled to a first node, the first node being coupled to gate terminals of first and second high voltage NMOS transistors; a second inverter, an input terminal of the second inverter being coupled to the first node, an output terminal of the second inverter being coupled to a second node, the second node being coupled to gate terminals of third and fourth high voltage NMOS transistors; at least one high voltage PMOS transistor coupled to the supply voltage, the at least one high voltage PMOS transistor having a gate terminal coupled to drain terminals of the first and third high voltage NMOS transistors; at least another high voltage PMOS transistor coupled to the high voltage, the at least another high voltage PMOS transistor having a gate terminal coupled to drain terminals of the second and fourth high voltage NMOS transistors; and an output terminal coupled to the high voltage PMOS transistors, wherein the detect signal controls a state of the first, second, third, and fourth high voltage NMOS transistors, and the high voltage NMOS transistors control a state of the high voltage PMOS transistors, the output terminal configured to transmit one of the supply voltage and the high voltage responsive to the state of the high voltage PMOS transistors."

The amendment to claim 5 is supported by at least page 5, lines 29-34, page 6, lines 1-5, and figure 6. The Applicant submits that the prior art fails to teach each of the limitations of claim 5; therefore, claim 5 is allowable.

Claims 6-17 have been canceled.

Claim 18 sets forth a charge pump circuit comprising: "a charge pump block including at least one charge pump part; a voltage level sensing block to sense a level of an output voltage and generate a level sensing signal responsive thereto; an oscillator to generate a pulse signal responsive to the level sensing signal; a detector to generate a detection signal responsive to a high voltage; and a selector to provide one of the high voltage and a power voltage responsive to the detection signal to the charge pump block; where the detector compares the high voltage to the power voltage; and where the output of the detector is high responsive to the high voltage being higher than the power voltage." Based on the defective combination of Horiguchi and Foss, as explained in detail above, claim 18 is in allowable form.

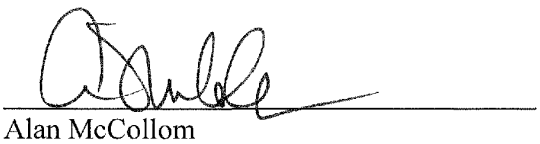
New Claims

New claims 19-32 generally correspond to limitations of amended claims 1-5. The Applicant submits that the prior art fails to teach each of the limitations of new claims 18-32.

For the foregoing reasons, reconsideration and allowance of claims 1-5 and 18-32 of the application as amended is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



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Electronic Acknowledgement Receipt

EFS ID:	2433619
Application Number:	10888667
International Application Number:	
Confirmation Number:	4240
Title of Invention:	Charge pump circuit operating responsive to a mode
First Named Inventor/Applicant Name:	Pyung-Moon Zhang
Customer Number:	20575
Filer:	Hosoon Lee/Stormi Davis
Filer Authorized By:	Hosoon Lee
Attorney Docket Number:	4591-380
Receipt Date:	06-NOV-2007
Filing Date:	08-JUL-2004
Time Stamp:	19:07:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		4591-380f.pdf	1244845 409e1bacf0c323a7cf9a8e8259aab69c8e07a511	yes	15

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Amendment - After Non-Final Rejection	2	2
	Specification	3	4
	Claims	5	10
	Applicant Arguments/Remarks Made in an Amendment	11	15
Warnings:			
Information:			
	Total Files Size (in bytes):	1244845	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

MISCELLANEOUS LETTER

REGARDING PAYMENT OF FEES AND EXTENSION OF TIME

	Claims Remaining After Amendment	Highest Number Previously Paid For	Present Extra Claims
Total Claims	20	18	0
Independent Claims	3	5	0

☒ Applicant petitions the Commissioner to extend the time for response (if applicable).

☒ Payment of fees is made via electronic filing system authorizing credit card payments for the extra claims and/or Petition.

☒ Applicant is paying with a Visa card; however, Applicant requests that any deficiency or overpayment be charged or credited to deposit account number 13-1703.

Respectfully submitted,

Customer No. 20575

MARGER JOHNSON & McCOLLOM, P.C.

Date: November 6, 2007

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PTO/SB/06 (07-06)
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
10/888,667	07/08/2004	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	11/06/2007	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $ =		OR	X $50=	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***5	= 0	X $ =		OR	X $210=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
Jermaine D. Minor

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/888,667	07/08/2004	Pyung-Moon Zhang	4591-380	4240

20575 7590 08/07/2007

MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
08/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/888,667	ZHANG ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's request for considered examination filed 06 June 07 has been received and the claims filed 06 June 07 have now been entered. The claims filed 06 June 2007 are considered below.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-5 and 7-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claims 1, 7 and 12, the above claims contain the misdescriptive recitation of "where the high voltage is higher than the supply voltage" (For instance, lines 4-5 of claim 1). This limitation is misdescriptive because the high voltage is not always higher than the supply voltage, i.e., there are times when the high voltage (i.e., Vpp of Fig. 4) is less than the supply voltage (i.e., Vcc of Fig. 4) otherwise the detector circuit of the claimed invention would be superfluous.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiguchi et al. (USPN 65,272,393)

With respect to claim 1, Horiguchi et al. discloses in Figs. 2(a), 2(b), 6, 10 and 13, "a charge pump circuit comprising (circuit of Fig. 10, i.e. 202 of Fig. 10, see Fig. 13 for further detail):

a charge pump block (280, 370, and 264 of Fig. 13) including at least one charge pump part (280, 370, and 264 includes at least one charge pump part since it is itself a charge pump); and

a voltage supply circuit (100 of Fig. 10, which supplies 202, i.e., Fig. 13) to supply one of a supply voltage (V1) or a high voltage (V2) to the at least one charge pump part responsive to a detect signal (output of 4), where the high voltage is higher than the supply voltage (V2 is higher than V1 during certain points of time, see Fig. 2(b))

Where the voltage supply circuit includes a detector circuit (4) to generate the detect signal responsive to a comparison of the supply voltage and the high voltage (output of 4 is responsive to a comparison of V1 and V2)

Where the detect signal is signal is high responsive to the high voltage being higher than the supply voltage (the output of 4 is high when the V2 is higher than V1)."

With respect to claim 2, Horiguchi et al. discloses, "the charge pump circuit of claim 1 where the voltage supply circuit is adapted to supply the supply voltage in a general mode (the above recitation is merely functional langue and when V1 is supplied to 202 corresponds to a "general mode")."

With respect to claim 3, Horiguchi et al. discloses, "the charge pump circuit of claim 1 where the voltage supply circuit is adapted to supply the high voltage in a test mode (the above recitation is merely functional langue and when V2 is supplied to 202 corresponds to a "test mode")."

With respect to claim 4, Horiguchi et al. discloses, "the charge pump circuit of claim 1 where the voltage supply circuit includes:

a selector circuit (3) to supply the one of the supply voltage or the high voltage responsive to the detect signal (3 outputs V1 or V2 responsive to the output of 4).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5 and 7-18 rejected under 35 U.S.C. 103(a) as being unpatentable over Horiguchi et al. (USPN 5,272,393) in view of Foss et al. (USPN 5,828,620).

With respect to claims 1, 5, 7, 12, 13 and 18, Horiguchi et al. discloses, "a charge pump circuit comprising (202 of Fig. 10):

a charge pump block to generate an output voltage (charge pump block of 202);

and a selecting circuit block (100), including a detector (4) and a selector (3), to generate a selected voltage that is one of a high voltage (V2) and a supply voltage (V1)

and to supply the selected voltage to the charge pump block responsive to detecting a level of the high voltage, the high voltage having a level higher than the supply voltage (100 supplies the higher of V1 and V2 to 202 based on detecting the level of V1 and V2, where V2 is higher than V1, see Fig. 2(b));

where the detector is configured to compare the supply voltage with the high voltage (4 compares V1 and V2);

where the detector output is high responsive to a level of the high voltage being higher than a level of the supply voltage (4 outputs a high when V2 is higher than V1); and

where the selector is configured to select the high voltage if the level of the high voltage is higher than the level of the supply voltage (3 selects the higher voltage of V1 and V2).

Horiguchi et al. fails to disclose, in Fig. 10, "a voltage level sensing block to generate a level sensing signal by sensing an output voltage; an oscillator to generate complementary pulse signals responsive to the level sensing signal." Note Horiguchi et al. merely discloses a generic word line driver (202). However, Foss et al. discloses, in Figs. 3 and 6, a specific world line driver (circuit of Fig. 6) that includes a charge pump (39) responsive "to a voltage level sensing block (35-38) to generate a level sensing signal (INHIBIT) by sensing an output voltage (Vpp); an oscillator (44) to generate complementary pulse signals responsive to the level sensing signal (44 generates complementary pulse signals Φ1 and Φ2 and Φ1 bar and Φ2 bar, see Fig. 3, responsive to the INHIBIT signal)." Foss et al.'s word line driving circuit provides a highly regulated

word line voltage signal that prevents both an over-voltage and an under-voltage condition of the word line diving signal, thus increasing the reliability of the circuit controlled by the boosted word line signal.

It would have been obvious to replace the generic word line driving circuit 202 of Fig. 10 of Horiguchi et al. with the specific word line driving circuit of Fig. 6 of Foss et al. for the purpose of increasing the reliability of the circuit of Fig. 10 of Horiguchi et al.

With respect to claims 8 and 14, the above combination discloses, that 26 of Fig. 3 of Foss et al. is a charge supply part that precharges a charge pump part (27) and a charging trapping part (16 with 15) that stores pumped charges from charge pump parts 27 and 22.

With respect to claims 9 and 15, the above combination discloses, two serially connected charge pump parts 27 and 22.

With respect to claims 10 and 16, the above combination discloses, 26 is a charge supply part that includes a high voltage PMOS transistor (i.e., 26 precharges 27 and is high voltage in that it withstands the high supply voltages of the circuit of Fig. 3)

With respect to claims 11 and 17, that above combination discloses, that NMOS transistors 17, 21, 23, and 25 are high voltage NMOS transistors in that they withstand the high supply voltage of the circuit of Fig. 3.

Response to Arguments

Applicant's arguments with respect to claims 1-5, and 7-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on M-F 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571)272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TH
August 3, 2007

/Kenneth B. Wells/
Primary Examiner
Art Unit 2816

Notice of References Cited	Application/Control No. 10/888,667	Applicant(s)/Patent Under Reexamination ZHANG ET AL.	
	Examiner Thomas J. Hiltunen	Art Unit 2816	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,828,620	10-1998	Foss et al.	365/226
*	B	US-5,272,393	12-1993	Horiguchi et al.	327/535
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
10/888,667	ZHANG ET AL.	
Examiner	**Art Unit**	
Thomas J. Hiltunen	2816	

SEARCHED			
Class	Subclass	Date	Examiner
327	536,537 143,82,60, 63	11/9/2005	TH
363	60	11/9/2005	TH
Updated	above	4/6/2006	TH
Updated	above	9/27/2006	TH
363	63	9/28/2006	TH
Updated	above	3/1/2007	TH
363	59	3/1/2007	TH
365	189.09	3/1/2007	TH

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
See attached EAST text search	11/14/2005	TH
See attached EAST text search	4/10/2006	TH
See attached EAST text search	9/28/2006	TH
See attached EAST text search	3/7/2007	TH

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	266516	(charge voltage current) with (pump$4 multipl$4 multiplication)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/08/02 12:41
L18	266516	(charge voltage current) with (pump$4 multipl$4 multiplication)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/08/02 12:41
L19	438455	(select$4 chang$4 switch$4 control$4 controll$4) with ((supply power) near2 (voltage supply))	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/08/02 12:42
L20	10921	18 with 19	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/08/02 12:43
L21	3151	20 same (voltage supply power) with (comparator monitor$4 detect$4 sens$4 differential adj amplifier)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/08/02 14:38
L22	1489	21 same (multiplexer multiplexor mux selector select$4 near2 (circuit element device block) switch$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/08/02 12:46
L23	109408	dll pll delay adj lock$4 adj loop phase adj lock$4 adj loop delay$1lock$5loop phase$1lock$5loop	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/08/02 14:16
L24	1366	22 not 23	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/08/02 13:34
L29	1483	21 not (22 23)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/08/02 13:53

EAST Search History

L36	15287	2 and oscillator and (detect$4 sens$4 monitor$4) and (power supply) with (select$4 switch$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/08/02 14:40
L37	10373	36 not(22 23 29)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/08/02 14:41
L38	4125	37 and test$4	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/08/02 14:42
L39	90	38 and selector with detector	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/08/02 14:44
L40	4035	38 not 39	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/08/02 14:45
L41	668	40 and charge adj pump$4	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/08/02 16:02

PATENT APPLICATION
Docket No.: 4591-380
Client Ref. No.: ID13095-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Pyung-Moon ZHANG, et al.		
Confirmation No.:	4240		
Serial No.:	10/888,667	Examiner:	Hiltunen, Thomas J.
Filed:	July 8, 2004	Group Art Unit:	2816
For:	CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INTERVIEW SUMMARY

Please accept the following statement regarding the substance of the telephonic interview between the undersigned and examiner Hiltunen on 6/25/07, initiated by the undersigned.

The telephonic interview discussed amendments to the independent claims 1, 7, 12, 13, and 18 made in an earlier response filed on 6/12/07 along with a request for continued examination. The examiner agreed that the amendment as filed earlier would make the claims allowable over the Javanifard reference.

Respectfully submitted,
MARGER JOHNSON & McCOLLOM, P.C.

Gradvela G. Cowger
Reg. No. 42,444

MARGER JOHNSON & McCOLLOM, P.C.
210 SW Morrison Street, Suite 400
Portland, OR 97204
503-222-3613
Customer No. 20575

Electronic Acknowledgement Receipt

EFS ID:	1917493
Application Number:	10888667
International Application Number:	
Confirmation Number:	4240
Title of Invention:	Charge pump circuit operating responsive to a mode
First Named Inventor/Applicant Name:	Pyung-Moon Zhang
Customer Number:	20575
Filer:	Hosoon Lee/Stormi Davis
Filer Authorized By:	Hosoon Lee
Attorney Docket Number:	4591-380
Receipt Date:	27-JUN-2007
Filing Date:	08-JUL-2004
Time Stamp:	17:15:45
Application Type:	Utility

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Applicant summary of interview with examiner	Interview_Summary.pdf	59896	no	1
Warnings:					

Information:	
Total Files Size (in bytes):	59896

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Applicant Initiated Interview Request Form

Application No:	**10/888,667**
First Named Applicant:	**Pyung-Moon ZHANG**
Examiner:	**Hiltunen, Thomas J.**
Group Art Unit:	2816
Status of Application:	pending

Tentative Participants:

1. Examiner Pyung-Moon Zhang
2. Graciela Cowger, attorney
3. Ayan Paul, patent engineer

Proposed Date of Interview:	June 25, 2007
Proposed Time:	2:00 PM Eastern Time
Type of Interview Requested:	Telephonic
Exhibit to be shown or demonstrated?	No
If yes, provide brief description:	

Issues to be Discussed

Issues (Rej., Obj., etc)	Claims/Figs. #s	Prior Art	Discussed	Agreed	Not Agreed
1. §103(a)	5, 7-10 and 12-17	Javanifard 5,483,486	☐	☐	☐
2. §102(b)	1-4	Javanifard 5,483,486	☐	☐	☐
3.			☐	☐	☐

☐ **Continuation sheet attached**

Brief Description of Arguments to be Presented:

An interview was conducted for the above-identified application on .

Note:
This form should be completed by applicant and submitted to the examiner in advance of the interview (see MPEP §713.01). This application will not be delayed from issue because of applicant's failure to submit a written record of this interview. Therefore, applicant is advised to file a statement of the substance of this interview (37 CFR §1.133(b)) as soon as possible.

(Applicant/Applicant's Representative Signature) (Examiner/SPE Signature)

This collection of information is required by 37 CFR 1.133. The information is required to obtain or retain a benefit by the public that is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 USC 122 and 37 CFR1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing , and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	1875114
Application Number:	10888667
International Application Number:	
Confirmation Number:	4240
Title of Invention:	Charge pump circuit operating responsive to a mode
First Named Inventor/Applicant Name:	Pyung-Moon Zhang
Customer Number:	20575
Filer:	Graciela G. Cowger/Lauren Ballard-Gemmell
Filer Authorized By:	Graciela G. Cowger
Attorney Docket Number:	4591-380
Receipt Date:	14-JUN-2007
Filing Date:	08-JUL-2004
Time Stamp:	19:03:42
Application Type:	Utility

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Letter Requesting Interview with Examiner	4591380intrvwrqst.pdf	226116	no	1
Warnings:					

Information:	
Total Files Size (in bytes):	226116

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/30EFS (08/06)
Approved for use through 08/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	10888667	Filing Date	2004-07-08	Docket Number (if applicable)	4591-380	Art Unit	2816
First Named Inventor	Pyung-Moon ZHANG et al.			Examiner Name	Hiltunen, Thomas J.		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____ (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 131703

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

Signature of Registered U.S. Patent Practitioner			
Signature	/Graciela G. Cowger/	Date (YYYY-MM-DD)	2007-06-06
Name	Graciela G. Cowger	Registration Number	42444

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2816

PATENT APPLICATION
Docket No.: 4591-380
Client Ref. No.: ID13095-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Pyung-Moon ZHANG, et al.		
Serial No.:	10/888,667	Examiner:	Hiltunen, Thomas J.
Filed:	July 8, 2004	Group Art Unit:	2816
Confirmation No.:	4240		
For:	CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE		

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CONTINUED EXAMINATION
WITH
AMENDMENT AS SUBMISSION UNDER 37 CFR 1.114

Responsive to the Final Office Action dated March 6, 2007 and advisory action dated May 14, 2007, please amend the application as follows.

Claims begin on page 2.

Remarks begin on page 6.

CLAIMS

Please amend the claims as follows.

1. (Currently amended) A charge pump circuit comprising:

a charge pump block including at least one charge pump part; and

a voltage supply circuit to supply one of a supply voltage or a high voltage to the at least one charge pump part responsive to a detect signal, where the high voltage is higher than the supply voltage;

where the voltage supply circuit includes a detector circuit to generate the detect signal responsive to a comparison of the supply voltage and the high voltage; and

where the detect signal is high responsive to the high voltage being higher than the supply voltage.

2. (Previously presented) The charge pump circuit of claim 1 where the voltage supply circuit is configured to supply the supply voltage in a general mode.

3. (Previously presented) The charge pump circuit of claim 1 where the voltage supply circuit is configured to supply the high voltage in a test mode.

4. (Previously presented) The charge pump circuit of claim 1 where the voltage supply circuit includes:

a selector circuit to supply the one of the supply voltage or the high voltage responsive to the detect signal.

5. (Previously presented) The charge pump circuit of claim 1

where the charge pump block is configured to generate an output voltage; and

where the voltage supply circuit comprises:

a voltage level sensing block to generate a level sensing signal responsive to a pump enable signal and the output voltage; and

an oscillator to generate complementary pulse signals responsive to the level sensing signal.

6. (Canceled)

7. (Currently amended) A charge pump circuit comprising:

a charge pump block to generate an output voltage;

a voltage level sensing block to generate a level sensing signal by sensing an output voltage;

an oscillator to generate complementary pulse signals responsive to the level sensing signal; and

a selecting circuit block to generate a selected voltage that is one of a high voltage and a supply voltage and to supply the selected voltage to the charge pump block responsive to detecting a level of the high voltage, the high voltage having a level higher than the supply voltage;

where the selecting circuit block includes a detector configured to compare the supply voltage with the high voltage; and

where the detector output is high responsive to the high voltage being higher than the supply voltage.

8. (Previously presented) The charge pump circuit of claim 7 where the charge pump block includes:

at least one charge pump part;

a charge supply part to precharge the at least one charge pump part with the selected voltage; and

a charge trapping part to store charges provided by the charge supply part.

9. (Original) The charge pump circuit of claim 8 where the at least one charge pump part pumps a charge to another charge pump part.

10. (Original) The charge pump circuit of claim 8 where the charge supply part comprises a high-voltage PMOS transistor.

11. (Previously presented) The charge pump circuit of claim 8 where the at least one charge pump part includes a high-voltage NMOS transistor.

12. (Currently amended) A charge pump circuit comprising:

a charge pump block to generate an output voltage;

a voltage level sensing block to generate a level sensing signal by sensing an output voltage;

an oscillator to generate complementary pulse signals responsive to the level sensing signal; and

a selecting circuit block, including a detector and a selector, to generate a selected voltage that is one of a high voltage and a supply voltage and to supply the selected voltage to the charge pump block responsive to detecting a level of the high voltage, the high voltage having a level higher than the supply voltage;

where the detector is configured to compare the supply voltage with the high voltage;

where the detector output is high responsive to a level of the high voltage being higher than a level of the supply voltage; and

where the selector is configured to select the high voltage if ~~a~~ the level of the high voltage is higher than ~~a~~ the level of the supply voltage.

13. (Currently amended) A charge pump circuit comprising:

a charge pump block including at least one charge pump part;

a voltage level sensing block to sense a level of an output voltage and generate a level sensing signal responsive thereto;

an oscillator to generate a pulse signal responsive to the level sensing signal;

a detector to generate a detection signal responsive to a comparison of a power voltage and a high voltage;

where the detection signal is high responsive to the high voltage being higher than the power voltage; and

a selector to provide one of the high voltage and the power voltage responsive to the detection signal to the charge pump block.

14. (Original) The charge pump circuit of claim 13 where the charge pump block comprises:

a charge supply part to precharge the at least one charge pump part; and

a charge trapping part to store charges pumped from the at least one charge pump part.

15. (Original) The charge pump circuit of claim 14 where the at least one charge pump part pumps charge to another serially connected charge pump part.

16. (Original) The charge pump circuit of claim 14 where the charge supply part includes a high-voltage PMOS transistor.

17. (Original) The charge pump circuit of claim 14 where the charge pump block includes a high-voltage NMOS transistor.

18. (Currently amended) A charge pump circuit comprising:

a charge pump block including at least one charge pump part;

a voltage level sensing block to sense a level of an output voltage and generate a level sensing signal responsive thereto;

an oscillator to generate a pulse signal responsive to the level sensing signal;

a detector to generate a detection signal responsive to a high voltage; and

a selector to provide one of the high voltage and a power voltage responsive to the detection signal to the charge pump block;

where the detector compares the high voltage to the power voltage; and

where the output of the detector is high responsive to the high voltage being higher than the power voltage.

REMARKS

The application includes claims 1-5 and 7-18 prior to entering this amendment.

The examiner objects to claims 2-3, 5 and 7-8 for certain informalities.

The examiner rejects claims 1-4 under 35 U.S.C. §102(b) as being anticipated by Javanifard, et al. (U.S. Patent 5,483,486).

The examiner rejects claims 5, 7-10 and 12-17 under 35 U.S.C. §103(a) as being unpatentable by Javanifard in view of Tanzawa, et al. (U.S. Patent 6,429,725).

The applicants amend claims 2, 3, 5, 7, 8 and 12. The application remains with claims 1-5 and 7-18 after entering this amendment.

The applicants add no new matter and request reconsideration.

Claim Objections

The examiner objects to claims 2-3, 5, and 7-8 for reciting "adapted to" and suggests amending the claims to read "configured to." The applicants note that claim 8 does not include the "adapted to" limitation. The applicants amend claims 2-3, 5, 7 and 12 as suggested by the examiner to obviate the objection.

Claim Rejections Under §102

The examiner rejects claims 1-4 as being old over Javanifard. Although the applicants disagree, the applicants amend claims 1, 7, 12-13 and 18 in order to further clarify applicant's techniques and to expedite examination of the application.

Claim 1 now recites *the voltage supply circuit includes a detector circuit to generate the detect signal responsive to a comparison of the supply voltage and the high voltage ... where the detect signal is high responsive to the high voltage being higher than the supply voltage.* Claims 7, 12-13 and 18 include similar limitations. The examiner alleges that Javanifard's 5V/12V VPP detector circuit[2] and the PD5VPP signal[3] "is responsive to a comparison of the supply voltage and the high voltage. (It can be seen in Fig. 11 that the PD5VPP signal is output responsive to a comparison between VPP (input to 170 of Fig. 11) and VCC (input to 175 of Fig. 11)."[4]

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[12] Javanifard, figures 11 and 13b.
[3] Javanifard, figure 11.
[4] Office action dated 03/06/2007, page 3.

Javanifard also discloses that "if the operating supply voltage VCC is greater than the programming supply voltage VPP, the circuit shown in FIG. 11 draws a constant DC current."[5] The examiner interprets this as a comparison between VCC (supply voltage) and VPP (high voltage).[6]

The applicants disagree with the examiner's interpretation of Javanifard. Javanifard's 5V/12V VPP level detector 55 "detects whether the programming supply voltage VPP is equal to 5 volts or 12 volts."[7] That is, Javanifard's PD5VPP signal (which is the output of the 5V/12V VPP level detector 55) is at logic high or logic low level depending on whether VPP is 5V or 12V. In contrast, the limitations of claims 1, 7, 12, 13 and 18 do not recite determining the level of the voltage VPP. Claim 1, rather, recites generating *the detect signal responsive to a comparison of the supply voltage and the high voltage*. Javanifard's PD5VPP signal is not responsive to a comparison of the supply voltage and the high voltage.

Additionally, claim 1 recites *where the detect signal is high responsive to the high voltage being higher than the supply voltage*. Claims 7, 12-13 and 18 include similar limitation. As discussed above, Javanifard does not compare the supply voltage VCC with the programming voltage VPP. Even assuming, *arguendo*, that Javanifard does a comparison of the two voltages, Javanifard, however, does not disclose that the output signal PD5VPP is high if the programming voltage VPP is higher than the supply voltage VCC, as would be required by claims 1, 7, 12, 13 and 18.

For at least these reasons, claims 1, 7, 12, 13 and 18 are in condition for allowance, along with associated dependent claims.

[5] Javanifard, column 15, lines 44-47.
[6] Advisory action, dated 5/14/2007, page 2.
[7] Javanifard, column 14, lines 60-63.

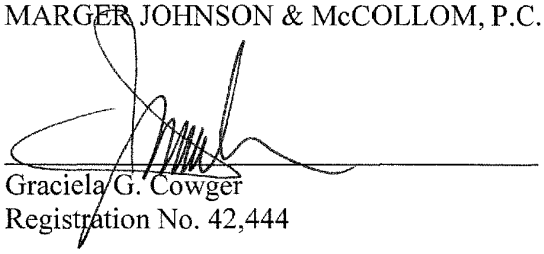
Conclusion

The applicants request reconsideration and allowance of remaining claims. The applicants encourage the Examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



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Electronic Patent Application Fee Transmittal

Application Number:	10888667
Filing Date:	08-Jul-2004
Title of Invention:	Charge pump circuit operating responsive to a mode
First Named Inventor/Applicant Name:	Pyung-Moon Zhang
Filer:	Alexander Charles Johnson/Li Mei Vermilya
Attorney Docket Number:	4591-380
Filed as Large Entity	

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	790	790
		Total in USD ($)		**790**

Electronic Acknowledgement Receipt

EFS ID:	1846644
Application Number:	10888667
International Application Number:	
Confirmation Number:	4240
Title of Invention:	Charge pump circuit operating responsive to a mode
First Named Inventor/Applicant Name:	Pyung-Moon Zhang
Customer Number:	20575
Filer:	Alexander Charles Johnson/Li Mei Vermilya
Filer Authorized By:	Alexander Charles Johnson
Attorney Docket Number:	4591-380
Receipt Date:	06-JUN-2007
Filing Date:	08-JUL-2004
Time Stamp:	18:32:00
Application Type:	Utility

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	$790
RAM confirmation Number	2799
Deposit Account	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)

1	Request for Continued Examination (RCE)	sb0030e_fill.pdf	641442	no	3
Warnings:					
Information:					
2		4591-380e.pdf	492118	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment Submitted/Entered with Filing of CPA/RCE	1	5
	Applicant Arguments/Remarks Made in an Amendment	6	8

Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	fee-info.pdf	8183	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	1141743	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

RCE filed

PTO/SB/06 (12-04)
Approved for use through 7/31/2006. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 10/888,667

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))				395			790
SEARCH FEE (37 CFR 1.16(k), (l), or (m))							
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							
TOTAL CLAIMS (37 CFR 1.16(i))	17 minus 20 = *		x 25 =		OR	x 50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	5 minus 3 = *		x 100 =			x 200 =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			180			360	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	790.00

APPLICATION AS AMENDED – PART II

AMENDMENT A	(Column 1)		(Column 2)		(Column 3)	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	4/6/07	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA					
	Total (37 CFR 1.16(i))	17	Minus	** 20	=	x 25 =		OR	x 50 =	
	Independent (37 CFR 1.16(h))	5	Minus	*** 5	=	x 100 =		OR	x 200 =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					180		OR	360	
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B	(Column 1)	CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))					x 25 =		OR	50	
	Independent (37 CFR 1.16(h))		Minus	***		x 100 =		OR	200	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					180		OR	360	
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/888,667	07/08/2004	Pyung-Moon Zhang	4591-380	4240

20575 7590 05/14/2007

MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

EXAMINER	
HILTUNEN, THOMAS J	
ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
05/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	Application No. 10/888,667	Applicant(s) ZHANG ET AL.	
	Examiner Thomas J. Hiltunen	Art Unit 2816	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 03 May 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-5 and 7-18*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See attached sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

Continuation Of Part 11 Of Page 1

Applicant's arguments filed 03 May 2007 have been fully considered but they are not persuasive.

With respect to claims 12 and claim 18, Applicant's amendment of "selector" to -- detector -- changed the scope of the claims and thus necessitated the new grounds of rejection (i.e., a selector merely selects between input signals, wherein a detector provides detection/comparison between input signals).

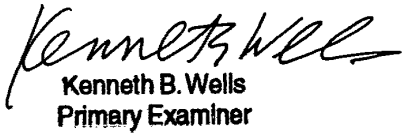
With respect to the argument that circuit 11 of Javanifard et al. (USPN 5,483,486) does not disclose "a detector circuit to generate the detect signal responsive to a comparison of the supply voltage and the high voltage" is not persuasive. It can be seen in Fig. 11 that when VCC is higher than VPP the output of Fig. 11 (i.e., the detect signal PD5VPP) draws a constant DC current (see Col. 15 lines 44-47). None of the claims require a specific relationship between the comparison of the supply voltage and the high voltage and the detect signals amplitude. The claims merely require that the detect signal is responsive to the comparison between the supply voltage and the high voltage, for instance see lines 6-7 of claim 1. The output of the of the detect signal of Fig. 11 (i.e., P5VPP) is at least responsive to a comparison between VCC (supply voltage) and VPP (high voltage), since its output current is a constant DC voltage when VCC is greater than VPP and the output of Fig. 11 is operates to indicate the level of VPP when VPP is larger than VCC.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on M-F 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TH
May 9, 2007



Kenneth B. Wells
Primary Examiner

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2816

PATENT APPLICATION
Docket No.: 4591-380
Client Ref. No.: ID13095-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Pyung-Moon ZHANG, et al.		
Confirmation No.:	4240		
Serial No.:	10/888,667	Examiner:	Hiltunen, Thomas J.
Filed:	July 8, 2004	Group Art Unit:	2816
For:	CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE		

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER FINAL REJECTION

To be entered
TJH
05/09/07

Responsive to the Final Office Action dated March 6, 2007, please amend the application as follows.

Claims begin on page 2.

Remarks begin on page 6.

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2816

PATENT APPLICATION
Docket No.: 4591-380
Client Ref. No.: ID13095-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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For:	CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE		

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER FINAL REJECTION

Responsive to the Final Office Action dated March 6, 2007, please amend the application as follows.

Claims begin on page 2.

Remarks begin on page 6.

CLAIMS

Please amend the claims as follows.

1. (Previously presented) A charge pump circuit comprising:

a charge pump block including at least one charge pump part; and

a voltage supply circuit to supply one of a supply voltage or a high voltage to the at least one charge pump part responsive to a detect signal, where the high voltage is higher than the supply voltage;

where the voltage supply circuit includes a detector circuit to generate the detect signal responsive to a comparison of the supply voltage and the high voltage.

2. (Currently amended) The charge pump circuit of claim 1 where the voltage supply circuit is ~~adapted~~ configured to supply the supply voltage in a general mode.

3. (Currently amended) The charge pump circuit of claim 1 where the voltage supply circuit is ~~adapted~~ configured to supply the high voltage in a test mode.

4. (Previously presented) The charge pump circuit of claim 1 where the voltage supply circuit includes:

a selector circuit to supply the one of the supply voltage or the high voltage responsive to the detect signal.

5. (Currently amended) The charge pump circuit of claim 1

where the charge pump block is ~~adapted~~ configured to generate an output voltage; and

where the voltage supply circuit comprises:

a voltage level sensing block to generate a level sensing signal responsive to a pump enable signal and the output voltage; and

an oscillator to generate complementary pulse signals responsive to the level sensing signal.

6. (Canceled)

7. (Currently amended) A charge pump circuit comprising:

a charge pump block to generate an output voltage;

a voltage level sensing block to generate a level sensing signal by sensing an output voltage;

an oscillator to generate complementary pulse signals responsive to the level sensing signal; and

a selecting circuit block to generate a selected voltage that is one of a high voltage and a supply voltage and to supply the selected voltage to the charge pump block responsive to detecting a level of the high voltage, the high voltage having a level higher than the supply voltage;

where the selecting circuit block includes a detector ~~adapted~~ configured to compare the supply voltage with the high voltage.

8. (Previously presented) The charge pump circuit of claim 7 where the charge pump block includes:

at least one charge pump part;

a charge supply part to precharge the at least one charge pump part with the selected voltage; and

a charge trapping part to store charges provided by the charge supply part.

9. (Original) The charge pump circuit of claim 8 where the at least one charge pump part pumps a charge to another charge pump part.

10. (Original) The charge pump circuit of claim 8 where the charge supply part comprises a high-voltage PMOS transistor.

11. (Previously presented) The charge pump circuit of claim 8 where the at least one charge pump part includes a high-voltage NMOS transistor.

12. (Currently amended) A charge pump circuit comprising:

a charge pump block to generate an output voltage;

a voltage level sensing block to generate a level sensing signal by sensing an output voltage;

an oscillator to generate complementary pulse signals responsive to the level sensing signal; and

a selecting circuit block, including a detector and a selector, to generate a selected voltage that is one of a high voltage and a supply voltage and to supply the selected voltage to the charge pump block responsive to detecting a level of the high voltage, the high voltage having a level higher than the supply voltage;

where the detector is ~~adapted~~ configured to compare the supply voltage with the high voltage; and

where the selector is ~~adapted~~ configured to select the high voltage if a level of the high voltage is higher than a level of the supply voltage.

13. (Previously presented) A charge pump circuit comprising:

a charge pump block including at least one charge pump part;

a voltage level sensing block to sense a level of an output voltage and generate a level sensing signal responsive thereto;

an oscillator to generate a pulse signal responsive to the level sensing signal;

a detector to generate a detection signal responsive to a comparison of a power voltage and a high voltage; and

a selector to provide one of the high voltage and the power voltage responsive to the detection signal to the charge pump block.

14. (Original) The charge pump circuit of claim 13 where the charge pump block comprises:

a charge supply part to precharge the at least one charge pump part; and

a charge trapping part to store charges pumped from the at least one charge pump part.

15. (Original) The charge pump circuit of claim 14 where the at least one charge pump part pumps charge to another serially connected charge pump part.

16. (Original) The charge pump circuit of claim 14 where the charge supply part includes a high-voltage PMOS transistor.

17. (Original) The charge pump circuit of claim 14 where the charge pump block includes a high-voltage NMOS transistor.

18. (Previously presented) A charge pump circuit comprising:

a charge pump block including at least one charge pump part;

a voltage level sensing block to sense a level of an output voltage and generate a level sensing signal responsive thereto;

an oscillator to generate a pulse signal responsive to the level sensing signal;

a detector to generate a detection signal responsive to a high voltage; and

a selector to provide one of the high voltage and a power voltage responsive to the detection signal to the charge pump block;

where the detector compares the high voltage to the power voltage.

REMARKS

The application includes claims 1-5 and 7-18 prior to entering this amendment.

The examiner objects to claims 2-3, 5 and 7-8 for certain informalities.

The examiner rejects claims 1-4 under 35 U.S.C. §102(b) as being anticipated by Javanifard, et al. (U.S. Patent 5,483,486).

The examiner rejects claims 5, 7-10 and 12-17 under 35 U.S.C. §103(a) as being unpatentable by Javanifard in view of Tanzawa, et al. (U.S. Patent 6,429,725).

The applicants amend claims 2, 3, 5, 7, 8 and 12. The application remains with claims 1-5 and 7-18 after entering this amendment.

The applicants add no new matter and request reconsideration.

FINALITY OF THE OFFICE ACTION

The applicants request that Examiner Hiltunen withdraw the finality of the office action for the following reasons.

The examiner rejected claims 12 and 18 under §112 in the immediately previous office action dated 10/05/2006. Specifically, the examiner objected to the phrase "selector" in claims 12 and 18. The applicants subsequently amended claims 12 and 18 to replace "selector" with "detector," without changing the scope of the recited "selector" (the amended "detector") element, and rewrote these claims in independent form.[1] The examiner made the current office action dated 03/06/2007 final, arguing that the applicants' amendment necessitated the new grounds of rejection.

The applicants believe that merely changing "selector" to "detector" in claims 12 and 18 and rewriting the claims in independent form does not change the scope of those claims. The new grounds of rejection for claims 12 and 18 were, thus, not necessitated by applicants' amendment, and hence, the current office action should not be final. MPEP 706.07(a).

Claim Objections

The examiner objects to claims 2-3, 5, and 7-8 for reciting "adapted to" and suggests amending the claims to read "configured to." The applicants note that claim 8 does not include

[1] Applicants' amendment filed on 01/04/2007.

the "adapted to" limitation. The applicants amend claims 2-3, 5, 7 and 12 as suggested by the examiner to obviate the objection.

Claim Rejections Under §102

The examiner rejects claims 1-4 as being old over Javanifard. The applicants traverse the rejection for the following reasons.

Claim 1 recites *the voltage supply circuit includes a detector circuit to generate the detect signal responsive to a comparison of the supply voltage and the high voltage.* Claims 7, 12-13 and 18 include similar limitations. The examiner alleges that Javanifard's 5V/12V VPP detector circuit[2] and the PD5VPP signal[3] "is responsive to a comparison of the supply voltage and the high voltage. (It can be seen in Fig. 11 that the PD5VPP signal is output responsive to a comparison between VPP (input to 170 of Fig. 11) and VCC (input to 175 of Fig. 11)."[4]

The applicants disagree with the examiner's interpretation of Javanifard. Javanifard's 5V/12V VPP level detector 55 "detects whether the programming supply voltage VPP is equal to 5 volts or 12 volts."[5] Javanifard discloses the following about the operation of the circuit:

"The operation of the circuit shown in FIG. 11 will now be discussed with respect to the time when power is first supplied to the flash EEPROM 20, at which time the external programming supply voltage VPP is equal to zero volts and begins to ramp towards its final value, which may be 5.0 volts or 12 volts. Initially, the voltage at node 157 is at system ground VSS, and the inverter 165 sets the control signal PD5VPP at a logic high level. As the programming supply voltage VPP increases, the amount of drain-source current for FET 155 increases, and node 157 begins to be pulled up towards the final value of VPP. If external VPP is sufficiently high, FET 155 acts as a strong pull-up device that overcomes the pull-down resistor 160. The inverter 165 sets the control signal PD5VPP at a logic low level if the voltage at node 157 is detected to be at a logic high level, indicating that the external programming supply voltage VPP is 12 volts. ... if the operating supply voltage VCC is greater than the programming supply voltage VPP, the circuit shown in FIG. 11 draws a constant DC current."[6] (Underline added.)

That is, Javanifard's PD5VPP signal is at logic high or logic low level depending on whether VPP is 5V or 12V. For example, if the signal PD5VPP is at a logic low level, it would indicate that the external programming supply voltage VPP is 12 volts.[7] In contrast, the limitations of claims 1, 7, 12, 13 and 18 do not recite determining the level of the voltage VPP.

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[2] Javanifard, figures 11 and 13b.
[3] Javanifard, figure 11.
[4] Office action dated 03/06/2007, page 3.
[5] Javanifard, column 14, lines 60-63.
[6] Javanifard, column 15, lines 21-47.
[7] Javanifard, column 15, lines 37-41.

Claim 1, rather, recites generating *the detect signal responsive to a comparison of the supply voltage and the high voltage*. Javanifard's PD5VPP signal is not responsive to a comparison of the supply voltage and the high voltage.

Although Javanifard discloses applying VCC to FET 175 in figure 11, it does not imply that the signal PD5VPP is responsive to a comparison of the VCC and VPP, as would be required by claims 1, 7, 12, 13 and 18. Rather, the FET 170 and the FET 175 merely "ensure correct operation of the 5 v/12 v VPP level detector 55 for the case wherein the operating supply voltage VCC is greater than the programming supply voltage VPP."[8]

Javanifard also discloses that "if the operating supply voltage VCC is greater than the programming supply voltage VPP, the circuit shown in FIG. 11 draws a constant DC current."[9] This disclosure, however, does not imply that the signal PD5VPP is generated in response to a comparison of VPP and VCC, as would be required by claims 1, 7, 12, 13 and 18.

For at least this reason, claims 1, 7, 12, 13 and 18 are in condition for allowance, along with associated dependent claims.

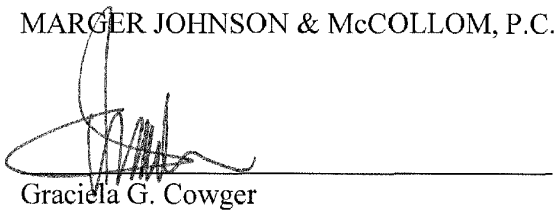
Conclusion

The applicants request reconsideration and allowance of remaining claims. The applicants encourage the Examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



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[8] Javanifard, column 15, lines 21-24.
[9] Javanifard, column 15, lines 44-47.

Electronic Acknowledgement Receipt

EFS ID:	1743112
Application Number:	10888667
International Application Number:	
Confirmation Number:	4240
Title of Invention:	Charge pump circuit operating responsive to a mode
First Named Inventor/Applicant Name:	Pyung-Moon Zhang
Customer Number:	20575
Filer:	Hosoon Lee/Stormi Davis
Filer Authorized By:	Hosoon Lee
Attorney Docket Number:	4591-380
Receipt Date:	03-MAY-2007
Filing Date:	08-JUL-2004
Time Stamp:	18:41:51
Application Type:	Utility

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1		4591-380d.pdf	604773	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Amendment After Final	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	9
Warnings:			
Information:			
	Total Files Size (in bytes):	604773	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

MISCELLANEOUS LETTER

REGARDING PAYMENT OF FEES AND EXTENSION OF TIME

	Claims Remaining After Amendment	Highest Number Previously Paid For	Present Extra Claims
Total Claims	17	18	0
Independent Claims	5	5	0

☒ Applicant petitions the Commissioner to extend the time for response (if applicable).

☒ Payment of fees is made via electronic filing system authorizing credit card payments for the extra claims and/or Petition.

☒ Applicant is paying with a Visa card; however, Applicant requests that any deficiency or overpayment be charged or credited to deposit account number 13-1703.

Respectfully submitted,

Customer No. 20575

MARGER JOHNSON & McCOLLOM, P.C.

Date: May 3, 2007

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PTO/SB/06 (08-03)
Approved for use through 7/31/2006. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 10886667

CLAIMS AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE	SMALL ENTITY FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY FEE
BASIC FEE (37 CFR 1.16(a))				$____	OR		$____
TOTAL CLAIMS (37 CFR 1.16(c))	17 minus 20 =	*	x $____ =		OR	x $____ =	
INDEPENDENT CLAIMS (37 CFR 1.16(b))	5 minus 3 =	*	x $____ =		OR	x $____ =	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(d))			+ $____ =		OR	+ $____ =	
			TOTAL		OR	TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

CLAIMS AS AMENDED – PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
5/3/07 Total (37 CFR 1.16(c))	* 17	Minus	** 20	=	x $____ =		OR	x $____ =	
Independent (37 CFR 1.16(b))	* 5	Minus	*** 5	=	x $____ =		OR	x $____ =	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $____ =		OR	+ $____ =	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
Total (37 CFR 1.16(c))	*	Minus	**	=	x $____ =		OR	x $____ =	
Independent (37 CFR 1.16(b))	*	Minus	***	=	x $____ =		OR	x $____ =	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $____ =		OR	+ $____ =	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
Total (37 CFR 1.16(c))	*	Minus	**	=	x $____ =		OR	x $____ =	
Independent (37 CFR 1.16(b))	*	Minus	***	=	x $____ =		OR	x $____ =	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $____ =		OR	+ $____ =	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

CLAIMS ONLY

Application Number: 10588667

Filing Date:

Applicant(s):

* May be used for additional claims or amendments

CLAIMS	AS FILED		AFTER FIRST AMENDMENT		AFTER SECOND AMENDMENT	
	Indep	Depend	Indep	Depend	Indep	Depend
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Total Depend			2			
Total Claims			7			

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Total Depend						
Total Claims						

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/888,667	07/08/2004	Pyung-Moon Zhang	4591-380	4240

20575 7590 03/06/2007

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PORTLAND, OR 97204

EXAMINER	
HILTUNEN, THOMAS J	
ART UNIT	PAPER NUMBER
2816	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/888,667	ZHANG ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Summary of Changes

1. Applicant's amendment/arguments has overcome all previous rejections under 35 USC § 112, second paragraph.
2. Claims 1-5, and 7-18 are newly rejected as necessitated by Applicant's Amendment.

Claim Objections

Claims 2, 3, 5, 7, and 8 are objected to because of the following informalities:

It has been held that the recitation that an element is "adapted to " perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchinson,* 69 USPQ 138. Thus it is suggested that the recitation(s) of "adapted to" in claims 2, 3, 5, 7, and 8 be amended to read --configured to --. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

Claims 1-4 rejected under 35 U.S.C. 102(b) as being anticipated by Javanifard et al . (USPN 5,483,486) (hereinafter Javanifard).

With respect to claim 1, Javanifard discloses in Figs. 3B, 11, 13B, and 17, "a charge pump circuit comprising (Circuit of Fig. 17):

a charge pump block (320a) including at least one charge pump part (320a inherently includes at least one charge pump part since it is itself a charge pump); and

a voltage supply circuit (419, and control logic 230 and circuits controlling control logic 230, (see Figs. 3B, 11, and 13B which discloses the details of the control logic and the circuits that output to the control logic) to supply one of a supply voltage (Vcc) or a high voltage (Vpp) to the at least one charge pump part responsive to a detect signal (320a's power supply of Vpp or Vcc is responsive to the detect signal output by 230), where the high voltage is higher than the supply voltage (Vpp is higher than Vcc)

Where the voltage supply circuit includes a detector circuit (5V/12V VPP detector that outputs PD5VPP, that controls 230 (see Figs. 11 and 13B)) to generate the detect signal (230 generates its output (i.e. detect signal) responsive to the PD5VPP signal output by the circuit of Fig. 11 (again see Figs. 11 and 13B)), which is responsive to a comparison of the supply voltage and the high voltage. (It can be seen in Fig. 11 that the PD5VPP signal is output responsive to a comparison between VPP (input to 170 of Fig. 11) and Vcc (input to 175 of Fig. 11). Clearly when Vcc is higher than Vpp the output of 165 (i.e. the PD5VPP signal) will be approximately equal to the Vcc supply voltage (see Col. 15 lines 44-47), and when VPP is sufficiently higher than VCC (i.e. approximately 12 V) 165 will output PD5VPP has a low (see Col. 15 lines 37-41). Thus the output of the circuit of Fig. 11 (i.e. PD5VPP) is responsive to a comparison between VPP and VCC, which controls logic circuit 230 which outputs the detect signal. Thus

the detect signal is generated responsive to a comparison of the supply voltage and the high voltage)."

With respect to claim 2, Javanifard discloses, "the charge pump circuit of claim 1 where the voltage supply circuit is adapted to supply the supply voltage in a general mode (the above recitation is merely functional langue and when Vcc is supplied to 320a corresponds to a "general mode")."

With respect to claim 3, Javanifard discloses, "the charge pump circuit of claim 1 where the voltage supply circuit is adapted to supply the high voltage in a test mode (the above recitation is merely functional langue and when Vpp is supplied to 320a corresponds to a "test mode")."

With respect to claim 4, Javanifard discloses, "the charge pump circuit of claim 1 where the voltage supply circuit includes:

a selector circuit (419 of Fig. 17) to supply the one of the supply voltage or the high voltage responsive to the detect signal (clearly 419 is controlled by the detect signal (i.e. output of control logic 230) and is controlled to select one of Vcc and Vpp to be supplied to 320a)."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented

and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, and 7-10, 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Javanifard (USPN 5,483,486) in view of Tanzawa et al. (USPN 6,429,725).

With respect to claim 5, Javanifard et al. discloses "the charge pump circuit of claim 1 (see above rejection) where the charge pump block is adapted to generate an output voltage (320a outputs a boosted voltage)."

Javanifard et al. fails to disclose the specifics of the charge pump circuit (320a). Thus, Javanifard et al. fails to disclose "a voltage level sensing block to generate a level sensing signal responsive to a pump enable signal and the output voltage; and an oscillator to generate complementary pulse signals responsive to the level sensing signal."

However, Tanzawa et al. discloses in Fig. 1 a specific charge pump circuit with constant boost efficiency (see Col. 4 lines 39-42) composed of a standby oscillator (OSC1) and an active oscillator (OSC2). Furthermore, Tanzawa et al. discloses "a voltage level sensing block (R11, R12 and OP1) to generate a level sensing signal (output of OP1) responsive to a pump enable signal (ACT) and the output voltage (OUT); and an oscillator (OSC1) to generate complementary pulse signals (clock signals output from I12 and I14) responsive to the level sensing signal (clearly OSC1 is responsive to the output of OP1 input to ND1)."

Therefore it would have been prima facie obvious to one of ordinary skill in the art at the time of the invention to replace the generic charge pump (320a) of Javanifard with the specific charge pump (charge pump of Fig. 1) of Tanzawa et al. for the purpose of increasing pump efficiency of the charge pump circuit of Javanifard. One would have been motivated to replace the generic charge pump (320a) of Javanifard with the specific charge pump (pump of Fig. 1) and oscillators (OSC1 and OSC2) of Tanzawa et al. to increase pump efficiency and maintain steady state operation. Thus the above combination discloses all of the recited limitations of claim 5.

With respect to claims 7 and 12, Javanifard discloses, in Figs. 3B, 11, 13B, and 17, "a charge pump block (320a of Fig. 17) to generate an output voltage (320a generates an output voltage); and

a selecting circuit block (419, and control logic 230 and circuits controlling control logic 230, (see Figs. 3B, 11, and 13B which discloses the details of the control logic and the circuits that output to the control logic), including a detector (circuit of Fig. 11 that detects the Vpp level) and a selector (419 and control logic 230 of Fig. 17, which selects between Vcc and Vpp) to generate a selected voltage that is one of a high voltage (Vpp) and a supply voltage (Vcc) to supply the selected voltage to the charge pump block responsive to detecting a level of the high voltage (Vpp and Vcc are supplied to 320a via switch circuit 419 according to the detection of Vpp in the circuit of Fig. 11 which controls the control logic 230 that controls switch 419 (see Fig. 13B and Fig. 11), the high having a level higher than the supply voltage (Vpp is higher than Vcc)

wherein the selection circuit block includes a detector (detector of Fig. 11 which controls control logic 230, see Figs. 11 and 13B) adapted to compare the supply voltage with high voltage (It can be seen in Fig. 11 that the PD5VPP signal is output responsive to a comparison between VPP (input to 170 of Fig. 11) and Vcc (input to 175 of Fig. 11). Clearly when Vcc is higher than Vpp the output of 165 (i.e. the PD5VPP signal) will be approximately equal to the Vcc supply voltage (see Col. 15 lines 44-47), and when VPP is sufficiently higher than VCC (i.e. approximately 12 V) 165 will output PD5VPP has a low (see Col. 15 lines 37-41). Thus the output of the circuit of Fig. 11 (i.e. PD5VPP) is responsive to a comparison between VPP and VCC, which controls logic circuit 230 which outputs the detect signal. Thus the detector compares the supply voltage with the high voltage.)

where the detector (detector of Fig. 11) is adapted to compare the supply voltage with the high voltage (It can be seen in Fig. 11 that the PD5VPP signal is output responsive to a comparison between VPP (input to 170 of Fig. 11) and Vcc (input to 175 of Fig. 11). Clearly when Vcc is higher than Vpp the output of 165 (i.e. the PD5VPP signal) will be approximately equal to the Vcc supply voltage (see Col. 15 lines 44-47), and when VPP is sufficiently higher than VCC (i.e. approximately 12 V) 165 will output PD5VPP has a low (see Col. 15 lines 37-41). Thus the output of the circuit of Fig. 11 (i.e. PD5VPP) is responsive to a comparison between VPP and VCC, which controls logic circuit 230 which outputs the detect signal. Thus the detector compares the supply voltage with the high voltage.); and

where the selector is adapted to select the high voltage if a level of the high voltage is higher than a level of the power supply voltage (if the control logic determines that a high voltage i.e. Vpp is required, then Vpp will be selected when Vpp is higher than Vcc)."

Javanifard fails to disclose the specifics of the charge pump circuit (320a). Thus, Javanifard fails to disclose "a voltage level sensing block to generate a level sensing signal by sensing an output voltage; and

an oscillator to generate complementary pulse signals responsive to the level sensing signal."

However, Tanzawa et al. discloses in Fig. 1 a specific charge pump circuit with constant boost efficiency (see Col. 4 lines 39-42) composed of a standby oscillator (OSC1) and an active oscillator (OSC2). Furthermore, Tanzawa et al. discloses "a voltage level sensing block (R11, R12, and OP1) to generate a level sensing signal (output of OP1) by sensing an output voltage (OUT (output of charge pump)); and

an oscillator (OSC1) to generate complementary pulse signals (output of I1 and I12) responsive to the level sensing signal (OSC1 is responsive to the output of OP1 input to ND1);

Therefore it would have been prima facie obvious to one of ordinary skill in the art at the time of the invention to replace the generic charge pump (320a) of Javanifard with the specific charge pump (pump of Fig. 1) and oscillators (OSC1 and OSC2) of Tanzawa et al. for the purpose of increasing pump efficiency of the charge pump circuit of Javanifard. One would have been motivated to replace the generic charge pump

(320a) of Javanifard. with the specific charge pump (pump of Fig. 1) and oscillators (OSC1 and OSC2) of Tanzawa et al to increase pump efficiency and maintain steady state operation. Thus the above combination discloses all of the recited limitations of claim 7.

With respect to claims 8 and 14, the above combination discloses, "the charge pump circuit of claim 7 where the charge pump block includes:

at least one charge pump part;

a charge supply part (N11) to precharge the at least one charge pump part with the selected voltage (N11 supplies one the selected to voltages of Vpp or Vcc as modified above to the charge pump of C11, C12, N12, and N13, to precharge node Cn1 to one of the selected voltages); and

a charge trapping part to store charges provided by the charge supply part (N13 "traps" the charge at node CN2 until the voltage at CN2 becomes larger than the threshold voltage of N13, and then the voltage at CN2 will be output)."

With respect to claims 9 and 15, the above combination discloses, "the charge pump circuit of claim 8 where the at least one charge pump part pumps a charge to another charge pump part (the charge pump connected at CN1 pumps charge into CN2, where N13 and C12 also function as a charge pump)."

With respect to claims 10 and 16, the above combination discloses, "the charge pump circuit of claim 8 where the charge supply part comprises a high-voltage PMOS transistor (N11 is a high voltage PMOS transistor)."

With respect to claims 13 and 18, the above combination discloses of Javanifard and Tanzawa et al, "a charge pump circuit comprising:

a charge pump block including at least one charge pump part (320a of Fig. 17 of Javanifard)

a voltage level sensing block (OP1, R11 and R12 of Fig. 1 of Tanzawa eat al.) to sense a level of an output voltage (OUT (output of charge pump 320a as modified above) and generate a level sensing signal responsive thereto (the output of OP1 is responsive to the OUT signal);

an oscillator to generate a pulse signal responsive to the level sensing signal (OSC1 Outputs a signal in response to OP1);

a detector to generate a detection signal responsive to a comparison of a power voltage and a high voltage (Circuit of Fig. 11 of Javanifard. It can be seen in Fig. 11 that the PD5VPP signal is output responsive to a comparison between VPP (input to 170 of Fig. 11) and Vcc (input to 175 of Fig. 11). Clearly when Vcc is higher than Vpp the output of 165 (i.e. the PD5VPP signal) will be approximately equal to the Vcc supply voltage (see Col. 15 lines 44-47), and when VPP is sufficiently higher than VCC (i.e. approximately 12 V) 165 will output PD5VPP has a low (see Col. 15 lines 37-41). Thus the output of the circuit of Fig. 11 (i.e. PD5VPP) is responsive to a comparison between VPP and VCC, which controls logic circuit 230 which outputs the detect signal. Thus the detector compares power voltage with the high voltage.);

a selector circuit (230 and 419 of Fig. 17 of Javanifard) to supply the one of the supply voltage or the high voltage responsive to the detect signal (clearly 230 is

controlled by the detect signal (see Fig. 13B) and 230 controls the 419 to selected one of Vcc and Vpp to be supplied to 320a);

where the detector compares the high voltage to the power voltage (Circuit of Fig. 11 of Javanifard. It can be seen in Fig. 11 that the PD5VPP signal is output responsive to a comparison between VPP (input to 170 of Fig. 11) and Vcc (input to 175 of Fig. 11). Clearly when Vcc is higher than Vpp the output of 165 (i.e. the PD5VPP signal) will be approximately equal to the Vcc supply voltage (see Col. 15 lines 44-47), and when VPP is sufficiently higher than VCC (i.e. approximately 12 V) 165 will output PD5VPP has a low (see Col. 15 lines 37-41). Thus the output of the circuit of Fig. 11 (i.e. PD5VPP) is responsive to a comparison between VPP and VCC, which controls logic circuit 230 which outputs the detect signal. Thus the detector compares power voltage with the high voltage)."

Claims 11, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Javanifard et al. (USPN 5,483,486) in view of Tanzawa et al. (USPN 6,429,725). Javanifard et al. and Tanzawa et al. teach the circuits as recited in claims 8 and 14 see above rejections. Tanzawa et al. fails to disclose is a charge pump with NMOS transistors. However, it is notoriously well-know in the art that the charge pump transistors of Tanzawa et al. are actually diode-connected transistors (connecting the gate of the transistors to the drain of the transistor). It is also notoriously well-know that both PMOS and NMOS transistors function the same when connected as diodes, and that it would make no difference if the PMOS transistors of the charge pumps of Tanzawa et al. where replace by NMOS transistors (For example, Rao (USPN

6,177,830) discloses a charge pump composed of diode connected NMOS transistors. Furthermore, Dosho et al. (USPN 5,751,142) discloses in Fig. 6 that diode circuits may be composed of either NMOS or PMOS transistors.).

It would have been *prima facie* obvious to one of ordinary skill in the art at the time the invention was made to replace the PMOS transistors, with NMOS transistors, due to the doctrine of equivalents.

With respect to claims 11 and 17, the above combination discloses, "the charge pump circuit of claim 7 where the at least one charge pump part includes a high-voltage NMOS transistor (N12 and N13 are both NMOS transistors as modified above)."

Response to Arguments

Applicant's arguments with respect to claims 1-5, and 7-18 have been considered but are moot in view of the new ground(s) of rejection.

Clearly it can be seen that claims 1, 7, 12, 13, and 18 have been amended to included new limitations that were not previously considered by the Examiner for instance a "*detector*" that compares the high voltage with the power (supply) voltage was not previously considered. Clearly it can be seen as previously recited the claims required "*a selector*" circuit that compares the high voltage with a power (supply) voltage. Thus the above claims are newly rejected as necessitated by Applicant's amendment.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH
March 1, 2007

LINH MY NGUYEN
PRIMARY EXAMINER

Notice of References Cited	Application/Control No. 10/888,667	Applicant(s)/Patent Under Reexamination ZHANG ET AL.	
	Examiner Thomas J. Hiltunen	Art Unit 2816	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,751,142	05-1998	Dosho et al.	323/316
*	B	US-5,483,486	01-1996	Javanifard et al.	365/185.17
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
10/888,667	ZHANG ET AL.	
Examiner	**Art Unit**	
Thomas J. Hiltunen	2816	

SEARCHED			
Class	Subclass	Date	Examiner
327	536,537 143,82,60, 63	11/9/2005	TH
363	60	11/9/2005	TH
Updated	above	4/6/2006	TH
Updated	above	9/27/2006	TH
363	63	9/28/2006	TH
Updated	above	3/1/2007	TH
363	59	3/1/2007	TH
365	189.09	3/1/2007	TH

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
See attached EAST text search	11/14/2005	TH
See attached EAST text search	4/10/2006	TH
See attached EAST text search	9/28/2006	TH
See attached EAST text search	3/7/2007	TH

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/888,667	ZHANG ET AL.
Examiner	**Art Unit**
Thomas J. Hiltunen	2816

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	3/1/07
	1	✓
	2	✓
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	4	✓
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	9	✓
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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L25	250930	(voltage current charge) with (pump$4 multipl$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/03/01 09:21
L26	863507	supply near2 voltage power near2 supply power near2 voltage	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/03/01 09:21
L27	94523	vcc vdd	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/03/01 09:21
L29	694371	(pump$3 boost$3 output high$4) near2 voltage	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/03/01 09:22
L30	860511	mux multiplexer multiplexor selecter selector select$3 near3 (circuit device element block)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/03/01 09:23
L31	4258083	sens$4 detect$4 monitor$4	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/03/01 09:24
L32	888245	26 27	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/03/01 09:24
L33	10525	vpp vpump vboost	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/03/01 09:24
L34	697345	33 29	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/03/01 09:24

EAST Search History

L36	10517	30 same 32 same 34	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/03/01 09:25
L37	1618	25 same 36	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/03/01 09:25
L38	482	37 same 31	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/03/01 09:30
L47	1136	37 not 38	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/03/01 11:10
L48	793	47 and 31	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/03/01 11:13

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Pyung-Moon ZHANG, et al.		
Serial No.:	10/888,667	Examiner:	Hiltunen, Thomas J.
Filed:	July 8, 2004	Group Art Unit:	2816
Confirmation No.:	4240		
For:	CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE		
Date:	January 4, 2007		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Responsive to the Office Action dated October 5, 2006, please amend the application as follows.

Claims begin on page 2.

Remarks begin on page 6.

CLAIMS

Please amend the claims as follows.

1. (Currently amended) A charge pump circuit comprising:

a charge pump block including at least one charge pump part; and

a voltage supply circuit to supply one of a supply voltage or a high voltage to the at least one charge pump part responsive to a detect signal ~~detecting a level of the high voltage~~, where the high voltage is higher than the supply voltage;

where the voltage supply circuit includes a detector circuit to generate the detect signal responsive to a comparison of the supply voltage and the high voltage.

2. (Previously presented) The charge pump circuit of claim 1 where the voltage supply circuit is adapted to supply the supply voltage in a general mode.

3. (Previously presented) The charge pump circuit of claim 1 where the voltage supply circuit is adapted to supply the high voltage in a test mode.

4. (Currently amended) The charge pump circuit of claim 1 where the voltage supply circuit ~~comprises~~ includes:

~~a detector circuit to generate a detect signal responsive to the high voltage; and~~

a selector circuit to supply the one of the supply voltage or the high voltage responsive to the detect signal.

5. (Previously presented) The charge pump circuit of claim 1

where the charge pump block is adapted to generate an output voltage; and

where the voltage supply circuit comprises:

a voltage level sensing block to generate a level sensing signal responsive to a pump enable signal and the output voltage; and

an oscillator to generate complementary pulse signals responsive to the level sensing signal.

6. (Canceled)

7. (Previously presented) A charge pump circuit comprising:

a charge pump block to generate an output voltage;

a voltage level sensing block to generate a level sensing signal by sensing an output voltage;

an oscillator to generate complementary pulse signals responsive to the level sensing signal; and

a selecting circuit block to generate a selected voltage that is one of a high voltage and a supply voltage and to supply the selected voltage to the charge pump block responsive to detecting a level of the high voltage, the high voltage having a level higher than the supply voltage;

where the selecting circuit block includes a detector adapted to compare the supply voltage with the high voltage.

8. (Previously presented) The charge pump circuit of claim 7 where the charge pump block includes:

at least one charge pump part;

a charge supply part to precharge the at least one charge pump part with the selected voltage; and

a charge trapping part to store charges provided by the charge supply part.

9. (Original) The charge pump circuit of claim 8 where the at least one charge pump part pumps a charge to another charge pump part.

10. (Original) The charge pump circuit of claim 8 where the charge supply part comprises a high-voltage PMOS transistor.

11. (Previously presented) The charge pump circuit of claim 8 where the at least one charge pump part includes a high-voltage NMOS transistor.

12. (Currently amended) ~~The charge pump circuit of claim 7~~ A charge pump circuit comprising:

a charge pump block to generate an output voltage;

a voltage level sensing block to generate a level sensing signal by sensing an output voltage;

an oscillator to generate complementary pulse signals responsive to the level sensing signal; and

a selecting circuit block, including a detector and a selector, to generate a selected voltage that is one of a high voltage and a supply voltage and to supply the selected voltage to the charge pump block responsive to detecting a level of the high voltage, the high voltage having a level higher than the supply voltage;

where the ~~selecting circuit block~~ detector is adapted to compare the supply voltage with the high voltage; and

where the ~~selecting circuit block~~ selector is adapted to select the high voltage if a level of the high voltage is higher than a level of the ~~power~~ supply voltage.

13. (Previously presented) A charge pump circuit comprising:

a charge pump block including at least one charge pump part;

a voltage level sensing block to sense a level of an output voltage and generate a level sensing signal responsive thereto;

an oscillator to generate a pulse signal responsive to the level sensing signal;

a detector to generate a detection signal responsive to a comparison of a power voltage and a high voltage; and

a selector to provide one of the high voltage and [[a]]the power voltage responsive to the detection signal to the charge pump block.

14. (Original) The charge pump circuit of claim 13 where the charge pump block comprises:

a charge supply part to precharge the at least one charge pump part; and

a charge trapping part to store charges pumped from the at least one charge pump part.

15. (Original) The charge pump circuit of claim 14 where the at least one charge pump part pumps charge to another serially connected charge pump part.

16. (Original) The charge pump circuit of claim 14 where the charge supply part includes a high-voltage PMOS transistor.

17. (Original) The charge pump circuit of claim 14 where the charge pump block includes a high-voltage NMOS transistor.

18. (Currently amended) ~~The charge pump circuit of claim 13~~ A charge pump circuit comprising:

a charge pump block including at least one charge pump part;

a voltage level sensing block to sense a level of an output voltage and generate a level sensing signal responsive thereto;

an oscillator to generate a pulse signal responsive to the level sensing signal;

a detector to generate a detection signal responsive to a high voltage; and

a selector to provide one of the high voltage and ~~the~~ a power voltage responsive to the detection signal to the charge pump block;

where the ~~selector~~ detector compares the high voltage to the power voltage.

REMARKS

The application includes claims 1-5 and 7-18 prior to entering this amendment.

The examiner rejects claims 12 and 18 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that the applicants regard as the invention.

The examiner rejects claims 1-4 under 35 U.S.C. § 102(b) as being anticipated by Javanifard, et al. (U.S. patent no. 5,781,473).

The examiner rejects claims 5, 7-10 and 13-16 under 35 U.S.C. §103(a) as being unpatentable by Javanifard in view of Tanzawa, et al. (U.S. patent no. 6,429,725).

The examiner rejects claims 11 and 17 under 35 U.S.C. 103(a) as being unpatentable by Javanifard in view of Tanzawa, et al. (U.S. patent no. 6,429,725).

The applicants amend claims 1, 4, 7, 12 and 13 and cancels claim 18. The application remains with claims 1-5 and 7-17 after this amendment. The applicants add no new matter and request reconsideration.

Claim Rejections Under §112

Although the examiner rejects claim 12 and 18 as indefinite, he does not reject claims 12 and 18 for any other patentability reason. The applicants rewrite claims 12 and 18 in independent form and to make clear that which the applicants claim as their invention. Claims 12 and 18 are now in condition for allowance.

Claim Rejections Under §102

The examiner rejects claims 1-4 as being old over Javanifard. The applicants traverse the rejection for the following reasons.

The applicants amend claim 1 to recite *the voltage supply circuit includes a detector circuit to generate the detect signal responsive to a comparison of the supply voltage and the high voltage*. The Applicants amend claims 7 and 13 to include similar limitations from claims 12 and 18, respectively. The examiner alleges that Javanifard discloses a voltage supply circuit, which includes level detectors 230 and 231 for detecting a level of the high voltage V_{PP}. Javanifard discloses, in figure 2, a 5/12 V_{PP} level detector 230 and a 3/5 V_{PP} level detector 231.

The 5/12 V_{PP} level detector 230 is used to determine whether V_{PP} is at 5 volts or 12 volts.[1] Similarly, the 3/5 V_{PP} level detector 231 is used to determine whether V_{PP} is at 3 volts or 5 volts. The level detectors 230 and 231, thus, detect the V_{PP} voltage level. But the level detectors do not compare the level of the supply voltage and the high voltage V_{PP}, as required by the claims. The applicants note that Javanifard does not disclose any details regarding how the level detectors 230 and 231 determine whether Vpp is 5 or 12 volts or 3 or 5 volts. Javanifard, thus, fails to disclose a detector circuit to generate a detect signal responsive to a comparison of the supply voltage and the high voltage, as recited in claims 1, 7 and 13. For at least this reason, claims 1, 7 and 13 should be allowable, along with associated dependent claims.

Conclusion

The applicants request reconsideration and allowance of remaining claims. The applicants encourage the Examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Customer No. 20575

Respectfully submitted,

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Graciela G. Cowger
Registration No. 42,444

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Portland, OR 97204
(503) 222-3613

[1] Javanifard, column 6, line 67-column 7, line 4.

Electronic Patent Application Fee Transmittal

Application Number:	10888667
Filing Date:	08-Jul-2004
Title of Invention:	Charge pump circuit operating responsive to a mode
First Named Inventor/Applicant Name:	Pyung-Moon Zhang
Filer:	Alexander Charles Johnson/Li mei Vermilya
Attorney Docket Number:	4591-380

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Independent claims in excess of 3	1201	2	200	400
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
		Total in USD ($)		**400**

Electronic Acknowledgement Receipt

EFS ID:	1417885
Application Number:	10888667
International Application Number:	
Confirmation Number:	4240
Title of Invention:	Charge pump circuit operating responsive to a mode
First Named Inventor/Applicant Name:	Pyung-Moon Zhang
Customer Number:	20575
Filer:	Alexander Charles Johnson/Li mei Vermilya
Filer Authorized By:	Alexander Charles Johnson
Attorney Docket Number:	4591-380
Receipt Date:	04-JAN-2007
Filing Date:	08-JUL-2004
Time Stamp:	20:11:56
Application Type:	Utility

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	$400
RAM confirmation Number	881
Deposit Account	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)

1		4591-380c.pdf	793882	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Amendment - After Non-Final Rejection	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	8

Warnings:

Information:

2	Fee Worksheet (PTO-06)	fee-info.pdf	8169	no	2

Warnings:

Information:

Total Files Size (in bytes):	802051

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

MISCELLANEOUS LETTER

REGARDING PAYMENT OF FEES AND EXTENSION OF TIME

	Claims Remaining After Amendment	Highest Number Previously Paid For	Present Extra Claims
Total Claims	17	17	
Independent Claims	5	3	2

☒ Applicant petitions the Commissioner to extend the time for response (if applicable).

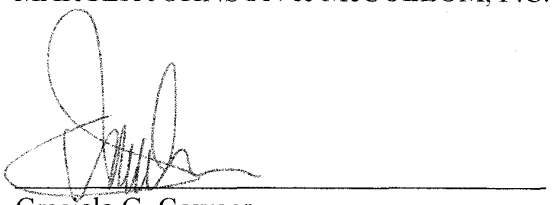
☒ Payment of fees is made via electronic filing system authorizing credit card payments for the extra claims and/or Petition.

☒ Applicant is paying with Visa card however requests that any deficiency or overpayment be charged or credited to deposit account number 13-1703.

Respectfully submitted,

Customer No. 20575

MARGER JOHNSON & McCOLLOM, P.C.



Date: January 4, 2007

Graciela G. Cowger
Reg. No. 42,444

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PTO/SB/06 (12-04)
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PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Application or Docket Number: 10/888,661

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE							770
SEARCH FEE (37 CFR 1.16(k), (l), or (m))							
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							
TOTAL CLAIMS (37 CFR 1.16(i))	18 minus 20 = *		x =		OR	x 18 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 = *		x =			x 86 =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))						390	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	770

APPLICATION AS AMENDED – PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
AMENDMENT A	7/21/06									
	Total (37 CFR 1.16(i))	* 17	Minus	** 20	=	x =		OR	50 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	=	x =		OR	x200 =	
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR	320	
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT B	4/4/07									
	Total (37 CFR 1.16(i))	* 17	Minus	** 17	= 0	x =		OR	x =	
	Independent (37 CFR 1.16(h))	* 5	Minus	*** 3	= 2	x =		OR	x 200 =	400,-
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	400,-

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/888,667	07/08/2004	Pyung-Moon Zhang	4591-380	4240

20575 7590 10/05/2006

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PORTLAND, OR 97204

EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/888,667	ZHANG ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-,5 and 7-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Summary of Changes

1. Applicant's amendment has successfully overcome the previous rejections of claims 1-5, 7-8, and 11-13 under 35 U.S.C. 112, second paragraph.
2. Claims 1-11, and 13-18 are newly rejected based on newly found art.

The indicated allowability of claims 7-18 is withdrawn in view of the newly discovered reference(s) to Javanifard (USPN 5,781,473). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 12 and 18 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 18, the recitation of "where the selector compares the high voltage to the power voltage" is misdescriptive, this is because "the selector" merely selects between Vcc (the supply voltage) and Vpp (the high voltage) and in no way does it "compare" the two voltages. For example see Fig. 6, which discloses "the selector" being composed switched circuit that in no way makes a comparison between Vcc and Vpp. Claim 12 is rejected for the same reasons as claim 18.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

Claims 1-4 rejected under 35 U.S.C. 102(b) as being anticipated by Javanifard et al (USPN 5,781,473).

With respect to claim 1, Javanifard et al. discloses in Fig. 2, "a charge pump circuit comprising:

a charge pump block (220) including at least one charge pump part (220 inherently includes at least one charge pump part since it is itself a charge pump); and

a voltage supply circuit (230, 231, 290 and switches connected to Vpp, Vcc, and 220) to supply one of a supply voltage (Vcc) or a high voltage (Vpp) to the at least one charge pump part responsive to detecting a level of the high voltage (Vpp and Vcc are supplied to 220 via switches connected to Vcc, Vpp, and 220 according to the detection of Vpp at 230 and 231), where the high voltage is higher than the supply voltage (Vpp is higher than Vcc)."

With respect to claim 2, Javanifard et al. discloses, "the charge pump circuit of claim 1 where the voltage supply circuit is adapted to supply the supply voltage in a general mode (the above recitation is merely functional langue and when Vcc is supplied to 220 corresponds to a "general mode")."

With respect to claim 3, Javanifard et al. discloses, "the charge pump circuit of claim 1 where the voltage supply circuit is adapted to supply the high voltage in a test

mode (the above recitation is merely functional langue and when Vpp is supplied to 220 corresponds to a "test mode")."

With respect to claim 4, Javanifard et al. discloses, "the charge pump circuit of claim 1 where the voltage supply circuit comprises:

a detector circuit (230 or 231) to generate a detect signal (output of 230 or 231) responsive to the high voltage (230 and 231 are responsive to Vpp); and

a selector circuit (290 and the switches connected to Vpp, Vcc, and 220) to supply the one of the supply voltage or the high voltage responsive to the detect signal (clearly 290 is controlled by the detect signals and controls the switches to selected one of Vcc and Vpp to be supplied to 220)."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 7-10, and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Javanifard et al. (USPN 5,781,473) in view of Tanzawa et al. (USPN 6,429,725).

With respect to claim 5, Javanifard et al. discloses "the charge pump circuit of claim 1 where the charge pump block is adapted to generate an output voltage (220

outputs a boosted voltage)." Furthermore, Javanifard et al. discloses the charge pump being responsive to an active oscillator (241) and standby oscillator (242).

Javanifard et al. fails to disclose the specifics of the charge pump circuit (220) and oscillator circuits (241 and 242). Thus, Javanifard et al. fails to disclose "a voltage level sensing block to generate a level sensing signal responsive to a pump enable signal and the output voltage; and an oscillator to generate complementary pulse signals responsive to the level sensing signal."

However, Tanzawa et al. discloses in Fig. 1 a specific charge pump circuit with constant boost efficiency (see Col. 4 lines 39-42) composed of a standby oscillator (OSC1) and an active oscillator (OSC2). Furthermore, Tanzawa et al. discloses "a voltage level sensing block (R11, R12 and OP1) to generate a level sensing signal (output of OP1) responsive to a pump enable signal (ACT) and the output voltage (OUT); and an oscillator (OSC1) to generate complementary pulse signals (clock signals output from I12 and I14) responsive to the level sensing signal (clearly OSC1 is responsive to the output of OP1 input to ND1)."

Therefore it would have been prima facie obvious to one of ordinary skill in the art at the time of the invention to replace the generic charge pump (220) and oscillators (241 and 242) of Javanifard et al. with the specific charge pump (pump of Fig. 1) and oscillators (OSC1 and OSC2) of Tanzawa et al. for the purpose of increasing pump efficiency of the charge pump circuit of Javanifard et al. One would have been motivated to replace the generic charge pump (220) and oscillators (241 and 242) of Javanifard et al. with the specific charge pump (pump of Fig. 1) and oscillators (OSC1

and OSC2) of Tanzawa et al to increase pump efficiency and maintain steady state operation. Thus the above combination discloses all of the recited limitations of claim 5.

With respect to claim 7, Javanifard et al. discloses, in Fig. 2, "a charge pump block (220) to generate an output voltage (220 generates an output voltage); and

a selecting circuit block (230, 231, 290 and switches connected to Vpp, Vcc, and 220) to generate a selected voltage that is one of a high voltage (Vpp) and a supply voltage (Vcc) to supply the at selected voltage to the charge pump block responsive to detecting a level of the high voltage (Vpp and Vcc are supplied to 220 via switches connected to Vcc, Vpp, and 220 according to the detection of Vpp at 230 and 231), the high having a level higher than the supply voltage (Vpp is higher than Vcc)." Furthermore, Javanifard et al. discloses the charge pump being responsive to an active oscillator (241) and standby oscillator (242).

Javanifard et al. fails to disclose the specifics of the charge pump circuit (220) and oscillator circuits (241 and 242). Thus, Javanifard et al. fails to disclose "a voltage level sensing block to generate a level sensing signal by sensing an output voltage; and

an oscillator to generate complementary pulse signals responsive to the level sensing signal."

However, Tanzawa et al. discloses in Fig. 1 a specific charge pump circuit with constant boost efficiency (see Col. 4 lines 39-42) composed of a standby oscillator (OSC1) and an active oscillator (OSC2). Furthermore, Tanzawa et al. discloses "a voltage level sensing block (R11, R12, and OP1) to generate a level sensing signal (output of OP1) by sensing an output voltage (OUT (output of charge pump)); and

an oscillator (OSC1) to generate complementary pulse signals (output of I1 and I12) responsive to the level sensing signal (OSC1 is responsive to the output of OP1 input to ND1);

Therefore it would have been prima facie obvious to one of ordinary skill in the art at the time of the invention to replace the generic charge pump (220) and oscillators (241 and 242) of Javanifard et al. with the specific charge pump (pump of Fig. 1) and oscillators (OSC1 and OSC2) of Tanzawa et al. for the purpose of increasing pump efficiency of the charge pump circuit of Javanifard et al. One would have been motivated to replace the generic charge pump (220) and oscillators (241 and 242) of Javanifard et al. with the specific charge pump (pump of Fig. 1) and oscillators (OSC1 and OSC2) of Tanzawa et al to increase pump efficiency and maintain steady state operation. Thus the above combination discloses all of the recited limitations of claim 7.

With respect to claims 8 and 14, the above combination discloses, "the charge pump circuit of claim 7 where the charge pump block includes:

at least one charge pump part;

a charge supply part (N11) to precharge the at least one charge pump part with the selected voltage (N11 supplies one the selected to voltages of Vpp or Vcc as modified above to the charge pump of C11, C12, N12, and N13, to precharge node Cn1 to one of the selected voltages); and

a charge trapping part to store charges provided by the charge supply part (N13 "traps" the charge at node CN2 until the voltage at CN2 becomes larger than the threshold voltage of N13, and then the voltage at CN2 will be output)."

With respect to claims 9 and 15, the above combination discloses, "the charge pump circuit of claim 8 where the at least one charge pump part pumps a charge to another charge pump part (the charge pump connected at CN1 pumps charge into CN2, where N13 and C12 also function as a charge pump)."

With respect to claims 10 and 16, the above combination discloses, "the charge pump circuit of claim 8 where the charge supply part comprises a high-voltage PMOS transistor (N11 is a high voltage PMOS transistor)."

With respect to claim 13, the above combination discloses of Javanifard et al. and Tanzawa et al, "a charge pump circuit comprising:

a charge pump block including at least one charge pump part (220 of Fig. 2 of Javanifard et al.)

a voltage level sensing block (OP1, R11 and R12 of Fig. 1 of Tanzawa eat al.) to sense a level of an output voltage (OUT (output of charge pump 220 as modified above) and generate a level sensing signal responsive thereto (the output of OP1 is responsive to the OUT signal);

an oscillator to generate a pulse signal responsive to the level sensing signal (OSC1 Outputs a signal in response to OP1);

a detector to generate a detection signal responsive to a high voltage (230 and 231 of Javanifard et al.);

a selector circuit (290 and the switches connected to Vpp, Vcc, and 220) to supply the one of the supply voltage or the high voltage responsive to the detect signal

(clearly 290 is controlled by the detect signals and controls the switches to selected one of Vcc and Vpp to be supplied to 220)."

Claims 11, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Javanifard et al. (USPN 5,781,473) in view of Tanzawa et al. (USPN 6,429,725)). Javanifard et al. and Tanzawa et al. teach the circuits as recited in claims 8 and 14 see above rejections. Tanzawa et al. fails to disclose is a charge pump with NMOS transistors. However, it is notoriously well-know in the art that the charge pump transistors of Tanzawa et al. are actually diode-connected transistors (connecting the gate of the transistors to the drain of the transistor). It is also notoriously well-know that both PMOS and NMOS transistors function the same when connected as diodes, and that it would make no difference if the PMOS transistors of the charge pumps of Tanzawa et al. where replace by NMOS transistors (For example, Rao (USPN 6,177,830) discloses a charge pump composed of diode connected NMOS transistors).

It would have been *prima facie* obvious to one of ordinary skill in the art at the time the invention was made to replace the PMOS transistors, with NMOS transistors, due to the doctrine of equivalents.

With respect to claims 11 and 17, the above combination discloses, "the charge pump circuit of claim 7 where the at least one charge pump part includes a high-voltage NMOS transistor (N12 and N13 are both NMOS transistors as modified above)."

With respect to claims 14-17, all of the claim limitations have been considered and it can be seen that claims 14-17 essentially recite the same limitations as claims 8-11. Thus claims 14-17 are rejected for at least the same reasons as claims 8-11.

Allowable Subject Matter

No allowable subject matter could be determined due to the deficiencies of claims 12 and 18.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

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TH
September 28, 2006

LINH MY NGUYEN
PRIMARY EXAMINER

Notice of References Cited	Application/Control No. 10/888,667	Applicant(s)/Patent Under Reexamination ZHANG ET AL.	
	Examiner Thomas J. Hiltunen	Art Unit 2816	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,781,473	07-1998	Javanifard et al.	365/185.18
*	B	US-2004/0125524	07-2004	Blyth, Trevor	361/100
*	C	US-6,654,290	11-2003	Lee et al.	365/185.23
*	D	US-5,889,701	03-1999	Kang et al.	365/185.18
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
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	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
10/888,667	ZHANG ET AL.	
Examiner	**Art Unit**	
Thomas J. Hiltunen	2816	

SEARCHED			
Class	Subclass	Date	Examiner
327	536,537 143,82,60, 63	11/9/2005	TH
363	60	11/9/2005	TH
Updated	above	4/6/2006	TH
Updated	above	9/27/2006	TH
363	63	9/28/2006	TH

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
See attached EAST text search	11/14/2005	TH
See attached EAST text search	4/10/2006	TH
See attached EAST text search	9/28/2006	TH

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	58845	charge with (pump$4 multipl$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 10:16
L2	412721	supply with voltage	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 10:16
L3	539423	high with voltage	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 10:17
L4	48468	test with mode	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 10:17
L5	6	1 with 2 with 3 with 4	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 10:20
L6	23	1 same 2 same 3 same 4	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 10:26
L7	1056	1 and 2 and 3 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 10:17
L8	949392	(pump$3 boost$3 output high$4) with voltage	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 10:21
L9	346974	mux multiplex?r select?r	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 10:21

EAST Search History

L10	3794208	sens$4 detect$4	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 10:22
L11	225113	10 with 8	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 10:56
L12	4521718	(select$4 choos$4 pick$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 10:25
L13	19577	12 with (2 and 8)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 10:25
L17	8182	11 and 13	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 10:57
L18	1296	17 and 1	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 10:57
L19	599	18 and 9	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 10:57
L21	455	18 not 19	USPAT	OR	ON	2006/09/28 12:55
L27	93436	program$4 and eras$4	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 12:52
L28	4510	1 and 27	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 12:53

EAST Search History

L29	101494	9 same 10	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 12:53
L30	598	28 and 29	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 12:54
L31	467	30 not 18	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 14:41
L32	455	18 not 19	USPAT	OR	ON	2006/09/28 12:55
L33	1	"5781473".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/09/28 14:41

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Pyung-Moon ZHANG and Seung-Keun LEE		
Serial No.:	10/888,667	Examiner:	Hiltunen, Thomas J.
Filed:	July 8, 2004	Group Art Unit:	2816
Confirmation No.:	4240		
For:	CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE		

Date: July 21, 2006

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Responsive to the office action, paper no. 20060406, dated April 24, 2006, please amend the application as follows.

Claims amendments begin on page 2.

Remarks begin on page 5.

CLAIMS

Amend the claims as follows.

1. (Currently amended) A charge pump circuit comprising:

a charge pump block including at least one charge pump part; and

a voltage supply circuit to supply one of a supply voltage or a high voltage ~~a variable pre-charge voltage~~ to the at least one charge pump part responsive to ~~a mode~~ detecting a level of the high voltage, where the high voltage is higher than the supply voltage.

2. (Currently amended) The charge pump circuit of claim 1 where the voltage supply circuit ~~pre-charge voltage is a~~ is adapted to supply the supply voltage in a general mode.

3. (Currently amended) The charge pump circuit of claim 1 where the voltage supply circuit ~~pre-charge voltage is a~~ is adapted to supply the high voltage ~~higher than the supply voltage~~ in a test mode.

4. (Currently amended) The charge pump circuit of claim 1 where the voltage supply circuit comprises:

a detector circuit to generate a detect signal responsive to [[a]]the high voltage; and

a selector circuit to supply the ~~pre-charge~~ one of the supply voltage or the high voltage responsive to the detect signal.

5. (Currently amended) The charge pump circuit of claim 1

where the charge pump block is adapted to generate an output voltage; and

where the voltage supply circuit comprises:

a voltage level sensing block to generate a level sensing signal responsive to a pump enable signal and the output voltage; and

an oscillator to generate complementary pulse signals responsive to the level sensing signal.

6. (Cancelled)

7. (Currently amended) A charge pump circuit comprising:

~~at least one~~ a charge pump ~~part~~ block to generate an output voltage;

a voltage level sensing block to generate a level sensing signal by sensing an output voltage;

an oscillator to generate complementary pulse signals responsive to the level sensing signal; and

a selecting circuit block to generate a selected voltage that is one of a high voltage and a supply voltage and to supply the selected voltage to the charge pump block ~~at least one charge pump part~~ responsive to detecting a level of the high voltage, the high voltage having a level higher than the supply voltage.

8. (Currently amended) The charge pump circuit of claim 7 ~~comprising~~ where the charge pump block includes:

at least one charge pump part;

a charge supply part to precharge the at least one charge pump part with the selected voltage; and

a charge trapping part to store charges provided by the charge supply part.

9. (Original) The charge pump circuit of claim 8 where the at least one charge pump part pumps a charge to another charge pump part.

10. (Original) The charge pump circuit of claim 8 where the charge supply part comprises a high-voltage PMOS transistor.

11. (Currently amended) The charge pump circuit of claim [[7]]8 where the at least one charge pump part includes a high-voltage NMOS transistor.

12. (Currently amended) The charge pump circuit of claim 7

where the selecting circuit block is adapted to compares the supply voltage with the high voltage; and

where the selecting circuit block is adapted to selects the high voltage if a level of the high voltage is higher than a level of the power voltage.

13. (Currently amended) A charge pump circuit comprising:

a charge pump block including at least one charge pump part;

a voltage level sensing block to sense a level of an output voltage and generate a level sensing signal responsive thereto;

an oscillator to generate a pulse signal responsive to the level sensing signal;

a detector to generate a detection signal responsive to a high voltage; and

a selector to provide one of the high voltage and ~~the~~ a power voltage responsive to the detection signal to the charge pump block.

14. (Original) The charge pump circuit of claim 13 where the charge pump block comprises:

a charge supply part to precharge the at least one charge pump part; and

a charge trapping part to store charges pumped from the at least one charge pump part.

15. (Original) The charge pump circuit of claim 14 where the at least one charge pump part pumps charge to another serially connected charge pump part.

16. (Original) The charge pump circuit of claim 14 where the charge supply part includes a high-voltage PMOS transistor.

17. (Original) The charge pump circuit of claim 14 where the charge pump block includes a high-voltage NMOS transistor.

18. (Original) The charge pump circuit of claim 13 where the selector compares the high voltage to the power voltage.

REMARKS

The application includes claims 1-18 prior to entering this amendment.

The examiner rejects claims 7-14 [sic] under 35 U.S.C. § 112 second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that the applicants regard as their invention. The examiner rejects 13-18 under 35 U.S.C. § 112 second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that applicants regard as the invention.

The examiner indicates claims 7-18 allowable if amended to overcome the § 112 rejections.

The examiner rejects claims 1-6 under 35 U.S.C. 102(b) as being anticipated by Tanzawa, et al. (U.S. Patent 6,429,725).

The applicants amend claims 1-5, 7-8, and 11-13, and cancel claim 6, without prejudice.

The application remains with claims 1-5 and 7-18 after entering this amendment.

The applicants add no new matter and request reconsideration.

Claim Rejections Under § 112

The applicants amend claims 1-5, 7-8 and 11-13 to overcome the § 112 rejections, correct typographical errors, and generally clarify the claims.

Claims Allowable

The applicants thank Examiner Hiltunen for indicating allowable claims 7-18 if amended to overcome the § 112 rejections.

The applicants amend claim 7 to provide better connection and/or cooperation between the elements and limitations.

The applicants amend claim 13 to provide antecedent basis for the power voltage.

Claims 7-18 are in condition for the examiner's allowance.

The applicants amend claim 1 to include *a voltage supply circuit to supply one of a supply voltage or a high voltage to the at least one charge pump part responsive to detecting a level of the high voltage, where the high voltage is higher than the supply voltage*. The examiner

indicates that the cited prior art fails to disclose such a circuit. As such, claims 1-5 are also in condition for the examiner's allowance.

Claim Rejections Under § 102

The applicants amend claims 1-5 and cancel claim 6. The applicants' claim amendments obviate the examiner's § 102 rejections as the applicants indicate in more detail above.

Conclusion

The applicants request reconsideration and allowance of all remaining claims. The applicants encourage the examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Graciela G. Cowger
Reg. No. 42,444

MARGER JOHNSON & McCOLLOM, P.C.
210 SW Morrison Street, Suite 400
Portland, OR 97204
503-222-3613

Customer No. 20575

Electronic Acknowledgement Receipt

EFS ID:	1123588
Application Number:	10888667
Confirmation Number:	4240
Title of Invention:	Charge pump circuit operating responsive to a mode
First Named Inventor:	Pyung-Moon Zhang
Customer Number:	20575
Filer:	Alexander Charles Johnson/Li mei Vermilya
Filer Authorized By:	Alexander Charles Johnson
Attorney Docket Number:	4591-380
Receipt Date:	21-JUL-2006
Filing Date:	08-JUL-2004
Time Stamp:	19:06:12
Application Type:	Utility
International Application Number:	

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part	Pages
1		4591380b.pdf	385015	yes	7

	Multipart Description		
	Doc Desc	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Amendment - After Non-Final Rejection	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	7
Warnings:			
Information:			
	Total Files Size (in bytes):	385015	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

MISCELLANEOUS LETTER

REGARDING PAYMENT OF FEES AND EXTENSION OF TIME

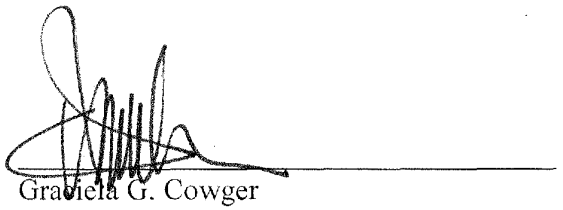
☒ Applicant petitions the Commissioner to extend the time for response (if applicable).

☒ Applicant requests that any deficiency or overpayment be charged or credited to deposit account number 13-1703.

Respectfully submitted,

Customer No. 20575

MARGER JOHNSON & McCOLLOM, P.C.



Date: July 21, 2006

Graciela G. Cowger
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PTO/SB/06 (12-04)
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PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Application or Docket Number

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE							770
SEARCH FEE (37 CFR 1.16(k), (i), or (m))							
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							
TOTAL CLAIMS (37 CFR 1.16(i))	18 minus 20 =	*	X	=	OR	X 18	=
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*	X	=		X 86	=
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))						290	770
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT A — 7/21/06

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 17	Minus	** 20	=	X =		OR	X 50 =	0
Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	=	X =		OR	X 200 =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR	310	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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CHANGE OF CORRESPONDENCE ADDRESS
Application

Address to:
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P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	10888667
Filing Date	2004-07-08
First Named Inventor	Pyung-Moon ZHANG
Art Unit	2816
Examiner Name	HILTUNEN, Thomas
Attorney Docket Number	4591-380

Please change the Correspondence Address for the above-identified patent application to:

☑ The address associated with Customer Number: 20575

OR

☐ Firm or Individual Name

Address

City	State	Zip

Country

Telephone	Email

This form cannot be used to change the data associated with a Customer Number. To change the data associated with an existing Customer Number use "Request for Customer Number Data Change" (PTO/SB/124).

I am the:

☐ Applicant/Inventor

☐ Assignee of record of the entire interest.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☑ Attorney or agent of record. Registration Number 29,396.

☐ Registered practitioner named in the application transmittal letter in an application without an executed oath or declaration. See 37 CFR 1.33(a)(1). Registration Number_____.

Signature

Typed or Printed Name Alexander C. Johnson, Jr.

Date 2006-06-21	Telephone 503-222-3613

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	1086614
Application Number:	10888667
Confirmation Number:	4240
Title of Invention:	Charge pump circuit operating responsive to a mode
First Named Inventor:	Pyung-Moon Zhang
Correspondence Address:	Alan T. McCollom MARGER JOHNSON & McCOLLOM, P.C. 1030 S.W. Morrison Street - Portland OR 97205 US 5032223613 -
Filer:	Ariel Shai Rogson/Christina Lawton
Filer Authorized By:	Ariel Shai Rogson
Attorney Docket Number:	4591-380
Receipt Date:	21-JUN-2006
Filing Date:	08-JUL-2004
Time Stamp:	14:12:30
Application Type:	Utility
International Application Number:	

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part	Pages
1	Change of Address	COA.pdf	108880	no	1
Warnings:					
Information:					
		Total Files Size (in bytes):	108880		

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National Stage of an International Application under 35 U.S.C. 371
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/888,667	07/08/2004	Pyung-Moon Zhang	4591-380	4240

7590 04/24/2006

Alan T. McCollom
MARGER JOHNSON & McCOLLOM, P.C.
1030 S.W. Morrison Street
Portland, OR 97205

EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

AD

Office Action Summary	Application No.	Applicant(s)	
	10/888,667	ZHANG ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/08/04* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Summary of changes in this action

1. The objection to the drawings has been overcome by Applicant's amendment.
2. The rejection of claims 6, 8-10, and 14-17 under 35 USC 112, second paragraph has been overcome by the Applicant's remarks.
3. New rejection to claims 7-14 under 35 U.S.C. § 112, second paragraph, are provided below.
4. New rejections to claims 1-6 under Tanazawa et al. (USPN 6,429,725) are provided below.
5. Claims 7-12 have been amended to include allowable subject matter.
6. The rejections of claims 1, 4, and 7-18 under 35 USC 103 as obvious under Tanazawa et al. (USPN 6,429,725) in view of in view of Arakawa (USPN 5,099,143) have been overcome by applicant's amendment and remarks.

Claim Rejections - 35 USC § 112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 7-14 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 7 there is no connection or cooperation provided between the claimed circuit elements. For example the voltage level sensing block sense an output, however it unclear how the output is produced. The only circuit elements that have connections and cooperation are the connection between the oscillator and the voltage sensing block. It is suggested that the connection and cooperation between all of the recited circuit elements be clearly defined.

Claim 13-18 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 13, there is no antecedent basis for "the power voltage" on line 7. It is suggested that claim 13 be amended to provide antecedent basis for "the power voltage". Claims 14-18 are rejected as to not adding any further clarification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, are rejected under 35 U.S.C. 102(b) as being anticipated by Tanazawa et al. (USPN 6,429,725).

With respect to claim 1, Tanazawa et al. discloses in Fig. 12, "a charge pump circuit comprising:

a charge pump block including at least one charge pump part (In Col. 13 lines 17-20, and lines 31-34 disclose that the booster sections are the same of that of Fig.1, and in Col. 13 lines 35-39 disclose that the only difference between the booster of Fig. 1 and Fig. 12 is that the detector resistors of the standby and active boosters are the same. N12 coupled with C11 is a charge pump block, in that it boosts the voltage provided by N11); and

a voltage supply circuit to supply a variable pre-charge voltage to the at least one charge pump part responsive to a mode (Terminals 12 supply a voltage (one of Vcc or Vp) to transistors N16, supply a variable pre-charge at node CN1 and N12, the pre-charge supplied by N16 is variable, because Vcc or Vp is supplied to N12 with respect to RSTPMP signal the higher RSTPMP is the more pre-charge will be supplied to CN1 and N12, additionally N16 is variable by being enabled and disabled, with respect to RSTPMP, and the ACT signal. As can be seen in Fig. 13, that the active charge pump is responsive to an active mode, when active mode signal ACT is in the ACTIVE region VppA will be output by the active booster of Fig. 1)."

With respect to claim 2, Tanazawa et al., discloses, "the charge pump circuit of claim 1 where the pre-charge voltage is a supply voltage in a general mode (When Vcc is chosen to be the supply voltage at 12, and the ACT signal enabled is the general

mode, then a supply voltage Vcc (Vcc is equal to the supply voltage of Vcc applied to node 11 and 14) well be supplied to the charge pump)."

With respect to claim 3, Tanazawa et al., discloses, "the charge pump circuit of claim 1 where the pre-charge voltage is a voltage higher than the supply voltage in a test mode (When ACT is activated the pre-charge is a voltage higher than Vcc, when Vp the chosen supply voltage at 12, Vp is higher than supply voltage Vcc (see Col. 7 lines 22-25), which is supplied in the ACTIVE region of Fig. 13. When the ACT is enabled is the test mode)."

With respect to claim 4, the above combination discloses, "the charge pump circuit of claim 1 where the voltage supply circuit comprises:

a detector circuit to generate a detect signal responsive to a high voltage (LD1 is a detector circuit which detects the level responsive to a high voltage Vpp (OUT), and generates a detect signal at is output); and

a selector circuit to supply the pre-charge voltage responsive to the detect signal (a signal responsive to the output of OP1 (RSTPMP, which is responsive to RST, which is responsive to the output to OP1) is input to N16, which selects the voltage at node 12 and outputs the pre-charge signal to N12 and CN1)."

With respect to claim 5, Tanazawa et al., discloses, "the charge pump circuit of claim 1 where the voltage supply circuit comprises:

a voltage level sensing block to generate a level sensing signal responsive to a pump enable signal (Op1 is a voltage detection circuit responsive to the ACT (enables

active charge pump see Fig 13) signal, which is connected to N14 of the resistive divider (R11 and R12) connected to OP1); and

an oscillator to generate complementary pulse signals responsive to the level sensing signal (OSC1 receives an output from OP1 at ND1. Which, outputs complementary signals to C11 and C12 at the outputs of 112 and 114)."

With respect to claim 6, Tanazawa et al., discloses, "a charge pump block including at least one charge pump part (In Col. 13 lines 17-20, and lines 31-34 disclose that the booster sections are the same of that of Fig.1, and in Col. 13 lines 35-39 disclose that the only difference between the booster of Fig. 1 and Fig. 12 is that the detector resistors of the standby and active boosters are the same. N12 coupled with C11 is a charge pump block); and

a voltage supply circuit to supply a variable pre-charge voltage to the at least one charge pump part responsive to a mode (Terminals 12 supply a voltage (one of Vcc or Vp) to transistors N16, supply a variable pre-charge at node CN1 and N12, the pre-charge supplied by N16 is variable, because Vcc or Vp is supplied to N12 with respect to RSTPMP signal the higher RSTPMP is the more pre-charge will be supplied to CN1 and N12, additionally N16 is variable by being enabled and disabled, with respect to RSTPMP, and the ACT signal. As can be seen in Fig. 13, that the active charge pump is responsive to an active mode, when active mode signal ACT is in the ACTIVE region VppA will be output by the active booster of Fig. 1);

where the voltage supply circuit comprises a charge trapping pad to generate an output voltage (N13 'traps" the charge at node CN2 until the voltage at CN2 becomes larger than the threshold voltage of N13, and then the voltage at CN2 will be output."

Allowable Subject Matter

Claims 7-18 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

With respect to claim 7, there is no cited prior art that discloses a selecting block, for selecting one of a high voltage and a supply voltage to a charge pump, where the selected voltage is responsive to detecting a level of the high voltage. The supplying a charge pump with a selected voltage that is responsive to a detected level of the high voltage is what distinguishes claim 7 over the prior art. Thus, claim 7 is allowable and claims 8-12 are allowable for at least the same reasons as claim 7.

With respect to claim 13, there is no cited prior art that discloses a selecting circuit that selects a supply voltage, or a high voltage responsive detecting the level of the high voltage, in which the high voltage is higher than the supply voltage. In a charge pump circuit as recited. The detection circuit that outputs a detection circuit responsive to a high voltage signal, wherein the selection circuit that outputs a supply voltage or a high voltage in response to the detection signal distinguishes claim 13 over the prior art, as is evidenced below. Thus claim 13 is allowable and claims 14-18 are allowable for at least the same reasons.

Tanzawa et al. discloses most the recitation of claim 13, however Tanzawa et al. does not disclose a selecting circuit that selects a supply voltage, or a high voltage responsive detecting the level of the high voltage, in which the high voltage is higher than the supply voltage. Tanzawa, only discloses selecting only one voltage supply signal at terminal 13. Thus Tanzawa does not read over claim 7 or 13.

Zanuccoli et al. (USPN 6,448,842), discloses in Fig. 1, a charge pump (stage 1) that is supplied a high (Vcc, which is higher than ground) or a supply voltage (ground), Zanuccoli et al. also discloses a sensing circuit (4), which outputs a control signal to an oscillator (3). However, Zanuccoli et al. discloses the selector (switch that selects between Vcc and ground) is controlled by control signal K. Zanuccoli et al. does not supply any support or motivation for considering K to be a "detection" signal, nor doe Zanuccoli et al. disclose a "detector" circuit. Also Zanuccoli et al. fails to teach K being a responsive to a high voltage signal. Thus Zanuccoli does not read over claim 7 or 13.

Coffman et al. (USPN 5,335,200), discloses in Fig. 2, a pre-charge circuit (98), a charge pump (82), and a dual supply voltage outputting selection/detection circuit. The inverter 96 outputs Vpp and Vss to the source of 98, with respect to the detection signal at 81 (81 detects a power off condition). However Coffman et al. fails to disclose the signal at 81, being dependent upon the high voltage (which is Vpp). Additionally, Coffman et al. fails to disclose the output level sensing circuit controlling the oscillator. Thus Coffman et al. does not read over claim 7 or 13.

Jang et al. (USPN 6,876,247), discloses a level detector that outputs a signal to a charge pump (through the oscillator circuits) based on a comparison between a supply

voltage (Vcore 1, Vcore 2), and a high voltage Vpp. However, Jang et al. does not provide additional circuit element capable of being interpreted as a level sensing unit that controls the oscillator, if element 10 is considered to be the detector/selector. Also, it should be noted that Jang et al. does not have a filing date that is older than Applicant's foreign priority date. Thus Jang et al. does not read over claim 7 or 13.

Narui et al. (USPN 6,954,386), discloses an output sensing circuit 23, controlling an oscillator, and a pre-charge circuit MP1. However, is only capable of supplying a single voltage. Thus Narui et al. dose not read over claim 7 or 13.

Cha et al. (USPN 6,522,191), discloses a control pre-charge circuit 30, however the pre-charge circuit cannot select more than one voltage. Thus Cha et al. does not read over claim 7 or 13.

Walimbe et al. (USPN 6,552,600), discloses in Fig. 2, a selecting circuit 24, that selects between a supply voltage (Pump Output is a supply voltage for the circuit receiving Pump Output), a higher voltage (GND is a higher voltage level than Pump Output) an output sensing circuit (21), which controls an oscillator (VCO with Clock Drivers) the oscillator outputs complementary clocks to multiple charge pumps (26a to 26n). However, the multiplexer 24 is not controlled by a detection voltage responsive to the high signal. Even if Walimbe et al.'s circuit was modified to a positive charge pump, Walimbe et al. would still fail to teach the required recitation of the selection circuit being responsive the detection signal, which is responsive to the high voltage. Thus Walimbe et al. does not read over claim 7 or 13.

Response to Arguments

With respect to claims 1-4 rejected under 35 USC 102 over Tanzawa, the examiner has changed the grounds of the rejection to more clearly define the rejection. Also claims 4-6 have been newly rejected under Tanzawa. The examiner disagrees with applicant that the amendment to claim 1 to include a "variable pre-charge" puts claim 1 in condition for allowance. Additionally, the active booster of Tanzawa is responsive to an active mode (activation of the ACT signal, see Fig 13). As can be seen above Tanzawa provides a variable pre-charge in at least two ways. First the pr-charge is variable because the pre-charge is either enabled (when ACTIVE signal is high, see Fig. 13), or disabled (when ACTIVE signal is low, see Fig. 13). Secondly, when the RSTPMP signal transitions it state the control voltage at the gate of N16 will transition also, thus causing N-16 to output a pre-charge that will also transition in time, thus varying from a lower to a higher voltage.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-

872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Terry D. Cunningham
Primary Examiner
Art Unit 2816

TH
April 17, 2006

Notice of References Cited	Application/Control No. 10/888,667	Applicant(s)/Patent Under Reexamination ZHANG ET AL.	
	Examiner Thomas J. Hiltunen	Art Unit 2816	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,954,386	10-2005	Narui et al.	365/189.11
*	B	US-6,876,247	04-2005	Jang et al.	327/536
*	C	US-6,552,600	04-2003	Walimbe et al.	327/536
*	D	US-6,522,191	02-2003	Cha et al.	327/536
*	E	US-6,448,842	09-2002	Zanuccoli et al.	327/536
*	F	US-5,335,200	08-1994	Coffman et al.	327/536
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination
	10/888,667	ZHANG ET AL.
	Examiner	Art Unit
	Thomas J. Hiltunen	2816

SEARCHED			
Class	Subclass	Date	Examiner
327	536,537 143,82,60, 63	11/9/2005	TH
363	60	11/9/2005	TH
Updated	above	4/6/2006	TH

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
See attached EAST text search	11/14/2005	TH
See attached EAST text search	4/10/2006	TH

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	17480	charge adj (pump$3 boost$3)	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 08:27
L2	422520	power adj supply	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 08:28
L3	140306	supply adj voltage	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 08:29
L4	207783	high adj voltage	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 08:29
L5	307284	comparator multiplex?r differential adj amplifier	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 08:29
L6	5842197	(vari$4 adjust$4 control$4 select$4)	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 08:30
L7	597643	2 3 4	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 08:31
L8	224591	6 with 7	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 08:31
L9	606208	7 (pre-charge precharge)	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 08:32
L10	224591	6 with 8	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 08:33
L11	7005	10 and 1	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 08:34
L12	3628	11 and 5	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 08:34
L13	3241	11 and (oscillator)	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 08:34
L14	2221447	13 (sens$3 detect$4)	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 08:35
L15	2837	13 and (sens$3 detect$4)	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 08:35

EAST Search History

L16	1945	15 and 5	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 08:36
L17	1881	16 and charge adj pump	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 09:12
S50	3	(variable adjustable) with (pre-charge precharge) and 327/536,537.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/06 14:02
S51	287	(pre-charge precharge) and 327/536, 537.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/06 14:02
S52	3	(variable adjustable) with (pre-charge precharge) and 327/535,536,537.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/06 14:02
S53	306	(pre-charge precharge) and 327/535, 536,537.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/06 14:05
S54	372	(pre-charg$3 precharg$4) and 327/535,536,537.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/06 14:06
S55	3	(variable adjustable controllable) with (pre-charg$3 precharg$4) and 327/535,536,537.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/06 14:06
S56	573	(variable adjustable controllable) with (pre-charg$3 precharg$4) "."	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/06 14:06
S57	573	(variable adjustable controllable) with (pre-charg$3 precharg$4)	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 08:29

EAST Search History

S60	78	(US-20040000945-$ or US-20040056707-$ or US-20040061549-$ or US-20040080359-$ or US-20010001230-$ or US-20030056165-$ or US-20050047181-$ or US-20050062520-$ or US-20050093615-$ or US-20050110560-$ or US-20020024380-$).did. or (US-4539490-$ or US-4916334-$ or US-4565932-$ or US-4670668-$ or US-4767950-$ or US-5138190-$ or US-5335200-$ or US-5099143-$ or US-5841725-$ or US-5627739-$ or US-5708387-$ or US-5717581-$ or US-5767735-$ or US-5801577-$ or US-6163487-$ or US-6052022-$ or US-6100748-$ or US-6242970-$ or US-6268761-$ or US-6288601-$ or US-6107862-$ or US-6177829-$ or US-6177830-$ or US-6198340-$ or US-6205079-$ or US-6294948-$).did. or (US-6300820-$ or US-6356501-$ or US-6373325-$ or US-6373327-$ or US-6404272-$ or US-6466079-$ or US-6483282-$ or US-6414881-$ or US-6448842-$ or US-6483378-$ or US-6486729-$ or US-6483377-$ or US-6492861-$ or US-6522191-$ or US-6522558-$ or US-6492862-$ or US-6501326-$ or US-6504422-$ or US-6515903-$ or US-6552600-$ or US-6518828-$ or US-6525972-$ or US-6693480-$ or US-6724240-$ or US-6734717-$ or US-6756837-$ or US-6531902-$).did. or (US-6538494-$ or US-6538930-$ or US-6556064-$ or US-6693479-$ or US-6762639-$ or US-6765428-$ or US-6774707-$ or US-6774708-$ or US-6798275-$ or US-6781439-$ or US-6876247-$ or US-5034625-$ or US-4961007-$ or US-6079037-$).did.	US-PGPUB; USPAT	OR	ON	2006/04/06 15:04
S81	12	("5029282" | "5553030" | "5717581" | "5920225" | "6067336" | "6107862" | "6111470" | "6181210" | "6320435" | "6385265" | "6690146").PN. OR ("6897709").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/07 11:19
S87	17480	charge adj (pump$3 boost$3)	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/07 13:54

EAST Search History

S88	140306	supply adj voltage	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 08:28
S89	307284	comparator multiplex?r differential adj amplifier	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/10 08:29
S90	7973	S88 with S89	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/07 13:56
S91	701	S90 and S87	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/07 14:15

EAST Search History

S98	96	(US-20050093615-$ or US-20010001230-$ or US-20020024380-$ or US-20050110560-$ or US-20050047181-$ or US-20040080359-$ or US-20040000945-$ or US-20030056165-$ or US-20050062520-$ or US-20040056707-$ or US-20040061549-$ or US-20020057124-$ or US-20020008568-$ or US-20020008567-$ or US-20010010477-$).did. or (US-6522191-$ or US-6700434-$ or US-6492862-$ or US-6400216-$ or US-6876247-$ or US-6107862-$ or US-6756837-$ or US-6052022-$ or US-5034625-$ or US-4961007-$ or US-6774708-$ or US-5506540-$ or US-6765428-$ or US-6356501-$ or US-6798275-$ or US-6954386-$ or US-6448842-$ or US-6515903-$ or US-6483378-$ or US-6294948-$ or US-6288601-$ or US-6268761-$ or US-6205079-$ or US-5841725-$ or US-5801577-$ or US-5708387-$).did. or (US-5701096-$ or US-6079037-$ or US-6774707-$ or US-6762639-$ or US-6734717-$ or US-6724240-$ or US-6693480-$ or US-6693479-$ or US-6552600-$ or US-6538930-$ or US-6538494-$ or US-6781439-$ or US-6504422-$ or US-6501326-$ or US-6486729-$ or US-6483377-$ or US-6414881-$ or US-6404272-$ or US-6373325-$ or US-6300820-$ or US-6177830-$ or US-6163487-$ or US-6100748-$ or US-5767735-$ or US-5627739-$ or US-6556064-$ or US-6531902-$).did. or (US-6525972-$ or US-6522558-$ or US-6518828-$ or US-6483282-$ or US-6492861-$ or US-6466079-$ or US-6373327-$ or US-5335200-$ or US-5099143-$ or US-4767950-$ or US-4670668-$ or US-4565932-$ or US-6242970-$ or US-6198340-$ or US-6177829-$ or US-5717581-$ or US-5138190-$ or US-4539490-$ or US-4916334-$ or US-5912560-$ or US-6147914-$ or US-6128242-$ or US-6847250-$ or US-6329869-$ or US-6297687-$ or US-5933047-$ or US-4904885-$).did. or (US-6154411-$).did.	US-PGPUB; USPAT	OR	ON	2006/04/07 15:20

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Certificate of Facsimile Transmission

I hereby certify that the attached Transmittal (1 page) and Response to the Office Action dated November 16, 2005 (9 pages), TWO replacement sheets drawings, TWO annotated sheets drawings are submitted to the U.S. Patent and Trademark Office via facsimile number (571) 273-8300 on the date shown below. (Total 14 pages).

Li Mei Vermilya

Date: February 14, 2006

PATENT APPLICATION
Docket No.: 4591-380
Client Ref. No.: ID13095-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Pyung-Moon ZHANG and Seung-Keun LEE		
Serial No.:	10/888,667	Examiner:	Hiltunen, Thomas J.
Filed:	July 8, 2004	Group Art Unit:	2816
Confirmation No.:	4240		
For:	CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Responsive to the Office Action dated November 16, 2005, enclosed is an amendment in the above-identified application.

The fee has been calculated as shown below.

CLAIMS AS AMENDED					
For:	Number After Amendment	Previous Number	Extra	Rate	Additional Fee
Total Claims	18	18	0	x $50 =	$0
Independent Claims	4	3	1	x $200 =	$200
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT					$200

*greater of twenty (20) or number for which fee has been paid
**greater of three (3) or number for which fee has been paid

☒ TWO replacement sheets drawings (comprises Figs. 1-3).
☒ TWO Annotated sheets drawings (comprises Figs. 1-3).
☒ Any deficiency or overpayment should be charged or credited to deposit account number 13-1703.

Customer No. 20575

Respectfully submitted,
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PAGE 1/14 * RCVD AT 2/14/2006 11:44:28 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/26 * DNIS:2738300 * CSID:5032744622 * DURATION (mm-ss):04-42

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PATENT APPLICATION
Docket No.: 4591-380
Client Ref. No.: ID13095-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Filed:	July 8, 2004	Group Art Unit:	2816
Confirmation No.:	4240		
For:	CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Responsive to the Office Action dated November 16, 2005, please amend the application as follows.

Drawing amendments begin on page 2 and include replacement and annotated sheets.

Claims amendments begin on page 3.

Remarks begin on page 6.

02/16/2006 WABDELR1 00000048 131703 10888667
01 FC:1201 200.00 DA

PAGE 2/14 * RCVD AT 2/14/2006 11:44:28 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/26 * DNIS:2738300 * CSID:5032744622 * DURATION (mm-ss):04-42

CLAIMS

Amend the application as follows.

1. (Currently amended) A charge pump circuit comprising:

a charge pump block including at least one charge pump part; and

a voltage supply circuit to supply a variable pre-charge voltage to the at least one charge pump part responsive to a mode.

2. (Original) The charge pump circuit of claim 1 where the pre-charge voltage is a supply voltage in a general mode.

3. (Original) The charge pump circuit of claim 1 where the pre-charge voltage is a voltage higher than the supply voltage in a test mode.

4. (Original) The charge pump circuit of claim 1 where the voltage supply circuit comprises:

a detector circuit to generate a detect signal responsive to a high voltage; and

a selector circuit to supply the pre-charge voltage responsive to the detect signal.

5. (Original) The charge pump circuit of claim 1 where the voltage supply circuit comprises:

a voltage level sensing block to generate a level sensing signal responsive to a pump enable signal; and

an oscillator to generate complementary pulse signals responsive to the level sensing signal.

6. (Currently amended) A ~~The~~ charge pump circuit ~~of claim 1~~ comprising:

a charge pump block including at least one charge pump part; and

a voltage supply circuit to supply a pre-charge voltage to the at least one charge pump part responsive to a mode;

where the voltage supply circuit comprises a charge trapping part to generate an output voltage.

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7. (Currently amended) A charge pump circuit comprising:

at least one charge pump part;

a voltage level sensing block to generate a level sensing signal by sensing an output voltage;

an oscillator to generate complementary pulse signals responsive to the level sensing signal; and

a selecting circuit block to generate a selected voltage that is one of a high voltage and a supply voltage to the at least one charge pump part responsive to detecting a level of the high voltage, the high voltage having a level higher than the supply voltage.

8. (Original) The charge pump circuit of claim 7 comprising:

a charge supply part to precharge the at least one charge pump part with the selected voltage; and

a charge trapping part to store charges provided by the charge supply part.

9. (Original) The charge pump circuit of claim 8 where the at least one charge pump part pumps a charge to another charge pump part.

10. (Original) The charge pump circuit of claim 8 where the charge supply part comprises a high-voltage PMOS transistor.

11. (Original) The charge pump circuit of claim 7 where the at least one charge pump part includes a high-voltage NMOS transistor.

12. (Original) The charge pump circuit of claim 7

where the selecting circuit block compares the supply voltage with the high voltage; and

where the selecting circuit selects the high voltage if a level of the high voltage is higher than a level of the power voltage.

13. (Original) A charge pump circuit comprising:

a charge pump block including at least one charge pump part;

a voltage level sensing block to sense a level of an output voltage and generate a level sensing signal responsive thereto;

PAGE 5/14 * RCVD AT 2/14/2006 11:44:28 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/26 * DNIS:2738300 * CSID:5032744622 * DURATION (mm-ss):04-42

an oscillator to generate a pulse signal responsive to the level sensing signal;

a detector to generate a detection signal responsive to a high voltage; and

a selector to provide one of the high voltage and the power voltage responsive to the detection signal to the charge pump block.

14. (Original) The charge pump circuit of claim 13 where the charge pump block comprises:

a charge supply part to precharge the at least one charge pump part; and

a charge trapping part to store charges pumped from the at least one charge pump part.

15. (Original) The charge pump circuit of claim 14 where the at least one charge pump part pumps charge to another serially connected charge pump part.

16. (Original) The charge pump circuit of claim 14 where the charge supply part includes a high-voltage PMOS transistor.

17. (Original) The charge pump circuit of claim 14 where the charge pump block includes a high-voltage NMOS transistor.

18. (Original) The charge pump circuit of claim 13 where the selector compares the high voltage to the power voltage.

PAGE 6/14 * RCVD AT 2/14/2006 11:44:28 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/26 * DNIS:2738300 * CSID:5032744622 * DURATION (mm-ss):04-42

DRAWINGS

Replace Figures 1-3 with the enclosed red-lined Figures 1-3 (2 sheets).

PAGE 3/14 * RCVD AT 2/14/2006 11:44:28 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/26 * DNIS:2738300 * CSID:5032744622 * DURATION (mm-ss):04-42

REMARKS

The examiner objects to drawing Figures 1-3 under 37 C.F.R. § 1.121(d).

The application includes claims 1-18 prior to entering this amendment.

The examiner rejects claims 6, 8-10 and 14-17 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that the applicants regard as their invention. The examiner rejects claims 1-4 under 35 U.S.C. § 102(b) as being anticipated by Tanzawa, et al. (U.S. Patent 6,429,725). The examiner rejects claims 1, 4-5, 7, 11-13 and 18 under 35 U.S.C. § 103(a) as being unpatentable by Tanzawa in view of Arakawa (U.S. Patent 5,099,143). The examiner rejects claims 11 and 17 under 35 U.S.C. 103(a) as being unpatentable by Tanzawa in view of Arakawa.

The applicants amend claims 1, 6, and 7.

The application remains with claims 1-18 after entering this amendment.

The applicants add no new matter and request reconsideration.

Drawing Objections

The applicants amend Figures 1-3 to add the legend —PRIOR ART— as suggested by the examiner.

Claim Rejections Under § 112

The examiner rejects claims 6, 8-10 and 14-17 because the recitation of the term "charge trapping circuit" is unclear. The examiner alleges that Figure 5 shows the "charge trapping circuit" as merely a capacitive diode. The examiner does not understand how the diode actually traps charge.

The applicants remind the examiner that they are their own lexicographer, particularly to terms that are not necessarily well known in the art. The specification describes the charge trapping part 160 in various pages. At page 5, lines 26-28, for example, the specification describes an embodiment of the charge trapping part 160 as follows.

> "The charge trapping part 160 comprises one PMOS transistor P160 and one capacitor. The PMOS transistor P160 is used as charge transfer device, and the capacitor is used as charge trapping device. The charge trapping part 160 generates the output voltage Vout."

PAGE 7/14 * RCVD AT 2/14/2006 11:44:28 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/26 * DNIS:2738300 * CSID:5032744622 * DURATION (mm-ss):04-42

The applicants believe that the examiner is incorrect when he describes the charge trapping part as merely a capacitive diode. The capacitor described in the passage above stores or "traps" charge. Claims 6, 8-10 and 14-17 are thus definite and no amendment is necessary.

The applicants note that claim 6 is rejected only based on § 112. The applicants' clarification, as they express above, and their amendment of claim 6 as an independent claim should, therefore, place claim 6 in condition for the examiner's allowance.

Claim Rejections Under §102

The examiner rejects claims 1-4 as old over Tanzawa. The applicants disagree for the reasons that follow.

Although the examiner initially rejects claims 1-4 as old over Tanzawa, he goes on to reject claims 1 and 4 as obvious over Tanzawa in view of Arakawa. Explaining his obviousness rejection, the examiner acknowledges that Tanzawa does not teach a voltage supply circuit capable of selecting between a supply voltage and a voltage higher than the supply voltage. It would appear to the applicants that Tanzawa cannot, therefore, disclose a voltage supply circuit that supplies a pre-charge voltage responsive to a mode as claim 1 recites and we explain in more detail below.

Claim 1 recites *a voltage supply circuit to supply a variable pre-charge voltage to the at least one charge pump part responsive to a mode*. The examiner alleges Tanzawa discloses the recited voltage supply circuit with its terminals 12 and 13 that supply transistors N16 and N17 [sic] with a precharge voltage at node CN1. According to the examiner, the "level of the precharge depends on the level of the signal PGM (if PGM is high, Vcc will be output, if PGM is low VPP is output)." Office action, page 3. The applicants ask the examiner to clarify since it did not find the signal PGM disclosed anywhere in Tanzawa.

Tanzawa discloses that a "voltage Vp, which is higher than the power supply voltage Vcc, can be applied to the power supply terminals 12 and 13. The voltage Vp is obtained by boosting the power supply voltage Vcc by another booster circuit (not shown)." Column 7, lines 22-26. That is, terminals 12 and 13 may receive either a power supply voltage Vcc or, alternatively, a voltage Vp obtained by boosting the supply voltage Vcc. Tanzawa is silent on the conditions necessary for providing Vcc or Vp on the terminals 12 and 13. That is, Tanzawa does not disclose supplying a variable pre-charge voltage responsive to a *mode*. The examiner's allegations suggest that he is equating Tanzawa's output voltage at terminal OUT (either Vcc or Vpp) with the recited pre-charge voltage. The pre-charge voltage, as

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recited, is applied to *the at least one charge pump part*. The examiner has identified the charge pump part as being disclosed by Tanzawa's transistors N16 and 17. According to Figure 1, however, the voltage at the terminal OUT is not provided to the transistors N16 and N17, as is required by the claim.

Claim Rejections Under § 103

The examiner initially indicates his rejection of claims 1, 4-5, 7, 11-13 and 17-18 as obvious over Tanzawa in view of Arakawa. In the body of the rejection, however, the examiner appears to actually reject claims 1, 4-5 and 7-18. The applicants will assume the examiner meant to reject claims 1, 4-5 and 7-18 as is indicated in the body of the rejection, and not necessarily as indicated initially.

Claim 7 recites *a selecting circuit block to generate a selected voltage that is one of a high voltage and a supply voltage to the at least one charge pump part responsive to detecting a level of the high voltage....* Claim 13 recites *a selector to provide one of the high voltage and the power voltage responsive to the detection signal to the charge pump block.* The examiner acknowledges that Tanzawa does not disclose a voltage supply circuit capable of selecting between a supply voltage and a voltage higher than the supply voltage. The examiner points to Arakawa's Figure 14 for providing the missing link. But Arakawa's voltage supply circuit does not operate responsive to detecting whether a level of the high voltage (or a detection signal) as claim 7 (and claim 13) require, but rather appear to operate responsive to an externally applied signal /PGM.

The examiner alleges in all other claim rejections that Arakawa's externally provided program signal /PGM. For example, with regard to claim 12, the examiner alleges that "if PGM is low, and φ is input to the voltage supply circuit, and Vpp is higher Vcc, Vpp will output from Arakawa's Fig. 14." But claim 12 recites *where the selecting circuit selects the high voltage if a level of the high voltage is higher than a level of the power voltage.* In Arakawa, whether Vpp or Vcc is provided at its output node depends on the external program signal PGM and a boosting pulse φ ("And in a write mode, the charge pump receives a boosting pulse φ and produces an output voltage (about 15 volts in case Vpp is 12 volts) higher than the total voltage of Vpp+Vth (where Vth is the threshold voltage of transistor Qa). In any other operation mode than the write mode, the boosting pulse φ is not received so that the voltage is not multiplied." Column 17, lines 24-32.) . Neither the PGM signal nor the boosting pulse φ have any relation or correlation to detecting a level of the high voltage.

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That is, the embodiment of the selecting circuit recited in the claims operates relatively independently of any externally provided signal.

The applicants believe claims 1-18 are in condition for allowance.

Conclusion

The applicants request reconsideration and allowance of all remaining claims. The applicants encourage the examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Customer No. 20575

Respectfully submitted,

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I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (571) 273-8300 on February 14, 2006.

Li Mei Vermilya

PAGE 10/14 * RCVD AT 2/14/2006 11:44:28 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/26 * DNIS:2738300 * CSID:5032744622 * DURATION (mm-ss):04-42

Pyung-Moon ZHANG, et al.
CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE
Attorney Docket No. 4591-380/Application No. Not yet assigned
1/2
Annotated Sheet Showing Changes

Fig. 1
(PRIOR ART)

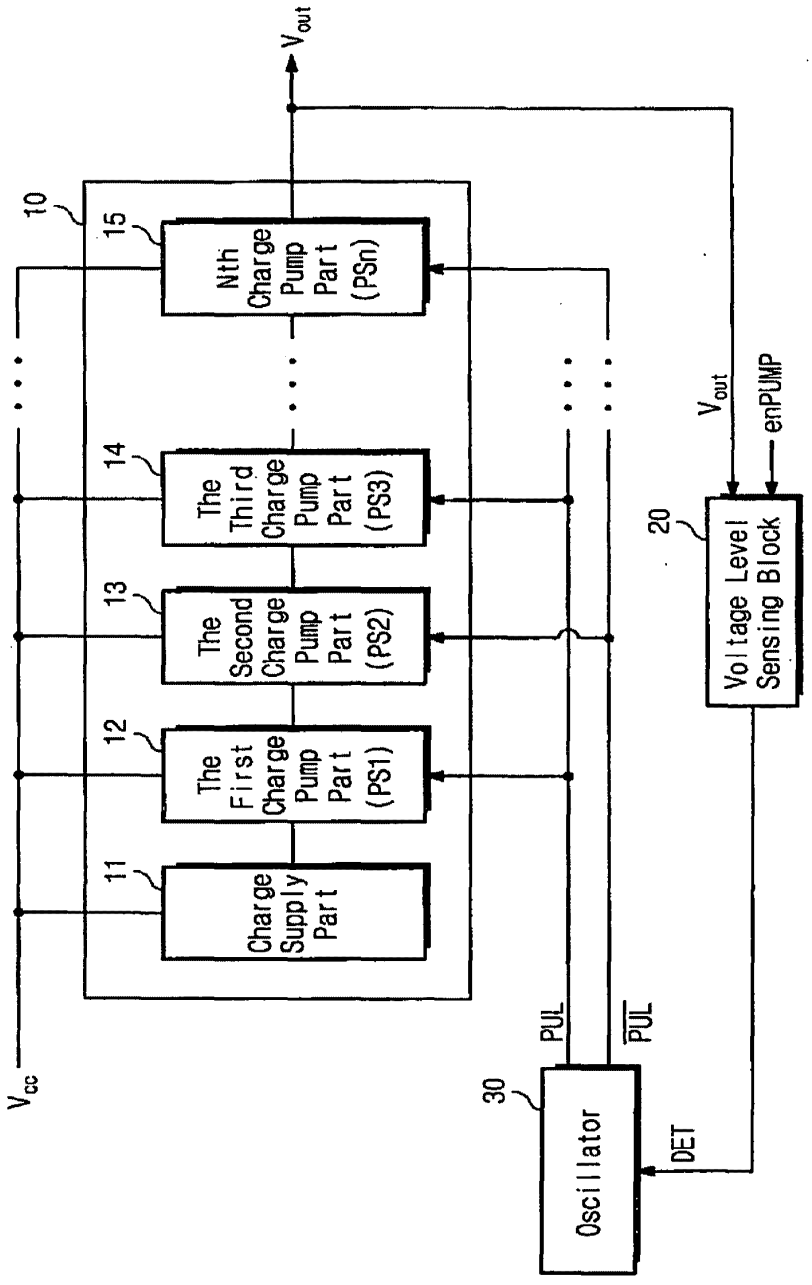


Fig. 2

(PRIOR ART)

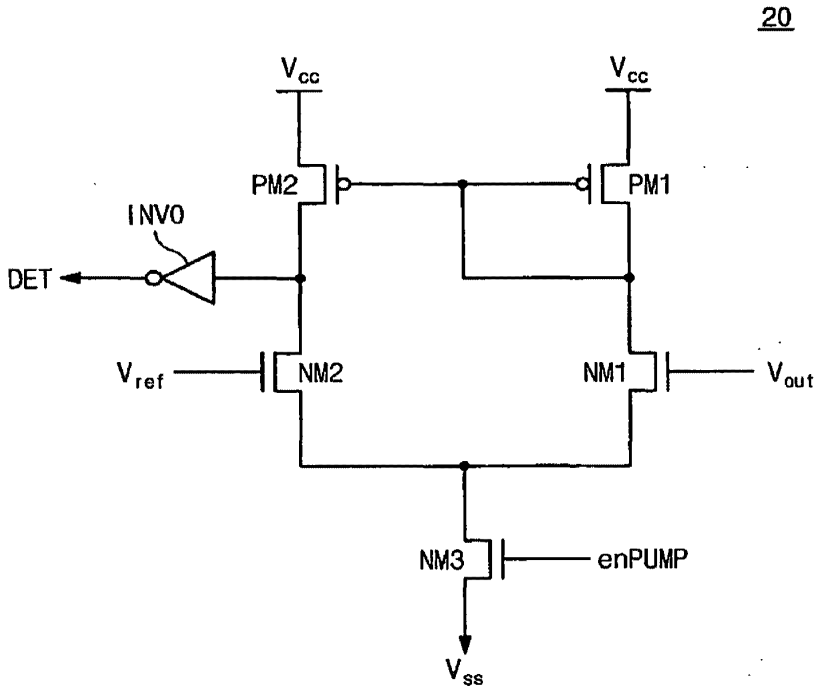


Fig. 3

(PRIOR ART)

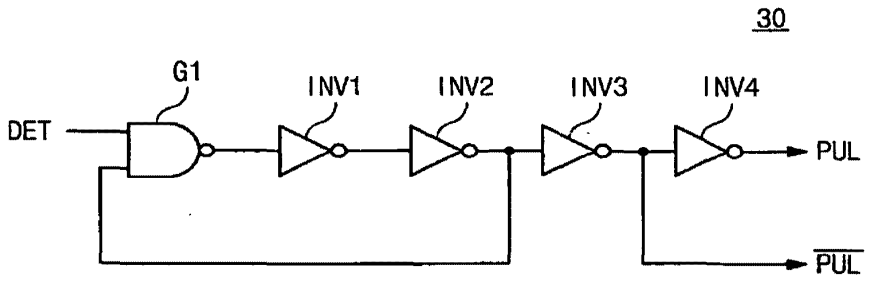


Fig. 1
(PRIOR ART)

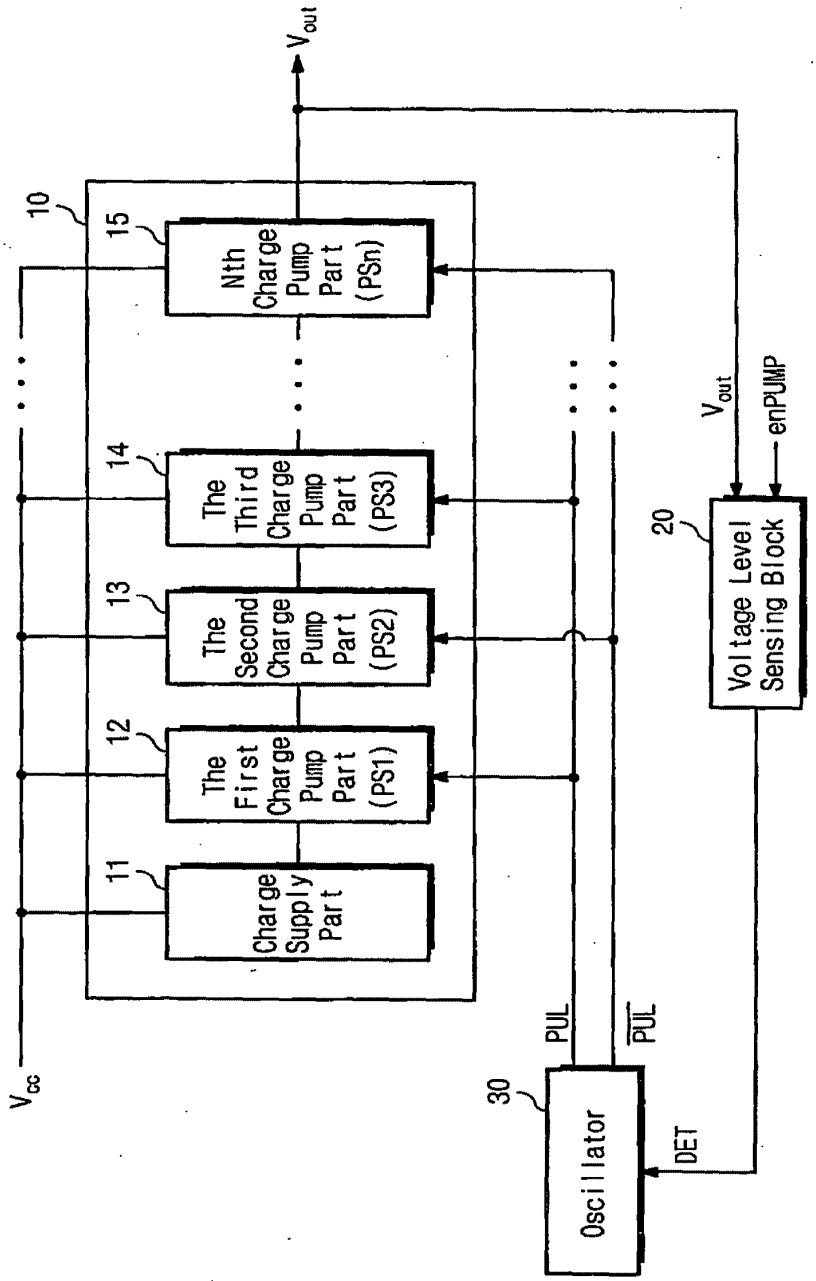


Fig. 2

(PRIOR ART)

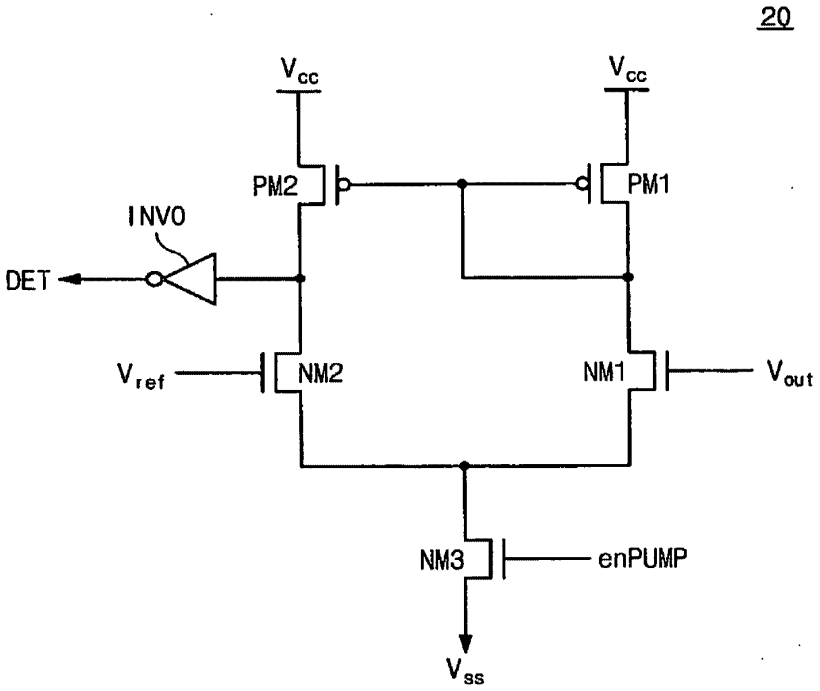
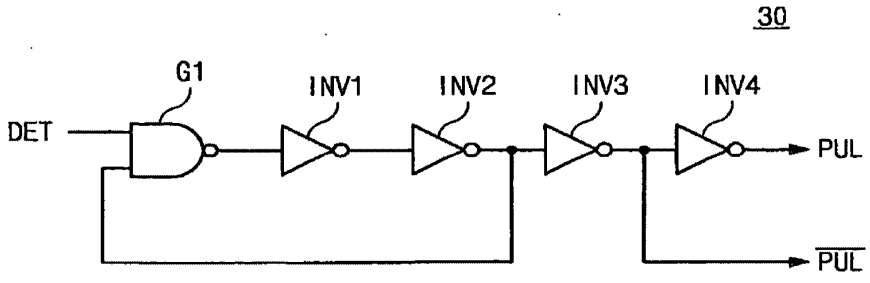


Fig. 3

(PRIOR ART)



PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number: 10888647

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	23	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	23 minus 20=	* 3
INDEPENDENT CLAIMS	5 minus 3 =	* 2
MULTIPLE DEPENDENT CLAIM PRESENT		☐

1 11 16 17 20

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	770.00
XS 9=	2700	OR	X$18=	
X43=	86.00	OR	X86=	
+145=		OR	+290=	
TOTAL	498.00	OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A	(Column 1)		(Column 2)	(Column 3)
1/13/06	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	* 10	Minus	** 23	=
Independent	* 1	Minus	*** 5	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/888,667	07/08/2004	Pyung-Moon Zhang	4591-380	4240

7590 11/16/2005

Alan T. McCollom
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1030 S.W. Morrison Street
Portland, OR 97205

EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/888,667	ZHANG ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/08/04* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/29/05, 10/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 6, 8-10, 14-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear what is meant by "charge trapping circuit" in the recited claims. In the drawings (Fig. 5), the "charge trapping circuit" seems to merely be a capacitive diode, and it is not understood how the capacitive diode would "trap charge".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

Claims 1-4 rejected under 35 U.S.C. 102(b) as being anticipated by Tanazawa et al by (USPN 6,429,725).

With respect to claim 1, the above combination discloses, "a charge pump circuit comprising:

a charge pump block including at least one charge pump part (N12 coupled with C11); and

a voltage supply circuit to supply a pre-charge voltage to the at least one charge pump part responsive to a mode (Terminals 12 and 13 supply a voltage (Vcc or Vp) to transistors N16 and N16, supply a pre-charge at node CN1 and N12. The level of the pre-charge depends on the level of the signal PGM (if PGM is high Vcc will be output, if PGM is low VPP is output)."

With respect to claim 2, the above combination discloses, "the charge pump circuit of claim 1 where the pre-charge voltage is a supply voltage in a general mode (Vcc is selected in general mode)."

With respect to claim 3, the above combination discloses, "the charge pump circuit of claim 1 where the pre-charge voltage is a voltage higher than the supply voltage in a test mode (Vp is higher than Vcc)."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-5, 7, 11-13, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanzawa et al. (USPN 6,429,725) in view of Arakawa (USPN 5,099,143). Tanzawa et al. teaches in Fig. 1 a charge pump that has a pre-charge voltage, which can be powered by a supply voltage (Vcc) or a higher than supply voltage (Vp), a voltage detector, and an oscillator circuit. Tanzawa et al. does not teach a voltage supply circuit capable of selecting between a supply voltage, and voltage that is higher than the supply voltage. However, Arakawa teaches, in Fig. 14, a voltage supply circuit capable of selecting between a supply voltage (Vcc), and a voltage higher than the supply voltage (Vpp). Arakawa also teaches a voltage supply circuit that minimizes amount current consumed when boosting a supply signal to a higher level. (See Col. 10 lines 10-21.)

It would have been *prima facie* obvious to one of ordinary skill in the art at the time the invention was made to use the voltage supply circuit of Arakawa to supply power to the circuit in Fig. 1 of Tanzawa et al. for the purpose of having a voltage supply circuit that can output two levels (Vcc and Vpp), and minimizes the amount of current used in the generation of the supply voltage. One skilled in the art would have been motivated to combine Tanazwa et al. and Arakawa with a reasonable expectation of success.

With respect to claim 1, the above combination discloses, "a charge pump circuit comprising:

a charge pump block including at least one charge pump part (N12 coupled with C11); and

a voltage supply circuit to supply a pre-charge voltage to the at least one charge pump part responsive to a mode (Arakawa's circuit outputs Vpp/Vcc to be supplied to terminals 12 and 13 of Tanzawa et al., which supply a pre-charge to node CN1 and N12. The level of the pre-charge depends on the level of the signal PGM (if PGM is high Vcc will be output, if PGM is low VPP is output)."

With respect to claim 4, the above combination discloses, "the charge pump circuit of claim 1 where the voltage supply circuit comprises: a detector circuit to generate a detect signal responsive to a high voltage (INV, detects the level of PGM, by detecting what its present level is and then inverting the level); and a selector circuit to supply the pre-charge voltage responsive to the detect signal (the "voltage supply ckt" of Fig. 14 of Arakawa supplies Vpp or Vcc to the circuit of Fig. 1 of Tanazwa et al.

depending on the detected level of the inverter inv, and if Φ is detected as an input to the circuit of Fig. 14 of Arakawa)."

With respect to claim 5, the above combination discloses, "the charge pump circuit of claim 1 where the voltage supply circuit comprises:

a voltage level sensing block to generate a level sensing signal responsive to a pump enable signal (Op1 is a voltage detection circuit responsive to the ACT (activate) signal, which is connected to N14 of the resistive divider (R11 and R12) connected to OP1); and

an oscillator to generate complementary pulse signals responsive to the level sensing signal (OSC1 receives an output from OP1 at ND1. Which, outputs complementary signals to C11 and C12 at the outputs of 112 and 114)."

With respect to claim 6, the above modified combination discloses, "the charge pump circuit of claim 1 where the voltage supply circuit comprises a charge trapping part to generate an output voltage (N13 "traps" the charge at node CN2 until the voltage at CN2 becomes larger than the threshold voltage of N13, and then the voltage at CN2 will be output)."

With respect to claim 7, the above combination discloses, "a charge pump circuit comprising:

at least one charge pump part (N12 coupled with C11 is a charge pump);

a voltage level sensing block to generate a level sensing signal by sensing an output voltage (OP1 senses the output signal OUT);

an oscillator to generate complementary pulse signals responsive to the level sensing signal (OSC1 is responsive to the output of OP1, and generates complementary signals at the outputs of 112 and 114); and

a selecting circuit block to generate a selected voltage that is one of a high voltage and a supply voltage to the at least one charge pump part, the high voltage having a level higher than the supply voltage (the supply circuit of Arakawa selects between Vcc and Vpp (Vpp is higher than Vcc) to be output to terminal 12 and 13 of Tanazawa et al.)."

With respect to claim 8, the above combination discloses, "The charge pump circuit of claim 7 comprising:

a charge supply part (N17 and N16) to pre-charge the at least one charge pump part (CN1 is charged which is part of the first charge pump (N12 with C11) with the selected voltage (Vcc or Vpp from Fig. 16 of Arakawa, is sent to terminals 13 and 12 of Tanzawa et al.); and

a charge trapping part to store charges provided by the charge supply part (N13 "traps" the charge at node CN2 until the voltage at CN2 becomes larger than the threshold voltage of N13, and then the voltage at CN2 will be output)."

With respect to claim 9, the above combination discloses, "the charge pump circuit of claim 8 where the at least one charge pump part pumps a charge to another charge pump part (the charge pump connected at CN1 pumps charge into CN2, where N13 and C12 also function as a charge pump)."

With respect to claim 10, the above combination discloses, the charge pump circuit of claim 8 where the charge supply part comprises a high-voltage PMOS transistor (N17 supplies charge to CN1 in conjunction with N16. It can be seen that N17 is a PMOS transistor)."

With respect to claim 12, the above combination discloses, "the charge pump circuit of claim 7 where the selecting circuit block compares the supply voltage with the high voltage (the selecting block compares Vcc and Vpp within the voltage supply ckt); and

where the selecting circuit selects the high voltage if a level of the high voltage is higher than a level of the power voltage (if PGM is low, and Φ is input to the voltage supply circuit, and Vpp is higher than Vcc, Vpp will output from Arakawa's Fig. 14)."

With respect to claim 13, the above combination discloses, "a charge pump circuit comprising:

a charge pump block including at least one charge pump part (N12 coupled with C11);

a voltage level sensing block to sense a level of an output voltage and generate a level sensing signal responsive thereto (OP1 detects the output of N12 and N13);

an oscillator to generate a pulse signal responsive to the level sensing signal (OSC1 Outputs a signal in response to OP1);

a detector to generate a detection signal responsive to a high voltage (inv of Fig. 14 of Arakawa detects if PGM is a high voltage or not and outputs a signal to the voltage supply circuit);

and a selector to provide one of the high voltage and the power voltage responsive to the detection signal to the charge pump block (the voltage supply circuit outputs Vpp or Vcc to terminal 12 and 13 of Fig. 14 of Tanzawa et al., which then sends a pre-charge signal to node CN1 and transistor N12)."

With respect to claim 14, the above combination discloses, "the charge pump circuit of claim 13 where the charge pump block comprises:

a charge supply part to pre-charge the at least one charge pump part (N17 and N16) operate together to supply a pre-charge to CN1 and N12); and

a charge trapping part to store charges pumped from the at least one charge pump part (N13 "traps" the charge at node CN2 until the voltage at CN2 becomes larger than the threshold voltage of N13, and then the voltage at CN2 will be output)."

With respect to claim 15, the above combination discloses, "the charge pump circuit of claim 14 where the at least one charge pump part pumps charge to another serially connected charge pump part (the output of N12 pumps into input node CN2 of N13)."

With respect to claim 16, the above combination discloses, "the charge pump circuit of claim 14 where the charge supply part includes a high-voltage PMOS transistor (N17 supplies charge to CN1 in conjunction with N16. It can be seen that N17 is a PMOS transistor)."

With respect to claim 18, the above combination discloses, "the charge pump circuit of claim 13 where the selector compares the high voltage to the power voltage (The selector of Arakawa compares the high voltage to the power voltage, by having

Vcc and Vpp input the voltage supply circuit, which are compared corresponding to the level of PGM and Φ (i.e. PGM is low and Φ is present Vpp is selected. Otherwise Vcc is selected to output)."

Claims 11, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanzawa et al. (USPN 6,429,725) in view of Arakawa (USPN 5,099,143). Tanazawa et al. and Arakawa teach the circuits as recited in claims 1-11, 12-16, and 18 above. Tanazawa et al. fails to disclose is a charge pump with NMOS transistors. However, it is notoriously well-know in the art that the charge pump transistors of Tanzawa et al. are actually diode-connected transistors (connecting the gate of the transistors to the drain of the transistor). It is also notoriously well-know that both PMOS and NMOS transistors function the same when connected as diodes, and that it would make no difference if the PMOS transistors of the charge pumps of Tanazawa et al. where replace by NMOS transistors (For example, Rao (USPN 6,177,830) discloses a charge pump composed of diode connected NMOS transistors).

It would have been *prima facie* obvious to one of ordinary skill in the art at the time the invention was made to replace the PMOS transistors, with NMOS transistors, due to the doctorine of equivalents.

With respect to claim 11, the above combination discloses, "the charge pump circuit of claim 7 where the at least one charge pump part includes a high-voltage NMOS transistor (N12 and N13 are both NMOS transistors as modified above)."

With respect to claim 17, the above combination discloses, "the charge pump circuit of claim 14 where the charge pump block includes a high-voltage NMOS

transistor (both N12, and N13 are NMOS as modified above).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Toyoshima et al. (USPN 5,448,198), Canclini (USPN 5,717,581), both disclose charge pump circuits that receive dual supply voltages.

Kang et al. (USPN 5,841,725) discloses a charge pump circuit with a high voltage detector and a pre-charge circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571) 272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH
November 14, 2005

Terry D. Cunningham
Primary Examiner
Art Unit 2816

PATENT APPLICATION

Atty. Docket No.:	4591-380	Serial No.	10/888,667
Applicant:	Pyung-Moon ZHANG and Seung-Keun LEE		
Filing Date:	July 8, 2004	Group:	2816

INFORMATION DISCLOSURE CITATION
FORM PTO-1449 (Modified)

U.S. PATENT DOCUMENTS

Exam Init	Ref	Document Number	Issue Date	Name	Class	Sub Class

FOREIGN PATENT DOCUMENTS

Exam Init	Ref	Document Number	Publication Date	Country	Name
TH	—	2002-0002541	Jan. 10, 02	Korea	Jae-Seok PARK

(No translation)

OTHER DOCUMENTS

Exam Init	Ref	Author, Title, Date, Pertinent Pages, Etc.)
TH	—	English language abstract of Korean Publication No. 2002-0002541

Examiner: [signature]

Date Considered: 11/14/05

10/843,383

PTO/SB/08a (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	1

Complete if Known	
Application Number	10/843,383
Filing Date	5/12/2004
First Named Inventor	Sommer, *et al.*
Art Unit	2818
Examiner Name	TBD
Attorney Docket Number	INF-152

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
TH	1	US-2003/0058165 A1	03-20-2003	Whetsel, Jr.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	11/10/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Copied from 10843383 on 11/04/2004

Notice of References Cited	Application/Control No. 10/888,667	Applicant(s)/Patent Under Reexamination ZHANG ET AL.	
	Examiner Thomas J. Hiltunen	Art Unit 2816	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,099,143	03-1992	Arakawa, Hideki	327/408
*	B	US-5,448,198	09-1995	Toyoshima et al.	327/530
*	C	US-5,717,581	02-1998	Canclini, Athos	363/60
*	D	US-5,841,725	11-1998	Kang et al.	365/226
*	E	US-6,177,830	01-2001	Rao, Kameswara K.	327/536
*	F	US-6,429,725	08-2002	Tanzawa et al.	327/536
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"5099143".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/11/14 07:39
L2	7449	charge near trap$4	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/11/14 07:39
L3	937256	charge pump with charge near trap$4	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/11/14 07:40
L4	15	charge near pump with charge near trap$4	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/11/14 07:56
L5	41	charge near pump with charge with trap$4	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/11/14 07:56
L6	425	(dual or multiple or two or many) near supply and charge near pump	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/11/14 08:49
L7	1678	charge near pump and voltage near detect$4	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/11/14 08:49
L8	3789	(dual or multiple or two or many) with supply and charge near pump	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/11/14 08:49
L11	9644	(dual or multiple or two or many) near supply and (charge near pump or multip$4 or boost$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/11/14 08:52
L12	48	(dual or multiple or two or many) near supply and (charge near pump or multip$4 or boost$4) and charge near trap$5	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/11/14 08:51

L13	1434	(dual or multiple or two or many) near supply and (charge near pump or multip$4 or boost$4) and oscillator	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/11/14 08:52
L14	1147	(dual or multiple or two or many) near supply and (charge near pump or multip$4 or boost$4) and oscillator and (sense or detect$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/11/14 08:52

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number: 10888647

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	23	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	23 minus 20=	* 3
INDEPENDENT CLAIMS	5 minus 3 =	* 2
MULTIPLE DEPENDENT CLAIM PRESENT		☐

1 11 16 17 20

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	770.00
X$ 9=	2700	OR	X$18=	
X43=	86.00	OR	X86=	
+145=		OR	+290=	
TOTAL	498.00	OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 5	Minus	** 20	=
Independent	* 1	Minus	*** 3	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☒

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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I hereby certify that the attached PTO form 1449 (3 pages), Information Disclosure Statement (1 page) and two cited references (15 pages) are submitted to the U.S. Patent and Trademark Office via facsimile number 703-872-9306 on the date shown below. (Total 19 pages).

Li Mei Vermilya

Date: March 29, 2005

PATENT APPLICATION
Attorney's Do. No. 4591-380
Client No. ID13095-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Pyung-Moon Zhang and Seung-Keun LEE		
Serial No.	10/888,667	Group Art Unit:	2816
Filed:	July 8, 2004	Examiner:	Not yet assigned
Confirmation No.	4240		
For:	CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

☐ under 37 CFR 1.97 (b); or
(Within three months of filing national application; or date of entry of International application; or before mailing date of first office action on the merits; or before the mailing of a first Office Action after the filing of a request for continued examination under §1.114; whichever occurs last)

☒ under 37 CFR 1.97 (c) together with either a:
- ☒ Statement under 37 CFR 1.97 (e), or
- ☐ a $180 fee under 37 CFR 1.17 (p); or

(After mailing of first Office Action, but prior to Notice of Allowance or Final Office Action)

☐ under 37 CFR 1.97 (d) together with:
- ☐ Statement under 37 CFR 1.97 (e), and
- ☐ a $180.00 fee set forth in 37 CFR 1.17 (p).

(Filed after final action or notice of allowance, whichever occurs first, but before payment of the issue fee)

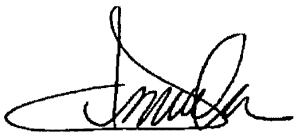
☒ Applicant(s) submit herewith Form PTO 1449- Information Disclosure Citation together with copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

It is requested that the information disclosed herein be made of record in this application.

Any deficiency or overpayment should be charged or credited to deposit account number 13-1703. A duplicate copy of this sheet is enclosed.

Customer No. 20575

Respectfully submitted,
MARGER JOHNSON & McCOLLOM, P.C.



Graciela G. Cowger, Reg. No. 42,444

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
503-222-3613

PATENT APPLICATION

Atty. Docket No.:	4591-380	Serial No.	10/888,667
Applicant:	Pyung-Moon ZHANG and Seung-Keun LEE		
Filing Date:	July 8, 2004	Group:	2816

INFORMATION DISCLOSURE CITATION
FORM PTO-1449 (Modified)

U.S. PATENT DOCUMENTS

Exam Init	Ref	Document Number	Issue Date	Name	Class	Sub Class

FOREIGN PATENT DOCUMENTS

Exam Init	Ref	Document Number	Publication Date	Country	Name
		2002-0002541	Jan. 10, 02	Korea	Jae-Seok PARK

OTHER DOCUMENTS

Exam Init	Ref	Author, Title, Date, Pertinent Pages, Etc.)
		English language abstract of Korean Publication No. 2002-0002541

Examiner: _____

Date Considered: _____

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MAR 29 2005

PATENT APPLICATION
Attorney's Do. No. 4591-380
Client No. ID13095-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Pyung-Moon Zhang and Seung-Keun LEE		
Serial No.	10/888,667	Group Art Unit:	2816
Filed:	July 8, 2004	Examiner:	Not yet assigned
Confirmation No.	4240		
For:	CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

STATEMENT ON FILING INFORMATION DISCLOSURE STATEMENT
(37 CFR 1.97(e))

I, Graciela G. Cowger, the person signing below state that:
each item of information contained in the Information Disclosure Statement submitted herewith was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Statement

no information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to the knowledge of the person signing this Statement after making reasonable inquiry, was known to any individual designated in § 1.56(c) more than three months prior to the filing of the Statement.

Applicant respectfully requests consideration of the accompanying Information Disclosure Statement.

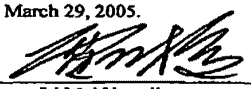
The person making this Statement is the attorney who signs below on the basis of the information in the attorney's file.

Respectfully submitted,
MARGER JOHNSON & McCOLLOM, P.C.

Graciela G. Cowger, Reg. No. 42,444

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
503-222-3613

I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number 703-872-9306, on March 29, 2005.



Li Mei Vermilya

PAGE 4/19 * RCVD AT 3/29/2005 4:30:46 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/7 * DNIS:8729306 * CSID:5032744622 * DURATION (mm-ss):07-38

(19) KOREAN INTELLECTUAL PROPERTY OFFICE

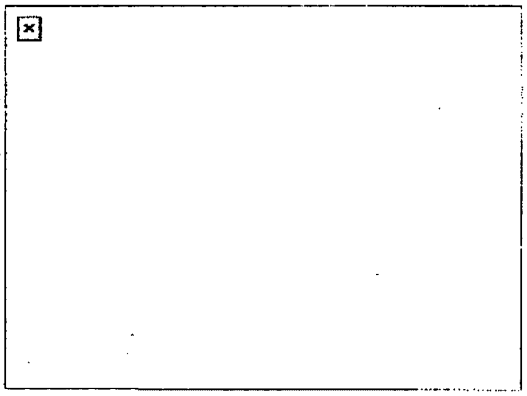
KOREAN PATENT ABSTRACTS

(11)Publication number: 1020020002541 A
(43)Date of publication of application: 10.01.2002

(21)Application number: 1020000036748
(22)Date of filing: 30.06.2000
(51)Int. Cl G11C 8/00

(71)Applicant: HYNIX SEMICONDUCTOR INC.
(72)Inventor: PARK, JAE SEOK

(54) DELAY LOCKED LOOP HAVING HIGH VOLTAGE GENERATOR FOR DELAY LOCKED LOOP WITH LOW JITTER



(57) Abstract:

PURPOSE: A delay locked loop(DLL) having a high voltage generator for a delay locked loop(DLL) with a low jitter is provided, which has the low jitter even in a high frequency operation by increasing a supply voltage of a unit delay used during an operation of the DLL to a high voltage.

CONSTITUTION: A pump control part(100) generates a pump control signal(pump_con) by receiving an active signal(cmp_en) of a phase detector comparing a phase difference between an external clock and an internal clock and a locking signal(Lockb) informing that the external clock is synchronized to an internal clock passing through a delay locked loop(DLL). A high voltage generation part(110) generates a high voltage by being controlled by the pump control signal. And a power supply variable circuit part(120) applies the high voltage and a power supply voltage selectively to a delay part of the delay locked loop by being controlled by the pump control signal.

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Legal Status

PAGE 5/19 * RCVD AT 3/29/2005 4:30:48 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/7 * DNIS:8729306 * CSID:5032744622 * DURATION (mm-ss):07-38

공개특허 특2002-0002541

(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

(51) Int. Cl. 7
G11C 8/00

(11) 공개번호 특2002-0002541
(43) 공개일자 2002년01월10일

(21) 출원번호 10-2000-0036748
(22) 출원일자 2000년06월30일

(71) 출원인 주식회사 하이닉스반도체
박종섭
경기 이천시 부발읍 아미리 산136-1

(72) 발명자 박재석
서울특별시광진구자양동774번지

(74) 대리인 특허법인 신성

심사청구 : 없음

(54) 적은 지터의 지연고정루프를 위해 고전압 발생 장치를갖는 지연고정루프

요약

본 발명은 반도체메모리 장치의 지연고정루프를 위해 고전압 발생 장치를 갖는 지연고정루프에 관한 것으로 지연고정루프의 동작 시에 쓰이는 단위 딜레이의 공급전원을 고전압으로 올려주어 고주파 동작 시에도 적은 지터 특성을 갖는 지연고정루프를 위한 고전압 발생 장치를 갖는 지연고정루프를 제공하는데 그 목적이 있다. 이를 위하여 본 발명은 반도체메모리 장치에 있어서, 외부의 클럭과 내부의 클럭 간의 위상 차를 비교하는 위상 검출기의 활성화신호와 외부 클럭과 지연고정루프를 거친 내부 클럭이 동기되었음을 알려주는 고정신호를 입력받아 펌프제어신호를 생성하기 위한 펌프제어부; 상기 펌프제어신호의 제어를 받아 고전압을 발생하기 위한 고전압펌핑부; 및 상기 펌프제어신호의 제어를 받아 지연고정루프의 딜레이부에 고전압과 전원전압을 선택적으로 인가하기 위한 전원공급가변회로부를 포함하여 이루어진다.

대표도
도 1

색인어
펌프제어부, 고전압펌핑부, 전원공급가변회로부, 내부전압전달부, 내부전압전달용 차지펌핑부, 고전압생성용 차지펌핑부, 고전압전달부

명세서

PAGE 6/19 * RCVD AT 3/29/2005 4:30:48 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/7 * DNIS:8729306 * CSID:5032744622 * DURATION (mm-ss):07-38

도면의 간단한 설명

도1은 본 발명의 고전압 발생 장치를 나타낸 블럭도,

도2는 펌프제어부의 상세한 회로도,

도3은 고전압펌핑부의 상세한 회로도,

도4는 상기 제1 내지 제4펄스신호(pl1, pl2, pr1, pr2)의 동작을 나타내는 파형도,

도5는 전원공급가변회로부의 블럭도,

도6은 제1전위변환기의 상세한 회로도,

도7은 제2전위변환기의 상세한 회로도.

* 도면의 주요 부분에 대한 부호의 설명 *

100 : 펌프제어부 110 : 고전압펌핑부

120 : 전원공급가변회로부 300 : 내부전압전달부

310 : 내부전압전달용 차지펌핑부 320 : 고전압생성용 차지펌핑부

330 : 고전압전달부

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 반도체메모리 장치에 관한 것으로, 특히 적은 지터(Jitter)의 지연고정루프를 위해 고전압 발생 장치를 갖는 지연고정루프에 관한 것이다.

일반적으로 DRAM에서의 고전압 발생 장치는 셀(Cell)의 데이터가 엔모스트랜지스터의 스위칭으로 인해 비트라인으로 전달될 때 셀의 엔모스트랜지스터의 게이트단에 전원전압보다 높은 전압을 인가하여 상기 엔모스트랜지스터의 문턱전압에 의한 손실을 없애기 위하여 사용되는 것이다. 즉, 셀 트랜지스터의 게이트단에 접속된 워드라인에 전원전압(Vcc) + 문턱전압(Vt) + α 의 전압을 인가함으로써 셀의 데이터가 문턱전압에 의하여 손실되는 것을 방지한다. 또한 상기 고전압 발생 장치는 빠른 속도를 요구하는 구동장치에서도 사용되는데, 이 때, 전원전압보다 높은 고전압으로 풀-업(Pull-up)시킴으로써 구동력을 증가시킬 수 있고 보다 빠른 스위칭을 얻을 수 있다.

한편, DRAM이 점 점 고속화되어 감에 따라, DDR(Double Data Rate) DRAM에서는 외부의 클럭을 내부에서 사용하는 클럭에 타이밍 딜레이가 없이 동일하게 동기되도록 하기 위하여 지연고정루프(Delay Locked Loop)를 사용하는데, 이러한 지연고정루프는 통상적으로, 외부클럭을 입력받는 외부클럭수신부와, 지연고정루프의 최종 출력 클럭을 입력받아 지연량을 모델링하기 위한 딜레이모니터와, 상기 외부클럭수신부의 입력된 클럭과 상기 딜레이모니터로부터 피드백된 신호와의 위상을 비교하여 클럭의 위상 차이를 검출하기 위한 위상검출기와, 상기 위상 검출기로부터 왼쪽이나 오른

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쪽으로 쉬프트하라는 신호를 입력받아 딜레이의 양을 제어하기 위한 쉬프트레지스터와, 상기 쉬프트레지스터의 제어를 받아 입력되는 클럭의 지연량을 조절하기 위한 딜레이부와, 최종 클럭 신호를 출력하기 위한 출력부로 구성되어 있다.

상기 딜레이부는 보통 난드게이트와 인버터 구성된 단위 딜레이를 여러 단으로 연결하여 구성되는데, 상기 난드게이트와 인버터로 구성된 딜레이부를 통과하는 시간이 지연고정루프의 해상도를 나타내는 지터(Jitter)를 결정하는데 중요한 관건이 된다.

이 지터(Jitter)가 작을수록 외부 클럭이 내부 클럭에 동기될 때의 오차가 작아지게 되는데, 상기 난드게이트와 인버터로 이루어진 단위 딜레이는 전원전압에 대해 일정한 시간 지연을 발생하기 때문에 상기 단위 딜레이가 가지고 있는 시간 지연량보다 적은 시간 지연을 조절할 수가 없게 된다.

종래의 기술은 지터(Jitter)의 크기를 결정하는 단위딜레이가 전원전압으로 구동하는 난드게이트와 인버터로 이루어져 있으므로 지터가 100ps 이상으로 크다. 이 것은 저전압으로 가면서 더욱 커지게 되는데 회로의 동작 속도가 고속화할수록 더욱 작은 지터(Jitter)가 요구되므로 향 후 전개될 저전압 초고속화 시대에 적합하지 못하다.

발명이 이루고자 하는 기술적 과제

본 발명은 상기와 같은 종래 기술의 문제점을 해결하기 위하여 안출된 것으로써, 지연고정루프의 동작 시에 쓰이는 단위 딜레이의 공급전원을 고전압으로 올려주어 고주파 동작 시에도 적은 지터 특성을 갖는 지연고정루프를 위해 고전압 발생 장치를 갖는 지연고정루프를 제공하는데 그 목적이 있다.

발명의 구성 및 작용

상기 목적을 달성하기 위하여 본 발명의 지연고정루프는 외부클럭을 입력받는 외부클럭수신부와, 지연고정루프의 최종 출력 클럭을 입력받아 지연량을 모델링하기 위한 딜레이모니터와, 상기 외부클럭수신부의 입력된 클럭과 상기 딜레이모니터로부터 피드백된 신호와의 위상을 비교하여 클럭의 위상 차이를 검출하기 위한 위상검출기와, 상기 위상 검출기로부터 왼쪽이나 오른쪽으로 쉬프트하라는 신호를 입력받아 딜레이의 양을 제어하기 위한 쉬프트레지스터와, 상기 쉬프트레지스터의 제어를 받아 입력되는 클럭의 지연량을 조절하기 위한 딜레이부와, 최종 클럭 신호를 출력하기 위한 출력부를 구비하는 지연고정루프에 있어서, 상기 딜레이부의 전원소스용 고전압 발생 장치를 구비하며, 상기 고전압 발생 장치는, 외부의 클럭과 내부의 클럭 간의 위상 차를 비교하는 위상 검출기의 활성화신호와 외부 클럭과 지연고정루프를 거친 내부 클럭이 동기되었음을 알려주는 고정신호를 입력받아 펌프제어신호를 생성하기 위한 펌프제어부; 상기 펌프제어신호의 제어를 받아 고전압을 발생하기 위한 고전압펌핑부; 및 상기 펌프제어신호의 제어를 받아 지연고정루프의 딜레이부에 고전압과 전원전압을 선택적으로 인가하기 위한 전원공급가변회로부

를 포함하여 이루어진다.

이하, 본 발명이 속하는 기술분야에서 통상의 지식을 가진 자가 본 발명의 기술적 사상을 용이하게 실시할 수 있을 정도로 상세히 설명하기 위하여, 본 발명의 가장 바람직한 실시예를 첨부한 도면을 참조하여 설명하기로 한다.

도1은 본 발명의 고전압 발생 장치를 나타낸 블럭도이다.

도1을 참조하면, 본 발명의 고전압 발생 장치는 외부의 클럭과 내부의 클럭 간의 위상 차를 비교하는 위상 검출기의 활성화신호(cmp_en)과 외부 클럭과 지연고정루프를 거친 내부 클럭이 동기되었음을 알려주는 고정신호(Lockb)를 입력받아 펌프제어신호(pump_con)를 생성하기 위한 펌프제어부(100)와, 상기 펌프제어신호(pump_con)의 제어를 받아 고전압을 발생하기 위한 고전압펌핑부(110)와, 상기 펌프제어신호(pump_con)의 제어를 받아 지연고정루프의 딜레이부에 고전압과 전원전압을 선택적으로 인가하기 위한 전원공급가변회로부(120)를 구비한다.

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도2는 상기 펌프제어부(100)의 상세한 회로도이다.

도2를 참조하면, 펌프제어부(100)는 상기 활성화신호(cmp_en)와 상기 고정신호(Lockb)를 입력받는 난드게이트(200)와, 상기 난드게이트(200)의 출력을 반전하여 펌프제어신호(pump_con)를 출력하는 인버터(110)를 구비한다.

동작을 설명하면, 초기 상태에서 상기 활성화신호(cmp_en)는 논리 로우이고 상기 고정신호(Lockb)는 논리 하이이므로, 상기 난드게이트(200)의 출력은 논리 하이이고 이 출력이 인버터(210)를 거치므로 상기 펌프제어신호(pump_con)는 논리 로우가 된다. 그리고나서 상기 활성화신호(cmp_en)가 논리 하이가 되면 상기 난드게이트(200)의 출력은 논리 로우가 되고 상기 펌프제어신호(pump_con)는 논리 하이가 되어 상기 고전압펌핑부(110)를 구동시키며 상기 전원공급가변회로부(120)에서 지연고정루프의 딜레이부의 공급전원을 전원전압(Vint)에서 고전압(Vpp)로 바꾸어주게 된다.

그리고나서 지연고정루프가 락킹(Locking)이 되면 상기 고정신호(Lockb)가 논리 로우가 되어 상기 난드게이트(200)의 출력은 논리 하이가 되고 상기 펌프제어신호(pump_con)는 논리 로우가 되어 상기 고정압펌프부(110)의 동작을 중지시키며 상기 전원공급가변회로부(120)에서 지연고정루프의 딜레이부의 공급전원을 고전압(Vpp)에서 전원전압(Vint)로 되돌리게 한다.

도3은 상기 고전압펌핑부(110)의 상세한 회로도이다.

도3을 참조하면, 상기 고전압펌핑부(110)는 펌핑 시에 전원전압을 전달하기 위한 내부전압전달부(300)와, 오실레이터에서 생성된 제1 및 제2 펄스신호(pl1, pr1)와 상기 펌프제어신호(pump_con)에 제어받아 상기 내부전압전달부(300)에 펌핑된 전압을 공급하기 위한 내부전압전달용 차지펌핑부(310)와, 펌핑 시에 고전압을 전달하기 위한 고전압전달부(330)와, 오실레이터에서 생성된 제3 및 제4 펄스신호(pl2, pr2)와 상기 펌프제어신호(pump_con)에 제어받아 고전압전달부(330)에 펌핑된 전압을 공급하기 위한 고전압생성용 차지펌핑부(320)를 구비한다.

구체적으로, 상기 내부전압전달부(300)는 내부전압전달용 차지펌핑부(310)의 제2출력을 게이트단으로 입력받고 소스-드레인 경로가 전원전압과 상기 내부전압전달용 차지펌핑부(310)의 제1출력 사이에 형성된 제1엔모스트랜지스터(301)와, 내부전압전달용 차지펌핑부(310)의 제1출력을 게이트단으로 입력받고 소스-드레인 경로가 전원전압과 상기 내부전압전달용 차지펌핑부(310)의 제2출력 사이에 형성된 제2엔모스트랜지스터(302)와, 상기 내부전압전달용 차지펌핑부(310)의 제1출력을 게이트단으로 입력받고 소스-드레인 경로가 전원전압과 노드1 사이에 형성된 제3엔모스트랜지스터(303)와, 상기 내부전압전달용 차지펌핑부(310)의 제2출력을 게이트단으로 입력받고 소스-드레인 경로가 전원전압과 노드2 사이에 형성된 제4엔모스트랜지스터(304)와, 전원전압을 게이트단으로 입력받고 소스-드레인 경로가 전원전압과 상기 내부전압전달용 차지펌핑부(310)의 제1출력 사이에 형성된 제5엔모스트랜지스터(305)와, 전원전압을 게이트단으로 입력받고 소스-드레인 경로가 전원전압과 상기 내부전압전달용 차지펌핑부(310)의 제2출력 사이에 형성된 제6엔모스트랜지스터(306)을 구비한다.

구체적으로, 상기 내부전압전달용 차지펌핑부(310)는 오실레이터의 제1펄스신호(pl1)를 반전하는 제1인버터(311)와, 상기 제1인버터(311)의 출력과 상기 펌프제어신호(pump_con)를 입력받는 제1난드게이트(312)와, 소스-드레인이 상기 제1난드게이트(312)의 출력단에 접속되어 있고 게이트단이 상기 제1출력을 출력하는 노드에 연결되어 있는 제1엔모스트랜지스터(313)와, 오실레이터의 제2펄스신호(pr1)를 반전하는 제2인버터(314)와, 상기 제2인버터(314)의 출력과 상기 펌프제어신호(pump_con)를 입력받는 제2난드게이트(315)와, 소스-드레인이 상기 제2난드게이트(315)

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의 출력단에 접속되어 있고 게이트단이 상기 제2출력을 출력하는 노드에 연결되어 있는 제2엔모스트랜지스터(316)를 구비한다.

구체적으로, 상기 고전압전달부(330)는 상기 노드2를 게이트단으로 입력받고 소스-드레인 경로가 상기 노드1과 고전압(Vpp) 사이에 형성된 제1피모스트랜지스터(331)와, 상기 노드1을 게이트단으로 입력받고 소스-드레인 경로가 상기 노드2과 고전압(Vpp) 사이에 형성된 제2피모스트랜지스터(332)를 구비한다.

구체적으로, 상기 고전압생성용 차지펌핑부(320)는 오실레이터의 제3펄스신호(pl2)를 반전하는 제1인버터(321)와, 상기 제1인버터(321)의 출력과 상기 펌프제어신호(pump_con)를 입력받는 제1난드게이트(322)와, 소스-드레인이 상기 제1난드게이트(322)의 출력단에 접속되어 있고 게이트단이 상기 노드1에 연결되어 있는 제1엔모스트랜지스터(323)와, 오실레이터의 제4펄스신호(pr2)를 반전하는 제2인버터(324)와, 상기 제2인버터(324)의 출력과 상기 펌프제어신호(pump_con)를 입력받는 제2난드게이트(325)와, 소스-드레인이 상기 제2난드게이트(325)의 출력단에 접속되어 있고 게이트단이 상기 노드2에 연결되어 있는 제2엔모스트랜지스터(326)를 구비한다.

도4는 상기 제1 내지 제4펄스신호(pl1, pl2, pr1, pr2)의 동작을 나타내는 파형도이다.

상기 도4를 참조하여 동작을 설명하면, 상기 제1 내지 제4펄스신호(pl1, pl2, pr1, pr2)는 모드 고전압 오실레이터에서 발생하는 지속적인 펄스신호들로써 상기 제1펄스신호(pl1)와 상기 제3펄스신호(pl2)는 서로 오버랩(Overlap)되지 않는 2 위상 펄스 신호이고 상기 제2펄스신호(pr1)와 상기 제4펄스신호(pr2)는 서로 오버랩되지 않는 2 위상 펄스 신호이다. 상기 제1 및 제2펄스신호(pl1, pr1)는 상기 노드1과 노드2를 손실 없는 온전한 내부 전압으로 만들기 위한 신호들이고 상기 제3 및 제4펄스신호(pl2, pr2)는 상기 노드1과 상기 노드2를 내부전압에서 고전압으로 승압시키기 위한 신호들이다. 이 신호들이 서로 오버랩되지 않으면서 작용하여 이중 펌핑을 하는 것이다. 상기 신호들이 인버터를 통과해서 입력되는 난드게이트의 타측 신호로써 펌프제어신호(pump_con)가 있는데, 상기 펌프제어신호(pump_con)가 논리 하이이면 상기 차지펌프부(310, 320)를 구동하고 논리 로우이면 동작을 중지하게 하여 지연고정루프가 동작할 때만 펌핑을 할 수 있게 한다.

도5는 상기 전원공급가변회로부(120)의 블럭도이다.

도5를 참조하면, 전원공급가변회로부(120)는 상기 펌프제어신호(pump_con)를 입력받아 펌프제어신호의 전원전압 레벨을 고전압(Vpp)으로 변환하기 위한 제1전위변환기(510)와, 상기 제1전위변환기(510)의 출력을 게이트단으로 입력받아 고전압(Vpp)을 공급접압으로 전달하기 위한 제1피모스트랜지스터(520)와, 상기 펌프제어신호(pump_con)를 입력받아 반전하는 인버터(530)와, 상기 인버터(530)의 출력을 입력받아 상기 인버터의 전원전압(Vcc)을 내부전압(Vint)으로 변환하기 위한 제2전위변환기(540)와, 상기 제2전위변환기(540)의 출력을 게이트단으로 입력받아 내부전압(Vint)을 공급전압으로 전달하기 위한 제2피모스트랜지스터(550)를 구비한다.

도6은 상기 제1전위변환기(510)의 상세한 회로도이다.

도6을 참조하면, 상기 제1전위변환기(510)는 상기 펌프제어신호(pump_con)를 입력받아 고전압(Vpp)으로 변환하는 차동증폭기(600)와, 상기 차동증폭기(600)의 출력을 반전하며 고전압(Vpp)을 풀-업하는 인버터(610)를 구비한다.

동작을 설명하면, 상기 펌프제어신호(pump_con)가 논리 하이인 경우에 상기 차동증폭기(600)에서 고전압(Vpp)이 출력되고 다음단의 인버터(610)를 통해서 출력이 논리 로우로 되어 상기 제1피모스트랜지스터(520)를 온시켜서 고전압(Vpp)을 공급전원으로 전달한다.

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도7은 상기 제2전위변환기(540)의 상세한 회로도이다.

도7을 참조하면, 상기 제2전위변환기(540)는 상기 인버터(530)의 출력을 입력받아 내부전압(Vint)으로 변환하는 차동증폭기(700)와, 상기 차동증폭기(700)의 출력을 반전하며 내부전압(Vint)을 풀-업하는 인버터(710)를 구비한다.

동작을 설명하면, 상기 인버터(530)의 출력이 논리 하이인 경우에, 즉 상기 펌프제어신호(pump_con)가 논리 로우인 경우에 상기 차동증폭기(600)에서 내부전압(Vint)이 출력되며 다음단의 인버터(710)를 통하여 출력이 논리 로우로 되어 상기 제2피모스트랜지스터(550)를 온시켜서 내부전압(Vint)을 공급전압으로 전달시킨다.

본 발명의 기술 사상은 상기 바람직한 실시예에 따라 구체적으로 기술되었으나 상기한 실시예는 그 설명을 위한 것이며 그 제한을 위한 것이 아님을 주의하여야 한다. 또한, 본 발명의 기술 분야의 통상의 전문가라면 본 발명의 기술 사상의 범위내에서 다양한 실시예가 가능함을 이해할 수 있을 것이다.

발명의 효과

상기와 같이 본 발명은 지연고정루프 동작시 딜레이부에 고전압을 공급함으로써 지연고정루프가 적은 지터(Jitter)를 갖게 할 수 있다. 또한, 고전압 발생 장치의 앞 단에 펌프제어부를 두어 필요할 때만 동작시키므로 액티브 전류 소모를 감소시킬 수 있다.

(57) 청구의 범위

청구항 1.

외부클럭을 입력받는 외부클럭수신부와, 지연고정루프의 최종 출력 클럭을 입력받아 지연량을 모델링하기 위한 딜레이 모니터와, 상기 외부클럭수신부의 입력된 클럭과 상기 딜레이모니터로부터 피드백된 신호와의 위상을 비교하여 클럭의 위상 차이를 검출하기 위한 위상검출기와, 상기 위상 검출기로부터 왼쪽이나 오른쪽으로 쉬프트하라는 신호를 입력받아 딜레이의 양을 제어하기 위한 쉬프트레지스터와, 상기 쉬프트레지스터의 제어를 받아 입력되는 클럭의 지연량을 조절하기 위한 딜레이부와, 최종 클럭 신호를 출력하기 위한 출력부를 구비하는 지연고정루프에 있어서,

상기 딜레이부의 전원소스용 고전압 발생 장치를 구비하며,

상기 고전압 발생 장치는,

외부의 클럭과 내부의 클럭 간의 위상 차를 비교하는 위상 검출기의 활성화신호와 외부 클럭과 지연고정루프를 거친 내부 클럭이 동기되었음을 알려주는 고정신호를 입력받아 펌프제어신호를 생성하기 위한 펌프제어부;

상기 펌프제어신호의 제어를 받아 고전압을 발생하기 위한 고전압펌핑부; 및

상기 펌프제어신호의 제어를 받아 지연고정루프의 딜레이부에 고전압과 전원전압을 선택적으로 인가하기 위한 전원공급가변회로부

를 포함하여 이루어진 지연고정루프.

청구항 2.

제 1 항에 있어서,

상기 펌프제어부는,

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상기 활성화신호와 상기 고정신호를 입력받는 난드게이트; 및

상기 난드게이트의 출력을 반전하여 펌프제어신호를 출력하는 인버터

를 포함하여 이루어진 것을 특징으로 하는 지연고정루프.

청구항 3.

제 1 항에 있어서,

상기 고전압펌핑부는,

펌핑 시에 제1노드와 제2노드에 전원전압을 전달하기 위한 내부전압전달부;

오실레이터에서 생성된 제1 및 제2 펄스신호와 상기 펌프제어신호에 제어받아 상기 내부전압전달부에 펌핑된 전압을 공급하기 위한 내부전압전달용 차지펌핑부;

펌핑 시에 제1노드와 제2노드의 전압을 입력받아 고전압을 전달하기 위한 고전압전달부;

오실레이터에서 생성된 제3 및 제4 펄스신호와 상기 펌프제어신호에 제어받아 제1노드와 제2노드에 펌핑된 전압을 공급하기 위한 고전압생성용 차지펌핑부

를 포함하여 이루어진 것을 특징으로 하는 지연고정루프.

청구항 4.

제 3 항에 있어서,

상기 내부전압전달부는,

내부전압전달용 차지펌핑부의 제2출력을 게이트단으로 입력받고 소스-드레인 경로가 전원전압과 상기 내부전압전달용 차지펌핑부의 제1출력 사이에 형성된 제1엔모스트랜지스터;

내부전압전달용 차지펌핑부의 제1출력을 게이트단으로 입력받고 소스-드레인 경로가 전원전압과 상기 내부전압전달용 차지펌핑부의 제2출력 사이에 형성된 제2엔모스트랜지스터;

상기 내부전압전달용 차지펌핑부의 제1출력을 게이트단으로 입력받고 소스-드레인 경로가 전원전압과 제1노드 사이에 형성된 제3엔모스트랜지스터;

상기 내부전압전달용 차지펌핑부의 제2출력을 게이트단으로 입력받고 소스-드레인 경로가 전원전압과 제2노드 사이에 형성된 제4엔모스트랜지스터;

전원전압을 게이트단으로 입력받고 소스-드레인 경로가 전원전압과 상기 내부전압전달용 차지펌핑부의 제1출력 사이에 형성된 제5엔모스트랜지스터; 및

전원전압을 게이트단으로 입력받고 소스-드레인 경로가 전원전압과 상기 내부전압전달용 차지펌핑부의 제2출력 사이에 형성된 제6엔모스트랜지스터

를 포함하여 이루어진 것을 특징으로 하는 지연고정루프.

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청구항 5.

제 3 항에 있어서,

상기 내부전압전달용 차지펌핑부는,

오실레이터의 제1펄스신호를 반전하는 제1인버터;

상기 제1인버터의 출력과 상기 펌프제어신호를 입력받는 제1난드게이트;

소스-드레인이 상기 제1난드게이트의 출력단에 접속되어 있고 게이트단이 상기 내부전압전달용 차지펌핑부의 제1출력을 출력하는 노드에 연결되어 있는 제1엔모스트랜지스터;

오실레이터의 제2펄스신호를 반전하는 제2인버터;

상기 제2인버터의 출력과 상기 펌프제어신호를 입력받는 제2난드게이트; 및

소스-드레인이 상기 제2난드게이트의 출력단에 접속되어 있고 게이트단이 상기 내부전압전달용 차지펌핑부의 제2출력을 출력하는 노드에 연결되어 있는 제2엔모스트랜지스터

를 포함하여 이루어진 것을 특징으로 하는 지연고정루프.

청구항 6.

제 3 항에 있어서,

상기 고전압전달부는,

상기 제2노드를 게이트단으로 입력받고 소스-드레인 경로가 상기 제1노드와 고전압 출력노드 사이에 형성된 제1피모스트랜지스터; 및

상기 제1노드를 게이트단으로 입력받고 소스-드레인 경로가 상기 제2노드와 고전압 출력노드 사이에 형성된 제2피모스트랜지스터

를 포함하여 이루어진 것을 특징으로 하는 지연고정루프.

청구항 7.

제 3 항에 있어서,

상기 고전압생성용 차지펌핑부는,

오실레이터의 제3펄스신호를 반전하는 제1인버터;

상기 제1인버터의 출력과 상기 펌프제어신호를 입력받는 제1난드게이트;

소스-드레인이 상기 제1난드게이트의 출력단에 접속되어 있고 게이트단이 상기 제1노드에 연결되어 있는 제1엔모스트랜지스터;

오실레이터의 제4펄스신호를 반전하는 제2인버터;

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상기 제2인버터의 출력과 상기 펌프제어신호를 입력받는 제2난드게이트; 및

소스-드레인이 상기 제2난드게이트의 출력단에 접속되어 있고 게이트단이 상기 제2노드에 연결되어 있는 제2엔모스트랜지스터

를 포함하여 이루어진 것을 특징으로 하는 지연고정루프.

청구항 8.

제 1 항에 있어서,

상기 전원공급가변회로부는,

상기 펌프제어신호를 입력받아 펌프제어신호의 전원전압 레벨을 고전압으로 변환하기 위한 제1전위변환기;

상기 제1전위변환기의 출력을 게이트단으로 입력받아 고전압을 공급접압으로 전달하기 위한 제1피모스트랜지스터;

상기 펌프제어신호를 입력받아 반전하는 인버터;

상기 인버터의 출력을 입력받아 상기 인버터의 전원전압을 내부전압으로 변환하기 위한 제2전위변환기; 및

상기 제2전위변환기의 출력을 게이트단으로 입력받아 내부전압을 공급전압으로 전달하기 위한 제2피모스트랜지스터

를 포함하여 이루어진 것을 특징으로 하는 지연고정루프.

청구항 9.

제 8 항에 있어서,

상기 제1전위변환기는,

상기 펌프제어신호를 입력받아 고전압으로 변환하는 차동증폭기; 및

상기 차동증폭기의 출력을 반전하며 고전압을 풀-업하는 인버터

를 포함하여 이루어진 것을 특징으로 하는 지연고정루프.

청구항 10.

제 8 항에 있어서,

상기 제2전위변환기는,

상기 인버터의 출력을 입력받아 내부전압으로 변환하는 차동증폭기; 및

상기 차동증폭기의 출력을 반전하며 내부전압을 풀-업하는 인버터

를 포함하여 이루어진 것을 특징으로 하는 지연고정루프.

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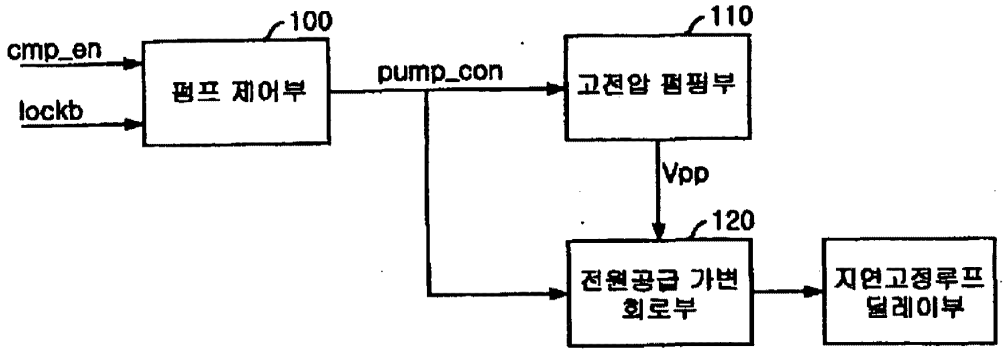
도면

도면 1



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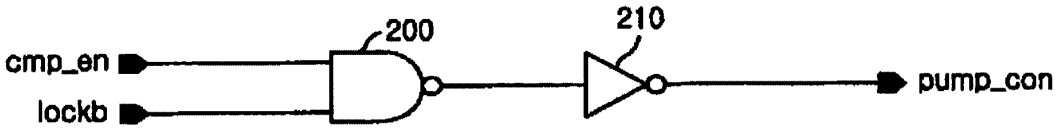

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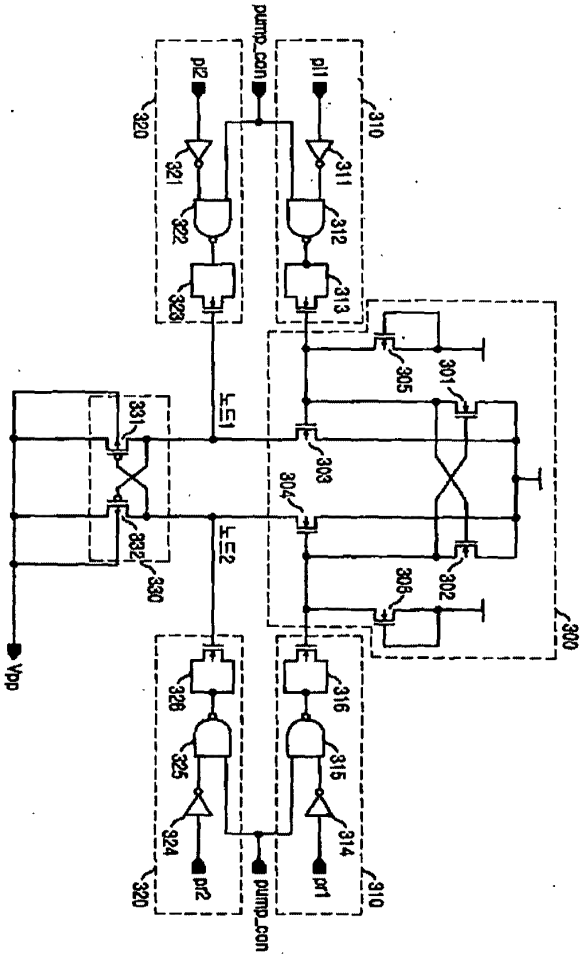
도면 3



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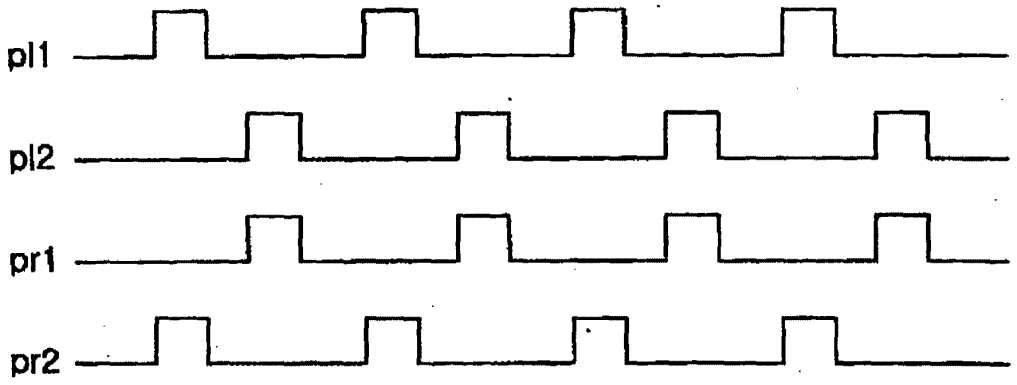
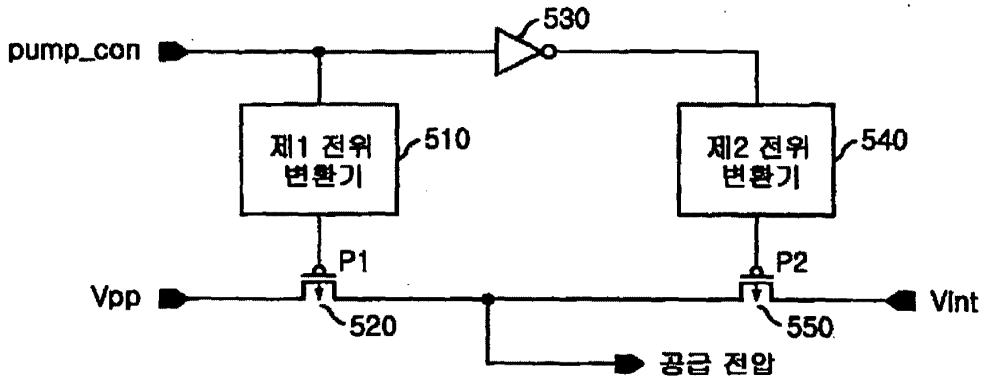
도면 4



도면 5



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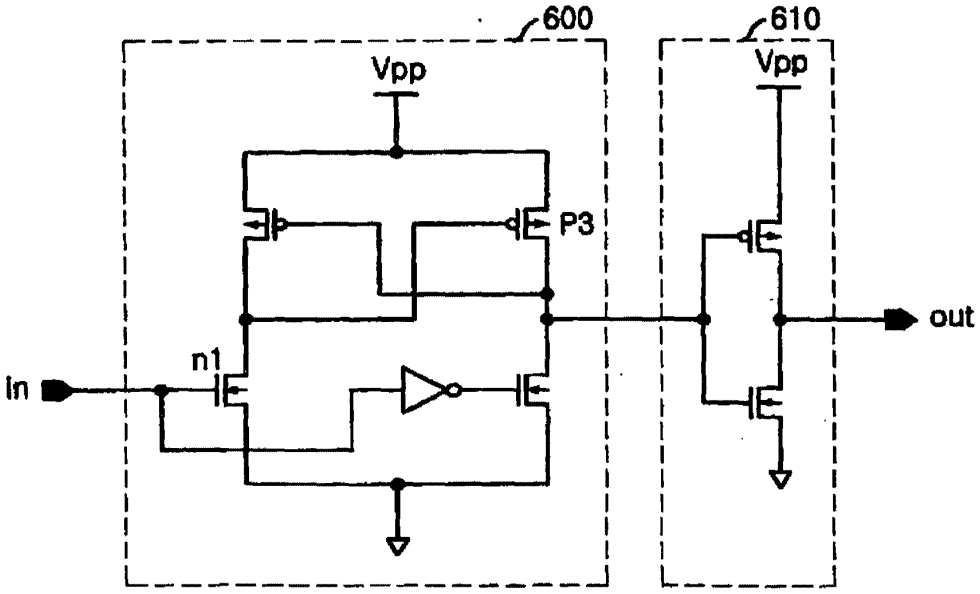
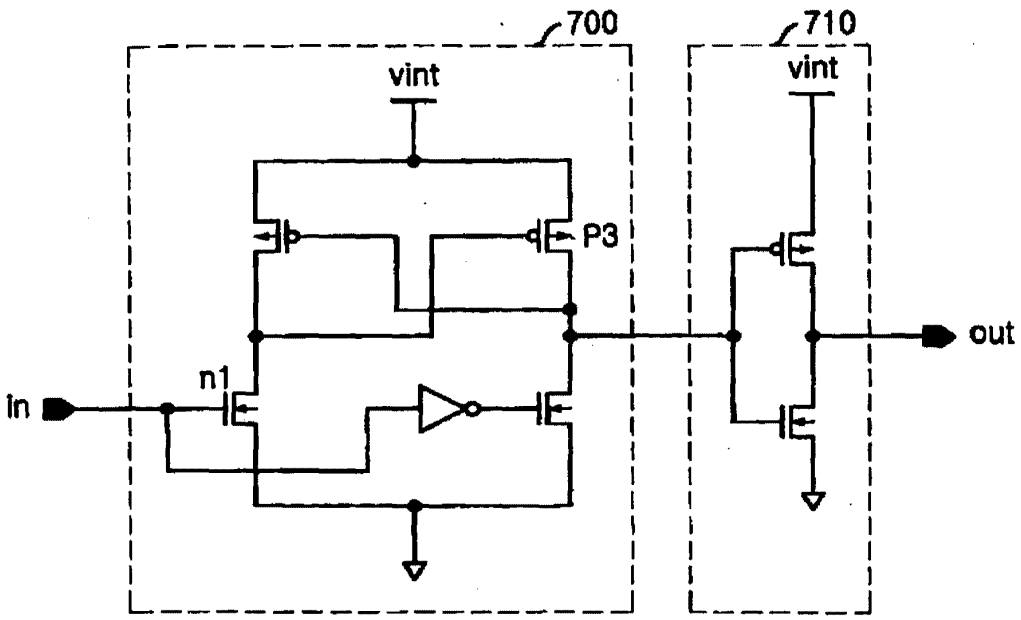
도면 6



PAGE 18/19 * RCVD AT 3/29/2005 4:30:46 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/7 * DNIS:8729306 * CSID:5032744622 * DURATION (mm-ss):07-38

도면 7



PAGE 19/19 * RCVD AT 3/29/2005 4:30:46 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/7 * DNIS:8729306 * CSID:5032744622 * DURATION (mm-ss):07-38

PATENT APPLICATION
Docket No. 4591-380
Client Ref. No. ID13095-US

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE**, the specification of which:

- ☒ is attached hereto.
- ☐ was filed on _____ as Application No. _____
- ☐ and was amended on _____(if applicable)
- ☐ with amendments through _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information that is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Sec. 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Sec. 119 (a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Claiming Priority?	
2003-46799	**Republic of Korea**	**10 July 2003**	☒	☐
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Sec. 119(e) of any United States provisional application listed below: **NONE.**

EXHIBIT A

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PAGE 3/10 * RCVD AT 10/13/2004 5:46:51 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729308 * CSID:5032744622 * DURATION (mm-ss):03-54

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I hereby claim the benefit under Title 35, United States Code, Sec. 120 or §365(c) of any PCT international application designating the United States of America listed below and, insofar as the subject mat ter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Sec. 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Sec. 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application: **NONE.**

I hereby appoint the following at torneys to prosecute the application, to file a corresponding international application, to prosecute and transact all business in the Patent and Trademark Office connected therewith:

Customer No. 20575

Attorney Name	**Registration No.**
Elmer W. Galbi	19,761
Jerome S. Marger	26,480
Alexander C. Johnson, Jr.	29,396
Alan T. McCollom	28,881
Stephen S. Ford	35,139
Julie L. Reed	35,349
Scott A. Schaffer	38,610
Joseph S. Makuch	39,286
James E. Harris	40,013
Kevin S. Ross	42,116
Graciela G. Cowger	42,444
Ariel Rogson	43,054
Craig R. Rogers	43,888
Hillary Brooks	45,815
Clifford D. Weston	48,307
Todd J. Iverson	53,057

Direct all telephone calls to Alan T. McCollom at (503) 222-3613 and send all correspondence to:

Alan T. McCollom
MARGER JOHNSON & McCOLLOM, P.C.
1030 S.W. Morrison Street
Portland, Oregon 97205
(503) 222-3613

PAGE 4/10 * RCVD AT 10/13/2004 5:46:51 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:5032744622 * DURATION (mm-ss):03-54

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; a nd further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statement s may jeopardize the validity of the application or any patent issued thereon.

Full name of first inventor: Pyung-Moon Zhang

Inventor's signature: Pyung-Moon Zhang 2 July 2004 (Date)

Residence: Gyeonggi-do, Republic of Korea

Citizenship: Republic of Korea

Post Office address: 8096Ho, Maronie-dong, Men's Dormitory, Samsung Electronics Co., Ltd., Giheung-factory, Giheung-eup, Yongin-si, Gyeonggi-do, Republic of Korea

Full name of second inventor: Seung-Keun Lee

Inventor's signature: Seung-keun Lee 2 July 2004 (Date)

Residence: Gyeonggi-do, Republic of Korea

Citizenship: Republic of Korea

Post Office address: 505-1204 Seongji-do Apt., Sinjeong-maeul, Pungdeokcheon-ri, Suji-eup, Yongin-si, Gyeonggi-do, Republic of Korea

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PATENT APPLICATION
Docket No. 4591-380
Client No. ID13095US

ASSIGNMENT

U.S.A. Patent Application
Sole or Joint
For Inventions Made Outside U.S.A.
Executed With Application

In consideration of the sum of Ten Dollars (10.00) and other good and valuable considerations paid to each of the undersigned, to wit:

(1) **Pyung-Moon Zhang**
(2) **Seung-Keun Lee**

☐ X if continued on separate page

the receipt and sufficiency of which are hereby acknowledged by the undersigned who hereby sell(s), assign(s) and transfer(s) unto:

SAMSUNG ELECTRONICS CO., LTD.
416 MAETAN-DONG, YEONGTONG-GU
SUWON-CITY, KYUNGKI-DO
REPUBLIC OF KOREA

(hereinafter designated "ASSIGNEE") the entire right, title and interest in and to the invention as defined in 35 USC §100, for the United States of America, the invention entitled:

CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE

for which an application for Letters Patent of the United States of America has been executed even date herewith by the undersigned, and in and to any and a ll divisionals, continuations, substitutes, and reissues thereof; and all resulting patents and the undersigned hereby authorizes and requests the United States Assistant Commissioner of Patents to issue said Letters Patent to the said ASSIGNEE, for its in terest as ASSIGNEE, its successors, assigns and legal representatives; the undersigned agrees that the attorneys of record in said application shall hereafter act on behalf of said ASSIGNEE;

And the undersigned hereby agrees to testify and execute any pap ers for ASSIGNEE, its successors, assigns and legal representatives, deemed essential by ASSIGNEE to ASSIGNEE'S full protection and title in and to the invention hereby transferred.

PAGE 6/10 * RCVD AT 10/13/2004 5:46:51 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:5032744622 * DURATION (mm-ss):03-54

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Please sign
concurrently
with Oath or Declaration
and Power of Attorn ey

SIGNED ON THE DATES INDICATED BESIDE OUR SIGNATURES:

INVENTOR(S)	DATE SIGNED	WITNESSED
(1) Pyung-Moon Zhang **Pyung-Moon Zhang**	2 July 2004	Bram LEE
(2) Seung-keun Lee **Seung-Keun Lee**	2 July 2004	at Kim Bo-Geun

PLEASE RETURN RECORDED ASSIGNMENT TO:

Alan T. McCollom
Marger Johnson & McCollom
1030 S.W. Morrison Street
Portland, OR 97205

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Washington, D.C. 20231

700117161A

SEPTEMBER 24, 2004

PTAS

MARGER JOHNSON & MCCOLLOM, P.C.
GRACIELA G. COWGER
1030 S.W. MORRISON STREET
PORTLAND, OREGON 97205

UNITED STATES PATENT AND TRADEMARK OFFICE
NOTICE OF RECORDATION OF ASSIGNMENT DOCUMENT

THE ENCLOSED DOCUMENT HAS BEEN RECORDED BY THE ASSIGNMENT DIVISION OF THE U.S. PATENT AND TRADEMARK OFFICE. A COMPLETE MICROFILM COPY IS AVAILABLE AT THE ASSIGNMENT SEARCH ROOM ON THE REEL AND FRAME NUMBER REFERENCED BELOW.

PLEASE REVIEW ALL INFORMATION CONTAINED ON THIS NOTICE. THE INFORMATION CONTAINED ON THIS RECORDATION NOTICE REFLECTS THE DATA PRESENT IN THE PATENT AND TRADEMARK ASSIGNMENT SYSTEM. IF YOU SHOULD FIND ANY ERRORS OR HAVE QUESTIONS CONCERNING THIS NOTICE, YOU MAY CONTACT THE EMPLOYEE WHOSE NAME APPEARS ON THIS NOTICE AT 703-308-9723. PLEASE SEND REQUEST FOR CORRECTION TO: U.S. PATENT AND TRADEMARK OFFICE, ASSIGNMENT DIVISION, BOX ASSIGNMENTS, CG-4, 1213 JEFFERSON DAVIS HWY, SUITE 320, WASHINGTON, D.C. 20231.

RECORDATION DATE: 09/22/2004 REEL/FRAME: 015168/0071
NUMBER OF PAGES: 3

BRIEF: ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS).
DOCKET NUMBER: 4591-380

ASSIGNOR:
ZHANG, PYUNG-MOON DOC DATE: 07/08/2004

ASSIGNOR:
LEE, SEUNG-KEUN DOC DATE: 07/08/2004

ASSIGNEE:
SAMSUNG ELECTRONICS CO., LTD.
416 MAETAN-DONG, YEONGTONG-GU
SUWON-CITY, KYUNGKI-DO
REPUBLIC
OF KOREA

SERIAL NUMBER: 10888667 FILING DATE: 07/08/2004
PATENT NUMBER: ISSUE DATE:
TITLE: CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE

EXHIBIT
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015168/0071 PAGE 2

ALLYSON PURNELL, EXAMINER
ASSIGNMENT DIVISION
OFFICE OF PUBLIC RECORDS

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09/22/2004
700117161

PATENT APPLICATION
Docket No. 4591-380
Client Ref. No. ID13095US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Mail Stop Assignment Recordation Services
Director of the U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Please record the attached original document or copy thereof and return the recorded instrument to the undersigned.

1. Name of parties conveying an interest: Pyung-Moon Zhang, and Seung-Keun Lee

2. Name and address of party(ies) receiving an interest: Samsung Electronics Co., Ltd.
416 Maetan-dong, Yeongtong-gu, Suwon-City
Kyungki-do, Republic of Korea

3. Description of the interest conveyed:

☒ Assignment ☐ Change of Name ☐ Security Agreement ☐ Merger

Date of execution of attached document: July 2, 2004

4. Application number(s) or patent number(s). Additional sheet attached? Yes___ No__X__.

If this document is being filed together with a new application, the execution date of the application is:

A. Patent Application No. 10/888,667 Filing Date: July 8, 2004

5. Name and address of party to whom correspondence concerning document should be mailed:

MARGER JOHNSON & McCOLLOM, P.C.
1030 S.W. Morrison Street
Portland, Oregon 97205
Telephone: (503) 222-3613

I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number 703-306-5995, on September 22, 2004.
Angie C. Farr

6. Number of applications and patents involved: 1

7. PTO Form 2038 authorizing credit card payment ($40) is enclosed.

8. Any deficiency or overpayment should be charged or credited to deposit account number 13-1703.

9. To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Dated: September 22, 2004

Respectfully submitted,
MARGER JOHNSON & McCOLLOM, P.C.

Graciela G. Cowger
Reg. No. 42,444

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
(503) 222-3613

Total number of pages comprising cover sheet and attached assignment: 3

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Certificate of Facsimile Transmission
I hereby certify that the REQUEST FOR ASSOCIATION OF CUSTOMER NO 20575 WITH COMBINED DECLARATION AND POWER OF ATTORNEY AND CORRESPONDENCE ADDRESS, copy of Combined Declaration and Power of Attorney (Exhibit A), Assignment (Exhibit B), and Notice of Recordation (Exhibit C) is being facsimile transmitted to the Patent and Trademark Office (Fax No. (703) 872-9306) on the date shown below. (Total pages transmitted are 10, including this one).

Dated: October 13, 2004

Lisbeth A. Nichols

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CENTRAL FAX CENTER
OCT 13 2004

PATENT APPLICATION
Attorney Docket No. 4591-380
Client No. ID13095-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Pyung-Moon ZHANG and Seung-Keun LEE		
Serial No.:	10/888,667	Art Unit:	2816
Filed:	July 8, 2004	Examiner:	Not yet assigned
For:	CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE		
Confirmation No.	4240		

REQUEST FOR ASSOCIATION OF CUSTOMER NO 20575 WITH COMBINED DECLARATION AND POWER OF ATTORNEY AND CORRESPONDENCE ADDRESS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

The undersigned previously submitted to the Patent Office a Combined Declaration and Power of Attorney executed by the inventors in the above-referenced application. The Combined Declaration and Power of Attorney was prepared before the revision of the Power of Attorney rules on June 25, 2004 and therefore listed more than ten registered patent practitioners along with an indication of our **Customer No. 20575**.

A copy of the Combined Declaration and Power of Attorney previously submitted (Exhibit A), Assignment (Exhibit B), and Notice of Recordation (Exhibit C) recorded on September 22, 2004, in Reel/Frame 015168/0071 are attached.

Pursuant to 37 CFR 1.32(c), applicant requests that the above-referenced application be associated with **Customer No. 20575**, rather than the individual-named attorneys, and that all correspondence be sent to the following address associated with **Customer No. 20575**.

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Applicant requests that your office reissue a corrected filing receipt incorporating the Power of Attorney associated with our customer number.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Graciela G. Cowger
Reg. No. 42,444

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
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Index of Claims

Application No.	Applicant(s)
10888667	
Examiner	**Art Unit**

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date	Claim		Date	Claim		Date
Final	Original		Final	Original		Final	Original	
	1			51			101	
	2			52			102	
	3			53			103	
	4			54			104	
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	34			84			134	
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	36			86			136	
	37			87			137	
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	44			94			144	
	45			95			145	
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	47			97			147	
	48			98			148	
	49			99			149	
	50			100			150	

OIPE JC13 SEP 27 2004 PATENT & TRADEMARK OFFICE

IFW

PATENT APPLICATION
Docket No. 4591-380
Client No. ID13095US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	Pyung-Moon Zhang, et al.	Conf. No.	4240
Serial No.:	10/888,667	Examiner:	Not yet assigned
Filing Date:	July 8, 2004	Art Unit:	2816
Title:	CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER

Enclosed for filing in the above-referenced application are the following:

☒ Certified Copy of Priority Document No. 10-2003-0046799, filed July 10, 2003.
☒ Return Postcard.
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Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450
Date: September 22, 2004
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대 한 민 국 특 허 청
KOREAN INTELLECTUAL PROPERTY OFFICE

별첨 사본은 아래 출원의 원본과 동일함을 증명함.

This is to certify that the following application annexed hereto is a true copy from the records of the Korean Intellectual Property Office.

출 원 번 호 : 10-2003-0046799
Application Number

CERTIFIED COPY OF PRIORITY DOCUMENT

출 원 년 월 일 : 2003년 07월 10일
Date of Application JUL 10, 2003

출 원 인 : 삼성전자주식회사
Applicant(s) SAMSUNG ELECTRONICS CO., LTD.

2004 년 01 월 15 일

특 허 청
COMMISSIONER

【서지사항】

【서류명】	특허출원서
【권리구분】	특허
【수신처】	특허청장
【참조번호】	0003
【제출일자】	2003.07.10
【발명의 명칭】	선택 모드를 갖는 전하 펌프 회로
【발명의 영문명칭】	CHARGE PUMP CIRCUIT HAVING SELECT MODE
【출원인】	
【명칭】	삼성전자 주식회사
【출원인코드】	1-1998-104271-3
【대리인】	
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【대리인코드】	9-1998-000386-5
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【대리인】	
【성명】	권혁수
【대리인코드】	9-1999-000370-4
【포괄위임등록번호】	1999-056971-6
【발명자】	
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【성명의 영문표기】	ZHANG,PYUNG-MOON
【주민등록번호】	720826-1637610
【우편번호】	449-711
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【우편번호】	449-846

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【주소】	경기도 용인시 수지읍 풍덕천리 신정마을 성지아파트 505동 1204호
【국적】	KR
【심사청구】	청구
【취지】	특허법 제42조의 규정에 의한 출원, 특허법 제60조의 규정에 의한 출원심사 를 청구합니다. 대리인 임창현 (인) 대리인 권혁수 (인)
【수수료】	
【기본출원료】	20 면 29,000 원
【가산출원료】	4 면 4,000 원
【우선권주장료】	0 건 0 원
【심사청구료】	15 항 589,000 원
【합계】	622,000 원
【첨부서류】	1. 요약서·명세서(도면)_1통

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【요약서】

【요약】

본 발명은 일반 동작 모드와 테스트 동작 모드에서 동시에 사용가능하도록 한 전하 펌프 회로에 관한 것이다. 본 발명에 따른 전하 펌프 회로는 차지 펌프부와; 상기 차지 펌프부의 출력전압의 레벨을 감지하기 위한 레벨 감지부와; 상기 레벨 감지부의 레벨 감지신호에 따라 펄스신호들을 발생하는 오실레이터와; 전원전압과 외부 고전압 중에서 어느 하나를 선택하는 선택기와; 상기 선택기에 검출신호를 보내는 검출기를 포함하는 것을 특징으로 한다. 상기 전하 펌프 회로에 의하면 짧은 시간 동안에 원하는 출력전압을 얻을 수 있다.

【대표도】

도 4

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【명세서】

【발명의 명칭】

선택 모드를 갖는 전하 펌프 회로{CHARGE PUMP CIRCUIT HAVING SELECT MODE}

【도면의 간단한 설명】

도 1은 종래의 전하 펌프 회로의 구성을 나타낸 블록도이다.

도 2는 도 1의 레벨 감지부를 구체적으로 나타낸 회로도이다.

도 3은 도 1의 오실레이터를 구체적으로 나타낸 회로도이다.

도 4는 본 발명에 따른 전하 펌프 회로의 구성을 나타낸 블록도이다.

도 5는 도 4의 차지 펌프부의 구체적 실시예를 나타낸 회로도이다.

도 6은 도 4의 선택기의 구체적 실시예를 나타낸 회로도이다.

도 7은 도 4의 검출기의 구체적 실시예를 나타낸 회로도이다.

도 8은 본 발명에 따른 전하 펌프 회로의 출력전압의 파형을 나타낸 그래프이다.

* 도면의 주요 부분에 대한 부호 설명 *

100 : 차지 펌프부	110 : 전하 공급단
120 : 제 1 차지 펌프단	130 : 제 2 차지 펌프단
140 : 제 3 차지 펌프단	150 : 제 n 차지 펌프단
160 : 전하 저장단	200 : 선택 회로부
210 : 선택기	220 : 검출기
300 : 오실레이터	400 : 레벨 감지부

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【발명의 상세한 설명】

【발명의 목적】

【발명이 속하는 기술분야 및 그 분야의 종래기술】

<16> 본 발명은 고전압 발생 회로에 관한 것으로, 좀 더 구체적으로는 전원전압과 외부 고전압 중에서 어느 하나를 선택하여 사용할 수 있는 전하 펌프 회로에 관한 것이다.

<17> 도 1은 종래의 전하 펌프 회로의 개략적인 구성을 나타낸 블록도이다. 도 1에 도시된 바와 같이 종래의 전하 펌프 회로는, 출력전압(Vout)의 레벨을 검출하는 레벨 감지부와, 펄스신호들(PUL, /PUL)을 발생하는 오실레이터와, 펌핑 동작을 수행하는 차지 펌프부로 구성된다.

<18> 상기 레벨 감지부는 도 2에 도시된 바와같이 차동 증폭기로 구성된다. 상기 레벨 감지부는 펌핑 인에이블신호(enPUMP)에 의해 동작되며, 출력전압(Vout)을 기준전압(Vref)과 비교하여, 그 결과로서 레벨 감지신호(DET)를 발생한다.

<19> 상기 오실레이터는 도 3에 도시된 바와같이 하나의 NOR 게이트(G1)와 4개의 인버터들(INV1, INV2, INV3, INV4)로 구성된다.상기 레벨 감지부에서 발생된 레벨 감지신호(DET)에 응답하여 동작하며, 그 결과로서 상보적 관계에 있는 펄스신호들 (PUL, /PUL)을 발생한다.

<20> 상기 차지 펌프부는 전하 공급단과 복수개의 차지 펌프단들로 구성된다. 상기 전하 공급단은 외부전압(Vcc)을 인가 받아 제 1 차지 펌프단(PS1)에 전하를 공급한다. 상기 차지 펌프단들(PS1, PS2, PS3,… PSn)은 상기 전하 공급단과 출력단자 사이에 직렬로 연결되며, 상기 전하 공급단에서 공급된 전하를 펌핑하여 원하는 출력전압(Vout)을 발생한다. 복수 개의 펌프단들 중 홀수번째(또는 짝수번째) 펌프단들은 펄스신호(PUL)에 응답하여 동작하고, 짝수번째(또는 홀수번째) 펌프단들은 펄스신호(/PUL)에 응답하여 동작한다.

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<21> 상술한 종래의 전하 펌프 회로의 동작 과정을 설명하면 다음과 같다. 레벨 감지부는 펌핑 인에이블신호(enPUMP)가 '하이'상태가 될 때 출력전압(Vout)과 기준전압(Vref)을 비교하여 출력전압(Vout)의 레벨을 감지한다. 즉, 기준전압(Vref)이 출력전압(Vout)보다 크면 상기 레벨 감지부는 '하이'상태의 레벨 감지신호(DET)를 발생하고, 출력전압(Vout)이 기준전압(Vref)보다 크면 '로우'상태의 레벨 감지신호(DEF)를 발생한다. 상기 오실레이터는 레벨 감지신호(DET)에 응답하여 그 결과로서 상기 차지 펌프단들(PS1, PS2, PS3,… PSn)을 동작시킨다. 즉, 레벨 감지신호(DET)가 '하이'상태이면, 상기 차지 펌프단들(PS1, PS2, PS3,… PSn)을 모두 동작시켜 출력전압(Vout)의 레벨을 증가시키고, 레벨 감지신호(DET)가 '로우'상태이면, 차지 펌프단들(PS1, PS2, PS3,… PSn)을 모두 정지시켜 출력전압(Vout)의 레벨을 감소시킨다.

<22> 종래의 전하 펌프 회로는 전하 공급단 및 차지 펌프단들의 각 노드에 외부전압(Vcc)에 상응하는 전하를 프리차지 한 후 펌핑 동작을 수행한다. 따라서 얻고자 하는 출력전압(Vout)이 높을수록 전하 펌프 회로가 동작하는데 많은 시간이 소요된다. 특히 칩을 테스트 하는 과정에서 짧은 시간 내에 고전압을 얻을 수 있어야 하는데, 상기한 종래의 전하 펌프 회로만으로는 한계가 있다. 따라서 일반 동작 모드에서 뿐만아니라 칩을 테스트 하는 테스트 동작 모드에서 짧은 시간 내에 고전압을 얻을 수 전하 펌프 회로가 요구된다.

【발명이 이루고자 하는 기술적 과제】

<23> 본 발명은 상술한 기술적 과제를 해결하기 위해 안출된 것으로, 본 발명의 목적은 일반 동작 모드에서 뿐만아니라 짧은 시간 내에 고전압을 필요로 하는 테스트 동작 모드에서도 사용 가능한 전하 펌프 회로를 제공하는 것이다.

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【발명의 구성 및 작용】

<24> 상기와 같은 본 발명이 이루고자 하는 기술적 과제를 달성하기 위한 본 발명에 따른 전하 펌프 회로는, 적어도 하나 이상의 차지 펌프단들을 포함하는 차지 펌프부와, 동작 모드에 따라 가변 가능한 프리차지 전압을 상기 차지 펌프단들로 공급하는 전압 공급 회로를 포함하는 것을 특징으로 한다.

<25> 이 실시예에 있어서, 일반 동작 모드시, 상기 전압 공급 회로는 상기 프리차지 전압으로서 전원전압(Vcc)을 공급하는 것을 특징으로 한다.

<26> 이 실시예에 있어서, 테스트 동작 모드시, 상기 전압 공급 회로는 상기 프리차지 전압으로서 상기 전원전압(Vcc)보다 높은 고전압(Vpp)을 공급하는 것을 특징으로 한다.

<27> 본 발명에 따른 전하 펌프 회로의 다른 일면은, 적어도 하나 이상의 차지 펌프단들을 포함하여 구성된 차지 펌프부와, 상기 차지 펌프부의 출력전압(Vout)의 레벨을 감지하여 레벨 감지 신호(DET)를 발생하는 레벨 감지부와, 상기 레벨 감지신호(DET)에 응답하여 펄스신호들(PUL, /PUL)을 발생하는 오실레이터와, 그리고 전원전압(Vcc)보다 높은 고전압(Vpp)을 선택하여 상기 차지 펌프부에 상기 선택된 고전압(Vpp)을 공급할 수 있는 선택 회로부를 포함하는 것을 특징으로 한다.

<28> 이 실시예에 있어서, 상기 차지 펌프부는, 상기 선택된 고전압(Vpp)에 해당하는 전하를 프리차지하여 상기 프리차지한 전하를 공급하는 전하 공급단과, 상기 전하 공급단에서 공급된 전하를 각각 펌핑하는 차지 펌프단들과, 그리고 상기 차지 펌프단들에서 펌핑된 전하를 최종적으로 저장하는 전하 저장단을 포함하되, 상기 차지 펌프단들은 상기 선택된 고전압(Vpp)에 상응하는 전하를 프리차지할 수 있는 프리 차지 수단들을 구비한 것을 특징으로 한다.

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<29> 이 실시예에 있어서, 상기 전하 공급단은 고전압 PMOS 트랜지스터(P110)를 포함하여 구성된 것을 특징으로 한다.

<30> 이 실시예에 있어서, 상기 프리 차지 수단들은 각각의 상기 차지 펌프단들에 연결된 각각의 고전압 NMOS 트랜지스터들(N120, N130, N140, N150)을 포함하여 구성된 것을 특징으로 한다.

<31> 이 실시예에 있어서, 상기 전하 공급단의 출력단 전압은 상기 선택된 고전압(Vpp)이고, 상기 차지 펌프단들의 출력단들에 프리차지된 전압은 상기 선택된 고전압(Vpp)전압에서 상기 각각의 고전압 NMOS 트랜지스터들(N120, N130, N140, N150)의 드레솔드 전압(Vth)을 뺀 전압(Vpp-Vth)인 것을 특징으로 한다.

<32> 이 실시예에 있어서, 상기 선택 회로부는 상기 전원전압(Vcc)과 상기 고전압(Vpp)를 비교하여, 상기 고전압(Vpp)이 상기 전원 전압(Vcc)보다 높을 경우에, 상기 고전압(Vpp)을 선택하는 것을 특징으로 한다.

<33> 또한 본 발명에 따른 전하 펌프 회로의 또 다른 일면은, 적어도 하나 이상의 차지 펌프단들을 포함하여 구성된 차지 펌프부와, 상기 차지 펌프부의 출력전압(Vout)의 레벨을 감지하여 레벨 감지 신호(DET)를 발생하는 레벨 감지부와, 상기 레벨 감지신호(DET)에 응답하여 펄스 신호들(PUL, /PUL)을 발생하는 오실레이터와, 외부에서 인가되는 고전압(Vpp)이 일정 전압 이상일 경우에 '하이'인 검출신호(Vdet)를 발생하는 검출기와, 그리고 상기 '하이'인 검출신호(Vdet)에 응답하여 상기 고전압(Vpp)을 선택한 후 상기 선택된 고전압(Vpp)을 상기 차지 펌프부에 공급하는 선택기를 포함하는 것을 특징으로 한다.

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<34> 이 실시예에 있어서, 상기 차지 펌프부는, 상기 선택된 고전압(Vpp)에 해당하는 전하를 프리차지하여 상기 프리차지한 전하를 공급하는 전하 공급단과, 상기 전하 공급단에서 공급된 전하를 각각 펌핑하는 차지 펌프단들과, 그리고 상기 차지 펌프단들에서 펌핑된 전하를 최종적으로 저장하는 전하 저장단을 포함하되, 상기 차지 펌프단들은 상기 선택된 고전압(Vpp)에 상응하는 전하를 프리차지할 수 있는 프리 차지 수단들을 구비한 것을 특징으로 한다.

<35> 이 실시예에 있어서, 상기 전하 공급단은 고전압 PMOS 트랜지스터(P110)를 포함하여 구성된 것을 특징으로 한다.

<36> 이 실시예에 있어서, 상기 프리 차지 수단들은 각각의 상기 차지 펌프단들에 연결된 각각의 고전압 NMOS 트랜지스터들(N120, N130, N140, N150)을 포함하여 구성된 것을 특징으로 한다.

<37> 이 실시예에 있어서, 상기 전하 공급단의 출력단 전압은 상기 선택된 고전압(Vpp)이고, 상기 차지 펌프단들의 출력단들에 프리차지된 전압은 상기 선택된 고전압(Vpp)전압에서 상기 각각의 고전압 NMOS 트랜지스터들(N120, N130, N140, N150)의 드레솔드 전압(Vth)을 뺀 전압(Vpp-Vth)인 것을 특징으로 한다.

<38> 이 실시예에 있어서, 상기 검출기는 상기 고전압(Vpp)을 입력받아 동작하며, 상기 고전압(Vpp)이 전원전압(Vcc) 이상일 경우에, '하이'의 검출신호(Vdet)를 발생하는 것을 특징으로 한다.

<39> 본 발명에 따른 전하 펌프 회로에 의하면, 종래 기술의 전하 펌프 회로와 같이 전하 펌프부에 전원전압(Vcc)만을 공급하지 않고, 외부의 고전압(Vpp)을 공급함으로써 보다 빠르게 원

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하는 고전압을 얻을 수 있다. 그리고 칩 테스트시에 빠르게 고전압을 얻을 수 있어 칩의 테스트 타임을 줄일 수 있다.

<40> 이하, 첨부 도면을 참조하여 본 발명의 바람직한 실시예를 상세히 설명한다.

<41> 도 4는 본 발명에 따른 전하 펌프 회로의 전체적인 구성을 나타내는 블록도이다. 도 4를 참조하면, 본 발명에 따른 전하 펌프 회로는 차지 펌프부(100)와 선택 회로부(200)와 오실레이터(300)와 레벨 감지부(400)를 포함하여 구성된다.

<42> 상기 차지 펌프부(200)는 전하 공급단(110)과 복수개의 차지 펌프단들(120, 130, 140, 150)과 전하 저장단(160)이 직렬로 연결된다.

<43> 상기 전하 공급단(110)은 상기 선택 회로부(200)에서 선택된 전압(Vsel)에 해당하는 전하를 제 1 차지 펌프단(120)에 공급한다. 상기 차지 펌프단들(120, 130, 140, 150)은 상기 선택전압(Vsel)에 상응하는 전하를 프리차지함과 동시에 상기 전하 공급단에서 넘어온 전하를 각각 다음 단으로 펌핑한다. 상기 전하 저장단(160)은 상기 차지 펌프단들(120, 130, 140, 150)을 각각 거치면서 펌핑된 전하들을 최종적으로 저장하여 출력전압(Vout)을 발생한다. 상기 전하 펌프부(100)를 구성하는 각각의 블록들에 대한 대표적인 실시예는 후술되는 도 5를 참조하여 상세히 기술된다.

<44> 상기 레벨 감지부(400)는 펌핑 인에이블신호(enPUMP)가 '하이'상태가 될 때 출력전압(Vout)의 레벨을 감지한다. 즉, 출력전압(Vout)이 기준전압보다 작으면 '하이'상태의 레벨 감지신호(DET)를 발생하고, 출력전압(Vout)이 기준전압보다 크면 '로우'상태의 레벨 감지신호(DEF)를 발생한다.

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<45> 상기 오실레이터(300)는 레벨 감지신호(DET)에 응답하여 펄스신호(PUL,/PUL)를 발생한다. 레벨 감지신호(DET)가 '하이'상태이면 상기 차지 펌프단들(120, 130, 140, 150)을 모두 동작시켜 출력전압(Vout)의 레벨을 증가시키고, 레벨 감지신호 (DET)가 '로우'상태이면 상기 차지 펌프단들(120, 130, 140, 150)을 모두 정지시킨다.

<46> 계속해서 도 4를 참조하면, 본 발명에 따른 전하 펌프 회로는, 도 1의 종래 기술과 비교하여, 선택 회로부(200)를 더 구비한다. 상기 선택 회로부(200)는 선택기(210)와 검출기(220)로 구성됨으로써 더 잘 구현될 수 있다. 본 명세서에서는 설명의 편의를 위해 일반 동작 모드에서 동작하는 전원전압 즉 동작전압을 Vcc로 표시하고, 테스트 동작 모드시에 외부에서 공급되는 고전압을 Vpp로 표시한다. 다만, 고전압(Vpp)이 반드시 테스트 동작 모드일 경우에만 외부에서 공급되는 것으로 한정하는 것은 아니며 일반 동작 모드일 경우에도 공급될 수 있다.

<47> 상기 선택 회로부(200)는 상기 전원전압(Vcc)과 상기 고전압(Vpp) 중에서 어느 하나를 선택할 수 있는 선택기(210)와 상기 고전압(Vpp)의 레벨을 검출하여 검출신호(Vdet)를 발생하는 검출기(220)로 구성된다. 상기 검출기(220)는 상기 고전압(Vpp)이 상기 전원전압(Vcc)보다 높을 경우에 '하이'레벨의 검출신호(Vdet)를 발생한다. 이때 상기 선택기(210)는 상기 전원전압(Vcc)에서 상기 고전압(Vpp)으로 스위칭되어 상기 고전압(Vpp)을 발생한다. 즉 일반 동작 모드일 경우에 Vsel = Vcc 가 되고, 고전압을 요하는 테스트 동작 모드일 경우에 Vsel = Vpp 가 되어 빠른 시간 안에 원하는 고전압을 얻을 수 있다. 상기 선택기(210) 및 상기 검출기(220)의 구체적인 설명은 후술하는 도6 및 도 7을 참조하여 기술된다.

<48> 도 5는 도 4의 차지 펌프부(100)를 구체적으로 나타내는 회로도이다. 도 5를 참조하여, 상기 차지 펌프부(100)의 구성 및 동작 원리를 기술하면 다음과 같다.

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<49> 상기 차지 펌프부(100)는 전하 공급단(110)과 차지 펌프단들(120, 130, 140, 150)과 전하 저장단(160)으로 구성된다.

<50> 상기 전하 공급단(110)은 일반 동작 모드와 테스트 동작 모드에서 동시에 사용 가능하도록 고전압 PMOS(High Voltage PMOS) 트랜지스터로 구성된다. 상기 고전압 PMOS 트랜지스터는 노드(1)과 노드(2) 사이에 연결된다. 상기 고전압 PMOS 트랜지스터의 소스 단자와 벌크 단자는 노드(1)에 연결되고, 드레인 단자는 노드(2)에 연결되며, 게이트는 그라운드(GND)로 연결된다. 상기 전하 공급단(110)은 전하 공급 소자로 사용되며, 다음 단에 위치한 제 1 차지 펌프단(120)에 전하를 공급한다. 예를 들면, 일반 동작 모드에서 Vsel = Vcc 이면 노드(2)의 전압은 전원전압(Vcc)에 상응하는 전하들이 프리차지된다. 테스트 동작 모드에서 Vsel = Vpp 이면 노드(2)의 전압은 고전압(Vpp)에 상응하는 전하들이 프리차지되어 전하 공급원으로 사용된다.

<51> 상기 차지 펌프단들(120, 130, 140, 150)은 각각 1개의 PMOS 트랜지스터와 1개의 캐패시터와 1개의 고전압 NMOS(High Voltage NMOS) 트랜지스터로 구성된다. 상기 고전압 NMOS 트랜지스터는 일반 동작 모드에서 뿐만 아니라 고전압이 요구되는 테스트 동작 모드에서도 사용하도록 하기 위함이다. 복수개의 차지 펌프단들 중 홀수번째(또는 짝수번째) 펌프단들은 펄스신호(PUL)에 응답하여 동작하고, 짝수번째(또는 홀수번째) 펌프단들은 펄스신호(/PUL)에 응답하여 동작한다.

<52> 본 명세서에서는 설명의 편의를 위하여 제 1 차지 펌프단(120)에 대해서만 설명한다. 하지만 나머지 펌프단들 역시 동일하게 설명된다. 전하 전달 소자로서 사용되는 PMOS 트랜지스터(P120)의 소스 단자는 노드(2)에 연결되고, 드레인 단자와 게이트 단자는 노드(3)에 연결되며, 벌크 단자는 플로우팅 상태에 있다. 전하 펌핑 소자로서 사용되는 커패시터(C120)

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는 노드(3)과 노드(8) 사이에 연결되며, 펄스신호(PUL)가 인가된다. 프리 차지 소자로서 사용되는 고전압 NMOS 트랜지스터(N120)의 게이트 단자와 드레인 단자는 노드(1)에 연결되고, 소스 단자는 노드(3)에 연결되며, 벌크는 그라운드(GND)에 연결된다. 상기 고전압 NMOS 트랜지스터는 노드(3)에 선택전압(Vsel)에 상응하는 전하를 프리차지한다. 예를 들면, 상기 고전압 NMOS 트랜지스터(N120)의 문턱전압이 Vth라면 Vsel-Vth에 상응하는 전하가 프리차지된다. 즉, 일반 동작 모드에서는 Vcc-Vth, 테스트 동작 모드에서는 Vpp-Vth에 상응하는 전하가 프리차지된다.

<53> 상기 전하 저장단(160)은 1개의 PMOS 트랜지스터(P160)와 1개의 커패시터로 구성된다. 여기서 상기 PMOS 트랜지스터(P160)는 전하 전달 소자로 사용되고, 커패시터(C160)는 전하 저장 소자로 사용되며, 최종적으로 출력전압(Vout)을 발생한다.

<54> 도 6은 도 4의 선택기(210)를 나타내는 회로도이다. 도 6을 참조하면, 상기 선택기(210)는 고전압(Vpp)을 제어하기 위하여 고전압 NMOS 트랜지스터들 (N211~N218)과 고전압 PMOS 트랜지스터들(P211~P218, P210_i;i=1~4) 및 2개의 인버터들로 구성된 레벨 쉬프터가 이용된다. 상기 레벨 쉬프터를 이용하면 전원전압(Vcc)과 고전압(Vpp) 중에서 어느 하나가 선택되어 상기 차지펌프부(100)에 공급된다. 예를 들면, 검출신호(Vdet)가 '하이'인 테스트 동작 모드에서는 고전압 NMOS 트랜지스터(N216, N217)는 턴온되므로 고전압 PMOS 트랜지스터(P210_3, P210_4)도 턴온된다. 따라서 Vsel = Vpp 가 된다. 그러나 상기 조건에서 고전압 NMOS 트랜지스터(N212, N213)는 턴오프되므로 고전압 PMOS 트랜지스터(P210_1, P210_2)도 턴-오프 된다. 따라서 Vsel ≠Vcc가 된다. 이와 반대로, 검출신호(Vdet)가 '로우'인 일반 동작 모드에서는 Vsel = Vcc 가 된다.

<55> 도 7은 도 4의 검출기(220)를 나타내는 회로도이다. 도 7을 참조하면, 상기 검출기(220)는 일반 동작 모드와 고전압을 요하는 테스트 동작 모드에서 동시에 사용할 수 있도록 고전압

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PMOS 트랜지스터 및 고전압 NMOS 트랜지스터들과 고전압 인버터(HV INV)와 저전압 인버터(LV INV)를 포함하여 구성된다. 예를 들어 설명하면, 외부 고전압(Vpp)이 전원전압(Vcc)보다 낮을 경우에는 A 노드의 전압은 Vcc-Vth 가 되어 PMOS(P221)는 오프된다. 이때 B 노드는 그라운드(GND)가 된다. 한편 고전압(Vpp)이 전원전압(Vcc) 보다 높을 경우에는 A 노드의 전압은 Vpp-Vth 가 된다. Vpp가 더욱 증가하면 B 노드는 충분히 높은 전압이 되어 고전압 인버터(HV INV)의 출력은 반전된다. 이 출력은 저전압 인버터(LV INV)를 통과하면서 '하이' 상태의 검출 신호(Vdet)를 발생한다.

<56> 도 8은 전원전압(Vcc)을 사용한 경우와 외부 고전압(Vpp)를 사용한 경우에 전하 펌프 회로에 대한 출력전압(Vout)의 파형을 비교하기 위한 그래프이다. 셋틀링 타임(Settling Time)은 원하는 출력전압(Vout)을 얻기까지 펌핑 동작을 하는데 소요되는 시간으로 정의된다. 도 8을 참조하면, 선택된 전압(Vsel)이 전원전압(Vcc = 1.8V)인 경우와 외부 고전압(Vpp = 8V) 인 경우에, 원하는 출력전압(Vout = 10V)에 도달하기 위한 셋틀링 타임(STp)에 있어서 약 4배의 차이가 있음을 알 수 있다. 즉, 전원전압(Vcc)을 공급할 때보다 외부의 고전압(Vpp)을 공급할 때 원하는 출력전압(Vout)에 더 빨리 도달할 수 있음을 보여준다.

【발명의 효과】

<57> 상술한 바와 같이, 본 발명에 따른 전하 펌프 회로는 차지 펌프부에 전원전압(Vcc) 대신에 외부의 고전압(Vpp)을 인가할 수 있는 선택 수단을 더 구비함으로써 원하는 출력전압(Vout)을 보다 짧은 시간 내에 얻을 수 있도록 한 것이다.

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【특허청구범위】

【청구항 1】

적어도 하나 이상의 차지 펌프단들을 포함하는 차지 펌프부와; 그리고 동작 모드에 따라 가변 가능한 프리차지 전압을 상기 차지 펌프단들로 공급하는 전압 공급 회로를 포함하는 전하 펌프 회로.

【청구항 2】

제 1 항에 있어서,

일반 동작 모드시, 상기 전압 공급 회로는 상기 프리차지 전압으로서 전원전압(Vcc)을 공급하는 전하 펌프 회로.

【청구항 3】

제 1 항에 있어서,

테스트 동작 모드시, 상기 전압 공급 회로는 상기 프리차지 전압으로서 전원전압(Vcc)보다 높은 고전압(Vpp)을 공급하는 전하 펌프 회로.

【청구항 4】

적어도 하나 이상의 차지 펌프단들을 포함하는 차지 펌프부와;

상기 차지 펌프부의 출력전압(Vout)의 레벨을 감지하여 레벨 감지 신호(DET)를 발생하는 레벨 감지부와;

상기 레벨 감지신호(DET)에 응답하여 펄스신호들(PUL, /PUL)을 발생하는 오실레이터와; 그리고

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전원전압(Vcc)보다 높은 고전압(Vpp)을 선택하여 상기 차지 펌프부에 상기 선택된 고전압(Vpp)을 공급할 수 있는 선택 회로부를 포함한 것을 특징으로 하는 전하 펌프 회로.

【청구항 5】

제 4 항에 있어서,

상기 차지 펌프부는, 상기 선택된 고전압(Vpp)에 해당하는 전하를 프리차지하여 상기 프리차지한 전하를 공급하는 전하 공급단과;

상기 전하 공급단에서 공급된 전하를 각각 펌핑하는 차지 펌프단들과; 그리고

상기 차지 펌프단들에서 펌핑된 전하를 최종적으로 저장하는 전하 저장단을 포함하되,

상기 차지 펌프단들은 상기 선택된 고전압(Vpp)에 상응하는 전하를 프리차지할 수 있는 프리 차지 수단들을 구비한 것을 특징으로 하는 전하 펌프 회로.

【청구항 6】

제 5 항에 있어서,

상기 전하 공급단은 고전압 PMOS 트랜지스터(P110)를 포함하여 구성된 것을 특징으로 하는 전하 펌프 회로.

【청구항 7】

제 5 항에 있어서,

상기 프리 차지 수단들은 각각의 상기 차지 펌프단들에 연결된 각각의 고전압 NMOS 트랜지스터들(N120, N130, N140, N150)을 포함하여 구성된 것을 특징으로 하는 전하 펌프 회로.

【청구항 8】

제 7 항에 있어서,

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상기 전하 공급단의 출력단(2)의 전압은 상기 선택된 고전압(Vpp)이고, 상기 차지 펌프 단들의 출력단들(3, 4, 5, 6)에 프리차지된 전압은 상기 선택된 고전압(Vpp)전압에서 상기 각각의 고전압 NMOS 트랜지스터들(N120, N130, N140, N150)의 드레솔드 전압(Vth)을 뺀 전압(Vpp-Vth)인 것을 특징으로 하는 전하 펌프 회로.

【청구항 9】

제 4 항에 있어서,

상기 선택 회로부는 상기 전원전압(Vcc)과 상기 고전압(Vpp)를 비교하여, 상기 고전압(Vpp)이 상기 전원 전압(Vcc) 이상이 될 때만, 상기 고전압(Vpp)을 선택하는 것을 특징으로 하는 전하 펌프 회로.

【청구항 10】

적어도 하나 이상의 차지 펌프단들을 포함하여 구성된 차지 펌프부와;

상기 차지 펌프부의 출력전압(Vout)의 레벨을 감지하여 레벨 감지 신호(DET)를 발생하는 레벨 감지부와;

상기 레벨 감지신호(DET)에 응답하여 펄스신호들(PUL, /PUL)을 발생하는 오실레이터와;

외부에서 인가되는 고전압(Vpp)이 일정 전압 이상일 경우에 '하이'인 검출신호(Vdet)를 발생하는 검출기와; 그리고

상기 '하이'인 검출신호(Vdet)에 응답하여 상기 고전압(Vpp)을 선택한 후 상기 선택된 고전압(Vpp)을 상기 차지 펌프부에 공급하는 선택기를 포함하는 것을 특징으로 하는 전하 펌프 회로.

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【청구항 11】

제 10 항에 있어서,

상기 차지 펌프부는, 상기 선택된 고전압(Vpp)에 해당하는 전하를 프리차지하여 상기 프리차지한 전하를 공급하는 전하 공급단과;

상기 전하 공급단에서 공급된 전하를 각각 펌핑하는 차지 펌프단들과; 그리고

상기 차지 펌프단들에서 펌핑된 전하를 최종적으로 저장하는 전하 저장단을 포함하되,

상기 차지 펌프단들은 상기 선택된 고전압(Vpp)에 상응하는 전하를 프리차지할 수 있는 프리 차지 수단들을 구비한 것을 특징으로 하는 전하 펌프 회로.

【청구항 12】

제 11 항에 있어서,

상기 전하 공급단은 고전압 PMOS 트랜지스터(P110)를 포함하여 구성된 것을 특징으로 하는 전하 펌프 회로.

【청구항 13】

제 11 항에 있어서,

상기 프리 차지 수단들은 각각의 상기 차지 펌프단들에 연결된 각각의 고전압 NMOS 트랜지스터들(N120, N130, N140, N150)을 포함하여 구성된 것을 특징으로 하는 전하 펌프 회로.

【청구항 14】

제 13 항에 있어서,

상기 전하 공급단의 출력단(2)의 전압은 상기 선택된 고전압(Vpp)이고, 상기 차지 펌프단들의 출력단들(3, 4, 5, 6)에 프리차지된 전압은 상기 선택된 고전압(Vpp)전압에서 상기 각

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각의 고전압 NMOS 트랜지스터들(N120, N130, N140, N150)의 드레솔드 전압(Vth)을 뺀 전압(Vpp-Vth)인 것을 특징으로 하는 전하 펌프 회로.

【청구항 15】

제 10 항에 있어서,

상기 검출기는 상기 고전압(Vpp)을 입력받아 동작하며, 상기 고전압(Vpp)이 전원전압(Vcc) 이상일 경우에, '하이'의 검출신호(Vdet)를 발생하는 것을 특징으로 하는 전하 펌프 회로.

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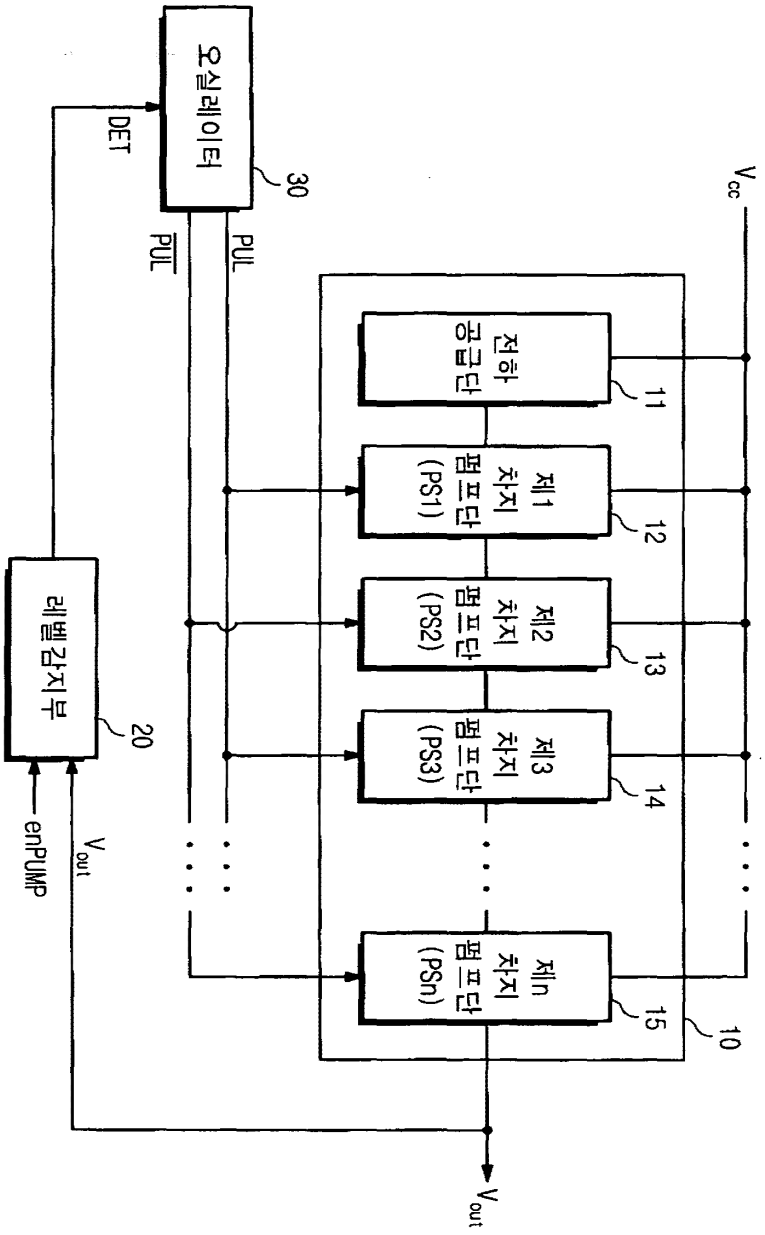
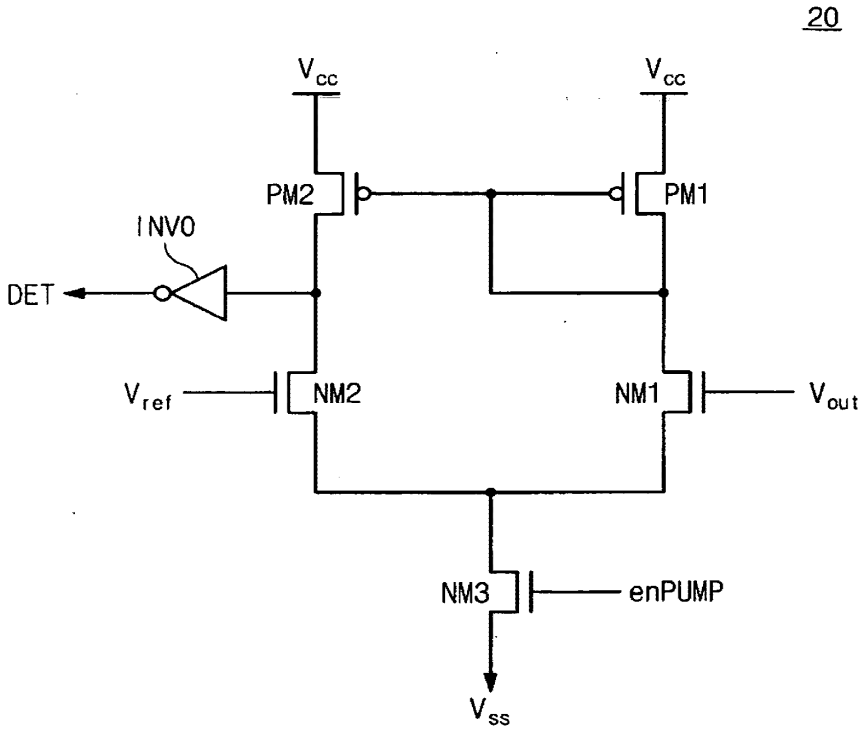
【도면】

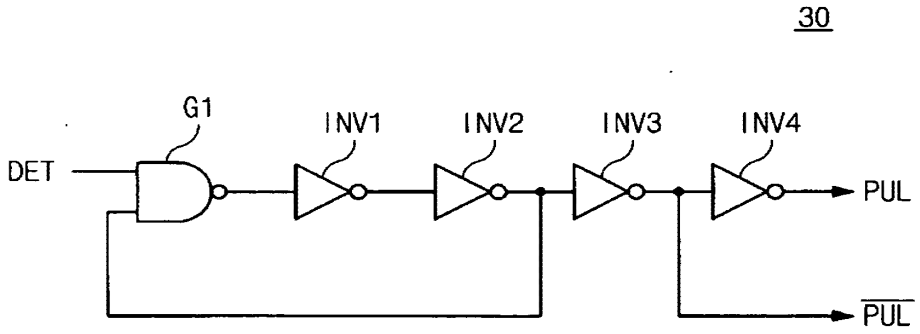
【도 1】


오실레이터
30
DET
PUL
PUL
V_{cc}
전하 공급단
11
제1 차지 펌프단 (PS1)
12
제2 차지 펌프단 (PS2)
13
제3 차지 펌프단 (PS3)
14
제n 차지 펌프단 (PSn)
15
10
레벨감지부
20
enPUMP
V_{out}
V_{out}

【도 2】



【도 3】



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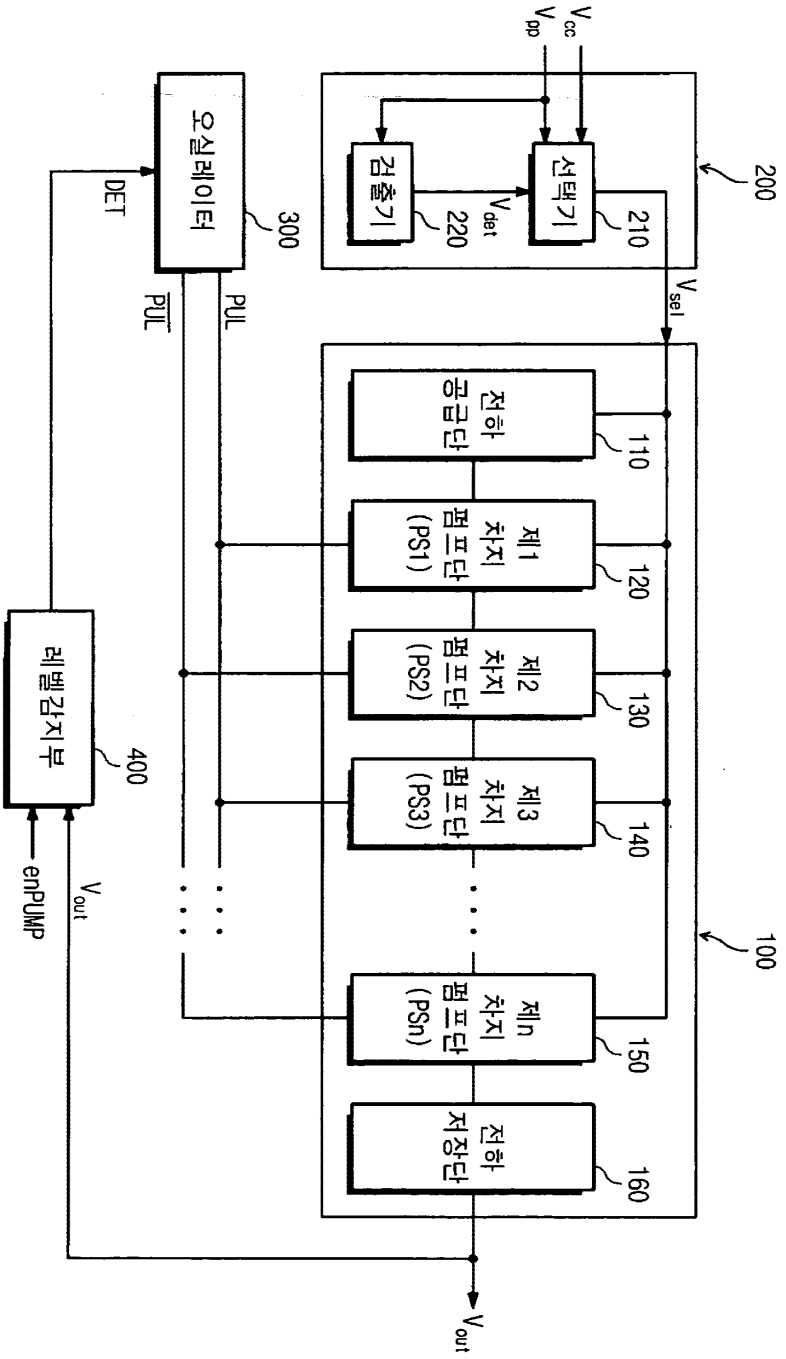
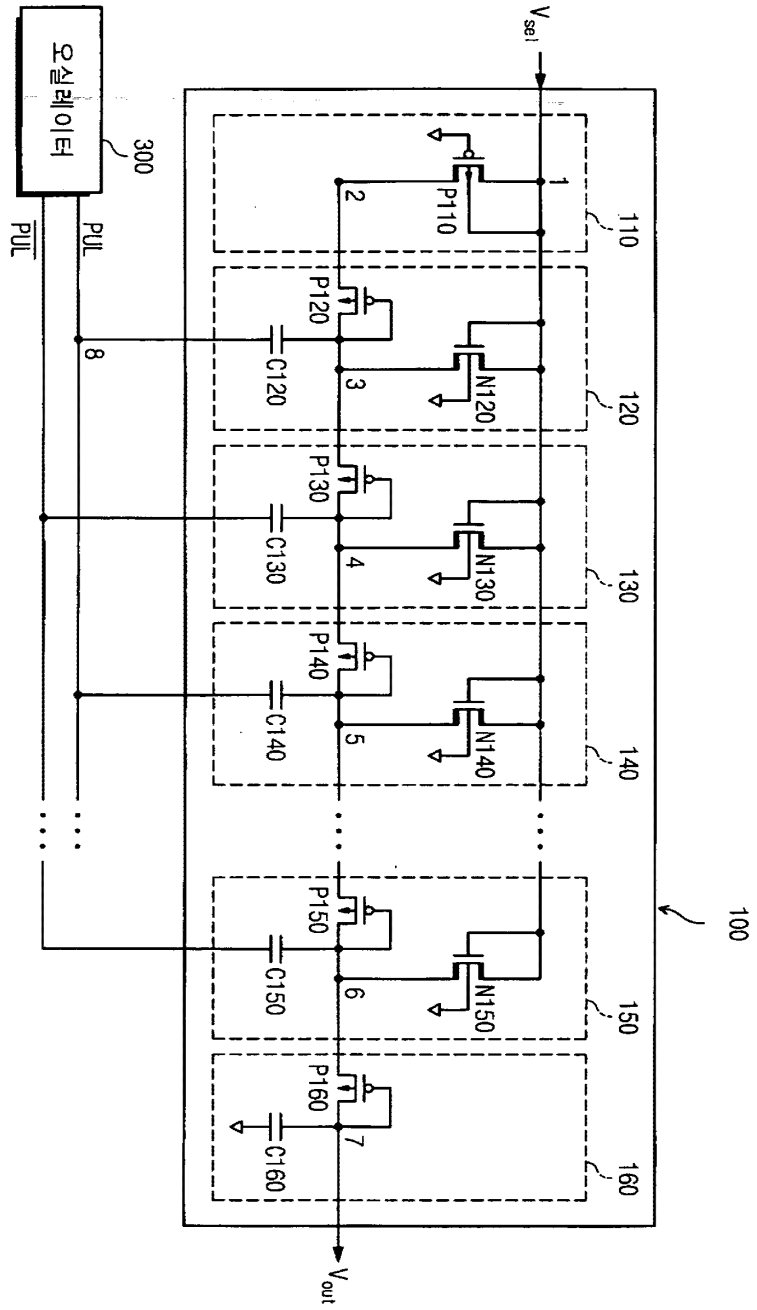
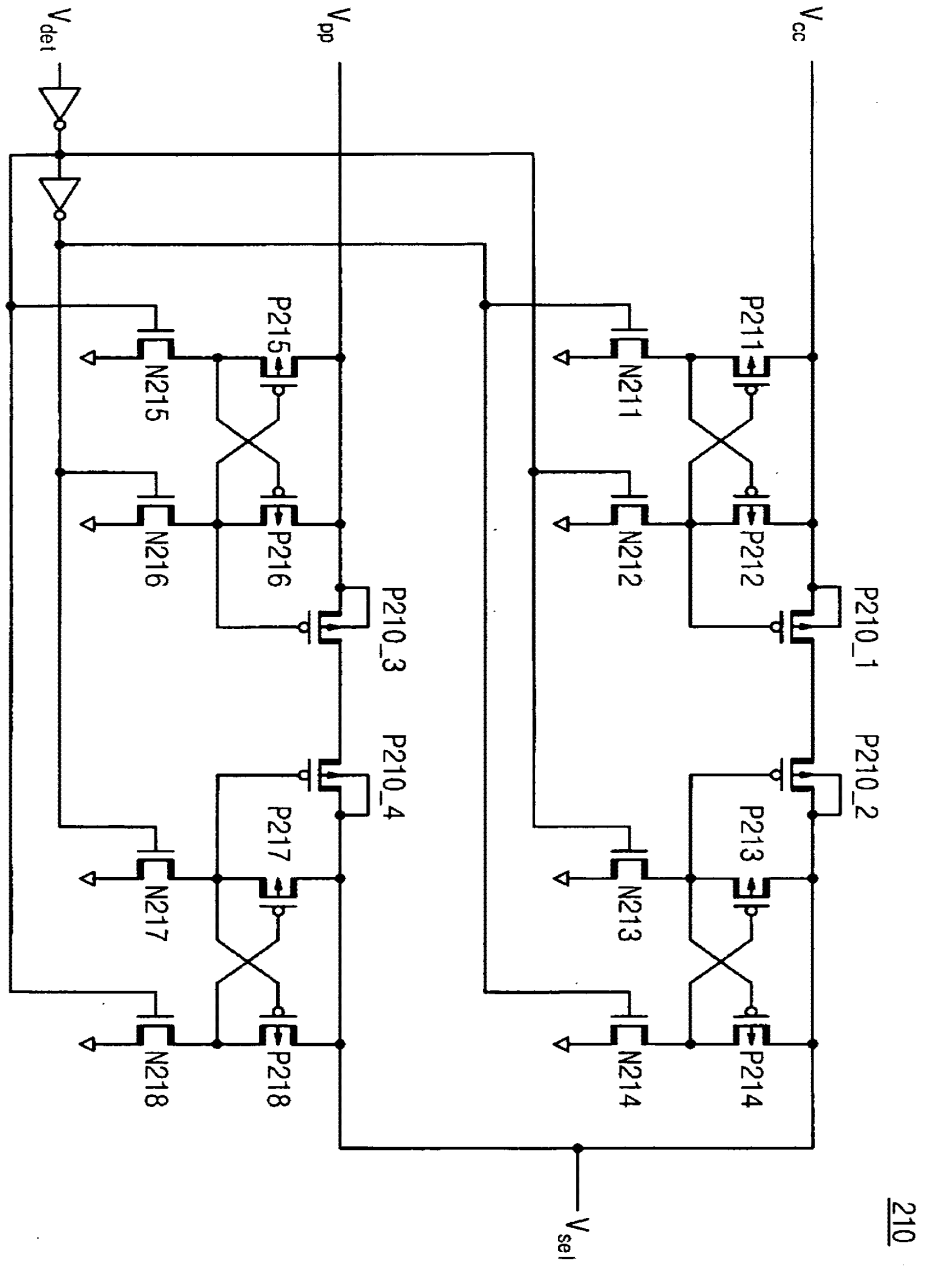
【도 4】


V_{cc}
V_{pp}
선택기
210
검출기
220
V_{det}
200
V_{sel}
오실레이터
300
DET
PUL
$\overline{PUL}$
전하 공급단
110
제1 차지 펌프단 (PS1)
120
제2 차지 펌프단 (PS2)
130
제3 차지 펌프단 (PS3)
140
제n 차지 펌프단 (PSn)
150
전하 저장단
160
100
레벨감지부
400
enPUMP
V_{out}
V_{out}

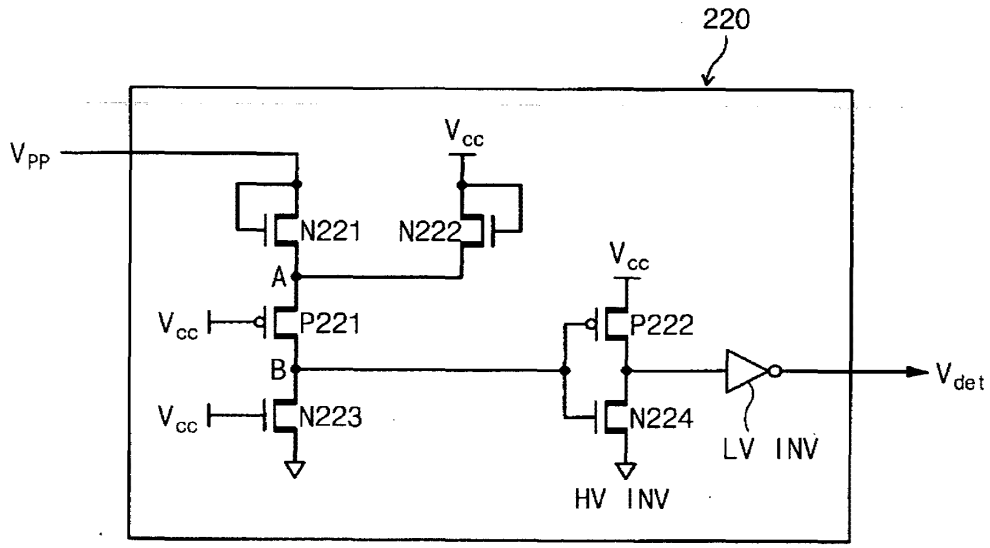
【도 5】


오실레이터
300
PUL
PUL
V_{sel}
V_{out}
100
110
120
130
140
150
160
P110
P120
P130
P140
P150
P160
N120
N130
N140
N150
C120
C130
C140
C150
C160
1
2
3
4
5
6
7
8

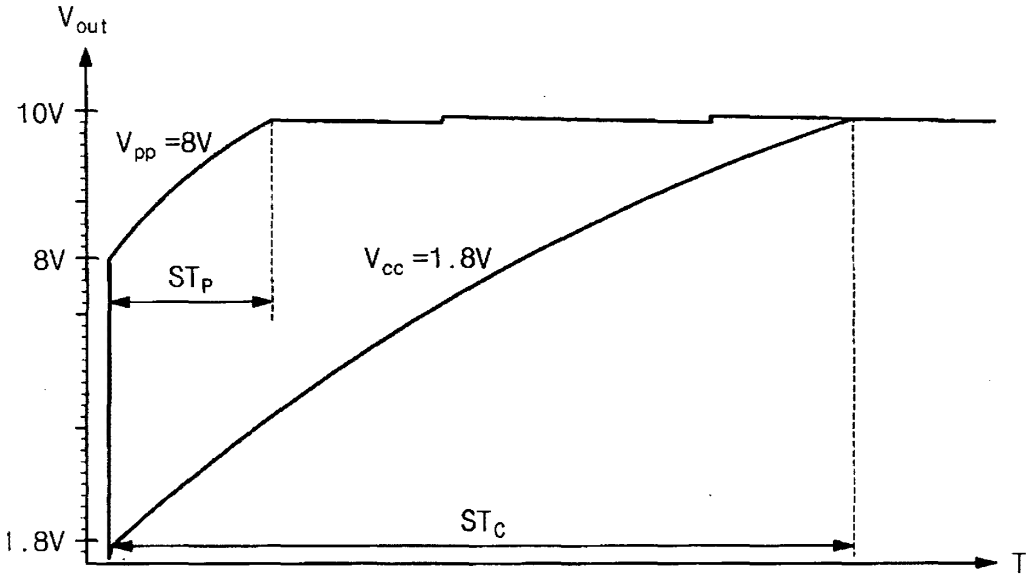
【도 6】


V_det
V_pp
V_cc
P215
N215
P211
N211
N216
P216
N212
P212
P210_3
P210_1
P210_4
P210_2
P217
N217
P213
N213
N218
P218
N214
P214
V_sel
210

【도 7】


220
V_{PP}
V_{cc}
N221
N222
A
V_{cc}
P221
V_{cc}
P222
B
V_{det}
V_{cc}
N223
N224
LV INV
HV INV

【도 8】


V_{out}
10V
V_{pp} =8V
8V
ST_P
V_{cc} =1.8V
1.8V
ST_C
T

01910 U.S.PTO
070804

PATENT APPLICATION
Docket No. 4591-380
Client No. ID13095-US

22782 U.S.PTO
10/888667
070804

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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I HEREBY CERTIFY THAT THIS PAPER AND ENCLOSURES AND/OR FEE ARE BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED ABOVE AND IS ADDRESSED TO: MAIL STOP PATENT APPLICATION, COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450.

LAUREN BALLARD-GEMMELL (SENDER'S PRINTED NAME)

Lauren Ballard-Gemmell (SIGNATURE)

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Enclosed for filing is a patent application under 37 CFR 1.53(b) of:

Inventor: Pyung-Moon Zhang and Seung-Keun Lee

For: CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE

Applicant requests FIG. 4 to be published with the application.

Enclosures:

- ☒ Specification (pages 1-6); Claims (pages 7-9); Abstract (page 10)
- ☒ SEVEN sheet(s) of FORMAL drawings (comprising 8 figures)
- ☐ Certified copy of Korean Priority Document No. 2003-46799, filed July 10, 2003, from which priority is claimed
- ☒ Return Postcard

CLAIMS AS FILED				
For	Number Filed	Number Extra	Rate	Basic Fee $770
Total Claims	18	0	x $ 18 =	$0.00
Independent Claims	3	0	x $ 86 =	$0.00
TOTAL FILING FEE				$770.00

- ☒ Combined Declaration and Power of Attorney
  - ☒ Newly executed (original)

☐ Assignment with cover sheet
Assignee Name and Address: Samsung Electronics Co., Ltd.
Suwon-city, Kyungki-do
REPUBLIC OF KOREA

☒ PTO Form 2038 authorizing credit card payment of $770.00 (filing fee) is enclosed.
☒ Any deficiency or overpayment should be charged or credited to deposit account number 13-1703.

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Respectfully submitted,

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CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE

BACKGROUND OF THE INVENTION

1. Priority Info

This application claims priority from Korean Patent Application Number 2003-46799, filed July 10, 2003, that we incorporate here by reference.

2. Field of the Invention

The present invention relates to high-voltage generators and, more specifically, to charge pump circuits operating responsive to a mode that enables selection of a power voltage or an external high voltage.

3. Discussion of the Related Art

FIG. 1 is a block diagram of a conventional charge pump circuit. As shown in FIG. 1, the conventional charge pump circuit comprises a voltage level sensing block 20, an oscillator 30, and a charge pump block 10. The voltage level sensing block 20 senses a level of the output voltage Vout. The oscillator 30 generates pulse signals PUL, /PUL responsive to a signal DET output from the block 20. The charge pump block 10 performs a pumping operation.

The voltage level sensing block 20, as shown in FIG. 2, comprises a differential amplifier. The voltage level sensing block 20 operates responsive to a pumping enable signal enPUMP and compares output voltage Vout with reference voltage VREF. The voltage level sensing block 20 generates a level sensing signal DET.

As shown in FIG. 3, the oscillator 30 comprises one NOR gate G1 and four invertors INV1, INV2, INV3 and INV4. And the oscillator 30 responds the level sensing signal DET to generate the complimentary pulse signals PUL, /PUL.

The charge pump block 10 comprises a charge supply part 11 and a plurality of charge pump parts 12-15. The charge supply part 11 receives an external voltage VCC and provides supply charges to a first charge pump part PS1. The charge pump parts PS1, PS2, PS3, ..., PSn are serially connected. The charge pump parts 12-15 generate an output voltage Vout by pumping charges supplied from the charge supply part 11. An odd number of pump parts 11-15 operates responsive to the pulse signal PUL, while an even number of them operate responsive to the inverted pulse signal /PUL.

The conventional charge pump shown in Fig. 1 operates as follows.

When the pumping enable signal enPUMP is in a predetermined logic level, e.g., becomes high, the voltage level sensing block 20 senses the level of the output voltage Vout by comparing output voltage Vout to a reference voltage VREF. If the reference voltage VREF is larger than the output voltage Vout, the voltage level sensing block 20 generates the level sensing signal DET having a predetermined state, e.g., high. On the other hand, if the output voltage Vout is larger than reference voltage VREF, the voltage level sensing block 20 generates the level sensing signal DET having e.g., a low state. The oscillator 30 provides the pulse signals PUL and /PUL to the charge pump parts PS1, PS2, PS3, ..., PSn responsive to the level sensing signal DET. That is, if the level sensing signal (DET) is enabled, all charge pump parts PS1, PS2, PS3, ..., PSn increase the level of the output voltage Vout. If the level sensing signal (DET) is disable, all charge pump parts PS1, PS2, PS3, ..., PSn decrease the level of the output voltage Vout.

The conventional charge pump circuit pre-charges the output voltage Vout corresponding to the external voltage VCC at each node of the charge supply part 11 and the charge pump parts 12-15. Accordingly, the time to precharge increases in the output voltage Vout. This additional time is undesired, particularly where testing integrated chips that require high voltages quickly. A need remains for an improved charge pump circuit.

SUMMARY

A feature of the invention is to address disadvantages associated with prior charge pumps.

Another feature of the invention is to provide a charge pump that operates both in a test and in a general operation mode.

A charge pump circuit includes at least one charge pump part. A voltage level sensing block generates a level sensing signal by sensing an output voltage. An oscillator 30 generates complementary pulse signals responsive to the level sensing signal. And a selecting circuit block generates a selected voltage that is one of a high voltage and a supply voltage to the at least one charge pump part, the high voltage having a level higher than the supply voltage.

BRIEF DESCRIPTION

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings

illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings:

FIG. 1 is a block diagram of a conventional charge pump circuit.

FIG. 2 is a circuit diagram of the sensing level sensing block 20 shown in FIG. 1.

FIG. 3 is a circuit diagram of the oscillator 30 shown in FIG. 1.

FIG. 4 is a block diagram of an embodiment of a charge pump circuit according to the present invention.

FIG. 5 is a circuit diagram of an embodiment of a charge pump part shown in FIG. 4.

FIG. 6 is a circuit diagram of an embodiment of the selector shown in FIG. 4.

FIG. 7 is a circuit diagram of an embodiment of the detector shown in FIG. 4.

FIG. 8 is a graph of the output voltage for the charge pump circuit of the present invention.

DETAILED DESCRIPTION

Reference will now be made in detail to embodiments of the present invention, examples of which are illustrated in the accompanying drawings. The present invention is, however, not limited to the embodiments illustrated here. Rather, the embodiments are introduced to provide easy and complete understanding of the scope and spirit of the present invention.

FIG. 4 is a block diagram of an embodiment of the charge pump circuit according to the present invention. Referring to FIG. 4, the charge pump circuit comprises a charge pump block 100, a selecting circuit block 200, an oscillator 300, and a voltage level sensing block 400.

The pump block 100 comprises a charge supply part 110, a plurality of charge pump parts 120, 130, 140, and 150 and a charge trapping part 160, all serially connected.

The charge supply part 110 provides a charge corresponding to voltage Vsel provided, in turn, by the selecting circuit block 200 to a first charge pump part 120. The charge pump parts 120, 130, 140 and 150 pre-charge a charge corresponding to the selected voltage Vsel and pumps a charge to a next serially connected charge supply part. The charge trapping part 160 traps the pumped charge through each charge pump part 120, 130, 140 and 150 to generate an output voltage Vout. FIG. 5 is a block diagram of the charge pump block 100 shown in FIG. 4.

Referring to FIG. 5, the sensing level part 400 senses level of output voltage Vout when a pumping enable signal enPUMP is enabled. In other words, if the output voltage

Vout is smaller than the reference voltage Vref, the level sensing signal DET is enabled. If the output voltage Vout is larger than the reference voltage Vref, on the other hand, the level sensing signal DET is disabled.

The oscillator 300 generates complementary pulse signals PUL and /PUL responsive to the level sensing signal DET. If the level sensing signal DE) is enabled, all charge pump parts 120, 130, 140 and 150 increase the output voltage Vout. If the level sensing signal DET is disabled, the charge pump parts 120, 130, 140 and 150 do not operate.

Referring to FIG. 4, the charge pump circuit according to the present invention comprises a selecting circuit block 200. The selecting circuit block 200 includes a selector 210 and a detector 220. In the specification power supply voltageVCC refers to the power voltage operating in general operation mode. The voltage VPP refers to a high voltage provided externally during a test operation mode. The high voltage VPP may be applied externally in the test operation mode as well as during the general operation mode.

The selecting circuit block 200 comprises the selector 210 and the detector 220. The selector 210 selects between the power voltage VCC and the high voltage VPP. The detector 220 detects the level of the high voltage VPP to generate detection signal VDET. The detector 220 enables the detection signal VDET when the high voltage VPP is higher than the power voltage VCC. The selector 210 switches between the power voltage VCC to the high voltage VPP responsive to the detection signal VDET. Put differently, the signal VSEL is VCC in the general operation mode and VPP in the test operation mode allowing for a high voltage within a short time. The selector 210 and the detector 220 are more fully described referring to FIGs. 6 and 7.

FIG. 5 is a circuit diagram of the charge pump block 100 shown in FIG. 4. Referring to FIG. 5, the charge pump block 100 operates as follows. The charge pump block 100 comprises the charge supply part 110, charge pump parts 120, 130, 140 and 150, and the charge trapping part 160.

The charge supply part 110 comprises high-voltage PMOS transistor P110 available simultaneously in general and test operation modes. The high-voltage PMOS transistor P110 is connected between node 1 and node 2. Source and bulk terminals of the high-voltage PMOS transistor P110 are connected to the node 1. A drain terminal is connected to the node 2. A gate is connected to a ground GND terminal. The charge supply part 110 is available for a charge supply device and supplies charges to a first charge pump part 120 located in next part. For example, if VSEL is VPP in the general operation mode, charges corresponding to the power voltage VCC are pre-charged at node 2. In addition, if VSEL is

VPP in test operation mode, charges corresponding to the high voltage VCC are pre-charged at node 2.

Each charge pump part 120, 130, 140 and 150 comprises one PMOS transistor, e.g., transistor P120, one capacitor, e.g., capacitor C120, and one high-voltage NMOS transistor, e.g., transistor N120. The high-voltage NMOS transistor, e.g., transistor N120, operates both in the general operation mode as well as the test operation mode. An odd number (or even number) of the charge pump parts operates responsive to the pulse signal PUL, while an even number (or odd number) of the charge parts operates responsive to the inverted pulse signal /PUL.

In the specification, pump parts except for the first charge pump part 120 is omitted for clarity. We describe only charge part 120 for simplicity. A person of reasonable skill should realize that other charge parts operate and include similar elements.

A source terminal of the PMOS transistor P120 is connected to the node 2. The source terminal of the PMOS transistor P120 is used as a charge transfer device. A drain terminal and a gate terminal are connected to the node 3. A bulk terminal is in a floating state. A capacitor C120 is used as a charge pumping device and is connected between the node 3 and the node 8. The pulse signal PUL or /PUL is applied to the capacitor C120. The drain of the NMOS transistor N120 is connected to the node 1. A source terminal is connected to the node 3, and the bulk terminal is connected to ground GND. The gate and drain terminals of high-voltage NMOS transistor N120 are used as a pre-charge device. The high-voltage NMOS transistor N120 pre-charges charges corresponding to the selecting voltage VSEL at the node 3. For example, if the threshold voltage of the high-voltage NMOS transistor N120 is VTH, charges corresponding to VSEL – VTH are pre-charged. In other words, charges corresponding to VCC – VTH are pre-charged in the general operation mode, and charges corresponding to VPP – VTH are pre-charged in the test mode.

The charge trapping part 160 comprises one PMOS transistor P160 and one capacitor. The PMOS transistor P160 is used as charge transfer device, and the capacitor is used as charge trapping device. The charge trapping part 160 generates the output voltage Vout.

FIG. 6 is a circuit diagram of the selector 210 shown in FIG. 4. Referring to FIG. 6, the selector 210 uses a level shifter to control the high voltage VPP. The selector 210 comprises high-voltage NMOS transistors N211 to N218, high-voltage PMOS transistors P211 to P218 and P210_I where i =1 to 4, and two serially connected inverters. The level shifter selects between the power voltage VCC and the high voltage VPP. For instance, the high-voltage NMOS transistors N216 and N217 turn on in the test operation mode where the

detection signal VDET is enables. The high-voltage PMOS transistors P210_3 and P210_4 turn on. As a result, VSEL is equal to VPP. However, since the high-voltage NMOS transistors N212 and N213 are turned off, the high-voltage PMOS transistors P210_1 and P210_2 are also turned off. Accordingly, VSEL is not equal to VCC. To the contrary, VSEL is equal to VCC in general operation mode where the detection signal VDET is disabled.

FIG. 7 is a circuit diagram of the detector 220 shown in FIG. 4. Referring to FIG. 7, the detector 220 comprises high-voltage PMOS transistors P221 and P222, high-voltage NMOS transistors N221-N224, a high-voltage inverter HV INV and a low-voltage inverter LV INV. The detector 220 can be used in the general as well as test operation mode requiring high voltage. For example, if external high-voltage VPP is lower than the power voltage VCC, a node A has a voltage that is VCC – VTH. Accordingly, the PMOS transistor P221 is off. At this time, node B voltage is ground GND. In another approach, if external high-voltage VPP is higher than the power voltage VCC, node A voltage is VPP – VTH. As VPP increases, node B has high enough voltage to inverse the output of the high-voltage inverter HV INV. This output generates a high detection signal VDET through passing the low-voltage inverter LV INV.

FIG. 8 is a graph of the output voltage Vout depending on whether the charge pump circuit uses the power voltage VCC or external high voltage VPP. Settling time is a time required for the pumping operation to obtain a wanted output voltage Vout. Referring to FIG. 8, if the selected voltage VSEL is under the condition that the power voltage VCC is equal to 1.8V, and the external voltage VPP is equal to 8V, it is known that four times settling times (STp) is required to obtain an output voltage Vout of 10V. That is, when external high voltage VPP is supplied with the power voltage VCC, a wanted output voltage Vout can be obtained within more short time.

As previously mentioned, the charge pump circuit can obtain a wanted output voltage Vout within a short time by further including selective means capable of applying high voltage rather than the power voltage VCC.

It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

CLAIMS

We claim the following.

1. A charge pump circuit comprising:

a charge pump block including at least one charge pump part; and

a voltage supply circuit to supply a pre-charge voltage to the at least one charge pump part responsive to a mode.

2. The charge pump circuit of claim 1 where the pre-charge voltage is a supply voltage in a general mode.

3. The charge pump circuit of claim 1 where the pre-charge voltage is a voltage higher than the supply voltage in a test mode.

4. The charge pump circuit of claim 1 where the voltage supply circuit comprises:

a detector circuit to generate a detect signal responsive to a high voltage; and

a selector circuit to supply the pre-charge voltage responsive to the detect signal.

5. The charge pump circuit of claim 1 where the voltage supply circuit comprises:

a voltage level sensing block to generate a level sensing signal responsive to a pump enable signal; and

an oscillator to generate complementary pulse signals responsive to the level sensing signal.

6. The charge pump circuit of claim 1 where the voltage supply circuit comprises a charge trapping part to generate an output voltage.

7. A charge pump circuit comprising:

at least one charge pump part;

a voltage level sensing block to generate a level sensing signal by sensing an output voltage;

an oscillator to generate complementary pulse signals responsive to the level sensing signal; and

a selecting circuit block to generate a selected voltage that is one of a high voltage and a supply voltage to the at least one charge pump part, the high voltage having a level higher than the supply voltage.

8. The charge pump circuit of claim 7 comprising:

a charge supply part to precharge the at least one charge pump part with the selected voltage; and

a charge trapping part to store charges provided by the charge supply part.

9. The charge pump circuit of claim 8 where the at least one charge pump part pumps a charge to another charge pump part.

10. The charge pump circuit of claim 8 where the charge supply part comprises a high-voltage PMOS transistor.

11. The charge pump circuit of claim 7 where the at least one charge pump part includes a high-voltage NMOS transistor.

12. The charge pump circuit of claim 7

where the selecting circuit block compares the supply voltage with the high voltage; and

where the selecting circuit selects the high voltage if a level of the high voltage is higher than a level of the power voltage.

13. A charge pump circuit comprising:

a charge pump block including at least one charge pump part;

a voltage level sensing block to sense a level of an output voltage and generate a level sensing signal responsive thereto;

an oscillator to generate a pulse signal responsive to the level sensing signal;

a detector to generate a detection signal responsive to a high voltage; and

a selector to provide one of the high voltage and the power voltage responsive to the detection signal to the charge pump block.

14. The charge pump circuit of claim 13 where the charge pump block comprises:

a charge supply part to precharge the at least one charge pump part; and

a charge trapping part to store charges pumped from the at least one charge pump part.

15. The charge pump circuit of claim 14 where the at least one charge pump part pumps charge to another serially connected charge pump part.

16. The charge pump circuit of claim 14 where the charge supply part includes a high-voltage PMOS transistor.

17. The charge pump circuit of claim 14 where the charge pump block includes a high-voltage NMOS transistor.

18. The charge pump circuit of claim 13 where the selector compares the high voltage to the power voltage.

CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE

ABSTRACT

Disclosed is a charge pump circuit that operates responsive to a test or general operation mode. The charge pump circuit includes at least one charge pump part. A voltage level sensing block generates a level sensing signal by sensing an output voltage. An oscillator generates complementary pulse signals responsive to the level sensing signal. And a selecting circuit block generates a selected voltage that is one of a high voltage and a supply voltage to the at least one charge pump part, the high voltage having a level higher than the supply voltage.

Fig. 1

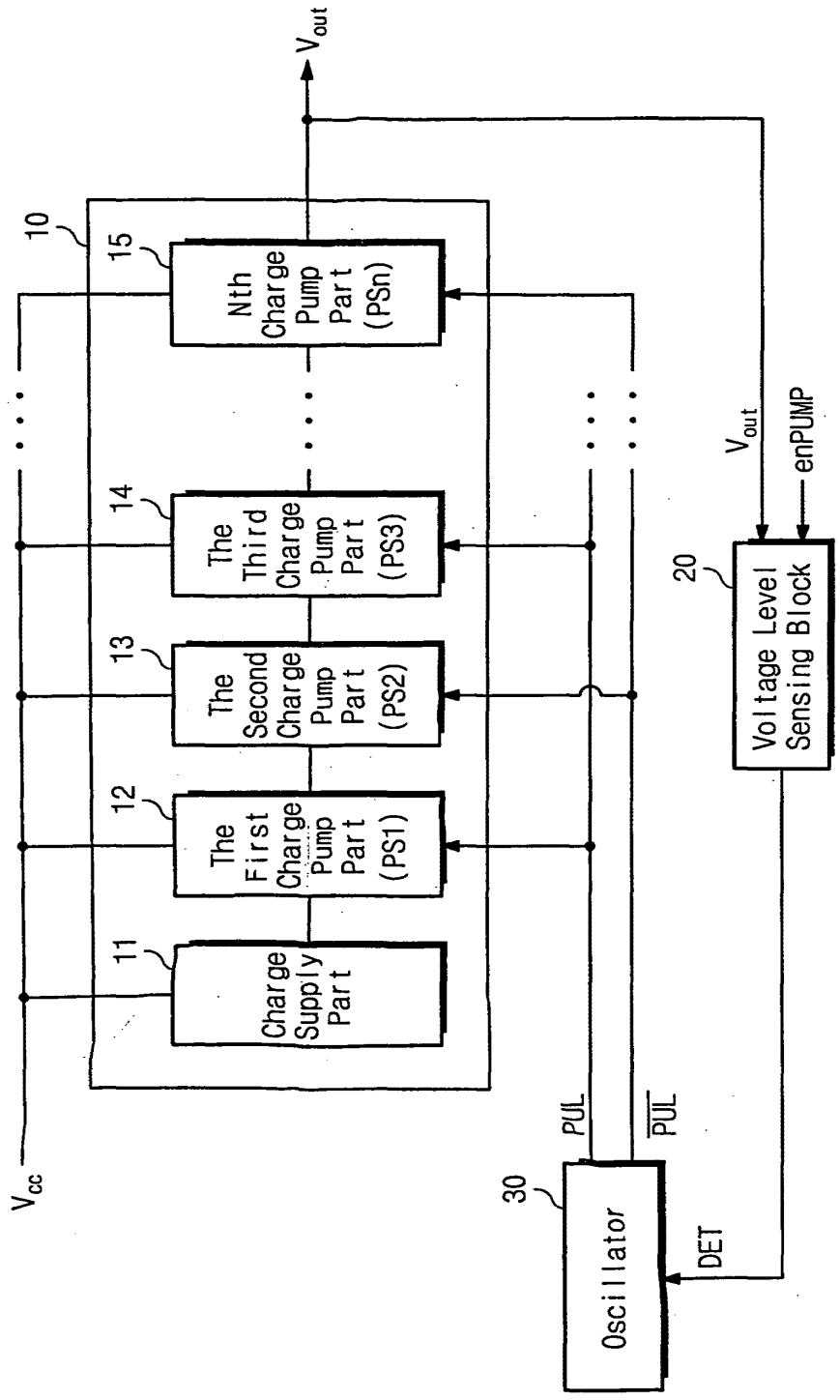

V_{out}
10
15
Nth Charge Pump Part (PSn)
14
The Third Charge Pump Part (PS3)
13
The Second Charge Pump Part (PS2)
12
The First Charge Pump Part (PS1)
11
Charge Supply Part
V_{cc}
V_{out}
enPUMP
20
Voltage Level Sensing Block
PUL
$\overline{PUL}$
30
Oscillator
DET

Fig. 2

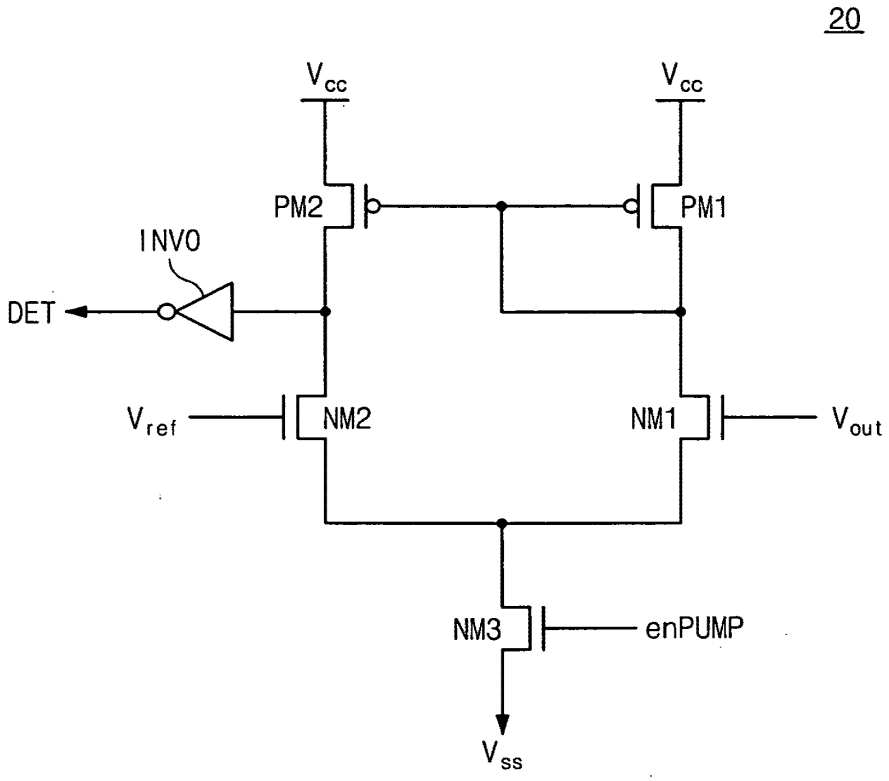

20
V_{cc}
V_{cc}
PM2
PM1
INV0
DET
V_{ref}
NM2
NM1
V_{out}
NM3
enPUMP
V_{ss}

Fig. 3

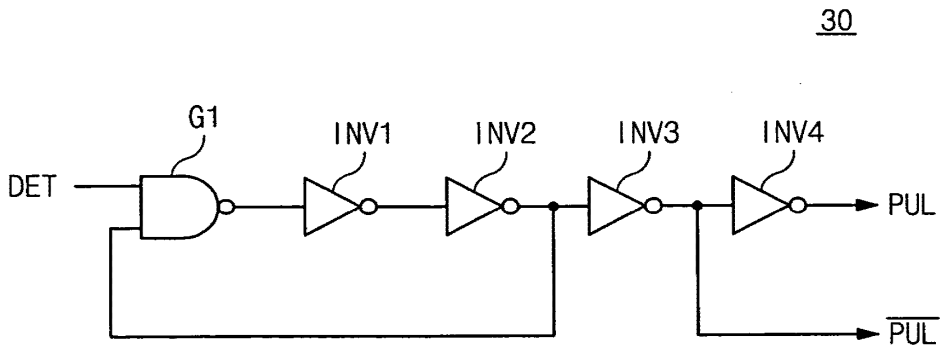

30
G1
INV1
INV2
INV3
INV4
DET
PUL
$\overline{PUL}$

Fig. 4

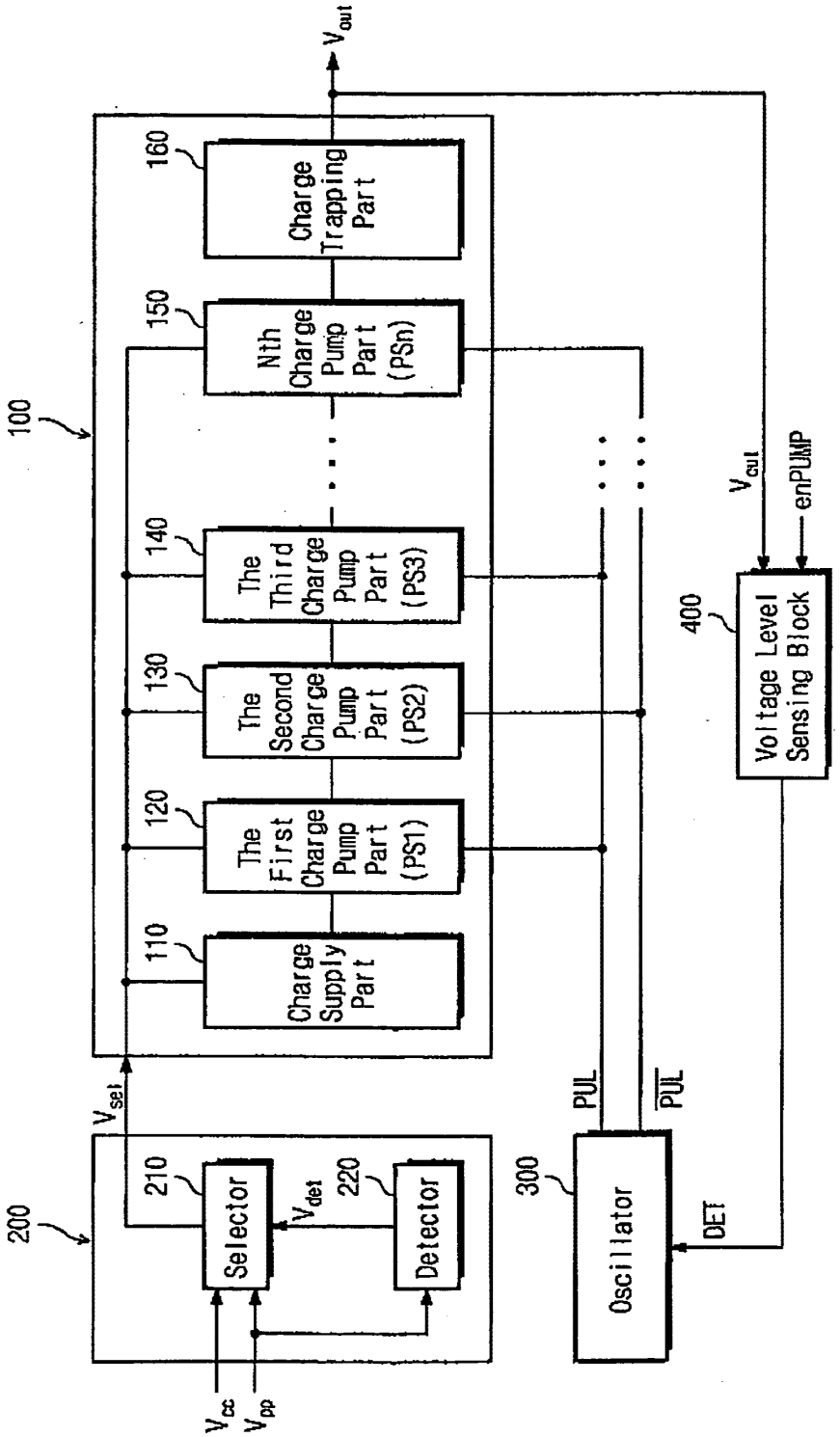

V_{out}
160
Charge Trapping Part
150
Nth Charge Pump Part (PSn)
100
140
The Third Charge Pump Part (PS3)
130
The Second Charge Pump Part (PS2)
120
The First Charge Pump Part (PS1)
110
Charge Supply Part
V_{out}
enPUMP
400
Voltage Level Sensing Block
V_{set}
PUL
$\overline{PUL}$
200
210
Selector
V_{det}
220
Detector
300
Oscillator
DET
V_{cc}
V_{pp}

Fig. 5

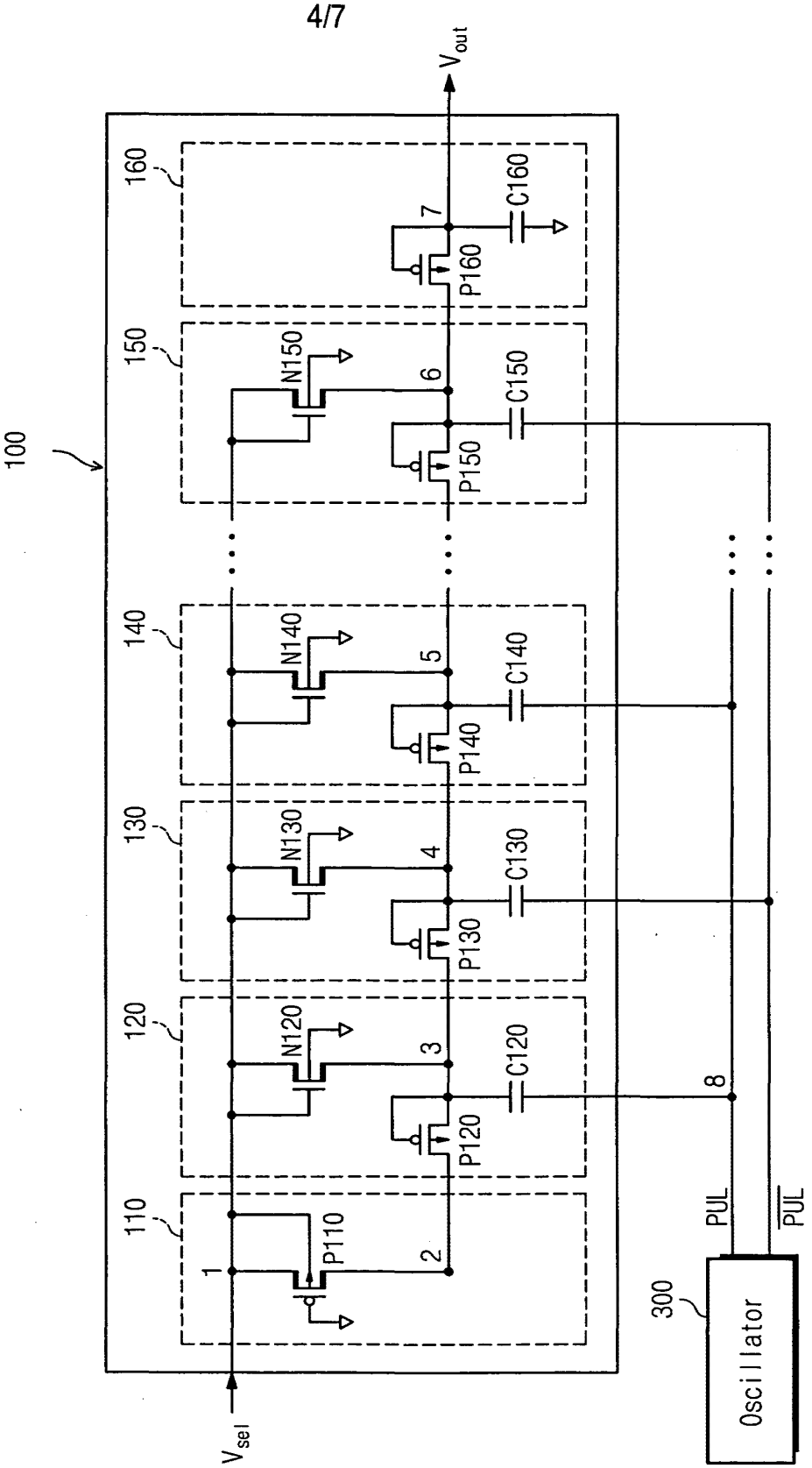

100
110
120
130
140
150
160
P110
N120
P120
N130
P130
N140
P140
N150
P150
P160
C120
C130
C140
C150
C160
1
2
3
4
5
6
7
8
V_{sel}
V_{out}
PUL
$\overline{PUL}$
300
Oscillator

Fig. 6

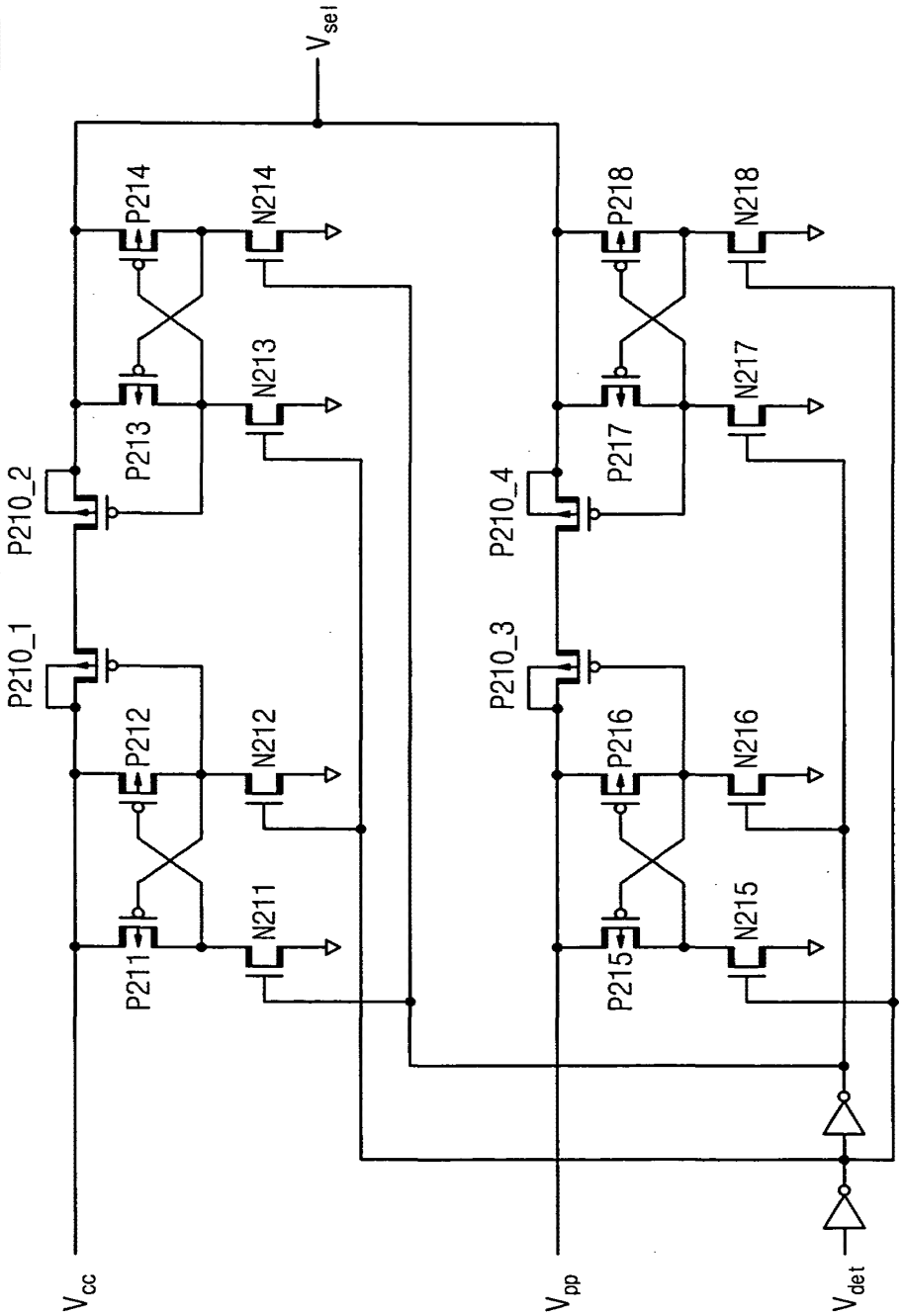

210
V_{sel}
P214
N214
P218
N218
N213
N217
P213
P217
P210_2
P210_4
P210_1
P210_3
P212
N212
P216
N216
N211
N215
P211
P215
V_{cc}
V_{pp}
V_{det}

Fig. 7

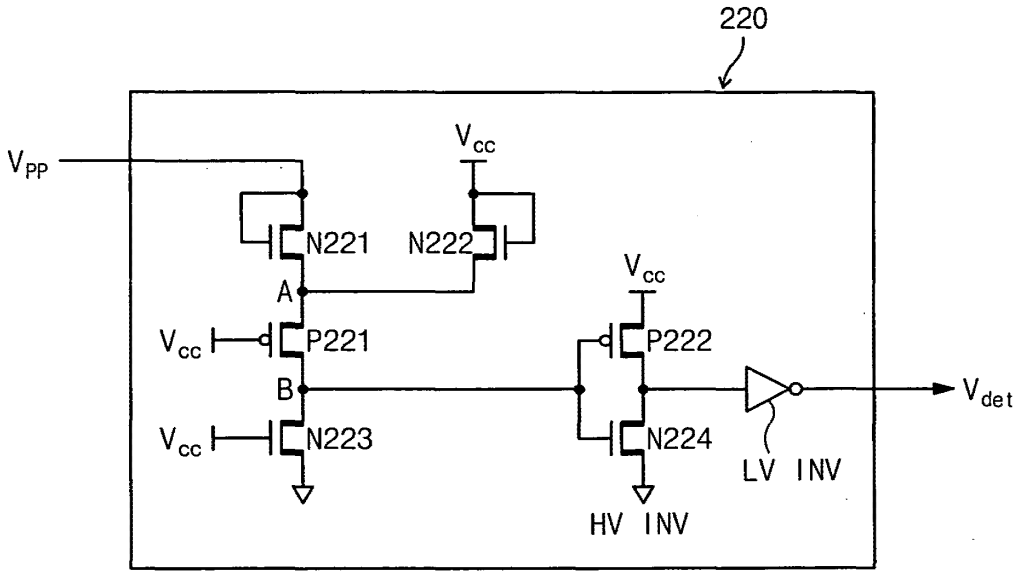
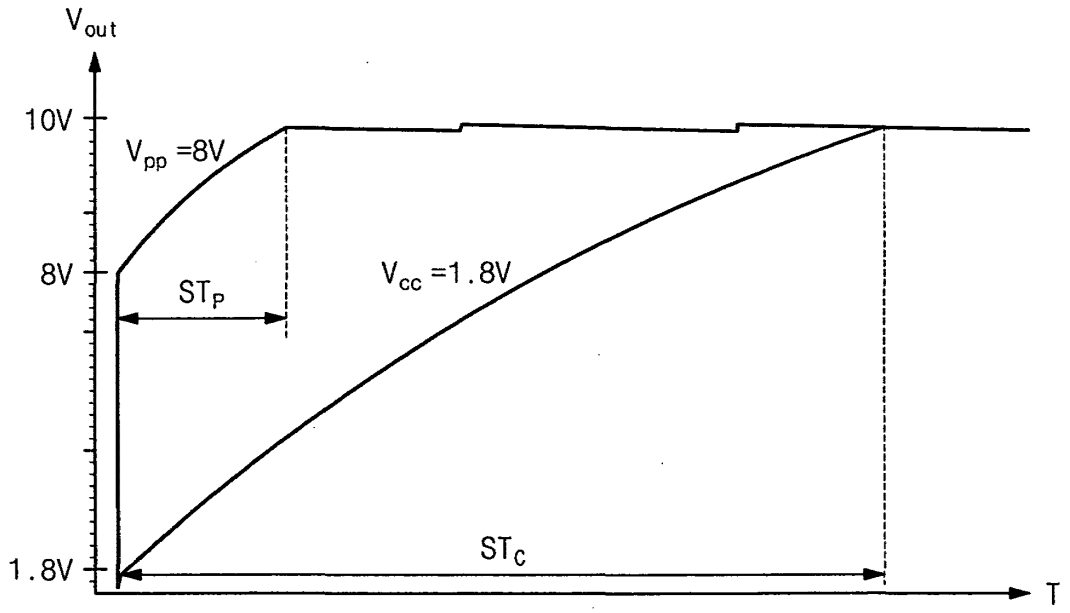

220
V_{PP}
V_{cc}
N221
N222
A
V_{cc}
P221
B
V_{cc}
N223
V_{cc}
P222
N224
HV INV
LV INV
V_{det}

Fig. 8



PATENT APPLICATION
Docket No. 4591-380
Client Ref. No. ID13095-US

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated b elow next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sou ght on the invention entitled **CHARGE PUMP CIRCUIT OPERATING RESPONSIVE TO A MODE**, the specification of which:

- ☒ is attached hereto.
- ☐ was filed on _____ as Application No. _____
- ☐ and was amended on _____(if applicable)
- ☐ with amendments through _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above -identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information that is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Sec. 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Sec. 119 (a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, li sted below and have also identified below any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Claiming Priority?
2003-46799 (Number)	**Republic of Korea** (Country)	**10 July 2003** (Day/Month/Year Filed)	☒ Yes ☐ No

I hereby claim the benefit under Title 35, United States Code, Sec. 119(e) of any United States provisional application listed below: **NONE.**

I hereby claim the benefit under Title 35, United States Code, Sec. 120 or §365(c) of any PCT international application designating the United States of America listed below and, insofar as the subject mat ter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Sec. 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Sec. 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application: **NONE.**

I hereby appoint the following at torneys to prosecute the application, to file a corresponding international application, to prosecute and transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; a nd further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statement s may jeopardize the validity of the application or any patent issued thereon.

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PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number: 10888667

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	18	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	18 minus 20=	* 0
INDEPENDENT CLAIMS	3 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	770.00
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL		OR	TOTAL	770

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

1, 7, 13,

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

07/14/2004 EAREGAY1 00000106 10888667
01 FC:1001 770.00 OP

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/69033