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Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/912,845	10/14/2014	8860499	Q204830	5774

23373 7590 09/24/2014
SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

ELPIDA MEMORY, INC., Tokyo, JAPAN, Assignee (with 37 CFR 1.172 Interest);
Koichiro HAYASHI, Tokyo, JAPAN;
Hitoshi TANAKA, Ome, JAPAN;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTALComplete and send this form, together with applicable fee(s), to: **Mail**Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
(571) 273-2885or **Fax**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS

(Note: Use Block 1 for any change of address)

23373

SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, NW
SUITE 800
WASHINGTON, DC 20037

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/912,845	06/07/2013	Koichiro HAYASHI	Q204830	5774

TITLE OF INVENTION: SUPPLY VOLTAGE GENERATING CIRCUIT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	Undiscounted	\$960	\$0	\$0	\$960	09/10/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
ALMO, KHAREEM E	2842	327-536000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363)

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached.
Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Sughrue Mion, PLLC

2

3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

PS4 Luxco S.a.r.l.**Luxembourg, Luxembourg**Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☒ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 19-4880 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
☐ Applicant asserting small entity status. See 37 CFR 1.27
☐ Applicant changing to regular undiscounted fee status

NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature	/ Carl J. Pellegrini /	Date	September 10, 2014
Typed or Printed Name	Carl J. Pellegrini	Registration No.	40,766

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal				
Application Number:		13912845		
Filing Date:		07-Jun-2013		
Title of Invention:		SUPPLY VOLTAGE GENERATING CIRCUIT		
First Named Inventor/Applicant Name:		Koichiro HAYASHI		
Filer:		J. Lytle/Jeffrey Kaufman		
Attorney Docket Number:		Q204830		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt	
EFS ID:	20094118
Application Number:	13912845
International Application Number:	
Confirmation Number:	5774
Title of Invention:	SUPPLY VOLTAGE GENERATING CIRCUIT
First Named Inventor/Applicant Name:	Koichiro HAYASHI
Customer Number:	23373
Filer:	J. Lytle/Jeffrey Kaufman
Filer Authorized By:	J. Lytle
Attorney Docket Number:	Q204830
Receipt Date:	10-SEP-2014
Filing Date:	07-JUN-2013
Time Stamp:	09:29:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 960
RAM confirmation Number	4859
Deposit Account	194880
Authorized User	SUGHRUE MION, PLLC
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Q204830IssueFeeTransmittal.pdf	37692	no	1
			6b53457289cd250d73913e213ff5a81cee424e63		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30449	no	2
			e9aea08a5280b4497e236a71a2a43a3b62fb6f7a		
Warnings:					
Information:					
Total Files Size (in bytes):			68141		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/912,845	06/07/2013	Koichiro HAYASHI	Q204830	5774
7590 06/30/2014 SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037			EXAMINER ALMO, KHAREEM E	
			ART UNIT	PAPER NUMBER
			2842	
			NOTIFICATION DATE	DELIVERY MODE
			06/30/2014	ELECTRONIC

Letter Withdrawing a Notice Requiring Inventor's Oath or Declaration

The Notice Requiring Inventor's Oath or Declaration mailed on 06/10/2014 was sent in error, and is hereby withdrawn. The time period set forth in the Notice of Allowance and Fee(s) Due to file a reply and pay the required fees continues to run from the mailing date of the Notice of Allowance and Fee(s) Due. Any time period set forth in the Notice of Allowability continues to run from the mailing date of the Notice of Allowability.

Questions relating to this Notice should be directed to the Application Assistance Unit at 571-272-4200.

(571)-272-4200 or 1(888)-786-0101

Patent Publication Branch

Office of Data Management



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

23373 7590 06/10/2014
SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER

ALMO, KHAREEM E

ART UNIT

PAPER NUMBER

2842

DATE MAILED: 06/10/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/912,845	06/07/2013	Koichiro HAYASHI	Q204830	5774

TITLE OF INVENTION: SUPPLY VOLTAGE GENERATING CIRCUIT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	09/10/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23373 7590 06/10/2014
SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/912,845	06/07/2013	Koichiro HAYASHI	Q204830	5774

TITLE OF INVENTION: SUPPLY VOLTAGE GENERATING CIRCUIT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	09/10/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
ALMO, KHAREEME	2842	327-536000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/912,845	06/07/2013	Koichiro HAYASHI	Q204830	5774
23373 7590 06/10/2014 SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037			EXAMINER ALMO, KHAREEM E	
			ART UNIT 2842	PAPER NUMBER

DATE MAILED: 06/10/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

<i>Notice Requiring Inventor's Oath or Declaration</i>	Application No. 13/912,845	Applicant(s) Koichiro HAYASHI	
	Examiner ALMO, KHAREEM E	Art Unit 2842	

This notice is an attachment to the Notice of Allowability (PTOL-37), or the Notice of Allowability For A Design Application (PTOL-37D).

An inventor's oath or declaration in compliance with 37 CFR 1.63 or 1.64 executed by or with respect to each inventor has not yet been submitted.

An oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each inventor (for any inventor for which a compliant oath, declaration, or substitute statement has not yet been submitted) **MUST** be filed no later than the date on which the issue fee is paid. See 35 U.S.C. 115(f). Failure to timely comply will result in ABANDONMENT of this application.

A properly executed inventor's oath to declaration has not been received for the following inventor(s):

If applicant previously filed one or more oaths, declarations, or substitute statements, applicant may have received an informational notice regarding deficiencies therein.

The following deficiencies are noted:

INFORMAL ACTION PROBLEMS

- A properly executed inventor's oath or declaration has not been received for the following inventor(s): **Koichiro HAYASHI and Hitoshi TANAKA.**

Applicant may submit the inventor's oath or declaration at any time before the Notice of Allowance and Fee(s) Due, PTOL-85, is mailed.

Questions relating to this Notice should be directed to the Application Assistance Unit at 571-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/912,845	Applicant(s) HAYASHI ET AL.	
	Examiner KHAREEM E. ALMO	Art Unit 2842	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to papers filed 4/9/2014.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-7 and 10-16. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☒ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 12052422.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	

KHAREEM E. ALMO Examiner Art Unit: 2842	
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1. The present application is being examined under the pre-AIA first to invent provisions.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/9/2014 has been entered.

Allowable Subject Matter

3. Claims 1-7 and 10-16 are allowed.
4. The following is an examiner's statement of reasons for allowance:

With respect to claim 1, the prior art of record fails to suggest or disclose a voltage booster circuit including a voltage output node and first and second boosting circuits each including a capacitor and each coupled to the internal voltage node, the voltage booster circuit being configured such that the first and second voltage boosting circuits are coupled in series to the voltage output node when the switching circuit takes the first switching state and that the first boosting circuit is coupled to the voltage output node and the second boosting circuit is disconnected from each of the first boosting circuit and the voltage output node when the switching circuit takes the second switching state and at least when the switching circuit takes a switching state, the capacitor of the first boosting circuit is coupled to the voltage output node and the

capacitor of the second boosting circuit is disconnected from each of the voltage output node and the capacitor of the first boosting circuit.

With respect to claim 10, the prior art of record fails to suggest or disclose a method for generating a supply voltage comprising: outputting, by a voltage booster circuit including first boosting circuit and second boosting circuit, either one of a first boosted voltage generated by coupling the first boosting circuit and the second boosting circuit in series to a voltage output node at the first switching state and a second boosted voltage generated by coupling the first boosting circuit to the voltage output node and disconnecting the second boosting circuit from each of the first boosting circuit and the voltage output node at the second switching state and the first and second boosting circuits being such that, at least when the switching circuit takes a switching state, a capacitor of the first boosting circuit is coupled to the voltage output node and a capacitor of the second boosting circuit is disconnected from each of the voltage output node and the capacitor of the first boosting circuit.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHAREEM E. ALMO whose telephone number is (571)272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on (571) 272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KHAREEM E. ALMO/
Examiner, Art Unit 2842
/LINCOLN DONOVAN/
Supervisory Patent Examiner, Art Unit 2842

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	4974	(327/535-537).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/05/16 18:36
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L5	2	("0000012").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/05/16 18:36
L6	6041	L3 L4	US-PGPUB; USPAT; USOCR	OR	OFF	2014/05/16 18:36
L7	4666	L6 and capacit\$4	US-PGPUB; USPAT; USOCR	OR	OFF	2014/05/16 18:36
L8	4432	L7 and (transistor switch mos)	US-PGPUB; USPAT; USOCR	OR	OFF	2014/05/16 18:36
L9	538	L8 and (booster)	US-PGPUB; USPAT; USOCR	OR	OFF	2014/05/16 18:36
L10	247	L8 and (step adj down)	US-PGPUB; USPAT; USOCR	OR	OFF	2014/05/16 18:36
L11	385	L8 and (gate near oxide)	US-PGPUB; USPAT; USOCR	OR	OFF	2014/05/16 18:36
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L14	122	L12 and (by-pass or bypass)	US-PGPUB; USPAT; USOCR; JPO	OR	OFF	2014/05/16 18:36
L15	52	L14 and variable	US-PGPUB; USPAT; USOCR; JPO	OR	OFF	2014/05/16 18:36
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EAST Search History (Interference)

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L2	4543	(327/535-537).CCLS.	US-PGPUB; USPAT; UPAD	OR	OFF	2014/05/16 18:36

5/16/2014 6:39:18 PM

C:\Users\kalmo\Documents\EAST\Workspaces\13912845.wsp



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BIB DATA SHEET

CONFIRMATION NO. 5774

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
13/912,845	06/07/2013	327	2842	Q204830		
APPLICANTS ELPIDA MEMORY, INC., Tokyo, JAPAN, Assignee (with 37 CFR 1.172 Interest); INVENTORS Koichiro HAYASHI, Tokyo, JAPAN; Hitoshi TANAKA, Ome, JAPAN; ** CONTINUING DATA ***** This application is a CON of 12/052,422 03/20/2008 PAT 8493132 ** FOREIGN APPLICATIONS ***** JAPAN 2007-081754 03/27/2007 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 06/27/2013						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and Acknowledged /KHAREEM E ALMO/ Examiner's Signature		☐ Met after Allowance KEA Initials	STATE OR COUNTRY JAPAN	SHEETS DRAWINGS 5	TOTAL CLAIMS 9	INDEPENDENT CLAIMS 1
ADDRESS SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037 UNITED STATES						
TITLE SUPPLY VOLTAGE GENERATING CIRCUIT						
FILING FEE RECEIVED 1740	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Search Notes 	Application/Control No. 13912845	Applicant(s)/Patent Under Reexamination HAYASHI ET AL.
	Examiner KHAREEM E ALMO	Art Unit 2816

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (A Copy of East is included)	5/16/2014	KEA
A limited search of class 327 subclasses 535-537	5/16/2014	KEA
A limited search fo class 363 subclasses 59-60	5/16/2014	KEA

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
327	535	5/16/2014	KEA
327	536	5/16/2014	KEA
327	537	5/16/2014	KEA
363	59	5/16/2014	KEA
363	60	5/16/2014	KEA

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Issue Classification 	Application/Control No. 13912845	Applicant(s)/Patent Under Reexamination HAYASHI ET AL.	
	Examiner KHAREEM E ALMO	Art Unit 2842	

CPC					
Symbol				Type	Version
G11C	5	145		I	2013-01-01
G05F	1	62		F	2013-01-01
H02M	3	07		I	2013-01-01
G11C	11	4074		I	2013-01-01

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

/KHAREEM E ALMO/ Examiner.Art Unit 2842 (Assistant Examiner)	5/16/2014 (Date)	Total Claims Allowed: 14	
/LINCOLN DONOVAN/ Supervisory Patent Examiner.Art Unit 2842 (Primary Examiner)	05/18/2014 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 2

Issue Classification 	Application/Control No. 13912845	Applicant(s)/Patent Under Reexamination HAYASHI ET AL.
	Examiner KHAREEM E ALMO	Art Unit 2842

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION														
CLASS			SUBCLASS			CLAIMED					NON-CLAIMED									
327			536			G	0	5	F	1 / 10 (2006.0)										
CROSS REFERENCE(S)																				
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																			

/KHAREEM E ALMO/ Examiner.Art Unit 2842 (Assistant Examiner)	5/16/2014 (Date)	Total Claims Allowed: 14	
/LINCOLN DONOVAN/ Supervisory Patent Examiner.Art Unit 2842 (Primary Examiner)	05/18/2014 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 2

☒ **Claims renumbered in the same order as presented by applicant** ☐ **CPA** ☐ **T.D.** ☐ **R.1.47**2

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL							
Application Number	13/912,845	Filing Date	June 7, 2013	Confirmation Number	5774	Docket Number	Q204830
First Named Inventor	Koichiro HAYASHI	Examiner Name	ALMO, KHAREEM E			Art Unit	2842
Title	SUPPLY VOLTAGE GENERATING CIRCUIT						
This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.							
SUBMISSION REQUIRED UNDER 37 CFR 1.114							
Note: If the RCE is proper, any previously filed unentered amendments and amendments attached with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).							
☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____ ☐ Other _____							
☐ Do NOT consider the amendment(s)/reply under 37 CFR 1.116 previously filed on _____							
☒ Attached ☒ Amendment/Reply ☐ Information Disclosure Statement (IDS) ☐ Affidavit(s)/Declaration(s) ☐ Other _____							
MISCELLANEOUS							
☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)							
☐ Other _____							
FEES							
The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.							
☒ Payment by credit card. ☒ The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.							
CORRESPONDENCE ADDRESS							
<i>Direct all correspondence to the address for SUGHRUE MION, PLLC filed under the Customer Number listed below:</i> WASHINGTON OFFICE <b style="font-size: 1.2em;">23373 CUSTOMER NUMBER							
SIGNATURE OF REGISTERED U.S. PATENT PRACTITIONER							
Signature <u>/Mingji Jin/</u>				Date <u>April 9, 2014</u>			
Name <u>Mingji Jin</u>				Registration No. <u>69,674</u>			

Electronic Patent Application Fee Transmittal				
Application Number:		13912845		
Filing Date:		07-Jun-2013		
Title of Invention:		SUPPLY VOLTAGE GENERATING CIRCUIT		
First Named Inventor/Applicant Name:		Koichiro HAYASHI		
Filer:		Carl Joseph Pellegrini/Catherine Merino		
Attorney Docket Number:		Q204830		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for Continued Examination	1801	1	1200	1200
Total in USD (\$)				1200

Electronic Acknowledgement Receipt	
EFS ID:	18720049
Application Number:	13912845
International Application Number:	
Confirmation Number:	5774
Title of Invention:	SUPPLY VOLTAGE GENERATING CIRCUIT
First Named Inventor/Applicant Name:	Koichiro HAYASHI
Customer Number:	23373
Filer:	Carl Joseph Pellegrini/Catherine Merino
Filer Authorized By:	Carl Joseph Pellegrini
Attorney Docket Number:	Q204830
Receipt Date:	09-APR-2014
Filing Date:	07-JUN-2013
Time Stamp:	17:20:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1200
RAM confirmation Number	3893
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1		Q204830Amendment114RCE.pdf	62269 2b58d0496dcb0f5156ddd8b00e129dc8f0f61904	yes	9
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment Submitted/Entered with Filing of CPA/RCE		1	1	
	Claims		2	6	
	Applicant Arguments/Remarks Made in an Amendment		7	8	
	Request for Continued Examination (RCE)		9	9	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30432 e435f238a244fb0e1176cf4278de4163bdf5508	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			92701		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	Docket No: Q204830
Koichiro HAYASHI, et al.	
Appln. No.: 13/912,845	Group Art Unit: 2842
Confirmation No.: 5774	Examiner: ALMO, KHAREEM E
Filed: June 7, 2013	
For: SUPPLY VOLTAGE GENERATING CIRCUIT	

AMENDMENT UNDER 37 C.F.R. § 1.114(c)

MAIL STOP RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated January 9, 2014, please amend the above-identified application as follows on the accompanying pages.

TABLE OF CONTENTS

AMENDMENTS TO THE CLAIMS	2
REMARKS	7

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A semiconductor device comprising:
 - first and second voltage terminals to be respectively supplied with first and second voltages different from each other;
 - an internal voltage node;
 - a switching circuit coupled between the first and second voltage terminals and the internal voltage node, the switching circuit to take either one of a first switching state in which the first voltage terminal and the internal voltage node are connected and a second switching state in which the second voltage terminal and the internal voltage node are connected; and
 - a voltage booster circuit including a voltage output node and first and second boosting ~~circuit-circuits~~ each including a capacitor and each coupled to the internal voltage node, the voltage booster circuit being configured such that the first and second voltage boosting circuits are coupled in series to the voltage output node when the switching circuit takes the first switching state and that the first boosting circuit is coupled to the voltage output node and the second boosting circuit is disconnected from each of the first boosting circuit and the voltage output node when the switching circuit takes the second switching state, and
at least when the switching circuit takes a switching state, the capacitor of the first boosting circuit is coupled to the voltage output node and the capacitor of the second boosting

circuit is disconnected from each of the voltage output node and the capacitor of the first boosting circuit.

2. (previously presented) The semiconductor device as claimed in claim 1, further comprising a first external voltage terminal to be supplied with the first voltage, the first external voltage terminal coupled to the first voltage terminal.

3. (previously presented) The semiconductor device as claimed in claim 2, further comprising a second external voltage terminal to be supplied with a third voltage and an internal voltage generator coupled to the second external voltage terminal to also be supplied with the third voltage and configured to generate the second voltage at the second voltage terminal.

4. (original) The semiconductor device as claimed in claim 3, wherein the third voltage is greater than the first voltage.

5. (original) The semiconductor device as claimed in claim 4, wherein the third voltage is greater than the second voltage.

6. (original) The semiconductor device as claimed in claim 1, wherein the second boosting circuit is configured to boost the first voltage supplied with the internal voltage node to generate a first boosting voltage and the first boosting circuit is configured to boost the first boosting voltage to generate at the voltage output node a second boosting voltage when the switching circuit takes the first switching state.

7. (original) The semiconductor device as claimed in claim 6, wherein the first boosting circuit is configured to boost the second voltage supplied with the internal voltage node to generate at the voltage output node a third boosting voltage when the switching circuit takes the second switching state.

8. (canceled).

9. (canceled).

10. (new) A method for generating a supply voltage, comprising:

providing, from a first voltage terminal and a second voltage terminal, first voltage and second voltage different from each other;

selecting, by a switching circuit coupled between the first voltage terminal and the second voltage terminal, either one of a first switching state in which the first voltage terminal and an internal voltage node are connected and a second switching state in which the second voltage terminal and the internal voltage node are connected; and

outputting, by a voltage booster circuit including first boosting circuit and second boosting circuit, either one of a first boosted voltage generated by coupling the first boosting circuit and the second boosting circuit in series to a voltage output node at the first switching state and a second boosted voltage generated by coupling the first boosting circuit to the voltage output node and disconnecting the second boosting circuit from each of the first boosting circuit and the voltage output node at the second switching state, and

the first and second boosting circuits being such that, at least when the switching circuit takes a switching state, a capacitor of the first boosting circuit is coupled to the voltage output node and a capacitor of the second boosting circuit is disconnected from each of the voltage output node and the capacitor of the first boosting circuit.

11. (new) The method of claim 10, further comprising a first external voltage terminal to be supplied with the first voltage, the first external voltage terminal coupled to the first voltage terminal.

12. (new) The method of claim 11, further comprising a second external voltage terminal to be supplied with a third voltage and an internal voltage generator coupled to the second external voltage terminal to also be supplied with the third voltage and configured to generate the second voltage at the second voltage terminal.

13. (new) The method of claim 12, wherein the third voltage is greater than the first voltage.

14. (new) The method of claim 13, wherein the third voltage is greater than the second voltage.

15. (new) The method of claim 10, wherein the second boosting circuit is configured to boost the first voltage supplied with the internal voltage node to generate a first boosting voltage and the first boosting circuit is configured to boost the first boosting voltage to generate at the

voltage output node a second boosting voltage when the switching circuit takes the first switching state.

16. (new) The method of claim 15, wherein the first boosting circuit is configured to boost the second voltage supplied with the internal voltage node to generate at the voltage output node a third boosting voltage when the switching circuit takes the second switching state.

REMARKS

By this Amendment, Applicant amends claim 1, cancels claims 8-9 without prejudice or disclaimer, and adds new claims 10-16. Thus, claims 1-7 and 10-16 are all the claims pending in the application. Reconsideration and allowance of the subject application are respectfully requested.

I. Allowable Subject Matter

Claim 9 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant thanks the Examiner for indicating the allowability of claim 9.

II. Claim Rejections under 35 U.S.C. § 102

Claims 1-8 are rejected under pre-AIA 35 U.S.C. § 102(b) as allegedly being anticipated by Kim (US 20050047180).

Applicant amends independent claim 1 to recite features of dependent claim 9 that, in view of the Examiner's statements found on p.7 of the Final Office Action to explain allowability of claim 9, Applicant interprets and submits will make claim 1 allowable.

Accordingly, Applicant respectfully submits that the amended claim 1 is patentable.

Applicant respectfully submits that dependent claims 2-7 are patentable at least by virtue of their respective dependencies.

III. New Claims

To provide varied protection, Applicant adds new claims 10-16. The new claims are supported by the present specification. No new matter is added.

Newly added independent claim 10 recites features that are similar to those of claim 1.

Accordingly, Applicant respectfully submits that claim 10 is patentable for the reasons similar to those discussed above with regard to claim 1.

Applicant respectfully submits that dependent claims 11-16 are patentable by virtue of their respective dependencies and also additional features as set therein.

IV. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

SUGHRUE MION, PLLC
Telephone: 202.293.7060
Facsimile: 202.293.7860

WASHINGTON OFFICE

23373

CUSTOMER NUMBER

Date: April 9, 2014

/Mingji Jin/
Mingji Jin
Registration No. 69,674

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 13/912,845	Filing Date 06/07/2013	☐ To be Mailed	
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO							
APPLICATION AS FILED – PART I							
(Column 1)		(Column 2)					
FOR	NUMBER FILED	NUMBER EXTRA			RATE (\$)	FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A			N/A		
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A			N/A		
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A			N/A		
TOTAL CLAIMS (37 CFR 1.16(j))	minus 20 =	*			X \$ =		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*			X \$ =		
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.					TOTAL		
APPLICATION AS AMENDED – PART II							
(Column 1)		(Column 2)		(Column 3)			
AMENDMENT	04/09/2014	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 14	Minus	** 20	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
TOTAL ADD'L FEE						0	
(Column 1)		(Column 2)		(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
TOTAL ADD'L FEE							
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.							

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/912,845	06/07/2013	Koichiro HAYASHI	Q204830	5774

23373	7590	01/09/2014
SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037		

EXAMINER	
ALMO, KHAREEM E	

ART UNIT	PAPER NUMBER
2842	

NOTIFICATION DATE	DELIVERY MODE
01/09/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PPROCESSING@SUGHRUE.COM
sughrue@sughrue.com
USPTO@sughrue.com

Office Action Summary	Application No. 13/912,845	Applicant(s) HAYASHI ET AL.	
	Examiner KHAREEM E. ALMO	Art Unit 2842	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12/12/2013.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-9 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-8 is/are rejected.
- 8) ☒ Claim(s) 9 is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 6/7/2013 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☒ All b) ☐ Some** c) ☐ None of the:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date ____.
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 4) ☐ Other: ____.

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

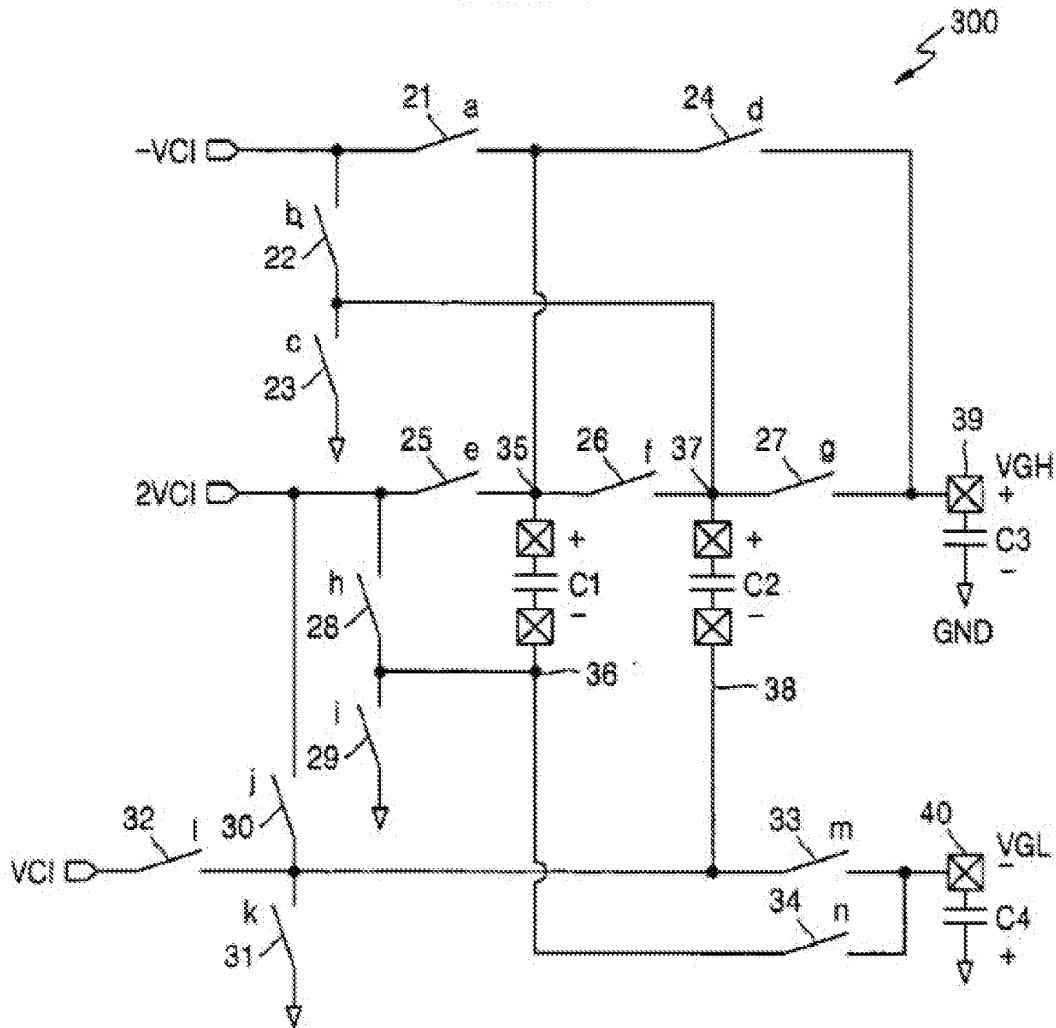
Claim Rejections - 35 USC § 102

2. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-8 are rejected under pre-AIA 35 U.S.C. 102b as being anticipated by Kim (US 20050047180).

FIG. 3



4. With respect to claim 1, figure 3 of Kim discloses a semiconductor device comprising: first and second voltage terminals to be respectively supplied with first (V_{CI}) and second ($-V_{CI}$) voltages different from each other; an internal voltage node ($2V_{CI}$); a switching circuit (a-n) coupled between the first and second voltage terminals and the internal voltage node, the switching circuit to take either one of a first switching state (+)

in which the first voltage terminal and the internal voltage node are connected and a second switching state (-) in which the second voltage terminal and the internal voltage node are connected; and a voltage booster circuit (C1 - C4) including a voltage output node (at 37 or 38) and first (C1) and second (C2) boosting circuit each coupled to the internal voltage node, the voltage booster circuit being configured such that the first and second voltage boosting circuits are coupled in series to the voltage output node when the switching circuit takes the first switching state and that the first boosting circuit coupled to the voltage output node and the second boosting circuit is disconnected from each of the first boosting circuit and the voltage output node when the switching circuit takes the second switching state.

With respect to claim 2, Kim discloses the semiconductor device as claimed in claim 1, further comprising a first external voltage terminal (37) to be supplied with the first voltage, the first external voltage terminal coupled to the first voltage terminal.

With respect to claim 3, Kim discloses the semiconductor device as claimed in claim 2, further comprising a second external voltage terminal (38) to be supplied with a third voltage and an internal voltage generator coupled (220) to the second external voltage terminal to also be supplied with the third voltage and configured to generate the second voltage at the second voltage terminal.

With respect to claim 4, the circuit above discloses the semiconductor device as claimed in claim 3, wherein the third voltage (VGH+) is greater than the first voltage (VCI+).

With respect to claim 5, the circuit above discloses the semiconductor device as claimed in claim 4, wherein the third voltage (V_{GH+}) is greater than the second voltage (V_{CL-}).

With respect to claim 6, the circuit above discloses the semiconductor device as claimed in claim 1, wherein the second boosting circuit (C2) is configured to boost the first voltage supplied with the internal voltage node to generate a first boosting voltage (V_{GH+}) and the first boosting circuit (C1) is configured to boost the first boosting voltage to generate at the voltage output node a second boosting voltage (V_{GL-}) when the switching circuit takes the first switching state.

With respect to claim 7, the circuit above discloses the semiconductor device as claimed in claim 6, wherein the first boosting circuit (C1) is configured to boost the second voltage supplied with the internal voltage node (V_{CL-}) to generate at the voltage output node a third boosting voltage (V_{GH+}) when the switching circuit takes the second switching state.

With respect to claim 8, the circuit above discloses the semiconductor device as claimed in claim 1, wherein each of the first and second boosting circuits includes a capacitor and the capacitors of the first and second boosting circuits are coupled in series to the voltage output node when the switching circuit takes the first switching state.

Response to Arguments

5. Applicant's arguments filed 12/12/2013 have been fully considered but they are not persuasive.

With respect to claim applicant's argument that "node 37 and 38" are for boosting of the input voltage not for outputting of boosted voltage, the examiner points out that an output can be taken at any node. Secondly the output can be local (i.e. boosting the input voltage can be a local output). Thirdly, the circuit merely needs to be capable of producing a voltage output, which it is. Finally, nodes 37 and 38 are the same nodes as 39 and 40 when 27 and 33 are closed.

With respect to applicant's argument, considering all possible routes, Kim does not disclose or suggest the feature that "the voltage booster circuit being configured such that the first and second voltage boosting circuits are coupled in series to the voltage output node when the switching circuit takes the first switching state." the examiner disagrees. When 26 is closed, during a first switching state C1 and C2 are connected in series (see figure 5, when f is closed and the output node is indeed at 37 and 38) Further note, that 37 and 38 are the same nodes as 39 and 40 when the switches are closed outputting the stored voltage.

With respect to applicant's argument that C1 and C2 are coupled in parallel to the voltage output nodes 39 and 40, the examiner disagrees, C1 and C2 are not coupled at two nodes at the time of the switching states.

Allowable Subject Matter

6. Claim 9 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 9, the prior art of record fails to suggest or disclose wherein the capacitor of the first boosting circuit is coupled to the voltage output node and the capacitor of the second boosting circuit is disconnected from each of the voltage output node and the capacitor of the first boosting circuit.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHAREEM E. ALMO whose telephone number is (571)272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on (571) 272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KHAREEM E. ALMO/
Examiner, Art Unit 2816
/Lincoln Donovan/
Supervisory Patent Examiner, Art Unit 2816

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	Docket No: Q204830
Koichiro HAYASHI, et al.	
Appln. No.: 13/912,845	Group Art Unit: 2842
Confirmation No.: 5774	Examiner: ALMO, KHAREEM E
Filed: June 7, 2013	
For: SUPPLY VOLTAGE GENERATING CIRCUIT	

AMENDMENT UNDER 37 C.F.R. § 1.111

MAIL STOP AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated September 13, 2013, please amend the above-identified application as follows on the accompanying pages.

TABLE OF CONTENTS

AMENDMENTS TO THE CLAIMS	2
REMARKS	5

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A semiconductor device comprising:
 - first and second voltage terminals to be respectively supplied with first and second voltages different from each other;
 - an internal voltage node;
 - a switching circuit coupled between the first and second voltage terminals and the internal voltage node, ~~taking the switching circuit to take~~ either one of a first switching state in which the first voltage terminal and the internal voltage node are connected and a second switching state in which the second voltage terminal and the internal voltage node are connected; and
 - a voltage booster circuit including a voltage output node and first and second boosting circuit each coupled to the internal voltage node, the voltage booster circuit being configured such that the first and second voltage boosting circuits are coupled in series to the voltage output node when the switching circuit takes the first switching state and that the first boosting circuit coupled to the voltage output node and the second boosting circuit is disconnected from each of the first boosting circuit and the voltage output node when the switching circuit takes the second switching state.

2. (currently amended) The semiconductor device as claimed in claim 1, further comprising a first external voltage terminal to be supplied with the first voltage, the first external voltage terminal coupled to the first voltage terminal.

3. (currently amended) The semiconductor device as claimed in claim 2, further comprising a second external voltage terminal to be supplied with a third voltage and an internal voltage generator coupled to the second external voltage terminal to also be supplied with the third voltage and configured to generate the second voltage at the second voltage terminal.

4. (original) The semiconductor device as claimed in claim 3, wherein the third voltage is greater than the first voltage.

5. (original) The semiconductor device as claimed in claim 4, wherein the third voltage is greater than the second voltage.

6. (original) The semiconductor device as claimed in claim 1, wherein the second boosting circuit is configured to boost the first voltage supplied with the internal voltage node to generate a first boosting voltage and the first boosting circuit is configured to boost the first boosting voltage to generate at the voltage output node a second boosting voltage when the switching circuit takes the first switching state.

7. (original) The semiconductor device as claimed in claim 6, wherein the first boosting circuit is configured to boost the second voltage supplied with the internal voltage node to

generate at the voltage output node a third boosting voltage when the switching circuit takes the second switching state.

8. (currently amended) The semiconductor device as claimed in claim 1, wherein each of the first and second boosting circuits includes a capacitor and the capacitors of the first and second boosting circuits are coupled in series to the voltage output node when the switching circuit takes the first switching state.

9. (original) The semiconductor device as claimed in claim 8, wherein the capacitor of the first boosting circuit is coupled to the voltage output node and the capacitor of the second boosting circuit is disconnected from each of the voltage output node and the capacitor of the first boosting circuit.

REMARKS

Claims 1-9 are all the claims pending in the application. By this Amendment, Applicant amends claims 1-3 and 8. Reconsideration and allowance of the subject application are respectfully requested.

I. Claim Rejections under 35 U.S.C. § 102

Claims 1-8 are rejected under pre-AIA 35 U.S.C. § 102b as allegedly being anticipated by Kim (US 20050047180).

Applicant respectfully traverses the rejections.

Applicant respectfully submits that independent claim 1 is patentable because Kim does not disclose or suggest each and every element of claim 1.

Independent claim 1 recites as follows (emphasis added):

A semiconductor device comprising:
first and second voltage terminals to be respectively supplied with first and second voltages different from each other;
an internal voltage node;
a switching circuit coupled between the first and second voltage terminals and the internal voltage node, the switching circuit to take either one of a first switching state in which the first voltage terminal and the internal voltage node are connected and a second switching state in which the second voltage terminal and the internal voltage node are connected; and
a voltage booster circuit including a voltage output node and first and second boosting circuit each coupled to the internal voltage node, the voltage booster circuit being configured such that the first and second voltage boosting circuits are coupled in series to the voltage output node when the switching circuit takes the first switching state and that the first boosting circuit coupled to the voltage output node and the second boosting circuit is disconnected from each of the first boosting circuit and the voltage output node when the switching circuit takes the second switching state.

Applicant submits that that Kim does not disclose or suggest at least the feature "the voltage booster circuit being configured such that the first and second voltage boosting circuits

are coupled in series to the voltage output node when the switching circuit takes the first switching state", as recited in claim 1. At pages 3-4 of the Office Action, the Examiner asserts that Kim discloses the above noted feature in FIG. 3. Applicant respectfully disagrees for the following reasons.

First of all, at page 4 of the Office Action, the Examiner asserts that the "node 37 and 38" of Kim correspond to the "voltage output node" as recited in claim 1. This is incorrect.

As shown in FIG. 3 of Kim, the node 37 and node 38 are two nodes that connect the capacitor C2. However, capacitor C2 is for boosting of input voltage, not for outputting of boosted voltage. Therefore, on the contrary to the Examiner's assertion, node 37 and node 38 are not voltage output nodes. Instead, as described in paragraph [0056], node 39 and node 40 are the voltage output nodes in Kim.

In addition, at page 3 of the Office Action, the Examiner asserts that VCl and 2VCl, as shown in FIG. 3 of Kim, respectively correspond to the first voltage terminal and the internal voltage node as recited in claim 1. In this scenario, "the first switching state in which the first voltage terminal and the internal voltage node are connected", as recited in claim 1, corresponds to the state that the VCl and the 2VCl are connected, which has several different routes by connecting different switches. For example, one of the routes is the connection between the VCl and the 2VCl by switch j (30) (FIG. 3).

Even considering all the possible routes corresponding to the above alleged first switching state, however, Kim does not disclose or suggest the feature that "the voltage booster circuit being configured such that the first and second voltage boosting circuits are coupled in series to the voltage output node when the switching circuit takes the first switching state", as recited in claim 1.

Kim discloses a boosting power supply unit including a boosting circuit having a small number of externally-mounted capacitors, which generate stepped-up and stepped-down boosted voltages through charging and pumping under two-phase control, so that the simultaneous output of the stepped-up voltage and the stepped-down voltage, the output of only the stepped-up voltage, the output of only the stepped-down voltage. At page 4 of the Office Action, the Examiner interprets the first voltage boosting circuit and the second voltage boosting circuit, as recited in claim 1, as being equivalent to the C1 and C2 of Kim. However, as shown in FIG. 3 of Kim, C1 and C2 are not coupled in series to the voltage output node 39 or 40. Rather, C1 and C2 are coupled in parallel to the voltage output node 39 or 40. This is the case because in Kim, as shown in FIG. 3 and also described in paragraph [0057], different capacitors are configured to respond to different logic states of a control signal by selectively connecting switches that connect the nodes of the different capacitors. For this purpose, the capacitors need to be coupled in parallel to the voltage output node.

In contrast, claim 1 recites that the voltage booster circuit being configured such that the first and second voltage boosting circuits are coupled in series to the voltage output node when the switching circuit takes the first switching state. For example, but not by way of limitation, as shown in FIG. 1 and also described in paragraph [0024] of the present specification, the booster circuit 21a and the booster circuit 21b are coupled in series by turning the switch SW2 ON, that is, the booster circuit 21b further boosts the power that has been already boosted in the booster circuit 21a. Therefore, as described in paragraph [0019] of the present specification, the number of booster stages (e.g., one stage or two stages) constituted by the multiple booster circuits 21a and 21b is changed over by the switch element SW2 in accordance with the power-supply

voltage applied to the booster 20. For this purpose, the booster circuits 21a and 21b are better to be coupled in series to the voltage output node.

From the discussions above, it is quite clear that the operation and intended purpose of Kim's booster circuit are different than that of the present application. Consequently, Kim discloses a booster circuit configuration that is different than that of the claimed invention. Nowhere does Kim disclose the feature "the voltage booster circuit being configured such that the first and second voltage boosting circuits are coupled in series to the voltage output node when the switching circuit takes the first switching state and that the first boosting circuit coupled to the voltage output node and the second boosting circuit is disconnected from each of the first boosting circuit and the voltage output node when the switching circuit takes the second switching state", as recited in claim 1.

Accordingly, Applicant respectfully submits that independent claim 1 is patentable because Kim does not disclose or suggest all of the features of claim 1.

Applicant respectfully submits that dependent claims 2-8 are patentable *at least* by virtue of their respective dependencies.

III. Allowable Subject Matter

Claim 9 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant thanks the Examiner for indicating the allowability of claim 9 but holds in abeyance of its rewriting in independent form until the Examiner has chance to consider the remarks presented above with regard to independent claim 1.

IV. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,
/ Carl J. Pellegrini /

SUGHRUE MION, PLLC
Telephone: 202.293.7060
Facsimile: 202.293.7860

Carl J. Pellegrini
Registration No. 40,766

WASHINGTON OFFICE

23373

CUSTOMER NUMBER

Date: December 12, 2013

Electronic Acknowledgement Receipt	
EFS ID:	17645671
Application Number:	13912845
International Application Number:	
Confirmation Number:	5774
Title of Invention:	SUPPLY VOLTAGE GENERATING CIRCUIT
First Named Inventor/Applicant Name:	Koichiro HAYASHI
Customer Number:	23373
Filer:	Carl Joseph Pellegrini/Catherine Merino
Filer Authorized By:	Carl Joseph Pellegrini
Attorney Docket Number:	Q204830
Receipt Date:	12-DEC-2013
Filing Date:	07-JUN-2013
Time Stamp:	16:48:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Q204830Amendment111.pdf	69922 ee0413f7167585c6aba5f159f0d7d91b10ef3521	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	4
	Applicant Arguments/Remarks Made in an Amendment	5	9
Warnings:			
Information:			
Total Files Size (in bytes):		69922	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 13/912,845		Filing Date 06/07/2013		☐ To be Mailed				
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO													
APPLICATION AS FILED – PART I													
(Column 1)			(Column 2)										
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)					
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A							
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))		N/A		N/A		N/A							
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A							
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*		X \$ =							
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*		X \$ =							
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).											
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))													
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL							
APPLICATION AS AMENDED – PART II													
(Column 1)			(Column 2)			(Column 3)							
AMENDMENT	12/12/2013		CLAIMS REMAINING AFTER AMENDMENT			HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))		* 9		Minus	** 20		= 0		X \$80 =		0	
	Independent (37 CFR 1.16(h))		* 1		Minus	***3		= 0		X \$420 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))												
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))												
	TOTAL ADD'L FEE											0	
(Column 1)			(Column 2)			(Column 3)							
AMENDMENT			CLAIMS REMAINING AFTER AMENDMENT			HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))		*		Minus	**		=		X \$ =			
	Independent (37 CFR 1.16(h))		*		Minus	***		=		X \$ =			
	☐ Application Size Fee (37 CFR 1.16(s))												
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))												
	TOTAL ADD'L FEE												
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.													

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/912,845	06/07/2013	Koichiro HAYASHI	Q204830

CONFIRMATION NO. 5774

23373
SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

PUBLICATION NOTICE



OC000000064321289

Title:SUPPLY VOLTAGE GENERATING CIRCUIT

Publication No.US-2013-0265103-A1

Publication Date:10/10/2013

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Docket No: Q204830

Koichiro HAYASHI, et al.

Appln. No.: 13/912,845

Group Art Unit: 2816

Confirmation No.: 5774

Examiner: ALMO, KHAREEM E

Filed: June 7, 2013

For: SUPPLY VOLTAGE GENERATING CIRCUIT

SUBMISSION OF EXECUTED DECLARATION

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In Response to the Notice mailed July 5, 2013, Applicant submits herewith a copy of the Declaration (3 pages) properly executed by the inventors for the above identified application.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,
/ Carl J. Pellegrini /

SUGHRUE MION, PLLC
Telephone: 202.293.7060
Facsimile: 202.293.7860

Carl J. Pellegrini
Registration No. 40,766

WASHINGTON OFFICE

23373

CUSTOMER NUMBER

Date: October 1, 2013

DECLARATION FOR PATENT APPLICATION (37 CFR 1.63)

特許出願宣言書(37 CFR 1.63)

Japanese Language Declaration

私は、下記に記載の発明者として、以下の通り宣言します。

本宣言書は、以下に關します。

☐ 添付の出願書、または、

☐ _____年__月__日に提出された米国出願あるいはPCT
国際出願番号_____

本件出願の名称は、以下の通りです。

上記に明示された出願は、私が作成した、または作成を許可したものです。

私は、本件出願において請求項に記載された発明の本来の発明者、または、本来の共同発明者であると信じています。

私は、本宣言書の提出に関わる本件出願の内容を検討し、理解しています。

私は、37 CFR 1.56に定義されるように、自身が知る全ての特許性に関する重要な情報を、米国特許商標庁に開示する義務があることを認識しています。

私は、本宣言書において故意に虚偽の供述を行った場合、18 USC 1001に基づき、罰金あるいは5年以下の懲役、または両方による処罰の対象となることを認識しています。

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States Application or PCT International Application
Number 13/912,845 filed on June 7, 2013.

The application is entitled:

SUPPLY VOLTAGE GENERATING CIRCUIT

The above identified application was made or was authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I have reviewed and understand the contents of the application for which this declaration is being submitted.

I am aware of the duty to disclose to the Office all information known to me to be material to patentability as defined in 37 CFR 1.56.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 USC 1001 by fine or imprisonment of not more than five (5) years, or both.

Japanese Language Declaration

参加管轄官庁に対する出願へのアクセス許可

☐ 印を付けた場合、下記の署名者は本書をもって、米国特許商標庁が、ヨーロッパ特許庁 (EPO)、日本特許庁 (JPO)、韓国知的所有権庁 (KIPO)、世界知的所有権機関 (WIPO)、および上記の出願に基づく優先権を主張する外国出願が提出されたその他の知的所有権管轄官庁に、上記の特許出願へのアクセス権を付与することを許可します。37 CFR 1.14(c)および(h)を参照。出願人が、EPO、JPO、KIPO、または上記の出願に基づく優先権を主張する外国出願が提出されたその他の知的所有権管轄官庁に対して、上記の出願へのアクセス権を付与することを希望しない場合には、この欄には印を付けないでください。

下記の署名者は、37 CFR 1.14(h)(3)に従い、1) 上記の出願時の特許出願、2) 35 USC 119(a)~(d)に従って、上記出願が優先権を主張するいずれの外国出願、(37 CFR 1.55の認証謄本の要件を満たす外国出願の写し上記の特許出願で提出された場合)、ならびに3) 上記の特許出願について、それによる利益を享受するいずれの出願時の米国出願に関して、出願時の出願書の写しへのアクセス権を付与します。

下記の署名者は、37 CFR 1.14(c)に従い、参加管轄官庁に対する出願へのアクセス許可の提出日に関する情報へのアクセス権を付与します。

本件出願についての全ての連絡事項は、下記にある米国特許商標庁顧客番号のもとで提出された住所まで直接お送りください。

Authorization To Permit Access To Application by Participating Office

☒ If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the above-identified application is filed access to the above-identified patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, or other intellectual property office in which a foreign application claiming priority to the above-identified application is filed to have access to the application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the application-as-filed with respect to: 1) the above-identified patent application-as-filed, 2) any foreign application to which the above-identified application claims priority under 35 USC 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the above-identified patent application, and 3) any U.S. application-as-filed from which benefit is sought in the above-identified patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing the Authorization to Permit Access to Application by Participating Office.

Direct all correspondence about the application to the address filed under the USPTO Customer Number below.

STATEMENT OF ACCURATE TRANSLATION IN ACCORDANCE WITH 37 CFR 1.69(b):

The declaration is an accurate translation of the corresponding English language declaration.

Signature

Date

9/28/2012

WASHINGTON OFFICE

23373

CUSTOMER NUMBER

電話連絡は下記へ：

SUGHRUE MION, PLLC
202.293.7060

Direct Telephone Calls to:

SUGHRUE MION, PLLC
202.293.7060

NAME OF SOLE OR FIRST INVENTOR: 唯一あるいは第一の発明者名		
Given Name (first and middle [if any]) 名 (名およびミドルネーム[該当する場合])	Family Name or Surname 姓	
Koichiro	HAYASHI	
Inventor's signature 発明者の署名	<i>Koichiro Hayashi</i>	Date 日付 August 27, 2013
Residence: 住所: Tokyo, Japan		
Mailing Address: 郵送先: c/o Elpida Memory, Inc., 2-1, Yaesu 2-chome, Chuo-ku, Tokyo, Japan		
NAME OF SECOND INVENTOR: 第二の発明者名:		
Given Name (first and middle [if any]) 名 (名およびミドルネーム[該当する場合])	Family Name or Surname 姓	
Hitoshi	TANAKA	
Inventor's signature 発明者の署名	<i>Hitoshi Tanaka</i>	Date 日付 August 27, 2013
Residence: 住所: Ome, Japan		
Mailing Address: 郵送先: c/o Hitachi ULSI Systems Co., Ltd., 22-1, Josuihoncho 5-chome, Kodaira-shi, Tokyo, 187-8522, Japan		

Electronic Acknowledgement Receipt	
EFS ID:	17007431
Application Number:	13912845
International Application Number:	
Confirmation Number:	5774
Title of Invention:	SUPPLY VOLTAGE GENERATING CIRCUIT
First Named Inventor/Applicant Name:	Koichiro HAYASHI
Customer Number:	23373
Filer:	J. Lytle/Alexander Cimon
Filer Authorized By:	J. Lytle
Attorney Docket Number:	Q204830
Receipt Date:	01-OCT-2013
Filing Date:	07-JUN-2013
Time Stamp:	14:30:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	Q204830TransmittalDeclaration.pdf	121448 84ce3b6d60e7ee91dfed360a19f502fad6cd944b	no	4

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/912,845	06/07/2013	Koichiro HAYASHI	Q204830	5774

23373	7590	09/13/2013
SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037		

EXAMINER	
ALMO, KHAREEM E	

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
09/13/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PPROCESSING@SUGHRUE.COM
sughrue@sughrue.com
USPTO@sughrue.com

Office Action Summary	Application No. 13/912,845	Applicant(s) HAYASHI ET AL.	
	Examiner KHAREEM E. ALMO	Art Unit 2816	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on papers filed 6/7/2013.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 5) ☒ Claim(s) 1-9 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-8 is/are rejected.
- 8) ☒ Claim(s) 9 is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 6/7/2013 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☒ All b) ☐ Some * c) ☐ None of the:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 6/7/2013
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____
- 4) ☐ Other: ____

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

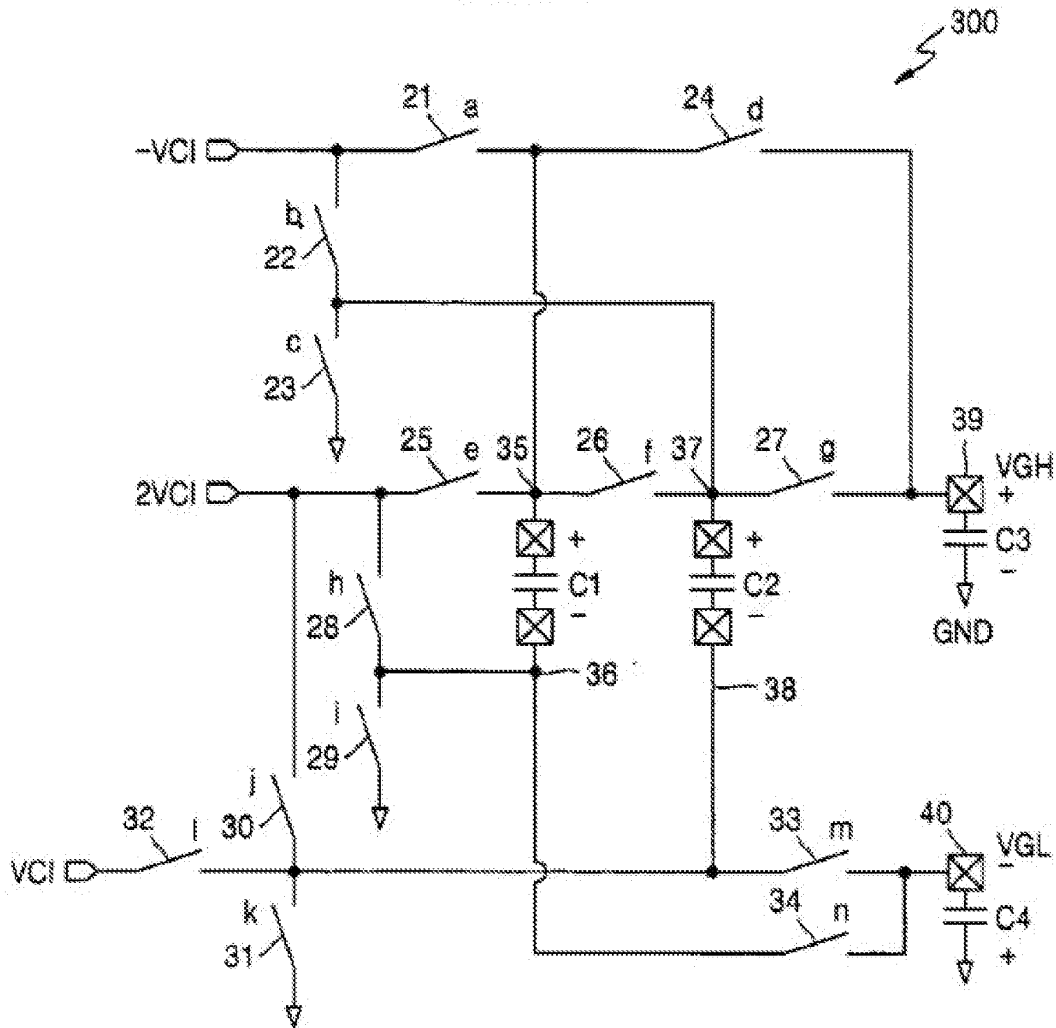
Claim Rejections - 35 USC § 102

2. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-8 are rejected under pre-AIA 35 U.S.C. 102b as being anticipated by Kim (US 20050047180).

FIG. 3



4. With respect to claim 1, figure 3 of Kim discloses a semiconductor device comprising: first and second voltage terminals respectively supplied with first (VCI) and second (-VCI) voltages different from each other; an internal voltage node (2VCI); a switching circuit (a-n) coupled between the first and second voltage terminals and the internal voltage node, taking either one of a first switching state (+) in which the first

voltage terminal and the internal voltage node are connected and a second switching state (-) in which the second voltage terminal and the internal voltage node are connected; and a voltage booster circuit (C1 - C4) including a voltage output node (at 37 or 38) and first (C1) and second (C2) boosting circuit each coupled to the internal voltage node, the voltage booster circuit being configured such that the first and second voltage boosting circuits are coupled in series to the voltage output node when the switching circuit takes the first switching state and that the first boosting circuit coupled to the voltage output node and the second boosting circuit is disconnected from each of the first boosting circuit and the voltage output node when the switching circuit takes the second switching state.

With respect to claim 2, Kim discloses the semiconductor device as claimed in claim 1, further comprising a first external voltage terminal (37) supplied with the first voltage, the first external voltage terminal coupled to the first voltage terminal.

With respect to claim 3, Kim discloses the semiconductor device as claimed in claim 2, further comprising a second external voltage terminal (38) supplied with a third voltage and an internal voltage generator coupled (220) to the second external voltage to be supplied with the third voltage and configured to generate the second voltage at the second voltage terminal.

With respect to claim 4, the circuit above discloses the semiconductor device as claimed in claim 3, wherein the third voltage (V_{GH+}) is greater than the first voltage (V_{CI+}).

With respect to claim 5, the circuit above discloses the semiconductor device as claimed in claim 4, wherein the third voltage (V_{GH+}) is greater than the second voltage(V_{CL-}).

With respect to claim 6, the circuit above discloses the semiconductor device as claimed in claim 1, wherein the second boosting circuit (C2) is configured to boost the first voltage supplied with the internal voltage node to generate a first boosting voltage (V_{GH+}) and the first boosting circuit (C1) is configured to boost the first boosting voltage to generate at the voltage output node a second boosting voltage (V_{GL-}) when the switching circuit takes the first switching state.

With respect to claim 7, the circuit above discloses the semiconductor device as claimed in claim 6, wherein the first boosting circuit (C1) is configured to boost the second voltage supplied with the internal voltage node (V_{CL-}) to generate at the voltage output node a third boosting voltage (V_{GH+}) when the switching circuit takes the second switching state.

With respect to claim 8, the circuit above discloses the semiconductor device as claimed in claim 1, wherein each of the first and second boosting circuits includes a capacitor and the capacitors of the first and second boosting circuits coupled in series to the voltage output node when the switching circuit takes the first switching state.

Allowable Subject Matter

5. Claim 9 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 9, the prior art of record fails to suggest or disclose wherein the capacitor of the first boosting circuit is coupled to the voltage output node and the capacitor of the second boosting circuit is disconnected from each of the voltage output node and the capacitor of the first boosting circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHAREEM E. ALMO whose telephone number is (571)272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on (571) 272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KHAREEM E. ALMO/
Examiner, Art Unit 2816
/Lincoln Donovan/
Supervisory Patent Examiner, Art Unit 2816

Notice of References Cited	Application/Control No. 13/912,845	Applicant(s)/Patent Under Reexamination HAYASHI ET AL.	
	Examiner KHAREEM E. ALMO	Art Unit 2816	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2005/0047180	03-2005	Kim, Hyoung-Rae	363/059
*	B	US-5,095,223	03-1992	Thomas, Alexander C.	307/110
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S52	4841	(327/535-537).OCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S53	1518	(363/59-60).OCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S54	2	("0000012").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S55	5881	S52 S53	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S56	4525	S55 and capacit\$4	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S57	4294	S56 and (transistor switch mos)	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S58	526	S57 and (booster)	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S59	238	S57 and (step adj down)	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S60	368	S57 and (gate near oxide)	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S61	2613	(327/536).OCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S62	0	("1and(by-passorbypass)").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S63	109	S61 and (by-pass or bypass)	US-PGPUB; USPAT; USOCR; JPO	OR	OFF	2013/09/06 12:28
S64	46	S63 and variable	US-PGPUB; USPAT; USOCR; JPO	OR	OFF	2013/09/06 12:28
S65	1	("20070139982").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S66	1	("6218818").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S67	1	("6504422").PN.	US-PGPUB; USPAT;	OR	OFF	2013/09/06 12:28

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S68	1	("20040017241").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S69	1	("20070024341").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S70	1	("7288984").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S71	7	("20020105312" "20060001474" "6392904" "6661683").PN. OR ("7288984").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
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S84	9396	(Vdd near vss)	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S85	6557	S84 and (capacit\$3 or boost\$3)	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S87	2085	S85 and (input adj terminal)	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S88	1685	S85 and ((input adj terminal) and (output adj terminal))	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S89	1566	S88 and (switch\$3 or select\$3)	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S90	4841	(327/535-537).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S91	1518	(363/59-60).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
S92	5881	S90 S91	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28

EAST Search History

S93	49	S92 and S89	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/06 12:28
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EAST Search History (Interference)

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Not for submission under 37 CFR 1.99)

Application Number	Not Yet Assigned
Confirmation Number	Not Yet Assigned
Filing Date	June 7, 2013
First Named Inventor	Koichiro HAYASHI
Art Unit	Not Yet Assigned
Examiner Name	ALMO, Khareem E. (parent)
Attorney Docket Number	Q204830

U.S. PATENTS

Examiner Initials	Cite No	Patent Number	Kind Code	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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/K.A./	20.	2005-158098	JP	A	2005-06-16	ELPIDA MEMORY INC.		
/K.A./	21.	2003249076	JP	A	2003-09-05	ELPIDA MEMORY INC. ET AL.		
/K.A./	22.	5259289	JP	A	1993-10-08	FUJITSU KK		
/K.A./	23.	11120784	JP	A	1999-04-30	TOSHIBA CORP.		

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. 2 Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). 3 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 4 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 5 Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED, EXCEPT WHERE LINED THROUGH. /K.A./

[Page 1 of 2]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	Not Yet Assigned
	Confirmation Number	Not Yet Assigned
	Filing Date	June 7, 2013
	First Named Inventor	Koichiro HAYASHI
	Art Unit	Not Yet Assigned
	Examiner Name	ALMO, Khareem E. (parent)
	Attorney Docket Number	Q204830

FOREIGN PATENT DOCUMENTS								
Examiner Initials	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
/K.A./	24.	2002237185	JP	A	2002-08-23	SANYO ELECTRIC CO.		
/K.A./	25.	200511475	JP	A	2005-01-13	MATSUSHITA ELECTRIC IND. CO.		

NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city, and/or country where published.	T
/K.A./	26.	Communication dated January 31, 2012 from the Japanese Patent Office in counterpart Japanese application no. 2007-081754	
/K.A./	27.	Non-final Office Action issued August 6, 2009 in Parent U.S. Application No. 12/052,422	N/A
/K.A./	28.	Non-final Office Action issued February 4, 2011 in Parent U.S. Application No. 12/052,422	N/A
/K.A./	29.	Non-final Office Action issued November 8, 2012 in Parent U.S. Application No. 12/052,422	N/A
/K.A./	30.	Final Office Action issued March 11, 2011 in Parent U.S. Application No. 12/052,422	N/A
/K.A./	31.	Final Office Action issued August 9, 2010 in Parent U.S. Application No. 12/052,422	N/A
/K.A./	32.	Final Office Action issued August 1, 2011 in Parent U.S. Application No. 12/052,422	N/A
/K.A./	33.	Advisory Action issued June 25, 2010 in Parent U.S. Application No. 12/052,422	N/A
/K.A./	34.	Advisory Action issued December 22, 2011 in Parent U.S. Application No. 12/052,422	N/A
/K.A./	35.	Notice of Allowance issued March 22, 2013 in Parent U.S. Application No. 12/052,422	N/A

EXAMINER SIGNATURE			
Examiner Signature	/Khareem Almo/	Date Considered	09/09/2013

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[Page 2 of 2]

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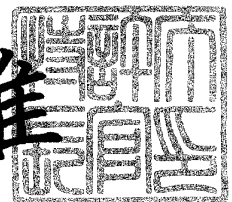
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【書類名】 特許請求の範囲

【請求項 1】

容量素子のチャージポンピングによって昇圧電圧を発生して出力する昇圧部と、
前記容量素子の耐圧範囲内の電圧に該外部電源の電圧を降圧して前記昇圧部の電源に与える電源降圧部と、

前記昇圧部の電源に前記外部電源を直接与えるか前記電源降圧部を介して与えるかを切り替えるスイッチ回路群と、

を備えることを特徴とする電源電圧発生回路。

【請求項 2】

前記容量素子を MOS トランジスタで構成し、該 MOS トランジスタのゲート酸化膜の厚さを、前記昇圧部の出力を電源とする負荷回路に含まれる MOS トランジスタのゲート酸化膜の厚さより薄くなるように構成することを特徴とする請求項 1 記載の電源電圧発生回路。

【請求項 3】

前記昇圧部は、多段の昇圧回路から構成され、該多段の昇圧回路のそれぞれに含まれる MOS トランジスタで構成される容量素子のゲート酸化膜の厚さが同一であることを特徴とする請求項 1 または 2 記載の電源電圧発生回路。

【請求項 4】

前記昇圧部は、前記多段の昇圧回路における昇圧段数を、前記昇圧部に与えられる電源電圧に応じて前記スイッチ回路群によって切り替えるように構成されることを特徴とする請求項 3 記載の電源電圧発生回路。

【請求項 5】

前記昇圧部は、前段および後段の昇圧回路を含み、

前記前段の昇圧回路は、前記外部電源の電位の二倍の電位と接地電位との間の振幅を有する第 1 の昇圧信号を生成し、

前記後段の昇圧回路は、前記電源降圧部の出力電位と接地電位との間の振幅を有する第 2 の昇圧信号、または前記第 1 の昇圧信号を入力し、

前記スイッチ回路群は、前記昇圧部の電源の接続先を、前記外部電源または前記電源降圧部の出力に切り替える第 1 のスイッチ素子と、前記後段の昇圧回路の入力の接続先を、前記第 1 または第 2 の昇圧信号に切り替える第 2 のスイッチ素子と、を含み、

前記第 1 のスイッチ素子が前記外部電源に切り替えられているときに前記第 2 のスイッチ素子が前記第 1 の昇圧信号に切り替えられ、前記第 1 のスイッチ素子が前記電源降圧部の出力に切り替えられているときに前記第 2 のスイッチ素子が前記第 2 の昇圧信号に切り替えられることを特徴とする請求項 4 記載の電源電圧発生回路。

【請求項 6】

前記昇圧部に与えられる電源電圧に応じて前記スイッチ回路群によって切り替えられて前記多段の昇圧回路における昇圧動作に不要となった容量素子を、前記スイッチ回路群によって接続して前記電源降圧部の出力安定用の容量素子として機能させるように構成することを特徴とする請求項 4 記載の電源電圧発生回路。

【請求項 7】

前記スイッチ回路群は、メタルオブション、ヒューズオブションおよびボンディングオブションのいずれかによって制御されることを特徴とする請求項 1、4、5、6 のいずれか一に記載の電源電圧発生回路。

【請求項 8】

請求項 1 乃至 7 のいずれか一に記載の電源電圧発生回路と、前記昇圧部の出力を電源とする負荷回路とを備える半導体記憶装置。

【書類名】明細書

【発明の名称】電源電圧発生回路

【技術分野】

【0001】

本発明は、電源電圧発生回路に係り、特に、半導体記憶装置の内部において昇圧電圧を発生する電源電圧発生回路に係る。

【背景技術】

【0002】

DRAMにおいて、仕様が大きく変更される場合や仕様が十分に固まっていない場合、ユーザからの要求で外部から供給される電源電圧が異なる場合がある。ワード線ドライブ用の電源電圧供給回路は、外部から印加される電源に異なる電源電圧を要求される回路の1つである。このような電源電圧供給回路を設計する上で設計側としては、最適に回路が動作する酸化膜厚をもつトランジスタを数種類用意し、数種類のトランジスタを基に回路の設計を行う。この時、供給される電源が仕様によって異なる場合を想定して昇圧回路を設計する場合、酸化膜耐圧問題やゲートリークによる消費電流問題を考慮しなければならない。このような問題を回避するため、仕様により設定されている電圧のうちの高い電圧に合わせて厚膜容量用のトランジスタを回路に用いると、昇圧回路の面積が大きくなってしまふ虞がある。

【0003】

そこで、動作電源電圧に応じて異なった膜厚のキャパシタを使い分けて、回路レイアウト面積を縮小し、安定した電源電圧を発生させる電源電圧発生回路が特許文献1に記載されている。この電源電圧発生回路は、装置の動作電源電圧を昇圧して出力する電源電圧発生回路であって、厚い絶縁膜で作られた第1のキャパシタと薄いゲート絶縁膜で作られた第2のキャパシタを備え、動作電源電圧に応じて第1、2のキャパシタの回路接続を変えるスイッチ回路を有するものである。

【0004】

【特許文献1】特開2005-158098号公報

【発明の開示】

【発明が解決しようとする課題】

【0005】

ところで、電源電圧発生回路の昇圧部には、トランジスタの酸化膜容量を利用した昇圧用のポンプ容量素子が備えられる。この昇圧用容量素子は、非常に大きな容量を必要とする場合が多く、多大な面積を必要とし、チップ全体の面積に対するインパクトも大きい。酸化膜容量は、酸化膜の厚さに反比例するので、通常は薄膜容量素子（薄膜トランジスタ）を用いたい。しかし、前述のように外部から供給される電源電圧が仕様により異なる場合、供給される電源電圧が薄膜トランジスタの耐圧をオーバーしないように昇圧用容量素子に厚膜トランジスタを用いるのが普通である。ワード線をドライブする電圧の値は、外部から供給される電源電圧の値が変化してもほとんど変更しないのが通常である。したがって、外部電源電圧が低い場合ほど多くのポンプ容量素子が必要であるにも関わらず、酸化膜の耐圧のために電圧が低い場合においても容量の少ない厚膜を使わざるを得ない。このように、従来の回路方式では、トランジスタの耐圧を外部電源電圧が高い側にあわせて設計せざるを得ない。このため、昇圧回路における昇圧容量の一部、例えば特許文献1では第1のキャパシタを厚膜容量素子にせざるを得ず、チップ面積をより小さくするには限度があった。

【0006】

したがって、本発明の目的は、チップ面積をより小さくする電源電圧発生回路を提供することにある。

【課題を解決するための手段】

【0007】

本発明の1つのアスペクトに係る電源電圧発生回路は、容量素子のチャージポンピング

によって昇圧電圧を発生して出力する昇圧部と、容量素子の耐圧範囲内の電圧に該外部電源の電圧を降圧して昇圧部の電源に与える電源降圧部と、昇圧部の電源に外部電源を直接与えるか電源降圧部を介して与えるかを切り替えるスイッチ回路群と、を備える。

【0008】

本発明の電源電圧発生回路において、容量素子をMOSトランジスタで構成し、該MOSトランジスタのゲート酸化膜の厚さを、昇圧部の出力を電源とする負荷回路に含まれるMOSトランジスタのゲート酸化膜の厚さより薄くなるように構成することが好ましい。

【0009】

本発明の電源電圧発生回路において、昇圧部は、多段の昇圧回路から構成され、該多段の昇圧回路のそれぞれに含まれるMOSトランジスタで構成される容量素子のゲート酸化膜の厚さが同一であることが好ましい。

【0010】

本発明の電源電圧発生回路において、昇圧部は、多段の昇圧回路における昇圧段数を、昇圧部に与えられる電源電圧に応じてスイッチ回路群によって切り替えるように構成されることが好ましい。

【0011】

本発明の電源電圧発生回路において、昇圧部は、前段および後段の昇圧回路を含み、前段の昇圧回路は、外部電源の電位の二倍の電位と接地電位との間の振幅を有する第1の昇圧信号を生成し、後段の昇圧回路は、電源降圧部の出力電位と接地電位との間の振幅を有する第2の昇圧信号、または第1の昇圧信号を入力し、スイッチ回路群は、昇圧部の電源の接続先を、外部電源または電源降圧部の出力に切り替える第1のスイッチ素子と、後段の昇圧回路の入力の接続先を、第1または第2の昇圧信号に切り替える第2のスイッチ素子と、を含み、第1のスイッチ素子が外部電源に切り替えられているときに第2のスイッチ素子が第1の昇圧信号に切り替えられ、第1のスイッチ素子が電源降圧部の出力に切り替えられているときに第2のスイッチ素子が第2の昇圧信号に切り替えられるようにしてもよい。

【0012】

本発明の電源電圧発生回路において、昇圧部に与えられる電源電圧に応じてスイッチ回路群によって切り替えられて多段の昇圧回路における昇圧動作に不要となった容量素子を、スイッチ回路群によって接続して電源降圧部の出力安定用の容量素子として機能させるように構成することが好ましい。

【0013】

本発明の電源電圧発生回路において、スイッチ回路群は、メタルオプション、ヒューズオプションおよびボンディングオプションのいずれかによって制御されるようにしてもよい。

【発明の効果】

【0014】

本発明によれば、外部電源の電圧が容量素子の耐圧を超える場合に、容量素子の耐圧範囲内の電圧に外部電源の電圧を降圧して昇圧部に供給するので、昇圧部における容量素子に全て薄膜の容量素子を用いることができる。したがって、チップ面積をより小さくすることができる。

【発明を実施するための最良の形態】

【0015】

図1は、本発明の実施形態に係る電源電圧発生回路の構成を示すブロック図である。図1において、電源電圧発生回路は、電源降圧部10と、昇圧部20と、スイッチ素子SW1と、を備える。

【0016】

昇圧部20は、容量素子のチャージポンピングによって昇圧電圧を発生して出力する。電源降圧部10は、外部電源の電圧が容量素子の耐圧を超える場合に、容量素子の耐圧範囲内の電圧に外部電源の電圧を降圧して昇圧部20の電源に与える。スイッチ素子SW1

は、昇圧部20の電源に外部電源を直接与えるか電源降圧部10を介して与えるかを切り替える。

【0017】

また、昇圧部20における容量素子がMOSトランジスタで構成され、このMOSトランジスタのゲート酸化膜の厚さは、昇圧部20の出力（図1のVPP）を電源とする負荷回路、例えばワード線ドライブ用の回路に含まれるMOSトランジスタのゲート酸化膜より薄いことが好ましい。

【0018】

さらに、昇圧部20は、多段の昇圧回路21a、21bから構成され、多段の昇圧回路21a、21bのそれぞれに含まれるMOSトランジスタで構成される容量素子のゲート酸化膜の厚さが同一であることが好ましい。

【0019】

また、昇圧部20は、多段の昇圧回路21a、21bにおける昇圧段数（例えば、一段か二段か）を、昇圧部20に与えられる電源電圧に応じてスイッチ素子SW2によって切り替えるように構成されることが好ましい。

【0020】

DRAM、特にDDR-SDARMに代表される半導体記憶装置は、以上のような構成の電源電圧発生回路と、昇圧部20の出力を電源とする図示されない負荷回路、例えばワード線ドライブ用の回路とを備えるようにしてもよい。

【0021】

以上のような構成の電源電圧発生回路によれば、外部電源電圧が仕様によって異なる条件の元で、外部電源電圧が容量素子（薄膜トランジスタ）の耐圧を超えるような高い場合に外部電源の電圧を電源降圧部10で降圧する。そして、容量の大きい薄膜の容量素子を、電源電圧が低い場合と共有して昇圧部20に用いることが可能となる。したがって、チップにおけるレイアウト面積を大幅に削減することが出来る。以下、実施例に即し、詳細に説明する。

【実施例1】

【0022】

図1は、本発明の実施例に係る電源電圧発生回路の回路図である。図1において、電源電圧発生回路は、電源降圧部10と、昇圧部20と、単極双投型のスイッチ素子SW1と、を備える。スイッチ素子SW1は、昇圧部20の電源Vddに対し、外部電源VDDP1を直接与えるか、外部電源VDDP2の電圧を電源降圧部10によって降圧して電源VDLPとして与えるかを切り替える。

【0023】

昇圧部20は、前段の昇圧回路21a、後段の昇圧回路21b、昇圧回路21a、21bを切り替える単極双投型のスイッチ素子SW2を備える。昇圧部20は、駆動信号S0を用いて容量素子のチャージポンピングによって電源Vddから昇圧電圧を発生し、電源VPPとして図示されない負荷回路、例えばワード線ドライブ用の回路に供給する。この時、スイッチ素子SW2は、昇圧部20における昇圧段数を、昇圧回路21bの1段とするか、昇圧回路21a、21bの2段とするかを切り替える。

【0024】

昇圧回路21aは、駆動信号S0を入力し、外部電源VDDP1の電位の二倍の電位と接地電位との間の振幅を有する信号（第1の昇圧信号）を出力する。また、昇圧回路21bは、駆動信号S0として電源VDLPの電位と接地電位との間の振幅を有する信号（第2の昇圧信号）、または昇圧回路21aの出力信号（第1の昇圧信号）を入力し、昇圧して電源VPPとして出力する。この時、スイッチ素子SW1が外部電源VDDP1に切り替えられているときにスイッチ素子SW2が第1の昇圧信号に切り替えられ、スイッチ素子SW1が電源降圧部10の出力（VDLP）に切り替えられているときにスイッチ素子SW2が第2の昇圧信号に切り替えられる。

【0025】

次に、昇圧部20の詳細について説明する。図2は、本発明の実施例に係る昇圧部の回路図である。図2において、昇圧部20は、昇圧回路21a、21bと、信号S0を入力して信号S1～S5を出力する信号供給回路22とを含む。昇圧回路21aは、NchトランジスタN1、N2、PchトランジスタP1、MOSトランジスタで構成される容量素子C1、単極双投型のスイッチ素子SW3～SW7を備える。また、昇圧回路21bは、NchトランジスタN3、N4、MOSトランジスタで構成される容量素子C2、スイッチ素子SW2を備える。ここでNchトランジスタN1および容量素子C1、C2は、ゲート絶縁膜の薄いトランジスタ（薄膜トランジスタ）である。また、NchトランジスタN2～N4、PchトランジスタP1は、ゲート絶縁膜の厚いトランジスタ（厚膜トランジスタ）である。さらに、スイッチ素子SW1～SW7は、メタルオプション、ヒューズオプション、ボンディングオプションのいずれかによる切り替えスイッチオプション信号によって制御される。

【0026】

NchトランジスタN1は、ドレインを電源Vddに接続し、他端が電源Vddに接続されるスイッチ素子SW4の一端およびPchトランジスタP1のソースにソースを接続し、ゲートをスイッチ素子SW5の単極側接点に接続する。PchトランジスタP1は、ドレインをNchトランジスタN2のドレインおよびスイッチ素子SW2の一端に接続し、ゲートをスイッチ素子SW3の単極側接点に接続する。NchトランジスタN2は、ソースを電源Vss（接地）に接続し、ゲートをスイッチ素子SW6の単極側接点に接続する。容量素子C1は、一端をスイッチ素子SW4の単極側接点に接続し、他端をスイッチ素子SW7の単極側接点に接続する。スイッチ素子SW3は、一端に信号S3を与え、他端を電源Vssに接続する。スイッチ素子SW5は、一端に信号S1を与え、他端を電源Vssに接続する。スイッチ素子SW7は、一端に信号S2を与え、他端を電源Vssに接続する。スイッチ素子SW6は、一端に信号S3を与え、他端を電源Vddに接続する。

【0027】

NchトランジスタN3は、ドレインを電源Vddに接続し、容量素子C2の一端およびNchトランジスタN4のドレインにソースを接続し、ゲートに信号S1を与える。NchトランジスタN4は、ソースを電源VPPとして接続し、ゲートに信号S5を与える。容量素子C2は、他端をスイッチ素子SW2の単極側接点に接続し、スイッチ素子SW2の他端には信号S4を与える。

【0028】

次に、図2におけるスイッチ素子SW2～SW7が図1のスイッチ素子SW1と連動して切り替わる際の昇圧回路の動作について説明する。図3は、外部電源VDDP1の電圧が薄膜トランジスタ耐圧より低い場合の接続、図4は、外部電源VDDP2の電圧が薄膜トランジスタ耐圧より高い場合の接続を示す。なお、以下において、電源の符号と、この電源の電圧値とを同じ符号で表すものとする。VDDP1が薄膜トランジスタ耐圧より低い外部電源電圧、VDDP2が薄膜トランジスタ耐圧より高い電源電圧、VPPはワード線ドライブ用などの電源電圧、VDLPはVDDP2を電源降圧部10によって薄膜トランジスタ耐圧許容範囲内までに降圧した電源電圧を示している。すなわち、薄膜トランジスタの耐圧許容範囲をVDLP以下、厚膜トランジスタの耐圧許容範囲をVPP程度以下とする。また、各電源電圧の関係は、簡単のため、 $VPP > VDDP2 > VDLP > VDDP1$ 、 $2 \cdot VDLP > VPP$ 、 $3 \cdot VDDP1 > VPP$ 、 $VPP > 2 \cdot VDDP1$ とする。

【0029】

図3は、昇圧部が二段動作を行う場合の等価回路および各部信号の波形を示す図である。図3(A)は、外部電源VDDP1の電圧が薄膜トランジスタ耐圧より低い場合における昇圧部20の接続に係る等価回路を示す。図3(B)は、各部の信号のタイミングチャートである。

【0030】

(1) 信号S1の電圧レベルが $2 \cdot VDDP1$ の時、ゲートに信号S1が与えられるN

c hトランジスタN 1は、オンとなり、N c hトランジスタN 1のソース、すなわち、容量素子C 1の一端は、VDDP 1に向けて充電される。この時、信号S 3の電圧レベルがVDDP 1であるので、P c hトランジスタP 1は、オフであり、容量素子C 1の充電動作に影響を与えない。なお、信号S 2の電圧レベルは、V s sである。したがって、容量素子C 1は、VDDP 1－V s sの電位で充電される。

【0031】

一方、信号S 1の電圧レベルが、 $2 \cdot VDDP 1$ であるので、N c hトランジスタN 3は、オンとなり、N c hトランジスタN 3のソースである接点A 2、すなわち容量素子C 2の一端の電位は、VDDP 1に向けて充電される。この時、信号S 3の電圧レベルがVDDP 1であるので、N c hトランジスタN 2は、オンであり、容量素子C 2の他端の電位はV s sである。

【0032】

(2) 信号S 1の電圧レベルがVDDP 1となると、信号S 2の電圧レベルがV s sからVDDP 1に上昇し、これに伴ってN c hトランジスタN 1のソース、すなわち容量素子C 1の一端の電位は、VDDP 1から $2 \cdot VDDP 1$ に上昇する。N c hトランジスタN 1は、オフとなり、この上昇の動作に影響を与えない。この時、信号S 3の電圧レベルがV s sであるので、P c hトランジスタP 1は、オンであり、N c hトランジスタN 2は、オフである。したがって、容量素子C 1の一端の電位は、接点A 1の電位として容量素子C 2の他端に伝達される。

【0033】

これによって、容量素子C 2の一端の電位は、VDDP 1から $3 \cdot VDDP 1$ に上昇する。この時、信号S 1の電圧レベルがVDDP 1であるので、N c hトランジスタN 3は、オフであって、この上昇の動作に影響を与えない。また、信号S 5の電圧レベルがVDDP 1+VPPであるので、N c hトランジスタN 4は、オンとなって、容量素子C 2の一端、すなわち接点A 2の電位がVPPに伝達される。外部に容量素子C 2の充電電荷が供給されることで、接点A 2の電位は、徐々に低下する。

【0034】

昇圧部20は、以上のように動作することでVPPに $2 \cdot VDDP 1$ に近い電圧を供給する。この際、昇圧部20において、容量素子C 1、C 2等の薄膜トランジスタで構成された箇所は、必ずゲート・ソース間もしくはゲート・ドレイン間にVDDP 1以下の差電位しかかかっていない。

【0035】

図4は、昇圧部が一段動作を行う場合の等価回路および各部信号の波形を示す図である。図4 (A)は、外部電源VDDP 2の電圧が薄膜トランジスタ耐圧より高い場合における昇圧部10の接続に係る等価回路を示す。この場合、VDDP 2は、電源降圧部10によってVDLPに降圧され、VDLPが昇圧部20の電源Vddとして与えられる。

【0036】

図2において、N c hトランジスタN 1は、ゲートがV s sに接続され、オフとなる。また、N c hトランジスタN 2は、ゲートがVddに接続され、オンとなり、P c hトランジスタP 1は、ゲートがV s sに接続され、オンとなる。したがって、昇圧動作から切り離されたN c hトランジスタN 1、N 2、P 1は、他の回路に影響を与えない。

【0037】

一方、図4 (A)に示すように容量素子C 1の一端は、電源Vdd、すなわち、電源降圧部10で降圧された電源VDLPに接続され、他端は、V s sに接続される。したがって、容量素子C 1は、昇圧部20におけるVdd/V s s間の安定化容量として機能する。

【0038】

図4 (B)は、図4 (A)の各部の信号のタイミングチャートである。

【0039】

(1) 信号S 1の電圧レベルが $2 \cdot VDLP$ の時、ゲートに信号S 1が与えられるN c

hトランジスタN3は、オンとなり、NchトランジスタN3のソース、すなわち、接点A2である容量素子C2の一端は、VDLPに向けて充電される。容量素子C2の他端は、信号S4によってVssとされる。

【0040】

(2) 信号S1の電圧レベルがVDLPとなると、信号S4の電圧レベルがVssからVDLPに上昇し、接点A2、すなわち容量素子C2の一端の電位は、VDLPから $2 \cdot \text{VDLP}$ に上昇する。この時、信号S1の電圧レベルがVDLPであるので、NchトランジスタN3は、オフであって、この上昇の動作に影響を与えない。また、信号S5の電圧レベルがVDLP+VPPであるので、NchトランジスタN4は、オンとなって、容量素子C2の一端、すなわち接点A2の電位がVPPに伝達される。容量素子C2の充電電荷が外部に供給されることで、接点A2の電位は、徐々に低下する。

【0041】

以上のように動作する昇圧部20において、容量素子C1、C2等の薄膜トランジスタで構成された箇所は、必ずゲート・ソース間もしくはゲート・ドレイン間にVDDP1以下の差電位しかかかっていない。

【0042】

以上のように構成される昇圧部20において、外部電源電圧がVDDP2である場合、昇圧段数を一段構成にしている。これは $2 \cdot \text{VDLP}$ がVPPに対してある程度大きく、二段構成よりも一段構成の方が消費電流が少なく、VPPレベルの電源が供給できるからである。この理由は、理想的には図3(A)における接点A1、A2は、それぞれ $2 \cdot \text{VDDP1}$ 、 $3 \cdot \text{VDDP1}$ になるが、実際には寄生容量の影響を受けて理想どおりの電位にはならない。したがって、寄生容量の影響を受けないようにできるだけ段数は少ない方が電圧変換効率が良く好ましい。また、一段構成よりも二段構成の方が動作する接点が多い分消費電流が多くなり好ましくない。

【0043】

図5は、電源降圧部10の回路図である。電源降圧部10は、VDDP2を降圧し、DRAM等内部で発生させたVDLP/2の電源電圧をVDLPレベルにしてドライブする回路である。電源降圧部10は、NchトランジスタN11~N16、PchトランジスタP11~P14、スイッチ素子SW8~SW10を備える。差動対であるNchトランジスタN12、N13は、ソースを共通に電流源となるNchトランジスタN11に接続し、ドレインをカレントミラーを構成するPchトランジスタP11、P12に接続する。NchトランジスタN12のゲートには、VDLP/2が与えられ、NchトランジスタN13のゲートには、それぞれがダイオード接続されたNchトランジスタN14、N15の直列回路の midpoint に接続される。NchトランジスタN12のドレインは、ソースがVDDP2に接続されるPchトランジスタP14のゲートに接続される。さらに、PchトランジスタP14のドレインは、電源降圧部10の出力としてVDLPを昇圧部20に供給すると共に、NchトランジスタN14のアノード（ドレインおよびゲート）に接続される。NchトランジスタN15は、ソースがVssに接続される。

【0044】

なお、電源降圧部10が降圧機能として用いられない場合、図5に示すSW8~SW10を切り替えて電源降圧部10を動作させないようにする。すなわち、PchトランジスタP13のゲートがVssとなって、PchトランジスタP13がオンとなって、PchトランジスタP11、P12、P14をオフとする。また、NchトランジスタN11のゲートがVssとなって、NchトランジスタN11がオフとなって、NchトランジスタN12、N13への電流供給を停止する。さらに、NchトランジスタN16のゲートがVDDP1となって、NchトランジスタN16がオンとなって、VDLPをVssのレベルに保つ。

【0045】

このような電源降圧部10の回路は、薄膜トランジスタ耐圧を超えるVDDP2が入力されるため、全て厚膜トランジスタで構成される。VDDP1が外部電源電圧として入力

される場合は、SW8～SW10を切り替えて降圧機能が無効にされる。尚、図5に示す電源降圧部10は、一例を示すものであり、必ずしもこの回路と同じ構成をとる必要はなく、VDDP2からVDLPレベルの電源電圧を出力する回路であれば他の回路構成であっても良い。

【0046】

以上のような構成の電源電圧発生回路によれば、外部電源電圧が薄膜トランジスタの耐圧を超える場合に、電源降圧部10によって薄膜トランジスタの耐圧範囲内の電圧に降圧し、薄膜トランジスタから構成された昇圧部20によってワード線ドライブ用の電源電圧を昇圧する。したがって、外部電源電圧が薄膜トランジスタの耐圧を超えるような高い場合であっても、電源電圧が低い場合と共有してワード線ドライブ用の昇圧部20に容量の大きい薄膜容量素子（薄膜容量トランジスタ）を用いることが可能となる。昇圧部20に全て薄膜の容量素子を用いることで、チップ面積をより減らすことができる。

【0047】

次に、具体的な数字例を用いて説明する。仮に $V_{PP} = 2.5\text{ V}$ 、 $V_{DDP2} = 1.8\text{ V}$ 、 $V_{DLP} = 1.5\text{ V}$ 、 $V_{DDP1} = 1.2\text{ V}$ 、薄膜トランジスタの耐圧 $= 1.5\text{ V}$ 、厚膜トランジスタの耐圧 $= 3.0\text{ V}$ とする。厚膜トランジスタの耐圧が薄膜トランジスタの耐圧の二倍であることから、酸化膜の厚さに関し、通常、厚膜は薄膜の二倍あるので、厚膜の容量は薄膜の容量の半分である。トランジスタの面積は、 V_{PP} の供給能力において最悪条件である $V_{DDP1} = 1.2\text{ V}$ の場合を想定して決められるが、厚膜容量素子を使用すると単純に薄膜の倍の面積が必要となってしまう。DRAMにおけるポンプ容量素子の面積は、数ミリ平方メートル程度になることが多いので、この面積が半分になると、チップ面積の削減においてかなり有利である。なお、電源電圧発生回路に電源降圧部が加わることで電源降圧部に対応するチップ面積が増えてしまう。しかしながら、電源降圧部の面積は、ポンプ容量素子の面積に比べると十分に小さく無視することができる（VDLP安定化容量を増やさなくても良い）。

【0048】

また、本実施例の電源電圧発生回路によれば、ワード線ドライブ用の電源昇圧回路の昇圧段数を、メタルオプション、ヒューズオプション、ボンディングオプションのいずれかによって切り替えて、外部電圧のレベルによって最も効率の良い昇圧段数に切り替えるように構成することが可能である。

【0049】

先に説明した条件と同じ条件で具体的に説明する。単純に $V_{PP} = 2.5\text{ V}$ を得るためには、外部電源電圧が $V_{DDP1} = 1.2\text{ V}$ の場合、 $3 \cdot V_{DDP1} = 3.6\text{ V}$ まで昇圧しなくてはならず二段昇圧にする。これに対し、 $V_{DDP2} = 1.8\text{ V}$ の場合は、 $V_{DLP} = 1.5\text{ V}$ で、 $2 \cdot V_{DLP} = 3.0\text{ V}$ であり、 V_{PP} に対して供給能力があるので、一段昇圧でよい。先に説明したように、段数が少ないほど V_{PP} に対する電源供給の効率は良い。

【0050】

以上の説明では、外部電源電圧によって昇圧回路を一段および二段に切り替える方式を説明した。しかし、これに限定されることなく、外部電源電圧に対する V_{PP} の値によって他の段数との切り替えが有効となる場合にも適用することができる。例えば、二段と三段、もしくは三段と四段等の切り替えに適用してもよい。また、極端な場合では、一段と三段の切り替えなどにも適用可能である。さらに、外部電源電圧が薄膜トランジスタの耐圧を超えることなく、かつ、一段の昇圧で V_{PP} への供給が間に合う場合も想定される。しかし、このような場合であっても本実施例の電源電圧発生回路を適用することができる。

【0051】

以上本発明を上記実施例に即して説明したが、本発明は、上記実施例にのみ限定されるものではなく、本願特許請求の範囲の各請求項の発明の範囲内で当業者であればなし得るであろう各種変形、修正を含むことは勿論である。

【図面の簡単な説明】

【0052】

【図1】 本発明の実施形態に係る電源電圧発生回路の構成を示すブロック図である。

【図2】 本発明の実施例に係る昇圧部の回路図である。

【図3】 昇圧部が二段動作を行う場合の等価回路および各部信号の波形を示す図である。

【図4】 昇圧部が一段動作を行う場合の等価回路および各部信号の波形を示す図である。

【図5】 電源降圧部の回路図である。

【符号の説明】

【0053】

10 電源降圧部

20 昇圧部

21 a、21 b 昇圧回路

22 信号供給回路

C1、C2 薄膜容量素子

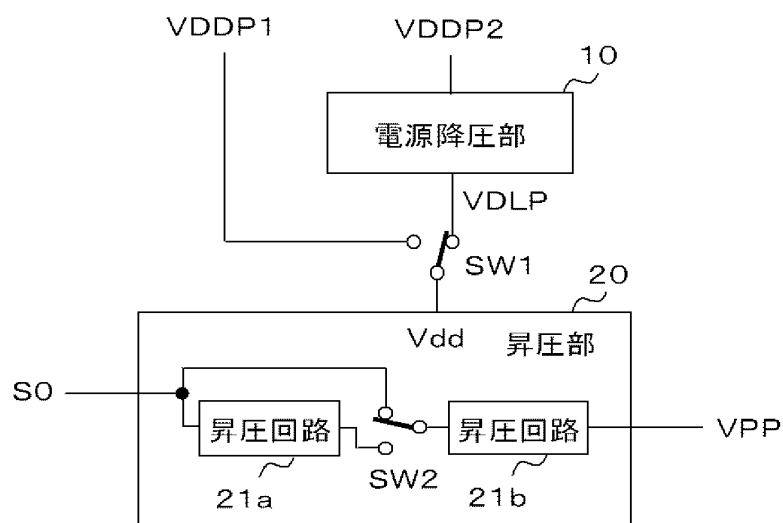
N1～N4、N11～N16 Nchトランジスタ

P1、P11～P14 Pchトランジスタ

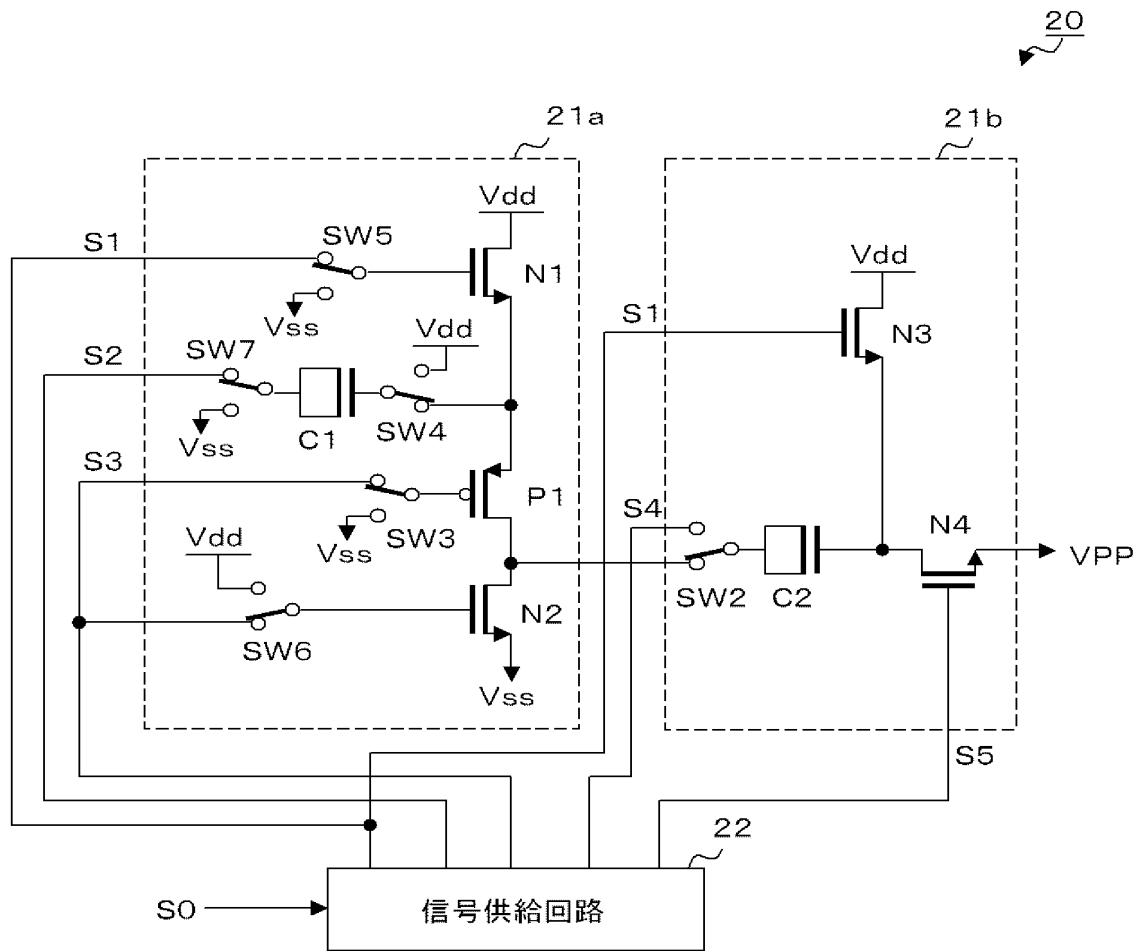
S0～S5 信号

SW1～SW10 スイッチ素子

【書類名】 図面
【図 1】

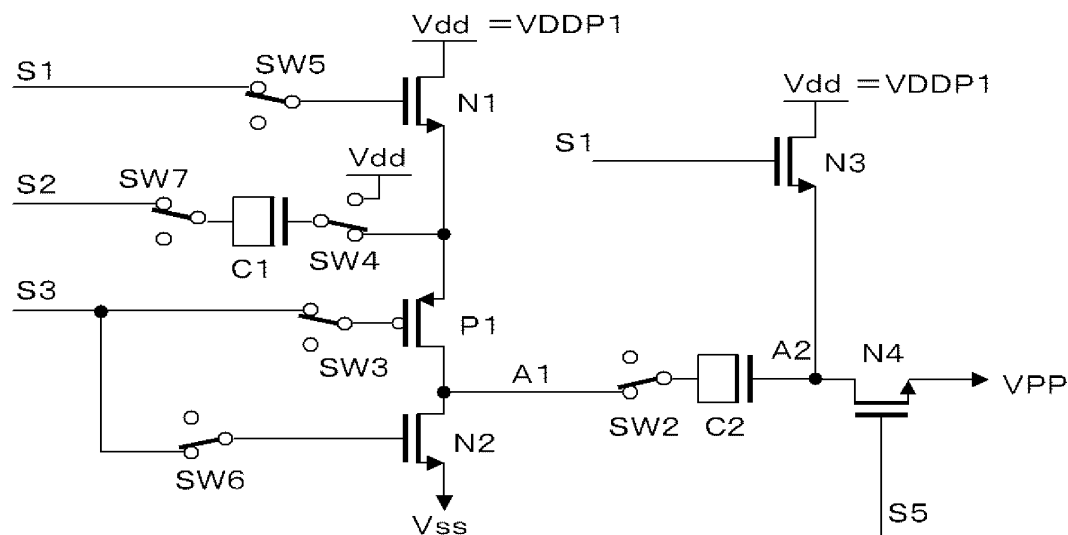


【図2】

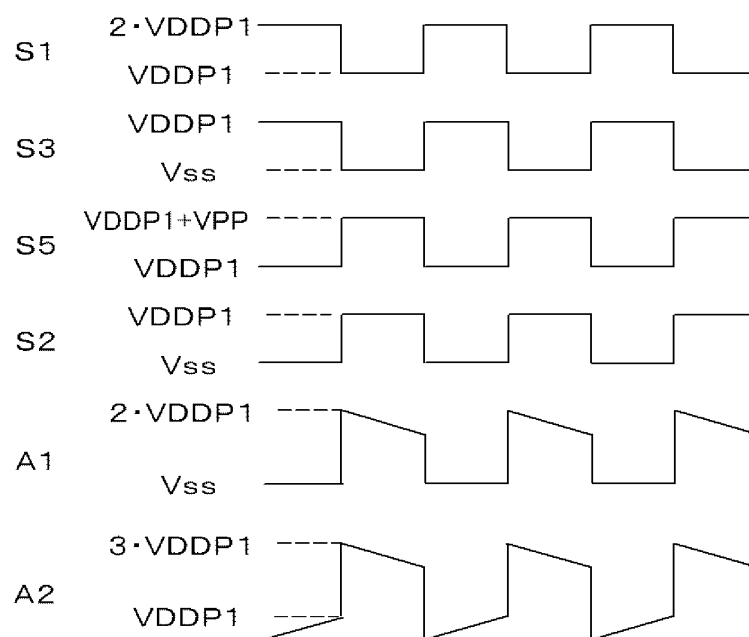


【图 3】

(A)

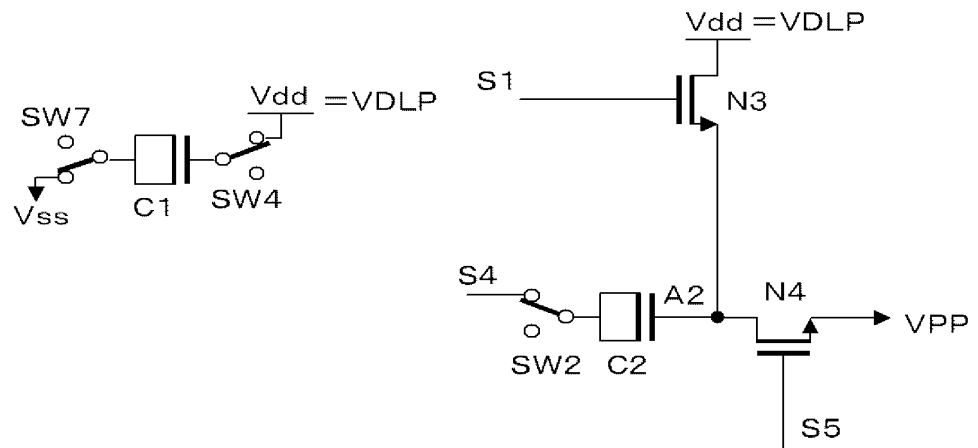


(B)

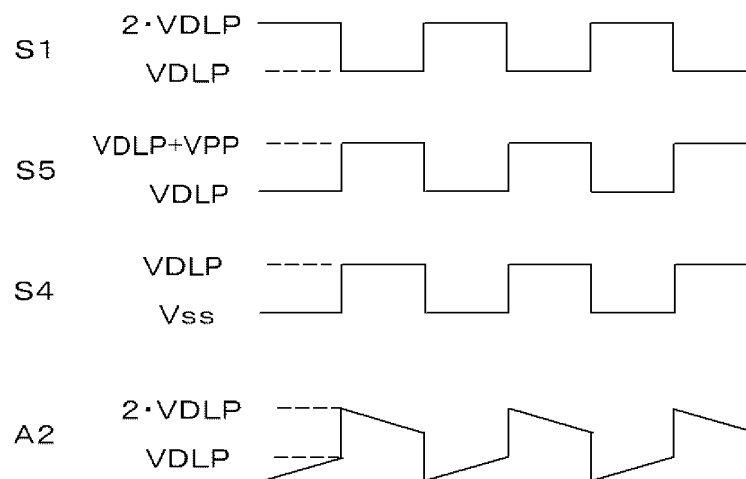


【図4】

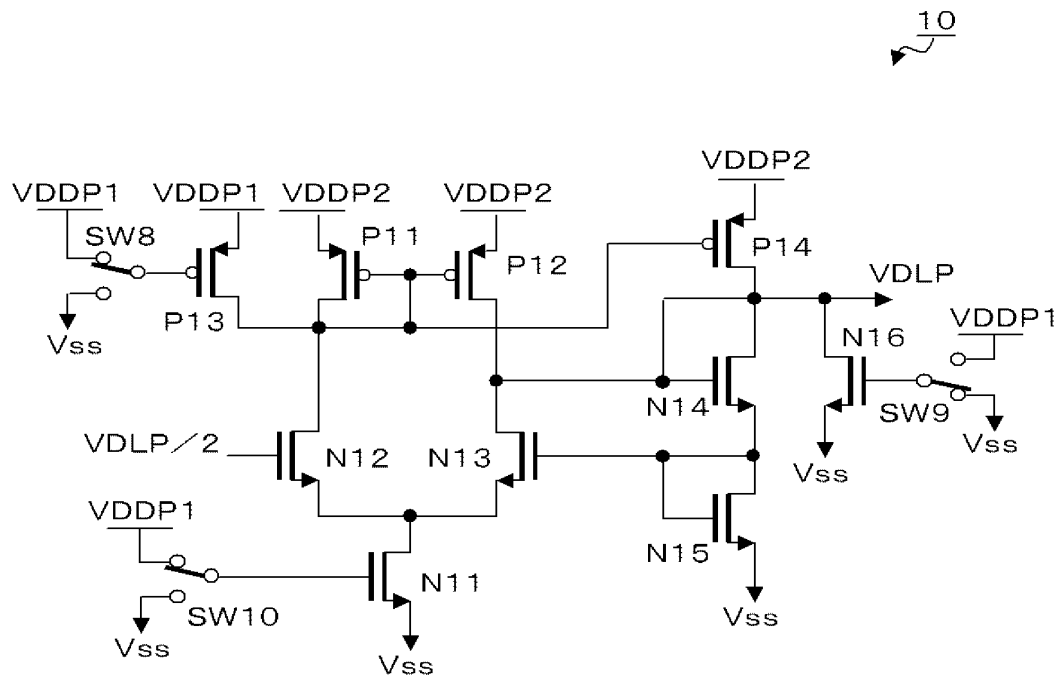
(A)



(B)



【図 5】



【書類名】 要約書

【要約】

【課題】 チップ面積をより小さくする。

【解決手段】 容量素子のチャージポンピングによって昇圧電圧を発生して出力する昇圧部20と、外部電源の電圧が容量素子の耐圧を超える場合に、容量素子の耐圧範囲内の電圧に外部電源の電圧を降圧して昇圧部20の電源に与える電源降圧部10と、昇圧部20の電源に外部電源を直接与えるか電源降圧部10を介して与えるかを切り替えるスイッチ素子SW1と、を備える。昇圧部20は、多段の昇圧回路から構成され、多段の昇圧回路のそれぞれに含まれるMOSトランジスタで構成される容量素子のゲート酸化膜の厚さが同一であり、昇圧部20の出力を電源とする回路に含まれるMOSトランジスタのゲート酸化膜より薄い。

【選択図】 図1

【書類名】 手続補正書
【整理番号】 22311733
【提出日】 平成19年 6月 7日
【あて先】 特許庁長官殿
【事件の表示】
 【出願番号】 特願2007- 81754
【補正をする者】
 【識別番号】 000233169
 【氏名又は名称】 株式会社日立超エル・エス・アイ・システムズ
【代理人】
 【識別番号】 100080816
 【弁理士】
 【氏名又は名称】 加藤 朝道
 【電話番号】 045-476-1131
【手続補正1】
 【補正対象書類名】 特許願
 【補正対象項目名】 提出物件の目録
 【補正方法】 追加
 【補正の内容】
 【提出物件の目録】
 【物件名】 委任状 1

【物件名】

委任状

【添付書類】



072

委 任 状

平成19年 5月21日

私儀弁理士 加 藤 朝 道 氏を以て代理人として下記事項
を委任します。

1. (特願 2007 - 81754 についての)

特許出願

に関する一切の件並びに本件に関する放棄若しくは取下げ、出願変更、拒絶査定
不服及び補正却下の決定に対する審判の請求並びに取下げ。

2. 上記出願又は平成 年 願第 号

に基づく「特許法第41条第1項及び実用新案法第8条第1項」の優先権主
張並びにその取下げ。

3. 上記出願の分割出願及び補正却下の決定に対する新たな出願に関する一切の
件並びに本件に関する上記事項一切。

4. 上記出願に関する審査請求、優先審査に関する事情説明書の提出、刊行物の
提出、証明の請求及び上記出願又は審判請求に関する物件の下附を受けること。

5. 第1項に関する通常実施権許諾の裁定請求、裁定取消請求並びにそれ等に対
する答弁、取下其他本件に関する提出書類及び物件の下附を受けること。

6. 上記出願に由来する全ての特許権又は登録及びこれらの権利に関する手続並
びにこれらの権利の放棄並びにこれらの手続に関する請求の取下げ、申請の取下
げ及び申立ての取下げ。

7. 上記出願に由来する全ての特許又は登録に対する異議申立てに関する一切の
手続。

8. 上記出願に由来する全ての特許又は登録に対する無効審判に関する一切の手
続。

9. 上記出願に由来する全ての特許又は登録に関する訂正審判の請求及びその取
下げ。

10. 上記各項に関し行政不服審査法に基づく諸手続を為すこと。

11. 上記事項を処理する為、復代理人を選任及び解任すること。

住 所 東京都小平市上水本町五丁目2番1号

名 称 株式会社 日立超エル・エス・アイ・システムズ
取締役社長 木 原 利 昌



【書類名】 手続補正書
【整理番号】 07P00014
【提出日】 平成24年 3月27日
【あて先】 特許庁長官殿
【事件の表示】
【出願番号】 特願2007- 81754
【補正をする者】
【識別番号】 500174247
【氏名又は名称】 エルピーダメモリ株式会社
【補正をする者】
【識別番号】 000233169
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【代理人】
【識別番号】 100080816
【弁理士】
【氏名又は名称】 加藤 朝道
【電話番号】 045-476-1131
【発送番号】 051592
【手続補正1】
【補正対象書類名】 特許請求の範囲
【補正対象項目名】 全文
【補正方法】 変更
【補正の内容】

【書類名】 特許請求の範囲
【請求項 1】

第1の厚さであるゲート酸化膜を備えたMOSトランジスタで構成される容量素子を其々含む多段の昇圧回路から構成され、前記複数の容量素子のチャージポンピングによって昇圧電圧を発生して出力する昇圧部と、

前記MOSトランジスタで構成される容量素子の前記ゲート酸化膜の前記第1の厚さに対応する耐圧範囲内の電圧に外部電源の電圧を降圧して前記昇圧部の電源に与える電源降圧部と、

前記昇圧部の電源に前記外部電源を直接与えるか前記電源降圧部を介して与えるかを切り替えるスイッチ回路群と、

を備え、

前記昇圧部は、前記多段の昇圧回路における昇圧段数を、前記昇圧部に与えられる電源電圧に応じて前記スイッチ回路群によって切り替えるように構成されることを特徴とする電源電圧発生回路。

【請求項 2】

前記MOSトランジスタのゲート酸化膜の厚さを、前記昇圧部の出力を電源とする負荷回路に含まれるMOSトランジスタのゲート酸化膜の厚さより薄くなるように構成することを特徴とする請求項1記載の電源電圧発生回路。

【請求項 3】

前記昇圧部は、前段および後段の昇圧回路を含み、

前記前段の昇圧回路は、前記外部電源の電位の二倍の電位と接地電位との間の振幅を有する第1の昇圧信号を生成し、

前記後段の昇圧回路は、前記電源降圧部の出力電位と接地電位との間の振幅を有する第2の昇圧信号、または前記第1の昇圧信号を入力し、

前記スイッチ回路群は、前記昇圧部の電源の接続先を、前記外部電源または前記電源降圧部の出力に切り替える第1のスイッチ素子と、前記後段の昇圧回路の入力の接続先を、前記第1または第2の昇圧信号に切り替える第2のスイッチ素子と、を含み、

前記第1のスイッチ素子が前記外部電源に切り替えられているときに前記第2のスイッチ素子が前記第1の昇圧信号に切り替えられ、前記第1のスイッチ素子が前記電源降圧部の出力に切り替えられているときに前記第2のスイッチ素子が前記第2の昇圧信号に切り替えられることを特徴とする請求項2記載の電源電圧発生回路。

【請求項4】

前記昇圧部に与えられる電源電圧に応じて前記スイッチ回路群によって切り替えられて前記多段の昇圧回路における昇圧動作に不要となった容量素子を、前記スイッチ回路群によって接続して前記電源降圧部の出力安定用の容量素子として機能させるように構成することを特徴とする請求項2記載の電源電圧発生回路。

【請求項5】

前記スイッチ回路群は、メタルオプション、ヒューズオプションおよびボンディングオプションのいずれかによって制御されることを特徴とする請求項1、3、4のいずれかに記載の電源電圧発生回路。

【請求項6】

請求項1乃至5のいずれかーに記載の電源電圧発生回路と、前記昇圧部の出力を電源とする負荷回路とを備える半導体記憶装置。

【手続補正2】

【補正対象書類名】 明細書

【補正対象項目名】 0007

【補正方法】 変更

【補正の内容】

【0007】

本発明の1つのアスペクトに係る電源電圧発生回路は、第1の厚さであるゲート酸化膜を備えたMOSトランジスタで構成される容量素子を其々含む多段の昇圧回路から構成され、複数の容量素子のチャージポンピングによって昇圧電圧を発生して出力する昇圧部と、MOSトランジスタで構成される容量素子のゲート酸化膜の第1の厚さに対応する耐圧範囲内の電圧に外部電源の電圧を降圧して昇圧部の電源に与える電源降圧部と、昇圧部の電源に外部電源を直接与えるか電源降圧部を介して与えるかを切り替えるスイッチ回路群と、を備える。ここで昇圧部は、多段の昇圧回路における昇圧段数を、昇圧部に与えられる電源電圧に応じてスイッチ回路群によって切り替えるように構成される。

出願人履歴

5 0 0 1 7 4 2 4 7

20000712

名称変更

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株式会社日立超エル・エス・アイ・システムズ

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/912,845				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	600			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720			
TOTAL CLAIMS (37 CFR 1.16(j))	9	minus 20 = *			OR	x 80 =	0.00			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1	minus 3 = *			OR	x 420 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
			TOTAL			TOTAL	1600			
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/912,845	06/07/2013	Koichiro HAYASHI	Q204830

CONFIRMATION NO. 5774

23373
SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

NOTICE



Date Mailed: 07/05/2013

INFORMATIONAL NOTICE TO APPLICANT

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
Koichiro HAYASHI
Hitoshi TANAKA

Applicant may submit the inventor's oath or declaration at any time before the Notice of Allowance and Fee(s) Due, PTOL-85, is mailed.



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
13/912,845	06/07/2013	2827	1740	Q204830	9	1

CONFIRMATION NO. 5774

23373
SUGHRUE MION, PLLC
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WASHINGTON, DC 20037

FILING RECEIPT



OC000000062256116

Date Mailed: 07/05/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Koichiro HAYASHI, Tokyo, JAPAN;
Hitoshi TANAKA, Ome, JAPAN;

Applicant(s)

ELPIDA MEMORY, INC., Tokyo, JAPAN

Power of Attorney: The patent practitioners associated with Customer Number 23373

Domestic Priority data as claimed by applicant

This application is a CON of 12/052,422 03/20/2008 PAT 8493132

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)
JAPAN 2007-081754 03/27/2007

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If Required, Foreign Filing License Granted: 06/27/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/912,845**

Projected Publication Date: 10/10/2013

Non-Publication Request: No

Early Publication Request: No
Title

SUPPLY VOLTAGE GENERATING CIRCUIT

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/912,845	06/07/2013	Koichiro HAYASHI	Q204830

CONFIRMATION NO. 5774

POA ACCEPTANCE LETTER

23373
SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037



Date Mailed: 07/05/2013

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 06/07/2013.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/Inguyen/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UTILITY PATENT APPLICATION TRANSMITTAL <i>(Only for new nonprovisional applications under 37 CFR 1.53(b))</i>		Attorney Docket No. Q204830	
		First Named Inventor Koichiro HAYASHI	
		Title	SUPPLY VOLTAGE GENERATING CIRCUIT
		Express Mail Label No.	
APPLICATION ELEMENTS <i>See MPEP chapter 600 concerning utility patent application contents.</i>		Commissioner for Patents P.O. Box 1450 Alexandria VA 22313-1450	
1. ☐ Fee Transmittal Form (PTO/SB/17 or equivalent) 2. ☐ Applicant asserts small entity status. See 37 CFR 1.27. 3. ☐ Applicant certifies micro entity status. See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent. 4. ☒ Specification [Total Pages <u>29</u>] Both the claims and abstract must start on a new page. (See MPEP § 608.01(a) for information on the preferred arrangement) 5. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets <u>5</u>] 6. Inventor's Oath or Declaration [Total Sheets <u> </u>] <i>(including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))</i> a. ☐ Newly executed (original or copy) b. ☐ A copy from a prior application (37 CFR 1.63(d)) 7. ☒ Application Data Sheet. *See note below. See 37 CFR 1.76 (PTO/AIA/14 or equivalent) 8. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (<i>Appendix</i>) ☐ Landscape Table on CD 9. ☐ Nucleotide and/or Amino Acid Sequence Submission <i>(if applications, items a. – c. are required)</i> a. ☐ Computer Readable Form (CRF) b. ☐ Specification Sequence Listing on: i. ☐ CD-ROM or CD-R (2 copies); or ii. ☐ Paper c. ☐ Statements verifying identity of above copies		ACCOMPANYING APPLICATION PAPERS 10. ☐ Assignment Papers (cover sheet & document(s)) Name of Assignee <u>ELPIDA MEMORY, INC.</u> 11. ☐ 37 CFR 3.73(c) Statement ☒ Power of Attorney <i>(when there is an assignee)</i> 12. ☐ English Translation Document <i>(if applicable)</i> 13. ☒ Information Disclosure Statement <i>(PTO/SB/08 or PTO-1449)</i> ☐ Copies of citations attached 14. ☐ Preliminary Amendment 15. ☐ Return Receipt PostCard <i>(MPEP § 503)(Should be specifically itemized)</i> 16. ☐ Certified Copy of Priority Document(s) <i>(if foreign priority is claimed)</i> 17. ☐ Nonpublication Request Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent. 18. ☒ Priority is claimed from: US 12/052,422 2008-03-20 JP 2007-081754 2007-03-27 The priority document(s) were filed in parent Application No. 12/052,422 19. ☐ Other:	
Note: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 must be included in an Application Data Sheet (ADS). (2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).			
☒ The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.			
20. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76: ☒ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: 12/052,422 Prior application information: Examiner: ALMO, KHAREEM Art Unit: 2816 E			
21. CORRESPONDENCE ADDRESS			
☒ The address associated with Customer Number: WASHINGTON OFFICE 23373 CUSTOMER NUMBER OR ☐ Correspondence address below			
Signature <u>/ Carl J. Pellegrini /</u>		Date June 7, 2013	
Name Carl J. Pellegrini		Registration No. 40,766	

FEE TRANSMITTAL		Complete if Known	
☐ Applicant asserts small entity status. See 37 CFR 1.27.		Application Number	Not Yet Assigned
☐ Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.		Filing Date	June 7, 2013
TOTAL AMOUNT OF PAYMENT (\$1,740		First Named Inventor	Koichiro HAYASHI
		Examiner Name	ALMO, Khareem E. (parent)
		Art Unit	Not Yet Assigned
		Docket No.	Q204830

METHOD OF PAYMENT (check all that apply)	
☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____	
☐ Deposit Account Deposit Account Number: <u>19-4880</u> Deposit Account Name: <u>Sughrue Mion, PLLC</u>	
For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)	
☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, except for the Issue Fee and the Publication Fee	
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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES (U = undiscounted fee; S = small entity fee; M = micro entity fee)										
	FILING FEES			SEARCH FEES			EXAMINATION FEES			
<u>Application Type</u>	<u>U(\$)</u>	<u>S(\$)</u>	<u>M(\$)</u>	<u>U(\$)</u>	<u>S(\$)</u>	<u>M(\$)</u>	<u>U(\$)</u>	<u>S(\$)</u>	<u>M(\$)</u>	<u>Fees Paid (\$)</u>
Utility	280	140*	70	600	300	150	720	360	180	1,600
Design	180	90	45	120	60	30	460	230	115	
Plant	180	90	45	380	190	95	580	290	145	
Reissue	280	140	70	600	300	150	2160	1080	540	
Provisional	260	130	65	0	0		0	0	0	

* The \$140 small entity status filing fee for a utility application is further reduced to \$70 for a small entity status applicant who filed the application via EFS-Web.

2. EXCESS CLAIM FEES			
<u>Fee Description</u>	<u>Undiscounted Fee (\$)</u>	<u>Small Entity Fee (\$)</u>	<u>Micro Entity Fee (\$)</u>
Each claim over 20 (including Reissues)	80	40	20
Each independent claim over 3 (including Reissues)	420	210	105
Multiple dependent claims	780	390	195
<u>Total Claims</u>	<u>Extra Claims</u>	<u>Fee (\$)</u>	<u>Fee Paid (\$)</u>
9 - 20 or HP =	0	X 80	= 0
HP = highest number of total claims paid for, if greater than 20.			
<u>Indep. Claims</u>	<u>Extra Claims</u>	<u>Fee (\$)</u>	<u>Fee Paid (\$)</u>
1 - 3 or HP =	0	X 420	= 0
HP = highest number of independent claims paid for, if greater than 3.			

3. APPLICATION SIZE FEE					
If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$400 (\$200 for small entity or \$ 100 for micro entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).					
<u>Total Sheets</u>	<u>Extra Sheets</u>	<u>Number of each additional 50 or fraction thereof</u>	<u>Fee(\$)</u>	<u>Fee Paid (\$)</u>	
34	- 100 =	0 / 50	0 (round up to a whole number) x	400	0
34 *.75	26 - 100 =	0 / 50	0 EFS Fee Discount	400	0

4. OTHER FEE(S)		Fees Paid (\$)
Non-English Specification, \$140 fee (\$ 70 for small entity or \$35 for micro entity)		
Non-electronic filing fee under 37 CFR 1.16(t) for a utility application, \$400 fee (\$200 small or micro entity)		
Other (e.g., late filing surcharge):		140

SUBMITTED BY			
Signature	/ Carl J. Pellegrini /	Registration No. (Attorney/Agent)	40,766
Name (Print/Type)	Carl J. Pellegrini	Telephone:	202.293.7060
		Date:	June 7, 2013

SUPPLY VOLTAGE GENERATING CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Continuation Application of U.S.
5 Application No. 12/052,422 filed March 20, 2008, which claims the
benefit of the priority of Japanese patent application No.
2007-081754, filed on March 27, 2007, the disclosures of which are
incorporated herein in their entirety by reference thereto.

10 FIELD OF THE INVENTION

[0001]

This invention relates to a supply voltage generating circuit
and, more particularly, to a supply voltage generating circuit for
generating a boosted voltage within a semiconductor storage device.

15 BACKGROUND OF THE INVENTION

[0002]

If specifications relating to a DRAM are changed or the
specifications have not been fully decided, there are cases where the
supply voltage supplied from the outside in accordance with a
20 request from the user differs. A supply voltage supply circuit for
driving a word line is one circuit for which different supply voltages
are required of externally applied power. Designing such a supply
voltage supply circuit involves preparing a plurality of types of
transistors having oxide-film thicknesses for which circuit operation
25 is optimum, and designing the circuit based upon the plurality of

types of transistors. If a booster circuit is designed assuming a case where the power supplied will differ depending upon the specifications, the problem of oxide-film withstand voltage and a current-consumption problem ascribable to gate leakage must be
5 taken into account. If, in order to avoid these problems, a transistor for thick-film capacitance is used in the circuit in accordance with the higher voltage among voltages that have been set depending upon specifications, there is the danger that this will result in a booster circuit of larger area.

10 [0003]

Patent Document 1 describes a supply voltage generating circuit in which capacitors having different film thicknesses are used selectively in dependence upon the operating supply voltage, thereby reducing circuit layout area and generating a stable supply voltage.
15 This supply voltage generating circuit is one that boosts the operating supply voltage of the device and outputs the boosted voltage and has a first capacitor made of a thick insulating film, a second capacitor made of a thin gate insulating film, and a switch circuit for changing the circuit connections of the first and second
20 capacitors in accordance with the operating supply voltage.

[0004]

[Patent Document 1]

Japanese patent Kokai Publication No. JP-P2005-158098A

SUMMARY OF THE DISCLOSURE

25 [0005]

The following analyses are given by the present invention. The entire disclosure of the above mentioned patent document is incorporated herein by reference thereto.

The booster of the supply voltage generating circuit has a
5 boosting pump capacitor element that utilizes the oxide-film
capacitance of a transistor. There are many cases where the
boosting capacitor element requires a very large capacitance. This
necessitates a large area and has a major impact upon the area of the
overall chip. Since the capacitance of the oxide film is inversely
10 proportional to the thickness of the oxide film, usually use of a
thin-film capacitor element (thin-film transistor) is desired.
However, in a case where the supply voltage supplied from the
outside differs depending upon the specifications, as mentioned
above, a thick-film transistor usually is used as the boosting
15 capacitor element in order that the supply voltage supplied will not
exceed the breakdown (or withstand) voltage of a thin-film transistor.
Normally the value of a voltage for driving a word line will exhibit
almost no change even if the supply voltage supplied from the
outside changes. Accordingly, regardless of the fact that the lower
20 the external supply voltage, the greater the number of pump
capacitor elements required, a thick film having little capacitance
must be used even in a case where voltage is low because of the
breakdown voltage of the oxide film. Thus, with the conventional
circuitry, the design must be such that transistor breakdown voltage
25 will be in conformity with the high side of the external supply

voltage. Consequently, part of the booster capacitance in the booster circuit, e.g., the first capacitor in Patent Document 1, must be made a thick-film capacitor element and, hence, the degree to which chip area can be reduced is limited.

5 [0006]

Accordingly, it is an object of the present invention to provide a supply voltage generating circuit of smaller chip area.

[0007]

According to a first aspect of the present invention, there is
10 provided a supply voltage generating circuit comprising: a booster that outputs a boosted voltage upon generating the boosted voltage by charge pumping of a capacitor element. There is a power-supply step-down unit that steps down voltage of an external power supply to a voltage within a breakdown-voltage range of the capacitor
15 element, and applies the stepped-down voltage to the power supply of the booster. There is a switch circuit group that switches between application of the external power supply to the power supply of the booster directly or via the power-supply step-down unit.

[0008]

20 Preferably, in the supply voltage generating circuit of the present invention, the capacitor element is constituted by a MOS transistor having a gate oxide film, and the thickness of the gate oxide film is made less than thickness of a gate oxide film of a MOS transistor included in a load circuit having the output of the booster
25 as its power supply.

[0009]

Preferably, in the supply voltage generating circuit of the present invention, the booster comprises multiple stages of booster circuits, and thicknesses of gate oxide films of capacitor elements
5 constituted by MOS transistors included in respective ones of the booster circuits are the same.

[0010]

Preferably, in the supply voltage generating circuit of the present invention, the booster is so adapted that the number of
10 booster stages in the multiple stages of booster circuits is changed over by the switch circuit group in accordance with the power-supply voltage applied to the booster.

[0011]

Preferably, in the supply voltage generating circuit of the present invention, the booster includes a pre-stage booster circuit
15 and a post-stage booster circuit; the pre-stage booster circuit generates a first boosted signal having an amplitude between ground potential and a potential that is double the potential of the external power supply; the post-stage booster circuit receives, as an input, the
20 first boosted signal or a second boosted signal having an amplitude between ground potential and the output potential of the power-supply step-down unit; and the switch circuit group has a first switch element for switching a connection destination of the power supply of the booster to the external power supply or to the output of
25 the power-supply step-down unit, and a second switch element for

switching a connection destination of the input of the post-stage booster circuit to the first or second boosted signal; wherein the second switch element is switched to the first boosted signal when the first switch element has been switched to the external power supply, and the second switch element is switched to the second boosted signal when the first switch element has been switched to the output of the power-supply step-down unit.

[0012]

Preferably, in the supply voltage generating circuit of the present invention, it is so arranged that a capacitor element that has become unnecessary for the boosting operation in the multiple stages of booster circuits owing to switching by the switch circuit group in accordance with the power-supply voltage applied to the booster is connected by the switch circuit group and made to function as a capacitor element for stabilizing the output of the power-supply step-down unit.

[0013]

Preferably, in the supply voltage generating circuit of the present invention, the switch circuit group is controlled by any of a metal option, fuse option and bonding option.

In a second aspect of the present invention, there is provided a semiconductor storage device comprising the supply voltage generating circuit, and a load circuit having the output of the booster as its power supply.

[0014]

The meritorious effects of the present invention are summarized as follows.

In accordance with the present invention, the voltage of the external power supply is stepped down to a voltage within the breakdown-voltage range of the capacitor element and is supplied to the booster in a case where the voltage of the external power supply exceeds the breakdown voltage of the capacitor element. As a result, thin-film capacitor elements can be used for all of the capacitor elements in the booster. This makes it possible to reduce chip area.

Other features and advantages of the present invention will be apparent from the following description taken in conjunction with the accompanying drawings, in which like reference characters designate the same or similar parts throughout the figures thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram illustrating the configuration of a supply voltage generating circuit according to an exemplary embodiment of the present invention;

Fig. 2 is a circuit diagram of a booster according to an exemplary embodiment of the present invention;

Fig. 3A is an equivalent circuit in a case where the booster performs a two-stage operation, and Fig. 3B is a timing chart illustrating the waveforms of signals associated with the equivalent circuit;

Fig. 4A is an equivalent circuit in a case where the booster

performs a single-stage operation, and Fig. 4B is a timing chart illustrating the waveforms of signals associated with the equivalent circuit; and

Fig. 5 is a circuit diagram of a power-supply step-down unit.

5 PREFERRED MODES OF THE INVENTION

A preferred exemplary embodiment of the present invention will now be described in detail with reference to the accompanying drawings.

[0015]

10 Fig. 1 is a block diagram illustrating the configuration of a supply voltage generating circuit according to an exemplary embodiment of the present invention. As shown in Fig. 1, the supply voltage generating circuit includes a power-supply step-down unit 10, a booster 20 and a switch element SW1.

15 [0016]

The booster 20 generates a boosted voltage by the charge pumping of capacitor elements and outputs the boosted voltage generated. In a case where the voltage of an external power supply exceeds the breakdown voltage of the capacitor elements, the
20 power-supply step-down unit 10 steps down the external supply voltage to a voltage within the range of breakdown voltage of the capacitor elements and applies the stepped-down voltage to the power supply of the booster 20. The switch element SW1 switches between application of the external power supply to the power supply
25 of the booster 20 directly or via the power-supply step-down unit 10.

[0017]

The capacitor elements in the booster 20 are constituted by MOS transistors. Preferably, the thickness of the gate oxide film of each MOS transistor is made less than the thickness of a gate oxide film of a MOS transistor included in a load circuit having the output VPP (Fig. 1) of the booster 20 as its power supply. An example of the load circuit is a circuit for driving a word line.

[0018].

Preferably, the booster 20 comprises multiple booster circuits 21a and 21b, and the thicknesses of gate oxide films of the capacitor elements constituted by the MOS transistors included in respective ones of the booster circuits are the same.

[0019]

Preferably, the booster 20 is so adapted that the number of booster stages (e.g., one stage or two stages) constituted by the multiple booster circuits 21a, 21b is changed over by a switch element SW2 in accordance with the power-supply voltage applied to the booster 20.

[0020]

It may be so arranged that a semiconductor storage device typified by a DRAM, particularly a DDR-SDRAM, includes a supply voltage generating circuit having the above-described configuration, and a load circuit (not shown) the power supply of which is the output of the booster 20. An example of the load circuit is a circuit for driving a word line.

[0021]

In accordance with the supply voltage generating circuit having the above-described configuration, the voltage of the external power supply is stepped down by the power-supply step-down unit 10 in a case where the external supply voltage is so high as to exceed the breakdown voltage of the capacitor elements (thin-film transistors). This is based upon the condition that the external supply voltage will differ depending upon the specifications. It is possible for thin-film capacitor elements having a large capacitance to be used in the booster 20 and to be used conjointly also in a case where the supply voltage is low. Accordingly, layout area in the chip can be reduced by a wide margin. Now an exemplary embodiment of the present invention will be described in detail.

[EXEMPLARY EMBODIMENT]

15 [0022]

Fig. 1 is a block diagram illustrating a supply voltage generating circuit according to an exemplary embodiment of the present invention. As shown in Fig. 1, the supply voltage generating circuit includes the power-supply step-down unit 10, booster 20 and switch element SW1, which is of single-pole, double-throw type. The switch element SW1 switches between application of the voltage of an external power supply VDDP1 to power supply Vdd of the booster 20 directly or as power supply VDLP following stepping down of the voltage of an external power supply VDDP2 by the power-supply step-down unit 10,

[0023]

The booster 20 includes a pre-stage booster circuit 21a, a post-stage booster circuit 21b, and single-pole, double-throw switch element SW2 for switching between the booster circuits 21a and 21b.

5 The booster 20 generates a boosted voltage from power supply Vdd by charge pumping of the capacitor elements using a driving signal S0, and supplies the boosted voltage to a load circuit, an example of which is a circuit for driving a word line, as power supply VPP. At this time the switch element SW2 changes over the number of

10 booster stages in the booster 20 to one stage, namely the booster circuit 21b, or to two stages, namely the booster circuits 21a and 21b.

[0024]

The booster circuit 21a receives the driving signal S0 as an

15 input and outputs a signal (a first boosted signal) having an amplitude between ground potential and a potential that is double the potential of the external power supply VDDP1. Further, the booster circuit 21b receives a signal (a second boosted signal) having an amplitude between ground potential and the potential of power

20 supply VDLP, or the output signal (the first boosted signal) of the booster circuit 21a, as an input, boosts the signal and outputs the boosted signal as power supply VPP. The switch element SW2 is switched to the first boosted signal when the switch element SW1 has been switched to the external power supply VDDP1, and the

25 switch element SW2 is switched to the second boosted signal when

the switch element SW1 has been switched to the output (VDLP) of the power-supply step-down unit 10.

[0025]

The details of the booster 20 will be described next. Fig. 2 is a circuit diagram of the booster according to this exemplary embodiment of the present invention. As shown in Fig. 2, the booster 20 includes the booster circuits 21a, 21b and a signal supply circuit 22 to which the signal S0 is input and which outputs signals S1 to S5. The booster circuit 21a has N-channel transistors N1, N2, a P-channel transistor P1, a capacitor element C1 constituted by a MOS transistor, and single-pole, double-throw switch elements SW3 to SW7. The booster circuit 21b has N-channel transistors N3, N4, a capacitor element C2 constituted by a MOS transistor, and the switch element SW2. The N-channel transistor N1 and capacitor elements C1, C2 are transistors (thin-film transistors) each having a thick gate insulating film. The N-channel transistors N2 to N4 and the P-channel transistor P1 are transistors (thick-film transistor) each having a thick gate insulating film. Furthermore, the switches SW1 to SW7 are controlled by a changeover switch-option signal according to any of a metal option, fuse option or bonding option.

[0026]

The N-channel transistor N1 has a drain connected to the power supply Vdd, a source connected to one end of the switch element SW4, the other end of which is connected to the power supply Vdd, and to the source of the P-channel transistor P1, and a

gate connected to the contact on the single-pole side of the switch element SW5. The P-channel transistor P1 has a drain connected to the drain of the N-channel transistor N2 and to one end of the switch element SW2, and a gate connected to the contact on the single-pole side of the switch element SW3. The N-channel transistor N2 has a source connected to power supply Vss (ground) and a gate connected to the single-pole side of the switch element SW6. The capacitor element C1 has one end connected to the contact on the single-pole side of the switch element SW4, and its other end connected to the contact on the single-pole side of the switch element SW7. The signal S3 is applied to one end of the switch element SW3, the other end of which is connected to the power supply Vss. The signal S1 is applied to one end of the switch element SW5, the other end of which is connected to the power supply Vss. The signal S2 is applied to one end of the switch element SW7, the other end of which is connected to the power supply Vss. The signal S3 is applied to one end of the switch element SW6, the other end of which is connected to the power supply Vdd.

[0027]

The N-channel transistor N3 has a drain connected to the power supply Vdd, a source connected to one end of the capacitor element C2 and to the drain of the N-channel transistor N4, and a gate to which the signal S1 is applied. The N-channel transistor N4 has a source connected as the power supply VPP and a gate to which the signal S5 is applied. The capacitor element C2 has its other end

connected to the contact on the single-pole side of the switch element SW2. The signal S4 is applied to the other end of the switch element SW2.

[0028]

5 Described next will be operation of the booster circuits when the switches SW2 to SW7 in Fig. 2 are changed over in operative association with the switch element SW1 in Fig. 1. Fig. 3A illustrates the connections in a case where the voltage of the external power supply VDDP1 is lower than the thin-film transistor
10 breakdown voltage, and Fig. 4A illustrates the connections in a case where the voltage of the external power supply VDDP2 is higher than the thin-film transistor breakdown voltage. It should be noted that the power supplies and the voltage values of these power supplies will be represented by the same reference characters. VDDP1
15 indicates external supply voltage that is lower than the thin-film transistor breakdown voltage, VDDP2 indicates external supply voltage that is higher than the thin-film transistor breakdown voltage, VPP indicates supply voltage for driving a word line, and VDLP indicates supply voltage obtained by stepping down VDDP2 to the
20 range of the thin-film transistor breakdown voltage by the power-supply step-down unit 10. That is, it is assumed that the allowable range of thin-film breakdown voltage is less than VDLP and that the allowable range of thick-film breakdown voltage is less than VPP. The relationships among these supply voltages are as
25 follows for the sake of simplicity: $VPP > VDDP2 > VDLP > VDDP1$,

$2 \cdot V_{DLP} > V_{PP}$, $3 \cdot V_{DDP1} > V_{PP}$, $V_{PP} > 2 \cdot V_{DDP1}$.

[0029]

Fig. 3A is an equivalent circuit in a case where the booster performs a two-stage operation, and Fig. 3B is a timing chart illustrating the waveforms of signals associated with the equivalent circuit. More specifically, Fig. 3A illustrates an equivalent circuit relating to the connections of the booster 20 in a case where the voltage of the external power supply V_{DDP1} is lower than the thin-film transistor breakdown voltage. Fig. 3B is a timing chart of the associated signals.

[0030]

(1) When the voltage level of the signal S1 is $2 \cdot V_{DDP1}$, the N-channel transistor N1 to the gate of which the signal S1 is applied turns on and the source of the N-channel transistor N1, namely one end of the capacitor element C1, is charged toward V_{DDP1} . Since the voltage level of the signal S3 is V_{DDP1} at this time, the P-channel transistor P1 is off and has no effect upon the charging operation of the capacitor element C1. It should be noted that the voltage level of the signal S2 is V_{SS} . Accordingly, the capacitor element C1 is charged by the potential $V_{DDP1} - V_{SS}$.

[0031]

On the other hand, since the voltage level of the signal S1 is $2 \cdot V_{DDP1}$, the N-channel transistor N3 turns on and contact A2, which is the source of the N-channel transistor N3, namely one end of the capacitor element C2, is charged toward V_{DDP1} . Since the

voltage level of the signal S3 is VDDP1 at this time, the N-channel transistor N2 is on and the potential at the other end of the capacitor element C2 is Vss.

[0032]

5 (2) If the voltage level of the signal S1 becomes VDDP1, then the voltage level of the signal S2 rises from Vss to VDDP1 and this is accompanied by a rise in the potential at the source of the N-channel transistor N1, namely at one end of the capacitor element C1, from VDDP1 to 2·VDDP1. The N-channel transistor N1 turns
10 off and has no effect upon the potential elevating operation. Since the voltage level of the signal S3 is Vss at this time, the P-channel transistor P1 is on and the N-channel transistor N2 is off. Accordingly, the potential at one end of the capacitor element C1 is transmitted to the other end of the capacitor element C2 as the
15 potential at contact (node) A1.

[0033]

As a result, the potential at one end of the capacitor element C2 rises from VDDP1 to 3·VDDP1. Since the voltage level of the signal S1 is VDDP1 at this time, the N-channel transistor N3 is off
20 and has no effect upon the potential elevating operation. Further, since the voltage level of the signal S5 is VDDP1+VPP, the N-channel transistor N4 turns on and the potential at one end of the capacitor element C2, namely at contact (node) A2, is transmitted to VPP. By supplying the electric charge that has accumulated by
25 charging in the capacitor element C2 to the outside, the potential at

contact A2 gradually declines.

[0034]

The booster 20 supplies VPP with a voltage close to $2 \cdot VDDP1$ by the operation described above. At this time, the locations at which the thin-film transistors of the capacitor elements C1 and C2, etc. are formed in the booster 20 are always subjected to only a difference potential of not more than VDDP1 across the gate and source or across the gate and drain.

[0035]

Fig. 4A is an equivalent circuit in a case where the booster performs a single-stage operation, and Fig. 4B is a timing chart illustrating the waveforms of signals associated with the equivalent circuit. More specifically, Fig. 4A illustrates an equivalent circuit relating to the connections of the booster 20 in a case where the voltage of the external power supply VDDP2 is higher than the thin-film transistor breakdown voltage. In this case, VDDP2 is stepped down to VDLP by the power-supply step-down unit 10 and VDLP is applied as the power supply Vdd of the booster 20.

[0036]

In Fig. 2, the N-channel transistor N1, which has its gate connected to Vss, is turned off. Further, the N-channel transistor N2, which has its gate connected to Vdd, turns on, and so does the P-channel transistor P1, which has its gate connected to Vss. Accordingly, the N-channel transistors N1, N2 and P-channel transistor P1, which have been isolated from the boosting operation,

have no effect upon the other circuits.

[0037]

On the other hand, as illustrated in Fig. 4A, one end of the capacitor element C1 is connected to the power supply Vdd, namely to the power supply VDLP which is the result or step-down by the power-supply step-down unit 10, and the other end of the capacitor element is connected to Vss. Accordingly, the capacitor element C1 functions as a stabilizing capacitance between Vdd/Vss in the booster 20.

10 [0038]

Fig. 4B is a timing chart of signals associated with Fig. 4A.

[0039]

(1) When the voltage level of the signal S1 is $2 \cdot VDDP1$, the N-channel transistor N3 to the gate of which the signal S1 is applied turns on and the source of the N-channel transistor N3, namely one end of the capacitor element C2, is charged toward VDLP. The other end of the capacitor element C2 is made Vss by the signal S4.

[0040]

(2) If the voltage level of the signal S1 becomes VDLP, then the voltage level of the signal S4 rises from Vss to VDLP and the potential at contact A2, namely at one end of the capacitor element C2, rises from VDLP to $2 \cdot VDLP$. Since the voltage level of the signal S1 is VDLP at this time, the N-channel transistor N3 is off and has no effect upon the potential elevating operation. Further, since the voltage level of the signal S5 is $VDLP + VPP$, the N-channel

transistor N4 turns on and the potential at one end of the capacitor element C2, namely at contact A2, is transmitted to VPP. By supplying the electric charge that has accumulated by charging in the capacitor element C2 to the outside, the potential at contact A2
5 gradually declines.

[0041]

The locations (portions) at which the thin-film transistors of the capacitor elements C1 and C2, etc. are formed in the booster 20 which operates as set forth above are always subjected to only a
10 difference potential of not more than V_{DDP1} across the gate and source or across the gate and drain.

[0042]

In a case where the external supply voltage is V_{DDP2} in the booster 20 constructed as described above, the configuration is made
15 one in which the number of booster stages is made a single stage. This is because $2 \cdot V_{DLP}$ is somewhat larger than VPP and the single-stage configuration is better than the two-stage configuration in that current consumption declines and a power supply at the VPP level is capable of being provided. The reason for this is that
20 although the contacts A1 and A2 in Fig. 3A should ideally take on potentials of $2 \cdot V_{DDP1}$ $3 \cdot V_{DDP1}$, respectively, in actuality the ideal potentials are not attained owing to the influence of parasitic capacitance. Accordingly, it is preferred in terms of obtaining good voltage conversion efficiency that the number of stages be made as
25 small as possible so as to eliminate the influence of parasitic

capacitance. Further, the two-stage configuration is not preferred over the one-stage configuration since current consumption increases by an amount commensurate with the increased number of operating contacts.

5 [0043]

Fig. 5 is a circuit diagram of the power-supply step-down unit 10. The power-supply step-down unit 10 is a circuit for performing driving by stepping down VDDP2 and bringing the power-supply voltage of VDLP/2, which has been generated within the DRAM, etc.,
 10 to the VDLP level. The power-supply step-down unit 10 has N-channel transistors N11 to N16, P-channel transistors P11 to P14 and switch elements SW8 to SW10. The N-channel transistors N12 and N13, which form a differential pair, have their sources tied together and connected to the N-channel transistor N11 serving as a
 15 current source, and have their drains connected respectively to the P-channel transistors P11, P12, which construct a current mirror. Further, VDLP/2 is applied to the gate of the N-channel transistor N12, and the gate of N-channel transistor N13 is connected to the middle point of a series circuit comprising diode-connected
 20 N-channel transistors N14 and N15. The drain of the N-channel transistor N12 is connected to the gate of the P-channel transistor P14, whose source is connected to VDDP2. Furthermore, the drain of the P-channel transistor P14 supplies the booster 20 with VDLP as the output of the power-supply step-down unit 10 and is connected to
 25 the anode (drain and gate) of the N-channel transistor N14. The

N-channel transistor N14 has its source connected to Vss.

[0044]

It should be noted that in a case where the step-down function of the power-supply step-down unit 10 is not used, the switch elements SW8 to SW10 shown in Fig. 5 are changed over so as not to actuate the power-supply step-down unit 10. That is, the gate of the P-channel transistor P13 becomes Vss, and P-channel transistor P13 turns on and the P-channel transistors P11, P12, P14 are turned off. Further, the gate of the N-channel transistor N11 becomes Vss, the N-channel transistor N11 turns off and supply of current to the N-channel transistors N12, N13 is halted. Furthermore, the gate of the N-channel transistor N16 becomes VDDP1, the N-channel transistor N16 turns on and VDLP is held at the level of Vss.

[0045]

The circuit of the power-supply step-down unit 10 is composed entirely of thick-film transistors since VDDP2, which exceeds the thin-film transistor breakdown voltage, is input to the circuit. In a case where VDDP1 is input as the external supply voltage, the switch elements SW8 to SW10 are changed over to deactivate the step-down function. It should be noted that the power-supply step-down unit 10 illustrated in Fig. 5 is one example and it is not necessarily required that the unit have a circuit configuration identical with that illustrated. Another circuit configuration may be adopted so long as it is one in which a power-supply voltage at the VDLP level is output from VDDP2.

[0046]

In accordance with the supply voltage generating circuit having the configuration described above, if external supply voltage exceeds the thin-film transistor breakdown voltage, then voltage is stepped down to a voltage within the breakdown-voltage range of the thin-film transistors and the supply voltage for driving a word line is boosted by the booster 20 composed of thin-film transistors. Accordingly, even in a case where the external supply voltage is so high as to exceed the thin-film transistor breakdown voltage, it is possible for thin-film capacitor elements (transistors for thin-film capacitance) having a large capacitance to be used in the booster 20, which is for driving a word line, and to be used conjointly also in a case where the supply voltage is low. Chip area can be reduced by constructing the booster 20 entirely of thin-film capacitor elements.

15 [0047]

Next, the invention will be described using specific numerical values. Assume that the following values hold: $V_{PP} = 2.5$ V, $V_{DDP2} = 1.8$ V, $V_{DLP} = 1.5$ V, $V_{DDP1} = 1.2$ V, thin-film transistor breakdown voltage = 1.5 V, and thick-film transistor breakdown voltage = 3.0 V. The thick-film transistor breakdown voltage is double the thin-film transistor breakdown voltage. In relation to the thickness of an oxide film, therefore, usually the thick film has twice the thickness of the thin film and, hence, the capacitance of the thick film is half that of the thin film. The transistor area is decided assuming a case where $V_{DDP1} = 1.2$ V holds, which is the

worst condition in terms of VPP supply capability. If thick-film capacitor elements are used, however, an area that is twice that for thin-film capacitor elements is required. The area of a pump capacitor element in a DRAM often is made several square millimeters. If area is halved, therefore, this is considerably beneficial in reducing chip area. It should be noted that chip area that corresponds to the power-supply step-down unit is increased by providing the supply voltage generating circuit with the power-supply step-down unit. In comparison with the area of the pump capacitor element, however, the area of the power-supply step-down unit is small enough to be negligible (the VDLP stabilizing capacitance need not be increased).

[0048]

In accordance with the supply voltage generating circuit of this exemplary embodiment, it is possible to adopt an arrangement in which the number of booster stages is changed over to the most efficient number depending upon the level of the external voltage by changing over the number of booster stages of the supply boosting circuitry for word-line drive by any of a metal option, fuse option or bonding option.

[0049]

This will be described in detail under conditions identical with those described earlier. In order to simply obtain $V_{PP} = 2.5 \text{ V}$, if the external supply voltage is $V_{DDP1} = 1.2 \text{ V}$, then boosting to $3 \cdot V_{DDP1} = 3.6 \text{ V}$ must be performed and two-stage boosting is

performed. By contrast, if $V_{DDP2} = 1.8 \text{ V}$ holds, then $2 \cdot V_{DLP} = 3.0 \text{ V}$ holds at $V_{DLP} = 1.5 \text{ V}$ and performance with regard to supplying VPP with power is good. This means that single-stage boosting suffices. The smaller the number of stages, the better the efficiency at which VPP is supplied with power.

[0050]

In the scheme described above, the booster circuits are switched between one and two stages depending upon the external supply voltage. However, the present invention is applicable also to a case where changeover between other numbers of stages becomes effective depending upon the value of VPP with respect to the external supply voltage. For example, the invention may be applied to changeover between two and three stages or between three and four stages, etc. Further, in extreme cases, the invention is applicable to changeover between one and three stages, etc. Furthermore, a case is conceivable in which external supply voltage does not exceed the thin-film transistor breakdown voltage and single-stage boosting is enough to supply power to VPP. Even in this case, however, the supply voltage generating circuit of this exemplary embodiment can be applied.

[0051]

Though the present invention has been described in accordance with the foregoing exemplary embodiments, the invention is not limited to these exemplary embodiments and it goes without saying that the invention covers various modifications and changes

that would be obvious to those skilled in the art within the scope of the claims.

It should be noted that other objects, features and aspects of the present invention will become apparent in the entire disclosure
5 and that modifications may be done without departing the gist and scope of the present invention as disclosed herein and claimed as appended herewith.

Also it should be noted that any combination of the disclosed and/or claimed elements, matters and/or items may fall under the
10 modifications aforementioned.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

first and second voltage terminals respectively supplied with first and second voltages different from each other;

an internal voltage node;

5 a switching circuit coupled between the first and second voltage terminals and the internal voltage node, taking either one of a first switching state in which the first voltage terminal and the internal voltage node are connected and a second switching state in which the second voltage terminal and the internal voltage node are connected; and

10 a voltage booster circuit including a voltage output node and first and second boosting circuit each coupled to the internal voltage node, the voltage booster circuit being configured such that the first and second voltage boosting circuits are coupled in series to the voltage output node when the switching circuit takes the first switching state and that the first boosting circuit coupled to the voltage output node and the
15 second boosting circuit is disconnected from each of the first boosting circuit and the voltage output node when the switching circuit takes the second switching state.

2. The semiconductor device as claimed in claim 1, further comprising a first external voltage terminal supplied with the first voltage, the first external voltage
20 terminal coupled to the first voltage terminal.

3. The semiconductor device as claimed in claim 2, further comprising a second external voltage terminal supplied with a third voltage and a internal voltage generator coupled to the second external voltage to be supplied with the third voltage

25 and configured to generate the second voltage at the second voltage terminal.

4. The semiconductor device as claimed in claim 3, wherein the third voltage is greater than the first voltage.

30 5. The semiconductor device as claimed in claim 4, wherein the third voltage is greater than the second voltage.

6. The semiconductor device as claimed in claim 1, wherein the second boosting circuit is configured to boost the first voltage supplied with the internal voltage node to generate a first boosting voltage and the first boosting circuit is configured to boost the first boosting voltage to generate at the voltage output node a second boosting voltage when the switching circuit takes the first switching state.

7. The semiconductor device as claimed in claim 6, wherein the first boosting circuit is configured to boost the second voltage supplied with the internal voltage node to generate at the voltage output node a third boosting voltage when the switching circuit takes the second switching state.

8. The semiconductor device as claimed in claim 1, wherein each of the first and second boosting circuits includes a capacitor and the capacitors of the first and second boosting circuits coupled in series to the voltage output node when the switching circuit takes the first switching state.

9. The semiconductor device as claimed in claim 8, wherein the capacitor of

50 the first boosting circuit is coupled to the voltage output node and the capacitor of the second boosting circuit is disconnected from each of the voltage output node and the capacitor of the first boosting circuit.

ABSTRACT OF THE DISCLOSURE

A supply voltage generating circuit that enables a reduction in chip area includes: a booster for outputting a boosted voltage upon
5 generating the boosted voltage by charge pumping of a capacitor element; a power-supply step-down unit for stepping down voltage of an external power supply to a voltage within a breakdown-voltage range of the capacitor element, and applying the stepped-down voltage to the power supply of the booster; and a switch element for
10 switching between application of the external power supply to the power supply of the booster directly or via the power-supply step-down unit. The booster comprises multiple stages of booster circuits. The thicknesses of gate oxide films of capacitor elements constituted by MOS transistors included in respective ones of the
15 booster circuits are the same and are made smaller than the thickness of a gate oxide film of a MOS transistor included in a load circuit having the output of the booster at its power supply.

FIG.1

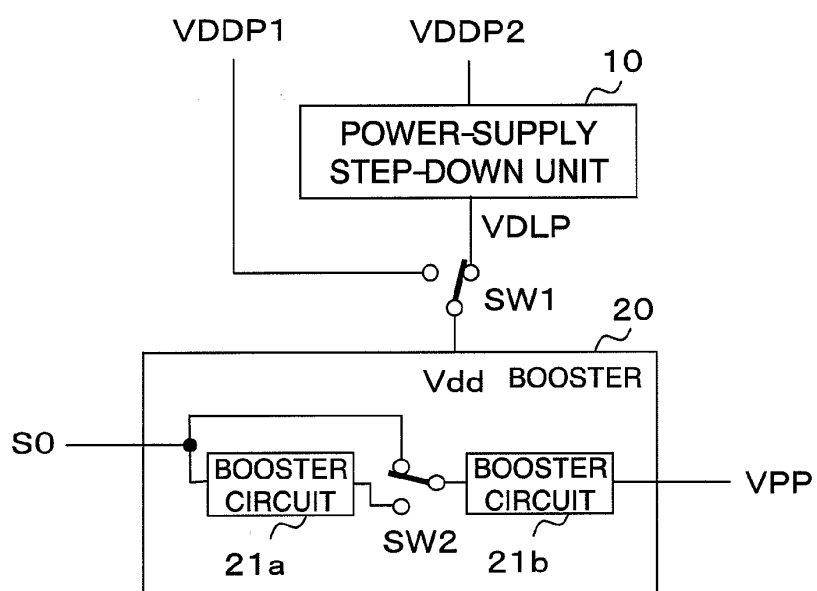


FIG.2

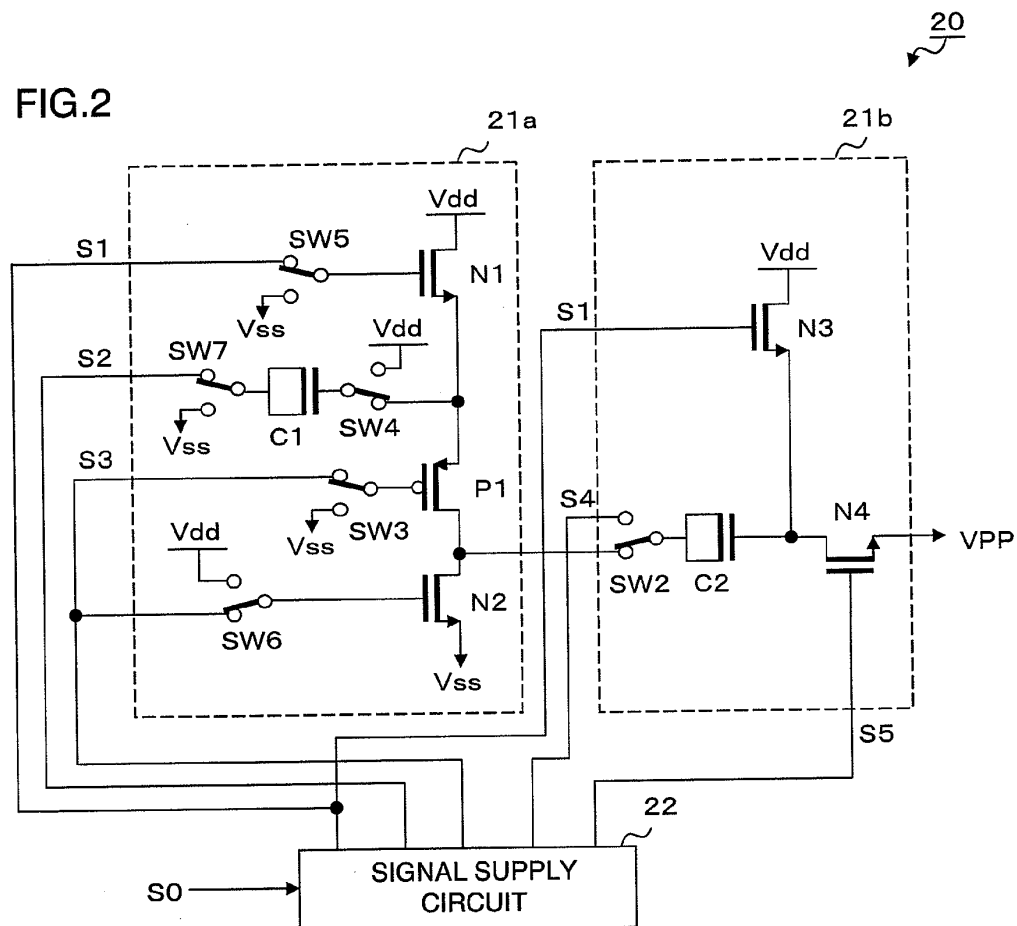


FIG.3A

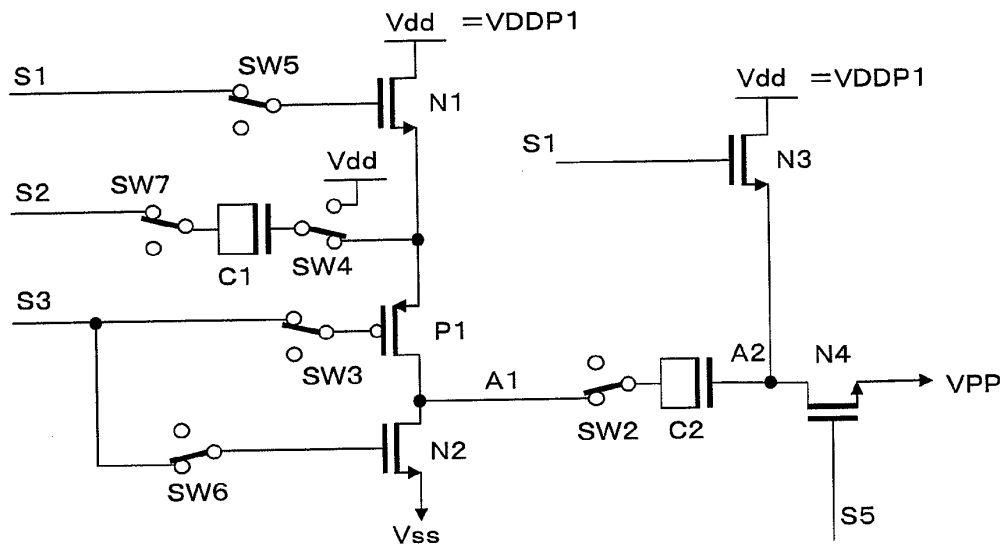


FIG.3B

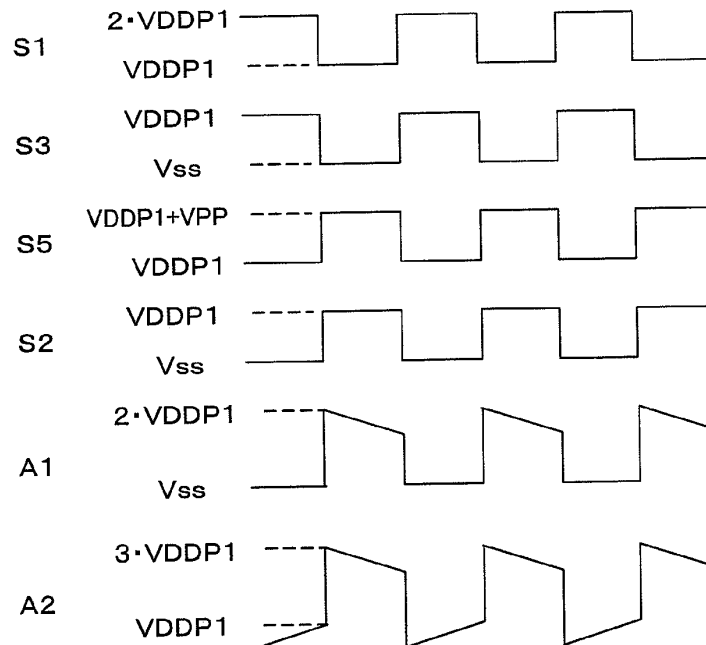


FIG.4A

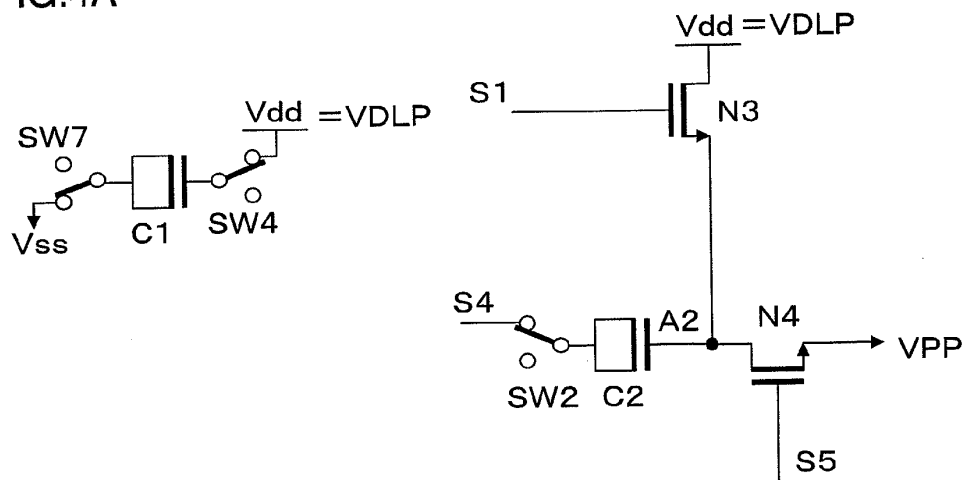


FIG.4B

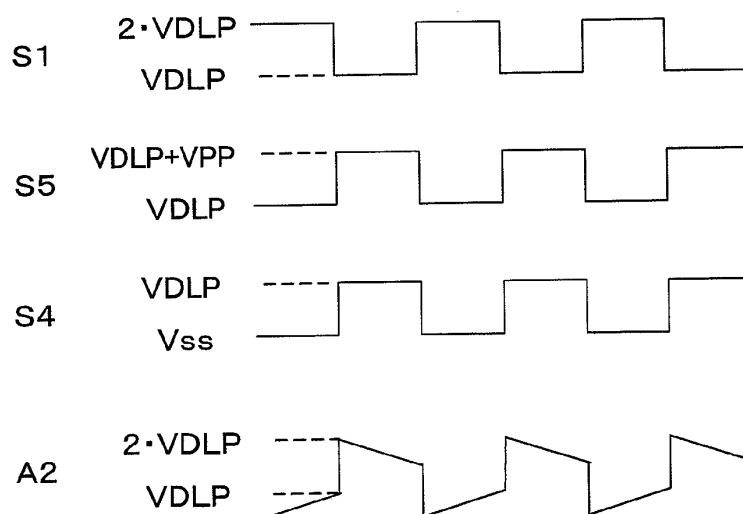
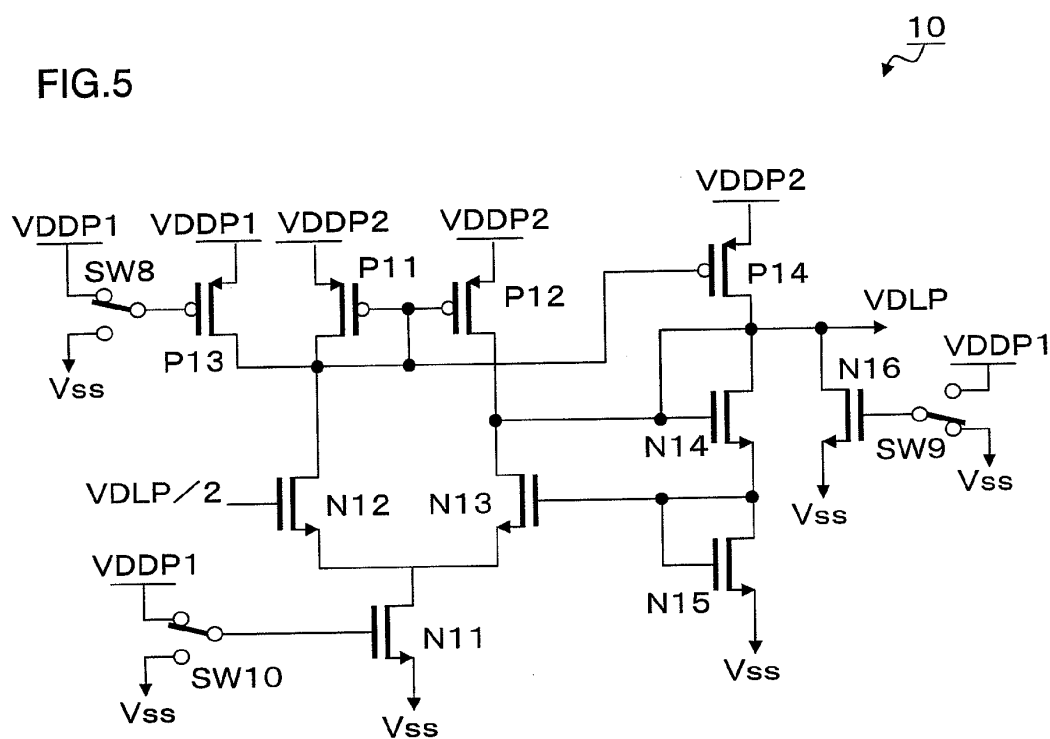


FIG.5



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Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
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2007-081754	JP	2007-03-27	

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Title of Invention	SUPPLY VOLTAGE GENERATING CIRCUIT		

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Docket No: Q204830

Koichiro HAYASHI, et al.

Appln. No.: Not Yet Assigned

Group Art Unit: Not Yet Assigned

Confirmation No.: Not Yet Assigned

Examiner: ALMO, Khareem E. (parent)

Filed: June 7, 2013

For: SUPPLY VOLTAGE GENERATING CIRCUIT

**INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §§ 1.97 and 1.98**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure under 37 CFR §1.56, Applicant hereby notifies the U.S. Patent and Trademark Office of the documents which are listed on the attached PTO/SB/08 A & B (modified) form which are all the references of record in parent application No. 12/052,422. Applicant is not submitting duplicate copies of these references but requests that they be listed on the face of any patent granted on the above application. (See 37 CFR §1.98(d)). Copies of any cited copending applications, if not previously submitted, are being submitted herewith.

The submission of the listed documents is not intended as an admission that any such document constitutes prior art against the claims of the present application. Applicant does not waive any right to take any action that would be appropriate to antedate or otherwise remove any listed document as a competent reference against the claims of the present application.

Respectfully submitted,

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §§ 1.97 and 1.98
U.S. Appln. No.: Not Yet Assigned

Attorney Docket No.: Q204830

/ Carl J. Pellegrini /

SUGHRUE MION, PLLC
Telephone: 202.293.7060
Facsimile: 202.293.7860

Carl J. Pellegrini
Registration No. 40,766

WASHINGTON OFFICE

23373

CUSTOMER NUMBER

Date: June 7, 2013

UTILITY PATENT APPLICATION TRANSMITTAL <i>(Only for new nonprovisional applications under 37 CFR 1.53(b))</i>		Attorney Docket No. Q204830	
		First Named Inventor Koichiro HAYASHI	
		Title	SUPPLY VOLTAGE GENERATING CIRCUIT
		Express Mail Label No.	
APPLICATION ELEMENTS <i>See MPEP chapter 600 concerning utility patent application contents.</i>		Commissioner for Patents P.O. Box 1450 Alexandria VA 22313-1450	
1. ☐ Fee Transmittal Form (PTO/SB/17 or equivalent) 2. ☐ Applicant asserts small entity status. See 37 CFR 1.27. 3. ☐ Applicant certifies micro entity status. See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent. 4. ☒ Specification [Total Pages <u>29</u>] Both the claims and abstract must start on a new page. (See MPEP § 608.01(a) for information on the preferred arrangement) 5. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets <u>5</u>] 6. Inventor's Oath or Declaration [Total Sheets <u> </u>] <i>(including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))</i> a. ☐ Newly executed (original or copy) b. ☐ A copy from a prior application (37 CFR 1.63(d)) 7. ☒ Application Data Sheet. *See note below. See 37 CFR 1.76 (PTO/AIA/14 or equivalent) 8. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (<i>Appendix</i>) ☐ Landscape Table on CD 9. ☐ Nucleotide and/or Amino Acid Sequence Submission <i>(if applications, items a. – c. are required)</i> a. ☐ Computer Readable Form (CRF) b. ☐ Specification Sequence Listing on: i. ☐ CD-ROM or CD-R (2 copies); or ii. ☐ Paper c. ☐ Statements verifying identity of above copies		ACCOMPANYING APPLICATION PAPERS 10. ☐ Assignment Papers (cover sheet & document(s)) Name of Assignee <u>ELPIDA MEMORY, INC.</u> 11. ☐ 37 CFR 3.73(c) Statement ☒ Power of Attorney <i>(when there is an assignee)</i> 12. ☐ English Translation Document <i>(if applicable)</i> 13. ☒ Information Disclosure Statement <i>(PTO/SB/08 or PTO-1449)</i> ☐ Copies of citations attached 14. ☐ Preliminary Amendment 15. ☐ Return Receipt PostCard <i>(MPEP § 503)(Should be specifically itemized)</i> 16. ☐ Certified Copy of Priority Document(s) <i>(if foreign priority is claimed)</i> 17. ☐ Nonpublication Request Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent. 18. ☒ Priority is claimed from: US 12/052,422 2008-03-20 JP 2007-081754 2007-03-27 The priority document(s) were filed in parent Application No. 12/052,422 19. ☐ Other:	
Note: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 must be included in an Application Data Sheet (ADS). (2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).			
☒ The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.			
20. If a CONTINUING APPLICATION , check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76: ☒ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: 12/052,422 Prior application information: Examiner: ALMO, KHAREEM Art Unit: 2816 E			
21. CORRESPONDENCE ADDRESS			
WASHINGTON OFFICE 23373 CUSTOMER NUMBER			
☒ The address associated with Customer Number:		OR ☐ Correspondence address below	
Signature / Carl J. Pellegrini / Name Carl J. Pellegrini		Date June 7, 2013 Registration No. 40,766	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	Not Yet Assigned
	Confirmation Number	Not Yet Assigned
	Filing Date	June 7, 2013
	First Named Inventor	Koichiro HAYASHI
	Art Unit	Not Yet Assigned
	Examiner Name	ALMO, Khareem E. (parent)
Attorney Docket Number	Q204830	

U.S. PATENTS						
Examiner Initials	Cite No	Patent Number	Kind Code	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	6,859,091		2005-02-22	NICHOLSON ET AL.	
	2.	7,288,984		2007-10-30	ARMAROLI ET AL.	
	3.	6,075,403		2000-06-13	ISHIKAWA ET AL.	
	4.	6,504,422		2003-01-07	RADER ET AL.	
	5.	6,218,818		2001-04-17	HAN-SANG KIM	
	6.	5,861,973	A	1999-01-19	INAGAKI ET AL.	

U.S. PATENT APPLICATION PUBLICATIONS						
Examiner Initials	Cite No	Publication Number	Kind Code	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	7.	2004/0155698	A1	2004-08-12	HAJIME KIMURA	
	8.	2007/0139982	A1	2007-06-21	UENO ET AL.	
	9.	2006/0186948	A1	2006-08-24	KELLY ET AL.	
	10.	2005/0219878	A1	2005-10-06	ITO ET AL.	
	11.	2007/0024341	A1	2007-02-01	MUGGLER ET AL.	
	12.	2004/0017241	A1	2004-01-29	TAKANORI SAEKI	
	13.	2005/0047180	A1	2005-03-03	HYOUNG-RAE KIM	
	14.	2005/0189983	A1	2005-09-01	SIVERO ET AL.	
	15.	2008/0094128	A1	2008-04-24	ITO ET AL.	
	16.	2007/0210774	A1	2007-09-13	KIMURA ET AL.	
	17.	2003/0169489	A1	2003-09-11	JIANG ET AL.	
	18.	2003/0048524	A1	2003-03-13	CHAVEZ-PIRSON ET AL.	
	19.	2006/0187540	A1	2006-08-24	ANDREJCO ET AL.	

FOREIGN PATENT DOCUMENTS								
Examiner Initials	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
	20.	2005-158098	JP	A	2005-06-16	ELPIDA MEMORY INC.		
	21.	2003249076	JP	A	2003-09-05	ELPIDA MEMORY INC. ET AL.		
	22.	5259289	JP	A	1993-10-08	FUJITSU KK		
	23.	11120784	JP	A	1999-04-30	TOSHIBA CORP.		

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. 2 Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). 3 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 4 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 5 Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	Not Yet Assigned
	Confirmation Number	Not Yet Assigned
	Filing Date	June 7, 2013
	First Named Inventor	Koichiro HAYASHI
	Art Unit	Not Yet Assigned
	Examiner Name	ALMO, Khareem E. (parent)
	Attorney Docket Number	Q204830

FOREIGN PATENT DOCUMENTS								
Examiner Initials	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
	24.	2002237185	JP	A	2002-08-23	SANYO ELECTRIC CO.		
	25.	200511475	JP	A	2005-01-13	MATSUSHITA ELECTRIC IND. CO.		

NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city, and/or country where published.	T
	26.	Communication dated January 31, 2012 from the Japanese Patent Office in counterpart Japanese application no. 2007-081754	
	27.	Non-final Office Action issued August 6, 2009 in Parent U.S. Application No. 12/052,422	N/A
	28.	Non-final Office Action issued February 4, 2011 in Parent U.S. Application No. 12/052,422	N/A
	29.	Non-final Office Action issued November 8, 2012 in Parent U.S. Application No. 12/052,422	N/A
	30.	Final Office Action issued March 11, 2011 in Parent U.S. Application No. 12/052,422	N/A
	31.	Final Office Action issued August 9, 2010 in Parent U.S. Application No. 12/052,422	N/A
	32.	Final Office Action issued August 1, 2011 in Parent U.S. Application No. 12/052,422	N/A
	33.	Advisory Action issued June 25, 2010 in Parent U.S. Application No. 12/052,422	N/A
	34.	Advisory Action issued December 22, 2011 in Parent U.S. Application No. 12/052,422	N/A
	35.	Notice of Allowance issued March 22, 2013 in Parent U.S. Application No. 12/052,422	N/A

EXAMINER SIGNATURE			
Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. 2 Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). 3 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 4 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 5 Applicant is to place a check mark here if English language translation is attached.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		SUPPLY VOLTAGE GENERATING CIRCUIT		
First Named Inventor/Applicant Name:		Koichiro HAYASHI		
Filer:		Carl Joseph Pellegrini/Hafida Sammane		
Attorney Docket Number:		Q204830		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Late Filing Fee for Oath or Declaration	1051	1	140	140
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1740

Electronic Acknowledgement Receipt	
EFS ID:	15982951
Application Number:	13912845
International Application Number:	
Confirmation Number:	5774
Title of Invention:	SUPPLY VOLTAGE GENERATING CIRCUIT
First Named Inventor/Applicant Name:	Koichiro HAYASHI
Customer Number:	23373
Filer:	Carl Joseph Pellegrini/Hafida Sammane
Filer Authorized By:	Carl Joseph Pellegrini
Attorney Docket Number:	Q204830
Receipt Date:	07-JUN-2013
Filing Date:	
Time Stamp:	16:15:12
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1740
RAM confirmation Number	3146
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Transmittal of New Application	UtilityTransmittal.PDF	83542 3b49962f7db5113978646b7c10d5c2b51e4f7ee1	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	FeeTransmittal.PDF	77172 ca28e290759d8536ec0f109cd58b81554fb3317f	no	1
Warnings:					
Information:					
3		SPECIFICATION.PDF	100013 39c94163a6287f008491b4c0749fc4f3668ff708	yes	29
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	25	
	Claims		26	28	
	Abstract		29	29	
Warnings:					
Information:					
4	Drawings-only black and white line drawings	DRAWINGS.PDF	50794 ba37c990de1e4e84a8ae5941a3858f28d8abe6c0	no	5
Warnings:					
Information:					
5	Application Data Sheet	ADS.PDF	1503135 e923dce0b3acbaae9e8b37a86bd437ad23347f	no	7
Warnings:					
Information:					
6		IDS.PDF	75184 e457ad29103701be993d336e34f5a3e64a101b3e	yes	4
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	2	
	Information Disclosure Statement (IDS) Form (SB08)		3	4	
Warnings:					

Information:					
7	Fee Worksheet (SB06)	fee-info.pdf	36433	no	2
			c7d228882289f3bac33473ce6cc3e436225 bcd28		
Warnings:					
Information:					
Total Files Size (in bytes):				1926273	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B or equivalent) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5. If the Power of Attorney by Applicant form is not accompanied by this transmittal form or an equivalent, the Power of Attorney will not be recognized in the application.

Application Number	13/912,845
Filing Date	June 7, 2013
First Named Inventor	Koichiro HAYASHI
Title	SUPPLY VOLTAGE GENERATING CIRCUIT
Art Unit	2816
Examiner Name	ALMO, Khareem E.
Attorney Docket Number	Q204830

SIGNATURE of Applicant or Patent Practitioner

Signature	/ Carl J. Pellegrini /	Date	June 7, 2013
Name	Carl J. Pellegrini	Telephone	202.293.7060

Registration Number	40766
---------------------	-------

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications.

☒ *Total of 1 forms are submitted.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

出願者による委任状 POWER OF ATTORNEY BY APPLICANT

私はここもと、添付の伝送書式中に同定されている出願書中の、以前のすべての委任状はこれを破棄する。
I hereby revoke all previous powers of attorney given in the application identified in the attached transmittal letter.

☒ 私は下記の顧客番号に関する特許弁護士を、私/私たちの弁護士あるいは代理人と指名し、添付の伝送書（(書式PTO/AIA/82A あるいはその同等書類)に記載されている出願に関連した米国特許商標局に対するすべての必要事項を遂行なすしめる。
I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

あるいは

OR

23373

☐ 私は下記の特許弁護士を、私/私たちの弁護士あるいは代理人と指名し、添付の伝送書（(書式PTO/AIA/82A あるいはその同等書類)に記載されている出願に関連した米国特許商標局に対するすべての必要事項を遂行なすしめる。
I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

登録名 Name Registration	番号 Number	登録名 Name Registration	番号 Number

上記に同定された特許の住所を認め、あるいは必要に応じて変更を行ってください。
Please recognize or change the correspondence address for the above-identified patent to:

☒ 上記顧客番号に関連した住所。
The address associated with the above-mentioned Customer Number.

あるいは

OR

☐ 顧客番号に関連した住所。
The address associated with Customer Number:

または

OR

☐ 事務所または個人名
Firm or Individual Name

住所 Address			
市町村名 City	州名 State	郵便番号 Zip	
国名 Country			
電話 Telephone		イーメール Email	

[1/2]

[Page 1 of 2]

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1460, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1460, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

出願者による委任状

POWER OF ATTORNEY BY APPLICANT

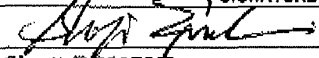
私は出願者であり:

I am the Applicant:

- ☐ 発明者あるいは共同発明者である
Inventor or Joint Inventor
- ☐ 死亡、あるいは禁治産者とされた発明者の法的代理人である
Legal Representative of a Deceased or Legally Incapacitated Inventor
- ☒ 被譲渡人あるいは発明者が譲渡する義務を負う人物である
Assignee or Person to Whom the Inventor is Under an Obligation to Assign
- 別面において十分な独力的所有権 (たとえば出願のなかで 37 CFR 1.46(b)(2) のもとにおける請願が出願のなかで受理された、あるいは本書類とともに申請がなされた場合) を有することを示した人物である)
- ☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document)

特許出願人の署名

SIGNATURE of Applicant for Patent

署名 Signature		日付 Date	October 22, 2012
姓名 Name	Shoji EGUCHI	電話 Telephone	(+81)-042-775-7632
肩書きおよび会社 Title and Company	Principal Professional / Elpida Memory, Inc.		

注記: 署名: 本書式は 37 CFR 1.33 にのっとり、出願者あるいは出願者の代理人の署名がなされていなければならない。署名およびその証明必要条件については 37 CFR 1.4 を参照のこと。署名がひとつ以上ある場合はその数の書式を提出すること。下記参照。

NOTE: Signature - This form must be signed by the applicant or applicant's representative in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms for more than one signature, see below.

☐ *提出書式の合計数は _____ である。

☐ *Total of _____ forms are submitted.

[2/2]

[Page 2 of 2]

Electronic Acknowledgement Receipt	
EFS ID:	15983236
Application Number:	13912845
International Application Number:	
Confirmation Number:	5774
Title of Invention:	SUPPLY VOLTAGE GENERATING CIRCUIT
First Named Inventor/Applicant Name:	Koichiro HAYASHI
Customer Number:	23373
Filer:	Carl Joseph Pellegrini/Hafida Sammane
Filer Authorized By:	Carl Joseph Pellegrini
Attorney Docket Number:	Q204830
Receipt Date:	07-JUN-2013
Filing Date:	
Time Stamp:	16:26:53
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	TransmittalPOA.PDF	379799 6e36ee6b8726fa758e6bce4cf0dad6799c3d92	no	3

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