

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,

Petitioner

v.

LONGITUDE LICENSING LTD.,

Patent Owner

IPR2023-01230
U.S. Patent No. 9,207,701

PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104

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PETITIONER'S EXHIBIT LIST

July 20, 2023

EX1001	U.S. Patent No. 9,207,701 to Hayashi et al. (“’701 patent”)
EX1002	Prosecution File History of the ’701 Patent (“’768 app”)
EX1003	Declaration of Dr. Harvey J. Stiegler
EX1004	CV of Dr. Harvey J. Stiegler
EX1005	U.S. Patent No. 7,427,888 to Zhang et al. (“Zhang”)
EX1006	U.S. Patent No. 5,767,735 to Javanifard et al. (“Javanifard”)
EX1007	Prosecution File History of Zhang (App. 10/888667) (“’667 app”)
EX1008	Charge Pump Circuit Design, Pan et al., 1st Edition, 2006 (“Pan”)
EX1009	Prosecution File History of Parent of ’701 patent (App. 12/052422) (“’422 app”)
EX1010	Prosecution File History of Parent of ’701 patent (App. 13/912845) (“’845 app”)
EX1011	Order Granting Western Digital’s Motion to Stay (Amazon) (05-16-23)
EX1012	Order Granting Western Digital’s Motion to Intervene (Amazon) (05-16-23)
EX1013	Director Vidal Memorandum re: Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, June 22, 2022
EX1014	U.S. Patent No. 7,579,902 to Frulio et al. (“Frulio”)
EX1015	U.S. Patent No. 7,477,093 to Al-Shamma et al. (“Al-Shamma”)
EX1016	U.S. Patent No. 7,046,076 to Daga et al. (“Daga”)
EX1017	U.S. Patent No. 6,157,242 to Fukui (“Fukui”)
EX1018	U.S. Patent No. 7,505,350 to Lee et al. (“Lee”)
EX1019	U.S. Patent No. 6,954,386 to Narui et al. (“Narui”)

EX1020	“Charge Pump Circuits with Low Area and High Power Efficiency for Memory Applications,” Kang et al., Journal of Semiconductor Technology and Science, Vol. 6, No. 4, December 2006
EX1021	U.S. Patent No. 6,034,539 to Hwang (“Hwang”)
EX1022	U.S. App. Pub. No. 2003/0067063A1 to Muff et al. (“Muff”)
EX1023	U.S. Patent No. 6,346,738 to Kim et al. (“Kim”)
EX1024	Declaration of Dr. Sylvia D. Hall-Ellis

LISTING OF CHALLENGED CLAIMS

Claim 1	
[1.0]	1. A method for generating a supply voltage, comprising:
[1.1]	selecting one of a first input node supplied with a first power supply voltage and a second input node supplied with a second power supply voltage that is higher than the first power supply voltage;
[1.2.1]	coupling a selected one of the first and second input nodes to booster circuitry comprising a plurality of booster stages to provide an output voltage,
[1.2.2]	wherein selection of the first input node corresponds to a first number of booster stages and
[1.2.3]	selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number; and
[1.3]	changing the booster circuitry from the first number of booster stages corresponding to selection of the first input node to the second number of booster stages when the second input node is selected.
Claim 2	
[2.0]	2. The method as claimed in claim 1, wherein the output voltage is the same when the first input node is selected and when the second input node is selected.
Claim 3	
[3.0]	3. The method as claimed in claim 1, wherein the output voltage is higher than the second power supply voltage.
Claim 4	

[4.0]	4. The method as claimed in claim 1, wherein the second number of booster stages is one.
Claim 5	
[5.0]	5. The method as claimed in claim 4, wherein the first number of booster stages is two.
Claim 6	
[6.0]	6. The method as claimed in claim 1, wherein the booster circuitry is changed between the first number of booster stages and the second number of booster stages with a switch.
Claim 7	
[7.0]	7. The method as claimed in claim 1, wherein the booster circuitry is changed with a selected one of a metal option, a bonding option, and a fuse option.
Claim 8	
[8.0]	8. The method as claimed in claim 1, wherein the output voltage is a power supply voltage VPP.
Claim 9	
[9.0]	9. The method as claimed in claim 1, wherein the booster circuitry comprises capacitors formed using thin gate oxide transistors.
Claim 10	
[10.0]	10. A semiconductor device comprising:
[10.1]	a first input node supplied with a first power supply voltage;
[10.2]	a second input node supplied with a second power supply voltage higher than the first power supply voltage;

[10.3]	booster circuitry comprising a plurality of booster stages to provide an output voltage; and
[10.4]	a first switch configured to couple a selected one of the first input node and the second input node to the booster circuitry,
[10.5]	wherein the booster circuitry configured to have a first number of booster stages when the first input node is selected and to be changed to a second number of booster stages when the second input node is selected, the second number being less than the first number.
Claim 11	
[11.0]	11. The semiconductor device as claimed in claim 10, wherein the output voltage is the same when the first input node is selected and when the second input node is selected.
Claim 12	
[12.0]	12. The semiconductor device as claimed in claim 10, wherein the output voltage is higher than the second power supply voltage.
Claim 13	
[13.0]	13. The semiconductor device as claimed in claim 10, wherein the second number of booster stages is one.
Claim 14	
[14.0]	14. The semiconductor device as claimed in claim 13, wherein the first number of booster stages is two.
Claim 15	
[15.0]	15. The semiconductor device as claimed in claim 10, wherein the booster circuitry is changed from the first number of booster stages and the second number of booster stages with a second switch.
Claim 16	

[16.0]	16. The semiconductor device as claimed in claim 10, wherein the booster circuitry is changed with a selected one of a metal option, a bonding option, and a fuse option.
Claim 17	
[17.0]	17. The semiconductor device as claimed in claim 10, wherein the output voltage is a power supply voltage VPP.
Claim 18	
[18.0]	18. The semiconductor device as claimed in claim 10, wherein the booster circuitry comprises capacitors formed using thin gate oxide transistors.

I. INTRODUCTION

U.S. Patent No. 9,207,701 (the “’701 Patent”) relates to “a supply voltage generating circuit and, more particularly, to a supply voltage generating circuit for generating a boosted voltage within a semiconductor storage device.” EX1001, ’701 patent, Title, 1:14-20. Western Digital Technologies, Inc. (“Petitioner” or “WDT”) respectfully request that the Board review and cancel as unpatentable under (pre-AIA) 35 U.S.C. §103(a) claims 1-18 (“Challenged Claims”) of the ’701 patent, which is all the claims of the patent.

II. GROUNDS FOR STANDING

Petitioner certifies that the ’701 patent is eligible for IPR and that Petitioner is not barred or estopped from requesting IPR challenging the patent claims. 37 C.F.R. § 42.104(a).

III. TECHNOLOGY BACKGROUND

Dr. Stiegler’s declaration provides a background of the relevant technology, including charge pumps and pump stages. EX1003, ¶¶33-41 (citing EX1008, EX1014, EX1015, EX1016).

IV. THE ’701 PATENT

A. Summary

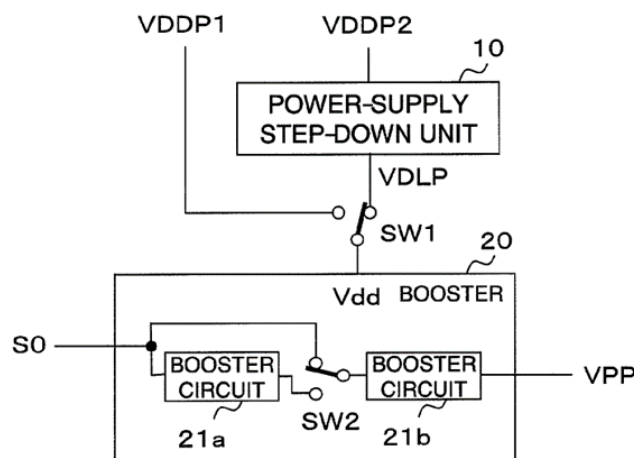
In conventional semiconductor storage devices, such as flash or EEPROM, there will be one or more power supply voltages such as VDD. For example, a first power supply voltage (VDD1) of 5V can be used for one section of the device,

and a second power supply voltage (VDD2) of 3.3V can be used in another section of the device. EX1003, ¶¶42-47.

Continuing with the example, these semiconductor storage devices may periodically require an additional, higher, supply voltage, such as 7V, to perform operations such as a memory erase. These additional supply voltages can be internally produced by a booster circuit, or charge pump circuit. Continuing with the examples above, it was well known that boosting a first power supply voltage VDD1 of 3.3V to a supply voltage 7V is different from boosting a second power supply voltage VDD2 of 5V to 7V.

FIG. 1 of '701 patent reproduced below shows a switch SW1 for selecting between two different power supply voltages VDDP1 and VDDP2 (VDLP). The selected supply voltage is then provided to a booster 20 for generating the pump voltage VPP. EX1001, '701 patent, 4:49-59.

FIG.1



EX1001, '701 patent, FIG. 1

The booster 20 includes a second switch SW2 for “switching between the booster circuits 21a and 21b,” based on the selection of switch SW1. EX1001, ’701 patent, 4:60-5:4. In this way, booster 20 with the corresponding number of booster stages (based on the configuration of booster circuits 21a and 21b) can be used for the selected supply voltage.

As discussed in detail below, the device and method presented in the ’701 patent, namely, changing the number of booster stages of a booster circuitry according to selection of the input power supply voltage, was well known to a POSITA before the priority date of the ’701 patent.

B. Prosecution History

In Office Actions dated October 7, 2014 and January 9, 2015, Examiner rejected claims 1-10 as anticipated over prior art. EX1002, ’768 app, 126-133 and 144-151; EX1003, ¶¶48-54.

After Applicant amended the claims, Notice of Allowance issued on August 3, 2015, and the examiner’s statement of reasons for allowance stated the prior art of record failed to suggest or disclose “wherein the booster circuitry configured to have a first number of booster stages when the first input node is selected to be changed to a second number of booster stages when the second input node is selected, the second number being less than the first number.” EX1002, ’768 app, 28.

V. LEVEL OF ORDINARY SKILL IN THE ART

The level of ordinary skill in the art may be reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). Here, a Person of Ordinary Skill in the Art (“POSITA”) at the time of the claimed invention would have a bachelor’s or the equivalent degree in electrical or computer engineering or a related field, and 2-3 years of professional experience relating to circuit design. EX1003, ¶58. Furthermore, a person with less formal education but more experience, or more formal education but less experience, could have also met the relevant standard for POSITA. *Id.* However, Petitioner does not imply that a person having an extraordinary level of skill should be regarded as POSITA.

VI. CLAIM CONSTRUCTION

During IPR, claims are construed according to the standard as set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. §42.100(b) (Nov. 13, 2018). Petitioner believes that, for the purposes of this proceeding and the analysis presented herein, no claim term requires express construction. *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999). Accordingly, this Petition analyzes the claims consistent with ordinary and customary meaning as would be understood by POSITA in light of the specification. *Phillips*, 415 F.3d at 1314-17; EX1003, ¶¶60-61.

VII. REQUESTED RELIEF

Petitioner asks the Board to institute trial and cancel the Challenged Claims.

VIII. OVERVIEW OF CHALLENGES

A. Challenged Claims

Claims 1-18 (“Challenged Claims”) of the ’701 patent are challenged.

B. Statutory Grounds for Challenges

Ground	Claims	Basis
#1	1-18	§103(a) over Zhang in view of Javanifard
#2	1-18	§103(a) over Javanifard
#3	9 and 18	§103(a) over Zhang in view of Javanifard and Kang
#4	9 and 18	§103(a) over Javanifard in view of Kang

Zhang was filed July 8, 2004, published January 13, 2005, and issued September 23, 2008. Zhang is prior art under at least §§102(a), 102(b), and §102(e).

Javanifard issued June 16, 1998, and is prior art under at least §§102(a) and 102(b).

Kang was published, indexed, and publicly accessible as of at least December 31, 2006, and is prior art under at least §102(a). EX1024, Hall-Ellis Declaration, ¶46; EX1003, ¶¶83-85.

C. Discretionary Denial is Not Warranted

Petitioner respectfully submits that the Board should not exercise its discretion under 35 U.S.C. §§314(a) or 325(d) to deny this Petition.

1. The Fintiv factors favor institution.

Denial would be improper based on factors in *Apple v. Fintiv*, IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) (precedential).

Factor 1: Stay in District Court Favors Institution

One litigation (Amazon Action) concerning the '701 Patent is pending in CDCA, involving the Patent Owner and WDT's customer Amazon. *See* XI. B. WD's motion to intervene was granted in the Amazon Action. EX1012. The Amazon Action with respect to Amazon is stayed pending the resolution of the Amazon Action with respect to WDT. EX1011. This factor weighs in favor of institution. *Snap, Inc. v. SRK Tech. LLC*, IPR2020-00820, Paper 15 at 8-9 (PTAB Oct. 21, 2020) (precedential) (granting stay allays concerns about inefficiency and duplication efforts).

Factor 2: Unscheduled Trial Date Favors Institution.

In the Amazon Action with respect to WDT, the litigation is in its early stages. The Court has not set a case schedule; the scheduling conference is set to occur on July 21, 2023. Amazon Action, Dkt. 46. No claim construction briefing has been scheduled. No trial date has been set.

Factor 3: Lack of Investment in Parallel Proceedings Favors Institution.

The co-pending litigation is either stayed or in early stages, and the investment has been minimal. The lack of investment in the parallel proceeding favors institution.

Factor 4: No Overlapping Issues with the Parallel Proceeding Favors Institution.

There is no overlap of prior art issues at this time. If the Board institutes trial, Petitioner will not assert in the co-pending litigation the combination of references on which trial is instituted for the claims on which trial is instituted, to the extent Petitioner even asserts the same combination in the district court. *See Verizon v. Huawei*, IPR2020-01079, Paper 10 at 38 (finding a similar stipulation “mitigates the concern about overlapping issues” and weighs “against discretionary denial of the Petition”).

Factor 5: Whether Petitioner is Defendant Is Neutral.

Petitioner is an intervener in the Amazon Action with respect to WDT. This factor is neutral and should not be a basis for denying institution. *See HP Inc. v. Slingshot Printing LLC*, IPR2020-01084, Paper 13 at 9 (having the “same parties as parallel proceeding” makes factor 5 “neutral”).

Factor 6: Other Circumstances Including Merits Favors Institution.

As detailed below, every element of the Challenged Claims is expressly shown in or obvious in view of well-known art, and as such, this petition “presents compelling evidence of unpatentability.” Director Vidal’s Guidance Memorandum,

EX1013, 2. Even if the Board determines that the other *Fintiv* factors favor a discretionary denial—which they do not—the Director’s *Fintiv* Guidance strongly supports institution of this challenge. See *CommScope Technologies LLC v. Dali Wireless, Inc.*, IPR2022-01242, Paper 23 at 4-5 (PTAB Feb. 27, 2023) (precedential).

In short, investments in the parallel proceeding is minimal, and *Fintiv* factors are either neutral or weigh against discretionary denial. Thus, the *Fintiv* factors weigh in favor of institution.

2. Advanced Bionics Test Favors Institution.

In determining whether to institute an IPR, the Board may consider whether “the same or substantially the same prior art or arguments previously were presented to the Office.” §325(d); *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 7 (PTAB Feb. 13, 2020).

The Advanced Bionics test regarding the prior art references favors institution because they were not the same or substantially the same art presented to the Office. The Examiner did not consider Zhang, Javanifard, or Kang during the prosecution. Moreover, they are non-cumulative, because they teach the claimed features including those provided by the reasons for allowance of the ’701 patent. See EX1002, ’768 App, 28-29.

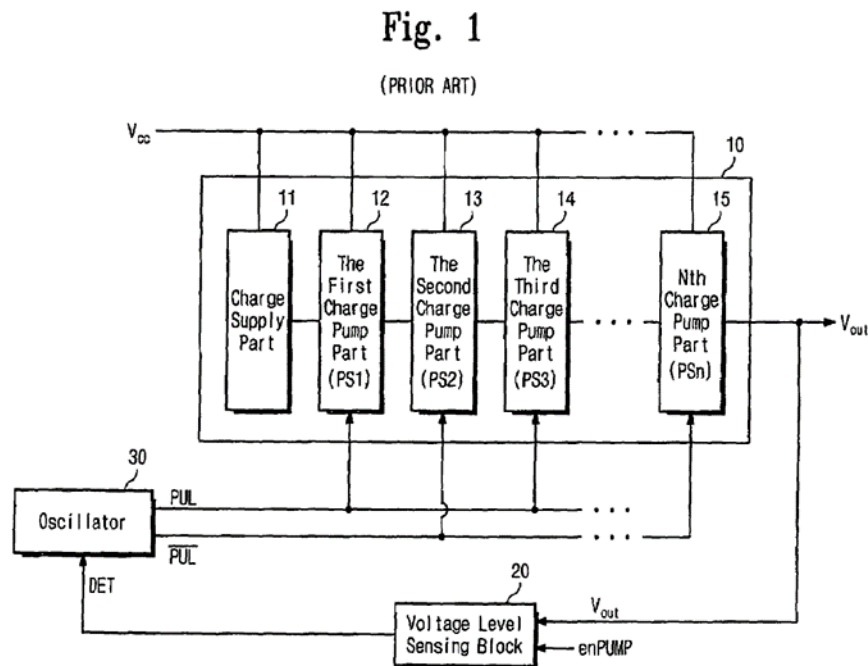
IX. IDENTIFICATION OF HOW THE CLAIMS ARE UNPATENTABLE

A. Overview of Prior Art

1. Zhang (EX1005)

Zhang describes a “Charge Pump Circuit Operating Responsive to a Mode,” and describes “a charge pump circuit that operates responsive to a test or general operation mode.” EX1005, Zhang, Title, Abstract; EX1003, ¶¶67-72.

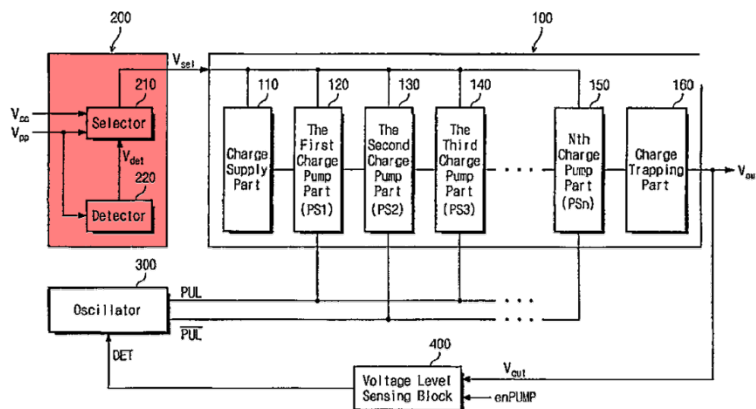
Zhang explains the issue with the conventional charge pump circuit, as shown in FIG. 1 below. Specifically, “the time to precharge [nodes of charge pump parts] increases in the output voltage V_{out} ,” and this “additional time is undesired, particularly where testing integrated chips that require high voltages quickly.” EX1005, Zhang, 1:15-18, 1:33-39, 1:63-2:2; EX1003, ¶¶68-69.



EX1005, Zhang, FIG. 1

To address this issue, Zhang describes an improved charge pump design, as shown in annotated FIG. 4 below, which by using a selecting circuit block 200 to supply a selected voltage from VCC and VPP to the charge pump block 100, “the charge pump circuit can obtain a wanted output voltage Vout **within a short time** by further including selective means capable of applying high voltage **rather than** the power voltage VCC.” EX1005, Zhang, 5:12-15, 2:9-19, 3:21-27; EX1003, ¶¶70-72.

Fig. 4



EX1005, Zhang, FIG. 4, annotated

2. Javanifard (EX1006)

Like the '701 patent, Javanifard is in the field of using charge pump circuits to provide a power supply voltage. EX1006, Javanifard, Title, 1:6-11; EX1003, ¶¶72-82. Specifically, it relates to “providing a charge pump having a **variable** number as opposed to a fixed number of stages **according to charge pump power supply input levels and desired charge pump output levels.**” EX1006,

Javanifard, 1:6-11. Javanifard's variable stage charge pump provides great design flexibility, which can both "accommodate different output levels for a given charge pump power supply input level," and "accommodate a given output level for different charge pump power supply input levels." EX1006, Javanifard, 2:19-24.

a. Embodiment 1

Specifically, as shown in FIG. 1 below, Javanifard's variable stage charge pump achieves these objects by providing different configurations, where **"the number of stages and the coupling of the charge pump stages** to each other may be varied." EX1006, Javanifard, 3:19-21; EX1003, ¶¶74-78. The variable stage charge pump may be identified as an "X/Y" stage pump, where "X" refers to the number of rungs that may be coupled in series, and "Y" indicates the number of stages for each fixed stage charge pump. FIG. 1 of Embodiment 1 illustrates a "2/2" stage pump, including two rungs, each rung including a two-stage charge pump.

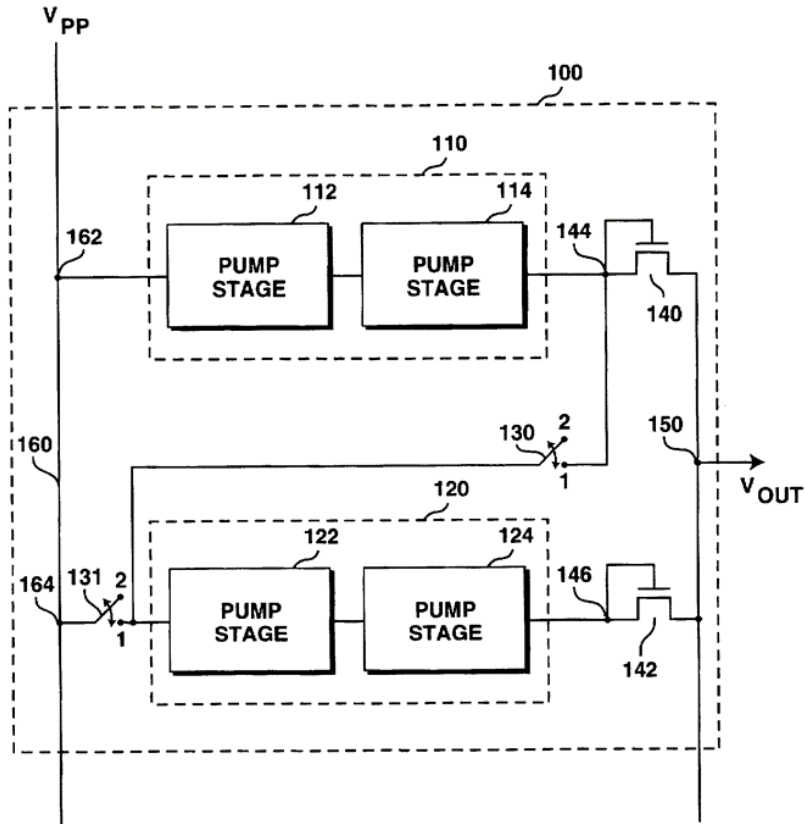


Figure 1

EX1006, Javanifard, FIG. 1

As shown in Table 1 of Javanifard below, there are three applicable configurations (corresponding to the first, second, and third rows of Table 1) out of four configurations, “[b]y choosing a different one of the four position combinations [of switches 130 and 131], the number of stages and the coupling of the charge pump stages to each other can be varied.” EX1006, Javanifard, 3:19-21. The fourth configuration (the fourth row) is included for completeness but is not to be used. EX1006, Javanifard, 3:66-4:5, 3:39-42, 3:50-53.

TABLE 1

Switch 130	Switch 131	Charge Pump 110	Charge Pump 120
OFF	OFF	ON	OFF
OFF	ON	ON	parallel-coupled to charge pump 110
ON	OFF	ON	series-coupled to charge pump 110
ON	ON	N/A	N/A

EX1006, Javanifard, Table 1

b. Embodiment 2

Embodiment 2 is described with reference to FIG. 2 (reproduced below) and Tables 2 and 3, and describes a multi-power-source charge pump system that selects from multiple power sources (e.g., VCC and VPP), and provides the selected power supply source to a variable stage charge pump. EX1006, Javanifard, 6:61-64; EX1003, ¶¶79-81.

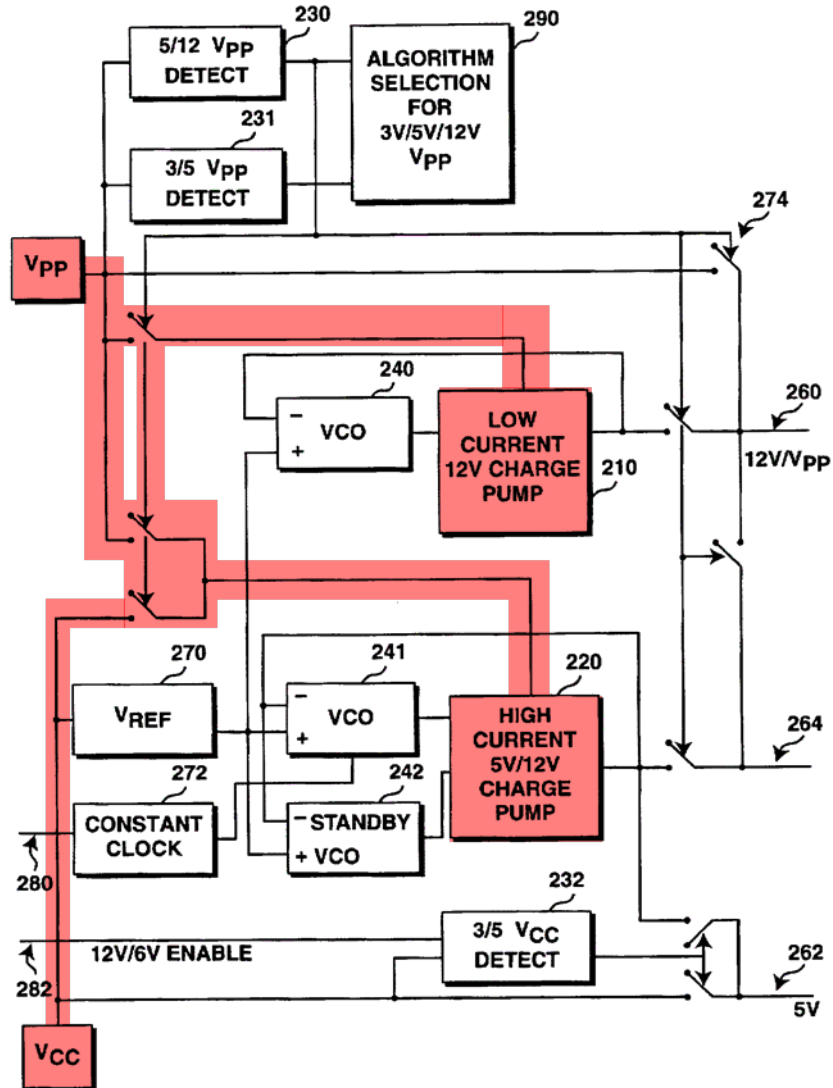


Figure 2

EX1006, Javanifard, FIG. 2, annotated

As shown in annotated FIG. 2 above, FIG. 2 “illustrates the power supply circuitry for a flash memory including variable stage charge pumps for accommodating a 5 volt, 9 volt, and 12 volt voltage level from either a 3.3 volt or 5 volt power supply,” using variable stage charge pumps 210 and 220. EX1006,

Javanifard, 6:61-64. Two different power supplies, VCC and VPP, to two input nodes respectively. Switches are used to select from the different power supplies VCC and VPP, and the selected input node is coupled to the variable stage charge pumps 210 and 220, which are configured based on the input power supply voltage (VCC or VPP) to provide required output voltage levels (e.g., at the output nodes 262 or 264). EX1006, Javanifard, 6:44-52 (describing that “power for the flash memory device is provided **by two sources**. These sources include a V_{CC} line and a V_{PP} line. The V_{CC} line is the primary power source for the flash device. The supplemental voltage provided by supply line, V_{PP}, is typically needed only when writing or erasing the memory because of the higher voltages needed during those operations.”).

A POSITA would have understood that FIG. 2 is an example of Embodiment 2, and that Embodiment 2 is not limited by FIG. 2.

c. Embodiment 3

Embodiment 3 is described with reference to FIG. 3 illustrating “a variable stage charge pump coupled to a flash memory array.” EX1006, Javanifard, 2:37-38; EX1003, ¶82. Similar to the variable stage charge pump of Embodiment 1, Javanifard describes that a variable stage charge pump “might be constructed with n rungs of charge pumps, each charge pump having y stages.” EX1006,

Javanifard, 4:49-51. FIG. 3 of Embodiment 3 illustrates a “12/2” stage pump, including twelve rungs, each rung including a two-stage charge pump.

3. Kang (EX1007)

Specifically, Kang is titled “Charge Pump Circuits with Low Area and High Power Efficiency for Memory Applications,” and describes charge pump circuits that use “the thin-oxide MOSFETs as the pumping capacitors” (also referred to as thin-oxide capacitors) to “reduce the area of charge pumps greatly while keeping their driving capability.” EX1020, Kang, Title, Abstract; EX1003, ¶¶83-85.

Referring to FIGS. 1(a) and 1(b) of Kang below, Kang illustrates a conventional charge pump using capacitors made with thick-oxide transistors (FIG. 1(a)) and proposes a low-area pump circuit where “C1, C2, and C3 as shown in Fig. 1(b) can be made with the **thin-oxide transistors**.” EX1020, Kang, 258.

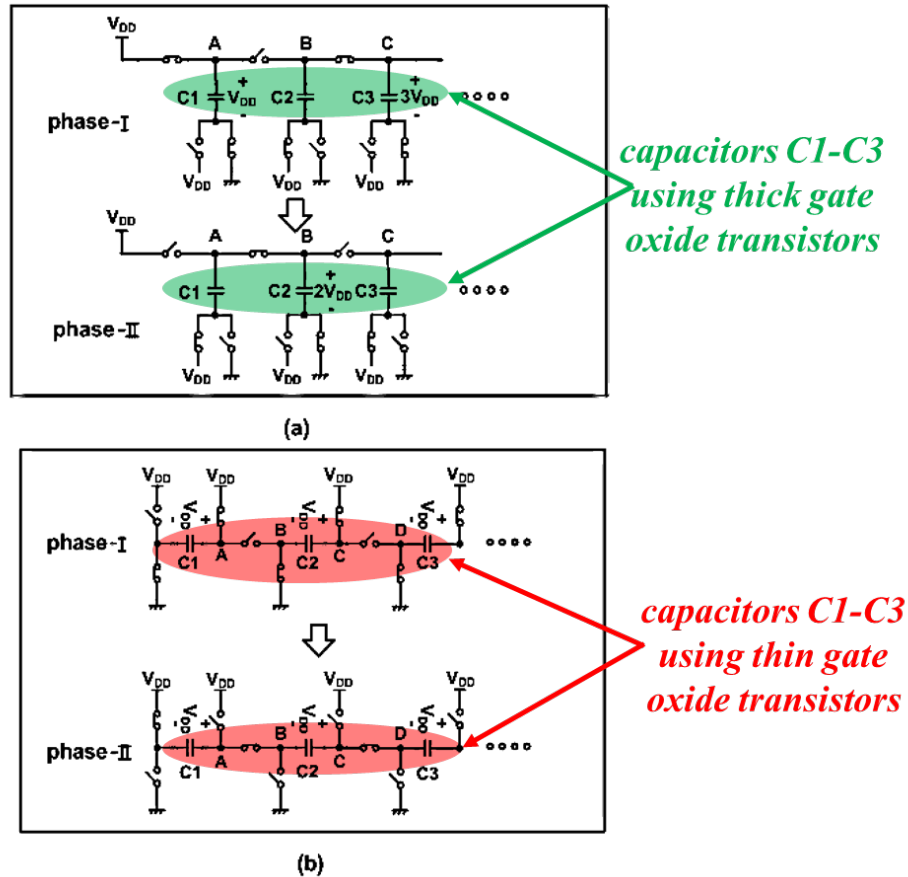


Fig. 1. (a) A conceptual diagram of the conventional charge pump (b) A conceptual diagram of new charge pump.

EX1020, Kang, FIG. 1, annotated

Kang provides that by using capacitors formed using thin oxide transistors, in the charge pump of FIG. 1(b), “the layout area of C1, C2, and C3 becomes **smaller** compared with that of thick oxide transistors,” thereby “reducing the total pump area.” EX1020, Kang, 258. Kang also provides additional charge pump designs (e.g., 3-stage pumps of FIGS. 2(c) and 2(d)) where in each pump stage, the pumping capacitor is a thin-oxide capacitor.

4. Analogous Art

Zhang, Javanifard, and Kang are analogous art to the '701 patent, because each is at least (1) in the same field of endeavor (charge pump system); or (2) reasonably pertinent to a problem with which the inventor of the '701 patent was involved (e.g., supporting multiple power supply sources and reducing chip area). EX1003, ¶86. *Compare* EX1001, Title (“Supply Voltage Generating Circuit”), Abstract (“A supply voltage generating circuit that enables a reduction in chip area includes: a booster for outputting a boosted voltage upon generating the boosted voltage by charge pumping of a capacitor element”); EX1005, Zhang, 1:10-13 (“The present invention relates to...charge pump circuits operating responsive to a mode that enables selection of a power voltage or an external high voltage.”); EX1006, Javanifard, 1:8-12 (“this invention relates to providing a charge pump having a variable number as opposed to a fixed number of stages according to charge pump power supply input levels and desired charge pump output levels.”); EX1020, Kang, Title (“Charge Pump Circuits with Low Area and High Power Efficiency for Memory Applications”), Abstract (describing charge pump designs to “reduce the area of charge pumps greatly while keeping their driving capability.”).

B. Ground 1: Claims 1-18 are Rendered Obvious under § 103 over Zhang in view of Javanifard

Zhang in view of Javanifard renders claims 1-18 of the '701 patent obvious. EX1003, ¶¶87-202.

While the analysis below mainly focuses on the example of FIG. 1 and Table 1 of Javanifard providing a “X=2/Y=2 stage pump,” it would have been obvious to a POSITA to use various suitable X, Y, and pump stage designs based on the design needs (e.g., to provide a required output voltage according to the different power supply input levels). EX1003, ¶88.

Further, the analysis below relies on pump stages (e.g., pump stages 112, 114, 122, and 124 of Javanifard) to disclose the claimed “*booster stages*,” as would have been understood by a POSITA. *See, e.g.*, EX1017, Fukui, 2:13-45 (referring to stages in a charge pump as “boosting stage” and “pump stage” interchangeably). To the extent that Patent Owner asserts that each claimed “*booster stage*” requires a charge pump circuit, Javanifard’s charge pump circuits (e.g., charge pump circuits 110 and 120) disclose such asserted “*booster stages*” and the associated configuration changes (e.g., by using switch 130) for the same reasons. EX1003, ¶89.

1. Reasons to Combine Zhang and Javanifard

A POSITA would have been motivated to apply Javanifard’s teaching of a variable stage charge pump in Zhang’s multi-power-source charge pump system to

produce the obvious, beneficial, and predictable results of a variable stage charge pump system, which can both “accommodate different output levels for a given charge pump power supply input level,” “accommodate a given output level for different charge pump power supply input levels,” and provide flexibility for design needs (e.g., power saving mode, and current requirements), area reduction, and performance improvement, as taught by Javanifard. EX1003, ¶¶90-96.

First, as discussed at IX.A.4, Zhang and Javanifard are analogous art to the ’701 patent. *see also* EX1007, ’667 app, 213 (another patent in the Javanifard family, US 5,781,473 (“Javanifard 473”), was listed on the face of Zhang and cited by examiner as anticipating claims of Zhang).

Second, Javanifard explicitly provides motivations to apply its teaching of the variable stage charge pump to replace the fixed stage charge pump in Zhang’s charge pump system. Javanifard addresses various disadvantages (e.g., area usage, performance including pump efficiency, lack of flexibility) of using the fixed stage charge pump, including, e.g., “us[ing] a number of charge pump circuits each having a fixed number of stages ...each charge pump circuit requires a dedicated space in the integrated circuit,” “the fixed stage method typically sacrifices performance at one power supply voltage to accommodate another power supply voltage.” EX1006, Javanifard, 1:48-53,1:66-2:2.

Javanifard achieves area reduction by using a single variable stage charge pump circuit to provide different output levels, and improves performance (e.g., pump efficiency) by configuring the number of pump stages based on the power supply voltage and the desired output voltage level. Javanifard's variable stage charge pump can both "accommodate different output levels for a given charge pump power supply input level," "accommodate a given output level for different charge pump power supply input levels," and provide flexibility for various design needs (e.g., configurations based on power saving mode, and/or current requirements). EX1006, Javanifard, 2:18-24, 3:39-42, 3:50-53.

A POSITA facing the need to improve its charge pump system would have looked to Javanifard and been motivated to apply Javanifard's teachings of the variable stage charge pump in the multi-power-source charge pump system of Zhang using fixed stage charge pump, because Javanifard's teachings provide the obvious, beneficial, and predictable results of a power supply generation circuit that can both "accommodate different output levels for a given charge pump power supply input level," "accommodate a given output level for different charge pump power supply input levels," with improved flexibility for design needs (e.g., power saving mode, and current requirements), area reduction, and performance improvement, as taught by Javanifard.

Furthermore, while Zhang describes “a charge pump circuit that operates responsive to a test or general operation mode,” Zhang’s teachings including its selector circuit are not limited for only “a test or general operation mode.” *See*, EX1005, Zhang, 5:23-51 (claiming a charge pump circuit including a selector circuit without any operation mode requirement). As such, a POSIA would have been motivated to apply Javanifard’s teachings in Zhang to provide a multi-power-source charge pump to support a device having multiple operation modes, including a device having “a test or general operation mode” and devices having other operation modes (e.g., a memory device having different read, write, programming modes). *See, e.g.*, EX1006, Javanifard, FIG. 2 (illustrating variable stage charge pumps used for a multi-power-source memory device with different modes).

Finally, applying Javanifard’s teachings in embodiments of Zhang would have been no more than the combination of known elements according to known methods (e.g., incorporating a charge pump circuit design in a multi-power-source charge pump system according to the known IC design) obvious to a POSITA. For example, techniques for configuring the variable stage charge pump (e.g., using control circuitry to generate signals to control the switches in the variable stage charge pump based on selected power supply and desired output voltage) were well-known. Techniques for designing (e.g., using IC design and simulation tools)

and making an IC including various components like charge pumps were well-known.

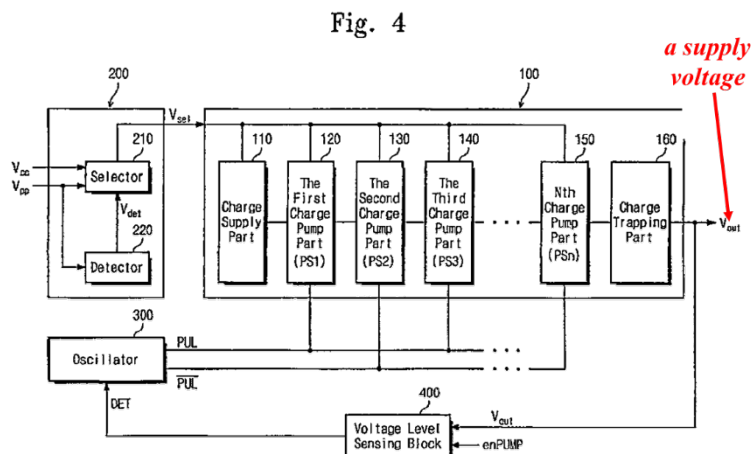
As such, the combination of Javanifard's variable stage charge pump with the multi-power-source charge pump system of Zhang is nothing more than the combination of known elements applying known methods, and would have been obvious to a POSITA.

2. Claim 1

[1.0] 1. A method for generating a supply voltage, comprising:

To the extent that the preamble is limiting, Zhang in view of Javanifard renders it obvious. EX1003, ¶¶97-101.

As shown in annotated FIG. 4 below, Zhang describes generating, using a charge pump circuit, an output voltage V_{out} (a supply voltage). EX1005, Zhang, 2:55-3:2, FIG. 8; EX1003, ¶98.



EX1005, Zhang, FIG. 2, annotated

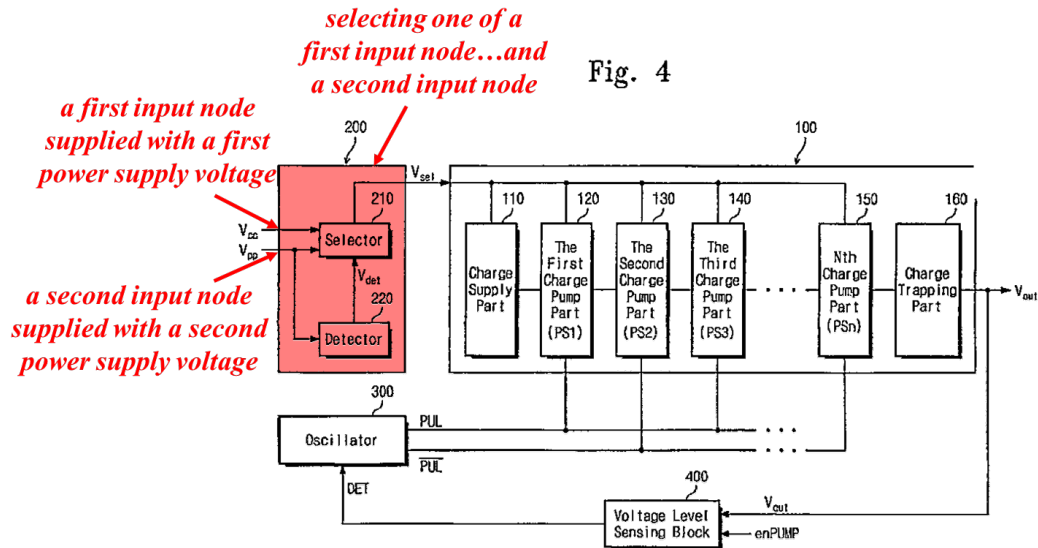
Similarly, Javanifard describes a variable stage charge pump providing a supply voltage in integrated circuits, e.g., to “provide the proper voltages for the memory circuitry.” EX1006, Javanifard, FIGS. 1, 2, 3, 2:18-24; 6:56-59.

Accordingly, in the combination of Zhang and Javanifard, a charge pump system generates an output voltage and supplies it as a supply voltage for a device, which renders obvious “[a] method for generating a supply voltage” as claimed.

[1.1] selecting one of a first input node supplied with a first power supply voltage and a second input node supplied with a second power supply voltage that is higher than the first power supply voltage;

Zhang teaches this element. EX1003, ¶¶102-106.

Specifically, as shown in annotated FIG. 4 of Zhang below, Zhang describes a selecting circuit block 200 that selects one of a first node supplied with VCC (a first power supply voltage) and a second node supplied with VPP (a second power supply voltage), where “the high voltage VPP is **higher than** the power voltage VCC.” EX1005, Zhang, 3:32-36; *see also* EX1005, Zhang, FIG. 8, 5:5-9 (illustrating that VPP (8V) is higher than VCC (1.8V)). It is noted that in the ‘701 patent specification, the first power supply voltage is an external power supply VDDP1, and the second power supply voltage is an internal power supply VDLP. EX1001, 5:5-19.



EX1005, Zhang, FIG. 4, annotated

Referring to FIG. 4, Zhang describes that the “charge supply part 110 provides a charge corresponding to **voltage Vsel provided, in turn, by the selecting circuit block 200.**” EX1005, Zhang, 2:62-64. Zhang provides that the “selecting circuit block 200 includes a selector 210 and a detector 220. In the specification power supply voltage VCC refers to the power voltage operating in general operation mode. The voltage VPP refers to a high voltage provided externally during a test operation mode. The high voltage VPP may be applied externally in the test operation mode as well as during the general operation mode.” EX1005, Zhang, 3:21-27.

Zhang describes that the “selector 210 selects between the power voltage VCC and the high voltage VPP. The detector 220 detects the level of the high voltage VPP to generate detection signal VDET. The detector 220 enables the

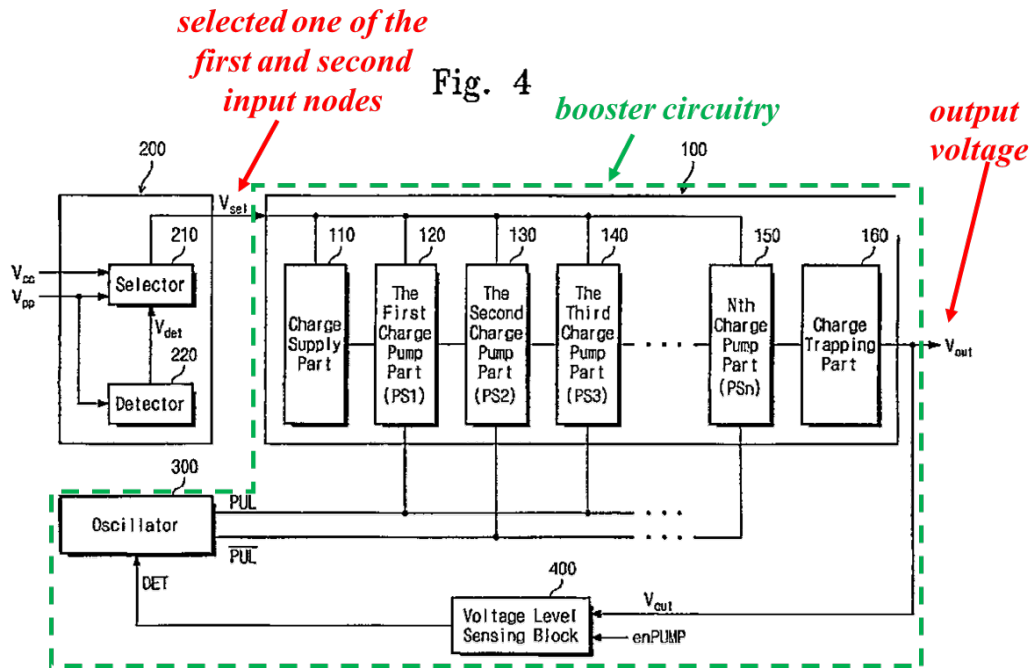
detection signal VDET when the high voltage VPP is higher than the power voltage VCC. The selector 210 switches between the power voltage VCC to the high voltage VPP responsive to the detection signal VDET. Put differently, the signal VSEL is VCC in the general operation mode and VPP in the test operation mode allowing for a high Voltage within a short time.” EX1005, Zhang, 3:29-40; *see also* EX1005, Zhang, FIGS. 6 and 7 (providing example selector 210 and detector 220 of FIG. 4).

Accordingly, Zhang discloses or renders obvious this element.

[1.2.1] coupling a selected one of the first and second input nodes to booster circuitry comprising a plurality of booster stages to provide an output voltage,

Zhang in view of Javanifard renders obvious this element. EX1003, ¶¶107-116. Zhang teaches claim element [1.2.1] by itself, and when combined with Javanifard, teaches claim elements [1.2.2] *et al.* which further describe and limit the claimed booster circuitry.

First, Zhang teaches claim element [1.2.1]. As shown in annotated FIG. 4 below, Zhang describes coupling Vsel (a selected one of the first and second input nodes) to a booster circuitry (including charge pump block 100) to provide Vout (an output voltage), which is a boosted voltage (e.g., 10V) that is higher than Vsel (e.g., one of VCC =1.8V and VPP = 8V). The charge pump block 100 of the booster circuitry includes a plurality of booster stages (First Charge Pump Part PS1, Second Charge Pump Part PS2, ... Nth Charge Pump Part PSn).

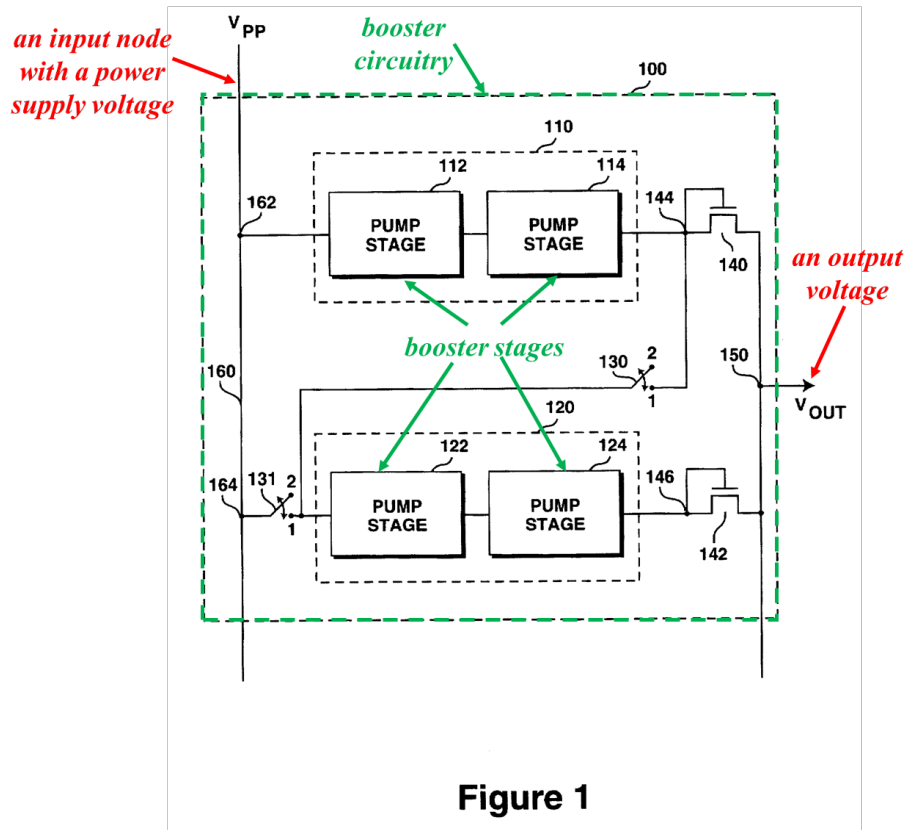


EX1005, Zhang, FIG. 4, annotated

Second, Javanifard describes coupling an input node with a power supply voltage to a booster circuitry comprising a plurality of booster stages to provide an output voltage. Javanifard also teaches a variable number of booster stages, which will be discussed later with reference to claim elements [1.2.2] and [1.2.3].

For example, referring to annotated FIG. 1 of Javanifard below, Javanifard describes that “[a] power supply voltage, V_{pp} , provides the supply voltage to common input bus 160,” which is coupled to a variable stage charge pump 100 (booster circuitry) providing an output voltage V_{out} . EX1006, Javanifard, 2:52-53. The variable stage charge pump 100 (booster circuitry) includes a plurality of pump stages 112, 114, 122, 124 (booster stages). It was well-known in the art that pump stages are also referred to as booster stages or boosting stages. *See, e.g.,*

EX1017, Fukui, 2:13-45 (referring to stages in a charge pump as “boosting stage” and “pump stage” interchangeably).



EX1006, Javanifard, FIG. 1, annotated

Similarly, as shown in FIG. 3 of Javanifard below, Javanifard describes coupling an input node with a power supply voltage to a booster circuitry comprising a plurality of booster stages to provide an output voltage, where the variable stage charge pump of the booster circuitry includes 12 rungs and is coupled to a flash memory array 390, “[e]ach rung includes a charge pump having 2 stages.” EX1006, Javanifard, 5:3-6.

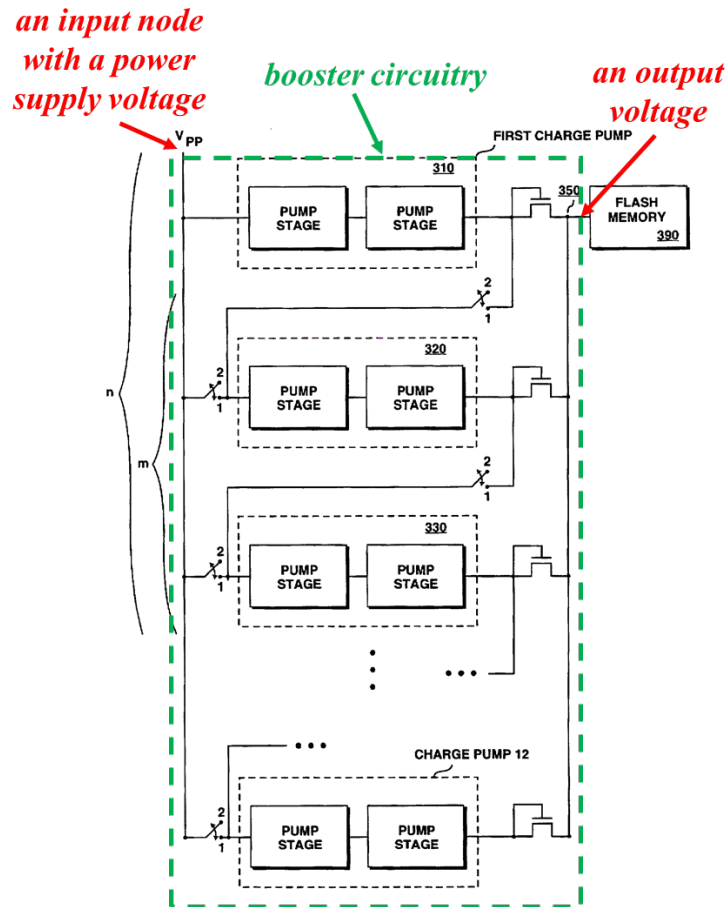
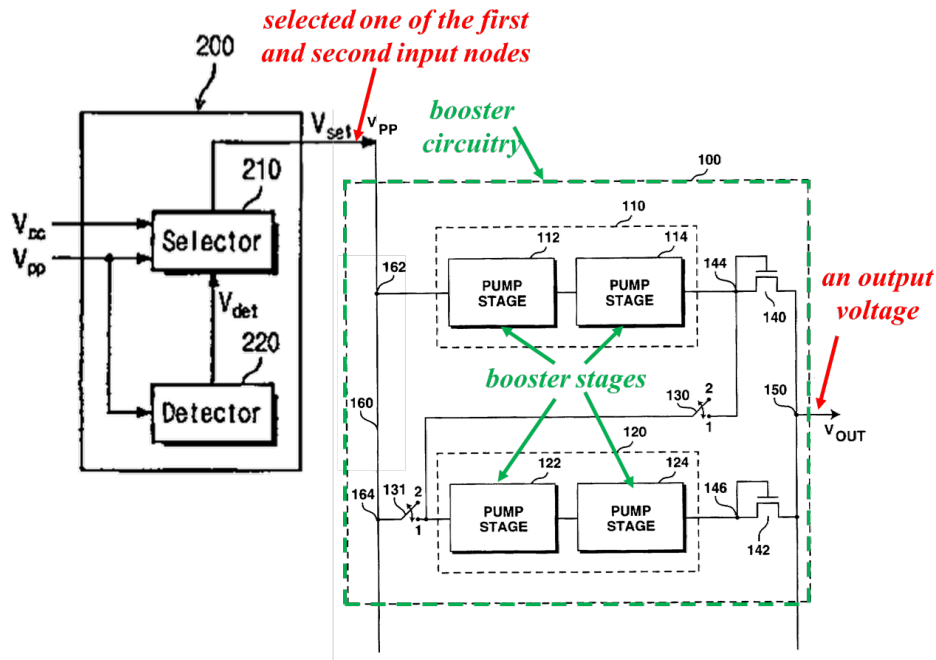


Figure 3

EX1006, Javanifard, FIG. 3, annotated

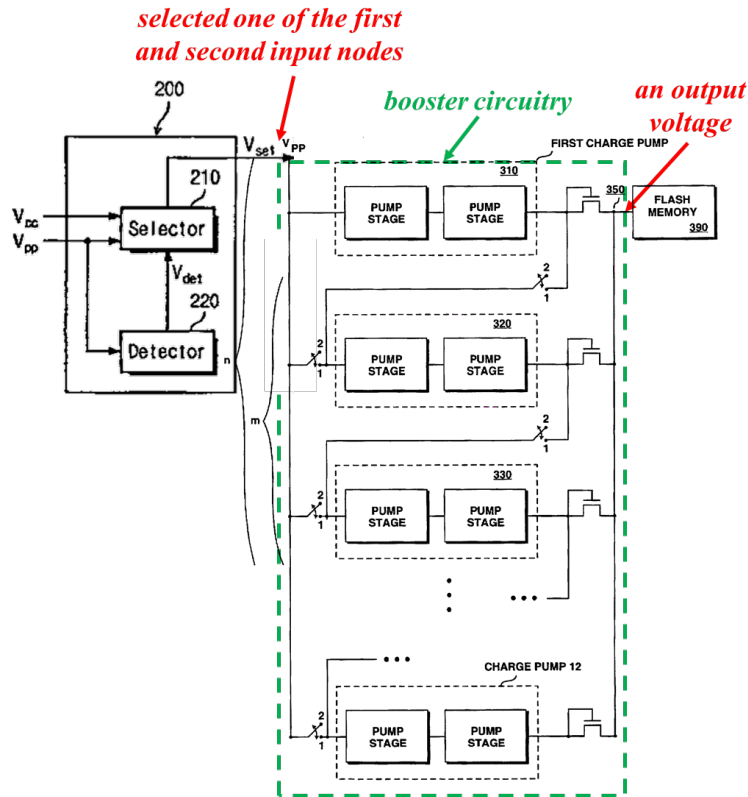
Third, a POSITA would have been motivated to apply Javanifard's teachings of a variable stage charge pump in Zhang's system, for the benefit of providing a charge pump that can both "accommodate different output levels for a given charge pump power supply input level," (EX1006, Javanifard, 2:18-20) and "accommodate a given output level for different charge pump power supply input levels." EX1006, Javanifard, 2:21-24.

An example (Example A) of the combination of Zhang and Javanifard is illustrated below, which is a composite figure of selecting circuit block 200 of FIG. 4 of Zhang and variable stage charge pump 100 of FIG. 1 of Javanifard.



Example A of Combination of Zhang and Javanifard

Another example (Example B) of the combination of Zhang and Javanifard is illustrated below, which is a composite figure of selecting circuit block 200 of FIG. 4 of Zhang and variable stage charge pump of FIG. 3 of Javanifard.



Example B of Combination of Zhang and Javanifard

As shown in Examples A and B, in the combination of Zhang and Javanifard, a selected one of the first and second input nodes (the selected input node of the corresponding supply voltage VCC or VPP) of Zhang is coupled to a variable stage charge pump comprising a plurality of booster stages as taught by Javanifard, to provide an output voltage, to achieve the benefits of a power supply circuit that can both “accommodate different output levels for a given charge pump power supply input level,” (EX1006, Javanifard, 2:18-20) and “accommodate a given output level for different charge pump power supply input levels.” EX1006, Javanifard, 2:21-24.

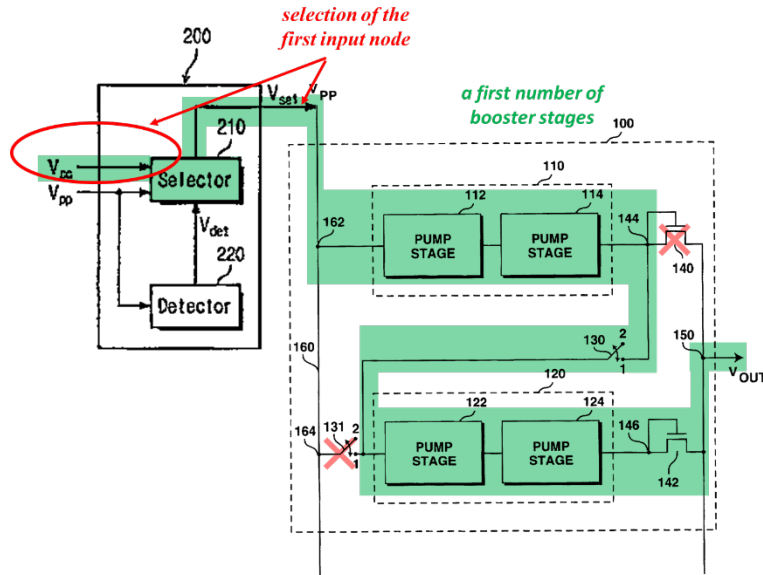
Accordingly, Zhang in view of Javanifard renders obvious this element.

[1.2.2] wherein selection of the first input node corresponds to a first number of booster stages and

Zhang in view of Javanifard renders obvious this element. EX1003, ¶¶117-124.

First, as discussed at [1.2.1], it would have been obvious to combine Zhang's teaching of a selecting circuit block and Javanifard's teaching of a variable stage charge pump, such that a selected one of the first node and second input node is coupled to a booster circuitry comprising a plurality of booster stages to provide an output voltage.

Second, as shown in the annotated figure for Example A of Zhang combined with Javanifard below, it would have been obvious that in the combination of Zhang and Javanifard, selection of the first input node (with a lower input power supply voltage level) corresponds to a first number (a higher number e.g., 4) of booster stages, e.g., for generating the same output voltage as the selection of the second input node with a higher input power voltage level.



Example A of Zhang Combined with Javanifard

(Selection of the First Input Node with Lower Supply Voltage)

Javanifard describes providing a variable stage charge pump to “accommodate a **given** output level for **different** charge pump power supply input levels.” EX1006, Javanifard, 2:22-24; *see also* EX1005, Zhang, FIG. 8 (providing the same output voltage level for different power supply input levels). Specifically, to “accommodate a **given** output level” (EX1006, Javanifard, 2:22-24) for the first input node with a lower power supply voltage, a POSITA would have configured the variable stage charge pump of FIG. 1 of Javanifard according to row 3 of Table 1 below, because row 3 of Table 1 provides a first (higher) number of serially connected booster stages to provide a higher voltage boost (e.g., by serially connecting charge pumps 110 and 120), compared to row 1 of Table 1 (by providing only charge pump 110 in operation and thereby having a lower

number of serially connected booster stages). Connecting more stages in series provide a higher voltage boost compared to using a smaller number of stages in series, as each stage in the charge pump contributes to increasing the voltage level, and the total voltage boost is the cumulative effect of all the stages. *See, e.g.*, EX1008, Pan, 93, ll.5-6.

TABLE 1

Switch 130	Switch 131	Charge Pump 110	Charge Pump 120	
OFF	OFF	ON	OFF	<i>a second number of booster stages, the second number being less than first number</i>
OFF	ON	ON	parallel-coupled to charge pump 110	
ON	OFF	ON	series-coupled to charge pump 110	<i>a first number of booster stages</i>
ON	ON	N/A	N/A	

EX1006, Javanifard, Table 1, annotated

Corresponding to row 3 of Table 1, Javanifard explains that “[i]f switch 130 is on and switch 131 is off, charge pump 120 will be coupled so that charge pumps 110 and 120 are series-coupled. In other words, the input voltage for charge pump 120 will be provided from the output of charge pump 110. Because both 110 and 120 are two stage charge pumps, this means that charge pump 100 will **effectively be a four stage charge pump with all four stages serially coupled.**” EX1006, Javanifard, 3:54-60; compare with row 1 of Table 1 (“this configuration of switches 130 and 131 will effectively result **in a two stage charge pump,**” and

this configuration “might be used in a power saving mode” compared with row 2 of Table 1). EX1006, Javanifard, 3:35-42.

Javanifard describes that “[i]n this configuration [of row 3 of Table 1], charge pump 100 will provide approximately twice the output voltage at node 150 as the previous two cases [including row 1 of Table 1].” EX1006, Javanifard, 3:60-63. A POSITA would have understood that this statement of “approximately twice the output voltage at node 150” applies when the input voltage levels are the same, and in a design to accommodate “a **given** output level for **different** charge pump power supply input levels,” the configuration of row 3 with more serially-connected stages provides more voltage boost for a lower power supply input level.

Similar analysis applies to Example B of the combination of Zhang and Javanifard. While the example of FIG. 1 and Table 1 of Javanifard provides a “X=2/Y=2 stage pump,” in the combination of Zhang and Javanifard, it would have been obvious to a POSITA to use various suitable X, Y, and pump stage designs to provide the required output voltage according to the different power supply input levels.

Accordingly, Zhang in view of Javanifard renders obvious this element.

[1.2.3] selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number; and

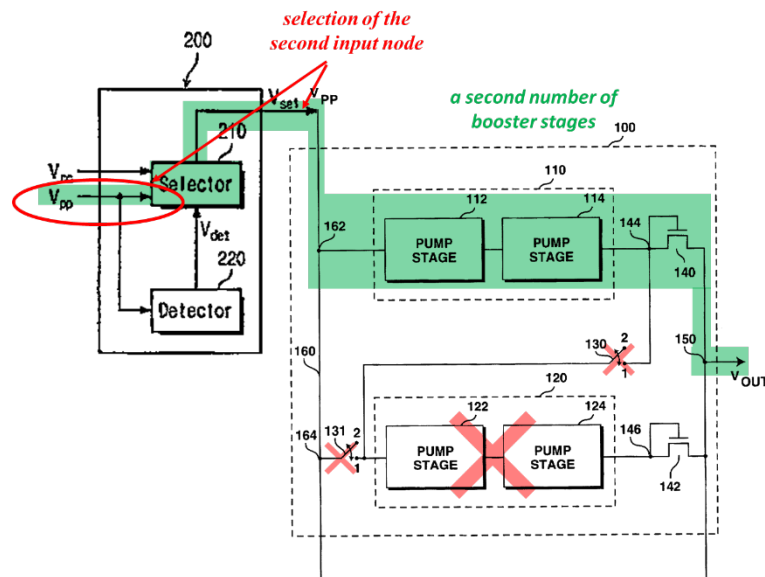
Zhang in view of Javanifard renders obvious this element. EX1003, ¶¶125-131.

First, as discussed at [1.2.1] and [1.2.2], it would have been obvious that in the combination of Zhang and Javanifard, selection of the first input node (with a lower input power supply voltage level) corresponds to a first number (a higher number, e.g., 4) of booster stages, e.g., for generating the same output voltage as the selection of the second input node with a higher input power voltage level.

Second, for the similar reasons as discussed at [1.2.2], as shown in the annotated figure for Example A of Zhang combined with Javanifard below, it would have been obvious that in the combination of Zhang and Javanifard, selection of the second input node (with a higher input power supply voltage level) corresponds to a second number (a lower number, e.g., 2) of booster stages, e.g., for generating the same output voltage as the selection of the first input node with a lower input power voltage level.

Javanifard describes providing a variable stage charge pump to “accommodate a **given output level** for **different** charge pump power supply input levels.” EX1006, Javanifard, 2:22-24; *see also* EX1005, Zhang, FIG. 8 (providing the same output voltage level for different power supply input levels). Specifically, to “accommodate a **given output level**” (EX1006, Javanifard, 2:22-24) for the second input node with a higher power supply voltage, a POSITA would have configured the variable stage charge pump of FIG. 1 of Javanifard according to row 1 of Table 1 below, because row 1 of Table 1 provides a second

(lower) number of serially connected booster stages to provide a lower voltage boost (by providing only charge pump 110 in operation and thereby having a lower number of serially connected booster stages). Connecting less stages in series provide a lower voltage boost compared to using a higher number of stages in series, as each stage in the charge pump contributes to increasing the voltage level, and the total voltage boost is the cumulative effect of all the stages.



Example A of Zhang Combined with Javanifard

(Selection of Second Input Node with Higher Supply Voltage)

TABLE 1

Switch 130	Switch 131	Charge Pump 110	Charge Pump 120	
OFF	OFF	ON	OFF	<i>a second number of booster stages, the second number being less than first number</i>
OFF	ON	ON	parallel-coupled to charge pump 110	
ON	OFF	ON	series-coupled to charge pump 110	<i>a first number of booster stages</i>
ON	ON	N/A	N/A	

EX1006, Javanifard, Table 1, annotated

Additionally, while configurations of rows 1 and 2 of Table 1 may provide substantially the same voltage boost, a POSITA would have used row 1 based on a design need for power saving mode. EX1006, Javanifard, 3:39-42 (“This configuration [of row 1] might be used in a power saving mode if charge pump 100 is otherwise providing sufficient current and voltage output levels.”).

Similar analysis applies to Example B of the combination of Zhang and Javanifard. While the example of FIG. 1 and Table 1 of Javanifard provides a “X=2/Y=2 stage pump,” in the combination of Zhang and Javanifard, it would have been obvious to a POSITA to use various suitable X, Y, and pump stage designs to provide the required output voltage according to the different power supply input levels.

Accordingly, Zhang in view of Javanifard renders obvious this element.

[1.3] changing the booster circuitry from the first number of booster stages corresponding to selection of the first input node to the second number of booster stages when the second input node is selected.

Zhang in view of Javanifard renders obvious this element. EX1003, ¶¶132-137.

First, as discussed at Ground 1: [1.2.2] and [1.2.3], in the combination of Zhang and Javanifard, selection of the first input node corresponds to a first number of booster stages, and selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number, e.g., to provide the same output voltage for different power supply voltage levels.

Second, Javanifard describes changing the booster circuitry from a higher number (e.g., 4) of booster stages corresponding to a lower power supply voltage to a lower number (e.g., 2) of booster stages when the power supply voltage is higher. EX1006, Javanifard, 1:8-12 (“providing a charge pump having a variable number as opposed to a fixed number of stages **according to charge pump power supply input levels** and desired charge pump output levels”); EX1006, Javanifard, 5:65-66 (“The control for the switches would be a function of the available power supply voltage, VPP, and the desired variable stage charge pump output voltage.”). Specifically, as shown in Table 1 below, the number of the booster stages of the booster circuitry is changed (e.g., reduced from 4 to 2) by changing switch 130

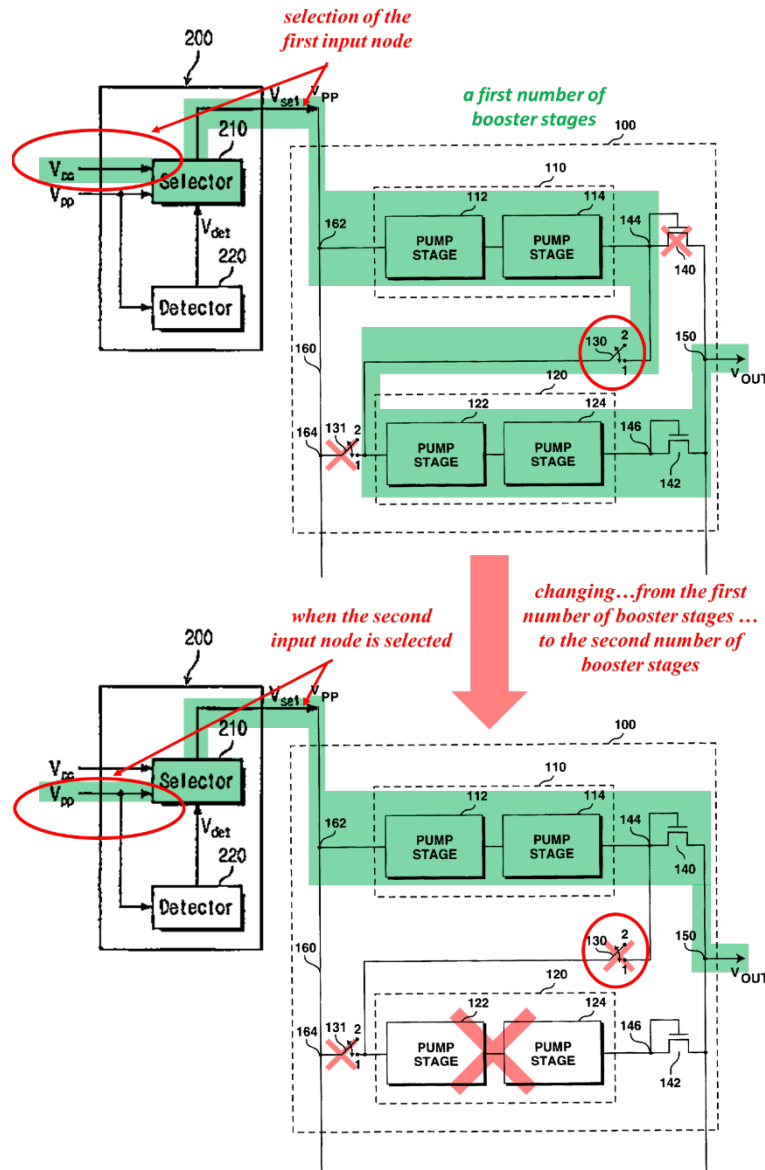
from on (row 3) to off (row 1) to provide the same output voltage level, when the charge pump power supply input level increases.

TABLE 1

Switch 130	Switch 131	Charge Pump 110	Charge Pump 120	
OFF	OFF	ON	OFF	<i>a second number of booster stages, the second number being less than first number</i>
OFF	ON	ON	parallel-coupled to charge pump 110	
ON	OFF	ON	series-coupled to charge pump 110	<i>a first number of booster stages</i>
ON	ON	N/A	N/A	

EX1006, Javanifard, Table 1, annotated

As shown in the figure of Example A of Zhang combined with Javanifard below, in the combination of Zhang and Javanifard, when the selection of the input node is changed to the higher power supply voltage, the booster circuitry is changed from the first number of booster stages (e.g., 4) to the second number of booster stages (e.g., 2), by turning off switch 130.



Example A of Zhang Combined with Javanifard (Changing Booster Circuitry with Switch 130)

Similar analysis applies to Example B of the combination of Zhang and Javanifard. While the example of FIG. 1 and Table 1 of Javanifard provides a “X=2/Y=2 stage pump,” in the combination of Zhang and Javanifard, it would have been obvious to a POSITA to use various suitable X, Y, and pump stage

designs to provide the required output voltage according to the different power supply input levels.

Accordingly, Zhang in view of Javanifard renders obvious this element.

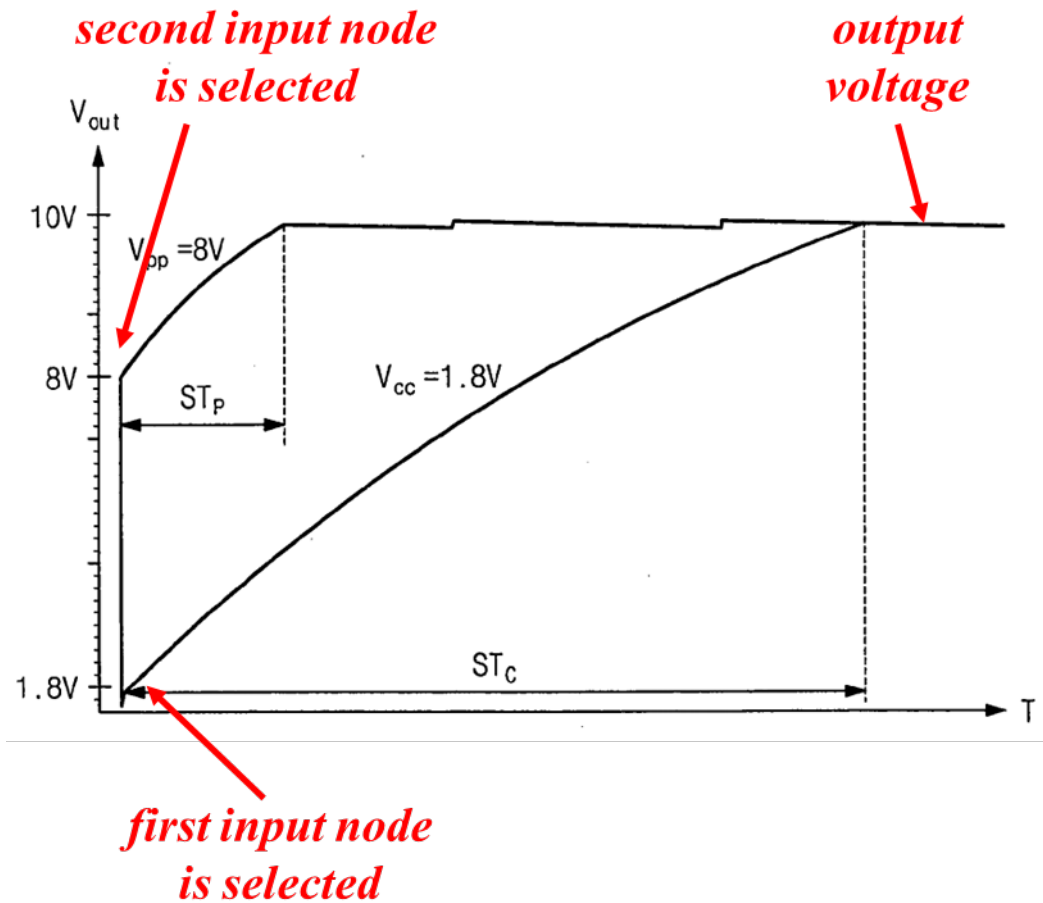
3. Claim 2

[2.0] The method as claimed in claim 1, wherein the output voltage is the same when the first input node is selected and when the second input node is selected.

Zhang in view of Javanifard renders obvious this element. EX1003, ¶¶138-142.

First, as shown in FIG. 8 below, Zhang describes that the output voltage (e.g., $V_{out} = 10V$) is the same when the first input node (e.g., $V_{CC} = 1.8V$) is selected and when the second input node (e.g., $V_{PP} = 8V$) is selected.

Fig. 8



EX1005, Zhang, FIG. 8, annotated

Second, Javanifard teaches this element as well. Javanifard describes using its variable charge pump to “accommodate a given output level for different charge pump power supply input levels.” EX1006, Javanifard, 2:21-24; EX1006, Javanifard, 1:8-12 (“providing a charge pump having a variable number as opposed to a fixed number of stages according to charge pump power supply input levels and desired charge pump output levels”); EX1006, Javanifard, 5:59-65

(“the designer can provide a control to the switches that will switch stages in and out, or change the coupling of the stages to **ensure the appropriate output voltage** from the variable stage charge pump **regardless** of the input voltage.”).

As such, in the combination of Zhang and Javanifard, a given output level is provided for different charge pump power supply input levels, e.g., by changing the configuration of the variable stage charge pump based on the required output level and the different charge pump power supply levels. Specifically, the output voltage is the same when the first input node is selected (e.g., with a lower input power supply voltage corresponding to a higher number of pump stages) and when the second input node is selected (e.g., with a higher input power supply voltage corresponding to a lower number of power stages).

Accordingly, Zhang in view of Javanifard renders obvious this element.

4. Claim 3

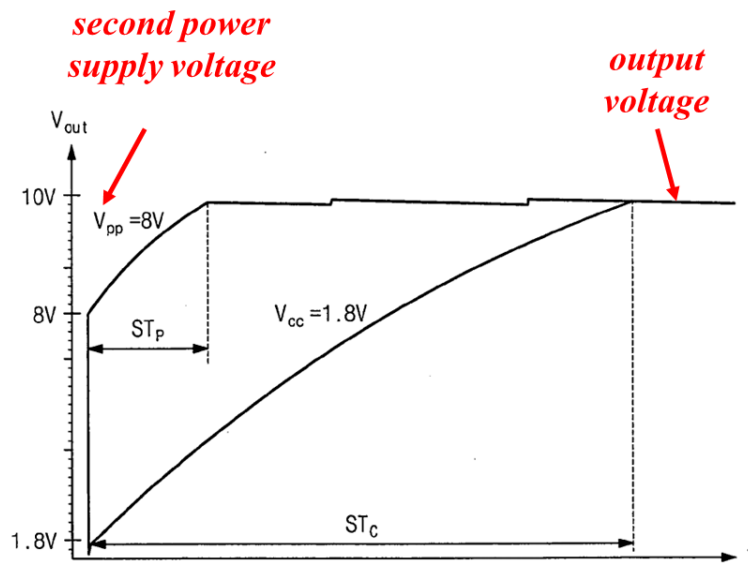
[3.0] 3. The method as claimed in claim 1, wherein the output voltage is higher than the second power supply voltage.

Zhang in view of Javanifard renders obvious this element. EX1003, ¶¶143-146.

Each of Zhang and Javanifard teaches this element, because each describes that the output voltage is greater than each of its voltage power supplies, including both the first and second power supply voltages. *See, e.g.*, EX1006, Javanifard, 1:20-30 (“Many operations, however, require voltages **greater than** that provided

by the lower voltage power supplies. ... Charge pump technology permits the generation of voltages having a magnitude greater than that of the power supply.”); EX1005, Zhang, annotated FIG. 8 below (illustrating that the charge pump circuit generates an output voltage (e.g., $V_{out} = 10V$) that is higher than the second power supply voltage V_{PP} (e.g., $V_{PP} = 8V$); EX1008, Pan, 43 (“Charge pumps are circuits that generate a voltage level higher than the chip supply voltage from which they operate.”).

Fig. 8



EX1005, Zhang, FIG. 8, annotated

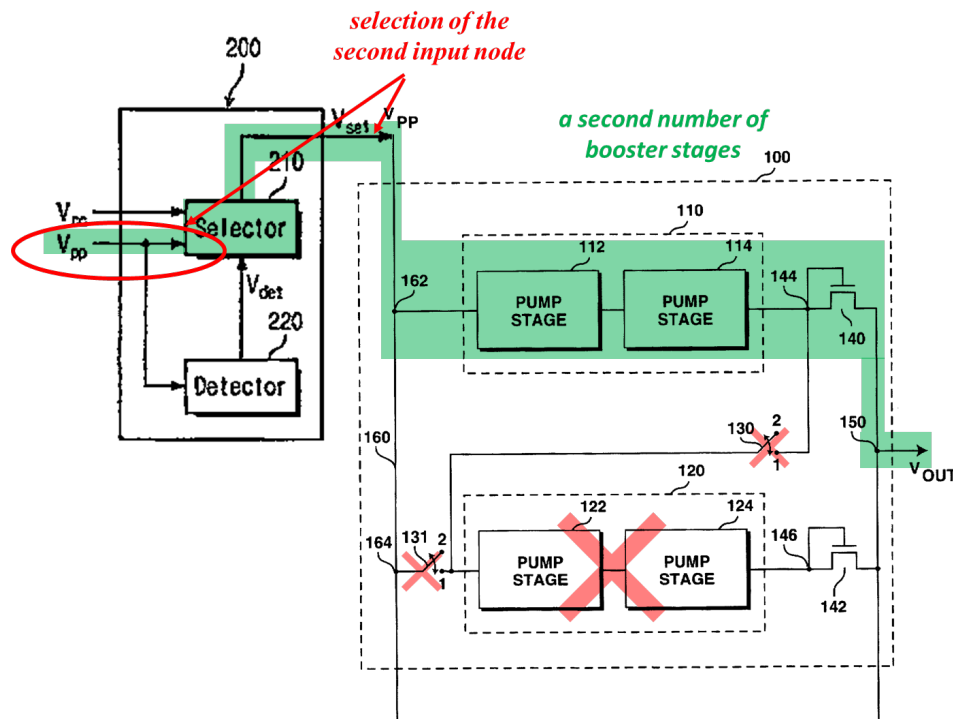
Accordingly, in the combination of Zhang and Javanifard, the charge pump system provides an output voltage higher than the input power supply voltage (including the second power supply voltage), which renders obvious “*wherein the output voltage is higher than the second power supply voltage*” as claimed.

5. Claim 4

[4.0] 4. The method as claimed in claim 1, wherein the second number of booster stages is one.

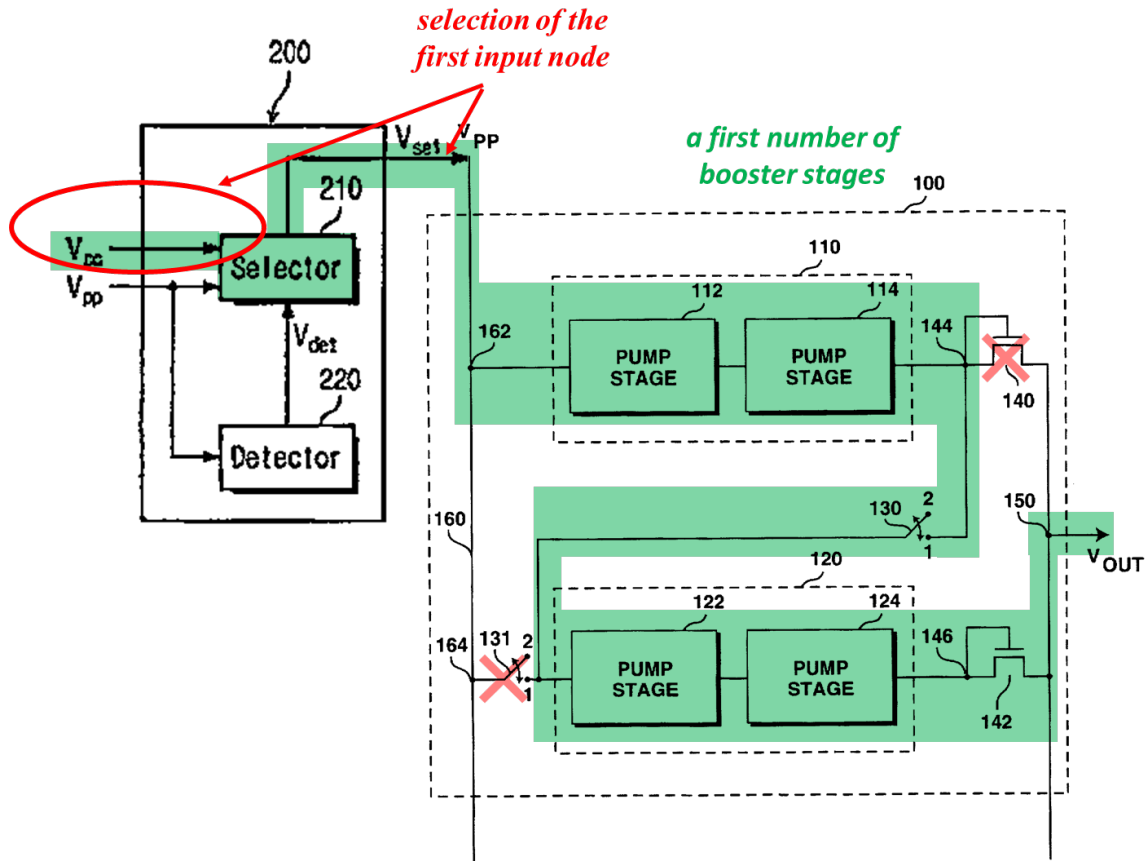
Zhang in view of Javanifard renders obvious the elements. EX1003, ¶¶147-151.

First, as discussed above at Ground 1: [1.2.2] and [1.2.3] and as shown in the figures of Example A below, in the combination of Zhang and Javanifard, selection of the second input node corresponds to selection of a second/lower number of booster stages, and selection of the first input node corresponds to selection of a first/higher number of booster stages.



Example A of Zhang Combined with Javanifard

(Selection of Second Input Node with Higher Supply Voltage)



Example A of Zhang Combined with Javanifard

(Selection of First Input Node with Lower Power Supply Voltage)

Second, Javanifard renders obvious that each of fixed stage charge pumps (e.g., 110 and 120) in the variable stage charge pump are implemented using a single pump stage.

Specifically, Javanifard describes that the variable stage charge pump may be configured as an “X/Y stage pump,” where “the ‘X’ refers to the number of rungs (and therefore the maximum number of fixed stage charge pumps) that may be coupled in series. The ‘Y’ indicates the number of stages for each fixed stage

charge pump.”). EX1006, Javanifard, 2:59-64. It would have been obvious to a POSITA to implement Y with any suitable numbers including one (1) based on the design needs. Various suitable pump stages (e.g., voltage doubler or other designs of pump stages) to be used to implement the pump stage in a single-stage charge pump were well-known. *See, e.g.*, EX1008, Pan, FIG. 3-2, 43-44; EX1015, Al-Shamma, FIGS. 1, 2, 4:61-5:59; EX1016, Daga, FIGS. 2A-2B and 4.

As such, in combination of Zhang and Javanifard, it would have been obvious to implement each of fixed stage charge pumps 110 and 120 with a single pump stage. In such implementation, when the second input node with the **higher** power supply voltage is selected, the booster circuitry 100 (including the selected charge pump 110) has one (1) booster stage. Accordingly, Zhang in view of Javanifard renders obvious that “*the second number of booster stages is one*” as claimed in claim 4.

6. Claim 5

[5.0] 5. The method as claimed in claim 4, wherein the first number of booster stages is two.

Zhang in view of Javanifard renders obvious the elements. EX1003, ¶¶152-156.

As discussed at Ground 1:[4.0], it would have been obvious to implement each of fixed stage charge pumps 110 and 120 of the variable stage charge pump as taught by Javanifard with a single pump stage.

In such implementation, when the first input node with the **lower** power supply voltage is selected, the booster circuitry 100 has two (2) booster stages from serially connected charge pumps 110 and 120 (each having one booster stage).

Accordingly, Zhang in view of Javanifard renders obvious that “*wherein the first number of booster stages is two*” as claimed in claim 5.

7. Claim 6

[6.0] 6. The method as claimed in claim 1, wherein the booster circuitry is changed between the first number of booster stages and the second number of booster stages with a switch.

Zhang in view of Javanifard renders obvious this element. EX1003, ¶¶157-159.

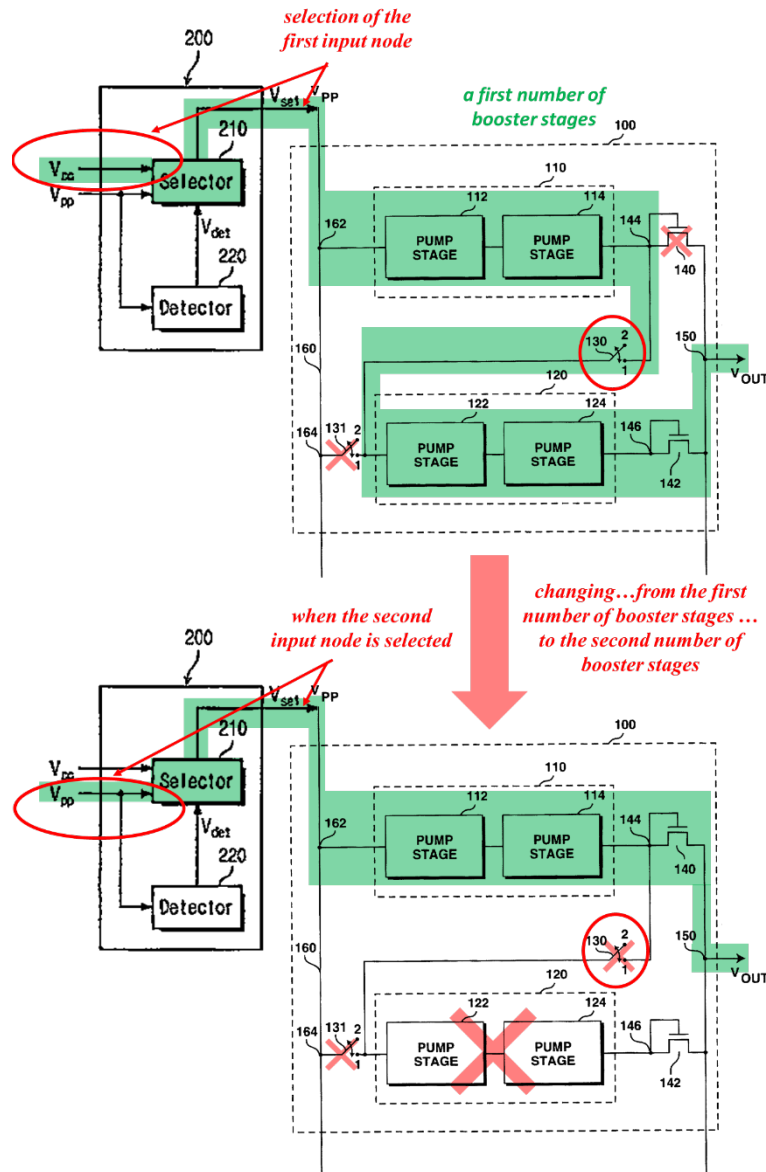
Javanifard teaches this element. As discussed at Ground 1:[1.3] and the annotated figures below, Javanifard teaches that the booster circuitry is changed between the first/higher number of booster stages (e.g., 4) and the second/lower number (e.g., 2) of booster stages, using a switch 130.

booster circuitry is changed...with a switch

TABLE 1

Switch 130	Switch 131	Charge Pump 110	Charge Pump 120	
OFF	OFF	ON	OFF	<i>a second number of booster stages, the second number being less than first number</i>
OFF	ON	ON	parallel-coupled to charge pump 110	
ON	OFF	ON	series-coupled to charge pump 110	<i>a first number of booster stages</i>
ON	ON	N/A	N/A	

EX1006, Javanifard, Table 1, annotated



Example A of Combination of Zhang and Javanifard (Changing Booster Circuitry with Switch 130)

Accordingly, as shown in Example A of the combination of Zhang in view of Javanifard, the booster circuitry 100 is changed between different number of stages using switch 130, which renders obvious this element.

8. Claim 7

[7.0] 7. The method as claimed in claim 1, wherein the booster circuitry is changed with a selected one of a metal option, a bonding option, and a fuse option.

Zhang in view of Javanifard renders obvious this element. EX1003, ¶¶160-165.

Javanifard teaches the element. As discussed at Ground 1:[6.0], Javanifard teaches that the booster circuitry is changed between different configurations (corresponding to different number of booster stages), e.g., by using a switch (e.g., switch 130). EX1006, Javanifard, 5:59-65.

Because Javanifard describes changing its booster circuitry between different configurations, a POSITA would know of three techniques to do so: using a bonding option, a metal option, or a fuse option. EX1003, ¶162 (citing EX1023, Kim, 1:15-18 (“IC products of a semiconductor use **an option operating method in order to change an operational mode [, which] is divided into a bonding option, a metal option or a fuse option.**”)); EX1018, Lee, 1:64-65). These known techniques for allowing a device maker to make changes, or options, for a device are fundamental to a POSITA, are used in the same known way, and are thus obvious. *See, KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 415-421, (2007); *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17 (S. Ct. 1966). In so doing, this allows the device maker to make a one-time change during the manufacture or assembly of the device to provide products of different

specifications, all from the same die design. For example, based on the needs of an end user, the device maker may use one of a bonding option, a metal option or a fuse option to configure devices of the same die design to provide (1) products that support both VCC and VPP supply lines, with the booster circuitry re-configurable using a control circuit, (2) products that support only the VCC supply line, with the booster circuitry configured based on VCC supply line; or (3) products that support only the VPP supply line, with the booster circuitry configured based on the VPP supply line. Thus, a POSITA would be well aware, as part of his/her basic knowledge of providing an “option” for the device to be modified as needed, using any of the three claimed techniques. *See also* the ’701 patent, which simply describes the general use of such well-known fundamental techniques. EX1003, ¶162 (citing EX1001, ’701 patent, 3:17-19).

A POSITA would have been motivated, in the multi-power-source charge pump design, to include the option operating design to change the booster circuitry, because it provides a manufacturer the flexibility to provide products with different specifications by configuring dies with the same multi-power-source charge pump design (e.g., during fabrication, packaging, or post-packaging process). A POSITA would have selected one of these well-known fundamental bonding option, metal option or fuse option based on the design needs (e.g., functionality, flexibility, cost considerations, process stage for configuration).

EX1003, ¶163 (citing EX1021, Hwang, 1:27-31; EX1022, Muff, [0014]; EX1023, Kim, 1:15-59).

Accordingly, in the combination of Zhang and Javanifard, a POSITA would have selected one of a bonding option, a metal option, or a fuse option to control the switch (e.g., switch 130) to change the booster circuitry configuration, based on the design needs, which renders obvious this element.

9. Claim 8

[8.0] 8. The method as claimed in claim 1, wherein the output voltage is a power supply voltage VPP.

Zhang in view of Javanifard renders obvious this element. EX1003, ¶¶166-171.

Javanifard teaches this element. Javanifard describes that the output voltage is provided as a power supply voltage to a local circuit, including for example, “various voltage levels required by a flash memory array” for each mode of operation including reading, erasing, programming, and therefore teaches that the output voltage is a power supply voltage VPP. EX1006, Javanifard, 6:5-17, FIG. 3 (the output voltage at output node 350 of the variable charge pump is provided as a power supply to a flash memory array 390), 5:56-59, 6:5-17, 8:34-38; EX1003, ¶¶167-168.

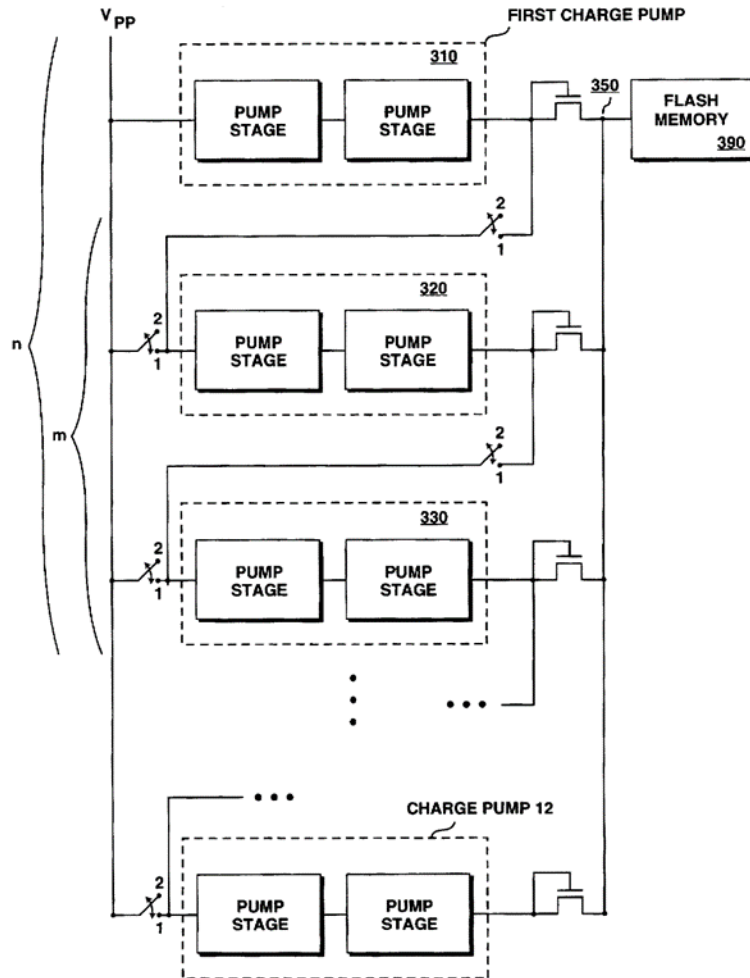


Figure 3

EX1006, Javanifard, FIG. 3

It was well-known in the art that the term “VPP” (also referred to as “V_{PP}”) is generally used to refer to power supply voltages to circuits, including for example, a power supply voltage to a charge pump circuit or a power supply voltage to a memory device. For example, in Javanifard, in FIGS. 1 and 3, VPP is used to refer to a power supply voltage provided to common input bus 160, and in FIG. 2, VPP is used to refer to a supplemental voltage provided to a flash memory

device where “VPP, is typically needed only when writing or erasing the memory because of the higher voltages needed during those operations.” EX1006, Javanifard, 6:44-51, FIG. 1, 2:52-53, 5:66-67; EX1005, Zhang, 3:24-25 (“The voltage VPP refers to a high voltage provided externally during a test operation mode.”). This general usage of “VPP” referring to a power supply voltage is consistent with the ’701 patent, which describes “**suppl[ying] the boosted voltage** to a local circuit,..., **as power supply VPP,**” and “an example of [local circuit] is a circuit for driving a word line.” EX1001, ’701 patent 4:63-67.

To the extent that Patent Owner attempts to assert that the claimed “*power supply voltage VPP*” requires a voltage for driving a word line, such arguments should be rejected, because the ’701 patent only provides “driving a word line” as an example use of VPP. Regardless, Javanifard teaches this element, because Javanifard’s variable stage charge pump provides various power supply voltage levels required by a flash memory device, including for driving a word line. EX1006, Javanifard, 6:5-17, 8:35-39.

Accordingly, Zhang in view of Javanifard renders obvious this element.

10.Claim 9

[9.0] 9. The method as claimed in claim 1, wherein the booster circuitry comprises capacitors formed using thin gate oxide transistors.

Zhang in view of Javanifard renders obvious this element. EX1003, ¶¶172-177.

Javanifard teaches this element. Javanifard teaches a variable stage charge pump, and it was well-known that pump stages in the variable stage charge pump include pumping capacitors for storing charges and thereby generating an output voltage higher than the input voltage. *See, e.g.,* EX1003, ¶173 (citing EX1014, Frulio, 1:23-34; EX1008, Pan, FIG. 3-2, 43-44; EX1015, Al-Shamma, FIG. 1, 4:61-64; 4:65-5:59; EX1016, Daga, FIGS. 2A-2B, FIG. 4); *see also* EX1005, Zhang, FIG. 5, 3:61-64.

A POSITA would have found it obvious to implement pumping capacitors in the variable stage charge pump of Javanifard in any of a variety of known and suitable ways—using either a thick gate oxide transistor or a thin gate oxide transistor in capacitor configuration (also referred to as a MOS capacitor), and would have been motivated to optimize the booster circuitry/variable stage charge pump of Javanifard by optimizing the pump capacitor by using a thin gate oxide transistor for the benefit of reduced area. EX1003, ¶174; EX1020, Kang, Abstract (“Using the thin-oxide capacitors can reduce the area of charge pumps greatly while keeping their driving capability.”), 258 (“Hence the pumping capacitors are C1, C2, and C3 as shown in Fig. 1(b) can be made with the thin-oxide transistors. By doing so, the layout area of C1, C2, and C3 becomes smaller compared with that of thick-oxide transistors. Because the area of the pumping capacitors takes the largest part of the total pump area, it is very helpful to make the area of the

pumping capacitors small for reducing the total pump area.”); EX1019, Narui, 9:51-64.

The prosecution history of the ’701 patent further supports that it would have been obvious to use a thin-oxide capacitor in the booster circuitry. EX1009, ’422 app, 280-290, 308-313. During the prosecution of the parent of the ’701 patent, Examiner rejected a claim limitation related to a thickness of the gate oxide film of a capacitor as obvious, explaining that “it is not inventive to discover the optimum or workable ranges by routine experimentation,” and therefore it would have been obvious to “**optimize the general capacitor**” with a specific gate oxide film thickness configuration. Applicant did not directly dispute Examiner’s rejection. EX1009, ’422 app, 268-274, 291-300.

As such, Zhang in view of Javanifard renders obvious this element.

11.Claim 10

[10.0] 10. A semiconductor device comprising:

To the extent that the preamble is limiting, Zhang discloses or renders obvious the preamble. EX1003, ¶¶178-180.

Specifically, Zhang describes a charge pump system implemented on integrated chips, as such, teaches a semiconductor device because an integrated chip includes semiconductor devices on a semiconductor wafer. EX1005, Zhang, 1:63-2:3 (“The conventional charge pump circuit pre-charges the output voltage V_{out} corresponding to the external voltage V_{CC} ...This additional time is

undesired, particularly where testing **integrated chips** that require high voltages quickly.”). Zhang teaches that the charge pump system is a semiconductor device including various circuits (e.g., selector 210) implemented using PMOS and NMOS transistors, which are semiconductor devices using semiconductor materials (e.g., p-type or n-type semiconductors). *See, e.g.*, EX1005, Zhang, 4:35-40 (“Referring to FIG. 6, the selector 210 uses a level shifter to control the high voltage VPP. The selector 210 comprises **high-voltage NMOS transistors N211 to N218, high-voltage PMOS transistors P211 to P218 and P210 I where i=1 to 4**, and two serially connected inverters.”).

Accordingly, Zhang discloses or renders obvious “*a semiconductor device*” as claimed.

[10.1]-[10.3]

Zhang in view of Javanifard renders obvious these elements for the reasons discussed at Ground 1:[1.1], [1.1], and [1.2.1] respectively. EX1003, ¶¶181-183.

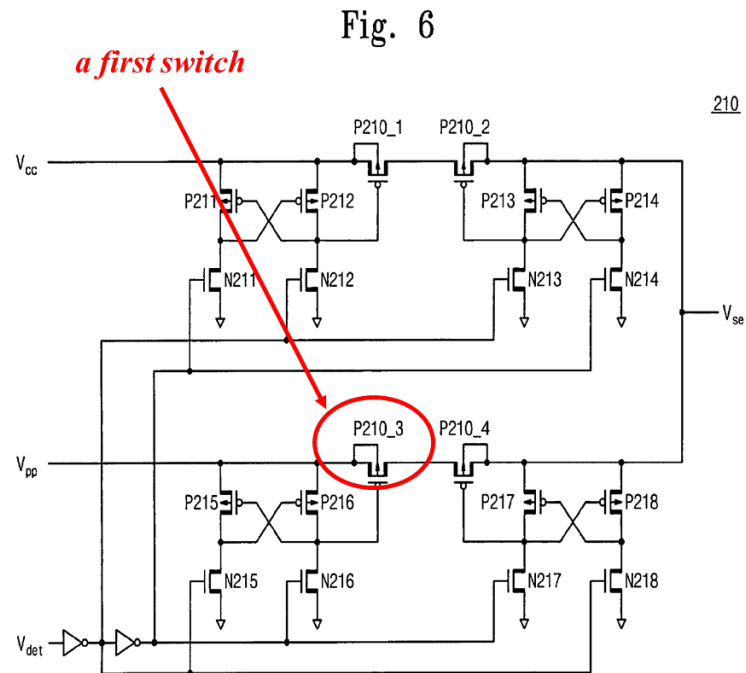
[10.4] a first switch configured to couple a selected one of the first input node and the second input node to the booster circuitry,

Zhang in view of Javanifard renders obvious this element. EX1003, ¶¶184-189.

First, as discussed at Ground 1:[1.2.1]-[1.2.3], in the combination of Zhang and Javanifard, a selected one of the first and second input nodes (e.g., as taught by the selecting circuit block 200 of Zhang) is coupled to booster circuitry (e.g., a

variable stage charge pump as taught by Javanifard) comprising a plurality of booster stages to provide an output voltage.

Second, referring to annotated FIG. 6 of Zhang below, Zhang describes that in selector 210 of the selecting circuit block 200 of the charge pump system, a first switch (P201_1, P210_2, P210_3, P210_4, and/or a combination thereof) is configured to couple a selected one of the first input node and the second input node to the booster circuitry.



EX1005, Zhang, FIG. 6, annotated

Specifically, Zhang describes that FIG. 6 is an example of the selector 210 of the selecting circuit block 200 of FIG. 4, and selector 210 uses one or more switches (using PMOS transistors) to select one of VCC and VPP as its output

voltage VSEL. EX1005, Zhang, 4:35-51. PMOS transistors are MOSFETS, and Zhang's use of PMOS transistors to implement switches was consistent with the well-known knowledge in the art. *See, e.g.,* EX1006, Javanifard, 3:13-15 (“switches 130 and 131 are implemented from metal oxide semiconductor field effect transistors (MOSFETs)”).

As such, in the combination of Zhang and Javanifard, the selecting circuit block (e.g., as taught by FIGS. 4 and 6 of Zhang) includes a switch configured to couple Vsel to a variable stage charge pump. Accordingly, Zhang in view of Javanifard renders obvious “*a first switch configured to couple a selected one of the first input node and the second input node to the booster circuitry*” as claimed.

[10.5]

Zhang in view of Javanifard renders obvious this element for the reasons at Ground 1:[1.2.2]-[1.2.3] and [1.3]. EX1003, ¶¶190-191.

12.Claims 11-14

Zhang in view of Javanifard renders obvious these elements for the reasons discussed at Ground 1:[2.0], [3.0], [4.0], and [5.0] respectively. EX1003, ¶¶192-195.

13.Claim 15

[15.0] 15. The semiconductor device as claimed in claim 10, wherein the booster circuitry is changed from the first number of booster stages and the second number of booster stages with a second switch.

Zhang in view of Javanifard renders obvious this element. EX1003, ¶¶196-199.

First, as discussed at Ground 1:[10.4], in the combination of Zhang and Javanifard, a first switch in a selecting block circuit is configured to couple a selected one of the first input node and the second input node to the booster circuitry.

Second, as discussed at Ground 1:[1.3] and [6.0], in the combination of Zhang and Javanifard, a switch (e.g., switch 130) in the variable stage charge pump, which is different from the first switch, is used to change the booster circuitry from the first number of booster stages to the second number of booster stages. The switch (e.g., switch 130) in the variable stage charge pump teaches “*a second switch*” as claimed.

Accordingly, Zhang in view of Javanifard renders obvious this element.

14.Claims 16-18

Zhang in view of Javanifard renders obvious these elements for the reasons discussed at Ground 1:[7.0], [8.0], and [9.0] respectively. EX1003, ¶¶200-202.

C. Ground 2: Claims 1-18 are Rendered Obvious under § 103 over Javanifard.

1. Reasons to Combine Embodiments of Javanifard.

As discussed above at IX.A.2, Javanifard describes various embodiments of variable stage charge pumps. A POSITA would have been motivated to combine Javanifard's embodiments. *Boston Scientific Scimed, Inc. v. Cordis Corp.*, 554 F.3d 982, 991 ("Combining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness."); EX1003, ¶¶203-209.

Embodiment 1 (described with example of FIG. 1 and Table 1 identifying a "2/2" stage pump) and **Embodiment 3** (described with example of FIG. 3 identifying a "12/2" stage pump) each describe a variable stage charge pump (identified as an "X/Y" stage pump) having a variable number (as opposed to a fixed number) of stages according to charge pump power supply input levels and desired charge pump output levels.

Embodiment 2 (described with example of FIG. 2 below and Tables 2 and 3) describes selecting from multiple power sources (e.g., VCC and VPP), and providing the selected power supply source to the variable stage charge pumps (e.g., variable stage charge pumps 210 and 220). EX1006, Javanifard, 6:61-64. Each of the variable stage charge pumps is configured based on the input power supply voltage (e.g., VCC or VPP) to provide required output voltage levels.

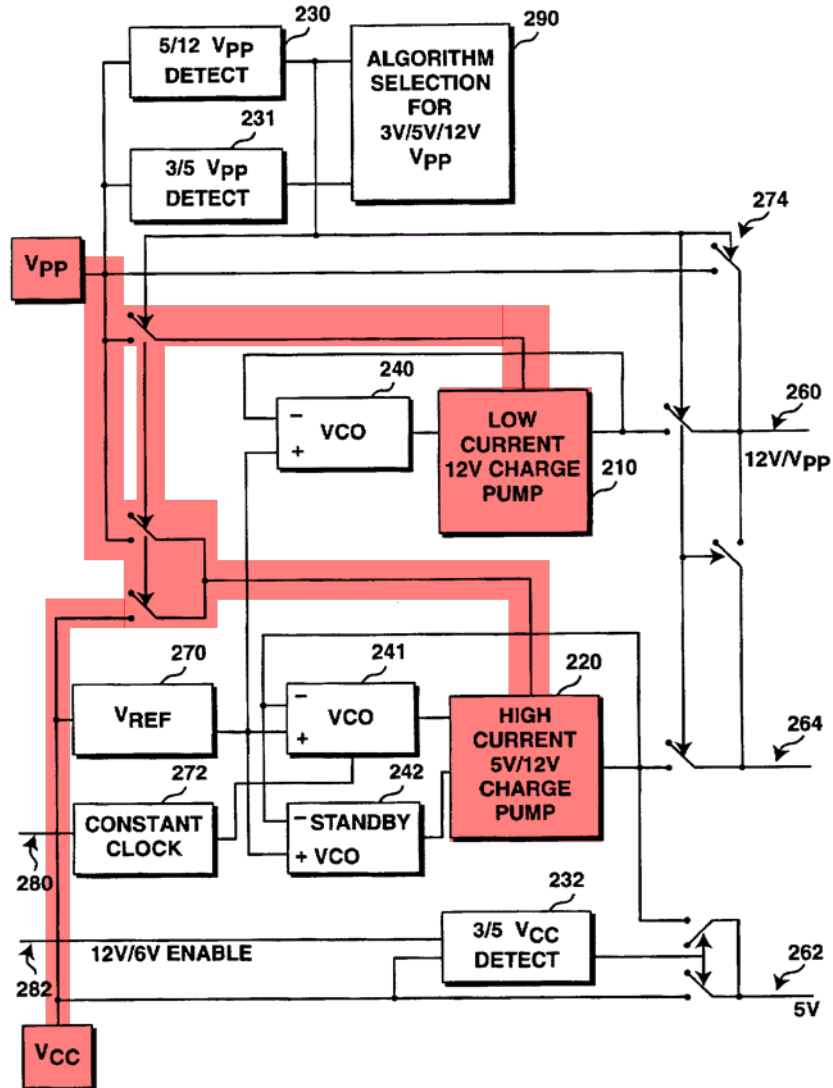


Figure 2

EX1006, Javanifard, FIG. 2, annotated

A POSITA would have been motivated to apply Embodiment 2's teachings of selection from multiple power sources to the variable stage charge pump as taught in Embodiments 1 or 3, by selecting and supplying the selected power supply source (as taught in Embodiment 2) to the input of the variable stage charge

pump, to produce the obvious, beneficial, and predictable results of a multi-power-source variable stage charge pump system. EX1003, ¶206; EX1006, Javanifard, 6:44-46; EX1005, Zhang, Abstract, FIG. 4).

Javanifard explicitly provides motivations to apply its teaching of selection from multiple power sources of Embodiment 2 to the variable stage charge pump of Embodiments 1 or 3, by providing the selected power supply to the variable stage charge pump. For example, one of Javanifard's objects is to "provide a charge pump that can accommodate a given output level for **different charge pump power supply input levels**." EX1006, Javanifard, 2:21-23. It was well-known that often different charge pump power supply input levels are provided by different power supply source lines. *See, e.g.*, EX1006, Javanifard, 6:44-46 and EX1005, Zhang, Abstract, FIG. 4. As such, it would have been obvious to apply Embodiment 2's teaching of selection from multiple power sources to the variable stage charge pump, to achieve Javanifard's object to "accommodate a given output level for different charge pump power supply input levels." EX1006, Javanifard, 2:21-23; EX1003, ¶207.

Applying Javanifard's teaching of selection from multiple power sources of Embodiment 2 to the variable stage charge pump of Embodiments 1 or 3 would have been no more than the combination of known elements according to known methods (e.g., incorporating a power source selection design in a variable stage

charge pump according to well-known IC design techniques including voltage detection and selection) obvious to a POSITA, which does no more than yield predictable results. EX1003, ¶208 (techniques (e.g., detectors and selectors) to select and provide a selected power supply voltage to a charge pump were well-known, citing EX1006, Javanifard, FIG. 2, EX1005, Zhang, FIG. 4).

As detailed below, the combination of Javanifard's embodiments renders Challenged Claims of the '701 patent obvious.

2. Claim 1

[1.0] 1. A method for generating a supply voltage, comprising:

Javanifard teaches the preamble to the extent it is limiting. EX1003, ¶¶210-212.

As shown in FIG. 1 of Javanifard below, Javanifard describes a variable stage charge pump generating a supply voltage for various devices, e.g., to **“provide the proper voltages** for the memory circuitry.” EX1006, Javanifard, FIG. 1, 5:17-24; 5:56-59, FIGS. 2, 3 (each illustrating generating a supply voltage to a memory device).

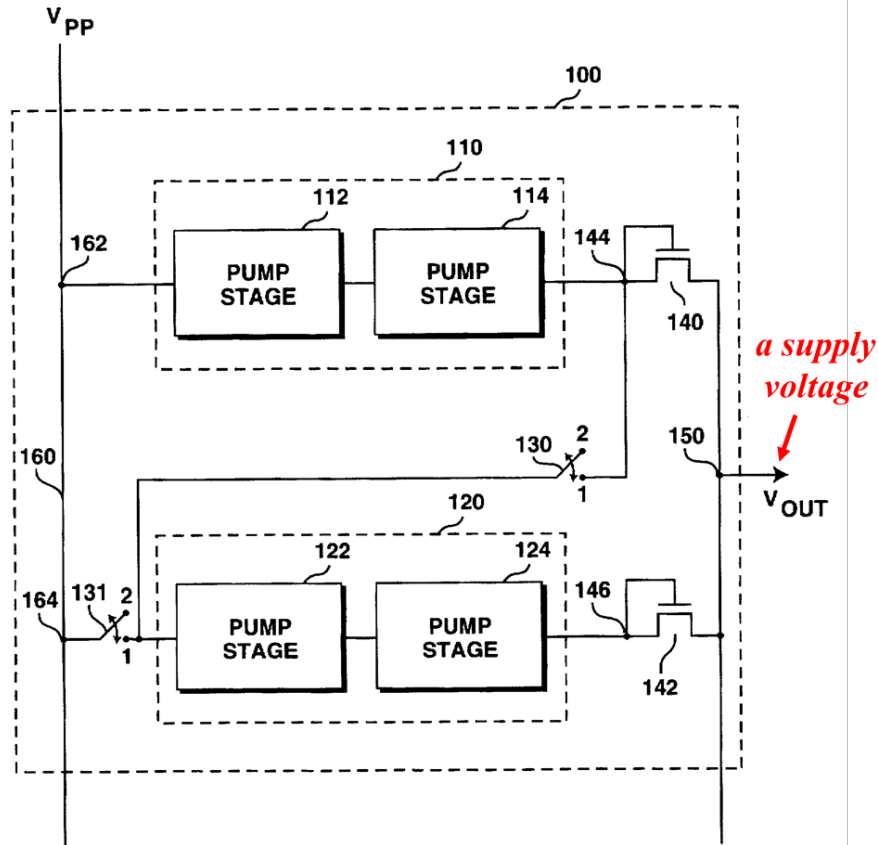


Figure 1

EX1006, Javanifard, FIG. 1, annotated

[1.1] selecting one of a first input node supplied with a first power supply voltage and a second input node supplied with a second power supply voltage that is higher than the first power supply voltage;

Javanifard teaches this element. EX1003, ¶¶213-220.

First, as discussed at Ground 1:[1.1], Javanifard describes coupling an input node with a power supply voltage to a booster circuitry comprising a plurality of booster stages to provide an output voltage, as shown in annotated FIG. 1 and FIG. 3 of Javanifard and below.

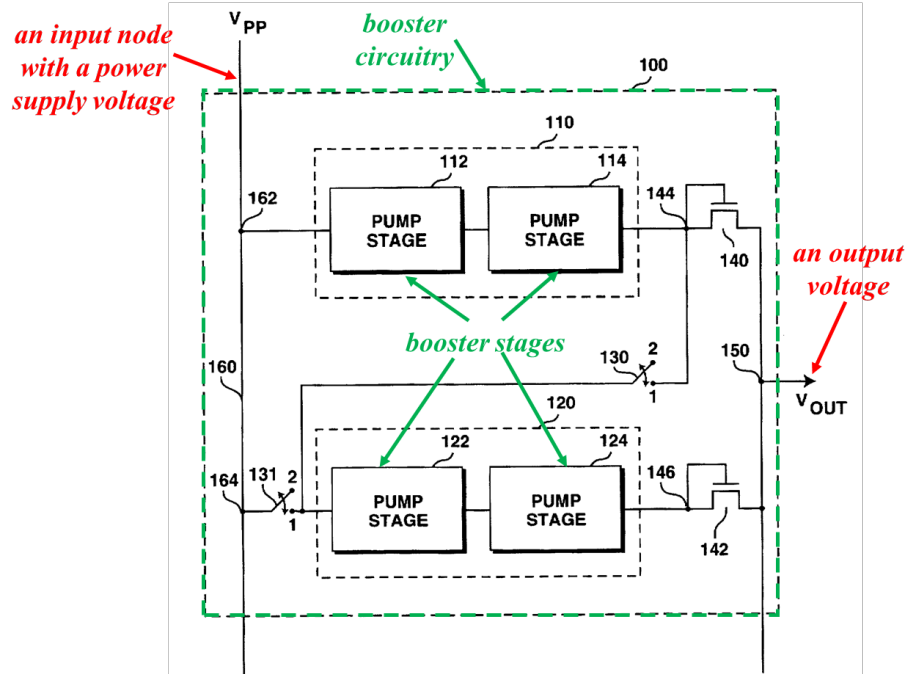
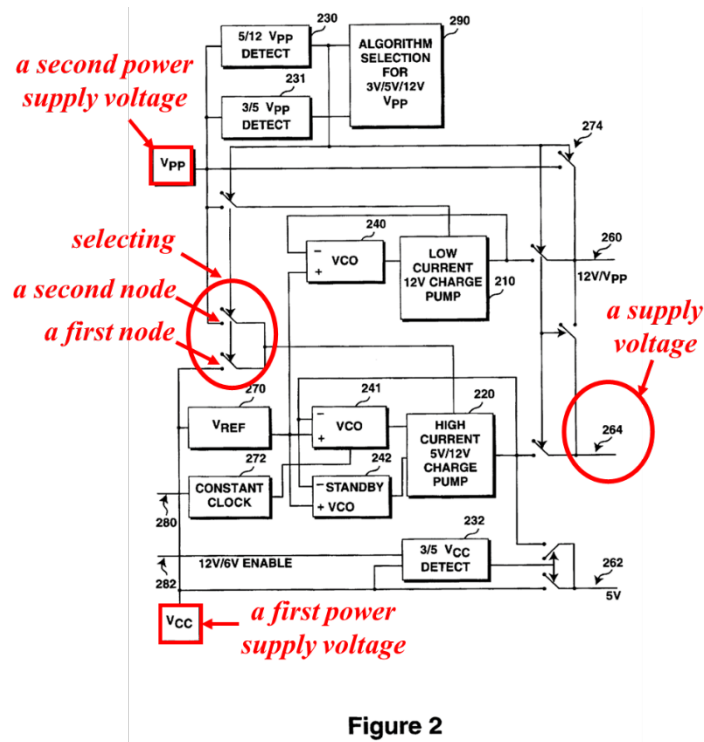


Figure 1

EX1006, Javanifard, FIG. 1, annotated

volt voltage level from **either a 3.3 volt or 5 volt power supply.**”); 7:15-17 (providing an example where “ $V_{CC} = 3.3$ volts”); 8:24-29 (providing an example where “ V_{PP} has a nominal value of 5 volts”). The switches for the selection are controlled by control signals provided by a selection circuit (e.g., selection circuit 290 with voltage detect circuits 230 and 231).



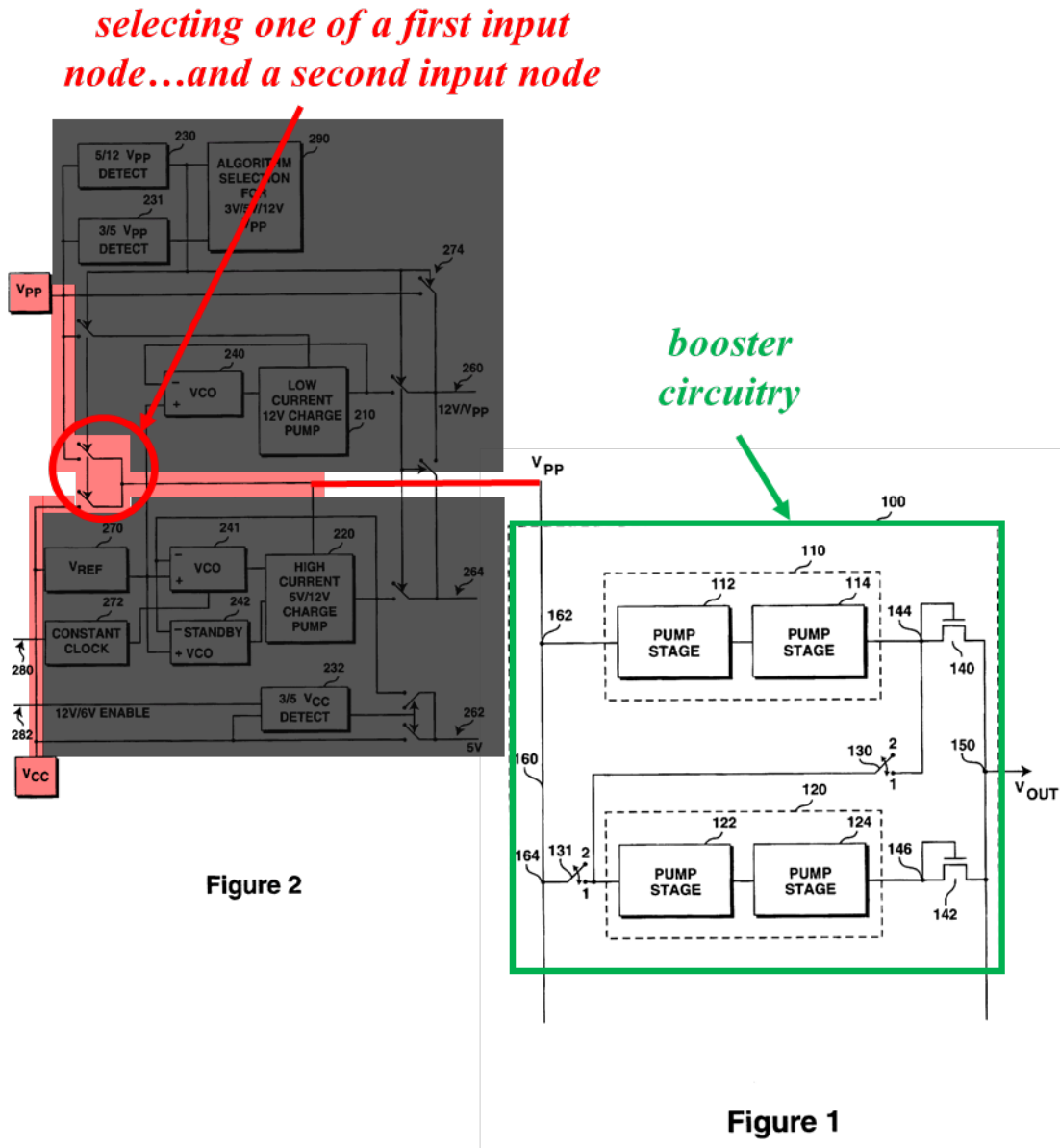
EX1006, Javanifard, FIG. 2, annotated

Third, as shown in the example figures of combinations of embodiments of Javanifard below, a POSITA would have been motivated to apply Javanifard teachings of an input power supply selector for selecting from input nodes supplied with different power supply voltages (as taught in Embodiment 2) in Javanifard’s variable stage charge pump system (e.g., as taught by the variable stage charge

pump of Embodiments 1 or 3). Such combinations have the benefit of providing a charge pump that can “**accommodate a given output level for different charge pump power supply input levels**”, e.g., for a device supplied with multiple power sources using two source lines (e.g., a primary power source and a supplemental power source). EX1006, Javanifard, 6:44-46 (describing that a flash memory device is provided by two sources including a primary power source VCC line and a supplemental power supply line, VPP); EX1005, Zhang, Abstract. FIG. 4; *see also* Ground 2: Reasons to Combine Embodiments of Javanifard.

As shown in the figures of Examples C and D below, in the combinations, one of a first input node supplied with a first (lower) power supply voltage and a second input node supplied with a second (higher) power supply voltage is selected, and provided to a booster circuitry. The figures below are simplified for illustration purposes, and it would have been obvious to a POSITA to implement additional well-known circuits (e.g., voltage detection circuit, voltage selection circuit providing control signals to selection switches, clock signals to drive the charge pumps) according to the design needs. Further, it would have been obvious to a POSITA that various voltages for VCC (e.g., 3.3 volts or other voltages) and VPP (e.g., 5 volts or other voltages greater than VCC) would be used based on design needs.

Example C (Embodiments 1 and 2 of Javanifard combined) is illustrated below, which is a composite figure of FIGS. 1 and 2 of Javanifard.



Example C (Embodiments 1 and 2 of Javanifard Combined)

Example D (Embodiments 2 and 3 of Javanifard combined) is illustrated below, which is a composite figure of FIGS. 2 and 3 of Javanifard.

*selecting one of a first input
node...and a second input node*

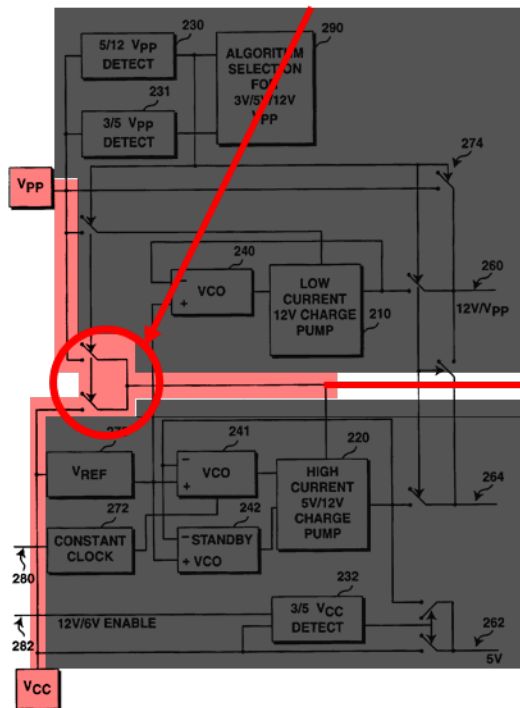


Figure 2

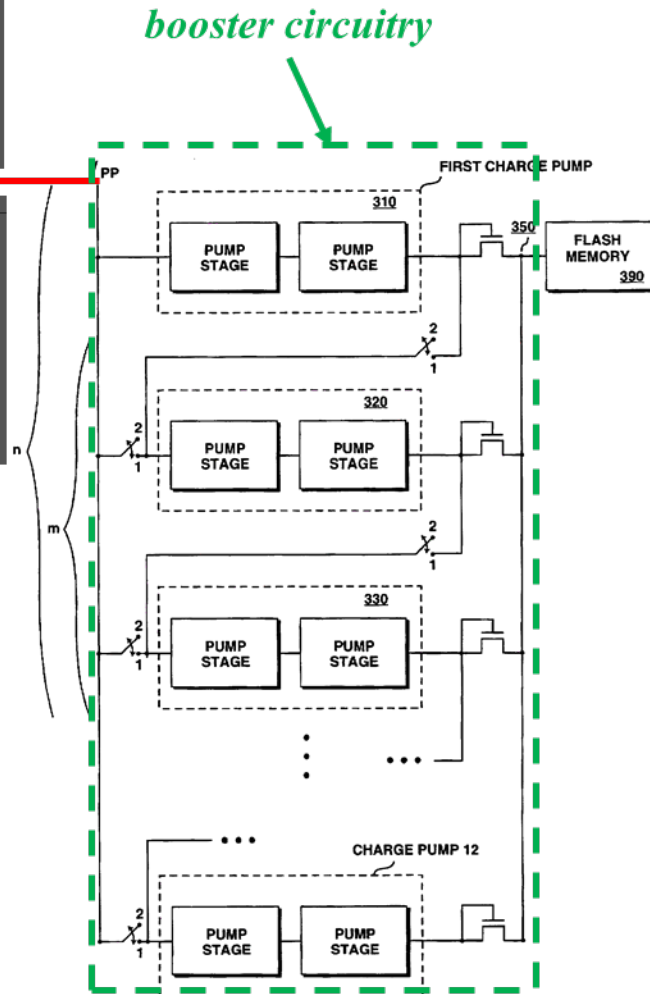


Figure 3

Example D (Embodiments 2 and 3 of Javanifard Combined)

Accordingly, Javanifard discloses or renders obvious this element.

[1.2.1] coupling a selected one of the first and second input nodes to booster circuitry comprising a plurality of booster stages to provide an output voltage,

Javanifard teaches this element. EX1003, ¶¶221-225.

First, as discussed at Ground 2:[1.1], the combinations of embodiments of Javanifard teach that a selected one of the first and second input nodes is coupled to a variable stage charge pump (booster circuitry).

Second, as discussed at Ground 1:[1.2.1], as shown in FIGS. 1 and 3 of Javanifard, Javanifard describes that its variable stage charge pump (booster circuitry) comprises booster stages to provide an output voltage.

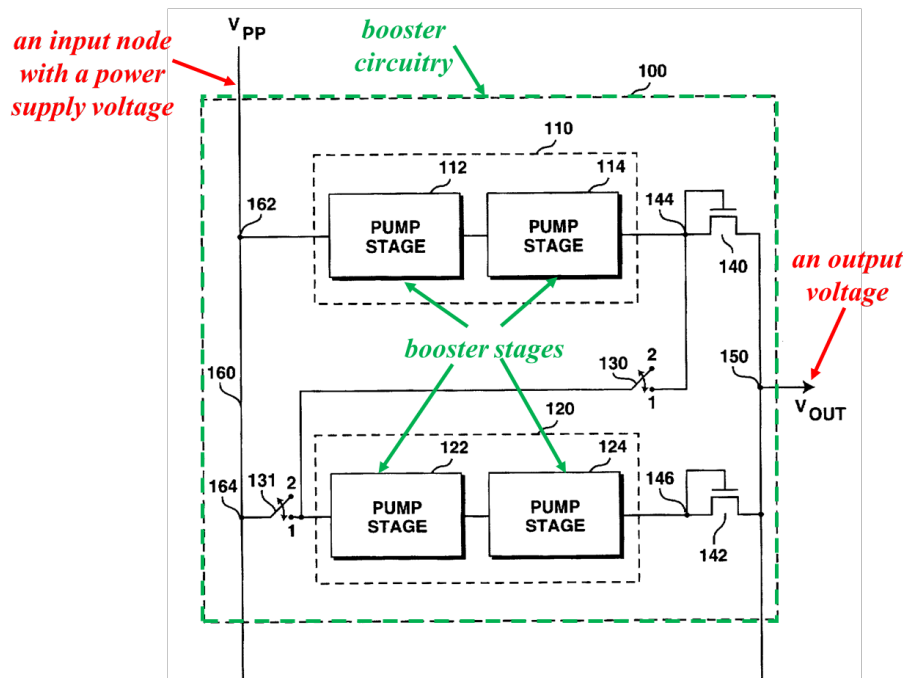


Figure 1

EX1006, Javanifard, FIG. 1, annotated

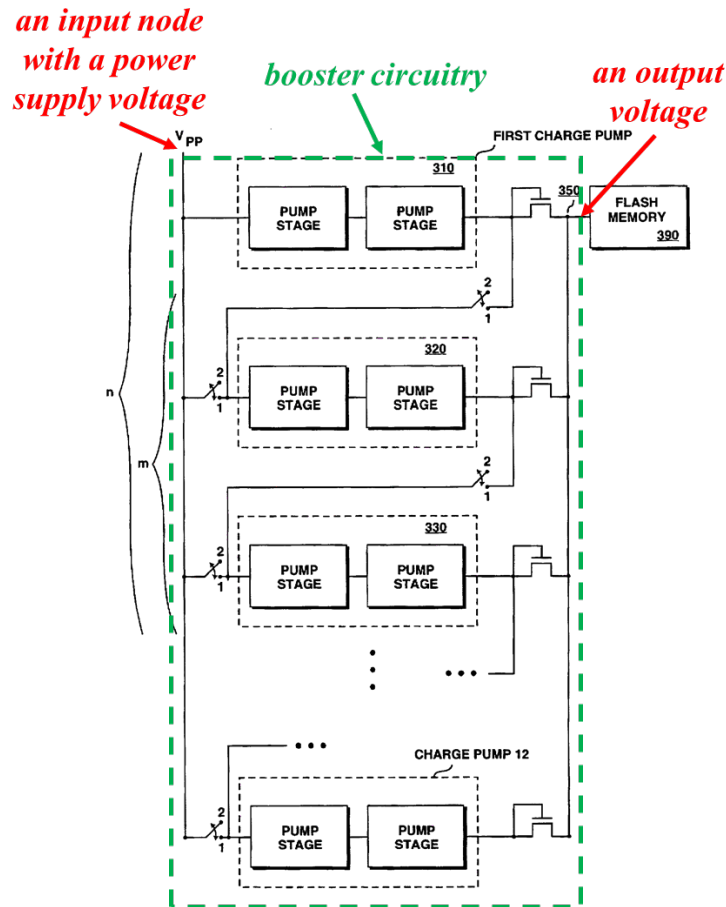


Figure 3

EX1006, Javanifard, FIG. 3, annotated

As such, in the combinations of embodiments of Javanifard, a selected one of the first and second input nodes corresponding to VCC and VPP is coupled to a variable stage charge pump (booster circuitry) to provide Vout, which renders obvious “coupling a selected one of the first and second input nodes to booster circuitry comprising a plurality of booster stages to provide an output voltage” as claimed.

[1.2.2] wherein selection of the first input node corresponds to a first number of booster stages and

Javanifard teaches this element. EX1003, ¶¶226-232.

As discussed above at Ground 1:[1.2.2], Javanifard describes providing a variable stage charge pump to “accommodate a **given output level for different** charge pump power supply input levels.” EX1006, Javanifard, 2:22-24. For example, a POSITA would have configured the variable stage charge pump of FIG. 1 of Javanifard according to row 3 of Table 1 for a lower charge pump power supply input level, such that selection of the first input node corresponds to a first number (a higher number, e.g., 4) of booster stages.

As such, in Example C, to “accommodate a **given output level” (EX1006, Javanifard, 2:22-24) for the first input node with a lower power supply voltage VCC, a POSITA would have configured the variable stage charge pump of FIG. 1 of Javanifard according to row 3 of Table 1 below, which provides a first number (a higher number, e.g., 4) of serially connected booster stages to provide a higher voltage boost (e.g., by serially connecting charge pumps 110 and 120), compared to row 1 of Table 1 (by providing only charge pump 110 in operation and thereby having a lower number (e.g., 2) of serially connected booster stages). EX1003, ¶228.**

TABLE 1

Switch 130	Switch 131	Charge Pump 110	Charge Pump 120	
OFF	OFF	ON	OFF	<i>a second number of booster stages, the second number being less than first number</i>
OFF	ON	ON	parallel-coupled to charge pump 110	
ON	OFF	ON	series-coupled to charge pump 110	<i>a first number of booster stages</i>
ON	ON	N/A	N/A	

EX1006, Javanifard, Table 1, annotated

Similar analysis applies to Example D. It would have been obvious to a POSITA to use various suitable X and Y in the “X/Y stage pump,” pump stage designs, and configurations to provide the required output voltage according to the different power supply input levels. EX1003, ¶231.

Accordingly, Javanifard renders obvious “*wherein selection of the first input node corresponds to a first number of booster stages*” as claimed.

[1.2.3] selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number; and

Javanifard teaches this element. EX1003, ¶¶233-239.

First, as discussed at Ground 2:[1.2.1] and [1.2.2], in the combination of Javanifard embodiments, selection of the first input node (with a lower input power supply voltage level) corresponds to a first number (a higher number, e.g., 4) of booster stages.

Second, for similar reasons as discussed at Ground 2:[1.2.2], in the combination of Javanifard embodiments, selection of the second input node (with

a higher input power supply voltage level) corresponds to a second number (a lower number, e.g., 2) of booster stages, e.g., for generating the same output voltage as the selection of the first input node with a lower input power voltage level (corresponding to a higher number of booster stages).

Javanifard describes providing a variable stage charge pump to “accommodate a **given output level** for **different** charge pump power supply input levels.” EX1006, Javanifard, 2:22-24. Specifically, to “accommodate a **given output level**” (EX1006, Javanifard, 2:22-24) for the second input node with a higher power supply voltage, a POSITA would have configured the variable stage charge pump of FIG. 1 of Javanifard according to row 1 of Table 1 below, because row 1 of Table 1 provides a second (lower, e.g., 2) number of serially connected booster stages to provide a lower voltage boost (by providing only charge pump 110 in operation and thereby having a lower number of serially connected booster stages). Connecting less stages in series provide a lower voltage boost compared to using a higher number of stages in series, as each stage in the charge pump contributes to increasing the voltage level, and the total voltage boost is the cumulative effect of all the stages.

TABLE 1

Switch 130	Switch 131	Charge Pump 110	Charge Pump 120	
OFF	OFF	ON	OFF	<i>a second number of booster stages, the second number being less than first number</i>
OFF	ON	ON	parallel-coupled to charge pump 110	
ON	OFF	ON	series-coupled to charge pump 110	<i>a first number of booster stages</i>
ON	ON	N/A	N/A	

EX1006, Javanifard, Table 1, annotated

Additionally, while configurations of rows 1 and 2 of Table 1 may provide substantially the same voltage boost, a POSITA would have used row 1 based on a design need for power saving mode, because it provides a lower current than row 2. EX1006, Javanifard, 3:39-42 (“This configuration [of row 1] might be used in a power saving mode if charge pump 100 is otherwise providing sufficient current and voltage output levels.”).

Similar analysis applies to Example D of the combination of Embodiments 2 and 3 of Javanifard. While the example of FIG. 1 and Table 1 of Javanifard provides a “X=2/Y=2 stage pump,” it would have been obvious to a POSITA to use various suitable X, Y, and pump stage designs to provide the required output voltage according to the different power supply input levels, where a lower input voltage corresponds to a selection of a higher number of booster stages.

Accordingly, Javanifard discloses or renders obvious “*selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number*” as claimed.

[1.3] changing the booster circuitry from the first number of booster stages corresponding to selection of the first input node to the second number of booster stages when the second input node is selected.

Javanifard teaches this element. EX1003, ¶¶240-245.

First, as discussed at Ground 2: [1.2.2] and [1.2.3], in the combination of Javanifard embodiments, selection of the first input node corresponds to a first number of booster stages, and selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number, e.g., to provide the same output voltage for different power supply voltage levels.

Second, as discussed at Ground 1:[1.3], Javanifard describes changing the booster circuitry from a higher number (e.g., 4) of booster stages corresponding to a lower power supply voltage to a lower number (e.g., 2) of booster stages when the power supply voltage is higher. EX1006, Javanifard, 1:8-12, 5:65-67. Specifically, as shown in Table 1 below, the number of the booster stages of the booster circuitry is changed (e.g., reduced from 4 to 2) by changing switch 130 from on (row 3) to off (row 1) to provide the same output voltage level, when the charge pump power supply input level increases.

TABLE 1

Switch 130	Switch 131	Charge Pump 110	Charge Pump 120	
OFF	OFF	ON	OFF	<i>a second number of booster stages, the second number being less than first number</i>
OFF	ON	ON	parallel-coupled to charge pump 110	
ON	OFF	ON	series-coupled to charge pump 110	<i>a first number of booster stages</i>
ON	ON	N/A	N/A	

EX1006, Javanifard, Table 1, annotated

Similar to the discussion at Ground 1:[1.3], in the combination of Javanifard embodiments, when the selection of the input node is changed to the higher power supply voltage, the booster circuitry is changed from the first number of booster stages (e.g., 4) to the second number of booster stages (e.g., 2), by turning off switch 130.

Similar analysis applies to Example D of the combination of Embodiments 2 and 3 of Javanifard. While the example of FIG. 1 and Table 1 of Javanifard provides a “X=2/Y=2 stage pump,” in the combination, it would have been obvious to a POSITA to use various suitable X, Y, and pump stage designs to provide the required output voltage according to the different power supply input levels.

Accordingly, Javanifard discloses or renders obvious “*changing the booster circuitry from the first number of booster stages corresponding to selection of the*

first input node to the second number of booster stages when the second input node is selected” as claimed.

3. Claims 2-3

For reasons explained above for Ground 1:[2.0] and [3.0], Javanifard teaches these elements. EX1003, ¶¶246-252.

4. Claims 4-5

For reasons explained above for Ground 1:[4.0] and [5.0], Javanifard teaches these elements. EX1003, ¶¶253-257.

For example, as shown in figure of Example C below and as discussed at Ground 2:[1.2.2] and [1.2.3], because each of fixed stage charge pumps 110 and 120 has two booster stages, selection of first/lower power supply VCC corresponds to selection of four (4) booster stages (pump stages 112, 114, 122, 124), and selection of second/higher power supply VPP corresponds to selection of two (2) booster stages (pump stages 112,114).

*selecting one of a first input
node...and a second input node*

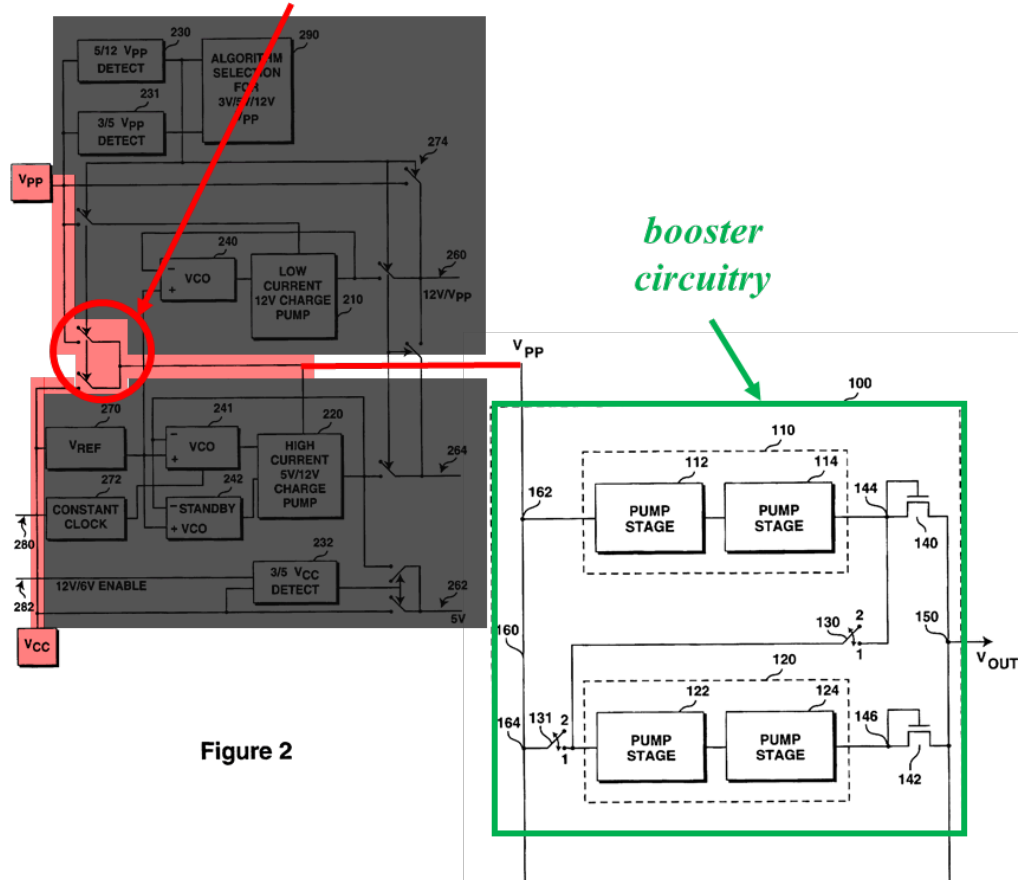


Figure 2

Figure 1

Example C (Embodiments 1 and 2 of Javanifard Combined)

As discussed at Ground 1:[4.0] and [5.0], it would have been obvious to implement each of fixed stage charge pumps 110 and 120 with one single booster stage. As such, it would have been obvious to modify Example C with such implementation. In such implementation, when the second input node with the higher power supply voltage is selected, the booster circuitry 100 (including the selected charge pump 110) has one (1) booster stage, which renders obvious claim

4. When the first input node with the lower power supply voltage is selected, the booster circuitry 100 has two (2) booster stages from serially connected charge pumps 110 and 120 (each having one booster stage), which renders obvious claim 5.

5. Claims 6-9

For reasons explained above for Ground 1:[6.0]-[9.0], Javanifard teaches these elements. EX1003, ¶¶258-264.

6. Claim 10

[10.0] 10. A semiconductor device comprising:

Javanifard teaches the preamble to the extent that it's limiting. EX1003, ¶¶265-267.

Specifically, Javanifard teaches a semiconductor device, because it describes charge pump systems implemented in “integrated circuits,” where an integrated circuit includes a set of electronic circuits integrated on a semiconductor chip. EX1006, Javanifard, 1:15-19, 3:13-15 (describing semiconductor components (e.g., switches 130 and 131) implemented from metal oxide semiconductor field effect transistors (MOSFETs), which are semiconductor devices). EX1003, ¶266.

[10.1]-[10.3]

Javanifard teaches these elements for the reasons discussed at Ground 2:[1.2]-[1.2.1]. EX1003, ¶¶268-270.

[10.4] a first switch configured to couple a selected one of the first input node and the second input node to the booster circuitry,

Javanifard teaches this element. EX1003, ¶¶271-275.

First, as discussed above at Ground 2:[1.1] and [1.2.1], Javanifard describes an input power supply selector (including one or more switches) for selecting from a first input node supplied with a first power supply voltage (e.g., VCC) and a second input node supplied with a second power supply voltage (e.g., VPP), and coupling the selected input node to the booster circuitry.

Second, as shown in annotated FIG. 2 of Javanifard below, Javanifard's input power supply selector includes one or more switches for selecting the input node. In FIG. 2 of Javanifard, two switches are illustrated for such selection, and either one of these switches teach the first switch as claimed. Furthermore, to the extent that Patent Owner argues that "only" one switch is used for such selection (which the claim does not require), it would have been obvious to a POSITA to implement the selection function as shown in FIG. 2 of Javanifard using either two switches (as illustrated in FIG. 2) or using a single switch (e.g., a three-way switch).

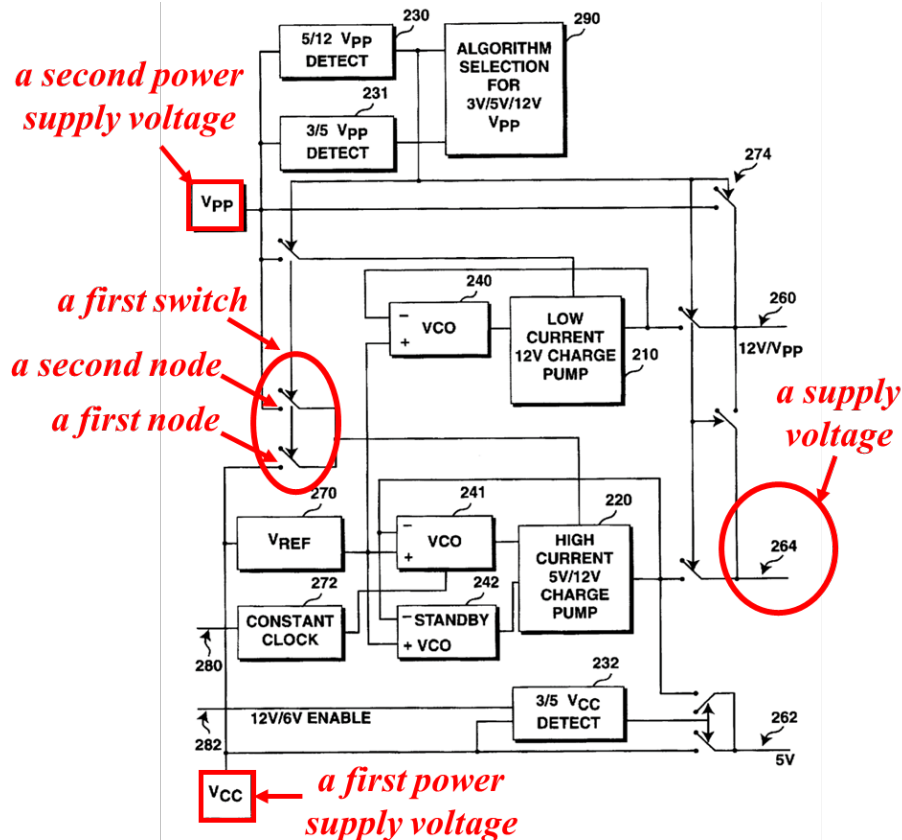


Figure 2

EX1006, Javanifard, FIG. 2, annotated

As such, in the combination (e.g., Examples C and D) of Javanifard embodiments, a switch is used to couple a selected input node to the booster circuitry, which renders obvious “*a first switch configured to couple a selected one of the first input node and the second input node to the booster circuitry*” as claimed.

[10.5]

Javanifard teaches this element for the reasons discussed at Ground 2:[1.2.2]-[1.2.3] and [1.3]. EX1003, ¶276.

7. Claims 11-14

Javanifard teaches these elements for the reasons discussed at Ground 2:[2.0], [3.0], [4.0], and [5.0] respectively. EX1003, ¶¶277-280.

8. Claim 15

[15.0] 15. The semiconductor device as claimed in claim 10, wherein the booster circuitry is changed from the first number of booster stages and the second number of booster stages with a second switch.

Javanifard renders obvious this element. EX1003, ¶¶281-284.

First, as discussed at Ground 2:[10.4], in the combination of Javanifard embodiments, a first switch in a selector circuit is configured to couple a selected one of the first input node and the second input node to the booster circuitry.

Second, as discussed at Ground 2:[1.3] and [6.0], Javanifard teaches using a second switch (e.g., switch 130) in the variable stage charge pump, which is different from the first switch in the selector, to change the booster circuitry from the first number of booster stages to the second number of booster stages.

Accordingly, Javanifard renders obvious that “*the booster circuitry is changed from the first number of booster stages and the second number of booster stages with a second switch*” as claimed.

9. Claims 16-18

Javanifard discloses or renders obvious these elements for the reasons discussed at Ground 2:[7.0], [8.0], and [9.0] respectively. EX1003, ¶¶285-287.

D. Grounds 3 and 4: Combination of Zhang, Javanifard, and Kang (Ground 3) and Combination of Javanifard and Kang Render Obvious Claims 9 and 18 (Ground 4).

The claim analysis for Grounds 3 and 4 rely on the analysis and evidence as provided for Ground 1 (Zhang and Javanifard) and Ground 2 (Javanifard), respectively, except for where additional analysis (applying for both Grounds 3 and 4) is provided below. EX1003, ¶¶288-300.

1. Reasons to Combine Javanifard and Kang

As discussed at Grounds 1 and 2 above, the combination of Zhang and Javanifard and the combination of Javanifard embodiments similarly teach a multi-power-source charge pump system using a variable stage charge pump as taught in Javanifard. EX1003, ¶¶289-294.

A POSITA would have been motivated to apply Kang’s teaching of using thin-oxide MOSFETs as the pumping capacitors in the variable stage charge pump, to produce the obvious, beneficial, and predictable results of a charge pump system with “low area and high power efficiency,” as taught by Kang.

Kang explicitly provides motivations to apply its teaching of using the thin-oxide MOSFETs as the pumping capacitors in a charge pump system, to achieve “charge pump circuits with low area and high power efficiency.” EX1020, Kang, 262. Specifically, Kang describes that by using thin-oxide transistors to form the pumping capacitors, “the layout area of [pumping capacitors] becomes smaller

compared with that of thick-oxide transistor,” and “[b]ecause the area of the pumping capacitors takes the largest part of the total pump area, it is very helpful to make the area of the pumping capacitors small for reducing the total pump area.” EX1020, Kang, 258; *see also* EX1019, Narui, 9:51-64.

A POSITA designing a charge pump system including a variable stage charge pump as taught by Javanifard would have been motivated to apply Kang’s teachings of a pump stage design using the thin-oxide MOSFETs as the pumping capacitors for the obvious, beneficial, and predictable results of an improved charge pump system by “reduc[ing] the area of charge pumps greatly while keeping their driving capability,” as taught by Kang.

Applying Kang’s teachings in the variable stage charge pump of Javanifard would have been no more than the combination of known elements according to known methods (implementing the generic pump stages of a variable stage charge pump using a pump stage design using thin-oxide pumping capacitors according to known IC design methods) obvious to a POSITA. While examples of Kang (e.g., FIG. 1(b), FIG. 2(c) and 2(d)) illustrate 3-stage charge pumps, it would have been obvious to a POSITA to apply Kang’s teaching of using thin-oxide capacitors in each pump stage of the charge pump, regardless of the charge pump’s number of stages. Techniques for designing (e.g., using IC design and simulation tools) and

making (e.g., using semiconductor fabrication processes) an IC including various components like charge pumps and pump stages were well-known.

2. Claim 9

[9.0] 9. The method as claimed in claim 1, wherein the booster circuitry comprises capacitors formed using thin gate oxide transistors.

Javanifard in view of Kang renders obvious this element. EX1003, ¶¶295-299.

First, as discussed in Grounds 1 and 2:[9.0], it would have been obvious to use pumping capacitors formed using thin gate oxide transistors in the variable stage charge pump for the benefit of area reduction.

Second, Kang explicitly describes pump stages with capacitors formed using thin gate oxide transistors. EX1020, Kang, Abstract, FIG. 1(b), 258, FIG. 2(c) and 2(d), 260-262.

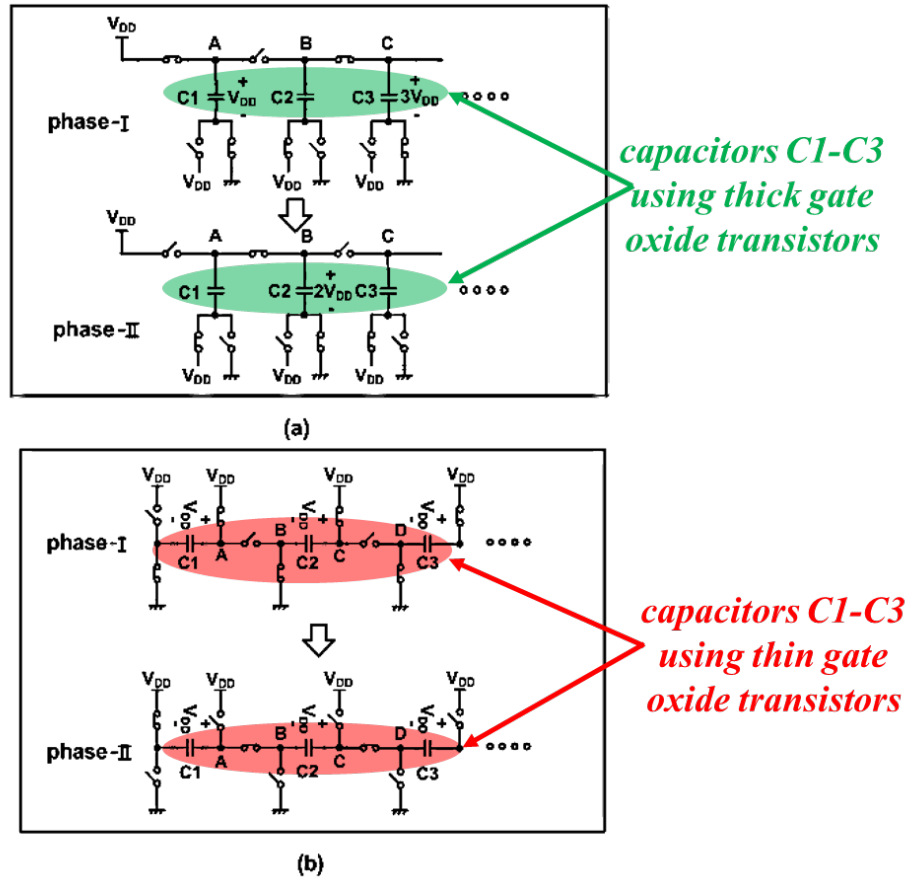


Fig. 1. (a) A conceptual diagram of the conventional charge pump (b) A conceptual diagram of new charge pump.

EX1020, Kang, FIG. 1, annotated

A POSITA would have been motivated to apply Kang's teaching of a pump stage design using thin-oxide MOSFETs as the pumping capacitors in Javanifard's variable stage charge pump to produce the obvious, beneficial, and predictable results of a charge pump system with "low area and high power efficiency," as taught by Kang. *See also* Grounds 3 and 4: Reasons to Combine Javanifard and Kang.

Accordingly, Javanifard combined with Kang renders obvious this element.

3. Claim 18

Javanifard in view of Kang renders obvious the element for the reasons discussed at Grounds 3 and 4:[9.0]. EX1003, ¶300.

X. CONCLUSION

Petitioner has established a reasonable likelihood that Challenged Claims of the '701 patent are unpatentable, and requests institution of *inter partes* review and cancelation of Challenged Claims.

Respectfully submitted,

Dated: July 20, 2023

/ *David O'Dell* /
David M. O'Dell
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Registration No. 42,044

XI. MANDATORY NOTICES

A. Real Party-in-Interest

The real party-in-interest is Western Digital Technologies, Inc. (“Petitioner” or “WDT”).

As shown in XI.B below, the Amazon Action concerning the ’701 patent is pending, involving WDT’s customer as the defendant. Petitioner submits that WDT is the only real party-in-interest, but regardless of whether the defendant should be named as an RPI, no RPI analysis is necessary because there are no time bar or estoppel implication for the defendant. *SharkNinja Operating LLC v. iRobot Corp.*, IPR2020-00734, Paper 11 (Oct. 6, 2020) (precedential) (no RPI analysis necessary at institution absent allegation of time bar or estoppel based on unnamed RPI).

B. Related Matter

As of the filing date of this Petition and to the best knowledge of Petitioner, the ’701 patent has been asserted in the following matter:

Case Heading	Number	Court	Filed	Status
<i>Longitude Licensing Limited v. Amazon.com, Inc.</i> (Amazon Action)	8-23-cv-00039	CDCA	Jan. 09, 2023	WDT’s motion to intervene granted; stayed pending the resolution of the Amazon Action with respect to WDT

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Please address all correspondence to lead and back-up counsel. Petitioner consents to electronic service and asks Patent Owner to do the same.

XII. CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24, the undersigned attorney for Petitioner declares that the argument section of this Petition (Sections I–X) has 13,965 words, according to the word count tool in Microsoft Word™.

/ *David O'Dell* /

David M. O'Dell

Lead Counsel for Petitioner

Registration No. 42,044

CERTIFICATE OF SERVICE

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105, service was made on Patent Owner as detailed below.

Date of service July 20, 2023

Manner of service FEDERAL EXPRESS

Documents served Petition for *Inter Partes* Review, including Exhibit List; Exhibits EX1001–EX1024

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