

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

LONGITUDE LICENSING LTD.,
Patent Owner.

Case IPR2023-01230
U.S. Patent No. 9,207,701

PATENT OWNER'S PRELIMINARY RESPONSE

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I. Introduction

The Petition does not demonstrate a reasonable likelihood of prevailing because the Petition sets forth no coherent motivation to combine the prior art in the way the Petition alleges would have been done.

The Petition's first ground involves a combination of Zhang (which claims priority to 2003) with Javanifard (which claims priority to 1995). The Petition relies almost exclusively on Javanifard's discussion of "disadvantages" of specific "prior art methods" for generating multiple output voltages as motivating its combination of Zhang with Javanifard. But the Petition does not allege (much less show) that any of these "disadvantages" would be applicable to Zhang, which is not prior art to Javanifard and does not practice the techniques Javanifard criticizes. Thus, the Petition provides no evidence that a POSITA would have been motivated to make the proposed modification to Zhang in view of Javanifard.

The Petition's second ground involves a hindsight-motivated combination of two different embodiments of Javanifard itself. Notably, the Petition does not combine these embodiments in the way that Javanifard itself suggests; rather, the Petition's combination involves *eliminating* the vast majority of functionality of one of the embodiments, rendering that embodiment inoperable for its intended purpose. And the Petition's sole alleged motivation to make that modification is a benefit that a POSITA would readily recognize was already present in the unmodified

embodiment, such that the proposed modification would not even arguably solve any problem present in Javanifard.

And the Petition's Grounds 3 and 4 do not cure any of these deficiencies; rather, those grounds "rely on the analysis and evidence as provided for Ground 1 (Zhang and Javanifard) and Ground 2 (Javanifard), respectively." Pet. 87.

Because the Petition fails to set forth a motivation to combine the prior art to arrive at the challenged claims, institution should be denied.

II. Background

A. Western Digital's Petition

Petitioner Western Digital Technologies, Inc. ("Petitioner" or "Western Digital") challenges claims 1-18 of U.S. Patent No. 9,207,701 (the "'701 Patent").

Petitioner structures its two asserted grounds for unpatentability as follows:

- Ground 1: Obviousness of claims 1-18 over Zhang in view of Javanifard.
- Ground 2: Obviousness of claims 1-18 over Javanifard.
- Ground 3: Obviousness of claims 9 and 18 over Zhang in view of Javanifard and Kang.
- Ground 4: Obviousness of claims 9 and 18 over Javanifard in view of Kang.

Because all challenged dependent claims depend from claims 1 and 10, this Preliminary Response need only address the Petition's arguments concerning claims

1 and 10. If the Petition does not show a reasonable likelihood of prevailing on claims 1 and 10, then it cannot prevail on any other challenged claim. And because the Petition only challenges the validity of claims 1 and 10 in Grounds 1 and 2, institution must be denied unless the Petition can establish a reasonable likelihood of prevailing as to either of those grounds.

B. Overview of the '701 Patent

At a high level, the '701 Patent is directed generally to a novel methods and devices for generating a given supply voltage by selecting between at least two different input voltages and between at least two different numbers of booster stages within a variable charge pump. *See, e.g.*, Ex. 1001, Claims 1, 10. The '701 Patent teaches that its invention allows the provision of “a supply voltage generating circuit of smaller chip area” over the prior art, because the design avoids the requirement of using “a thick-film capacitor element” to account for variations in external supply volage. *See id.* at 1:61-2:27 (“[I]n a case where the supply voltage supplied from the outside differs depending on the specifications, as mentioned above, a thick-film transistor usually is used [in the prior art] as the boosting capacitor element in order that the supply voltage supplied will not exceed the breakdown (or withstand) voltage of a thin-film transistor.... Accordingly, it is an object of the present invention to provide a supply voltage generating circuit of smaller chip area.”).

Claim 1 of the '701 Patent is representative, and recites:

1. A method for generating a supply voltage, comprising:

selecting one of a first input node supplied with a first power supply voltage and a second input node supplied with a second power supply voltage that is higher than the first power supply voltage;

coupling a selected one of the first and second input nodes to booster circuitry comprising of)booster stages to provide an output voltage, wherein selection of the first input node corresponds to a first number of booster stages and selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number; and

changing the booster circuitry from the first number of booster stages corresponding to selection of the first input node to the second number of booster stages when the second input node is selected.

III. Level of Ordinary Skill in the Art

The Petition proposes that a person of ordinary skill in the art in the field of the '701 Patent “would have a bachelor’s or the equivalent degree in electrical or computer engineering or a related field and 2-3 years of professional experience relating to circuit design.” Pet. 4. For purposes of this Preliminary Response only, Patent Owner does not challenge that definition.

IV. Claim Construction

The Petition states that “for purposes of this proceeding and the analysis presented herein, no claim term requires express construction.” Pet. 4. For purposes

of this Preliminary Response only, Patent Owner agrees that no express construction of any term is necessary.

V. The Petition’s Ground 1 fails.

The Petition provides a “kitchen sink” approach to motivations to combine Zhang with Javanifard, in proposing motivations that the Petition does not allege (much less show) would be applicable to the system the Petition proposes modifying.

Petitioner’s proposed “motivations” for the combination are addressed in turn; as explained below, none would have actually motivated a POSITA to combine Zhang with Javanifard in the manner alleged by the Petition.

First, the Petition alleges that a POSITA would be motivated to combine Zhang with Javanifard because “Zhang and Javanifard are analogous art to the ’701 Patent.” Pet. 20. But analogous art is a baseline *requirement* for an obviousness combination, not a factor weighing in favor of finding of a motivation to combine. *See In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004) (“*References within the statutory terms of 35 U.S.C. § 102 qualify as prior art for an obviousness determination only when analogous to the claimed invention.*”).¹

¹ All emphases herein are added unless otherwise specified.

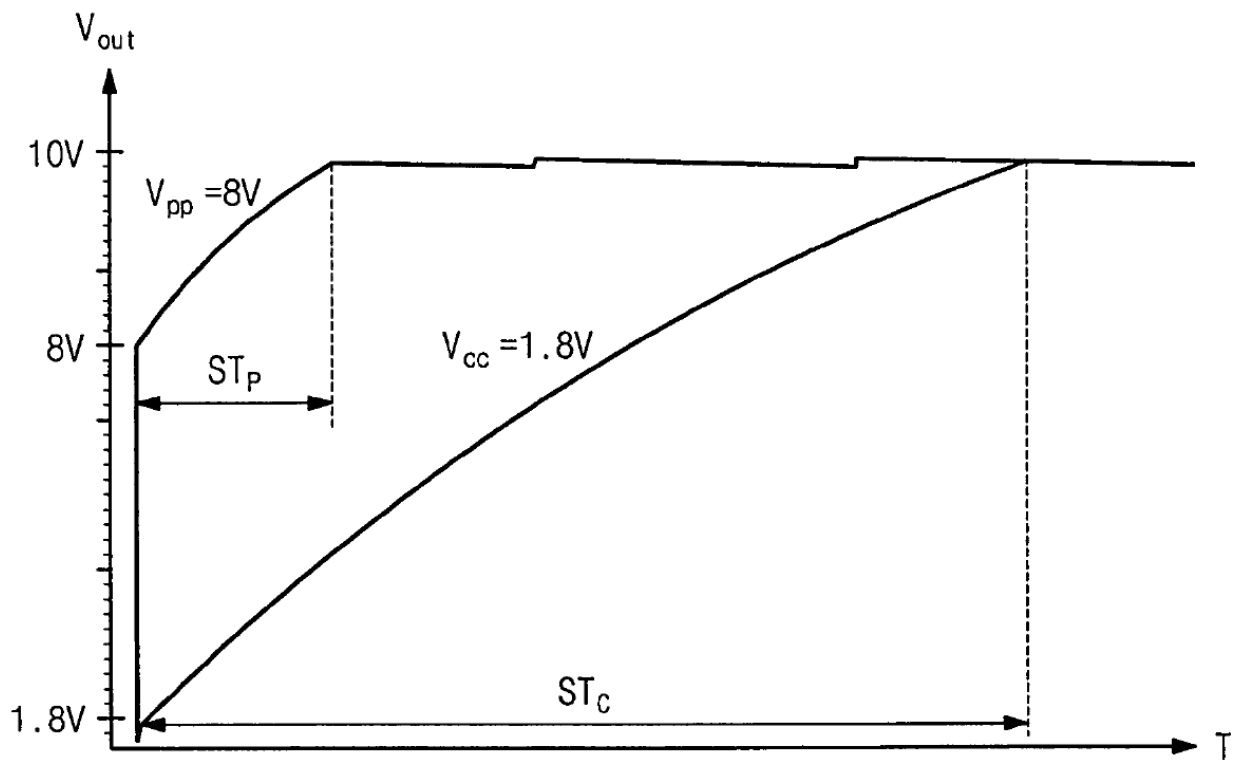
Second, the Petition states that “Javanifard explicitly provides motivations to apply its teachings of the variable stage charge pump to replace the fixed stage charge pump in Zhang’s charge pump system,” because it “addresses various disadvantages... of using the fixed stage charge pump.” Pet. 20 (citing Ex. 1006, 1:48-53, 1:66-2:2). But it is apparent from even a cursory review of Zhang and the cited portions of Javanifard that the “disadvantages” that Javanifard discusses do not apply to Zhang’s system.

In particular, Javanifard’s statements relate to “*prior art method[s] used to generate multiple higher voltage levels* from a single power supply voltage.” Ex. 1006, 1:48-53, 1:60-2:2. In contrast, Zhang is explicit, including in teachings relied on by the Petition itself, that Zhang does not “generate *multiple higher voltage levels* from a single power supply voltage,” but instead generates a *single* voltage level from a selection of two different power supply voltages.² For example, Zhang’s

² Zhang is also not a “prior art method” to Javanifard; the Javanifard reference claims priority to September 29, 1995 (Ex. 1006 at 1:3-4), whereas Zhang claims priority to July 10, 2003 (Ex. 1005 at cover). This is a still further reason why a POSITA would not view Javanifard’s statement of “disadvantages” of “prior art method[s] used to generate multiple higher voltage levels” as applying to Zhang’s system.

Figure 8 is reproduced below, and makes clear that the final output voltage level in Zhang's is the *same* (10V) regardless of what input voltage is applied.

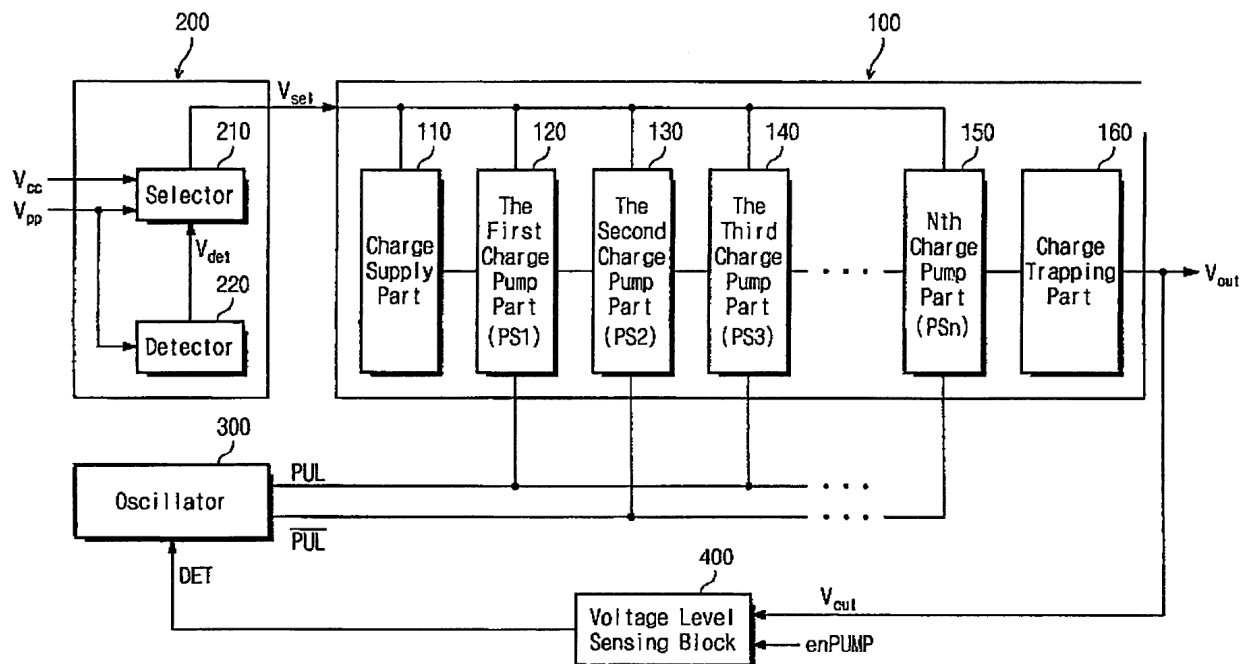
Fig. 8



Ex. 1005 at FIG. 8; *see also id.* at 6:1-11 (explaining that the same “wanted output voltage V_{out} can be obtained” from both “power voltage V_{CC} [of 1.8V] or external high voltage V_{PP} [of 8V],” just with different settling times ST_C and ST_P); Pet. 42-44 (explicitly relying on this disclosure of Zhang as being part of its Ground 1 combination).

Accordingly, the disadvantages recited by Javanifard are simply inapplicable to Zhang's teachings. This is apparent in evaluating the specific "disadvantages" in relationship to Zhang's FIG. 4 (reproduced below), which the Petition relies on as the basis for its combination. *See, e.g.*, Pet. 23, 25, 27.

Fig. 4



Ex. 1005, FIG. 4. Zhang's Figure 4 clearly discloses a *single* "charge pump block 100" with a fixed number of "N" stages, "all serially connected." *Id.* at 2:54-61.

According to Javanifard, one disadvantage attributable to the "prior art method[s]" include that "each charge pump circuit" (out of "a number of charge pump circuits") "requires a dedicated space in the integrated circuit." Ex. 1006, 1:51-53. In other words, Javanifard teaches that the use of multiple separate charge pump

circuits is problematic because adding multiple charge pump circuits to a system requires additional physical space. The Petition relies on this stated disadvantage as relating to “area usage.” *See* Pet. 20. But, as shown above, Zhang’s Figure 4 embodiment does not have that problem, because only a *single* charge pump circuit is required.

Similarly, Javanifard states another disadvantage to “prior art method[s]” is that due to the need to “us[e] voltage divider networks in conjunction with [a] single charge pump,” “power is wasted on the voltage divider networks.” Ex. 1006, 1:63-66. The Petition appears to rely on this stated disadvantage by paraphrasing it as “performance including pump efficiency.” *See* Pet. 20. But Zhang also clearly does not have this disadvantage either, because Zhang does not disclose the use of “voltage divider networks” to arrive at different output voltage levels. *See generally* Ex. 1005, FIG. 4 & associated text (no discussion or depiction of voltage dividers).³

³ The Petition also does not allege or show that Zhang suffers from the problem of “sacrific[ing] performance at one power supply voltage to accommodate another power supply voltage.” Pet. 20 (citing Ex. 1006, 1:66-2:2). Nor could the Petition have made such a showing, because Javanifard discusses “power supply voltage” as

Because the alleged disadvantages discussed in Javanifard are not present in Zhang, those “disadvantages” cannot provide a motivation to combine. *In re Schweickert*, 676 F. App’x 988, 994 (Fed. Cir. 2017) (finding no motivation to combine where the “record describes no problem in [the prior art] that would be resolved by the [proposed combination]”).

The Petition further alleges that “Javanifard achieves area reduction by using a single variable stage charge pump circuit to provide different output levels.” *See* Pet. 21 (discussing purported advantages to that approach). But critically, whether or not a POSITA would have viewed using “a single variable stage charge pump circuit to provide *different* output levels” as beneficial is *irrelevant* to the Petition’s

referring to a given *output* voltage, and Zhang’s system is configured to provide only a *single* output voltage. *See* Ex. 1005, FIG. 8 & associated text. Thus, because Zhang provides only one power supply voltage, Zhang does not “sacrific[e] performance at one power supply voltage to accommodate another power supply voltage” as described by Javanifard. *See* Ex. 1006, 1:66-2:2. Additionally, Javanifard’s discussion of that problem again relates to a method where “voltage levels are provided by using voltage divider networks” (*id.*, 1:60-2:2), which is not a technique used by Zhang’s system.

Ground 1 theory, which (like Zhang) involves providing only a *single* output level. See Pet. 36 (alleging that “it would have been obvious” to “generat[e] the same output voltage as the selection of the first input node with a lower input power voltage level,” and citing Zhang at FIG. 8 which discloses “providing the same output voltage level for different power supply input levels”); see also Pet. 42-44 (alleging that in the combination, the output voltage would be the same regardless of input voltage). Thus, because the Petition’s proposed combination does not involve “provid[ing] different output levels,” that cannot be a motivation to pursue the combination.

The Petition further states that “a POSIA [sic] would have been motivated to apply Javanifard’s teachings in Zhang to provide a multi-power source charge pump *to support a device having multiple operation modes*, including a device having ‘a test or general operation mode’ and devices having other operation modes (e.g., a memory device having different read, write, programming modes).” Pet. 22 (citing Javanifard’s at FIG. 2 as “illustrating variable stage charge pumps used for a multi-power-source memory device with different modes”). But the Petition does not explain how *its proposed combination* would achieve that result. See *id.* Specifically, the Petition’s combination is focused on applying the teachings of Javanifard’s *Figure 1* to Zhang, not the Figure 2 teachings that involve a “power supply circuitry for a flash memory” to accommodate different operational modes

such as “program,” “verify,” and “erase.” *See* Ex. 1006 at FIG. 2, 6:61-64, 8:1-23 (Javanifard’s tables 2 and 3, showing the use of different operational modes in the Figure 2 embodiment); Pet. 22 (citing only Javanifard’s Figure 2 as illustrating the ability to “support a device having multiple operation modes”). The Petition does not explain how any of the benefits of Javanifard’s Figure 2 (such as supporting multiple operation modes) would be realized by its proposed combination, because the Petition does not allege that Zhang would be modified to incorporate the teachings of Javanifard’s Figure 2. *See generally* Pet. 23-61.⁴ In short, the Petition cannot rely on benefits of features of Javanifard’s Figure 2 as motivating its proposed combination, when the proposed combination is not alleged to include any of those allegedly beneficial features of Javanifard’s Figure 2.

Finally, the Petition alleges that “applying Javanifard’s teachings in embodiments of Zhang would have been no more than the combination of known elements according to known methods (e.g., incorporating a charge pump circuit

⁴ For its Claim 8 analysis, the Petition refers in passing to Javanifard’s Figure 2, but it is only in the context of explaining that the term “VPP” has a known meaning in the art, not in alleging that Javanifard’s Figure 2 would somehow be combined with Zhang. *See* Pet. 54-55.

design in a multi-power source charge pump system according to known IC design) obvious to a POSITA. Pet. 22-23. But this is simply a high-level summary statement of what the combination is, accompanied by attorney argument that the combination would be done “according to known methods.” *Id.* Notably, the Petition does not provide **any** evidentiary support for this allegation. *See* Pet. 22-23 (no citations in support of the Petition’s allegations in this regard). This is unsurprising, as the Petition seems to imply that the entire field of “IC design” encompasses a “known method[.]” *Id.* at 22.

Furthermore, even assuming the Petition’s conclusory allegation that the combination—which requires not a simple substitution of elements, but a complete reworking of various functionality within Zhang⁵—is simply a combination of

⁵ For example, Zhang’s Figure 4 includes a charge pump block 100, selection block 200, Oscillator 300, and Voltage Level Sensing Block 400. *See* Ex. 1005, FIG. 4. The Petition’s combination not only replaces Zhang’s charge pump block 100 with a different type of charge pump from Javanifard (without any coherent motivation to do so), but also eliminates Zhang’s Oscillator 300 and Voltage Level Sensing Block 400 without explanation. *See* Pet. 30-31 (providing examples A and B of a

known elements, that is insufficient to establish obviousness. Rather it is “important to identify a *reason* that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does,” “because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418–19 (2007). Therefore, “obviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.” *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (emphases in original). As explained in detail above, the Petition’s purported “motivations” to combine Zhang with Javanifard in the proposed manner ring hollow because they are inconsistent with the teachings of Zhang, Javanifard, and even the Petition’s own combination. Thus, there is no evidence that a POSITA would have been motivated to make the proposed combination.

combination of Zhang with Javanifard, both of which eliminate the circuit blocks 300 and 400 of Zhang’s FIG. 4).

Accordingly, the Petition does not demonstrate a reasonable likelihood of prevailing with respect to Ground 1.

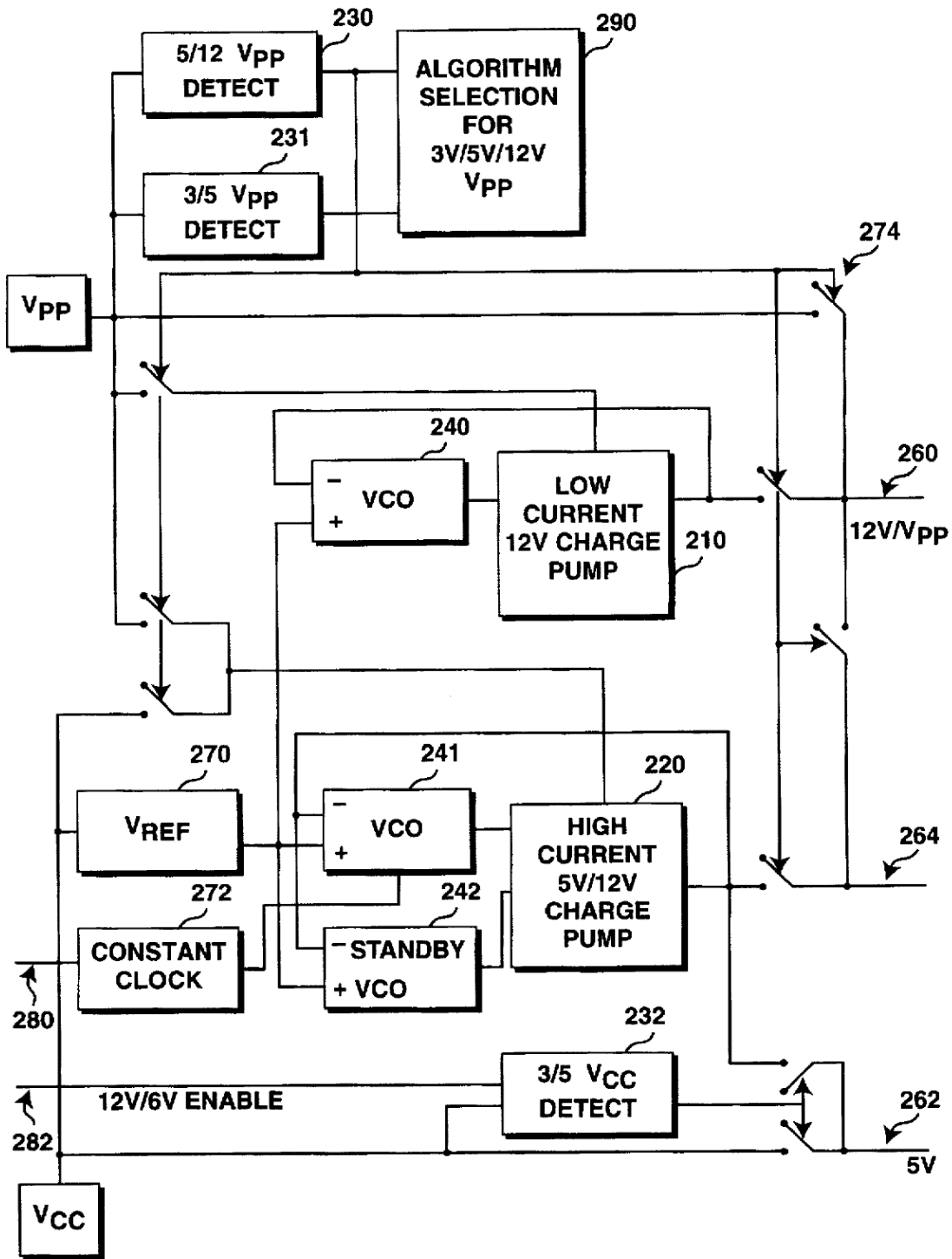
VI. The Petition's Ground 2 fails.

The Petition's Ground 2 presents a single-reference obviousness allegation. Typical single-reference obviousness theories involve a relatively straightforward modification or obvious variant to an embodiment of the reference at issue. *See, e.g., Boston Scientific Scimed, Inc. v. Cordis Corp.*, 554 F. 3d 982, 991 (Fed. Cir. 2009) (cited by Pet. 62) ("Just as the stent in figure 3B benefits from the two layers, one containing a drug and the other limiting diffusion of the drug, so would the stent in figure 4 benefit from the same two coating layers."). Not so here: the Petition proposes extensive modifications to Javanifard's Figure 2 embodiment that a POSITA would not have contemplated in light of Javanifard's own disclosures, and in a way that would render that embodiment inoperable for its intended purpose because it would remove what Javanifard itself describes as mandatory functionality of that embodiment. *See Plas-Pak Indus., Inc. v. Sulzer Mixpac AG*, 600 F. App'x 755, 760 (Fed. Cir. 2015) (affirming the Board's finding that a combination of references would render the reference "'inoperable for its intended purpose,' and a person of ordinary skill would thus not have been motivated to pursue the combination"). Furthermore, the Petition's combination does not identify any

advantage or benefit of its proposed modification that was not *already* present in Javanifard's Figure 2, without modification.

A. Overview of the Petition's Proposed Modification to Javanifard's Figure 2

By way of background, Javanifard's Figure 2 (reproduced below) "illustrates the power supply circuitry for a flash memory including variable stage charge pumps for accommodating a 5 volt, 9 volt, and 12 volt voltage level from either a 3.3 volt or 5 volt power supply." Ex. 1006, 6:61-64.



Id., FIG. 2. Javanifard's Figure 2 involves a moderately complex arrangement of detection circuitry, algorithm selection circuitry, and a combination of two distinct

variable-stage charge pumps configured to provide a variety of output voltages with different current requirements. *See id.* at 7:11-20 (explaining the charge pumps are configured to provide 5 volt, 9 volt, and 12 volt outputs according to variations in V_{pp} as well as “the mode of operation of the flash memory”); *id.* at 7:27-32 (making clear that both charge pump 210 and charge pump 220 are “[v]ariable stage charge pump[s]” that provide either “high current” or “low current” depending on the mode of operation of the flash memory, i.e., “read, program, and erase operations”).

Not only is Javanifard’s Figure 2 system capable of providing three separate output voltages at two different current levels in three operational modes, but it is able to do so while accommodating any combination of V_{cc} and V_{pp} where V_{cc} is 3.3 volts or 5 volts, and V_{pp} is 3.3 volts, 5 volts, or 12 volts (as detected by “[l]evel detectors 230, 231, and 232”). *See id.* at 7:23-24; 7:35-36 (“These algorithms may vary depending upon V_{pp} and V_{cc} .”); *id.* at 7:24:24-26 (“5/12 volt V_{pp} detector 230 is used to determine whether V_{pp} is at 5 volts or 12 volts.”); *id.* at 7:62-65 (“The high current and the low current variable stage charge pumps are reconfigured depending upon the operational mode and the nominally detected values of V_{pp} (i.e., 3.3 or 5 volts.”); *id.*, FIG. 2 & 8:35-44 (illustrating block 232 to detect whether V_{cc} is closer to 3 volts or 5 volts, and explaining how the system responds depending on the detected voltage level).

Although Javanifard's Figure 2 does not itself disclose the circuit structure of its variable stage charge pumps, Javanifard's Figures 1 and 3 both teach examples of how those charge pumps could be implemented. *See* Ex. 1006 at 2:42-43 ("FIG. 1 illustrates one embodiment of a variable stage charge pump."); *id.* at 5:3-5 ("FIG. 3, for example, illustrates a variable stage charge pump with 12 rungs coupled to a flash memory array 390."). Thus, a POSITA reviewing Javanifard would have understood that Javanifard's variable-stage charge pumps 210 and 220 of Figure 2 would be implemented using the structures of Javanifard's Figure 1 and/or Figure 3, as that is the clear implication of the Javanifard reference itself.

As straightforward as the above understanding is, that is ***not*** the combination proposed in the Petition's Ground 2 theory of invalidity. Rather, the Petition proposes removing ***nearly all*** of the functionality of Javanifard's Figure 2, and replacing that functionality with a ***single*** variable-stage charge pump according to Javanifard's Figure 1 or Figure 3. The Petition's proposed combination of Javanifard's Figure 2 with Figure 1 is reproduced below, with the Petition's annotations.

*selecting one of a first input
node...and a second input node*

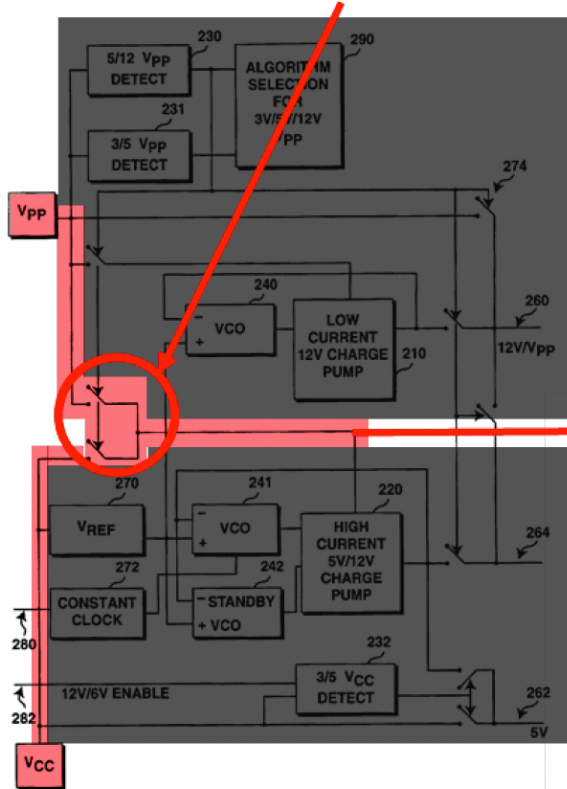


Figure 2

*booster
circuitry*

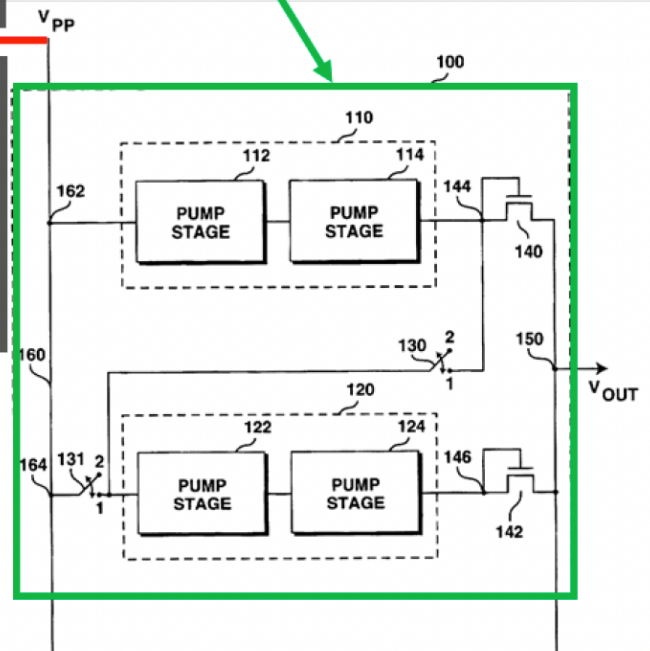


Figure 1

Example C (Embodiments 1 and 2 of Javanifard Combined)

Pet. 71. As can be readily seen from the diagram above, nearly *all* of the components from Javanifard's Figure 2 (other than circuitry to select between Vcc and Vpp) have

been removed, including Figure 2's *two* separate variable-stage charge pumps 210 and 220, and in their place only a single variable-stage charge pump has been added.

There is no apparent reason (other than Petitioner's motivation to allege invalidity of the challenged claims) as to why the Petition proposes *this* modification to Javanifard's Figure 2, rather than what Javanifard clearly intended would be done, which is to leave the functionality of Figure 2 in place, and simply implement the variable-stage charge pumps 210 and 220 using Javanifard's teachings from Figure 1 and/or Figure 3. Even *assuming* the Petition's proposed combination might have some benefits (as explained below, the Petition has provided no evidence of that), the Petition's combination is so far afield from what Javanifard actually teaches and implies that there is no reason to believe a POSITA would have ever thought to make that combination in the first place.

B. The Petition provides no coherent motivation for a POSITA to have made its arbitrary proposed modification to Javanifard's Figure 2 embodiment.

As summarized in the preceding section, Javanifard's Figure 2 embodiment discloses "the power supply circuitry for a flash memory" capable of providing a variety of different output voltages at different current requirements according to a variety of different operating modes, all while accommodating variation in both Vcc and Vpp input voltage levels. Javanifard clearly teaches that this level of flexibility is important "[t]o maximize the utility of a flash memory system." Ex. 1006, 6:61-

64; *id.*, 6:12-17 (“Different voltage requirements are needed by the flash memory cells for the different operational modes” which “include reading, programming, and erasing.”). Indeed, Javanifard is explicit that the ability to handle three different output voltages in response to variation in input voltage is a **mandatory** aspect of its system. *Id.*, 6:56-60 (“To maximize the utility of a flash memory system... the variable stage charge pump **must** be able to generate approximately 5 volts, 9 volts, and 12 volts from either a 3.3 volt or 5 volt power supply.”). The Petition, in its Ground 1 analysis, acknowledges that these features of Javanifard’s Figure 2 embodiment would have been recognized as beneficial by a POSITA. *See* Pet. 22 (alleging that a POSITA would have been motivated to look to Javanifard, as the Figure 2 embodiment supports “other operation modes (e.g., a memory device having different read, write, programming modes)”).⁶

The Petition’s proposed combination would gut these core features and benefits of Javanifard’s Figure 2 embodiment. The Petition’s Ground 2 never

⁶ As explained above in Section V, the Petition’s reliance on Javanifard’s Figure 2 embodiment as providing a motivation to make the Ground 1 combination is misplaced, because the Petition’s Ground 1 combination does not involve Javanifard’s Figure 2 embodiment.

provides any allegation that in its proposed combination, the output voltage would be configured to vary at all, much less to provide three separate output levels from two different input voltages, as Javanifard teaches its system “must be able to” do. Ex. 1006, 6:56-60 (“To maximize the utility of a flash memory system... the variable stage charge pump ***must be able to generate approximately 5 volts, 9 volts, and 12 volts from either a 3.3 volt or 5 volt power supply.***”). And the Petition alleges that its combination would satisfy claim 2 of the ’701 Patent, wherein the “output voltage is the ***same*** when the first input node is selected and when the second input node is selected” (see Pet. 81; Ex. 1001, Claim 2), further emphasizing that the Petition’s combination would be configured to provide only a ***single*** level of voltage output, not the three levels Javanifard teaches are necessary. When a substitution such as the Petition’s would “defeat[] the purpose of” the system being modified, that “substitution is illogical” and cannot provide the basis for an obviousness determination. *In re Schweickert*, 676 F. App’x 988, 994 (Fed. Cir. 2017); see also *Plas-Pak*, 600 F. App’x at 760 (affirming the Board’s finding that a combination of references would render the reference “‘inoperable for its intended purpose,’ and a person of ordinary skill would thus not have been motivated to pursue the combination”).

Nor does the Petition provide any explanation as to how its modification would allow for selectable operational modes including “reading, programming, and

erasing,” (Ex. 1006, 6:14-17, 7:17-20), or how it would accommodate variation in the voltage levels of Vcc and Vpp themselves (rather than simply accommodating selection between Vcc and Vpp as the Petition proposes). *See* Ex. 1006, 7:23-24; 7:35-36 (“These algorithms may vary depending upon Vpp and Vcc.”); *id.*, 7:24:24-26 (“5/12 volt Vpp detector 230 is used to determine whether Vpp is at 5 volts or 12 volts.”); *id.*, 7:62-65 (“The high current and the low current variable stage charge pumps are reconfigured depending upon the operational mode and the nominally detected values of Vpp (i.e., 3.3 or 5 volts.”); *id.*, FIG. 2 & 8:35-44 (illustrating block 232 to detect whether Vcc is closer to 3 volts or 5 volts, and explaining how the system responds depending on the detected voltage level).

The Petition’s Ground 2 entirely ignores Javanifard’s discussion of these benefits of the functionality that would be removed under the Petition’s combination. Instead, for its purported motivation to modify Javanifard, the Petition focuses on a single sentence in the summary of the invention: that an “object is to provide a charge pump that can accommodate a given output level for different charge pump power supply input levels.” Ex. 1006, 2:22-24 (quoted by Pet. 64).

But the Petition fails to either recognize or acknowledge that Javanifard *already* accommodates a given output level for different charge pump power supply input levels. In particular, Javanifard’s Figure 2 is able to choose between any one of “a 5 volt, 9 volt, or 12 volt level” output “from either a 3.3 volt or 5 volt power

supply.” Ex. 1006 at 6:56-64. Thus, Javanifard’s system is clearly able to maintain “a given output level” (e.g., 9 volts) “for different charge pump power supply input levels” (e.g., 3.3 or 5 volt power supplies). Accordingly, the Petition alleges no problem in Javanifard that would be resolved by the Petition’s proposed modification, and the purported goal of “accommodate[ing] a given output level for different charge pump power supply input levels” therefore cannot motivate the Petition’s complete rearchitecting of Javanifard’s Figure 2. *See Schweickert*, 676 F. App’x at 995-96 (finding no motivation to pursue a modification where the “record describes no problem in [the prior art] that would be resolved by the [proposed modification]”).

The Petition also alleges that its combination involving the gutting of Javanifard’s core functionality would “produce the obvious, beneficial, and predictable results of a multi-power-source variable stage charge pump system.” Pet. 63-64. But again, Javanifard *already* discloses a multi-power source system that makes use of variable stage charge pumps, and discloses far *more* functionality and

flexibility than the Petition’s proposed modification.⁷ It appears that in their quest to invalidate the ’701 Patent, Petitioner and its expert neglected to place themselves in the shoes of a POSITA as of the ’701 Patent’s priority; and such a POSITA certainly would not seek to achieve a result that was ***already taught*** by Javanifard’s Figure 2 embodiment by abandoning other core functionality and benefits of that embodiment. *See Adidas AG v. Nike, Inc.*, 963 F.3d 1355, 1359 (Fed. Cir. 2020) (affirming PTAB’s decision not finding obviousness where a proposed modification would “change the principles under which [the prior art] operates”); *Schweickert*, 676 F. App’x at 995-96.

As noted above in Section VI.A, a much less contrived combination of Javanifard’s Figure 1 charge pump with Javanifard’s Figure 2 power supply system would simply involve implementing Javanifard’s “low current 12V charge pump” 210 and “high current 5V/12V charge pump” 220 using the variable stage charge

⁷ The same is true of the extremely straightforward combination of using Javanifard’s Figures 1 or 3 to implement the variable stage charge pumps 210, 220, because that combination would not involve modifying any functionality of Figure 2, but would instead simply rely on Figures 1 and 3 for implementation details regarding the Figure 2 variable-stage charge pumps.

pump described in Figure 1. This makes logical sense, and is likely what Javanifard himself had in mind, because “FIG. 1 illustrates one embodiment of a variable stage charge pump,” “FIG. 2 illustrates circuitry including variable stage charge pumps for supplying power to a flash memory array” (Ex. 1006, 2:34-37). This straightforward and commonsense combination, unlike the extensive modification proposed by the Petition’s invalidity theory, would have all of the benefits of Javanifard’s Figure 2. The Petition does not present that commonsense combination, however, because such a combination would not read on the challenged claims of the ’701 Patent.⁸

⁸ Because the Petition does not even allege that the straightforward combination of using the teachings of the variable charge pump circuit of Javanifard’s Figure 1 to implement the variable charge pump circuits 210, 220 in Javanifard’s Figure 2 system would render obvious any challenged claim, Patent Owner need not distinguish that combination here. However, for purposes of clarity, as one exemplary reason why that combination would not arrive at the challenged claims, Javanifard only teaches that Vcc would act as an input to any charge pump in exactly *one* scenario: when Vpp is set to zero volts during a read mode. *See* Ex. 1006, 8:32-

Finally, the Petition alleges that “[a]pplying Javanifard’s teaching of selection from multiple power sources of Embodiment 2 to the variable stage charge pump of Embodiments 1 or 3 would have been no more than the combination of known elements according to known methods (e.g., incorporating a power source selection design in a variable stage charge pump according to well-known IC design techniques including voltage detection and selection) obvious to a POSITA, which does no more than yield predictable results.” Pet. 64-65. This allegation, however, assumes, without any explanation, that the removal of large swaths of functionality

35 (“During a read operation V_{pp} might be zero. Therefore, if high current charge pump 220 is needed it will receive its power from V_{cc} instead of V_{pp} during the read mode.”). Thus, whenever the input node corresponding to V_{cc} is selected, V_{cc} would necessarily be the higher “second power supply voltage” of limitation [1.1] and V_{pp} (of zero volts) would be the lower “first power supply voltage” of limitation [1.1]. But if and when the zero-volt supply of V_{pp} were selected, there would be no reason to select “a first [higher] number of booster stages” as required by limitations [1.2.2] and [1.2.3] for a zero-volt input, because a zero-volt input will always result in a zero volt output from a charge pump circuit regardless of the number of booster stages.

from Javanifard's Figure 2 is simply a "combination of known elements." *Id.* And the Petition provides no explanation as to why a POSITA would be motivated to implement the alleged "combination of known elements according to known methods," when the Petition's proposal is contradictory with Javanifard's teachings that its "flash memory system... **must** be able to generate approximately 5 volts, 9 volts, and 12 volts from either a 3.3 volt or 5 volt power supply." Ex. 1006, 6:56-60; *Plas-Pak*, 600 F. App'x at 760 (affirming the Board's finding that a combination of references would render the reference "'inoperable for its intended purpose,' and a person of ordinary skill would thus not have been motivated to pursue the combination"); *see also Adidas*, 963 F.3d at 1359 (affirming the Board's decision not finding obviousness where a proposed modification would "change the principles under which [the prior art] operates").

Ultimately, the Petition's proposed modification to Javanifard in a way that neither Javanifard nor the Petition provides any coherent motivation to pursue is strongly suggestive of improper hindsight reasoning. *See KSR*, 550 U.S. at 421 ("A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning."). And the fact that the Petition may, with the benefit of hindsight, cobble together a combination of known elements that might, when arranged in a specific way, teach the invention, is not evidence of obviousness, "because inventions in most, if not all, instances rely

upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.” *Id.* at 418–19; *Cheese Sys., Inc. v. Tetra Pak Cheese & Powder Sys., Inc.*, 725 F.3d 1341, 1352 (Fed. Cir. 2013) (“Obviousness ‘cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention.’”) (quoting *ATD Corp. v. Lydall, Inc.*, 159 F.3d 534, 546 (Fed. Cir. 1998)). “[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention” (*Belden*, 805 F.3d at 1073 (Fed. Cir. 2015) (emphases in original)) and the Petition ultimately provides no coherent reason why a POSITA *would have been motivated to make* the specific modifications to Javanifard it alleges.

Accordingly, the Petition does not demonstrate a reasonable likelihood of prevailing with respect to Ground 2.

VII. The Petition’s Grounds 3-4 also fail.

The Petition is explicit that the “analysis for Grounds 3 and 4 rel[ies] on the analysis and evidence as provided for Ground 1 (Zhang and Javanifard) and Ground 2 (Javanifard), respectively.” Pet. 87. Thus, the theories presented in Grounds 3 and 4 fail for at least the same reasons applicable to Grounds 1 and 2.

VIII. Conclusion

Because the Petition fails to provide evidence that a POSITA would have been motivated to make the modifications to the prior art on which the Petition's invalidity theories rely, institution should be denied.

Date: October 25, 2023

Respectfully submitted,
/ James A. Milkey /
James A. Milkey, Reg. No. 79,503
Russ, August & Kabat
12424 Wilshire Blvd., 12th Floor
Los Angeles, CA 90025

Counsel for Patent Owner

CERTIFICATION REGARDING WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner certifies that there are 5,885 words in the paper excluding the portions exempted under 37 C.F.R. §42.24(a)(1).

Date: October 25, 2023

Respectfully submitted,
/ James A. Milkey /
James A. Milkey, Reg. No. 79,503
Russ, August & Kabat
12424 Wilshire Blvd., 12th Floor
Los Angeles, CA 90025

Attorney for Patent Owner

CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e)(1))

The undersigned hereby certifies that the above document was served on October 25, 2023, by filing this document through the Patent Trial and Appeal Case Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

David O'Dell
Hong Shi
david.odell.ipr@haynesboone.com
hong.shi.ipr@haynesboone.com
HAYNES AND BOONE, LLP

Date: October 25, 2023

/ James A. Milkey /

RUSS AUGUST & KABAT
12424 Wilshire Blvd., 12th Fl.
Los Angeles, CA 90025
(310) 826-7474

James A. Milkey, Reg. No. 79,503
Reg. No. 79,503
Attorney for Patent Owner