

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.
Petitioner,

v.

LONGITUDE LICENSING LTD.,
Patent Owner.

IPR2023-01230
Patent 9,207,701 B2

Before RICHARD M. LEBOVITZ, DAVID C. McKONE, and
KEVIN C. TROCK, *Administrative Patent Judges*.

LEBOVITZ, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Western Digital Technologies, Inc. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–18 of U.S. Patent No. 9,207,701 B2 (“the ’701 Patent”) on July 20, 2023. Paper 2 (“Pet.”); Paper 3 (filing date accorded).

Longitude Licensing LTD (“Patent Owner”) filed a Preliminary Response to the Petition on October 25, 2023. Paper 6 (“Prelim. Resp.”).

Under 37 C.F.R. § 42.4(a), we have authority to determine whether to institute an *inter partes* review. An *inter partes* review may be instituted only if “the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). The following findings of fact and conclusions of law are not final, but are made for the sole purpose of determining whether Petitioner meets the threshold for initiating review. Any final decision shall be based on the full trial record, including any response timely filed by Patent Owner. Any arguments not raised by Patent Owner in a timely filed response may be deemed waived.

For the reasons below, we determine that Petitioner has established a reasonable likelihood that it would prevail in showing that at least one of the claims challenged in the petition is unpatentable. *See* 37 C.F.R. § 42.108(c) (2023). Accordingly, we institute an *inter partes* review of the challenged claims on all grounds raised in the Petition.

B. *Real Parties in Interest*

Petitioner identifies the real party in interest as Western Digital Technologies, Inc. (“Petitioner”). Pet. 93.

Patent Owner identifies Longitude Licensing LTD, as the real party in interest. Paper 4 (Patent Owner Mandatory Notices), 2.

C. Related Matters

Patent Owner identifies the following civil actions that “may affect, or be affected by, a decision in this proceeding.” (Paper 4):

Longitude Licensing Limited v. ASUSTeK Computer Inc., Case 8-23-cv-00033 (C.D. Cal.); *Longitude Licensing Limited v. Lenovo Group Limited*, Case 8-23-cv-00035 (C.D. Cal.); *Longitude Licensing Limited v. Acer Inc.*, Case 8-23-cv-00036 (C.D. Cal.); *Longitude Licensing Limited v. HP Inc.*, Case 8-23-cv-00038 (C.D. Cal.); and *Longitude Licensing Limited v. Amazon.com, Inc.*, Case 8-23-cv-00039 (C.D. Cal.); *Longitude Licensing Limited v. Dell Technologies Inc.*, Case 8-22-cv-02312 (C.D. Cal.).

Petitioner intervened in the *Amazon* litigation listed above and the District Court stayed the six litigations pending the resolution of Patent Owner’s infringement claims with respect to Petitioner’s accused devices in the *Amazon* litigation. Ex. 1011, 4.

D. The ’701 Patent

The ’701 patent is titled “Supply Voltage Generating Circuit.” Ex. 1001, code (54). The patent issued on December 8, 2015. *Id.* at code (45). The ’701 patent claims U.S. priority back to a U.S. application filed March 20, 2008 and foreign priority to a Japanese application filed March 27, 2007. *Id.* at codes (21), (22), (63), (30).

The ’701 patent describes “a supply voltage generating circuit . . . for generating a boosted voltage within a semiconductor storage device.” Ex. 1001, 1:16–19.

The ’701 patent discloses that different supply voltages may be required from an externally applied power source. Ex. 1001, 1:23–28. An

example disclosed in the '701 patent in which different supply voltages may be needed is for dynamic random-access memory (DRAM). *Id.* To address this need, the '701 patent discloses a “supply voltage generating circuit” which comprises “a booster that outputs a boosted voltage upon generating the boosted voltage by charge pumping of a capacitor element.” *Id.* at 2:29–31. The booster (also known as a “booster circuit” or “charge pump circuit”) provides internally-generated supply voltages that are higher than the input power supply voltages. Ex. 1003¹ ¶ 42.

Figure 1 of the '701 patent shows the circuitry for generating supply voltage VPP. Figure 1 is reproduced below:

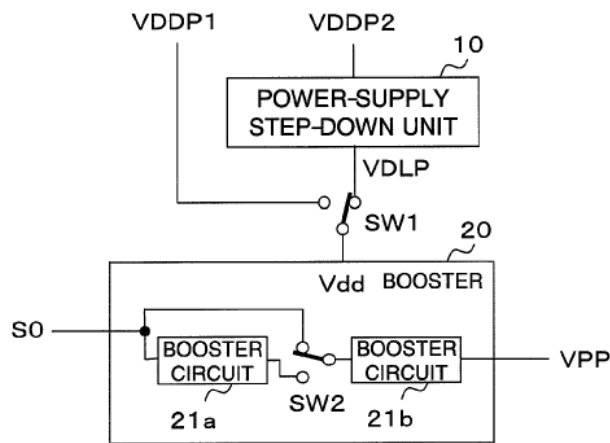


Figure 1 is a block diagram illustrating the configuration of an exemplary “supply voltage generating circuit” of the '701 patent. Ex. 1001, 3:63–65. The figure shows two voltage sources (VDDP1 and VDDP2), booster 20 for generating a boosted voltage by charge pumping (Ex. 1001, Abstract, 2:28–

¹ Petitioner relies on the Declaration of Harvey J. Stiegler, Ph.D. (Ex. 1003, “Stiegler Declaration” or “Stiegler Decl.”). Dr. Ziegler states that he has “over 25 years of industry experience in the semiconductor industry serving in IC design, design management, and technology development.” Ex. 1003 ¶ 6. In 1989, Dr. Stiegler obtained a Ph.D. in Electrical and Computer Engineering from Rice University. *Id.* ¶ 17.

31; 4:1–3), and driving signal S0. Switch element SW1 switches between VDDP1 and the step-down voltage VDLP (from VDDP2). Ex. 1001, 4:54–59. Switch element SW1 supplies voltage to booster 20. The booster 20 includes a second switch SW2 for “switching between the booster circuits 21a and 21b.” *Id.* at 4:60–64. The booster 20 includes a pre-stage booster circuit 21a, a post-stage booster circuit 21b, and a switch element SW2 for switching between the booster circuits 21a and 21b. *Id.* at 4:60–63. The booster 20 generates a boosted voltage from VDDP1 or VDLP “by charge pumping of the capacitor elements using a driving signal S0,” which “supplies the boosted voltage to a load circuit, an example of which is a circuit for driving a word line, as power supply VPP.” *Id.* at 4:63–67.

The ’701 patent further discloses selecting first and second nodes associated with different power supplies (e.g., VDDP1, VDLP) of the supply voltage generating circuit:

The switch element SW2 is switched to the first boosted signal when the switch element SW1 has been switched to the external power supply VDDP1, and the switch element SW2 is switched to the second boosted signal when the switch element SW1 has been switched to the output (VDLP) of the power-supply step-down unit 10.

Ex. 1001, 5:14–19.

The ’701 patent discloses that “the booster 20 is so adapted that the number of booster stages (e.g., one stage or two stages) constituted by the multiple booster circuits 21a, 21b is changed over by a switch element SW2 in accordance with the power-supply voltage [VDDP1, VDLP] applied to the booster 20.” Ex. 1001, 4:24–28.

In accordance with this supply voltage generating circuit, the ’701 patent teaches that the number of booster stages (e.g., 21a, 21b) can be

“changed over to the most efficient number depending upon the level of the external voltage.” Ex. 1001, 9:43–50. Depending on the specified VPP voltage (e.g., 2.5V) and the externally supplied voltage (e.g., 1.2V or 1.5V), a one- or two-booster stage circuit may be necessary. *Id.* at 9:51–60. The ’701 patent teaches that “[t]he smaller the number of stages, the better the efficiency at which VPP is supplied with power.” *Id.* at 9:58–60. To sum up, the number of booster stages that may be used to provide the supply voltage VPP may be varied, making the circuit a variable booster circuit.

With respect to the ’701 patent disclosure, Petitioner’s declarant, Harvey Stiegler, Ph.D., testifies that “[i]n conventional semiconductor storage devices, such as flash or EEPROM [electrically erasable programmable read-only memory], there will be one or more power supply voltages.” Ex. 1003 ¶ 42. “For example, a first power supply voltage (VDD1) of 5V can be used for one section of the device, and a second power supply voltage (VDD2) of 3.3V can be used in another section of the device.” *Id.* Dr. Stiegler further explains that “semiconductor storage devices may periodically require additional, often higher, internally-generated supply voltages, such as 7V, to perform operations such as a memory erase.” *Id.* Dr. Stiegler testifies that the internal voltages, or pump voltages (“VPP”), “are produced by a booster circuit, also called a charge pump circuit.” *Id.*

E. Challenged Claims

Petitioner challenges the patentability of claims 1–18 (“Challenged Claims”) of the ’701 patent, which are all the claims of the patent. Pet. 1. Claims 1 and 10, the challenged independent claims, are reproduced below as annotated by Petitioner with bracketed numbers:

[1.0] 1. A method for generating a supply voltage,
comprising:

[1.1] selecting one of a first input node supplied with a first power supply voltage and a second input node supplied with a second power supply voltage that is higher than the first power supply voltage;

[1.2.1] coupling a selected one of the first and second input nodes to booster circuitry comprising a plurality of booster stages to provide an output voltage,

[1.2.2] wherein selection of the first input node corresponds to a first number of booster stages and

[1.2.3] selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number; and

[1.3] changing the booster circuitry from the first number of booster stages corresponding to selection of the first input node to the second number of booster stages when the second input node is selected.

[10.0] 10. A semiconductor device comprising:

[10.1] a first input node supplied with a first power supply voltage;

[10.2] a second input node supplied with a second power supply voltage higher than the first power supply voltage;

[10.3] booster circuitry comprising a plurality of booster stages to provide an output voltage; and

[10.4] a first switch configured to couple a selected one of the first input node and the second input node to the booster circuitry,

[10.5] wherein the booster circuitry configured to have a first number of booster stages when the first input node is selected and to be changed to a second number of booster stages when the second input node is selected, the second number being less than the first number.

F. Prior Art and Asserted Grounds

Petitioner raises the following grounds of unpatentability with respect to the challenged claims (Pet. 2):

Claims Challenged	35 U.S.C. § ²	Reference(s)
1–18	103(a)	Zhang, ³ Javanifard ⁴
1–18	103(a)	Javanifard
9, 18	103(a)	Zhang, Javanifard, Kang ⁵
9, 18	103(a)	Javanifard, Kang

Petitioner asserts that Zhang is prior art under at least §§ 102(a), 102(b), and 102(e), and Javanifard under at least §§ 102(a) and 102(b). *Id.*

Petitioner asserts that Kang was published, indexed, and publicly accessible as of at least December 31, 2006, and is prior art under at least §102(a). *Id.* (citing Ex. 1024 ¶ 46; Ex. 1003 ¶¶ 83–85).

At this stage of the proceeding, Patent Owner does not dispute that each reference qualifies as prior art. *See* Prelim. Resp. 1–3 (summarizing Petitioner’s proposed patentability challenges, but providing no arguments at this time that the challenges are deficient because the cited publications are not prior art to the challenged claims).

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. We apply the pre-AIA version of 35 U.S.C. § 103 because it appears the claims at issue have an effective filing date prior to March 16, 2013, the effective date of the AIA. *See* Ex. 1001, codes (22), (60).

³ Zhang et al., U.S. Pat. 7,427,888 B2, issued September 23, 2008, was filed July 8, 2004, and claims foreign priority to July 10, 2003. Ex. 1005, codes (45), (22), (30).

⁴ Javanifard et al., U.S. Pat. 5,767,735, issued June 16, 1998, and claims priority back to September 29, 1995. Ex. 1006, codes (45), (22), (62).

⁵ Kang et al., “Charge Pump Circuits with Low Area and High Power Efficiency for Memory Applications,” *J. Semiconductor Tech. Sci.*, 6(4):257–63 (2006).

II. ANALYSIS

A. *Legal Standards*

“In an [*inter partes* review], the Petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–1327 (Fed. Cir. 2008)) (discussing the burden of proof in *inter partes* review). Furthermore, Petitioner must explain with particularity how the prior art would have rendered the challenged claims unpatentable. 35 U.S.C. § 312(a)(3); 37 C.F.R. § 42.104(b)(4) (“The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon.”).

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The obviousness inquiry requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)). Petitioner cannot satisfy its burden of proving obviousness by employing “mere

conclusory statements,” but “must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art at the time of the alleged invention “would have a bachelor’s or the equivalent degree in electrical or computer engineering or a related field, and 2–3 years of professional experience relating to circuit design.” Pet. 4 (citing Ex. 1003 ¶ 58. Petitioner further states “a person with less formal education but more experience, or more formal education but less experience, could have also met the relevant standard for POSITA” [person of ordinary skill in the art]. *Id.* Petitioner states that “a person having an extraordinary level of skill should” not be regarded as POSITA. *Id.*

Patent Owner, for purposes of this Preliminary Response only, does not dispute Petitioner’s definition a person of ordinary skill in the art. Prelim. Resp. 4. Based on the current record, we adopt Petitioner’s definition of the level of skill of one person of ordinary skill in the art at the time of the invention.

C. Claim Construction

We construe claim terms “using the same claim construction standard” that district courts use to construe claim terms in civil actions under 35 U.S.C. § 282(b). *See* 37 C.F.R. § 42.100(b). Under that standard, claim terms “are given their ordinary and customary meaning, which is the meaning the term would have to a person of ordinary skill in the art at the time of the invention.” *Power Integrations, Inc. v. Fairchild Semiconductor Int’l, Inc.*, 904 F.3d 965, 971 (Fed. Cir. 2018) (citing *Phillips v. AWH Corp.*,

415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc)). The meaning of claim terms may be determined by “look[ing] principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner states that “for the purposes of this proceeding and the analysis presented herein, no claim term requires express construction.” Pet. 4 (citing *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“only those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy”)). Accordingly, Petitioner states that, in the Petition, it “analyzes the claims consistent with ordinary and customary meaning as would be understood by POSITA in light of the specification. *Phillips*, 415 F.3d at 1314–17. *Id.* (citing Ex. 1003 ¶¶ 60–61).

Patent Owner responds that for the purposes of the Preliminary Response only, it agrees that no express construction of any term is necessary. Prelim. Resp. 4–5.

Based on the current record, we determine that no claim term requires an explicit construction to decide whether Petitioner satisfies the “reasonable likelihood” standard for instituting *inter partes* review.

D. Obviousness challenge based on Zhang and Javanifard

Petitioner argues that claims 1–18 are unpatentable under 35 U.S.C. § 103 as obvious over the combination of Zhang and Javanifard. Pet. 19–61. We first provide an overview of the two cited prior art references and then address the obviousness challenge to claim 1 based on these references.

1. *Overview of Javanifard (Exhibit 1006)*

Javanifard describes its invention as “a charge pump having a variable number as opposed to a fixed number of stages according to charge pump power supply input levels and desired charge pump output levels.” Ex. 1001, 1:8–11. Javanifard describes disadvantages of charge pumps having a fixed number of stages. *Id.* at 1:48–63.

Javanifard explains that a “trend in the electronics industry is to reduce the power requirements of integrated circuitry.” *Id.* at 1:15–16. Javanifard teaches that “to reduce power consumption, integrated circuits are being designed to use lower voltage supply levels such as 3.3 volts instead of 5 volts.” *Id.* at 1:16–19. However, Javanifard teaches that certain operations “require voltages greater than that provided by the lower voltage power supplies.” *Id.* at 1:20–21. “For example, flash electrically-erasable programmable read only memory (flash EEPROM) requires approximately 12 volts for erase and programming operations.” *Id.* at 1:21–24. Javanifard teaches that “[c]harge pump technology permits the generation of voltages having a magnitude greater than that of the power supply. Through the use of charge pump circuitry 12 volts can be generated from 3.3 volts by using one or more charge pump stages.” *Id.* at 1:25–29.

Javanifard discloses at least two objects of its invention. First, “to provide a charge pump that can accommodate different output levels for a given charge pump power supply input level.” Ex. 1006, 2:19–21. Second, “to provide a charge pump that can accommodate a given output level for different charge pump power supply input levels.” *Id.* at 2:22–24.

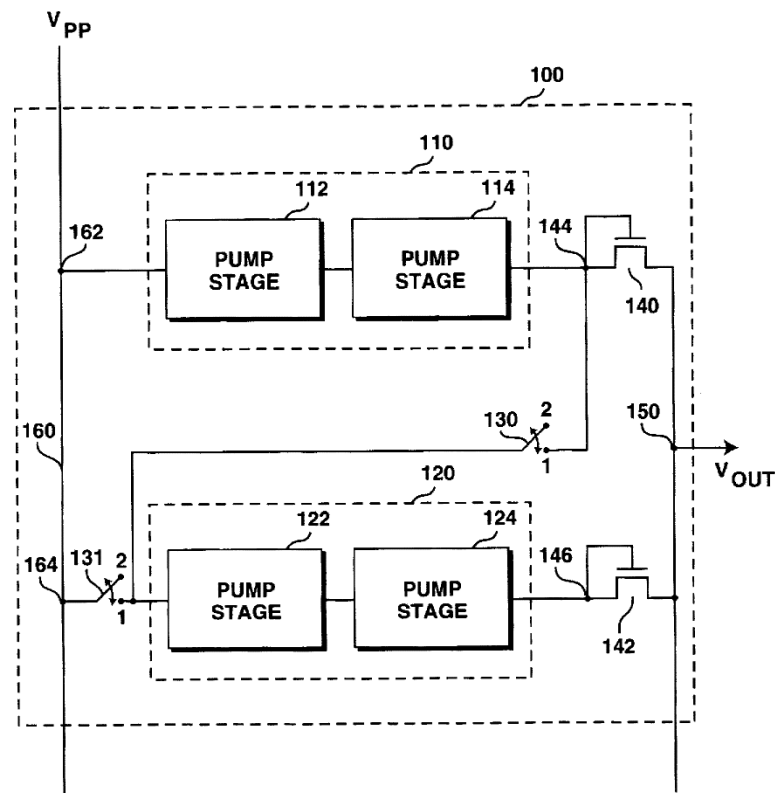
Figures 1, 2, and 3 illustrate three different representations of Javanifard’s disclosure. Figures 1 and 3 show a variable stage charge pump with one voltage power source and multiple “rungs” of charge pump stages,

where the charge pump can utilize one or more charge pump rungs to vary the number of pump stages employed to produce the output supply voltage.

The variable stage pump illustrated in Figure 3 is shown as having more rungs of charge pumps than Figure 1, and is coupled to flash memory. Otherwise, the charge pump of Figure 3 operates in the same way as the charge pump of Figure 1.

Javanifard's Figure 2 shows a variable stage charge pump with two voltage power sources, and three supply voltages, 5 volt, 9 volt, and 12 volt, for a flash memory.

Figure 1 of Javanifard is reproduced below:



Javanifard's Figure 1 is a block diagram of a variable stage charge pump 100 which includes two charge pump "rungs," labelled 162 and 164. Ex. 1006,

2:42–44. The rungs are coupled by bus 160 and have common output V_{out} 150. One power supply is shown in Figure 1, labeled “ V_{PP} ,” which supplies the supply voltage to the bus 160. Each rung 162, 164 includes a charge pump. Rung 162 includes charge pump 110 with pump stages 112 and 114. Rung 164 includes charge pump 120 with pump stages 122 and 124. Each rung is capable of boosting the voltage of V_{PP} . The pump stages in each rung are series-coupled. Javanifard teaches that “[t]he variable stage charge pump 100 may also be identified by the expression ‘X/Y stage pump’,” where the “X” refers to the number of rungs and “Y” to the number of pump stages. *Id.* at 2:59–67. The variable stage charge pump 100 has switches 130 and 131. First switch 130 “controls whether the output of the first charge pump is provided as an input to the second charge pump.” *Id.* at 2:54–56. Second switch 131 “is used to couple the input of the second charge pump to V_{pp} .” *Id.* at 2:56–57.

When switch 130 is on and switch 131 is off, the charge pumps 110 and 120 are series-coupled. Ex. 1006, 3:54–56. “When 110 and 120 are series-coupled, charge pump 100 might only be able to provide approximately $\frac{1}{2}$ the current as was the case when charge pumps 110 and 120 were parallel-coupled.” *Id.* at 3:63–65. When switch 130 is off and switch 131 is on, the charge pumps 110 and 120 are parallel-coupled. *Id.* at 3:43–44. “Because 110 and 120 are parallel-coupled, charge pump 100 will be able to provide approximately twice the amount of current as was the case when only charge pump 110 was operating.” *Id.* at 3:50–53.⁶

⁶ Petitioner states that a POSITA would have understood these statements to indicate “a design to accommodate ‘a **given output level** for **different** charge pump power supply input levels.’” Pet. 35.

Figure 3 of Javanifard (not reproduced) “illustrates a variable stage charge pump coupled to a flash memory array.” Ex. 1006, 2:38–39. The illustrated embodiment has 12 rungs, each with a charge pump, and each charge pump having 2 pump stages. *Id.* at 5:3–6. “The output of each of the n charge pumps is coupled to a same output node 350,” which provides power to the flash memory. *Id.* at 5:15–16. Similar to Figure 1, different currents can be provided by the circuitry shown in Figure 3. We focus the discussion on the embodiment shown in Figure 1 because Figure 3 has a similar circuitry and operates the same, but has a larger number of rungs and pump stages, and therefore can provide a larger number of variable currents.

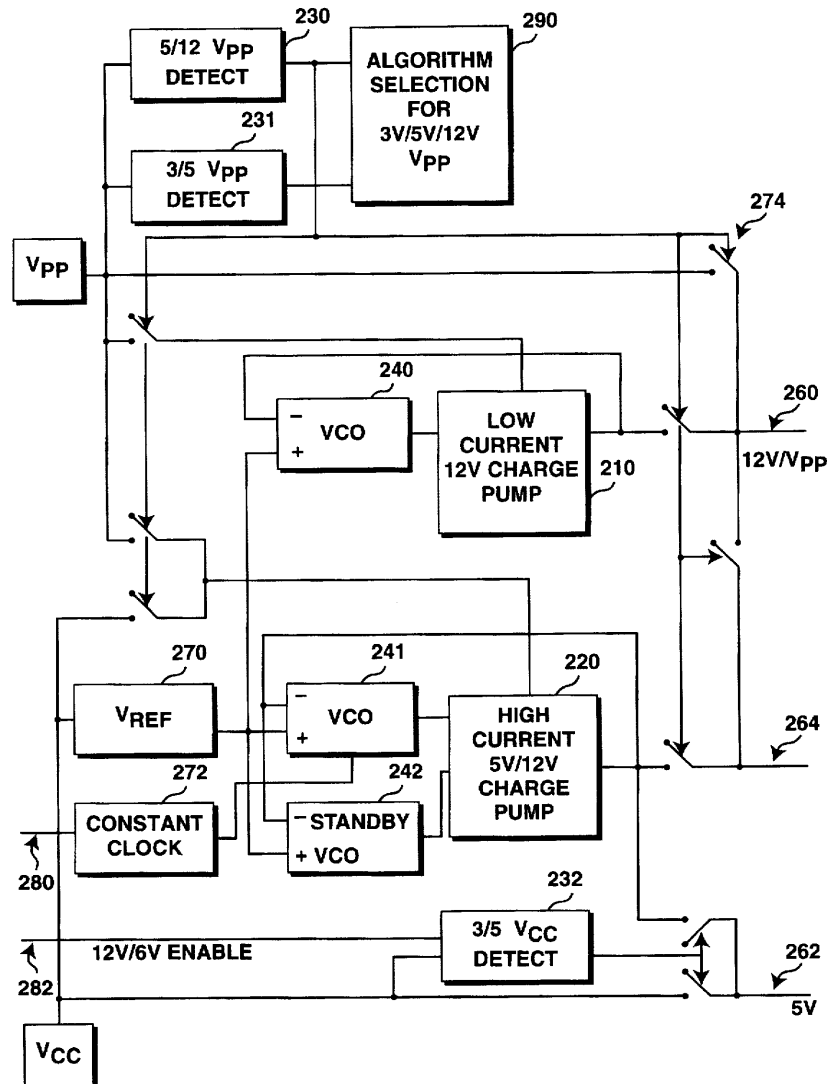
Javanifard teaches the advantages of varying the number of booster stages to achieve the desired supply voltage:

Designing the variable stage charge pump with an appropriate number of stages permits a charge pump circuit that can provide the proper voltages for the memory circuitry irrespective of the available power supply voltage. For example, if 6 and 12 volt supplies are required from the variable stage charge pump, the designer can provide a control to the switches that will switch stages in and out, or change the coupling of the stages to ensure the appropriate output voltage from the variable stage charge pump regard less of the input voltage. The control for the switches would be a function of the available power supply voltage, V_{pp} , and the desired variable stage charge pump output voltage.

Ex. 1006, 5:56–66.

We next turn to Figure 2 of Javanifard. Figure 2 illustrates a circuit with two power supplies and three supply output voltage lines. Figure 2 also shows “circuitry including variable stage charge pumps for supplying power to a flash memory array.” Ex. 1006, 2:36–37.

Figure 2 is reproduced below:



Javanifard’s Figure 2 is a block diagram showing “the power supply circuitry for a flash memory including variable stage charge pumps for accommodating a 5 volt, 9 volt, and 12 volt voltage level from either a 3.3 volt or 5 volt power supply.” Ex. 1006, 6:61–64. The figure shows two power supplies, V_{PP} and V_{CC} . Javanifard discloses that “two charge pumps (210, 220) are used to increase the internal node’s voltages to different voltages during the read mode (5 volt charge pumps), the programming

mode (12 volt and 9 volt charge pumps), and the erase mode (12 volt and 9 volt charge pumps).” *Id.* at 7:10–19. “Variable stage charge pump 220 is a high current variable stage charge pump used during the read, program, and erase operations.” *Id.* at 7:27–29. “Variable stage charge pump 210 is a low current variable stage charge pump used in addition to charge pump 220 only during program and erase operations.” *Id.* at 7:29–31. Javanifard further discloses the uses of different power supplies and different numbers of charge pump stages to achieve different supply voltages:

when V_{pp} has a nominal value of 5 volts, variable stage charge pump 210 (the high current charge pump) is configured to have 18 parallel-coupled sets of stages, each set including 3 serially coupled stages during the program, verify, and erase operational modes.

Id. at 8:24–30.

For the read mode, low current variable stage charge pump 220 is not used and can be turned off. During a read operation V_{pp} might be zero. Therefore if high current charge pump 220 is needed it will receive its power from V_{CC} instead of V_{PP} during the read mode.

Id. at 8:31–35.

2. Overview of Zhang (Exhibit 1005)

Zhang describes its invention as relating “to charge pump circuits operating responsive to a mode that enables selection of a power voltage or an external high voltage.” Ex. 1005, 1:11–14.

Zhang discloses a prior art charge pump circuit which comprises a charge supply part 11 and a plurality of charge pump parts 12–15. Ex. 1005, 1:33–34 (referencing a block diagram of a conventional charge pump circuit shown in Figure 1 (not reproduced)). Zhang teaches that charge supply part 11 “receives an external voltage V_{CC} and provides supply charges to a first

charge pump part PS1,” which is connected serially to additional charge pump parts 11 to 15. *Id.* at 1:34–37 (shown in Figure 1 as PS1 (part 12), PS2 (part 13), PS3 (part 14) and PSn (part 15)). “The charge pump parts 12–15 generate an output voltage V_{out} by pumping charges supplied from the charge supply part 11.” *Id.* at 1:38–39

Zhang discloses that a “conventional charge pump circuit pre-charges the output voltage V_{out} corresponding to the external voltage V_{CC} at each node of the charge supply part 11 and the charge pump parts 12–15.”

Ex. 1005, 1:63–66. With this circuit, Zhang teaches that “the time to precharge increases in the output voltage V_{out} .” *Id.* at 1:66–67. Zhang teaches that the “additional time” to precharge is “undesired particularly where testing integrated chips that require high voltages quickly. A need remains for an improved charge pump circuit.” *Id.* at 1:67–2:3.

Figure 4 of Zhang, reproduced below, shows a charge pump circuit that is asserted by Zhang to address the disadvantages of the conventional charge pump circuit.

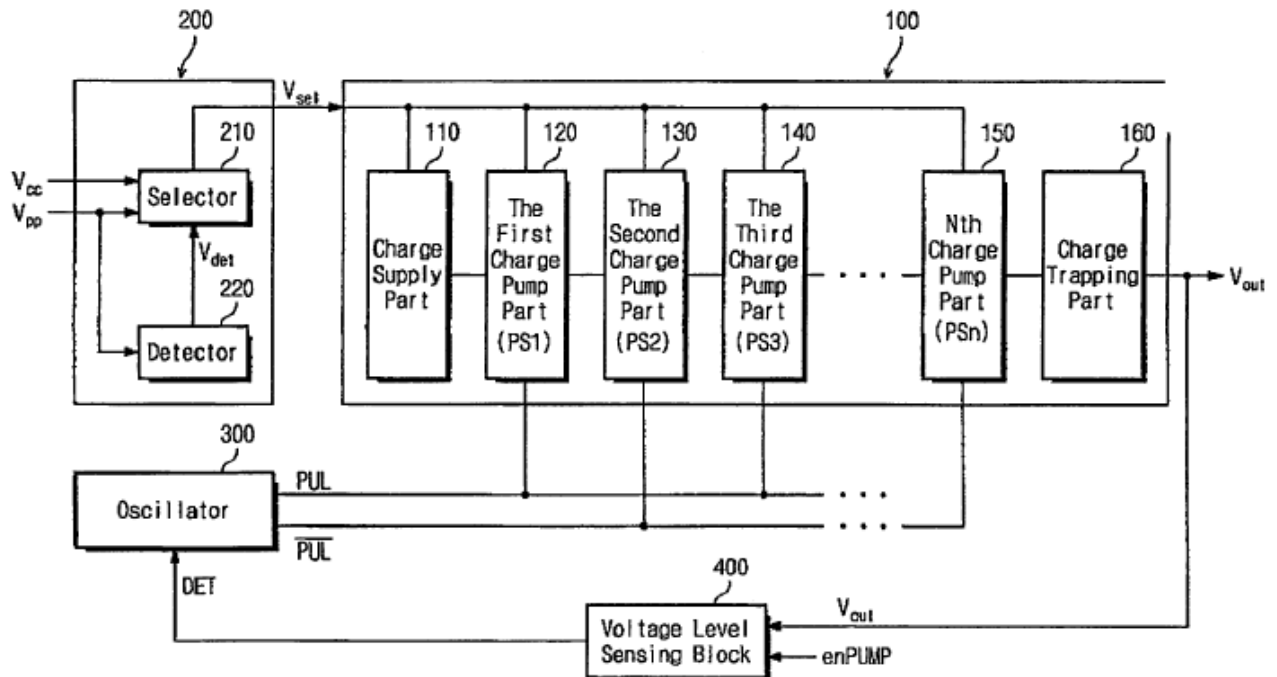


Figure 4 of Zhang shows a block diagram of a charge pump circuit 100.

Ex. 1005, 2: 54–55. The charge pump circuit comprises a charge pump block 100, a selecting circuit block 200, an oscillator 300, and a voltage level sensing block 400. *Id.* at 2:55–58. “The pump block 100 comprises a charge supply part 110, a plurality of charge pump parts 120, 130, 140, and 150 and a charge trapping part 160, all serially connected.” *Id.* at 2:59–61. The circuit has two power supplies, V_{CC} and V_{PP} .

The figure shows charge pump parts 110, 120, 130, 140, and 150. Part 150 is indicated as the nth charge pump part. The charge pump block 100 is therefore not restricted to five charge pump parts, but can have n number of parts. Circuit block 200 of Figure 4 provides voltage V_{sel} (from the power supplies V_{CC} or V_{PP}) to charge supply part 110, which then provides the voltage to the first charge part 120. Ex. 1005, 2: 62–64. First charge pump part 120 provides charge to the next charge pump part 130 and so on. *Id.* at 2:62–64. Each charge pump part “pumps a charge to a next serially

connected charge supply part.” *Id.* at 2:66–67. “The charge pump parts 120, 130, 140 and 150 pre-charge a charge corresponding to the selected voltage V_{sel} .” *Id.* at 2:64–66. Charge trapping part 160 “traps the pumped charge through each charge pump part 120, 130, 140 and 150 to generate an output voltage V_{out} .” *Id.* at 3:1–2.

As shown in Figure 4, the charge pump circuit comprises selecting circuit block 200 which includes selector 210 and detector 220. Ex. 1005, 3:19–22. Selector 210 is shown as receiving power voltage V_{CC} or external high voltage V_{PP} . Power supply voltage V_{CC} refers to the power voltage operating in general operation. *Id.* at 3:22–24. “The voltage V_{PP} refers to a high voltage provided externally during a test operation mode.” *Id.* at 3:24–25.

Figure 8 of Zhang, reproduced below, “is a graph of the output voltage V_{out} depending on whether the charge pump circuit uses the power voltage V_{CC} or external high voltage V_{PP} .” Ex.1005, 5:1–3 (Fig. 8).

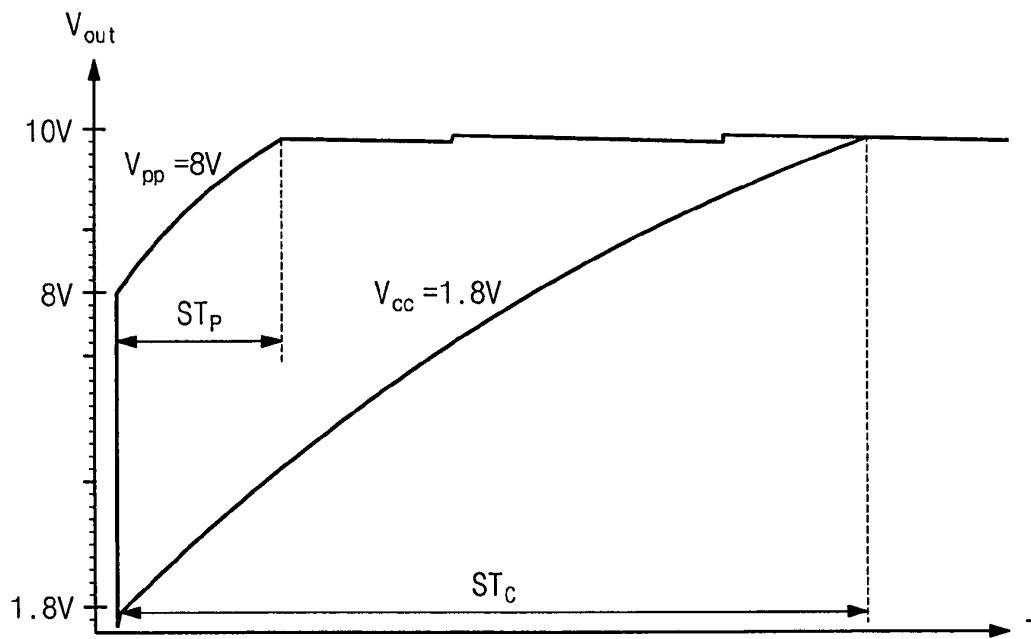


Figure 8 is a graph showing the time (on the X-axis) to obtain a “wanted voltage V_{out} ” (on the Y-axis), which in the figure is 10V. *Id.* at 5:3–9.

“[W]hen external high voltage V_{PP} is supplied with the power voltage V_{CC} , a wanted output voltage V_{out} can be obtained within a shorter time.” *Id.* at 5:9–11. Thus, Zhang describes how to achieve the *same* voltage output using two different voltage power supplies.

3. *Independent claim 1*

Petitioner challenges the patentability of claims 1–18 under 35 U.S.C. § 103(a) as obvious in view of Zhang and Javanifard. Pet. 5. The patentability challenge is based on the obviousness of combining Zhang’s circuit having first and second power supply voltages, with Javanifard’s circuit capable of selecting a variable number of booster stages (*see* Figures 1 and 3), to generate a “supply voltage” as recited in claim 1.

Patent Owner’s principal contention at this stage in the proceeding is that Petitioner has not provided evidence that a person of ordinary skill in the art would have been motivated to combine Zhang and Javanifard. Prelim. Resp. 5–14. Patent Owner does not challenge on the record before us that the individual elements of the claim are not disclosed in Zhang and Javanifard, but instead disputes Petitioner’s asserted motivation to combine the elements. In *KSR*, 550 U.S. at 398, although the Supreme Court emphasized “an expansive and flexible approach” to the obviousness question, *id.* at 415, it also reaffirmed the importance of determining “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *Id.* at 418.

We summarize Petitioner's contentions below on how the limitations in the claim are met by the combination of Zhang and Javanifard. We also address Patent Owner's arguments regarding Petitioner's reasoning to combine these prior art publications. On the current record, we find that there is sufficient evidence to support Petitioner's contentions of how the combined teachings of Zhang and Javanifard meet claim 1's limitations.

[1.0] 1. *A method for generating a supply voltage, comprising:*

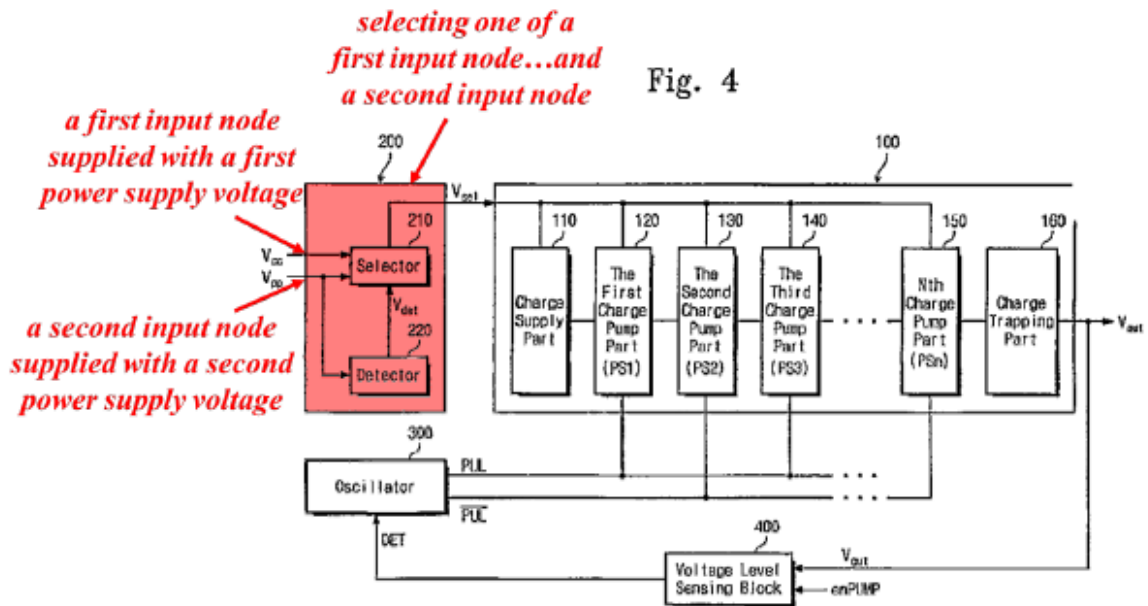
Petitioner provides evidence that Zhang describes generating a supply voltage (" v_{out} ") using a charge pump circuit. Pet. 23 (citing Ex. 1005, 2:55–3:2; Fig. 8; Ex. 1003 ¶ 98). Figure 4 of Zhang, reproduced above, illustrates this configuration.

Javanifard, as explained above, also describes generating a supply voltage. Javanifard describes a variable stage charge pump providing a supply voltage in integrated circuits, which in one embodiment is to "provide the proper voltages for the memory circuitry." Pet. 24 (citing Ex. 1006, Figs. 1–3; 2:18–24; 6:56–59). In Figure 1 of Javanifard, the supply voltage is labeled " V_{out} ."

[1.1] *selecting one of a first input node supplied with a first power supply voltage and a second input node supplied with a second power supply voltage that is higher than the first power supply voltage;*

Petitioner provides evidence that limitation [1.1] is described by Zhang. Pet. 24–25 (citing Ex. 1003 ¶¶ 102–106). With specific reference to Figure 4 of Zhang, Petitioner identifies "selecting circuit block 200 that selects one of a first node supplied with VCC (a first power supply voltage) and a second node supplied with VPP (a second power supply voltage)" as

corresponding to the selection of first and second nodes supplied with first and second power supply voltages, respectively, as evidence of the recited limitation. Pet. 24. Petitioner provides annotated Figure 4 of Zhang to show these elements. Pet. 25. Figure 4 annotated by Petitioner is copied below:



Annotated Figure 4 of Zhang shows selector 210 which selects VCC (or V_{CC}) (the claimed “first input node supplied with a first power supply voltage”) and VPP (or V_{PP}) (the claimed “second input node supplied with a second power supply voltage that is higher than the first power supply voltage”). VCC refers to the power voltage operating in general operation mode; VPP refers to a high voltage provided externally during a test operation mode. Ex. 1005, 3:21–27. The figure shows pump block 100 comprising “a plurality of charge pump parts 120, 130, 140, and 150 and a charge trapping part 160, all serially connected.” *Id.* at 2:59–61. The “charge pump parts” correspond to the claimed “booster stages.” The circuit has a fixed number of n stages.

Zhang further describes circuit block 200, which supplies voltage to charge pump block 100 (as illustrated in Figure 4):

The selector 210 selects between the power voltage VCC and the high voltage VPP. The detector 220 detects the level of the high voltage VPP to generate detection signal VDET. The detector 220 enables the detection signal VDET when the high voltage VPP is higher than the power voltage VCC. The selector 210 switches between the power voltage VCC to the high voltage VPP responsive to the detection signal VDET. Put differently, the signal VSEL is VCC in the general operation mode and VPP in the test operation mode allowing for a high voltage within a short time.

Ex. 1005, 3:29–38.

For the requirement of the claim that the second power supply voltage is higher than the first, Petitioner identifies the disclosure in Figure 8 of Zhang which shows that VPP (8V) is higher than VCC (1.8V). Pet. 24 (citing Ex. 1005, 5:5–9; *id.* at 3:32–36 (“The selector 210 selects between the power voltage VCC and the high voltage VPP”)). Petitioner points out that the ’701 patent has external and internal power supplies as does Zhang. *Id.*

[1.2.1] *coupling a selected one of the first and second input nodes to booster circuitry comprising a plurality of booster stages to provide an output voltage,*

Petitioner provides evidence that Zhang in view of Javanifard describes limitation [1.2.1] of claim 1. Pet. 26–31 (citing Ex. 1003 ¶¶ 107–116).

As explained above, Figure 4 of Zhang shows charge pump circuit 100 coupled to circuit block 200. Circuit block 200 comprises power voltage VCC and high voltage VPP. Circuit block 200 comprises first and second input nodes, as claimed, supplied with voltage by VCC and VPP, respectively. The charge pump block 100, comprising charge pump parts

110 to 150, the latter which correspond to the claimed “plurality of booster stages.” Pet. 26. Only one charge pump 100 is shown in Zhang; the circuit has a fixed number of stages which cannot be varied, i.e., all the stages are utilized when the circuit is open.

Returning to Javanifard, Petitioner provides evidence that Javanifard “describes coupling an input node with a power supply voltage to a booster circuitry comprising a plurality of booster stages to provide an output voltage.” Pet. 27. Javanifard has been discussed above. Figure 1 of Javanifard, as annotated by Petitioner, shows the elements asserted to correspond to the limitations in the claim. *Id.* at 28. Figure 1 of Javanifard annotated by Petitioner is reproduced below:

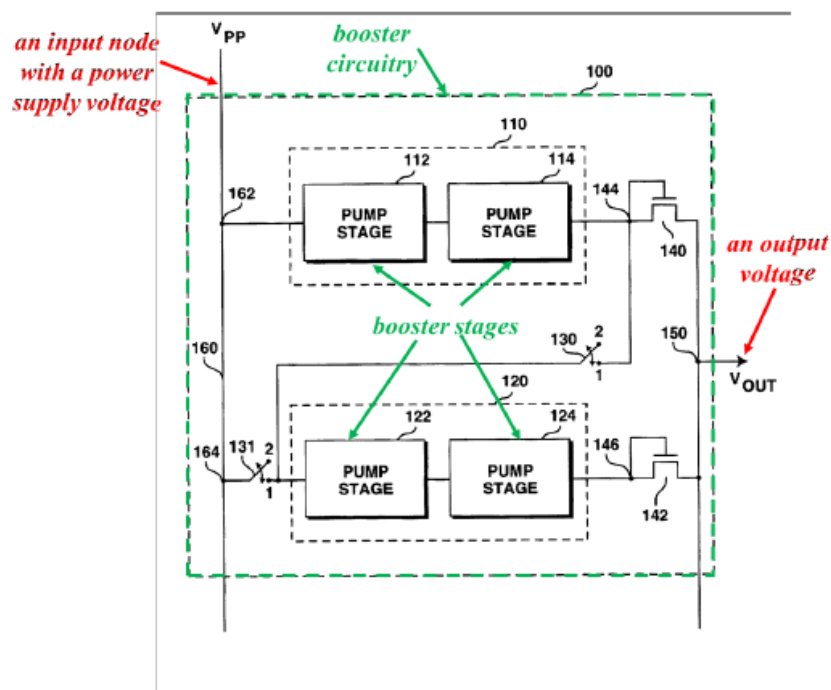


Figure 1 shows an input node with power supply V_{PP} coupled to charge pump 100. Figure 1 shows two rungs, 162 and 164, each with two serially-coupled pump stages: 110 comprising 112 and 114; 120 comprising 122 and 124. Pump stages 112, 114, 122, and 124 correspond to the claimed

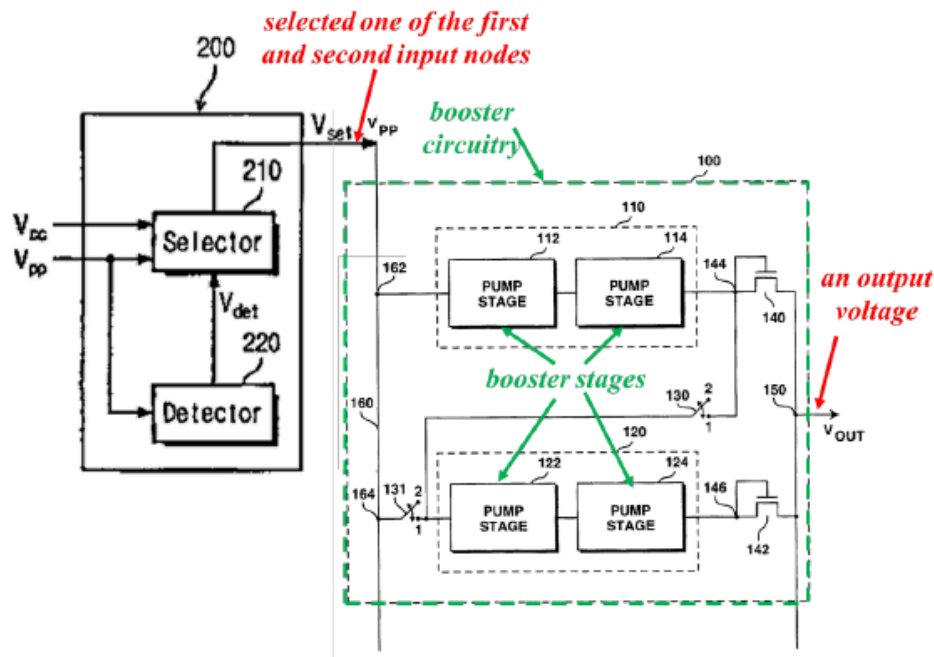
booster stages. Pet. 28. The “output voltage” of Javanifard’s Figure 1 corresponds to the “supply voltage” of claim 1.

Petitioner annotates Javanifard’s Figure 3, similarly to Figure 1, to show the elements which correspond to the claimed input node and booster circuitry. We understand on the current record that the main asserted differences between Figures 1 and 3 of Javanifard is that the latter figure shows more booster rungs and pump stages, and that the supply output voltage is coupled to a flash memory.

While Zhang’s circuit has two power supplies as required by claim 1, it has a fixed number of stages and not a variable number of booster stages as required by claim 1. For this reason, Petitioner turns to Javanifard.

Petitioner creates “Example A,” which is a combination of Zhang’s Figure 4 and Javanifard’s Figure 1. Pet. 30. The purpose of the composite figure is to provide Zhang’s “first input node supplied with a first power supply voltage and a second input node supplied with a second power supply voltage that is higher than the first power supply voltage” with a “first number of booster stages” and “a second number of booster stages,” where “the second number being less than first number” as recited in claim 1. *See* Pet. 30–31. The fixed booster stage circuitry in Zhang therefore is replaced by Javanifard’s variable booster circuitry.

Example A, as constructed by Petitioner, is reproduced below:



Example A shows circuit block 200 of Zhang coupled to variable charge pump 100 of Javanifard. According to Petitioner, this composite provides Javanifard's charge pump 100 with the ability to receive voltage from VCC or VPP using Zhang's circuit block 200. Pet. 31. Petitioner makes the same composite of Zhang's Figure 4 and Javanifard's Figure 3 (Example B), having the same functionality as Example A. *Id.* Because of the redundancy between Figures 1 and Figures 3 of Javanifard, we focus on Example A incorporating the circuit of Figure 1. The same facts and reasoning would apply to Example B.

Petitioner asserts that one of ordinary skill in the art would have been motivated to apply Javanifard's teaching of a variable stage charge pump to Zhang's multi-power-source charge pump system (which has a fixed charge pump)

to produce the obvious, beneficial, and predictable results of a variable stage charge pump system, which can both "accommodate different output levels for a given charge pump power supply input level," "accommodate a given output level

for different charge pump power supply input levels,” and provide flexibility for design needs (e.g., power saving mode, and current requirements), area reduction, and performance improvement, as taught by Javanifard. EX1003, ¶¶ 90–96.

Pet. 19–20.

Petitioner contends that the POSITA would have had reason to replace Zhang’s fixed stage pump with Javanifard’s variable stage charge pump because of the disadvantages of fixed stage pumps disclosed by Javanifard. Pet. 20 (citing Ex. 1006, 1:48–53 (“dedicated space in integrated circuit”); “lack of flexibility”; *id.* at 1:66–2:2 (“sacrifices performance” at one power supply to accommodate a second power supply)). Thus, for the reasons stated above, Petitioner contends that “[a] POSITA facing the need to improve its charge pump system would have looked to Javanifard and been motivated to apply Javanifard’s teachings of the variable stage charge pump in the multi-power-source charge pump system of Zhang using fixed stage charge pump.” Pet. 21.

Patent Owner contends that the disadvantages that Javanifard addressed in its circuitry do not apply to Zhang. Prelim. Resp. 1. Patent Owner argues that Zhang is not prior art to Javanifard⁷ and “does not practice the techniques Javanifard criticizes” and identifies as disadvantages. Prelim. Resp. 1. More specifically, Patent Owner argues that Javanifard discloses disadvantages of a “prior art method used to generate multiple higher voltage levels from *a single power supply voltage*” that “use a number of charge pump circuits each having a fixed number of stages.” Ex. 1006, 1:48–51 (cited Prelim. Resp. 6) (emphasis added). However,

⁷ Zhang need not be prior art to Javanifard for a skilled artisan to have combined Zhang and Javanifard at the time of the invention of the ’701 patent.

Patent Owner identifies the disclosure in Zhang in which only a single voltage level is generated from two different power supplies, not multiple levels generated as described in Javanifard, making Javanifard inapplicable to Zhang in Patent Owner's view. Prelim. Resp. 6–8 (citing Zhang, Fig. 8).

Patent Owner also contends that Javanifard's teaching that a disadvantage of the prior art is having multiple charge circuits which require additional physical space does not apply to Zhang because Zhang only has a single charge pump circuit. Prelim. Resp. 8–9.

In sum, Patent Owner argues that the disadvantages discussed in Javanifard cannot provide a motivation to combine because they are not present in Zhang. Prelim. Resp. 10 (citing *In re Schweickert*, 676 F. App'x 988, 994 (Fed. Cir. 2017) (finding no motivation to combine where the "record describes no problem in [the prior art] that would be resolved by the [proposed combination]").

Patent Owner's contentions overlook the principle that the disadvantages disclosed in the prior art need not precisely match Petitioner's reasoning to combine the prior art to make the claimed invention. According to *KSR*, 550 U.S. at 419–20, any known need or problem in the field can provide a reason to combine elements. ("[N]either the particular motivation nor the avowed purpose of the patentee controls . . . [A]ny need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed."); see also *In re Kemps*, 97 F.3d 1427, 1430 (Fed. Cir. 1996) ("[T]he motivation in the prior art to combine the references does not have to be identical to that of the applicant to establish obviousness.").

Petitioner here provided sufficient fact-based evidence that one of ordinary skill would have had reason to modify Zhang with Javanifard to

overcome the disadvantages of using a fixed pump stage to save space and improve flexibility (Pet. 20–21). Specifically, Zhang describes a fixed number of stages that would be unable to provide multiple output supply voltages when desired or necessary. Javanifard addressed this disadvantage by replacing the fixed booster circuitry with variable booster circuitry.

Ex. 1006, 1:48–59. While it is true that Zhang describes only supplying a single voltage level, the reason to apply Javanifard to Zhang is to avoid redundancy when a device requires more than one voltage level by providing a single booster circuit capable of delivering multiple supply levels instead of requiring multiple fixed circuits that take up space and reduce flexibility. Petitioner’s reasoning is therefore logical and consistent with the objectives disclosed by Javanifard.

While Zhang describes a charge pump which operates in a general operation mode or a test mode, Petitioner provides evidence that Zhang is not limited to these modes. Pet. 22 (Ex. 1005, 5:23–51 (“claiming a charge pump circuit including a selector circuit without any operation mode requirement”). In view of this teaching and Javanifard’s, Petitioner contends that the skilled worker would have had reason “to provide a multi-power source charge pump to support a device having multiple operation modes, including a device having ‘a test or general operation mode’ and devices having other operation modes (e.g., a memory device having different read, write, programming modes)” as described by Javanifard. Pet. 22 (citing Ex. 1006, Fig. 2).

In response, Patent Owner argues that Zhang’s circuitry provides only a *single output level*, making it irrelevant to Javanifard which describes using a single variable stage charge pump circuit to provide *different output levels*. Prelim. Resp. 10–11 (citing Pet. 36, 42–44). Patent Owner contends

that “because the Petition’s proposed combination does not involve ‘provid[ing] different output levels,’ that cannot be a motivation to pursue the combination.” *Id.* at 11.

Petitioner’s reasoning to combine Zhang and Javanifard is based on the obviousness of using Zhang’s two-voltage power supplies to operate a circuit with different modes of operation. Zhang discloses different operation modes, albeit to achieve the same voltage level. Javanifard also describes different operation modes, but also is capable of providing different output supply levels. We agree with Petitioner that Zhang’s teaching of using two input voltage supplies to power at least two modes of operation would have reasonably suggested to one of ordinary skill in the art that such input voltage supplies could be adapted to operate modes that require different levels of output voltage as described in Javanifard.

Patent Owner criticizes Petitioner’s reason to combine because Javanifard teaches different supply voltage outputs, in contrast to Zhang’s single output level. Prelim. Resp. 11. We have already explained above the ground is based on the obviousness of adapting Zhang’s circuit to provide different supply outputs as described in Javanifard. We additionally note that Patent Owner’s criticism does not account for the other object of the invention disclosed in Javanifard of using different power supplies to provide “a given output level,” i.e., a single level, as asserted by Patent Owner to be described in Zhang. *See* Ex. 1006, 2:22–24 (“a charge pump that can accommodate a *given output level* for different charge pump power supply input levels”). Petitioner specifically cited this embodiment in its reason to combine Zhang and Javanifard. Pet. 20. Thus, using Javanifard’s booster circuitry to achieve one level of output supply voltage is also consistent with Javanifard’s objective. *See* also limitation [1.2.2] describing

how the booster circuitry of Javanifard, when combined with Zhang, can be utilized to provide a “given” output supply voltage for different input levels. Pet. 35. For this reason, we find Petitioner’s reasoning to be factually-supported by the evidence before us at this stage of the proceeding.

In making its argument of the obviousness of applying Javanifard to Zhang, Petitioner cites Figure 2 of Javanifard, explaining that the figure illustrates “variable stage charge pumps used for a multi-power-source memory device with different modes.” Pet. 22.

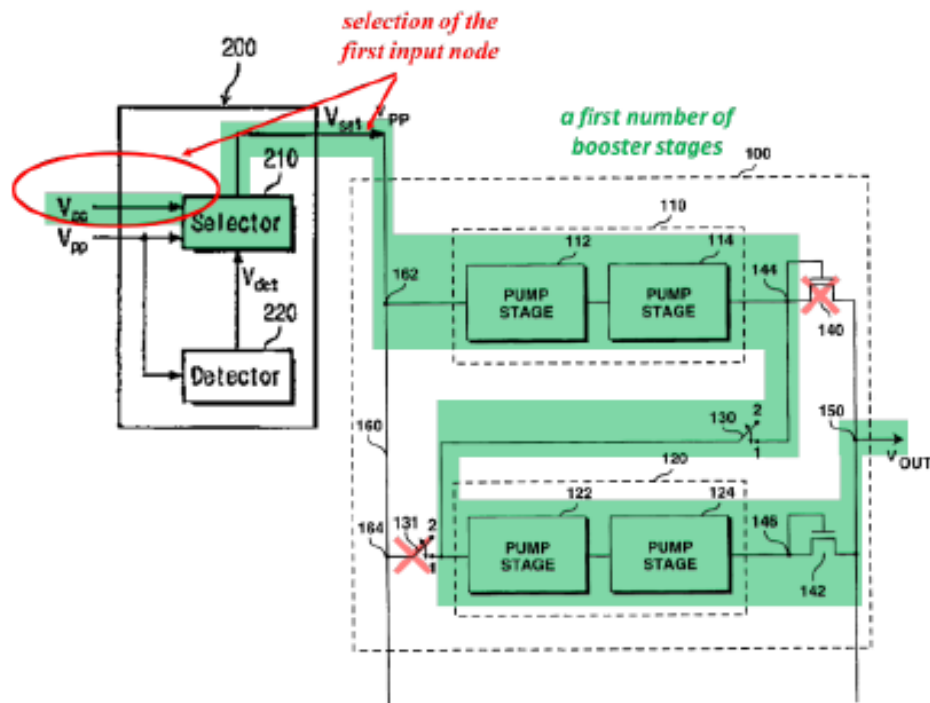
Responding to this contention, Patent Owner argues that the combination proposed in the Petition is based on applying the teachings of Javanifard’s Figure 1 to Zhang, not Figure 2. Prelim. Resp. 12. Patent Owner contends that the “Petition does not explain how any of the benefits of Javanifard’s Figure 2 (such as supporting multiple operation modes) would be realized by its proposed combination, because the Petition does not allege that Zhang would be modified to incorporate the teachings of Javanifard’s Figure 2.” Prelim. Resp. 12.

Patent Owner’s argument is unpersuasive. As discussed earlier, Javanifard describes using its variable charge pump to provide both a given output voltage and different output voltages. Ex. 1006, 2:18–24. Petitioner cites Javanifard for its teaching of “improved flexibility for design needs.” Pet. 21. Dr. Stiegler testifies in his declaration (Ex. 1003) that using a variable stage pump, which is a single circuit, is advantageous because a single circuit can be used to “provide different output levels,” rather than requiring a number of charge pumps, each having fixed number of stages. Ex. 1003 ¶ 92 (citing Ex. 1006, 1:67–2:2). This is one of the disadvantages of fixed booster circuits disclosed by Javanifard. Ex. 1006, 1:48–51 (“One prior art method used to generate multiple higher voltage levels from a

single power supply voltage is to use a number of charge pump circuits each having a fixed number of stages.”). Zhang has fixed stages. Ex. 1003 ¶ 93. Thus, Dr. Stiegler addresses a benefit of the proposed combination that takes advantage of the ability of the variable circuit to provide different supply voltages, replacing the need for multiple circuits, each having one fixed stage pump. While Figure 2 of Javanifard is cited by Petitioner, it is not the figure used in the combination of Zhang and Javanifard; the figure is cited for its teaching of different modes of operation consistent with Zhang’s teaching of different operational modes, providing a reason to apply Javanifard to Zhang. Pet. 22. The evidence before us therefore supports Petitioner’s reason to combine Zhang and Javanifard.

[1.2.2] *wherein selection of the first input node corresponds to a first number of booster stages and*

Petitioner contends that the combination of Zhang and Javanifard makes limitation [1.2.2] obvious. Pet. 32 (citing Ex. 1003 ¶¶ 117–124). Zhang provides a circuit with the capability to choose from two power sources. Ex. 1005, Figure 4. Javanifard provides a circuit with the capability to choose from different combinations of charge pumps and pump stages. Ex. 1006, Figure 1. The obvious combination of Zhang and Javanifard would result in a circuit in which “selection of the first input node (with a lower input power supply voltage level) corresponds to a first number (a higher number e.g., 4) of booster stages, e.g., for generating the same output voltage as the selection of the second input node with a higher input power voltage level.” Pet. 32 (citing annotated Example A). Petitioner shows this circuitry as follows as Example A, which is a composite of Zhang’s Figure 4 and Javanifard’s Figure 1 created by Petitioner (Pet. 33):



Petitioner-annotated Example A (combining Zhang Figure 4 on left with Javanifard Figure 1 on right) shows the selection of the first input node 210 associated with V_{cc} (having a lower input power supply level), as provided by Zhang, combined with Javanifard’s variable booster circuitry. Pet. 32. Javanifard is configured to “accommodate a given output level” (Ex. 1006, 2:22–24) by serially connecting charge pumps 110 and 120 according to row 3 of Table 1 to provide a higher voltage boost for a lower power supply level. *Id.* at 33–35. As shown in the above figure, the serial connections are achieved by having switch 130 on, switch 131 off, and no current flow through transistor 140 (*see* Ex. 1006, 4:22–36). “Because both 110 and 120 are two stage charge pumps, this means that charge pump 100 will effectively be a four stage charge pump with all four stages serially coupled.” Ex. 1006, 3:54–60 (cited at Pet. 34). Thus, as recited in limitation

[1.2.2], the “selection of the first input node corresponds to a first number of booster stages” (the serially-connected pump stages 112, 114, 122, and 124).

Petitioner explains:

A POSITA would have understood that this statement of “approximately twice the output voltage at node 150” applies when the input voltage levels are the same, and in a design to accommodate “a given output level for different charge pump power supply input levels,” the configuration of row 3 with more serially connected stages provides more voltage boost for a lower power supply input level.

Pet. 35.

As explained above in the discussion of limitation [1.2.1], Javanifard discloses at least two objects of its invention, one is “to provide a charge pump that can accommodate different output levels for a given charge pump power supply input level” and another is “to provide a charge pump that can accommodate a given output level for different charge pump power supply input levels.” Ex. 1006, 2:19–24. Petitioner’s evidence that Javanifard describes using two voltage input levels to provide a “given output level” is consistent with the latter objective, as well as Zhang which discloses the same goal. Accordingly, we find that Petitioner’s reasoning and evidence supports the obviousness of claim 1.

[1.2.3] *selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number; and*

Petitioner contends that the combination of Zhang and Javanifard makes limitation [1.2.3] obvious. Pet. 35–36 (citing Ex. 1003 ¶¶ 125–131).

Petitioner makes the same argument as for limitation [1.2.2]. To support this argument, Petitioner cites Table 1 of Javanifard, annotating it as follows (Pet. 34):

TABLE 1			
Switch 130	Switch 131	Charge Pump 110	Charge Pump 120
OFF	OFF	ON	OFF
OFF	ON	ON	parallel-coupled to charge pump 110
ON	OFF	ON	series-coupled to charge pump 110
ON	ON	N/A	N/A

a second number of booster stages, the second number being less than first number

a first number of booster stages

Petitioner contends that “to accommodate a given output level” (Ex. 1006, 2:22–24 (cited at Pet. 36)) “for the second input node with a higher power supply voltage, a POSITA would have configured the variable stage charge pump of FIG. 1 of Javanifard according to row 1 of Table 1 . . . , because row 1 of Table 1 provides a second (lower) number of serially connected booster stages to provide a lower voltage boost (by providing only charge pump 110 in operation and thereby having a lower number of serially connected booster stages).” Pet. 36–37. Row 1, annotated in red, shows switches 130 and 131 off. Petitioner contends that this selection would have been made by a POSITA “based on a design need for power saving mode.” *Id.* at 38 (citing Ex. 1006, 3:39–42). For this reason, as for limitation [1.2.2], Petitioner contends that it would have been obvious to one of ordinary skill in the art to select “pump stage designs to provide the required output voltage according to the different power supply input levels.” Pet. 38.

As addressed above in the discussion accompanying limitation [1.2.1], Petitioner’s argument is consistent with the objectives of Javanifard to provide a charge pump that can “accommodate different output levels for a

given charge pump power supply input level” and also “a given output level for different charge pump power supply input levels.” Ex. 1006, 2:19–24.

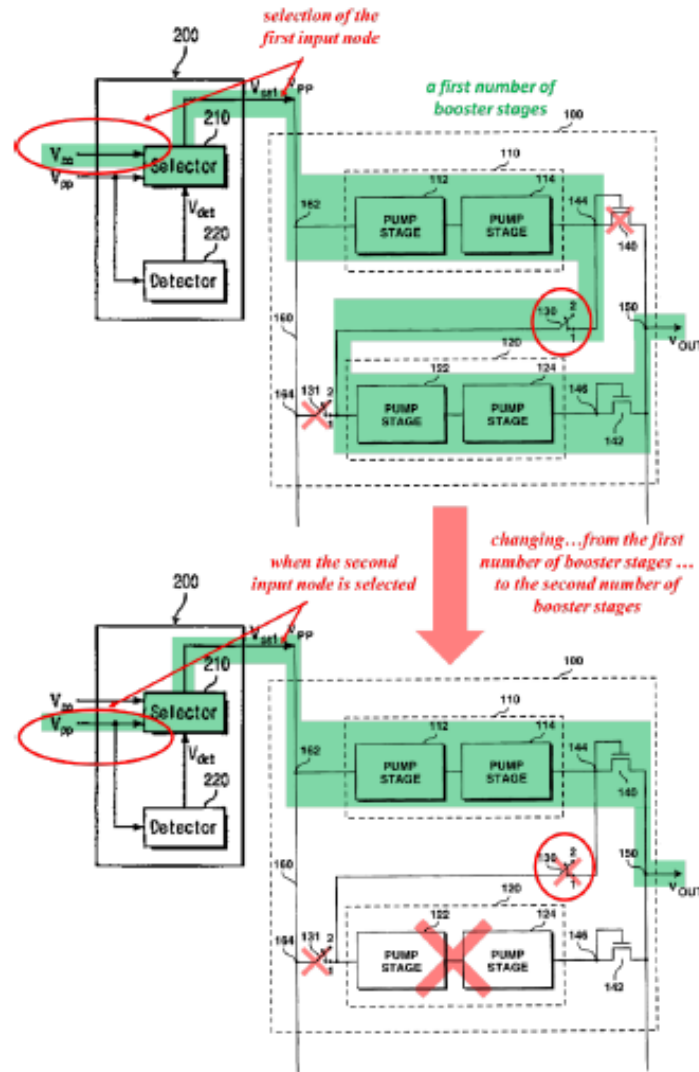
[1.3] *changing the booster circuitry from the first number of booster stages corresponding to selection of the first input node to the second number of booster stages when the second input node is selected.*

Citing Zhang, Figure 4, and Javanifard, Figure 1 and Table 1, as evidence, Petitioner explains that the number of booster stages in Figure 1 of Javanifard can be changed from 2 to 4 by changing the switch configuration. Pet. 39–40. Petitioner contends, based on its discussion of limitations [1.2.2] and [1.2.3], that:

selection of the first input node corresponds to a first number of booster stages, and selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number, e.g., to provide the **same** output voltage for different power supply voltage levels.

Pet. 39.

Below, Petitioner shows how the booster circuitry is changed by turning switch 130 from on to off. Pet. 41 (another modification of Example A of Zhang combined with Javanifard).



Petitioner-modified Example A shows that, when the lower power voltage VCC is selected (top), switch 130 is on, switch 131 is off, and four booster stages are engaged. When the higher power supply VPP is selected (bottom), switch 130 is changed from on to off, and “the booster circuitry is changed from the first number of booster stages (e.g., 4) to the second number of booster stages (e.g., 2).” Pet. 40.

Annotated Table 1 showing this change is reproduced below (Pet. 40):

TABLE 1

Switch 130	Switch 131	Charge Pump 110	Charge Pump 120	
OFF	OFF	ON	OFF	<i>a second number of booster stages, the second number being less than first number</i>
OFF	ON	ON	parallel-coupled to charge pump 110	
ON	OFF	ON	series-coupled to charge pump 110	<i>a first number of booster stages</i>
ON	ON	N/A	N/A	



Annotated Table 1 shows that when the selection of the input node is changed to the higher power supply voltage, the booster circuitry is changed from the first number of booster stages (e.g., 4) to the second number of booster stages (e.g., 2), by turning off switch 130. Pet. 40.

4. Summary

In sum, Petitioner provides evidence that the combination of Zhang and Javanifard reasonably suggests a circuit that has advantages over the fixed booster stage circuit described by Zhang with the capability to “accommodate” both “different output levels for a given charge pump power supply input level” and “a given output level for different charge pump power supply input levels” as described by Javanifard (Ex. 1006, 2:19–24). Thus, Petitioner demonstrates a reasonable likelihood of proving that claim 1 is unpatentable under § 103(a) as obvious over Zhang in view of Javanifard.

5. Claims 2–18

Petitioner asserts that claims 2–9, which depend from claim 1, and claims 11–18, which depend from claim 10, are unpatentable under 35 U.S.C. § 103 as obvious over the combination of Zhang and Javanifard. Pet. 42–61. Claim 10 has substantially the same limitations as claim 1, but is directed to a semiconductor device.

We have reviewed Petitioner's arguments and evidence and we find them to be persuasive on the current record. Patent Owner in its Preliminary Response does not address claims 2–18 separately.

Based on the current record and for the reasons discussed above for claim 1, Petitioner has demonstrated a reasonable likelihood of proving that claims 2–18 are unpatentable under 35 U.S.C. § 103 as obvious over the combination of Zhang and Javanifard.

E. Obviousness challenge based on Javanifard

Petitioner challenges the patentability of claims 1–18 under 35 U.S.C. § 103(a) as obvious over Javanifard. Pet. 62–86. The patentability challenge is based on the obviousness of combining 1) Javanifard's power supply circuitry for a flash memory including variable stage charge pumps for accommodating three different voltage levels from two different power supplies as illustrated in Figure 2 (Ex. 1006, 6:61–64) with 2) Javanifard's variable stage charge pumps, illustrated in Figures 1 and 3, having a number of booster rungs, each rung having one or more fixed charge pump stages (Ex. 1006, 2:41–51). The charge pumps of Figures 1 and 3 are illustrated as having only one power supply. Petitioner argues that it would have been obvious to apply Figure 2's teaching of multiple power sources to the variable stage charge pumps of Figures 1 and 3, to achieve Javanifard's object to "accommodate a given output level for different charge pump power supply input levels." Pet. 64 (citing Ex. 1006, 2:21–23; Ex. 1003 ¶ 207).

At this stage in the proceeding, Patent Owner's main contention is that Petitioner has not provided a reason why a person of ordinary skill in the art would have been motivated to combine Figure 2 of Javanifard with Figures

1 or 3 into a single embodiment in the fashion asserted by Petitioner. Prelim. Resp. 15–30. Patent Owner does not challenge on the record before us that the individual elements of the claims are disclosed Javanifard, but instead disputes Petitioner’s asserted motivation to combine the elements. In *KSR*, 550 U.S. at 398, although the Supreme Court emphasized “an expansive and flexible approach” to the obviousness question, *id.* at 415, it also reaffirmed the importance of determining “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *Id.* at 418.

We turn to claim 1 and Petitioner’s contentions on how the limitations in the claim are met by the combination of Figure 2 with Figures 1 or 3 of Javanifard. Patent Owner has not disputed these contentions, which we find to be supported by sufficient evidence on the current record.

Petitioner’s contentions for each limitation are summarized below.

[1.0] *1. A method for generating a supply voltage, comprising:*

Petitioner cites Javanifard’s disclosure, as illustrated in Figure 1, of a variable stage charge pump generating a power supply for various devices. Pet. 65–66 (citing Ex. 1006, 5:17–24; 5:56–59; Figs. 2, 3 which illustrate generating a supply voltage to a memory device).

[1.1] *selecting one of a first input node supplied with a first power supply voltage and a second input node supplied with a second power supply voltage that is higher than the first power supply voltage;*

Petitioner provides evidence that Javanifard discloses a circuitry which meets the claimed limitation. Pet. 66–69 (citing Ex. 1003 ¶¶ 213–220).

Specifically, Petitioner identifies the circuitry shown in Figure 2 of Javanifard as showing “selecting from a first input node supplied with a first power supply voltage (e.g., VCC)” and “a second input node supplied with a second power supply voltage (e.g., VPP), where VPP (e.g., VPP = 5 volts) is higher than VCC (e.g., VCC = 3.3 volts).” Pet. 68 (citing Ex. 1006, 6:61–64; 7:15–17; 8:24–29. Figure 2, as annotated by Petitioner, is reproduced below:

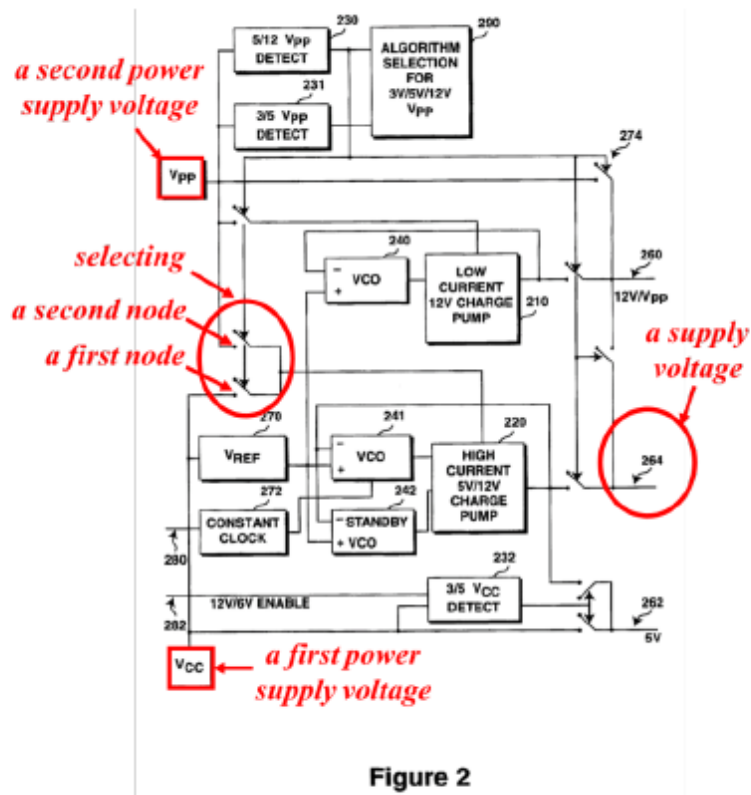


Figure 2

Petitioner-annotated Figure 2 shows a switch for selecting a first power supply VCC or a second power supply VPP (see switch on left circled in red). Petitioner states that the switch is “controlled by control signals provided by a selection circuit (e.g., selection circuit 290 with voltage detect circuits 230 and 231).” Pet. 69. The supply voltage 294 is circled in red on the right.

[1.2.1] *coupling a selected one of the first and second input nodes to booster circuitry comprising of) booster stages to provide an output voltage,*

To meet the recited limitation in the claim, Petitioner contends it would have been obvious to combine the circuitry shown in Figure 2 with the charge pumps shown in Figures 1 and 3 of Javanifard. Pet. 62–65, 69–70, 73 (citing Ex. 1003 ¶¶ 221–225). First, Petitioner provides a composite drawing made by combining Javanifard’s Figures 1 and 2, which Petitioner refers to as “Example C.” *Id.* The composite, annotated in red by Petitioner, is reproduced below:

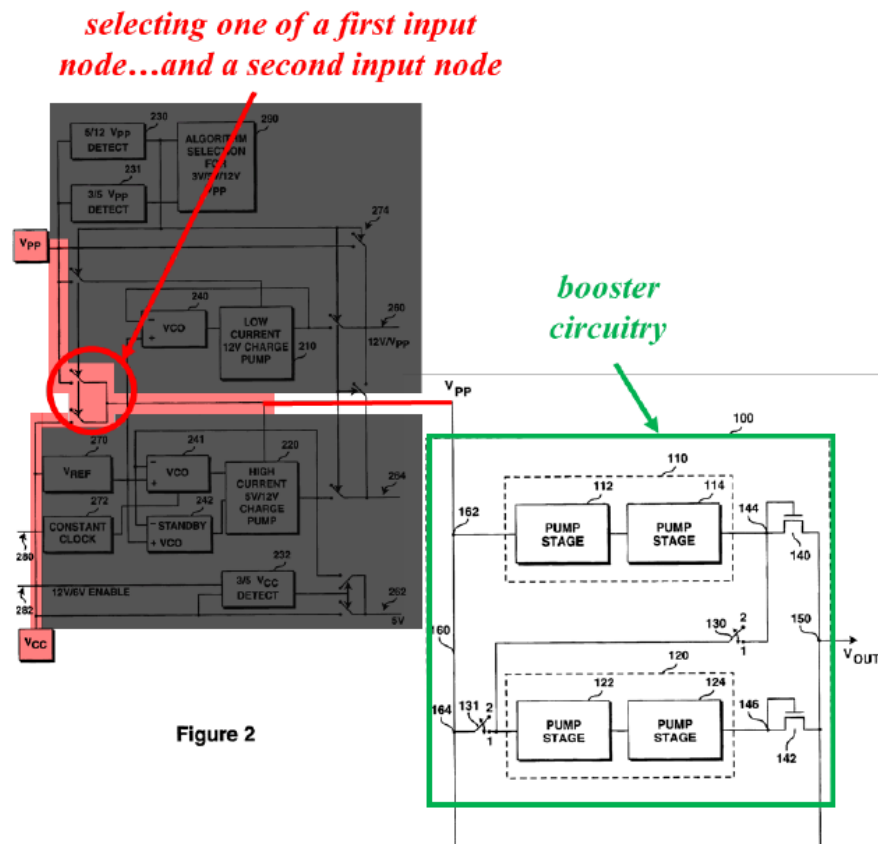


Figure 2

Figure 1

Example C, reproduced above, shows the combination of the circuitry of Figure 2 with the charge pump of Figure 1. Figure 2 of Javanifard (on the

left) shows circuitry comprising two power supplies, V_{pp} and V_{cc} , and a selector switch that can select the power supply V_{pp} at one node or the power supply V_{cc} at the other node. Figure 1 (on the right) shows circuitry comprising charge pumps 110 and 120. Each charge pump comprises one or more fixed stages. Ex. 1006, 2:48–49. Petitioner labels Figure 1 as the “booster circuitry,” i.e., the circuitry that boosts the voltage level. *See* Ex. 1003 ¶ 36. *See also* Pet. 73 (labeling the pump stages 112, 114, 122, 124 in Javanifard’s Figure 1 as “booster stages”).

Example D (not reproduced here) provided by Petitioner uses the booster circuitry illustrated in Javanifard’s Figure 3 instead of Figure 1. Pet. 72.

Petitioner contends that “one of a first input node supplied with a first (lower) power supply voltage and a second input node supplied with a second (higher) power supply voltage is selected, and provided to a booster circuitry.” Pet. 70. Petitioner explains that the figures “are simplified for illustration purposes, and it would have been obvious to a POSITA to implement additional well-known circuits (e.g., voltage detection circuit, voltage selection circuit providing control signals to selection switches, clock signals to drive the charge pumps) according to the design needs.” *Id.*

Petitioner contends:

A POSITA would have been motivated to apply Embodiment 2’s [Figure 2] teachings of selection from multiple power sources to the variable stage charge pump as taught in Embodiments 1 or 3 [Figures 1 or 3], by selecting and supplying the selected power supply source (as taught in Embodiment 2) to the input of the variable stage charge pump, to produce the obvious, beneficial, and predictable results of a multi-power source variable stage charge pump system.

Pet. 62–63. To support this contention, Petitioner cites the disclosure in Javanifard of one of its objects as providing “a given output level for different charge pump power supply input levels.” Ex. 1006, 2:21–23 (cited at Pet. 64). That is, Petitioner’s reason to combine the two circuits is to use the two power sources to achieve a “given” supply voltage, i.e., the same voltage supply level using different input power supplies.

Petitioner contends that it would have been obvious to a POSITA to combine the circuitry of Figure 2 of Javanifard (different power supply voltages) with the circuitry of Figures 1 and 3 of Javanifard (variable stage pumps). Petitioner explains that “a POSITA would have been motivated to apply Javanifard teachings of an input power supply selector for selecting from input nodes supplied with different power supply voltages” in Javanifard’s variable stage charge pump system “to “have the benefit of providing a charge pump that can ‘**accommodate a given output level for different charge pump power supply input levels**’, e.g., for a device supplied with multiple power sources using two source lines” (e.g., Vcc and Vpp). Pet. 69–70 (citing Ex. 1006, 6:44–46⁸).

In response to Petitioner’s reason to combine Figure 2 with Figures 1 or 3 of Javanifard, Patent Owner argues that the combination is not compatible because Figure 2 provides multiple output voltages while Figures 1 and 3 provide only one. Pet. 21–23.

⁸ “[P]ower for the flash memory device is provided by two sources. These sources include a Vcc line and a Vpp line. The Vcc line is the primary power source for the flash device. The supplemental voltage provided by supply line, Vpp, is typically needed only when writing or erasing the memory because of the higher voltages needed during those operations.”

Specifically, Patent Owner argues that Javanifard's Figure 2 provides circuitry for flash memory that is "capable of providing a variety of different output voltages at different current requirements according to a variety of different operating modes, all while accommodating variation in both V_{cc} and V_{pp} input voltage levels." Prelim. Resp. 21. Patent Owner argues that this "level of flexibility" is "important" and "mandatory." *Id.* (citing Ex. 1006, 6:61–64; 6:12–17; 6:56–60 ("To maximize the utility of a flash memory system . . . the variable stage charge pump must be able to generate approximately 5 volts, 9 volts, and 12 volts from either a 3.3 volt or 5 volt power supply.")). Yet, Patent Owner argues that Petitioner's reason to combine Figure 2 with Figures 1 and 3 is to provide the same output voltage level. Patent Owner asserts that the Petition "never provides any allegation that in its proposed combination, the output voltage would be configured to vary at all, much less to provide three separate output levels from two different input voltages, as Javanifard teaches its system 'must be able to' do." Prelim. Resp. 22.

Based on the current record, we agree with Patent Owner that the obviousness challenge is defective. Figure 2 of Javanifard is described as showing "the power supply circuitry for a flash memory including variable stage charge pumps for accommodating a 5 volt, 9 volt, and 12 volt voltage level from either a 3.3 volt or 5 volt power supply." Ex. 1006, 6:61–64. Despite this express teaching of a multi-power source circuit (V_{PP} , V_{CC}) designed to deliver three different voltage levels to flash memory to accommodate different memory operations (*id.* at 7:10–20), Petitioner's reasoning to combine Figure 2 with Figures 1 or 3 is to provide "a given output level." Pet. 64, 70, 75, 77. We understand the repeated references in the Petition to Javanifard's disclosure of a "given output level" (Ex. 1006,

2:22–24) to mean the same output level, in contrast to the other “object” disclosure by Javanifard of “different output levels” (Ex. 1006, 19–21). *See* also Pet. 79 (“to provide the same output voltage level”). Thus, based on the evidence before us at this time, Petitioner’s reason to use two different power sources to provide the same level of supply voltage appears to change the principle upon which Javanifard’s circuitry in Figure 2 operates. *See Adidas AG v. Nike, Inc.*, 963 F.3d 1355, 1359 (Fed. Cir. 2020) (affirming PTAB’s decision not finding obviousness where a proposed modification would “change the principles under which [the prior art] operates”).

Dr. Stiegler’s testimony does not address Patent Owner’s concern. Dr. Stiegler asserts that Javanifard “explicitly provides motivations to apply its teaching of selection from multiple power sources of Embodiment 2 [Figure 2] to the variable stage charge pump of Embodiments 1 or 3 [Figures 1 and 3], by providing the selected power supply to the variable stage charge pump.” Ex. 1003 ¶ 207. However, Dr. Stiegler merely repeats what is in the Petition about the obviousness of using different power supplies to achieve a given output level, and that such configuration was well-known; however, he fails to explain the reason why one of ordinary skill in the art would have used two power supplies to provide only one output supply voltage. Thus, his testimony is conclusory and unsupported. *See Xerox Corp. v. ByteMark, Inc.*, IPR2022-00624, Paper 9 at 15 (PTAB Aug. 24, 2022) (precedential).

Dr. Stiegler explains how combining the different teachings of Javanifard would produce circuitry capable of providing a given output level, but fails to provide a sufficient reason that would have prompted a POSITA to replace the two booster circuits in Figure 2 with the one variable booster of Figures 1 and 3. *See, e.g.*, Ex. 1003 ¶¶ 227–231. “[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements;

instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *KSR*, 550 U.S. at 418 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). The reason to combine is an essential element to establish obviousness “because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.” *Id.* at 418–19.

Patent Owner also contends that “a POSITA reviewing Javanifard would have understood that Javanifard’s variable-stage charge pumps 210 and 220 of Figure 2 would be implemented using the structures of Javanifard’s Figure 1 and/or Figure 3, as that is the clear implication of the Javanifard reference itself.” Prelim. Resp. 19. Patent Owner states that “nearly all of the components from Javanifard’s Figure 2 (other than circuitry to select between Vcc and Vpp) have been removed, including Figure 2’s two separate variable-stage charge pumps 210 and 220, and in their place only a single variable-stage charge pump has been added.” *Id.* at 20–21. Patent Owner contends that there is no apparent reason why this modification has been proposed when Javanifard “clearly intended . . . to leave the functionality of Figure 2 in place, and simply implement the variable-stage charge pumps 210 and 220 using Javanifard’s teachings from Figure 1 and/or Figure 3.” *Id.*

The ground is based on what would have been obvious to one of ordinary skill in the art, not on what Javanifard “clearly intended” or described in its disclosure. Prelim. Resp. 21. Thus, while it may be true that the most logical interpretation of Javanifard’s Figure 2 is that each charge pump 210 and 220 was meant to be a charge pump of Figure 1 and 3, this finding is not dispositive. Nevertheless, in making an obviousness

determination, “it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does.” *KSR*, 550 U.S. at 418. As explained above, Petitioner *did* not do so here. Pet. 63–65, 69–70.

Specifically, where Figure 2 shows two different charge pumps, one of low current and the other of high current, Petitioner has not explained the reason to eliminate these two and replace them with a single charge pump as illustrated in Figures 1 and 3. For example, Petitioner has not asserted equivalency between the structures that would have led the POSITA to replace one with the other. *Compare Wm. Wrigley Jr. Co. v. Cadbury Adams USA LLC*, 683 F.3d 1356, 1364 (Fed. Cir. 2012) (“strong case of obviousness based on the prior art references of record” because the claim “recites a combination of elements that were all known in the prior art, and all that was required to obtain that combination was to substitute one well-known . . . agent for another.”). Indeed, as indicated by Patent Owner, replacing the two charge pumps in Figure 2 with the charge pump of Figures 1 or 3 results in a circuit with only one output supply voltage, rather than three supply outputs, and therefore on the current record does not appear to be equivalent to the circuit in Figure 2 and its application for flash memory.

Patent Owner further argues that “Javanifard already accommodates a given output level for different charge pump power supply input levels.” Prelim. Resp. 24 (citing Ex. 1006, 6:56–64 (“Figure 2 is able to choose between any one of ‘a 5 volt, 9 volt, or 12 volt level’ output ‘from either a 3.3 volt or 5 volt power supply.’”)); Prelim. Resp. 26 (“Javanifard already discloses a multi-power source system that makes use of variable stage charge pumps.”). Patent Owner contends that the Petition “alleges no problem in Javanifard that would be resolved by the Petition’s proposed

modification, and the purported goal of ‘accommodat[ing] a given output level for different charge pump power supply input levels’ therefore cannot motivate the Petition’s complete rearchitecting of Javanifard’s Figure 2.”

Prelim. Resp. 25 (citing *Schweickert*, 676 F. Appx at 995–96 (“finding no motivation to pursue a modification where the ‘record describes no problem in [the prior art] that would be resolved by the [proposed modification]”).). Thus, Patent Owner contends that because the Petition does not provide “any coherent motivation to pursue” the proposed modification of Javanifard, it “is strongly suggestive of improper hindsight reasoning.” Prelim. Resp. 29.

The obviousness of a preferred combination of elements does not negate the obviousness of other combinations, even if inferior, that can accomplish the same goal. The “case law is clear. It’s not necessary to show that a combination is ‘the best option, only that it be a suitable option.’” *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021) (quoting *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1197–98 (Fed. Cir. 2014)). However, as already explained above, the evidence does not support Petitioner’s reason to combine Figure 2 with the charge pumps of Figures 1 and 3. As indicated by Patent Owner, Figure 2 comprises two variable charge pumps. Ex. 1006, 6: 61–66; 7:21–22. Petitioner has not articulated a reason with rationale underpinnings which would have prompted the POSITA to substitute these two charge pumps with the single charge pump of Figures 1 or 3. It is not enough to say that they can be combined to produce a given supply output voltage as asserted in Dr. Stiegler’s largely conclusory testimony; there must be a reason to do so.

As to Patent Owner’s contention, citing *Schweickert*, that the rejection is deficient because no problem is resolved by the proposed combination, we agree that the Federal Circuit in *Schweickert* did make such a statement, but

in reference to an alternative basis for the rejection affirmed by PTAB. *Schweickert*, 675 Fed. Appx at 995. The underlying reason the Federal Circuit reversed PTAB was because the “Board’s decision is deficient in another respect.” *Id.* “[T]he Board has not explained why or how a skilled artisan would further configure or manipulate Birrell’s RAM such that there would be multiple lockable buffers as claimed in the ’272 Patent.” *Id.* *Schweickert* found the Board’s decision deficient because the motivation to combine the references lacked support (“the record does not appear to substantiate” the Board’s finding; “the record lacks support for this supposed motivation to introduce Cunniff’s semaphore into Birrell’s RAM”). The court summed up: “the Board has proffered no sufficient basis for why a skilled artisan would have readily applied Cunniff to Birrell.” *Id.* The reasoning in *Schweickert* applies here too because Petitioner’s reasoning to combine the different embodiments of Javanifard is not supported by sufficient evidence.

[1.2.2] *wherein selection of the first input node corresponds to a first number of booster stages and*

As evidence that one of ordinary skill in the art would select a “first input node correspond[ing] to a first number of booster stages,” Petitioner cites Javanifard’s disclosure that an object of its invention “is to provide a charge pump that can accommodate a given output level for different charge pump power supply input levels. Ex. 1006, 2:22–24 (cited at Pet. 75).

The Petition further cites Table 1 of Javanifard for describing the selection of “a lower charge pump power supply input level, such that selection of the first input node corresponds to a first number (a higher number, e.g., 4) of booster stages.” Pet. 75. Table 1 shows the four different

possible combinations for switches 130 and 131 of Javanifard’s Figure 1. “The phrase ‘on’ when referring to switches 130 and 131 means that the switches provide a current path. The phrase ‘off’ when referring to switches 130 and 131 means that the switches are in an open-circuit state.” Ex. 1006, 3:8–11. “A first switch (130) controls whether the output of the first charge pump is provided as an input to the second charge pump. A second switch (131) is used to couple the input of the second charge pump to Vpp,” which is the voltage output. *Id.* at 2:54–57. Each charge pump is shown in Figure 1 of Javanifard as having a specific number of “pump stages,” where each pump stage corresponds to the claimed “booster stage.”

Table 1, as annotated by Petitioner, is copied below:

TABLE 1			
Switch 130	Switch 131	Charge Pump 110	Charge Pump 120
OFF	OFF	ON	OFF
OFF	ON	ON	parallel-coupled to charge pump 110
ON	OFF	ON	series-coupled to charge pump 110
ON	ON	N/A	N/A

a second number of booster stages, the second number being less than first number

a first number of booster stages

Table 1 shows selecting switch 130 “ON” and switch “OFF”, resulting in coupling charge pumps 110 and 120 in series (third line, in green).

Table 1, row 1 (in red) shows selecting both switches 130 and 131 “OFF”, resulting in charge pump 110 “ON” and charge pump 120 “OFF”.

Table 1, row 3 (in green), “provides a first number (a higher number, e.g., 4) of serially connected booster stages to provide a higher voltage boost (e.g., by serially connecting charge pumps 110 and 120).” Pet. 75. Row 1 (in red) of Table 1, in contrast, provides “a lower number (e.g., 2) of serially

connected booster stages” by having only charge pump 110 in operation.”
Id. See Ex. 1003 ¶ 228.

[1.2.3] *selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number; and*

To meet the claim limitation, Petitioner provides evidence that the first row of Table 1 (reproduced above) “provides a second (lower, e.g., 2) number of serially connected booster stages to provide a lower voltage boost (by providing only charge pump 110 in operation and thereby having a lower number of serially connected booster stages)” than the third row of Table 1. Pet. 77. Dr. Stiegler testifies:

Connecting more stages in series provide a higher voltage boost compared to using a smaller number of stages in series, as each stage in the charge pump contributes to increasing the voltage level, and the total voltage boost is the cumulative effect of all the stages.

Ex. 1003 ¶ 228.

Petitioner also contends that “a POSITA would have used row 1 based on a design need for power saving mode, because it provides a lower current than row 2.” Pet. 78 (citing Ex. 1006, 3:39–42 (“This configuration [of row 1] might be used in a power saving mode if charge pump 100 is otherwise providing sufficient current and voltage output levels.”))).

[1.3] *changing the booster circuitry from the first number of booster stages corresponding to selection of the first input node to the second number of booster stages when the second input node is selected.*

As discussed above under [1.2.2] and [1.2.3], in the combination of

the Javanifard embodiments, selection of the first input node corresponds to selecting a first number of booster stages, and selection of the second input node corresponds to selecting a second number of booster stages. The selection of the second node (row 1 of Table 1) results in selecting less booster stages than the first node (row 3 of Table 1).

Javanifard further discloses that “control for the switches would be a function of the available power supply voltage, V_{pp} , and the desired variable stage charge pump output voltage.” Ex. 1006, 5:65–67 (cited at Pet. 79). Thus, Petitioner contends, “when the selection of the input node is changed to the higher power supply voltage, the booster circuitry is changed from the first number of booster stages (e.g., 4) to the second number of booster stages (e.g., 2), by turning off switch 130.” Pet. 79–80. To illustrate this change in the booster/charge pump circuitry, Petitioner provides the following annotated Table 1:

TABLE 1				
Switch 130	Switch 131	Charge Pump 110	Charge Pump 120	
OFF	OFF	ON	OFF	<i>a second number of booster stages, the second number being less than first number</i>
OFF	ON	ON	parallel-coupled to charge pump 110	
ON	OFF	ON	series-coupled to charge pump 110	<i>a first number of booster stages</i>
ON	ON	N/A	N/A	

Table 1, reproduced above, shows that, when switch 130 is turned off, the number of booster stages/pump stages changes from a first number to a second number which is less than the first number.

1. Summary

In sum, the patentability challenge to claim 1 of the '701 patent, based on Javanifard alone, lacks a requisite reason to combine the circuitry of Figure 2 with the circuitry of Figures 1 and 3. Accordingly, Petitioner has not established a reasonable likelihood that it would prevail in showing claim 1 is unpatentable over Javanifard.

2. Claims 2–18

Petitioner asserts that claims 2–9, which depend from claim 1, and claims 11–18, which depend from claim 10, are unpatentable under 35 U.S.C. § 103 as obvious over Javanifard. Pet. 81–86. Claim 10 has substantially the same limitations as claim 1, but is directed to a semiconductor device. All these claims recite, or incorporate by dependency, the same limitations which, as discussed above, are not made obvious by the specific combination of Javanifard's teachings as proposed in the Petition.

Hence, based on the current record, Petitioner has not demonstrated a reasonable likelihood of proving that claims 1–18 are unpatentable under § 103(a) as obvious over Javanifard.

F. Obviousness challenge based on Zhang, Javanifard, and Kang

Petitioner asserts that claims 9 and 18, which depend from claims 1 and 10, respectively, are unpatentable under 35 U.S.C. § 103 as obvious over Zhang, Javanifard, and Kang. Pet. 87–91.

We have reviewed Petitioner's arguments and evidence and we find them to be persuasive. Patent Owner's Preliminary Response does not separately address these dependent claims.

Thus, based on the evidence in this present record, we are persuaded that Petitioner has shown sufficiently for purposes of this Decision that the combination of Zhang, Javanifard, and Kang teaches or suggests all of the limitations recited in dependent claims 9 and 18, and has articulated sufficient reasoning to combine these references. Therefore, Petitioner has demonstrated a reasonable likelihood of showing that these claims are unpatentable over Zhang, Javanifard, and Kang.

G. Obviousness challenge based on Javanifard and Kang

Petitioner asserts that claims 9 and 18, which depend from claims 1 and 10, respectively, are unpatentable under 35 U.S.C. § 103 as obvious over Javanifard and Kang. Pet. 87–91.

Petitioner’s contentions regarding Kang do not address the deficiencies discussed above in the patentability challenge based on Javanifard. *See* Section II.E. Consequently, for the same reasons applied to claim 1, we determine, based on the current record, that Petitioner has not demonstrated a reasonable likelihood of proving that claims 9 and 18 are unpatentable under § 103(a) as obvious over Javanifard.

CONCLUSION

We determine that Petitioner establishes a reasonable likelihood that it would prevail in showing that at least one of the challenged claims 1–18 of the ’701 patent is unpatentable. Hence, we institute an *inter partes* review of all challenged claims on all challenges included in the Petition. *See SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1355 (2018) (noting that the language of 35 U.S.C. § 314(b) “indicates a binary choice—either institute review or don’t”); *PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018)

(interpreting the statute as requiring “a simple yes-or-no institution choice respecting a petition, embracing all challenges included in the petition”). At this juncture in the proceeding, we have not made a final determination with respect to the patentability of the challenged claims, or with respect to claim construction.

III. ORDER

It is

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–18 of the ’701 patent is instituted commencing on the entry date of this Decision; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of trial. The trial will commence on the entry date of this Decision and proceed in accordance with a separately entered Scheduling Order.

IPR2023-01230
Patent 9,207,701 B2

FOR PETITIONER:

David O'Dell
Hong Shi
david.odell.ipr@haynesboone.com
hong.shi.ipr@haynesboone.com

For PATENT OWNER:

James Milkey
Qi Tong
jmilkey@raklaw.com
ptong@raklaw.com