

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner

v.

LONGITUDE LICENSING LTD.,
Patent Owner

IPR2023-01230

U.S. Patent No. 9,207,701

PETITIONER'S REPLY

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PETITIONER'S EXHIBIT LIST

Updated: July 30, 2024

EX1001	U.S. Patent No. 9,207,701 to Hayashi et al. ("’701 patent")
EX1002	Prosecution File History of the ’701 Patent ("’768 app")
EX1003	Declaration of Dr. Harvey J. Stiegler
EX1004	CV of Dr. Harvey J. Stiegler
EX1005	U.S. Patent No. 7,427,888 to Zhang et al. ("Zhang")
EX1006	U.S. Patent No. 5,767,735 to Javanifard et al. ("Javanifard")
EX1007	Prosecution File History of Zhang (App. 10/888667) ("’667 app")
EX1008	Charge Pump Circuit Design, Pan et al., 1st Edition, 2006 ("Pan")
EX1009	Prosecution File History of Parent of ’701 patent (App. 12/052422) ("’422 app")
EX1010	Prosecution File History of Parent of ’701 patent (App. 13/912845) ("’845 app")
EX1011	Order Granting Western Digital’s Motion to Stay (Amazon) (05-16-23)
EX1012	Order Granting Western Digital’s Motion to Intervene (Amazon) (05-16-23)
EX1013	Director Vidal Memorandum re: Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, June 22, 2022
EX1014	U.S. Patent No. 7,579,902 to Frulio et al. ("Frulio")
EX1015	U.S. Patent No. 7,477,093 to Al-Shamma et al. ("Al-Shamma")
EX1016	U.S. Patent No. 7,046,076 to Daga et al. ("Daga")
EX1017	U.S. Patent No. 6,157,242 to Fukui ("Fukui")
EX1018	U.S. Patent No. 7,505,350 to Lee et al. ("Lee")
EX1019	U.S. Patent No. 6,954,386 to Narui et al. ("Narui")
EX1020	"Charge Pump Circuits with Low Area and High Power Efficiency for Memory Applications," Kang et al., Journal of Semiconductor

	Technology and Science, Vol. 6, No. 4, December 2006
EX1021	U.S. Patent No. 6,034,539 to Hwang (“Hwang”)
EX1022	U.S. App. Pub. No. 2003/0067063A1 to Muff et al. (“Muff”)
EX1023	U.S. Patent No. 6,346,738 to Kim et al. (“Kim”)
EX1024	Declaration of Dr. Sylvia D. Hall-Ellis
(New) EX1025	U.S. Patent No. 7,170,197 to Lopata (“Lopata”)
(New) EX1026	“Charge-Pump Circuits: Power-Consumption Optimization,” Palumbo et al., IEEE Transactions on Circuits and Systems—I: Fundamental Theory and Applications, Vol. 49, No. 11, November 2002 (“Palumbo”)
(New) EX1027	Texas Instruments, Power Management Selection Guide, August 30, 2004, https://web.archive.org/web/20050306072641/http://focus.ti.com:80/lit/ml/slvt145d/slvt145d.pdf (retrieved July 19, 2024), accessible also through “download” hyperlink in EX1028 (“TI-Guide”)
(New) EX1028	Texas Instruments, DC Converters Selection Guides, 2024, https://web.archive.org/web/20040909150107/http://focus.ti.com:80/analog/docs/analogtechdoc.tsp?navSection=sel_guides&templateId=2&familyId=490 (retrieved July 19, 2024) (“TI DC Converters Selection Guides”)
(New) EX1029	Bruce Jacob deposition transcript, June 21, 2024 (“Jacob Deposition”)
(New) EX1030	U.S. Patent No. 6,927,441 to Pappalardo et al. (“Pappalardo”)
(New) EX1031	U.S. Patent No. 6,060,942 to Oh (“Oh”)

I. Introduction

Longitude (“Patent Owner” or “PO”), in its Patent Owner’s Response (“POR”), cannot dispute that the claims are rendered obvious by the prior art. So, to avoid a clear finding of unpatentability, they attempt to distort the teachings of prior art, misrepresent Petition’s combinations, and misapply the law. The Board should disregard these arguments and find the challenged claims unpatentable.

II. Claim Construction

For purposes of this proceeding and the analysis presented herein, no claim term requires express construction.

III. Grounds 1-4: No Specific Limitations are in Dispute.

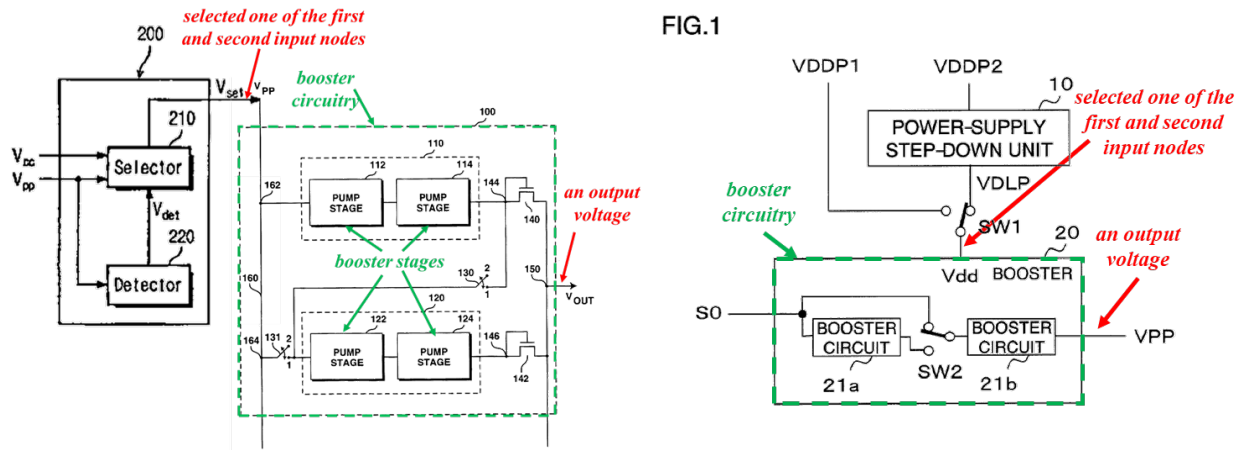
No specific limitations are in dispute. Also, PO does not dispute the combination with Kang in Grounds 3-4. Thus, arguments about specific limitations and the combination with Kang should be deemed waived. “Any arguments not raised by Patent Owner in a timely filed response may be deemed waived.” Paper 7, 2.

IV. Ground 1: Combination of Zhang and Javanifard (Zhang-Javanifard) Renders the Claims Obvious.

As a general reply and as Petition points out, Zhang and Javanifard both describe charge pump systems. Pet. 19-23; EX1003, ¶¶73-82; 87-96. Javanifard specifically provides Zhang the benefit of configurability of the pump stage topology (including “the number of stages and the coupling of the charge pump

stages”), based on design needs, which is not contested by PO. Pet. 10-16, 21; EX1003, ¶¶73-82; 87-96; *see generally* POR, 12-24. PO presents meritless arguments against other potential benefits of Javanifard, but regardless, at least Javanifard’s uncontested benefit of configurability of the pump stage topology is sufficient to combine Zhang and Javanifard. *Outdry Techs. v. Geox S.p.A.*, 859 F.3d 1364, 1370-71 (Fed. Cir. 2017) (“Any motivation to combine references, whether articulated in the references themselves or supported by evidence of the knowledge of a skilled artisan, is sufficient to combine those references.”).

As illustrated in the side-by-side illustration of Petition’s Example A of Zhang-Javanifard and FIG. 1 of ’701 Patent below, Zhang-Javanifard discloses the purported invention as claimed in the ’701 Patent, because it provides a power supply source selector coupled to a variable stage charge pump, where the pump stage topology including the stage numbers is configurable based on the selected power supply source. Pet. 30-31 (providing also Petition’s Example B of Zhang-Javanifard); ’701 Patent, Claim 1.



Example A (Zhang-Javanifard) vs. '701 Patent, FIG. 1

As such, PO's no-motivation-arguments fail, because they do *not* even dispute Petition's fundamental motivation that Javanifard provides the beneficial configurability of stage topology based on design needs. Regardless, as detailed below, PO's no-motivation-arguments also fail because they are based on mischaracterization of Petition's combination, contradict prior art and POSITA's knowledge and common sense, and misapply the law.

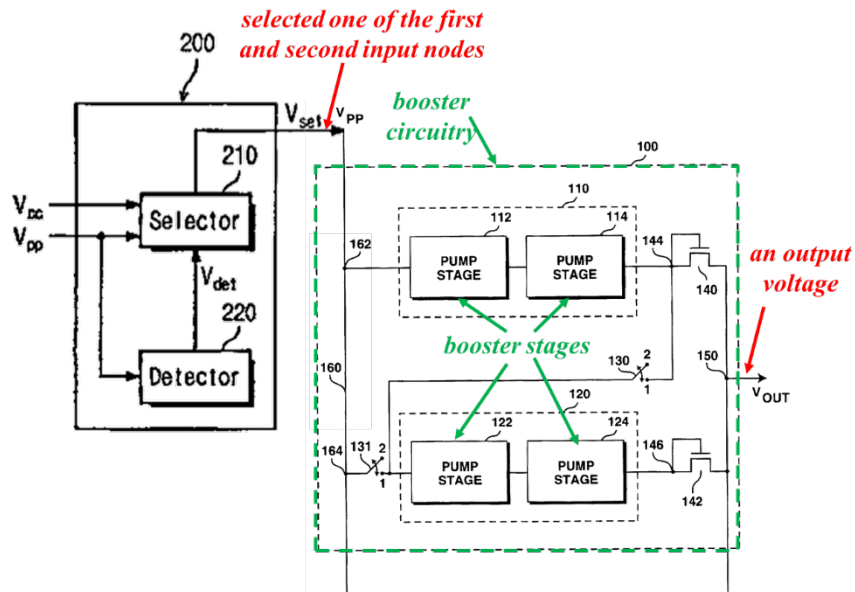
A. PO mischaracterizes Petition's combination as a system that “would result in only a *single* voltage output.”

PO states, “Petition's proposed combination of Zhang with Javanifard involves providing *only a single* output voltage level,” and as such, “fails to motivate a modification to Zhang *for the purpose* of providing a single output level.” POR, 5- 6. This is not only incorrect, but also irrelevant: claim limitations of the '701 Patent do not impose such a purported requirement of *only a single* voltage output level.

PO's purported requirement for "only a single voltage output level" contradicts Zhang, Javanifard, and Petition's combination. *See, e.g.*, EX1005, claim 1 (claiming a charge pump circuit without such a purported requirement); EX1006, claim 1 (claiming a variable stage charge pump without such a purported requirement), 1:8-11 (Javanifard relates to "providing a charge pump having a variable number...**according to** charge pump power supply input levels and **desired charge pump output levels.**"). Further, it directly contradicts Petition's motivations based on the well-known need for one or more output voltage levels, expressly disclosed in Javanifard. Pet., 19-20 (explaining that Petitioner's motivations include being capable to "**both** 'accommodate **different output levels** for a given charge pump power supply input level' [and] 'accommodate a given output level for different charge pump power supply input levels'"); EX1003, ¶¶90-96; EX1006, 1:30-32 ("**In the electronics field**, the practitioner often needs to generate **a number of voltages...**"); EX1014, Title ("Charge Pump for Generation of **Multiple Output-Voltage-Levels**"); EX1030, 2:20-27.

As illustrated in Petition's Example A below, Zhang-Javanifard provides a variable stage charge pump system with various configurations, e.g., providing "different output levels" under a subset of configurations, and providing "a given output level" under another subset of configurations. Further, contrary to PO's assertion of only a single fixed output level, Javanifard's "a given output level"

means a “*desired*” output level that can be changed by the designer/user based on output voltage specifications. EX1006, 1:8-11 (“providing a charge pump having a variable number...*according to...desired charge pump output levels.*”).



Example A of Zhang-Javanifard

As PO acknowledged, Javanifard Table 1 below provides how the charge pumps can be configured. POR, 7.

TABLE 1

Switch 130	Switch 131	Charge Pump 110	Charge Pump 120	
OFF	OFF	ON	OFF	<i>a second number of booster stages, the second number being less than first number</i>
OFF	ON	ON	parallel-coupled to charge pump 110	
ON	OFF	ON	series-coupled to charge pump 110	<i>a first number of booster stages</i>
ON	ON	N/A	N/A	

EX1006, Javanifard, Table 1, annotated

The table below illustrates example configurations of Example A configurable according to Table 1. The number of configurations would increase for an “X/Y stage pump” (e.g., Example B with a “12/2 stage pump”) as X and/or Y increase. EX1006, FIG. 3, 4:49-55.

Configuration # of Zhang-Javanifard	Selected Power Supply Source	Boost Circuitry Configuration of Javanifard, Table 1	Output Voltage Level
1	Vcc	Row 1 (two stages series-coupled)	Vout Level 1
2	Vcc	Row 2 (charge pumps 110 and 120 parallel-coupled)	Vout Level 1
3	Vcc	Row 3 (four stages series-coupled, as annotated in green in Table 1 above)	Vout Level 2
4	Vpp	Row 1 (two stages series-coupled, as annotated in red in Table 1 above)	Vout Level 2
5	Vpp	Row 2 (charge pumps 110 and 120 parallel-coupled)	Vout Level 2
6	Vpp	Row 3 (four stages series-coupled)	Vout Level 3

As shown in Example A, some configurations (e.g., configurations 1 (and 2) and 3 for Vcc) enable different output voltage levels (Voltage Levels 1 and 2) with the same input level, and some configurations (e.g., configurations 3, 4, and 5 for Vcc and Vpp) enable a given output voltage level (e.g., Vout Level 2) with different input levels. Moreover, in Zhang-Javanifard, a given output voltage level (e.g., Vout Levels 1, 2, or 3) is not limited to *only a single fixed level*, and could

be configured to different given output voltage levels based on different specifications.

Additionally, this table illustrates another motivation not contested by PO: Javanifard provides the configurability of the stage topology including the coupling of stages in series/parallel for different output current levels (e.g., configurations 1 and 2), which provides flexibility for various design needs (e.g., power save mode, output current levels). Pet. 21; *see generally* POR, 12-24.

Accordingly, PO's arguments fail because they mischaracterize Zhang-Javanifard, and misrepresent *example* configurations of Zhang-Javanifard for a given output level (which can be configured to different levels) as *limiting* Zhang-Javanifard to only a single fixed output level. *See*, e.g., POR, 5, 8 (relying on Petition's analysis based on example configurations stating "*e.g.*, for generating the same output voltage" (Pet. 36) and for dependent Claim 2).

B. PO's arguments that Javanifard has potential benefits not applying to Zhang should be rejected.

PO presents extensive arguments contending that numerous potential benefits (e.g., multiple output levels, area reduction, performance improvement including pump efficiency) of Javanifard "do not apply to Zhang." POR, 12-24. However, PO's arguments are irrelevant, and are also incorrect both legally and technically.

First, PO's arguments are irrelevant, because the uncontested foundational advantage of Javanifard—configurability of the stage topology that enables those potential benefits based on design needs—*alone* is sufficient for motivation to combine Zhang and Javanifard. *See e.g.*, EX1006, 1:8-11 (Javanifard relates to “providing a charge pump having *a variable number as opposed to a fixed number of stages* according to charge pump power supply input levels and desired charge pump output levels.”). Each of Javanifard's embodiments (e.g., FIGS. 1, 2, or 3) provides this uncontested foundational advantage of a variable stage charge pump.

This undisputed foundational advantage of Javanifard is further supported by the well-known knowledge that stage topology (including the number of stages and coupling thereof) is critical for charge pump design. For example, the number of stages determines voltage boosting capabilities, and impacts critical performance factors such as efficiency, current output, and overall circuit complexity. *See, e.g.*, EX1003, ¶36 (“Each stage in the charge pump contributes to increasing the voltage level, and *the total voltage boost* is the cumulative effect of *all the stages*.”); EX1026, 1535 (providing “an optimized strategy for designing charge pumps with *minimum power consumption*” by “defin[ing] *the number of stages* that, for a given input, and an output voltage, *maximize power efficiency*”), 1537 (defining “charge-pump efficiency” as the ratio of output power over input power); EX1030,

1:15-2:17 (describing a variable stage charge pump, where “[i]n order to *maximize the current output* from the charge pump,...*the number of stages N can be opportunely chosen.*”); EX1020, 261.

This need for configurability of stage topology including stage numbers is the exact alleged problem of the claims of the '701 Patent. *See e.g.*, '701 Patent, 8:15-21 (“it is preferred in terms of obtaining *good voltage conversion efficiency* that the number of stages be made as small as possible”), 9:45-60; EX1002, 28 (Examiner’s statement of reasons for allowance based on the claimed feature of configuring the stage numbers).

Second, PO’s attempt to limit Petitioner’s motivations within Javanifard’s articulated benefits is contrary to the law. The law is clear that it does not require motivations to be articulated in the references themselves. *Outdry Techs.*, 859 F.3d at 1370–71.

PO also argues that Javanifard’s articulated prior art disadvantages do not apply to Zhang, because Zhang is not a specific prior art reference explicitly referenced in Javanifard. POR, 13-14. However, whether Zhang is explicitly referenced in Javanifard is irrelevant, because Javanifard’s disclosure and benefits are evaluated from the perspective and knowledge of a POSITA.

Regardless, Petitioner has provided **both** motivations articulated in Javanifard itself **and** motivations supported by evidence of the knowledge of a skilled artisan, each sufficient to combine Zhang and Javanifard.

Third, PO's arguments related to Javanifard's potential benefits are also technically incorrect. They are only supported by conclusory testimony from its expert Dr. Jacob, who admitted having no real-world charge pump design experience and even denied that power loss is related to the performance of charge pump. EX1029, 37:20-38:10 (Dr. Jacob denying that power loss is even related to the performance of charge pump), 41:12-23 (admitting that he had never measured the performance of charge pump), 45:13-17 (admitting no experience for designing commercially used charge pumps).

Specifically, regarding area reduction, PO argues circularly that it does not apply to Zhang because Zhang's system does not provide multiple output levels and as such requires "only a **single** charge pump circuit." POR, 14-15, 17. PO fails to dispute that providing multiple higher voltage levels was a well-known need in the electronics field, which applies to Zhang. *See, e.g.*, EX1006, 1:31-33. In fact, Zhang's lack of multiple output levels alone provides a motivation to combine: Javanifard's variable stage charge pump provides a suitable option for addressing Zhang's need for multiple output levels.

Regarding performance benefits including pump efficiency enabled by Javanifard's configurability of the stage topology, PO's arguments that Zhang does not use voltage divider networks (POR, 17-18) and is allegedly "extremely efficient" in time are completely misplaced, failing to address Javanifard's performance advantage including power conversion efficiency. POR, 17-18 (citing EX1003, ¶78 related to "achieve higher voltage *more quickly*"). Such misplacements are consistent with Dr. Jacob's lack of experience with charge pump performance (including power conversion efficiency) as admitted at deposition:

12	Q. How do you usually measure the performance?
13	A. I don't --
14	MR. MILKEY: Objection to form.
15	THE WITNESS: I'm sorry. I don't measure
16	performance of charge pump.
17	BY MS. SHI:
18	Q. You have never measured the performance of a
19	charge pump.
20	A. I don't. It's not something that I do.
21	Q. So when you designed --
22	A. What I care about is what voltage it produces
23	and that is basically it.

EX1029, 41:12-23; *see also* EX1029, 37:20-38:10 (Dr. Jacob denying that power loss is even related to the performance of charge pump), 45:13-17.

Dr. Jacob's failure to recognize, much less consider in his analysis, the well-known knowledge that pump power efficiency (also referred as efficiency in the art) was critical for charge pump design. *See, e.g.*, EX1027, 22 (providing pump efficiency as a critical design factor for charge pumps); EX1020, Kang, FIGs. 4(a) and 4(b); EX1006, 1:66-2:2 ("the ***fixed*** stage method ***typically*** sacrifices ***performance*** at one power supply voltage to accommodate another power supply voltage"); EX1026, 1535 (describing that the number of stages impacts pump performance including power conversion efficiency); EX1030, 1:15-2:17; *see also* '701 Patent, 8:15-21; 9:45-47; 9:58-60 (describing the impact of stage numbers on power conversion efficiency).

Additionally, PO does not even dispute Javanifard's benefits of "flexibility for design needs (e.g., power saving mode, and current requirements)" achieved by configurability of the stage number as explained by Petition. Pet., 20-21. PO only argues that Zhang is "flexible" because it "allows one to reach ***any desired output level*** by adjusting the Vref voltage." POR, 18. As an initial matter, PO's assertion to "to reach ***any desired*** output level" by adjusting Vref is incorrect, because Vref is only used regulate and fine tune Vout within the output voltage range determined by the stage numbers. EX1003, ¶35-38 (explaining that a regulator regulates Vout within the output range determined by the number of stages, citing

EX1014, Frulio, FIGS. 1-2, 1:40-47); EX1005, FIG. 2 (illustrating that Vref 270 is used to regulate Vout of variable stage charge pumps); EX1014, Frulio, FIG. 7.

Furthermore, PO's argument that a different technique (e.g., adjusting Vref) could have been implemented in Zhang for achieving multiple output voltage levels is not relevant to the combination, because "[i]t's not necessary to show that a combination is 'the best option, only that it be a suitable option.'" *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021).

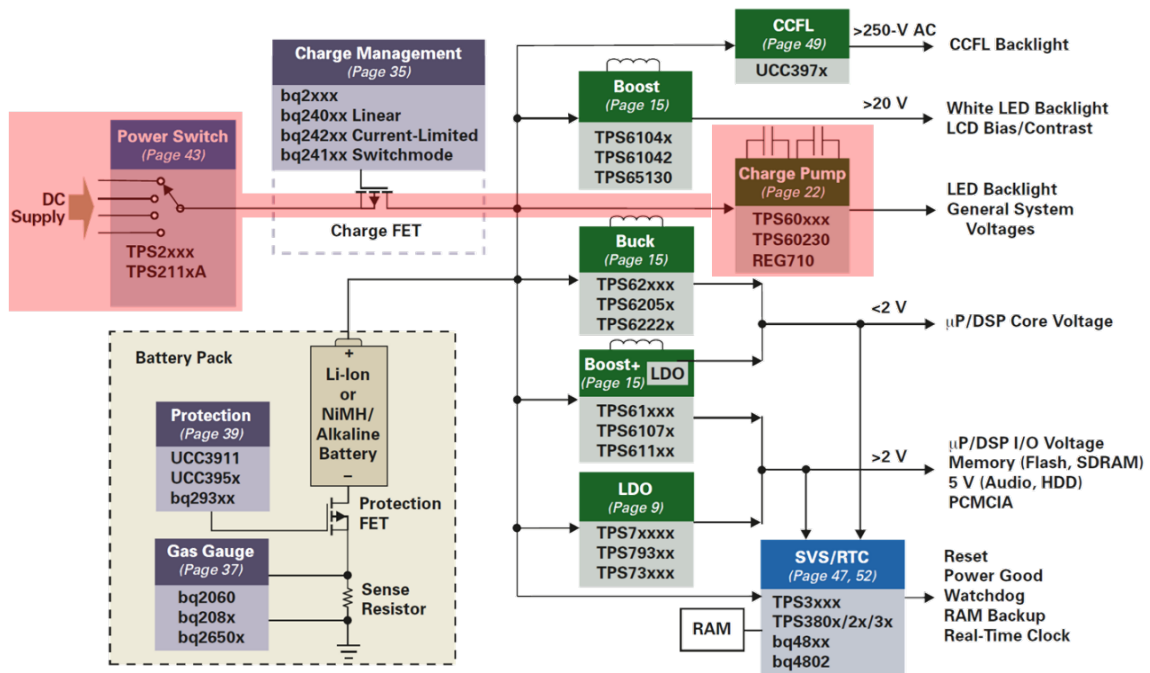
C. PO fails to perform the correct *KSR* analysis.

a. Record supports Petition's combination under *KSR*.

PO states that Petition's combination reasoning involving "known elements" and "known methods" is unsupported, asserting that "a POSITA would recognize that IC design is far from straightforward when analog design techniques (such as charge pump circuits) are used," and that the combination requires "a complete reworking of various functionality within Zhang" including "removing the control circuitry of Zhang." POR, 24-26, 28-30. PO's arguments are contrary to the record, and incorrectly require bodily incorporation.

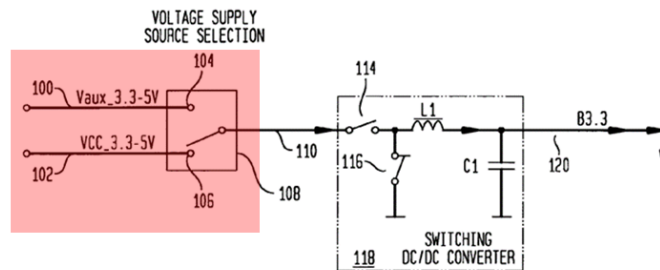
First, as shown in annotated figures below, combining known elements (power supply selection e.g., using a power switch) and voltage conversion (e.g., a DC/DC converter including charge pumps) was a basic and well-known practice prior to the '701 Patent. EX1027, 3, 22, 43; EX1025, FIG. 1, 2:5-7.

Portable Power Solutions



EX1027, 3, annotated

FIG. 1
(PRIOR ART)



EX1025, FIG. 1, annotated

This is supported by prior art, knowledge in the art, and the '701 Patent itself. *See e.g.*, EX1006, FIG. 2; EX1027, 2 (Texas Instruments (TI), an industry leader in power solutions, “makes designing easier by providing leading-edge support tools such as training, a broad selection of evaluation modules (EVMs),

application notes, comprehensive technical documentation and more.”), 16

(illustrating an example power supply design software tool “that speeds novice designers and veteran power supply engineers”), 22, 43; EX1028, 1 (TI websites providing various technical documents); *see also* ’701 Patent, FIG. 1 and claim 1 (mentioning ***no*** “risk of unanticipated effects” for coupling power supply selection to the booster circuitry).

Second, PO’s arguments (POR, 25-26, n.9; 29) incorrectly require bodily incorporation, because combining the teachings of Zhang and Javanifard does not require “a complete reworking of various functionality within Zhang” or “removing the control circuitry of Zhang” as asserted by PO. “The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference.... Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art.” *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981).

PO’s argument that “one ***cannot*** use Zhang’s selecting circuit block 200 without also providing a control mechanism” (POR, 34) directly contradicts Zhang’s disclosure. *See, e.g.*, EX1005, claim 1 (claiming a charge pump circuit without requiring an oscillator and a voltage level sensing block). To the extent that such a control mechanism (well-known as regulator) is desirable in Zhang-

Javanifard based on design needs, its implementation would have been within a POSITA's skills. Pet., 22-23; EX1006, FIG. 2 (implementing the variable stage charge pump *with* regulators based on Vref); EX1003, ¶¶35-38 (citing EX1014, Frulio, 1:40-47, FIGS. 1-2); EX1014, Frulio, FIG. 3A (illustrating well-known pulse-skip regulation).

In fact, PO's reliance on Pan's (EX2005) "inherent risk of unanticipated effects" description in charge pump design supports Petition's combination. PO fails to show how Pan's "inherent risk of unanticipated effects" even applies to Petition's coupling a charge pump and power supply selection. Regardless, Pan provided that well-known techniques (e.g., "meticulous design techniques, intensive semiconductor device analysis, careful design layout planning, and accurate parasitic extraction process") were within a POSITA's skills to address this well-known risk if needed. *See* POR, 25; EX1006, FIG. 2; EX1027, 3, 43, 22, 16; and EX1025, FIG. 1; *see also* '701 Patent, FIG. 1.

b. PO's "changes the principle of operation" arguments fail.

Citing *Adidas AG v. Nike, Inc.*, 963 F.3d 1355, 1359 (Fed. Cir. 2020), PO argues that Zhang-Javanifard "changes the principle of operation of Zhang's selecting circuit block 200," because Zhang's selecting circuit block "is to switch between an external supply voltage and the chip's operating voltage" "allowing for both a general operation mode and a test mode," while in the combination

“Javanifard would switch between different operating voltages *during operation*.”

POR, 27 (emphasis original).

PO's reliance on *Adidas AG* is inapposite, because unlike *Adidas AG*, here PO fails to allege any fundamental difference between Javanifard and Zhang that would affect the motivation to combine inquiry. *See Adidas AG*, at 1358-59 (finding that “the Board properly considered the fundamental differences in the seaming techniques of Reed and Nishida”).

PO's mischaracterization of Zhang as limited to *only* a general operation mode and a test mode is contrary to the record. Pet. 22 (EX1005, 5:23–51 (“claiming a charge pump circuit including a selector circuit without any operation mode requirement”)); Pet. 25 (Ex. 1005, 3:21-27 (“The high voltage VPP may be applied externally in the test operation mode as well as during the general operation mode.”)).

Similarly, PO's mischaracterization of Javanifard and Zhang-Javanifard as limited to *only* switching “during operation” is contrary to the record. POR, 27. *See, e.g.*, EX1006, claim 1 (claiming a variable stage charge pump without any requirement of “during operation”); EX1003, ¶163 (Dr. Stiegler explaining, in undisputed claim 7 analysis, it would have been obvious to configure the variable stage charge pump “with a selected one of a metal option, a bonding option, and a fuse option,” and accordingly switching could operate during any stage (e.g.,

manufacture, packaging, testing, operation) based on design needs); EX1031, 3 (“an electrical fuse, can be cut...**at any stage** during manufacture and operation including the package stage.”); *see also* ’701 Patent, claim 1, 3:18-19 (providing that “the switch circuit group is controlled by any of a metal option, fuse option and bonding option,” without any limitation to **only** switching “during operation”).

c. Petition’s analysis is based on the prior art—not hindsight.

PO states that Petition’s combination is not “advantageous over the disclosures of either Zhang or Javanifard,” which “is strongly suggestive of improper hindsight reasoning.” POR, 32. PO’s hindsight arguments fail because they are contradictory to both the law and the record.

First, the law is clear that it does not require Petitioner to show that the combination was “an improvement in a categorical sense.” *Intel Corp. v. PACT XPP SCHWEIZ AG*, 61 F.4th 1373, 1381 (Fed. Cir. 2023). Like *Intel*, here, Petitioner has shown that Javanifard’s variable stage charge pump was a suitable option to implement Zhang’s charge pump (e.g., the “charge pump block” claimed in Zhang claim 1, the example fixed stage charge pump 100 of Zhang, FIG. 4).

Second, Zhang-Javanifard improves Zhang with the advantage of Javanifard's variable stage charge pump, including the configurability of the stage topology and numerous benefits enabled thereby.¹

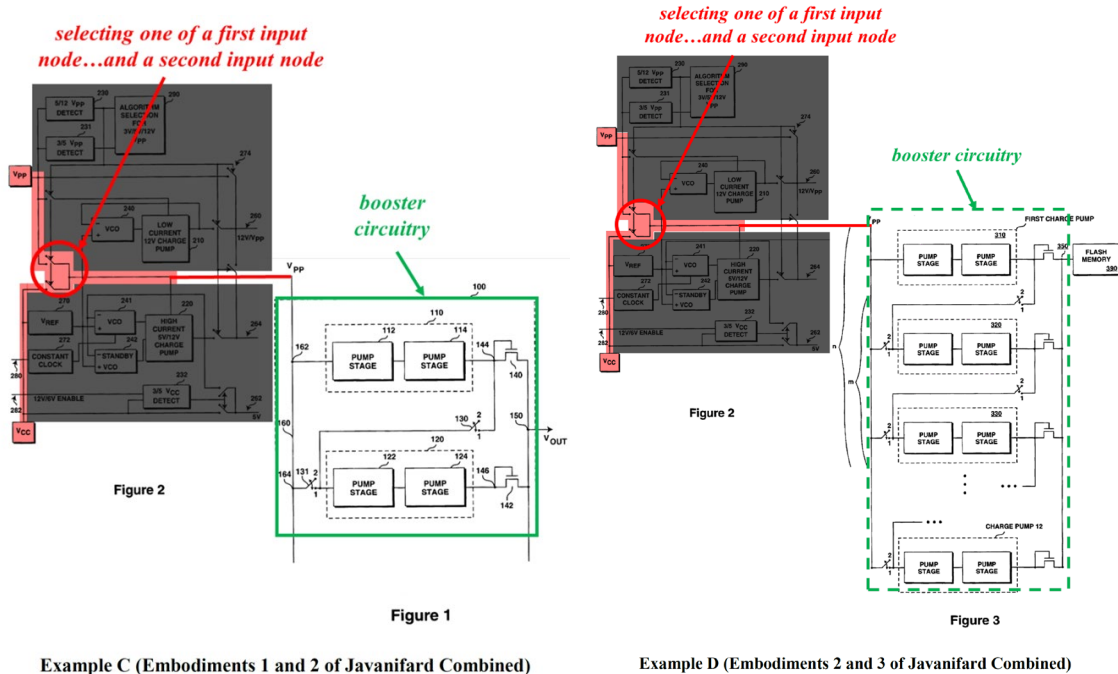
PO then argues that hindsight "was confirmed by Petitioner's expert, who testified that 'of course' he used the "claim language as a roadmap.'" POR, 34. However, Dr. Stiegler performed the exact correct motivation to combine analysis under *KSR*, giving technical reasons why a POSITA would combine the art. *KSR*, at 1735 ("Under the correct analysis, any need or problem known in the field and addressed by the patent can provide a reason for ***combining the elements in the manner claimed.***"). Also, Dr. Stiegler, who is not an attorney, but rather a career-long chip designer, explained what he meant by using the claim language as a roadmap—he first read the patent and claims to understand its technical content. EX2004, 38:12-20.

¹ PO's assertion that Zhang-Javanifard lacks advantage over Javanifard is even less irrelevant under *Intel*, but regardless, Zhang-Javanifard provides multi-power-source selection over Javanifard's FIGS. 1 and 3, and provides over FIG. 2 the advantages of using a single variable stage charge pump instead of two for less design complexity, lower cost, reduced area, and a broader range of applications.

V. Ground 2: Javanifard Renders the Claims Obvious.

As Petition pointed out, Javanifard's Embodiment 1 (FIG. 1 and Table 1) and Embodiment 3 (FIG. 3) each describe a variable stage charge pump supplied with a single power supply source line Vpp. Pet. 62-65, EX1003, ¶¶203-209. Javanifard's Embodiment 2 (FIG. 2 and Tables 2, 3) describes selecting from power supply source lines Vcc and Vpp and providing the selected power supply source to variable stage charge pumps. *Id.* A POSITA would have understood that Embodiments 1 and 3 each have the need of supplying their variable stage charge pump with "*different power supply source lines*" (Pet. 64) (e.g., Vcc and Vpp), that Embodiment 2's power source selection provides a suitable option for addressing this need, and modifying Embodiments 1 and 3 with the power source selection teaching of Embodiment 2 was within the skills of a POSITA. Nothing more is required to show a motivation to combine (although the present paper will still address the PO's additional arguments below). *Intel*, 61 F. 4th at 1381 ("It's enough for [patent-challenger] to show that there was a known problem of cache coherency in the art, that Bauman's secondary cache helped address that issue, and that combining the teachings of Kabemoto and Bauman wasn't beyond the skill of an ordinary artisan. Nothing more is required to show a motivation to combine under *KSR*.").

As illustrated below, Petition's Example C illustrates combination of Javanifard Embodiments 1 and 2 (hereinafter "Javanifard Combination 1-2"), and Example D illustrates combination of Javanifard Embodiments 3 and 2 (hereinafter "Javanifard Combination 3-2").² Petition, 71-72.



As illustrated in the side-by-side illustration of Petition's Example C and FIG. 1 of '701 Patent below, Javanifard Combination 1-2 discloses the purported invention as claimed in '701 Patent, because it provides a power supply source selector coupled to a variable stage charge pump, where the pump stage topology

² These illustrations include greyed-out circuits not used in the combination. In analysis below, the greyed-out circuits are removed from the figures to avoid any confusion and making the combined figures easier to read.

including the stage numbers is configurable based on the selected power supply source. *See also* '701 Patent, Claim 1.

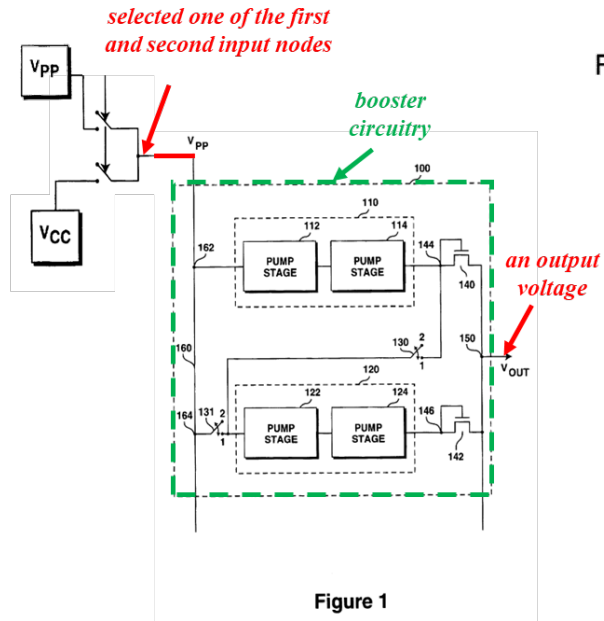
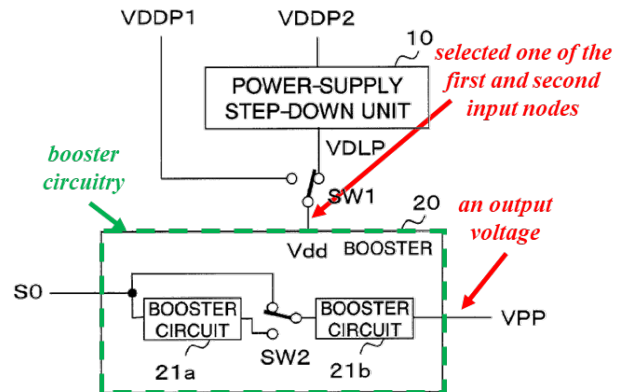


FIG.1



Example C (Javanifard Combination 1-2) vs. '701 Patent, FIG. 1

Similarly, as illustrated below, Javanifard Combination 3-2 (Petition's Example D) also discloses the purported invention as claimed in '701 Patent.

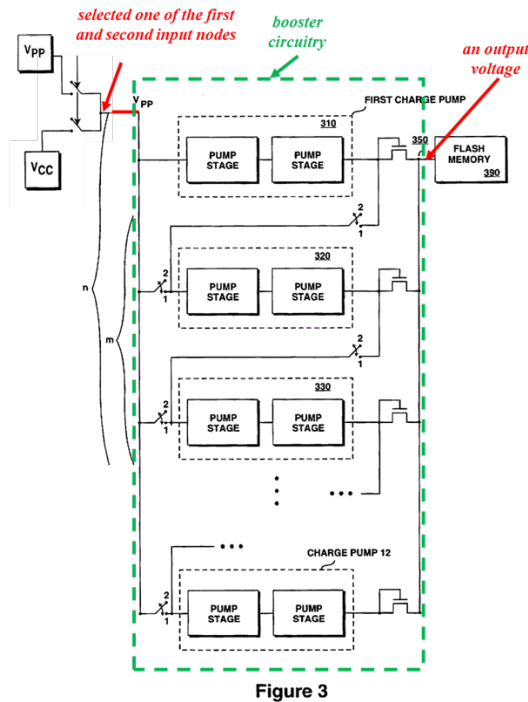
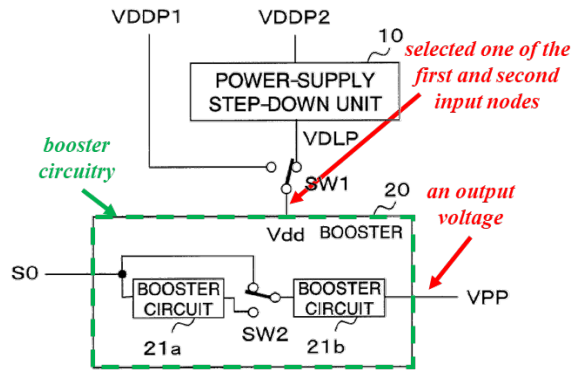


FIG.1



Example D (Javanifard Combination 3-2) vs. '701 Patent, FIG. 1

PO's arguments are not even directed at the combination presented by Petition. They do not dispute that Embodiments 1 and 3 each have the need of supplying their variable stage charge pump with “*different power supply source lines*,” do not dispute that Embodiment 2 provides a suitable option for providing power source selection, and do not dispute that modifying Embodiments 1 and 3 with the power source selection teaching of Embodiment 2 was within the skills of a POSITA. *See generally* POR, 38-55.

Instead, PO's arguments disregard Petition's combination of modifying the primary embodiments (Embodiments 1 and 3) with specific features of the secondary embodiment (power supply source selection of Embodiment 2), and

misrepresent Petition's combination as requiring "extensive modifications" to the secondary embodiment (Embodiment 2). *See* POR, 38-55. PO's "inoperable for its intended purpose" and "change the principle of operation" tests were based on the same incorrect requirement of "extensive modifications" to FIG. 2, and should be rejected. *See* POR, 46.

A. Petition's combination proposes no modification to Javanifard's FIG. 2, and PO's attempt to bodily incorporate FIG. 2 should be rejected.

PO states that "Petition proposes extensive modifications to Javanifard's Figure 2 embodiment that a POSITA would not have contemplated in light of Javanifard's own disclosures." POR, 39. That is incorrect.

First, Petition proposes no modification, much less "extensive modification" to Javanifard's Figure 2 as asserted by PO. Petition's combination simply modifies Embodiments 1 and 3 (primary embodiments) by applying the power supply source selection feature of Embodiment 2 (secondary embodiment) to the input of the charge pump. Petition's combination does not modify FIG. 2.

Second, PO's alleged "extensive modifications" to FIG. 2 would be necessary only if a POSITA is required to start from bodily incorporating *entire* FIG. 2 in the combination. This is contrary to the law. *See In re Keller*, 642 F.2d at 425. PO's attempt to bodily incorporate the *entirety* of FIG. 2 in the combination permeates its arguments, and should be rejected. *See, e.g.*, POR, 42

(misrepresenting that “Petition proposes removing *nearly all* of the functionality of Javanifard’s Figure 2”); 43-44; 46.

B. PO’s “inoperable” and “change the principle of operation” arguments fail.

PO repeatedly cites to Javanifard at 6:56-60 stating that “[t]o maximize the utility of a flash memory system, however, the variable stage charge pump *must be able* to generate approximately 5 volts, 9 volts, and 12 volts from either a 3.3 volt or 5 volt power supply” (referred to herein as “Javanifard’s must-be-able-to statement”). POR, 45-46. PO asserts, that “Javanifard is explicit that the ability to handle three different output voltages in response to variation in input voltage is a *mandatory* aspect of its system.” POR, 45 (emphasis original). PO’s arguments at least fail because they are based on its purported “extensive modifications” to Figure 2. *See* V.A. They are also contrary to the record and the law.

a. Javanifard does not impose a “mandatory” intended purpose on any of FIGS. 1, 2, and 3 embodiments.

Javanifard’s must-be-able-to statement merely describes a specific example embodiment that includes a *single* variable stage charge pump. *See* EX1006, 6:5-7 (“*In one embodiment*, a variable stage charge pump *might* be used to provide the various voltage levels required by a flash memory array.”), followed by 6:56-60 (“...*the variable stage charge pump* must be able to...”). As such, it cannot

impose a mandatory intended purpose to FIG. 2 including multiple variable stage charge pumps.

Similarly, it is undisputed that Javanifard does not impose such a mandatory intended purpose to FIGS. 1 and 3. *See* EX1006, FIGS. 1, 3, claims 1-4 (describing/claiming a variable stage charge pump without limiting its application to a flash memory system with specific input/output levels); 6:5-7; 8:53-57. PO also fails to explain why its purported requirement *only* selectively applies to Embodiment 2, but not other embodiments, in particular Embodiment 3 coupled to a flash memory system. EX1006, FIG. 3.

b. PO's "inoperable" argument is contrary to the law, which does not apply to the secondary reference.

Citing *Plas-Pak Indus., Inc. v. Sulzer Mixpac AG* 600 F. App'x 755, 760 (Fed. Cir. 2015), PO states that "Petition proposes extensive modifications to Javanifard's Figure 2 embodiment...in a way that would render that embodiment inoperable for its intended purpose..." POR, 39, 46-47.

PO's reliance on *In re Schweickert* and *Plas-Pak* is misplaced, because the inoperable test described therein is directed at *the primary reference* being modified with the special features of the secondary reference. POR, 46 (citing *In re Schweickert* for the assertion of "'defeat[ing] the purpose of' *the system being modified*"); *Plas-Pak Indus.*, 600 Fed.Appx. at 760 (Fed. Cir. agreed with the Board's finding that "modifying [primary reference] to accommodate the spray

nozzle [of secondary reference] would *render [primary-reference]* ‘inoperable for its intended purpose.’”).³ PO’s arguments directed at FIG. 2 are contrary to the law, because in Petition’s combination, FIGS. 1 and 3 are the primary reference/embodiments being modified with specific features of FIG. 2.

c. PO’s reliance on Petitioner’s dependent claim 2 analysis to limit Petition’s combination as “would be configured to provide only a *single* level of voltage output” is misplaced.

PO states, “Petition alleges that its combination would satisfy *claim 2* of the ’701 Patent, wherein the “output voltage is the same when the first input node is selected and when the second input node is selected” (see Pet. 81; Ex.1001, Claim 2), further emphasizing that Petition’s combination would be configured to *provide only a single level of voltage output*, not the three levels Javanifard teaches are necessary.” POR, 46.

For similar reasons discussed above in Ground 1 at IV.A, none of Javanifard’s embodiments and Petition’s combination requires only a single level of voltage output. Furthermore, PO’s arguments are not addressing any claim element of the ’701 Patent. Even claim 2 cited by PO only requires that “the output voltage *is the same* when the first input node is selected and when the second input node is selected,” and does not limit the output voltage to be only a single fixed

³ This very principle is also discussed at MPEP §2145.

level. Under claim 2, the output voltage can be the same voltage level for both input nodes during a first time period, and another same voltage level during a second time period.

C. PO's no advantages beyond Javanifard's Figure-2 arguments are contrary to the law and the record.

PO states that a POSITA would not be motivated to “modify Javanifard to achieve a result that was already thought by Javanifard's Figure 2,” (POR, 50), relying upon Dr. Jacob's opinion that “combining Javanifard with itself provides no advantages beyond Javanifard's Figure-2 embodiment alone.” EX2003, ¶¶133-140. PO's argument should be rejected, because it is contrary to the law and the record of evidence.

a. Petition's identified problem of Embodiments 1 and 3 and the combination' improvement thereof are not disputed.

PO states that “Petition alleges *no problem* in Javanifard” resolved by Petition's combination. POR, 48-49. Not so. Petition acknowledges that Javanifard (including each of its FIGS. 1, 2, and 3 embodiments) *already* accommodates *both* “different output levels for a given charge pump power supply input level” and “a given output level for different charge pump power supply input levels.” Pet., 10-16; EX1003, ¶¶72-82. Petition explains the need of FIGS. 1 and 3 to receive different input levels at its input node “*provided by different power supply source lines.*” Pet., 64; EX1003, ¶207; EX1006, 6:44-46; EX1005, Abstract, FIG. 4. Petition explains that

the power source line selection feature of FIG. 2 is a known technique for this need, and applying this technique to FIGS. 1 and 3 is within a POSITA's skill. Pet. 63-65.

b. PO's requirement of advantages beyond Javanifard's Figure 2 is contrary to law.

The law does not require Petitioner to show that the combination was "an improvement in a categorical sense." *Intel Corp. v. PACT XPP SCHWEIZ AG*, 61 F. 4th at 1381. Like *Intel*, Petitioner has shown that Javanifard Embodiment 2's teaching of power supply source selection is a suitable option for enabling Javanifard Embodiments 1 and 3 to support multiple power supply source lines, which is sufficient to show motivation to combine.

c. Petition's combination provides various advantages over FIG. 2.

Regardless, contrary to PO's assertion, Petition's combination provide various improvements to Javanifard's Figure-2 embodiment, including (1) area savings/reduced cost/reduced complexity by using a single variable stage charge pump instead of two charge pumps; (2) a broader range of applications (e.g., LEDs, PCMCIA/CardBus applications, "power ICs, filters, memories, etc.") not limited to flash memory systems (EX1014, Frulio, 1:15-16; EX1027, 3, 22, 43); (3) flexibility for different design specifications. *See* EX1029, 58:17-19 (Dr. Jacob agreed that dealing with trade-off between overdesign and underdesign is a general issue in circuit design, stating "[a]ll designers want to come up with something that's appropriate.").

D. Petition's combination is further supported by PO's admission of an "extremely straightforward" Javanifard combination.

PO states, "a POSITA reviewing Javanifard would have understood that Javanifard's variable-stage charge pumps 210 and 220 of Figure 2 would be implemented using the structures of Javanifard's Figure 1 and/or Figure 3," which is an "*extremely straightforward* combination."⁴ POR, 42, and 50 n.12.

Like PO's proposed combination, Petition's combination also involves the technique of coupling the power supply source selection of FIG. 2 with the variable stage charge pump of FIGS. 1 and 3. As such, PO's arguments support Petition's combination, because it admits that this technique applied in Petition's combination is extremely straightforward.

⁴ PO presents a long and convoluted explanation why its proposed combination does not render obvious the Challenged Claims, but it is incorrectly based on a zero-volts V_{pp} directly contradicting with Javanifard's disclosure that V_{pp} is 5V .
POR, 52-53 n.13.

VI. Conclusion

The Board should find all challenged claims unpatentable.

Respectfully submitted,

Dated: July 30, 2024

/David M. O'Dell/
David M. O'Dell
Lead Counsel for Petitioner
Registration No. 42,044

VII. Certificate of Word Count

Pursuant to 37 C.F.R. § 42.24, the undersigned attorney for the Petitioner declares that the argument section of this Petition (Sections I-VI) has a total of 5,489 words, according to the word count tool in Microsoft Word™.

/David M. O'Dell/
David M. O'Dell
Lead Counsel for Petitioner
Registration No. 42,044

CERTIFICATE OF SERVICE

Date of service July 30, 2024

Manner of service Electronic Mail:
jmilkey@raklaw.com
ptong@raklaw.com
pkroeger@raklaw.com
bledahl@raklaw.com

Documents served **PETITIONER'S REPLY;
Petitioner's Updated Exhibit List; and
Exhibits EX1025 - EX1031**

Persons served James Milkey
Qi Tong
Paul A. Kroeger
Brian D. Ledahl
RUSS AUGUST & KABAT
12424 Wilshire Blvd., 12th Fl.
Los Angeles, CA 90025

/David M. O'Dell/
David M O'Dell
Lead Counsel for Petitioner
Registration No. 40,107