

Charge-Pump Circuits: Power-Consumption Optimization

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Abstract—In this paper, an optimized strategy for designing charge pumps with minimum power consumption is presented. The approach allows designers to define the number of stages that, for a given input, and an output voltage, maximize power efficiency. Capacitor value is then set to provide the current capability required. This approach was analytically developed and validated through simulations and experimental measurements on 0.35- μm EEPROM CMOS technology. This approach was then compared with one which minimized the silicon area and it was shown that only a small increase in area is needed to minimize power consumption.

Index Terms—Charge pump, integrated circuit (IC), power consumption, voltage multiplier.

I. INTRODUCTION

THE REDUCTION of power consumption has become one of the dominant-design aspects for many very large-integration systems (VLSI) systems. In general, the most common and efficient way to cut down power consumption in digital systems is to reduce the power-supply voltage. To reduce power consumption in electronic systems, the standard supply voltage tends to scale down to values as low as 1.5 V or lower [1]–[6]. However, too low a power supply can greatly reduce the circuit performance. Indeed, there ensues a reduction in speed and noise margins in digital circuits [5], [6], a reduction of dynamic range in analog circuits [4], and additionally, difficulties arise in allowing read and write operations to take place in memories [7]. To avoid these drawbacks, charge-pump circuits providing output voltages higher than the power supply, which are commonly used in nonvolatile memories [8]–[12] and in smart power integrated circuits (ICs) [13]–[17], will also be extensively used inside IC systems in the future [18]–[20].

In his first integrated version of charge pumps, Dickson [21] proposed their theoretical analysis and modeling. In particular, Dickson's paper [21] introduced their static behavior, further developed by assuming MOS diodes in [22], while their dynamic behavior was to be discussed in papers [23]–[26]. Some of these papers report design strategies. To this end, an interesting work which gives guidelines for minimizing area by assuming fixed drive capability has recently been presented in [27].

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In some papers, even if the power consumption is discussed in a general way, there is no clear presentation of a design strategy to minimize it. This, despite the fact, that the power consumption of charge pumps is not negligible, especially in memory applications and its minimization is an important target to pursue. Indeed, charge pumps that try to improve their efficiency through topological solutions have recently been proposed [28]–[31].

In this paper, we present a methodology for designing charge pumps with a minimum power consumption which is independent of their specific topological implementation. The approach is based on a simple analytical model and can be performed in a pencil-and-paper manner.

In Section II, starting from the main relationship that models charge-pump behavior, the terms of power consumption are derived and discussed. The ideal case without losses is developed in Appendix II. The number of stages which minimize power consumption together with an example showing their use during the design of the derived result and the efficiency of the optimized charge pump are discussed in Section III. Simulation and experimental measurements were carried out to validate the model used to optimize consumption. In particular, the technology used was the F6Y EEPROM by ST Microelectronics (a 0.35 μm CMOS). A summary of simulations and experimental results is given in Section IV. In Section V, the design strategy proposed to minimize power consumption is compared with the traditional approach that minimizes silicon area. Final conclusions are given in Section VI. In addition, a demonstration that the best choice is to have each stage with equal capacitance C and the development of ideal charge-pump consumption are reported in Appendixes I and II, respectively.

II. CHARGE-PUMP CONSUMPTION

The first integrated charge pump is reported in Fig. 1(a) [21], and without loss of generality, can be assumed as a model even for the other topologies which use switches instead of diodes. More specifically, implementations which use switches allow us to avoid the threshold voltage of the diode, and are hence more suited to low-voltage implementation. Thus, in the following, we shall consider the charge pump in Fig. 1(a) assuming diodes with an ideal threshold equal to zero and a clock amplitude equal to the power supply V_{DD} or equivalently, the charge pump with ideal switches depicted in Fig. 1(b). Moreover, usually, all stages are assumed to have equal capacitance. Indeed, as demonstrated in Appendix I, this is the design condition which maximizes the driving capability for a defined amount of charge-pump capacitance.

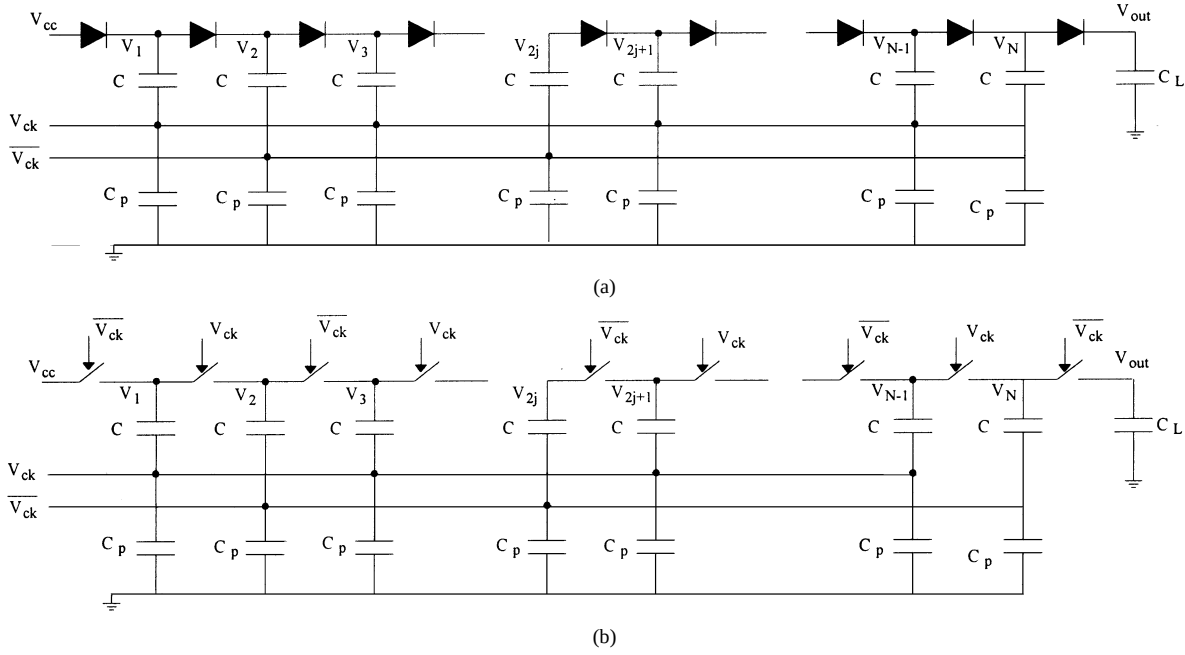


Fig. 1. Charge pump. (a) With diodes. (b) With ideal switches.

Considering a clock frequency f , the output voltage of an N -stage charge pump with ideal diode or switches is equal to [21]

$$V_{\text{out}} = (N + 1)V_{DD} - \frac{NI_L}{fC}. \quad (1)$$

As briefly developed in Appendix II, an ideal charge pump (i.e., without loss) has a current consumption at steady state equal to $(N + 1)I_L$, [22]. However, real charge pumps have losses which reduce their efficiency to values lower than one, as actual current consumption has to take into account other current contributions. Hence, the current consumption of a real charge pump can be modeled as

$$I_{\text{power}} = (N + 1)I_L + I_{\text{ni}} \quad (2)$$

where current I_{ni} represents the nonideality term. In general, the current term I_{ni} is due to the current required to charge and discharge the upper and the bottom parasitic of a stage capacitor C . Thus, after neglecting others losses (such as for example the parasitic in the switches or diodes) and without introducing a significant error, we need only consider parasitic capacitance at the bottom plate, C_p , which is generally more than one order of magnitude higher than that of the other plate. To reduce the loss in the output voltage amplitude, the bottom plate is driven by clock [21], [24]. Hence, the current wasted to charge and discharge the bottom plate parasitic capacitance C_p in each clock period is given by

$$I_{\text{ni}} = NC_p f V_{DD}. \quad (3)$$

Since the bottom-plate parasitic capacitance C_p is proportional to the stage capacitance C , we can rewrite (3) versus C

$$I_{\text{ni}} = \alpha NC f V_{DD} \quad (4)$$

where parameter α is the ratio between the parasitic capacitance at the bottom plate of a stage capacitance and the stage capacitance itself. It is apparent that (4) shows the linear dependence between current I_{ni} and the total capacitance used in the charge pump. Hence, more generally, parameter α can represent a term which links the current loss to the total capacitance of the charge pump and for real charge pump it is greater than zero.

Deriving the capacitance of a stage in (1) we can write

$$C = \frac{NI_L}{[(N + 1)V_{DD} - V_{\text{out}}]f} \quad (5)$$

and substituting (5) in (4), current term I_{ni} becomes

$$I_{\text{ni}} = \alpha \frac{N^2 I_L}{[(N + 1)V_{DD} - V_{\text{out}}]} V_{DD}. \quad (6)$$

Thus, current consumption can be expressed independently of the charge-pump capacitance, and the only design-free variable contained is the number of stages

$$I_{\text{power}} = \left[(N + 1) + \alpha \frac{N^2}{(N + 1)V_{DD} - V_{\text{out}}} V_{DD} \right] I_L. \quad (7)$$

III. POWER-CONSUMPTION MINIMIZATION AND DESIGN STRATEGY

A. Power Minimization

To minimize power consumption, we have to minimize current consumption. Hence, deriving (7) for the number of stages

$$\frac{dI_{\text{power}}}{dN} = \left\{ 1 + \alpha \frac{N[(N + 2)V_{DD} - 2V_{\text{out}}]}{[(N + 1)V_{DD} - V_{\text{out}}]^2} V_{DD} \right\} I_L \quad (8)$$

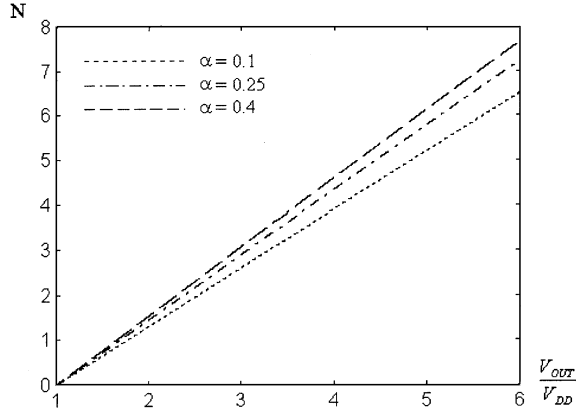


Fig. 2. Minimum number of stages versus the ratio between the output voltage and the power supply for different values of α .

and setting to zero the results, the number of stages that reduces current consumption is given by

$$N_{op} = \left(1 + \sqrt{\frac{\alpha}{1+\alpha}}\right) (K-1) \quad (9)$$

where K is the multiplier factor

$$K = \frac{V_{out}}{V_{DD}}. \quad (10)$$

It is worth noting that the number of stages that optimize power consumption is independent of the load current or the charge-pump capacitances. Even so, it only depends on the multiplier factor, and on the technological parameter α , which gives the degree of capacitor nonideality.

Relationship (9) versus the multiplier factor K is plotted in Fig. 2 for different values of parasitic capacitance percentage, α . Fig. 2 shows a low dependency versus the technological parameter α . And this low dependence is also demonstrated by the sensitivity of (9) for variations of α , which is equal to

$$S_{\alpha}^{N_{op}} = \frac{\alpha}{N_{op}} \frac{dN_{op}}{d\alpha} = \frac{1}{2} \frac{1}{1+\alpha} \frac{1}{1+\sqrt{1+\frac{1}{\alpha}}} \quad (11)$$

and is always lower than one.

Relationship (9) allows us to choose the number of stages independently of the current that the charge pump has to provide. Then, through (5) in which the optimum number of stages is used, we can determine the capacitance value that guarantees the required current capability.

B. Design Example

To better understand the use of the results obtained, consider a typical application in which the charge pump is used to perform the read operation in a smart card powered with a minimum 2.2-V value. The charge pump is adopted here to generate a 5-V voltage to be used during reading operation to speed out access time; and the current required has to be more than 600 μ A. Moreover, assume parameter α to be about equal to 0.2. From (9), we get an optimum number of stages equal to 2. Then, from (5) and assuming a maximum clock frequency equal to 10 MHz, we get a charge-pump capacitance equal to 75 pF (i.e., a total capacitance equal to 150 pF).

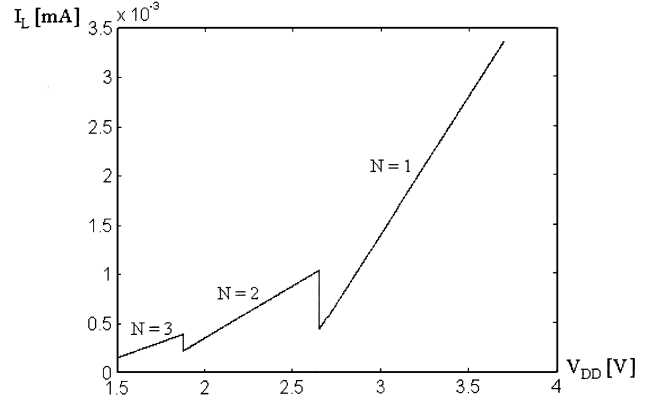


Fig. 3. Maximum current load for the optimum number of stages (150-pF total capacitance, 5-V output voltage and $\alpha = 0.2$).

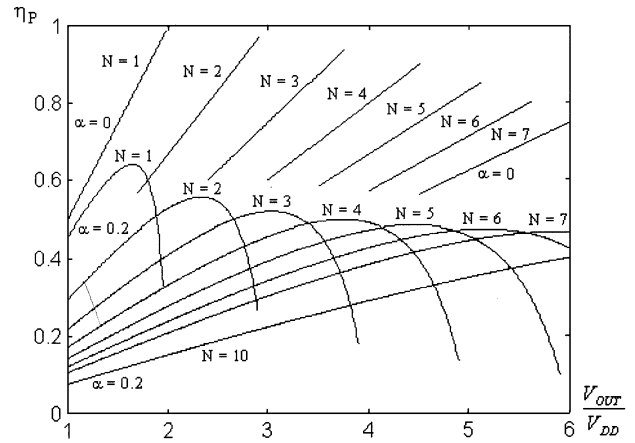


Fig. 4. Charge-pump efficiency versus the multiplier factor for different numbers of stages with $\alpha = 0.2$ and $\alpha = 0$ (ideal case).

To show the drive capability of the designed charge pump, we plot in Fig. 3, the maximum current versus the input voltage of a charge pump with an optimum number of stages, assuming a 150-pF total capacitance, a 5-V output voltage and α equal to 0.2.

C. Charge-Pump Efficiency

The efficiency η_p of the charge pump is equal to

$$\eta_p = \frac{I_L V_{out}}{I_{power} V_{DD}} = \frac{K}{N+1+\alpha \frac{N^2}{N+1-K}} \quad (12)$$

and is plotted in Fig. 4 versus the multiplier factor for a different number of stages and assuming $\alpha = 0.2$. The figure also includes the efficiency of the charge pump for the ideal case in which $\alpha = 0$. By inspection of Fig. 4, we derive that the advantages of using the optimum number of stages decreases for increasing values of the multiplier factor. Indeed, considering a design with the optimum number of stage given by (9) we get the following maximum efficiency:

$$\eta_{p \max} = \frac{K}{1 + \frac{1+\gamma}{1-\gamma} (K-1)} \quad (13)$$

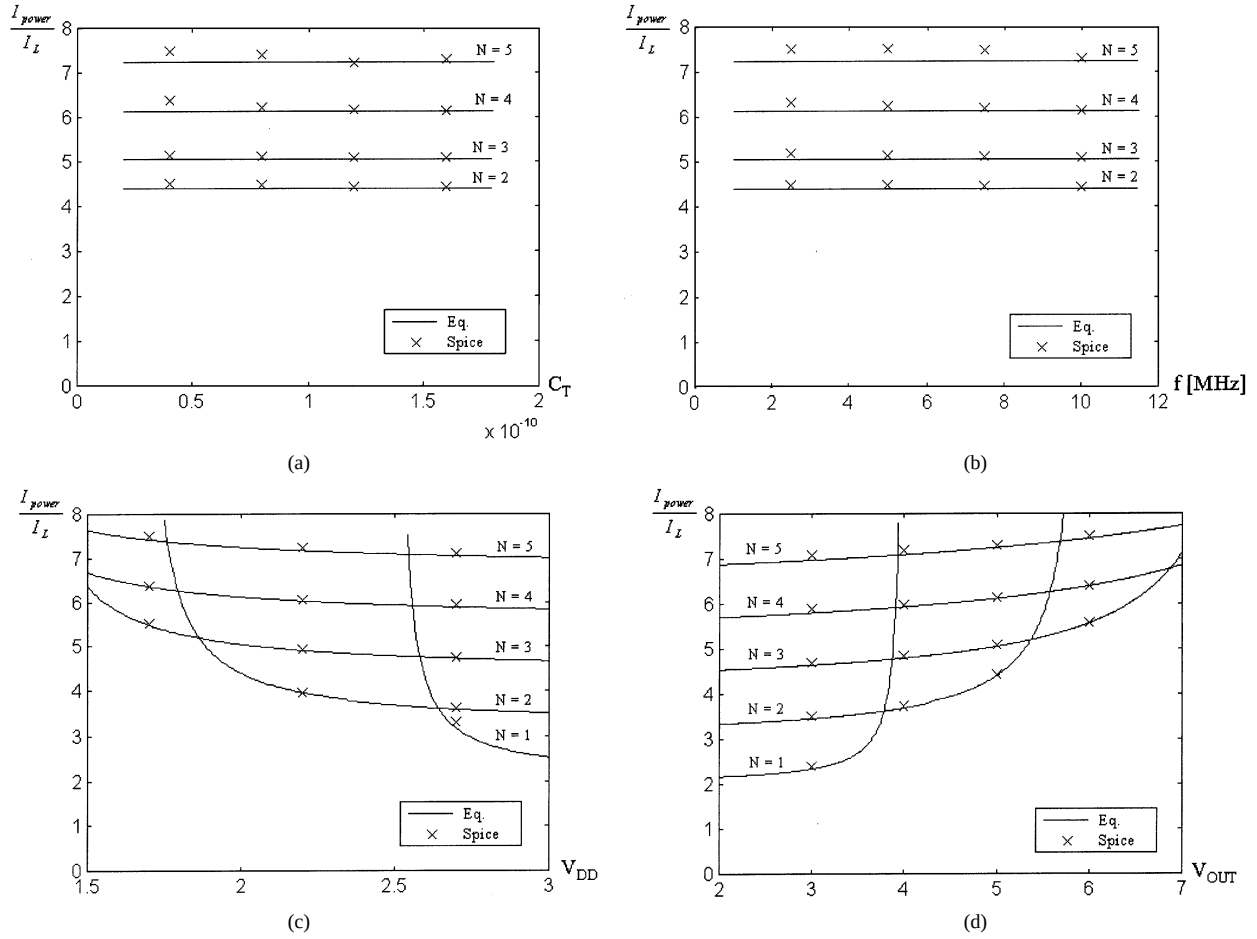


Fig. 5. Comparison between simulated results (crosses) and (7) (continuous line). (a) Versus total capacitance. (b) Versus frequency. (c) Versus power supply. (d) Versus output voltage.

where parameter γ depends only on the technological parameter α and is defined by

$$\gamma = \sqrt{\frac{\alpha}{1+\alpha}}. \quad (14)$$

It is apparent that (13) tends asymptotically to a constant value for increasing values of K .

Sometimes, charge-pump designers prefer to evaluate the ratio of the current sunk from the power supply to that delivered to the load, instead of using the efficiency in (12). This ratio can be simply derived from (12) and is equal to

$$\frac{I_{power}}{I_L} = N + 1 + \alpha \frac{N^2}{N + 1 - K} \quad (15)$$

that in the case of optimum design results

$$\left(\frac{I_{power}}{I_L} \right)_{\min} = 1 + \frac{1+\gamma}{1-\gamma} (K-1). \quad (16)$$

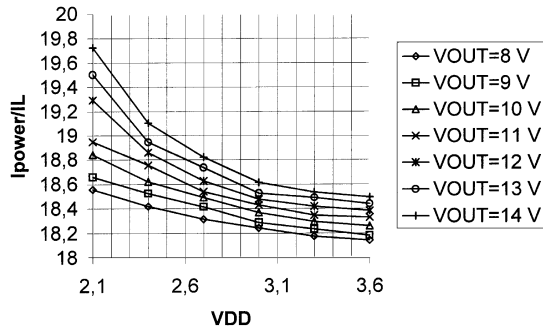
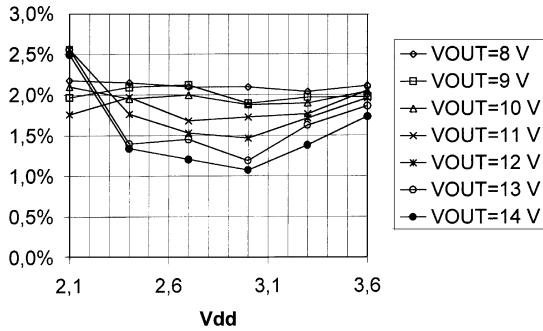
IV. SIMULATION AND EXPERIMENTAL RESULTS

The proposed design strategy was validated using the F6Y technology by ST Microelectronics which is a 0.35- μm EEPROM technology. In this technology, the charge-pump

capacitors are implemented between the polysilicon plate and an n-well, through a gate oxide. The measured α is roughly equal to 0.18. It is worth noting that, as discussed in Section II, parameter α was not measured as the C_p/C ratio which is about equal to 0.12 for the technology considered, but it is instead derived through measurements of the input and output current. However, the low sensitivity of (9) for α does not lead to great differences.

To validate the theoretical analysis developed in Section II, many Eldo simulations were carried out. Charge pumps with a number of stages ranging from 1 to 5 were simulated under many different design conditions. In particular, starting from the design conditions in which the charge-pump capacitance, the frequency, the power supply and the output voltage were set to 160 pF, 10 MHz, and 2 and 5 V, respectively, we varied: the charge-pump capacitance from 40 to 160 pF with a step of 40 pF, the frequency from 2.5 to 10 MHz with a step of 2.5 MHz, the power supply from 1.7 to 2.7 V with a step of 0.5 V, and the output voltage from 3 to 6 V with a step of 1 V.

As shown in Fig. 5, where the analytical value resulting from (7) are plotted with the continuous line and the simulated results are represented by crosses, the simulations agree with the theoretical analysis and a maximum error always lower than 4% was found.

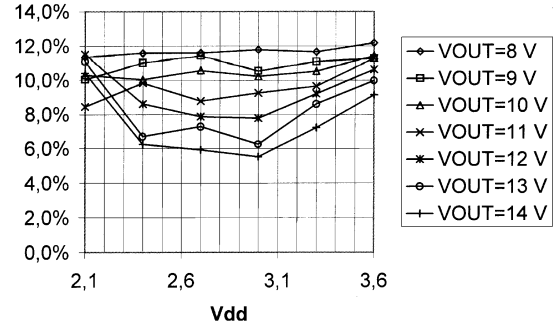
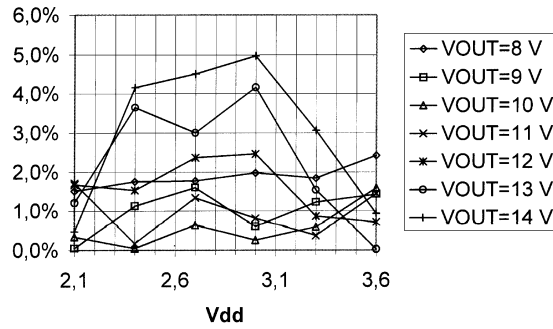
Fig. 6. Measured I_{power}/I_L of a 14-stage charge pump.Fig. 7. Errors on analytical and measured I_{power}/I_L assuming $\alpha = 0.18$.

The proposed model was also experimentally tested. Measurements on a 14-stage charge pump implemented with the same technology used for simulations were carried out. In particular, we varied both the power supply from 2.1 to 3.6 V with a step of 0.3 V, we forced, with a voltage generator, the output voltage, from 8 to 14 V with 1-V steps. The current ratio I_{power}/I_L measured for all these cases is plotted in Fig. 6.

By assuming a value of 0.18 for parameter α , as derived by simulations, we plot the error between the measured and the analytical value given by (7) [i.e., (15)] in Fig. 7. The error found is always lower than 3%. Thus, to better verify the accuracy of our model, we subtracted term $N+1$ both from the measured and the analytical results. This procedure only allows the term dependent on parameter α to be compared. The error is plotted in Fig. 8 and is always lower than 15%. Finally, to better tune the value of parameter α , we derived it from one set of measurements. The value obtained was 0.2. This was because the charge pump measured underwent a further loss due to the phase generator not included in the simulations. The error found on the measured and analytical current ratio by subtracting $N+1$ with $\alpha = 0.2$ is plotted in Fig. 9 and is always lower than 5%.

V. COMPARISON OF THE DESIGN STRATEGY

Unlike the design strategies in [24] and [25], in which the procedure guidelines derive from the start up behavior of the charge pump, the design approach proposed in this paper is based on power consumption evaluation which is a steady-state characteristic. Another design strategy based on a steady-state characteristic is the one presented in [27] where the number of stages which minimize the area (i.e., the charge-pump capacitance) for a defined load current is derived. Equivalently, it maximizes

Fig. 8. Errors on analytical and measured $I_{\text{power}}/I_L-(N+1)$ assuming $\alpha = 0.18$.Fig. 9. Errors on analytical and measured $I_{\text{power}}/I_L-(N+1)$ assuming $\alpha = 0.2$.

the load current for a defined charge-pump capacitance. The strategy was well known to charge-pump designers before it was presented in [27]. However, to the authors' knowledge, [27] is the first paper in which it was analytically derived. It says that to minimize the charge capacitance we have to choose a number of stages equal to

$$N' = 2(K-1) \quad (17)$$

again, (17) is independent of the load current which sets the capacitance of a stage (i.e., the total charge-pump capacitance).

In order to compare the area required in each design strategy, the total charge-pump capacitances must be evaluated in both cases. Since the total capacitance is equal to NC , substituting (17) in (5) we find that the total capacitance in the case we minimize the silicon area is

$$C'_T = 4(K-1) \frac{I_L}{V_{DD}f} \quad (18)$$

and substituting (9) in (5), the total capacitance in the case we minimize the power consumption is given by

$$C_{T \text{ op}} = \frac{(1+\gamma)^2}{\gamma} (K-1) \frac{I_L}{V_{DD}f}. \quad (19)$$

Hence, the area increase in the case of power-consumption optimization turns out to be

$$\frac{C_{T \text{ op}} - C'_T}{C'_T} = \frac{(1+\gamma)^2}{4\gamma} - 1 = \frac{\left(1 + \sqrt{\frac{\alpha}{1+\alpha}}\right)^2}{4\sqrt{\frac{\alpha}{1+\alpha}}} - 1. \quad (20)$$

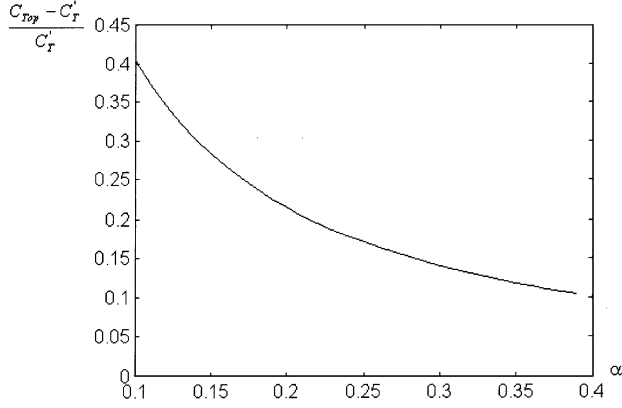


Fig. 10. Increment of capacitance (i.e., area) in the case of power-consumption optimization compared to the area minimization case.

Relationship (20) is plotted in Fig. 10. It is a decreasing function of α , and it is about equal to 0.4 and 0.2 (i.e., 40% and 20% more area) for α equal to 0.1, and 0.2, respectively. It is apparent that for very low values of α (much lower than 0.1) the minimum power consumption strategy can need an huge amount of silicon area with respect the minimum area strategy, but this results in a gain of the charge-pump efficiency.

It is worth noting that both (9) and (17) should be integer numbers. However, it can be demonstrated¹ that the difference in area considering discrete values of N' and N_{op} is lower than the value given by (20).

To compare the improved efficiency of the proposed strategy compared to the one proposed in [27], firstly compute the efficiency of the approach in [27] substituting (17) into (12)

$$\eta'_p = \frac{1}{1 + (1 + 4\alpha)(1 - \frac{1}{K})}. \quad (21)$$

Hence, the increment of efficiency of our approach is equal to

$$\frac{\eta_{p\max} - \eta'_p}{\eta'_p} = \frac{K + (1 + 4\alpha)(K - 1)}{1 + \frac{1+\gamma}{1-\gamma}(K - 1)} - 1. \quad (22)$$

By inspection of its plot in Fig. 11, we see that it is reduced after increasing the parameter α , and it is increased after increasing the multiplier factor, K . Thus, its maximum is represented by the curve

$$\lim_{K \rightarrow \infty} \frac{\eta_{p\max} - \eta'_p}{\eta'_p} = \left(\frac{1 - \gamma}{1 + \gamma} \right)^2. \quad (23)$$

VI. CONCLUSION

A new design strategy for charge pumps has been given. The procedure allows designers to choose the number of stages to minimize power consumption, which is becoming a mandatory target, since charge-pump circuits waste a lot of energy. The approach is based on an analytical model developed in the paper and validated through simulation and experimental measurements.

¹This demonstration can be achieved by considering N' or N_{op} higher (or lower) by one unit, which means considering the maximum difference between them due to approximation to the integer.

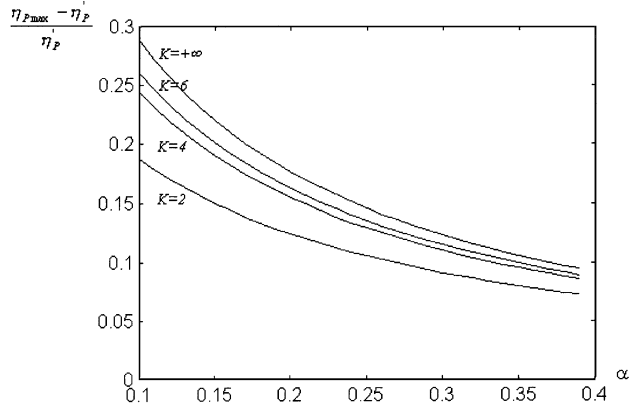


Fig. 11. Increment of efficiency in the case of power-consumption optimization compared to the area minimization case.

Although the relationships found depend on the technology, it has been demonstrated that dependence is low, and, hence, the technological parameters required, which give the degree of nonideality, do not need to be extracted with high accuracy.

In the paper, a comparison with the design strategy which minimizes silicon area was also carried out. The comparison shows, that for typical cases, a silicon area increase no greater than 20% is required for the design which optimizes power consumption.

APPENDIX I

Consider an N -stage charge pump having a generic-stage capacitance C_i . Under this general condition, (1) is

$$V_{out} = (N + 1)V_{DD} - \sum_{i=1}^N \frac{I_L}{fC_i}. \quad (A1.1)$$

Hence, inverting it we get

$$I_L = \frac{(N + 1)V_{DD} - V_{out}}{\frac{1}{f} \sum_{i=1}^N \frac{1}{C_i}}. \quad (A1.2)$$

To maximize the output current for a total charge-pump capacitance, $C_T = \sum_{i=1}^N 1/C_i$, we have to minimize the denominator of (A1.2), and following the traditional procedure

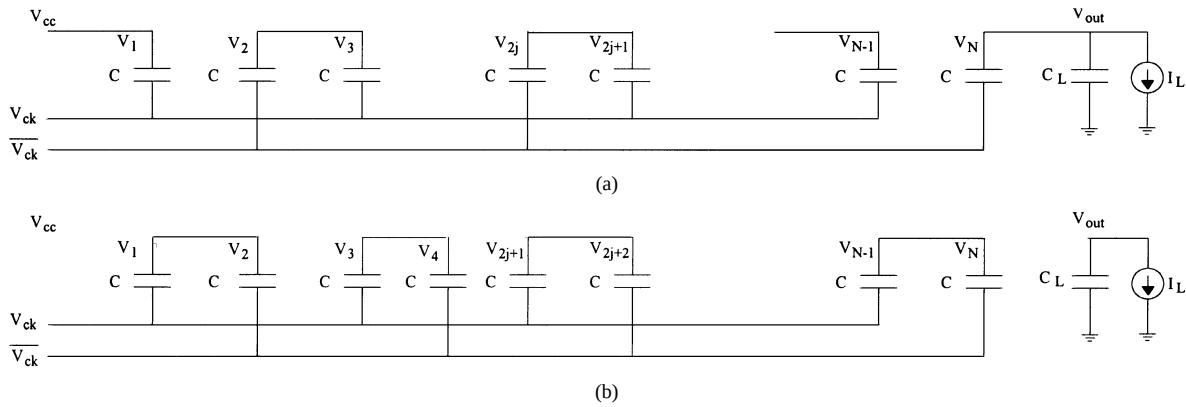
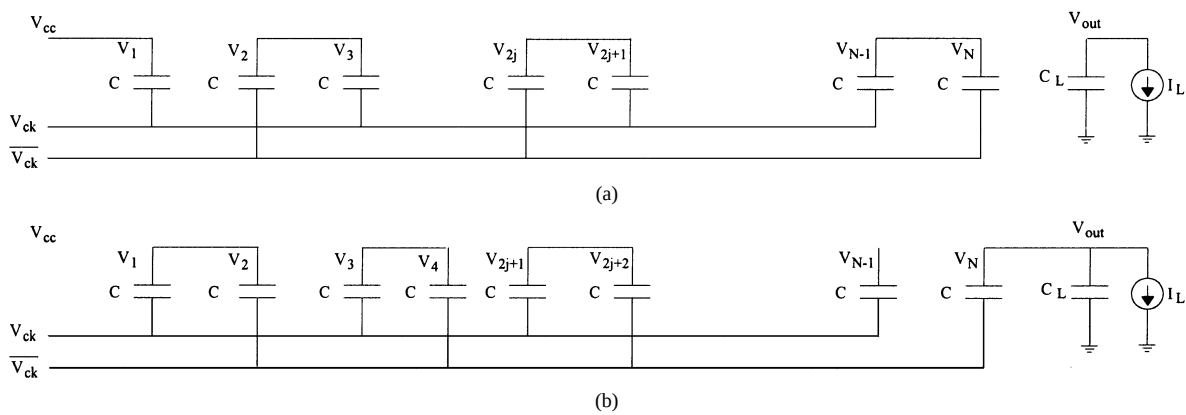
$$\begin{aligned} \nabla f(C_1, C_2, \dots, C_N) \\ = \nabla \left(\frac{1}{C_T - C_2 - \dots - C_N} + \frac{1}{C_2} + \dots + \frac{1}{C_N} \right) = 0 \end{aligned} \quad (A1.3)$$

which means $\forall i = 2, \dots, N$

$$\frac{\partial f(C_1, C_2, \dots, C_N)}{C_i} = \frac{1}{(C_T - C_2 - \dots - C_N)^2} - \frac{1}{C_i^2} = 0 \quad (A1.4)$$

from which we get $C_i = C_1 \forall i = 2, \dots, N$. Thus, in other words, to maximize the current for a prefixed charge-pump capacitance, we have to set all capacitance equal

$$C_i = \frac{C_T}{N}. \quad (A1.5)$$

Fig. 12. Ideal charge pump with an even number of stages. (a) V_{ck} low. (b) V_{ck} high.Fig. 13. Ideal charge pump with an odd number of stages. (a) V_{ck} low. (b) V_{ck} high.

APPENDIX II

A. An Even Number of Stages

Firstly consider an even number of stages. In the two time frames assuming ideal diodes (or switches), we have the two corresponding conditions in Fig. 12. By inspection of Fig. 12(a) in the steady-state condition, the first stage and the other interconnected stages excepting the last sink a charge ΔQ from the power supply equal to that lost in the previous time frame from the odd capacitances, so that the total amount of charge is $N\Delta Q/2$. During this time frame, the last stage sinks two charge contributions. The former is due to the current source, and is equal to $I_L T/2$. The latter is equal to that lost by the load capacitance in the previous time frame and it is again equal to $I_L T/2$. In conclusion, during this time period the charge provided by the power supply is

$$\Delta Q_{T1} = \frac{N}{2} \Delta Q + I_L T. \quad (\text{A2.1})$$

In the next time frame, we have the corresponding network in Fig. 12(b). Hence, all the interconnected stages sink from the power supply the charge lost by the even capacitor in the previous time frame for a total amount equal to $N\Delta Q/2$. It is apparent that in steady-state terms ΔQ is equal to the loss of charge in the last stage when it is connected with the load. Thus,

the total current consumption of an ideal charge pump with an even number of stages is given by

$$I_{\text{power}} = (N + 1)I_L. \quad (\text{A2.2})$$

B. An Odd Number of Stages

By inspection of Fig. 13(a) in a steady-state condition, the first stage and the other interconnected stages sink from the power supply a charge, ΔQ , equal to that lost in the previous time frame from the odd capacitances, so that the total amount of charge is now $(N + 1)\Delta Q/2$. Moreover the load capacitance is losing a charge equal to $I_L T/2$. By inspection of Fig. 13(b) which refers to the next time frame, all the interconnected stages excepting the last gain a charge, ΔQ , lost by the even capacitor. Hence, the power supply provides a charge equal to $(N - 1)\Delta Q/2$. In this time frame, the last stage sinks from the power supply the charge that feeds to the current source plus the charge previously lost by the load capacitance. The amount of charge sunk by the last stage is equal to $I_L T$. In a steady state it is also equal to those circulating in the interconnected stages, ΔQ .

In conclusion, in the two time frames we waste a charge $N\Delta Q + I_L T$, which, as expected, means a total current consumption of an ideal charge pump with an odd number of stages given by (A2.2).

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