

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

LONGITUDE LICENSING LTD.,
Patent Owner.

IPR2023-01230
U.S. Patent No. 9,207,701

**WESTERN DIGITAL AND SANDISK'S
NOTICE OF APPEAL TO THE
UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT**

via P-TACTS
Patent Trial and Appeal Board

via Email
Director of the United States Patent and Trademark Office
efileSO@uspto.gov

via CM/ECF
United States Court of Appeals for the Federal Circuit

Pursuant to 28 U.S.C. § 1295(a)(4)(A), 35 U.S.C. §§ 141(c), 142, and 319, and 37 C.F.R. §§ 90.2(a), 90.3, 5 U.S.C. §§ 701–706, and Federal Circuit Rule 15(a)(1), Petitioners Western Digital Technologies, Inc. (“Western Digital”) and SanDisk Technologies, Inc. (“SanDisk”)¹ (collectively, “Petitioners”) provide notice that they appeal to the United States Court of Appeals for the Federal Circuit from the Final Written Decision of the Patent Trial and Appeal Board (“Board”) entered January 21, 2025 (Paper 31) and from all underlying and related orders, decisions, rulings, and opinions regarding U.S. Patent No. 9,207,701 (“the ’701 patent”) in *Inter Partes* Review IPR2023-01230.

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), the expected issues on appeal include, but are not limited to: the Board’s error(s) in determining that Petitioners

¹ After the Final Written Decision issued, the Board granted permission to add SanDisk as a co-petitioner party in IPR2023-01230. *Western Digital Technologies, Inc. v. Longitude Licensing, Ltd.*, IPR2023-01230, Exhibit 3001 (Mar. 6, 2025). The Board also permitted Western Digital to update its Mandatory Notices to list SanDisk as a Real Party-in-Interest in this IPR proceeding. *Id.*; *see also* IPR2023-01230, Paper 32 (Mar. 11, 2025) (Petitioners’ Updated Mandatory Notices) and Paper 33 (Mar. 11, 2025) (SanDisk’s Power of Attorney).

have failed to demonstrate that challenged claims 1–18 of the '701 patent are unpatentable, and any finding or determination supporting or related to that determination, including the Board's errors regarding motivation to combine Zhang and Javanifard, motivation to combine the teachings of Javanifard, as well as all other issues decided adversely to Petitioners in any orders, decisions, rulings, or opinions in *Inter Partes* Review IPR2023-01230.

Pursuant to 35 U.S.C. § 142 and 37 C.F.R. § 90.2(a), this Notice is being filed with the Director of the United States Patent and Trademark Office and with the Patent Trial and Appeal Board. In addition, a copy of this Notice and the required docketing fees are being filed with the Clerk's Office for the United States Court of Appeals for the Federal Circuit via CM/ECF.

Respectfully submitted,

Dated: March 24, 2025

/David M. O'Dell/
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CERTIFICATE OF FILING

The undersigned hereby certifies that, in addition to being electronically filed through PTAB P-TACTS, a true and correct copy of the above-captioned PETITIONERS' NOTICE OF APPEAL TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT is being filed by email with the Director on March 24, 2025, at efileSO@uspto.gov.

The undersigned also hereby certifies that a true and correct copy of the above-captioned PETITIONERS' NOTICE OF APPEAL TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT and the filing fee is being filed via CM/ECF with the Clerk's Office of the United States Court of Appeals for the Federal Circuit on March 24, 2025.

Respectfully submitted,

Dated: March 24, 2025

/David M. O'Dell/
David M. O'Dell
Lead Counsel for Petitioners
Registration No. 42,044

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6, this is to certify that a true and correct copy of the foregoing "Petitioners' Notice of Appeal to the United States Court of Appeals for the Federal Circuit" was served on counsel for Patent Owner Longitude Licensing Ltd. as detailed below:

<i>Date of service</i>	March 24, 2025
<i>Manner of service</i>	Electronic Service by E-mail: – jmilkey@raklaw.com – ptong@raklaw.com – bledahl@raklaw.com – pkroeger@raklaw.com
<i>Documents served</i>	Petitioners' Notice of Appeal to the United States Court of Appeals for the Federal Circuit
<i>Persons served</i>	<i>Counsel for Longitude Licensing Ltd.</i> Jim Milkey (jmilkey@raklaw.com) Peter Tong (ptong@raklaw.com) Brian D. Ledahl (bledahl@raklaw.com) Paul A. Kroeger (pkroeger@raklaw.com) RUSS AUGUST & KABAT 12424 Wilshire Blvd., 12th Fl. Los Angeles, CA 90025

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

LONGITUDE LICENSING LTD.,
Patent Owner.

IPR2023-01230
Patent 9,207,701 B2

Before RICHARD M. LEBOVITZ, DAVID C. McKONE, and
KEVIN C. TROCK, *Administrative Patent Judges*.

LEBOVITZ, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Western Digital Technologies, Inc. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–18 of U.S. Patent No. 9,207,701 B2 (“the ’701 patent”) on July 20, 2023. Paper 2 (“Pet.”); Paper 3 (filing date accorded). Longitude Licensing LTD. (“Patent Owner”) filed a Preliminary Response to the Petition on October 25, 2023. Paper 6. In the Institution Decision, we instituted review of all challenged claims included in the Petition. Paper 7 (“Inst. Dec.”).

We have jurisdiction under 35 U.S.C. § 6. We issue this Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons explained below, Petitioner has not shown by a preponderance of the evidence that claims 1–18 are unpatentable. *See* 35 U.S.C. § 316(e) (2018).

II. BACKGROUND

A. *Procedural History*

After we instituted review, Patent Owner filed a Response to the Petition. Paper 18 (“PO Resp.”). Petitioner filed a Reply to Patent Owner’s Response. Paper 21 (“Pet. Reply”). Patent Owner filed a Sur-reply to Petitioner’s Reply. Paper 23 (“PO Sur-reply”).

On October 24, 2024, we held an oral hearing. The hearing transcript has been entered into the record. Paper 30 (“Tr.”).

B. *Real Parties in Interest*

Petitioner identifies the real party in interest as Western Digital Technologies, Inc. (“Petitioner”). Pet. 93.

Patent Owner identifies Longitude Licensing LTD., as the real party in interest. Paper 4 (Patent Owner Mandatory Notices), 2.

C. Related Matters

Patent Owner identifies the following civil actions that “may affect, or be affected by, a decision in this proceeding.” (Paper 13):

Longitude Licensing Limited v. ASUSTeK Computer Inc., Case 8-23-cv-00033 (C.D. Cal.); *Longitude Licensing Limited v. Lenovo Group Limited*, Case 8-23-cv-00035 (C.D. Cal.); *Longitude Licensing Limited v. Acer Inc.*, Case 8-23-cv-00036 (C.D. Cal.); *Longitude Licensing Limited v. HP Inc.*, Case 8-23-cv-00038 (C.D. Cal.); *Longitude Licensing Limited v. Amazon.com, Inc.*, Case 8-23-cv-00039 (C.D. Cal.); and *Longitude Licensing Limited v. Dell Technologies Inc.*, Case 8-22-cv-02312 (C.D. Cal.).

D. Testimonial Evidence

To support its challenge, Petitioner relies on the Declaration of Harvey J. Stiegler, Ph.D. (Ex. 1003, “Stiegler declaration”).

Patent Owner relies on the declaration of Bruce Jacob Ph.D. (Ex. 2003, “Jacob declaration”).

Additionally, Patent Owner submits Dr. Stiegler’s deposition testimony, and Petitioner submits Dr. Jacob’s deposition testimony. *See* Ex. 2004 (Apr. 1, 2024); Ex. 1029 (Jan. 10, 2024).

E. The ’701 Patent (Ex. 1001)

The ’701 patent is titled “Supply Voltage Generating Circuit.” Ex. 1001, code (54). The patent issued on December 8, 2015. *Id.* at code (45). The ’701 patent claims U.S. priority back, through a string of applications, to a U.S. application filed March 20, 2008, and foreign priority to a Japanese application filed March 27, 2007. *Id.* at codes (21), (22), (63), (30).

The '701 patent describes “a supply voltage generating circuit . . . for generating a boosted voltage within a semiconductor storage device.”

Ex. 1001, 1:16–19. The '701 patent further discloses that the “supply voltage generating circuit” comprises “a booster that outputs a boosted voltage upon generating the boosted voltage by charge pumping of a capacitor element.”

Id. at 2:29–31. The booster (also known as a “booster circuit” or “charge pump circuit”) provides internally-generated supply voltages that are higher than the input power supply voltages. Ex. 1003 ¶ 42.

Figure 1 of the '701 patent shows the circuitry for generating supply voltage VPP. Figure 1 is reproduced below:

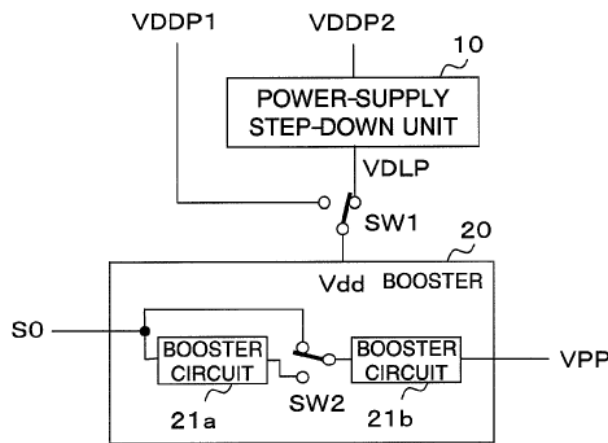


Figure 1 is a block diagram illustrating the configuration of an exemplary “supply voltage generating circuit” of the '701 patent. Ex. 1001, 3:63–65. The figure shows two voltage sources (VDDP1 and VDDP2), booster 20 for generating a boosted voltage by charge pumping (Ex. 1001, 2:28–31; 4:1–3), and driving signal S0. Switch element SW1 switches between VDDP1 and the step-down voltage VDL P (from VDDP2). Ex. 1001, 4:54–59. Switch element SW1 supplies voltage to booster 20. The booster 20 includes a pre-stage booster circuit 21a, a post-stage booster

circuit 21b, and a switch element SW2 for switching between the booster circuits 21a and 21b. *Id.* at 4:60–63.

The booster 20 generates a boosted voltage from VDDP1 or VDLP “by charge pumping of the capacitor elements using a driving signal S0,” which “supplies the boosted voltage to a load circuit, an example of which is a circuit for driving a word line, as power supply VPP.” *Id.* at 4:63–67.

The ’701 patent further discloses selecting first and second nodes associated with different power supplies (e.g., VDDP1, VDLP) of the supply voltage generating circuit:

The switch element SW2 is switched to the first boosted signal when the switch element SW1 has been switched to the external power supply VDDP1, and the switch element SW2 is switched to the second boosted signal when the switch element SW1 has been switched to the output (VDLP) of the power-supply step-down unit 10.

Ex. 1001, 5:14–19.

The ’701 patent discloses that “the booster 20 is so adapted that the number of booster stages (e.g., one stage or two stages) constituted by the multiple booster circuits 21a, 21b is changed over by a switch element SW2 in accordance with the power-supply voltage [VDDP1, VDLP] applied to the booster 20.” Ex. 1001, 4:24–28.

In accordance with this supply voltage generating circuit, the ’701 patent teaches that the number of booster stages (e.g., 21a, 21b) can be “changed over to the most efficient number depending upon the level of the external voltage.” Ex. 1001, 9:43–50. Depending on the specified VPP voltage (e.g., 2.5V) and the externally supplied voltage (e.g., 1.2V or 1.5V), a one- or two-booster stage circuit may be necessary. *Id.* at 9:51–60. The ’701 patent teaches that “[t]he smaller the number of stages, the better the

efficiency at which VPP is supplied with power.” *Id.* at 9:58–60. To sum up, the number of booster stages that may be used to provide the supply voltage VPP may be varied, making the circuit a variable booster circuit.

F. Challenged Claims

Petitioner challenges the patentability of claims 1–18 (“Challenged Claims”) of the ’701 patent, which are all the claims of the patent. Pet. 1. Claims 1 and 10, the challenged independent claims, are reproduced below as annotated by Petitioner with bracketed numbers:

[1.0] 1. A method for generating a supply voltage, comprising:

[1.1] selecting one of a first input node supplied with a first power supply voltage and a second input node supplied with a second power supply voltage that is higher than the first power supply voltage;

[1.2.1] coupling a selected one of the first and second input nodes to booster circuitry comprising a plurality of booster stages to provide an output voltage,

[1.2.2] wherein selection of the first input node corresponds to a first number of booster stages and

[1.2.3] selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number; and

[1.3] changing the booster circuitry from the first number of booster stages corresponding to selection of the first input node to the second number of booster stages when the second input node is selected.

[10.0] 10. A semiconductor device comprising:

[10.1] a first input node supplied with a first power supply voltage;

[10.2] a second input node supplied with a second power supply voltage higher than the first power supply voltage;

[10.3] booster circuitry comprising a plurality of booster stages to provide an output voltage; and

[10.4] a first switch configured to couple a selected one of the first input node and the second input node to the booster circuitry,

[10.5] wherein the booster circuitry configured to have a first number of booster stages when the first input node is selected and to be changed to a second number of booster stages when the second input node is selected, the second number being less than the first number.

G. Prior Art and Asserted Grounds

Petitioner raises the following grounds of unpatentability with respect to the Challenged Claims (Pet. 2):

Claims Challenged	35 U.S.C. §¹	Reference(s)
1–18	103(a)	Zhang, ² Javanifard ³
1–18	103(a)	Javanifard
9, 18	103(a)	Zhang, Javanifard, Kang ⁴
9, 18	103(a)	Javanifard, Kang

Petitioner asserts that Zhang is prior art under at least §§ 102(a), 102(b), and 102(e), and Javanifard under at least §§ 102(a) and 102(b). *Id.*

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. §§ 102 and 103. We apply the pre-AIA versions of 35 U.S.C. §§ 102 and 103 because it appears the claims at issue have an effective filing date prior to March 16, 2013, the effective date of the AIA. *See* Ex. 1001, codes (22), (60).

² Zhang et al., U.S. Pat. 7,427,888 B2, issued September 23, 2008, was filed July 8, 2004, and claims foreign priority to July 10, 2003. Ex. 1005, codes (45), (22), (30).

³ Javanifard et al., U.S. Pat. 5,767,735, issued June 16, 1998, and claims priority back to September 29, 1995. Ex. 1006, codes (45), (22), (62).

⁴ Kang et al., *Charge Pump Circuits with Low Area and High Power Efficiency for Memory Applications*, 6(4) J. SEMICONDUCTOR TECH. SCI. 257–63 (2006).

Petitioner asserts that Kang was published, indexed, and publicly accessible as of at least December 31, 2006, and is prior art under at least §102(a). *Id.* (citing Ex. 1024 ¶ 46; Ex. 1003 ¶¶ 83–85).

Patent Owner does not dispute that each reference qualifies as prior art. *See* PO Resp. 2, 5, 38–39 (providing no arguments that the challenges are deficient because the cited publications are not prior art to the Challenged Claims).

III. BURDEN

In an *inter partes* review, a petitioner bears the burden of persuasion to prove “unpatentability by a preponderance of the evidence.” *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (quoting 35 U.S.C. § 316(e)); *see* 37 C.F.R. § 42.1(d) (2024). This burden never shifts to Patent Owner. *Dynamic Drinkware*, 800 F.3d at 1378 (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–1327 (Fed. Cir. 2008) (discussing the burden of proof in *inter partes* review). Petitioner must explain with particularity how the prior art would have rendered the Challenged Claims unpatentable. 35 U.S.C. § 312(a)(3); 37 C.F.R. § 42.104(b)(4) (“The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon.”).

IV. PATENTABILITY ANALYSIS

A. Legal Standards

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The obviousness inquiry requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)). Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements,” but “must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art at the time of the alleged invention “would have a bachelor’s or the equivalent degree in electrical or computer engineering or a related field, and 2–3 years of professional experience relating to circuit design.” Pet. 4 (citing Ex. 1003 ¶ 58). Petitioner further states “a person with less formal education but more experience, or more formal education but less experience, could have also met the relevant standard for [a person of ordinary skill in the art (POSITA)].” *Id.* Petitioner states that “a person having an extraordinary level of skill should” not be regarded as POSITA. *Id.*

Patent Owner, for purposes of its Response, does not dispute Petitioner’s definition a person of ordinary skill in the art. PO Resp. 4.

Based on the record before us, we adopt Petitioner’s definition of the level of skill of a person of ordinary skill in the art at the time of the invention.

C. Claim Construction

Petitioner states that “for the purposes of this proceeding and the analysis presented herein, no claim term requires express construction.” Pet. 4 (citing *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“only those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy”)). Petitioner states that, in the Petition, it “analyzes the claims consistent with ordinary and customary meaning as would be understood by [a] POSITA in light of the specification.” *Phillips*, 415 F.3d at 1314–17. *Id.* (citing Ex. 1003 ¶¶ 60–61). *See also* Pet. Reply 2 (“Claim Construction”).

Patent Owner “agrees that no express construction of any term is necessary.” PO Resp. 4.

We concur that claim construction is unnecessary and move directly to the obviousness analysis.

D. Obviousness challenge based on Zhang and Javanifard

Petitioner argues that claims 1–18 are unpatentable under 35 U.S.C. § 103 over the combination of Zhang and Javanifard. Pet. 19–61. We first provide an overview of the two cited prior art references and then address the obviousness challenge to claim 1 based on these references.

1. Overview of Zhang (Exhibit 1005)

Zhang describes its invention as relating “to charge pump circuits operating responsive to a mode that enables selection of a power voltage or an external high voltage.” Ex. 1005, 1:11–14.

Zhang discloses a prior art charge pump circuit that comprises a charge supply part 11 and a plurality of charge pump parts 12–15. Ex. 1005,

1:33–34 (referencing a block diagram of a conventional charge pump circuit shown in Figure 1 (not reproduced)). Zhang teaches that charge supply part 11 “receives an external voltage VCC and provides supply charges to a first charge pump part PS1,” which is connected serially to additional charge pump parts 11 to 15. *Id.* at 1:34–37 (shown in Figure 1 as PS1 (part 12), PS2 (part 13), PS3 (part 14), and PSn (part 15)). “The charge pump parts 12–15 generate an output voltage Vout by pumping charges supplied from the charge supply part 11.” *Id.* at 1:38–39.

Zhang discloses that a “conventional charge pump circuit pre-charges the output voltage Vout corresponding to the external voltage VCC at each node of the charge supply part 11 and the charge pump parts 12–15.” Ex. 1005, 1:63–66. With this circuit, Zhang teaches that “the time to precharge increases in the output voltage Vout.” *Id.* at 1:66–67. Zhang teaches that the “additional time” to precharge is “undesired particularly where testing integrated chips that require high voltages quickly. A need remains for an improved charge pump circuit.” *Id.* at 1:67–2:3.

Figure 4 of Zhang, reproduced below, shows a charge pump circuit that is asserted by Zhang to address the disadvantages of the conventional charge pump circuit.

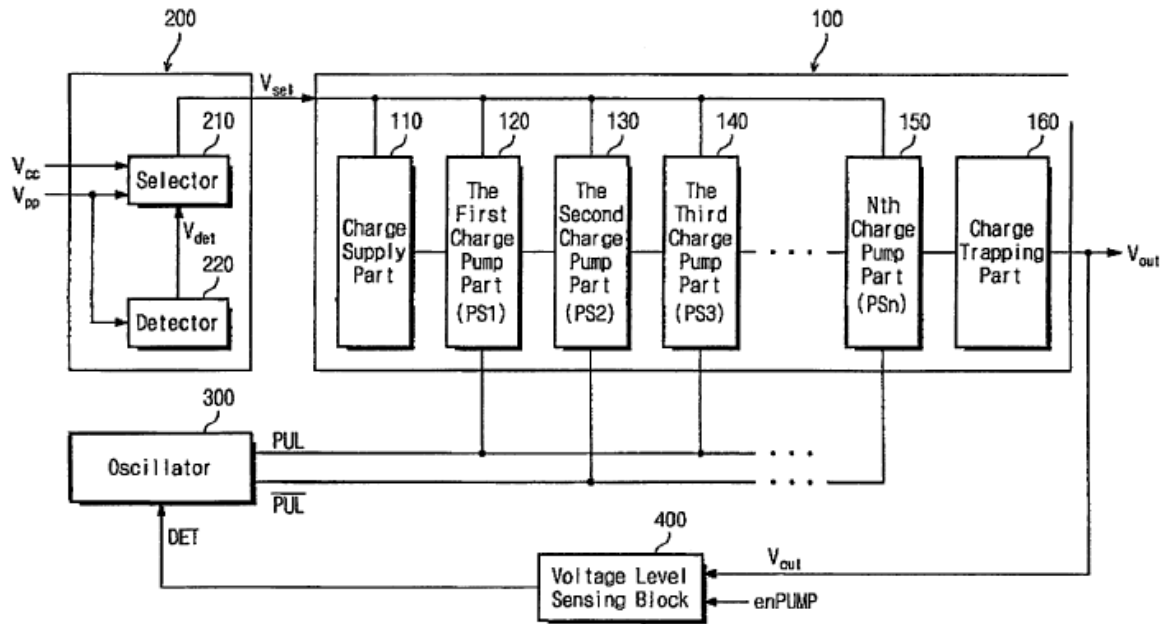


Figure 4 of Zhang shows a block diagram of a charge pump circuit 100. Ex. 1005, 2:54–55. The charge pump circuit comprises a charge pump block 100, a selecting circuit block 200, an oscillator 300, and a voltage level sensing block 400. *Id.* at 2:55–58. “The pump block 100 comprises a charge supply part 110, a plurality of charge pump parts 120, 130, 140, and 150 and a charge trapping part 160, all serially connected.” *Id.* at 2:59–61. The circuit has two power supplies, V_{CC} and V_{PP} .

The figure shows charge pump parts 110, 120, 130, 140, and 150. Part 150 is indicated as the *n*th charge pump part. The charge pump block 100 is therefore not restricted to five charge pump parts, but can have *n* number of parts. Circuit block 200 of Figure 4 provides voltage V_{sel} (from the power supplies V_{CC} or V_{PP}) to charge supply part 110, which then provides the voltage to the first charge part 120. Ex. 1005, 2: 62–64. First charge pump part 120 provides charge to the next charge pump part 130 and so on. *Id.* at 2:62–64. Each charge pump part “pumps a charge to a next serially connected charge supply part.” *Id.* at 2:66–67. “The charge pump parts 120,

130, 140 and 150 pre-charge a charge corresponding to the selected voltage V_{sel} .” *Id.* at 2:64–66. Charge trapping part 160 “traps the pumped charge through each charge pump part 120, 130, 140 and 150 to generate an output voltage V_{out} .” *Id.* at 3:1–2.

As shown in Figure 4, the charge pump circuit comprises selecting circuit block 200 which includes selector 210 and detector 220. Ex. 1005, 3:19–22. Selector 210 is shown as receiving power voltage V_{CC} or external high voltage V_{PP} . Power supply voltage V_{CC} refers to the power voltage operating in general operation. *Id.* at 3:22–24. “The voltage V_{PP} refers to a high voltage provided externally during a test operation mode.” *Id.* at 3:24–25.

Figure 8 of Zhang, reproduced below, “is a graph of the output voltage V_{out} depending on whether the charge pump circuit uses the power voltage V_{CC} or external high voltage V_{PP} .” Ex.1005, 5:1–3 (Fig. 8).

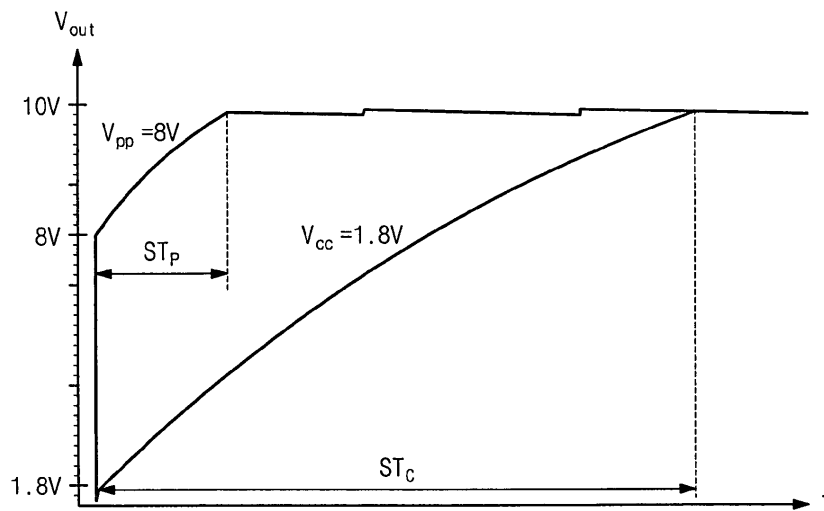


Figure 8 is a graph showing the time (on the X-axis) to obtain a “wanted voltage V_{out} ” (on the Y-axis), which in the figure is 10V. *Id.* at 5:3–9. “[W]hen external high voltage V_{PP} is supplied with the power voltage V_{CC} , a wanted output voltage V_{out} can be obtained within a shorter

time.” *Id.* at 5:9–11. Thus, Zhang describes how to achieve the *same* voltage output using two different voltage power supplies.

2. Overview of Javanifard (*Exhibit 1006*)

Javanifard describes its invention as “a charge pump having a variable number as opposed to a fixed number of stages according to charge pump power supply input levels and desired charge pump output levels.” Ex. 1006, 1:8–11. Javanifard describes disadvantages of charge pumps having a fixed number of stages. *Id.* at 1:48–63.

Javanifard explains that a “trend in the electronics industry is to reduce the power requirements of integrated circuitry.” *Id.* at 1:15–16. Javanifard teaches that “to reduce power consumption, integrated circuits are being designed to use lower voltage supply levels such as 3.3 volts instead of 5 volts.” *Id.* at 1:16–19. However, Javanifard teaches that certain operations “require voltages greater than that provided by the lower voltage power supplies.” *Id.* at 1:20–21. “For example, flash electrically-erasable programmable read only memory (flash EEPROM) requires approximately 12 volts for erase and programming operations.” *Id.* at 1:21–24. Javanifard teaches that “[c]harge pump technology permits the generation of voltages having a magnitude greater than that of the power supply. Through the use of charge pump circuitry 12 volts can be generated from 3.3 volts by using one or more charge pump stages.” *Id.* at 1:25–29.

Javanifard discloses at least two objects of its invention: (1) “to provide a charge pump that can accommodate different output levels for a given charge pump power supply input level,” and (2) “to provide a charge pump that can accommodate a given output level for different charge pump power supply input levels.” Ex. 1006, 2:19–24.

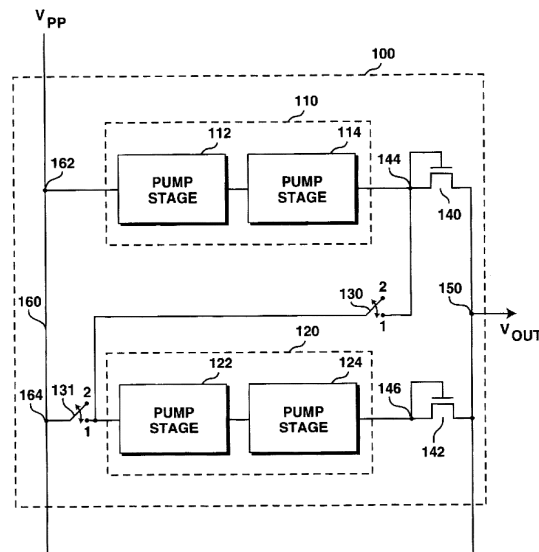
Figures 1, 2, and 3 illustrate three different representations of Javanifard's variable charge pump.

Each of Figures 1 and 3 show a variable stage charge pump circuit with one voltage power source and multiple "rungs" of charge pump stages, where each rung has two charge pump stages. Ex. 1006, 2:42–52. The circuit can be utilized to vary the number of pump stages employed to produce the output supply voltage. *Id.* at 2:54–3:5.

The variable stage pump circuit illustrated in Figure 3 differs from Figure 1 in having more charge pump rungs and as being coupled to flash memory. Otherwise, the charge pump of Figure 3 operates in the same way as the charge pump of Figure 1.

Javanifard's Figure 2 shows a variable stage charge pump with two voltage power sources, and three supply voltages, 5 volt, 9 volt, and 12 volt, for a flash memory.

Figure 1 of Javanifard is reproduced below:



Javanifard's Figure 1 is a block diagram of a variable stage charge pump 100 which includes two charge pump "rungs," labelled 162 and 164. Ex. 1006, 2:42–44. The rungs are coupled by bus 160 and have common

output V_{out} 150. One power supply is shown in Figure 1, labeled “ V_{PP} ,” which supplies the supply voltage to the bus 160. Each rung 162, 164 includes a charge pump. Rung 162 includes charge pump 110 with pump stages 112 and 114. Rung 164 includes charge pump 120 with pump stages 122 and 124. Each rung is capable of boosting the voltage of V_{PP} . The pump stages in each rung are series-coupled. Javanifard teaches that “[t]he variable stage charge pump 100 may also be identified by the expression ‘X/Y stage pump,’” where the “X” refers to the number of rungs and “Y” to the number of pump stages. *Id.* at 2:59–67. The variable stage charge pump 100 has switches 130 and 131. First switch 130 “controls whether the output of the first charge pump is provided as an input to the second charge pump.” *Id.* at 2:54–56. Second switch 131 “is used to couple the input of the second charge pump to V_{pp} .” *Id.* at 2:56–57.

The various switch configurations are shown in Table 1:

TABLE 1			
Switch 130	Switch 131	Charge Pump 110	Charge Pump 120
OFF	OFF	ON	OFF
OFF	ON	ON	parallel-coupled to charge pump 110
ON	OFF	ON	series-coupled to charge pump 110
ON	ON	N/A	N/A

Ex. 1006, 3:23–34.

Table 1 shows the four different position combinations of switches 130 and 131 and how the different positions (on or off) effect the coupling between the charge pumps. Ex. 1006, 3:19–22.

When switch 130 is on and switch 131 is off, the charge pumps 110 and 120 are series-coupled. Ex. 1006, 3:54–56. “When 110 and 120 are series-coupled, charge pump 100 might only be able to provide

approximately $\frac{1}{2}$ the current as was the case when charge pumps 110 and 120 were parallel-coupled.” *Id.* at 3:63–65. When switch 130 is off and switch 131 is on, the charge pumps 110 and 120 are parallel-coupled. *Id.* at 3:43–44. “Because 110 and 120 are parallel-coupled, charge pump 100 will be able to provide approximately twice the amount of current as was the case when only charge pump 110 was operating.” *Id.* at 3:50–53.⁵ In other words, using the same power supply, row 3 produces twice the voltage output as rows 1 and 2, thus achieving the first objective of Javanifard “to provide a charge pump that can accommodate different output levels for a given charge pump power supply input level.” *Id.* at 2:19–21.

In sum, by setting the switches appropriately, the charge pumps 110 and 120 can be configured to produce different numbers of charge-pump stages in series and in parallel. Ex. 106, 3:25–65.

Figure 3 of Javanifard (not reproduced) “illustrates a variable stage charge pump coupled to a flash memory array.” Ex. 1006, 2:38–39. The illustrated embodiment has 12 rungs, each with a charge pump, and each charge pump having 2 pump stages. *Id.* at 5:3–6. “The output of each of the *n* charge pumps is coupled to a same output node 350,” which provides power to the flash memory. *Id.* at 5:15–16. Similar to Figure 1, different current and voltages can be provided by the circuitry shown in Figure 3.

We focus the obviousness discussion below on the embodiment shown in Figure 1 because Figure 3 has a similar circuitry and operates in the same manner, but using a larger number of rungs and pump stages.

⁵ Petitioner states that a POSITA would have understood these statements to indicate “a design to accommodate ‘a **given output level for different** charge pump power supply input levels.’” Pet. 35.

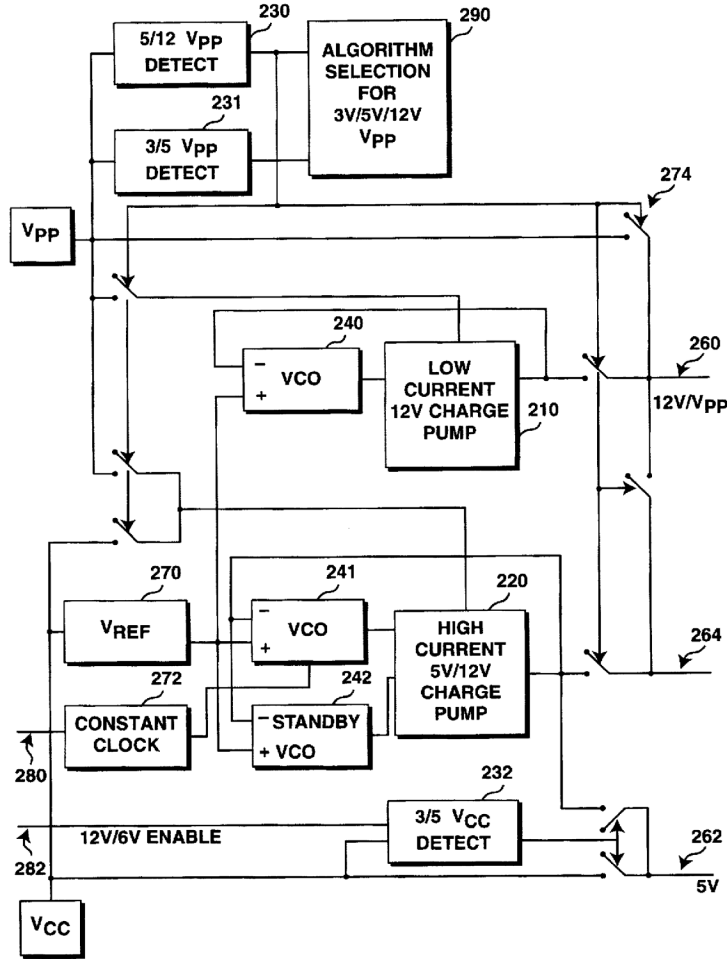
Javanifard teaches the advantages of varying the number of booster stages to achieve a desired supply voltage:

Designing the variable stage charge pump with an appropriate number of stages permits a charge pump circuit that can provide the proper voltages for the memory circuitry irrespective of the available power supply voltage. For example, if 6 and 12 volt supplies are required from the variable stage charge pump, the designer can provide a control to the switches that will switch stages in and out, or change the coupling of the stages to ensure the appropriate output voltage from the variable stage charge pump regardless of the input voltage. The control for the switches would be a function of the available power supply voltage, V_{pp} , and the desired variable stage charge pump output voltage.

Ex. 1006, 5:56–66.

We next turn to Figure 2 of Javanifard. Figure 2 illustrates a circuit with two power supplies and three supply output voltage lines. Figure 2 also shows “circuitry including variable stage charge pumps for supplying power to a flash memory array.” Ex. 1006, 2:36–37.

Figure 2 is reproduced below:



Javanifard’s Figure 2 is a block diagram showing “the power supply circuitry for a flash memory including variable stage charge pumps for accommodating a 5 volt, 9 volt, and 12 volt voltage level from either a 3.3 volt or 5 volt power supply.” Ex. 1006, 6:61–64. The figure shows two power supplies, V_{PP} and V_{CC} . Javanifard discloses that “two charge pumps (210, 220) are used to increase the internal node’s voltages to different voltages during the read mode (5 volt charge pumps), the programming mode (12 volt and 9 volt charge pumps), and the erase mode (12 volt and 9 volt charge pumps).” *Id.* at 7:10–19. “Variable stage charge pump 220 is a high current variable stage charge pump used during the read, program, and erase operations.” *Id.* at 7:27–29. “Variable stage charge pump 210 is a low

current variable stage charge pump used in addition to charge pump 220 only during program and erase operations.” *Id.* at 7:29–31.

Javanifard discloses the uses of different power supplies and different numbers of charge pump stages to achieve different supply voltages. Specifically, Javanifard discloses that the “high current and the low current variable stage charge pumps are reconfigured depending upon the operational mode and the nominally detected values of V_{pp} (i.e., 3.3 or 5 volts).” Ex. 1006, 7:62–65.

Javanifard provides Table 2 to illustrate configurations for charge pump 220 having 18 parallel-coupled sets of stages, each set including 3 serially coupled stages (“18/3”). Ex. 1006, 7:65–8:12; 8:24–30.

Javanifard provides Table 3 to illustrate configurations for charge pump 210 having 4 parallel-coupled set of stages, each set including 3 serial couple stages (“4/3”) and 2 parallel-coupled set of stages, each set including 2 serial couple stages (“2/6”). Ex. 1006, 8:15–23.

With respect to the objective “to provide a charge pump that can accommodate a given output level for different charge pump power supply input levels,” Tables 2 and 3 indicate that the charge pump stages can be reconfigured to achieve the same output voltages for the different V_{pp} voltages (i.e., 5 and 3.3 volts). *See* Ex. 2003 ¶¶ 122–125.

3. *Independent claim 1*

Petitioner challenges the patentability of claims 1–18 under 35 U.S.C. § 103(a) as obvious in view of Zhang and Javanifard. Pet. 5. The patentability challenge is based on the obviousness of combining Zhang’s circuit having first and second power supply voltages as shown in Figure 4, with Javanifard’s circuit which is capable of selecting a variable number of

booster stages, as shown in Figures 1 and 3, to generate the desired “supply voltage” of claim 1. Pet. 30–31.

Patent Owner’s principal contention is that the Petition is deficient in the reasons to combine Zhang and Javanifard to reach the limitations of claim 1 of the ’701 patent. PO Resp. 6, 11–27, 31–38. Patent Owner also asserts that the Petition fails to explain how the combination of the two references would provide different output voltages. *Id.* at 9, 28–30.

Patent Owner does not challenge on the record before us that the individual elements of the claim are disclosed or suggested by the combination of Zhang and Javanifard, but instead disputes Petitioner’s asserted motivation to combine the elements. PO Resp. 5, 11. In *KSR*, 550 U.S. at 398, although the Supreme Court emphasized “an expansive and flexible approach” to the obviousness question, *id.* at 415, it also reaffirmed the importance of determining “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *Id.* at 418.

We summarize Petitioner’s contentions below on how the limitations in the claim are met by the combination of Zhang and Javanifard. We also address Patent Owner’s arguments regarding Petitioner’s reasoning to combine these prior art patents.

As discussed in detail below, based on the totality of the evidence before us, we conclude that Petitioner has not met the burden of demonstrating by a preponderance of the evidence that independent claim 1 would have been obvious based on the combination of Zhang and Javanifard.

[1.0] 1. *A method for generating a supply voltage, comprising:*

The Petition provides evidence that each of Zhang and Javanifard describes the preamble of independent claim 1.

Specifically, Zhang describes generating a supply voltage (“ V_{out} ” or “ V_{out} ”) using a charge pump circuit. Pet. 23 (citing Ex. 1005, 2:55–3:2; Fig. 8; Ex. 1003 ¶ 98). Figure 4 of Zhang, reproduced above, illustrates this configuration.

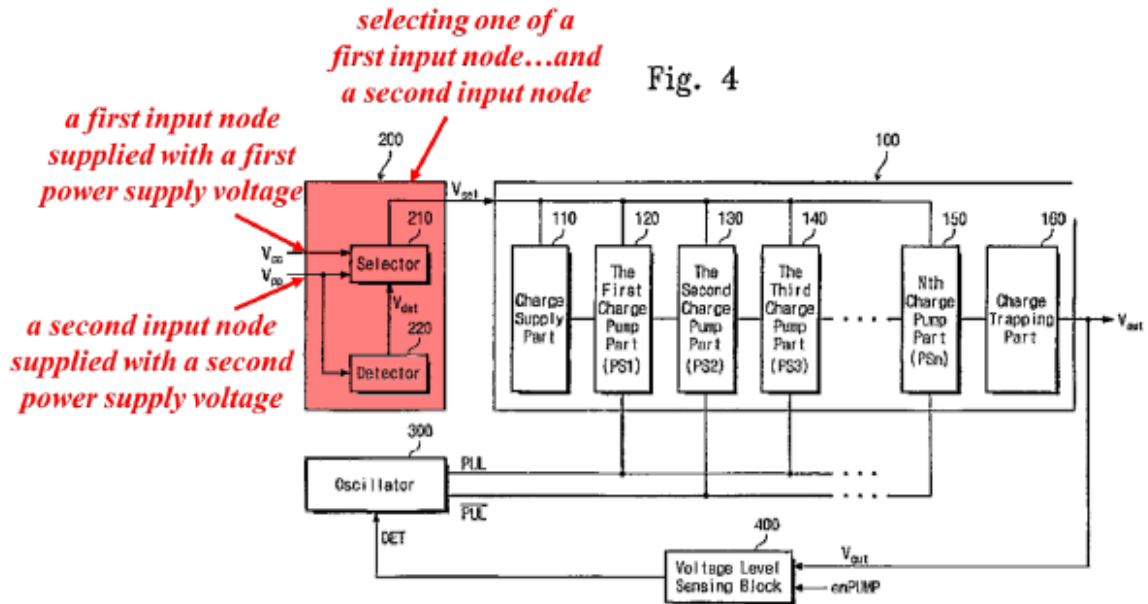
Javanifard, as explained above, also describes generating a supply voltage. Javanifard describes a variable stage charge pump providing a supply voltage in integrated circuits, which in one embodiment is to “provide the proper voltages for the memory circuitry.” Pet. 24 (citing Ex. 1006, Figs. 1–3; 2:18–24; 6:56–59). In Figure 1 of Javanifard, the supply voltage is labeled “ V_{out} .”

Patent Owner does not dispute the Petition’s contentions that limitation [1.0] is described or suggested by the combination of Zhang and Javanifard, which we find to be supported by a preponderance of the evidence.

[1.1] *selecting one of a first input node supplied with a first power supply voltage and a second input node supplied with a second power supply voltage that is higher than the first power supply voltage;*

The Petition provides evidence that limitation [1.1] is described by Zhang. Pet. 24–25 (citing Ex. 1003 ¶¶ 102–106). With specific reference to Figure 4 of Zhang, Petitioner identifies “selecting circuit block 200 that selects one of a first node supplied with VCC (a first power supply voltage) and a second node supplied with VPP (a second power supply voltage)” as corresponding to the selection of first and second nodes supplied with first

and second power supply voltages, respectively, as evidence of the recited limitation. Pet. 24. The Petition provides annotated Figure 4 of Zhang to show these elements. Pet. 25. Figure 4, as annotated by Petitioner, is copied below:



Annotated Figure 4 of Zhang shows selector 210, which selects VCC (or V_{CC}) (the claimed “first input node supplied with a first power supply voltage”) and VPP (or V_{PP}) (the claimed “second input node supplied with a second power supply voltage that is higher than the first power supply voltage”). VCC refers to the power voltage supply operating in general operation mode; VPP refers to the high voltage power supply provided externally during a test operation mode. Ex. 1005, 3:21–27. The figure shows pump block 100 comprising “a plurality of charge pump parts 120, 130, 140, and 150 and a charge trapping part 160, all serially connected.” *Id.* at 2:59–61. The “charge pump parts” correspond to the claimed “booster stages.” The circuit has a fixed number of n stages.

Zhang further describes circuit block 200, which supplies voltage to charge pump block 100 (as illustrated in Figure 4):

The selector 210 selects between the power voltage VCC and the high voltage VPP. The detector 220 detects the level of the high voltage VPP to generate detection signal VDET. The detector 220 enables the detection signal VDET when the high voltage VPP is higher than the power voltage VCC. The selector 210 switches between the power voltage VCC to the high voltage VPP responsive to the detection signal VDET. Put differently, the signal VSEL is VCC in the general operation mode and VPP in the test operation mode allowing for a high voltage within a short time.

Ex. 1005, 3:29–38.

For the requirement of the claim that the second power supply voltage is higher than the first, Petitioner identifies the disclosure in Figure 8 of Zhang which shows that VPP (8V) is higher than VCC (1.8V). Pet. 24 (citing Ex. 1005, 5:5–9; *id.* at 3:32–36 (“The selector 210 switches between the power voltage VCC [and] the high voltage VPP”). Petitioner points out that the ’701 patent has external and internal power supplies as does Zhang. *Id.*

Patent Owner does not dispute the Petition’s contentions that limitation [1.1] of independent claim 1 is described by Zhang, which we find to be supported by a preponderance of the evidence.

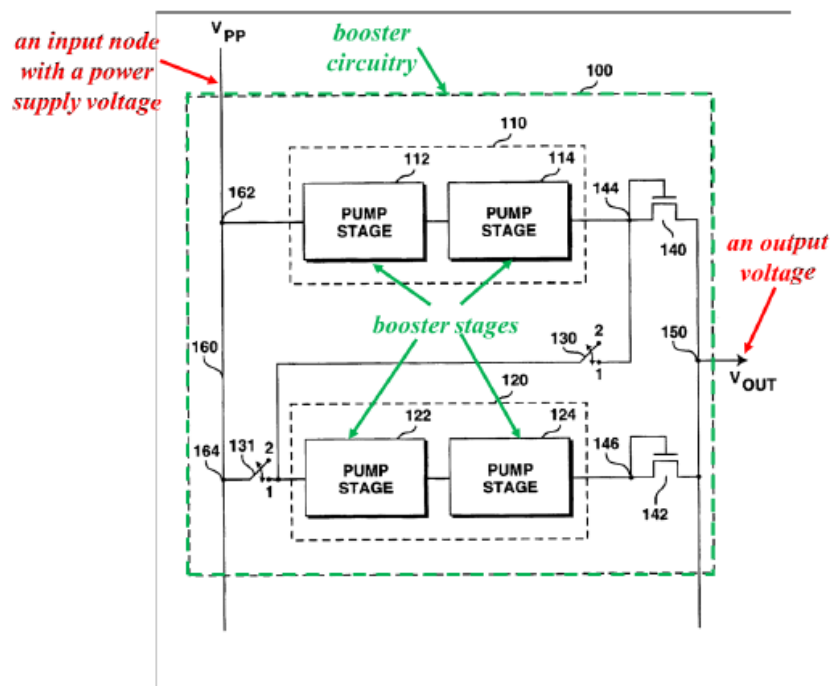
[1.2.1] *coupling a selected one of the first and second input nodes to booster circuitry comprising a plurality of booster stages to provide an output voltage,*

The Petition provides evidence that Zhang in view of Javanifard describes limitation [1.2.1] of claim 1. Pet. 26–31 (citing Ex. 1003 ¶¶ 107–116).

As explained above, Figure 4 of Zhang shows charge pump circuit 100 coupled to circuit block 200. Circuit block 200 comprises power voltage

VCC and high voltage VPP. Circuit block 200 comprises first and second input nodes, as claimed, supplied with voltage from VCC and VPP, respectively. The charge pump block 100 comprises charge pump parts 110 to 150, which correspond to the claimed “plurality of booster stages.” Pet. 26. Only one charge pump 100 is shown in Zhang; the circuit has a fixed number of stages which cannot be varied, i.e., all the stages are utilized when the circuit is open.

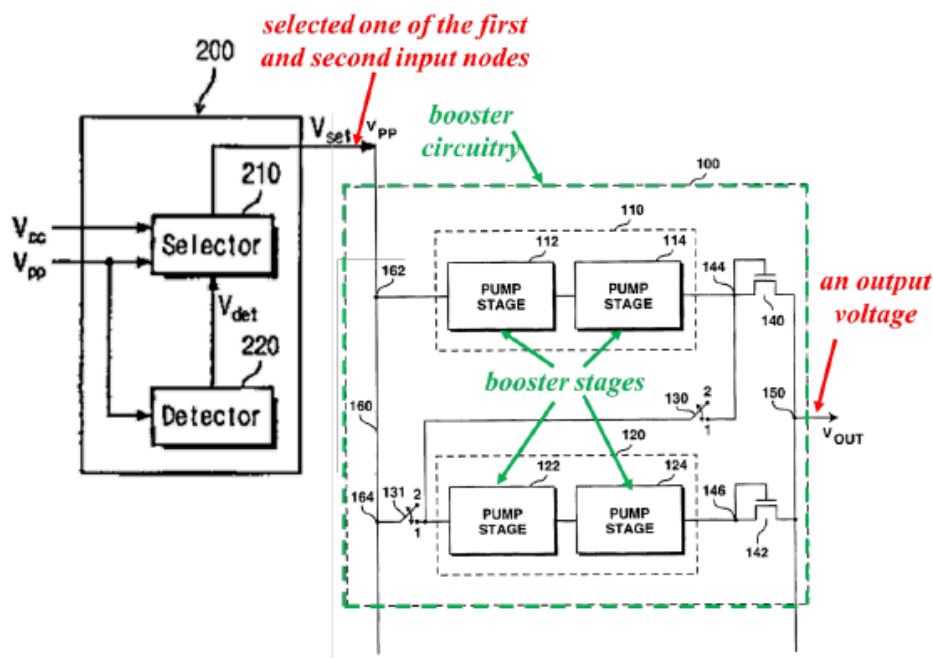
Returning to Javanifard, the Petition provides evidence that Javanifard “describes coupling an input node with a power supply voltage to a booster circuitry comprising a plurality of booster stages to provide an output voltage.” Pet. 27. Javanifard has been discussed above. Figure 1 of Javanifard, as annotated by Petitioner, shows the elements asserted to correspond to the limitations in the claim. *Id.* at 28. Figure 1 of Javanifard annotated by Petitioner is reproduced below:



Annotated Figure 1, reproduced above, shows an input node with power supply V_{PP} coupled to charge pump 100. Annotated Figure 1 shows two rungs, 162 and 164, each with two serially-coupled pump stages: 110 comprises 112 and 114; 120 comprises 122 and 124. Pump stages 112, 114, 122, and 124 correspond to the claimed booster stages. Pet. 28. The “output voltage” of Javanifard’s Figure 1 corresponds to the “supply voltage” of claim 1.

The Petition annotates Javanifard’s Figure 3, similarly to Figure 1, to show the elements which it contends correspond to the claimed input node and booster circuitry. Pet. 29. The main asserted differences between Figures 1 and 3 of Javanifard is that the latter figure shows more booster rungs and pump stages, and the supply output voltage is coupled to a flash memory.

Petitioner creates “Example A,” which is a combination of Zhang’s Figure 4 and Javanifard’s Figure 1. Pet. 30. Example A, as constructed by Petitioner, is reproduced below:



Example A, copied above, shows circuit block 200 of Zhang coupled to variable charge pump 100 of Javanifard. Circuit block 200 replaces Vpp of Javanifard. According to Petitioner, this composite provides Javanifard's charge pump 100 with the ability to receive voltage from VCC or VPP using Zhang's circuit block 200. Pet. 31. Petitioner makes the same composite of Zhang's Figure 4 and Javanifard's Figure 3 (Example B), having the same functionality as Example A. *Id.* Because of the redundancy between Figure 1 and Figure 3 of Javanifard, we focus on Example A incorporating the circuit of Figure 1. The same facts and reasoning would apply to Example B.

Patent Owner does not challenge the Petition's contentions that the combination of Zhang and Javanifard meets limitation [1.2.1] of claim 1. Instead, Patent Owner's principal argument is a lack of reason to combine the two references. In this regard, the Petition asserts that one of ordinary skill in the art would have been motivated to apply Javanifard's teaching of a variable stage charge pump to Zhang's multi-power-source charge pump system (which has a fixed charge pump)

to produce the obvious, beneficial, and predictable results of a variable stage charge pump system, which can both "accommodate different output levels for a given charge pump power supply input level," "accommodate a given output level for different charge pump power supply input levels," and provide flexibility for design needs (e.g., power saving mode, and current requirements), area reduction, and performance improvement, as taught by Javanifard. EX1003, ¶¶ 90–96.

Pet. 19–20; *see also id.* at 31.

The Petition asserts that a POSITA would have had reason to replace Zhang's fixed stage pump with Javanifard's variable stage charge pump because of the disadvantages of fixed stage pumps disclosed by Javanifard. Pet. 20 (citing Ex. 1006, 1:48–53 ("dedicated space in integrated circuit"));

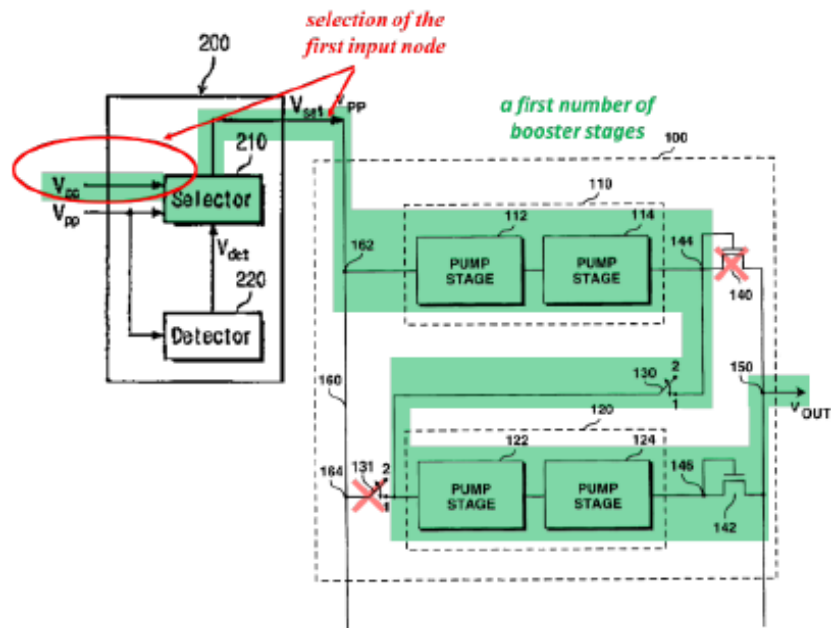
id. at 1:66–2:2 (“sacrifices performance” at one power supply to accommodate a second power supply); “lack of flexibility”). Thus, for the reasons stated above, Petitioner contends that “[a] POSITA facing the need to improve [Zhang’s] charge pump system would have looked to Javanifard and been motivated to apply Javanifard’s teachings of the variable stage charge pump in the multi-power-source charge pump system of Zhang using [a] fixed stage charge pump.” Pet. 21.

We address these reasons in Section IV.D.4 below.

[1.2.2] *wherein selection of the first input node corresponds to a first number of booster stages and*

The Petition contends that the combination of Zhang and Javanifard teaches or suggests claim limitation [1.2.2]. Pet. 32 (citing Ex. 1003 ¶¶ 117–124). Zhang provides a circuit with the capability to choose from two power sources (first and second input nodes). Ex. 1005, Fig. 4. The Petition contends that Javanifard’s charge pump provides the capability to choose from different combinations of charge pumps and pump stages. Ex. 1006, Fig. 1; Ex. 1003 ¶¶ 120–122.

The Petition asserts that the combination of Zhang and Javanifard would result in a circuit in which “selection of the first input node (with a lower input power supply voltage level) corresponds to a first number (a higher number e.g., 4) of booster stages, e.g., for generating the same output voltage as the selection of the second input node with a higher input power voltage level.” Pet. 32 (citing annotated Example A). Petitioner shows this circuitry, reproduced below as Example A, which is a composite of Zhang’s Figure 4 and Javanifard’s Figure 1 created by Petitioner (Pet. 33):



Petitioner-annotated Example A (combining Zhang Figure 4 on left with Javanifard Figure 1 on right) shows the selection of the first input node 210 associated with V_{cc} (having a lower input power supply level), as provided by Zhang, combined with Javanifard’s variable booster circuitry. Pet. 32. Javanifard is configured to “accommodate a given output level” (Ex. 1006, 2:22–24) by serially connecting charge pumps 110 and 120 according to row 3 of Table 1 to provide a higher voltage boost for a lower power supply level. Pet. 33–35. As shown in the above figure, the serial connections are achieved by having switch 130 on, switch 131 off, and no current flow through transistor 140 (*see* Ex. 1006, 4:22–36). “Because both 110 and 120 are two stage charge pumps, this means that charge pump 100 will effectively be a four stage charge pump with all four stages serially coupled.” Ex. 1006, 3:54–60 (cited at Pet. 34). Thus, as recited in limitation [1.2.2], the “selection of the first input node corresponds to a first number of booster stages” (the serially-connected pump stages 112, 114, 122, and 124).

Petitioner explains:

A POSITA would have understood that this statement of “approximately twice the output voltage at node 150” applies when the input voltage levels are the same, and in a design to accommodate “a given output level for different charge pump power supply input levels,” the configuration of row 3 with more serially connected stages provides more voltage boost for a lower power supply input level.

Pet. 35.

As explained above in the discussion of limitation [1.2.1], Javanifard discloses at least two objects of its invention, one of which is “to provide a charge pump that can accommodate different output levels for a given charge pump power supply input level” and another is “to provide a charge pump that can accommodate a given output level for different charge pump power supply input levels.” Ex. 1006, 2:19–24. Petitioner’s evidence that Javanifard describes using two voltage input levels to provide a “given output level” is consistent with the latter objective, as well as Zhang, which discloses the same goal.

Patent Owner does not dispute that the configuration described in the composite drawings of Examples A and B meets limitation [1.2.1], which we agree is supported by a preponderance of the evidence in this record.

[1.2.3] selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number; and

The Petition contends that the combination of Zhang and Javanifard teaches or suggests claim limitation [1.2.3]. Pet. 35–36 (citing Ex. 1003 ¶¶ 125–131).

To support this argument, Petitioner cites Table 1 of Javanifard, annotating it as follows (Pet. 34):

TABLE 1				
Switch 130	Switch 131	Charge Pump 110	Charge Pump 120	
OFF	OFF	ON	OFF	<i>a second number of booster stages, the second number being less than first number</i>
OFF	ON	ON	parallel-coupled to charge pump 110	
ON	OFF	ON	series-coupled to charge pump 110	<i>a first number of booster stages</i>
ON	ON	N/A	N/A	

Table 1 shows the four different position combinations of switches 130 and 131 and how the different positions (on or off) effect the coupling between the charge pumps. Ex. 1006, 3:19–22.

Petitioner contends that “to accommodate a given output level” (Ex. 1006, 2:22–24 (cited at Pet. 36)):

for the second input node with a higher power supply voltage, a POSITA would have configured the variable stage charge pump of FIG. 1 of Javanifard according to row 1 of Table 1 . . . , because row 1 of Table 1 provides a second (lower) number of serially connected booster stages to provide a lower voltage boost (by providing only charge pump 110 in operation and thereby having a lower number of serially connected booster stages).

Pet. 36–37.

Row 1, annotated above in red, shows switches 130 and 131 off. Petitioner contends that this selection would have been made by a POSITA “based on a design need for power saving mode.” *Id.* at 38 (citing Ex. 1006, 3:39–42). For this reason, as for limitation [1.2.2], Petitioner contends that it would have been obvious to one of ordinary skill in the art to select “pump stage designs to provide the required output voltage according to the different power supply input levels.” Pet. 38.

Dr. Stiegler testifies that it would have been obvious that “selection of the first input node (with a lower input power supply voltage level)

corresponds to a first number (a higher number e.g., 4) of booster stages, e.g., for generating the same output voltage as the selection of the second input node with a higher input power voltage level.” Ex. 1003 ¶ 119.

Petitioner’s argument is consistent with the objectives of Javanifard to provide a charge pump that can “accommodate different output levels for a given charge pump power supply input level” and also “a given output level for different charge pump power supply input levels.” Ex. 1006, 2:19–24.

Patent Owner does not dispute that the combination of Zhang and Javanifard as exemplified in composite drawings A and B meets claim limitation [1.2.3], which we find to be supported by a preponderance of the evidence before us.

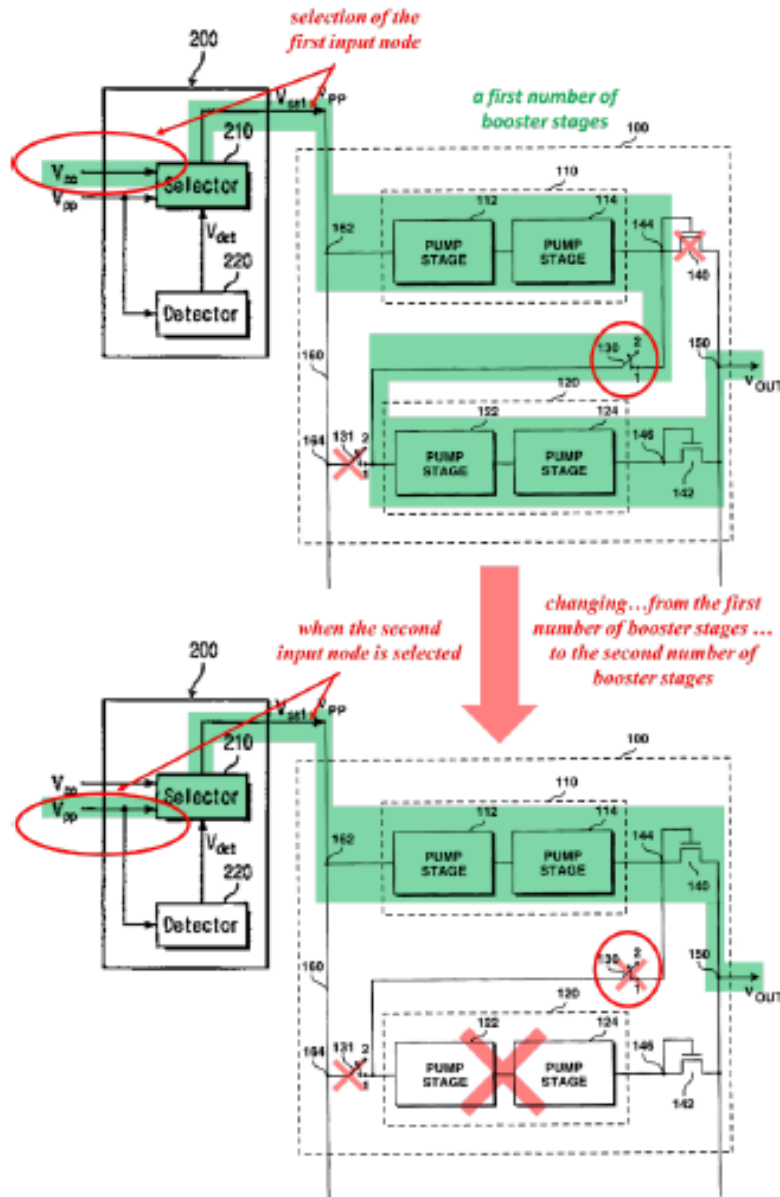
[1.3] *changing the booster circuitry from the first number of booster stages corresponding to selection of the first input node to the second number of booster stages when the second input node is selected.*

The Petition contends that the combination of Zhang and Javanifard teaches or suggests claim limitation [1.3]. Pet. 39–40. Citing Zhang, Figure 4, and Javanifard, Figure 1 and Table 1, as evidence, Petitioner explains that the number of booster stages in Figure 1 of Javanifard can be changed from 2 to 4 by changing the switch configuration. *Id.* Petitioner contends, based on its discussion of limitations [1.2.2] and [1.2.3], that

selection of the first input node corresponds to a first number of booster stages, and selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number, e.g., to provide the **same** output voltage for different power supply voltage levels.

Pet. 39.

As reproduced below, Petitioner shows in an annotated figure another modification of Example A of Zhang combined with Javanifard, and how the booster circuitry is changed by turning switch 130 from on to off. Pet. 41 (another modification of Example A of Zhang combined with Javanifard).



Petitioner-modified Example A shows switch 131 off and switch 130 being changed from on to off. When the lower power voltage VCC is selected (top), switch 130 is on, switch 131 is off, and four booster stages are

engaged. When the higher power supply VPP is selected (bottom), switch 130 is changed from on to off, and “the booster circuitry is changed from the first number of booster stages (e.g., 4) to the second number of booster stages (e.g., 2).” Pet. 40.

Annotated Table 1 showing this change is reproduced below (Pet. 40):

TABLE 1				
Switch 130	Switch 131	Charge Pump 110	Charge Pump 120	
OFF	OFF	ON	OFF	<i>a second number of booster stages, the second number being less than first number</i>
OFF	ON	ON	parallel-coupled to charge pump 110	
ON	OFF	ON	series-coupled to charge pump 110	<i>a first number of booster stages</i>
ON	ON	N/A	N/A	

Annotated Table 1 shows the four different position combinations of switches 130 and 131 and how the different positions (on or off) effect the coupling between the charge pumps. Ex. 1006, 3:19–22. The annotation in the Table 1 shows that when the selection of the input node is changed to the higher power supply voltage, the booster circuitry is changed from the first number of booster stages (e.g., 4) to the second number of booster stages (e.g., 2), by turning off switch 130. Pet. 40.

Patent Owner does not dispute that the combination of Zhang and Javanifard as exemplified in composite drawings A and B meets claim limitation [1.3]. which we find to be supported by a preponderance of the evidence before us.

4. *Reasons to combine*

The principal dispute in this *inter partes* review is whether Petitioner established a reason to combine Zhang and Javanifard. Primarily, the Petition pointed to disadvantages in the “prior art” identified by Javanifard,

and the solution to the disadvantages provided by Javanifard, as the motivation to apply Javanifard to Zhang's fixed stage circuit. Pet. 19–20 (citing Ex. 1003 ¶¶ 90–96). Specifically, the Petition identifies the following reasons as motivation to combine Zhang and Javanifard (citing Ex. 1006, 1:48–53; 1:66–2.2):

1. ““accommodate different output levels for a given charge pump power supply input level.””
2. ““accommodate a given output level for different charge pump power supply input levels.””
3. “provide flexibility for design needs (e.g., power saving mode, and current requirements).”
4. “area reduction.”
5. “performance improvement,” “including pump efficiency,” because ““the fixed stage method typically sacrifices performance at one power supply voltage to accommodate another power supply voltage.””
6. “provide a multipower-source charge pump to support a device having multiple operation modes.”
7. “no more than the combination of known elements according to known methods.”

As explained in more detail below, we find these reasons insufficient to have made it obvious to one of ordinary skill in the art to have combined Zhang and Javanifard in the manner proposed in the Petition.

1, 2. accommodate same or different outputs using same or different supply input voltages

Javanifard discloses:

One object is to provide a charge pump that can accommodate different output levels for a given charge pump power supply input level.

Another object is to provide a charge pump that can accommodate a given output level for different charge pump power supply input levels.

Ex. 1006, 2:18–24.

The Petition identifies the ability to perform both functions as an obvious and beneficial result achieved by applying Javanifard to Zhang. Pet. 20.

A POSITA would have been motivated to apply Javanifard’s teaching of a variable stage charge pump in Zhang’s multi-power-source charge pump system to produce the obvious, beneficial, and predictable results of a variable stage charge pump system, which can both “accommodate different output levels for a given charge pump power supply input level,” “accommodate a given output level for different charge pump power supply input levels.”

Pet. 19–20.

Patent Owner argues that both functions can be performed by Zhang. PO Resp. 18–20.

To address this issue, we first turn to Zhang. Figure 4 of Zhang, showing the design of its fixed-charge point design, is reproduced below:

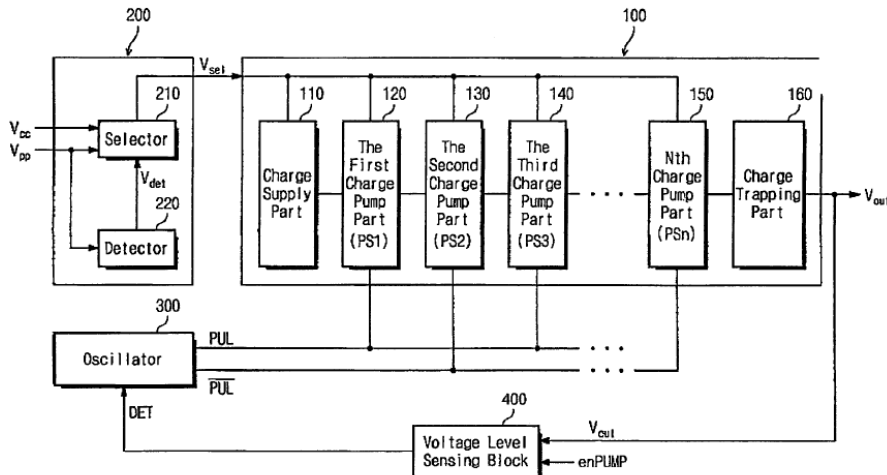


Figure 4 is a block diagram of Zhang's charge pump circuit comprising two power supplies, selecting circuit block 200, voltage level sensing block 400, and one fixed stage charge pump. Ex. 1005, 2:54–61.

Zhang explains that the voltage level sensing block 400 senses the level of output voltage, V_{out} , “when a pumping enable signal enPUMP is enabled.” Ex. 1005, 3:5–7. This signal determines whether Zhang's circuit is monitoring or regulating the output voltage. Specifically, when “the output voltage V_{out} is smaller than the reference voltage V_{ref} , the level sensing signal DET [V_{det}] is enabled.” *Id.* at 3:7–9. The enabling of the DET signal indicates that pumping action is required to raise the output voltage to the desired level. *Id.* Conversely, when “the output voltage V_{out} is larger than the reference voltage V_{ref} , the level sensing signal DET is disabled.” *Id.* at 3:10–12. The disabling of the DET signal indicates that no further pumping action is necessary because the desired voltage level has been reached.

The voltage “ V_{sel} ” in Figure 4 is the supply voltage provided to the charge pump circuitry. Ex. 1005, 2:62–67. Zhang discloses that V_{sel} is set to either the power supply voltage V_{cc} or the high external voltage V_{pp} ,

depending on the mode of operation. Specifically, Zhang states that “the signal VSEL is [power supply voltage] VCC in the general operation mode and [high external voltage] VPP in the test operation mode.” *Id.* at 3:36–38. In the test operation mode, Zhang’s circuit allows for a high output voltage “within a short time,” leveraging the higher Vpp voltage. *Id.* at 3:36–39.

Zhang further explains that a Vout of 10V can be achieved using either a Vsel of 1.8V (derived from Vcc in the general operation mode) or 8V (derived from Vpp in the test operation mode). Ex. 1005, 5:1–11. This capability arises from Zhang’s use of a fixed-stage charge pump architecture, which accommodates different input power supply voltages (Vcc or Vpp) to produce the same desired output voltage. By adjusting the pumping conditions based on the supply voltage, Zhang’s circuit enables the same output performance when different input voltages are applied.

In summary, Zhang’s design allows for achieving the same output voltage, such as 10V, using either the lower Vcc (e.g., 1.8V) or the higher Vpp (e.g., 8V). This flexibility is possible because the circuit dynamically adapts its pumping action in response to the selected power supply voltage, thereby “accommodating a given output level for different charge pump power supply input levels.” *Id.* at 5:10–11.

Zhang can also “accommodate different output levels for a given charge pump power supply input level.”⁶ Patent Owner’s expert Dr. Jacob testified that the output level of Zhang’s fixed-stage pump can be varied “by

⁶ Patent Owner asserts that “[n]owhere does the Petition explain how its proposed combination of Zhang with Javanifard would provide for *different* output voltages, or when those different output voltages would be used. See Ex. 2003 ¶¶75–76.” PO Resp. 9. We consider this issue moot because, as explained below, both Patent Owner and Petitioner acknowledge that Zhang can output different voltages by adjusting the Vref.

adjusting” Vref. Ex. 2003 ¶ 78 n.1. Patent Owner made similar statements on page 19 of the Patent Owner Response.⁷

Petitioner agreed with Dr. Jacob’s testimony:

MR. O’DELL:

...

So, in Zhang, I wanted to be clear that Zhang has an output as voltage selector circuit up front in a fixed booster circuitry 100, and a single output voltage VOUT. That VOUT can be moved—can be boosted to different levels. And I don’t believe the parties are in disagreement here. And in fact, I have a quote from the Patent Owner that a POSITA would readily recognize that Zhang does encompass generating multiple voltages by changing this feedback signal VREF, that it’ll be one voltage at a time, of course. It’s just one output then.

Tr. 6:1–8.

JUDGE MCKONE: But I think you’ve also admitted that Zhang teaches the same thing [as Javanifard], that you can adjust voltages, you know, after you’ve manufactured the circuit. That’s what that VREF signal is.

MS. SHI: You’re right.

JUDGE MCKONE: Your co-counsel has already conceded that point.

MS. SHI: Yes, exactly. And that’s correct. But Zhang uses VREF to adjust the VOUT. So, it cannot adjust the number of the stages [as in Javanifard] as I just described.

Id. at 16:9–17

JUDGE LEBOVITZ: . . . But my question is, it looks like you can use Javanifard to change the voltage by using series. So, that’s one way of doing it. But you could also change

⁷ “Zhang’s design already accommodates such a result with a simple variation in the Vref voltage level. *See* Ex. 2003 ¶ 110 (‘A person of skill would have easily recognized that, if he varied the Vref voltage, Zhang’s voltage Level Sensing Block 400 would trigger at different voltage levels and thus would provide different output voltages.’).” (Emphasis omitted).

the voltage in Zhang by changing the VREF. And you've admitted that, right?

MS. SHI: Correct.

Id. at 16:19–25.

Despite these admissions, Petitioner argues in its Reply that Patent Owner's assertion "'to reach any desired output level' by adjusting Vref is incorrect, because Vref is only used [to] regulate and fine tune Vout within the output voltage range determined by the stage numbers." Pet. Reply 12. To support this statement, Petitioner cites "EX1003, ¶35–38 (explaining that a regulator regulates Vout within the output range determined by the number of stages, citing EX1014, Frulio, FIGS. 1–2, 1:40–47); EX1005, FIG. 2 (illustrating that Vref 270 is used to regulate Vout of variable stage charge pumps); EX1014, Frulio, FIG. 7." Reply 12–13.

Paragraphs 35–38 of the Stiegler declaration do not refer to Vref. Dr. Stiegler states, citing Ex. 1014 (Frulio) 1:40–47, that "a regulator circuit 16 may be used to ensure that the output voltage does not exceed a maximum value and does not drop below a minimum value." Ex. 1003 ¶ 35. But these disclosures from the Stiegler declaration (Ex. 1003), Zhang (Ex. 1005), and Frulio (Ex. 1014) do not disclose that voltage output is limited to certain output levels and could not be changed to the desired level by adjusting Vref.

With respect to the asserted beneficial function of being capable of "accommodate[ing] a given output level for different charge pump power supply input levels" (Pet. 20), as explained above, it is undisputed on the record that Zhang uses two different voltage sources, Vcc and Vpp, to achieve the same voltage out (Vout). *See* Ex. 1005, Fig. 8; PO Resp. 14 ("For example, Zhang's Figure 8 . . . makes clear that the final output

voltage level in Zhang is the *same* (10V) regardless of what input voltage is applied.”).

In sum, the purported benefits described by Petitioner for modifying Zhang with Javanifard’s teaching of providing the ability to accommodate the same voltage output levels using different power supply input levels and to accommodate different output levels using the same charge pump supply input level (by varying the V_{ref}) can be achieved by Zhang, alone. Zhang does not require modification with Javanifard’s teaching to achieve both these functions. *See also* PO Resp. 19.⁸

Under 35 U.S.C. § 103(a), a motivation to combine references does not require identifying a deficiency or problem in Zhang.⁹ However, there must be a reason to combine the references that is supported by the evidence. Here, Petitioner’s asserted motivation for combining Javanifard with Zhang is that it allows the resulting device to achieve the same two objectives described by Javanifard: (1) accommodating the same output

⁸ “Thus, to the extent the Petition contends there would be an advantage to ‘accomodat[ing] different output levels for a given charge pump power supply input level,’ Zhang’s design *already* accommodates such a result with a simple variation in the V_{ref} voltage level. *See* Ex. 2003 ¶ 110 (‘A person of skill would have easily recognized that, if he varied the V_{ref} voltage, Zhang’s voltage Level Sensing Block 400 would trigger at different voltage levels and thus would provide different output voltages.’).”

⁹ “[T]he suggestion to combine references may flow from the nature of the problem.” *Ecolchem, Inc. v. Southern California Edison Co.*, 227 F.3d 1361, 1372 (Fed. Cir. 2000). But here, Petitioner does not identify a problem with Zhang that is solved by the teachings in Javanifard. Petitioner asserts that the motivation to apply Javanifard to Zhang is “to produce the obvious, beneficial, and predictable results of a variable stage charge pump system” which can generate the same given output using different supply input levels and different output levels using the same given power supply. Pet. 20.

voltage with different power supply input levels and (2) accommodating different output voltages with the same power supply input level. Ex. 1006, 2:18–23. These two objectives are already met by Zhang’s design and are achieved without the need for modification. Zhang’s use of two power supply inputs (e.g., V_{cc} and V_{pp}) allows it to produce the same output voltage regardless of the input source, as seen in Figure 8. Zhang also uses its V_{ref} mechanism to vary the output voltage for a given input as acknowledged by both parties. Ex. 2003 ¶ 78 n.1.; Tr. 6:1–8; 16:9–17.

Thus, Zhang already achieves the stated objectives without the need for Javanifard’s teachings.

In sum, Petitioner did not present an evidence-supported rationale for the proposed modification. The proposed motivation collapses because the very functions identified as reasons for combining the references are fully realized by Zhang’s existing design. Petitioner cannot simply reiterate the functions Zhang already performs as a rationale for combining it with Javanifard without showing why a person of ordinary skill in the art would have had reason to do so. Petitioner’s asserted motivation to combine the two references amounts to conclusory reasoning insufficient to support a finding of obviousness.

Petitioner appears to recognize the weakness of its argument by subsequently making the argument that “the uncontested foundational advantage of Javanifard—configurability of the stage topology that enables those potential benefits based on design needs—alone is sufficient for motivation to combine Zhang and Javanifard.” Pet. Reply 8. But, as indicated by Patent Owner, this argument is a “new theory” and a new argument that was not presented in the Petition. PO Sur-reply. It is

impermissible to raise a new theory of unpatentability in a reply.

Corephotonics, Ltd. v. Apple Inc., 84 F.4th 990, 1008 (Fed. Cir. 2023).¹⁰

The phrase “configurability of the stage topology” does not appear in the Petition nor does Petitioner identify where this concept was discussed in the Petition. For the first time, Petitioner, in its Reply, refers to row 2 of Table 1 of Javanifard, and provides a table identifying six configurations of Javanifard to illustrate the asserted “configurability of the stage topology.” Pet. Reply 6–7. However, the Petition’s Ground 1 does not discuss, nor even mention “row 2” of Javanifard’s Table 1, yet it appears in Petitioner’s newly presented table in its Reply with its output level identified. *See* PO Resp. 6.

In its Reply, Petitioner asserts the “foundational advantage of Javanifard” as motivation was not contested by Patent Owner, but Petitioner fails to identify where this motivation was described in the Petition. Pet. Reply 7. Petitioner points to pages 12–24 of the Patent Owner Response in

¹⁰ “We begin by further explaining the permissible scope of an IPR petitioner’s reply. The [Administrative Procedure Act (APA)], the IPR statute, the Board’s regulations, and our precedents collectively impose two separate, but related, restrictions on what a petitioner may include in its reply. First, the arguments and evidence in the reply must not be part of a new theory of unpatentability. Second, the arguments and evidence in the reply must be responsive to the patent owner’s contentions or the Board’s institution decision.

The ‘newness’ restriction prohibits the petitioner from raising, in reply, ‘an entirely new theory of prima facie obviousness absent from the petition,’ even if the new theory is responsive to the patent owner’s response or the Board’s institution decision. [*Wasica Finance GmbH v. Continental Automotive Systems, Inc.*, 853 F.3d 1272, 1286 (Fed. Cir. 2017)]; *see also* 35 U.S.C. § 312(a)(3) (requiring petition to identify ‘with particularity . . . the grounds on which the challenge to each claim is based’). Determining whether a reply has improperly raised a new theory or argument requires a comparison between the petitioner’s petition and the petitioner’s reply.”

an apparent attempt to establish that its argument is responsive to Patent Owner's Response (Paper 18) to the Petition, but Petitioner fails to specifically identify in those 13 pages where and what was Patent Owner's response and the particular argument in Patent Owner's Response Petitioner is addressing in its Reply. Pet. Reply 7. *See* 37 C.F.R. § 42.23(b) ("A reply may only respond to arguments raised in the corresponding opposition, patent owner preliminary response, patent owner response, or decision on institution."). Simply referring broadly to 13 pages of a response without pinpointing specific arguments does not demonstrate compliance with 37 C.F.R. § 42.23(b) because it is not responsive to an argument made in Patent Owner's Response. In fact, Patent Owner did not contest this motivation because it was argued for the first time in Petitioner's Reply.

In sum, Petitioner's stated reason to have combined Zhang and Javanifard is not persuasive.

3. "[P]rovide flexibility for design needs (e.g., power saving mode, and current requirements)."

Petitioner contends that Javanifard's variable stage charge pump provides "flexibility for various design needs (e.g., configurations based on power saving mode, and/or current requirements)." Pet. 20, 21 (citing Ex. 1006, 2:18–24, 3:39–42, 3:50–53).

Patent Owner responds that the Petition "provides no evidence" that the ordinarily skilled worker would view Zhang as lacking flexibility. PO Resp. 18. Patent Owner argues that "'Zhang's sensor-driven approach is arguably more flexible than Javanifard, because it allows one to reach any desired output level by adjusting the Vref voltage level accordingly.'" *Id.* at 18–19 (citing Ex. 2003 ¶ 78 n.1).

In its subsequent Reply, Petitioner contends that its newly created table (appearing on page 6 of Petitioner’s Reply) “illustrates another motivation not contested by [Patent Owner]: Javanifard provides the configurability of the stage topology including the coupling of stages in series/parallel for different output current levels (e.g., configurations 1 and 2), which provides flexibility for various design needs (e.g., power save mode, output current levels).” Pet. Reply 7.

Petitioner also argues that Patent Owner “does not even dispute Javanifard’s benefits of ‘flexibility for design needs (e.g., power saving mode, and current requirements)’ achieved by configurability of the stage number as explained by [the] Petition.” Pet. Reply 12 (citing Pet. 20–21).

Petitioner’s arguments do not persuade us that the Petition met the burden of establishing that one of ordinary skill in the art would have been motivated to combine Zhang and Javanifard to “provide flexibility for design needs (e.g., power saving mode, and current requirements).” Pet. 20.

While Petitioner argues that Javanifard’s variable stage charge pump provides configurability for different design needs, including power saving modes and output current levels (Pet. Reply 12–13), Petitioner does not provide factual evidence to support the contention it would have been obvious to apply this teaching to Zhang. Specifically, Petitioner’s Reply and accompanying Stiegler declaration (Ex. 1003) lack an adequate factual basis to show that the ordinarily skilled worker would have viewed Zhang as deficient in flexibility or that Javanifard’s flexibility would be necessary or desirable in Zhang’s system. In contrast, Patent Owner provided sufficient evidence that Zhang’s method of adjusting output levels via V_{ref} voltage is “arguably more flexible than Javanifard.” PO Resp. 18–19. This point is further supported by evidence from Patent Owner’s expert, which

undermines the weight of Petitioner's assertion that Javanifard offers this unique advantage that would motivate the combination. Ex. 2003 ¶ 78.¹¹

Petitioner's reliance in its Reply on the newly created table to illustrate the configurability of Javanifard's stage topology is unpersuasive. *See* Pet. Reply 6 (showing table with six rows). The table is considered part of the impermissible new theory of unpatentability that was not presented in the Petition. Nonetheless, we note that Petitioner asserts that there are six possible configurations in Example A of the combination of Zhang and Javanifard, and that "some configurations (e.g., configurations 1 (and 2) and 3 for Vcc) enable different output voltage levels (Voltage Levels 1 and 2) with the same input level, and some configurations (e.g., configurations 3, 4, and 5 for Vcc and Vpp) enable a given output voltage level (e.g., Vout Level 2) with different input levels." Pet. Reply 6. Zhang, however, as explained above, is capable of performing both functions.

Petitioner, relying on the same new theory, also contends the table "illustrates another motivation not contested by [Patent Owner]: Javanifard provides the configurability of the stage topology including the coupling of stages in series/parallel for different output current levels (e.g., configurations 1 and 2), which provides flexibility for various design needs (e.g., power save mode, output current levels)." Pet. Reply 7.

¹¹ "Zhang's sensor-driven approach is arguably *more* flexible than Javanifard, because it allows one to reach any desired output level by adjusting the Vref voltage level accordingly (Zhang causes the charge pump to stop when the desired level is reached), whereas Javanifard can only reach output levels that correspond to the number of charge-pump stages in series. Zhang can thus target in-between voltage levels that Javanifard cannot." Ex. 2003 ¶ 78 n.1.

This argument was not made in the Petition. The Petition reproduced and annotated Javanifard's Table 1, but only discussed row 1, two stages series coupled, and the four series-coupled pumps in row 3. Pet. 34. There was no discussion or mention of row 2, where the charge pumps are parallel-coupled. *Id.* In contrast, the new table in Petitioner's Reply, which is based on Javanifard's Table 1, identifies, for the first time, row 2 as an advantage of Javanifard, and a reason to modify Zhang with it. Pet. Reply 6–7. This argument is an impermissible new theory of patentability. *Corephotonics*, 84 F.4th at 1008. Moreover, even if we were to consider this argument, it would not be persuasive, as Petitioner cites no evidence to support its attorney argument. Pet. Reply 6–7.

Ultimately, the evidence and arguments presented by Petitioner fail to demonstrate that one of ordinary skill in the art would have been motivated to apply Javanifard's teachings to Zhang by the desire to achieve flexibility for design needs. Consequently, Petitioner has not met the burden of showing a persuasive rationale for combining Zhang and Javanifard.

4. “[A]rea reduction”

The Petition identifies “area reduction” as an obvious benefit of applying Javanifard's teachings to Zhang. Pet. 20. Javanifard discloses:

One prior art method used to generate multiple higher voltage levels *from a single power supply voltage* is to use a number of charge pump circuits each having a fixed number of stages. One disadvantage of this method is that each charge pump circuit requires a dedicated space in the integrated circuit.

Ex. 1006, 1:48–53 (emphasis added).

The Petition asserts that Javanifard “achieves area reduction by using a single variable stage charge pump circuit to provide different output levels,

and improves performance (e.g., pump efficiency) by configuring the number of pump stages based on the power supply voltage and the desired output voltage level.” Pet. 21.

Patent Owner responds:

In other words, Javanifard teaches that the use of multiple separate charge pump circuits is problematic because adding multiple charge pump circuits to a system requires additional physical space. The Petition relies on this stated disadvantage as relating to “area usage.” *See* Pet. 20. But as . . . explained by Dr. Jacob, Zhang’s Figure 4 embodiment does not have that problem, because only a *single* charge pump circuit is required. Ex. 2003 ¶78 (“Zhang can be made smaller than other charge pumps, due to the additional voltage input (see element 200 in the figure below), and it is a single-pump design, not a multiple-pump design) . . .”).

PO Resp. 17.

Petitioner replies that Patent Owner’s argument that Javanifard does not apply to Zhang is circular because “Zhang’s system does not provide multiple output levels and as such requires ‘only a single charge pump circuit.’ [PO Resp.] 14–15, 17.” Pet. Reply 10. Petitioner states that “providing multiple higher voltage levels was a well-known need in the electronics field,” and that “Zhang’s lack of multiple output levels alone provides a motivation to combine: Javanifard’s variable stage charge pump provides a suitable option for addressing Zhang’s need for multiple output levels.” *Id.*

Patent Owner’s contention that Javanifard does not apply to Zhang, because the disadvantage in space disclosed by Javanifard is not a characteristic of Zhang, is supported by persuasive evidence in this record. Javanifard specifically states that when generating higher voltage levels “from a single power source,” the “prior art method” is “to use a number of

charge pump circuits each having a fixed number of stages,” which is disadvantageous because “each charge pump circuit requires a dedicated space in the integrated circuit.” Ex. 1006, 1:48–53. However, Zhang uses two power sources, not a single source, and therefore Patent Owner is correct that the stated disadvantage does not apply to Zhang. Dr. Jacob testified, and we agree, that “Zhang can be made smaller than other charge pumps, due to the additional voltage input . . . , and it is a single-pump design, not a multiple-pump design; the extra voltage input allows Zhang to achieve higher voltages more quickly than other charge pumps.” Ex. 2003 ¶ 78.

Petitioner’s response is to attack Dr. Jacob’s expertise (Pet. Reply 11), ignoring his experience in circuit design. Ex. 2003 ¶¶ 13, 15 (Dr. Jacob holds three patents “in the area of circuit design”), 17; Ex. 1029, 42:19–23 (“Q. Have you drawn a schematic of a charge pump that was eventually implemented according to your design of physical product? A. Well, yeah. I just told you. We built these in a lab at Maryland.”).

As far as the alleged “circularity” because Zhang does not provide multiple output levels (Pet. Reply 10), we have already addressed this issue and found, based on the evidence of record, that Zhang’s fixed-stage charge pump can produce multiple output levels by adjusting the V_{ref} . Ex. 2003 ¶ 78 n.1.

In sum, Petitioner’s stated reason to have combined Zhang and Javanifard is not persuasive.

5. “[P]erformance improvement,” “including pump efficiency,” because “the fixed stage method typically sacrifices performance at one power supply voltage to accommodate another power supply voltage.”

Javanifard discloses that a disadvantage of the prior art “is that the fixed stage method typically sacrifices performance at one power supply voltage to accommodate another power supply voltage.” Ex. 1006, 1:66–2:2. Petitioner identifies this as a deficiency in Zhang’s fixed stage circuit that would be improved by Javanifard’s teachings. Pet. 20, 21. Petitioner’s expert Dr. Stiegler testifies in his declaration that performance is improved, “e.g., pump efficiency,” “by configuring the number of pump stages based on the power supply voltage and the desired output voltage level.” Ex. 1003 ¶ 92.

Patent Owner responds that the Petition does not show that Zhang “suffers from the problem” of sacrificing performance by adding another power supply to a charge pump circuit having a fixed number of stages. PO Resp. 18 n.6. Dr. Jacob, Patent Owner’s expert, testifies that Dr. Stiegler does not describe how this disadvantage applies to Zhang. Ex. 2003 ¶ 78. To the contrary, Dr. Jacob explains that “the extra voltage input [of the second power supply] allows Zhang to achieve higher voltages more quickly than other charge pumps (i.e., Zhang is extremely efficient).” *Id.*

In response, Petitioner cites Exhibits 1003, 1020, 1026, and 1030 as establishing that “the number of stages determines voltage boosting capabilities, and impacts critical performance factors such as efficiency, current output, and overall circuit complexity.” Pet. Reply 8–9.

Exhibits 1026 and 1030 are newly cited by Petitioner. Pet. Reply iv. A petitioner “may introduce new evidence after the petition stage if the evidence is a legitimate reply to evidence introduced by the patent owner.” *Anacor Pharms., Inc. v. Iancu*, 889 F.3d 1372, 1380–82 (Fed. Cir. 2018).

See also Patent Trial and Appeal Board Consolidated Trial Practice Guide (Nov. 2019), 73 *available at*

<https://www.uspto.gov/TrialPracticeGuideConsolidated> (“Petitioner may not submit new evidence or argument in reply that it could have presented earlier, e.g., to make out a prima facie case of unpatentability.”). Newly cited Exhibits 1026 and 1030 are not identified by Petitioner as responsive to Patent Owner’s Response. Rather, the new evidence cited by Petitioner is improperly being used to supply evidentiary support for an argument made in the Petition that lacked such support. A reply cannot be used to introduce new evidence to fill gaps in the Petition or bolster arguments that were inadequately supported in the Petition. The introduction of such evidence constitutes an improper attempt to remedy deficiencies in the Petition, which should have initially contained necessary evidence and arguments to support Ground 1. Accordingly, we find that the introduction of Exhibits 1026 and 1030 as evidence for Ground 1 is impermissible.

Although not necessary, we have considered these references to the extent they have been referenced in Petitioner’s Reply.

Exhibit 1026 is cited by Petitioner as providing “an optimized strategy for designing charge pumps with minimum power consumption” by “defin[ing] the number of stages that, for a given input, and an output voltage, maximize power efficiency” (*id.* at 1535) and as defining “charge-pump efficiency” as the ratio of output power over input power (*id.* at 1537). Pet. Reply 8 (quoting from Ex. 1026). While Patent Owner contends that this disclosure describes the characteristics of Javanifard, without more, it does not alone define the reason to apply these teachings in Javanifard to Zhang and is unsupported by factual evidence.

Petitioner's Reply further cites Exhibit 1030 as describing a variable stage charge pump, where "[i]n order to maximize the current output from the charge pump, . . . the number of stages N can be opportunely chosen." Pet. Reply 9. Again, these are characteristics of a variable stage charge pump and not a reason by itself to modify Zhang with such a pump.

Exhibit 1020 (Kang) was cited in Grounds 3 and 4 in the Petition. Pet. 5. Kang was never cited in the Petition as evidence under Ground 1. Petitioner's Reply cites page 261, with no explanation of the relevance. Pet. Reply 9. Page 261 has graphs of pump efficiency, but Petitioner does not explain how these graphs and the underlying disclosure provide a reason to combine Zhang and Javanifard.

In cited paragraph 36 of the Stiegler declaration, Dr. Stiegler states that it was "well-known" that a charge pump can include one or more stages which contribute to the total voltage boost. Ex. 1003 ¶ 36. This is simply a generic statement of the known properties of a variable stage charge pump, such as the variable charge pump of Javanifard. Dr. Stiegler's testimony in this paragraph provides no reason to modify Zhang to improve performance when a second power supply is added to a first power supply, the basis of Petitioner's reason 5 to modify Zhang with Javanifard's teachings. Ex. 1006, 1:66–2:2. Dr. Stiegler merely asserts a fact without providing a rationale for combining the teachings of the two references.

Patent Owner's expert Dr. Jacob testifies Zhang's pump is "extremely efficient" and "at least as flexible" as "Javanifard's reconfigurable stages in its ability to target different output levels." Ex. 2003 ¶ 78.

Petitioner responds that the "allegedly 'extremely efficient' in time [for Zhang's fixed stage charge pump] . . . [is] completely misplaced, failing to address Javanifard's performance advantage including power conversion

efficiency.” Pet. Reply 11. Petitioner, however, does not provide factual evidence, such as expert testimony, etc., to establish that Dr. Jacob’s testimony about Zhang’s fixed stage charge pump and its efficiency is factually incorrect or “misplaced.” We note that the phrase “power conversion efficiency” does not even appear in the Petition nor in Javanifard; Petitioner fails to identify where in the Petition or in Javanifard this concept is discussed.

Petitioner further contends that Dr Jacob’s “misplacements are consistent with Dr. Jacob’s lack of experience with charge pump performance (including power conversion efficiency) as admitted at deposition.” Pet. Reply 11. Petitioner cites Dr. Jacob’s response in his deposition to the question “You have never measured the performance of a charge pump” of “I don’t. It is not something that I do,” as evidence of his inexperience. *Id.* at 11 (quoting from Ex. 1029, 40:12–20).

We disagree with Petitioner’s contention that Dr. Jacob lacks experience in charge pump design. Previously in the deposition, Dr. Jacob made the following statements, indicating he was knowledgeable about measuring charge pump efficiency and performance:

Q. And will there be -- how do you measure the efficiency of the charge pumps conversion?

MR. MILKEY: Object to form.

THE WITNESS: It depends on what your metric is.

BY MS. SHI:

Q. What are some examples of the metric?

A. Well, this was your question. Tell me what you are trying to measure.

Q. What if we would like to measure the power efficiency?

A. And by that, what do you mean?

Q. So what are the metrics for measuring – are you aware of any metrics for measuring the performance of a charge pump?

MR. MILKEY: Objection to form.

THE WITNESS: There are ways to measure the behavior of the charge pump. Like, for instance, what voltage it produces, and how long it takes to get there.

Ex. 1029, 22:16–34:9.

Petitioner further questions Dr. Jacob:

Q. Are you aware of any other parameters for measuring the behavior of the charge pump in addition to the voltage level it produces and the time it takes to get there?

MR. MILKEY: Objection to form.

WITNESS: I am not exactly sure what you are trying to get at. I mean, if you are asking about what are the metrics that we care about regarding charge pumps, well, for instance, how big it is matters. How big is the circuit -- how big are the capacitors that you are using and so forth. There are a number of metrics.

BY MS. SHI:

Q. What are the number of metrics --

A. I don't --

Q. -- other than the one which you mentioned?

MR. MILKEY: Objection to form.

THE WITNESS: I don't know off the top of my head how many metrics there are.

Ex. 1029, 35:4–22.

Dr. Jacob further testified that while he was aware of the metrics, he did not have them “memorized,” but if given a “list,” he could tell “whether or not they applicable.” Ex. 1029, 36:12–23. He was not given a list.

When asked about whether the frequency of the clock signal coming from the bottom plate of a charge could “affect the power efficiency” of the charge pump discussed in paragraph 25 of Dr. Jacob’s declaration, he responded “for instance, if you run the frequency faster than you can charge up the capacitor, then you get a non-functioning boost circuit” that “doesn’t

actually boost the voltage,” further indicating his knowledge of charge pump efficiency. Ex. 1029, 39:15–40:7. Dr. Jacob testified in his declaration that he does not measure charge performance himself, but he further noted that he “drew . . . semantics [schematics]” for charge pump designs, and they were built in his lab at the University of Maryland.¹² Ex. 1029, 40:24–25.

Thus, in contrast to Petitioner’s allegations, the facts in the record support Dr. Jacob’s experience in charge pump design and his corresponding testimony about Zhang’s fixed stage charge pump and its efficiency and flexibility. Ex. 2003 ¶ 78.

Petitioner cites Exhibits 1020, 1026, 1027, and 1030, which Petitioner impermissibly attempts to introduce as new evidence to support unpatentability challenge Ground 1. Pet. Reply 12. We have considered these references to the extent they have been characterized in Petitioner’s Reply, i.e., as evidence to show that pump efficiency and the number of stages are critical design factors impacting power conversion efficiency. *Id.* Petitioner contends that Dr. Jacob failed to recognize these factors. *Id.*

While the factors identified in these references were not discussed by Dr. Jacob, the expert indicated an awareness of factors (“metrics”) associated with power efficiency, demonstrating a broad understanding of the topic. *See* Ex. 1029, 34:21–35:15; *see also* 41:1–43:10, 43:18–44:11, 45:9–17 (describing his experience in designing charge pump circuits). As

¹² Q. You said, “We built these in the lab at Maryland.” What do you mean by “we”?

A. The students. I ran a lab, I taught it, I showed the students how to build a charge pump in class.

Q. Did you or your students build the charge pump?

A. Both.

Ex. 1029, 43:4–10.

such, these references do not establish that Dr. Jacob lacks the expertise necessary to evaluate the power efficiency of Zhang's circuit. While Petitioner, in citing Exhibits 1020, 1026, 1027, and 1030, highlights certain factors influencing power efficiency, Dr. Jacob's acknowledgment of the relevant metrics indicates his ability to assess power efficiency.

Furthermore, as indicated above in his deposition, Dr. Jacob testifies that he does not measure pump efficiency himself, but he has experience in charge pump design, is aware of the metrics used to measure charge pump efficiency, and taught students how to build charge pump circuits. For example, Dr. Jacob mentions size of capacitors as influencing pump performance. *Id.* at 25:9–14. Dr. Stiegler also describes capacitor choice as a factor in charge pump design. Ex. 1003 ¶ 297. Consequently, these additional references do not undermine Dr. Jacob's qualifications or his ability to provide a credible assessment of the power efficiency of Zhang's charge pump circuit.

In sum, Petitioner's stated reason to have combined Zhang and Javanifard is not persuasive.

6. *“provide a multipower-source charge pump to support a device having multiple operation modes”*

Dr. Stiegler testifies in his declaration that Zhang teaches that its charge pump circuit is not limited to test or general operation modes.

Ex. 1003 ¶ 94. Dr. Stiegler states:

As such, a POSI[T]A would have been motivated to apply Javanifard's teachings in Zhang to provide a multipower-source charge pump to support a device having multiple operation modes, including a device having “a test or general operation mode” and devices having other operation modes (e.g., a

memory device having different read, write, programming modes). *See, e.g.*, EX1006, Javanifard, FIG. 2 (illustrating variable stage charge pumps used for a multi-power-source memory device with different modes).

Id. (see also Pet. 22).

We initially note that Javanifard's Figure 2, which is not the figure of Javanifard combined with Zhang, has three outputs, while the combination suggested by Petitioner as shown in Example A (Pet. 30) and Example B (Pet. 31) has only a single output. *See* PO Resp. 21; PO Sur-reply 2. We therefore agree with Patent Owner that Figure 2 is not pertinent to the patentability challenge because it has a different configuration than put forth by Petitioner in Ground 1. *Id.*

As far as the alleged advantage of having multiple operations modes, Zhang has at least two modes of operation and, as acknowledged by Petitioner, the V_{ref} can be used to vary the voltage output level, providing other output voltages and modes of operation. *See supra.* at 38–40. Consequently, we are not persuaded that Javanifard's ability "to provide a multipower-source charge pump to support a device having multiple operation modes" is a sufficient reason to modify Zhang with Javanifard's teachings. Pet. 22.

In sum, Petitioner's stated reason to have combined Zhang and Javanifard is not persuasive.

7. *"no more than the combination of known elements according to known methods"*

Petitioner asserts that the application of Javanifard's teachings to Zhang "applying Javanifard's teachings in embodiments of Zhang would have been no more than the combination of known elements according to

known methods (e.g., incorporating a charge pump circuit design in a multi-power-source charge pump system according to the known IC design) obvious to a POSITA.” Pet. 22. Petitioner contends that techniques for configuring charge pumps and designing circuits were well-known. *Id.* at 22–23.

Patent Owner argues that the asserted motivation “is simply a high-level summary statement of what the combination is, accompanied by attorney argument that the combination would be done “according to known methods.” PO Resp. 24 (citing Pet. 22–23). Patent Owner contends that no evidence has been provided by Petitioner to support this allegation. *Id.* To the contrary, Patent Owner argues that “a POSITA would recognize that IC design is far from straightforward when analog design techniques (such as charge pump circuits) are used.” *Id.* at 25 (citing Ex. 2003 ¶ 91; Ex. 2005 (preface)). But Patent Owner argues that even if the combination of Zhang and Javanifard is no more than a combination of known elements, as asserted by Petitioner, there must still be a reason to combine them in the way the claim does. PO Resp. 26 (citing *KSR*, 550 U.S. at 418–19). Patent Owner, as explained above, contends that the motivation to combine Zhang and Javanifard is deficient. *Id.*

In its Reply, Petitioner cites evidence for the first time that combining the recited elements “was a basic and well-known practice prior to the ’701 [p]atent.” Pet. Reply 13–14 (referencing newly cited Ex. 1025, Ex. 1027, and Ex. 1028). Petitioner annotated a figure from Exhibit 1027 showing a DC power supply and switch connected to a charge pump. *Id.* at 14. Petitioner does not explain how the annotation provides a reason to have taken the circuit block of Zhang comprising the switch and power supply

and combining it with Javanifard's charge pump. Pet. 30. Zhang's Figure 4 already shows a power supply switch connected to a charge pump.

Notwithstanding that the newly cited references were not cited in the Petition and have not been shown to be responsive to an argument made in Patent Owner's Response, we find Petitioner's reasoning to be defective. As indicated by Patent Owner, although the Supreme Court emphasized "an expansive and flexible approach" to the obviousness question, *KSR*, 550 U.S. at 415, it also reaffirmed the importance of determining "whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *Id.* at 418. Thus, as the Federal Circuit has since explained, "obviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention." *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015). Here, as explained above, Petitioner did not provide sufficient reason to combine Zhang and Javanifard to make the claimed method for generating a supply voltage of claim 1.

5. *Summary*

Based on the entire record, and for the reasons discussed above, Petitioner has failed to establish by a preponderance of the evidence that claim 1 is unpatentable under § 103(a) as obvious based on Zhang and Javanifard.

6. *Claims 2–18*

Petitioner asserts that claims 2–9, which depend from claim 1, and claims 11–18, which depend from independent claim 10, are unpatentable

under 35 U.S.C. § 103(a) as obvious based on the combination of Zhang and Javanifard. Pet. 42–61.

Claim 10 has substantially the same limitations as claim 1, but the claim is directed to a semiconductor device. The Petition relies on essentially the same findings and reasons for finding claim 10 obvious based on Zhang and Javanifard as for the obviousness of claim 1. Pet. 57–60. Accordingly, as for claim 1, Petitioner has failed to establish by a preponderance of the evidence that claim 10 is unpatentable under § 103(a) as obvious based on Zhang and Javanifard.

All the dependent claims recite, or incorporate by dependency, the limitations of claims 1 and 10 which, as discussed above, are not described or suggested by the combination of Zhang and Javanifard as proposed in the Petition.

Because Petitioner has failed by a preponderance of the evidence to establish sufficient reason to combine Zhang and Javanifard to meet all the limitation of claims 1 and 10, the unpatentability challenge to dependent claims 2–9 and 11–18, which depend on independent claims 1 and 10, and incorporate all their limitations, also fails.

E. Obviousness challenge based on Javanifard

Petitioner challenges the patentability of claims 1–18 under 35 U.S.C. § 103(a) as obvious over Javanifard. Pet. 62–86.

The patentability challenge is based on the obviousness of combining 1) Javanifard’s power supply circuitry for a flash memory including variable stage charge pumps for accommodating three different voltage levels from two different power supplies as illustrated in Figure 2 (Ex. 1006, 6:61–64) with 2) Javanifard’s variable stage charge pumps, illustrated in Figures 1 and

3, having a number of booster rungs, each rung having one or more fixed charge pump stages (Ex. 1006, 2:42–53). The charge pumps of Figures 1 and 3 are illustrated as having only one power supply. The claim requires two.

The Petition contends that it would have been obvious to apply Figure 2’s teaching of two power sources (Embodiment 2) to the variable stage charge pump of Figures 1 or 3, having only a single voltage supply (Embodiments 1 and 3), “to produce the obvious, beneficial, and predictable results of a multi-power-source variable stage charge pump system.” Pet. 64 (citing Ex. 1003 ¶ 206; Ex. 1006 6:44–46; Ex. 1005, code (57), Fig. 4).¹³ The Petition further contends that the motivation to combine Figure 2 and Figures 1 or 3 is based on Javanifard’s object to “accommodate a given output level for different charge pump power supply input levels.” Ex. 1006, 2:21–23 (cited at Pet. 64).

The Petition also asserts that the combination of Embodiment 2 with Embodiments 1 or 3 “would have been no more than the combination of known elements according to known methods (e.g., incorporating a power source selection design in a variable stage charge pump according to well-known IC design techniques including voltage detection and selection) obvious to a POSITA, which does no more than yield predictable results.” Pet. 64–65 (citing Ex. 1003 ¶ 208; Ex. 1005, Fig. 4).

¹³ Figures 1, 2, and 3 are representative of what Petitioner calls Embodiments 1, 2, and 3, respectively. The terms are used interchangeability throughout this Decision. We do not consider them separate embodiments, however. Rather, as Patent Owner explains, Figures 1 and 3 are examples of circuitry that would be used in the circuit of Figure 2. PO Resp. 42.

Patent Owner does not challenge on the record before us that the individual elements of the claims are disclosed by Javanifard, but instead disputes the Petition's asserted motivation to combine the elements.

1. Independent Claim 1

We turn to claim 1 and Petitioner's contentions on how the limitations in the claim are met by the combination of Figure 2 with Figures 1 or 3 of Javanifard. Patent Owner has not disputed these contentions, which we find to be supported by sufficient evidence on the full trial record.

Petitioner's contentions for each limitation are summarized below.

[1.0] *1. A method for generating a supply voltage, comprising:*

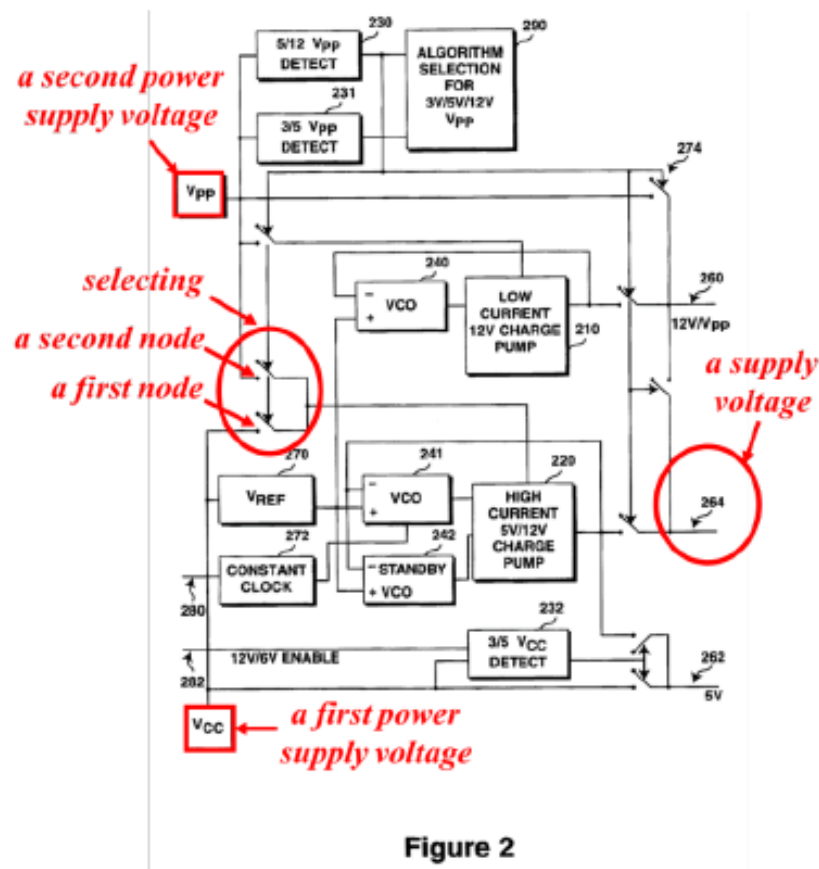
For claim preamble [1.0], the Petition cites Javanifard's disclosure, as illustrated in Figures 1, 2, and 3, of a variable stage charge pump generating a power supply for various devices. Pet. 65–66 (citing Ex. 1006, 5:17–24, 5:56–59, Figs. 2, 3, which illustrate generating a supply voltage to a memory device).

Patent Owner does not dispute the Petition's contentions that the claim preamble of independent claim 1 is described by Javanifard, which we find to be supported by a preponderance of the evidence.

[1.1] *selecting one of a first input node supplied with a first power supply voltage and a second input node supplied with a second power supply voltage that is higher than the first power supply voltage;*

The Petition asserts that Javanifard discloses circuitry in its Figure 2 which meets the claim limitation [1.1]. Pet. 66–69 (citing Ex. 1003 ¶¶ 213–220). Specifically, Petitioner points to the circuitry depicted in Figure 2 of

Javanifard as demonstrating “selecting from a first input node supplied with a first power supply voltage (e.g., VCC)” and “a second input node supplied with a second power supply voltage (e.g., VPP), where VPP (e.g., VPP = 5 volts) is higher than VCC (e.g., VCC = 3.3 volts).” Pet. 68 (citing Ex. 1006, 6:61–64, 7:15–17, 8:24–29). Figure 2, as annotated in the Petition, is reproduced below:



Petitioner-annotated Figure 2 shows a switch for selecting a first power supply Vcc or a second power supply Vpp (see switch on left circled in red)¹⁴ to produce an output supply voltage. Petitioner states that the switch is “controlled by control signals provided by a selection circuit (e.g.,

¹⁴ V_{cc} and V_{pp}, Vcc and Vpp, and VCC and VPP, are used interchangeably.

selection circuit 290 with voltage detect circuits 230 and 231).” Pet. 69. The supply voltage 294 is circled in red on the right.¹⁵ Figure 2 also produces supply voltages 260 and 262 as shown to the right of the figure.

Patent Owner does not dispute the Petition’s contention that limitation [1.1] of independent claim 1 is described by Javanifard, which we find to be supported by a preponderance of the evidence.

[1.2.1] *coupling a selected one of the first and second input nodes to booster circuitry comprising a plurality of booster stages to provide an output voltage,*

To meet the recited limitation [1.2.1] in the claim, the Petition asserts it would have been obvious to combine the switch¹⁶ and power supplies V_{cc} and V_{pp} shown in Figure 2 with the charge pumps shown in Figures 1 and 3 of Javanifard. Pet. 62–65, 69–70, 73 (citing Ex. 1003 ¶¶ 221–225). The Petition provides a composite drawing made by combining Javanifard’s Figure 2 (for the two power supplies) and Figure 1 (for the booster stages), which Petitioner refers to as “Example C.” *Id.* The composite, annotated in red by Petitioner, is reproduced below:

¹⁵ “The output of the V_{pp} detectors is provided to circuitry 290 to select the appropriate erase and programming algorithms for the various V_{pp} levels. These algorithms may vary depending upon V_{pp} and V_{cc}. Circuitry 290 controls the appropriate switches (e.g. switch 274) in accordance with the erase and programming algorithms.” Ex. 1006, 7:32–38.

¹⁶ Dr. Jacob testifies that “Javanifard however cannot satisfy all of the ’701 claim limitations by itself, which seems to be the main reason for including the switch in the way that Dr. Stiegler does.” Ex. 2003 ¶ 41.

*selecting one of a first input
node...and a second input node*

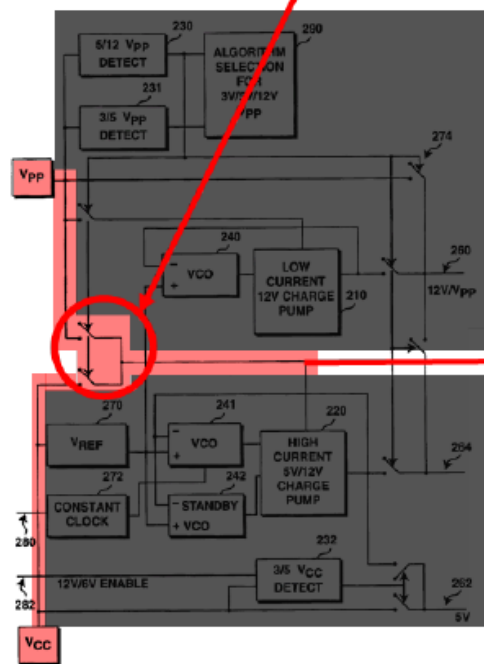


Figure 2

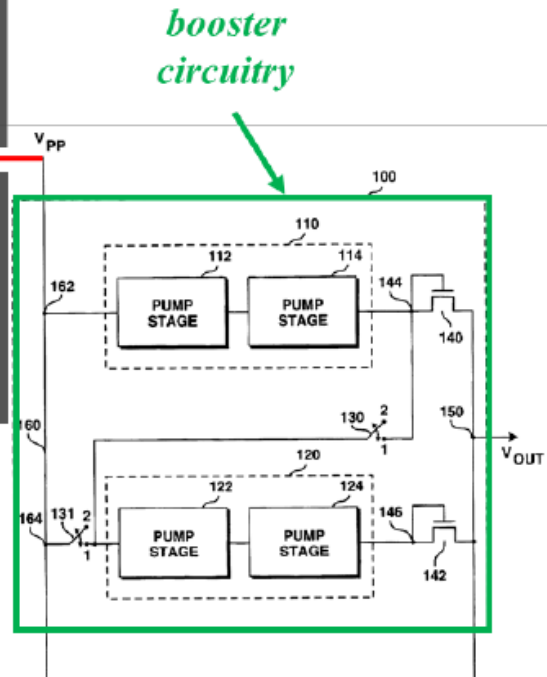


Figure 1

Example C shows the combination of Javanifard's Figures 2 (on the left) and 1 (on the right); the power supplies of Figure 2 are shown as coupled to the variable stage booster circuitry of Figure 1.

Figure 2 shows circuitry comprising two power supplies. The circuitry 290, and elements 230 and 231, controlling the switches, is eliminated. Vpp is at one node and Vcc is at the other node. The switch is asserted to select between power supplies Vcc and Vpp, but the annotated Example C only shows Vpp providing voltage to the variable charge pump. The variable charge pump of Figure 1, comprising fixed stage charge pumps 110 and 120

(Ex. 1006, 2:42–52) is combined with the switch and power supplies of Figure 2. The Petition labels Figure 1 as the “booster circuitry,” i.e., the circuitry that boosts the voltage provided by the power supplies. *See* Ex. 1003 ¶ 36. *See also* Pet. 73 (labeling the pump stages 112, 114, 122, 124 in Javanifard’s Figure 1 as “booster stages”).

In Petitioner’s proposed combination of Javanifard’s Figure 2 and Figures 1 or 3, the control circuitry of Figure 2 is omitted (e.g., elements 270, 241). *See* Ex. 2003 ¶¶ 139–140.

Example D (not reproduced here) is a composite drawing which depicts the booster stage circuitry illustrated in Javanifard’s Figure 3 instead of Figure 1, combined with the two power supplies of Figure 2. Pet. 72.

The Petition asserts that, in the combinations depicted in Examples C and D, “one of a first input node supplied with a first (lower) power supply voltage and a second input node supplied with a second (higher) power supply voltage is selected, and provided to a booster circuitry.” Pet. 70. In other words, one of Vcc or Vpp is asserted in the Petition to be selectable for supply to the single variable charge pump. The combined embodiments have only one voltage output in contrast to Figure 2 which has three output voltages in its unmodified form.

Petitioner explains that the figures “are simplified for illustration purposes, and it would have been obvious to a POSITA to implement additional well-known circuits (e.g., voltage detection circuit, voltage selection circuit providing control signals to selection switches, clock signals to drive the charge pumps) according to the design needs.” *Id.*

The Petition asserts:

A POSITA would have been motivated to apply Embodiment 2’s [Figure 2] teachings of selection from multiple power

sources to the variable stage charge pump as taught in Embodiments 1 or 3 [Figures 1 or 3], by selecting and supplying the selected power supply source (as taught in Embodiment 2) to the input of the variable stage charge pump, to produce the obvious, beneficial, and predictable results of a multi-power source variable stage charge pump system.

Pet. 63–64.

To support this contention, the Petition points to the disclosure in Javanifard of one of its objects as providing “a given output level for different charge pump power supply input levels.” Ex. 1006, 2:21–23 (cited at Pet. 64). That is, Petitioner’s reason to combine circuitry of the embodiments is to use the two power sources to achieve a “given” supply voltage, i.e., the same voltage supply level using different input power supplies.

The Petition further asserts that “a POSITA would have been motivated to apply Javanifard teachings of an input power supply selector for selecting from input nodes supplied with different power supply voltages” in Javanifard’s variable stage charge pump system to “have the benefit of providing a charge pump that can ‘**accommodate a given output level for different charge pump power supply input levels**’, e.g., for a device supplied with multiple power sources using two source lines” (e.g., Vcc and Vpp). Pet. 69–70 (citing Ex. 1006, 6:44–46¹⁷).

Patent Owner, in response, contends that Javanifard’s Figure 2 depicts a sophisticated system consisting of detection circuitry, algorithm selection,

¹⁷ “[P]ower for the flash memory device is provided by two sources. These sources include a Vcc line and a Vpp line. The Vcc line is the primary power source for the flash device. The supplemental voltage provided by supply line, Vpp, is typically needed only when writing or erasing the memory because of the higher voltages needed during those operations.”

and two distinct variable-stage charge pumps that generate multiple output voltages with varying current requirements. PO Resp. 41 (citing Ex. 1006, 7:11–20; 7:27–32). The charge pumps, Patent Owner explains, are designed to provide 5V, 9V, and 12V outputs based on fluctuations in V_{pp} and the operational mode of the flash memory, such as read, program, or erase modes. *Id.* According to Patent Owner, the system can supply three different output voltages at two current levels (“low current” or “high current”), accommodating any combination of V_{cc} (either 3.3V or 5V) and V_{pp} (3.3V, 5V, or 12V), with voltage detection accomplished through level detectors (230, 231, and 232). *Id.* (citing Ex. 1006, 7:23–24, 7:27–32, 7:35–36, 7:62–65). These detectors, Patent Owner asserts, identify the voltage levels of V_{pp} and V_{cc}, which influence the algorithms that control the system’s operation. *Id.* The charge pumps are reconfigured to adjust to the detected voltage levels and operational modes. *Id.* (citing Ex. 1006, 7:11–20, 7:23–24, 7:27–32, 7:35–36, 7:62–65, Fig. 2; Ex. 2003 ¶¶ 120–126).

Figure 2 of Javanifard depicts low current 12V charge pump 210 and high current 5V/12V charge pump 220. The figure does not show the structure of these charge pumps, but Patent Owner asserts that one of ordinary skill in the art would have understood that “variable-stage charge pumps 210 and 220 of Figure 2 would be implemented using the structures of Javanifard’s Figure 1 and/or Figure 3, as that is the clear implication of the Javanifard reference itself.” PO Resp. 42 (citing Ex. 2003 ¶ 129 (Dr. Jacob explains that Figure 2 of Javanifard identifies 210 and 220 as variable stage charge pumps and Figures 1 and 3 are variable stage charge pumps)).

Despite this straightforward understanding, Patent Owner contends that the Petition, instead, “proposes removing nearly all of the functionality

of Javanifard's Figure 2, and replacing that functionality with a single variable-stage charge pump according to Javanifard's Figure 1 or Figure 3." PO Resp. 42 (citing Ex. 2003 ¶¶ 133–140). Patent Owner contends that there is no apparent reason why this modification has been proposed when Javanifard "clearly intended . . . to leave the functionality of Figure 2 in place, and simply implement the variable-stage charge pumps 210 and 220 using Javanifard's teachings from Figure 1 and/or Figure 3." *Id.*

Patent Owner argues that the embodiment illustrated in Figure 2 as power supply circuitry for flash memory must be "capable of providing a variety of different output voltages at different current requirements according to a variety of different operating modes, all while accommodating variation in both V_{cc} and V_{pp} input voltage levels." PO Resp. 44–45. Patent Owner contends this "flexibility is important '[t]o maximize the utility of a flash memory system.'" PO Resp. 45 (citing Ex. 1006, 6:61–64, 6:12–17). Patent Owner argues that this "level of flexibility" is "important" and "mandatory." *Id.* (citing Ex. 1006, 6:61–64, 6:12–17, 6:56–60 ("To maximize the utility of a flash memory system . . . the variable stage charge pump must be able to generate approximately 5 volts, 9 volts, and 12 volts from either a 3.3 volt or 5 volt power supply.")). Yet, Patent Owner contends that the "proposed combination would gut these core features and benefits of Javanifard's Figure 2 embodiment." *Id.* at 46 (citing Ex. 2003 ¶¶ 138–140). Patent Owner also argues that the proposed substitution would defeat the purpose of Javanifard's embodiment exemplified in Figure 2 which is to provide three levels of voltage, not a single level as proposed. *Id.*

Patent Owner further argues that the Petition's reason to combine Figure 2 with Figures 1 and 3 is to provide the same output voltage level.

PO Resp. 46. Patent Owner asserts that the Petition “never provides any allegation that in its proposed combination, the output voltage would be configured to vary at all, much less to provide three separate output levels from two different input voltages, as Javanifard teaches its system ‘must be able to’ do.” PO Resp. 46 (citing Ex. 1006, 6:56–60).

Patent Owner argues that “the Petition fails to either recognize or acknowledge that Javanifard already accommodates a given output level for different charge pump power supply input levels.” PO Resp. 48 (citing Ex. 2003 ¶ 137) (emphasis omitted), 49 (“Javanifard’s Figure 2 is able to choose between any one of ‘a 5 volt, 9 volt, or 12 volt level’ output ‘from either a 3.3 volt or 5 volt power supply.’ Ex. 1006 at 6:56–64.” Therefore, “Javanifard’s system is clearly able to maintain ‘a given output level’ (e.g., 9 volts) ‘for different charge pump power supply input levels’ (e.g., 3.3 or 5 volt power supplies).”). Patent Owner asserts the Petition “alleges no problem in Javanifard that would be resolved by the Petition’s proposed modification.” *Id.*

Relying on the testimony of Dr. Jacob, Patent Owner argues that the Petition proposes to use the switch differently than how Javanifard uses it with no motivation to make the change. *Id.* at 51 (citing Ex. 2003 ¶¶ 132, 120–121).

We address these arguments below, as well as the additional arguments made by Petitioner.

2. *Reasons to combine*

Ground 2 is based on what would have been obvious to one of ordinary skill in the art, not on what Javanifard “clearly intended” or expressly described in its disclosure. PO Resp. 44. Thus, even were it true

that the most logical interpretation of Javanifard's Figure 2 is that each charge pump 210 and 220 was meant to be a variable charge pump of Figures 1 and 3,¹⁸ this finding is not dispositive. *Id.* The issue is whether one of ordinary skill in the art would have had reason to make the proposed combination.

In making an obviousness determination, "it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does." *KSR*, 550 U.S. at 418. However, as explained below and consistent with Patent Owner's arguments, Petitioner does not provide a sufficient reason for combining Figure 2 with Figures 1 or 3. *See* Pet. 63–65, 69–70.

Specifically, where Figure 2 shows two different charge pumps, one of low current and the other of high current, Petitioner has not provided an adequate reason to eliminate these two variable charge pumps and replace them with a single variable charge pump as illustrated in Figures 1 and 3. For example, Petitioner has not asserted equivalency between the structures that would have led a POSITA to replace one with the other. *See Wm. Wrigley Jr. Co. v. Cadbury Adams USA LLC*, 683 F.3d 1356, 1364 (Fed. Cir. 2012) ("strong case of obviousness based on the prior art references of record" because the claim "recites a combination of elements that were all known in the prior art, and all that was required to obtain that combination was to substitute one well-known . . . agent for another"). Indeed, as

¹⁸ Javanifard, in fact, describes the variable charge pumps 210, in one embodiment, as "configured to have 18 parallel-coupled sets of stages, each set including 3 serially coupled stages during the program, verify, and erase operational modes." Ex. 1006, 8:24–30. Charge pump 220 can also be in the 18/3 configuration. *Id.* at 8:39–40.

indicated by Patent Owner, replacing the two charge pumps in Figure 2 with the charge pump of Figures 1 or 3 results in a circuit with only one output supply voltage, rather than three supply outputs, and therefore has not been demonstrated by Petitioner to be equivalent to the circuit in Figure 2 and its application for flash memory. PO Resp. 44–46.

Petitioner challenges Patent Owner’s contention that Javanifard “impose[s] a mandatory intended purpose to FIG. 2 including multiple variable stage charge pumps.” Pet. Reply 25–26. This argument is not persuasive. Regardless of whether Javanifard characterized the two power supplies and ability to generate three different output voltages as mandatory, Javanifard’s Figure 2 shows exactly this configuration and capability. *See* PO Resp. 45–46; Ex. 1006, 6:61–64, 7:11–19. Petitioner’s argument is therefore not factually supported by Javanifard’s disclosure.

Patent Owner contends that the Petition “alleges no problem in Javanifard that would be resolved by the Petition’s proposed modification, and the purported goal of ‘accommodat[ing] a given output level for different charge pump power supply input levels’ therefore cannot motivate the Petition’s complete rearchitecting of Javanifard’s Figure 2.” PO Resp. 49 (citing *In re Schweickert*, 676 F. App’x 988, 995–96 (Fed. Cir. 2017) (finding no motivation to pursue a modification where the “record describes no problem in [the prior art] that would be resolved by the [proposed modification]”). Thus, Patent Owner contends that because the Petition does not provide “any coherent motivation to pursue” the proposed modification of Javanifard, it “is strongly suggestive of improper hindsight reasoning.” PO Resp. 54.

Initially, we do not agree that, to establish obviousness, the proposed modification must solve a problem associated with Javanifard’s Figure 2 or

improve upon it. The only requirement under 35 U.S.C. § 103(a) to establish obviousness is a “reason” to combine the prior art teachings. *KSR*, 550 U.S. at 418. The disclosure of a preferred combination of elements does not negate the obviousness of other combinations that can accomplish the same goal, even if inferior. The “case law is clear. It’s not necessary to show that a combination is ‘the best option, only that it be a suitable option.’” *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021) (quoting *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1197–98 (Fed. Cir. 2014)). Moreover, “[u]nder the correct [obviousness] analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.” *KSR*, 550 U.S. at 420. The rationale to combine does not have to come from Javanifard.

However, when we closely examine the Petition’s reasons to modify Javanifard’s Figures 1 and 3 with the teachings associated with Javanifard’s Figure 2, we find the reasoning factually deficient. As indicated by Patent Owner, Figure 2 comprises two variable charge pumps. Ex. 1006, 6:61–66; 7:21–22. Petitioner has not articulated a reason with rationale underpinnings which would have prompted a POSITA to substitute these two charge pumps with the single charge pump of Figures 1 or 3. The proposed combination simply takes two variable charge pumps out, and then swaps one variable charge pump in, which seems to put back what has been taken out.

Dr. Stiegler’s testimony is that it would been obvious to combine Figure 2 with Figures 1 or 3 to satisfy Javanifard’s stated objective “to provide a charge pump that can accommodate a given output level for different charge pump power supply input levels.” Ex. 1006, 2:22–24 (cited Ex. 1003 ¶ 207). However, as explained by Dr. Jacob, this capability is

already possessed by Javanifard's Figure 2 embodiment (*see* Ex. 2003 ¶¶ 136, 141) which is consistent with one of Javanifard's stated objectives (Ex. 1006, 2:22–24). Consistently, Figure 2 represents the only embodiment which employs different charge pump power supply input levels. Dr. Stiegler also recognizes that this objective is met by the embodiment of Figure 2:

Javanifard explicitly provides motivations to apply its teaching of selection from multiple power sources of Embodiment 2 to the variable stage charge pump of Embodiments 1 or 3, by providing the selected power supply to the variable stage charge pump. For example, one of Javanifard's objects is to "provide a charge pump that can accommodate a given output level for **different charge pump power supply input levels.**" EX1006, Javanifard, 2:21–23. It was well-known that often different charge pump power supply input levels are provided by different power supply source lines. *See, e.g.*, EX1006, Javanifard, 6:45–46 and EX1005, Zhang, Abstract, FIG. 4. As such, it would have been obvious to apply Embodiment 2's teaching of selection from multiple power sources to the variable stage charge pump, to achieve Javanifard's object to "accommodate a given output level for different charge pump power supply input levels." EX1006, Javanifard, 2:21–23.

Ex. 1003 ¶ 207.

Even aside from the fact that Figure 2 already possesses the capability asserted by Petitioner as the motivation to combine, the Petition's reasoning lacks sufficient factual basis as to why the skilled worker would have eliminated the switch circuitry in Figure 2 (e.g., elements 274, 290, 230, 231) and variable charge pumps 210 and 220 and replaced them with the single variable charge pump of Figures 1 and 2. Dr. Stiegler's testimony that the single-pump with two power supplies can achieve the given voltage output as the configuration in Figure 2 is not a reason to make this modification. Ex. 2003 ¶ 216.

Dr. Jacob specifically testified that the modification proposed by Dr. Stiegler includes eliminating, without explanation, “voltage-level tolerances, recognition of and response to operational mode, detection of and response to different voltage input levels, detection and selection of appropriate output voltage levels, etc.” Ex. 2003 ¶ 139. Petitioner has not rebutted Dr. Jacob’s testimony.

Petitioner appears to acknowledge a deficiency in the combination by explaining that Examples C and D “are simplified for illustration purposes, and it would have been obvious to a POSITA to implement additional well-known circuits (e.g., voltage detection circuit, voltage selection circuit providing control signals to selection switches, clock signals to drive the charge pumps) according to the design needs.” Pet. 70. Dr. Stiegler makes the same statement in his declaration, but fails to identify what is missing from the circuit and evidence that one of ordinary skill in the art would know how to implement what is missing. Ex. 1003 ¶ 217. The expert’s statement is conclusory. We do not accord weight to conclusory expert testimony. *See TQ Delta, LLC v. CISCO Sys., Inc.*, 942 F.3d 1352, 1359 n.5, 1360 (Fed. Cir. 2019); 37 C.F.R. §42.65(a),

Dr. Jacob, on the other hand, describes the specific control circuitry which has been eliminated from Javanifard’s Figure 2. Ex. 2003 ¶ 139. Dr. Jacob testifies that “Dr. Stiegler’s choice to eliminate all the mechanisms and control circuitry designed to perform the functions described above significantly changes the entire principle of operation of the Figure-2 embodiment.” *Id.* ¶ 140. Dr. Jacob further testifies that Dr. Stiegler “does not explain anywhere why such a significant modification to the Figure-2 embodiment would have been obvious to a person of ordinary skill” nor does he “explain why it would have been necessary.” *Id.*

In order to provide a sufficient rationale, Petitioner needs to provide a reason to replace the two variable charge pumps of Figure 2 with the single variable charge pump of Figures 1 and 3, and a reason to eliminate the control circuitry of Figure 2. Petitioner did not provide a reason for the latter in the Petition nor in Petitioner's Reply.

As to Patent Owner's contention (PO Resp. 46–47), citing *Schweickert*, that the proposed combination is deficient because it resolves no problem, it is true that the Federal Circuit in *Schweickert* did make such a statement. *Schweickert*, 675 Fed. App'x at 995. But the underlying reason the Federal Circuit reversed the Board was because the "Board's decision is deficient in another respect." *Id.* "[T]he Board has not explained why or how a skilled artisan would further configure or manipulate Birrell's RAM such that there would be multiple lockable buffers as claimed in the '272 Patent." *Id.* *Schweickert* found the Board's decision defective because the motivation to combine the references lacked support ("the record does not appear to substantiate" the Board's finding; "the record lacks support for this supposed motivation to introduce Cunniff's semaphore into Birrell's RAM"). The court summed up: "the Board has proffered no sufficient basis for why a skilled artisan would have readily applied Cunniff to Birrell." *Id.* The reasoning in *Schweickert* applies here too because Petitioner's reasoning to combine the different embodiments of Javanifard is not supported by sufficient factual evidence.

In Petitioner's Reply, Petitioner contends that "Embodiments 1 and 3 each have the need of supplying their variable stage charge pump with 'different power supply source lines' (Pet. 64) (e.g., Vcc and Vpp)." Pet. Reply 20 (emphasis omitted). Petitioner asserts that Embodiment 2's power source section provides "a suitable option for addressing this need" and it

was within the level of ordinary skill in the art to implement it. *Id.* Petitioner concludes that “[n]othing more is required to show a motivation to combine.” *Id.*

Petitioner does not identify why Embodiments 1 and 3, represented by Javanifard’s Figures 1 and 3, “need” the multiple power supplies of Embodiment 2, represented by Javanifard’s Figure 2. Pet. Reply. 20. Each of Embodiment 1 and 3 already have a power source supply; Petitioner does not identify a reason for replacing it with the power source selection of Embodiment 2. Page 64 of the Petition, cited by Petitioner as support for the “need” argument, refers to the objective disclosed in Javanifard of a “given” output level for different power supply sources and that such configuration was “well-known,” but provides no reason why Embodiments 1 and 3 “need” to select from multiple power sources. Pet. 64. Petitioner asserts the reason is to achieve the same voltage output by the ability to select from multiple sources, but this objective was already satisfied by Embodiment 2. *Id.* The contention that nothing more is required than the asserted “need” might be true if Petitioner had established a “need” for selecting multiple power sources in Embodiments 1 and 3, but a “need” was not identified and the argument fails to establish the obviousness of combining the embodiments. No expert testimony was cited by Petitioner to provide evidence of the asserted “need.”

Petitioner asserts that Patent Owner “do[es] not dispute that Embodiments 1 and 3 each have the need of supplying their variable stage charge pump with ‘different power supply source lines.’” Pet. Reply 23. This statement fails to acknowledge that the reason Patent Owner does not dispute the asserted “need” is because the Petition did not make this assertion; page 64 of the Petition, identified as support for the argument,

makes the same contentions about “given” output using multiple power sources that Patent Owner responded to in the Patent Owner Response.

Petitioner disputes that ““extensive modifications”” have been made to Figure 2. Pet. Reply 24 (citing PO Resp. 39). Petitioner claims that the combination “simply modifies Embodiments 1 and 3 (primary embodiments) by applying the power supply source selection feature of Embodiment 2 (secondary embodiment) to the input of the charge pump.” *Id.* Petitioner further asserts that the alleged extensive modifications would only be necessary if a “POSITA is required to start from bodily incorporating [the] *entire* FIG. 2 in the combination.” *Id.*

Petitioner has not provided evidence or expert testimony to support these contentions. The modifications proposed in the Petition omit the control circuitry of Figure 2. Pet. Reply 21 n.2 (in reference to Examples C and D (Pet. 71–72), the greyed-out areas include control circuitry: “These illustrations include greyed-out circuits not used in the combination. In analysis below, the greyed-out circuits are removed from the figures to avoid any confusion and making the combined figures easier to read.”). Petitioner provides no explanation as to why eliminating all the control circuitry from Figure 2 is not “extensive.”

Petitioner makes a “bodily incorporation” argument, asserting that extensive modifications would only be necessary if the entire Figure 2 were incorporated into the combination. Petitioner’s argument hinges on the position that selectively incorporating the multiple power supplies from Figure 2 into Figure 1 achieves the claimed configuration without requiring extensive redesign or wholesale incorporation of Figure 2 into the combination.

This argument strays from Patent Owner’s objection. Patent Owner’s position is that Figure 2 is extensively modified by removing its control circuitry. By selectively focusing on using only the multiple power sources of Figure 2 in combination with Figure 1, Petitioner asserts no extensive modification to the combination is necessary, but fails to address the modifications to Figure 2. Moreover, Petitioner admitted that further modification to the combination of Figure 2 and Figures 1 or 3 is necessary:

Examples C and D “are simplified for illustration purposes, and it would have been obvious to a POSITA to implement additional well-known circuits (e.g., voltage detection circuit, voltage selection circuit providing control signals to selection switches, clock signals to drive the charge pumps) according to the design needs.”

Pet. 70.

Petitioner asserts that Patent Owner’s arguments “disregard [the] Petition’s combination of modifying the primary embodiments (Embodiments 1 and 3) with specific features of the secondary embodiment (power supply source selection of Embodiment 2).” Pet. Reply 23 (citing PO Resp. 38–50). By the phrase “primary reference/embodiments,”¹⁹ Petitioner means that Figures 1 and 3 are “modified with specific features of FIG. 2.” Pet. Reply 27. The terms “primary” and “secondary” were not used in the Petition. *See* PO Sur-reply 27–28.

¹⁹ *See also* Pet. Reply 24 (“[The] Petition’s combination simply modifies Embodiments 1 and 3 (primary embodiments) by applying the power supply source selection feature of Embodiment 2 (secondary embodiment) to the input of the charge pump. [The] Petition’s combination does not modify FIG. 2.”). *See also* Pet. Reply 26–27, referring to Embodiments 1 and 3, as represented by Figure 1 and 3, as the “primary reference/embodiments.”

Nonetheless, these designations are inaccurate. As explained above, Figure 2 incorporates the circuitry of Figure 1 or Figure 3 (or both), and is not a separate embodiment. *See, e.g.*, Ex. 1006, 8:24–30, describing charge pump 210 of Figure 2 as having an 18/3 pump stage configuration, the same structure suggested in Figure 3. Thus, Figure 2 is not a secondary embodiment. What Petitioner seeks to do is to rewire Figure 2 to remove most of the circuitry, including circuitry that would be contributed by Figures 1 and 3, leaving merely a switch, which is then added back in Figure 1 or Figure 3.

In the Petition, Petitioner stated that a person of ordinary skill in the art:

would have been motivated to apply Embodiment 2's teachings of selection from multiple power sources to the variable stage charge pump as taught in Embodiments 1 or 3, by selecting and supplying the selected power supply source (as taught in Embodiment 2) to the input of the variable stage charge pump, to produce the obvious, beneficial, and predictable results of a multi-power-source variable stage charge pump system.

Pet. 63–64. The Petition's patentability challenge applied the multiple power sources of Embodiment 2 to Embodiments 1 and 3, each having only one power supply. An alternative way of stating it is that Embodiments 1 and 3 are modified by replacing their single power supply with the ability to select from at least two variable charge pumps. Whether stated in terms of replacing the variable charge pumps in Embodiment 2 with the single charge pump of Embodiments 1 and 3, or replacing the single power supply in Figure 1 with the multiple power supplies of Embodiment 2, establishing obviousness requires a reason to make either of these modifications.

Patent Owner addressed the deficiency in the reasons to combine the embodiments. PO Resp. 40–55. Petitioner does not identify what argument

by Patent Owner disregards the modification of Embodiments 1 and 3 with the teachings of Embodiment 2. Pet. Reply 23. Because Petitioner cites a broad range of pages from 38 to 50 of Patent Owner's Response, without pinpointing or describing the specific argument made by Patent Owner, Patent Owner is unable to respond to this generic statement by Petitioner. We also are unable to do so.

Patent Owner contends that the modifications to Javanifard's Figure 2 embodiment would render it inoperable because of the functionality removed. Citing paragraph 112 of the Jacob declaration, Patent Owner argues that the combination is conclusory and "makes no sense" to the ordinarily skilled worker. PO Resp. 39. Petitioner argues that Patent Owner's reliance on *Schweickert* and *Plas-Pak Indus., Inc. v. Sulzer Mixpac AG*, 600 F. App'x 755, 760 (Fed. Cir. 2015), "is misplaced, because the inoperable test described therein is directed at the primary reference being modified with the special features of the secondary reference," but Patent Owner's argument is directed at Figure 2, the second reference. Pet. Reply 26–27.

We do not agree that the "inoperable" test is so narrowly construed. See PO Resp. 28. As explained in *Plas-Pak*:

combinations that change the "basic principles under which the [prior art] was designed to operate," *In re Ratti*, 46 CCPA 976, 270 F.2d 810, 813 (1959), or that render the prior art "inoperable for its intended purpose," *In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984), may fail to support a conclusion of obviousness.

Plas-Pak, 600 F. App'x at 758. Thus *Plas-Pak* has a general statement about the operability of "combinations," without regard to the so-called primary and second references.

Paragraph 112 of the Jacob declaration, cited by Patent Owner, makes the following contentions:

In his Grounds-2 analysis, Dr. Stiegler misrepresents the behavior of Javanifard's main working embodiment, misrepresents the purpose of Javanifard's design, and misrepresents circuit design in general. The result is a conclusory combination that would have made no sense to a person of ordinary skill.

Dr. Jacob explains the misrepresentation in subsequent paragraphs 113–126.

Dr. Jacob's testimony is un rebutted by Petitioner.

Petitioner further asserts that the "Petition's combination provide[s] various improvements to Javanifard's Figure-2 embodiment." Pet. Reply 29. Three improvements/advantages are disclosed. *Id.* Notwithstanding the fact that these asserted improvements were not identified in the Petition, Petitioner has not provided sufficient evidence that the improvements apply to Figure 2 of Javanifard or its combination with the embodiments of Figures 1 and 3.

Petitioner asserts that advantage (1) provides "area savings/reduced cost/reduced complexity by using a single variable stage charge pump instead of two charge pumps." Pet. Reply 29. The only relevant citation is to Exhibit 1027, pages 3, 22, 43.²⁰ Other than citing these page numbers, Petitioner has not given any meaningful analysis to these disclosures. For example, page 3 shows diagrams of power solutions, page 22 refers to "a tradeoff between efficiency and solution size needs to be made" and to a space saving package, and page 43 describes power switches. Petitioner does not identify the specific disclosure on these pages that it considers relevant

²⁰ Exhibit 1027 is new evidence that is not responsive to Patent Owner's Response or to the Institution Decision.

to advantage (1) nor does Petitioner provide evidence that the advantages allegedly disclosed in Exhibit 1027 are applicable to Javanifard's Figure 2 or the proposed combination.

Petitioner also asserts that the combination provides "(2) a broader range of applications." Pet. Reply 29. Petitioner cites Frulio (Ex. 1014) for this advantage, specifically citing column 1, lines 15–16: "Charge pumps are widely used in the integrated circuit industry in many applications such as power ICs, filters, memories, etc."

Each of Figures 1, 2, and 3 of Javanifard are or include charge pumps. Petitioner does not explain how the asserted broader range of applications applies to the proposed combination but not to the variable charge pumps of Figures 1, 2, and 3 of Javanifard prior to any modification.

For advantage "(3) flexibility for different design specifications," Petitioner refers to the following statements in Dr. Jacob's deposition:

- 17. Q. So is the -- dealing with trade-off between
- 18. overdesign and underdesign a general issue in circuit
- 19. design?
- 20. A. I would say that yeah, people do worry about
- 21. that. All designers want to come up with something
- 22. that's appropriate.

Ex. 1029, 58:17–22.

The context in which Dr. Jacob made this statement was in response to the question "What does 'overdesigning' mean," because the term "overdesigning" was used by Dr. Jacob in his declaration to characterize disclosure in the '701 patent. Ex. 1029, 55:16–25 ("The '701 patent (Hayashi) is concerned with the trade-off between overdesigning a charge pump and underdesigning the charge pump.").

Dr. Jacob explains that “overdesigning” in chip design refers to making components, like capacitors, larger or more robust than necessary to avoid potential failure due to unexpected voltage conditions. *Id.* In the case of a charge pump, he explains that this could involve using a thicker dielectric in the capacitor to prevent its breakdown, but this adaptation results in a larger, more expensive design. *Id.* Dr. Jacob states that the goal of the design is to make the charge pump as small and cost-effective as possible, while still ensuring it works across a range of potential operating voltages without failure. *Id.*

Petitioner does not point to any specific part of the expert’s deposition testimony that explains how the proposed combination of Embodiment 2 with Embodiments 1 and 3 of Javanifard provides “flexibility” that is not already characteristic of the unmodified designs. Dr. Jacob’s testimony is about the tradeoffs of choosing the capacitors used in charge pumps, which would be a consideration in designing any charge pump chip.

Dr. Stiegler’s testimony does not address Patent Owner’s concerns. Dr. Stiegler asserts that Javanifard “explicitly provides motivations to apply its teaching of selection from multiple power sources of Embodiment 2 [Figure 2] to the variable stage charge pump of Embodiments 1 or 3 [Figures 1 and 3], by providing the selected power supply to the variable stage charge pump.” Ex. 1003 ¶ 207. Dr. Stiegler merely repeats what is in the Petition about the obviousness of using different power supplies to achieve a given output level, and that such configuration was well-known; however, he fails to explain the reason why one of ordinary skill in the art would have used two power supplies to provide only one output supply voltage. Thus, his testimony is conclusory and unsupported. *See Xerox Corp. v. Bytemark, Inc.*,

IPR2022-00624, Paper 9 at 15 (PTAB Aug. 24, 2022) (precedential); 37 C.F.R. § 42.65(a).

Dr. Stiegler asserts that combining the different teachings of Javanifard would produce circuitry capable of providing a given output level, but fails to provide a sufficient reason that would have prompted a POSITA to replace the two booster circuits in Figure 2 with the one variable charge pump booster of Figures 1 and 3. *See, e.g.*, Ex. 1003 ¶¶ 227–231. For example, Dr. Stiegler explains how the charge pump of Figure 1 would be configured to accommodate a “given” voltage level using different charge pumps. *Id.* The reason Dr. Stiegler gives for making the combination is “to produce the obvious, beneficial, and predictable results of a multi-power-source variable stage charge pump system that supports multiple power sources, e.g., supporting a device provided by multiple power sources.” *Id.* ¶ 206. But, as explained above, this asserted benefit is already possessed by the circuitry of Figure 2.

In sum, Petitioner has not met the burden of establishing that one of ordinary skill in the art would have had reason to combine Figure 2 with Figures 1 and 3.

[1.2.2] *wherein selection of the first input node corresponds to a first number of booster stages and*

As evidence that one of ordinary skill in the art would select a “first input node correspond[ing] to a first number of booster stages,” the Petition cites Javanifard’s disclosure that an object of its invention “is to provide a charge pump that can accommodate a given output level for different charge pump power supply input levels.” Ex. 1006, 2:22–24 (cited at Pet. 75).

The Petition further cites Table 1 of Javanifard for describing the selection of “a lower charge pump power supply input level, such that selection of the first input node corresponds to a first number (a higher number, e.g., 4) of booster stages.” Pet. 75. Table 1 shows the four different possible combinations for switches 130 and 131 of Javanifard’s Figure 1. “The phrase ‘on’ when referring to switches 130 and 131 means that the switches provide a current path. The phrase ‘off’ when referring to switches 130 and 131 means that the switches are in an open-circuit state.” Ex. 1006, 3:8–11. “A first switch (130) controls whether the output of the first charge pump is provided as an input to the second charge pump. A second switch (131) is used to couple the input of the second charge pump to V_{pp},” which is the voltage output. *Id.* at 2:54–57. Each charge pump is shown in Figure 1 of Javanifard as having a specific number of “pump stages,” where each pump stage corresponds to the claimed “booster stage.”

Table 1, as annotated by Petitioner, is copied below:

TABLE 1			
Switch 130	Switch 131	Charge Pump 110	Charge Pump 120
OFF	OFF	ON	OFF
OFF	ON	ON	parallel-coupled to charge pump 110
ON	OFF	ON	series-coupled to charge pump 110
ON	ON	N/A	N/A

a second number of booster stages, the second number being less than first number

a first number of booster stages

Annotated Table 1 shows the four different position combinations of switches 130 and 131 and how the different positions (on or off) effect the coupling between the charge pumps. Ex. 1006, 3:19–22. Table 1, row 1 (labeled in red) shows selecting both switches 130 and 131 “OFF,” resulting in charge pump 110 “ON” and charge pump 120 “OFF.”

Table 1, row 3 (labeled in green), shows selecting switch 130 “ON” and switch “OFF,” resulting in coupling charge pumps 110 and 120 in series (third line, in green).

Charge pumps 110 and 120 each have 2 pump stages. Ex. 1006, Fig. 1.

Table 1, row 3 (labeled in green), “provides a first number (a higher number, e.g., 4) of serially connected booster stages to provide a higher voltage boost (e.g., by serially connecting charge pumps 110 and 120).” Pet. 75. Row 1 (labeled in red) of Table 1, in contrast, provides a lower number (e.g., 2) of serially connected booster stages by having only charge pump 110 in operation. *Id.* See Ex. 1003 ¶ 228.

Patent Owner does not challenge the Petition’s contention that this configuration meets claim limitation [1.2.2], which is supported by a preponderance of the evidence.

[1.2.3] *selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than first number; and*

To meet claim limitation [1.2.3], Petitioner provides evidence that the first row of Table 1 (reproduced above) “provides a second (lower, e.g., 2) number of serially connected booster stages to provide a lower voltage boost (by providing only charge pump 110 in operation and thereby having a lower number of serially connected booster stages)” than the third row of Table 1. Pet. 77. Dr. Stiegler testifies:

Connecting more stages in series provide a higher voltage boost compared to using a smaller number of stages in series, as each stage in the charge pump contributes to increasing the voltage

level, and the total voltage boost is the cumulative effect of all the stages.

Ex. 1003 ¶ 228.

The Petition asserts that “a POSITA would have used row 1 based on a design need for power saving mode, because it provides a lower current than row 2.” Pet. 78 (citing Ex. 1006, 3:39–42 (“This configuration [of row 1] might be used in a power saving mode if charge pump 100 is otherwise providing sufficient current and voltage output levels.”)).

Patent Owner does not challenge the Petition’s contention that this configuration meets claim limitation [1.2.3], which is supported by a preponderance of the evidence.

[1.3] *changing the booster circuitry from the first number of booster stages corresponding to selection of the first input node to the second number of booster stages when the second input node is selected.*

As discussed above under [1.2.2] and [1.2.3], in the combination of the Javanifard embodiments, selection of the first input node corresponds to selecting a first number of booster stages, and selection of the second input node corresponds to selecting a second number of booster stages. The selection of the second node (row 1 of Table 1) results in selecting less booster stages than the first node (row 3 of Table 1).

Javanifard further discloses that “control for the switches would be a function of the available power supply voltage, V_{pp} , and the desired variable stage charge pump output voltage.” Ex. 1006, 5:65–67 (cited at Pet. 79). Thus, Petitioner contends, “when the selection of the input node is changed to the higher power supply voltage, the booster circuitry is changed from the first number of booster stages (e.g., 4) to the second number of booster

stages (e.g., 2), by turning off switch 130.” Pet. 79–80. To illustrate this change in the booster/charge pump circuitry, Petitioner provides the following annotated Table 1:

TABLE 1

Switch 130	Switch 131	Charge Pump 110	Charge Pump 120	
OFF	OFF	ON	OFF	<i>a second number of booster stages, the second number being less than first number</i>
OFF	ON	ON	parallel-coupled to charge pump 110	
ON	OFF	ON	series-coupled to charge pump 110	<i>a first number of booster stages</i>
ON	ON	N/A	N/A	



Annotated Table 1 shows the four different position combinations of switches 130 and 131 and how the different positions (on or off) effect the coupling between the charge pumps. Ex. 1006, 3:19–22. Table 1 shows that, when switch 130 is turned off, the number of booster stages/pump stages changes from a first number to a second number which is less than the first number (the switching is shown by a red arrow pointing from row 3 to row 1).

Patent Owner does not challenge the Petition’s contention that this configuration meets claim limitation [1/3], which is supported by a preponderance of the evidence.

3. Summary

Based on the entire record, and for the reasons discussed above, Petitioner has failed to establish by a preponderance of the evidence that claim 1 is unpatentable under § 103(a) as obvious based on Javanifard.

4. *Claims 2–18*

Petitioner asserts that claims 2–9, which depend from claim 1, and claims 11–18, which depend from claim 10, are unpatentable under 35 U.S.C. § 103(a) as obvious based on Javanifard. Pet. 81–86.

Claim 10 has substantially the same limitations as claim 1, but the claim is directed to a semiconductor device. The Petition relies on essentially the same findings and reasons for finding claim 10 obvious based on Javanifard as for the obviousness of claim 1. Pet. 83–85. Accordingly, as for claim 1, Petitioner has failed to establish by a preponderance of the evidence that claim 10 is unpatentable under § 103(a) as obvious based on Javanifard.

All the dependent claims recite, or incorporate by dependency, the limitations of claims 1 and 10 which, as discussed above, are not described or suggested by the combination of Javanifard’s teachings as proposed in the Petition.

Because Petitioner has failed by a preponderance of the evidence to establish sufficient reason to combine the embodiments of Javanifard to meet all the limitation of claims 1 and 10, the unpatentability challenge to dependent claims 2–9 and 11–18, which depend on independent claims 1 and 10, and incorporate all their limitations, also fails.

F. *Obviousness challenge based on Zhang, Javanifard, and Kang*

Petitioner asserts that claims 9 and 18, which depend from claims 1 and 10, respectively, are unpatentable under 35 U.S.C. § 103(a) as obvious over Zhang, Javanifard, and Kang. Pet. 87–91.

Citing the statement in the Petition that the analysis for Ground 3 relies “on the analysis and evidence as provided for Ground 1 (Zhang and

Javanifard)” (Pet. 87), Patent Owner states that the theory presented in Ground 3 fails “at least the same reasons applicable” to Ground 1. PO Resp. 56.

We concur. The additional discussion of Kang does not make up for the deficiencies in the challenge based on Zhang and Javanifard. Pet. 87. For the reasons discussed above, Petitioner has failed to establish by a preponderance of the evidence that claims 9 and 18 are unpatentable over the combination of Zhang, Javanifard, and Kang.

G. Obviousness challenge based on Javanifard and Kang

Petitioner asserts that claims 9 and 18, which depend from claims 1 and 10, respectively, are unpatentable under 35 U.S.C. § 103(a) as obvious over Javanifard and Kang. Pet. 87–91.

Citing the statement in the Petition that the analysis for Ground 4 relies “on the analysis and evidence as provided for Ground 2 (Zhang and Javanifard)” (Pet. 87), Patent Owner states that the theory presented in Ground 3 fails “at least the same reasons applicable” to Ground 1. PO Resp. 56.

We concur. The additional discussion of Kang does not make up for the deficiencies in the challenge based on Javanifard. Pet. 87. For the reasons discussed above, Petitioner has failed to establish by a preponderance of the evidence that claims 9 and 18 are unpatentable over the combination of Javanifard and Kang.

V. CONCLUSION

Based on the evidence presented with the Petition, the evidence introduced during the trial, and the parties’ respective arguments, Petitioner

has not shown by a preponderance of the evidence that claims 1–18 of the '701 patent are unpatentable under § 103(a) as obvious over 1) Zhang and Javanifard, and 2) Javanifard, alone; and that claims 9 and 18 are unpatentable under § 103(a) as obvious over 3) Zhang, Javanifard, and Kang, or 4) Javanifard and Kang.

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/ Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1–18	103(a)	Zhang, Javanifard		1–18
1–18	103(a)	Javanifard		1–18
9, 18	103(a)	Zhang, Javanifard, Kang		9, 18
9, 18	103(a)	Javanifard, Kang		9, 18
Overall Outcome				1–18

VI. ORDER

Accordingly, it is

ORDERED that claims 1–18 of U.S. Patent 9,207,701 B2 are not determined to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2023-01230
Patent 9,207,701 B2

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